

Triathlon

Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

星期三, 七月 12, 2006

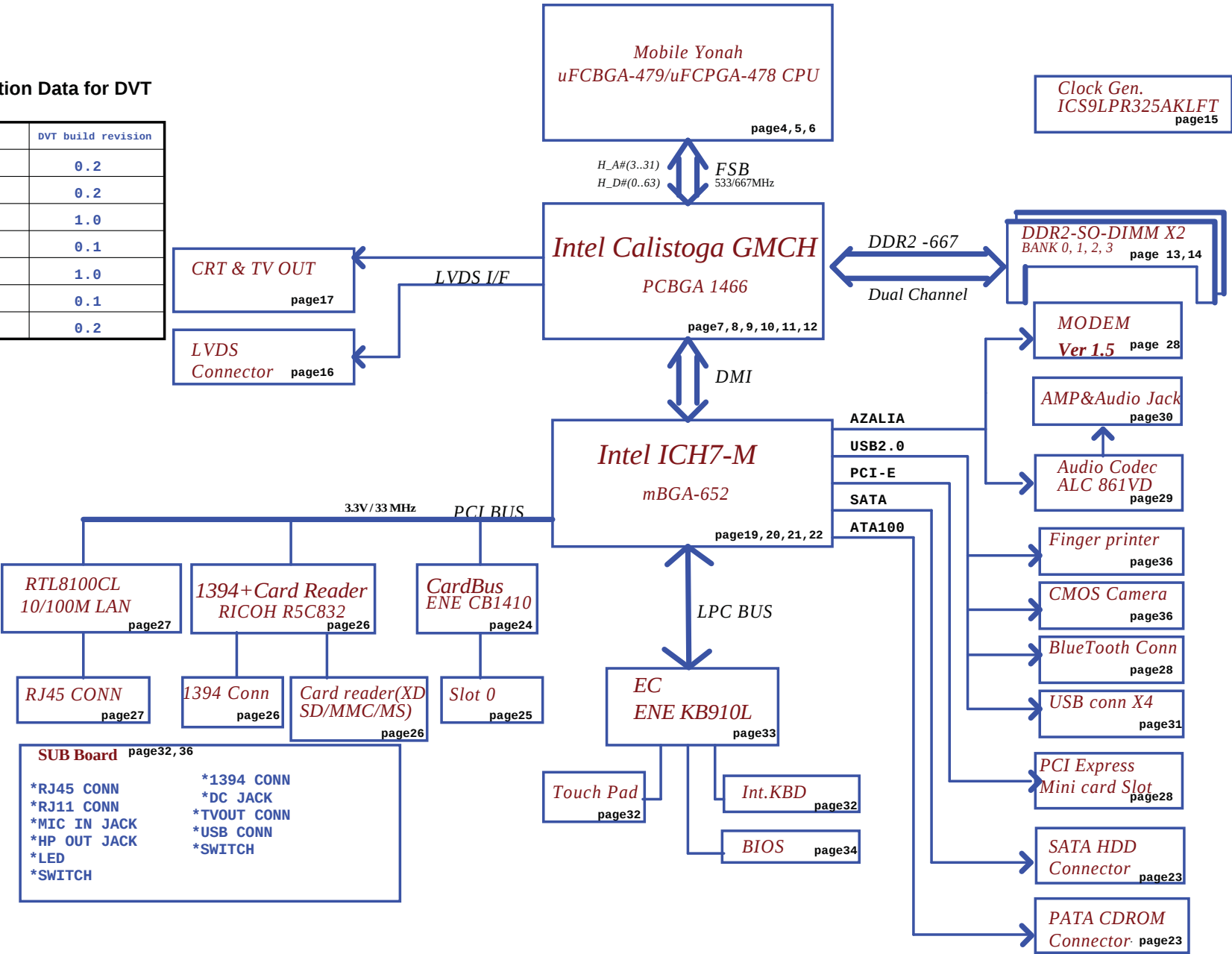
REV:0.3

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				Size	Document Number	Rev
				Custom	401429	B
Date:				Sheet 1 of 47		



HDL20 PCB panelization Data for DVT

PCB Function	PCB Number	DVT build revision
MB	LA3281P	0.2
Audio/USB	LS3251P	0.2
SW board	LS3102P	1.0
CRT board	LS3253P	0.1
TP board	LS3104P	1.0
FP Board	LS3255P	0.1
LED board	LS3256P	0.2



Voltage Rails

power plane	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
State				
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

0 MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H
LAN	AD17	3	PIRQF
CardBus	AD20	2	PIRQA

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	MB ID(H)	MB ID(L)
0		
1		
2		
3	HDL10	HDL00
* 4		HDL20
5	IDL12	HDL30
6		
7		

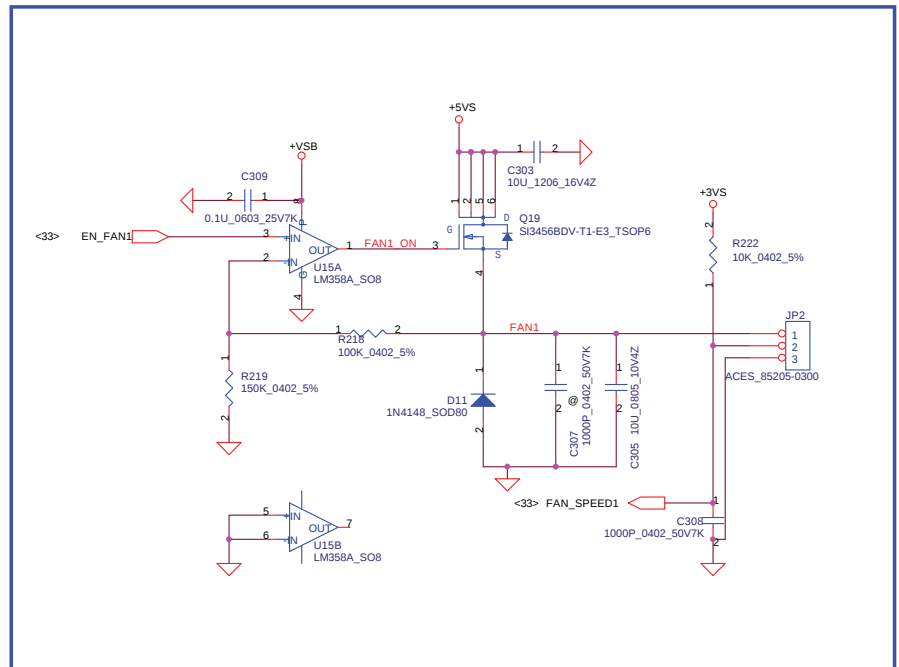
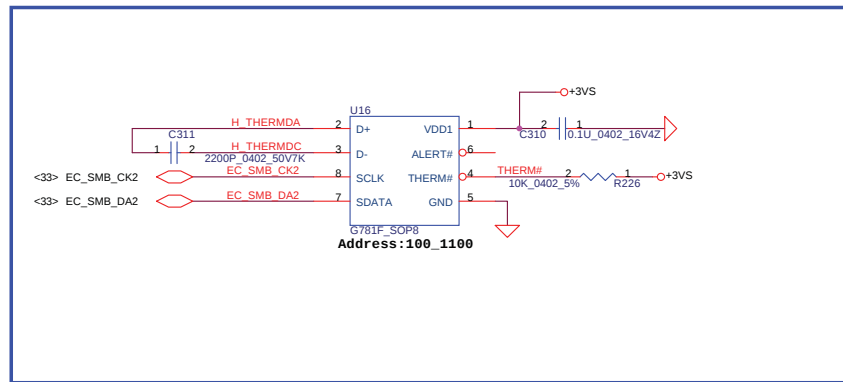
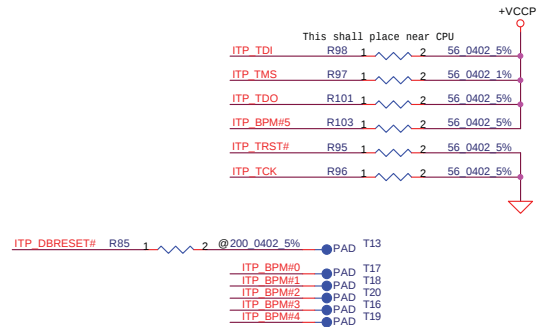
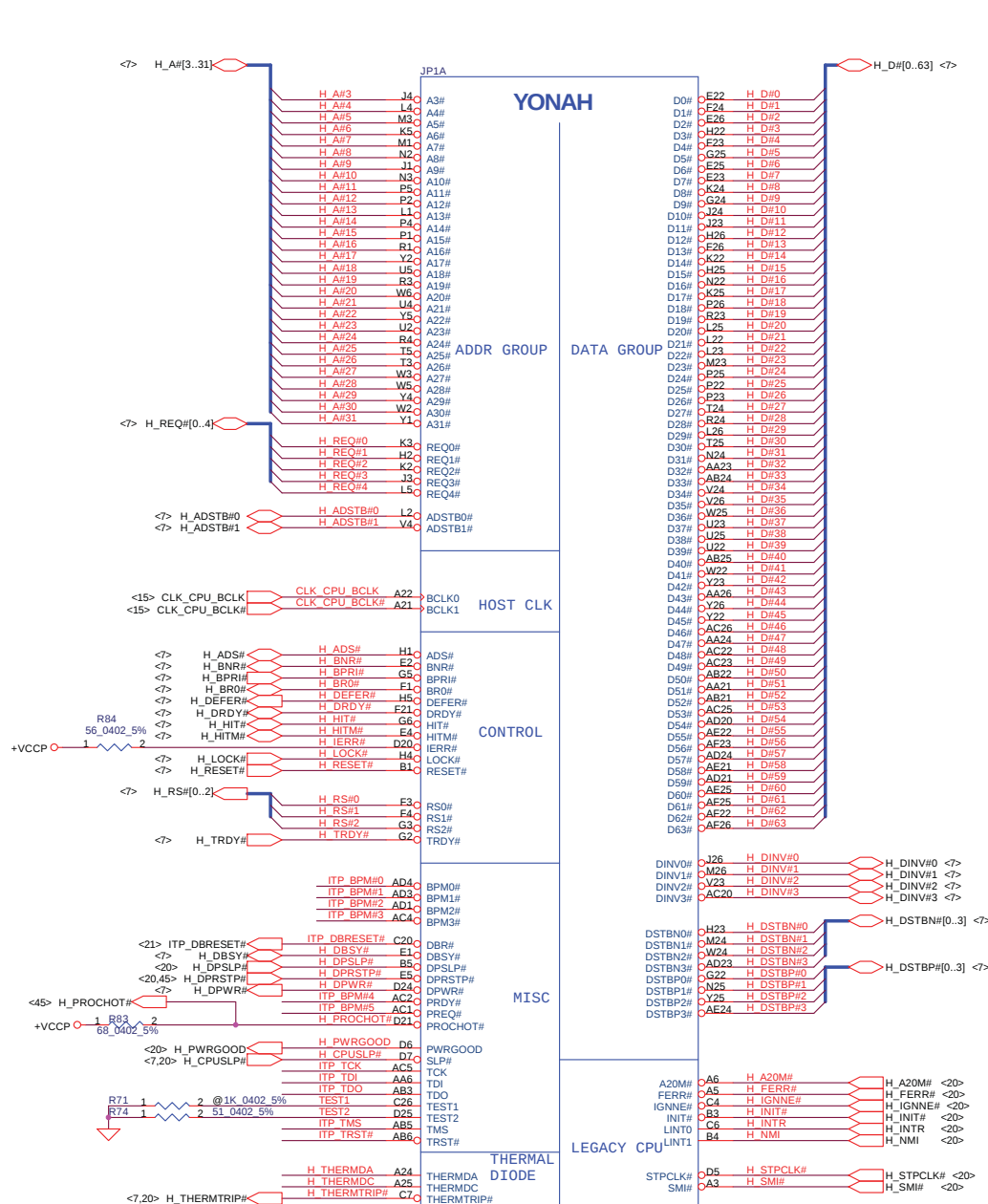
	MB ID
H	15"
L	14"

BOM Structure

MARK	FUNCTION
@	NC FOR ALL
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8100CL 10/100Mb LAN
UMA@	Internal 945GM
VGA@	External G7xM

USB PORT LIST

PORT	DEVICE
0	LEFT SIDE
1	BT(HDL00/10)
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	RIGHT SIDE
7	BT(HDL20)



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				Date	Rev B
				星期三, 七月 12, 2006	Sheet 4 of 47

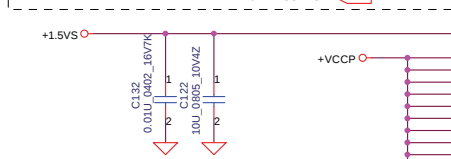
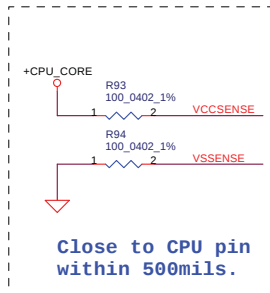
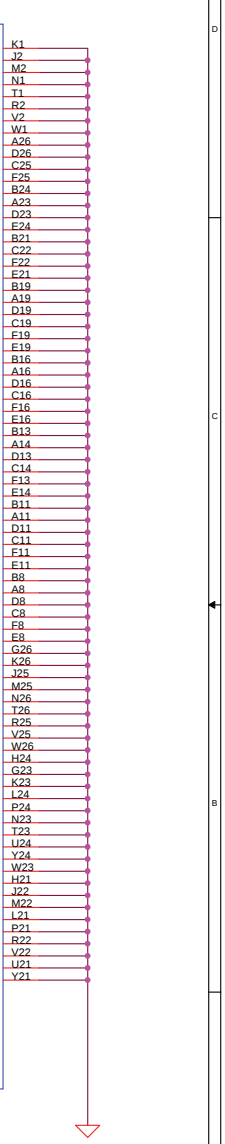
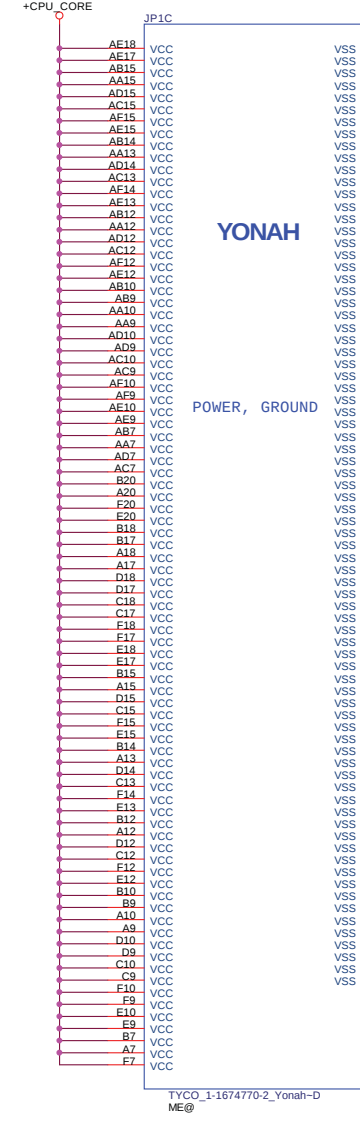
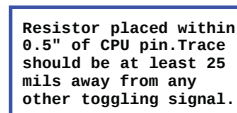
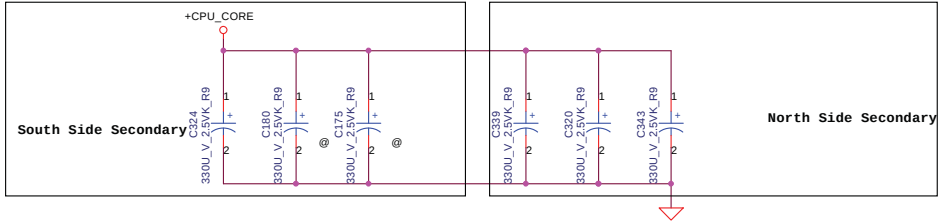
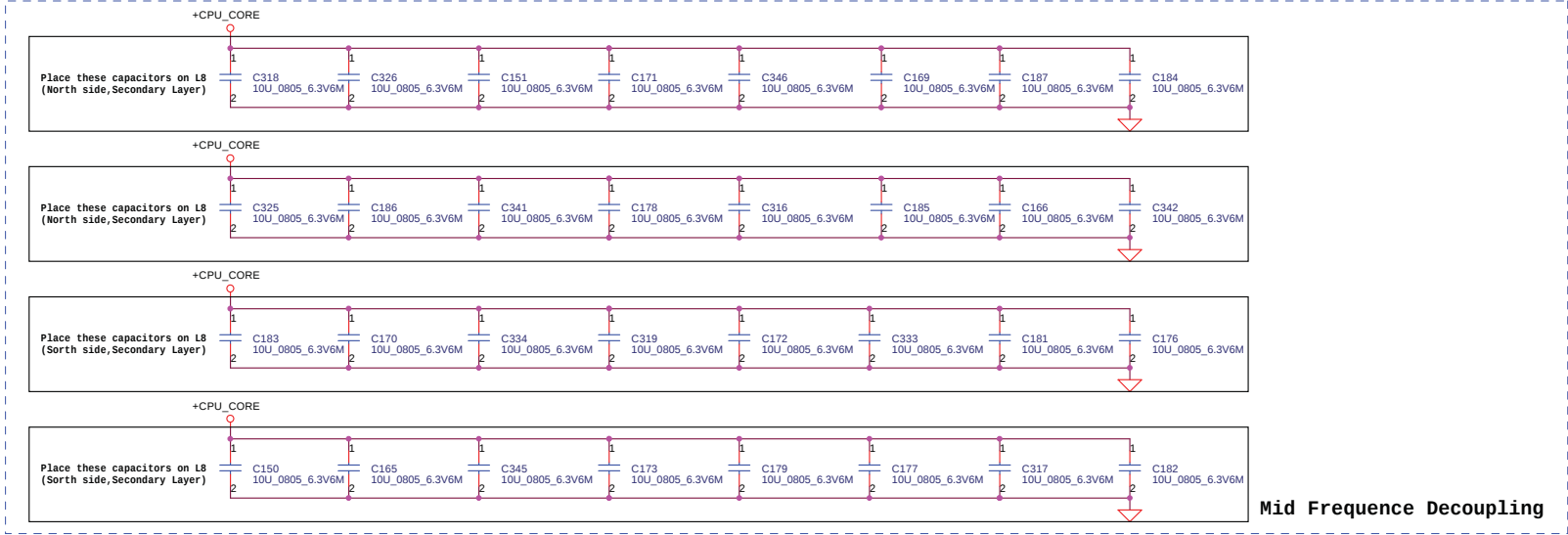


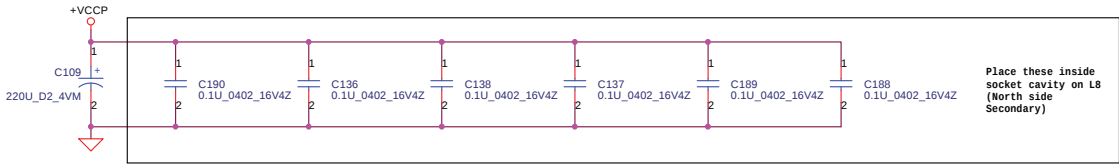
Diagram illustrating the connections for the PSII module:

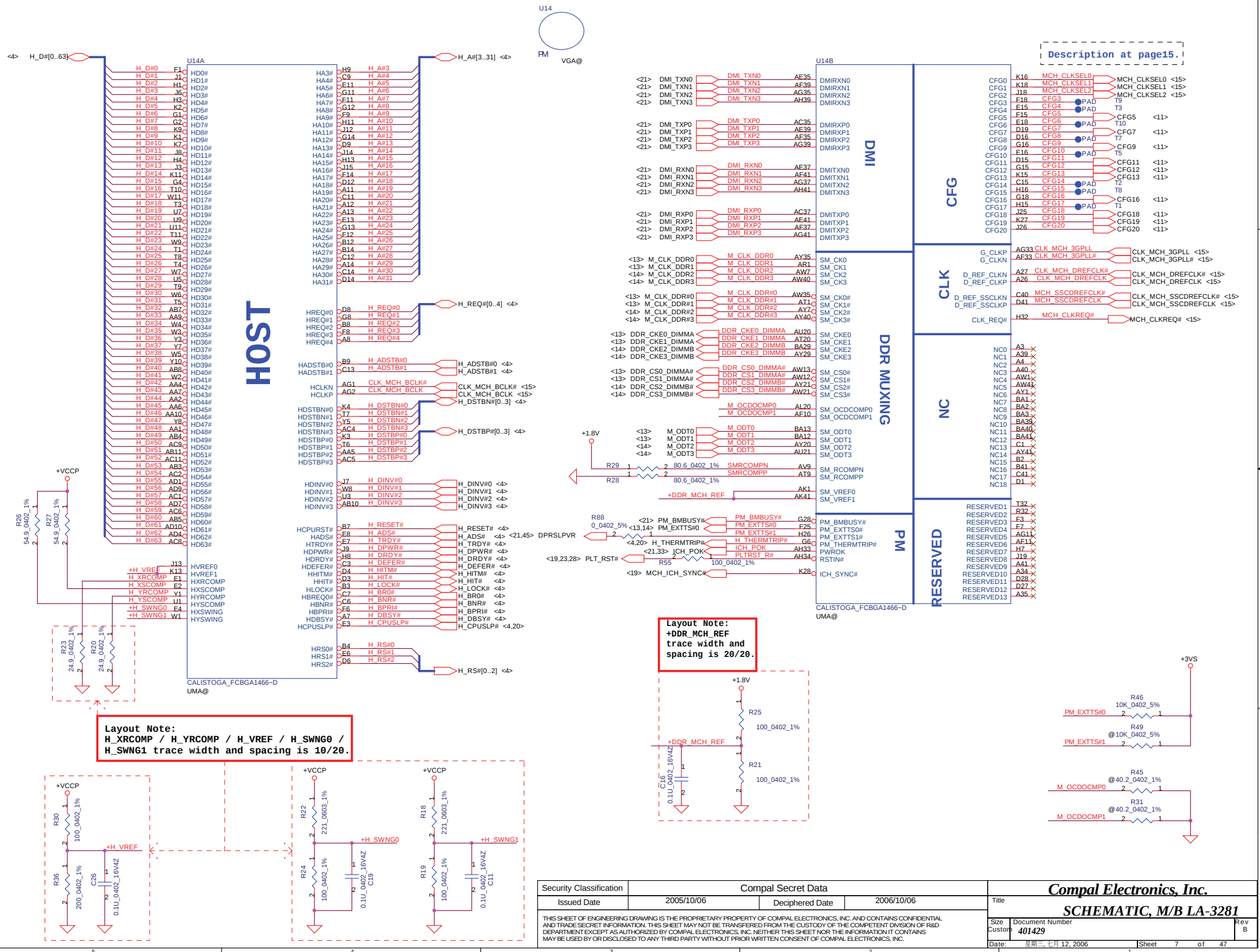
- PSII#** (Module) is connected to:
 - H_PSI#** (A60)
 - CPU_VID0** (AD6)
 - CPU_VID1** (AF5)
 - CPU_VID2** (AE5)
 - CPU_VID3** (AD5)
 - CPU_VID4** (AE3)
 - CPU_VID5** (AF2)
 - CPU_VID6** (AE2)
- PSII#** (Module) is connected to:
 - B22**
 - B23**
 - C21**
- PSII#** (Module) is connected to:
 - +CPU_GTLREF** (AD26)
 - CPU_BSEL0** (B22)
 - CPU_BSEL1** (B23)
 - CPU_BSEL2** (C21)



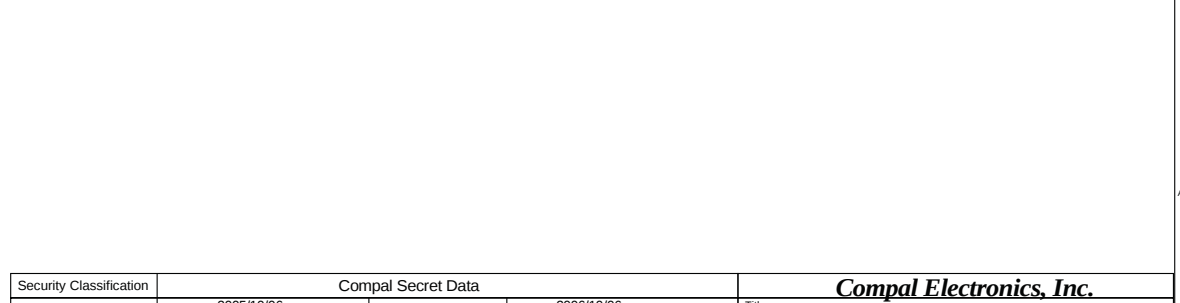
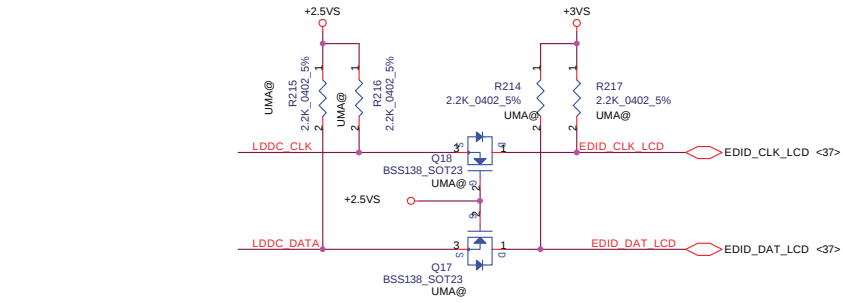
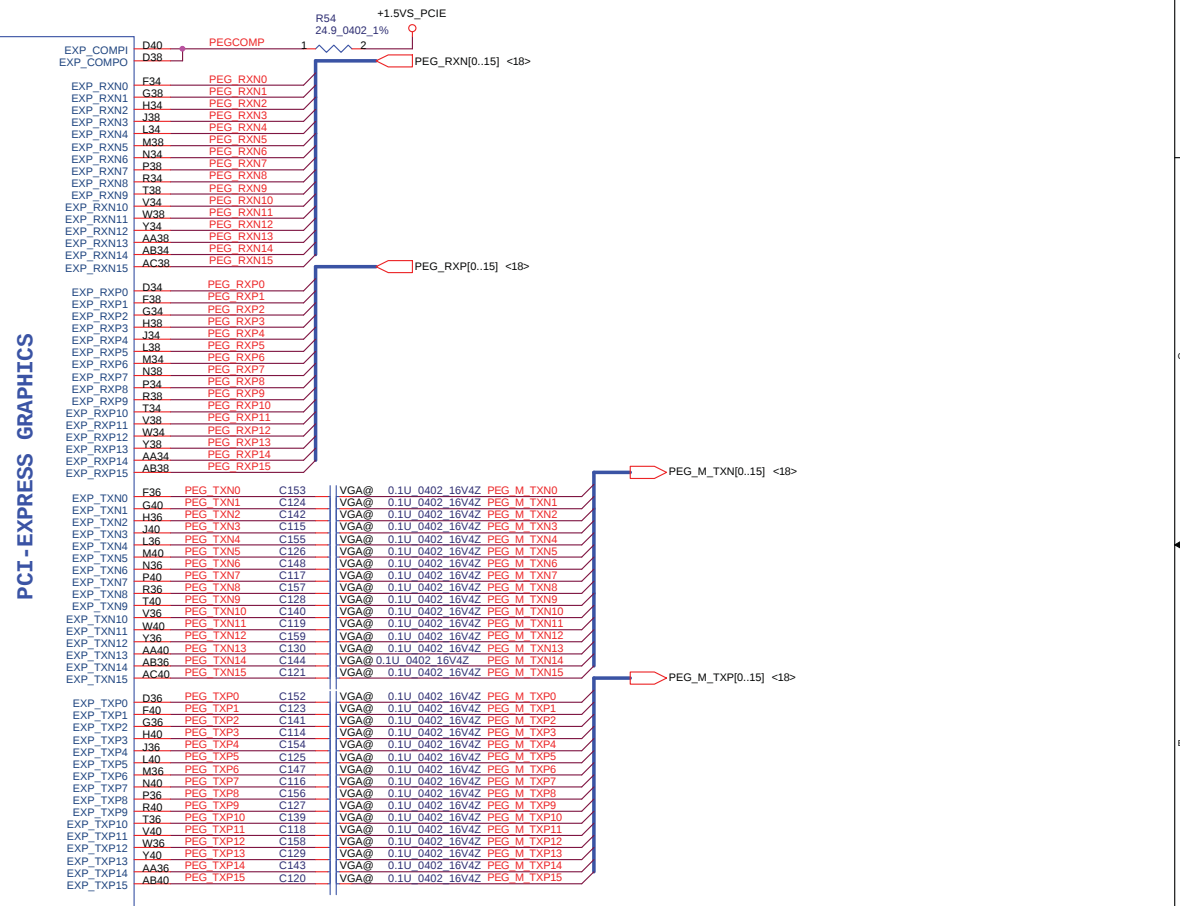
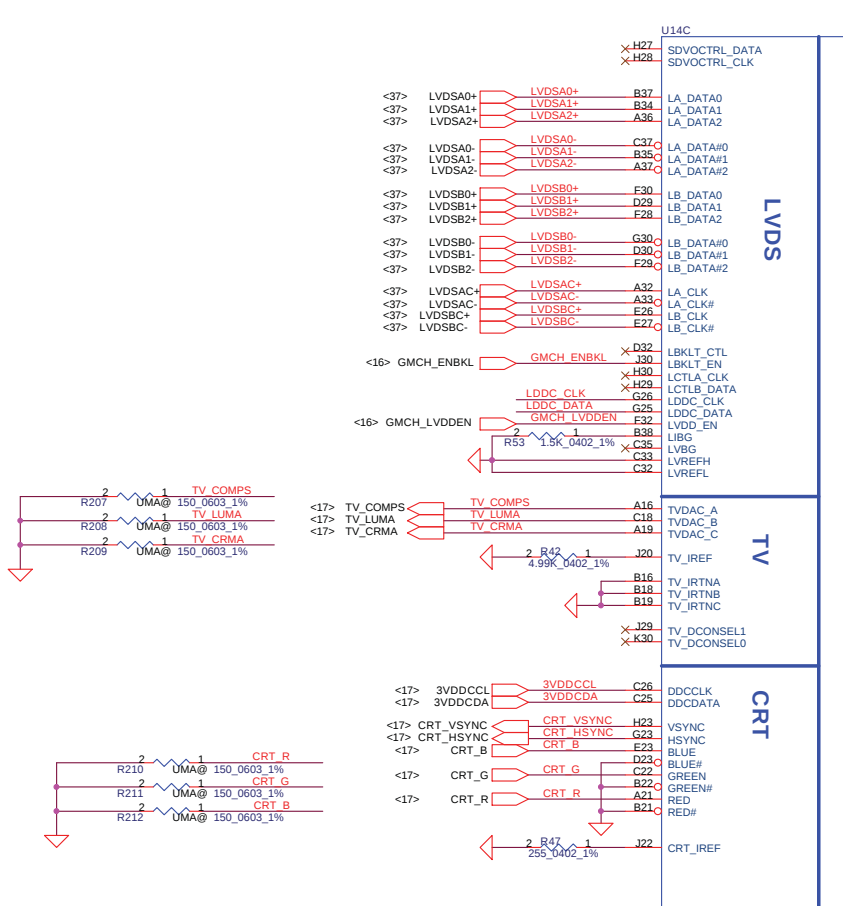


ESR <= 1.5m ohm
Capacitor > 1980uF





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				Date:	星期三, 七月 12, 2006 Sheet 7 of 47		

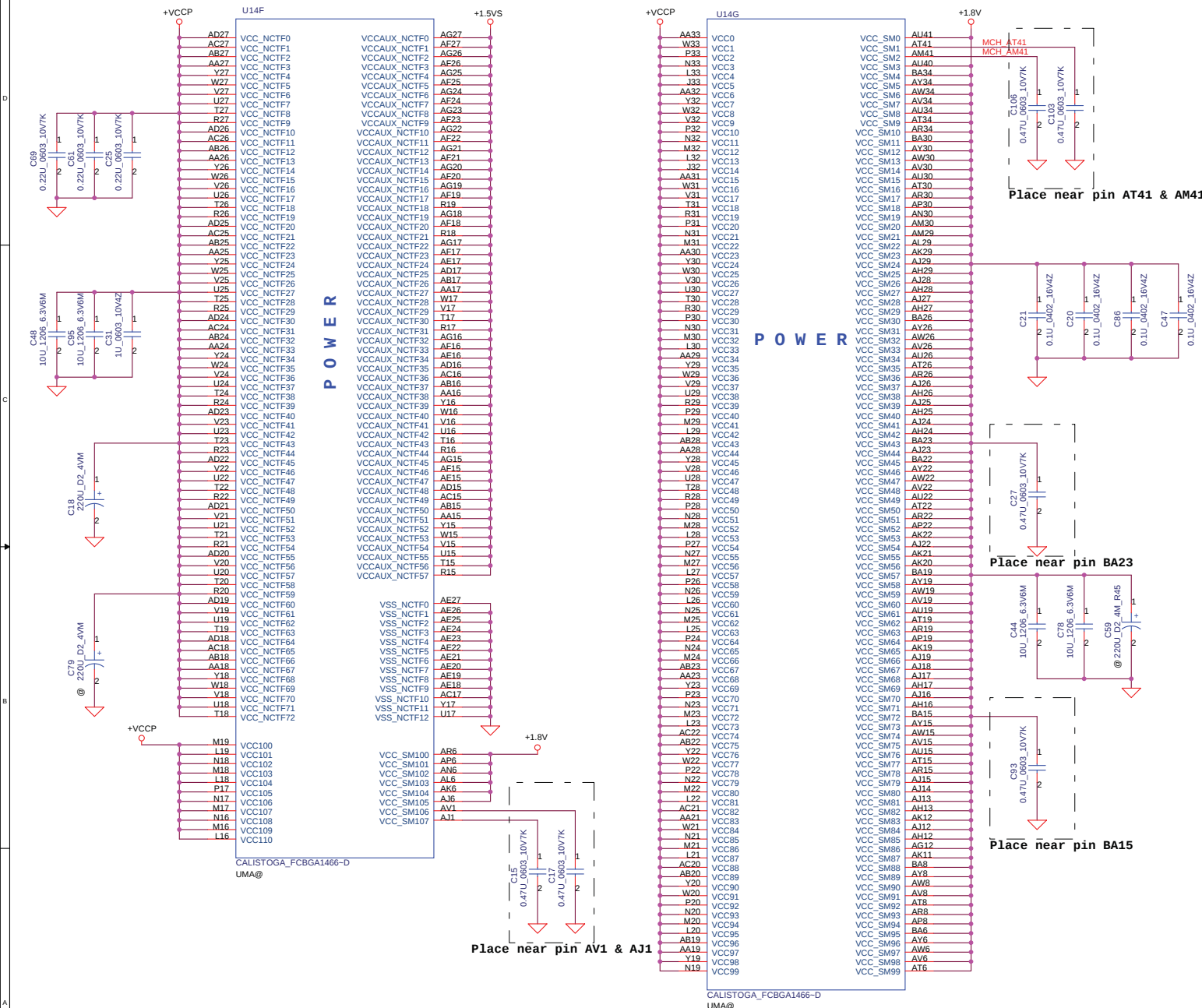


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Custom	401429	Date		Rev	
Date		2006/10/06		Sheet 9 of 47	

Strap Pin Table

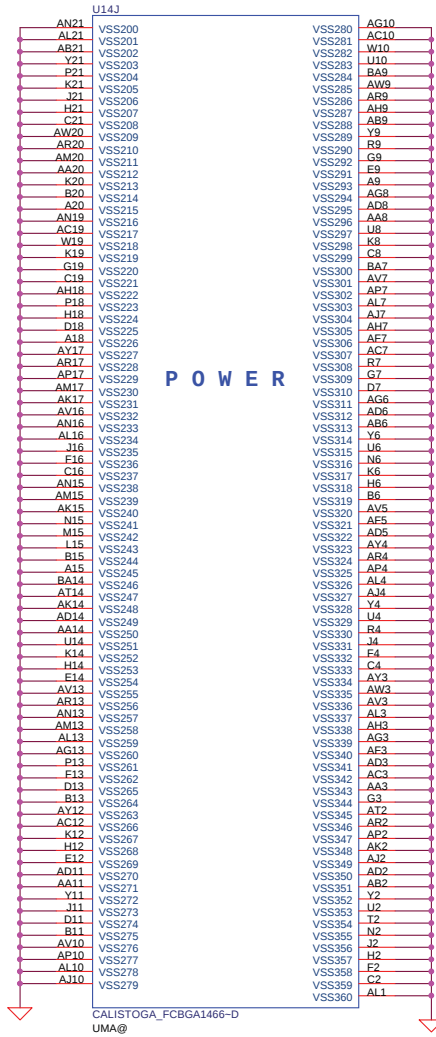
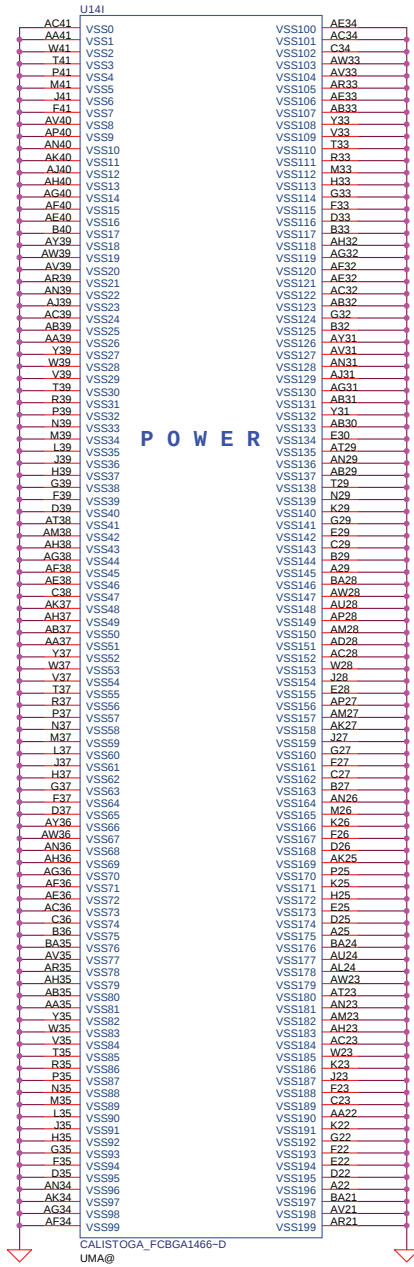
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



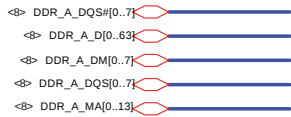
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				Sheet	11 of 47

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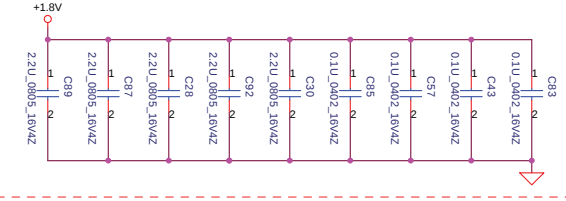


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				Rev	B

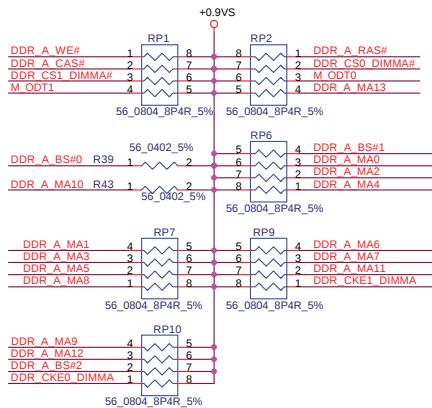
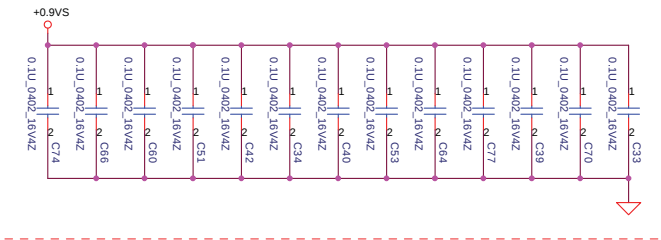
SCHEMATIC, M/B LA-328I



Layout Note:
Place near JP41



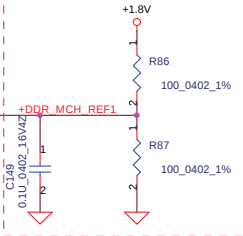
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP41, all
trace length Max=1.5"

Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.

<14> +DDR_MCH_REF1



<14.33> EC_P80_DATA

<7> DDR_CKE0_DIMMA

<14.33> EC_P80_CLK

<8> DDR_A_BS#2

<8> DDR_A_BS#0

<8> DDR_A_WE#

<8> DDR_A_CAS#

<7> DDR_CS1_DIMMA#

<7> M_ODT1

<7> M_ODT1

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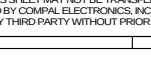
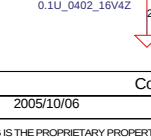
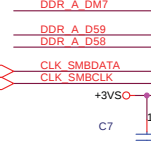
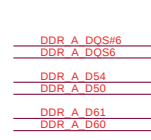
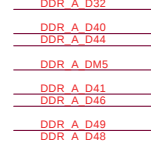
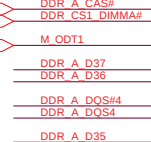
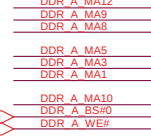
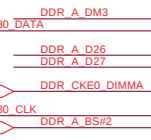
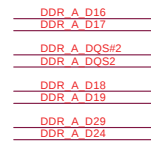
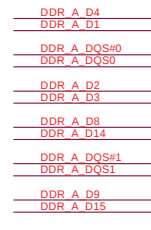
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<7> M_ODT1

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<7> M_ODT1



+1.8V

+3VSO

0.1u_0402_16V4Z

SO-DIMM A

Top side

+1.8V

+3VSO

0.1u_0402_16V4Z

SO-DIMM A

Top side

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13				of				47			

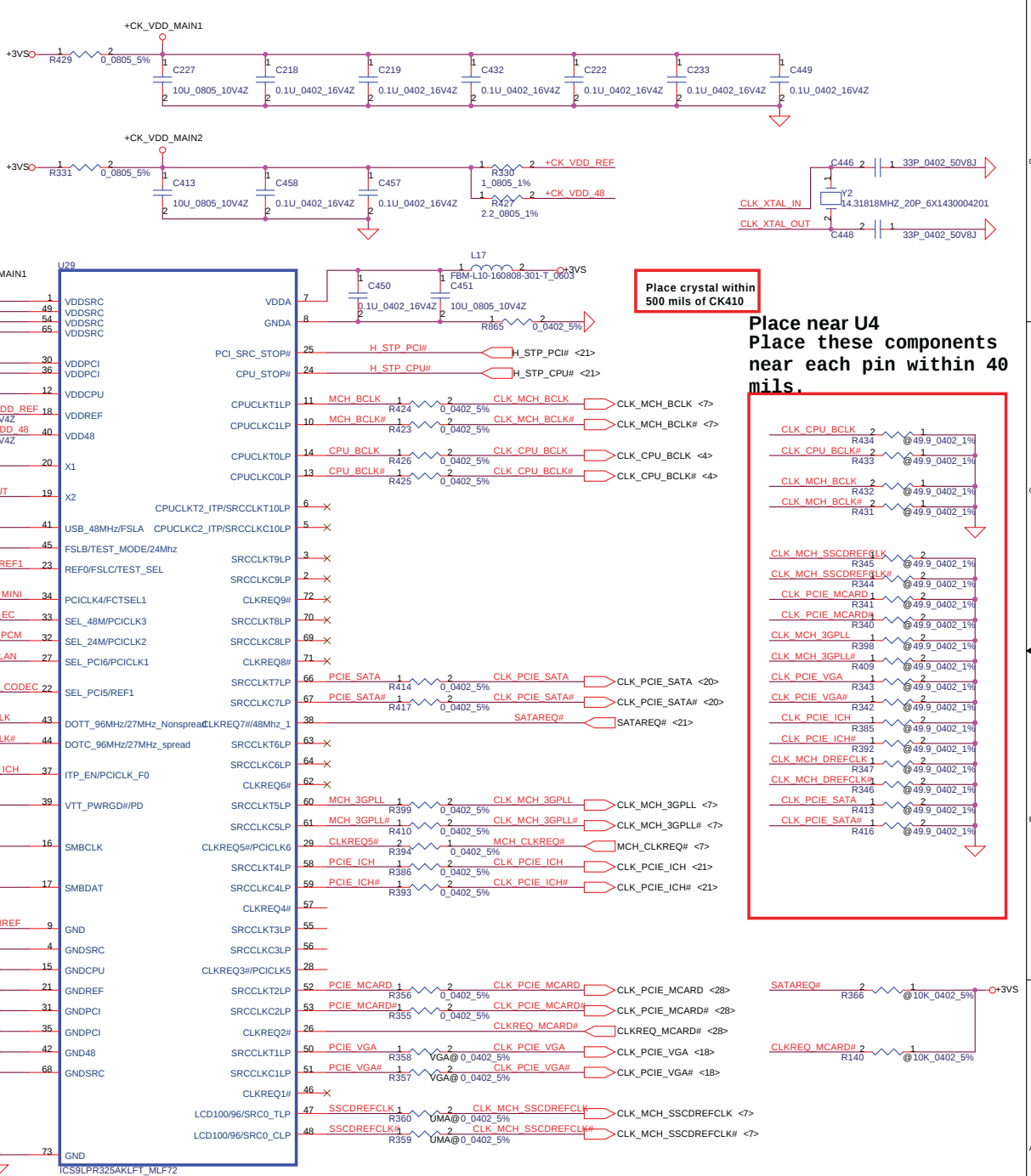
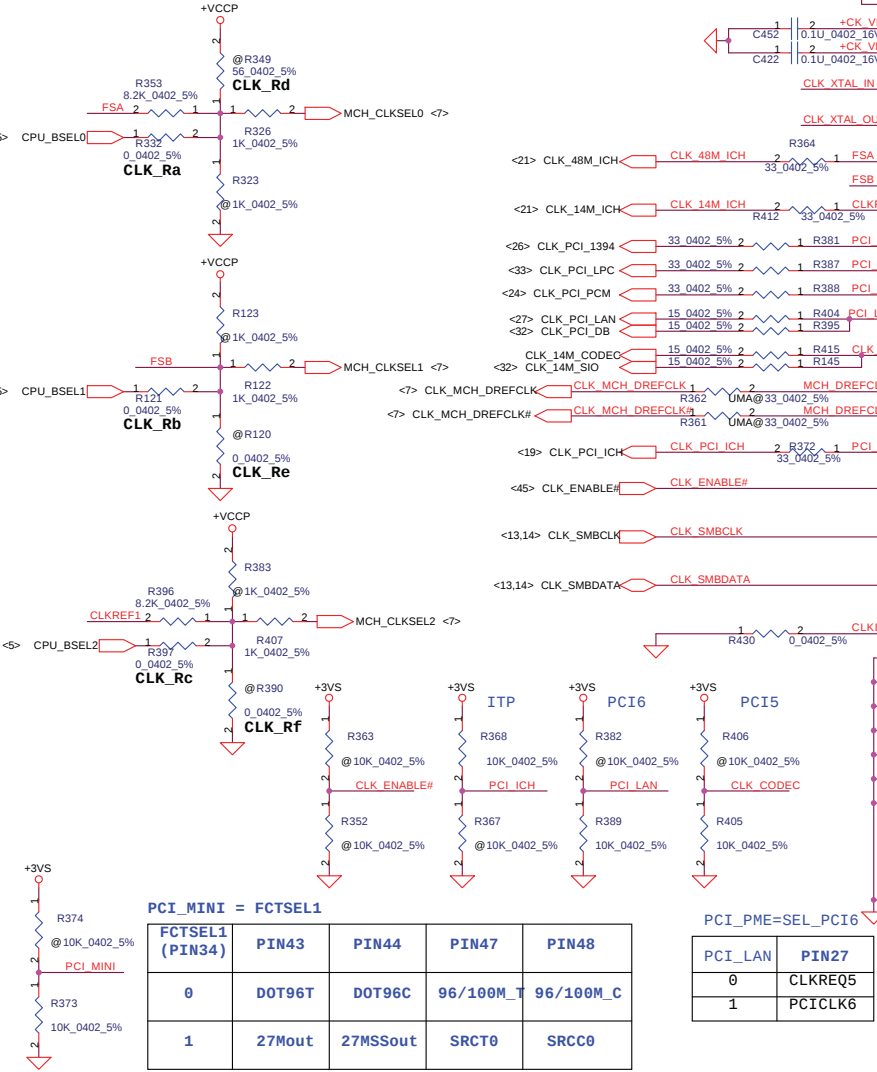
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				Date	星期日, 七月 12, 2006	
				Sheet	14	of 47

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

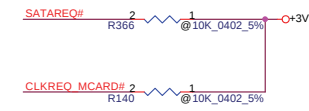
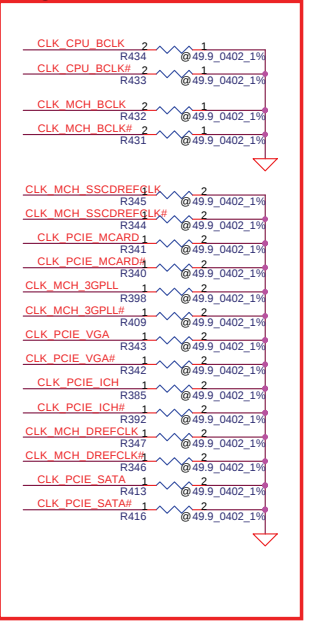
FSB Frequency Selet:

CPU Driven * (Default)	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



Place crystal within
500 mils of CK410

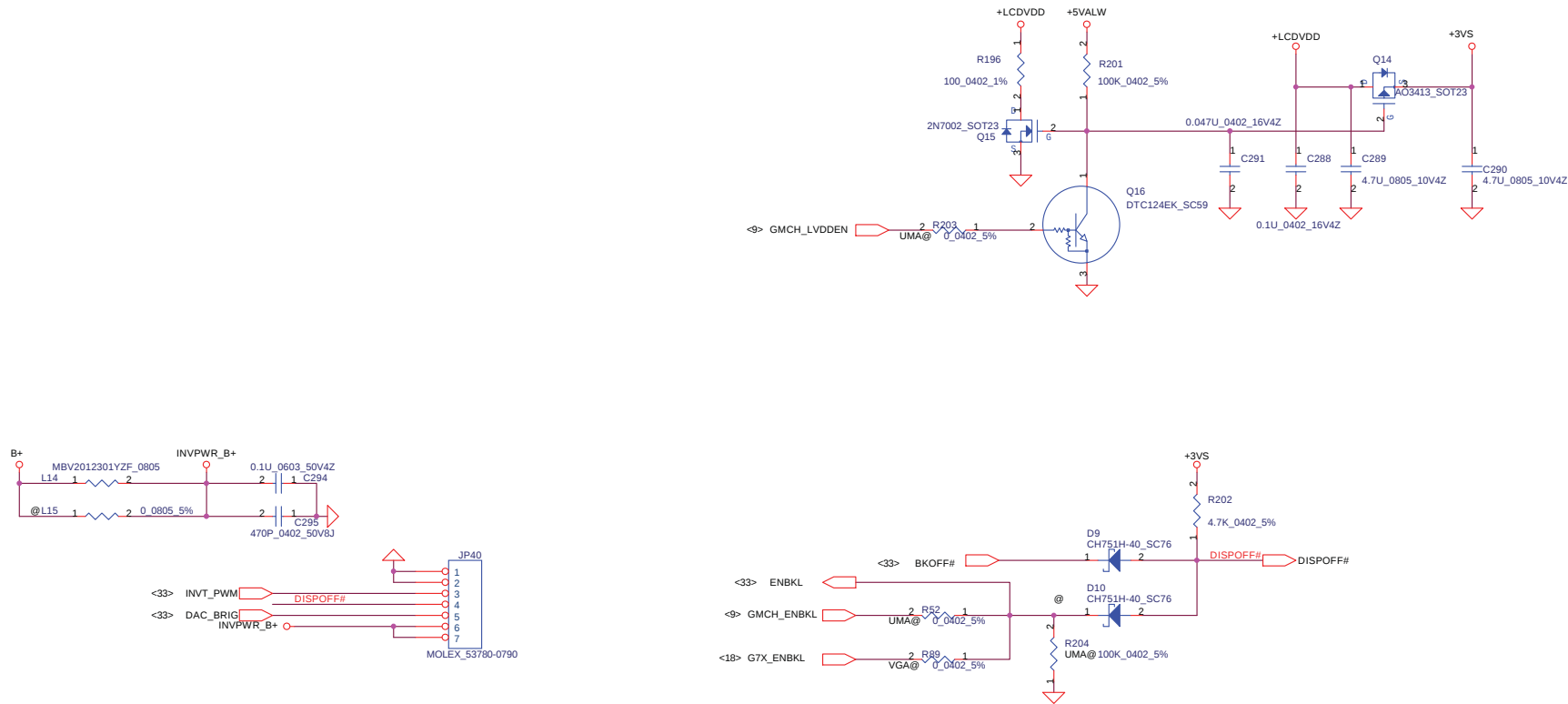
Place near U4
Place these components
near each pin within 40
mils.



PCI_MINI = FCTSEL1				
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSSout	SRCT0	SRCC0

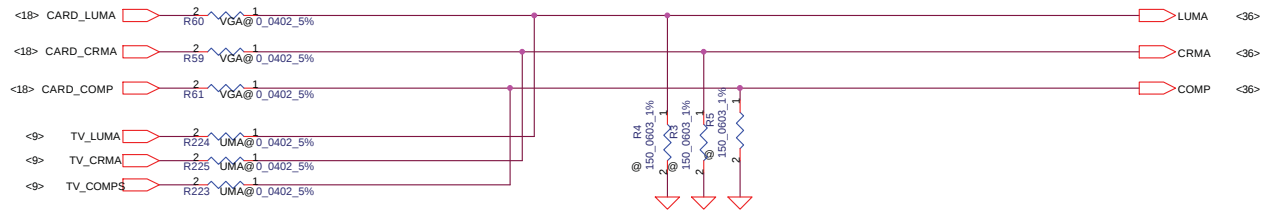
PCI_PME=SEL_PCI6	
PCI_LAN	PIN27
0	CLKREQ5
1	PCICLK6

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Sheet 15 of 47				Rev B	



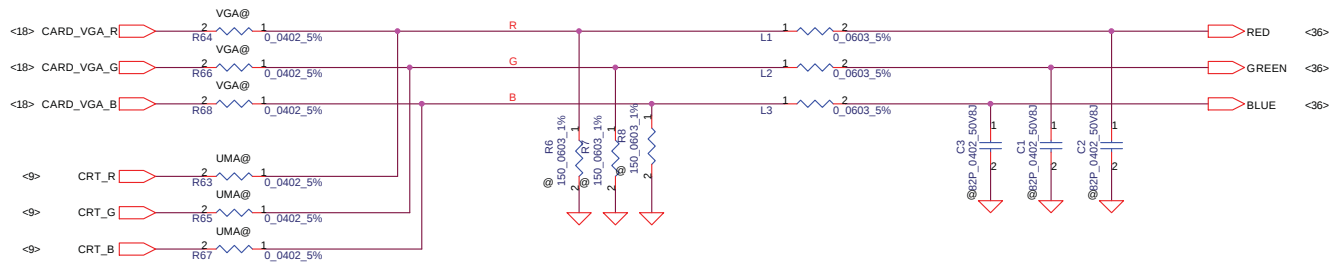
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Custom		401429		B	
Date		Sheet		of	
2006/07/12		16		47	

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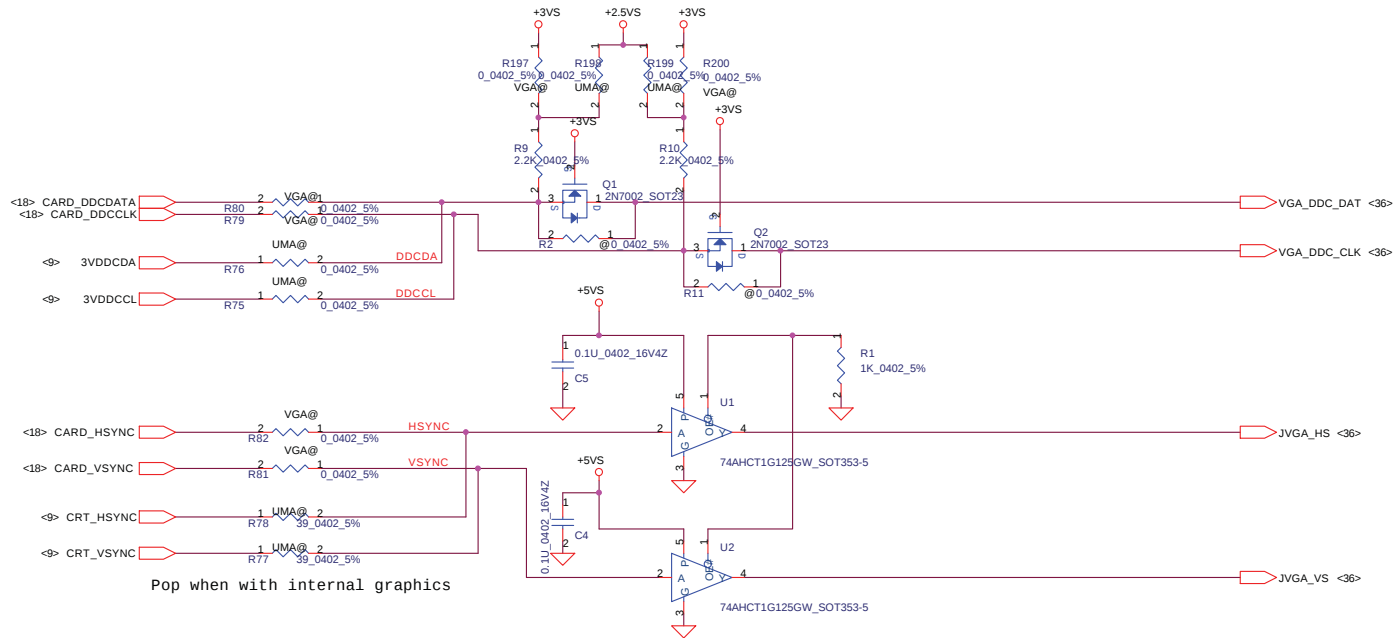


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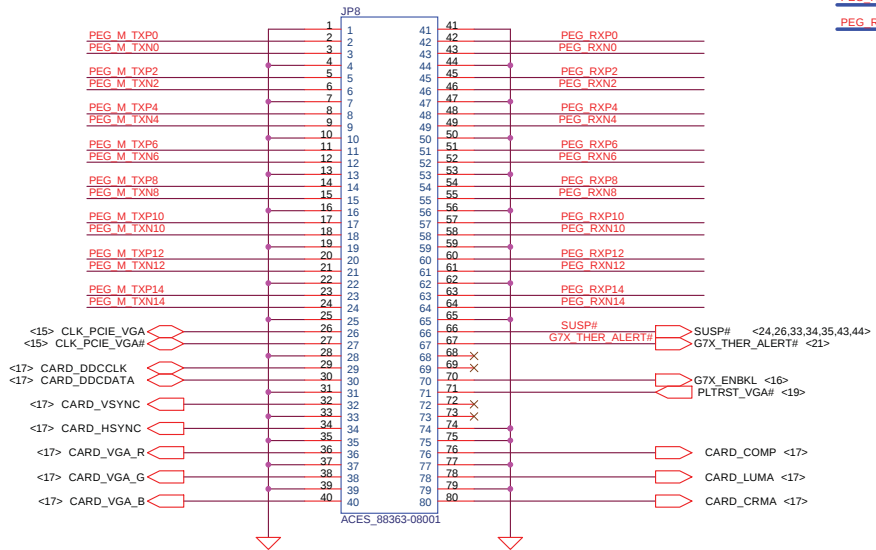
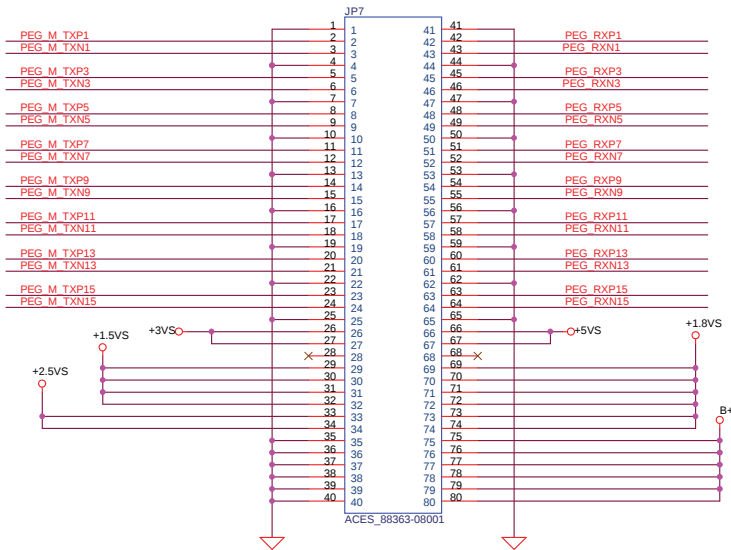


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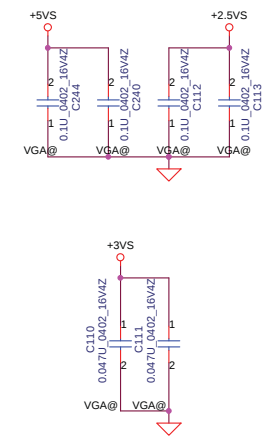
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				Custom	401429
				Date	Rev B
				星期三, 七月 12, 2006	Sheet 17 of 47



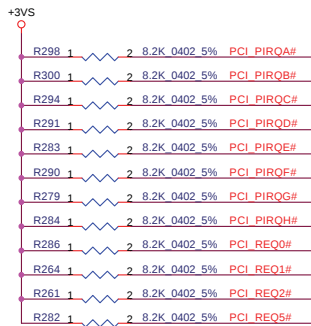
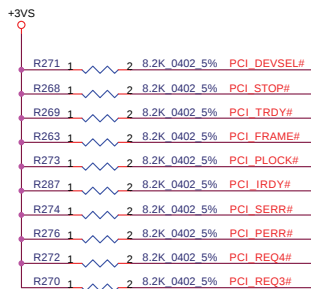
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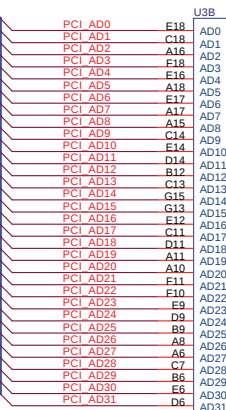


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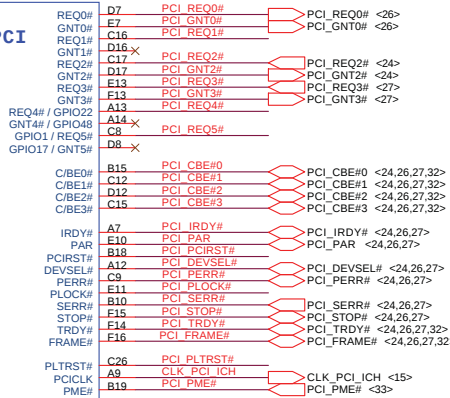
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SCHEMATIC, M/B LA-3281			
Title			
Size	Document Number	Rev	
Custor	401429	B	
Date	星期三, 七月 12, 2006	Sheet	18 of 47



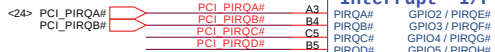
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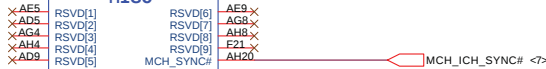
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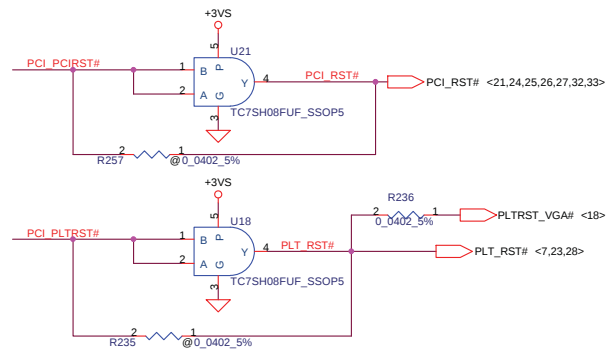
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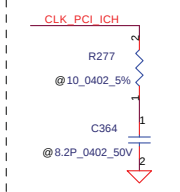
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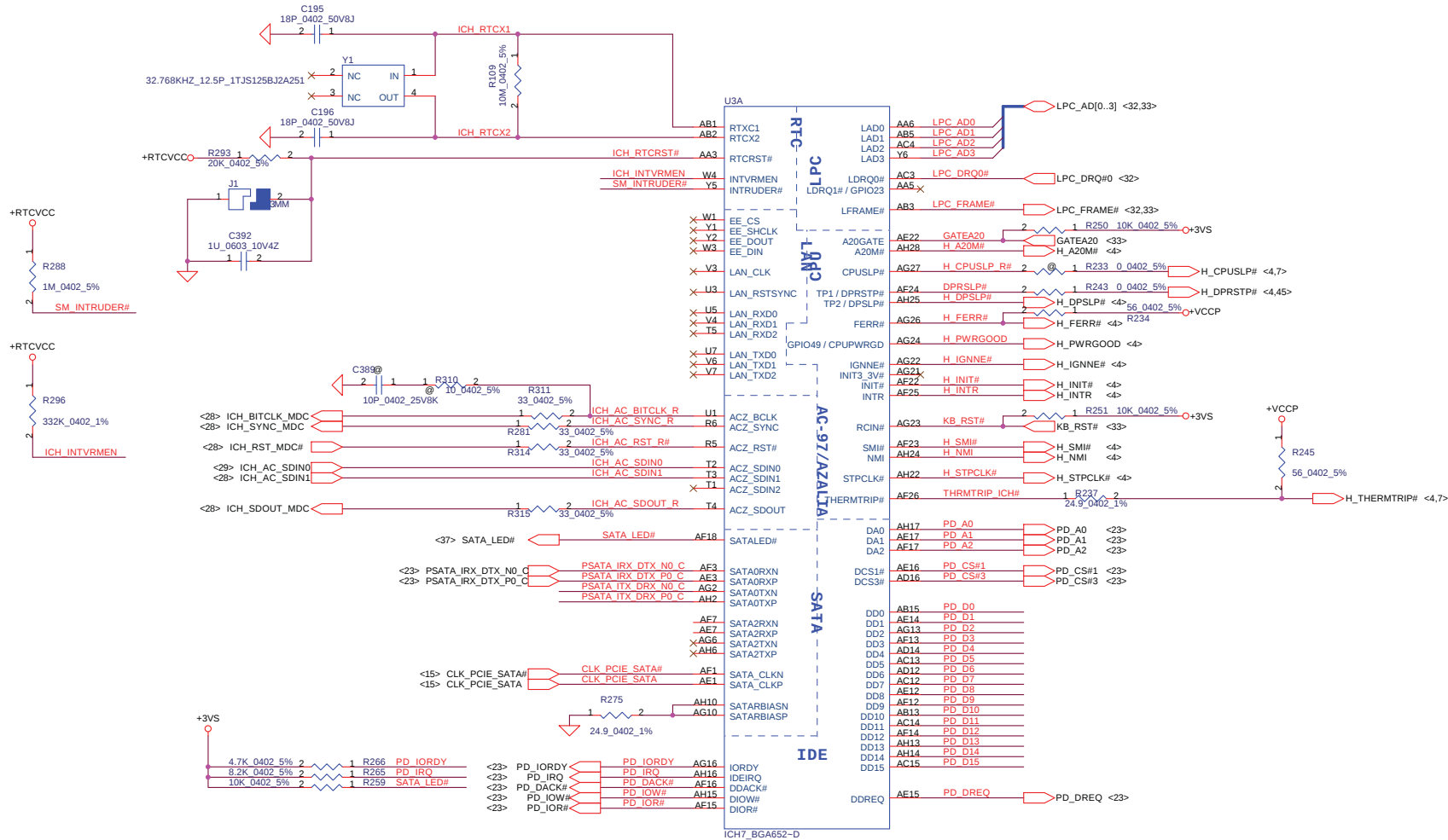
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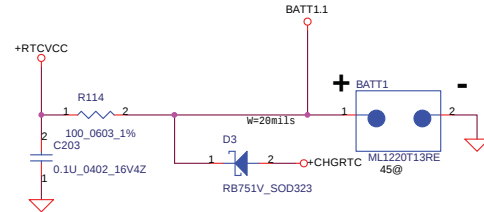
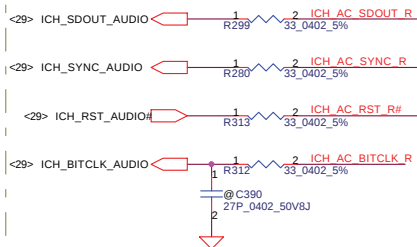
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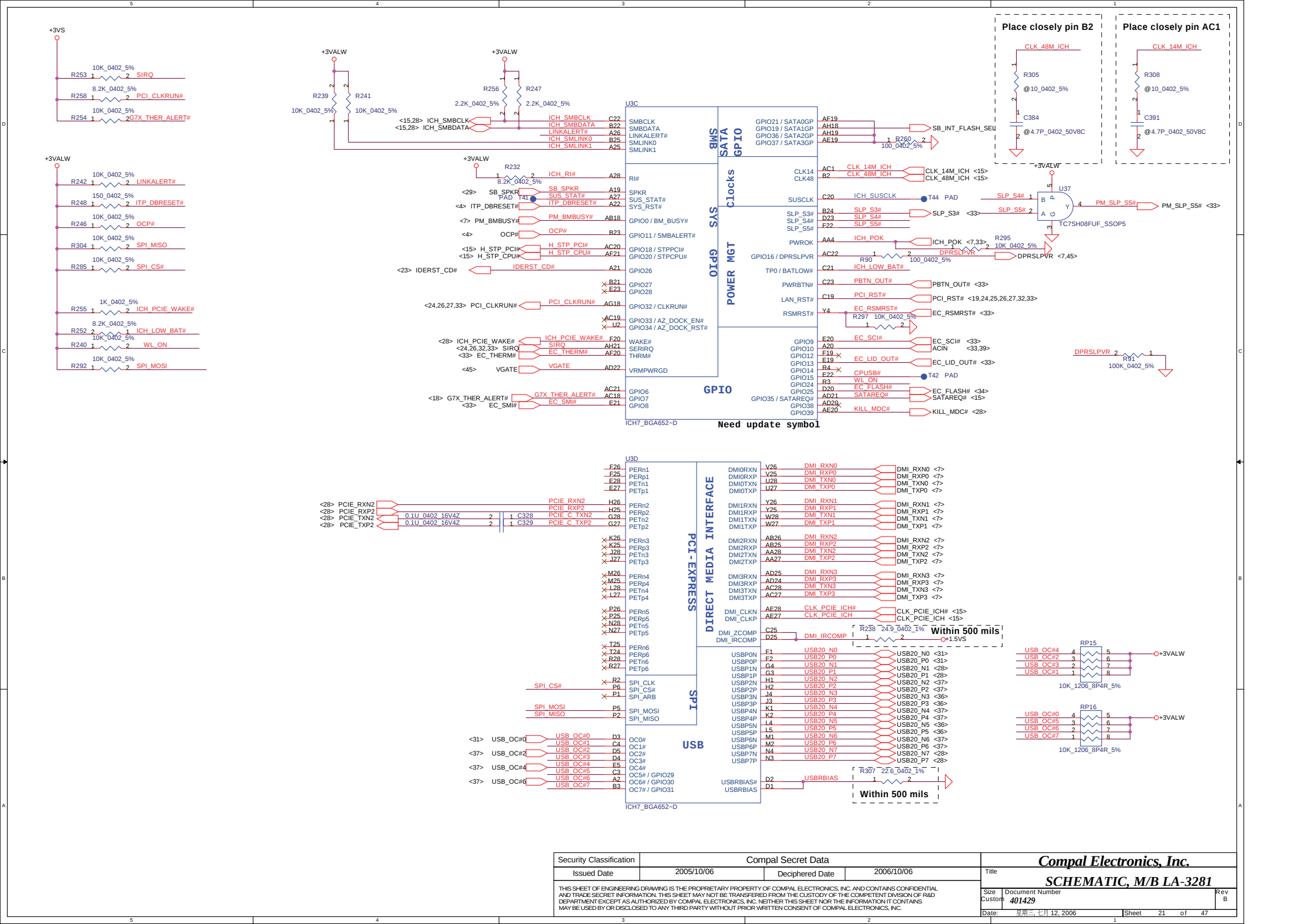
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Size		Document Number		Rev	
Date		Sheet		of	
2006/10/06		19		47	

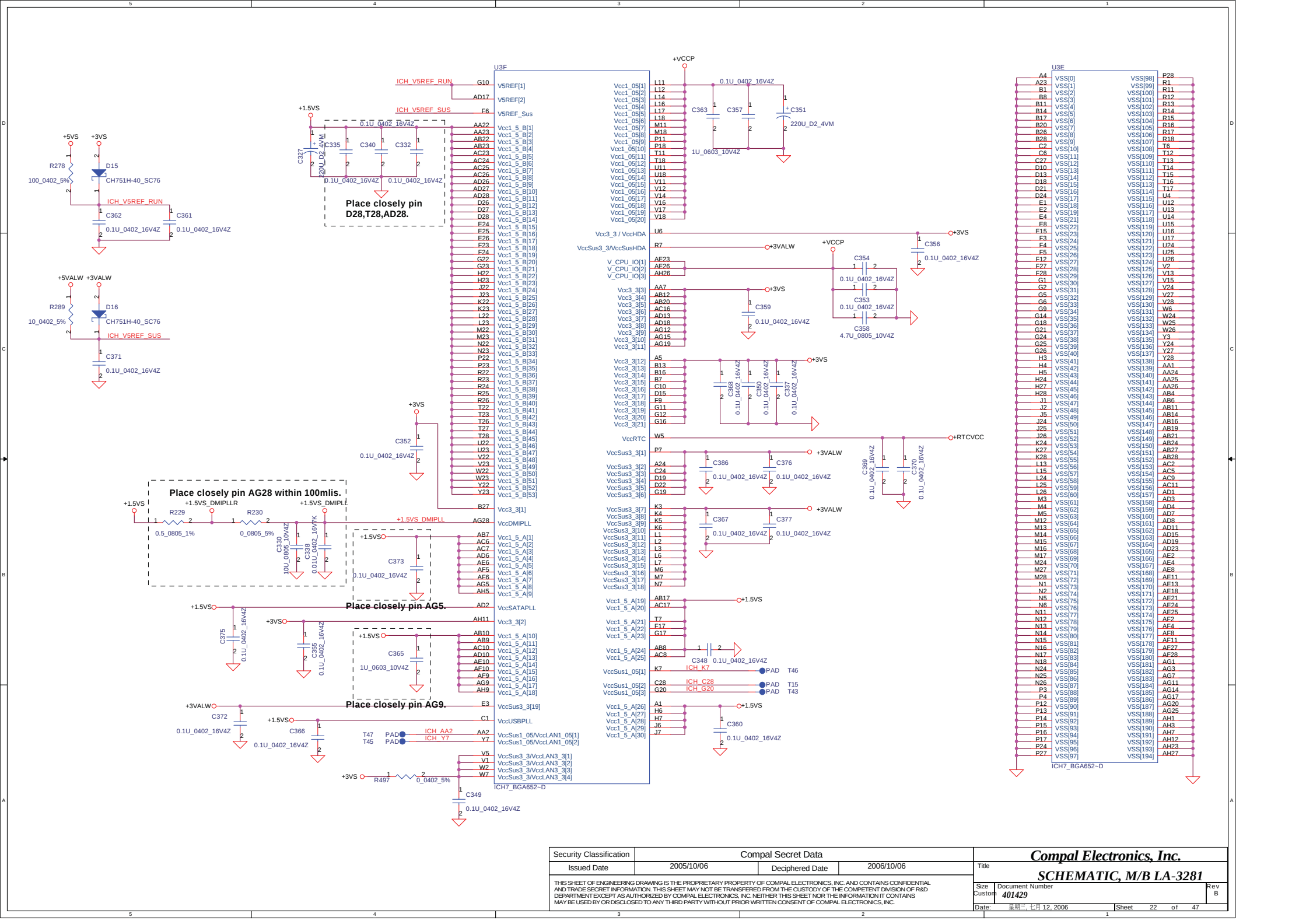


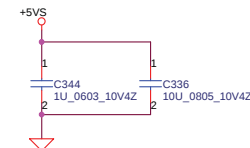
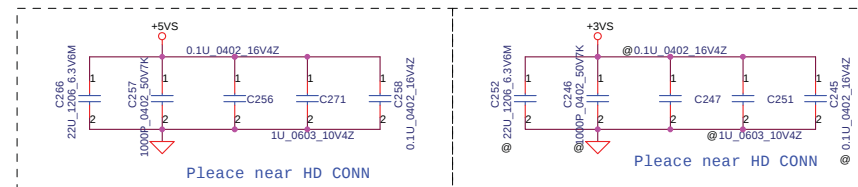
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				Custom	401429
				Rev	B
				Date	星期三, 七月 12, 2006
				Sheet	20 of 47

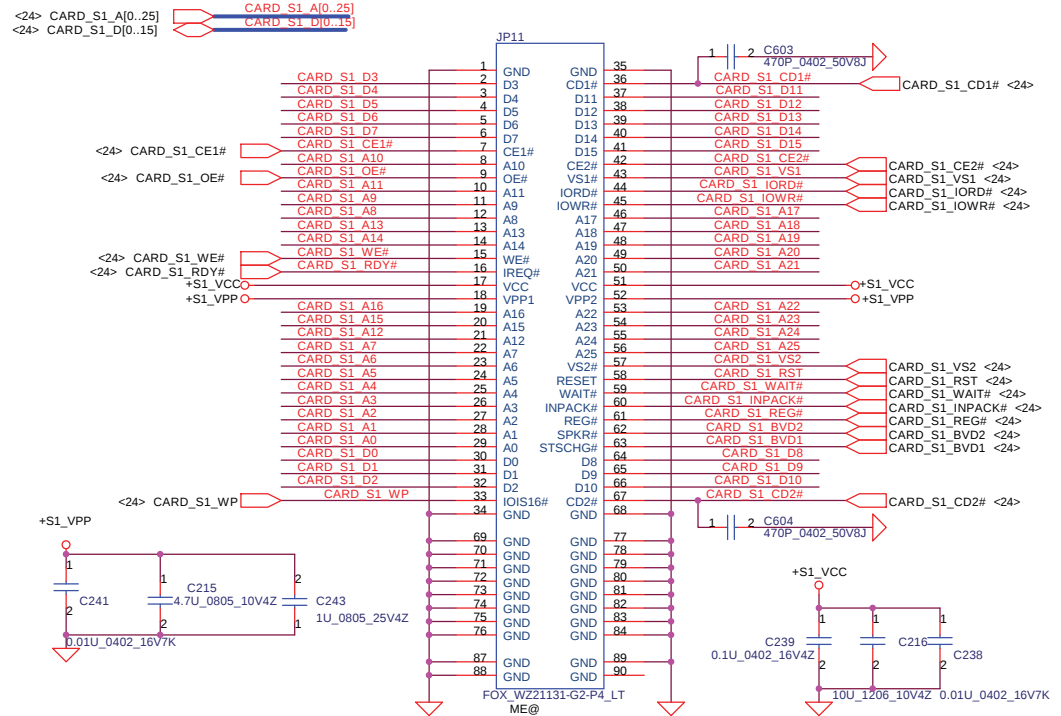
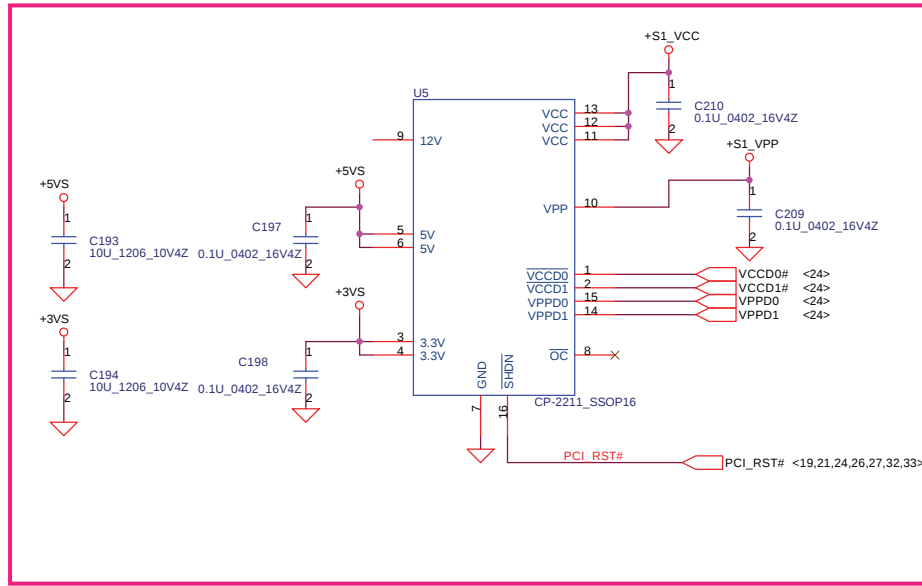




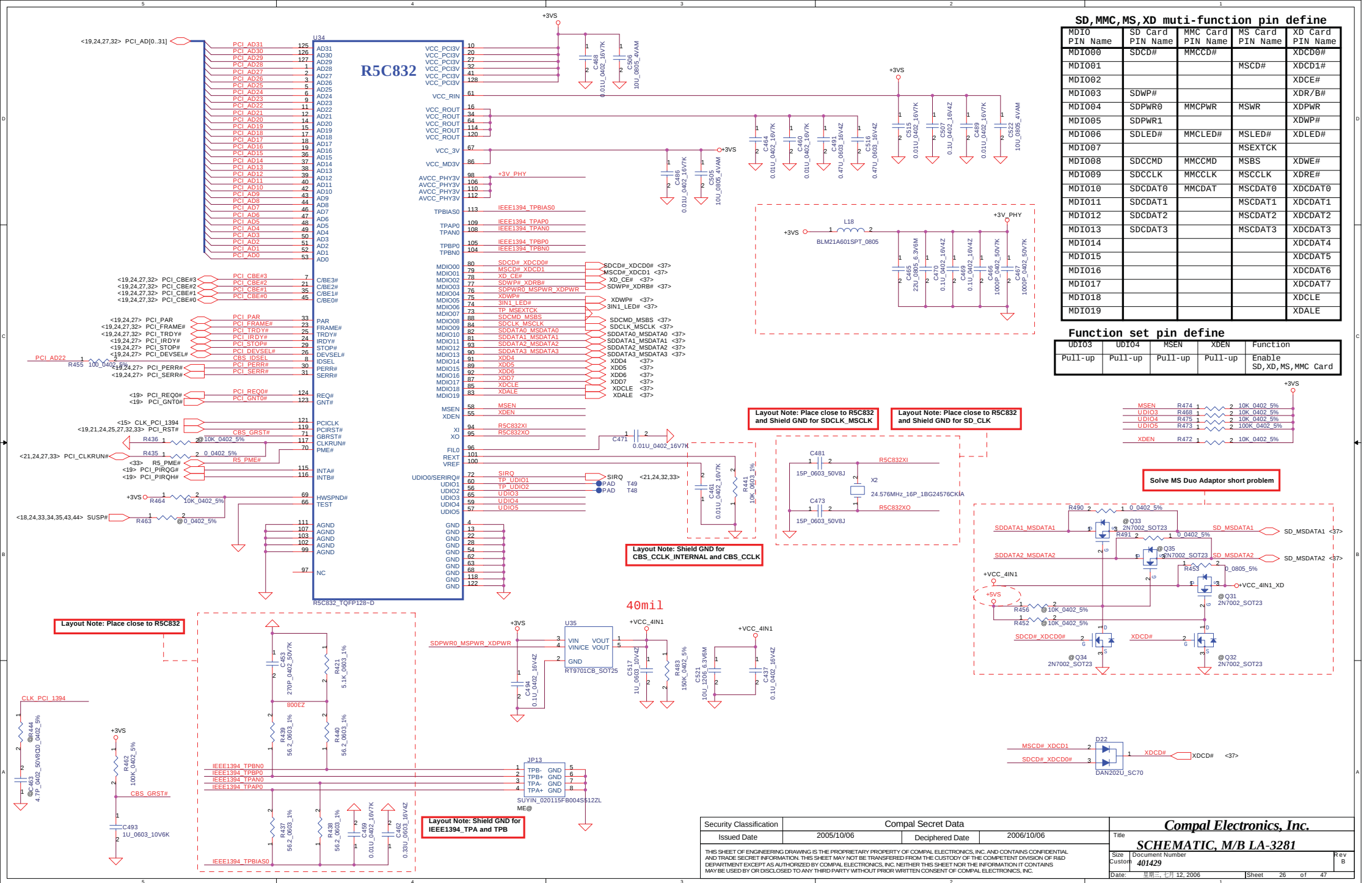


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Date: 星期三, 七月 12, 2006		Sheet 23 of 47			

PCMCIA Power Controller



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				Date: 星期二, 七月 12, 2006	Rev B
				Sheet 25 of 47	

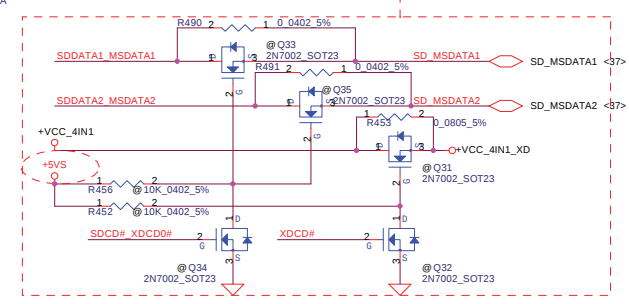


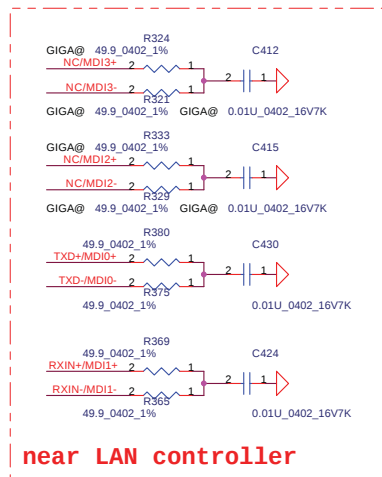
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MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPCR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLD#	MSLED#	XDLED#
MDIO07				
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCL
MDIO19				XDAL

Function set pin define				
UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

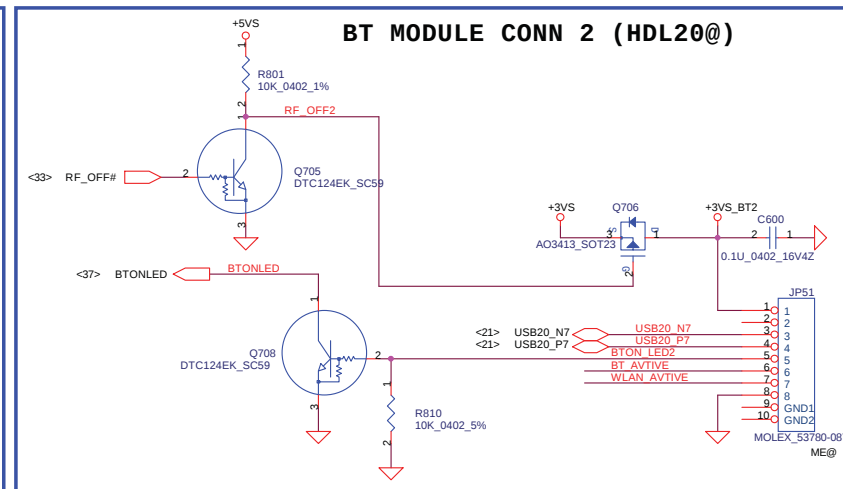
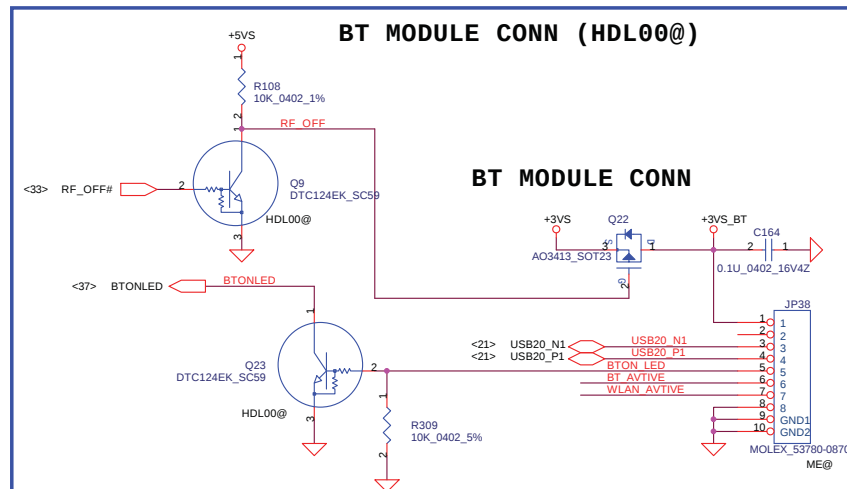
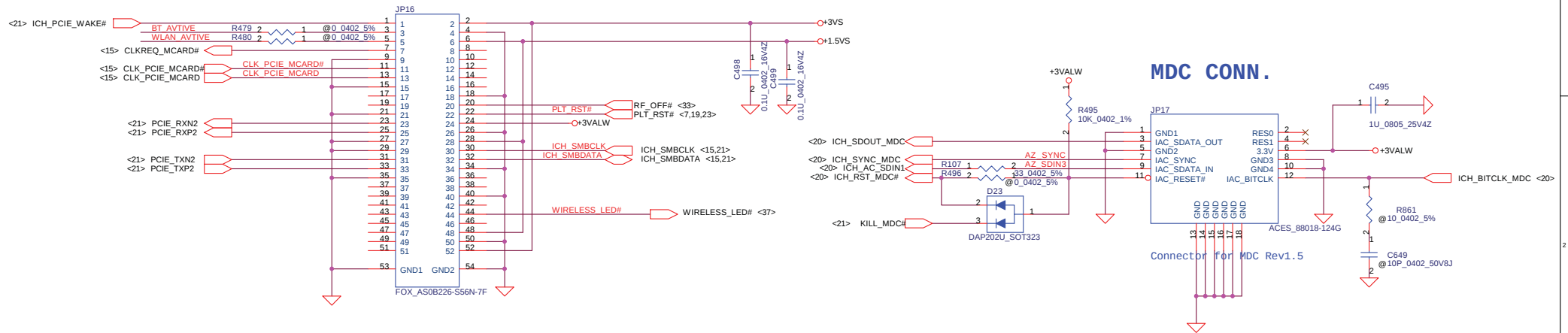


Solve MS Duo Adaptor short problem

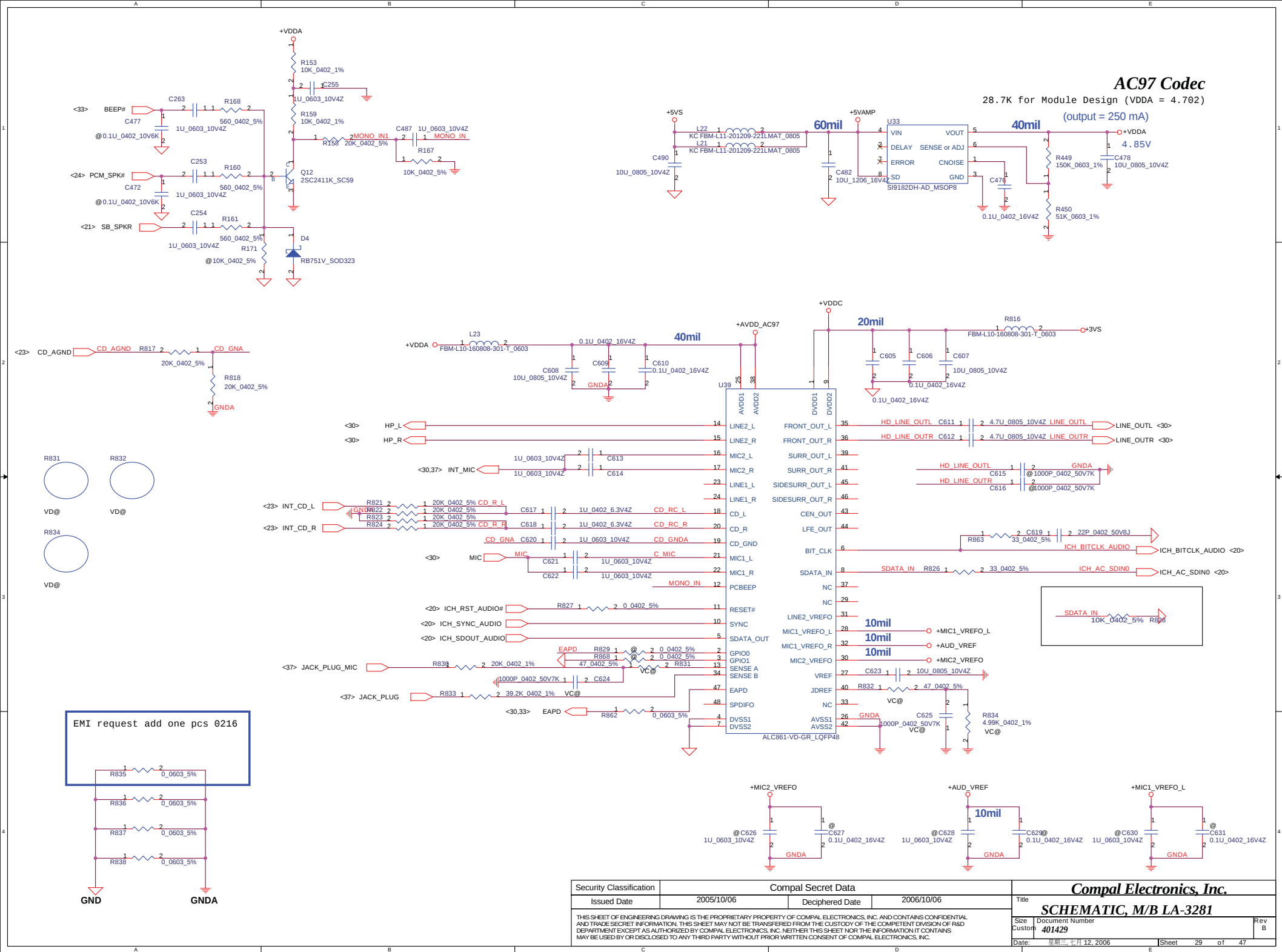


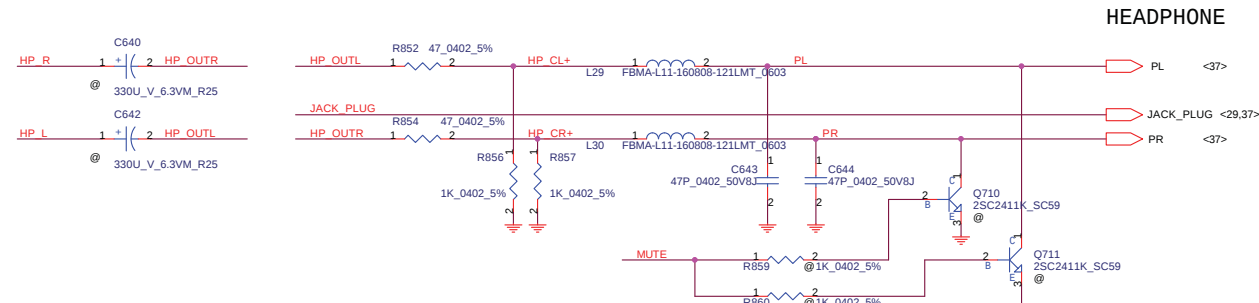
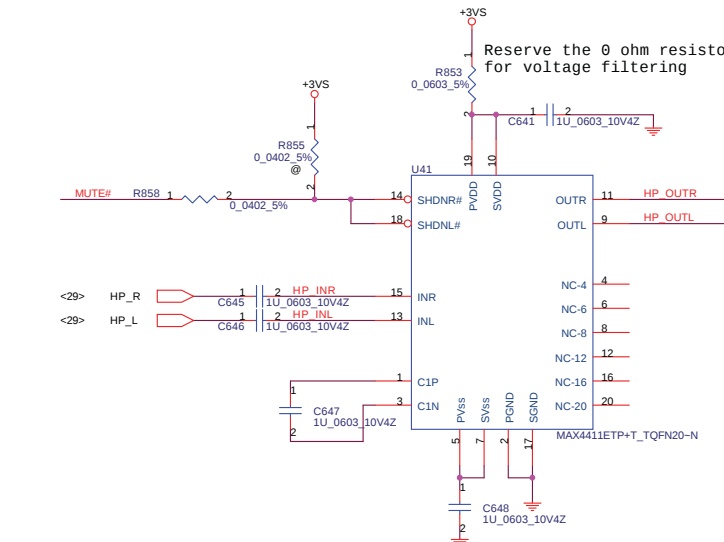
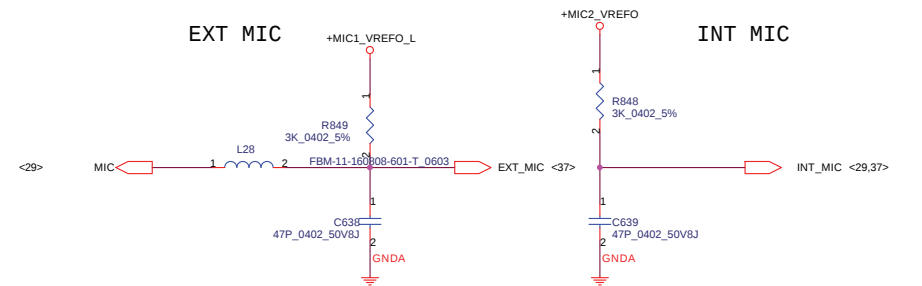
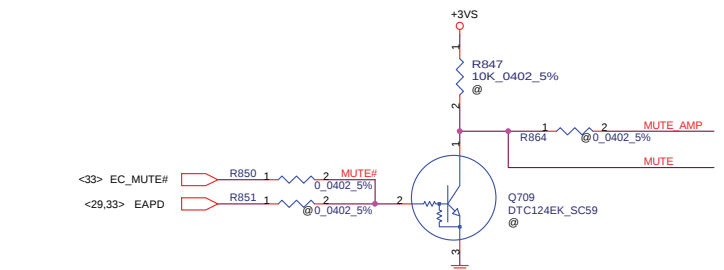
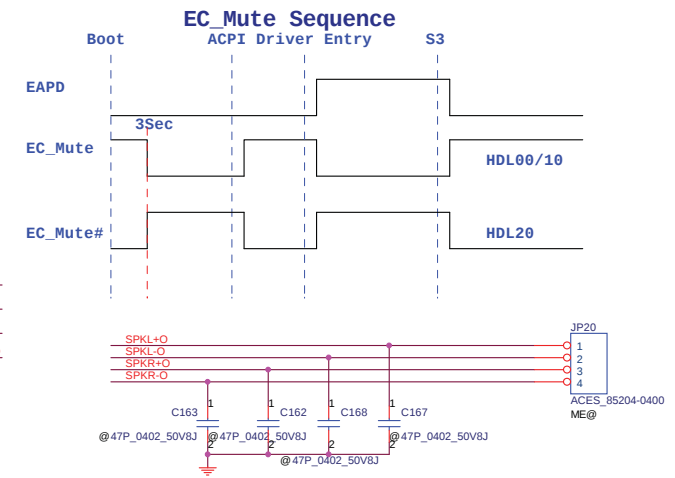
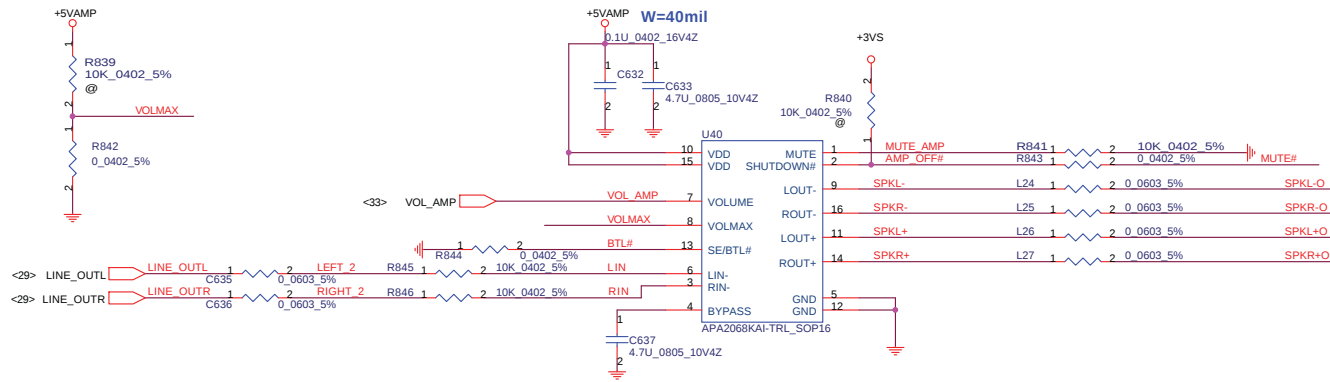


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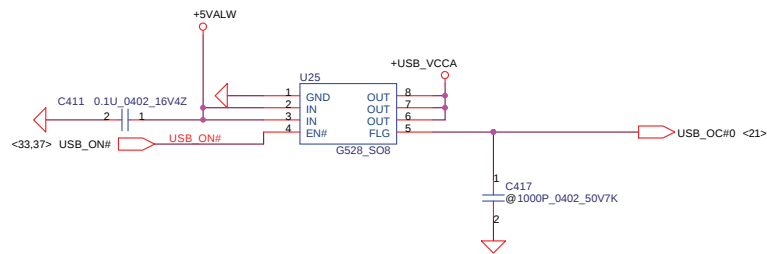


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				Custom	B
				Document Number 401429	
Date: 星期二, 七月 12, 2006				Sheet 28 of 47	

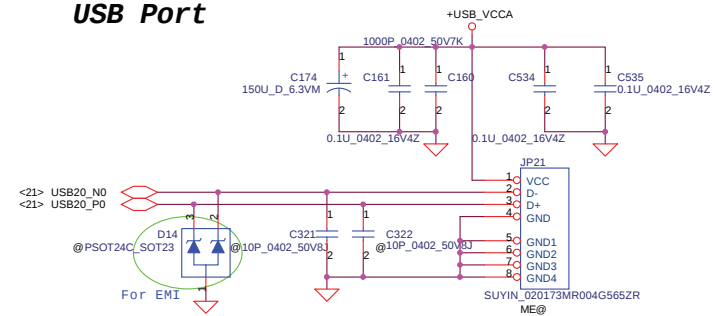




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Date: 星期三, 七月 12, 2006		Sheet 30 of 47			

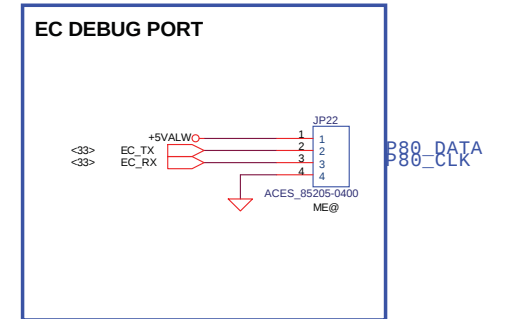
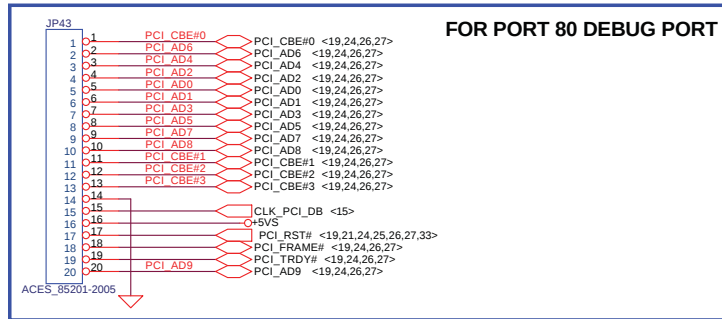
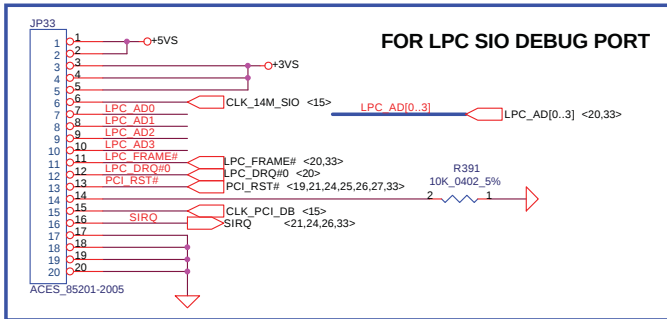
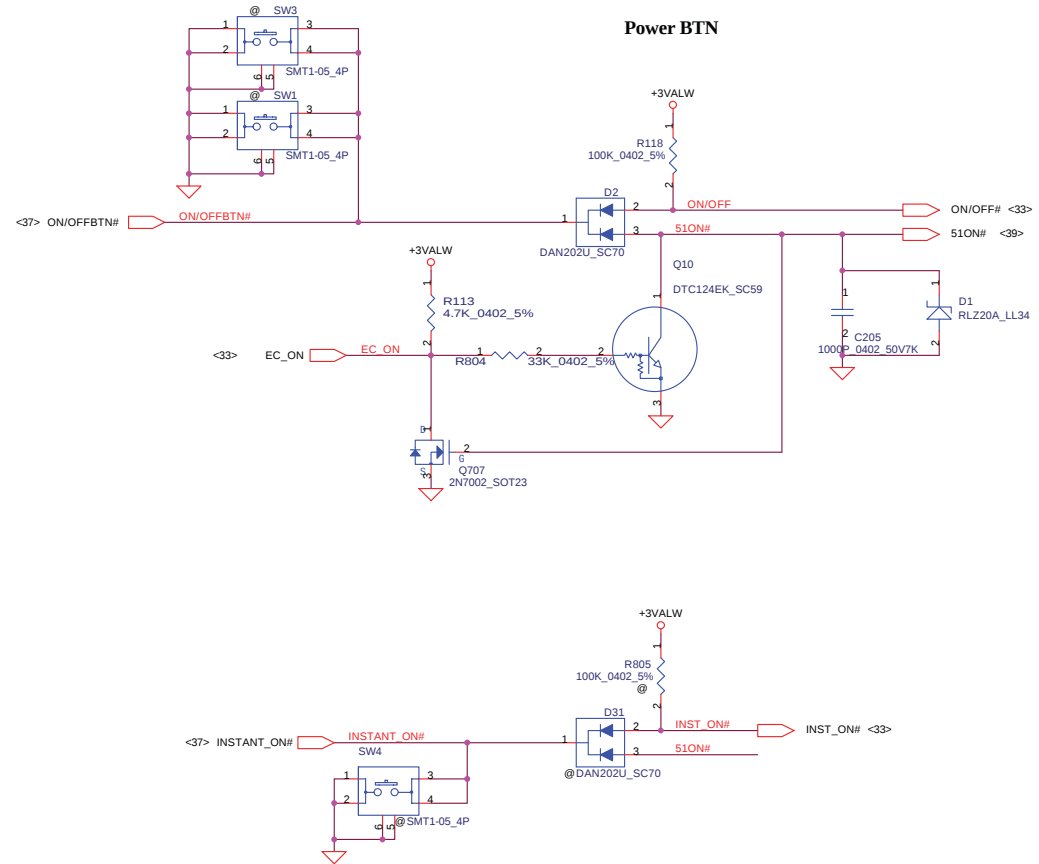
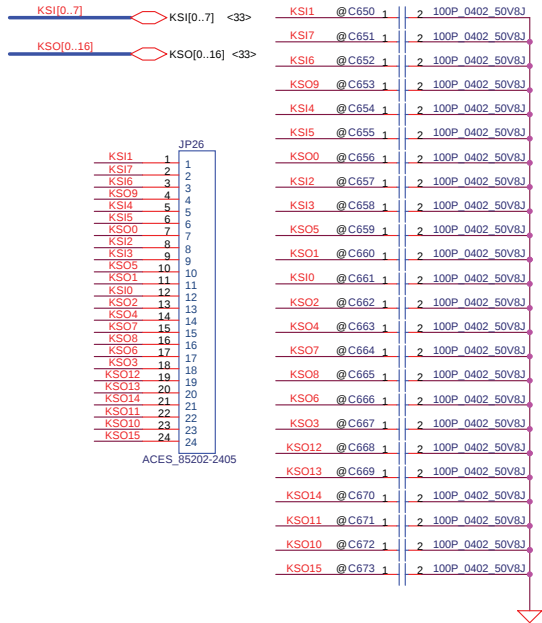


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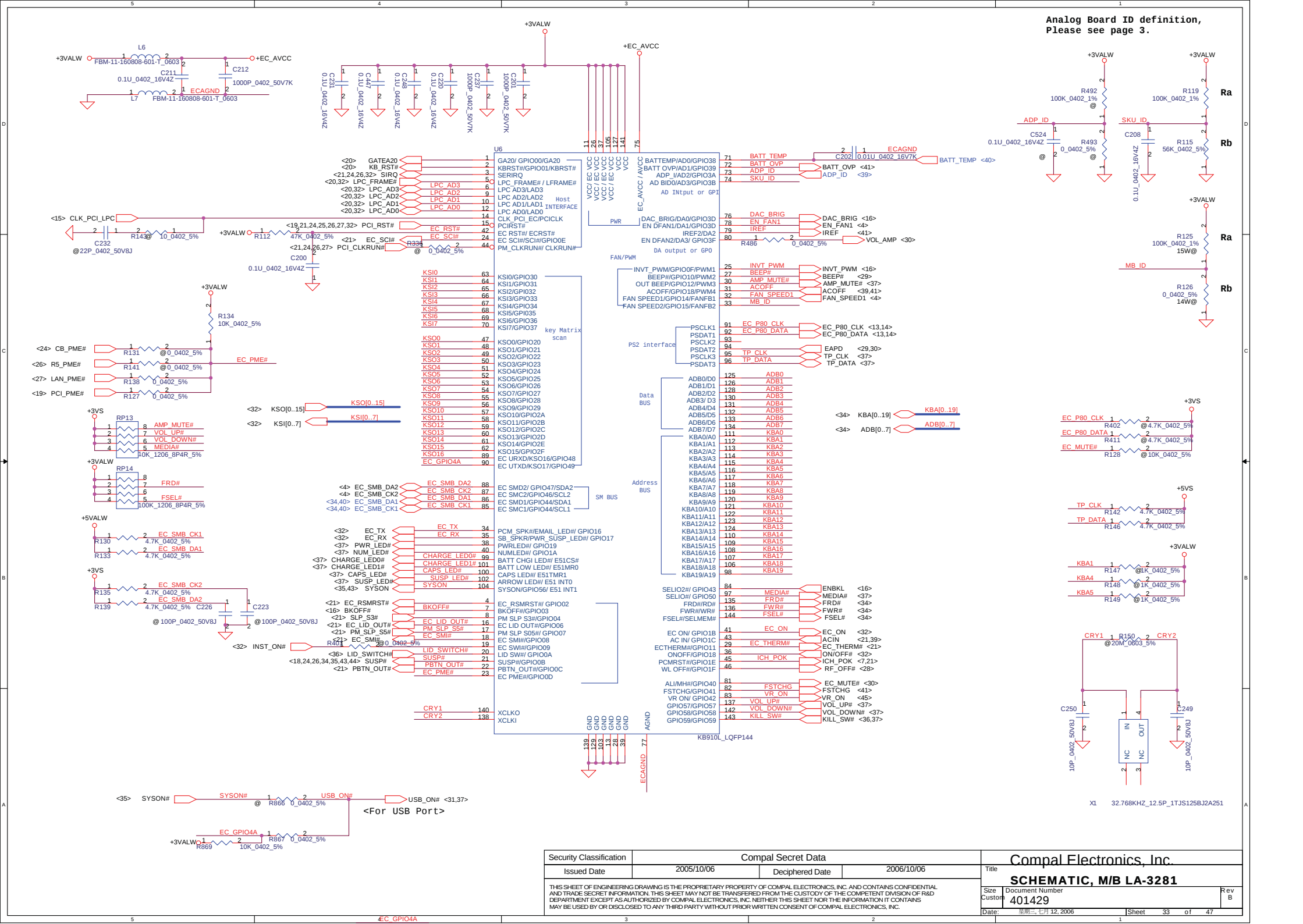


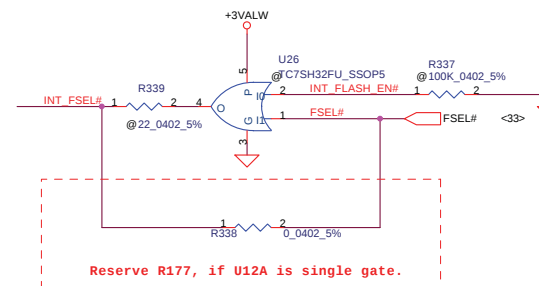
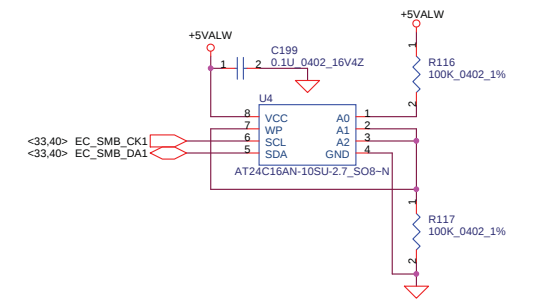
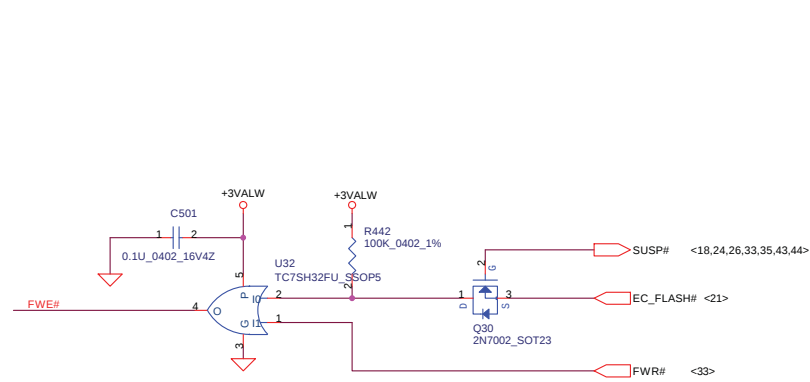
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				Date:	Rev B
				星期三, 七月 12, 2006	Sheet 31 of 47

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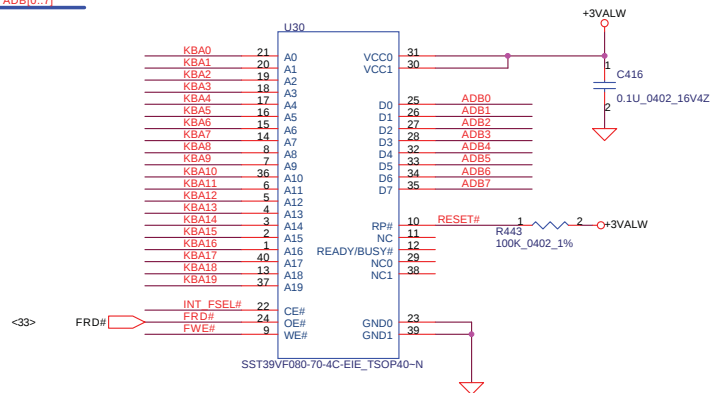
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				401429	Rev B
Date: 星期三, 七月 12, 2006				Sheet	32 of 47



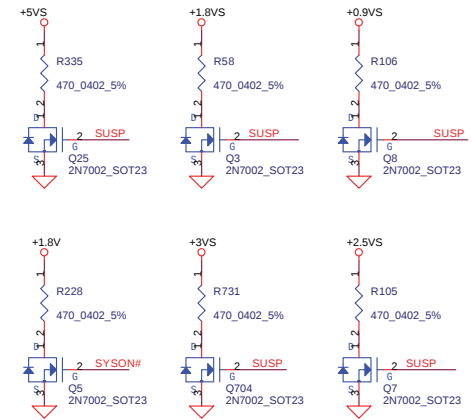
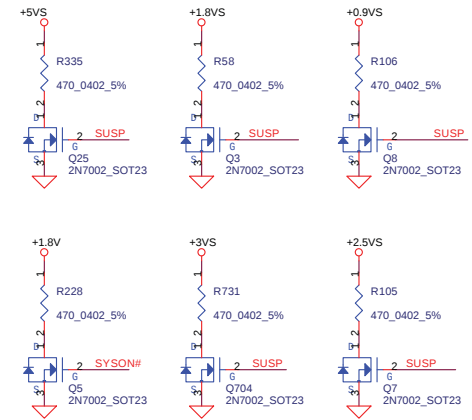
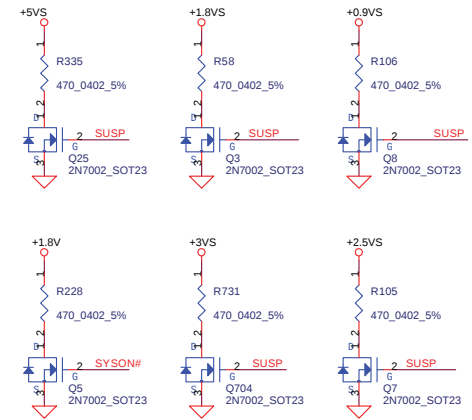
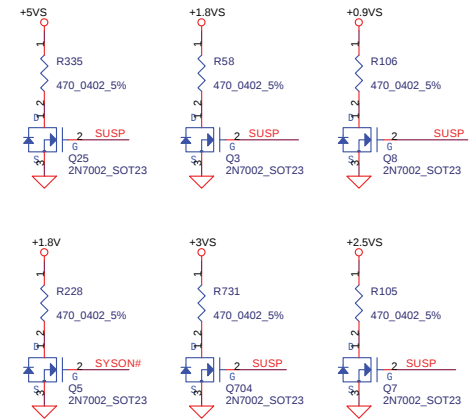
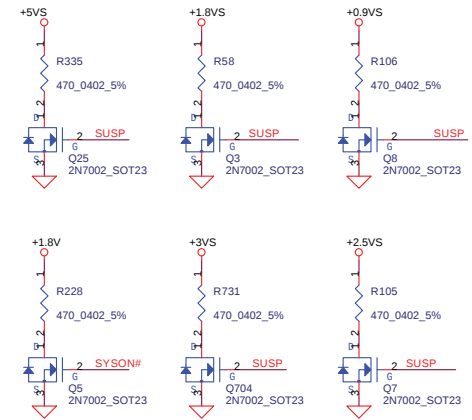
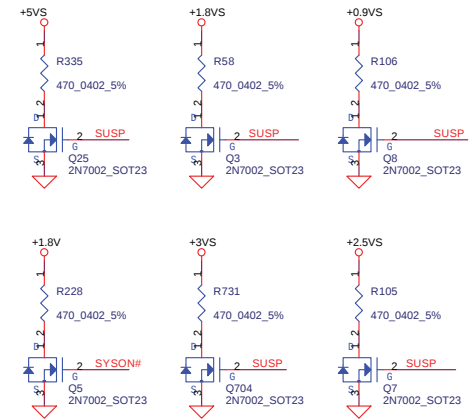
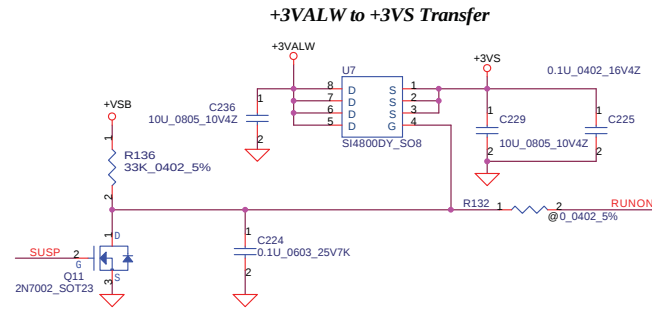
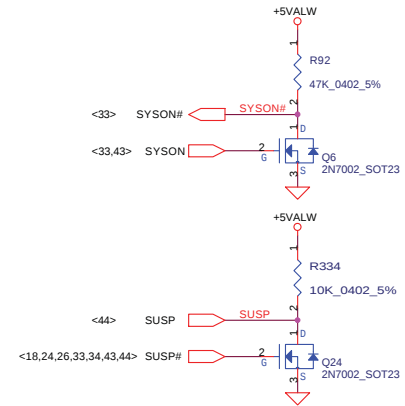
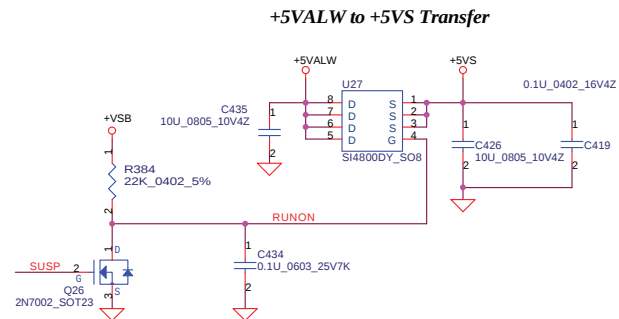


<33> KBA[0..19] KBA[0..19]
<33> ADB[0..7] ADB[0..7]

1MB Flash ROM

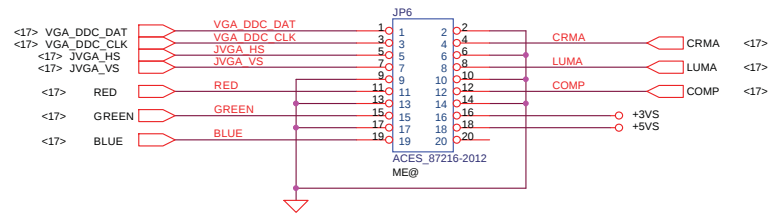


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				Custom	401429	B
				Date:	星期三, 七月 12, 2006	Sheet 34 of 47

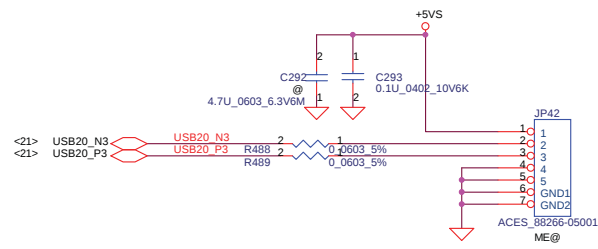


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				401429	Rev B
				Date:	星期三, 十月 12, 2006
				Sheet	35 of 47

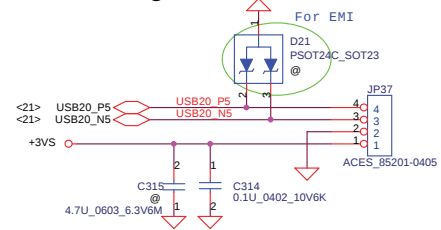
VGA I/O PORT Connector



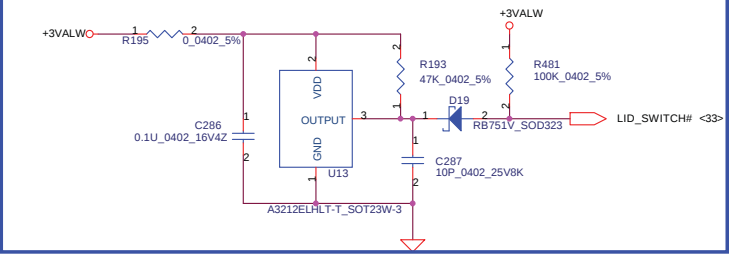
CMOS Camera Conn



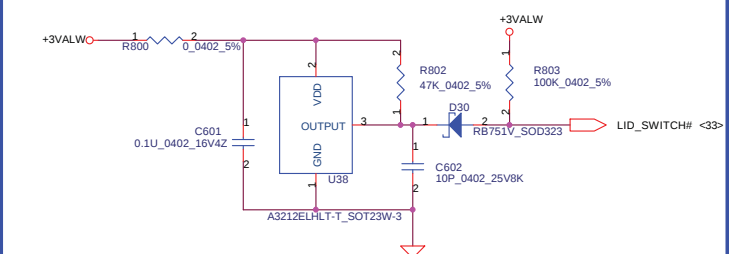
Finger Print board



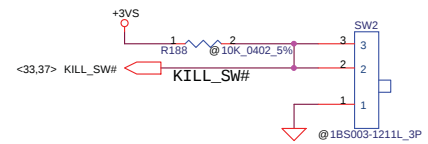
LID Switch (HDL00@)



LID Switch 2 (HDL20@)



Kill Switch



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Size		Document Number		Rev	
Custom		401429		B	
Date		星期三, 七月 12, 2006		Sheet 36 of 47	

[illegible]

INST ON & LED

INST ON & LED

Pinout diagram for INST ON & LED:

- Pin 12: INT_MIC
- Pin 11: WIRELESS_LED#
- Pin 10: BTONLED
- Pin 9: SUSP_LED#
- Pin 8: CHARGE_LED0#
- Pin 7: CHARGE_LED1#
- Pin 6: KILL_SW#
- Pin 5: +3VS
- Pin 4: +3VALW
- Pin 3: GND
- Pin 2: GND
- Pin 1: GND

ACES_85202-1205
ME@

Front LEDs (HDL00@)

The schematic diagram illustrates the wiring for the front LEDs (HDL00@). It shows five LED pins connected to a +3VSW and +3VALW supply. Each LED pin is connected to a resistor (R190, R194, R191, R192, R189) and then to the +3VSW supply. The LEDs are labeled HT-110UYG-CT_YEL/GRN, HT-110UYG-CT_YEL/GRN, HT-110UYG-CT_YEL/GRN, HT-210UD/UYG_AMB/GRN, and HT-210UD/UYG_AMB/GRN. The pins are labeled 1, 2, and 3. The +3VSW and +3VALW supplies are connected to the LEDs. The +3VSW supply is connected to the LEDs. The +3VALW supply is connected to the LEDs.

WIRELESS_LED#

<28> WIRELESS_LED# 2 R190 1 200_0402_5% 1 D6 HT-110UYG-CT_YEL/GRN 2 +3VSW

BTONLED

<28> BTONLED 2 R194 1 200_0402_5% 1 D7 HT-110UYG-CT_YEL/GRN 2 +3VSW

SUSP_LED#

<33> SUSP_LED# 2 R191 1 200_0402_5% 1 D8 HT-110UYG-CT_YEL/GRN 2 +3VSW

CHARGE_LED0#

<33> CHARGE_LED0# 1 R192 2 200_0402_5% 2 D5 HT-210UD/UYG_AMB/GRN 1 +3VALW

CHARGE_LED1#

<33> CHARGE_LED1# 1 R189 2 200_0402_5% 3 HT-210UD/UYG_AMB/GRN 1 +3VALW

Physical Layout

The physical layout shows the placement of the LEDs on the PCB. The LEDs are labeled KILL, WL, BT, CHARGE, SLP, and MIC1. The KILL LED is a square component, while the others are circular components. The KILL LED is connected to the +3VSW supply. The WL, BT, CHARGE, SLP, and MIC1 LEDs are connected to the +3VALW supply.

PWR ON/OFF SW & LED

PWR ON/OFF SW & LED

+3VALW +3VS

JP29

Pin	Signal
1	+3VALW
2	+3VS
3	AMP_MUTE#
4	VOL_UP#
5	VOL_DOWN#
6	MEDIA#
7	ON/OFFBTN#
8	PWR_LED#
9	INSTANT_ON#
10	NUM_LED#
11	CAPS_LED#
12	DRIVE_LED#
13	
14	

ACES_85202-1405
ME@

+3VS

5V

U20

A B C D E F G H Y

TC7SH08FUF_SS0P5

DRIVE_LED#

+3VS

5V

U20

A B C D E F G H Y

TC7SH08FUF_SS0P5

DRIVE_LED#

T/P Board

The diagram shows a schematic for the T/P Board. A component labeled JP28 is connected to a component labeled ACES_85201-0605. The connections are as follows:

- Pin 1 of JP28 is connected to Pin 1 of ACES_85201-0605.
- Pin 2 of JP28 is connected to Pin 2 of ACES_85201-0605.
- Pin 3 of JP28 is connected to Pin 3 of ACES_85201-0605.
- Pin 4 of JP28 is connected to Pin 4 of ACES_85201-0605.
- Pin 5 of JP28 is connected to Pin 5 of ACES_85201-0605.
- Pin 6 of JP28 is connected to Pin 6 of ACES_85201-0605.

Additionally, there is a +5VS connection to Pin 1 of ACES_85201-0605. The output signals are TP_DATA <33> and TP_CLK <33>.

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UMA LCD/PANEL Conn.

(60 MIL)

JPS

+LCDVDD

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

EDID_CLK_LCD

EDID_DAT_LCD

LVDSAC+

LVDSAC-

LVDSB+

LVDSB-

LVDSB1+

LVDSB1-

LVDSB0+

LVDSB0-

LVDSAC+

LVDSAC-

LVDSB+

LVDSB-

LVDSB1+

LVDSB1-

LVDSB0+

LVDSB0-

GND

ME@ ACES_88107-30001

Audio Jack/USB Conn.

ACES_87213-2000 ME@

INT_MIC

WM-64PCY_2P

+5VALW

U9

G528_S08

OUT

IN

EN#

USB_ON#

USB_OC#2 <21>

USB_OC#4 <21>

+USB_VCCB

C500

@ 1000P_0402_50V7K

+5VALW

U10

G528_S08

OUT

IN

EN#

USB_ON#

USB_OC#6 <21>

+USB_VCCC

R172

0_0402_5%

C273

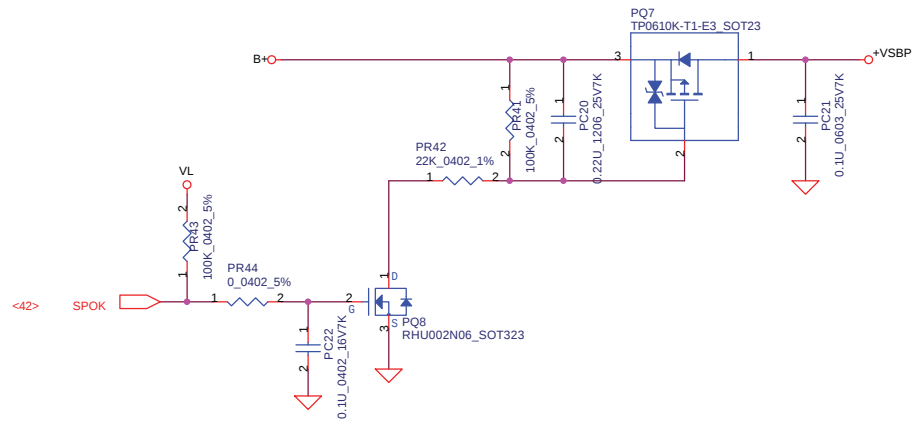
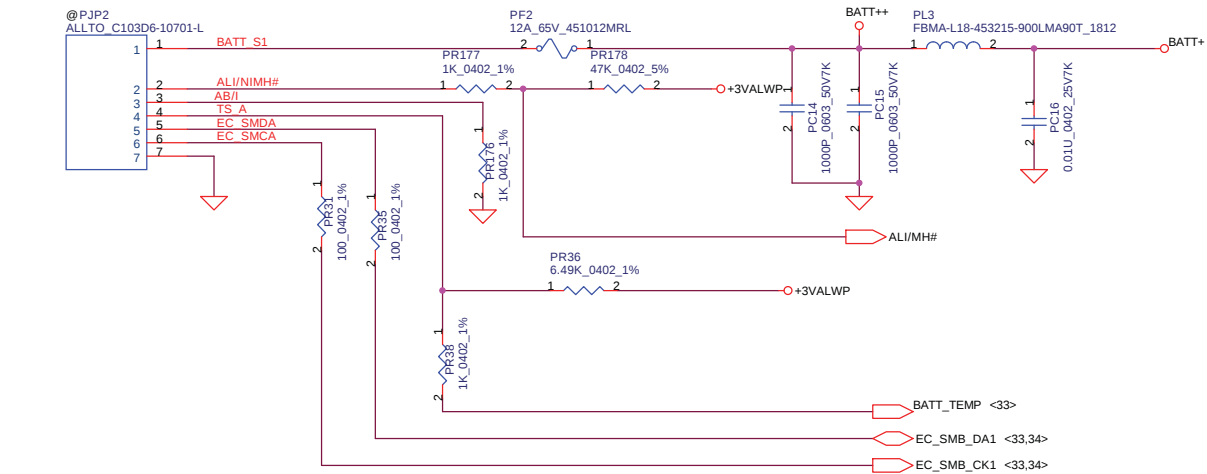
@ 1000P_0402_50V7K

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Deciphered Data	2006/10/06		Title	401429
			Size	Document Number
			Custom	401429
			Date	2006/10/12
			Sheet	27 of 47

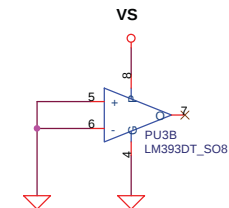
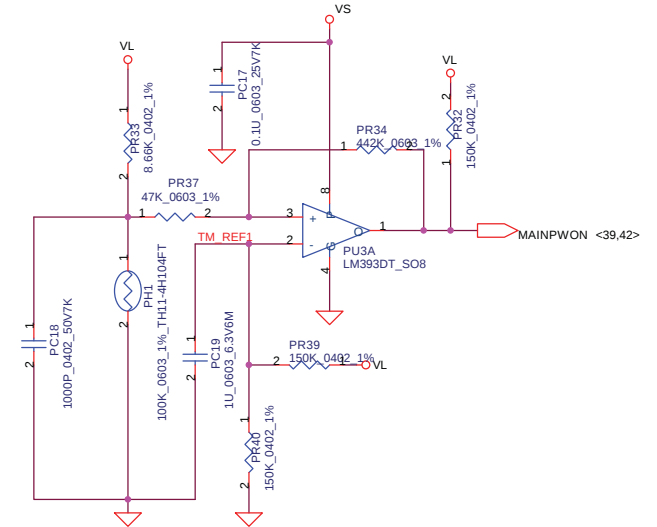
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						Custom	401429		
Date						日期	2006 年 12 月 12 日	Sheet	27 of 47



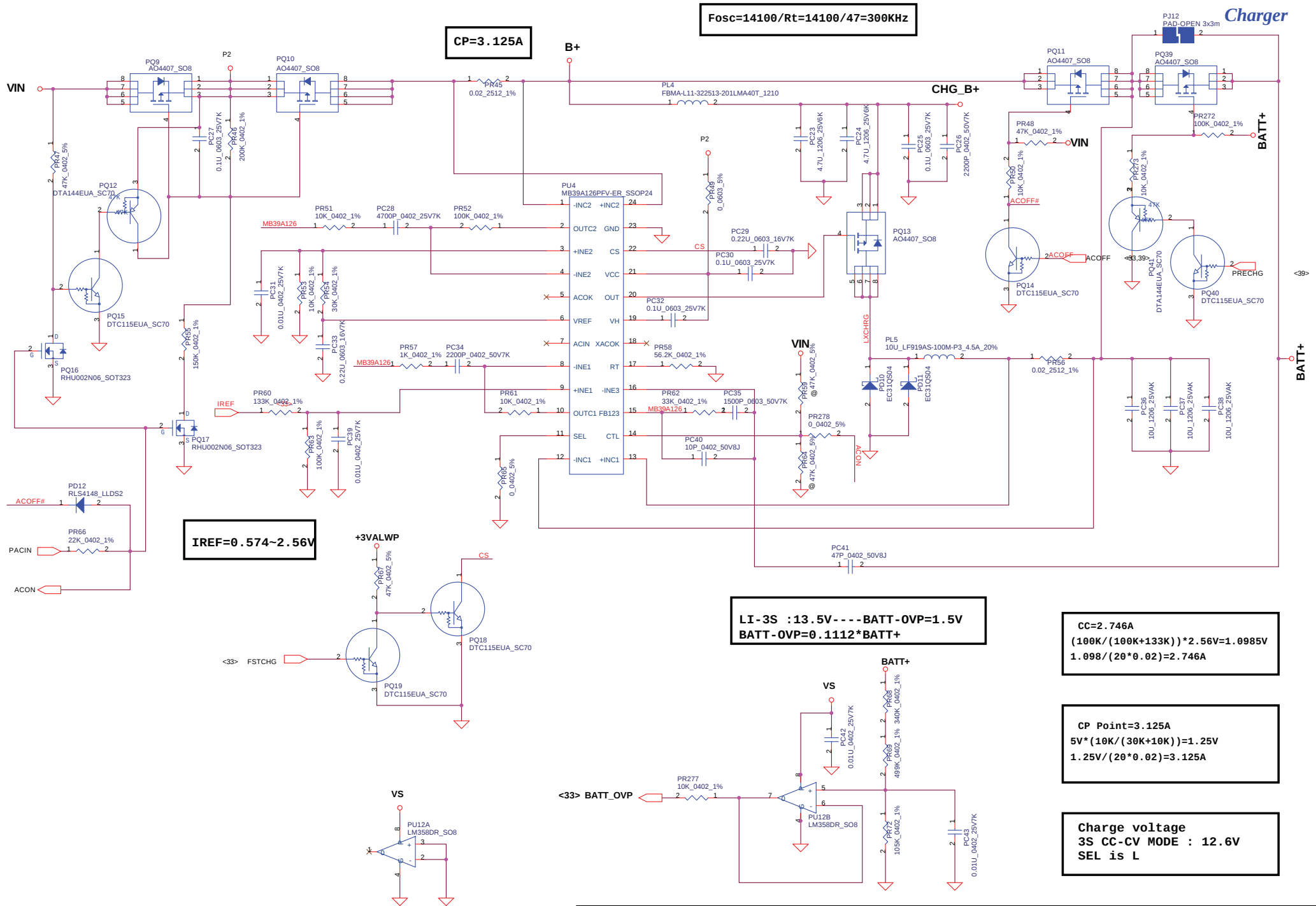
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				Customer	401429
				Date:	星期三, 十月 12, 2006
				Sheet	38 of 47
				Rev	B



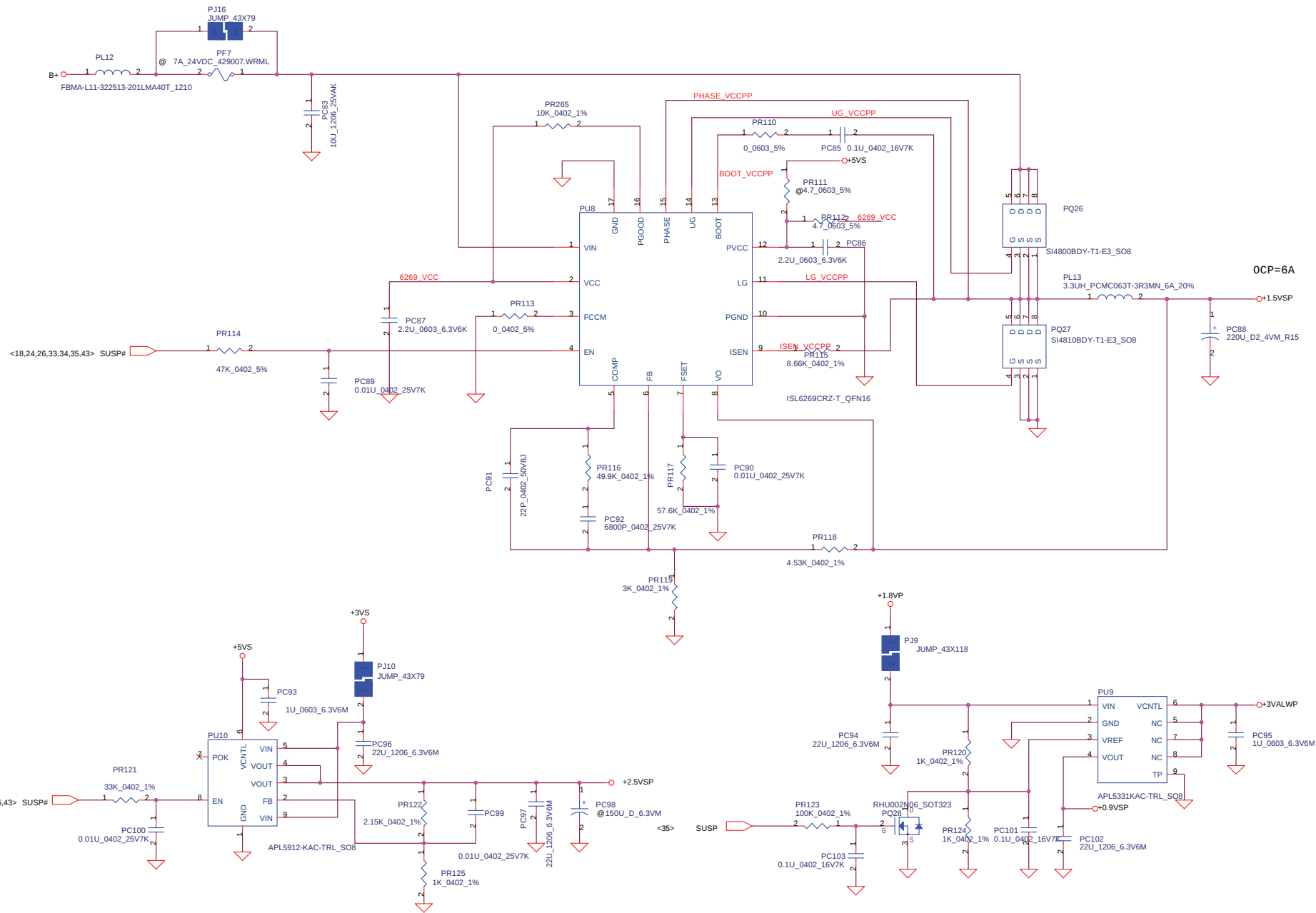
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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				401429	Rev B
Date: 星期三, 七月 12, 2006				Sheet	40 of 47



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				B				401429			
Date				星期三, 七月 12, 2006				Sheet			
				41				of			
				47				Rev			
				B							



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					Size	Document Number	Rev
				401429	B		
Date:					日 期: 七月 12, 2006	Sheet	44 of 47

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Title			
SCHEMATIC, M/B LA-3281			
Size	Document Number		Rev
	401429		B
Date:	星期二, 七月 12, 2006	Sheet	46 of 47

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Version change list (P.I.R. List)

Item	Fixed Issue/Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
A Test						
1	Copy schematic from HDL00					
2	Add 2nd BT connector	0.1	28	Add JP51, C60, Q706, Q705, Q708, R801, R810		
3	Add 2nd LID switch	0.1	36	Add U38, D30, R800, R802, R803, C601, C602		
4	Remove Front LEDs from MB	0.1	37	Del D6, D7, D8, D5, R190, R194, R191, R192, R189		
B Test						
5	Change audio solution from AD1986A to ALC861	0.2	29/30			
6	Add Front LEDs to MB(Reverse HDL00 Design)	0.2	37	Add D6, D7, D8, D5, R190, R194, R191, R192, R189		
C Test						
7	Sloving ICS pin 50, 51 no clock issue	0.3	15	Add R865 to U29.8 and grounded		
8	wake up on USB when AC-IN.	0.3	31, 33, 37	1. Add R866, R867 2. change EC pin 90 from KS017 to EC_GPI04A 3. connect R866, R867 pin2 together, and net name is USB_ON#. 4. change syson# to USB_ON#, and control U9, U10 and U25.		
9	EMI solution	0.3	16	1. change L14 from 0 ohm to bead 300 ohm 2. change C295 from 0.8pF to 470pF		
10						
11						
12						
13						
14						

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Size	Document Number	Rev
	401429	B
Date:	星期三, 七月 12, 2006	Sheet 47 of 47