LZ2 Block Diagram

Project code: 91.4K101.001 ZY LZ2
91.4J301.001 XR LX2
PCB P/N : 08214-1
Revision : -1

CLK GEN. 3

Mobile CPU
Penryn SV 35W
4, 5

EMC2102 07

HOST BUS 800/1066MHz@1.05V

DDR3 socket 15 — 800/1066MHz

DDR3 socket 16 — 800/1066MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13,14

R.G.B → CRT 18

LVDS → 12"W LCD 17

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
12 USB
High Definition Audio
LPC I/F
Serial Peripheral I/F
19,20,21,22,23

INT MIC
SPR x2
Codec ALC269 (include AMP) 25
AZALIA

MIC In
HP

RJ11 — MODEM MDC Card 24

USB → Realtek RTS5158E Cardreader 28 → SD/MMC/MS 3 in 1 28

PCIe → LAN Boardcom 5906M 26 → RJ45 27

PCIe/ USB → Mini Card a/b/g/n 31

LPC BUS → KBC Winbond WPC776 29 (SPI I/F → BIOS 2M byte 34; G-sensor 30; Touch Pad 34; INT. KB 34)

LPC DEBUG CONN. 24

New card 31 — PCI Express / USB

Power switch 31

SATA → SATA-HDD 24

SATA → SATA-ODD 24

USB → Finger Print 32

USB → BlueTooth 24

USB → CAMERA 17

USB → USB 3 Port 32

PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 37	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3

TPS51100 38	
1D5V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
1D5V_S3	33 1D5V_S0

CHARGER BQ24740 39	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V UP+5V 5V 100mA

CPU DC/DC ADP3208 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: LZ2 | Rev: SB
Date: Wednesday, May 28, 2008 | Sheet 1 of 41

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved Rising Edge of PWROK.	This signal has a weak internal pull-down. Note:This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap(Server Only) Rising edge of PWROK	Tying this strap low configures DMI for SIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server latforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG11 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1= The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE1	BroadCom LAN
LANE2	MiniCard WLAN
LANE4	NewCard

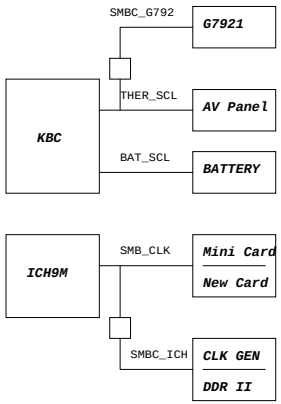
History:

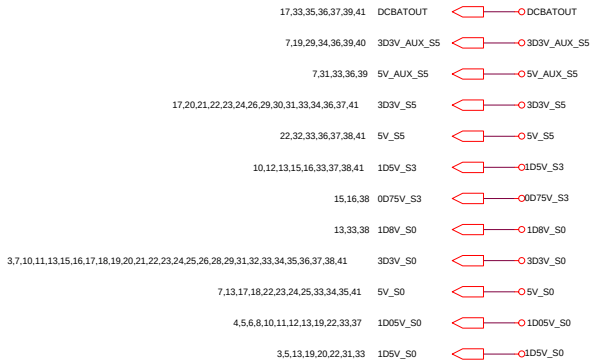
LAB: 2008/01/02

USB Table

USB	
Pair	Device
0	JACK0
1	NC
2	JACK2
3	NC
4	BLUETOOTH
5	JACK1
6	Fringer Print
7	Mini Card
8	CAMERA
9	NEW CARD
10	CARDREADER
11	NC

SMBus





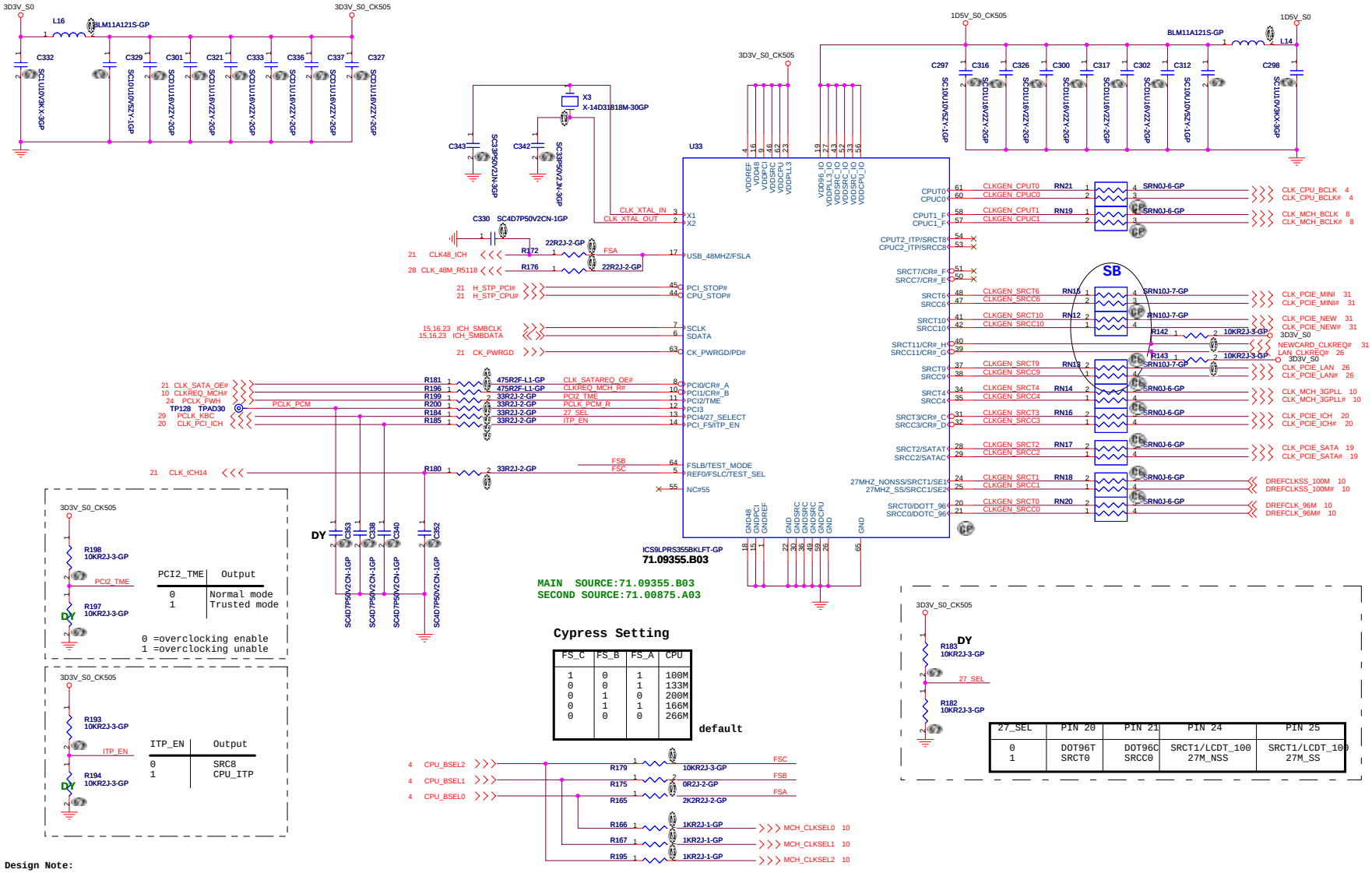
<Variant Name>

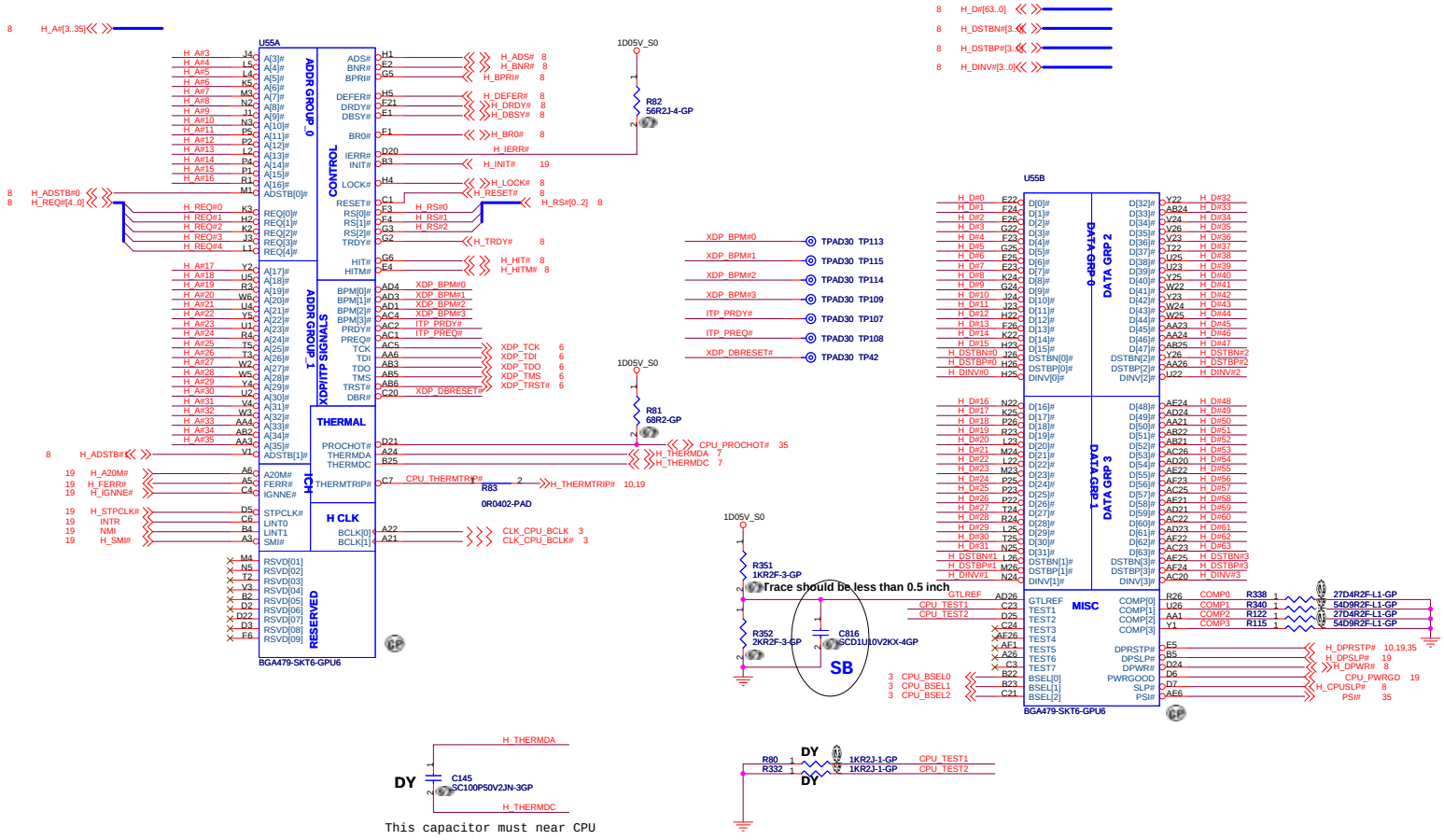
蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size	Document Number	Rev
C	LZ2	SB

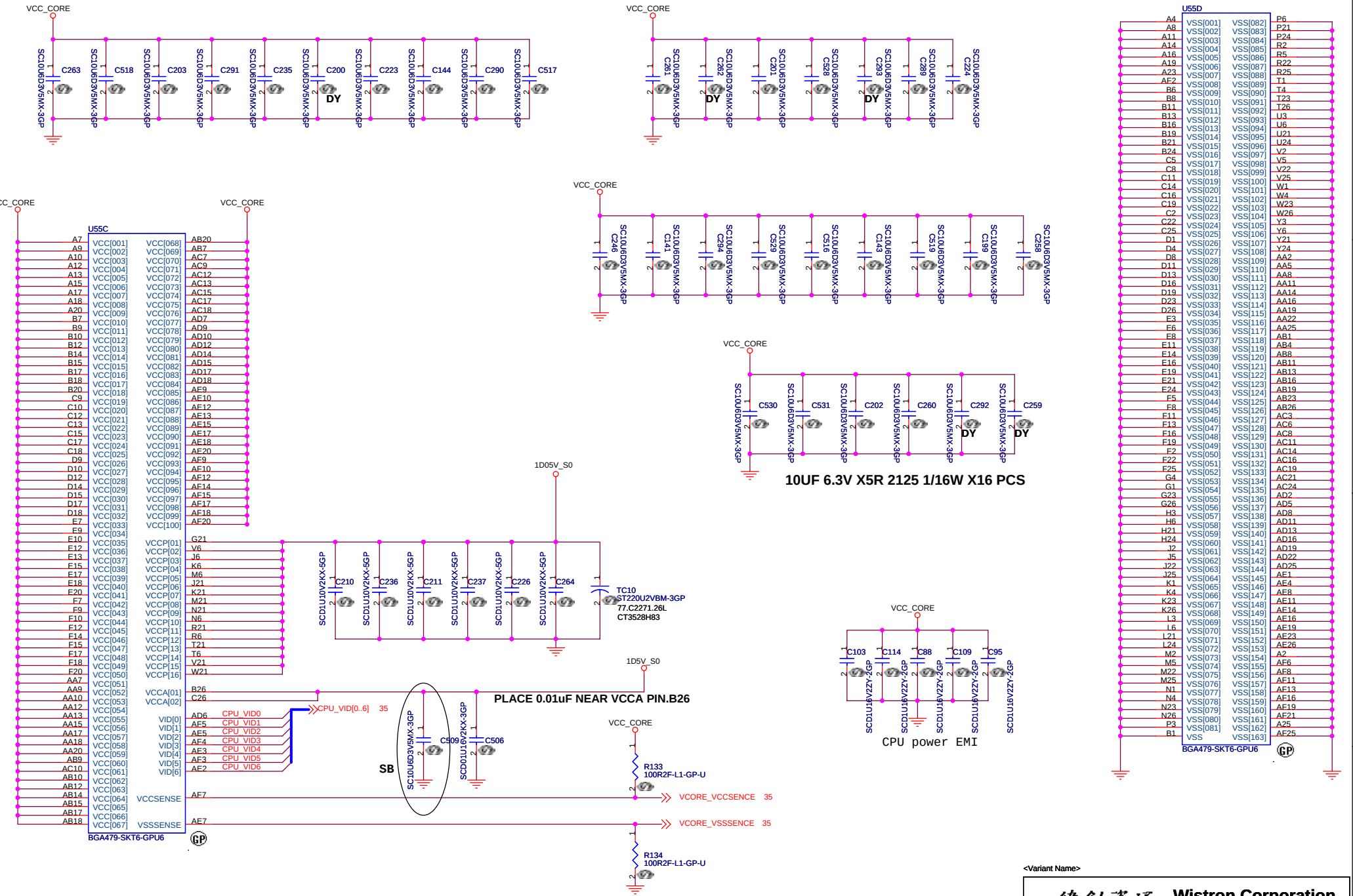
Date: Thursday, June 05, 2008 Sheet 2 of 41


3D3V_S0
3D3V_S0_CK505
1D5V_S0_CK505
1D5V_S0
L16
BLM11A121S-GP
L14
X3
X-14D31818M-30GP
U33
ICS9LPRS355BKLFT-GP
71.09355.B03
MAIN SOURCE:71.09355.B03
SECOND SOURCE:71.00875.A03
SB
DY
CLK_XTAL_IN
CLK_XTAL_OUT
USB_48MHZ/FSLA
PCI_STOP#
CPU_STOP#
SCLK
SDATA
CK_PWRGD/PD#
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
PCI2_TME
PCI2_TME | Output
0 | Normal mode
1 | Trusted mode
0 =overclocking enable
1 =overclocking unable
ITP_EN
ITP_EN | Output
0 | SRC8
1 | CPU_ITP
27_SEL
27_SEL | PIN 20 | PIN 21 | PIN 24 | PIN 25
0 | DOT96T | DOT96C | SRCT1/LCDT_100 27M_NSS | SRCT1/LCDT_100 27M_SS
1 | SRCT0 | SRCC0
Cypress Setting
FS_C | FS_B | FS_A | CPU
1 | 0 | 1 | 100M
0 | 0 | 1 | 133M
0 | 1 | 0 | 200M
0 | 1 | 1 | 166M
0 | 0 | 0 | 266M
default
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size
Document Number
LZ2
Rev
SB
Date: Thursday, June 05, 2008
Sheet 3 of 41



<variant_name>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Penryn CPU(1/2)		
Size: C	Document Number: LZ2	Rev: SB
Date: Thursday, June 05, 2008	Sheet 4 of 41	



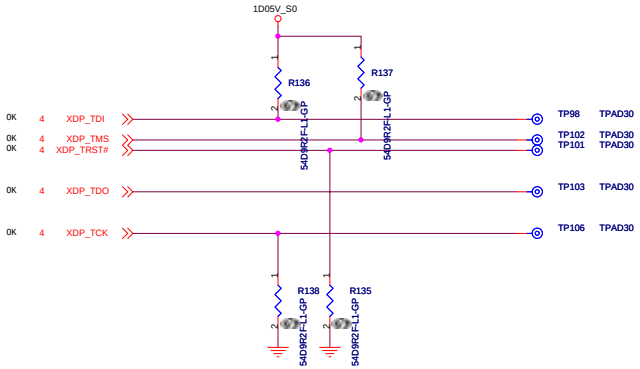
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(2/2)

Size	Document Number	Rev
A3	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 5 of 41



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ITP CONN*

Size	Document Number	Rev
C	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 6 of 41

Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing

Layout notice :
Both H_THERMDA_1 and THERMDC_1 routing
10 mil trace width and 10 mil spacing

Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing

Layout notice :
C809, C811, C812
close to chip side;

CPU0

SYSTEM

This cap should close to thermal diode.

Layout 15 mil

SC

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)

220ms delay time after Power-on

Dummy when G792 enhanced T8 function

HW thermal shut down tempature
setting 95 degree . Put Near CPU .

Rset=0.0012*T^2-0.9308*T+96.147

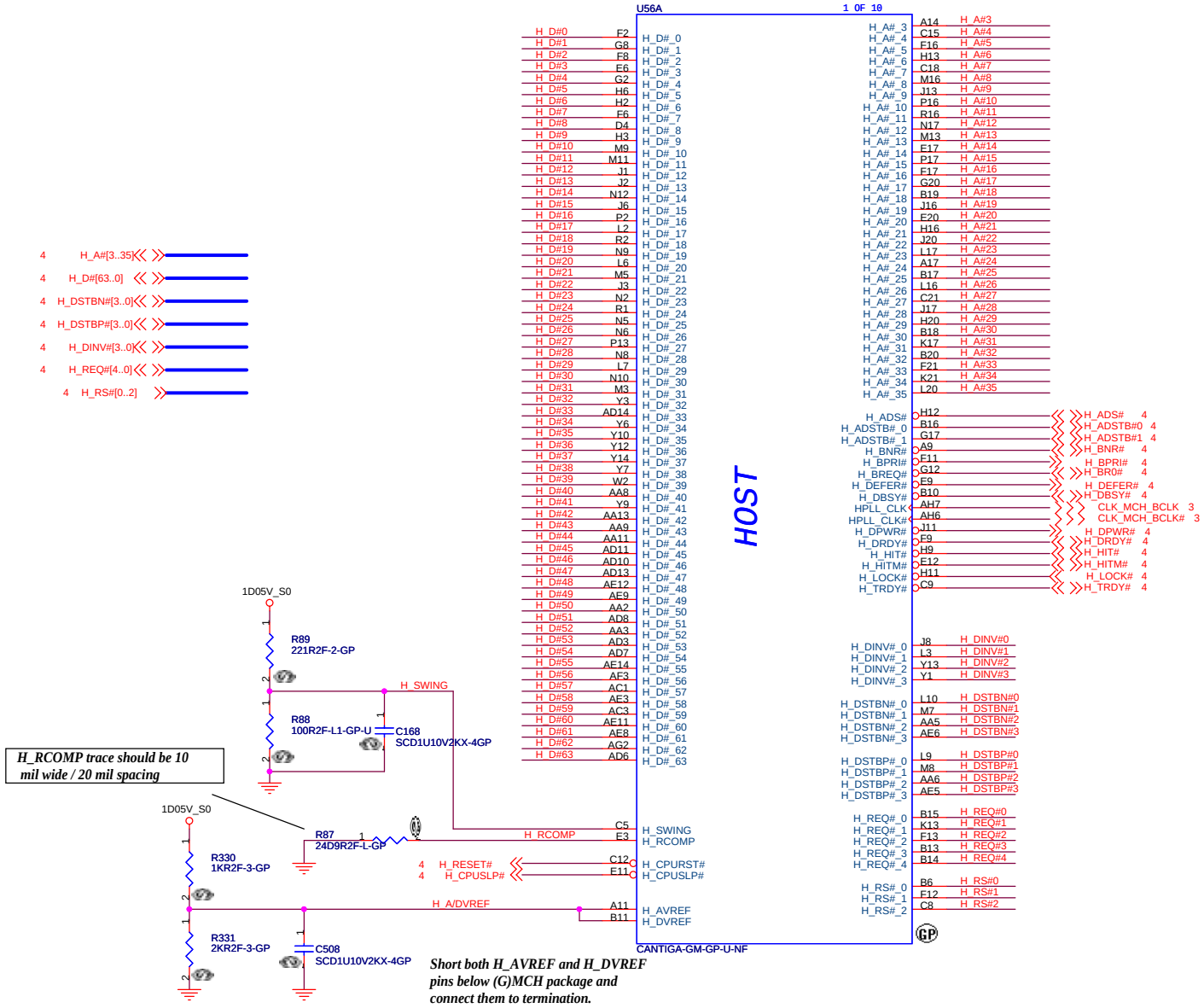
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: LZ2 | Rev: SB

Date: Thursday, June 05, 2008 | Sheet 7 of 41



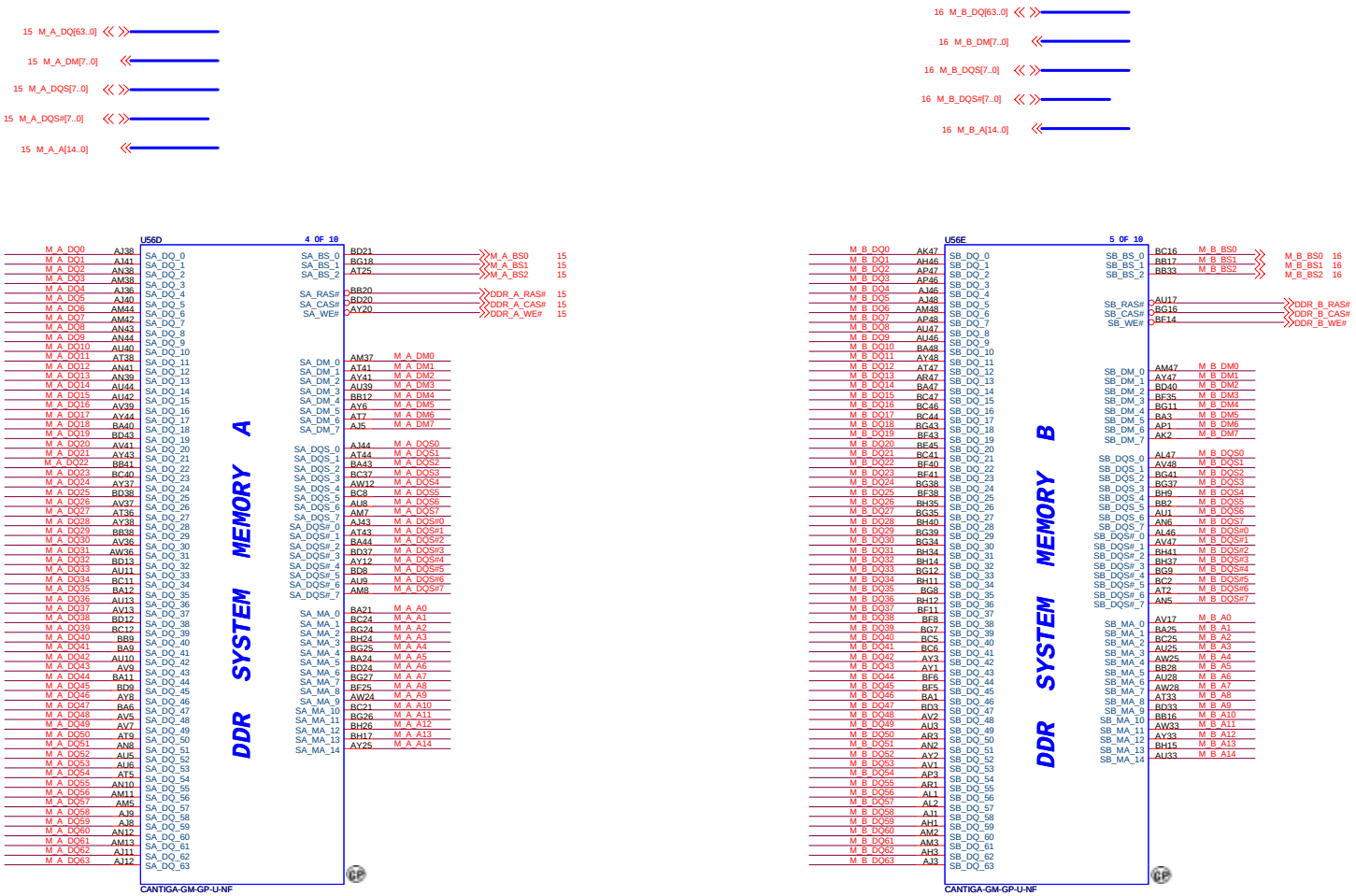
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga(1/7):HOST I/F**

Size	Document Number	Rev
A3	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 8 of 41



<variant_name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(2/7):DDR3

Size	Document Number	Rev
C	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 9 of 41

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown

U56B — 2 OF 10 — CANTIGA-GM-GP-U-NF

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA

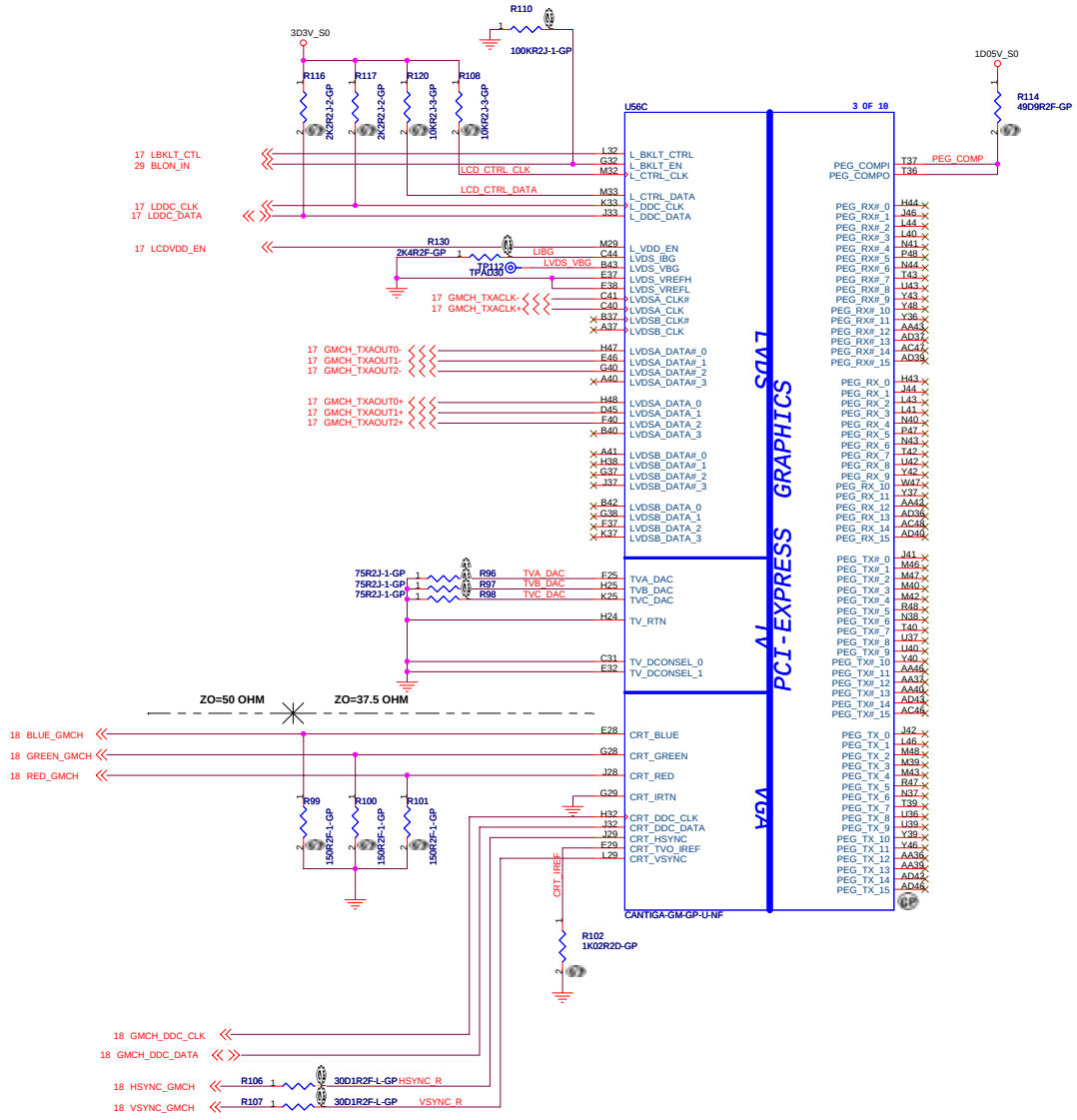
SM_REXT:Constant circuit reference for clocks.

INTEL Suggest use 511

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(3/7):DMI/PM/CFG/GF
Size: C | Document Number: LZ2 | Rev: SB
Date: Thursday, June 05, 2008 | Sheet 10 of 41



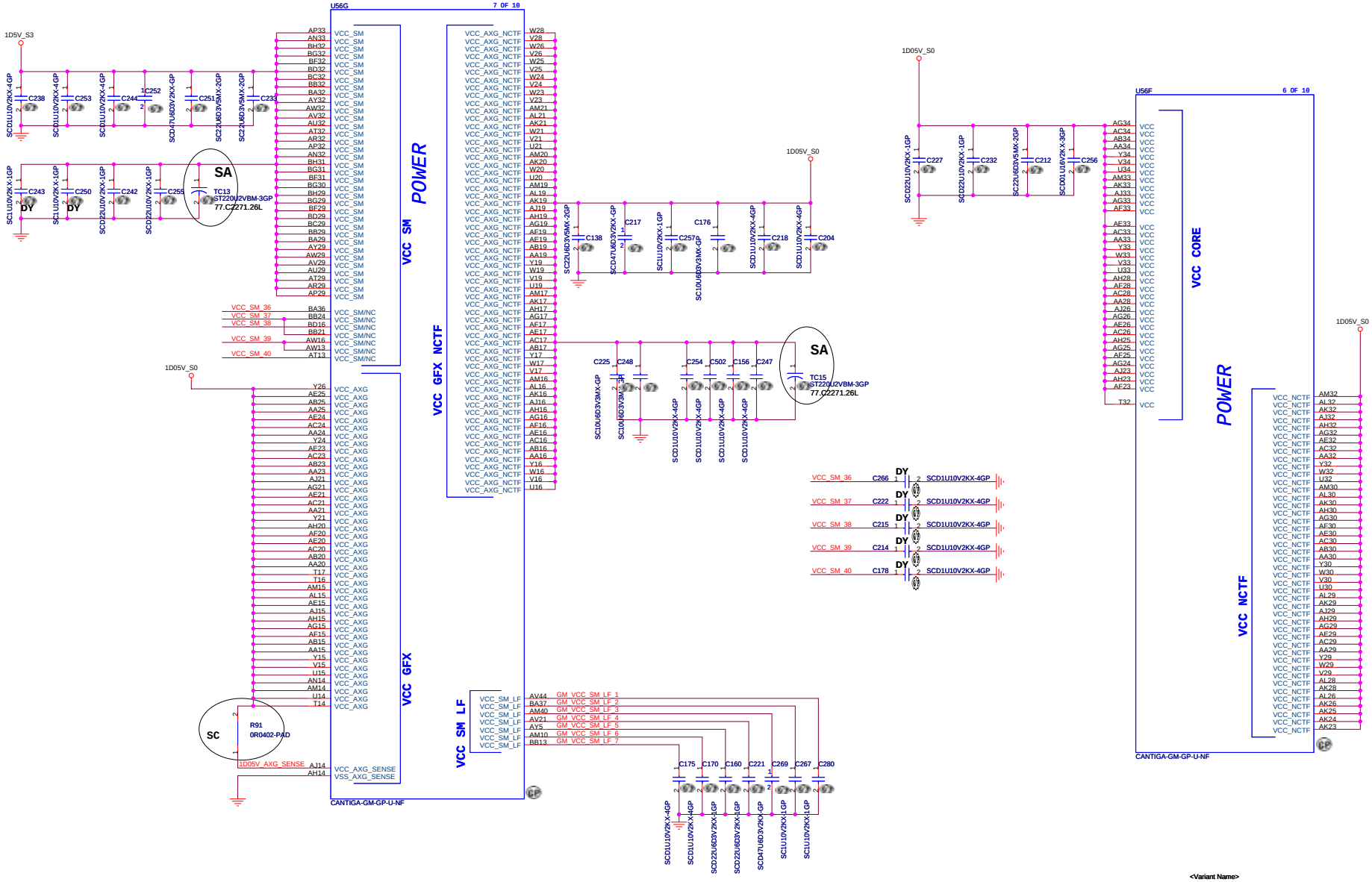
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CANTIGA(5/7)-VGA/LVDS

Size	Document Number	Rev
C	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 11 of 41



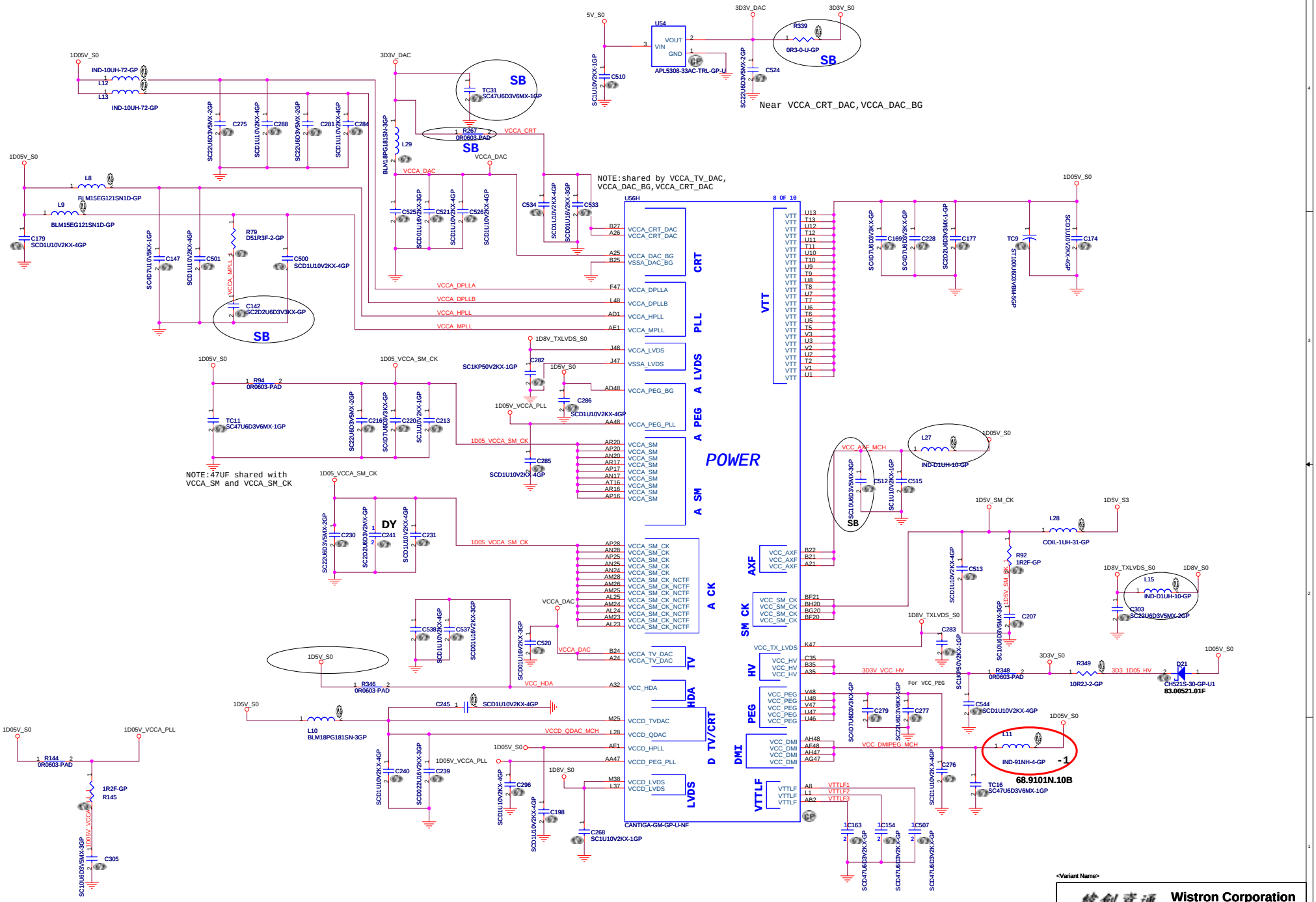
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(5/7):VCC

Size	Document Number	Rev
C	LZ2	SB

Date: Friday, April 11, 2008 Sheet 12 of 41



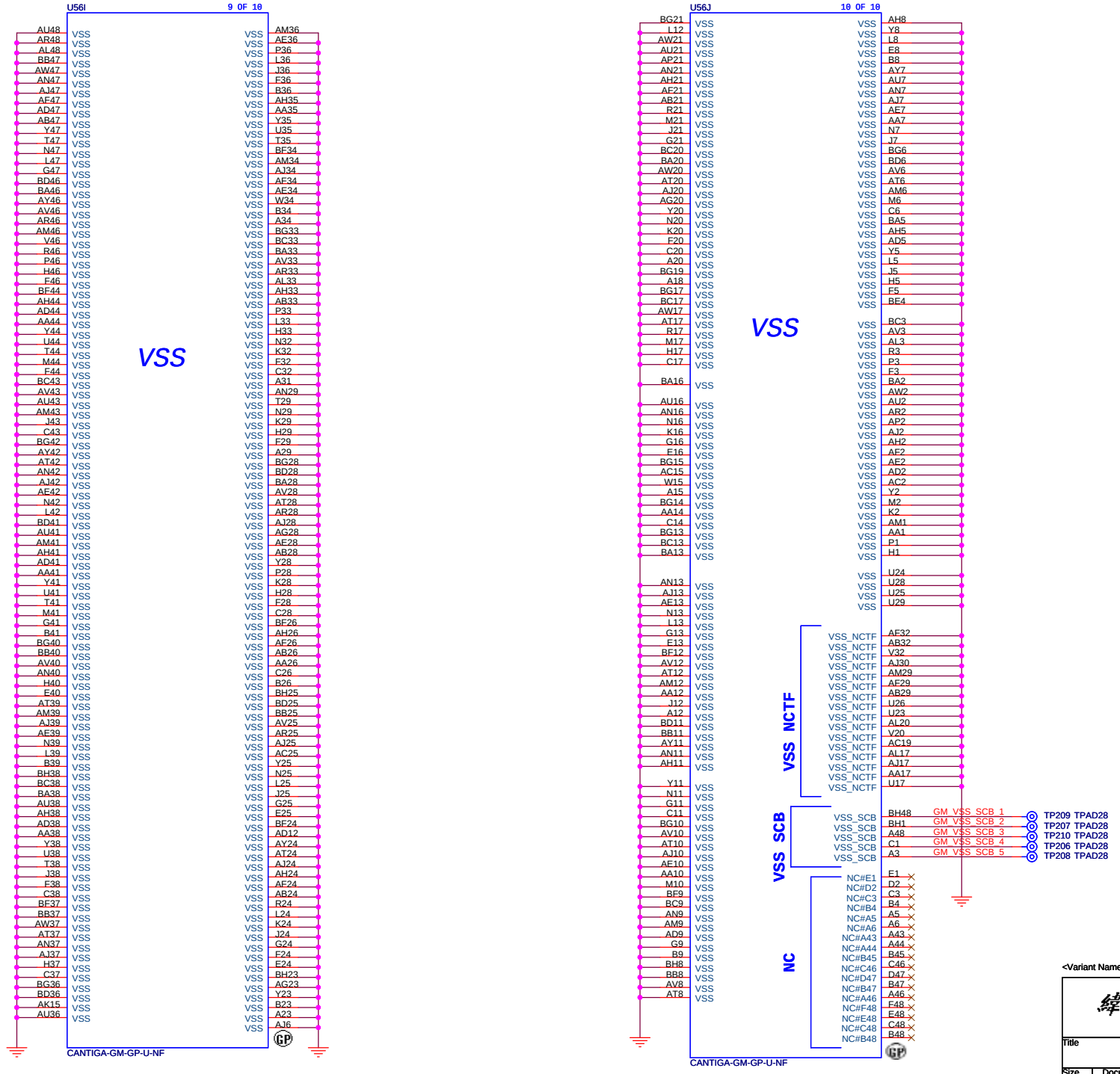
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: Cantiga(6/7):VCC

Size: C | Document Number: LZ2 | Rev: SB

Date: Wednesday, June 04, 2008 | Sheet 13 of 41



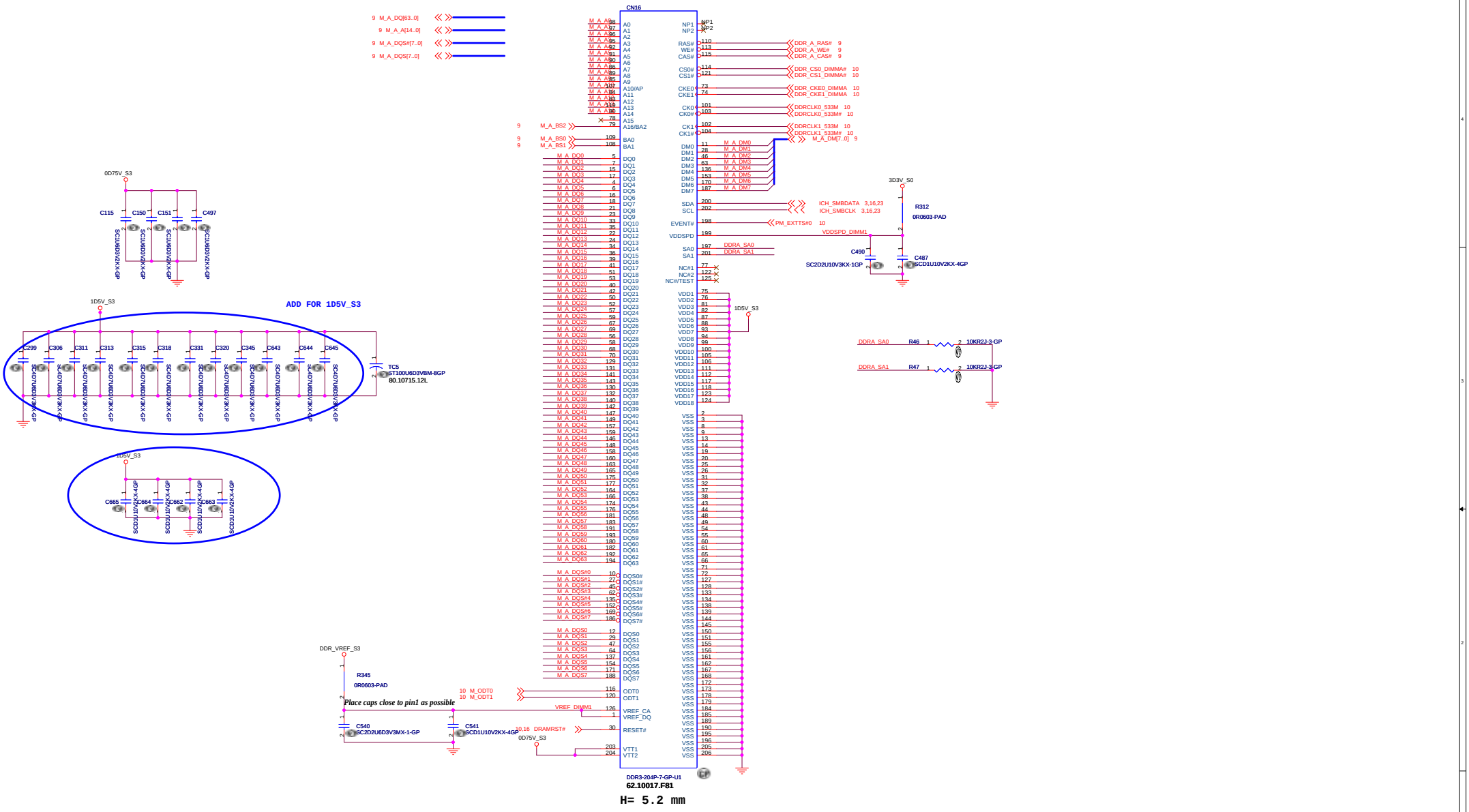
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga(8/7):GND**

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 09, 2008 Sheet 14 of 41



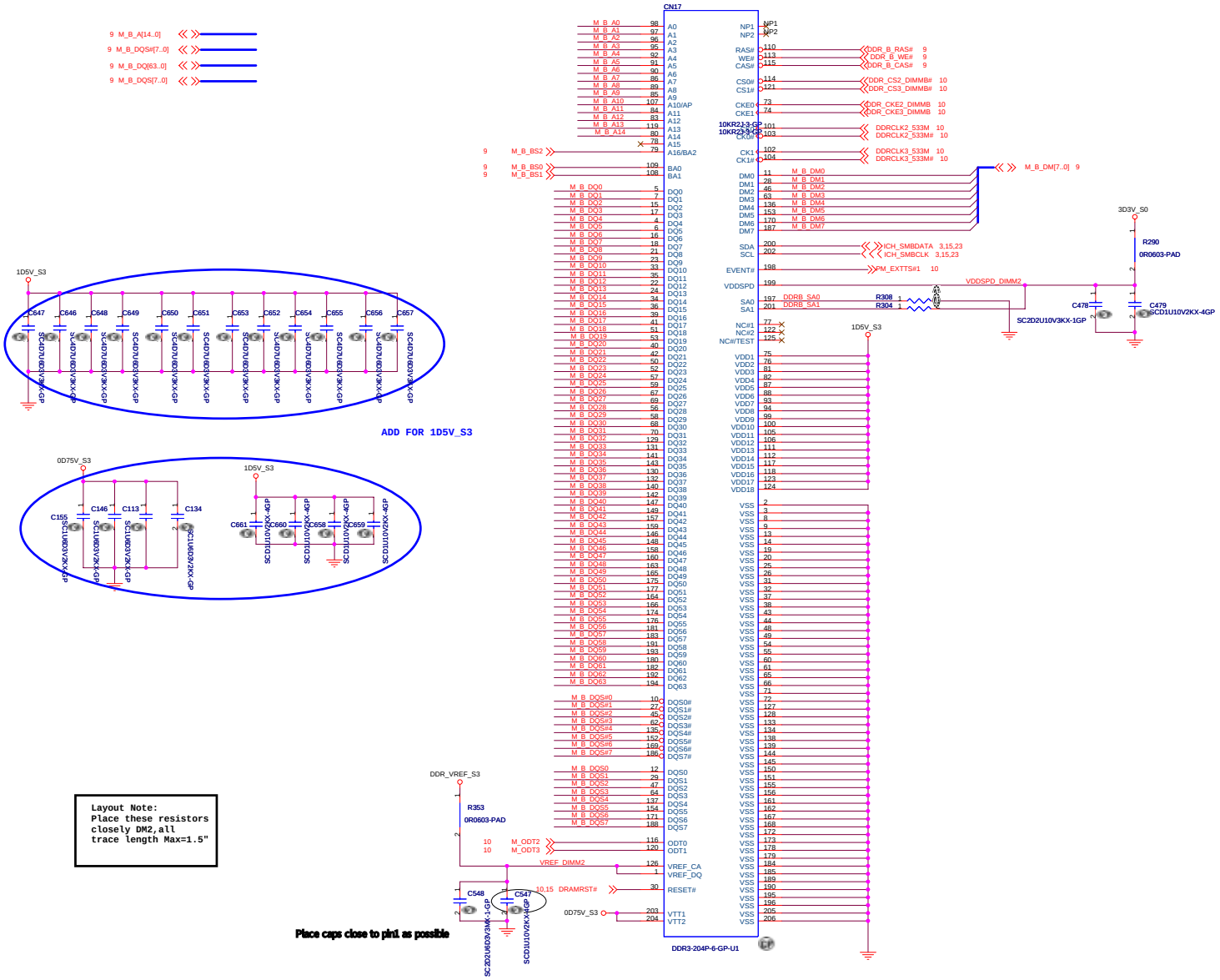
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-A (NORMAL TYPE)

Size	Document Number	Rev
A2	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 15 of 41



<Variant Name>

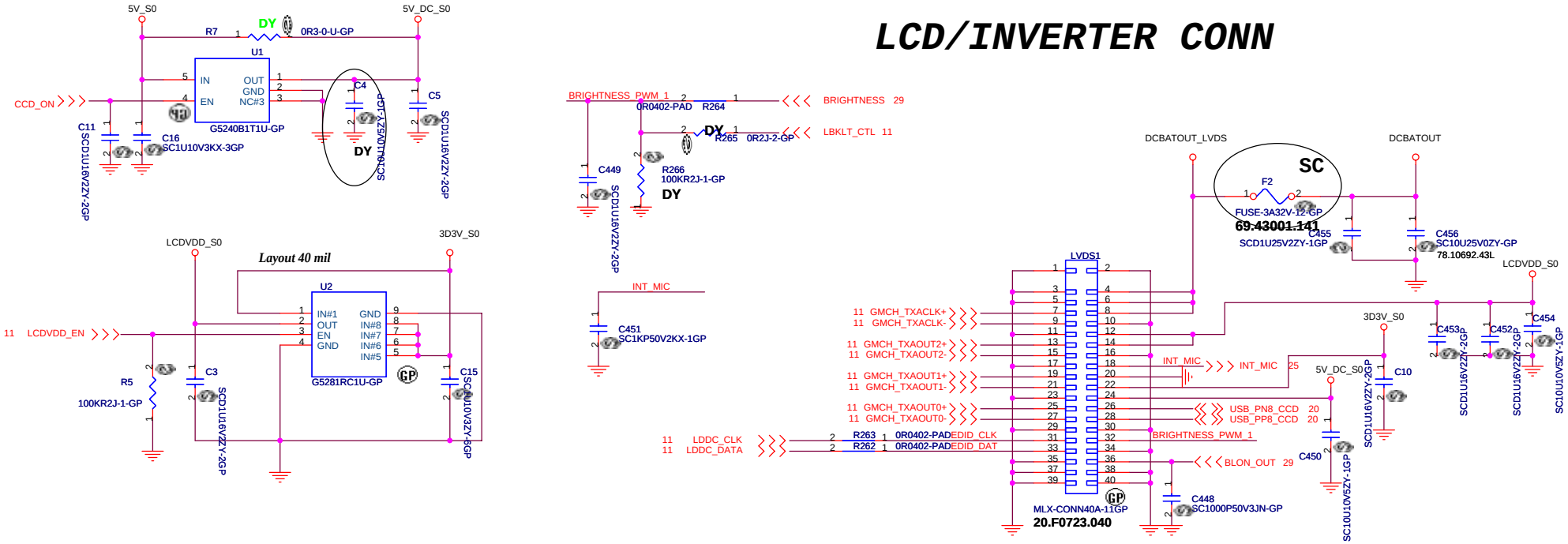
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-B (REVERSE TYPE)

Size	Document Number	Rev
A2	LZ2	SB

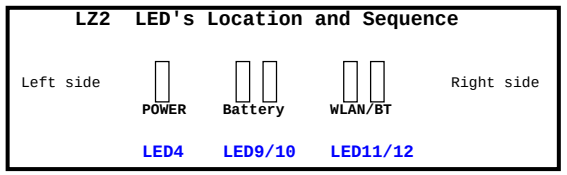
Date: Thursday, June 05, 2008 Sheet 16 of 41

LCD/INVERTER CONN



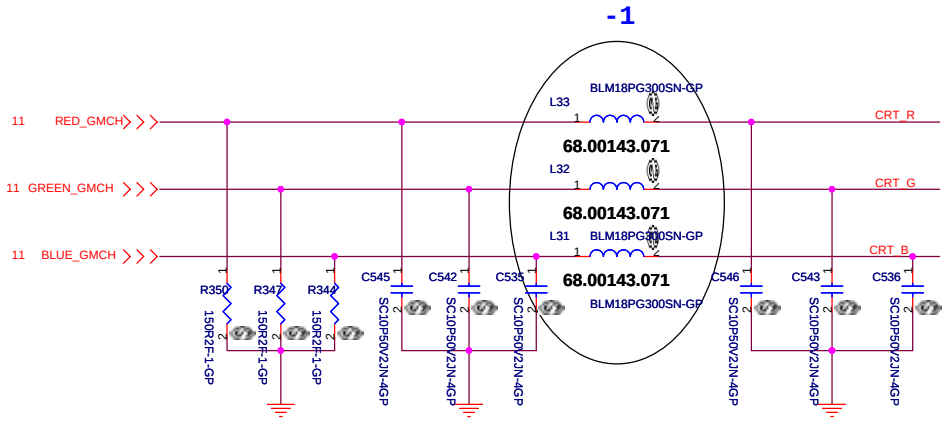
M/B LED

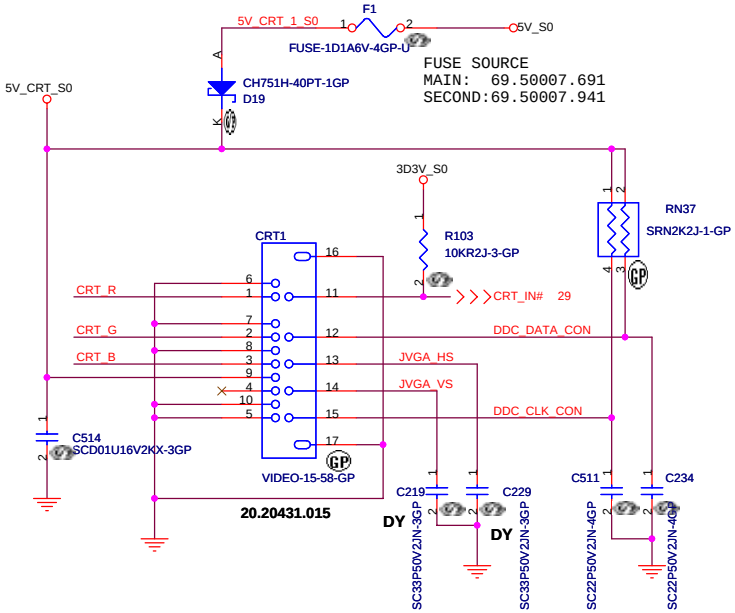
LZ2 LED's Location and Sequence

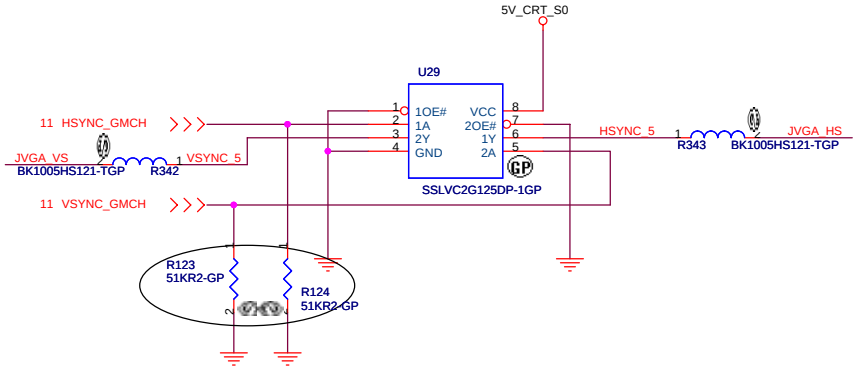


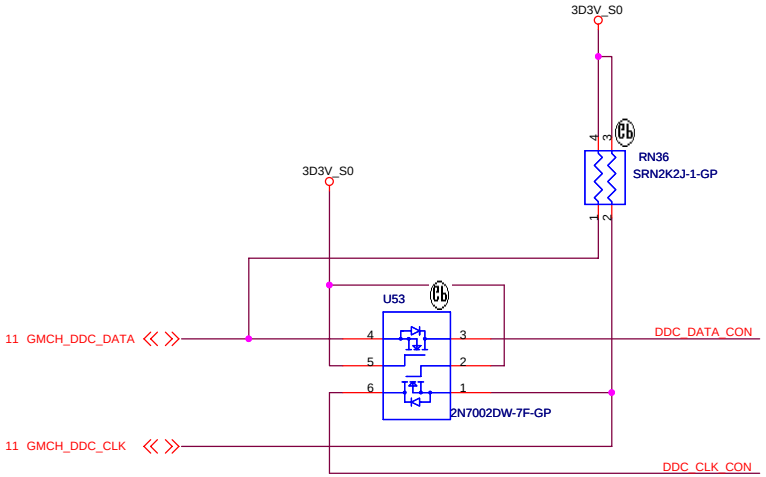
BOM1

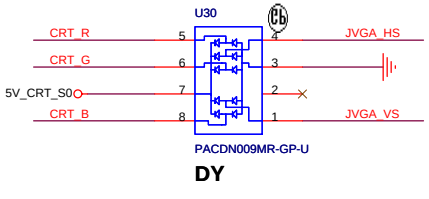
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*LCD CONN & CAMERA & DIG-MIC*
Size / Document Number	LZ2
Rev	SB
Date: Thursday, June 05, 2008	Sheet 17 of 41

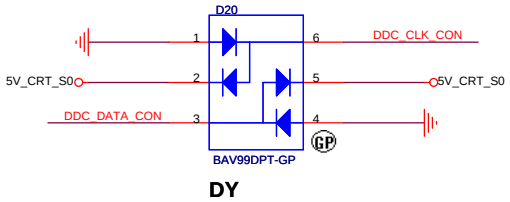










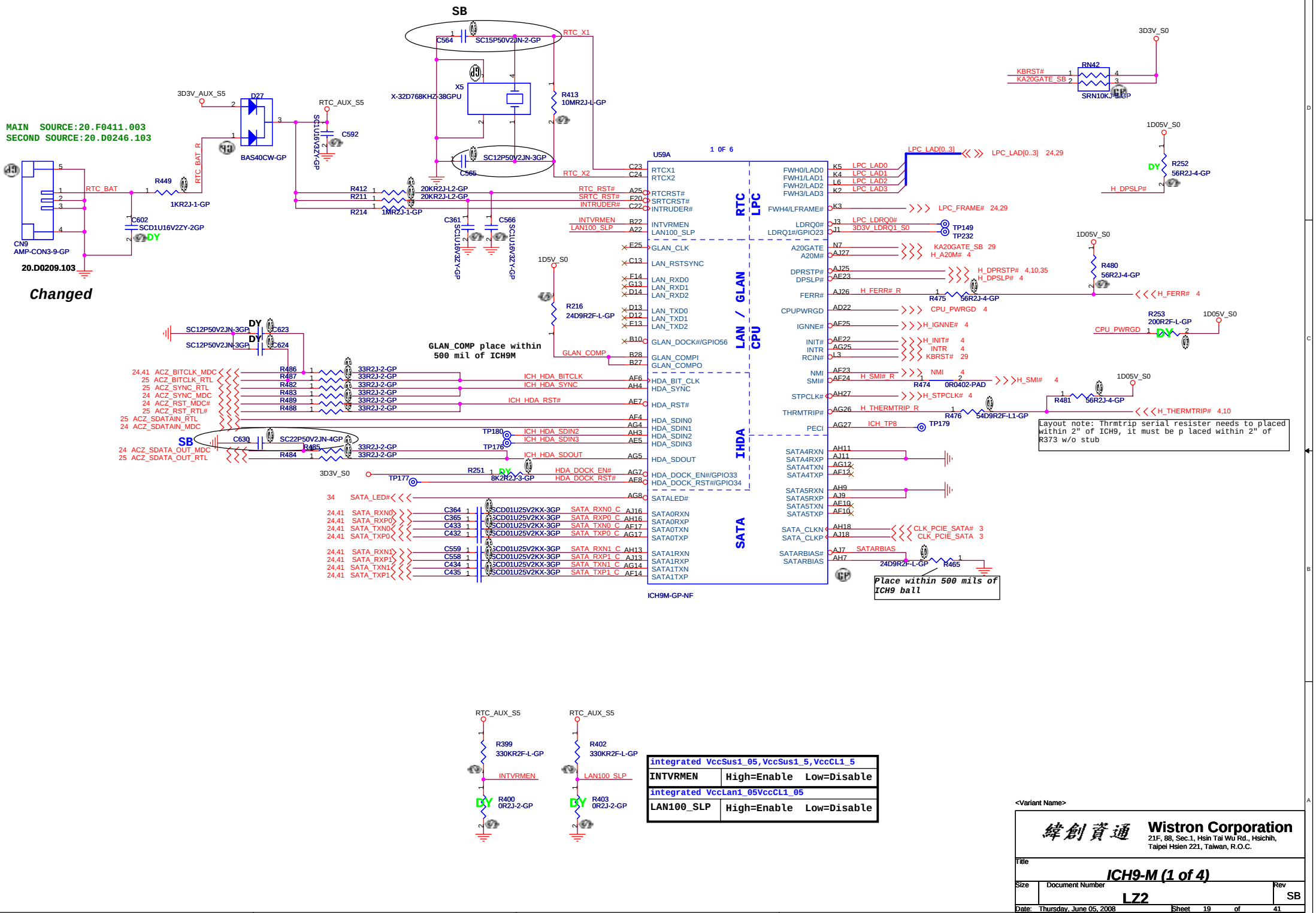


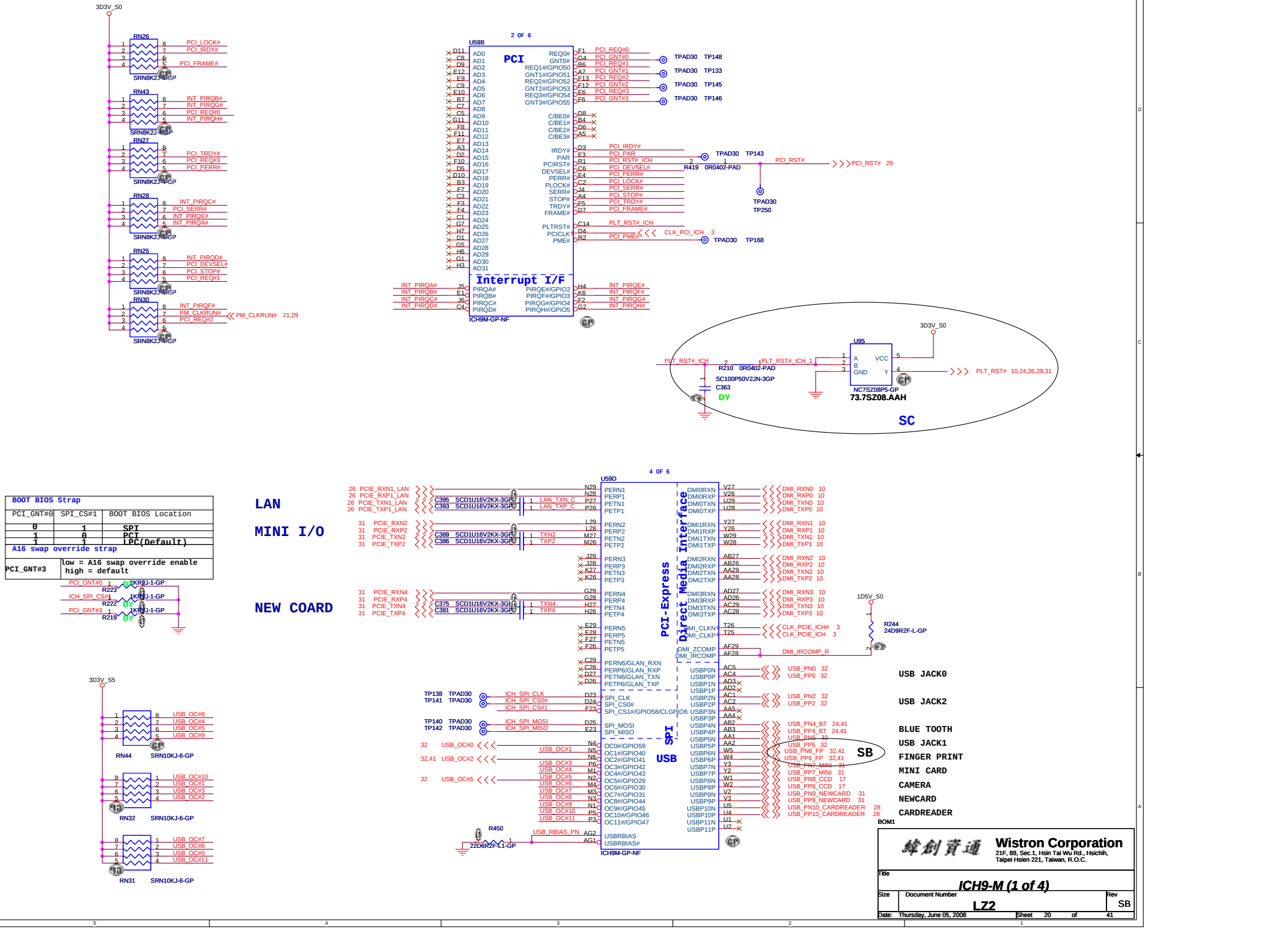
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

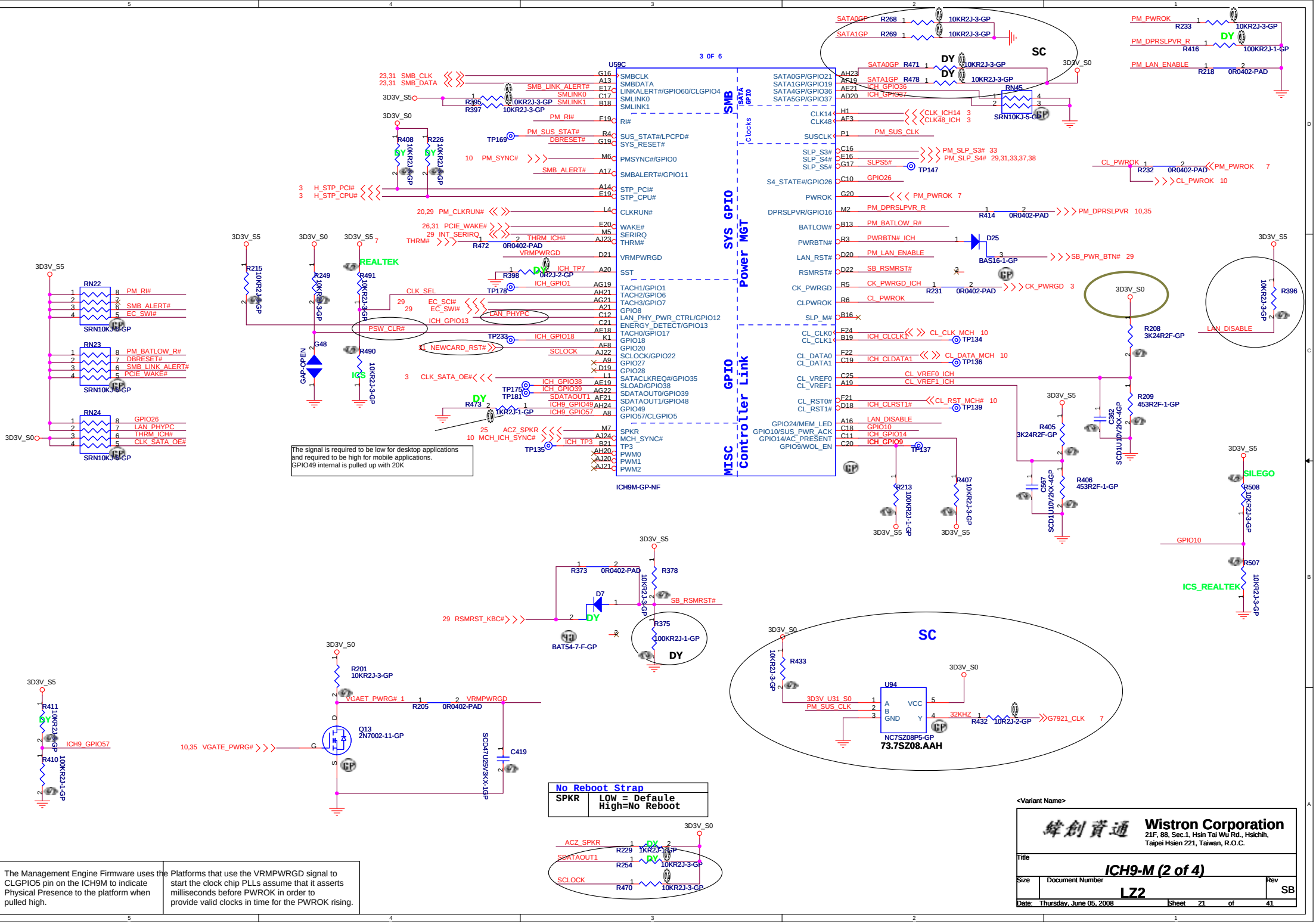
Title: CRT/TV Connector

Size | Document Number: LZ2 | Rev: SB

Date: Thursday, June 05, 2008 | Sheet 18 of 41


SB
MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103
20.D0209.103
Changed
U59A
1 OF 6
ICH9M-GP-NF
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: Thrmtrip serial resister needs to placed within 2" of ICH9, it must be p laced within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
LZ2
SB
Thursday, June 05, 2008
Sheet 19 of 41


3D3V_S0
RN26
PCI_LOCK#
PCI_IRDY#
PCI_FRAME#
SRN8K2J-1-GP
RN43
INT_PIRQB#
INT_PIRQG#
PCI_REQ#0
INT_PIRQH#
RN27
PCI_TRDY#
PCI_REQ#3
PCI_PERR#
RN28
INT_PIRQC#
PCI_SERR#
INT_PIRQE#
INT_PIRQA#
RN25
INT_PIRQD#
PCI_DEVSEL#
PCI_STOP#
PCI_REQ#1
RN30
INT_PIRQF#
PM_CLKRUN#
PCI_REQ#2
PM_CLKRUN# 21,29
2 OF 6
U59B
PCI
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
REQ0#
GNT0#
REQ1#/GPIO50
GNT1#/GPIO51
REQ2#/GPIO52
GNT2#/GPIO53
REQ3#/GPIO54
GNT3#/GPIO55
C/BE0#
C/BE1#
C/BE2#
C/BE3#
IRDY#
PAR
PCIRST#
DEVSEL#
PERR#
PLOCK#
SERR#
STOP#
TRDY#
FRAME#
PLTRST#
PCICLK
PME#
PCI_REQ#0
PCI_GNT#0
PCI_REQ#1
PCI_GNT#1
PCI_REQ#2
PCI_GNT#2
PCI_REQ#3
PCI_GNT#3
TPAD30 TP148
TPAD30 TP133
TPAD30 TP145
TPAD30 TP146
PCI_IRDY#
PCI_PAR
PCI_RST# ICH
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
TPAD30 TP143
R419 0R0402-PAD
PCI_RST#
PCI_RST# 29
TPAD30 TP250
PLT_RST# ICH
CLK_PCI_ICH 3
PCI_PME#
TPAD30 TP168
Interrupt I/F
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
ICH9M-GP-NF
3D3V_S0
U95
PLT_RST# ICH
PLT_RST#_ICH_1
R210 0R0402-PAD
SC100P50V2JN-3GP
C363
DY
A
B
GND
VCC
Y
NC7SZ08P5-GP
73.7SZ08.AAH
PLT_RST# 10,24,26,29,31
SC
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
PCI_GNT#0 R223 1KR2J-1-GP
ICH_SPI_CS#1 R222 DY 1KR2J-1-GP
PCI_GNT#3 R219 DY 1KR2J-1-GP
LAN
MINI I/O
NEW COARD
4 OF 6
U59D
PCI-Express
Direct Media Interface
SPI
USB
26 PCIE_RXN1_LAN
26 PCIE_RXP1_LAN
26 PCIE_TXN1_LAN
26 PCIE_TXP1_LAN
C395 SCD1U16V2KX-3GP
C393 SCD1U16V2KX-3GP
LAN_TXN_C
LAN_TXP_C
31 PCIE_RXN2
31 PCIE_RXP2
31 PCIE_TXN2
31 PCIE_TXP2
C389 SCD1U16V2KX-3GP
C386 SCD1U16V2KX-3GP
TXN2
TXP2
31 PCIE_RXN4
31 PCIE_RXP4
31 PCIE_TXN4
31 PCIE_TXP4
C375 SCD1U16V2KX-3GP
C381 SCD1U16V2KX-3GP
TXN4
TXP4
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_RXN0 10
DMI_RXP0 10
DMI_TXN0 10
DMI_TXP0 10
DMI_RXN1 10
DMI_RXP1 10
DMI_TXN1 10
DMI_TXP1 10
DMI_RXN2 10
DMI_RXP2 10
DMI_TXN2 10
DMI_TXP2 10
DMI_RXN3 10
DMI_RXP3 10
DMI_TXN3 10
DMI_TXP3 10
CLK_PCIE_ICH# 3
CLK_PCIE_ICH 3
1D5V_S0
R244 24D9R2F-L-GP
DMI_IRCOMP_R
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO
TP138 TPAD30 ICH_SPI_CLK
TP141 TPAD30 ICH_SPI_CS0#
ICH_SPI_CS1#
TP140 TPAD30 ICH_SPI_MOSI
TP142 TPAD30 ICH_SPI_MISO
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USB_PN0 32
USB_PP0 32
USB_PN2 32
USB_PP2 32
USB_PN4_BT 24,41
USB_PP4_BT 24,41
USB_PN5 32
USB_PP5 32
USB_PN6_FP 32,41
USB_PP6_FP 32,41
USB_PN7_MINI 31
USB_PP7_MINI 31
USB_PN8_CCD 17
USB_PP8_CCD 17
USB_PN9_NEWCARD 31
USB_PP9_NEWCARD 31
USB_PN10_CARDREADER 28
USB_PP10_CARDREADER 28
SB
USB JACK0
USB JACK2
BLUE TOOTH
USB JACK1
FINGER PRINT
MINI CARD
CAMERA
NEWCARD
CARDREADER
BOM1
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9
USB_OC#10
USB_OC#11
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47
32 USB_OC#0
32,41 USB_OC#2
32 USB_OC#5
R450 22D6R2F-L1-GP
USB_RBIAS_PN
USB_RBIAS#
USBRBIAS
USBRBIAS#
ICH9M-GP-NF
3D3V_S5
RN44 SRN10KJ-6-GP
RN32 SRN10KJ-6-GP
RN31 SRN10KJ-6-GP
USB_OC#8
USB_OC#4
USB_OC#5
USB_OC#9
USB_OC#10
USB_OC#1
USB_OC#3
USB_OC#2
USB_OC#7
USB_OC#6
USB_OC#0
USB_OC#11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
LZ2
Rev
SB
Date: Thursday, June 05, 2008
Sheet 20 of 41


U59C
3 OF 6
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
SC
REALTEK
ICS
SILEGO
GAP-OPEN
The signal is required to be low for desktop applications and required to be high for mobile applications.
GPIO49 internal is pulled up with 20K
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
The Management Engine Firmware uses the CLGPIO5 pin on the ICH9M to indicate Physical Presence to the platform when pulled high.
Platforms that use the VRMPWRGD signal to start the clock chip PLLs assume that it asserts milliseconds before PWROK in order to provide valid clocks in time for the PWROK rising.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
LZ2
Rev
SB
Date: Thursday, June 05, 2008
Sheet 21 of 41

6 OF 6

U59F

VccRTC=6uA in G3

Vcc1_5_B=646mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

V5REF=2mA

V5REF_Sus=2mA

VccSATAPLL=47mA

Vcc1_5_A=1.342A

USBPLL=11mA

VccLAN3_3=19mA

VccGLANPLL=23mA

VccGLAN1_5=80mA

VccGLAN3_3=1mA

Vcc1_05=1.634A

Layout Note:Place near ICH9M

VccDMIPLL=23mA

VccDMI=48mA

V_CPU_IO=2mA

VCC3_3=308mA

VccHDA=11mA

VccSusHDA=11mA

VccSus3_3=212mA

VccCL3_3=19mA

VccLAN3_3=19mA in S0;78mA in S3/S4/S5,The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.

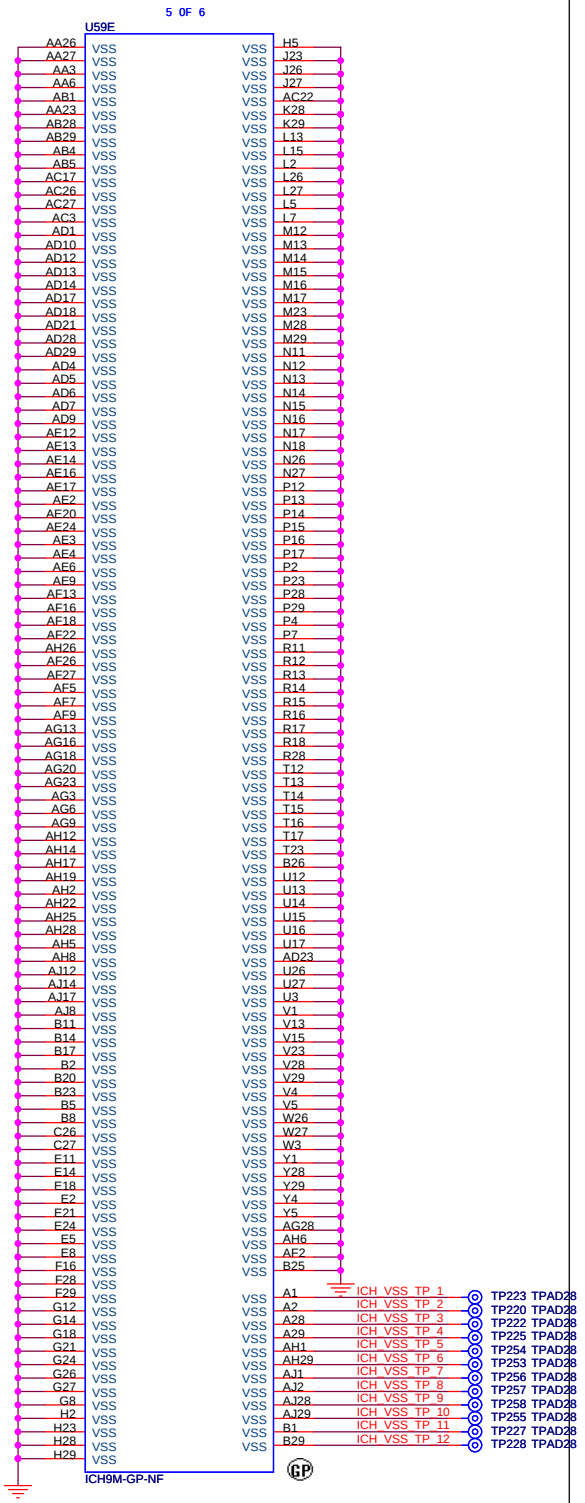
ICH9M-GP-NF

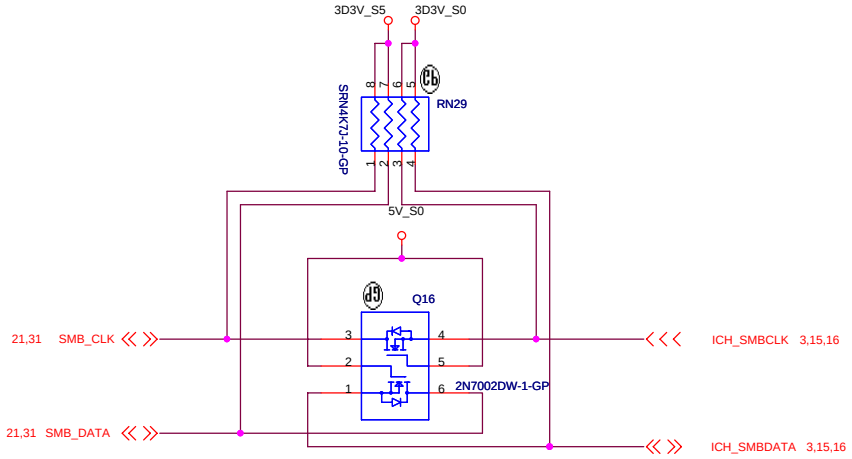
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (3 of 4)

Size | Document Number: LZ2 | Rev: SB

Date: Thursday, May 29, 2008 | Sheet 22 of 41



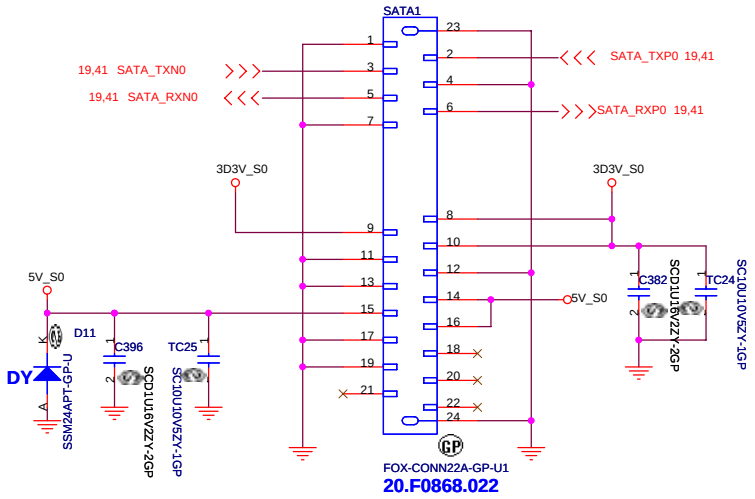


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

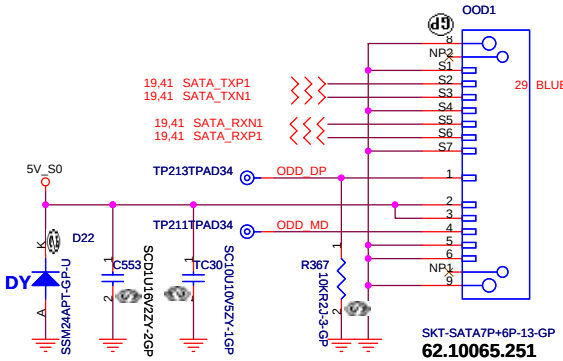
SMBUS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ICH9-M (4 of 4)*		
Size	Document Number: LZ2	Rev: SB
Date: Thursday, June 05, 2008	Sheet 23 of 41	

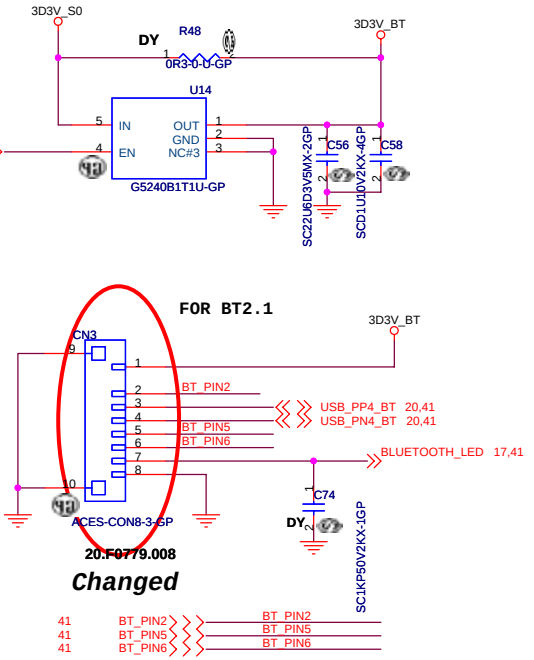
SATA HD Connector



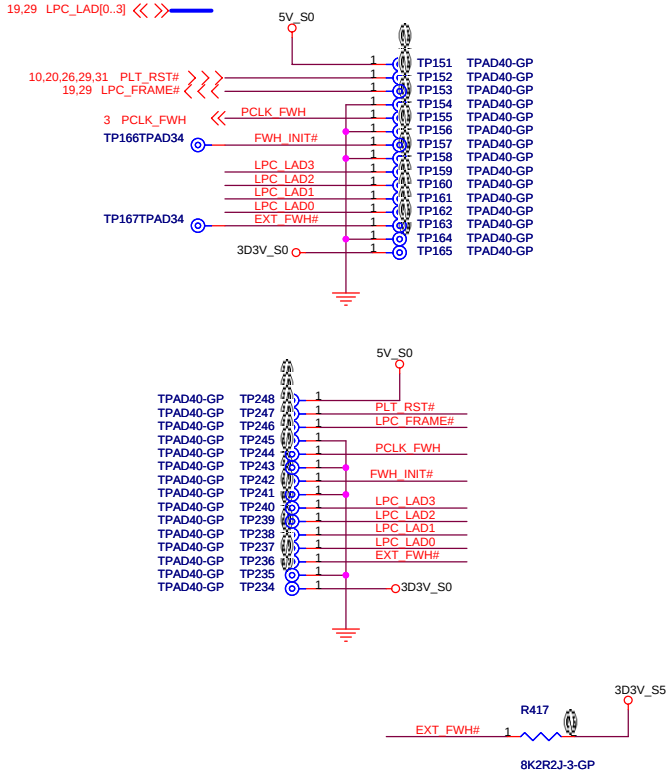
ODD Connector



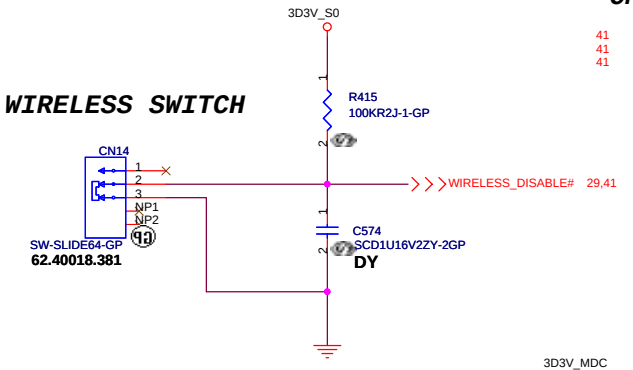
BT CONNECTOR



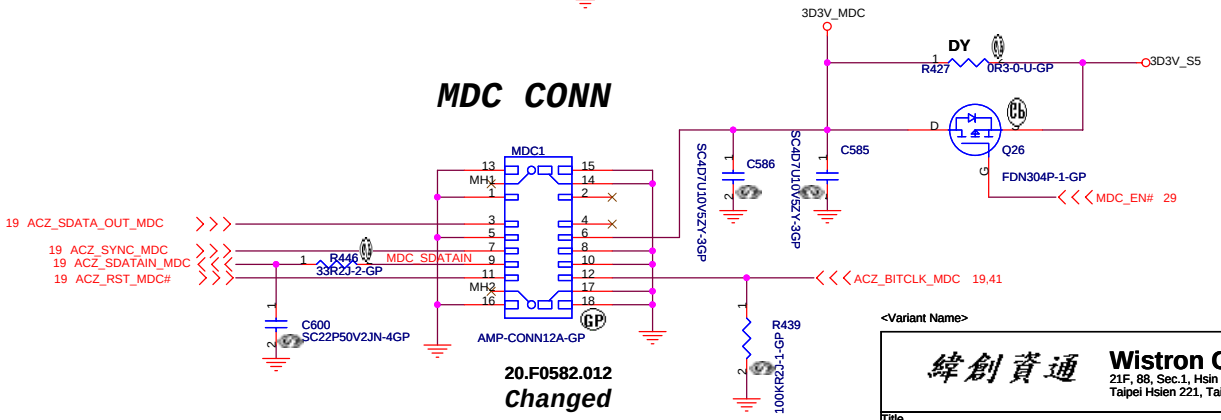
GOLDEN FINGER FOR DEBUG BOARD



WIRELESS SWITCH



MDC CONN



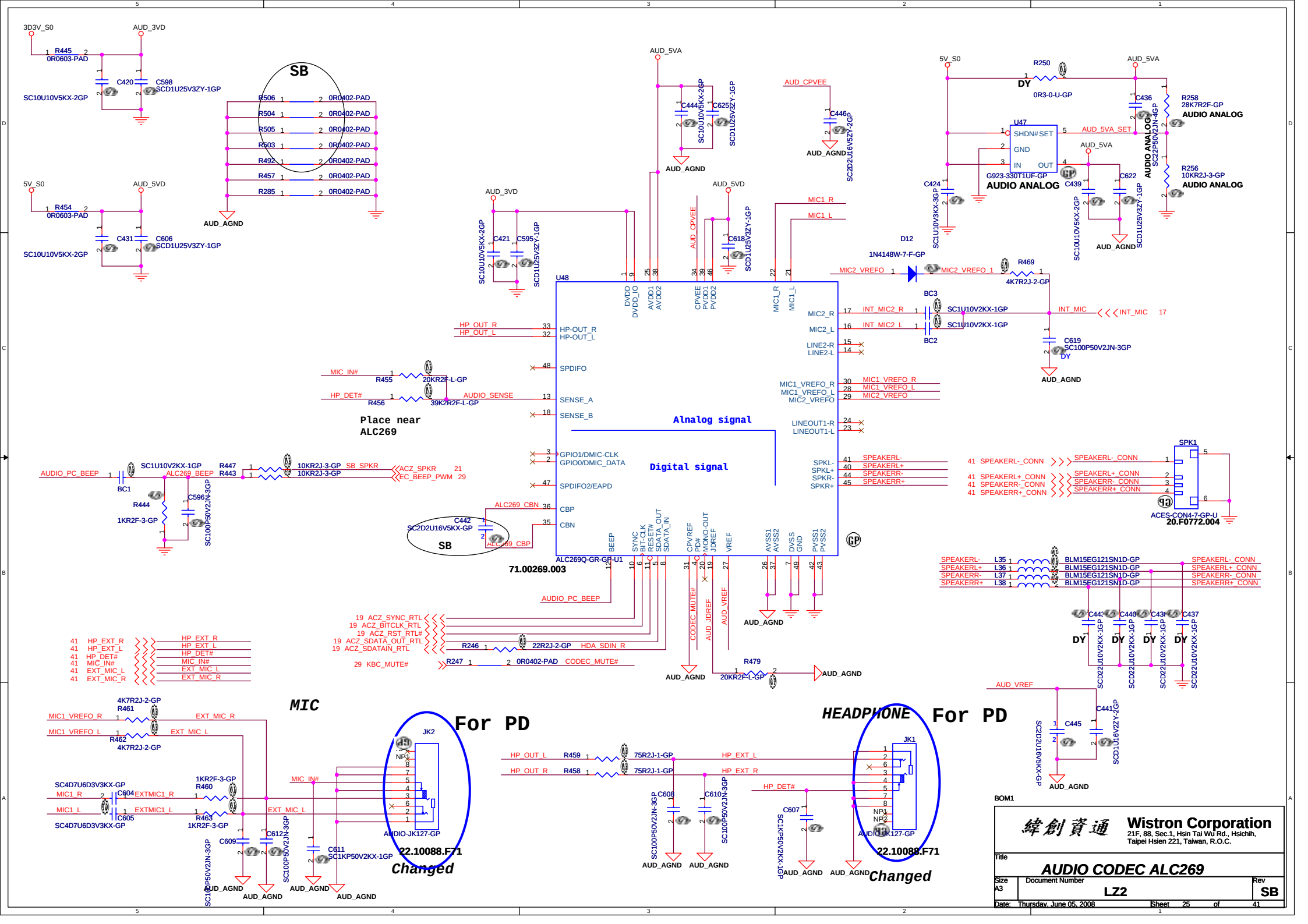
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/CDROM/DEBUG /MODEM/WIRELESS SW/BT**

Size	Document Number	Rev
	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 24 of 41



BOM1

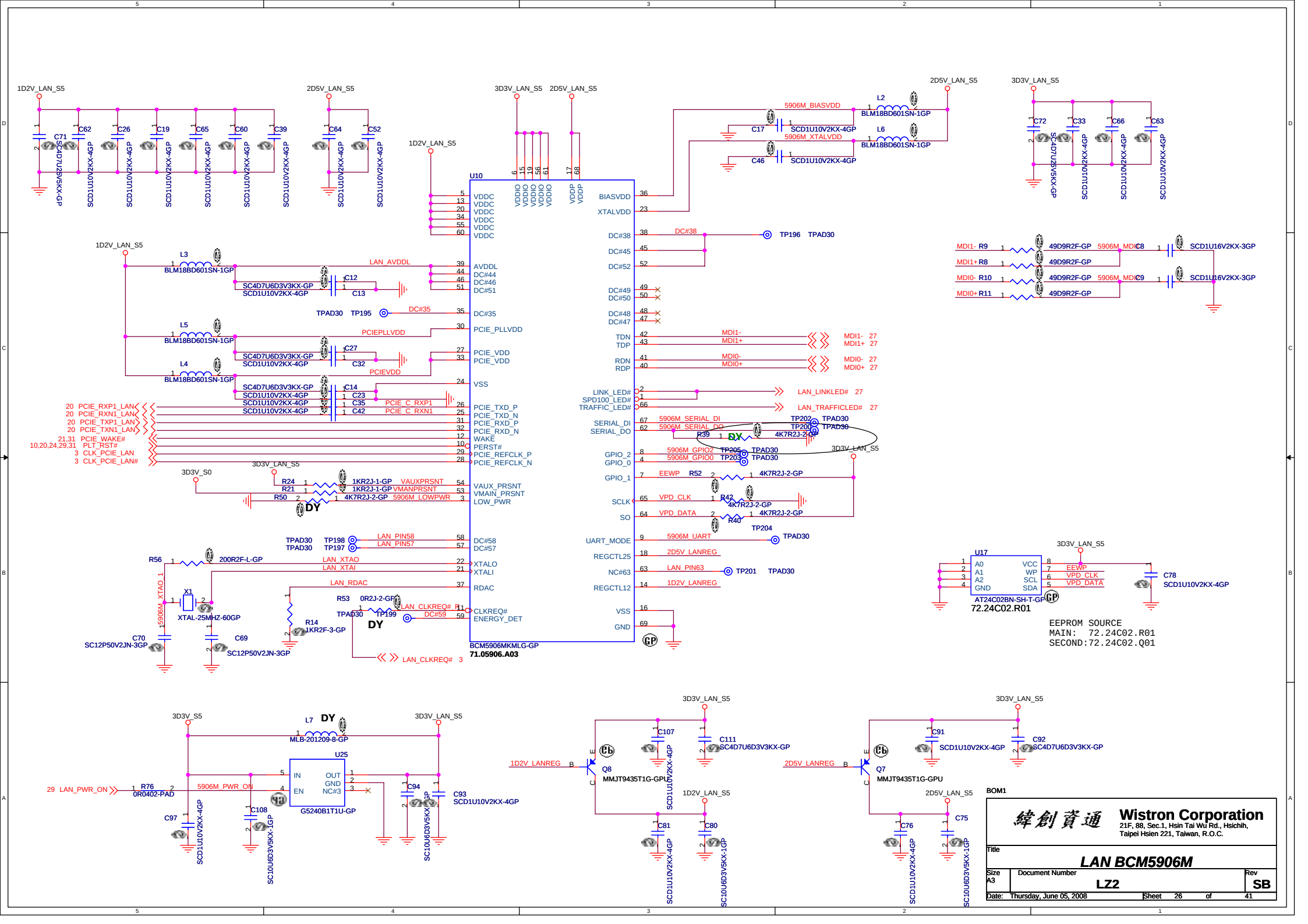
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC ALC269**

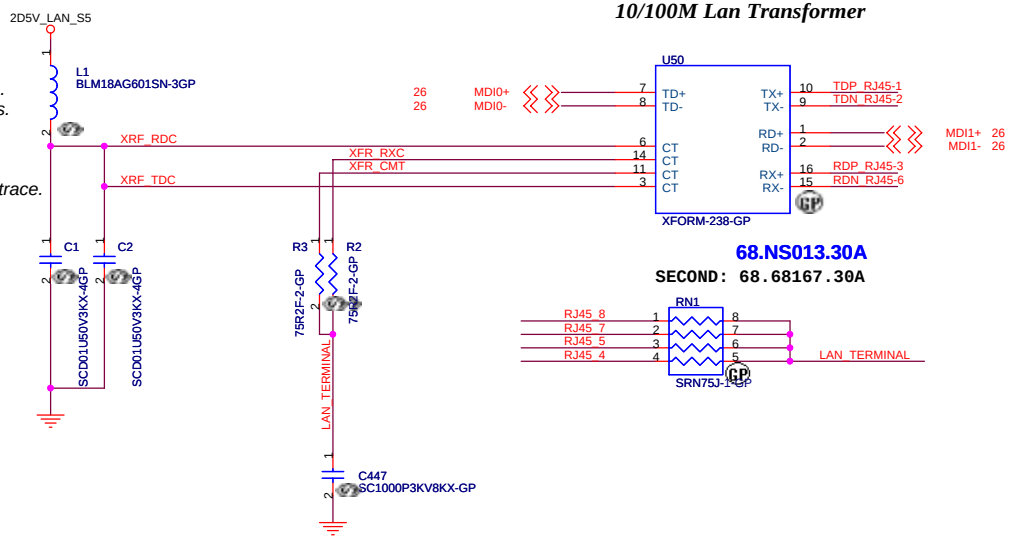
Size	Document Number	Rev
A3	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 25 of 41

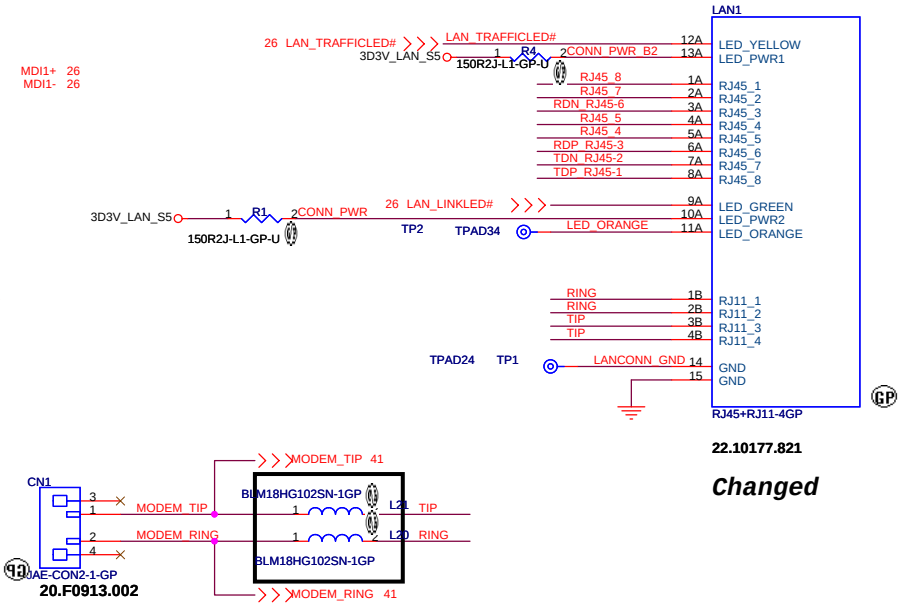

U10
BCM5906MKMLG-GP
71.05906.A03
U17
AT24C02BN-SH-T-GP
72.24C02.R01
EEPROM SOURCE
MAIN: 72.24C02.R01
SECOND:72.24C02.Q01
U25
G5240B1T1U-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN BCM5906M
LZ2
SB
Thursday, June 05, 2008

10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



68.NS013.30A
SECOND: 68.68167.30A



22.10177.821

Changed

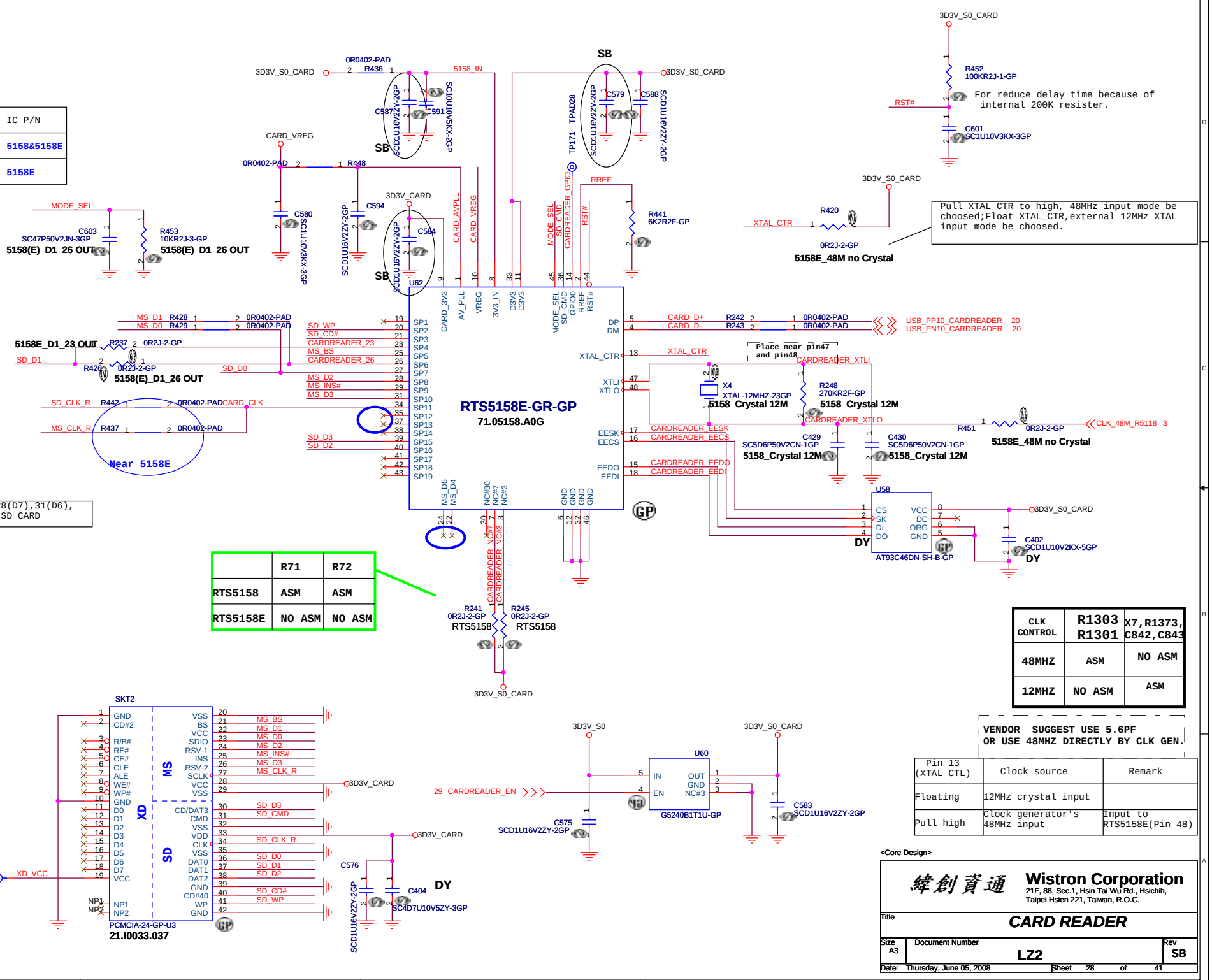
20.F0913.002

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN connector/NEW CARD/SIM***	
Size A3	Document Number **LZ2**	Rev **SB**
Date: Thursday, June 05, 2008	Sheet 27 of 41	

For 3in1 SD/MMC/MS CARD

R1302	C38	SD_D1 OUT FROM	IC P/N
10K	47 PF	PIN 26(MS_D1)	5158&5158E
NC	NC	PIN 23	5158E



	R71	R72
RTS5158	ASM	ASM
RTS5158E	NO ASM	NO ASM

CLK CONTROL	R1303 R1301	X7,R1373, C842,C843
48MHZ	ASM	NO ASM
12MHZ	NO ASM	ASM

Pin 13 (XTAL CTL)	Clock source	Remark
Floating	12MHz crystal input	
Pull high	Clock generator's 48MHz input	Input to RTS5158E(Pin 48)

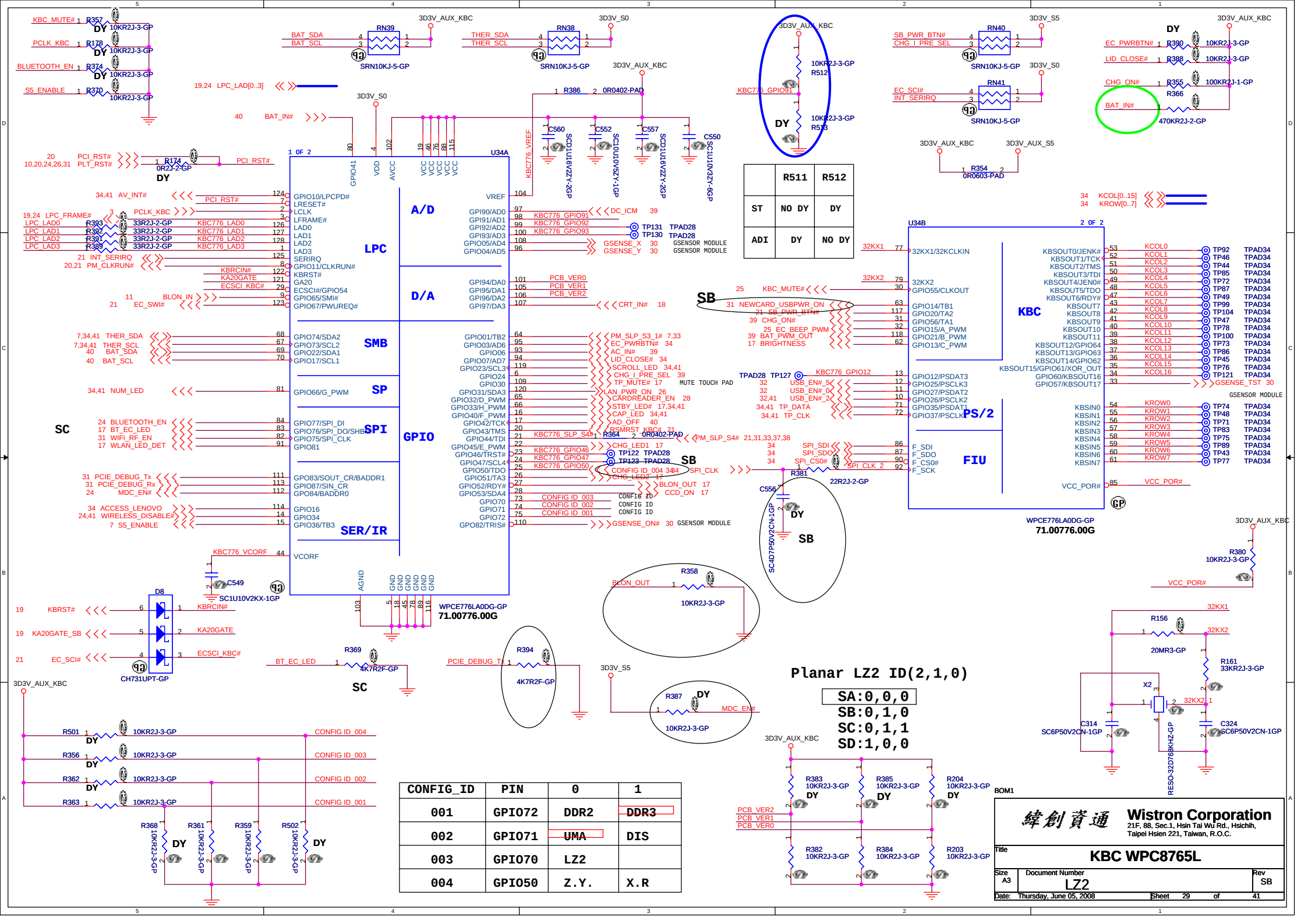
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER

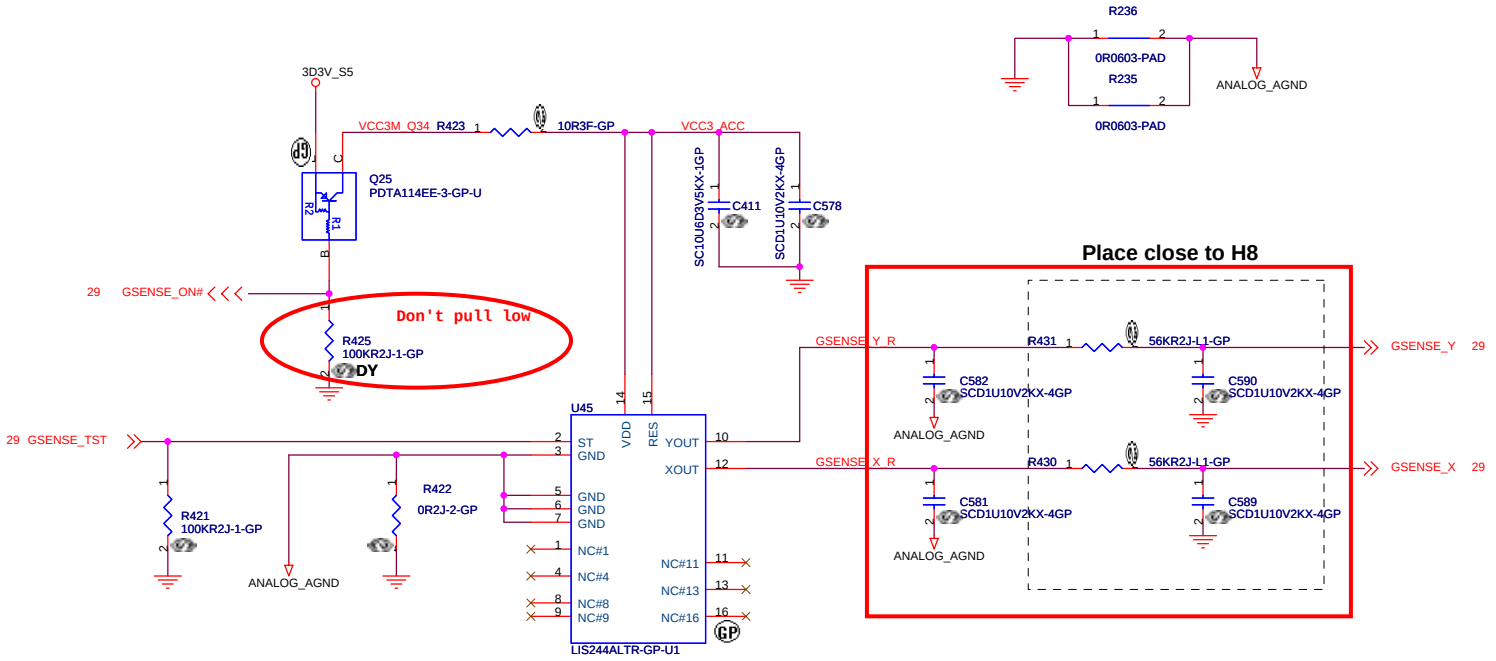
Size: A3 | Document Number: LZ2 | Rev: SB

Date: Thursday, June 05, 2008 | Sheet 28 of 41



	R511	R512
ST	NO DY	DY
ADI	DY	NO DY

CONFIG_ID	PIN	0	1
001	GPIO72	DDR2	DDR3
002	GPIO71	UMA	DIS
003	GPIO70	LZ2	
004	GPIO50	Z.Y.	X.R



Main :74.00244.0BZ
2nd: 41A1237AA

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

BOM1

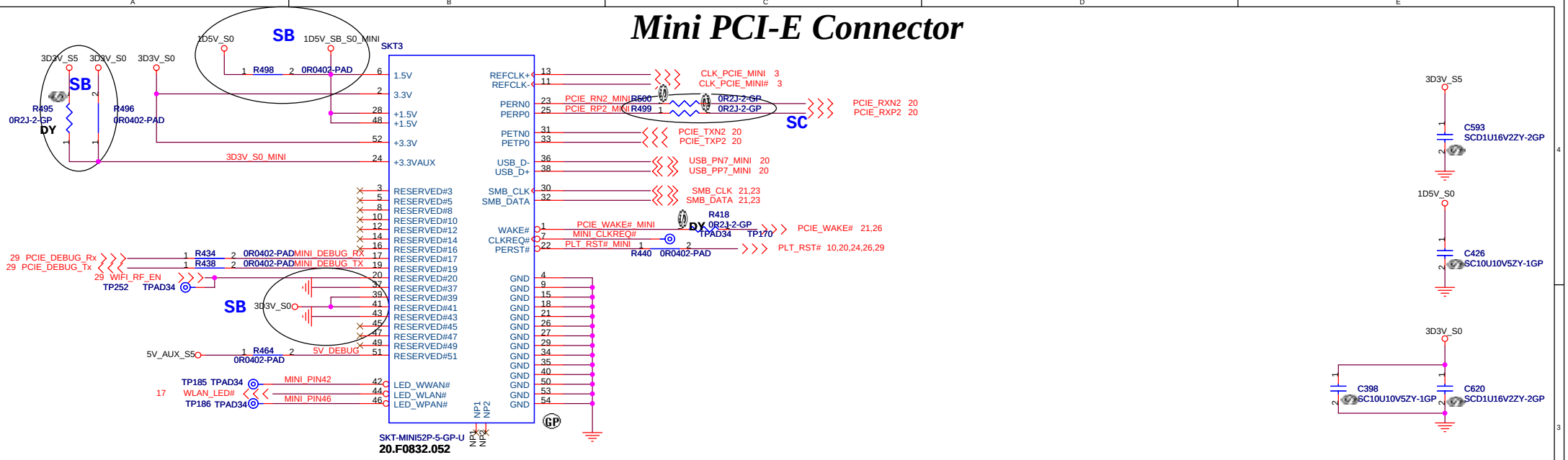
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GSENSOR**

Size	Document Number	Rev
	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 30 of 41

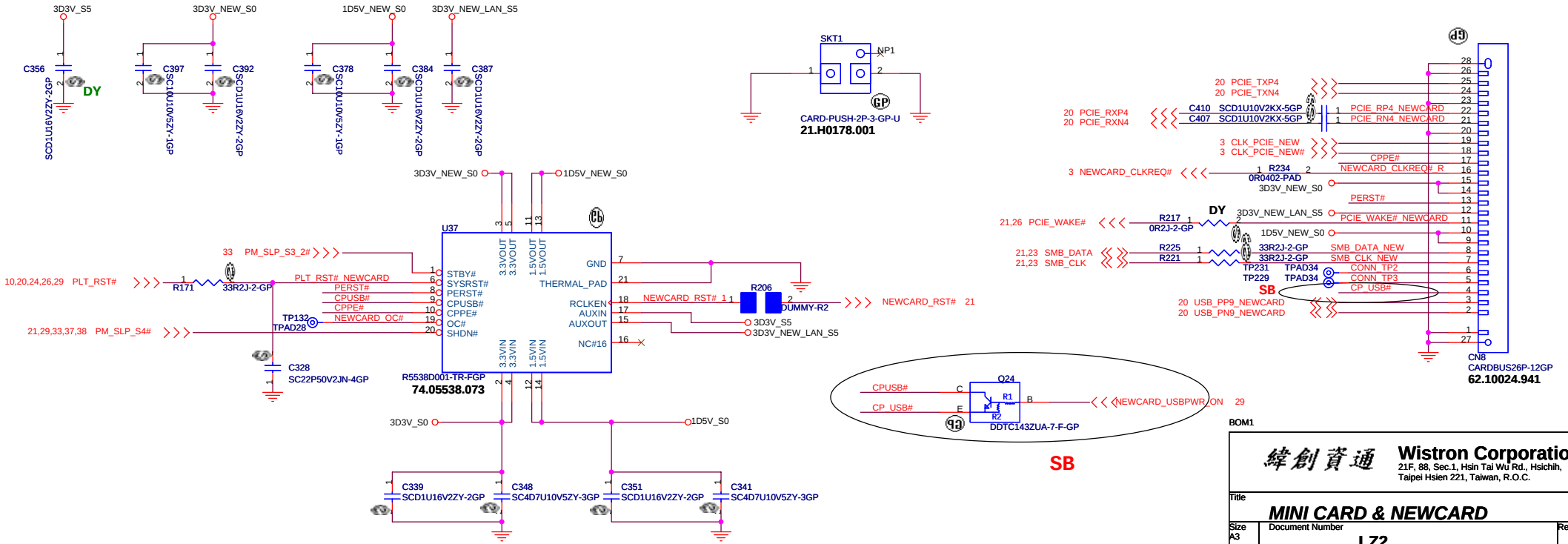
Mini PCI-E Connector



Place them Near to Chip

Place them Near to Connector

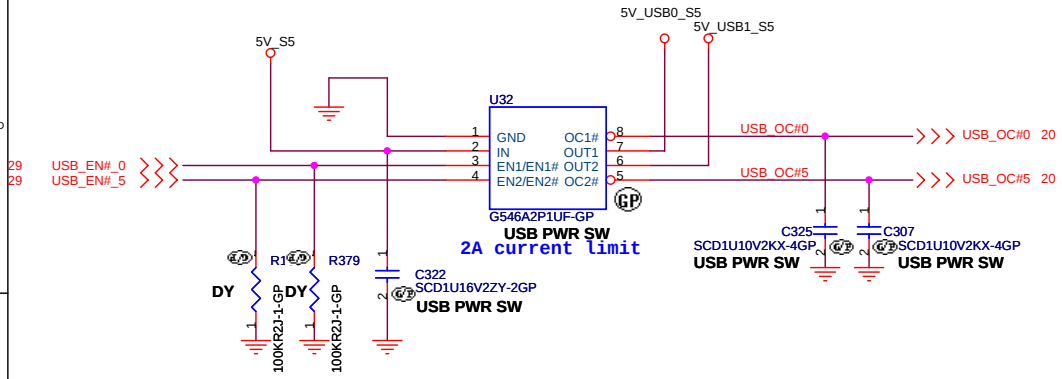
.N.E.W.C.A.R.D. C.O.N.N.

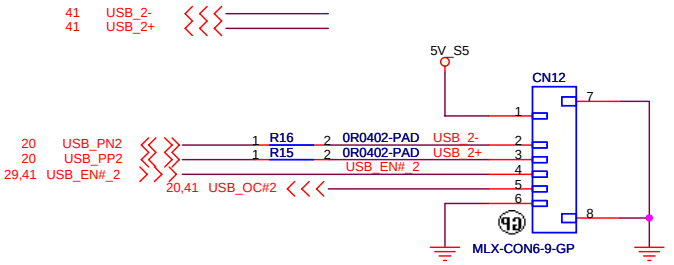


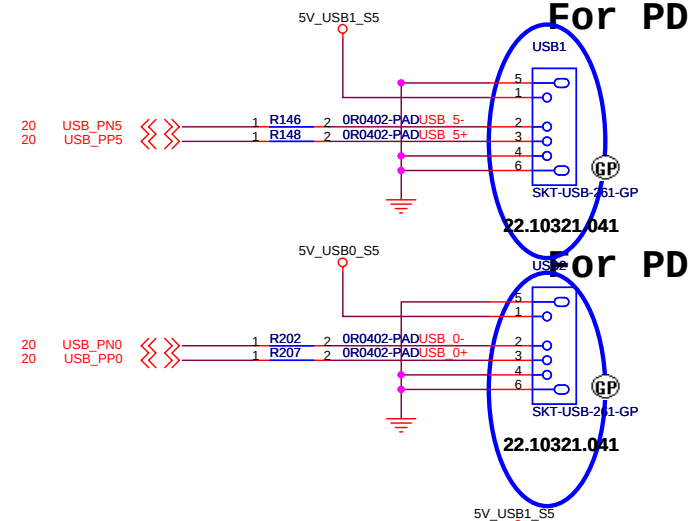
BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD & NEWCARD***
Size A3	Document Number **LZ2** Rev **SB**
Date: Thursday, June 05, 2008	Sheet 31 of 41

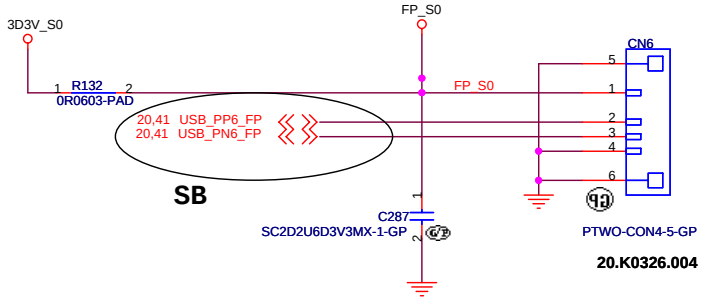
USB * 3 PORT

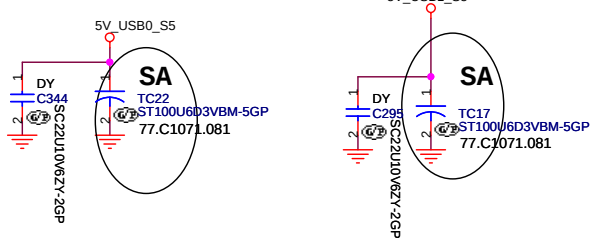


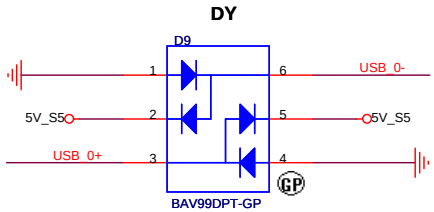


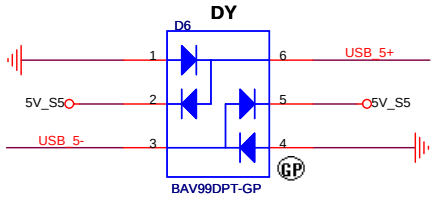


Finger Print









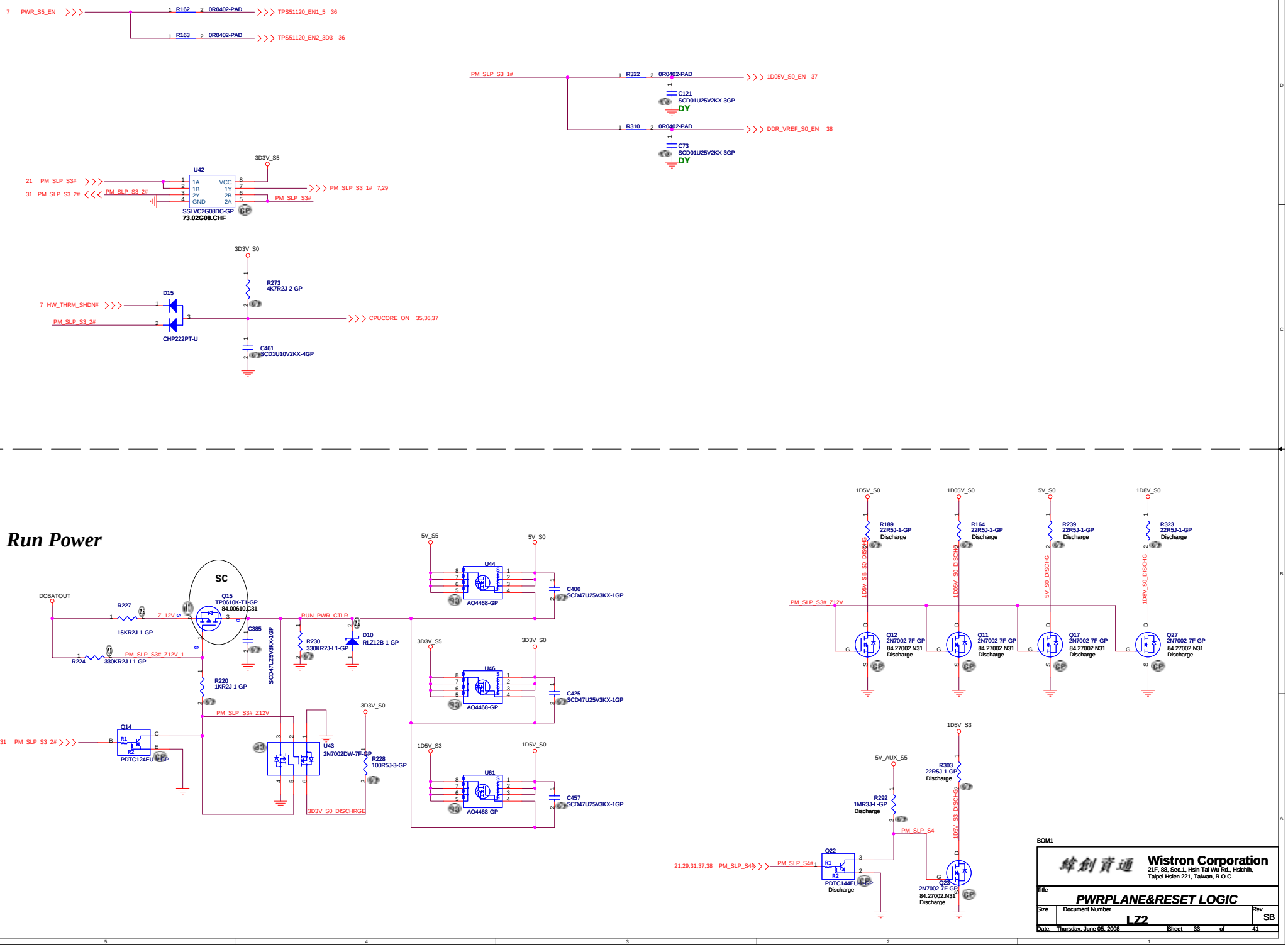
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

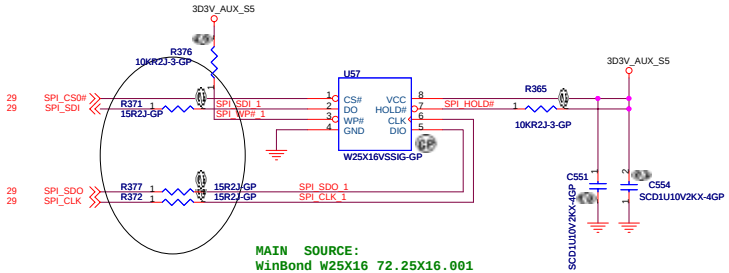
Title: **USB CONN/FINGER PRINT**

Size	Document Number	Rev
B	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 32 of 41


7 PWR_S5_EN
R162 0R0402-PAD
TPS51120_EN1_5 36
R163 0R0402-PAD
TPS51120_EN2_3D3 36
PM_SLP_S3_1#
R322 0R0402-PAD
1D05V_S0_EN 37
C121 SCD01U25V2KX-3GP DY
R310 0R0402-PAD
DDR_VREF_S0_EN 38
C73 SCD01U25V2KX-3GP DY
3D3V_S5
U42
21 PM_SLP_S3#
31 PM_SLP_S3_2#
PM_SLP_S3_2#
PM_SLP_S3_1# 7,29
PM_SLP_S3#
SSLVC2G08DC-GP
73.02G08.CHF
3D3V_S0
R273 4K7R2J-2-GP
D15
7 HW_THRM_SHDN#
PM_SLP_S3_2#
CPUCORE_ON 35,36,37
CHP222PT-U
C461 SCD1U10V2KX-4GP
Run Power
SC
DCBATOUT
Q15 TP0610K-T1-GP 84.00610.C31
R227 15KR2J-1-GP
Z_12V
R224 330KR2J-L1-GP
PM_SLP_S3#_Z12V_1
C385 SCD47U25V3KX-1GP
R220 1KR2J-1-GP
PM_SLP_S3#_Z12V
RUN_PWR_CTLR
R230 330KR2J-L1-GP
D10 RLZ12B-1-GP
5V_S5
5V_S0
U44 AO4468-GP
C400 SCD47U25V3KX-1GP
3D3V_S5
3D3V_S0
U46 AO4468-GP
C425 SCD47U25V3KX-1GP
1D5V_S3
1D5V_S0
U61 AO4468-GP
C457 SCD47U25V3KX-1GP
Q14
31 PM_SLP_S3_2#
PDTC124EU-GP
U43 2N7002DW-7F-GP
R228 100R5J-3-GP
3D3V_S0_DISCHRGE
1D5V_S0
5V_S0
1D8V_S0
R189 22R5J-1-GP Discharge
R164 22R5J-1-GP Discharge
R239 22R5J-1-GP Discharge
R323 22R5J-1-GP Discharge
1D5V_S3_S0_DISCHG
1D05V_S0_DISCHG
5V_S0_DISCHG
1D8V_S0_DISCHG
PM_SLP_S3#_Z12V
Q12 2N7002-7F-GP 84.27002.N31 Discharge
Q11 2N7002-7F-GP 84.27002.N31 Discharge
Q17 2N7002-7F-GP 84.27002.N31 Discharge
Q27 2N7002-7F-GP 84.27002.N31 Discharge
1D5V_S3
5V_AUX_S5
R303 22R5J-1-GP Discharge
R292 1MR3J-L-GP Discharge
1D5V_S3_DISCHG
PM_SLP_S4
21,29,31,37,38 PM_SLP_S4#
PM_SLP_S4#
Q22
PDTC144EU-GP Discharge
Q23 2N7002-7F-GP 84.27002.N31 Discharge
BOM1
鋒創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PWRPLANE&RESET LOGIC
Size
Document Number
LZ2
Rev
SB
Date: Thursday, June 05, 2008
Sheet 33 of 41

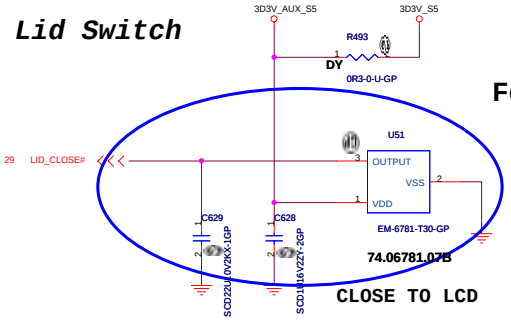
SPI Flash



MAIN SOURCE:
WinBond W25X16 72.25X16.001
SECOND SOURCE:
MXIC MX25L1605 72.25165.001

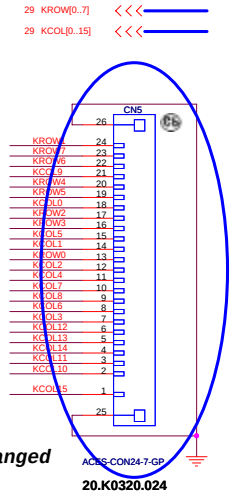
Lid Switch

For PD



CLOSE TO LCD

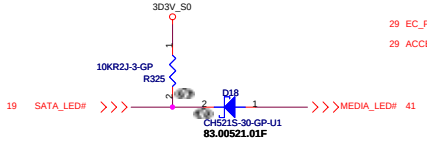
Keyboard Connector

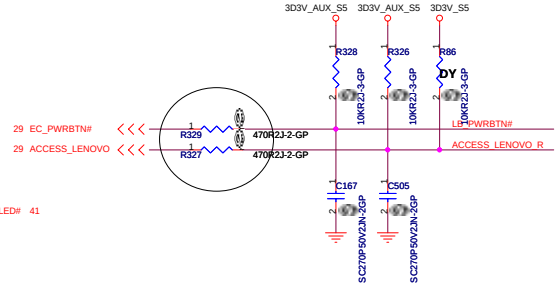


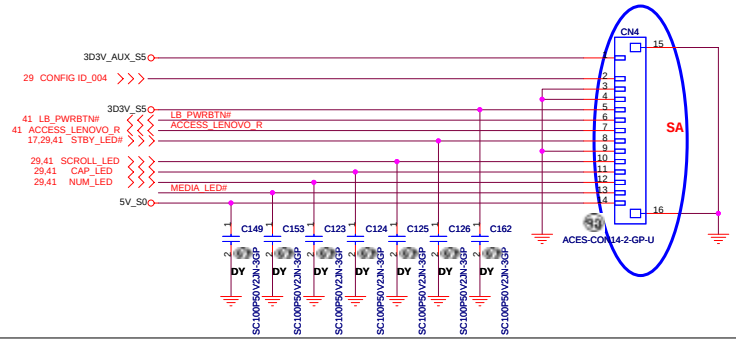
Changed

20.K0320.024

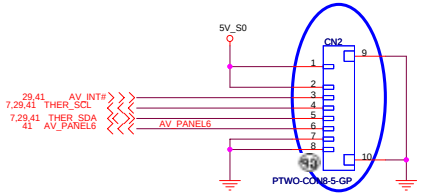
Launch Board





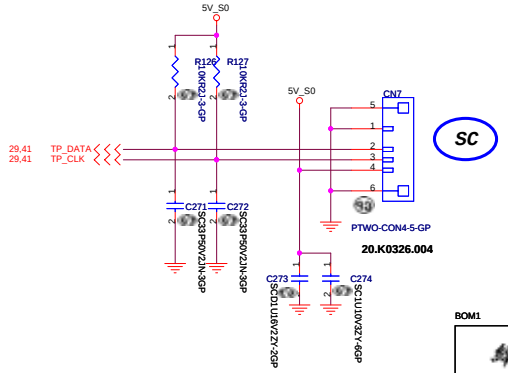


AV Panel



20.K0369.008

TouchPad Connector



20.K0326.004

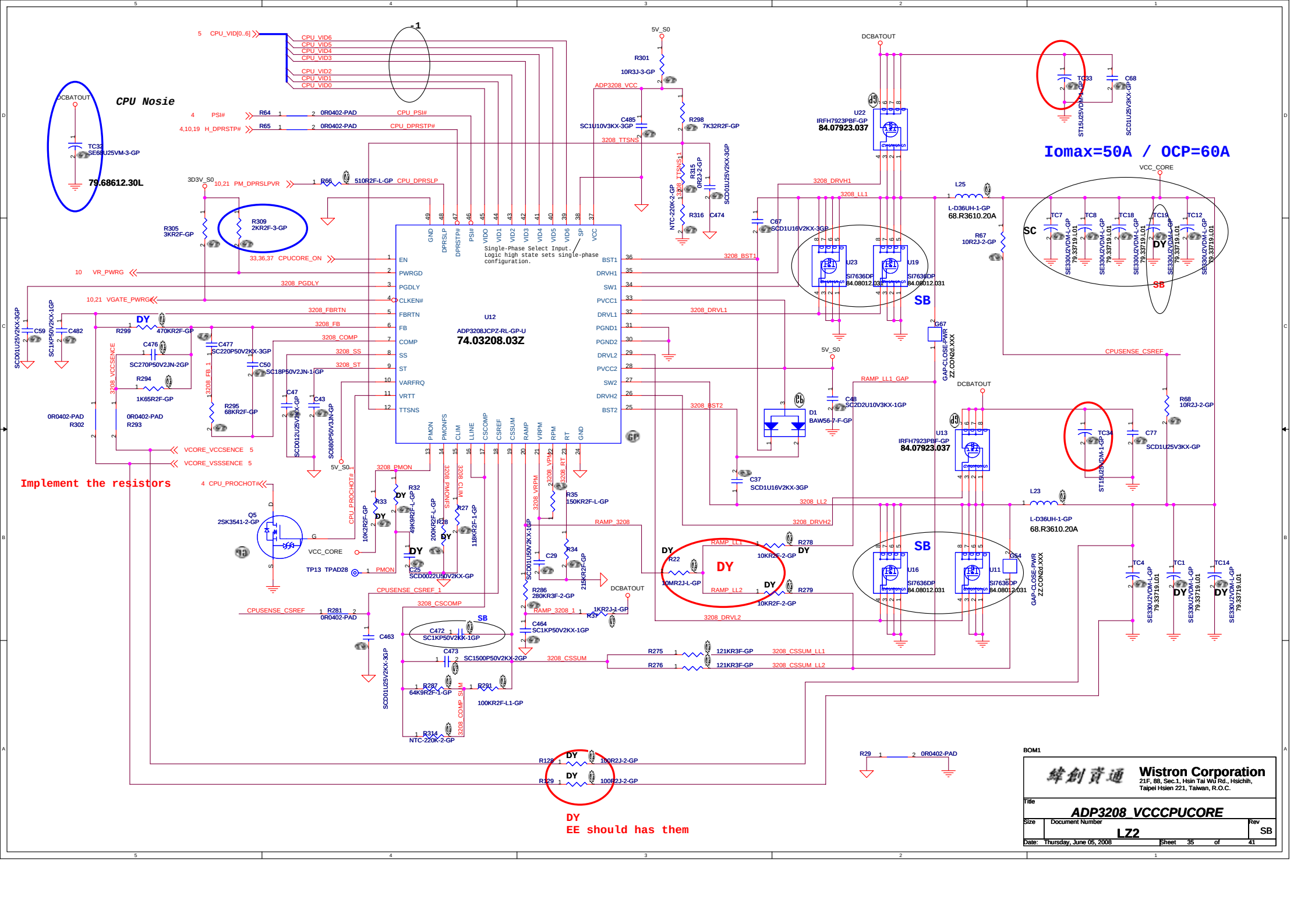
BOM1

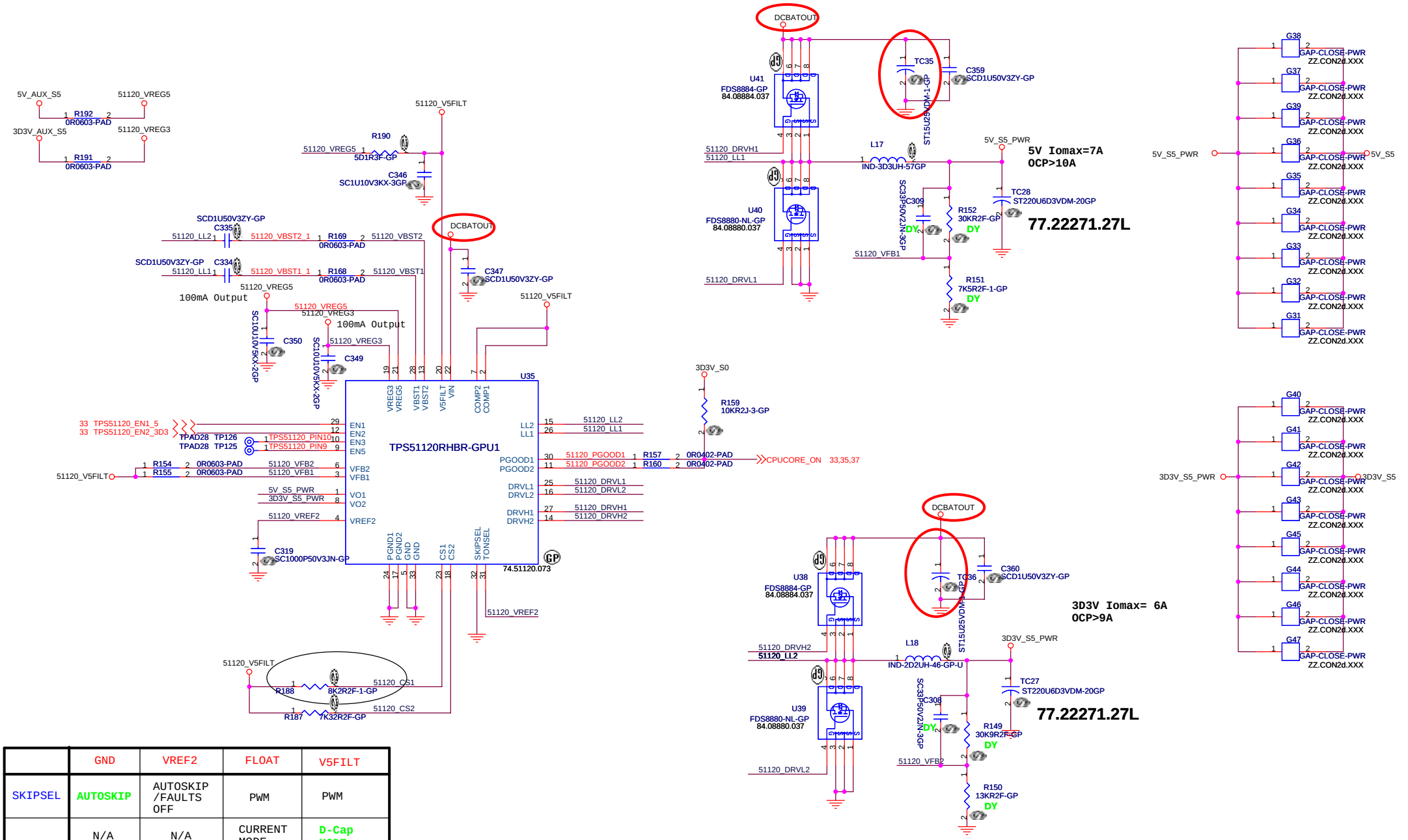
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP/SPI/AV/Charger

Size	Document Number	Rev
	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 34 of 41


CPU Nosie
79.68612.30L
U12
ADP3208JCPZ-RL-GP-U
74.03208.03Z
Single-Phase Select Input. Logic high state sets single-phase configuration.
Iomax=50A / OCP=60A
Implement the resistors
DY
EE should has them
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ADP3208_VCCCPUCORE
LZ2
Thursday, June 05, 2008
Sheet 35 of 41



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	Switcher OFF	not use	Swithchr ON	Switcher ON
	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

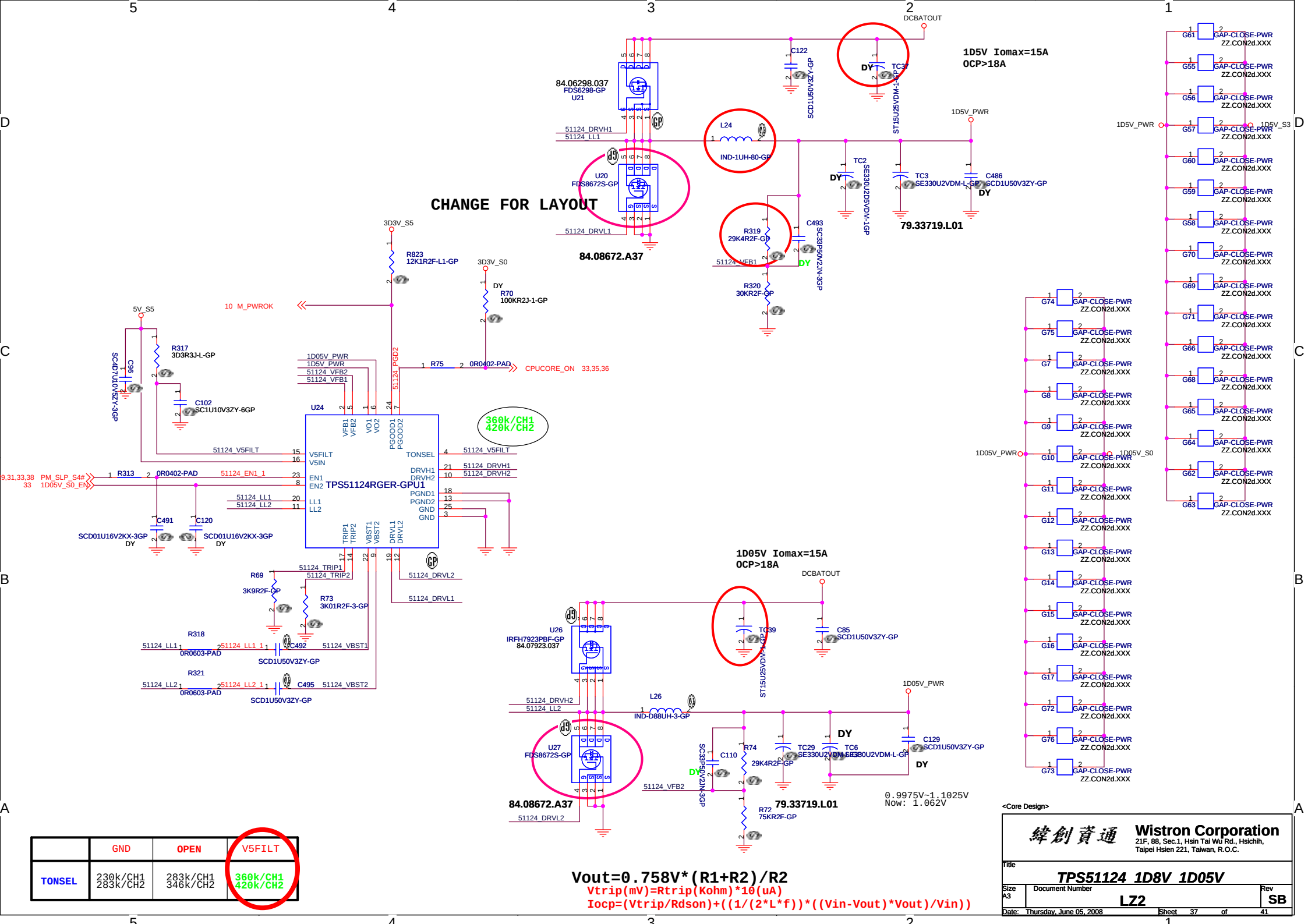
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size	Document Number	Rev
A3	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 36 of 41



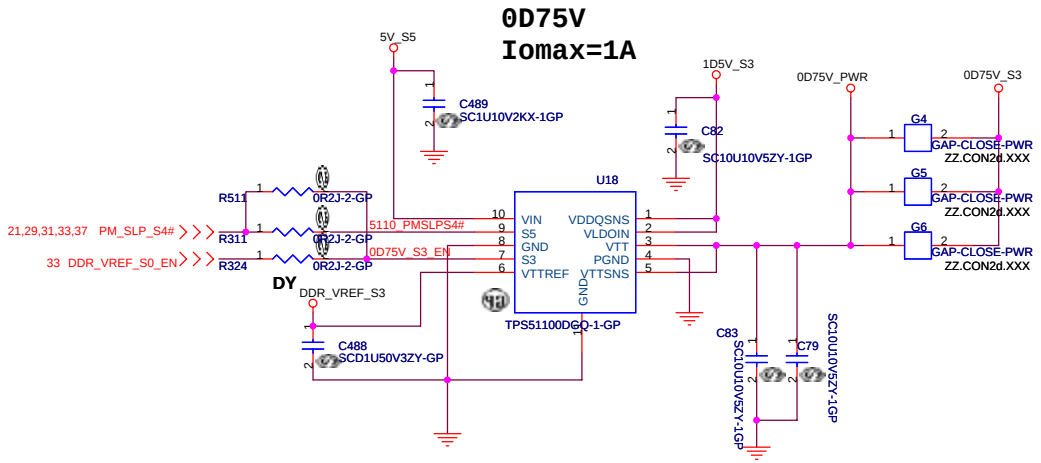
	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360k/CH1 420k/CH2

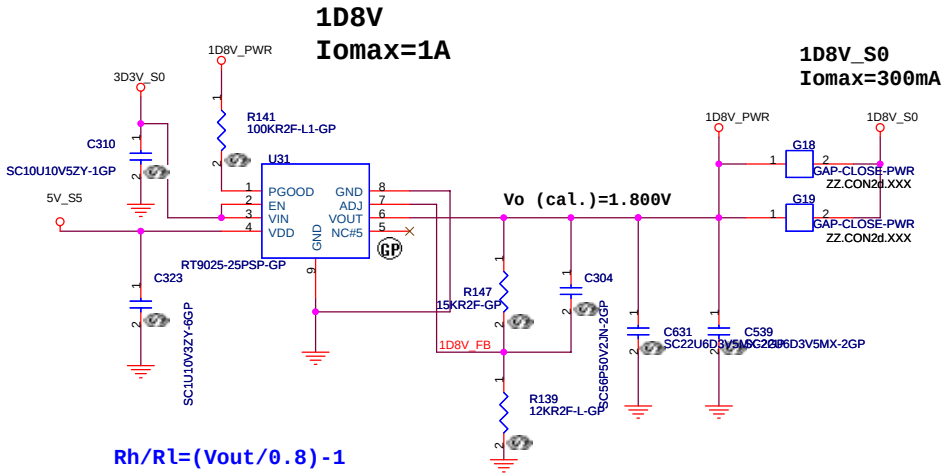
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Thursday, June 05, 2008 | Sheet 37 of 41





<Core Design>

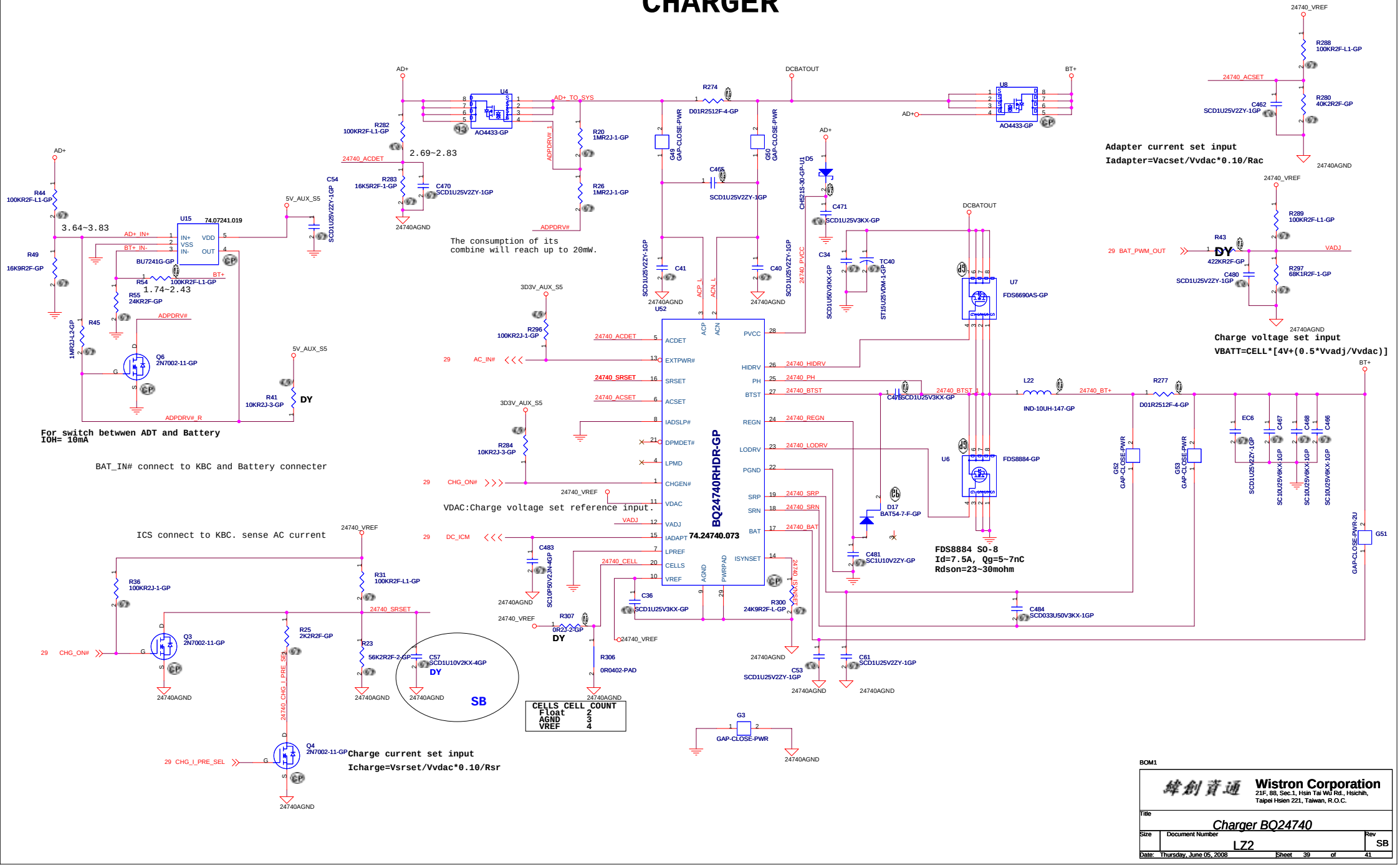
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
LDO 0D9V / 1D5V_S0

Size	Document Number	Rev
A3	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 38 of 41

CHARGER



BOM1

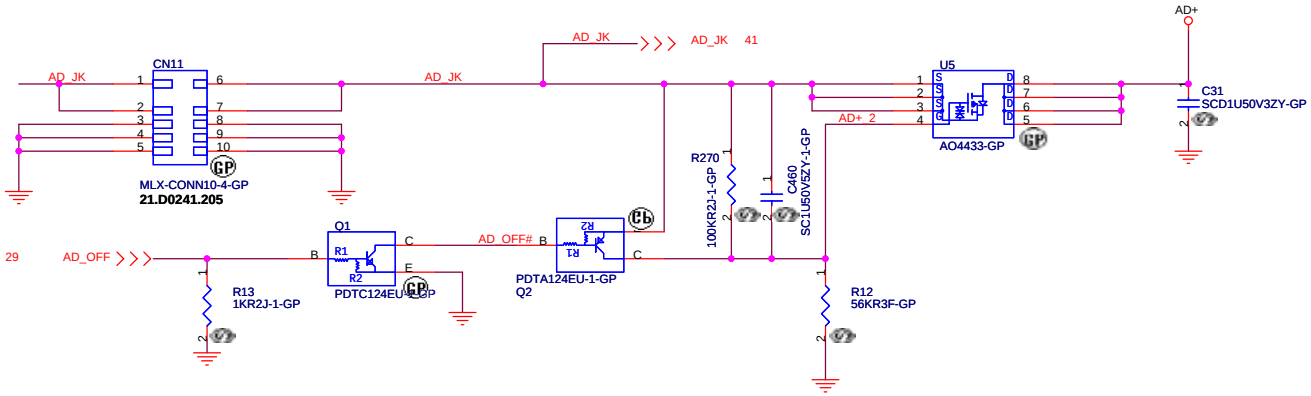
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger BQ24740

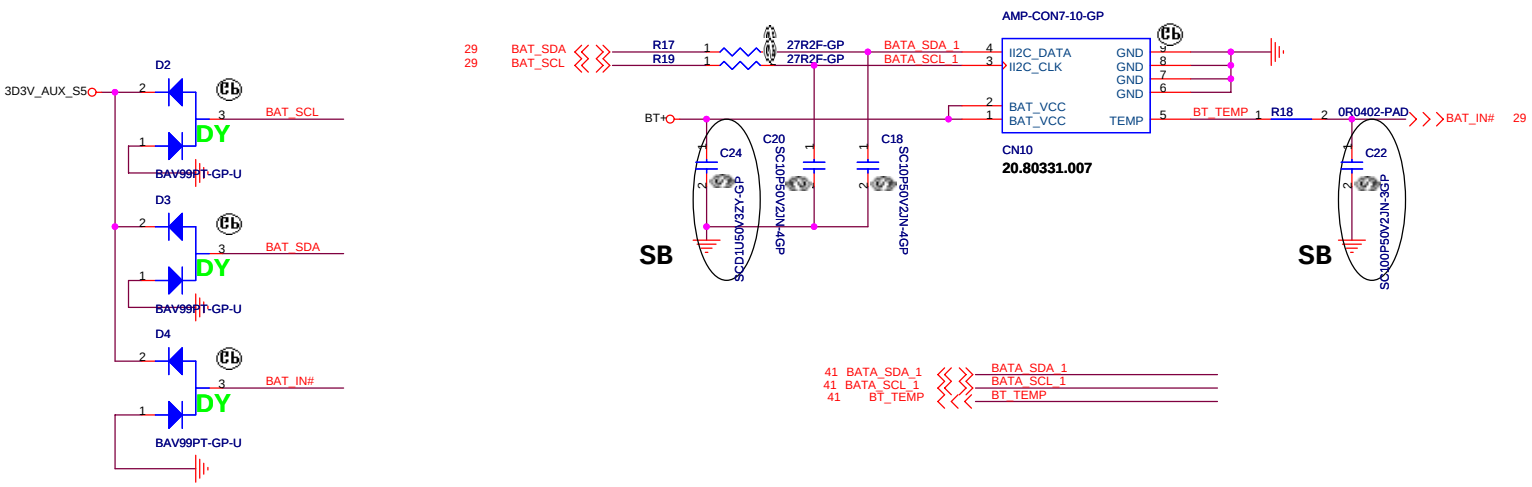
Size	Document Number	Rev
	LZ2	SB

Date: Thursday, June 05, 2008 Sheet 39 of 41

Adaptor in to generate DCBATOUT



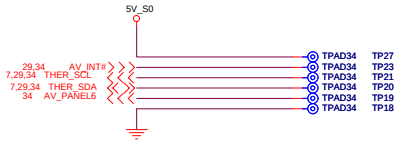
BATTERY CONNECTOR



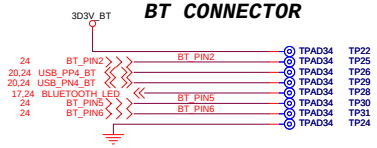
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *PTH FOR SCREW HOLES*		
Size: A3	Document Number: LZ2	Rev: SB
Date: Thursday, June 05, 2008	Sheet 40 of 41	

AV Panel



BT CONNECTOR

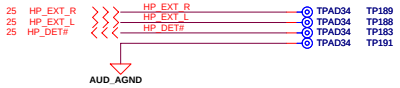


SATA CONN

TouchPad Connector

WIRELESS SWITCH

HEADPHONE CONN



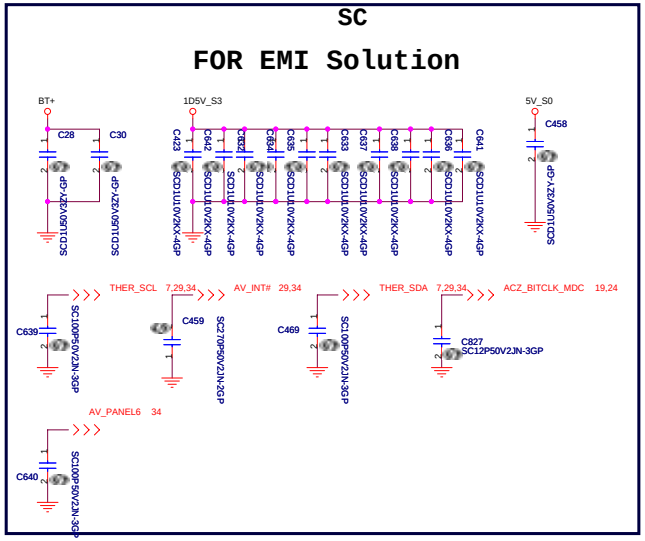
ODD CONN

MIC CONN

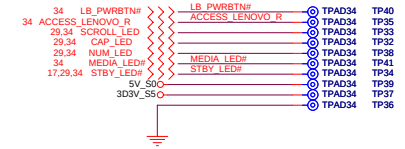
FAN CONN

SC

FOR EMI Solution

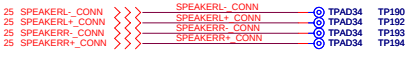


Launch Board

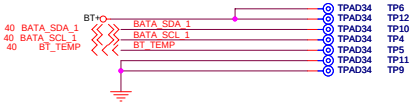


ADT BOARD CONN

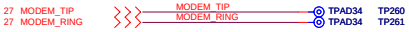
SPEAKER CONN



BATTERY CONN

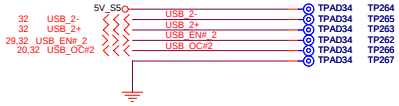


MODEM CABLE CONN



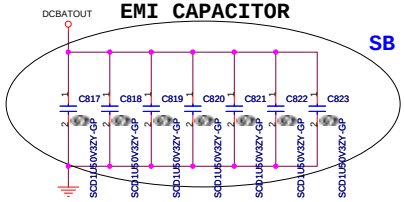
Finger Print CONN

USB BOARD CONN

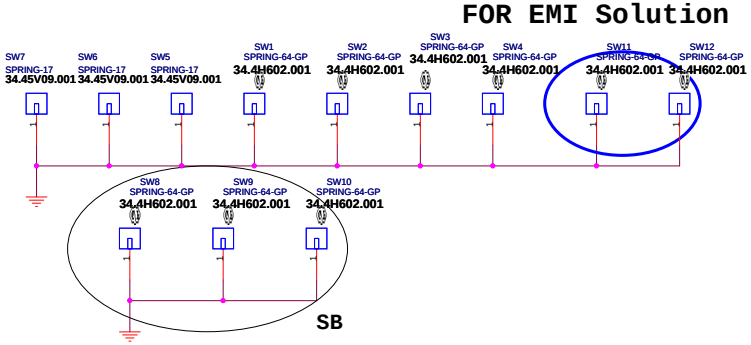


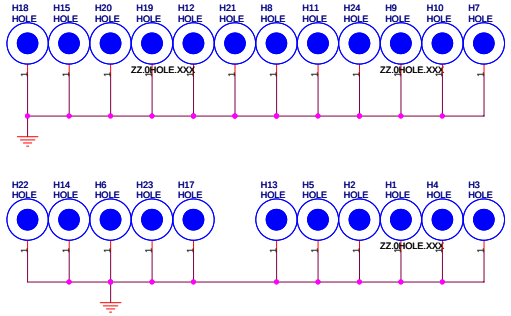
EMI CAPACITOR

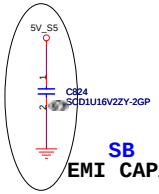
SB



FOR EMI Solution







SB

EMI CAPACITOR

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TTEST_PAD

Size: C | Document Number: LZ2 | Rev: SB

Date: Thursday, June 05, 2008 | Sheet 41 of 41