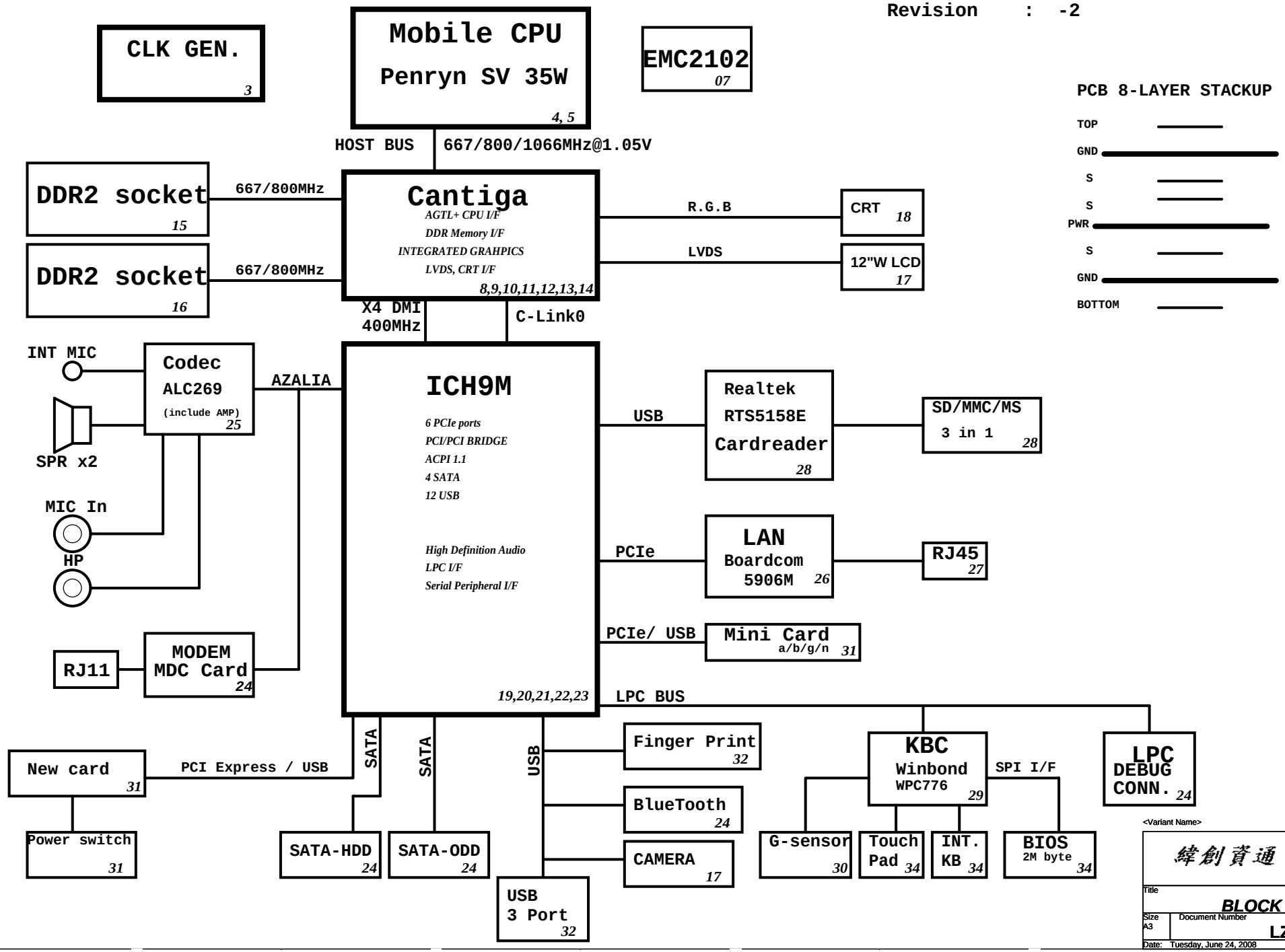
LZ2 Block Diagram

Project code: 91.4K101.001 ZY LZ2
91.4J301.001 XR LX2
PCB P/N : 07260-2
Revision : -2



PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC TPS51120 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 38

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5912 38

1D8V_S3	1D5V_NB_S0

APL5912 38

1D8V_S3	1D5V_SB_S0

CHARGER BQ24740 39

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V UP+5V 5V 100mA

CPU DC/DC ADP3208 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: LZ2 | Rev: SB
Date: Tuesday, June 24, 2008 | Sheet 1 of 41

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved Rising Edge of PWROK.	This signal has a weak internal pull-down. Note:This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap(Server Only) Rising edge of PWROK	Tying this strap low configures DMI for SIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server latforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5
page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG11 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1= The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

17,33,35,36,37,39,41	DCBATOUT	DCBATOUT
7,19,29,34,36,39,40	3D3V_AUX_S5	3D3V_AUX_S5
7,31,33,36,39	5V_AUX_S5	5V_AUX_S5
17,20,21,22,23,24,26,29,30,31,33,34,36	3D3V_S5	3D3V_S5
17,22,32,33,34,36,37,38,41	5V_S5	5V_S5
10,12,13,15,16,33,37,38,41	1D8V_S3	1D8V_S3
3,7,10,11,13,15,16,17,18,19,20,21,22,23,24,25,26,28,29,31,32,33,34,35,36,37,41	3D3V_S0	3D3V_S0
7,13,17,18,22,23,24,25,33,34,35,41	5V_S0	5V_S0
4,5,6,8,10,11,12,13,19,22,33,37	1D05V_S0	1D05V_S0
19,20,22,31,33,38	1D5V_SB_S0	1D5V_SB_S0
3,5,13,31,33,38	1D5V_NB_S0	1D5V_NB_S0

PCIE Routing

LANE1	BroadCom LAN
LANE2	MiniCard WLAN
LANE4	NewCard

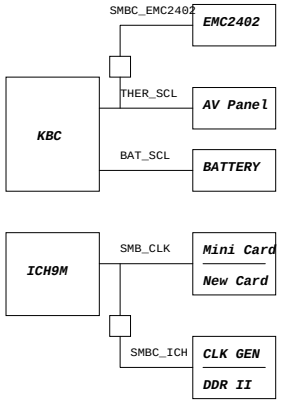
History:

LAB: 2008/01/02

USB Table

USB	
Pair	Device
0	JACK0
1	NC
2	JACK2
3	NC
4	BLUETOOTH
5	JACK1
6	Fringer Print
7	Mini Card
8	CAMERA
9	NEW CARD
10	CARDREADER
11	NC

SMBus



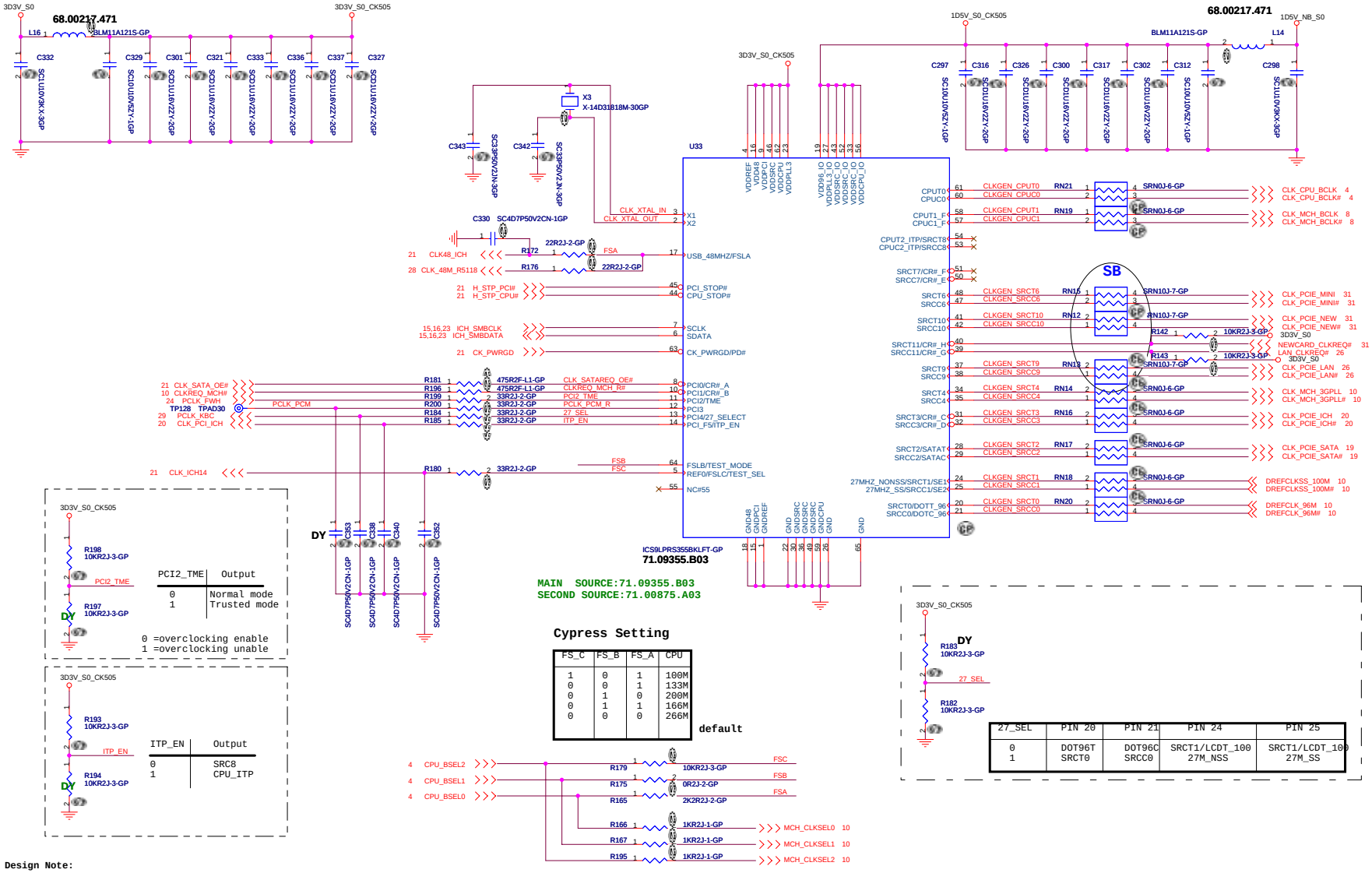
<Variant Name>

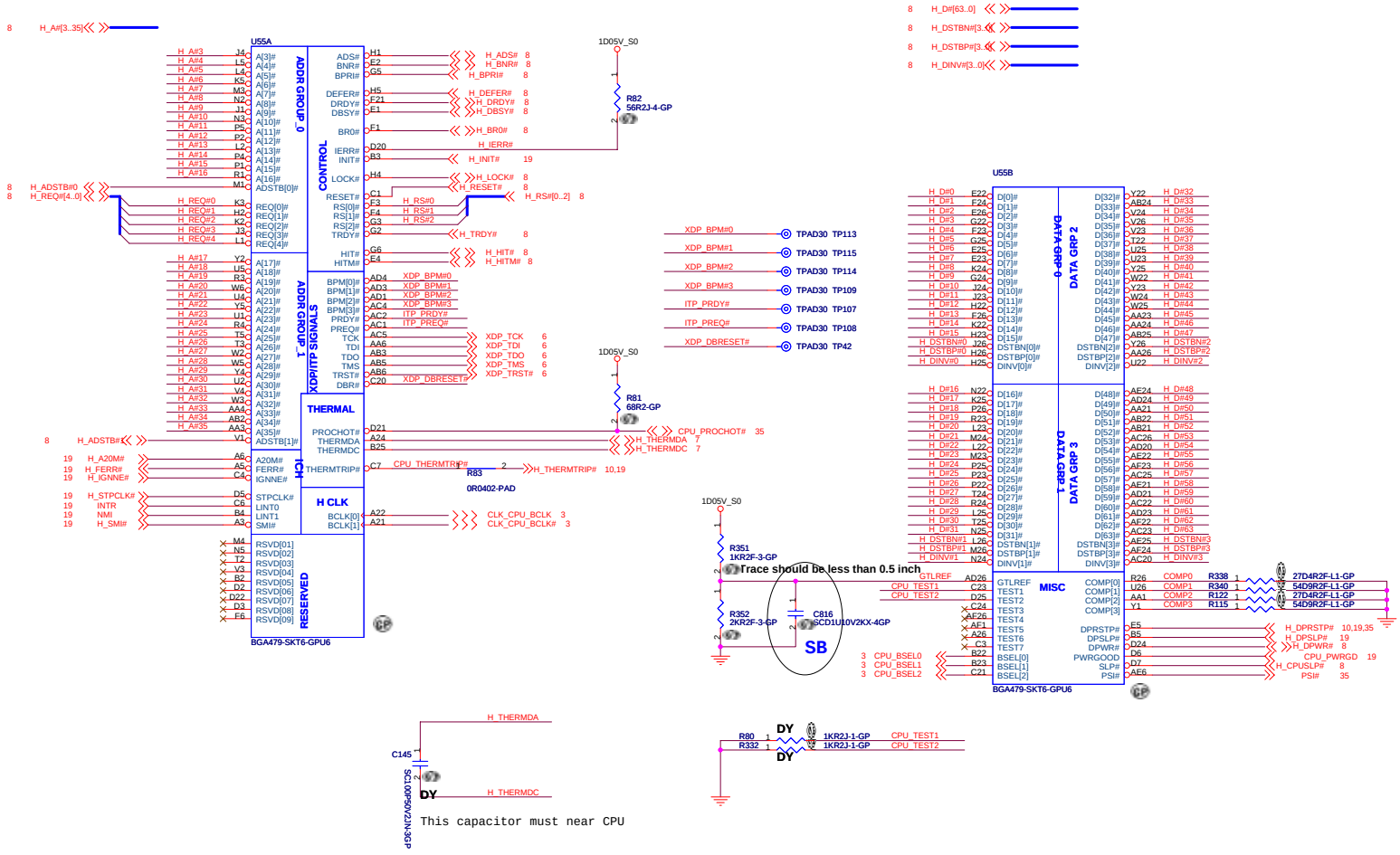
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 2 of 41


68.00217.471
3D3V_S0
3D3V_S0_CK505
L16
BLM11A121S-GP
C332
C329
C301
C321
C333
C336
C337
C327
SCD1U16V2ZY-2GP
SC10U6V5KX-3GP
SC10U6V5ZY-1GP
X3
X-14D31818M-30GP
C343
C342
SC33P50V2CN-4GP
C330
SC4D7P50V2CN-1GP
U33
ICS9LPRS355BKLFT-GP
71.09355.B03
CLK_XTAL_IN
CLK_XTAL_OUT
22R2J-2-GP
R172
R176
CLK48_ICH
CLK_48M_R5118
FSA
USB_48MHZ/FSLA
H_STP_PCI#
H_STP_CPU#
PCI_STOP#
CPU_STOP#
ICH_SMBCLK
ICH_SMBDATA
SCLK
SDATA
CK_PWRGD
CK_PWRGD/PD#
R181
R196
R199
R200
R184
R185
475R2F-L1-GP
33R2J-2-GP
CLK_SATAREQ_OE#
CLKREQ_MCH_R#
PCI2_TME
PCLK_PCM_R
27_SEL
ITP_EN
PCLK_PCM
TP128
TPAD30
PCLK_KBC
CLK_PCI_ICH
CLK_SATA_OE#
CLKREQ_MCH#
PCLK_FWH
PCI0/CR#_A
PCI1/CR#_B
PCI2/TME
PCI3
PCI4/27_SELECT
PCI_F5/ITP_EN
CLK_ICH14
R180
FSB
FSC
FSLB/TEST_MODE
REF0/FSLC/TEST_SEL
NC#55
1D5V_S0_CK505
1D5V_NB_S0
BLM11A121S-GP
L14
C297
C316
C326
C300
C317
C302
C312
C298
SC10U6V5KX-3GP
SC10U6V5ZY-1GP
SC1U16V2ZY-2GP
CPUT0
CPUC0
CPUT1_F
CPUC1_F
CPUT2_ITP/SRCT8
CPUC2_ITP/SRCC8
SRCT7/CR#_F
SRCC7/CR#_E
SRCT6
SRCC6
SRCT10
SRCC10
SRCT11/CR#_H
SRCC11/CR#_G
SRCT9
SRCC9
SRCT4
SRCC4
SRCT3/CR#_C
SRCC3/CR#_D
SRCT2/SATAT
SRCC2/SATAC
27MHZ_NONSS/SRCT1/SE1
27MHZ_SS/SRCC1/SE2
SRCT0/DOTT_96
SRCC0/DOTC_96
CLKGEN_CPUT0
CLKGEN_CPUC0
CLKGEN_CPUT1
CLKGEN_CPUC1
CLKGEN_SRCT6
CLKGEN_SRCC6
CLKGEN_SRCT10
CLKGEN_SRCC10
CLKGEN_SRCT9
CLKGEN_SRCC9
CLKGEN_SRCT4
CLKGEN_SRCC4
CLKGEN_SRCT3
CLKGEN_SRCC3
CLKGEN_SRCT2
CLKGEN_SRCC2
CLKGEN_SRCT1
CLKGEN_SRCC1
CLKGEN_SRCT0
CLKGEN_SRCC0
RN21
RN19
RN15
RN12
RN13
RN14
RN16
RN17
RN18
RN20
SRN0J-6-GP
SRN10J-7-GP
RN10J-7-GP
SB
R142
R143
10KR2J-3-GP
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
CLK_PCIE_MINI
CLK_PCIE_MINI#
CLK_PCIE_NEW
CLK_PCIE_NEW#
NEWCARD_CLKREQ#
LAN_CLKREQ#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
CLK_PCIE_ICH
CLK_PCIE_ICH#
CLK_PCIE_SATA
CLK_PCIE_SATA#
DREFCLKSS_100M
DREFCLKSS_100M#
DREFCLK_96M
DREFCLK_96M#
DY
R198
R197
PCI2_TME
PCI2_TME | Output
0 | Normal mode
1 | Trusted mode
0 =overclocking enable
1 =overclocking unable
R193
R194
ITP_EN
ITP_EN | Output
0 | SRC8
1 | CPU_ITP
R183
R182
27_SEL
27_SEL | PIN 20 | PIN 21 | PIN 24 | PIN 25
0 | DOT96T | DOT96C | SRCT1/LCDT_100 27M_NSS | SRCT1/LCDT_100 27M_SS
1 | SRCT0 | SRCC0
MAIN SOURCE:71.09355.B03
SECOND SOURCE:71.00875.A03
Cypress Setting
FS_C | FS_B | FS_A | CPU
1 | 0 | 1 | 100M
0 | 0 | 1 | 133M
0 | 1 | 0 | 200M
0 | 1 | 1 | 166M
0 | 0 | 0 | 266M
default
CPU_BSEL2
CPU_BSEL1
CPU_BSEL0
R179
R175
R165
10KR2J-3-GP
0R2J-2-GP
2K2R2J-2-GP
R166
R167
R195
1KR2J-1-GP
MCH_CLKSEL0
MCH_CLKSEL1
MCH_CLKSEL2
Design Note:
1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 3 of 41



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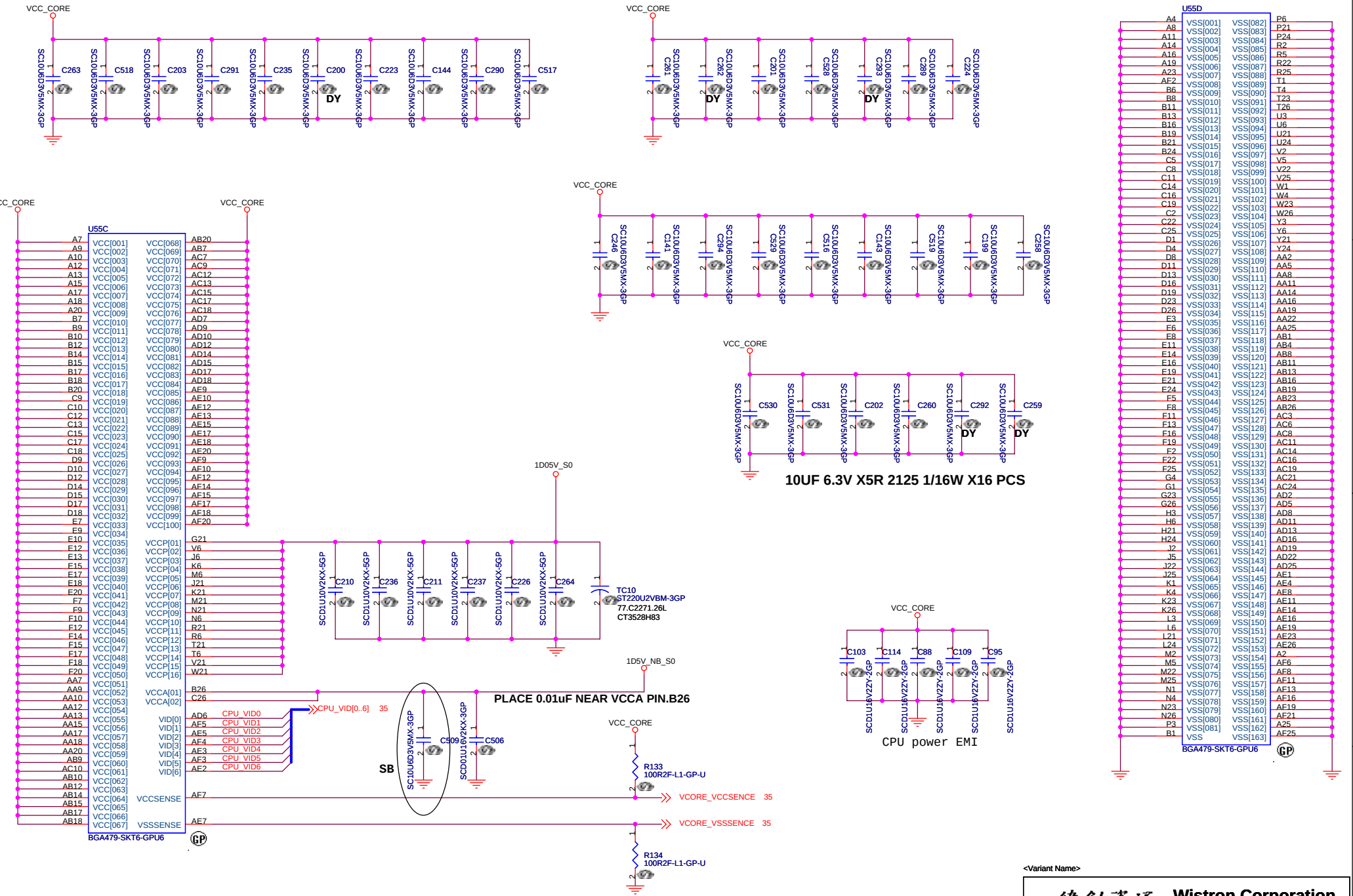
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***Penryn CPU(1/2)***		
Size C	Document Number **LZ2**		Rev **SB**
Date: Monday, June 23, 2008	Sheet 4 of 41		



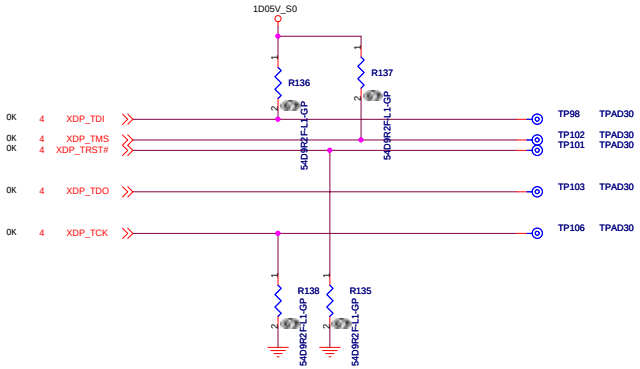
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Penryn CPU(2/2)

Size	Document Number	Rev
A3	LZ2	SB

Date: Monday, June 23, 2008 Sheet 5 of 41



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鋒創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ITP CONN***

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 6 of 41

Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing

Layout notice :
Both H_THERMDA_1 and THERMDC_1 routing
10 mil trace width and 10 mil spacing

Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing

Layout notice :
C809, C811, C812
close to chip side;

CPU0

SYSTEM

This cap should close to thermal diode.

Layout 15 mil

20.F0714.003

SC

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

SC

220ms delay time after Power-on

Dummy when G792 enhanced T8 function

HW thermal shut down tempature
setting 95 degree . Put Near CPU .

Rset=0.0012*T^2-0.9308*T+96.147

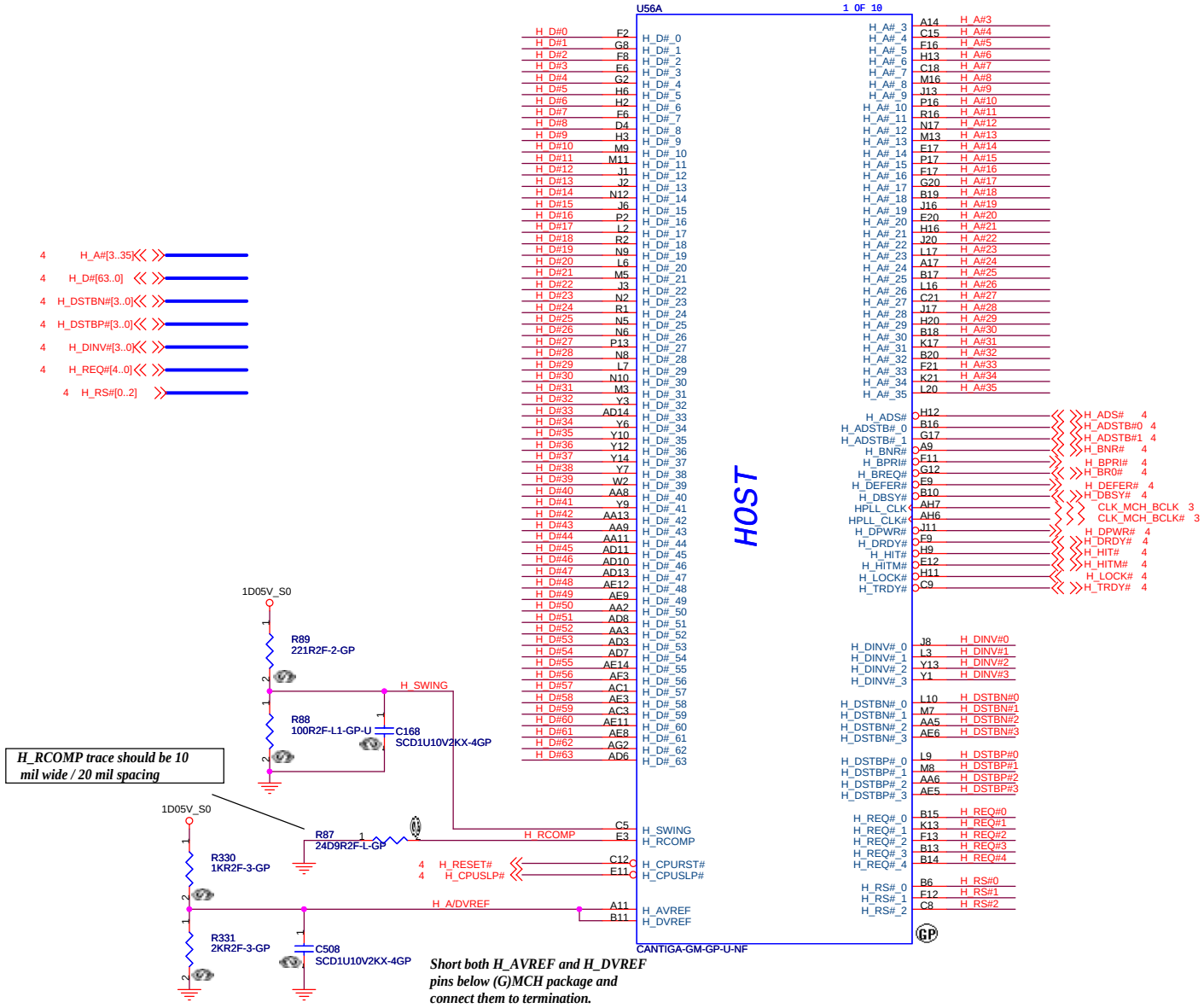
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 7 of 41



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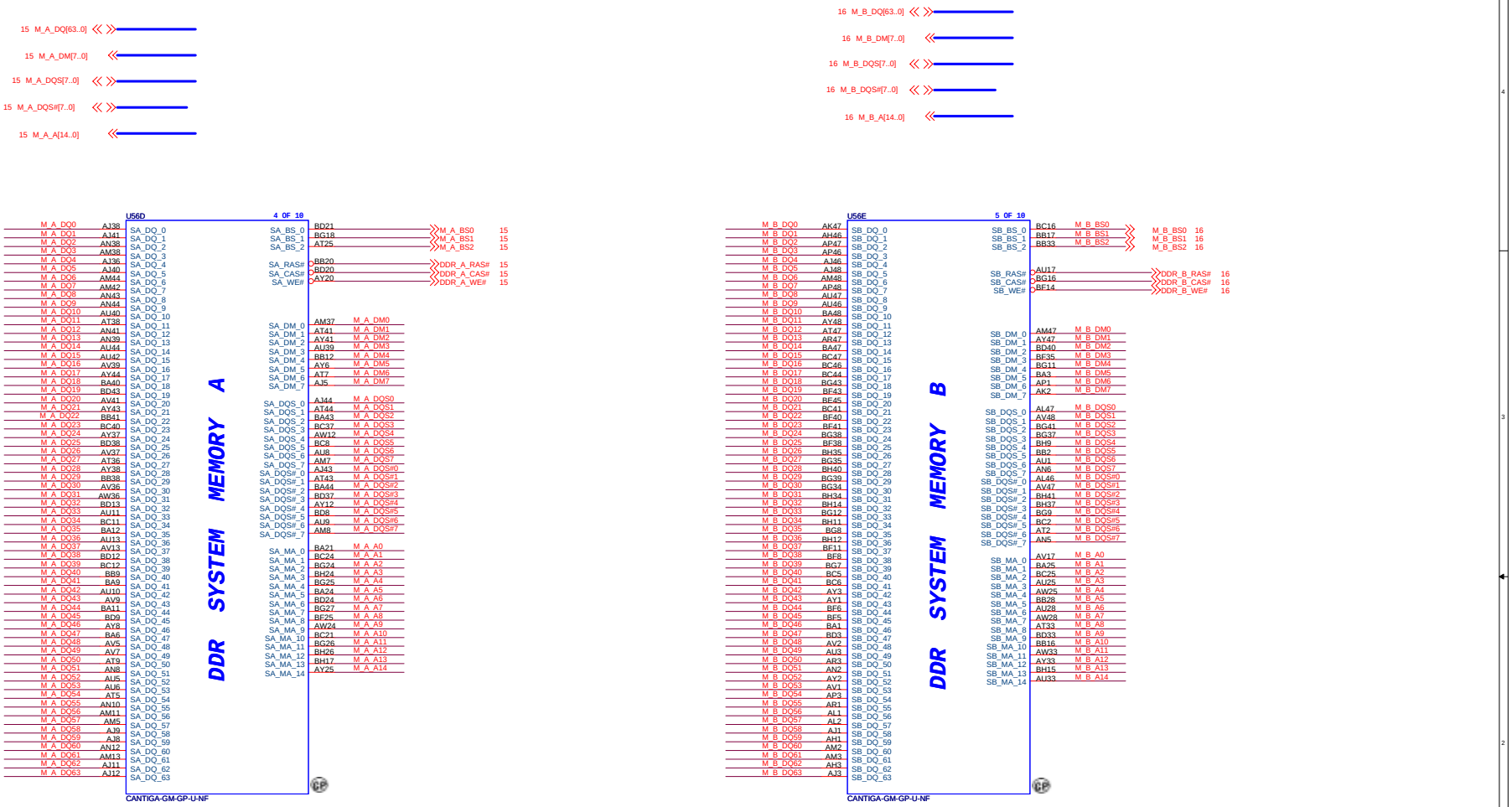
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(1/7):HOST I/F

Size	Document Number	Rev
A3	LZ2	SB

Date: Monday, June 23, 2008 Sheet 8 of 41



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Taipei Hsien 221, Taiwan, R.O.C.

<variant_name>

Title: Cantiga(2/7):DDR3

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 9 of 41

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown

U56B — 2 OF 10 — CANTIGA-GM-GP-U-NF

RSVD: RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0, SA_CK_1, SB_CK_0, SB_CK_1, SA_CK#_0, SA_CK#_1, SB_CK#_0, SB_CK#_1, SA_CKE_0, SA_CKE_1, SB_CKE_0, SB_CKE_1, SA_CS#_0, SA_CS#_1, SB_CS#_0, SB_CS#_1, SA_ODT_0, SA_ODT_1, SB_ODT_0, SB_ODT_1, SM_RCOMP, SM_RCOMP#, SM_RCOMP_VOH, SM_RCOMP_VOL, SM_VREF, SM_PWROK, SM_REXT, SM_DRAMRST#

CLK: DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#, PEG_CLK, PEG_CLK#

DMI: DMI_RXN_0..3, DMI_RXP_0..3, DMI_TXN_0..3, DMI_TXP_0..3

CFG: CFG_0..CFG_20

GRAPHICS VID: GFX_VID_0..4, GFX_VR_EN

PM: PM_SYNC#, PM_DPRSTP#, PM_EXT_TS#_0, PM_EXT_TS#_1, PWROK, RSTIN#, THERMTRIP#, DPRSLPVR

ME: CL_CLK, CL_DATA, CL_PWROK, CL_RST#, CL_VREF

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

MISC: DDPC_CTRLCLK, DDPC_CTRLDATA, SDVO_CTRLCLK, SDVO_CTRLDATA, CLKREQ#, ICH_SYNC#, TSATN#

HDA: HDA_BCLK, HDA_RST#, HDA_SDI, HDA_SDO, HDA_SYNC

SM_REXT:Constant circuit reference for clocks.

10K P/L in DDRII

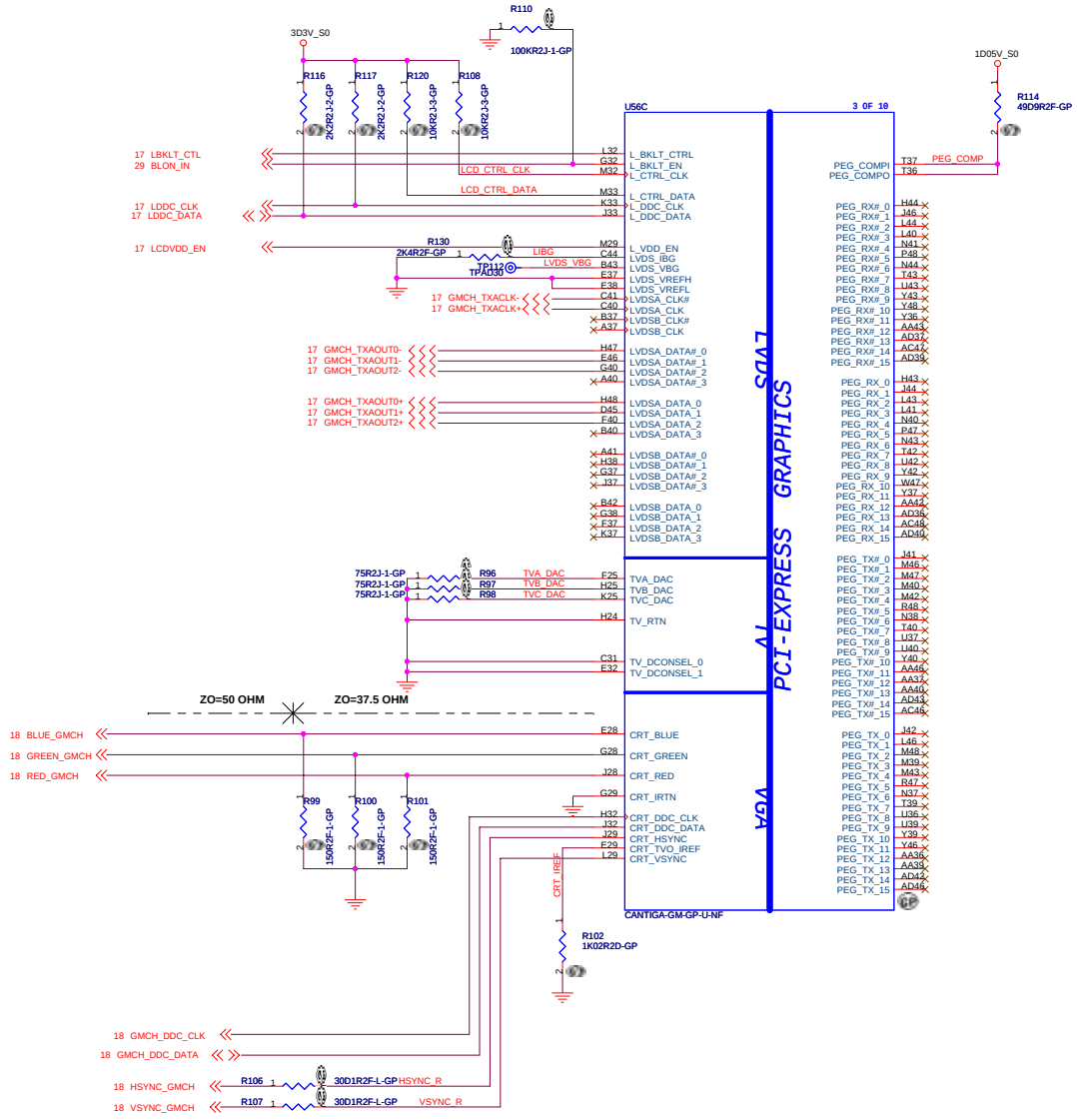
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: Cantiga(3/7):DMI/PM/CFG/GF

Size: C | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 10 of 41



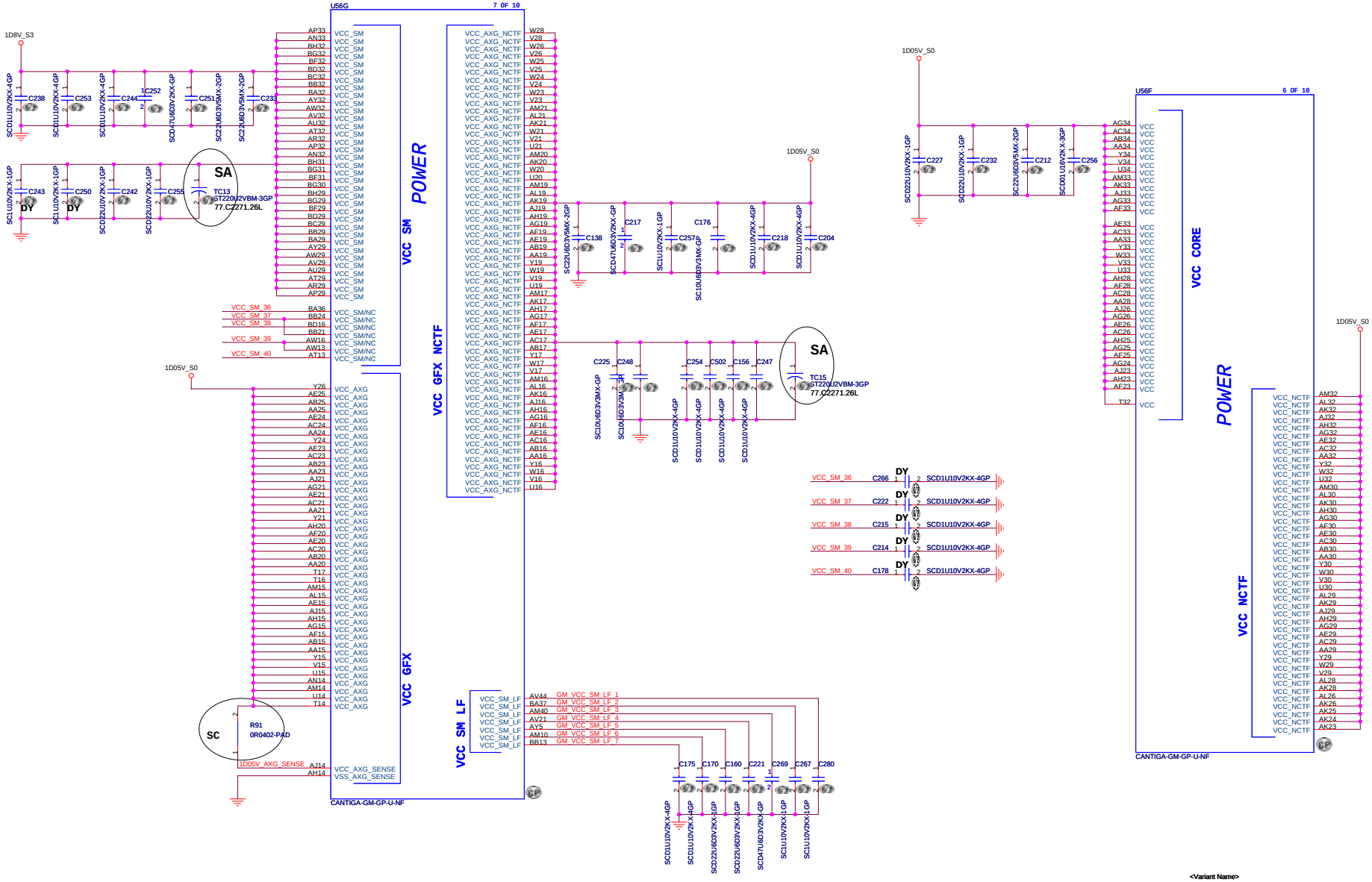
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CANTIGA(5/7)-VGA/LVDS

Size	Document Number	Rev
C	LZ2	SB

Date: Monday, June 23, 2008 Sheet 11 of 41



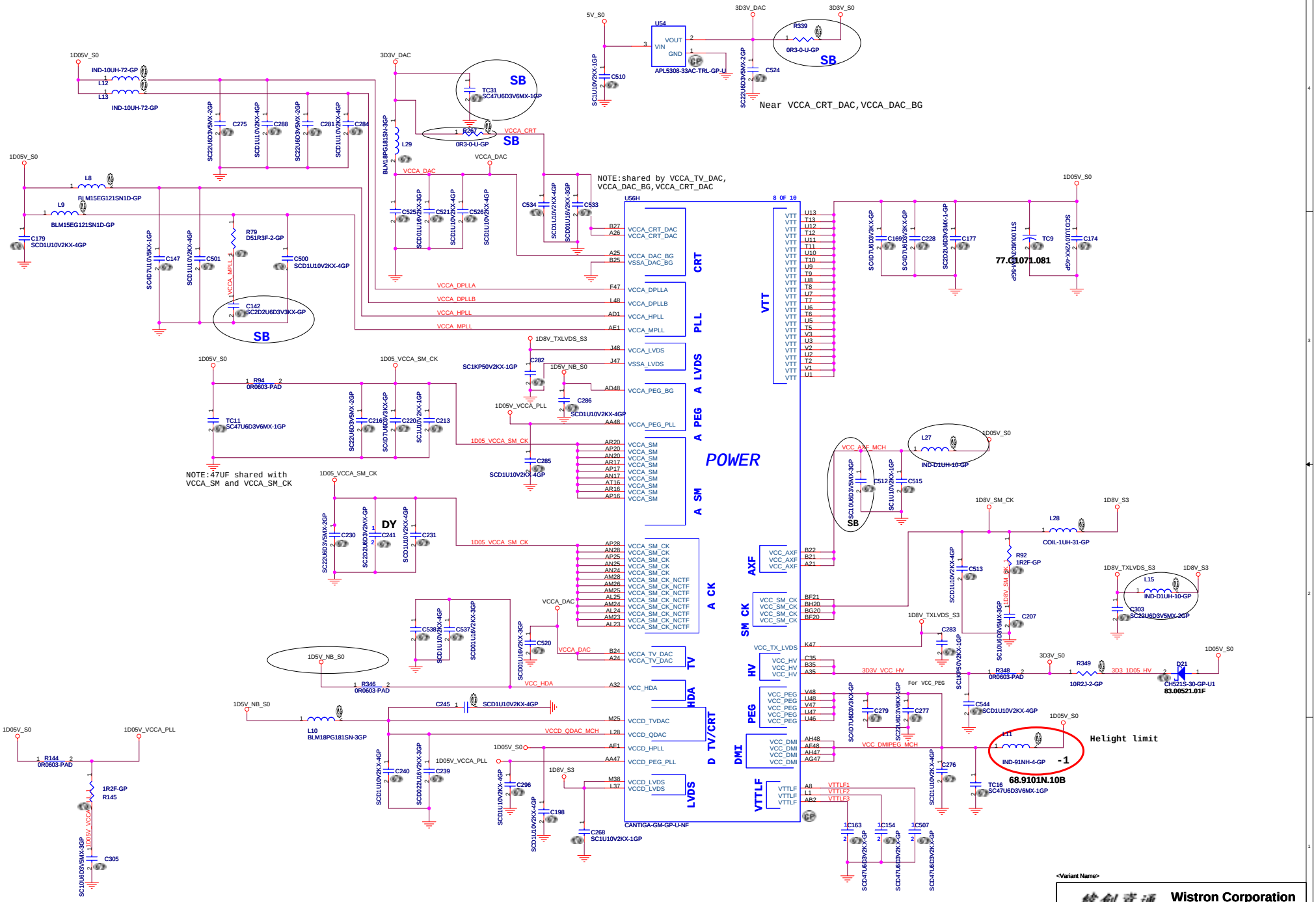
<Variant Name>

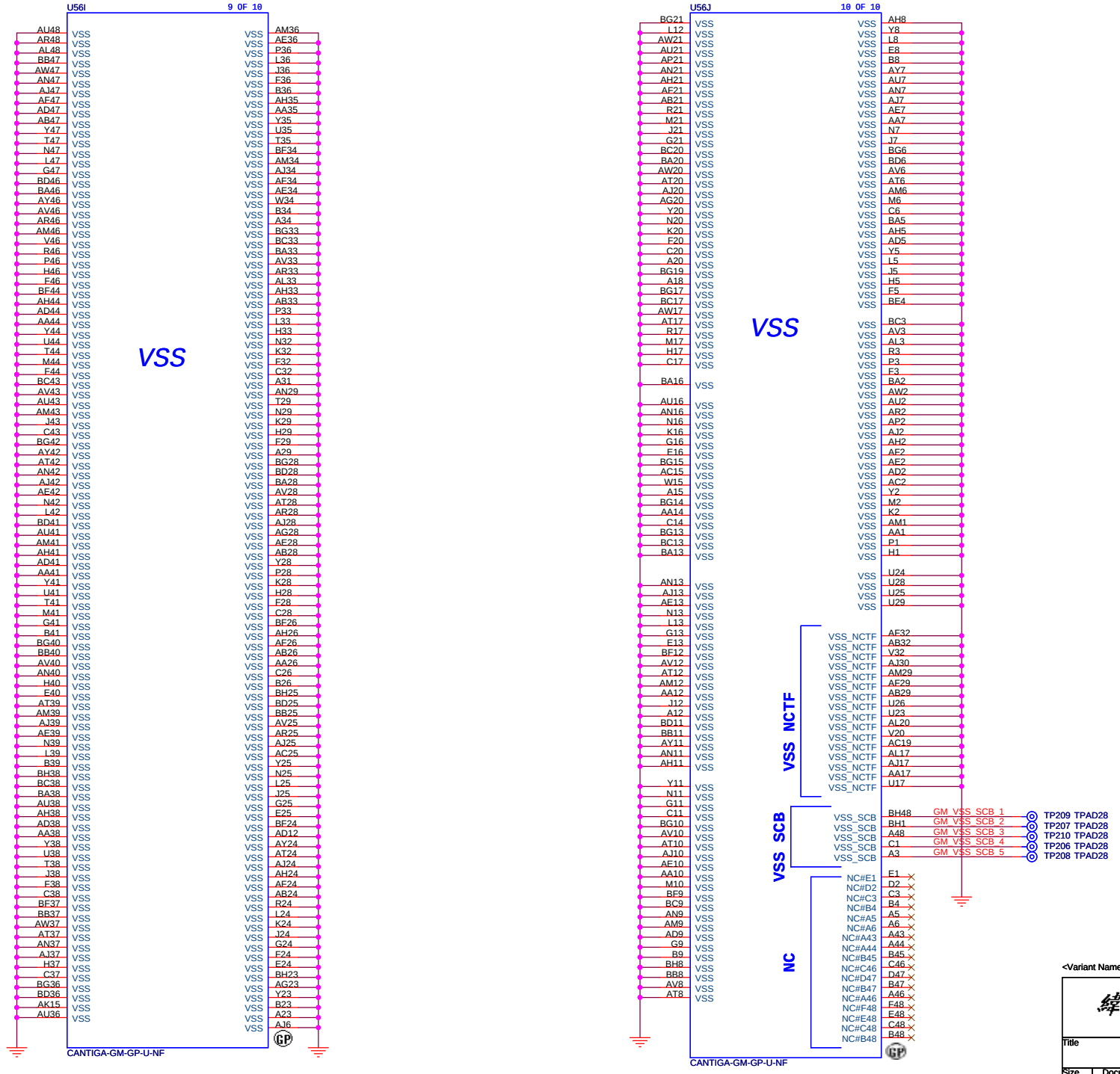
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga(5/7):VCC

Size	Document Number	Rev
C	LZ2	SB

Date: Wednesday, April 09, 2008 Sheet 12 of 41


U56H
8 OF 10
CANTIGA-GM-GP-U-NF
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
AXF
SM CK
HV
PEG
DMI
TV
HDA
D TV/CRT
VTT
VTTLF
LVDS
NOTE:shared by VCCA_TV_DAC, VCCA_DAC_BG,VCCA_CRT_DAC
Near VCCA_CRT_DAC,VCCA_DAC_BG
NOTE:47UF shared with VCCA_SM and VCCA_SM_CK
SB
DY
Helight limit
-1
68.9101N.10B
77.01071.081
83.00521.01F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
Cantiga(6/7):VCC
Size C
Document Number LZ2
Rev SB
Date: Friday, June 06, 2008
Sheet 13 of 41



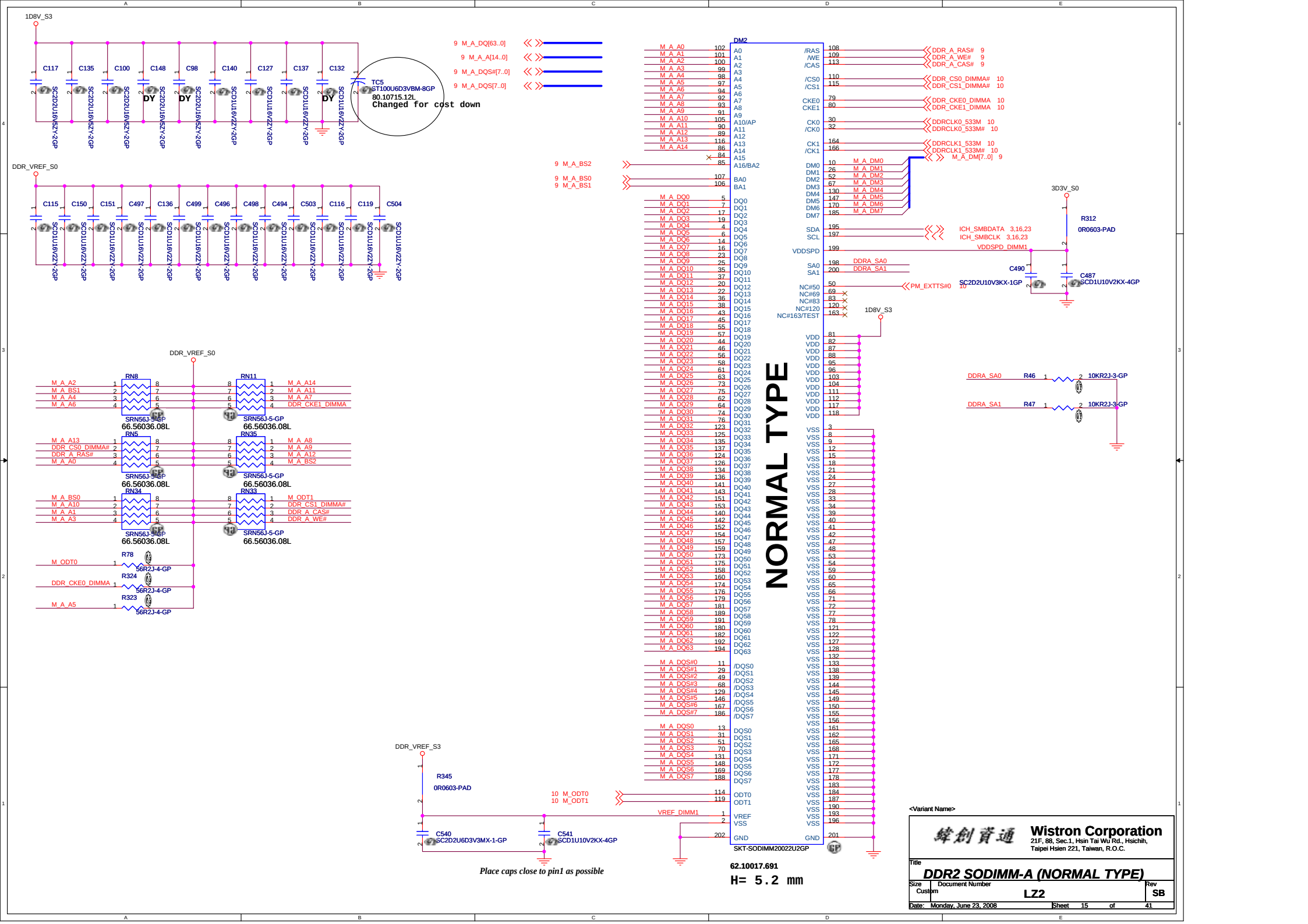
<Variant Name>

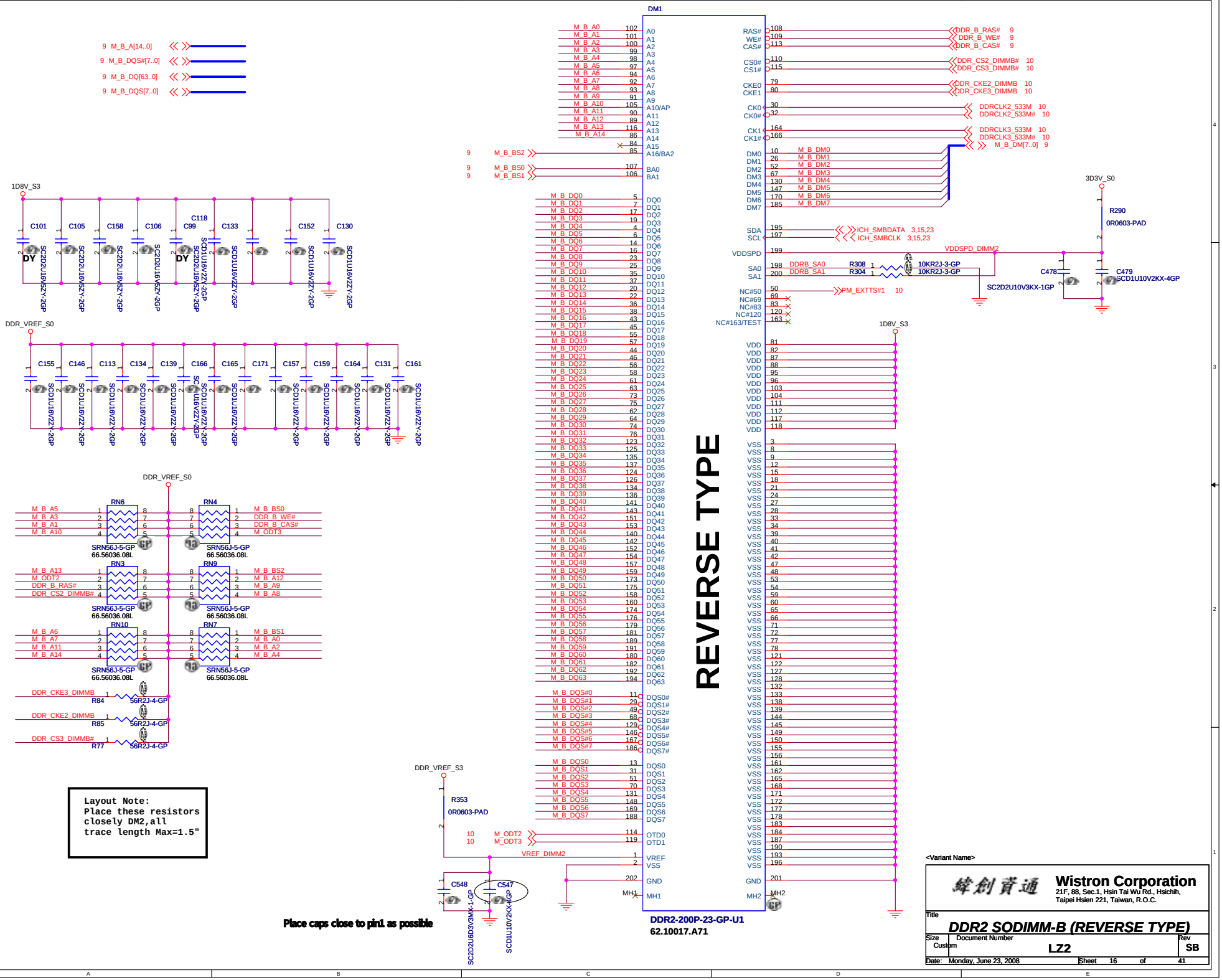
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga(8/7):GND**

Size	Document Number	Rev
A3	LZ2	SB

Date: Wednesday, April 09, 2008 Sheet 14 of 41


1D8V_S3
C117 C135 C100 C148 C98 C140 C127 C137 C132
SC2D2U16V5ZY-2GP
SCD1U16V2ZY-2GP
DY
TC5
ST100U6D3VBM-8GP
80.10715.12L
Changed for cost down
9 M_A_DQ[63..0]
9 M_A_A[14..0]
9 M_A_DQS#[7..0]
9 M_A_DQS[7..0]
DDR_VREF_S0
C115 C150 C151 C497 C136 C499 C496 C498 C494 C503 C116 C119 C504
SCD1U16V2ZY-2GP
DDR_VREF_S0
RN8 RN11 RN5 RN35 RN34 RN33
SRN56J-5-GP
66.56036.08L
M_A_A2 M_A_BS1 M_A_A4 M_A_A6
M_A_A14 M_A_A11 M_A_A7 DDR_CKE1_DIMMA
M_A_A13 DDR_CS0_DIMMA# DDR_A_RAS# M_A_A0
M_A_A8 M_A_A9 M_A_A12 M_A_BS2
M_A_BS0 M_A_A10 M_A_A1 M_A_A3
M_ODT1 DDR_CS1_DIMMA# DDR_A_CAS# DDR_A_WE#
R78 M_ODT0
R324 DDR_CKE0_DIMMA
R323 M_A_A5
56R2J-4-GP
DDR_VREF_S3
R345
0R0603-PAD
C540
SC2D2U6D3V3MX-1-GP
C541
SCD1U10V2KX-4GP
10 M_ODT0
10 M_ODT1
VREF_DIMM1
Place caps close to pin1 as possible
DM2
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15
9 M_A_BS2
9 M_A_BS0
9 M_A_BS1
A16/BA2 BA0 BA1
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
/DQS0 /DQS1 /DQS2 /DQS3 /DQS4 /DQS5 /DQS6 /DQS7
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7
ODT0 ODT1
VREF VSS GND
/RAS /WE /CAS
/CS0 /CS1
CKE0 CKE1
CK0 /CK0
CK1 /CK1
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL
VDDSPD
SA0 SA1
NC#50 NC#69 NC#83 NC#120 NC#163/TEST
VDD VSS
NORMAL TYPE
SKT-SODIMM20022U2GP
DDR_A_RAS# 9
DDR_A_WE# 9
DDR_A_CAS# 9
DDR_CS0_DIMMA# 10
DDR_CS1_DIMMA# 10
DDR_CKE0_DIMMA 10
DDR_CKE1_DIMMA 10
DDRCLK0_533M 10
DDRCLK0_533M# 10
DDRCLK1_533M 10
DDRCLK1_533M# 10
M_A_DM[7..0] 9
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
ICH_SMBDATA 3,16,23
ICH_SMBCLK 3,16,23
VDDSPD_DIMM1
DDRA_SA0
DDRA_SA1
PM_EXTTS#0 10
3D3V_S0
R312
0R0603-PAD
C490
SC2D2U10V3KX-1GP
C487
SCD1U10V2KX-4GP
DDRA_SA0 R46 10KR2J-3-GP
DDRA_SA1 R47 10KR2J-3-GP
62.10017.691
H= 5.2 mm
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 SODIMM-A (NORMAL TYPE)
Size Custom
Document Number LZ2
Rev SB
Date: Monday, June 23, 2008
Sheet 15 of 41


DM1
REVERSE TYPE
DDR2-200P-23-GP-U1
62.10017.A71
9 M_B_A[14..0]
9 M_B_DQS#[7..0]
9 M_B_DQ[63..0]
9 M_B_DQS[7..0]
1D8V_S3
DDR_VREF_S0
DDR_VREF_S3
3D3V_S0
VDDSPD_DIMM2
SC2D2U10V3KX-1GP
R290
0R0603-PAD
R353
0R0603-PAD
C101
C105
C158
C106
C118
C99
C133
C152
C130
C155
C146
C113
C134
C139
C166
C165
C171
C157
C159
C164
C131
C161
C548
C547
C478
C479
SCD1U10V2KK-4GP
RN6
RN4
RN3
RN9
RN10
RN7
SRN56J-5-GP
66.56036.08L
R84
R85
R77
56R2J-4-GP
R308
R304
10KR2J-3-GP
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_A14
M_B_BS0
M_B_BS1
M_B_BS2
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
M_B_DQ0
M_B_DQ1
M_B_DQ2
M_B_DQ3
M_B_DQ4
M_B_DQ5
M_B_DQ6
M_B_DQ7
M_B_DQ8
M_B_DQ9
M_B_DQ10
M_B_DQ11
M_B_DQ12
M_B_DQ13
M_B_DQ14
M_B_DQ15
M_B_DQ16
M_B_DQ17
M_B_DQ18
M_B_DQ19
M_B_DQ20
M_B_DQ21
M_B_DQ22
M_B_DQ23
M_B_DQ24
M_B_DQ25
M_B_DQ26
M_B_DQ27
M_B_DQ28
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M_B_DQ45
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M_B_DQ52
M_B_DQ53
M_B_DQ54
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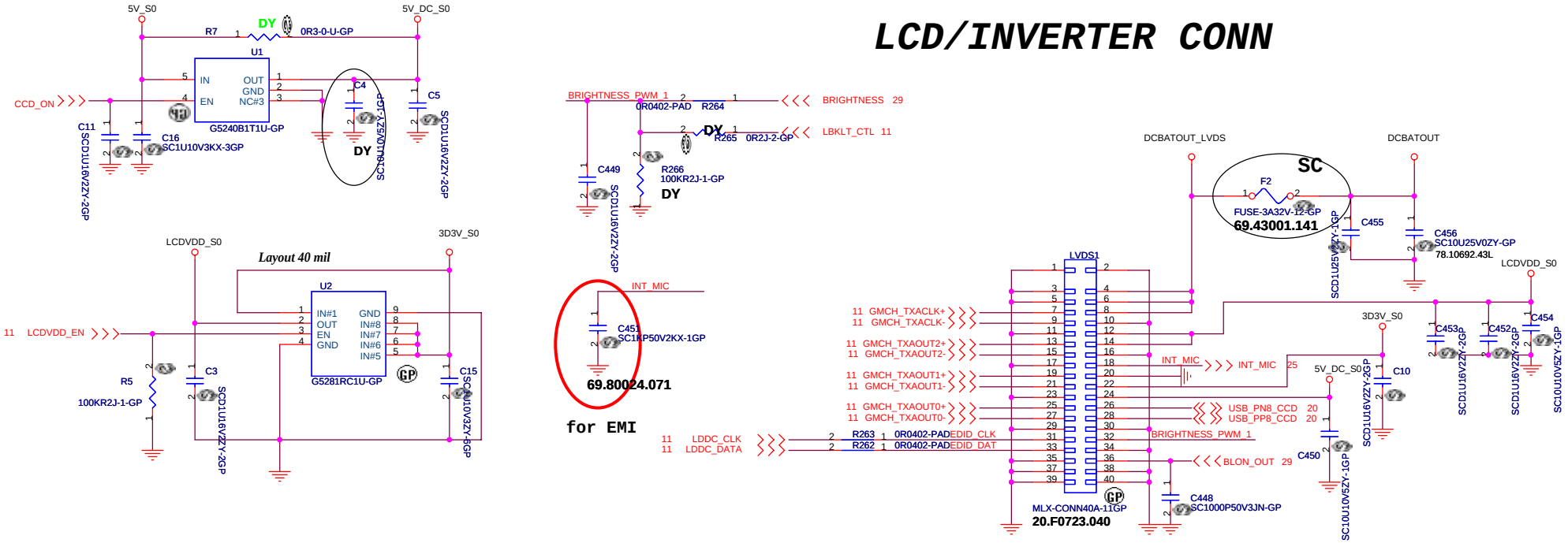
M_B_DQ58
M_B_DQ59
M_B_DQ60
M_B_DQ61
M_B_DQ62
M_B_DQ63
M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
M_ODT2
M_ODT3
VREF_DIMM2
DDR_B_RAS#
DDR_B_WE#
DDR_B_CAS#
DDR_CS2_DIMMB#
DDR_CS3_DIMMB#
DDR_CKE2_DIMMB
DDR_CKE3_DIMMB
DDRCLK2_533M
DDRCLK2_533M#
DDRCLK3_533M
DDRCLK3_533M#
ICH_SMBDATA 3,15,23
ICH_SMBCLK 3,15,23
DDRB_SA0
DDRB_SA1
PM_EXTTS#1
Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"
Place caps close to pin1 as possible
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 SODIMM-B (REVERSE TYPE)
Size
Custom
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 16 of 41

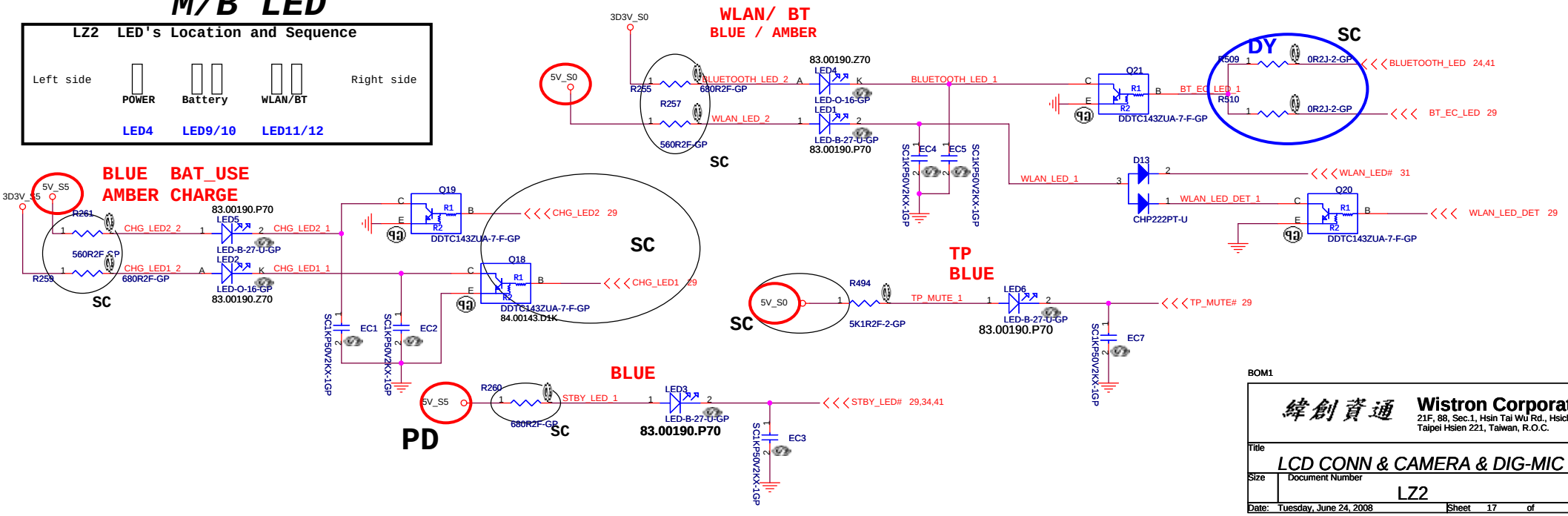
LCD/INVERTER CONN



M/B LED

LZ2 LED's Location and Sequence

Left side	POWER	Battery	WLAN/BT	Right side
	LED4	LED9/10	LED11/12	



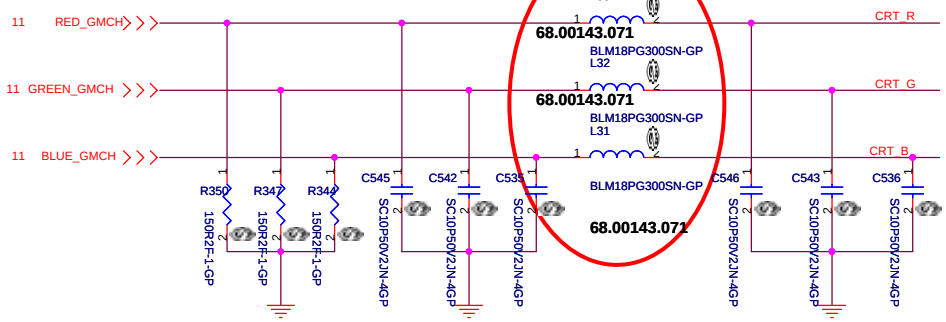
BOM1

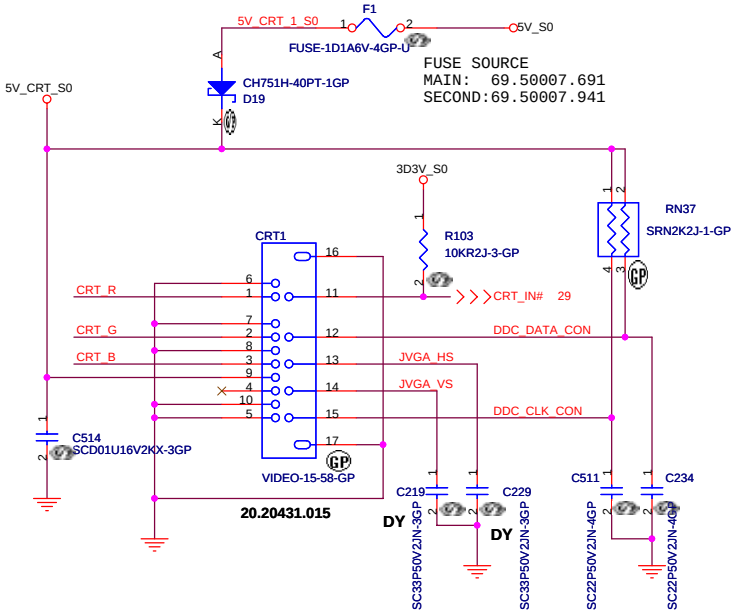
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

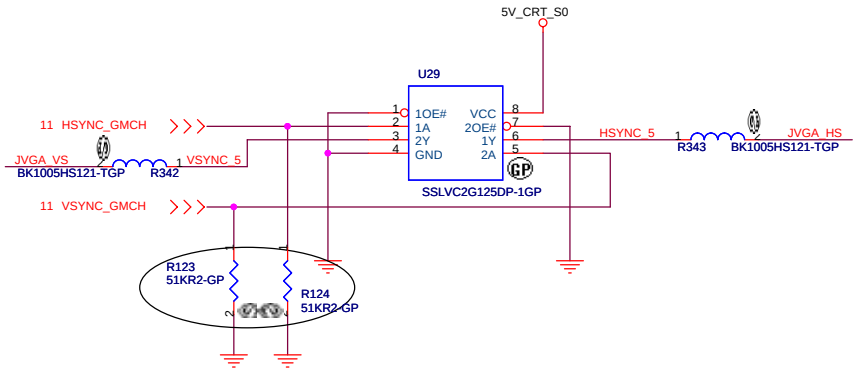
Title	LCD CONN & CAMERA & DIG-MIC	
Size	Document Number: LZ2	Rev: SB
Date: Tuesday, June 24, 2008	Sheet 17 of 41	

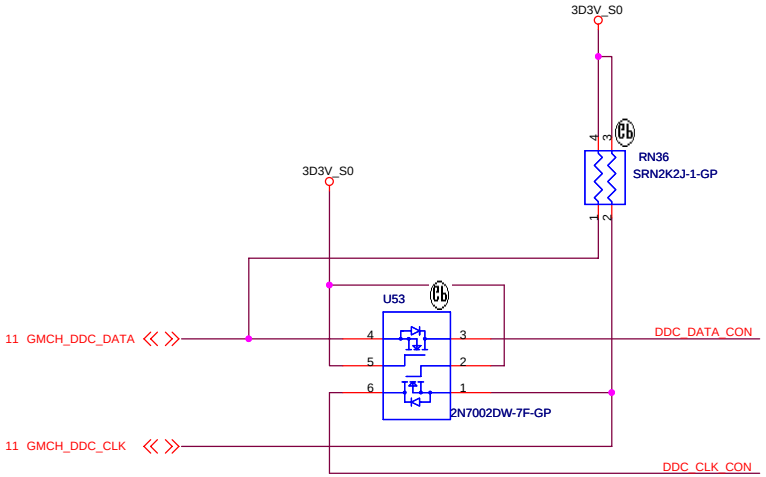
-1

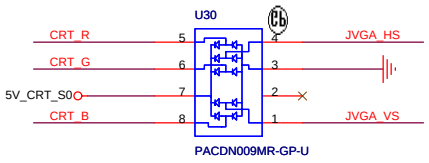
FOR EMI



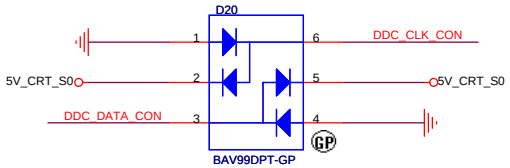






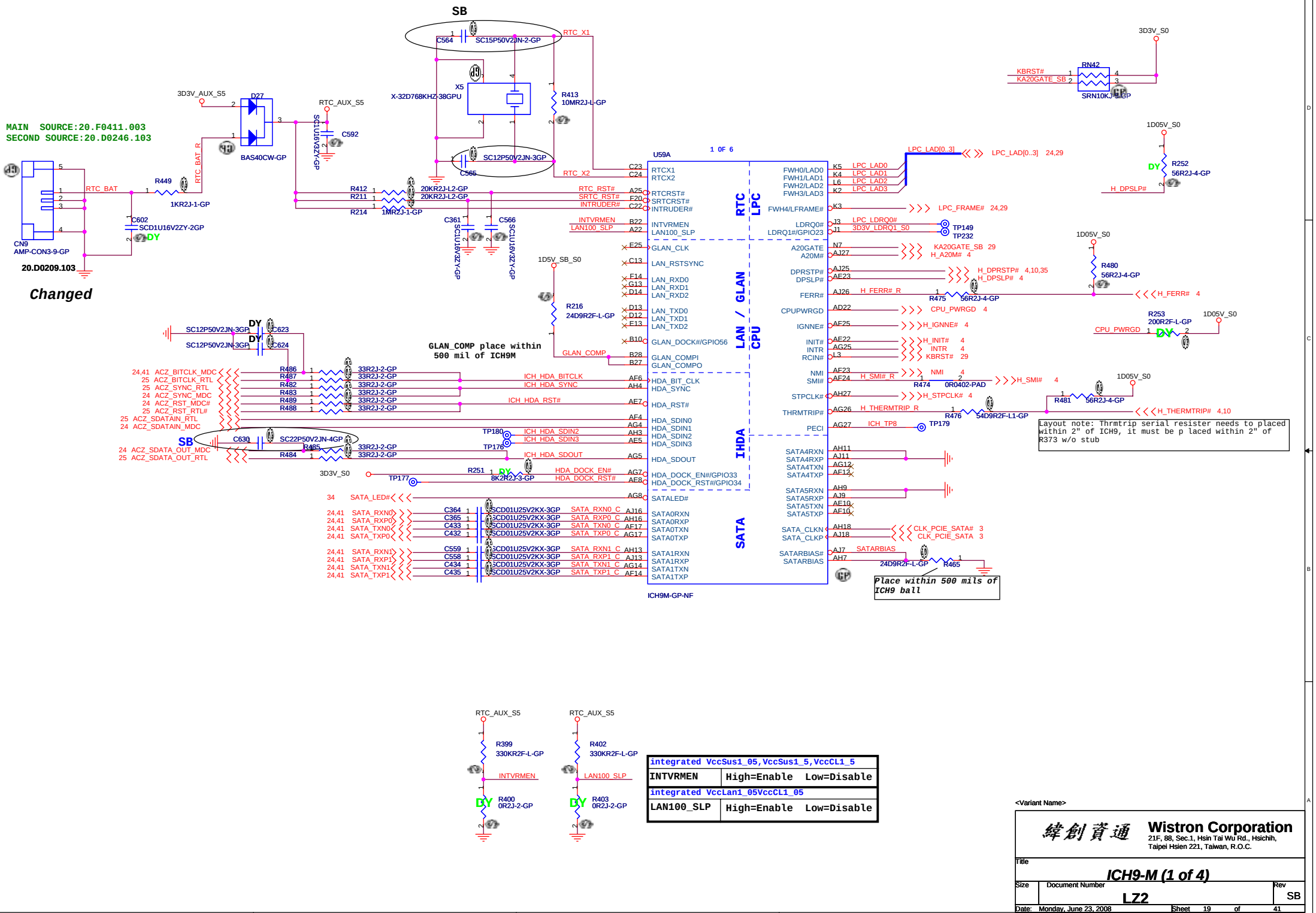


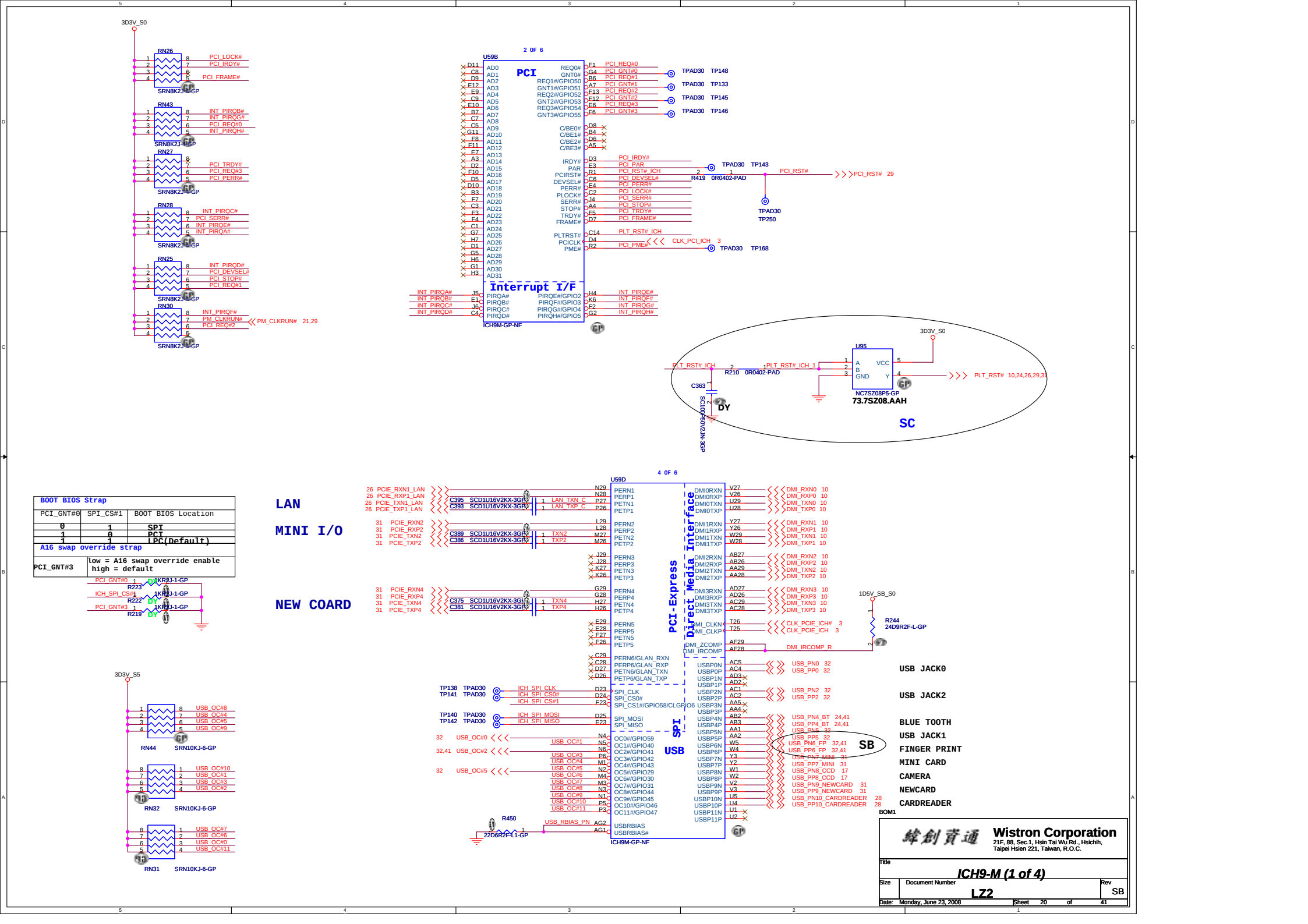
DY



DY

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT/TV Connector*	
Size	Document Number: LZ2	Rev: SB
Date: Monday, June 23, 2008	Sheet 18 of 41	


SB
MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103
20.D0209.103
Changed
U59A
1 OF 6
ICH9M-GP-NF
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
Layout note: Thrmtrip serial resister needs to placed within 2" of ICH9, it must be p laced within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
LZ2
SB
Monday, June 23, 2008
19 of 41


3D3V_S0
RN26
PCI_LOCK#
PCI_IRDY#
PCI_FRAME#
SRN8K2J-1-GP
RN43
INT_PIRQB#
INT_PIRQG#
PCI_REQ#0
INT_PIRQH#
RN27
PCI_TRDY#
PCI_REQ#3
PCI_PERR#
RN28
INT_PIRQC#
PCI_SERR#
INT_PIRQE#
INT_PIRQA#
RN25
INT_PIRQD#
PCI_DEVSEL#
PCI_STOP#
PCI_REQ#1
RN30
INT_PIRQF#
PM_CLKRUN#
PCI_REQ#2
PM_CLKRUN# 21,29
2 OF 6
U59B
PCI
REQ0#
GNT0#
REQ1#/GPIO50
GNT1#/GPIO51
REQ2#/GPIO52
GNT2#/GPIO53
REQ3#/GPIO54
GNT3#/GPIO55
PCI_REQ#0
PCI_GNT#0
PCI_REQ#1
PCI_GNT#1
PCI_REQ#2
PCI_GNT#2
PCI_REQ#3
PCI_GNT#3
TPAD30 TP148
TPAD30 TP133
TPAD30 TP145
TPAD30 TP146
C/BE0#
C/BE1#
C/BE2#
C/BE3#
IRDY#
PAR
PCIRST#
DEVSEL#
PERR#
PLOCK#
SERR#
STOP#
TRDY#
FRAME#
PCI_IRDY#
PCI_PAR
PCI_RST# ICH
PCI_DEVSEL#
PCI_PERR#
PCI_LOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
TPAD30 TP143
R419 0R0402-PAD
PCI_RST#
PCI_RST# 29
TPAD30 TP250
PLTRST#
PCICLK
PME#
PLT_RST# ICH
CLK_PCI_ICH 3
PCI_PME#
TPAD30 TP168
Interrupt I/F
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
ICH9M-GP-NF
3D3V_S0
U95
PLT_RST# ICH
R210 0R0402-PAD
PLT_RST# ICH_1
A
B
GND
VCC
Y
NC7SZ08P5-GP
73.7SZ08.AAH
PLT_RST# 10,24,26,29,31
C363
SCD100V50V2JN-3GP
DY
SC
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable high = default
PCI_GNT#0 R223 1KR2J-1-GP
ICH_SPI_CS#1 R222 1KR2J-1-GP
PCI_GNT#3 R219 1KR2J-1-GP
DY
LAN
MINI I/O
NEW COARD
4 OF 6
U59D
PCI-Express
Direct Media Interface
SPI
USB
26 PCIE_RXN1_LAN
26 PCIE_RXP1_LAN
26 PCIE_TXN1_LAN
26 PCIE_TXP1_LAN
C395 SCD1U16V2KX-3GP
C393 SCD1U16V2KX-3GP
LAN_TXN_C
LAN_TXP_C
31 PCIE_RXN2
31 PCIE_RXP2
31 PCIE_TXN2
31 PCIE_TXP2
C389 SCD1U16V2KX-3GP
C386 SCD1U16V2KX-3GP
TXN2
TXP2
31 PCIE_RXN4
31 PCIE_RXP4
31 PCIE_TXN4
31 PCIE_TXP4
C375 SCD1U16V2KX-3GP
C381 SCD1U16V2KX-3GP
TXN4
TXP4
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_RXN0 10
DMI_RXP0 10
DMI_TXN0 10
DMI_TXP0 10
DMI_RXN1 10
DMI_RXP1 10
DMI_TXN1 10
DMI_TXP1 10
DMI_RXN2 10
DMI_RXP2 10
DMI_TXN2 10
DMI_TXP2 10
DMI_RXN3 10
DMI_RXP3 10
DMI_TXN3 10
DMI_TXP3 10
CLK_PCIE_ICH# 3
CLK_PCIE_ICH 3
1D5V_SB_S0
R244 24D9R2F-L-GP
DMI_IRCOMP_R
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USB_PN0 32
USB_PP0 32
USB_PN2 32
USB_PP2 32
USB_PN4_BT 24,41
USB_PP4_BT 24,41
USB_PN5 32
USB_PP5 32
USB_PN6_FP 32,41
USB_PP6_FP 32,41
USB_PN7_MINI 31
USB_PP7_MINI 31
USB_PN8_CCD 17
USB_PP8_CCD 17
USB_PN9_NEWCARD 31
USB_PP9_NEWCARD 31
USB_PN10_CARDREADER 28
USB_PP10_CARDREADER 28
SB
USB JACK0
USB JACK2
BLUE TOOTH
USB JACK1
FINGER PRINT
MINI CARD
CAMERA
NEWCARD
CARDREADER
BOM1
TP138 TPAD30
TP141 TPAD30
ICH_SPI_CLK
ICH_SPI_CS0#
ICH_SPI_CS#1
SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
TP140 TPAD30
TP142 TPAD30
ICH_SPI_MOSI
ICH_SPI_MISO
SPI_MOSI
SPI_MISO
32 USB_OC#0
32,41 USB_OC#2
32 USB_OC#5
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47
USB_OC#1
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9
USB_OC#10
USB_OC#11
R450
USB_RBIAS_PN
USB_RBIAS#
USBRBIAS
USBRBIAS#
22D6R2F-L1-GP
ICH9M-GP-NF
3D3V_S5
RN44 SRN10KJ-6-GP
USB_OC#8
USB_OC#4
USB_OC#5
USB_OC#9
RN32 SRN10KJ-6-GP
USB_OC#10
USB_OC#1
USB_OC#3
USB_OC#2
RN31 SRN10KJ-6-GP
USB_OC#7
USB_OC#6
USB_OC#0
USB_OC#11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
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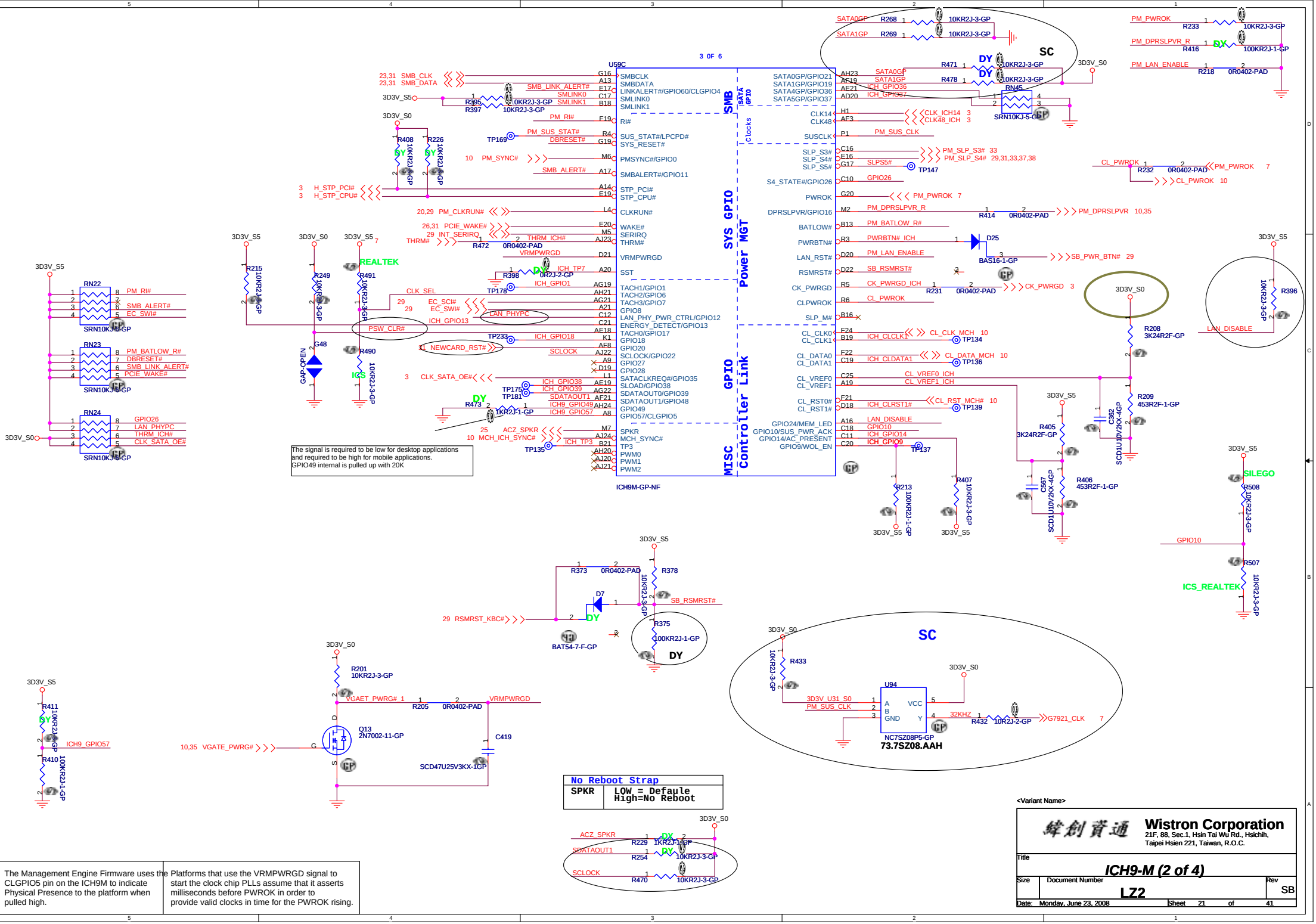
Date: Monday, June 23, 2008
Sheet 20 of 41


U59C
3 OF 6
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
SC
REALTEK
ICS
SILEGO
ICS_REALTEK
RN22
RN23
RN24
SRN10KJ-5-GP
PM_RI#
SMB_ALERT#
EC_SWI#
PM_BATLOW_R#
DBRESET#
SMB_LINK_ALERT#
PCIE_WAKE#
GPIO26
LAN_PHYPC
THRM_ICH#
CLK_SATA_OE#
SMB_CLK
SMB_DATA
SMB_LINK_ALERT#
PM_SUS_STAT#
DBRESET#
PM_SYNC#
H_STP_PCI#
H_STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
THRM#
CLK_SEL
EC_SCI#
EC_SWI#
LAN_PHYPC
ICH_GPIO13
PSW_CLR#
NEWCARD_RST#
CLK_SATA_OE#
ACZ_SPKR
MCH_ICH_SYNC#
ICH_GPIO1
ICH_GPIO18
ICH_GPIO38
ICH_GPIO39
SDATAOUT1
ICH9_GPIO49
ICH9_GPIO57
ICH_TP3
ICH_TP7
SATA0GP
SATA1GP
ICH_GPIO36
ICH_GPIO37
CLK_ICH14
CLK48_ICH
PM_SUS_CLK
PM_SLP_S3#
PM_SLP_S4#
SLPS5#
GPIO26
PM_PWROK
PM_DPRSLPVR_R
PM_BATLOW_R#
PWRBTN#_ICH
LAN_RST#
RSMRST#
CK_PWRGD_ICH
CL_PWROK
CL_CLK_MCH
ICH_CLCLK1
CL_DATA_MCH
ICH_CLDATA1
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST_MCH#
ICH_CLRST1#
LAN_DISABLE
GPIO10
ICH_GPIO14
ICH_GPIO9
SB_PWR_BTN#
SB_RSMRST#
PM_PWROK
PM_DPRSLPVR_R
PM_LAN_ENABLE
CL_PWROK
R268
R269
R471
R478
R233
R416
R218
R414
R232
R231
R208
3K24R2F-GP
R209
453R2F-1-GP
R405
3K24R2F-GP
R406
453R2F-1-GP
R213
100KR2J-1-GP
R407
10KR2J-3-GP
R508
R507
R396
LAN_DISABLE
D25
BAS16-1-GP
TP134
TP136
TP139
TP137
TP147
TP169
TP178
TP233
TP175
TP181
TP135
R215
R249
R491
R490
R398
R472
R395
R397
R408
R226
R473
G48
GAP-OPEN
R373
R378
D7
BAT54-7-F-GP
R375
100KR2J-1-GP
R201
10KR2J-3-GP
VGAET_PWRG#_1
R205
VRMPWRGD
Q13
2N7002-11-GP
C419
SCD47U25V3KX-1GP
R411
R410
ICH9_GPIO57
10,35 VGATE_PWRG#
R433
U94
NC7SZ08P5-GP
73.7SZ08.AAH
3D3V_U31_S0
32KHZ
R432
G7921_CLK
R229
R254
R470
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
The signal is required to be low for desktop applications and required to be high for mobile applications. GPIO49 internal is pulled up with 20K
The Management Engine Firmware uses the CLGPIO5 pin on the ICH9M to indicate Physical Presence to the platform when pulled high.
Platforms that use the VRMPWRGD signal to start the clock chip PLLs assume that it asserts milliseconds before PWROK in order to provide valid clocks in time for the PWROK rising.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
ICH9-M (2 of 4)
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U59F

VccRTC=6uA in G3

Vcc1_5_B=646mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

V5REF=2mA

V5REF_Sus=2mA

Layout Note: Place near ICH9

VccSATAPLL=47mA

Vcc1_5_A=1.342A

USBPLL=11mA

VccLAN3_3=19mA

VccLAN3_3=19mA in S0;78mA in S3/S4/S5,The current for this rail in S3 and S4/S5 is based on the integrated LAN running at 10/100.

VccGLANPLL=23mA

VccGLAN1_5=80mA

VccGLAN3_3=1mA

Vcc1_05=1.634A

Layout Note:Place near ICH9M

VccDMIPLL=23mA

VccDMI=48mA

V_CPU_IO=2mA

VCC3_3=308mA

VccHDA=11mA

VccSusHDA=11mA

VccSus3_3=212mA

VccCL3_3=19mA

ICH9M-GP-NF

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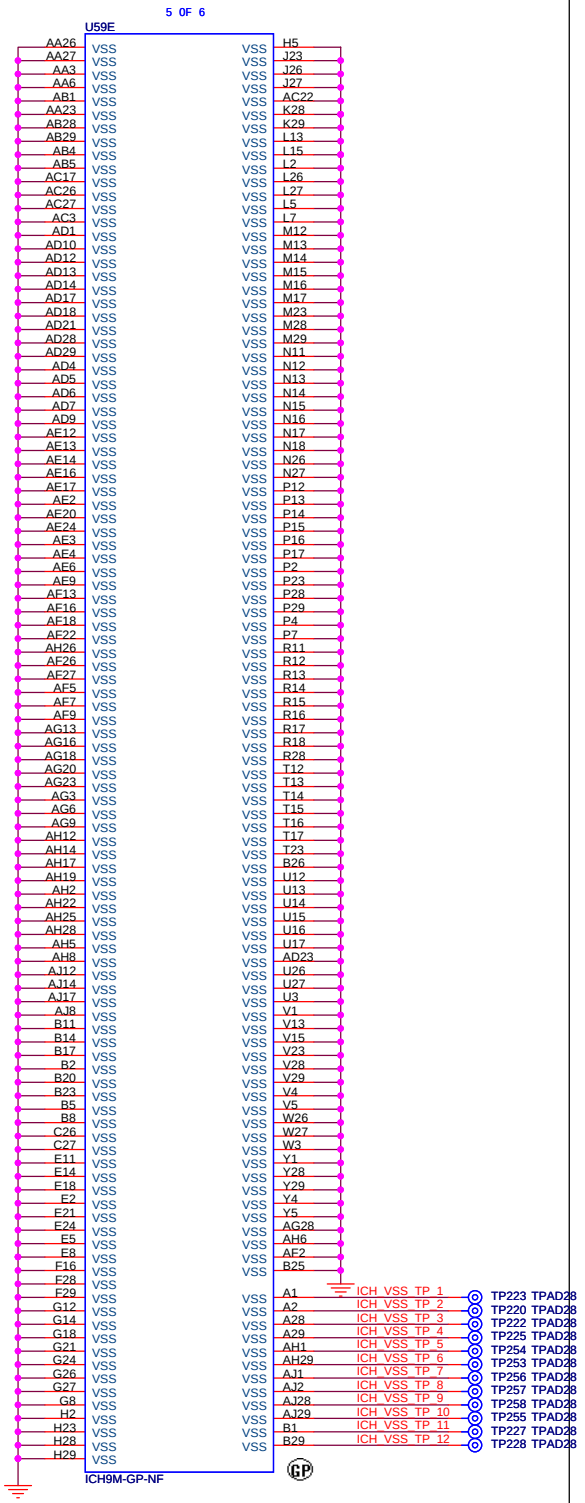
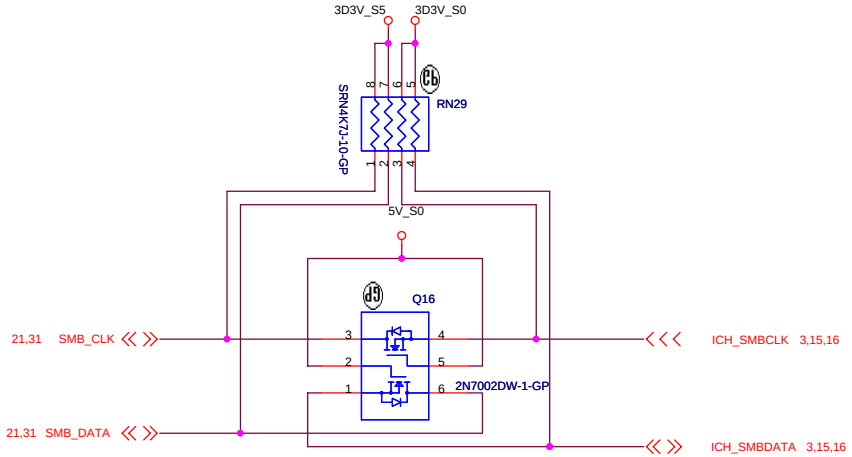
Title: ICH9-M (3 of 4)

Size: | Document Number: LZ2 | Rev: SB

Date: Tuesday, May 13, 2008 | Sheet 22 of 41





Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *ICH9-M (4 of 4)*		
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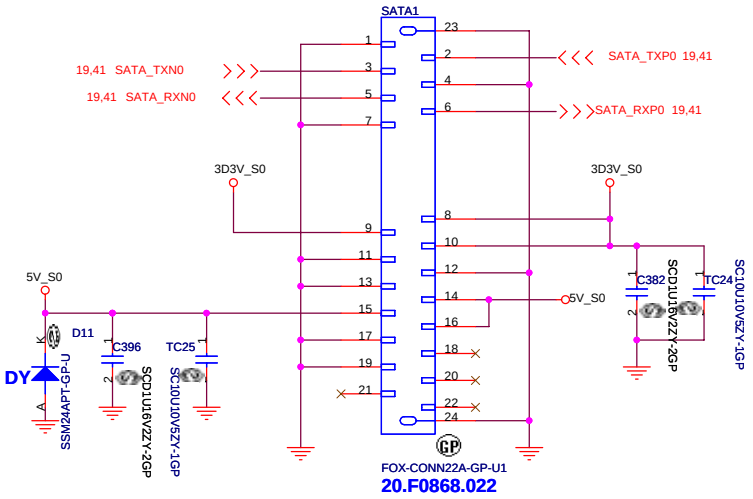
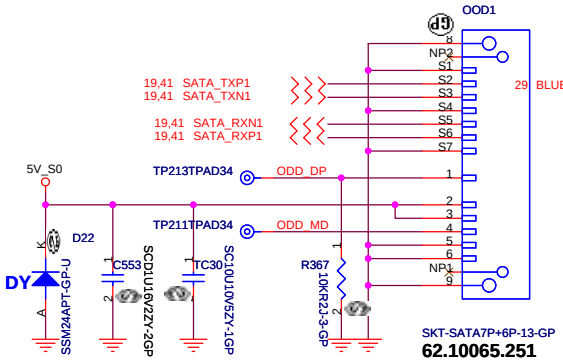
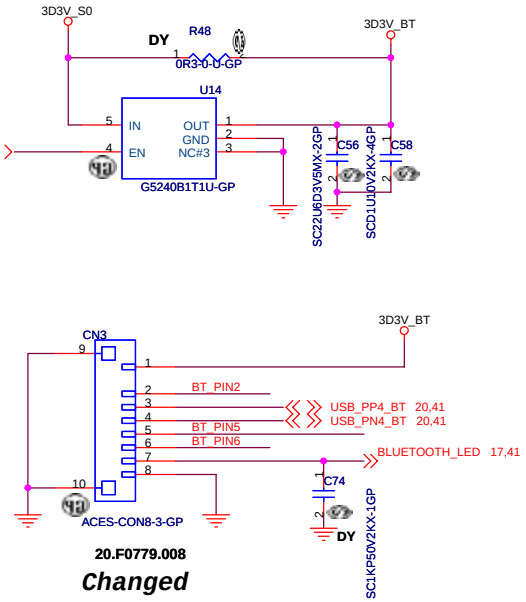
SATA HD Connector



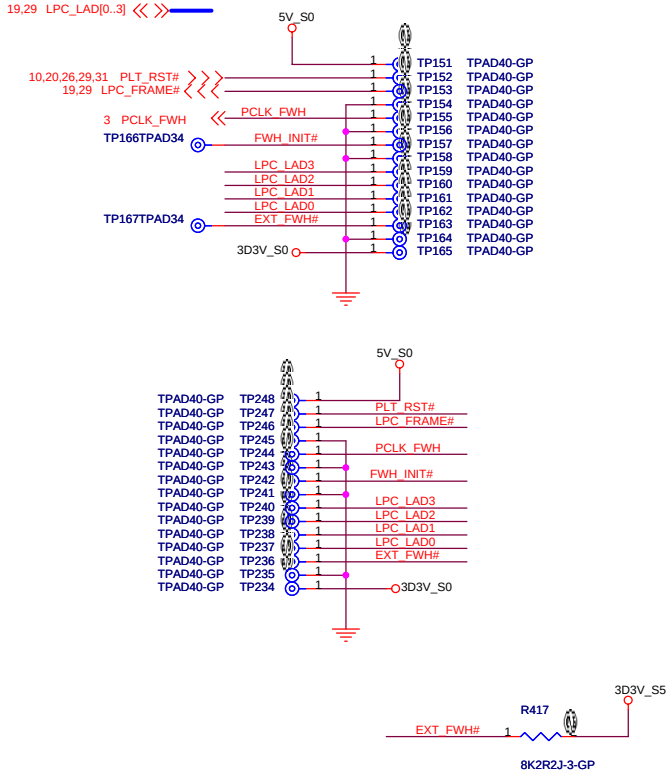
ODD Connector



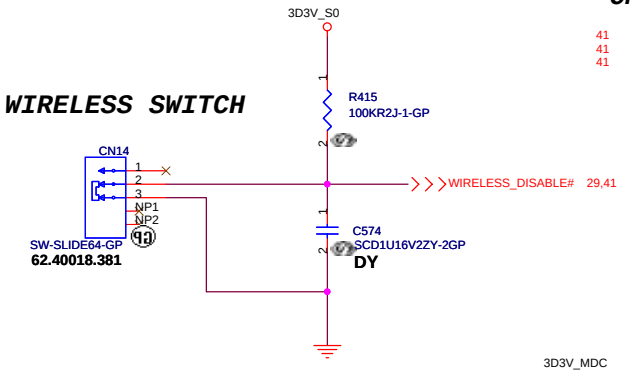
BT CONNECTOR



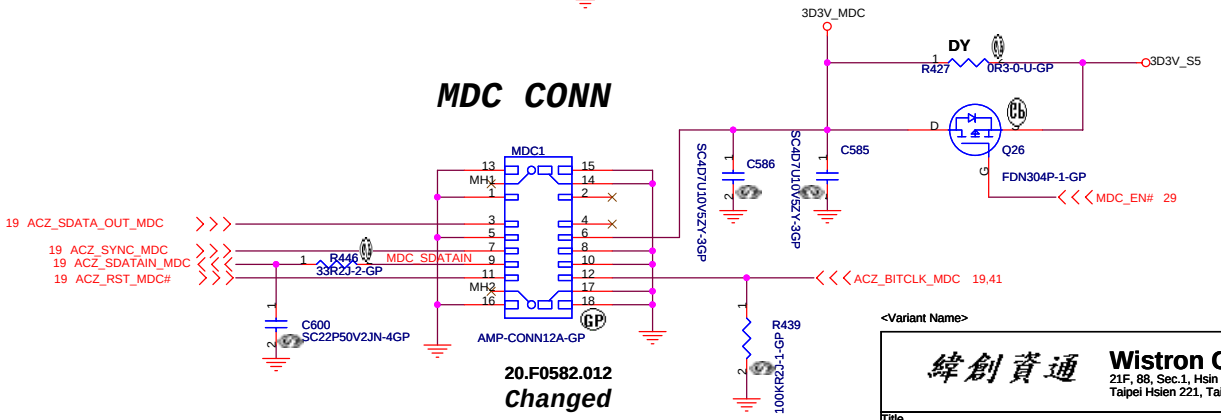
GOLDEN FINGER FOR DEBUG BOARD



WIRELESS SWITCH



MDC CONN



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/CDROM/DEBUG /MODEM/WIRELESS SW/BT**

Size	Document Number	Rev
	LZ2	SB

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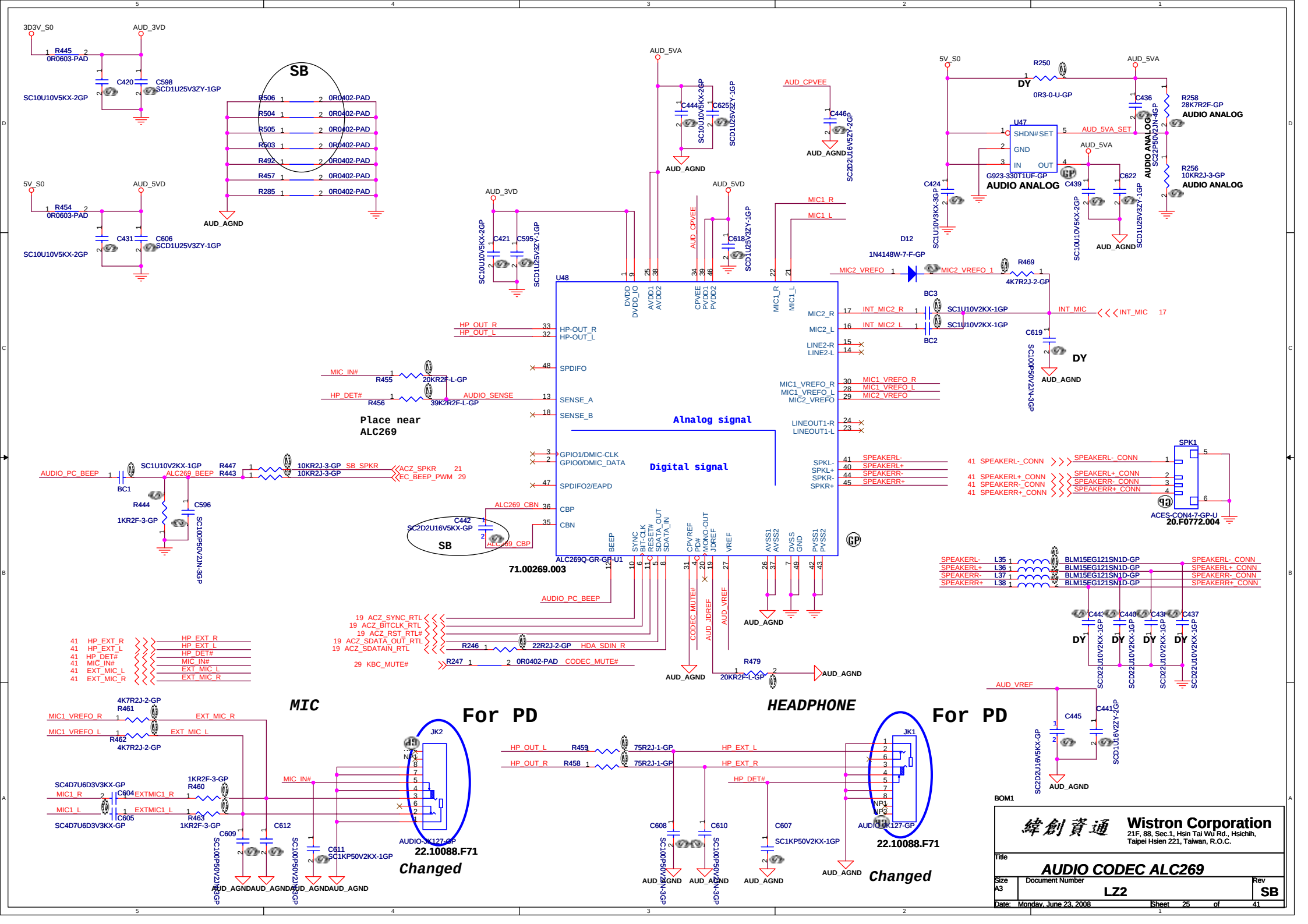
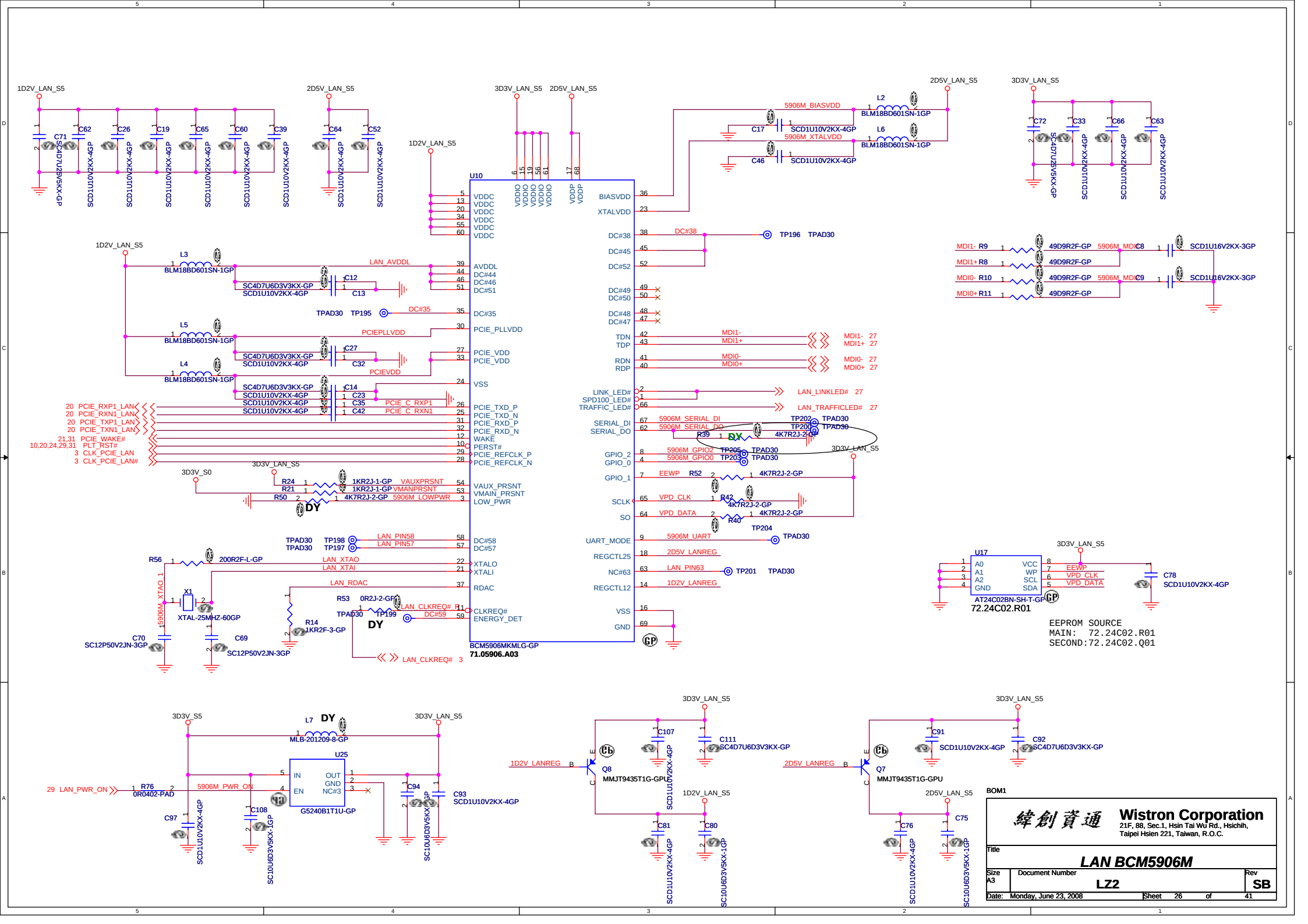

3D3V_S0
AUD_3VD
R445
0R0603-PAD
C420
SC10U10V5KX-2GP
C598
SCD1U25V3ZY-1GP
SB
R506
R504
R505
R503
R492
R457
R285
0R0402-PAD
AUD_AGND
5V_S0
AUD_5VD
R454
C431
C606
AUD_5VA
C444
C625
C446
SC2D2U16V5ZY-2GP
AUD_CPVEE
AUD_3VD
C421
C595
C618
MIC1_R
MIC1_L
D12
1N4148W-7-F-GP
MIC2_VREFO
MIC2_VREFO_1
R469
4K7R2J-2-GP
U48
DVDD
DVDD_IO
AVDD1
AVDD2
CPVEE
PVDD1
PVDD2
HP_OUT_R
HP_OUT_L
MIC2_R
MIC2_L
LINE2-R
LINE2-L
SPDIFO
SENSE_A
SENSE_B
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
LINEOUT1-R
LINEOUT1-L
GPIO1/DMIC-CLK
GPIO0/DMIC_DATA
SPDIFO2/EAPD
CBP
CBN
SPKL-
SPKL+
SPKR-
SPKR+
BEEP
SYNC
BIT-CLK
RESET#
SDATA_OUT
SDATA_IN
CPVREF
PD#
MONO-OUT
JDREF
VREF
AVSS1
AVSS2
DVSS
GND
PVSS1
PVSS2
ALC269Q-GR-GP-U1
71.00269.003
Alnalog signal
Digital signal
Place near
ALC269
MIC_IN#
HP_DET#
R455
20KR2F-L-GP
R456
39K2R2F-L-GP
AUDIO_SENSE
INT_MIC2_R
INT_MIC2_L
BC3
BC2
SC1U10V2KX-1GP
INT_MIC
C619
DY
SC100P50V2JN-3GP
5V_S0
R250
0R3-0-U-GP
U47
SHDN#
SET
GND
IN
OUT
G923-330T1UF-GP
AUDIO ANALOG
AUD_5VA_SET
C436
C424
C439
C622
R258
28K7R2F-GP
R256
10KR2J-3-GP
SC22P50V2JN-4GP
SC1U10V3KX-3GP
SC10U10V5KX-2GP
SCD1U25V3ZY-1GP
AUDIO_PC_BEEP
ALC269_BEEP
R447
R443
10KR2J-3-GP
SB_SPKR
ACZ_SPKR
EC_BEEP_PWM
BC1
R444
1KR2F-3-GP
C596
ALC269_CBN
ALC269_CBP
C442
SC2D2U16V5KX-GP
SPEAKERL-
SPEAKERL+
SPEAKERR-
SPEAKERR+
SPK1
ACES-CON4-7-GP-U
20.F0772.004
BLM15EG121SN1D-GP
SC22U10V2KX-1GP
DY
AUD_VREF
C445
SC2D2U16V5KX-GP
SCD1U16V2ZY-2GP
19 ACZ_SYNC_RTL
19 ACZ_BITCLK_RTL
19 ACZ_RST_RTL#
19 ACZ_SDATA_OUT_RTL
19 ACZ_SDATAIN_RTL
29 KBC_MUTE#
R246
22R2J-2-GP
HDA_SDIN_R
R247
0R0402-PAD
CODEC_MUTE#
R479
20KR2F-L-GP
41 HP_EXT_R
41 HP_EXT_L
41 HP_DET#
41 MIC_IN#
41 EXT_MIC_L
41 EXT_MIC_R
MIC
For PD
HEADPHONE
For PD
R461
R462
4K7R2J-2-GP
MIC1_VREFO_R
MIC1_VREFO_L
EXT_MIC_R
EXT_MIC_L
SC4D7U6D3V3KX-GP
C604
C605
R460
R463
1KR2F-3-GP
EXTMIC1_R
EXTMIC1_L
C609
C612
C611
SC1KP50V2KX-1GP
JK2
AUDIO-JK127-GP
22.10088.F71
Changed
R459
R458
75R2J-1-GP
HP_EXT_L
HP_EXT_R
HP_DET#
C608
C610
C607
JK1
AUDIO-JK127-GP
22.10088.F71
Changed
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC ALC269
Size
A3
Document Number
LZ2
Rev
SB
Date: Monday, June 23, 2008
Sheet 25 of 41


1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
U10
BCM5906MKMLG-GP
71.05906.A03
5906M_BIASVDD
5906M_XTALVDD
LAN_AVDDL
PCIEPLLVDD
PCIEVDD
PCIE_RXP1_LAN
PCIE_RXN1_LAN
PCIE_TXP1_LAN
PCIE_TXN1_LAN
PCIE_WAKE#
PLT_RST#
CLK_PCIE_LAN
CLK_PCIE_LAN#
LAN_LINKLED#
LAN_TRAFFICLED#
5906M_SERIAL_DI
5906M_SERIAL_DO
5906M_GPIO2
5906M_GPIO0
EEWP
VPD_CLK
VPD_DATA
5906M_UART
2D5V_LANREG
1D2V_LANREG
LAN_PIN63
LAN_XTAO
LAN_XTAI
LAN_RDAC
LAN_CLKREQ#
LAN_PIN58
LAN_PIN57
VAUXPRSNT
VMAINPRSNT
5906M_LOWPWR
MDI1-
MDI1+
MDI0-
MDI0+
XTAL-25MHZ-60GP
MLB-201209-8-GP
G5240B1T1U-GP
MMJT9435T1G-GPU
AT24C02BN-SH-T-GP
72.24C02.R01
EEPROM SOURCE
MAIN: 72.24C02.R01
SECOND:72.24C02.Q01
29 LAN_PWR_ON
5906M_PWR_ON
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN BCM5906M
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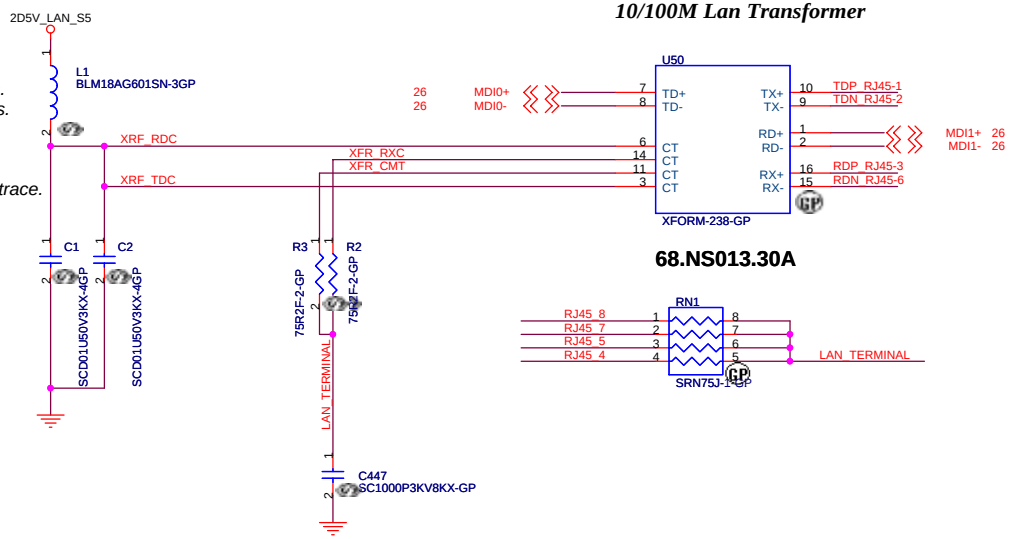
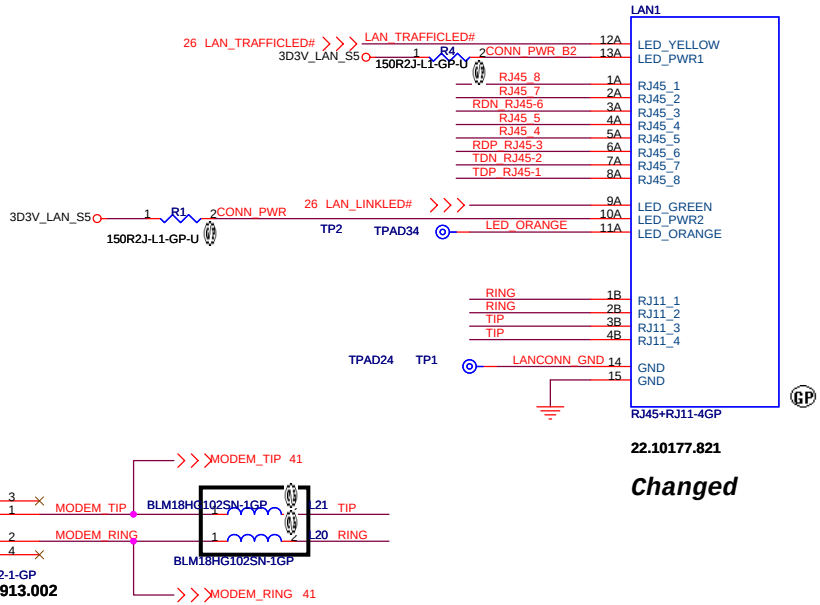
10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN connector/NEW CARD/SIM		
Size: A3	Document Number: LZ2	Rev: SB
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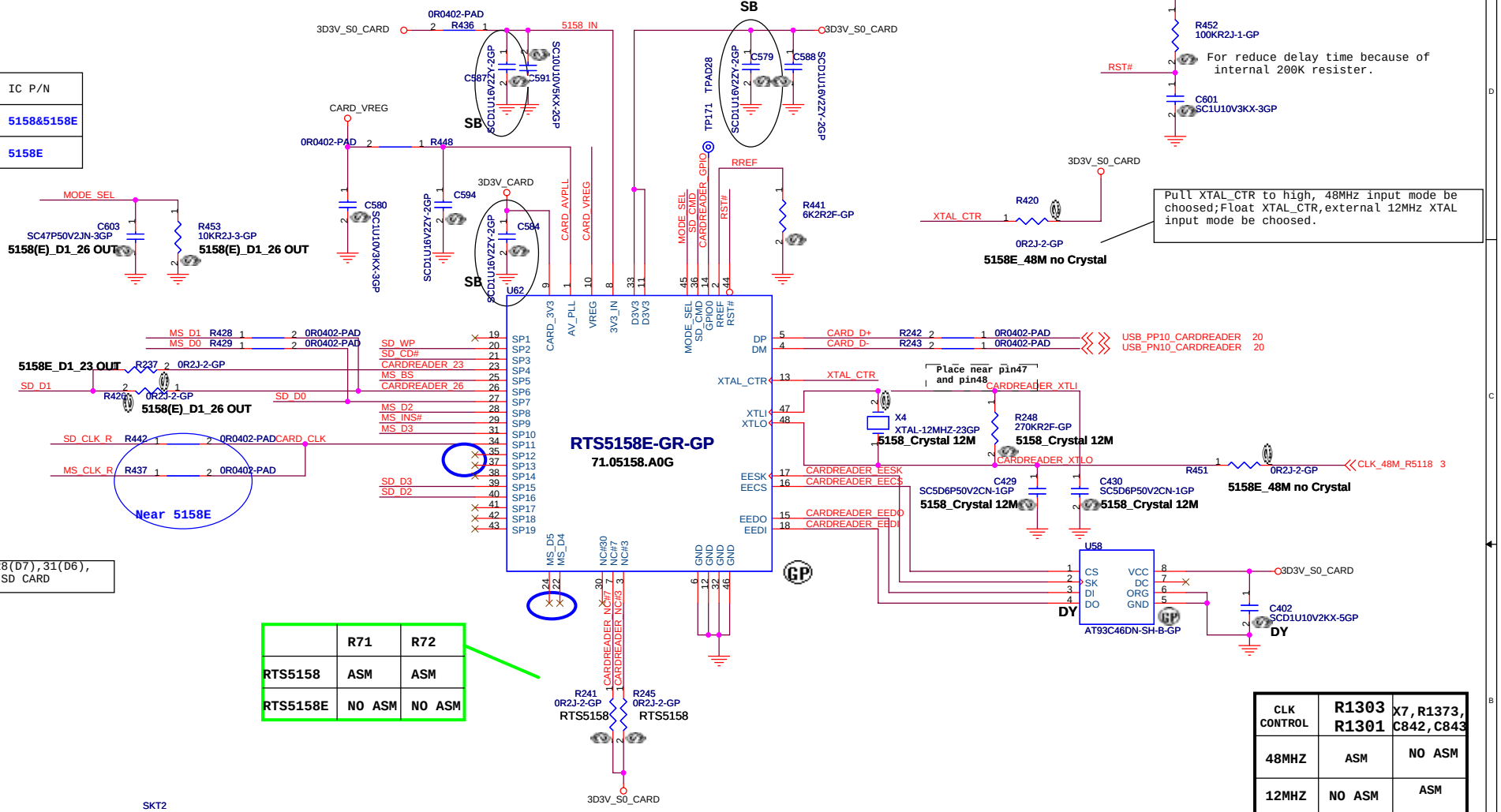
For 3in1 SD/MMC/MS CARD

R1302	C38	SD_D1 OUT FROM	IC P/N
10K	47 PF	PIN 26(MS_D1)	5158&5158E
NC	NC	PIN 23	5158E



*Vendor suggest: SD section--pin 28(D7),31(D6),
**35(D5),37(D4) RESERVED FOR 8PIN SD CARD

	R71	R72
RTS5158	ASM	ASM
RTS5158E	NO ASM	NO ASM

CLK CONTROL	R1303 R1301	X7,R1373, C842,C843
48MHZ	ASM	NO ASM
12MHZ	NO ASM	ASM

Pin 13 (XTAL CTL)	Clock source	Remark
Floating	12MHz crystal input	
Pull high	Clock generator's 48MHz input	Input to RTS5158E(Pin 48)

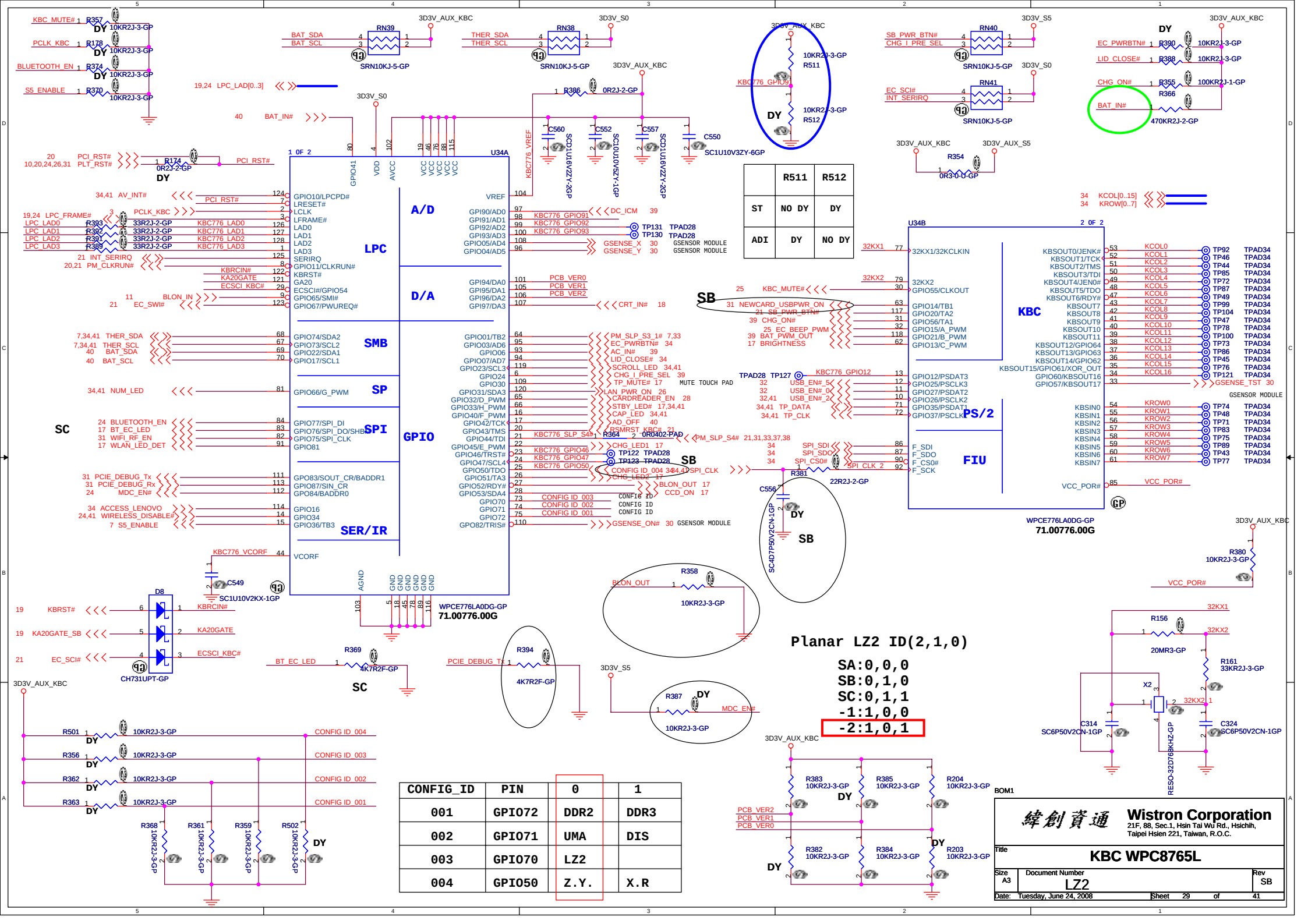
<Core Design>

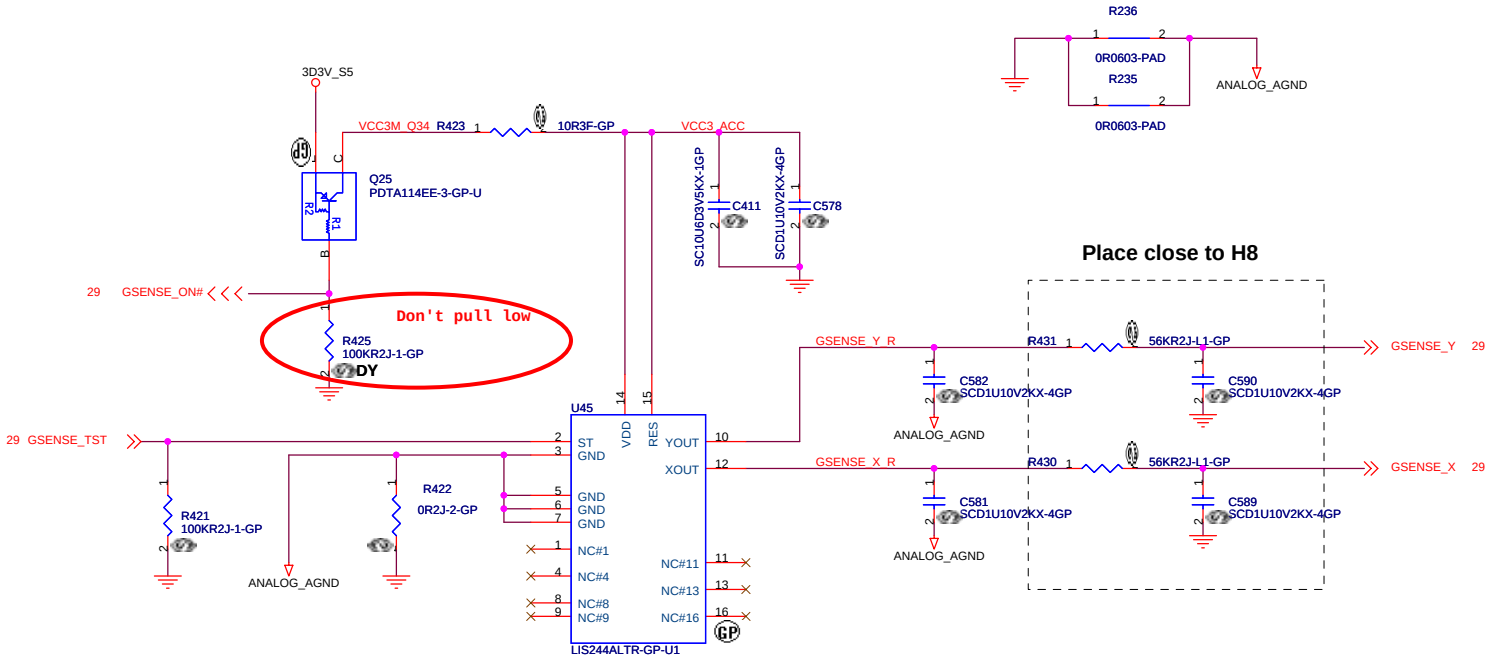
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 28 of 41


U34A
1 0F 2
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
SB
U34B
2 0F 2
KBC
PS/2
FIU
WPCE776LA0DG-GP
71.00776.00G
WPCE776LA0DG-GP
71.00776.00G
CH731UPT-GP
SC
SB
DY
Planar LZ2 ID(2,1,0)
SA:0,0,0
SB:0,1,0
SC:0,1,1
-1:1,0,0
-2:1,0,1
R511 R512
ST NO DY DY
ADI DY NO DY
CONFIG_ID PIN 0 1
001 GPIO72 DDR2 DDR3
002 GPIO71 UMA DIS
003 GPIO70 LZ2
004 GPIO50 Z.Y. X.R
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC8765L
Size A3
Document Number LZ2
Rev SB
Date: Tuesday, June 24, 2008
Sheet 29 of 41



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

BOM1

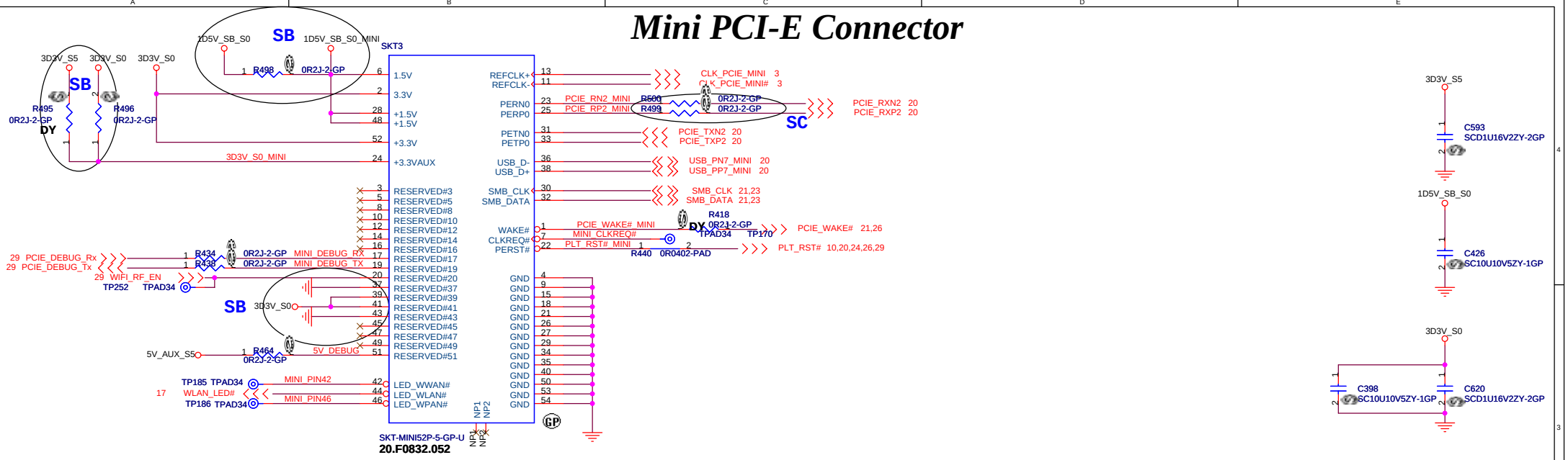
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GSENSOR**

Size	Document Number	Rev
	LZ2	SB

Date: Monday, June 23, 2008 Sheet 30 of 41

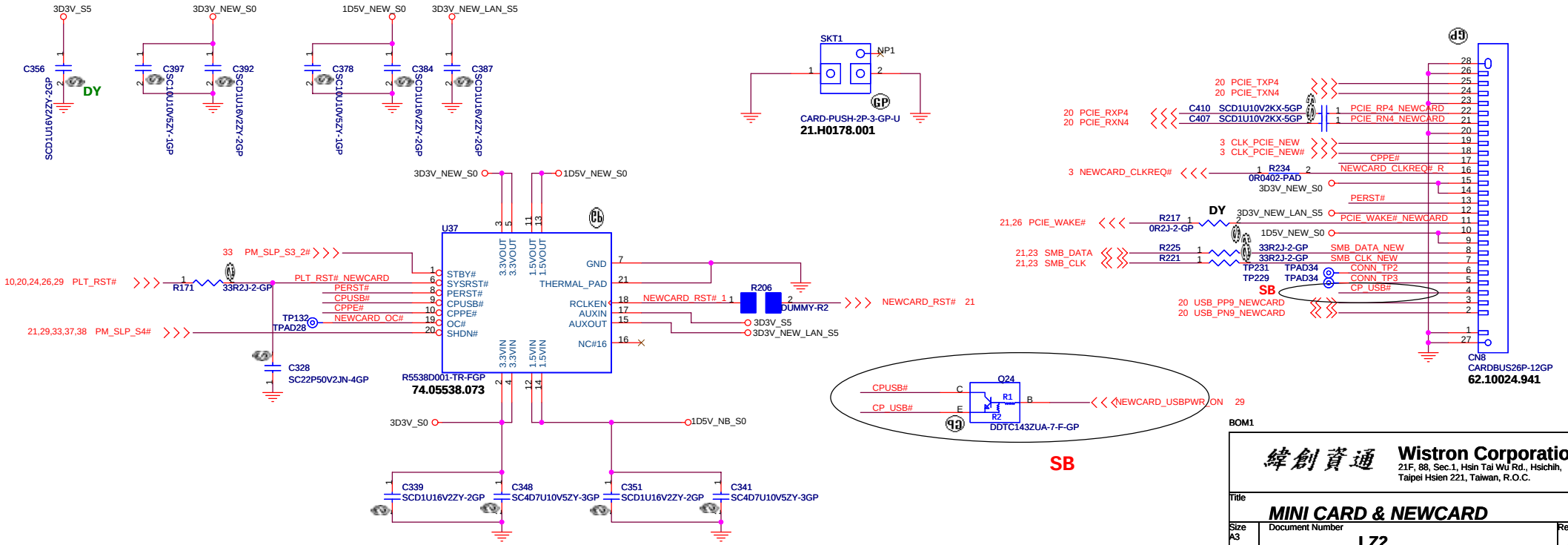
Mini PCI-E Connector



Place them Near to Chip

Place them Near to Connector

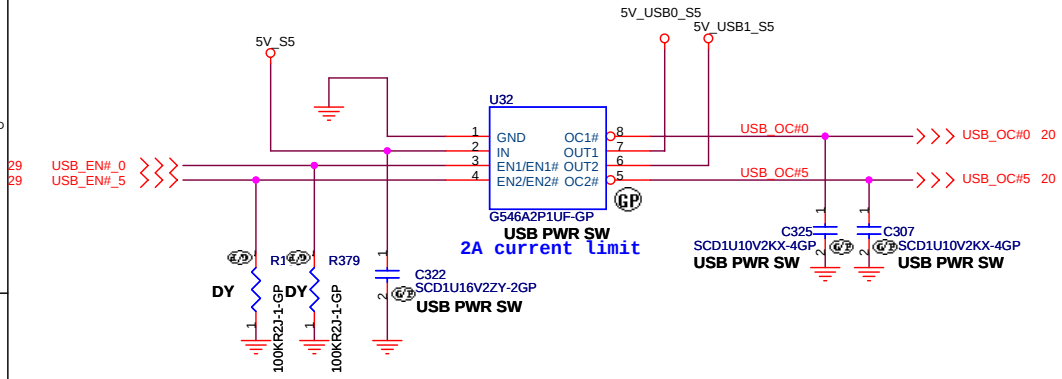
.N.E.W.C.A.R.D. C.O.N.N.

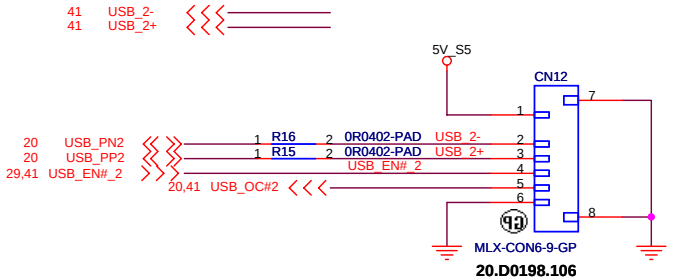


BOM1

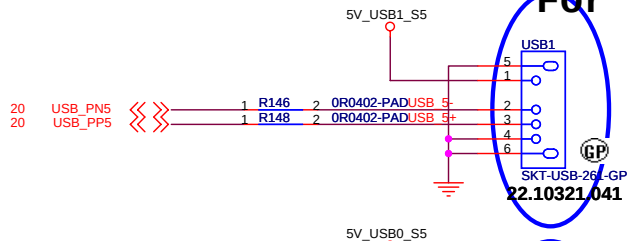
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD & NEWCARD	
Size A3	Document Number LZ2	Rev SB
Date: Monday, June 23, 2008	Sheet 31 of 41	

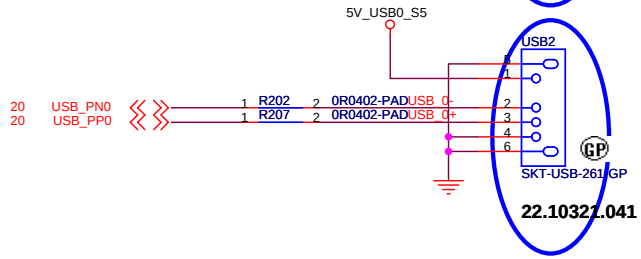
USB * 3 PORT



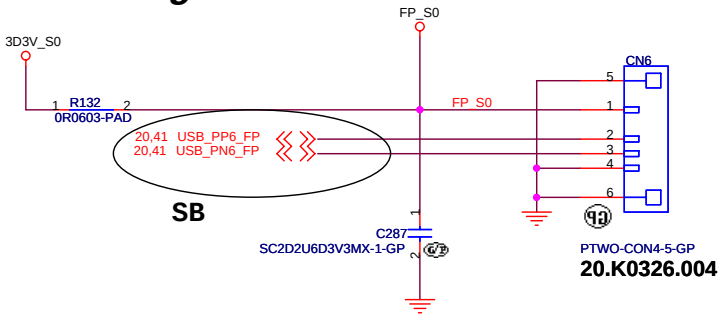


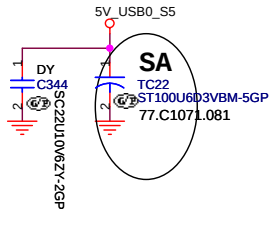
For PD

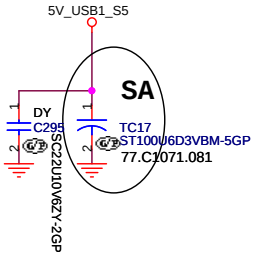


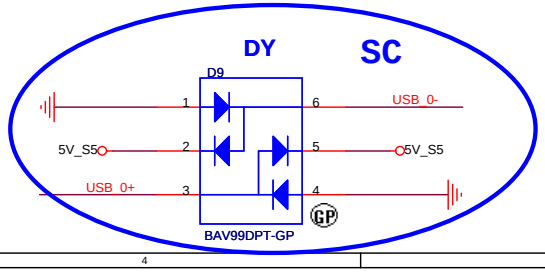


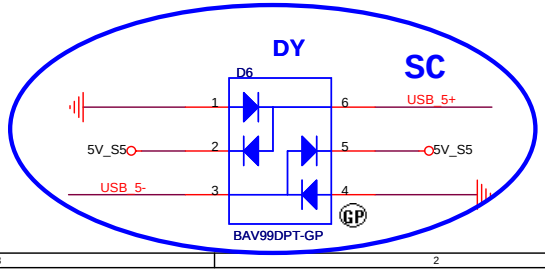
Finger Print











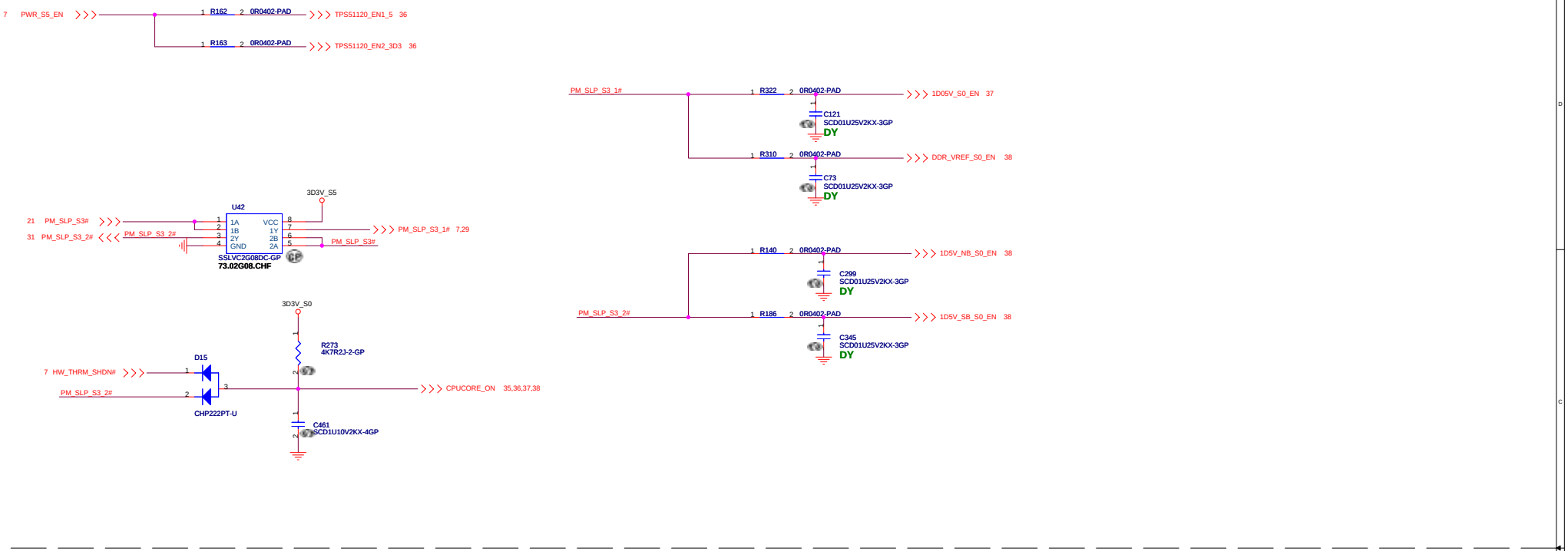
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

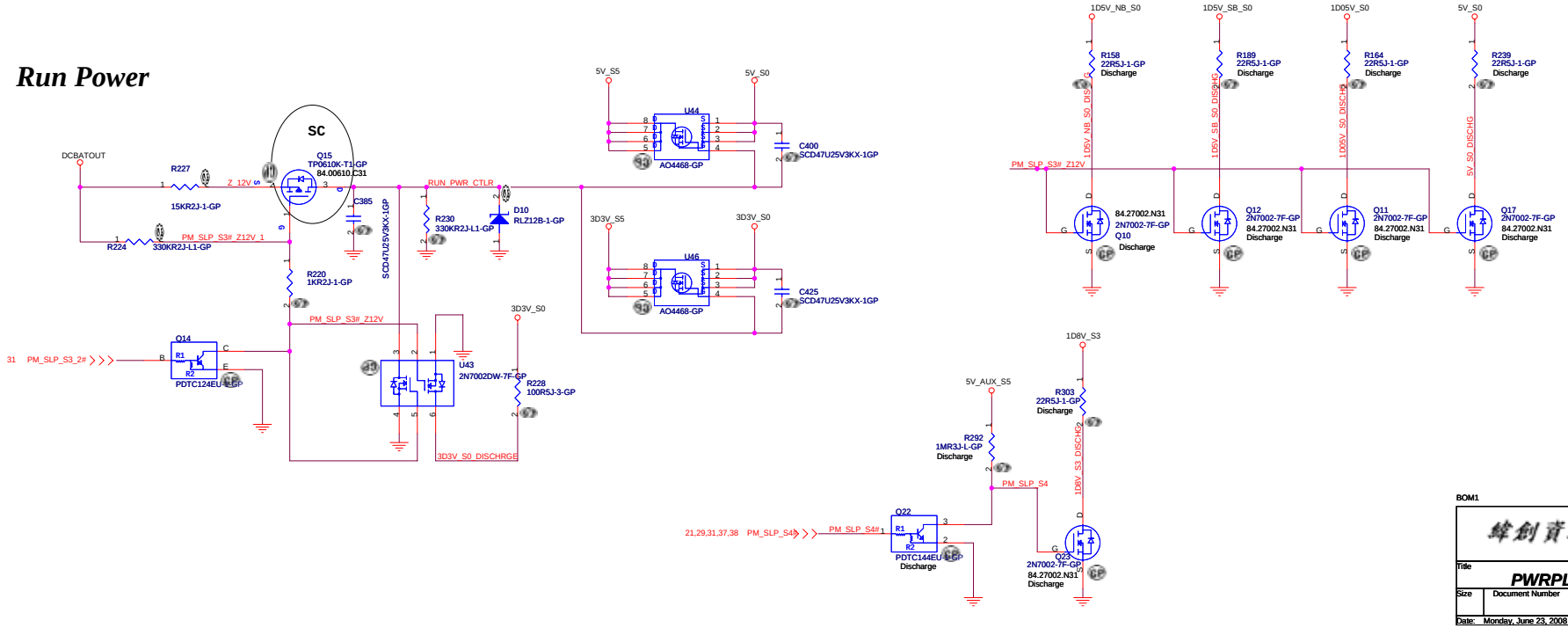
Title: **USB CONN/FINGER PRINT**

Size	Document Number	Rev
B	LZ2	SB

Date: Monday, June 23, 2008 Sheet 32 of 41



Run Power



BOM1

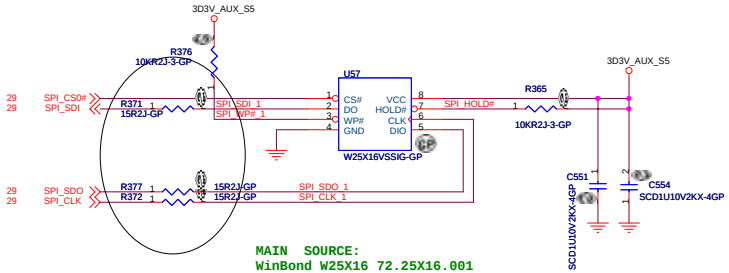
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWRPLANE&RESET LOGIC

Size	Document Number	Rev
	LZ2	SB

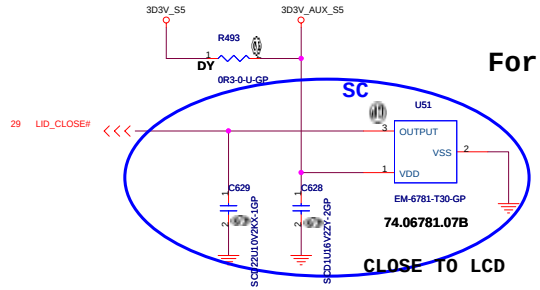
Date: Monday, June 23, 2008 Sheet 33 of 41

SPI Flash



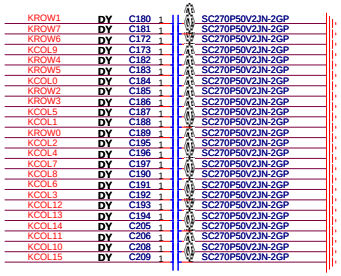
MAIN SOURCE:
WinBond W25X16 72.25X16.001
SECOND SOURCE:
MXIC MX25L1605 72.25165.001

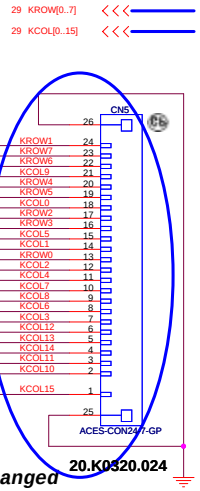
Lid Switch



For PD

Keyboard Connector





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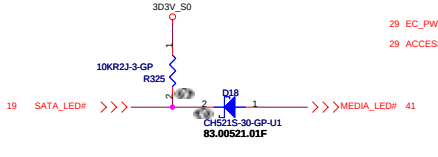
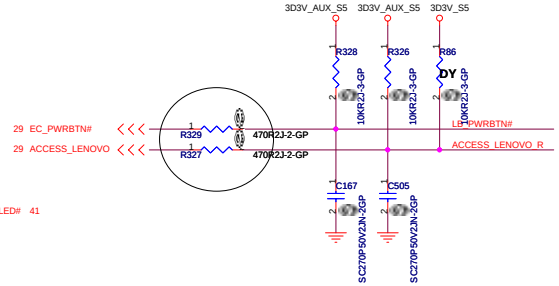
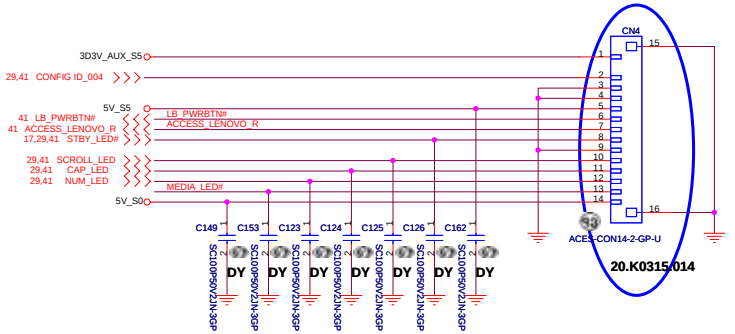
20.K0320.024

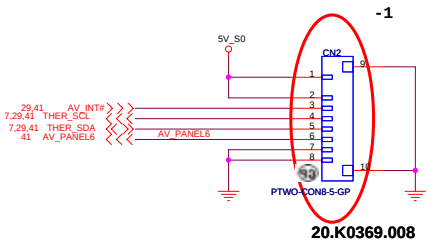
Launch Board





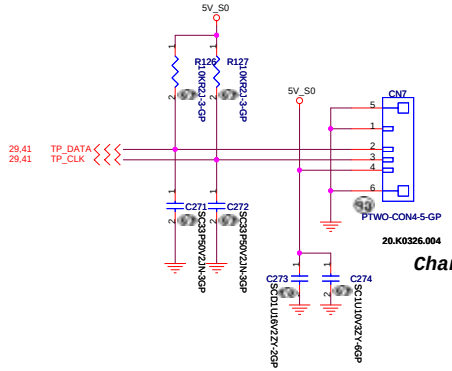


AV Panel



20.K0369.008

TouchPad Connector



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BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP/SPI/AV/Charger

Size	Document Number	Rev
	LZ2	SB

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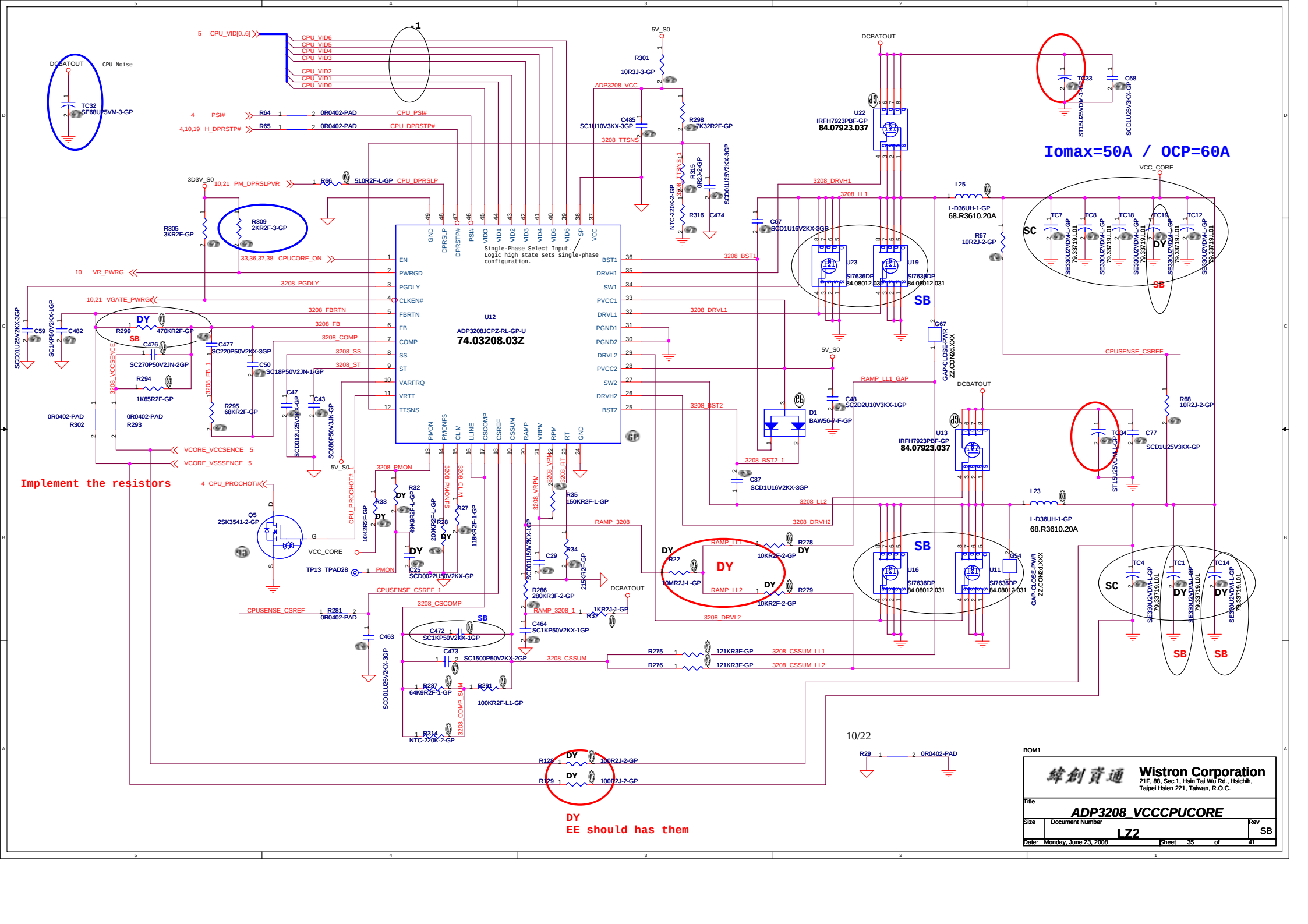
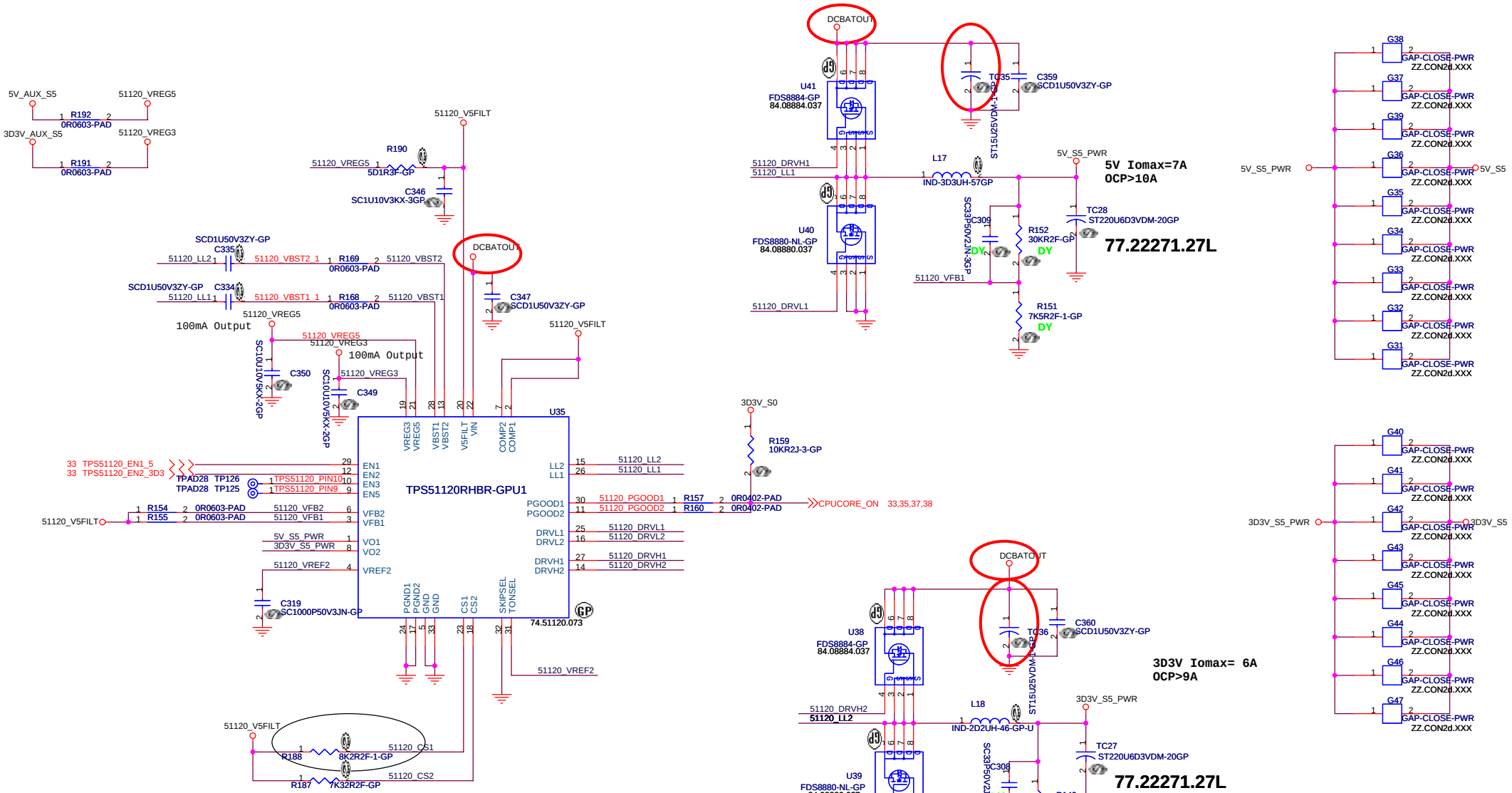

U12
ADP3208JCPZ-RL-GP-U
74.03208.03Z
Single-Phase Select Input.
Logic high state sets single-phase configuration.
Iomax=50A / OCP=60A
Implement the resistors
DY
EE should has them
SB
DCBATOUT
CPU Noise
VCC_CORE
5V_S0
3D3V_S0
CPU_VID[0..6]
CPU_PSI#
CPU_DPRSTP#
CPU_DPRSLP
VR_PWRG
VGATE_PWRG
CPUCORE_ON
VCORE_VCCSENCE
VCORE_VSSSENCE
CPU_PROCHOT#
PM_DPRSLPVR
H_DPRSTP#
PSI#
PMON
CPUSENSE_CSREF
IRFH7923PBF-GP
84.07923.037
SI7636DP
84.08012.031
L-D36UH-1-GP
68.R3610.20A
GAP-CLOSE-PWR
ZZ.CON2d.XXX
D1
BAW56-7-F-GP
Q5
2SK3541-2-GP
TP13 TPAD28
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ADP3208_VCCCPUCORE
LZ2
SB
Date: Monday, June 23, 2008
Sheet 35 of 41
10/22



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
	N/A	N/A	CURRENT MODE	D-Cap MODE
	380k/CH1 590k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
	N/A	not use	ADJ.	5V Fixed Output
	N/A	not use	ADJ.	3.3V Fixed Output
	Switcher OFF	not use	Swithchr ON	Switcher ON
	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

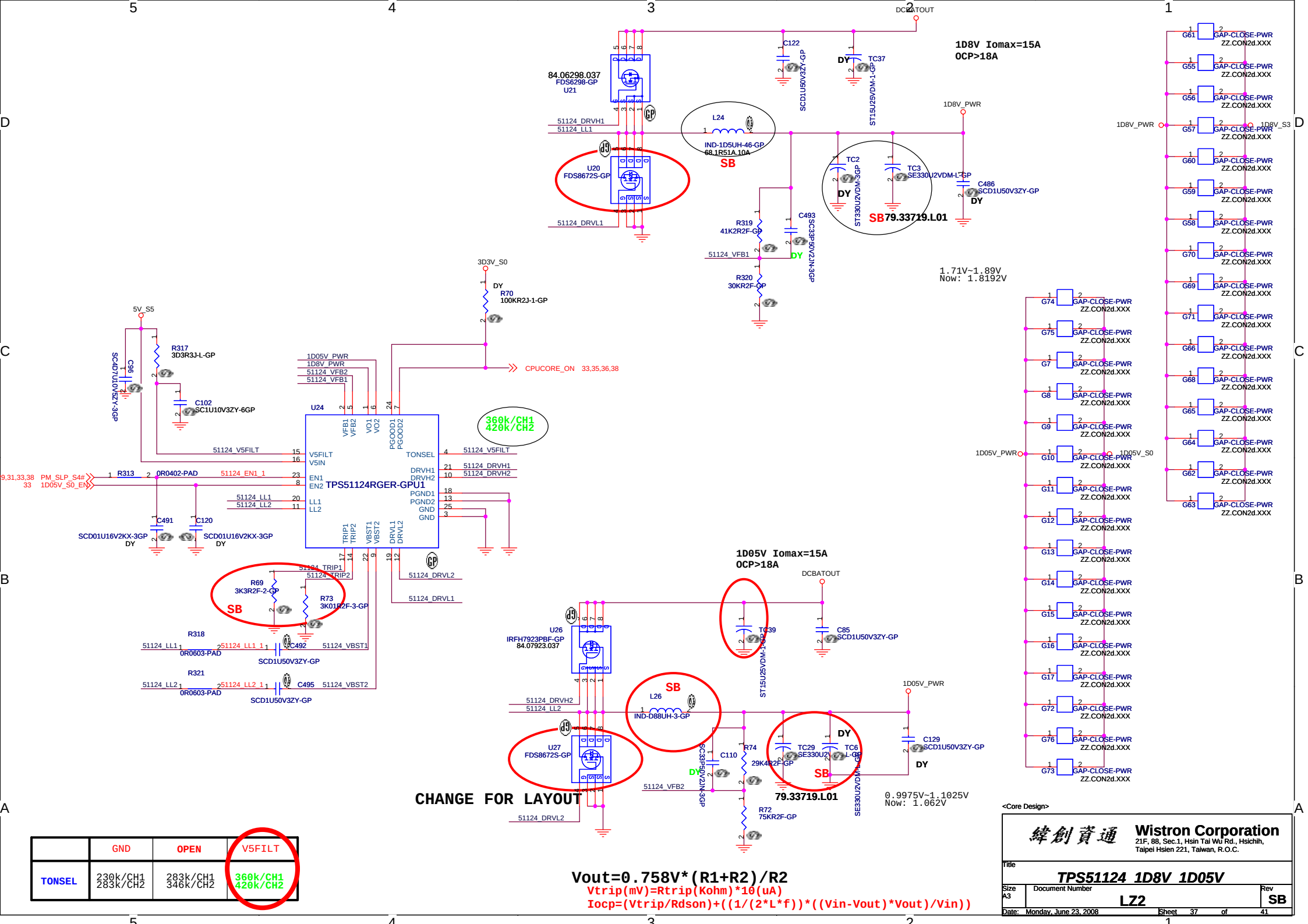
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size	Document Number	Rev
A3	LZ2	SB

Date: Monday, June 23, 2008 Sheet 36 of 41



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2

Vtrip(mV)=Rtrip(Kohm)*10(uA)

Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

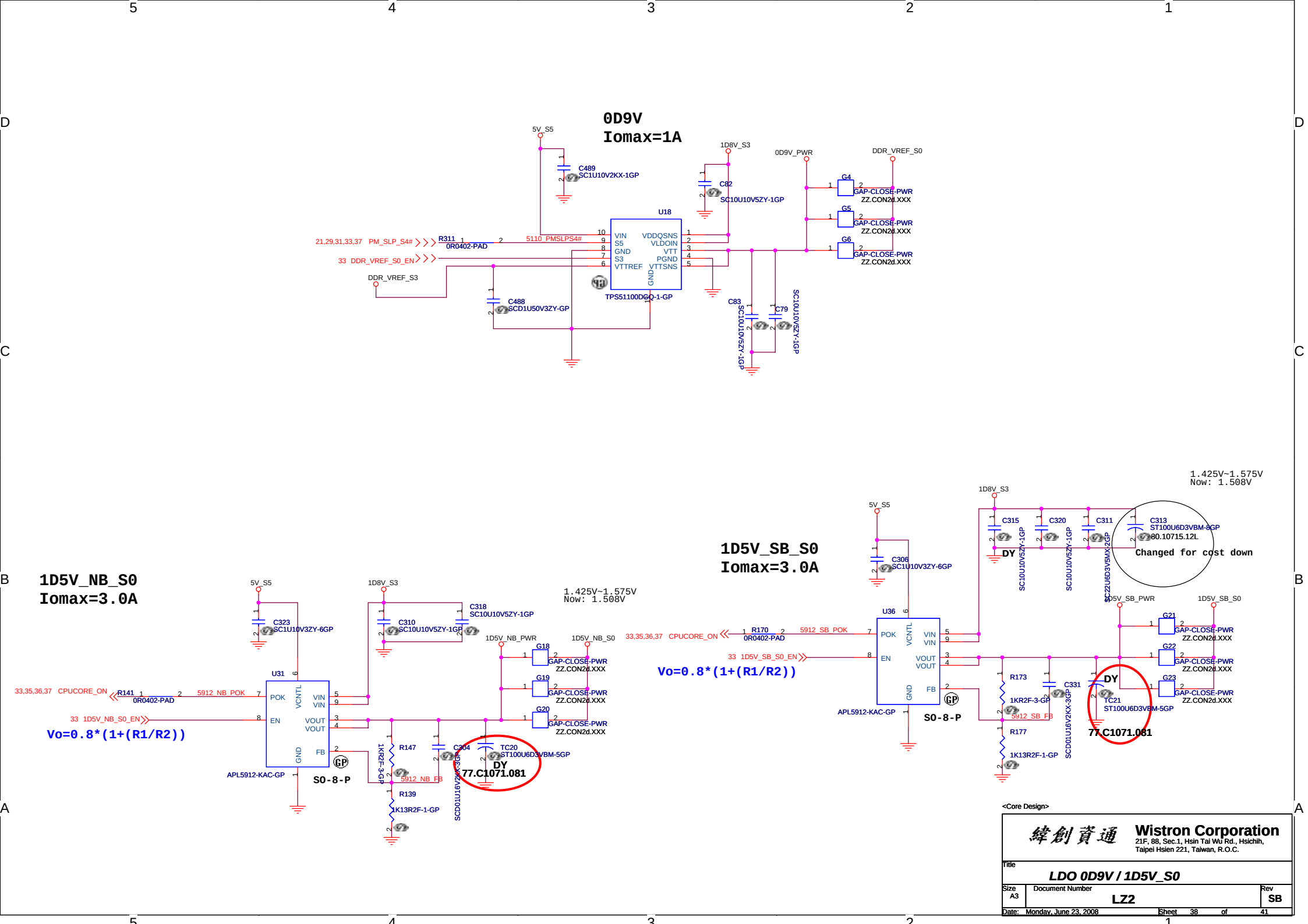
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size: A3 | Document Number: LZ2 | Rev: SB

Date: Monday, June 23, 2008 | Sheet 37 of 41



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 0D9V / 1D5V_S0

Size	Document Number	Rev
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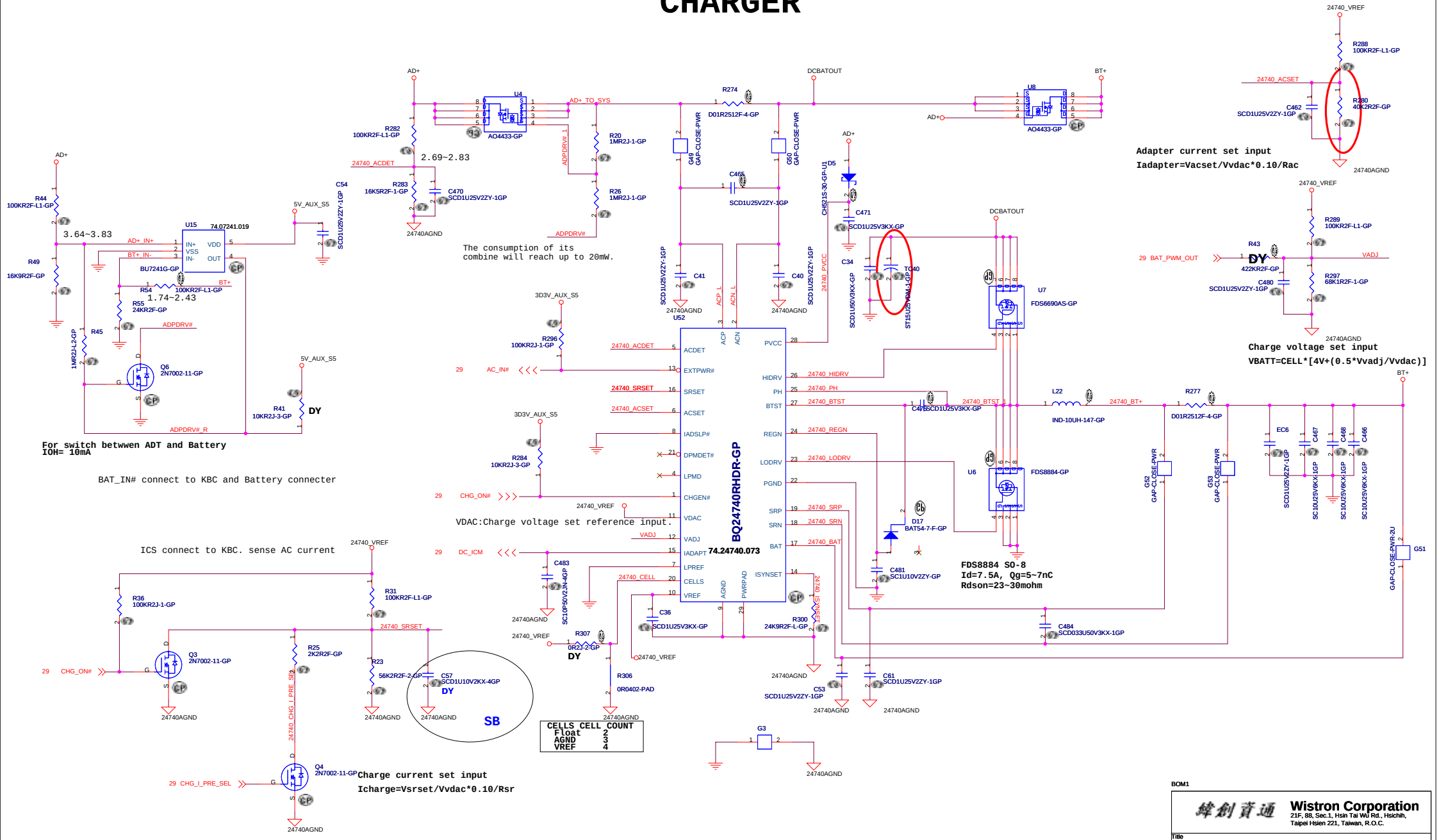
CHARGER



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger BQ24740

Size	Document Number	Rev
	LZ2	SB

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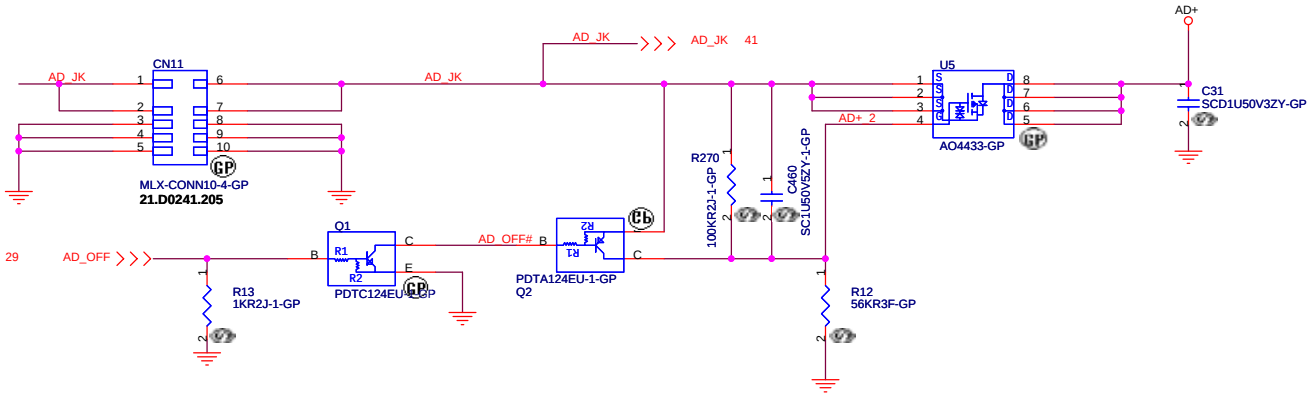
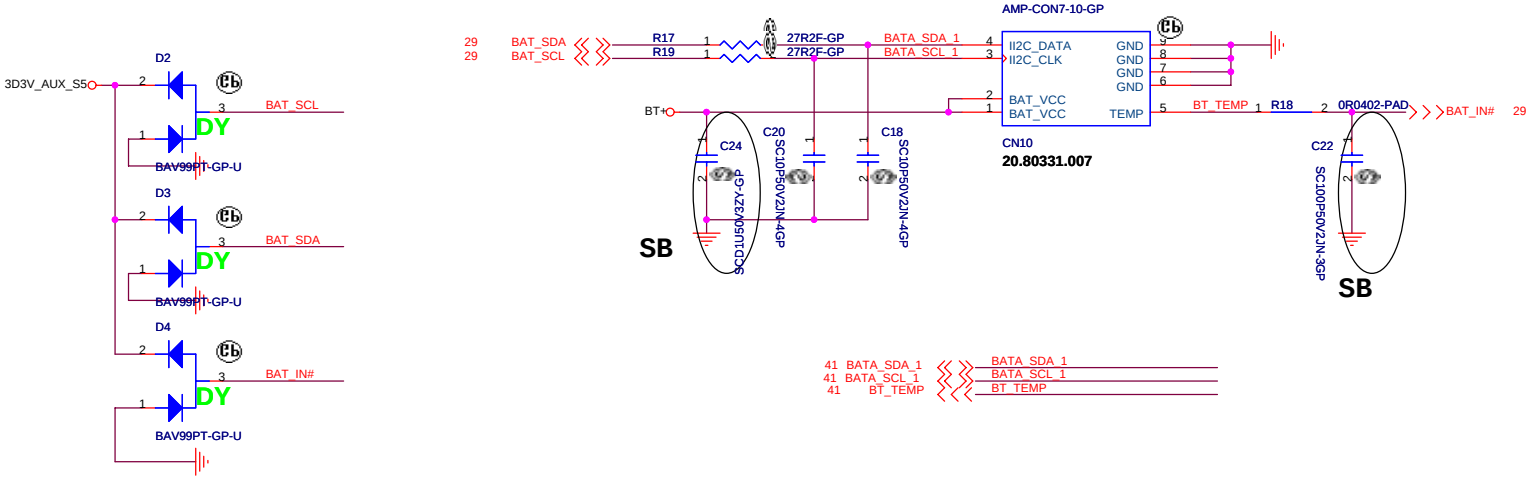
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

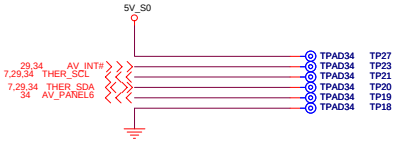
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PTH FOR SCREW HOLES**

Size	Document Number	Rev
A3	LZ2	SB

Date: Monday, June 23, 2008 Sheet 40 of 41

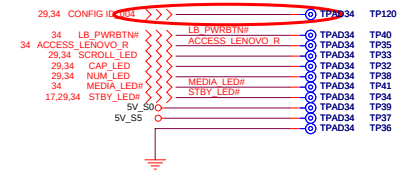
AV Panel



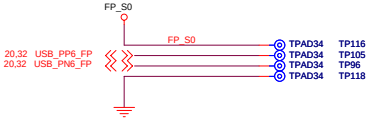
TouchPad Connector

ODD CONN

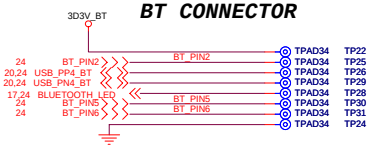
Launch Board



Finger Print CONN



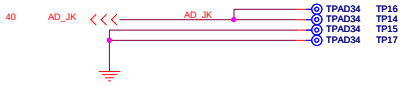
BT CONNECTOR



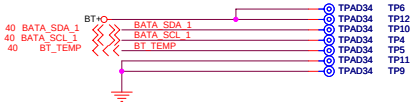
WIRELESS SWITCH

MIC CONN

ADT BOARD CONN

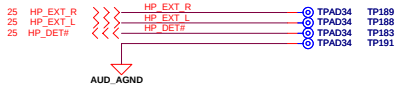


BATTERY CONN



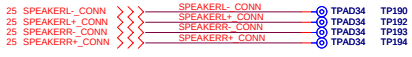
SATA CONN

HEADPHONE CONN

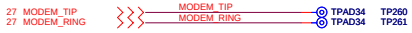


FAN CONN

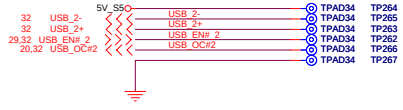
SPEAKER CONN



MODEM CABLE CONN

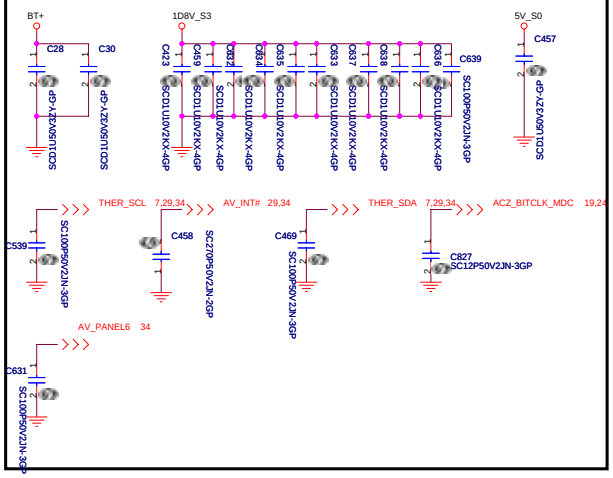


USB BOARD CONN

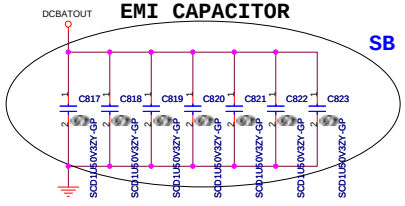


SC

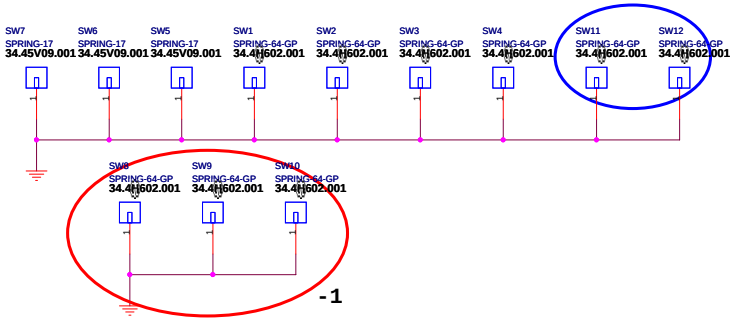
FOR EMI Solution

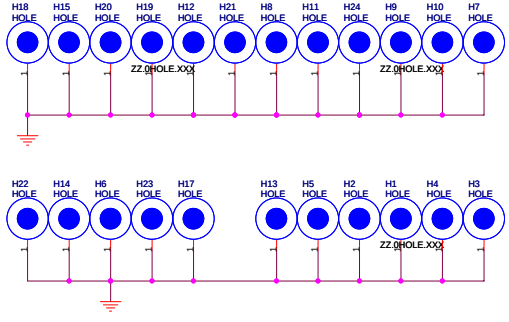


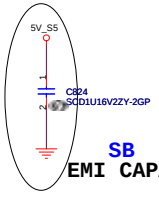
EMI CAPACITOR



FOR EMI Solution







SB

EMI CAPACITOR

BOM1

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Title: TTEST_PAD

Size: C | Document Number: LZ2 | Rev: SB

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