LE6 BLOCK DIAGRAM

01

PCB STACK UP

6L

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU Penryn
478P (uPGA)/35W
PAGE 4,5

CPU THERMAL SENSOR
PAGE 6

FSB 667/800/1066

14.318MHz

CLOCK GEN
ALPRS355B MLF64PIN
PAGE 3

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Cantiga
PAGE 7,8,9,10,11

DDRII-SODIMM1
PAGE 12,13

DDRII-SODIMM2
PAGE 12,13

DDRII 667/800 MHz

CRT
PAGE 18

Dual Link

LCD CONN
PAGE 18

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH-9M
PAGE 14,15,16,17

SATA - HDD
PAGE 25

SATA0 150MB

SATA - CD-ROM
PAGE 25

SATA4 150MB

USB2.0

USB2.0 Ports X3
PAGE 26

BlueTooth
PAGE 25

CCD
PAGE 26

PCI-E

Azalia

X1 Mini PCI-E Card
(Wireless LAN)
PAGE 25

X1 LAN
BROADCOM BCM 5906M
(10/100 LAN)
PAGE 20

X1 Express Card
(NEW CARD)
PAGE 25

X1 J Micro 385
PAGE 19

25MHz

RJ45
PAGE 20

Memory CardReader
PAGE 19

AUDIO CODEC
CX20561-12Z
PAGE 21

MDC CONN
PAGE 21

AUDIO Amplifier
TPA6017A2
PAGE 22

32.768KHz

LPC

Keyboard
Touch Pad PAGE 23

ITE
8502E-L
PAGE 24

microphone
PAGE 21

Audio Jacks
(Phone/ MIC)
PAGE 22

Jack to Speaker
PAGE 22

GMT G9931P1U
FAN
PAGE 23

SPI
PAGE 24

SYSTEM DISCHARGER
PAGE 28

SYSTEM CHARGER(ISL6251AHAZ-T)
PAGE 29

DDR II SMDDR_VTERM
1.8V/1.8VSUS(TPS51116REGR)
PAGE 30

VCCP +1.5V AND GMCH
1.05V(RT8204)
PAGE 31

CPU CORE ISL6266A
PAGE 32

SYSTEM POWER ISL6237IRZ-T
PAGE 33

PROJECT : LE6

Quanta Computer Inc.

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Custom	*BLOCK DIAGERAM*	1A

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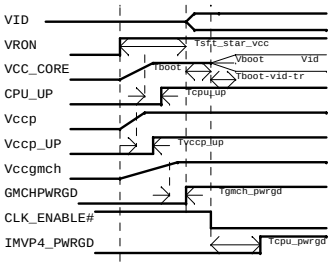
Board Stack up Description

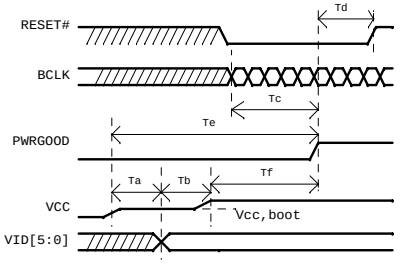
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		BOTTOM

Power On Sequencing Timing Diagram



YONAH Power-up Timing Specifications

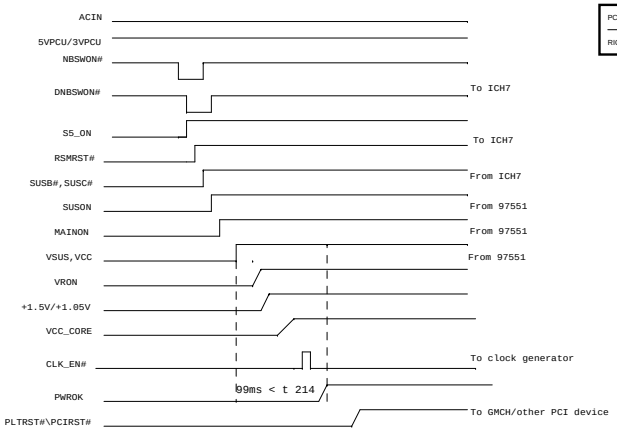


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDDR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC_GFX_CORE/+1.2V_GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICOH832	AD25	REQ0# / GNT0#	INT E#/F#

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

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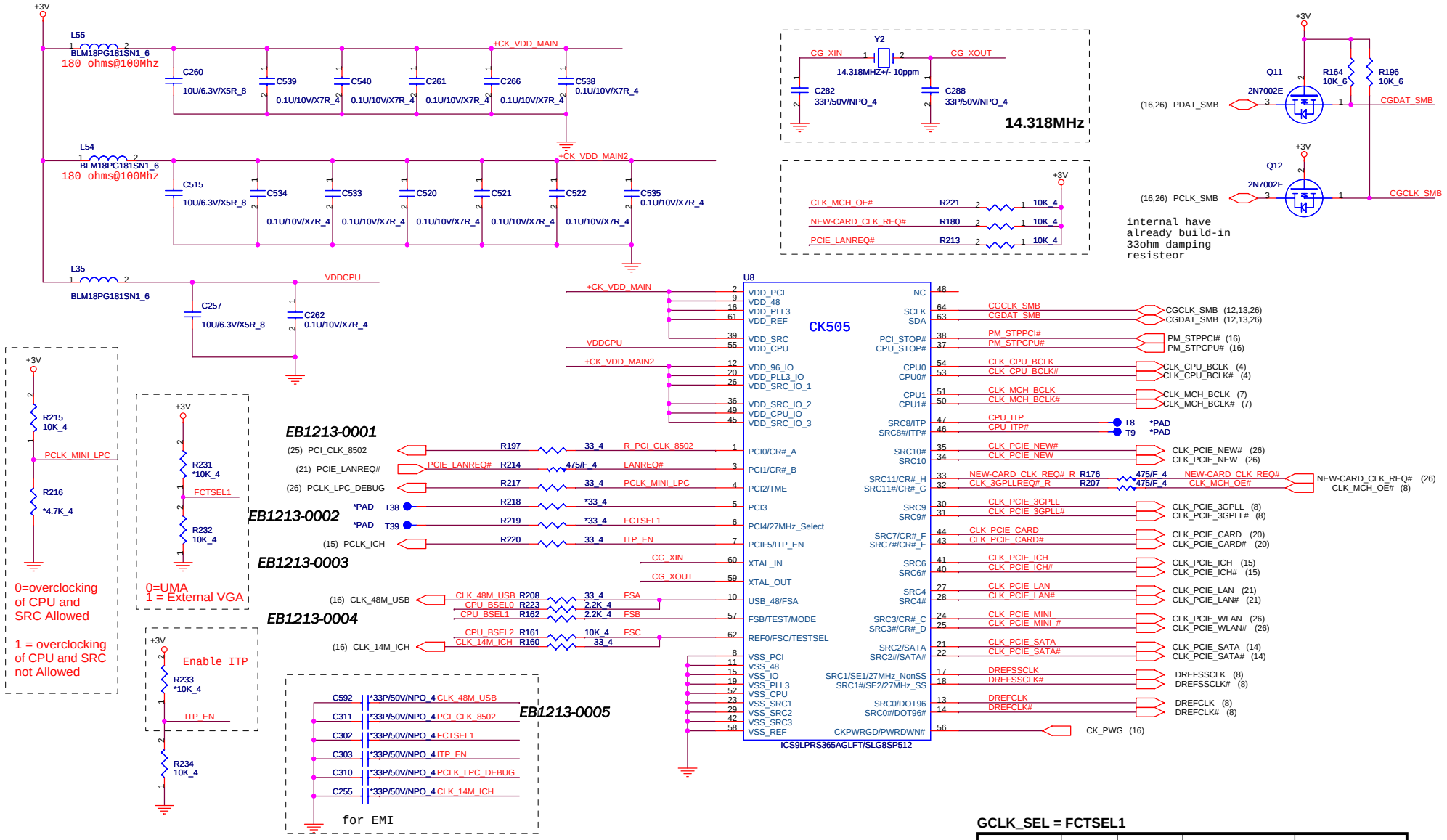
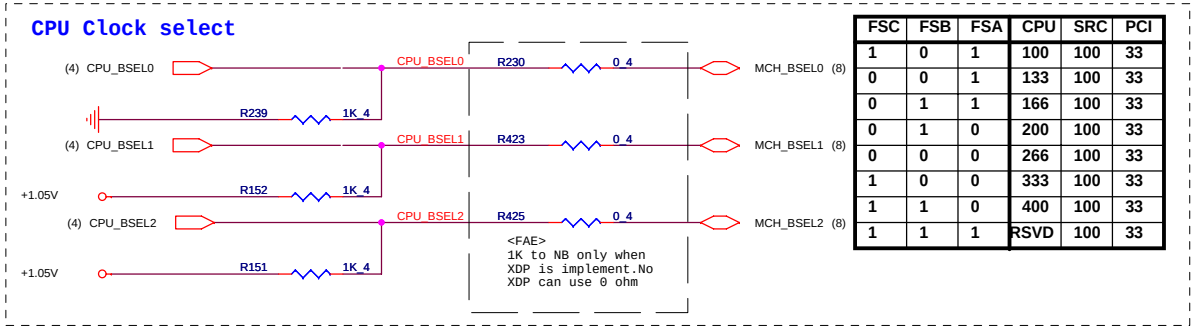


GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN24	PIN25
0=UMA	DREFCLK	DREFCLK#	SRCT1/LCDT_100	SRCT1/LCDT_100



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A
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(3,5,7,8,10,11,14,17,29,32,33) +1.05V

U24A

(7) H_A#[35:3]

H_A#3 J4 A[3]# ADDR GROUP 0
H_A#4 L5 A[4]#
H_A#5 L4 A[5]#
H_A#6 K5 A[6]#
H_A#7 M3 A[7]#
H_A#8 N2 A[8]#
H_A#9 J1 A[9]#
H_A#10 N3 A[10]#
H_A#11 P5 A[11]#
H_A#12 P2 A[12]#
H_A#13 L2 A[13]#
H_A#14 P4 A[14]#
H_A#15 P1 A[15]#
H_A#16 R1 A[16]#

(7) H_ADSTB#0 M1 ADSTB[0]#
(7) H_REQ#[4:0]
H_REQ#0 K3 REQ[0]#
H_REQ#1 H2 REQ[1]#
H_REQ#2 K2 REQ[2]#
H_REQ#3 J3 REQ[3]#
H_REQ#4 L1 REQ[4]#

H_A#[35:3]

H_A#17 Y2 A[17]# ADDR GROUP 1
H_A#18 U5 A[18]#
H_A#19 R3 A[19]#
H_A#20 W6 A[20]#
H_A#21 U4 A[21]#
H_A#22 Y5 A[22]#
H_A#23 U1 A[23]#
H_A#24 R4 A[24]#
H_A#25 T5 A[25]#
H_A#26 T3 A[26]#
H_A#27 W2 A[27]#
H_A#28 W5 A[28]#
H_A#29 Y4 A[29]#
H_A#30 U2 A[30]#
H_A#31 V4 A[31]#
H_A#32 W3 A[32]#
H_A#33 AA4 A[33]#
H_A#34 AB2 A[34]#
H_A#35 AA3 A[35]#

(7) H_ADSTB#1 V1 ADSTB[1]#

(14) H_A20M# A6 A20M#
(14) H_FERR# A5 FERR#
(14) H_IGNNE# C4 IGNNE#

(14) H_STPCLK# D5 STPCLK#
(14) H_INTR C6 LINT0
(14) H_NMI B4 LINT1
(14) H_SMI# A3 SMI#

+1.05V R96 *51/F_4 F6 TDI_1/RSV
D3 TDO_2/RSV

ITP_BPM1#0 N5 BMP_1#[0]/RSV
ITP_BPM1#1 M4 BMP_1#[1]/RSV
ITP_BPM1#2 B2 BMP_1#[2]/RSV
ITP_BPM1#3 AE8 BMP_1#[3]/VSS
D8 DCLKPH_1/VSS
GTLREF_CTL F8 ACLKPH_1/VSS
H_GTLREF2 D22 GTLREF_2/RSV
H_THERMDA2 T2 THRMDA_1/RSV
H_THERMDC2 V3 THRMDC_1/RSV
AA8 HFPLL_1/VSS
AC8 SPARE_1[4]/VSS
+VCORE AA7 BR1#/VCC

TP117
TP1
TP47

LE6B: Connect to +VCORE according to Intel DG 0429

Penryn Ball-out Rev 1a

ADS# H1
BNR# E2
BPRI# G5
DEFER# H5
DRDY# F21
DBSY# E1
BR0# F1
IERR# D20
INIT# B3
LOCK# H4
RESET# C1
RS[0]# F3
RS[1]# F4
RS[2]# G3
TRDY# G2
HIT# G6
HITM# E4

CONTROL

H_ADS# (7)
H_BNR# (7)
H_BPRI# (7)
H_DEFER# (7)
H_DRDY# (7)
H_DBSY# (7)
HBREQ#0 (7)
H_IERR# R36 56.2/F_4 +1.05V
H_INIT# (14)
H_LOCK# (7)
H_CPURST# (7)
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] (7)
H_TRDY# (7)
H_HIT# (7)
H_HITM# (7)

XDP/ITP SIGNALS

BPM[0]# AD4 ITP_BPM#0
BPM[1]# AD3 ITP_BPM#1
BPM[2]# AD1 ITP_BPM#2
BPM[3]# AC4 ITP_BPM#3
PRDY# AC2 ITP_BPM#4
PREQ# AC1 ITP_BPM#5
TCK AC5 ITP_TCK
TDI AA6 ITP_TDI
TDO AB3 ITP_TDO
TMS AB5 ITP_TMS
TRST# AB6 ITP_TRST#
DBR# C20
SYS_RST# (16)

EB1213-0006

THERMAL

PROCHOT# D21 R495 *0_4 H_PROCHOT# (33) +1.05V
THERMDA A24 R33 68_4 +1.05V
THERMDC B25 H_THERMDA (6)
H_THERMDC (6)

ICH

THERMTRIP# C7 PM_THRMTRIP# (8,14)

H CLK

BCLK[0] A22 CLK_CPU_BCLK (3)
BCLK[1] A21 CLK_CPU_BCLK# (3)

Quard Core Only

RSVD[06] D2

CPU_TEST2 R37 *1K/F_4
CPU_TEST1 R40 *1K/F_4

EB1213-0007

R102 54.9/F_4 ITP_TCK
R98 54.9/F_4 ITP_TRST#

+1.05V
R101 *51/F_4
R421 54.9/F_4
R89 54.9/F_4
R90 54.9/F_4
R514 54.9/F_4

ITP_TDI
ITP_TMS
ITP_TDO TP118
H_CPURST# R108 *1K/F_4 ITP_RST# TP42
SYS_RST# TP116
ITP_BPM#2 TP121
ITP_BPM#4 TP120
ITP_BPM#5 TP119

C165 *100P/50V_4

EB1213-0008

(7) H_D#[63:0]

U24B

H_D#0 E22 D[0]# DATA GRP 0
H_D#1 F24 D[1]#
H_D#2 E26 D[2]#
H_D#3 G22 D[3]#
H_D#4 F23 D[4]#
H_D#5 G25 D[5]#
H_D#6 E25 D[6]#
H_D#7 E23 D[7]#
H_D#8 K24 D[8]#
H_D#9 G24 D[9]#
H_D#10 J24 D[10]#
H_D#11 J23 D[11]#
H_D#12 H22 D[12]#
H_D#13 F26 D[13]#
H_D#14 K22 D[14]#
H_D#15 H23 D[15]#

(7) H_DSTBN#0 J26 DSTBN[0]#
(7) H_DSTBP#0 H26 DSTBP[0]#
(7) H_DINV#0 H25 DINV[0]#

H_D#[63:0]

H_D#16 N22 D[16]# DATA GRP 1
H_D#17 K25 D[17]#
H_D#18 P26 D[18]#
H_D#19 R23 D[19]#
H_D#20 L23 D[20]#
H_D#21 M24 D[21]#
H_D#22 L22 D[22]#
H_D#23 M23 D[23]#
H_D#24 P25 D[24]#
H_D#25 P23 D[25]#
H_D#26 P22 D[26]#
H_D#27 T24 D[27]#
H_D#28 R24 D[28]#
H_D#29 L25 D[29]#
H_D#30 T25 D[30]#
H_D#31 N25 D[31]#

(7) H_DSTBN#1 L26 DSTBN[1]#
(7) H_DSTBP#1 M26 DSTBP[1]#
(7) H_DINV#1 N24 DINV[1]#

H_D#[63:0]

Y22 D[32]# H_D#32 DATA GRP 2
AB24 D[33]# H_D#33
V24 D[34]# H_D#34
V26 D[35]# H_D#35
V23 D[36]# H_D#36
T22 D[37]# H_D#37
U25 D[38]# H_D#38
U23 D[39]# H_D#39
Y25 D[40]# H_D#40
W22 D[41]# H_D#41
Y23 D[42]# H_D#42
W24 D[43]# H_D#43
W25 D[44]# H_D#44
AA23 D[45]# H_D#45
AA24 D[46]# H_D#46
AB25 D[47]# H_D#47

Y26 DSTBN[2]# H_DSTBN#2 (7)
AA26 DSTBP[2]# H_DSTBP#2 (7)
U22 DINV[2]# H_DINV#2 (7)

H_D#[63:0]

AF24 D[48]# H_D#48 DATA GRP 3
AD24 D[49]# H_D#49
AA21 D[50]# H_D#50
AB22 D[51]# H_D#51
AB21 D[52]# H_D#52
AC26 D[53]# H_D#53
AD20 D[54]# H_D#54
AE22 D[55]# H_D#55
AF23 D[56]# H_D#56
AC25 D[57]# H_D#57
AE21 D[58]# H_D#58
AD21 D[59]# H_D#59
AC22 D[60]# H_D#60
AD23 D[61]# H_D#61
AF22 D[62]# H_D#62
AC23 D[63]# H_D#63

AE25 DSTBN[3]# H_DSTBN#3 (7)
AF24 DSTBP[3]# H_DSTBP#3 (7)
AC20 DINV[3]# H_DINV#3 (7)

R403 1K/F_4
R404 2K/F_4

H_GTLREF AD26 GTLREF
CPU_TEST1 C23 TEST1
CPU_TEST2 D25 TEST2
CPU_TEST3 C24 TEST3
CPU_TEST4 AE26 TEST4
CPU_TEST5 AE1 TEST5
CPU_TEST6 A26 TEST6
CPU_TEST7 C3 TEST7
B22 BSEL[0]
B23 BSEL[1]
C21 BSEL[2]

TP3
TP105
TP122
TP2
TP36

(3) CPU_BSEL0
(3) CPU_BSEL1
(3) CPU_BSEL2

MISC

COMP[0] R26 COMP0 R405 27.4/F_4
COMP[1] U26 COMP1 R406 54.9/F_4
COMP[2] AA1 COMP2 R420 27.4/F_4
COMP[3] Y1 COMP3 R419 54.9/F_4

E5 DPRSTP# H_DPRSTP# (8,14,33)
B5 DPSLP# H_DPSLP# (14)
D24 DPWR# H_DPWR# (7)
D6 PWRGOOD H_PWRGD (14)
D7 SLP# H_CPUSLP# (7)
AE6 PSI# PM_PSI# (33)

EB1213-0010

Penryn Ball-out Rev 1a

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PENRYN 1/2	2A
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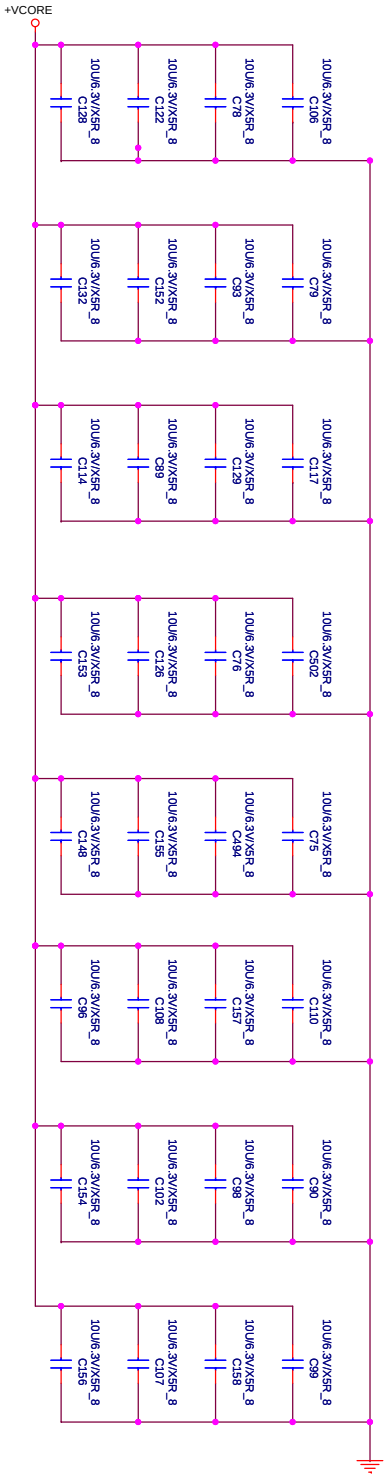

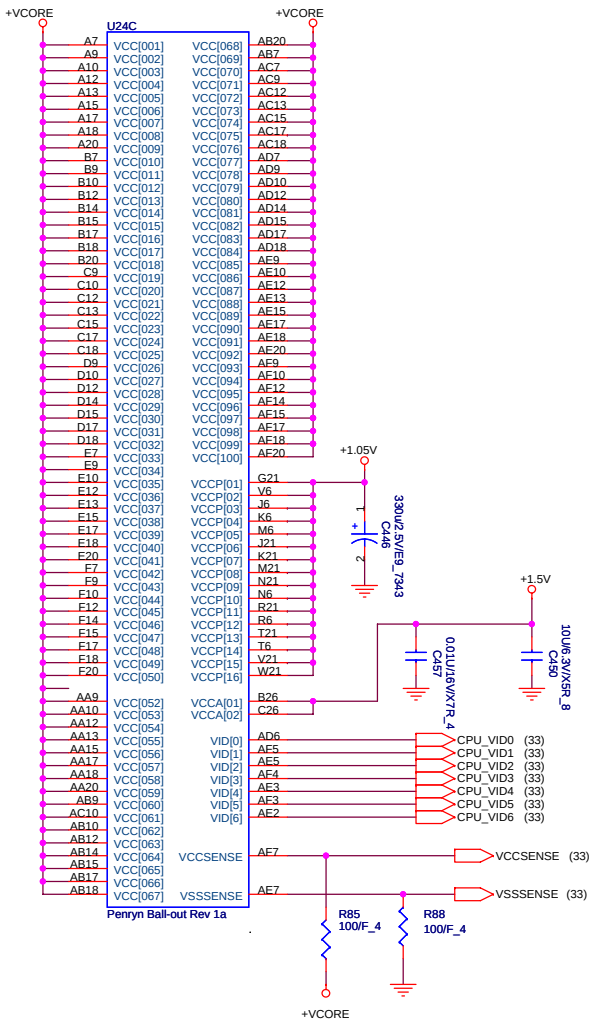

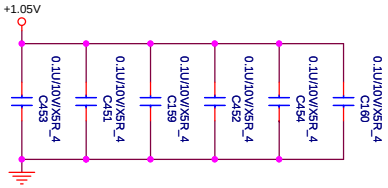

05

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PENRYN 2/2	1A
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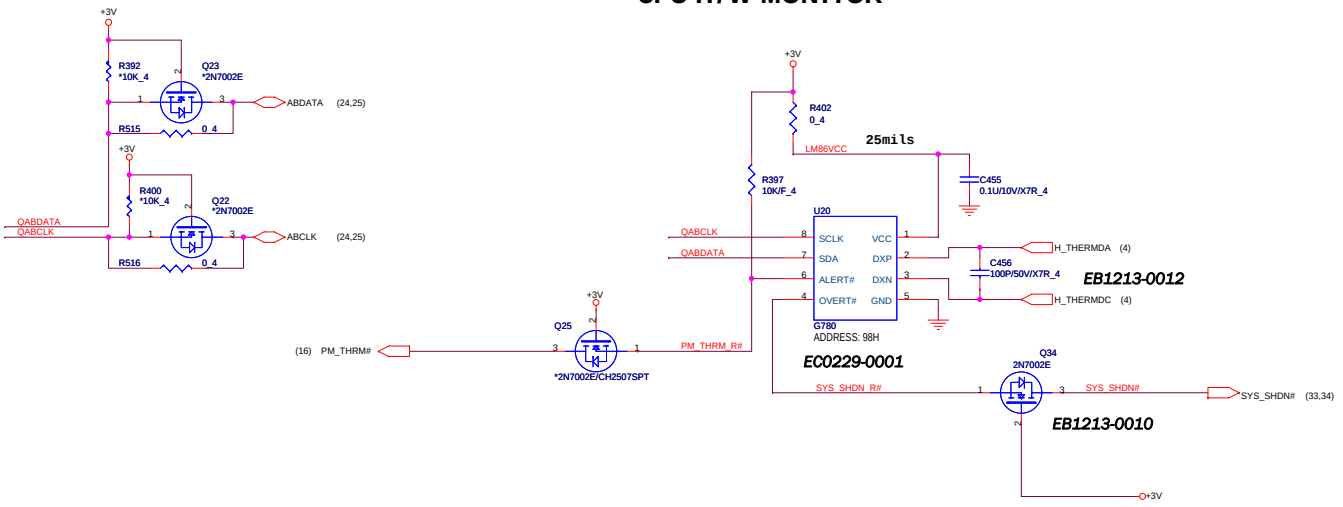
CPU H/W MONITOR



EB1213-0011

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	CPU THERMAL/HW PRODCT	1A

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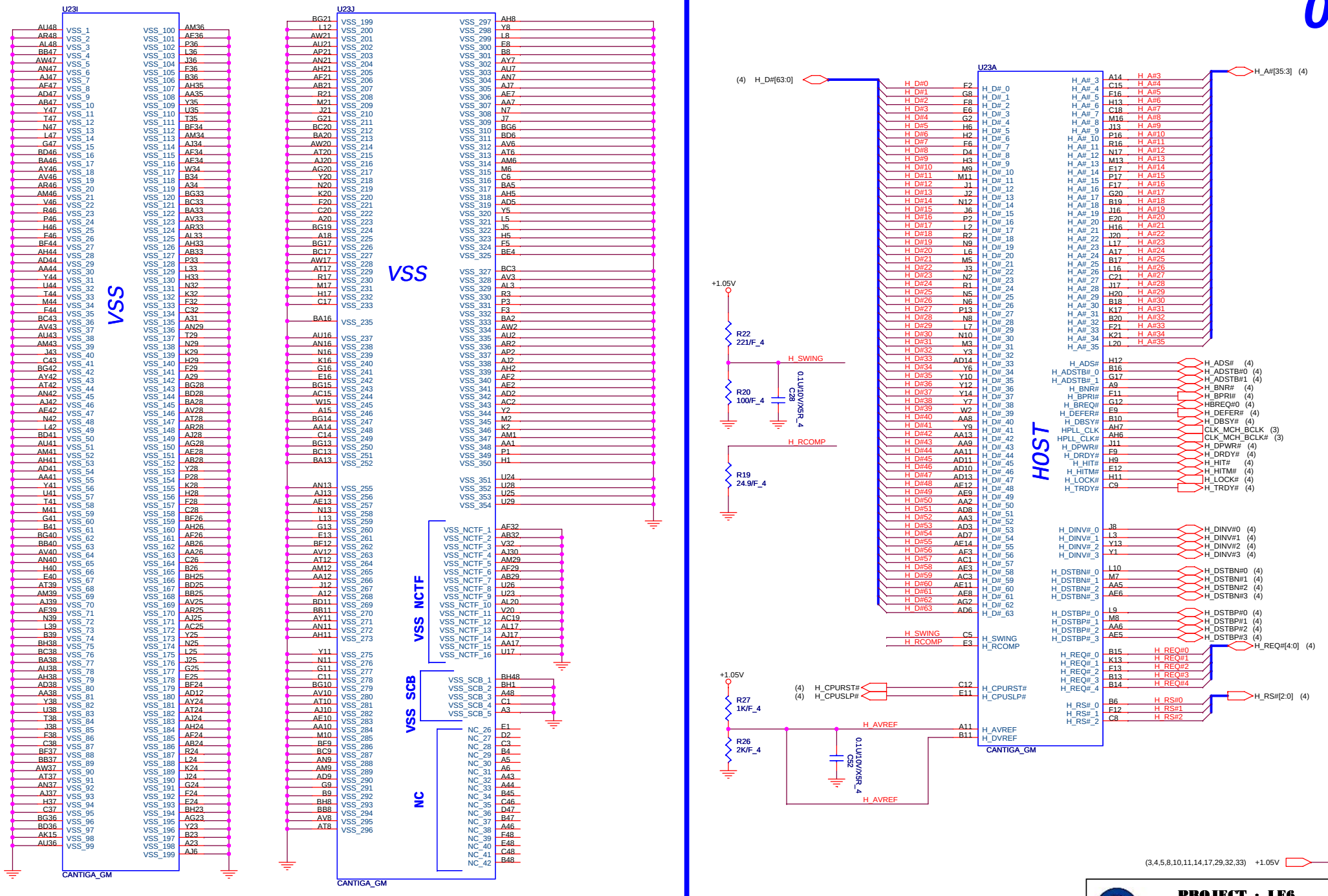

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Host & VSS 1/5	1A

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MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

(3,6,11,12,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V
(10,11,12,29,31,32) +1.8VSUS
(3,4,5,7,10,11,14,17,29,32,33) +1.05V
(11) +1.05V_PEG

U23B

RSVD: RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST# M_A_CLK0 (12) M_A_CLK1 (12) M_B_CLK0 (12) M_B_CLK1 (12) M_A_CLK0# (12) M_A_CLK1# (12) M_B_CLK0# (12) M_B_CLK1# (12) M_A_CKE0 (12,13) M_A_CKE1 (12,13) M_B_CKE0 (12,13) M_B_CKE1 (12,13) M_A_CS#0 (12,13) M_A_CS#1 (12,13) M_B_CS#0 (12,13) M_B_CS#1 (12,13) M_A_ODT0 (12,13) M_A_ODT1 (12,13) M_B_ODT0 (12,13) M_B_ODT1 (12,13) SM_RCOMP_VOH SM_RCOMP_VOL +0.9VSMVREF_MCH SW_PWROK_NB SM_REXT TP_SM_DRAMRST# R62 80.6/F_4 R48 80.6/F_4 R79 10K/F_4 R35 499/F_4 TP18 +1.8VSUS

CLK: DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK# DREFCLK (3) DREFCLK# (3) DREFSSCLK (3) DREFSSCLK# (3) CLK_PCIE_3GPLL (3) CLK_PCIE_3GPLL# (3)

ME JTAG: TP22 TP16 TP15 TP14 ME_JTAG_TCK ME_JTAG_TDI ME_JTAG_TDO ME_JTAG_TMS

DMI: DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 DMI_TXN[3:0] (15) DMI_TXP[3:0] (15) DMI_RXN[3:0] (15) DMI_RXP[3:0] (15)

CFG: MCH_BSEL0 (3) MCH_BSEL1 (3) MCH_BSEL2 (3) MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_10 MCH_CFG_11 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_20 R55 R52 R50 R51 R42 R57 2.2K_4 4.02K/F_4 TP5 TP10 TP8 TP9 TP7 TP4 TP6 TP13 +3V

GRAPHICS VID: GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN GFXVR_VID_0 GFXVR_VID_1 GFXVR_VID_2 GFXVR_VID_3 GFXVR_VID_4 GFXVR_EN TP114 TP115 TP17 TP24 TP20 TP113

PM: (16) PM_SYNC# (4,14,33) H_DPRSTP# (12,13) PM_EXTTS#0 (13) PM_EXTTS#1 (16,33) DELAY_VR_PWRGOOD (15) PLT_RST-R# (4,14) PM_THRMTRIP# (16,33) DPRSLPVR PM_EXTTS#0 PM_EXTTS#1 R24 100/F_4 RST_IN# MCH R500 *0_4 LE6B : Add R500 4/29 +3V R77 10K/F_4 PM_EXTTS#0 R73 10K/F_4 PM_EXTTS#1

ME: CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF CL_CLK0 (16) CL_DATA0 (16) ECPWROK (16,25) CL_RST#0 (16) 0.35 V MCH_CLVREF R113 1K/F_4 R109 499/F_4 0.1U/10V/X5R_4 C108 +1.05V

MISC: DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN# DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CLK SDVO_DATA CLK_MCH_OE# (3) MCH_ICH_SYNC# (16) MCH_TSATN R25 56.2/F_4 R527 R528 R529 *0_4 TP11 TP12 TP134 TP135 +1.05V

HDA: HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC TP136 TP138 TP137 TP139 TP140 EC0225-0001

NC: NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

CANTIGA_GM

U23C

LVDS: DPST_PWM (18) LVDS_BLON (18) EDIDCLK (18) EDIDDATA (18) DISP_ON (18) LA_CLK# (18) LA_CLK (18) LA_DATAN0 (18) LA_DATAN1 (18) LA_DATAN2 (18) LA_DATAP0 (18) LA_DATAP1 (18) LA_DATAP2 DPST_PWM_INT LVDS_BLON_INT L_CTRL_CLK L_CTRL_DATA EDIDCLK_INT EDIDDATA_INT DISP_ON_INT LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK LA_DATAN3 LA_DATAP3 LVDSA_DATA#_0 LVDSA_DATA#_1 LVDSA_DATA#_2 LVDSA_DATA#_3 LVDSA_DATA_0 LVDSA_DATA_1 LVDSA_DATA_2 LVDSA_DATA_3 LVDSB_DATA#_0 LVDSB_DATA#_1 LVDSB_DATA#_2 LVDSB_DATA#_3 LVDSB_DATA_0 LVDSB_DATA_1 LVDSB_DATA_2 LVDSB_DATA_3 R72 10K/F_4 R78 10K/F_4 R418 2.37K/F_4 TP109 TP108 TP110 TP112 TP111 TP107 TP25 TP19 TP23 TP106 TP26 TP21 TP28 +3V

TV: TVA_DAC TVB_DAC TVC_DAC TV_RTN TV_COMP1 TV_Y/G1 TV_C/R1 TV_DCONSEL_0 TV_DCONSEL_1 TV_DCONSEL0 TV_DCONSEL1 R43 R45 R49 75/F_4 R83 R82 0_4

VGA: CRT_B (18) CRT_G (18) CRT_R (18) DDCCLK (18) DDCDATA (18) HSYNC_COM (18) VSYNC_COM CRT_B_1 CRT_G_1 CRT_R_1 DDCCLK_INT DDCDATA_INT HSYNC_INT CRTIREF VSYNC_INT CRT_BLUE CRT_GREEN CRT_RED CRT_IRTN CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_TVO_IREF CRT_VSYNC R59 R56 R60 150/F_4 R76 R80 R75 33_4 1.02K/F_4

PCI-EXPRESS GRAPHICS: PEG_COMPI PEG_COMPO PEG_COMP R81 49.9/F_4 +1.05V_PEG PEG_RX#_0 PEG_RX#_1 PEG_RX#_2 PEG_RX#_3 PEG_RX#_4 PEG_RX#_5 PEG_RX#_6 PEG_RX#_7 PEG_RX#_8 PEG_RX#_9 PEG_RX#_10 PEG_RX#_11 PEG_RX#_12 PEG_RX#_13 PEG_RX#_14 PEG_RX#_15 PEG_RX_0 PEG_RX_1 PEG_RX_2 PEG_RX_3 PEG_RX_4 PEG_RX_5 PEG_RX_6 PEG_RX_7 PEG_RX_8 PEG_RX_9 PEG_RX_10 PEG_RX_11 PEG_RX_12 PEG_RX_13 PEG_RX_14 PEG_RX_15 PEG_TX#_0 PEG_TX#_1 PEG_TX#_2 PEG_TX#_3 PEG_TX#_4 PEG_TX#_5 PEG_TX#_6 PEG_TX#_7 PEG_TX#_8 PEG_TX#_9 PEG_TX#_10 PEG_TX#_11 PEG_TX#_12 PEG_TX#_13 PEG_TX#_14 PEG_TX#_15 PEG_TX_0 PEG_TX_1 PEG_TX_2 PEG_TX_3 PEG_TX_4 PEG_TX_5 PEG_TX_6 PEG_TX_7 PEG_TX_8 PEG_TX_9 PEG_TX_10 PEG_TX_11 PEG_TX_12 PEG_TX_13 PEG_TX_14 PEG_TX_15

CANTIGA_GM

+1.8VSUS R69 1K/F_4 SM_RCOMP_VOH SM_RCOMP_VOL R64 3.01K/F_4 R61 1K/F_4 0.01U/16V/X7R_4 C105 C115 2.2U/6.3V/X5R_6 C100 C111

+1.8VSUS R104 *1K/F_4 R105 0_4 +0.9VSMVREF (12,31) +0.9VSMVREF_MCH C162 0.1U/10V/X5R_4 C161 470P/50V/X7R_4 R97 *1K/F_4 HP SVTP TEST

For UMA HDMI Function

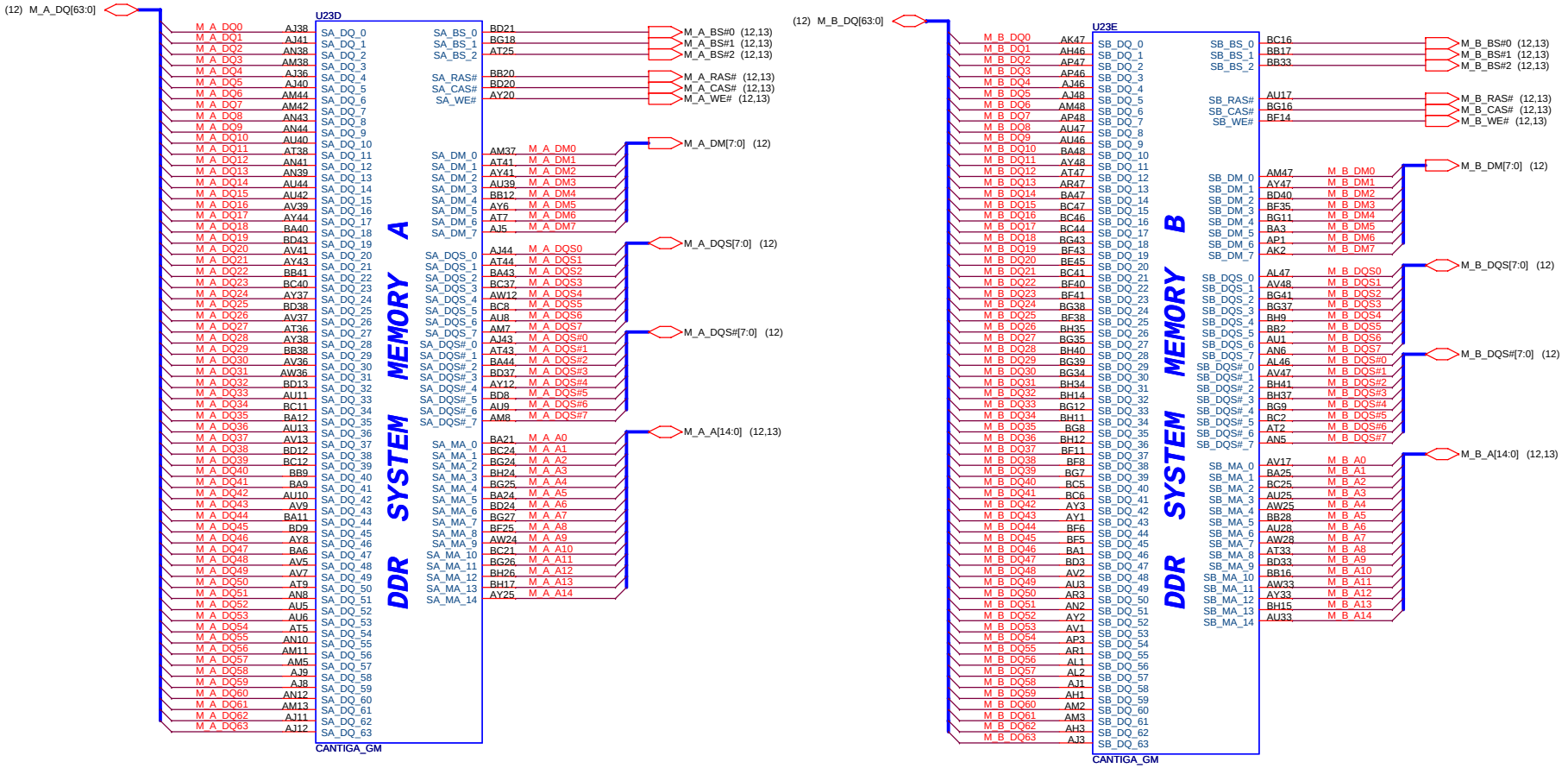
EB1213-0013

HPD# Inverting Level Shifting Circuit

PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Canting DMIDISP 2/5	1A

Date: Friday, May 02, 2008 Sheet 8 of 34

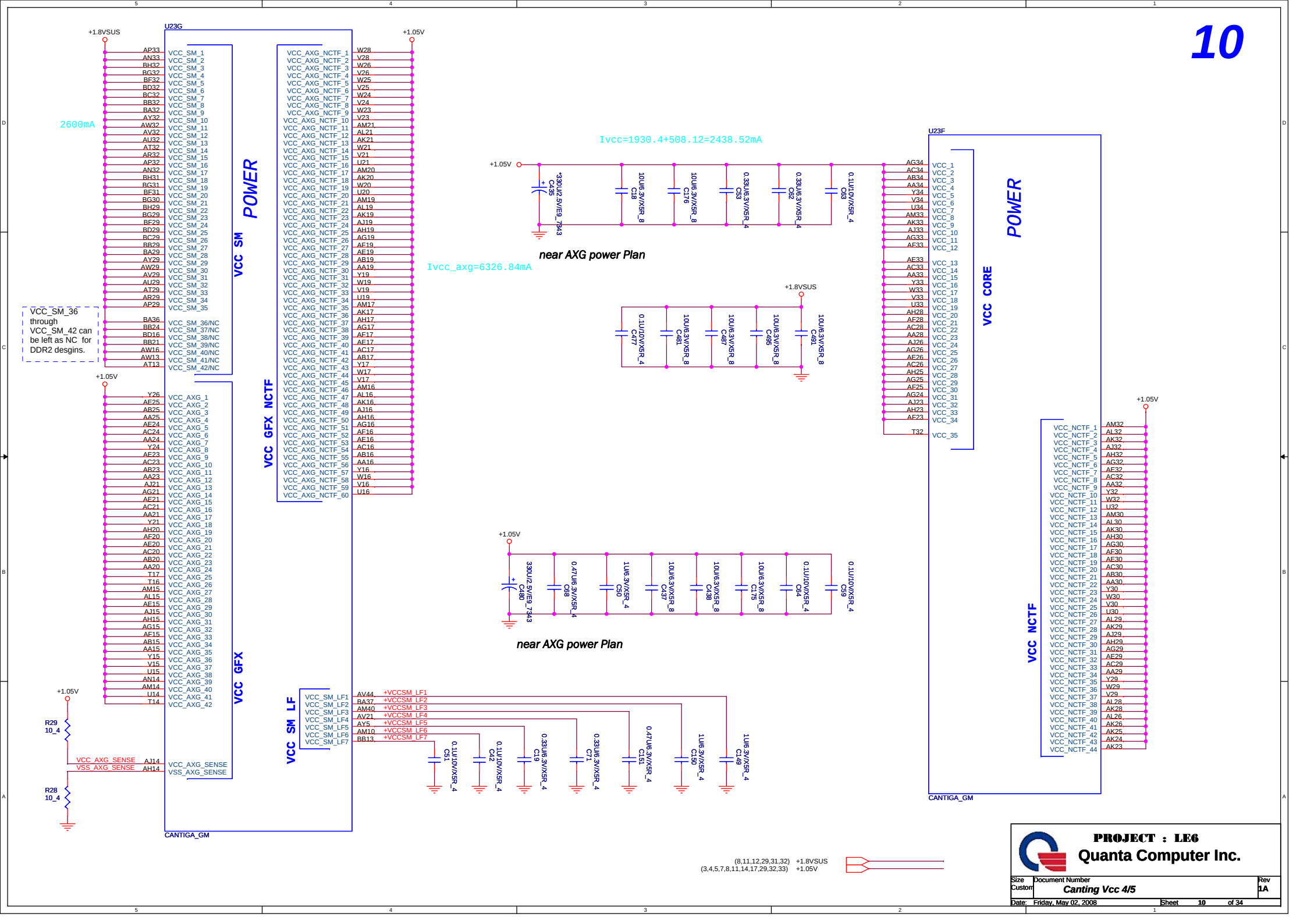


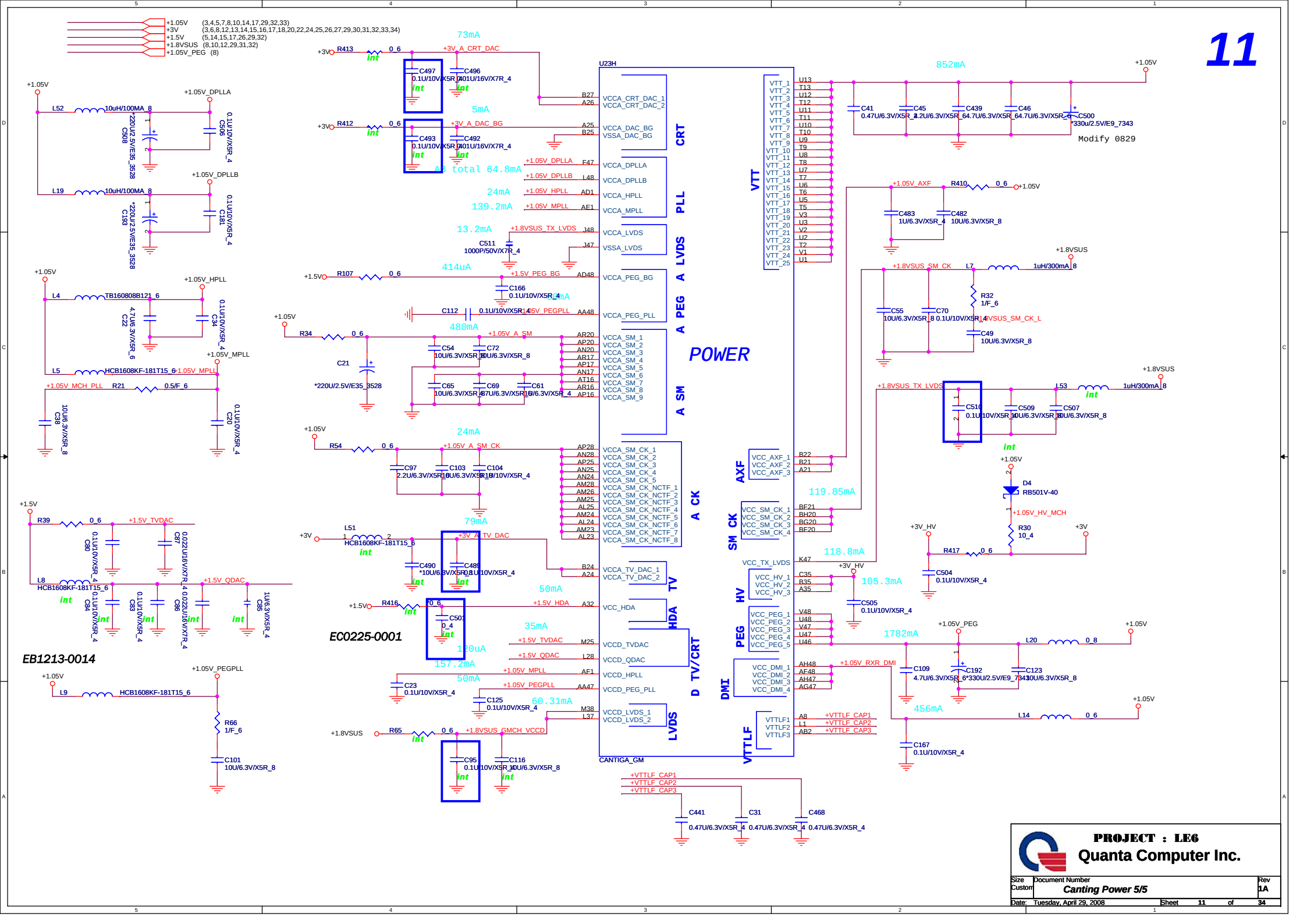
PROJECT : LE6

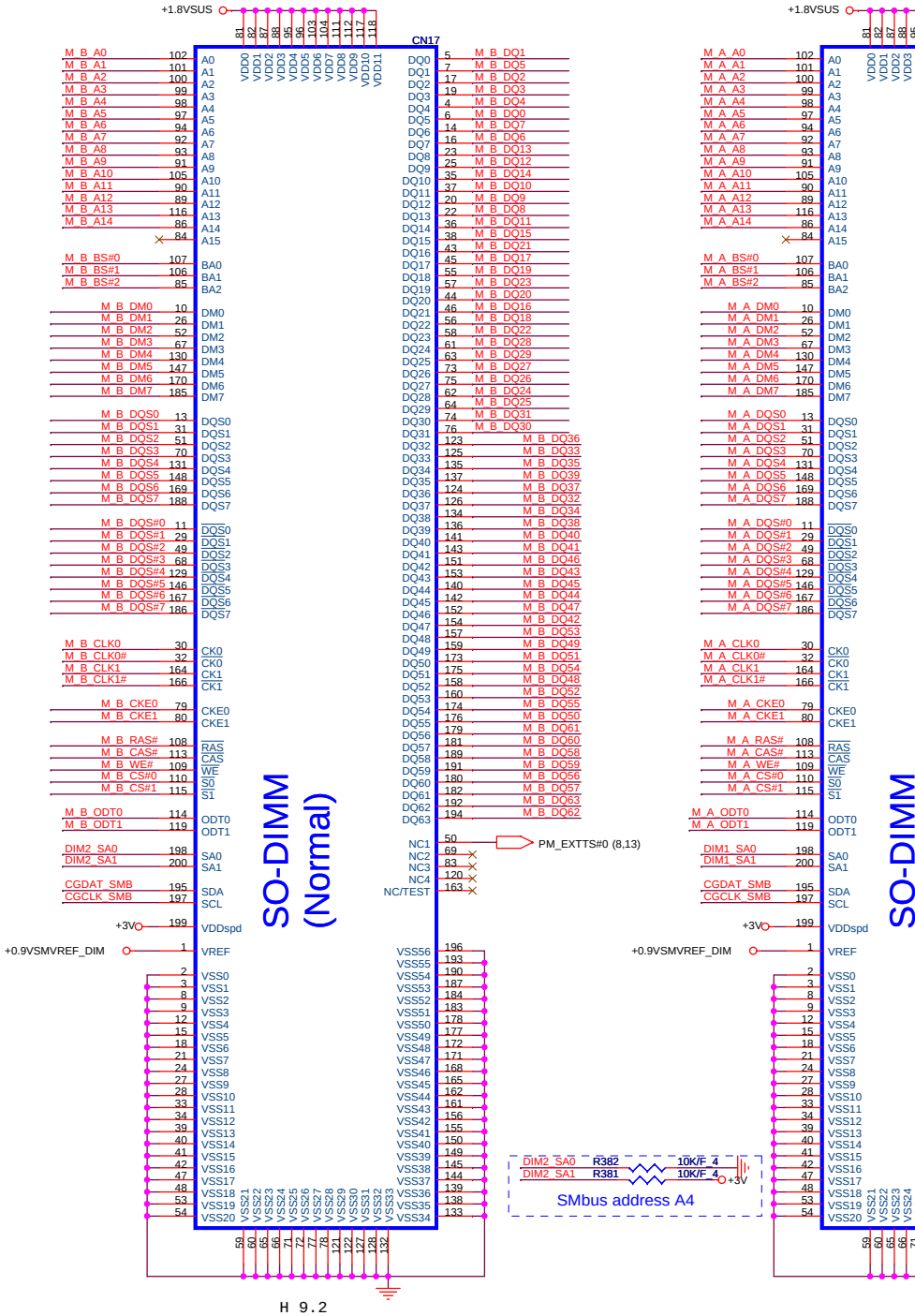
Quanta Computer Inc.

Size	Document Number	Rev
Custom	*Canting DDR2 3/5*	1A

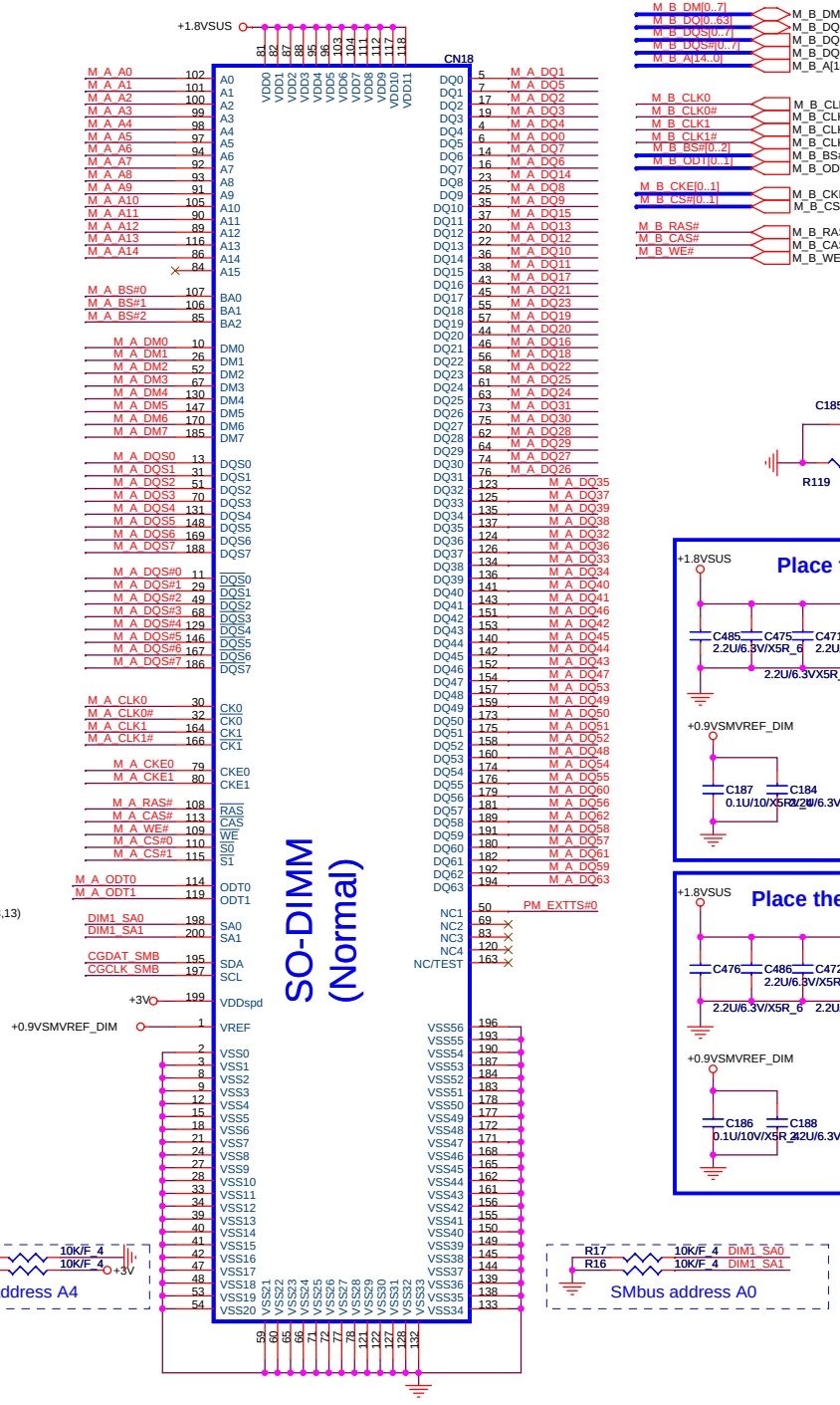
Date: Tuesday, April 29, 2008 Sheet 9 of 34


U23G
+1.8VSUS
+1.05V
2600mA
VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desgins.
VCC SM
POWER
VCC GFX NCTF
VCC GFX
VCC SM LF
CANTIGA_GM
R29 10_4
R28 10_4
VCC_AXG_SENSE
VSS_AXG_SENSE
Ivcc=1930.4+508.12=2438.52mA
Ivcc_axg=6326.84mA
near AXG power Plan
near AXG power Plan
U23F
VCC CORE
POWER
VCC NCTF
CANTIGA_GM
PROJECT : LE6
Quanta Computer Inc.
Size Custom
Document Number
Canting Vcc 4/5
Rev 1A
Date: Friday, May 02, 2008
Sheet 10 of 34

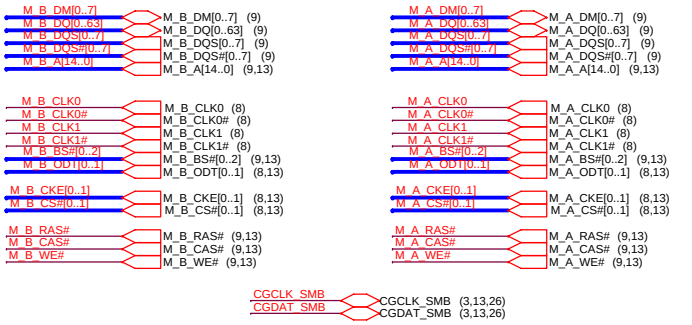

11
+1.05V (3,4,5,7,8,10,14,17,29,32,33)
+3V (3,6,8,12,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34)
+1.5V (5,14,15,17,26,29,32)
+1.8VSUS (8,10,12,29,31,32)
+1.05V_PEG (8)
POWER
U23H
CANTIGA_GM
CRT
PLL
LVDS
A PEG
A SM
A CK
SM CK
AXF
HV
PEG
DMI
TV
HDA
D TV/CRT
VTT
VTTLF
EC0225-0001
EB1213-0014
PROJECT : LE6
Quanta Computer Inc.
Canting Power 5/5
Modify 0829
Tuesday, April 29, 2008

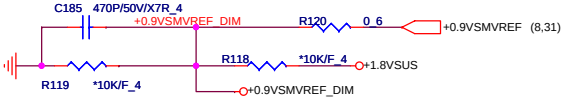


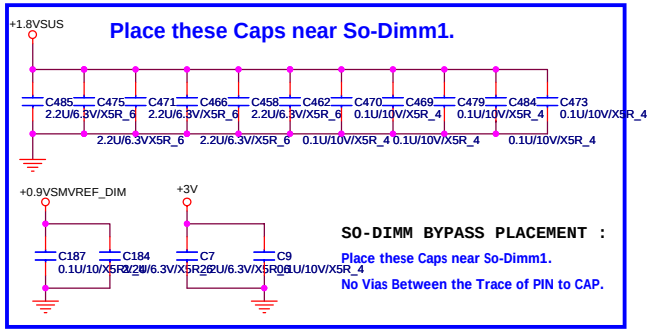
H 9.2

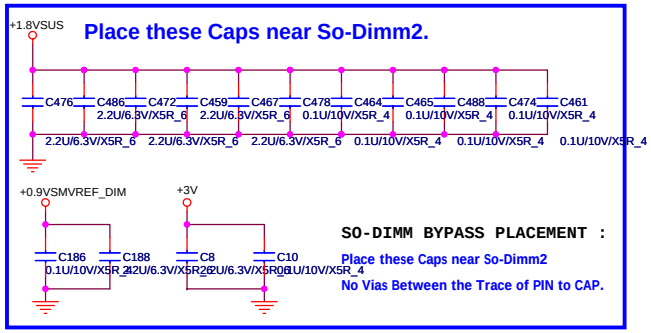


H 5.2









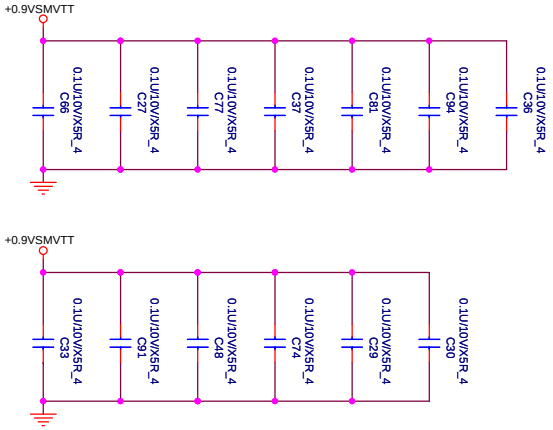
(8,10,11,29,31,32) +1.8VSUS
(3,6,8,11,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V

PROJECT : LE6
Quanta Computer Inc.

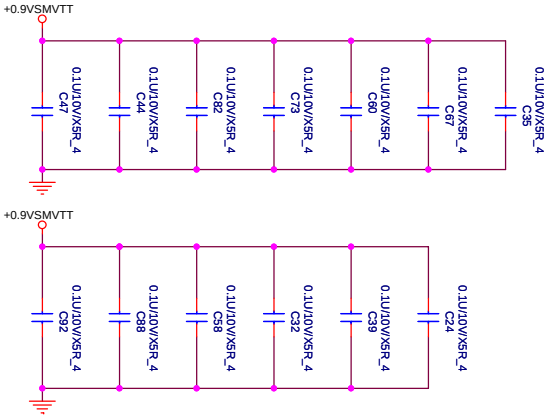
Size	Document Number	Rev
Custom	DDR2 DIMM	1A
Date: Tuesday, April 29, 2008	Sheet 12 of 34	

DDRII DUAL CHANNEL A,B.

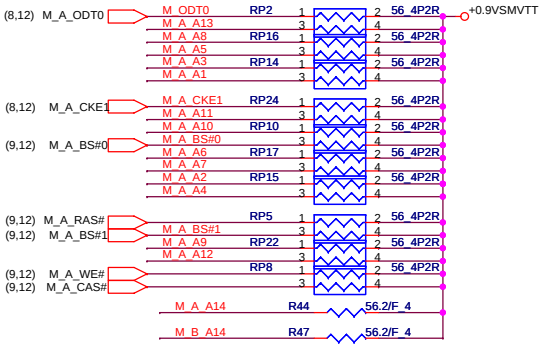
DDRII A CHANNEL

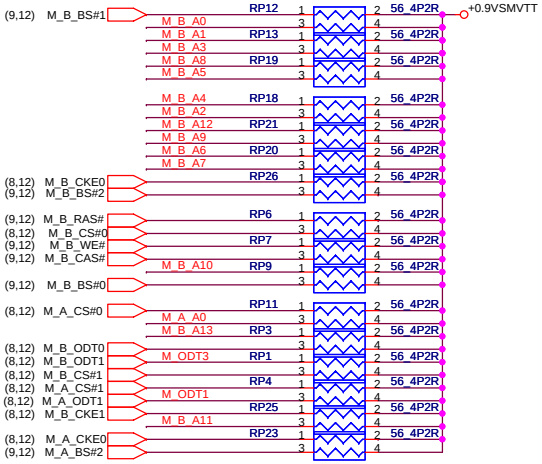


DDRII B CHANNEL



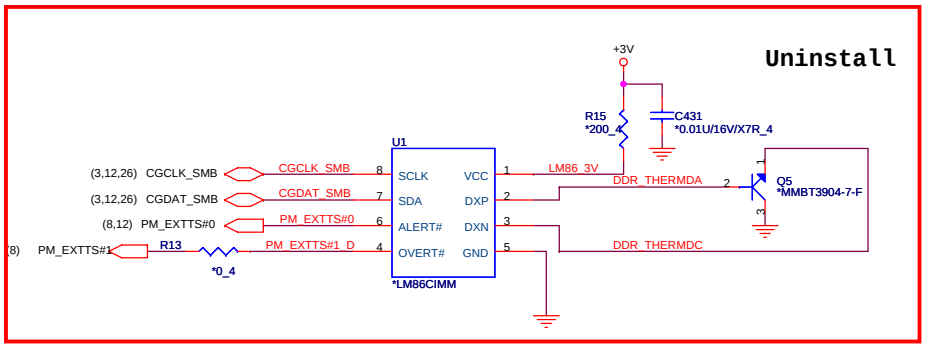
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





M_B_A[14..0] M_B_A[14..0] (9,12)

M_A_A[14..0] M_A_A[14..0] (9,12)



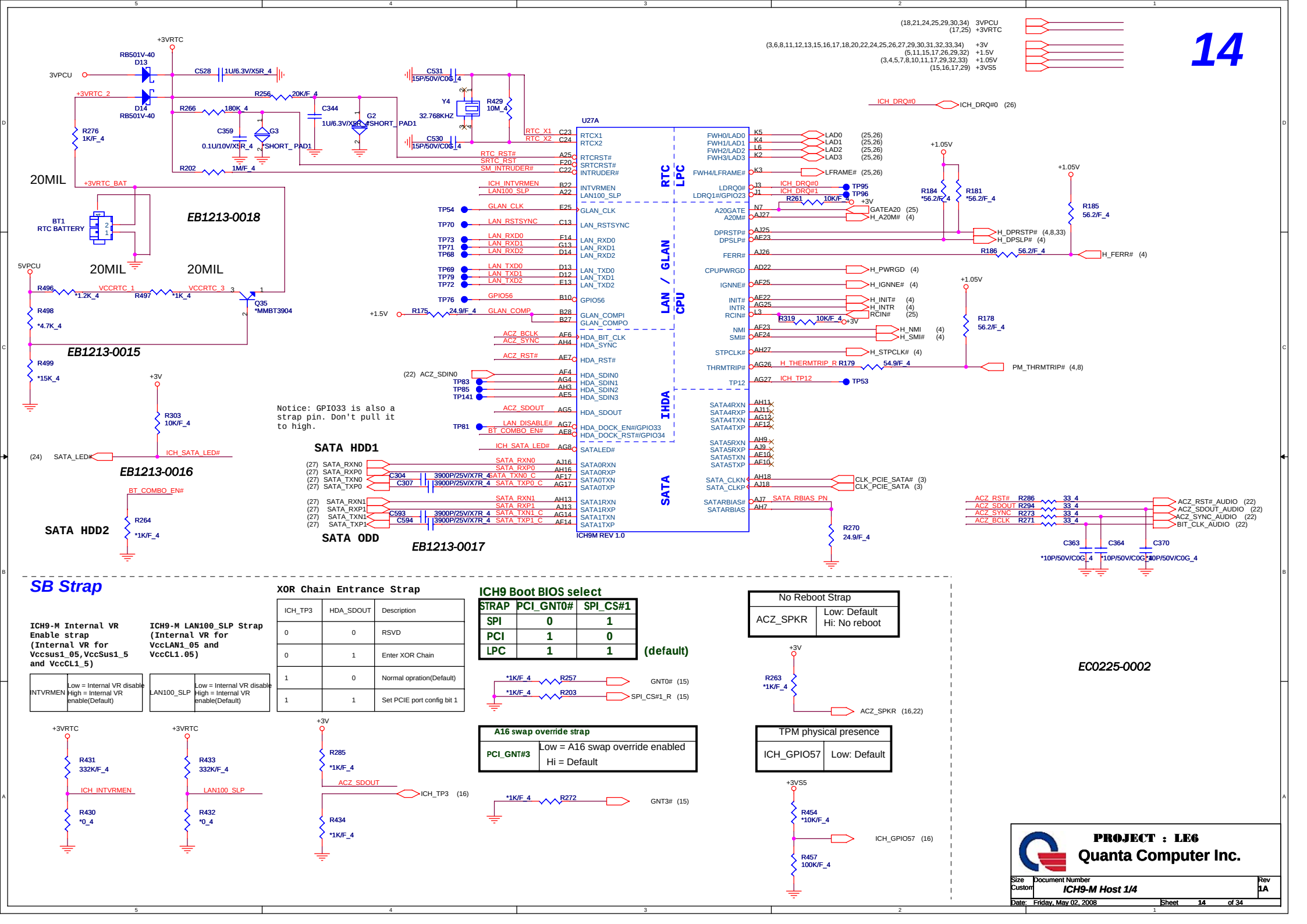
+0.9VSMVTT (29,31)

+3V (3,6,8,11,12,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34)

PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	*DDR2 termination*	1A
Date: Tuesday, April 29, 2008	Sheet 13 of 34	



INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

PCI_GNT#3	Low = A16 swap override enabled Hi = Default

ACZ_SPKR	Low: Default Hi: No reboot

ICH_GPIO57	Low: Default

Size	Document Number	Rev
Custom	ICH9-M Host 1/4	1A

Date: Friday, May 02, 2008 Sheet 14 of 34

(5,11,14,17,26,29,32) +1.5V
(3,6,8,11,12,13,14,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V
(16,22,24,26,29,33) 3VSUS

EC0225-0004

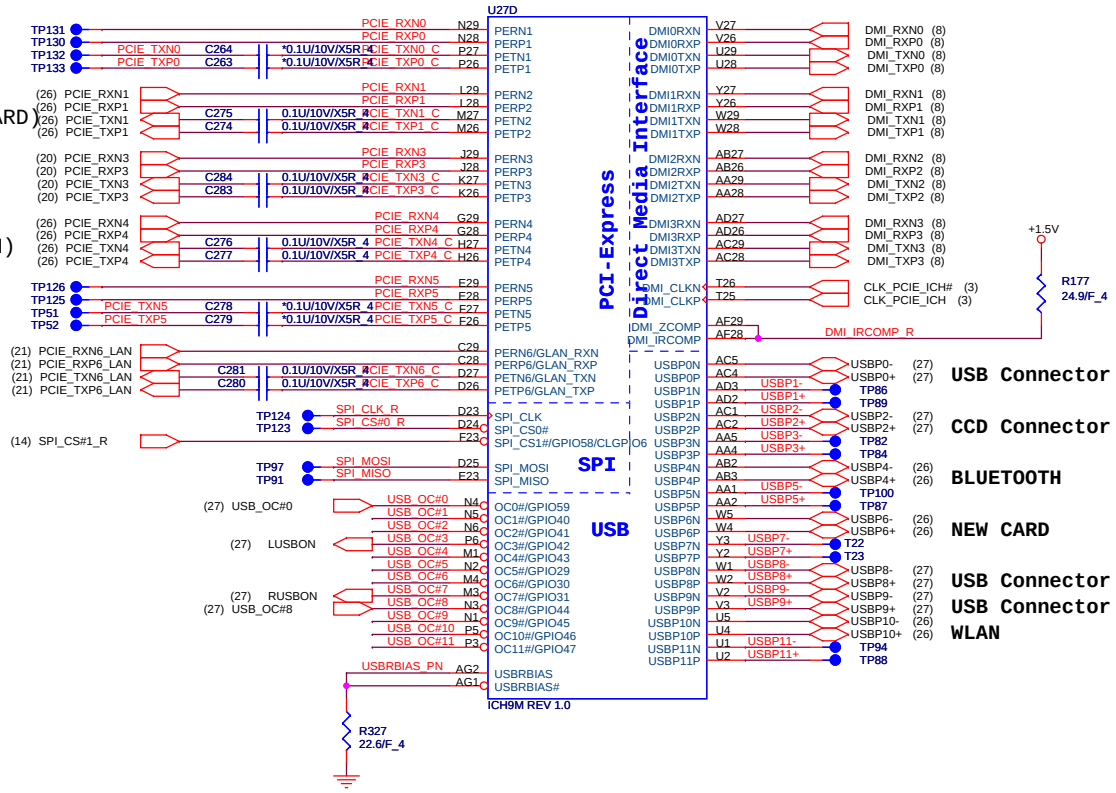
EXPRESS CARD (NEW CARD)

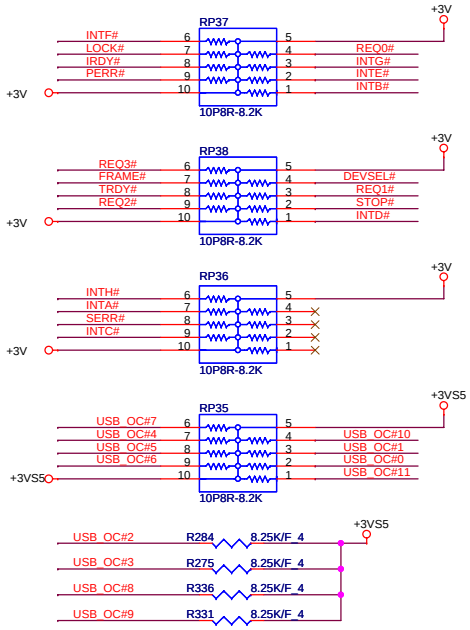
CRAD READER PCI-E

MINI CARD PCI-E(WLAN)

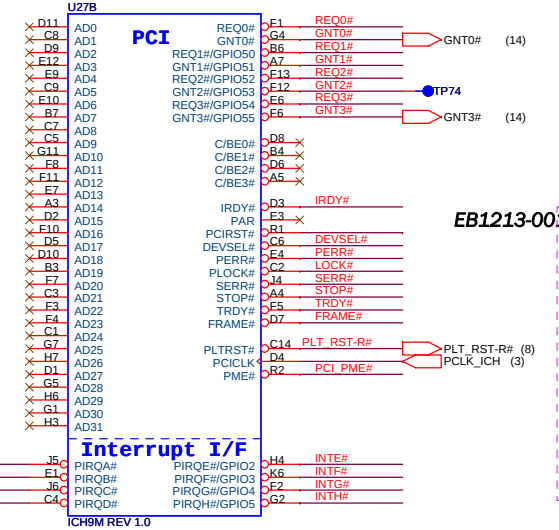
EC0225-0003

PCIE-LAN

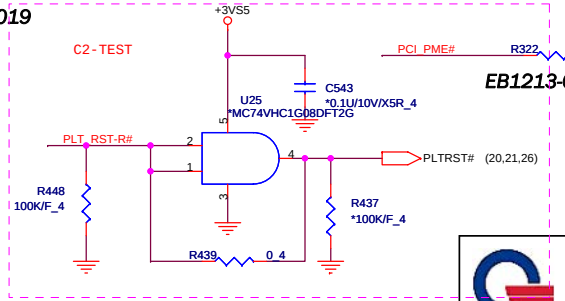




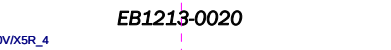
LE6B: Delete HDMI SPI flash IC and relate circuit
2008-4-24



EB1213-0019

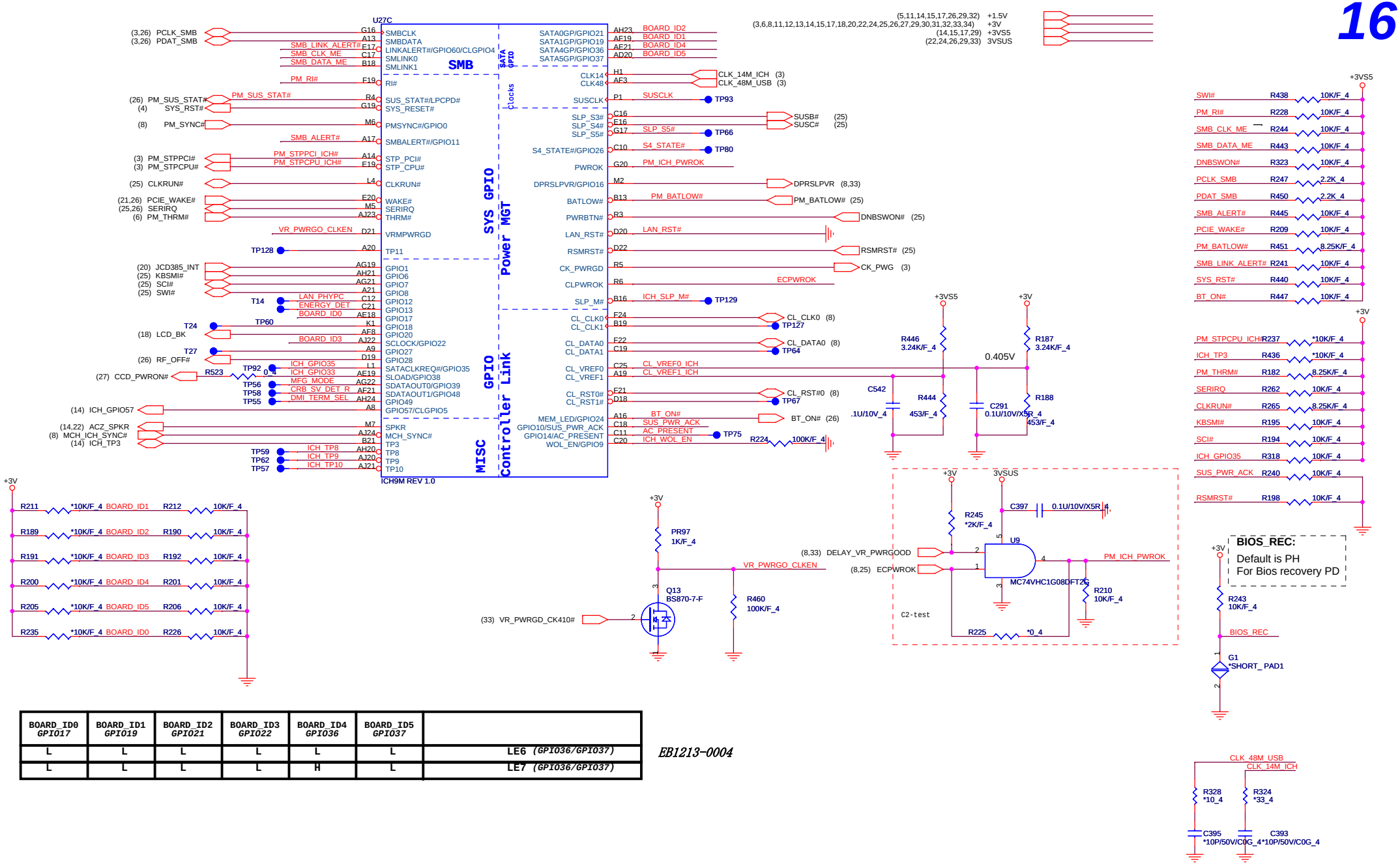


EB1213-0020



PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M PCIE 2/4	1A
Date: Friday, May 02, 2008	Sheet 15 of 34	



BOARD_ID0 GPIO17	BOARD_ID1 GPIO19	BOARD_ID2 GPIO21	BOARD_ID3 GPIO22	BOARD_ID4 GPIO36	BOARD_ID5 GPIO37	
L	L	L	L	L	L	LE6 (GPIO36/GPIO37)
L	L	L	L	H	L	LE7 (GPIO36/GPIO37)

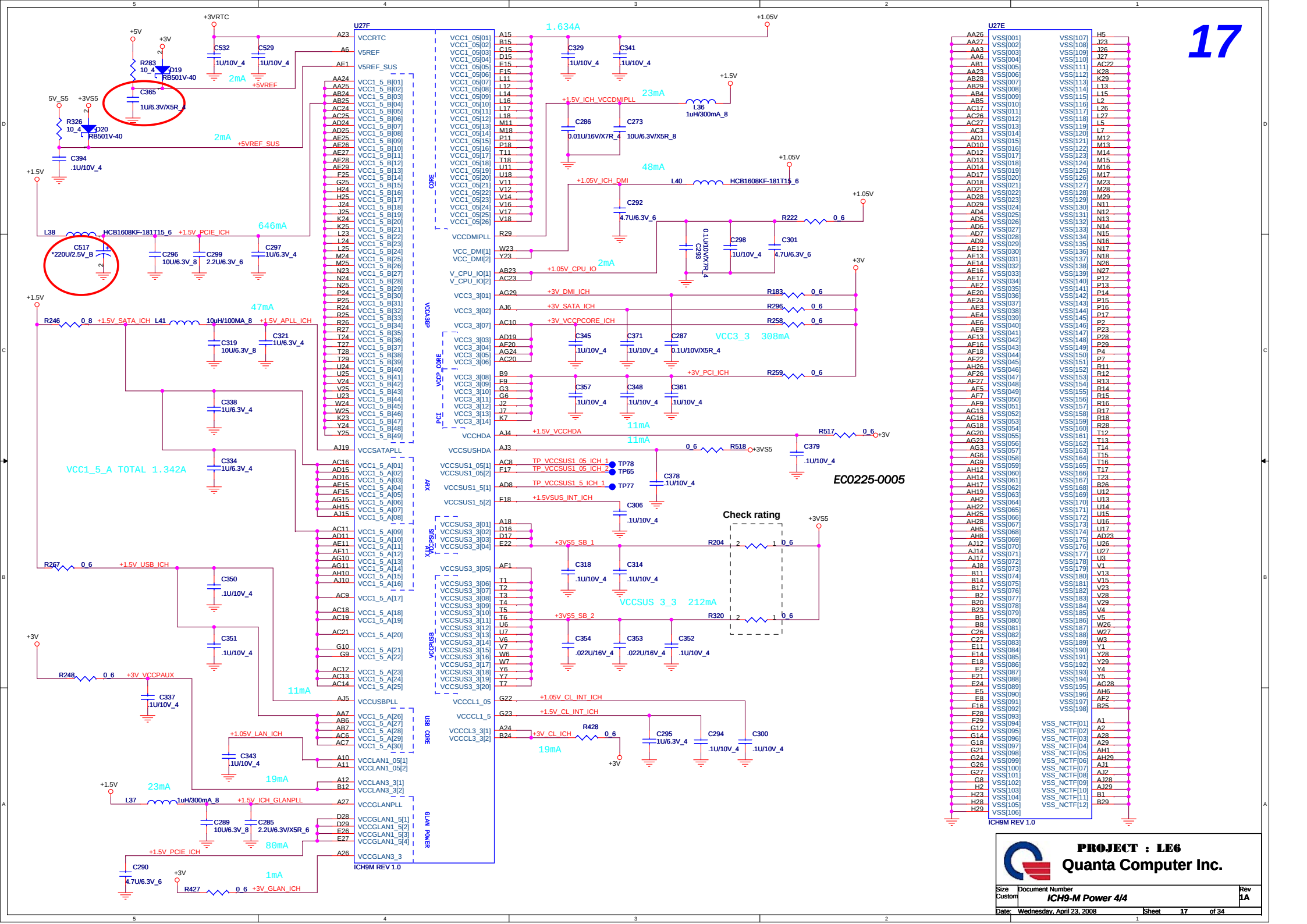
EB1213-0004

PROJECT : LE6

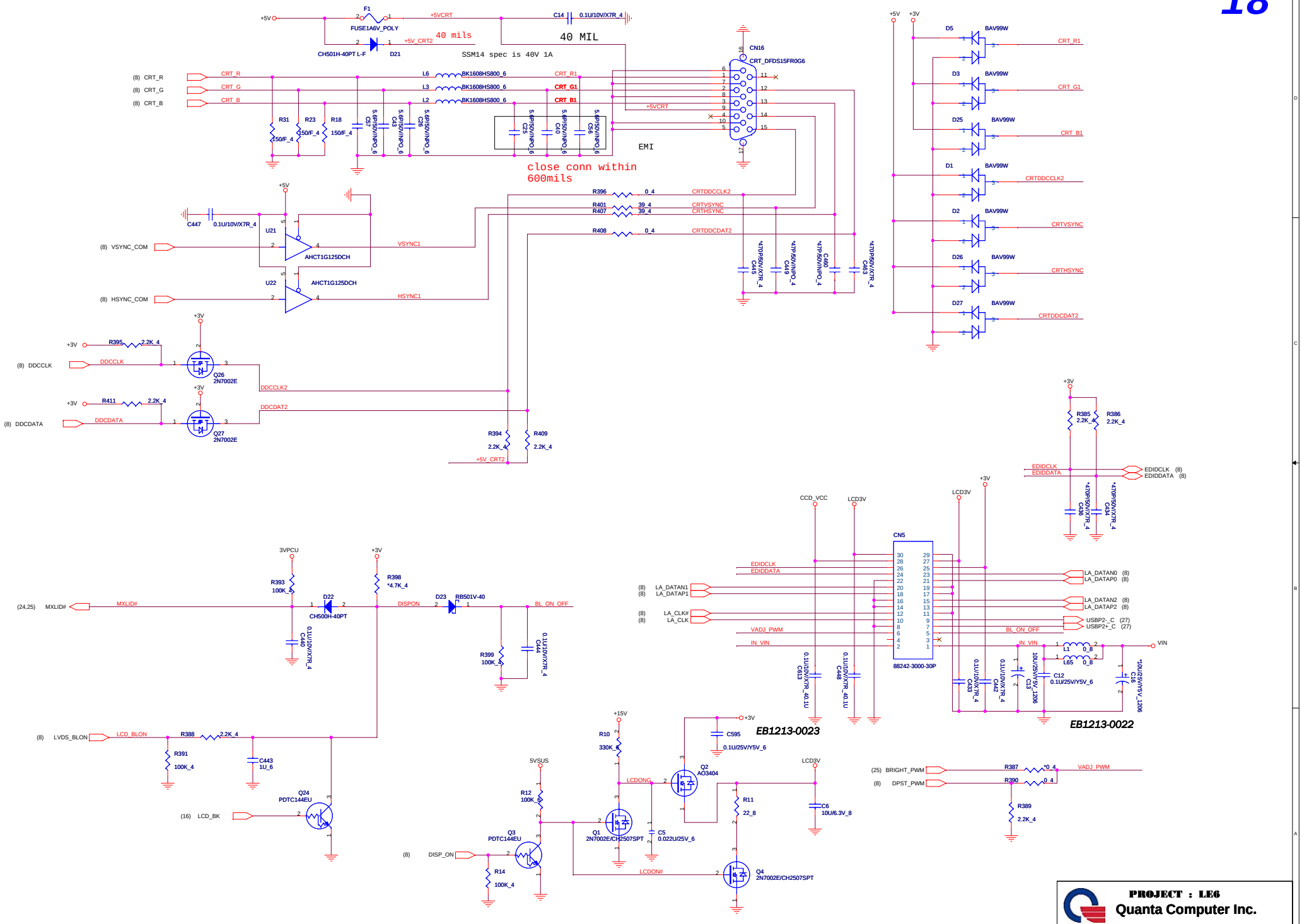
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	1A

Date: Friday, May 02, 2008 Sheet 16 of 34


17
U27F
ICH9M REV 1.0
U27E
ICH9M REV 1.0
EC0225-0005
Check rating
VCC1_5_A TOTAL 1.342A
VCCUS 3_3 212mA
VCC3_3 308mA
PROJECT : LE6
Quanta Computer Inc.
ICH9-M Power 4/4
Size Custom
Document Number
Rev 1A
Date: Wednesday, April 23, 2008
Sheet 17 of 34

CRT PORT



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
C	CRT/LCD/LID SWITCH	1A

Date: Friday, May 02, 2008 Sheet 18 of 34

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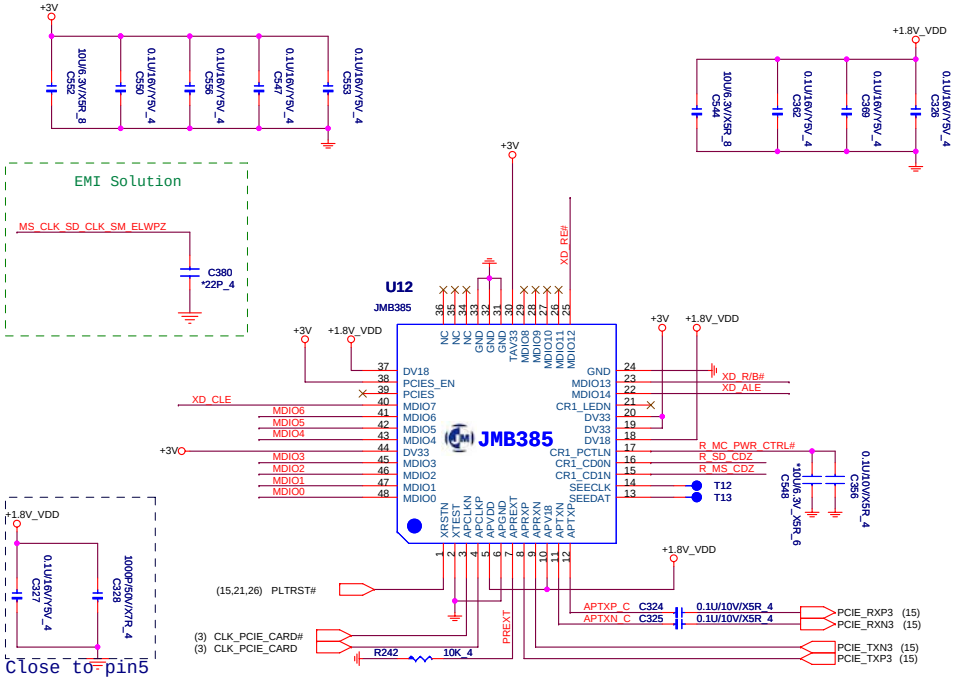
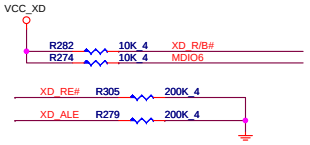
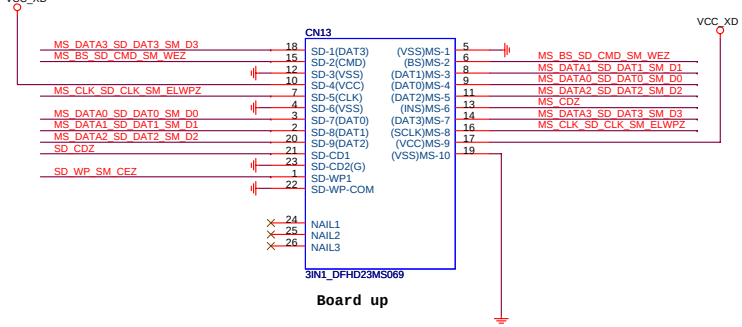
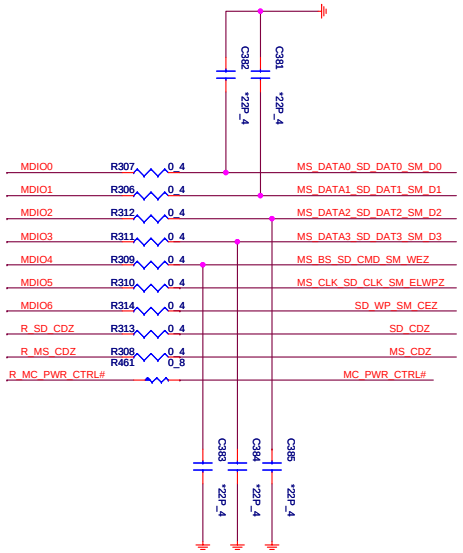
3 IN 1 CARD READER









CARDREADER POWER

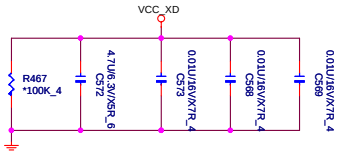
Memory Card Power Supply

EB1213-0025

Use 0805 type and over 20 mils trace width on both side

EB1213-0026

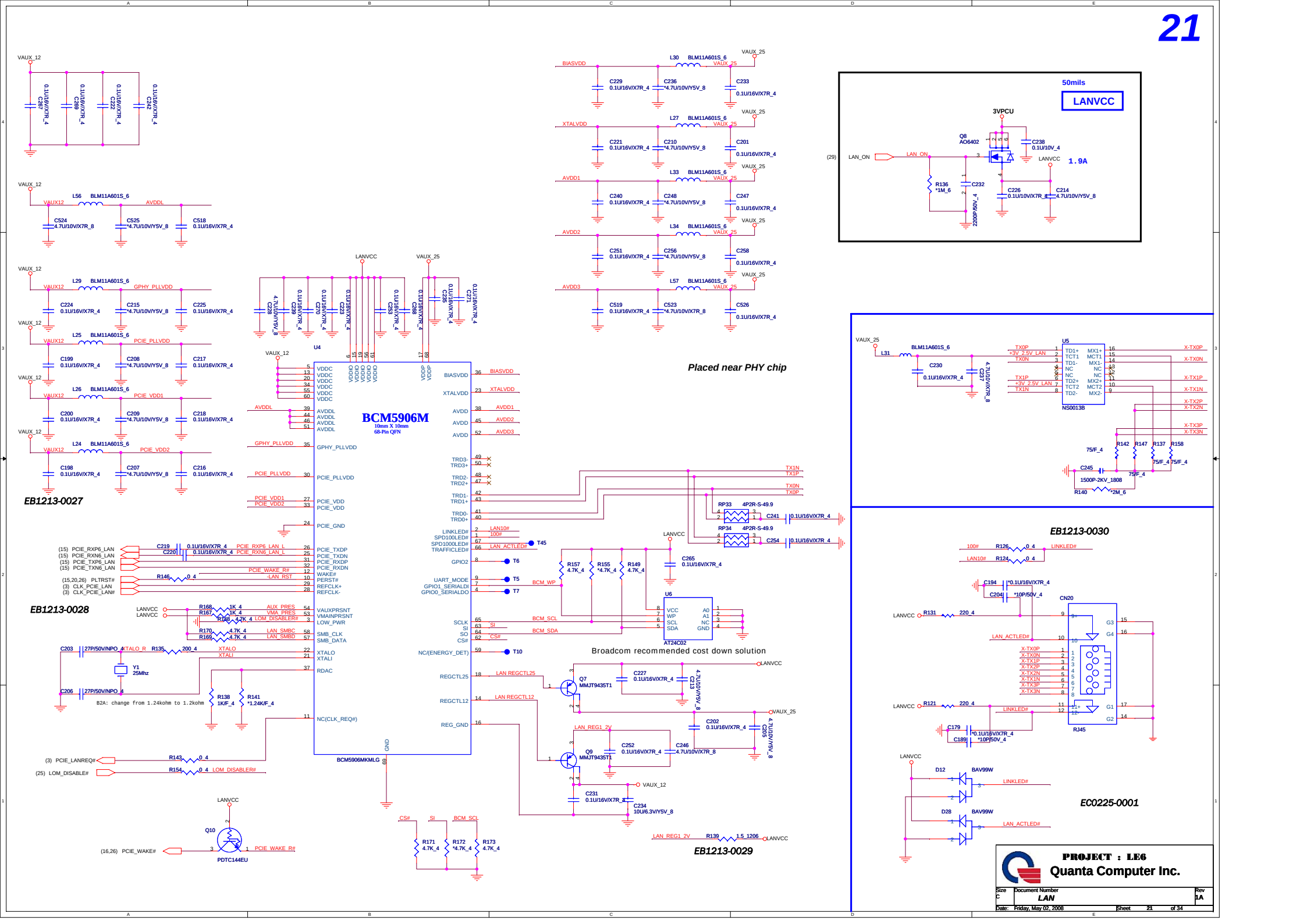
DEL some parts for Q32 R469 C577



PROJECT : LE6

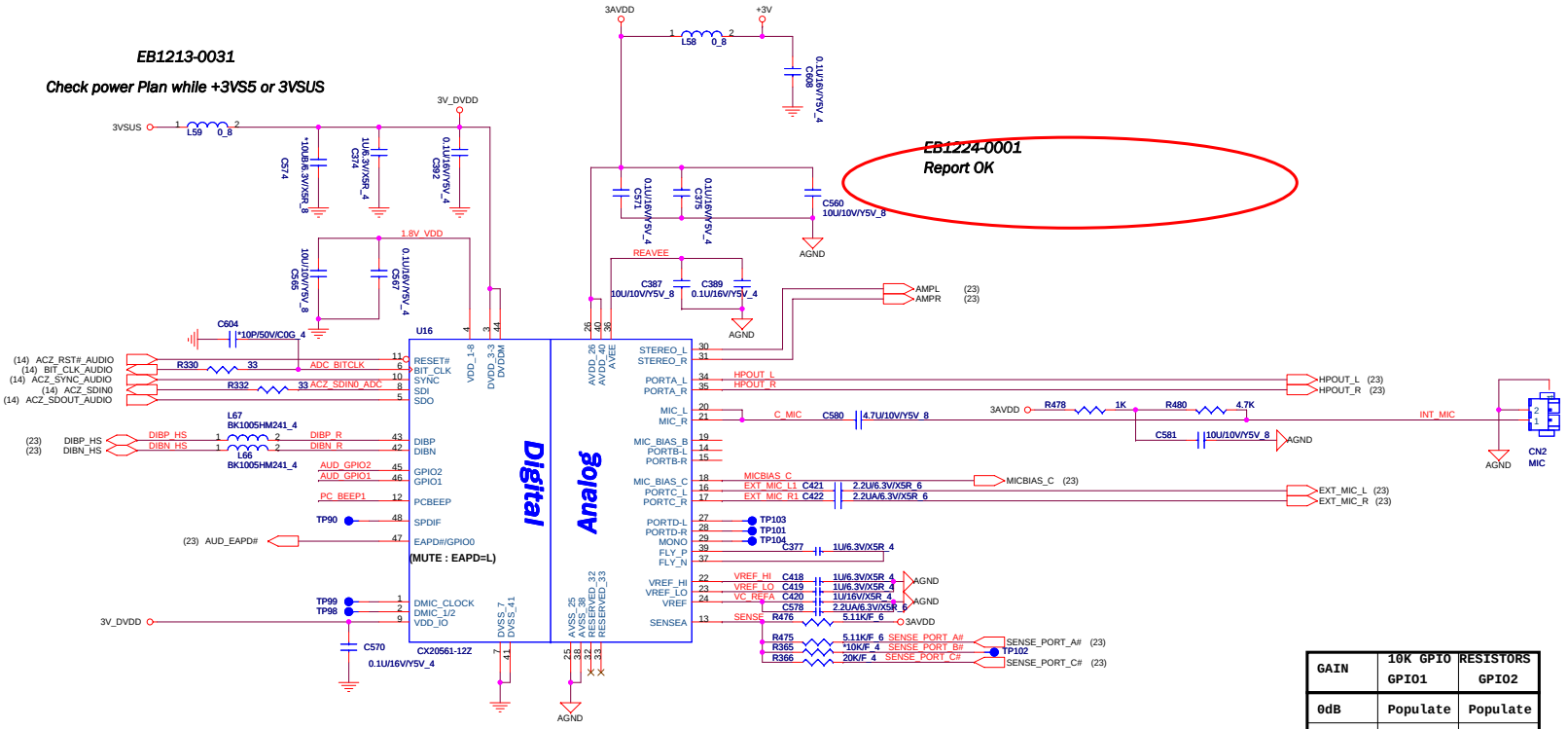
Quanta Computer Inc.

Size	Document Number	Rev
Custom	JMB385 - Card Reader	2A
Date: Tuesday, April 29, 2008	Sheet 20 of 34	


BCM5906M
10mm X 10mm
68-Pin QFN
BCM5906MKMLG
EB1213-0027
EB1213-0028
EB1213-0029
EB1213-0030
EC0225-0001
Placed near PHY chip
Broadcom recommended cost down solution
LANVCC
50mils
3VPCU
1.9A
U4
U5
U6
Q7
Q8
Q9
Q10
RJ45
CN20
NS0013B
AT24C02
PDTC144EU
PROJECT : LE6
Quanta Computer Inc.
Size C
Document Number LAN
Rev 1A
Date: Friday, May 02, 2008
Sheet 21 of 34

EB1213-0031

Check power Plan while +3VS5 or 3VSUS



EB1224-0001
Report OK

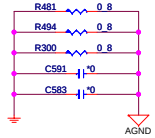
EB1213-0032

Check power Plan while +1.5VS5 or 1.5VSUS

GAIN	10K GPIO GPIO1	RESISTORS GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

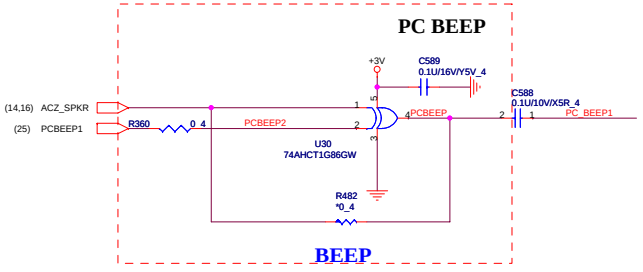
STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-B	EXTERNAL MIC

FOR EMI SOLUTION



Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

LE6B:Add R360 and change U30 to OR gate base on customer request



PROJECT : LE6
Quanta Computer Inc.

Size	Document Number	Rev
C	AUDIO CODEC(CX20561-12Z)	1A

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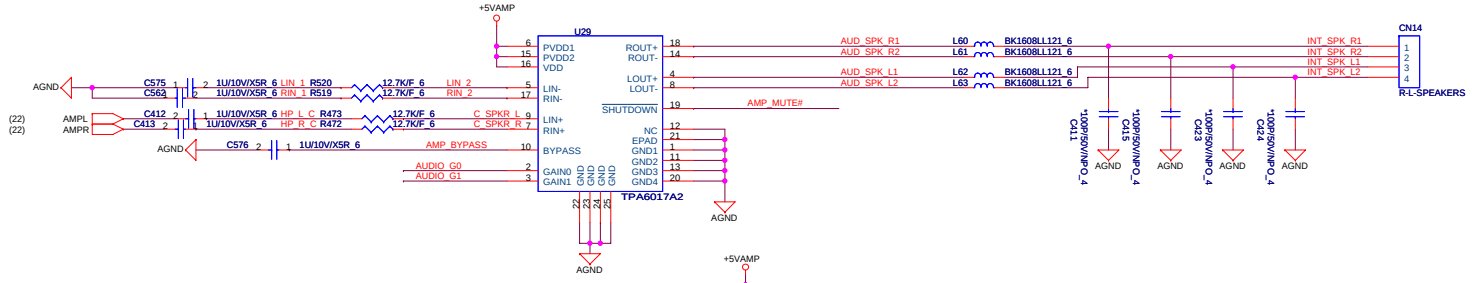
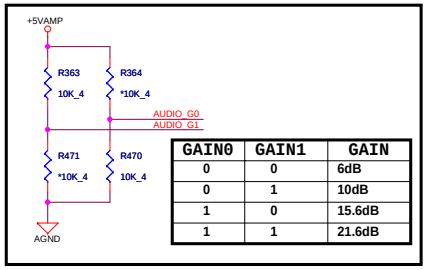
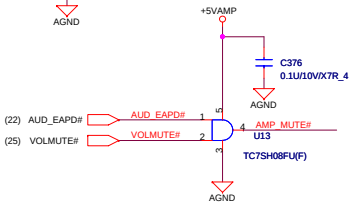
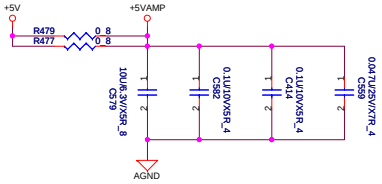
INTERNAL SPEAKER AMPLIFIER





GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

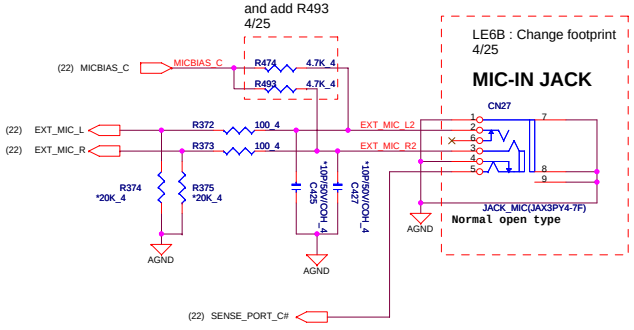




LE6B : Change connrction of MICBIAS_C and add R493 4/25

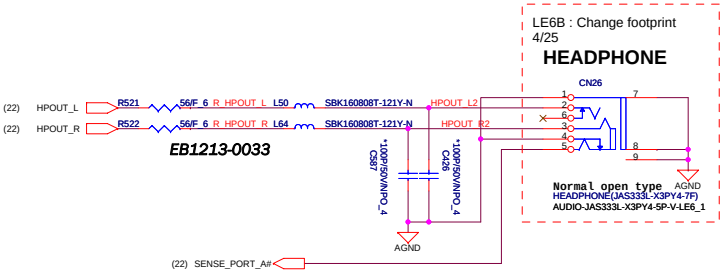
LE6B : Change footprint 4/25

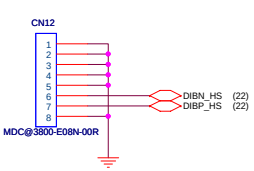
MIC-IN JACK



LE6B : Change footprint 4/25

HEADPHONE





Modem connector

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Quanta Computer Inc.

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C	TPA6017 & JACKS & MDC	1A

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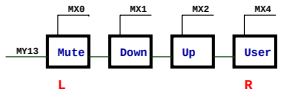
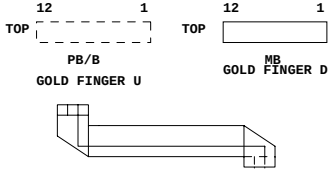
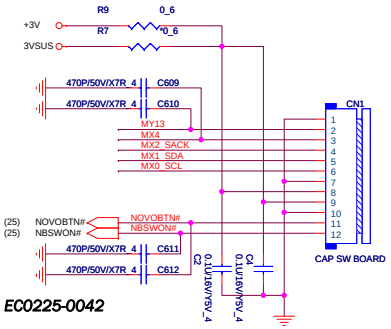
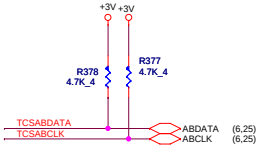
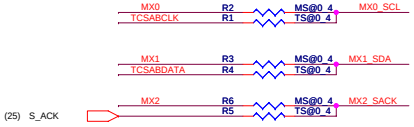






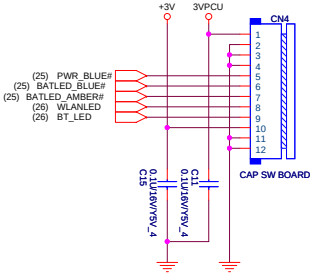
EC0225-0042

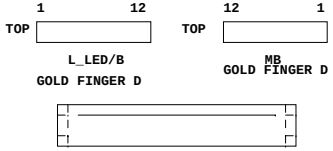


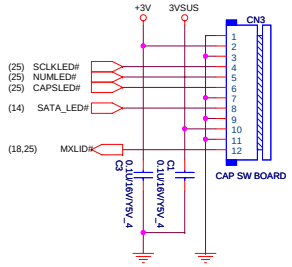


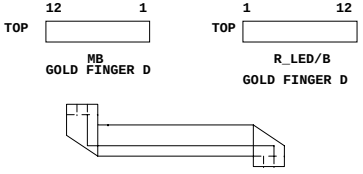
check EC and Vendor for CTS

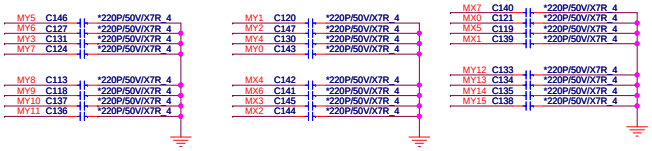
EB1213-0022



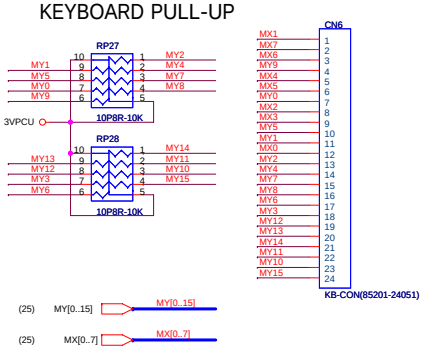




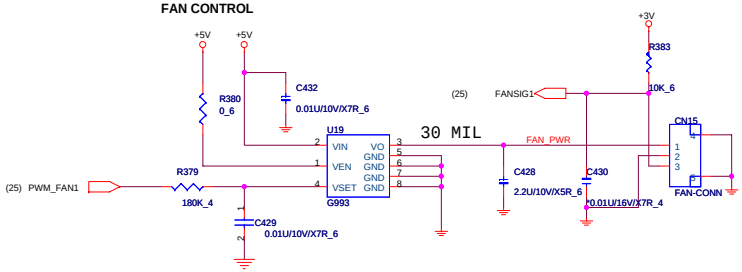


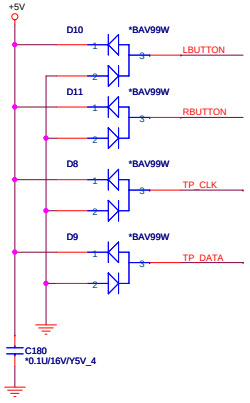


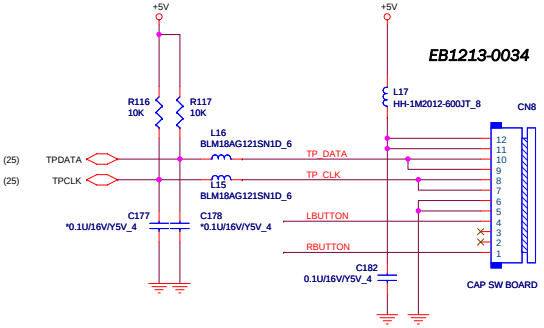
KEYBOARD PULL-UP



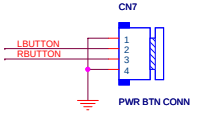
FAN CONTROL







EB1213-0034



PROJECT : LE6

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C	*KEYBOARD/FAN*	1A

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IT8512/IT8502

L46 BLM18AG121SN1D 3VPCU
L49 BLM18AG121SN1D 3VPCU
(For PLL Power)
C372 1000P/16V/X7R_4
C373 0.1U/10V/X5R_4
C410 0.1U/10V/X5R_4
L47 BLM18AG121SN1D
IT8512_AGND

+3VRTC
R333 0_4
RTC_VCC
3VPCU
Layout Note:
Place all capacitors close to IT8512.
C399 0.1U/16V/Y5V_4
C555 0.1U/16V/Y5V_4
C409 0.1U/16V/Y5V_4
C340 0.1U/16V/Y5V_4
C400 0.1U/16V/Y5V_4
C558 0.1U/16V/Y5V_4
C408 0.1U/16V/Y5V_4

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
+3V
3VPCU
RTC_VCC
C391 0.1U/16V/Y5V_4

MBCLK R356 4.7K_4
MBDATA R357 4.7K_4
ABCLK R358 *4.7K_4
ABDATA R359 *4.7K_4
MY16 R252 10K_4
MY17 R251 10K_4
NOVOBTN# R253 10K_4
3VPCU

POWER SWITCH
3VPCU
R462 10K_4
NBSWON#
C563 0.1U/10V/X5R_4
G4 SHORT_PAD1

OL_EVENT
GLOBAL_WL_DISABLE#
T46
GLOBAL_WL_DISABLE# (26)
LOM_DISABLE# (21)
MY16
MY17
T16
VOLMUTE# (23)
ECPWROK (8,16)
BAYINS#
T34
RSMRST# (16)
VRON (29,33)
LAN_POWER (29)
MAINON (29,31,32)
SUSON (29,31)
S5_ON (29)
R334 0_4 CLKRUN# (16)
HWPG R281 10K_4 +3V

U14
IT8502E-L

(14,26) LAD0
(14,26) LAD1
(14,26) LAD2
(14,26) LAD3
(18,24) MXLID#
(3) PCI_CLK_8502
(14,26) LFRAME#
(16) SWI# SW1010CPT D16 BAYSWAP#
(14) GATEA20
(16,26) SERIRQ
(16) KBSMI# SW1010CPT D18 D_KBSMI#
(16) SCI# SW1010CPT D15 D_SCI#
WRST_8512#
(14) RCIN# RCIN#
(24) TP_LED#
LPC

GPIO
SM BUS
PS/2
SMCLK0/GPB3 MBCLK (30)
SMDAT0/GPB4 MBDATA (30)
SMCLK1/GPC1 ABCLK (6,24)
SMDAT1/GPC2 ABDATA (6,24)
SMCLK2/GPE6 CAPSLED# (24)
SMDAT2/GPF7 NUMLED# (24)
PS2CLK0/GPF0 MSCLK T42
PS2DAT0/GPF1 MSDATA T43
PS2CLK1/GPF2 KPCLK T40
PS2DAT1/GPF3 KPDATA T41
PS2CLK2/GPF4 TPCLK
PS2DAT2/GPF5 TPDATA
TPCLK (24)
TPDATA (24)

EB1213-0035

(30) D/C# T33 CIR_TX CIR

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

PWM
PWM0/GPA0 PWR_BLUE PWR_BLUE# (24)
PWM1/GPA1 LED_ON# T28
PWM2/GPA2 PWM_FAN1 (24)
PWM3/GPA3 PCBEEP1 PCBEEP1 (22)
PWM4/GPA4 LAN_WOL_EN T18
PWM5/GPA5 SCLKLED SCLKLED# (24)
PWM6/GPA6 ME_EC_ALERT_1 T17
PWM7/GPA7 BRIGHT_PWM BRIGHT_PWM (18)
TACH0/GPD6 FANSIG2 T15 FANSIG1 (24)
TACH1/GPD7
TMR0/WUI2/GPC4 ADIN# (30)
TMR1/WUI3/GPC6 S_ACK S_ACK (24)

WAKE UP
PWRSW/GPE4 NBSWON# NBSWON# (24)
RI1#/WUI0/GPD0 SUSB# (16)
RI2#/WUI1/GPD1 ACIN (30)
WUI5/GPE5 NOVOBTN#
RING#/PWRFAIL#/LPCRST#/GPB7 D30 SW1010CPT NOVOBTN# (24) PM_BATLOW# (16)

UART
TXD/GPB1 BATLED_AMBER# (24)
RXD/GPB0 BATLED_BLUE# (24)

A/D D/A
ADC0/GPI0 TEMP_MBAT (30)
ADC1/GPI1 MBATV (30)
ADC2/GPI2 ICMNT (30)
ADC3/GPI3 ABATV T19
ADC4/GPI4 MEP_CLK T21
ADC5/GPI5 MEP_DATA T29
ADC6/GPI6 HWPG (31,32,33,34)
ADC7/GPI7 SUSC# (16)
DAC0/GPJ0 CC-SET (30)
DAC1/GPJ1 CV_SET T30
DAC2/GPJ2 BL/C# (30)
DAC3/GPJ3 DAREF T47
DAC4/GPJ4 DNBSWON#_R T31
DAC5/GPJ5 D17 SW1010CPT DNBSWON# (16)

CLOCK
CK32KE
CK32K
CRY2
CRY1
Y3
32.768KHZ
C406 10P/50V/CGO_4
C407 10P/50V/CGO_4

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

3VPCU
R316 470K_4
WRST_8512#
C386 0.1U/10V/X5R_4
R355 *10K_4
IT8512_TM
R354 100K_4

TMKBC Function	
High	Enable
Low	Disable

FLASH
(30) CELL_SLT R353 0_4 IT8512_TM
T35 PCICGRST#
8512_SCK
8512_SO
8512_SI
8512_SCE#
EC_ME_ALERT_1
T36
FLRST#/WUI7/GPG0/TM
FLCLK/SCK
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE#
FLFRAME#/GPG2

KBMX
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

(24) MY[0..15]
(24) MX[0..7]

VSS VSS VSS VSS VSS VSS VSS VSS AVSS
IT8512_AGND
C597 0.1U/10V/X5R_4
C598 1U/6.3V/X5R_4

EB1213-0036
EC0225-0042

16Mbit (2M Byte), SPI
3VPCU
R367 10K_4
R371 10K_4
U18
8512_SCE# CE#
8512_SCK SCK
8512_SI SI
8512_SO SO
WP#
VDD
HOLD#
VSS
R352 47_4
R351 47_4
R370 15_4
C416 0.1U/16V/Y5V_4
ST_SST25VF008B

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

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Custom	EC IT8502	1A

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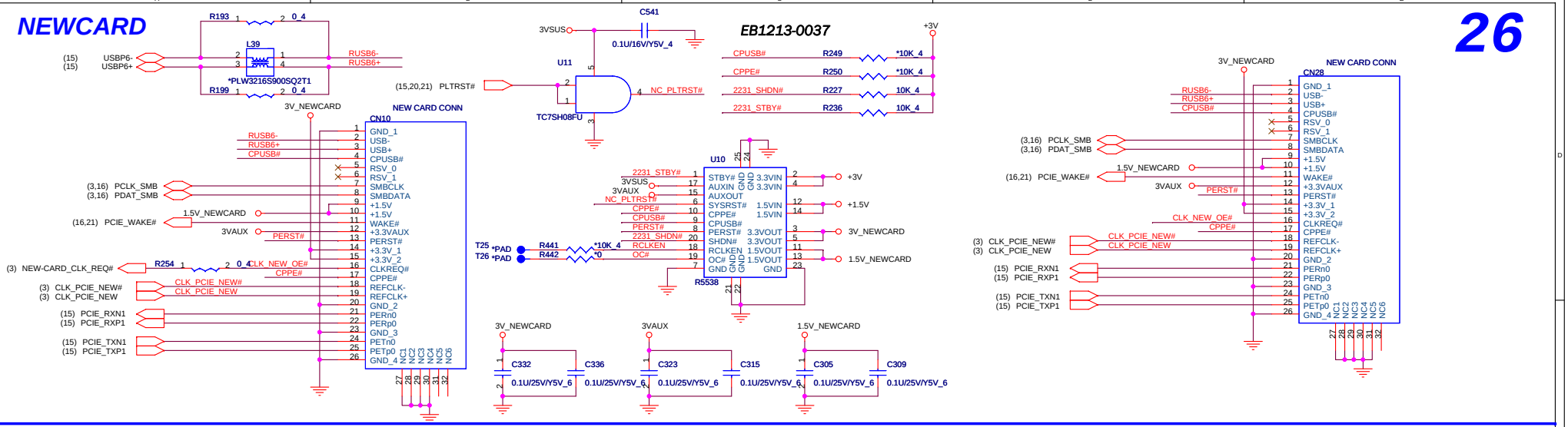
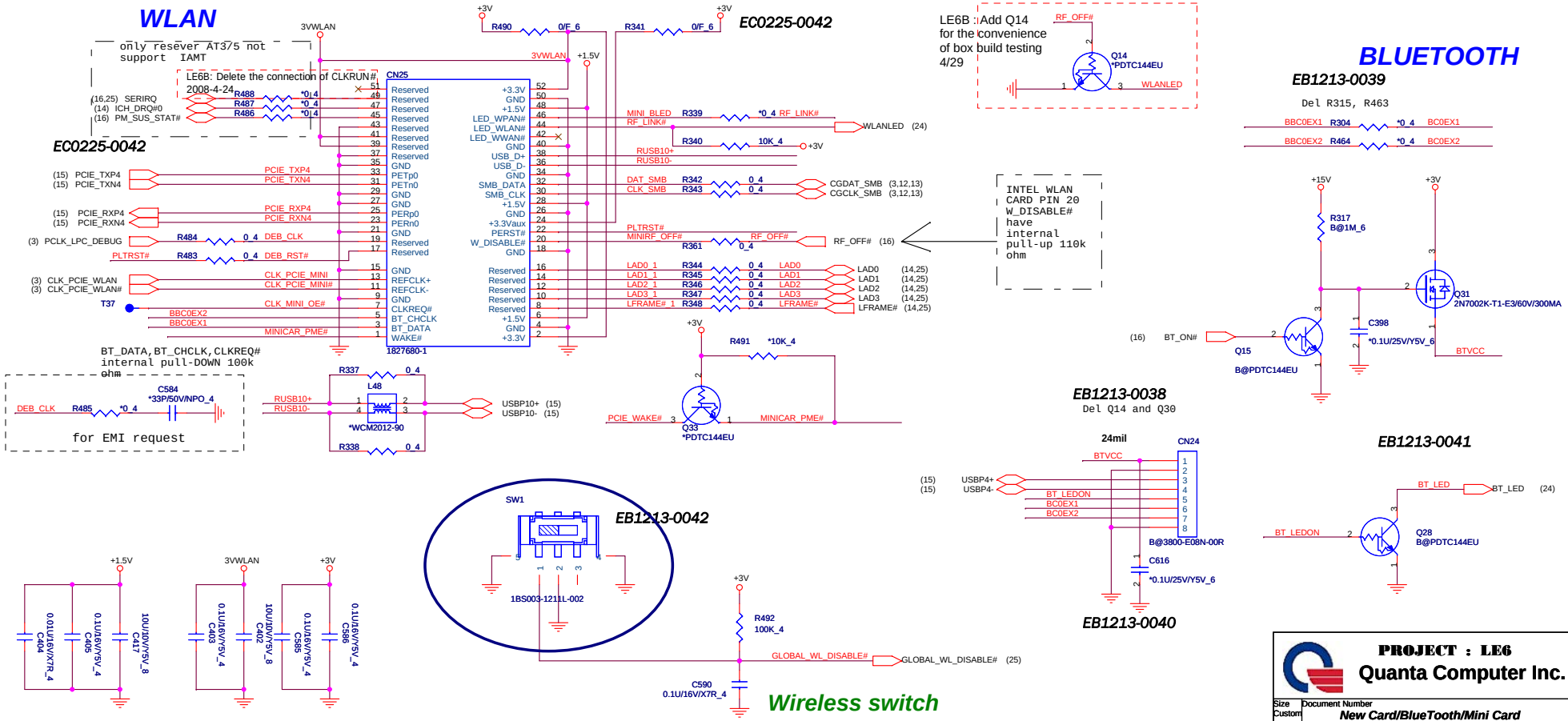
NEWCARD



Mini PCI-E Card 1
WLAN



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Quanta Computer Inc.

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Custom	New Card/BlueTooth/Mini Card	1A
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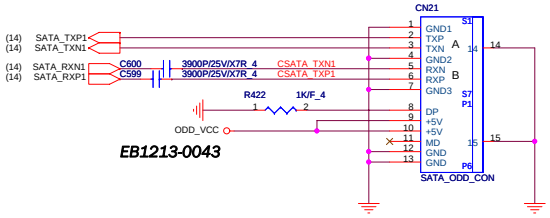
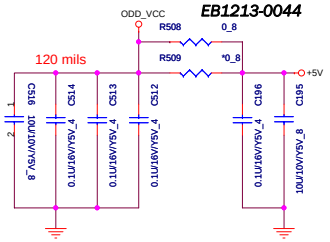
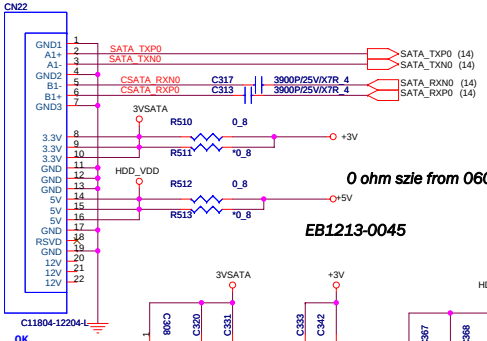
SATA CD-ROM



0 ohm szie from 0603 to 0805

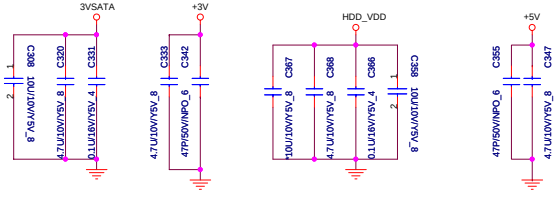


SATA_1 CONNECTOR

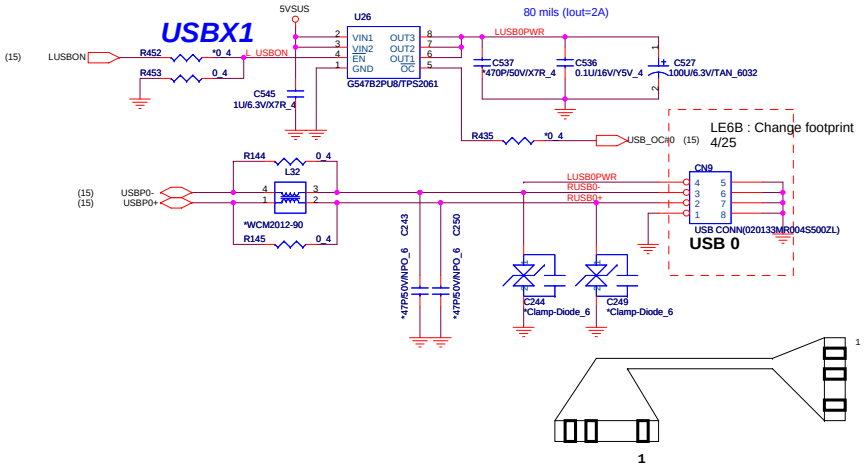


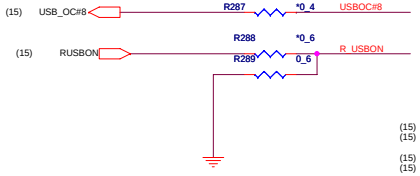
0 ohm szie from 0603 to 0805

EB1213-0045

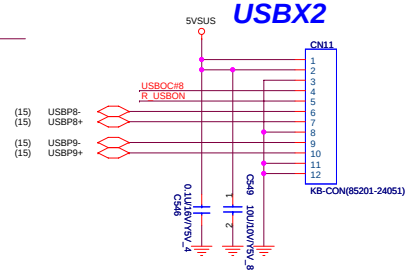


USBX1

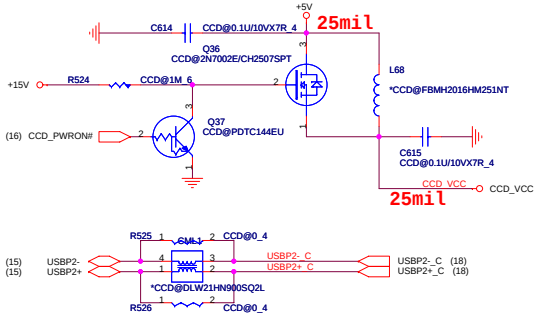




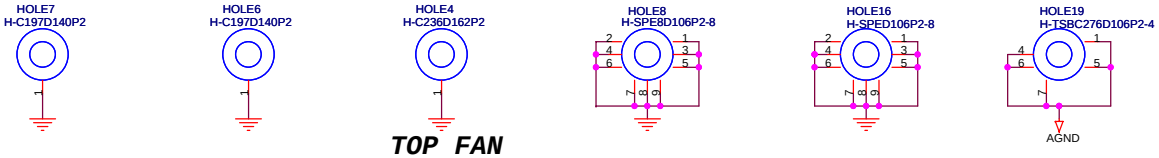
USBX2



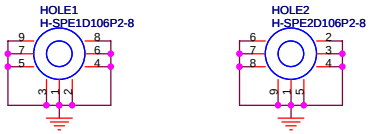
CCD MODULE

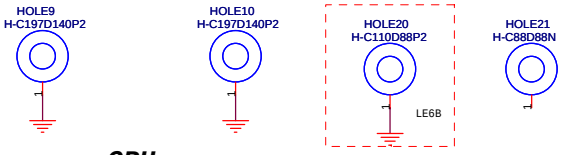


CCD_PWRON#	High	Low
	Disable	Enable



TOP FAN





CPU

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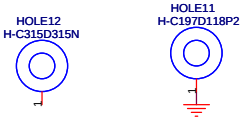

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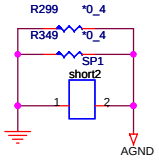
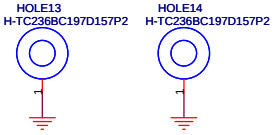
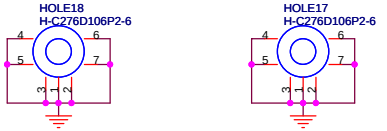




MINI-PCIe



USB

EB1224-0001

RSPKR

RSPKL

BOT NB

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Size	Document Number	Rev
Custom	EMI PAD/SCREW/DEBUG PORT	1A
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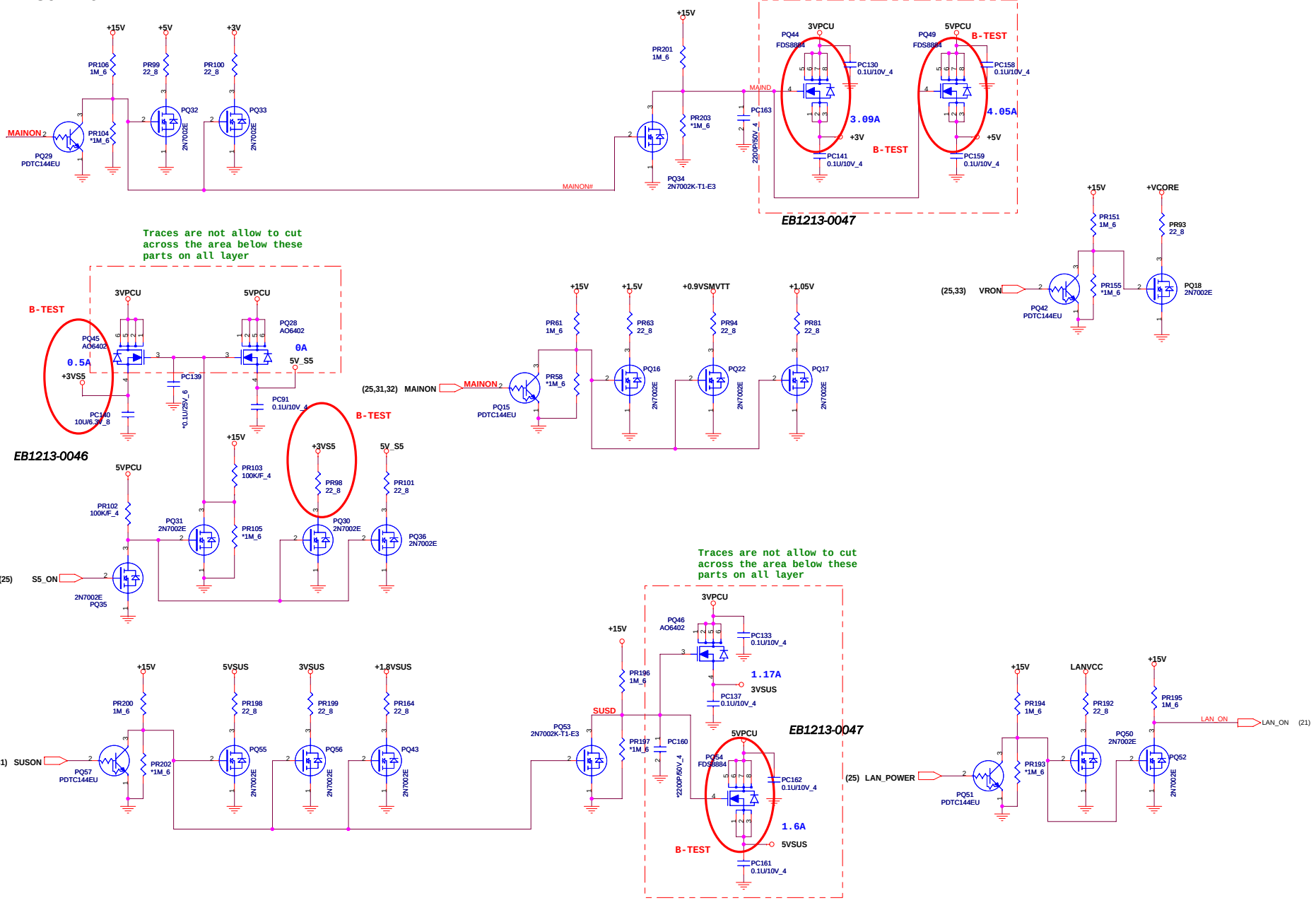
DISCHARGE



PROJECT : LE6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

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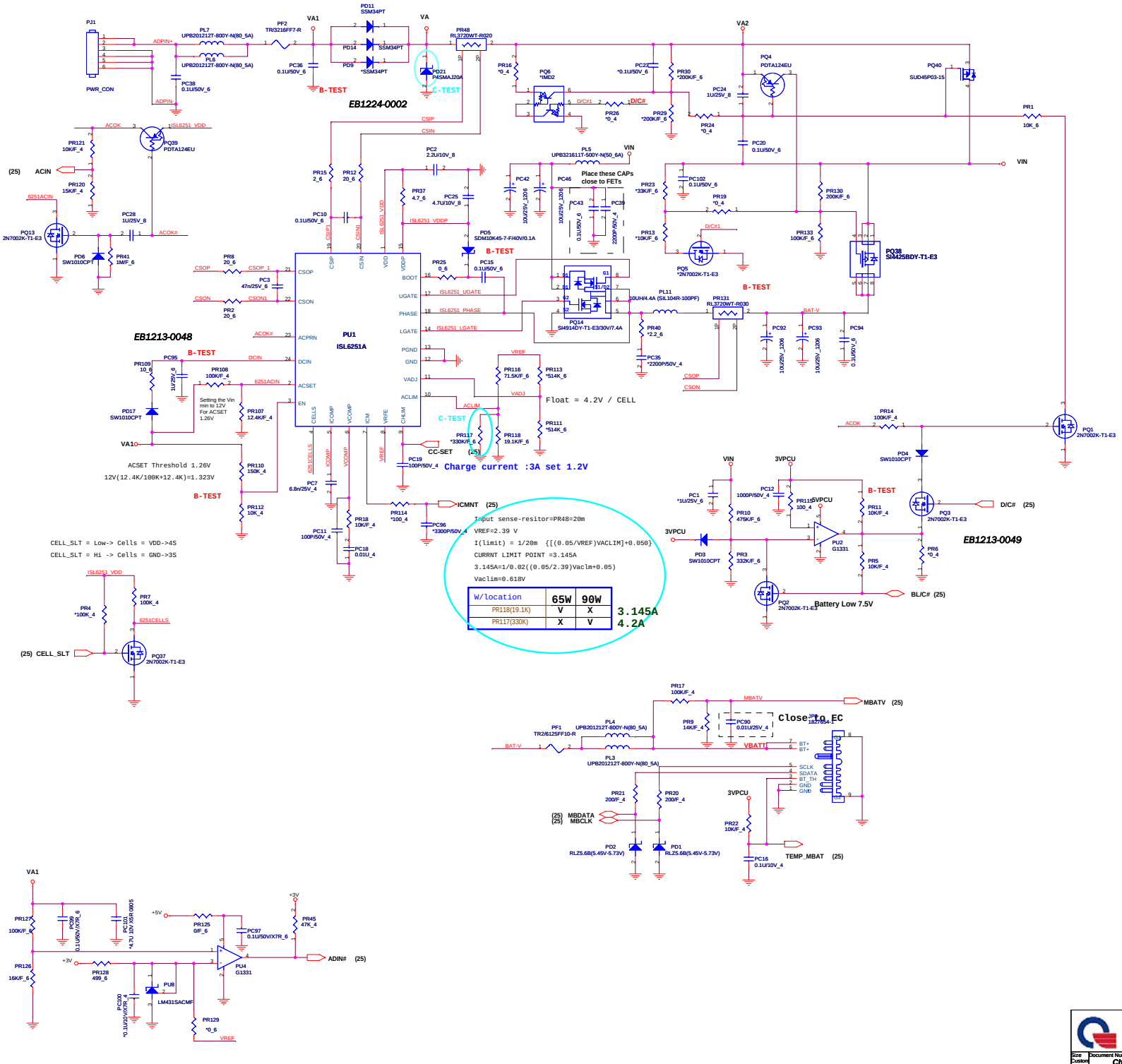

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Size: Custom	Document Number: Charger (ISL6251A)	Rev: 1A
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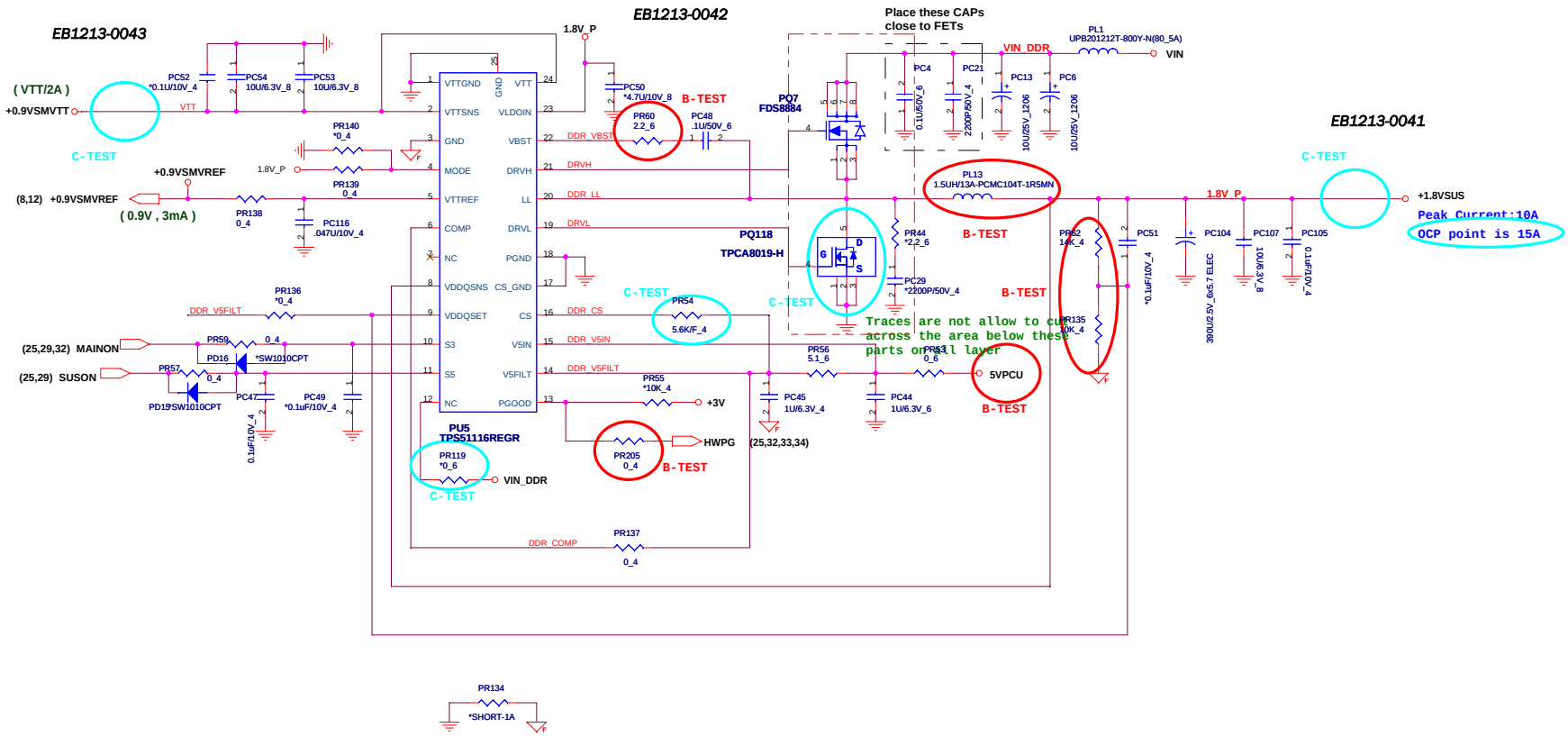

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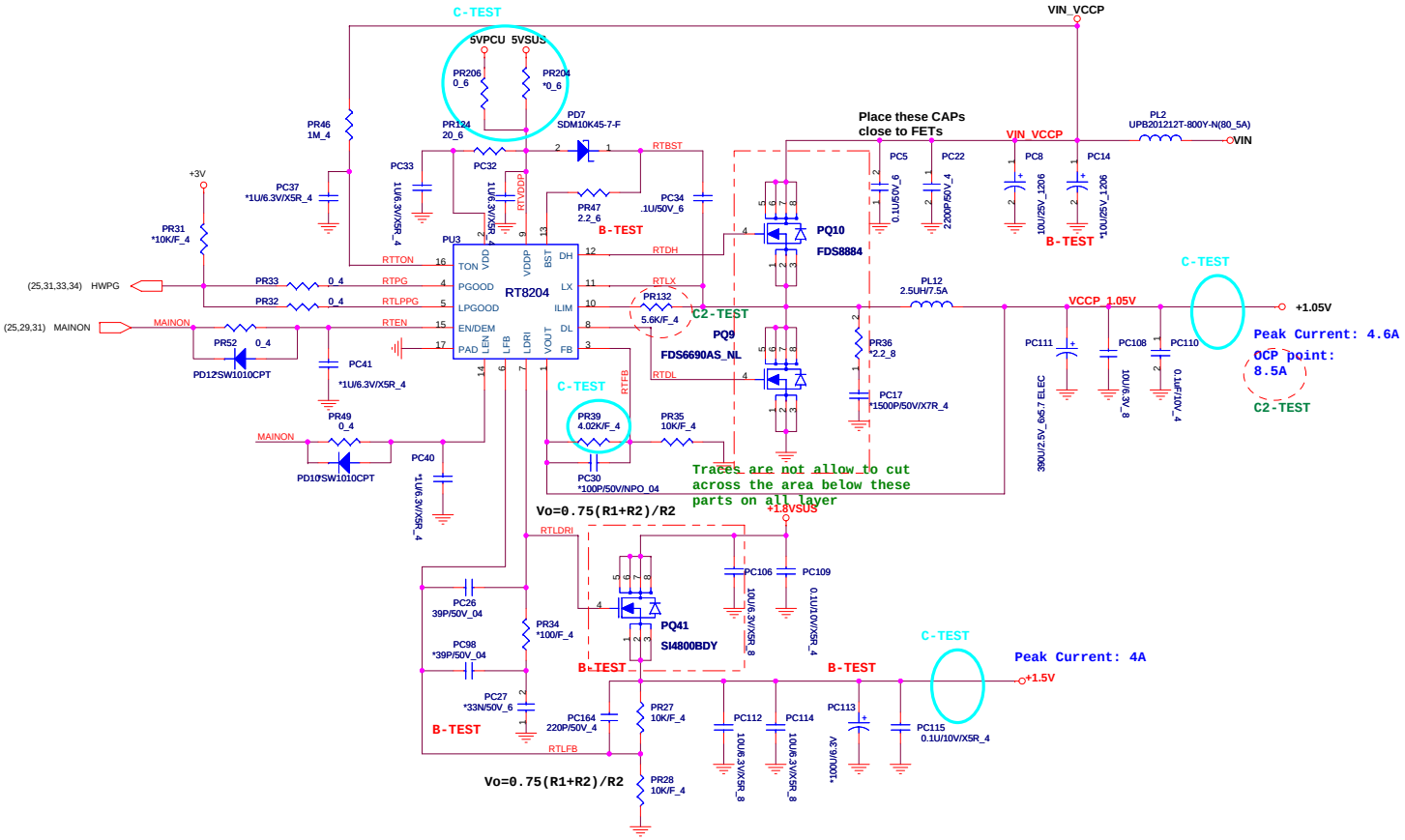

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Quanta Computer Inc.

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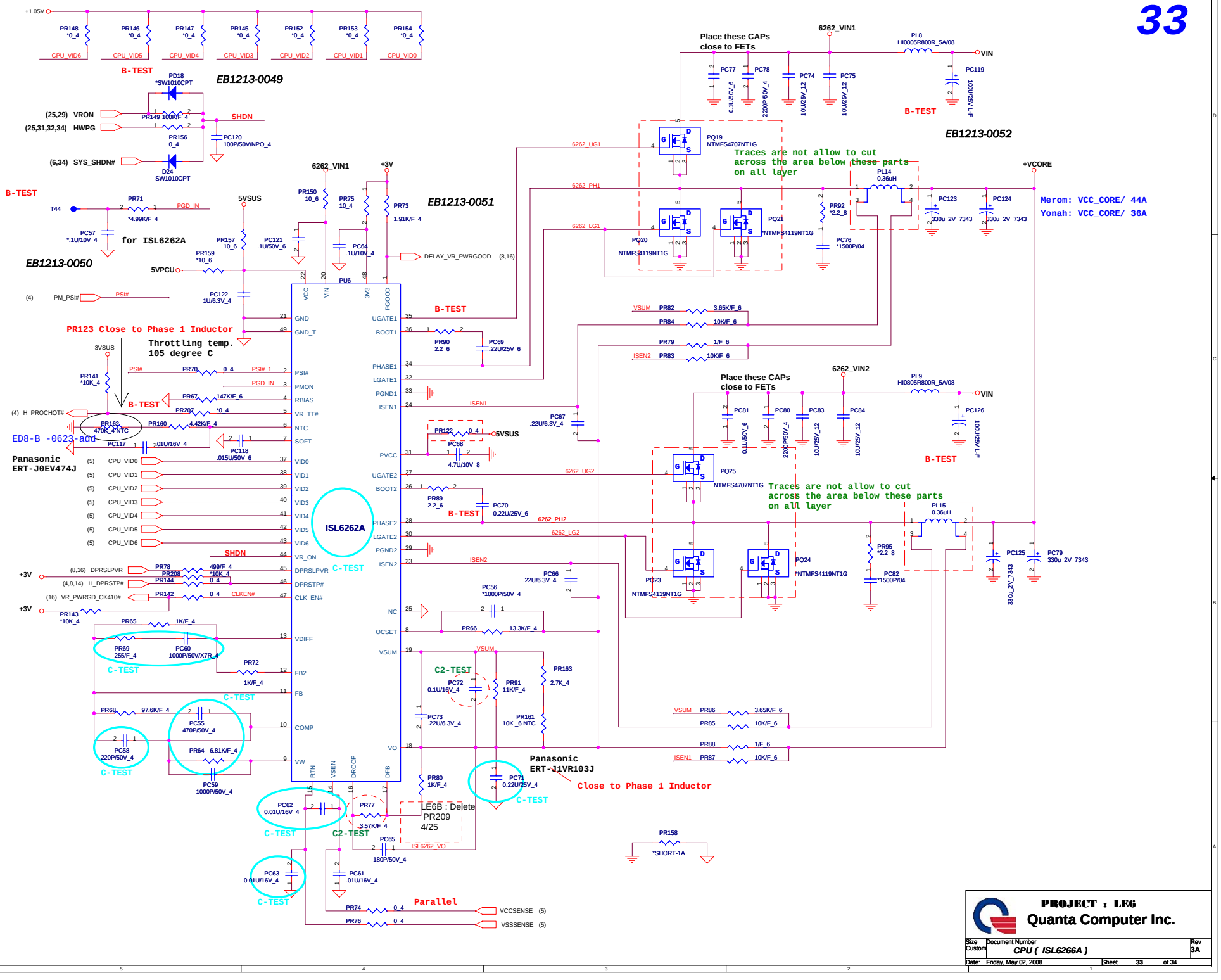

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Quanta Computer Inc.			
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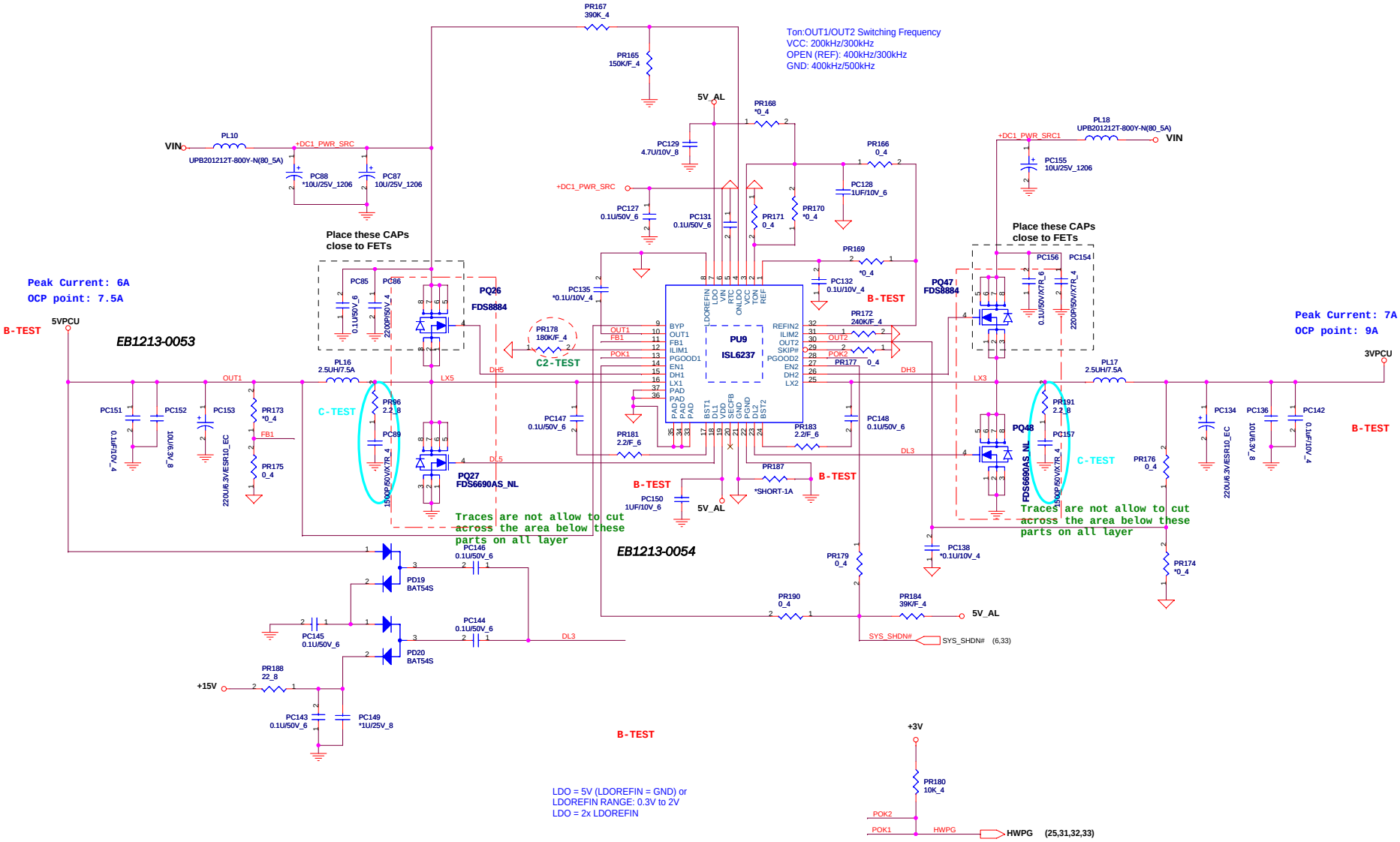
DC/DC 3VPCU/5VPCU/+15V



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Rev:	3A
Date: Friday, May 02, 2008	Sheet 34 of 34