KIWA7/A8

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:0.4

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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Title: **Cover Sheet**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

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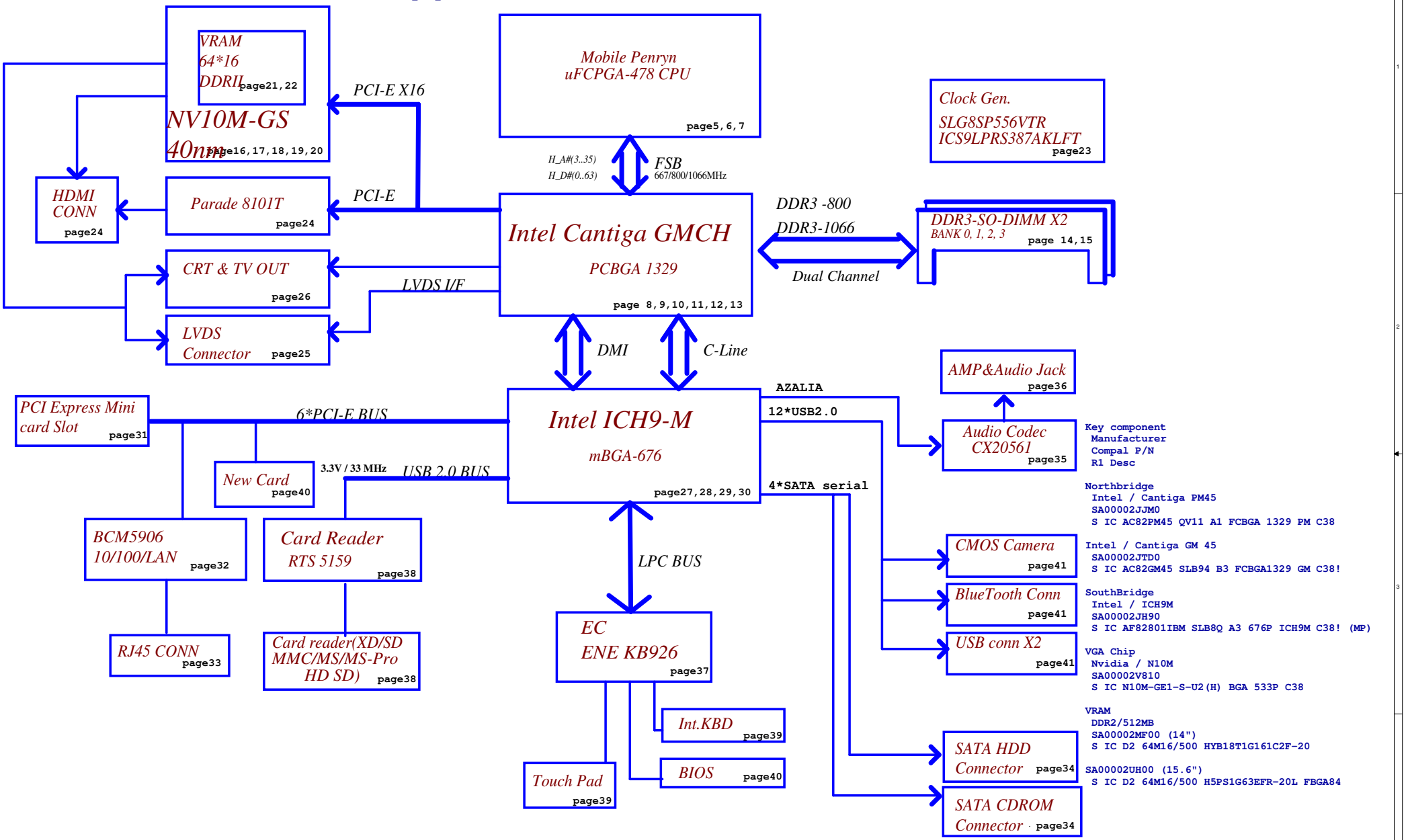
Compal confidential
File Name :

ZZZ
15W_PCB_LA5082P

POWER Board

CAP SENSE LEDs Board

USB board



Key component
Manufacturer
Compal P/N
R1 Desc

Northbridge
Intel / Cantiga PM45
SA00002JJM0
S IC AC82PM45 QV11 A1 FCBGA 1329 PM C38

Intel / Cantiga GM 45
SA00002JTD0
S IC AC82GM45 SLB94 B3 FCBGA1329 GM C38!

SouthBridge
Intel / ICH9M
SA00002JH90
S IC AF82801IBM SLB8Q A3 676P ICH9M C38! (MP)

VGA Chip
Nvidia / N10M
SA00002V810
S IC N10M-GE1-S-U2(H) BGA 533P C38

VRAM
DDR2/512MB
SA00002MF00 (14")
S IC D2 64M16/500 HYB18T1G161C2F-20

SA00002UH00 (15.6")
S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	V	X	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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Title: MB Notes List			
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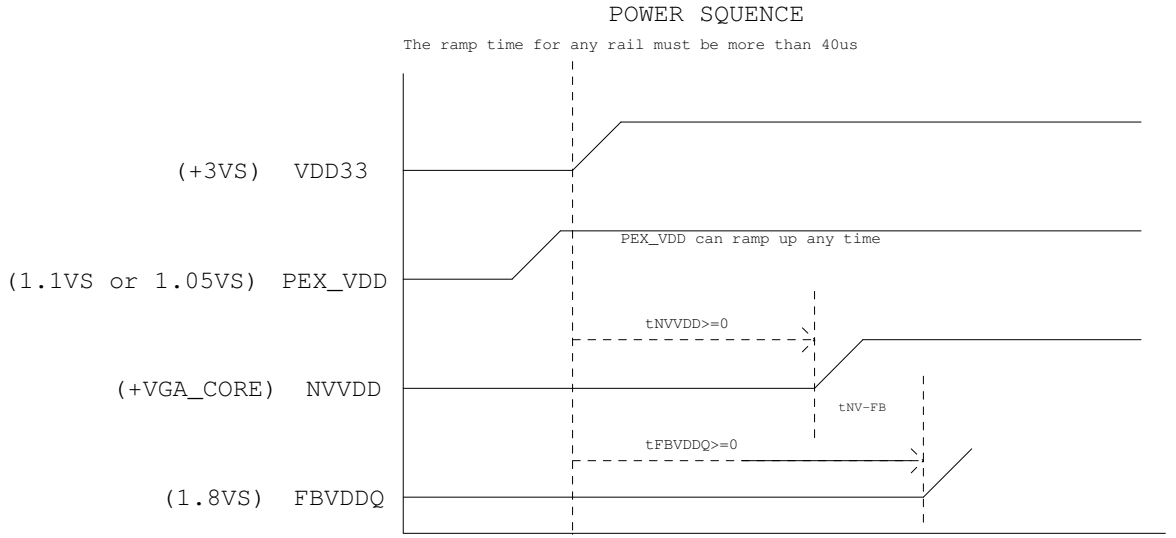
VGA and DDR2 Voltage Rails (N10M)

power plane / State				+3VS +VGA_CORE +1.1VS (for 55nm) +1.05VS (for 40nm) +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SQUENCE



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Title: VGA Notes List

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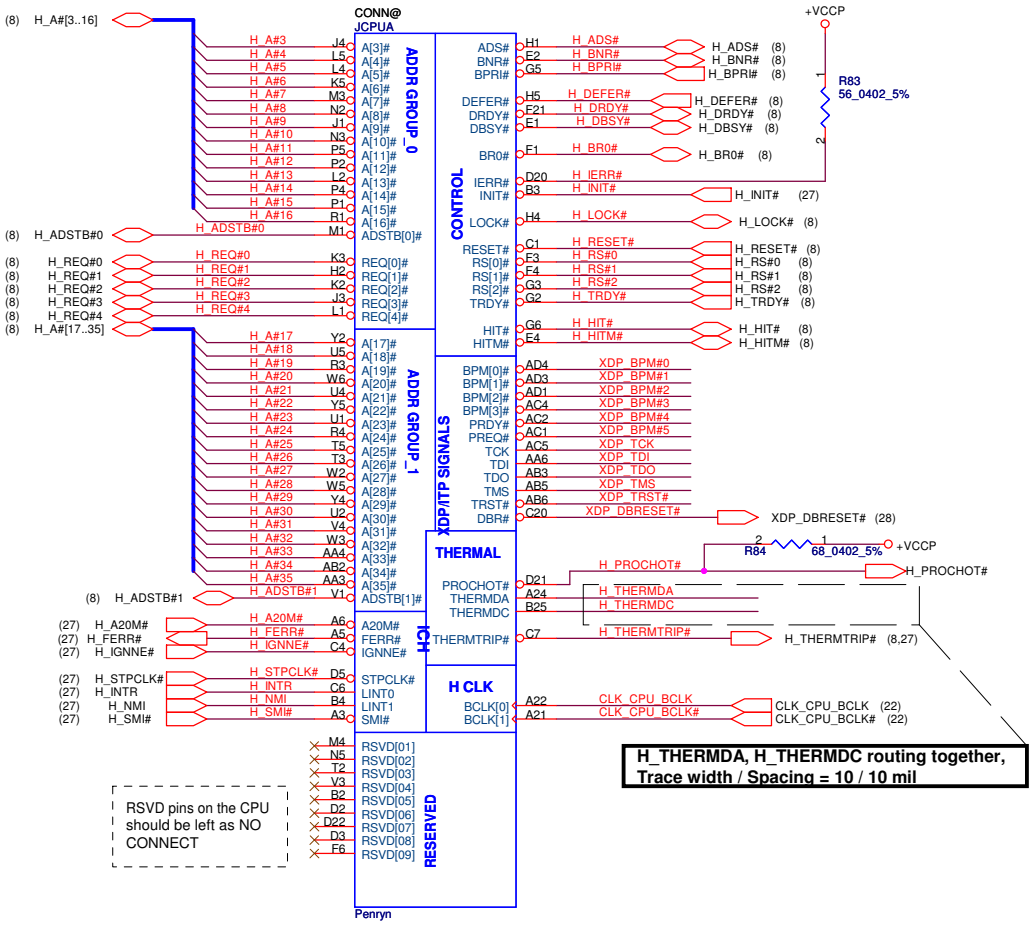
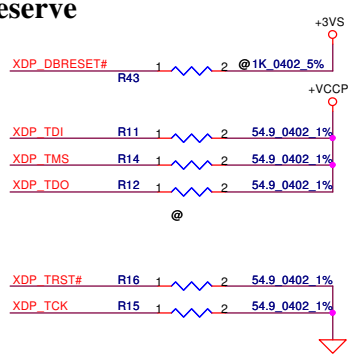
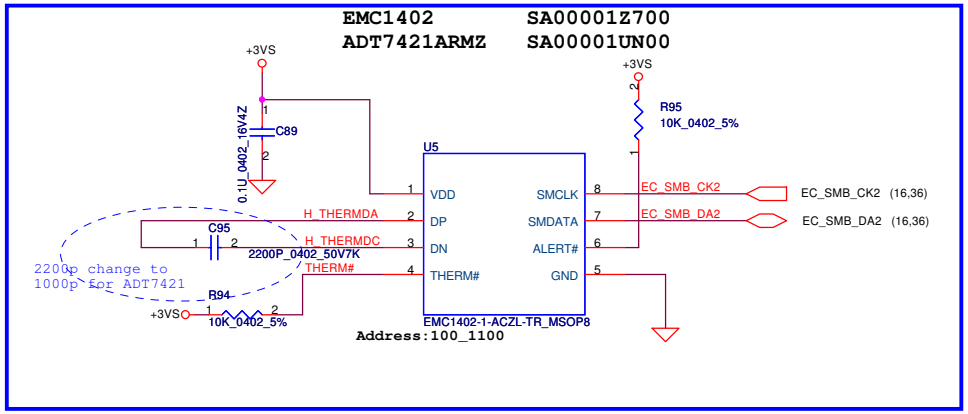
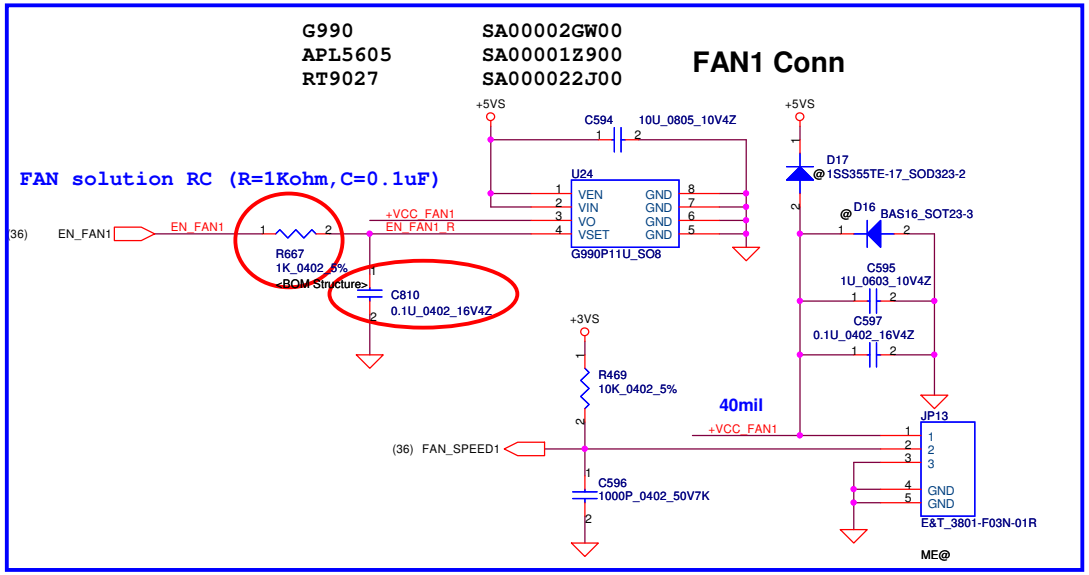


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

XDP Reserve







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Title: **Penryn (1/3)**

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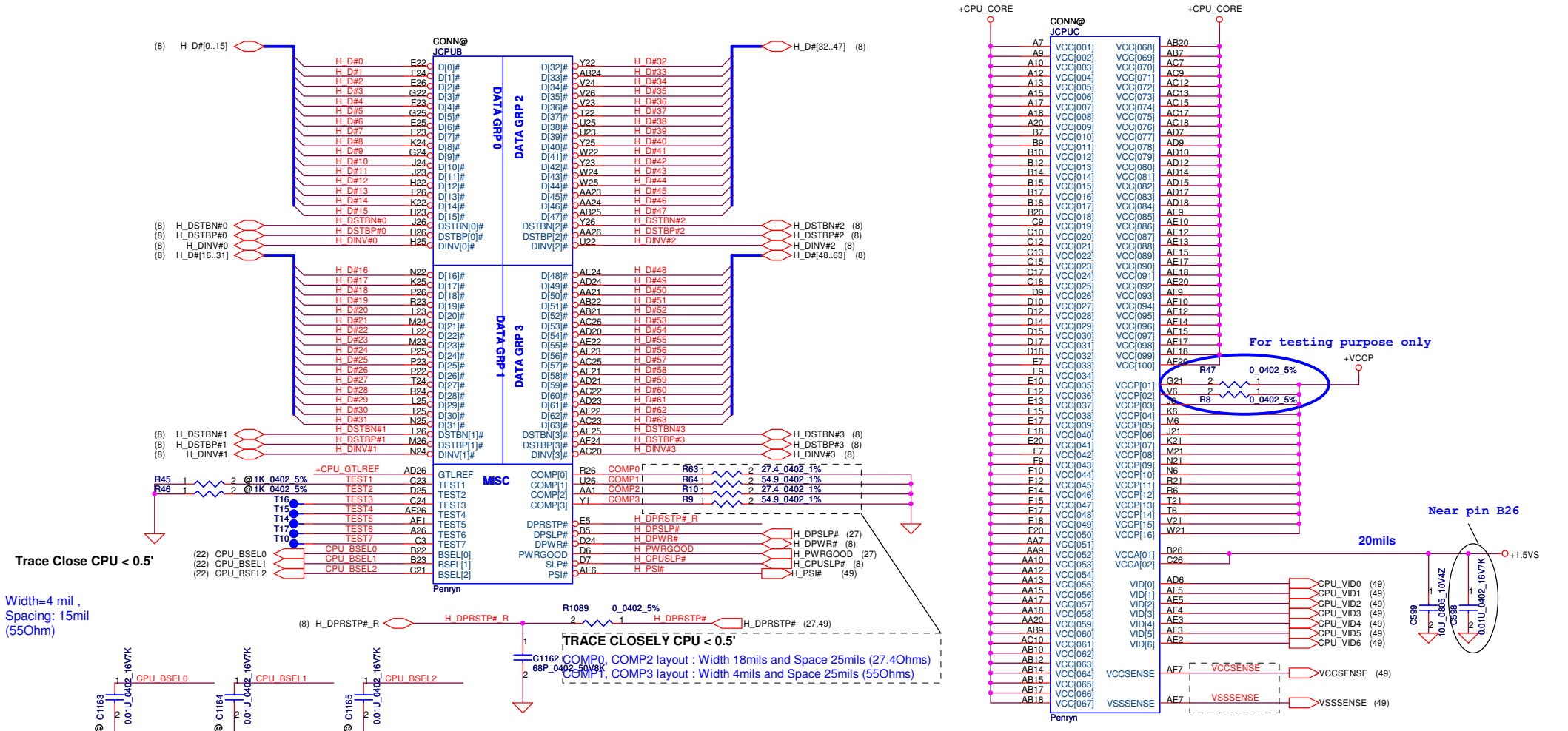

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

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Compal Electronics, Inc.			
Title: Penryn (2/3)			
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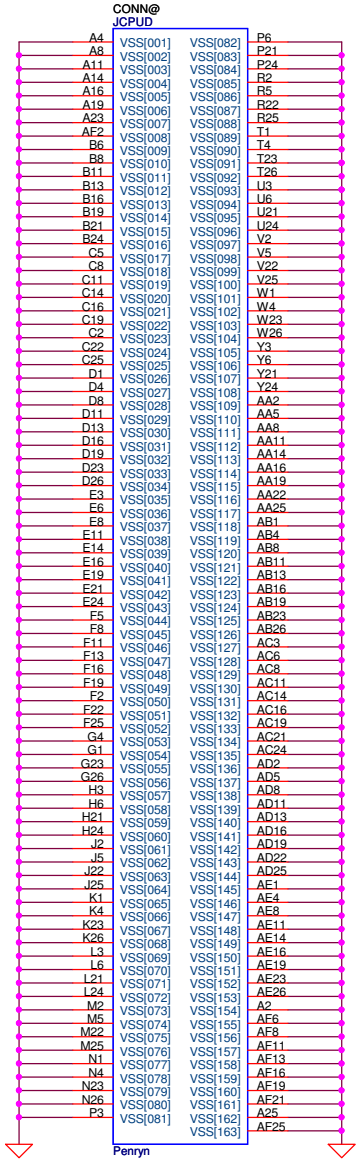
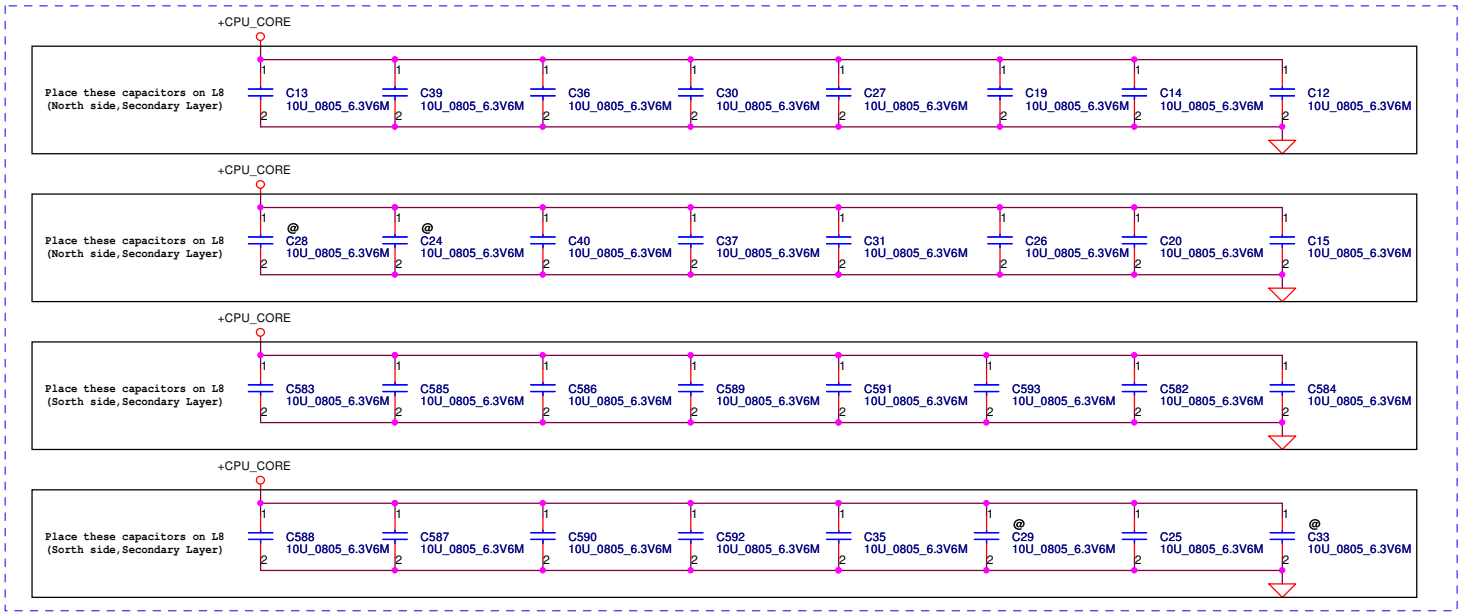
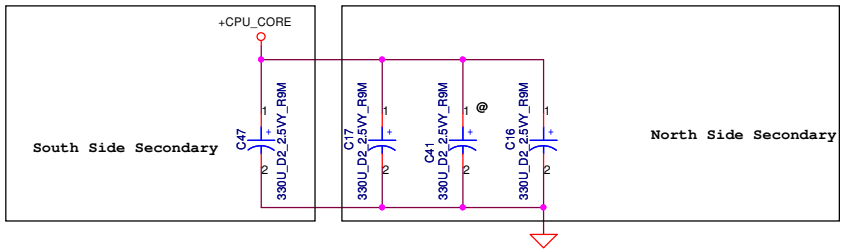
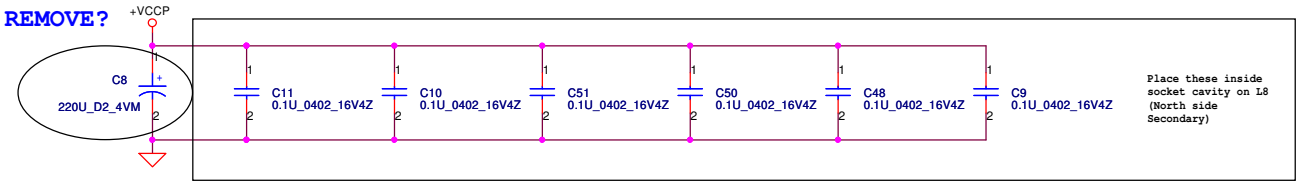




Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF



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Compal Electronics, Inc.			
Title: Penryn (3/3)			
Size: B	Document Number: KIWAX_LA-5082P		Rev: 0.4
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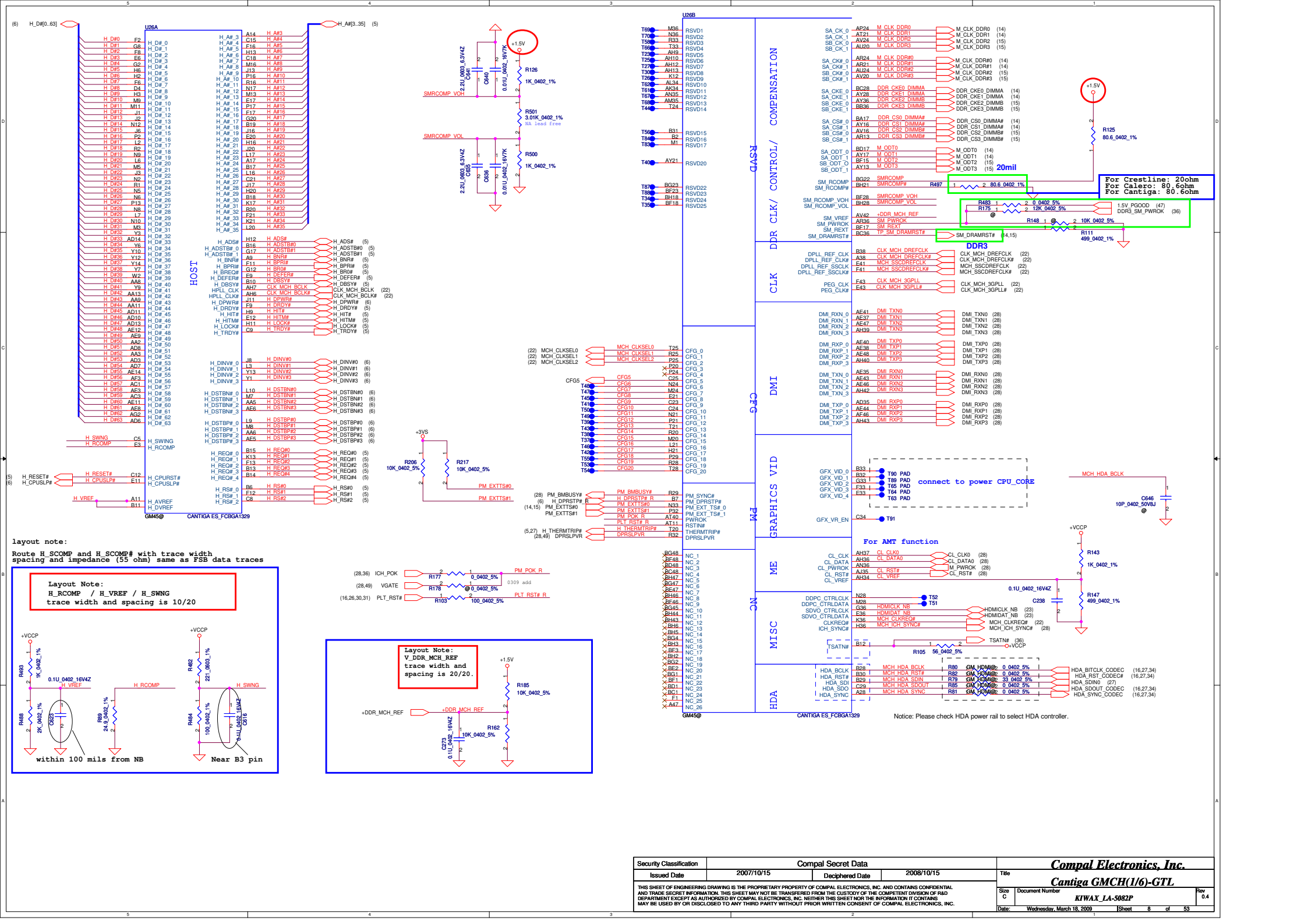

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Title	Compal Electronics, Inc.		
	Cantiga GMCH(1/6)-GTL		
Size C	Document Number KIWAX_LA-5082P		Rev 0.4
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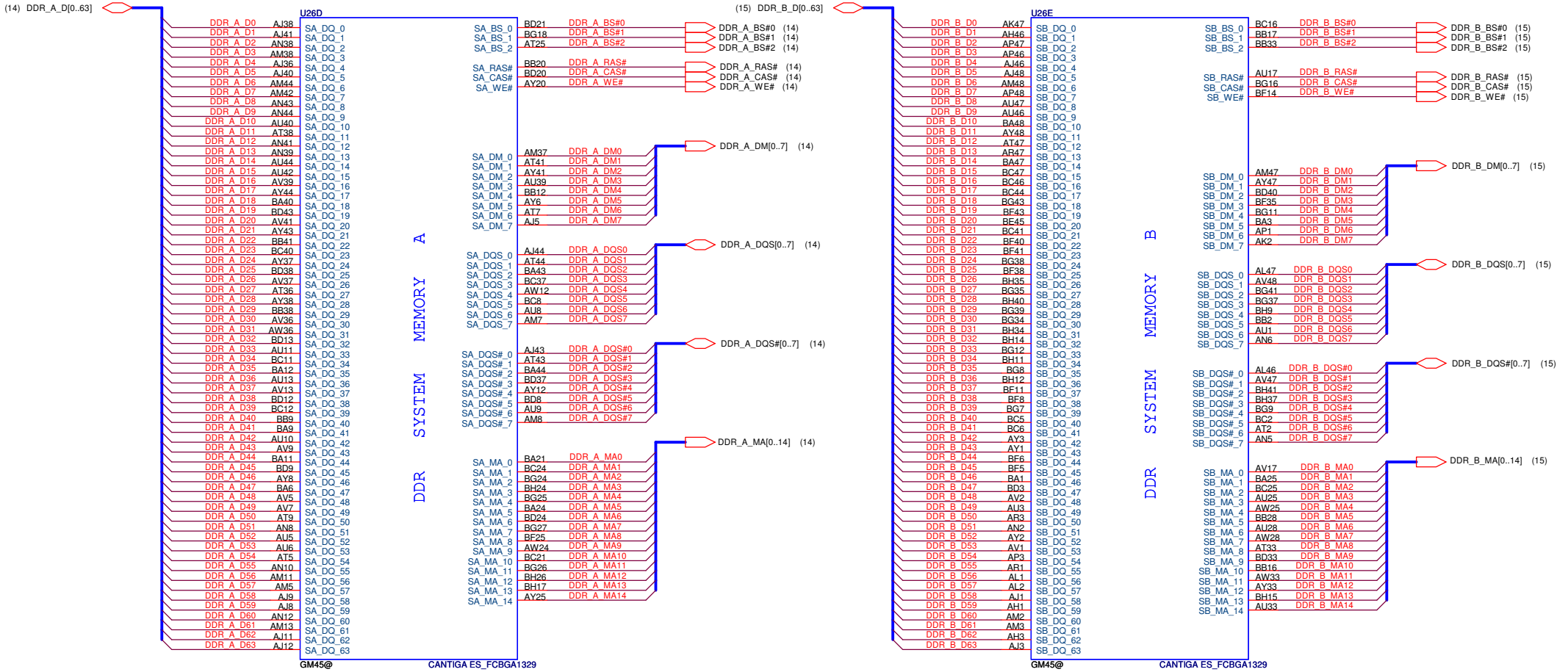

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Compal Electronics, Inc.

Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

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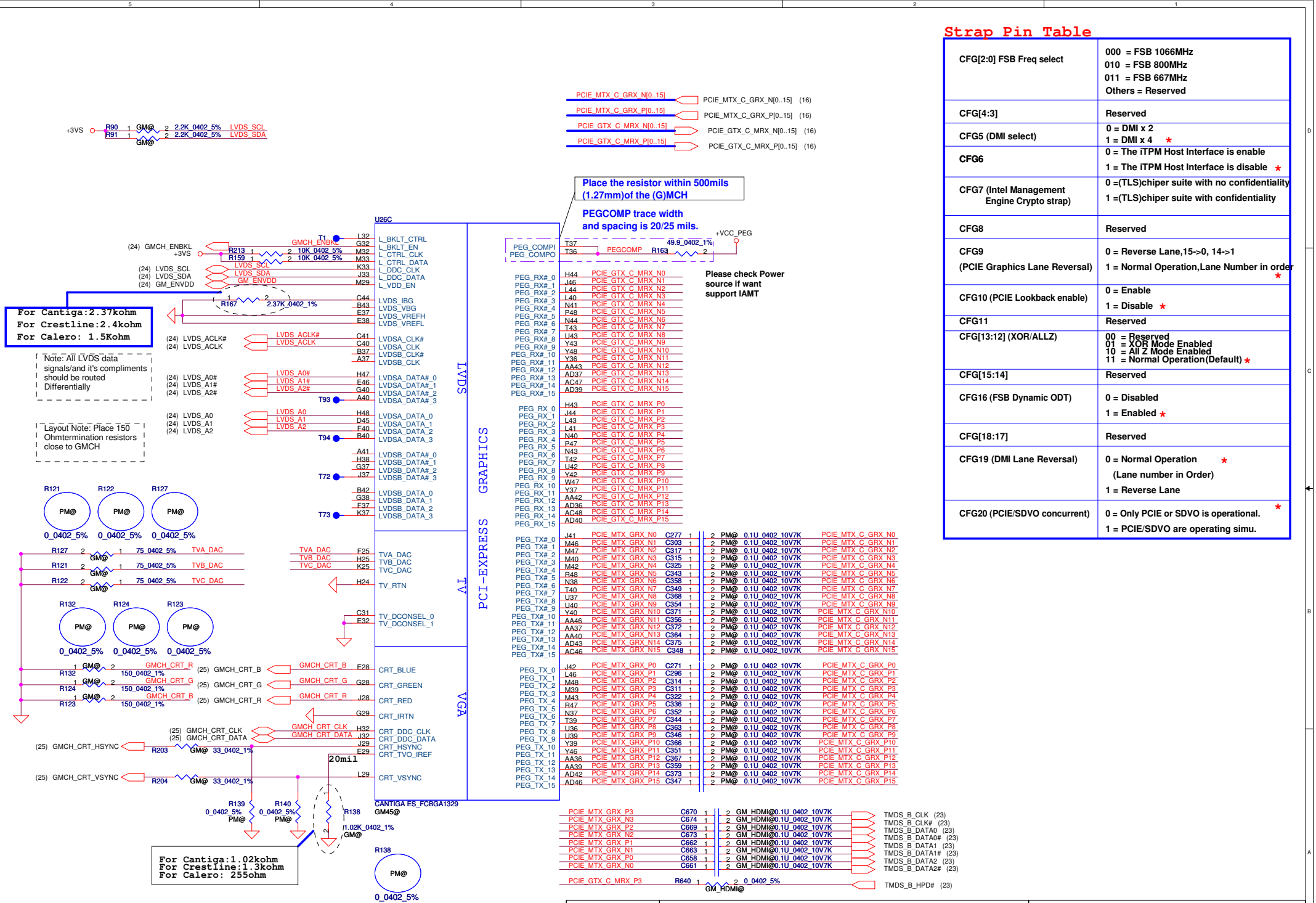

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga GMCH (3/6)-VGA/LVDS/TV**

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Custom	KIWAX_LA-5082P	0.4

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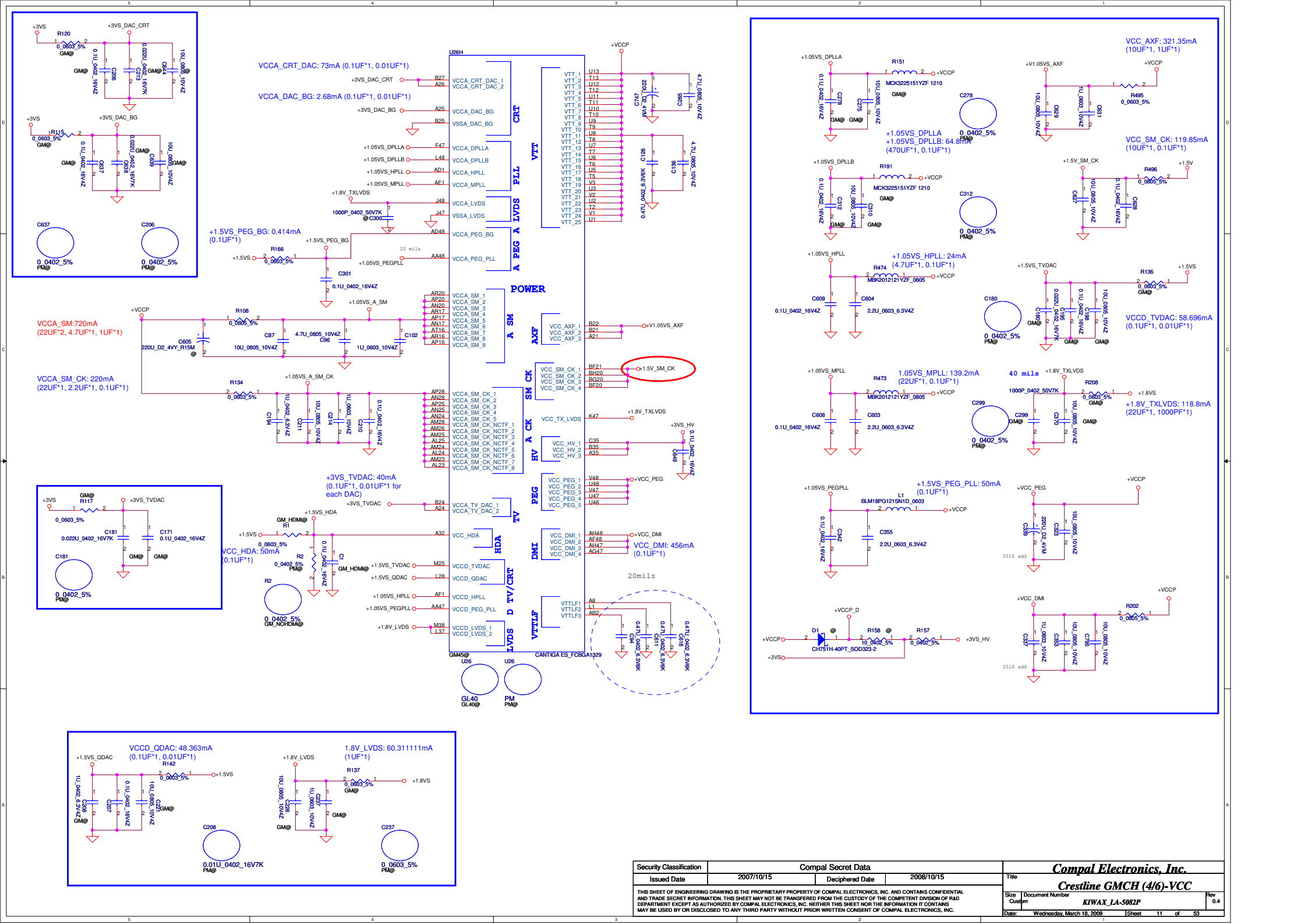
VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)
+1.5VS_PEG_BG: 0.414mA (0.1UF*1)
VCCA_SM:720mA (22UF*2, 4.7UF*1, 1UF*1)
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)
+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
VCC_HDA: 50mA (0.1UF*1)
VCC_DMI: 456mA (0.1UF*1)
VCC_AXF: 321.35mA (10UF*1, 1UF*1)
VCC_SM_CK: 119.85mA (10UF*1, 0.1UF*1)
+1.05VS_DPLLA
+1.05VS_DPLLB: 64.8mA (470UF*1, 0.1UF*1)
+1.05VS_HPLL: 24mA (4.7UF*1, 0.1UF*1)
VCCD_TVDAC: 58.696mA (0.1UF*1, 0.01UF*1)
1.05VS_MPLL: 139.2mA (22UF*1, 0.1UF*1)
+1.8V_TXLVDS: 118.8mA (22UF*1, 1000PF*1)
+1.5VS_PEG_PLL: 50mA (0.1UF*1)
VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)
1.8V_LVDS: 60.311111mA (1UF*1)
U26H
CRT
PLL
LVDS
A PEG
POWER
A SM
AXF
SM CK
A CK
HV
PEG
TV
HDA
DMI
D TV/CRT
VTTLF
LVDS
VTT
CANTIGA ES_FCBGA1329
20mils
40 mils
0316 add
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Compal Secret Data
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2007/10/15
Deciphered Date
2008/10/15
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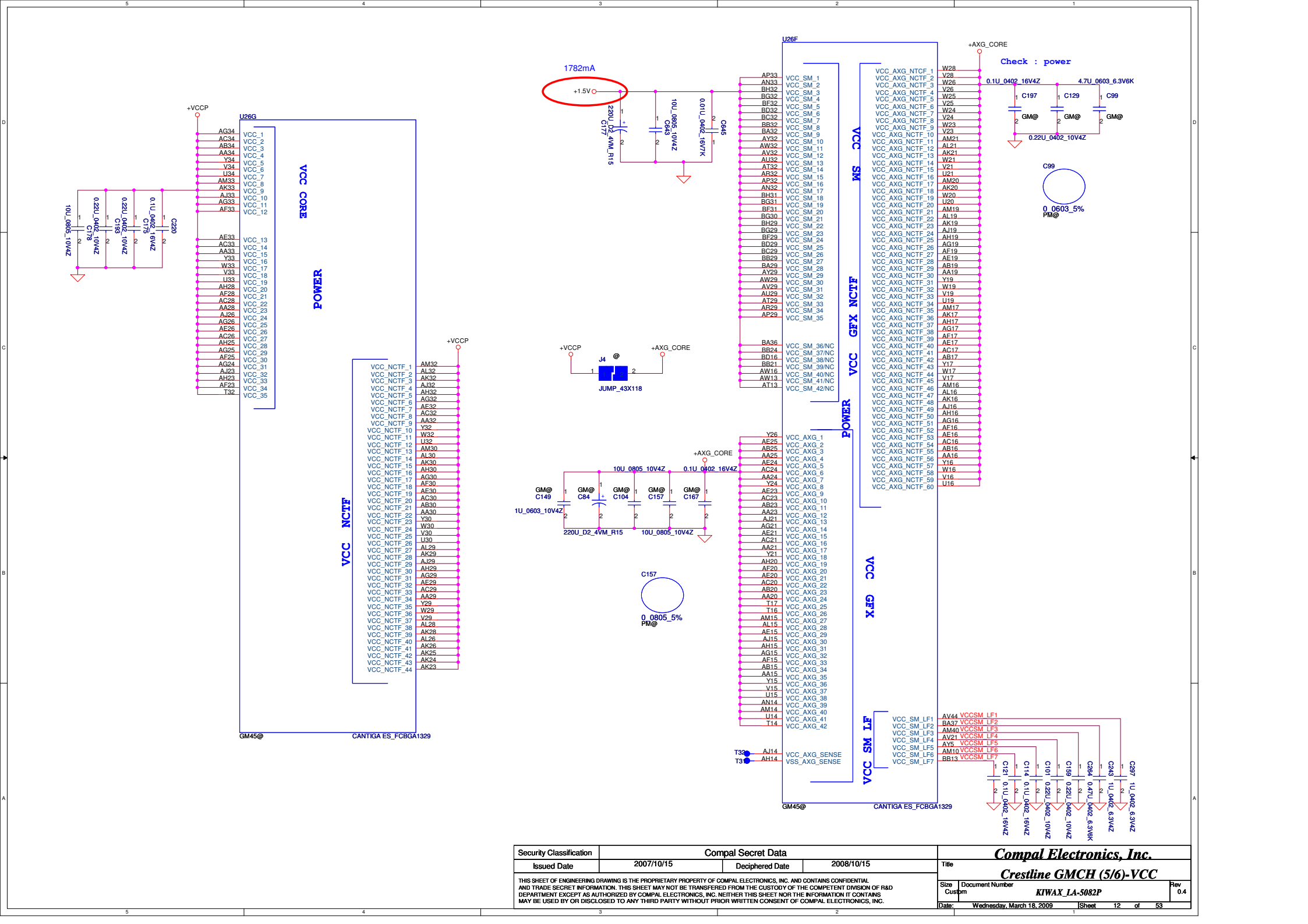

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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
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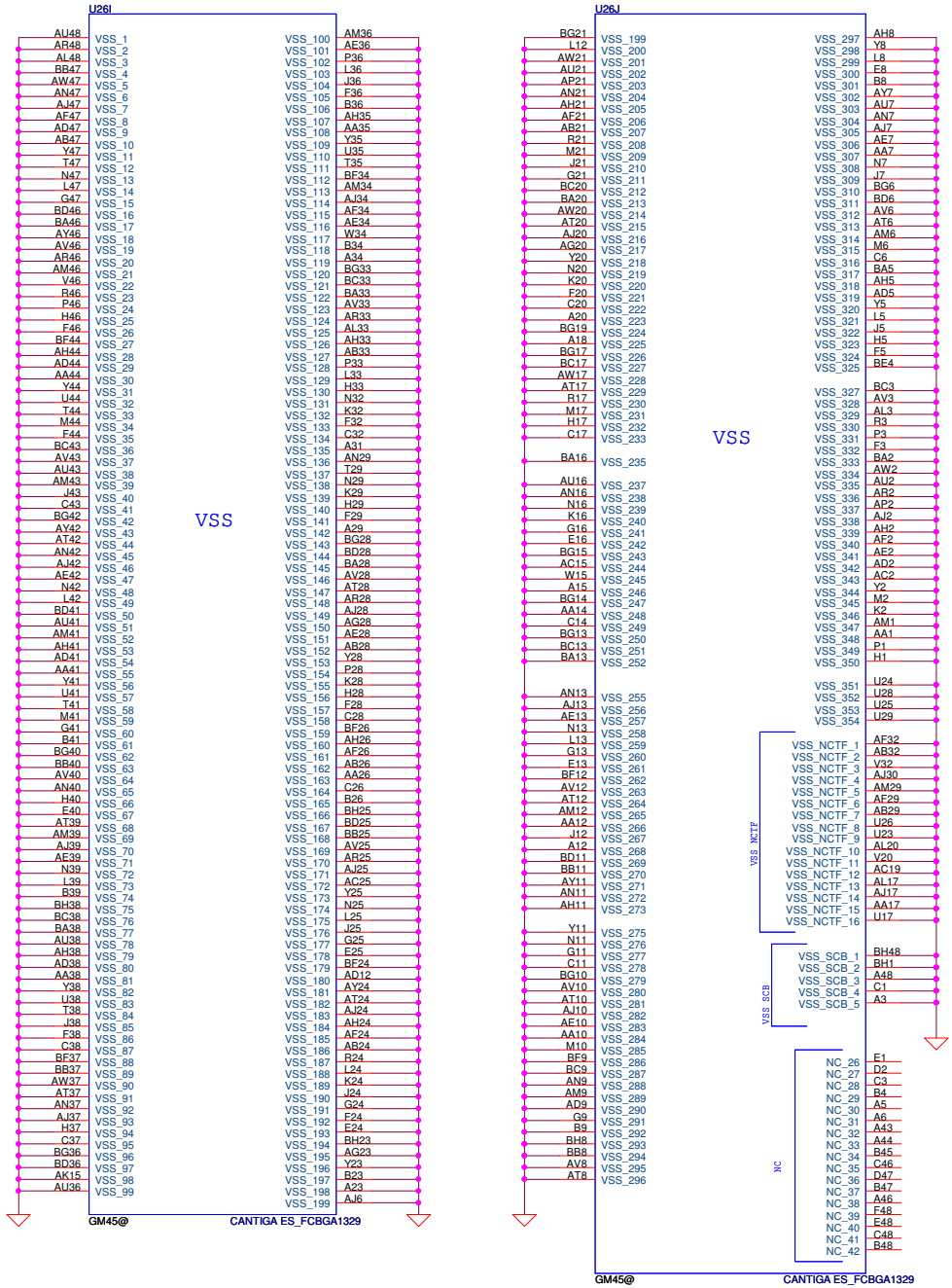

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Title: **Cantiga GMCH (6/6)-GND**

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(9) DDR_A_DQS#[0..7]
(9) DDR_A_D[0..63]
(9) DDR_A_DM[0..7]
(9) DDR_A_DQS[0..7]
(9) DDR_A_MA[0..14]

+1.5V
R625 100_0402_1%
+V_DDR3_DIMM_REF
R626 100_0402_1%
C755 0.1U_0402_16V4Z

Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C761 10U_0805_6.3V6M
C762 10U_0805_6.3V6M
C767 10U_0805_6.3V6M
C763 10U_0805_6.3V6M
C764 10U_0805_6.3V6M
C765 10U_0805_6.3V6M
C766 10U_0805_6.3V6M
C750 0.1U_0402_16V4Z
C752 0.1U_0402_16V4Z
C749 0.1U_0402_16V4Z
C753 0.1U_0402_16V4Z
C787 470U_D2_2.5VM_R15 @

<BOM Structure> <BOM Structure> <BOM Structure> <BOM Structure>

Layout Note:
Place near JP4.203 & JP4.204

+0.75VS
1U_0603_10V4Z C778
1U_0603_10V4Z C779
1U_0603_10V4Z C776
1U_0603_10V4Z C777
10U_0805_6.3V6M C762

+1.5V
+V_DDR3_DIMM_REF
JP17

		1	VREF_DQ	VSS1	2	
		3	VSS2	DQ4	4	DDR_A_D4
DDR_A_D0		5	DQ0	DQ5	6	DDR_A_D5
DDR_A_D1		7	DQ1	VSS3	8	
		9	VSS4	DQS#0	10	DDR_A_DQS#0
DDR_A_DM0		11	DM0	DQS0	12	DDR_A_DQS0
		13	VSS5	VSS6	14	
DDR_A_D2		15	DQ2	DQ6	16	DDR_A_D6
DDR_A_D3		17	DQ3	DQ7	18	DDR_A_D7
		19	VSS7	VSS8	20	
DDR_A_D8		21	DQ8	DQ12	22	DDR_A_D12
DDR_A_D9		23	DQ9	DQ13	24	DDR_A_D13
		25	VSS9	VSS10	26	
DDR_A_DQS#1		27	DQS#1	DM1	28	DDR_A_DM1
DDR_A_DQS1		29	DQS1	RESET#	30	SM_DRAMRST#
		31	VSS11	VSS12	32	
DDR_A_D10		33	DQ10	DQ14	34	DDR_A_D14
DDR_A_D11		35	DQ11	DQ15	36	DDR_A_D15
		37	VSS13	VSS14	38	
DDR_A_D16		39	DQ16	DQ20	40	DDR_A_D20
DDR_A_D17		41	DQ17	DQ21	42	DDR_A_D21
		43	VSS15	VSS16	44	
DDR_A_DQS#2		45	DQS#2	DM2	46	DDR_A_DM2
DDR_A_DQS2		47	DQS2	VSS17	48	
		49	VSS18	DQ22	50	DDR_A_D22
DDR_A_D18		51	DQ18	DQ23	52	DDR_A_D23
DDR_A_D19		53	DQ19	VSS19	54	
		55	VSS20	DQ28	56	DDR_A_D28
DDR_A_D24		57	DQ24	DQ29	58	DDR_A_D29
DDR_A_D25		59	DQ25	VSS21	60	
		61	VSS22	DQS#3	62	DDR_A_DQS#3
DDR_A_DM3		63	DM3	DQS3	64	DDR_A_DQS3
		65	VSS23	VSS24	66	
DDR_A_D26		67	DQ26	DQ30	68	DDR_A_D30
DDR_A_D27		69	DQ27	DQ31	70	DDR_A_D31
		71	VSS25	VSS26	72	
(8) DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	73	CKE0	CKE1	74	DDR_CKE1_DIMMA
		75	VDD1	VDD2	76	
(9) DDR_A_BS#2	DDR_A_BS2	77	NC1	A15	78	
		79	BA2	A14	80	DDR_A_MA14
		81	VDD3	VDD4	82	
DDR_A_MA12		83	A12/BC#	A11	84	DDR_A_MA11
DDR_A_MA9		85	A9	A7	86	DDR_A_MA7
		87	VDD5	VDD6	88	
DDR_A_MA8		89	A8	A6	90	DDR_A_MA6
DDR_A_MA5		91	A5	A4	92	DDR_A_MA4
		93	VDD7	VDD8	94	
DDR_A_MA3		95	A3	A2	96	DDR_A_MA2
DDR_A_MA1		97	A1	A0	98	DDR_A_MA0
		99	VDD9	VDD10	100	
(8) M_CLK_DDR0	M_CLK_DDR0	101	CK0	CK1	102	M_CLK_DDR1 (8)
(8) M_CLK_DDR#0	M_CLK_DDR#0	103	CK0#	CK1#	104	M_CLK_DDR#1 (8)
		105	VDD11	VDD12	106	
DDR_A_MA10		107	A10/AP	BA1	108	DDR_A_BS1
(9) DDR_A_BS#0	DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS#
		111	VDD13	VDD14	112	
DDR_A_WE#		113	WE#	S0#	114	DDR_CS0_DIMMA#
(9) DDR_A_CAS#	DDR_A_CAS#	115	CAS#	ODT0	116	M_ODT0 (8)
		117	VDD15	VDD16	118	
DDR_A_MA13		119	A13	ODT1	120	M_ODT1 (8)
(8) DDR_CS1_DIMMA#	DDR_CS1_DIMMA#	121	S1#	NC2	122	
		123	VDD17	VDD18	124	
		125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA
		127	VSS27	VSS28	128	
DDR_A_D32		129	DQ32	DQ36	130	DDR_A_D36
DDR_A_D33		131	DQ33	DQ37	132	DDR_A_D37
		133	VSS29	VSS30	134	
DDR_A_DQS#4		135	DQS#4	DM4	136	DDR_A_DM4
DDR_A_DQS4		137	DQS4	VSS31	138	
		139	VSS32	DQ38	140	DDR_A_D38
DDR_A_D34		141	DQ34	DQ39	142	DDR_A_D39
DDR_A_D35		143	DQ35	VSS33	144	
		145	VSS34	DQ44	146	DDR_A_D44
DDR_A_D40		147	DQ40	DQ45	148	DDR_A_D45
DDR_A_D41		149	DQ41	VSS35	150	
		151	VSS36	DQS#5	152	DDR_A_DQS#5
DDR_A_DM5		153	DM5	DQS5	154	DDR_A_DQS5
		155	VSS37	VSS38	156	
DDR_A_D42		157	DQ42	DQ46	158	DDR_A_D46
DDR_A_D43		159	DQ43	DQ47	160	DDR_A_D47
		161	VSS39	VSS40	162	
DDR_A_D48		163	DQ48	DQ52	164	DDR_A_D52
DDR_A_D49		165	DQ49	DQ53	166	DDR_A_D53
		167	VSS41	VSS42	168	
DDR_A_DQS#6		169	DQS#6	DM6	170	DDR_A_DM6
DDR_A_DQS6		171	DQS6	VSS43	172	
		173	VSS44	DQ54	174	DDR_A_D54
DDR_A_D50		175	DQ50	DQ55	176	DDR_A_D55
DDR_A_D51		177	DQ51	VSS45	178	
		179	VSS46	DQ60	180	DDR_A_D60
DDR_A_D56		181	DQ56	DQ61	182	DDR_A_D61
DDR_A_D57		183	DQ57	VSS47	184	
		185	VSS48	DQS#7	186	DDR_A_DQS#7
DDR_A_DM7		187	DM7	DQS7	188	DDR_A_DQS7
		189	VSS49	VSS50	190	
DDR_A_D58		191	DQ58	DQ62	192	DDR_A_D62
DDR_A_D59		193	DQ59	DQ63	194	DDR_A_D63
		195	VSS51	VSS52	196	
		197	SA0	EVENT#	198	PM_EXTTS#0
		199	VDDSPD	SDA	200	CLK_SMBDATA
		201	SA1	SCL	202	CLK_SMBCLK
		203	VTT1	VTT2	204	+0.75VS
		205	G1	G2	206	

FOX_AS0A626-U2RN-7F
ME@

R627 10K_0402_5%
+3VS
C784 2.2U_0603_6.3V4Z
C754 0.1U_0402_16V4Z
R628 10K_0402_5%

R623 0_0402_5%
+V_DDR3_DIMM_REF
C785 2.2U_0603_6.3V4Z
C751 0.1U_0402_16V4Z

DDR_CKE1_DIMMA (8)
DDR_A_BS#1 (9)
DDR_A_RAS# (9)
DDR_CS0_DIMMA# (8)
M_ODT1 (8)
SM_DRAMRST# (8,15)
PM_EXTTS#0 (8,15)
CLK_SMBDATA (15,22)
CLK_SMBCLK (15,22)

DDR3 SO-DIMM A REVERSE

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 Sheet 14 of 53

(9) DDR_B_DQS#[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_DM[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_MA[0..14]

Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C771 10U_0805_6.3V6M
C775 10U_0805_6.3V6M
C772 10U_0805_6.3V6M
C769 10U_0805_6.3V6M
C774 10U_0805_6.3V6M
C773 10U_0805_6.3V6M
C768 10U_0805_6.3V6M
C756 0.1U_0402_16V4Z
C757 0.1U_0402_16V4Z
C760 0.1U_0402_16V4Z
C759 0.1U_0402_16V4Z
C788 470U_D2_2.5VM_R15 @

<BOM Structure> <BOM Structure> <BOM Structure> <BOM Structure>

Layout Note:
Place near JP5.203 & JP5.204

+0.75VS
1U_0603_10V4Z C780
1U_0603_10V4Z C781
1U_0603_10V4Z C783
1U_0603_10V4Z C782
10U_0805_6.3V6M C770

+1.5V
+V_DDR3_DIMM_REF

JP16

		VREF_DQ	1	VSS1	
		VSS2	3	DQ4	DDR_B_D4
DDR_B_D0		DQ0	5	DQ5	DDR_B_D5
DDR_B_D1		DQ1	7	VSS3	
		VSS4	9	DQS#0	DDR_B_DQS#0
DDR_B_DM0		DM0	11	DQS0	DDR_B_DQS0
		VSS5	13	VSS6	
DDR_B_D2		DQ2	15	DQ6	DDR_B_D6
DDR_B_D3		DQ3	17	DQ7	DDR_B_D7
		VSS7	19	VSS8	
DDR_B_D8		DQ8	21	DQ12	DDR_B_D12
DDR_B_D9		DQ9	23	DQ13	DDR_B_D13
		VSS9	25	VSS10	
DDR_B_DQS#1		DQS#1	27	DM1	DDR_B_DM1
DDR_B_DQS1		DQS1	29	RESET#	SM_DRAMRST# (8,14)
		VSS11	31	VSS12	
DDR_B_D10		DQ10	33	DQ14	DDR_B_D14
DDR_B_D11		DQ11	35	DQ15	DDR_B_D15
		VSS13	37	VSS14	
DDR_B_D16		DQ16	39	DQ20	DDR_B_D20
DDR_B_D17		DQ17	41	DQ21	DDR_B_D21
		VSS15	43	VSS16	
DDR_B_DQS#2		DQS#2	45	DM2	DDR_B_DM2
DDR_B_DQS2		DQS2	47	VSS17	
		VSS18	49	DQ22	DDR_B_D22
DDR_B_D18		DQ18	51	DQ23	DDR_B_D23
DDR_B_D19		DQ19	53	VSS19	
		VSS20	55	DQ28	DDR_B_D28
DDR_B_D24		DQ24	57	DQ29	DDR_B_D29
DDR_B_D25		DQ25	59	VSS21	
		VSS22	61	DQS#3	DDR_B_DQS#3
DDR_B_DM3		DM3	63	DQS3	DDR_B_DQS3
		VSS23	65	VSS24	
DDR_B_D26		DQ26	67	DQ30	DDR_B_D30
DDR_B_D27		DQ27	69	DQ31	DDR_B_D31
		VSS25	71	VSS26	
(8) DDR_CKE2_DIMMB		CKE0	73	CKE1	DDR_CKE3_DIMMB (8)
		VDD1	75	VDD2	
(9) DDR_B_BS#2		NC1	77	A15	
		BA2	79	A14	DDR_B_MA14
DDR_B_MA12		VDD3	81	VDD4	
DDR_B_MA9		A12/BC#	83	A11	DDR_B_MA11
		A9	85	A7	DDR_B_MA7
DDR_B_MA8		VDD5	87	VDD6	
DDR_B_MA5		A8	89	A6	DDR_B_MA6
		A5	91	A4	DDR_B_MA4
DDR_B_MA3		VDD7	93	VDD8	
DDR_B_MA1		A3	95	A2	DDR_B_MA2
		A1	97	A0	DDR_B_MA0
(8) M_CLK_DDR2	M_CLK_DDR2	VDD9	99	VDD10	
(8) M_CLK_DDR#2	M_CLK_DDR#2	CK0	101	CK1	M_CLK_DDR3
		CK0#	103	CK1#	M_CLK_DDR#3 (8)
DDR_B_MA10		VDD11	105	VDD12	M_CLK_DDR#3 (8)
DDR_B_BS0		A10/AP	107	BA1	DDR_B_BS1
(9) DDR_B_BS#0		BA0	109	RAS#	DDR_B_RAS#
		VDD13	111	VDD14	DDR_B_BS#1 (9)
(9) DDR_B_WE#	DDR_B_WE#	WE#	113	S0#	DDR_B_RAS# (9)
(9) DDR_B_CAS#	DDR_B_CAS#	CAS#	115	ODT0	DDR_CS2_DIMMB#
		VDD15	117	VDD16	M_ODT2
DDR_B_MA13		A13	119	ODT1	M_ODT2 (8)
(8) DDR_CS3_DIMMB#	DDR_CS3_DIMMB#	S1#	121	NC2	M_ODT3
		VDD17	123	VDD18	M_ODT3 (8)
		NCTEST	125	VREF_CA	DDR_VREF_CA_DIMMB
		VSS27	127	VSS28	
DDR_B_D32		DQ32	129	DQ36	DDR_B_D36
DDR_B_D33		DQ33	131	DQ37	DDR_B_D37
		VSS29	133	VSS30	
DDR_B_DQS#4		DQS#4	135	DM4	DDR_B_DM4
DDR_B_DQS4		DQS4	137	VSS31	
		VSS32	139	DQ38	DDR_B_D38
DDR_B_D34		DQ34	141	DQ39	DDR_B_D39
DDR_B_D35		DQ35	143	VSS33	
		VSS34	145	DQ44	DDR_B_D44
DDR_B_D40		DQ40	147	DQ45	DDR_B_D45
DDR_B_D41		DQ41	149	VSS35	
		VSS36	151	DQS#5	DDR_B_DQS#5
DDR_B_DM5		DM5	153	DQS5	DDR_B_DQS5
		VSS37	155	VSS38	
DDR_B_D42		DQ42	157	DQ46	DDR_B_D46
DDR_B_D43		DQ43	159	DQ47	DDR_B_D47
		VSS39	161	VSS40	
DDR_B_D48		DQ48	163	DQ52	DDR_B_D52
DDR_B_D49		DQ49	165	DQ53	DDR_B_D53
		VSS41	167	VSS42	
DDR_B_DQS#6		DQS#6	169	DM6	DDR_B_DM6
DDR_B_DQS6		DQS6	171	VSS43	
		VSS44	173	DQ54	DDR_B_D54
DDR_B_D50		DQ50	175	DQ55	DDR_B_D55
DDR_B_D51		DQ51	177	VSS45	
		VSS46	179	DQ60	DDR_B_D60
DDR_B_D56		DQ56	181	DQ61	DDR_B_D61
DDR_B_D57		DQ57	183	VSS47	
		VSS48	185	DQS#7	DDR_B_DQS#7
DDR_B_DM7		DM7	187	DQS7	DDR_B_DQS7
		VSS49	189	VSS50	
DDR_B_D58		DQ58	191	DQ62	DDR_B_D62
DDR_B_D59		DQ59	193	DQ63	DDR_B_D63
		VSS51	195	VSS52	
		SA0	197	EVENT#	PM_EXTTS#0 (8,14)
		VDDSPD	199	SDA	CLK_SMBDATA
		SA1	201	SCL	CLK_SMBDATA (14,22)
		VTT1	203	VTT2	CLK_SMBCLK
			205		CLK_SMBCLK (14,22)
		G1		G2	+0.75VS
					206

FOX_AS0A626-UARN-7F
ME@

R624 1 2 0_0402_5%
+V_DDR3_DIMM_REF
C798 2.2U_0603_6.3V4Z
C758 0.1U_0402_16V4Z

+3VS
R630 1 2 10K_0402_5%
R629 1 2 10K_0402_5%
C761 0.1U_0402_16V4Z

same with intel DDR3 CRB connection

DDR3 SO-DIMM B
REVERSE

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT2			
Size	Document Number: KIWAX_LA-5082P		Rev: 0.4
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GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10,12
1	1	1.20V	0
0	1	1.09V	8

	Device ID
NB9M-GS	0x06E9
N10M-GE1-S (55nm)	0x6EC

For N10M 40NM

U59A

Part 1 of 5

PCI EXPRESS

GPIO

DACA

DACB

DACC

I2C

TEST

CLK

HDA

NB9M-GS_BGA533

PM@

CRT OUT

EMI

External Spread Spectrum

If External Spread Spectrum not stuff than stuff resistor

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10M PCIE,LVDS,GPIO,CLK

Size	Document Number	Rev
B	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 16 of 53

FBAD[0..63] → FBAD[0..63] (20,21)
FBAA[0..13] → FBAA[0..13] (20,21)
FBBA[2..5] → FBBA[2..5] (21)
FBADQM#[0..7] → FBADQM#[0..7] (20,21)
FBADQS[0..7] → FBADQS[0..7] (20,21)
FBADQS#[0..7] → FBADQS#[0..7] (20,21)

CKEcs0ODT

R131 & R132 Pull-down for initialization
CKE & RESET/ODT

For N10M

U59B — MEMORY INTERFACE — Part 2 of 5 — NB9M-GS_BGA533 — PM@

U59C — LVDS/TMDS — Part 3 of 5 — NB9M-GS_BGA533 — PM@

R118 10K_0402_5% 40NM@ — FBB_CKE (21)
R119 10K_0402_5% PM@ — FBA_CKE (20,21)

R130 10K_0402_5% 40NM@
R129 10K_0402_5%
R128 10K_0402_5%
R127 10K_0402_5% 55NM@
40NM@

R985 @1K_0402_5%
R986 @1K_0402_5%
R987 1K_0402_5%
PM@

R988 1.3K_0402_1% @
R991 1.3K_0402_1% @
1.27V~0.9V
C970 0.01U_0402_16V7K @

R992 60.4_0402_1% PM@

R974 40NM@ 0_0402_5%
R975 0_0402_5% 40NM@
R976 0_0402_5% @
R978 0_0402_5% 40NM@

R982 40.2K_0402_1% PM@
R983 40.2K_0402_1% PM@

PAD T164
PAD T165
PAD T167

for GT21x request

R989 4.7K_0402_5% 40NM_HDMI@
R993 4.7K_0402_5% 40NM_HDMI@
Q42A 2N7002DW-T/R7_SOT363-6 40NM_HDMI@
Q42B 2N7002DW-T/R7_SOT363-6 40NM_HDMI@

5V PULL UP IN CONNECTER SIDE

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.
Title: N10M Memory
Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 0.4
Date: Wednesday, March 18, 2009 | Sheet 17 of 53

FOR N10M 40NM , 1.1VS needs to be changed to 1.05VS

+VGA_CORE
13.56A
NEAR BALL
0.1U_0402_16V4Z
0.1U_0402_16V4Z
0.1U_0402_16V4Z
220U_20_4VM_R15M
C978 C979 C980 C981 C982 C983
PM@
0.1U_0402_16V4Z
0.1U_0402_16V4Z
0.1U_0402_16V4Z
0.47U_0402_6.3V6K
0.47U_0402_6.3V6K
C990 C991 C992 C993 C994 C995
PM@
0.47U_0402_6.3V6K
0.47U_0402_6.3V6K
0.47U_0402_6.3V6K
0.47U_0402_6.3V6K

4.7U 6.3V K X5R 0603
C1001 C1002
PM@
NEAR BGA
4.7U 6.3V K X5R 0603

+3VS
NEAR BGA
80mA
0.1U_0402_16V4Z
NEAR BALL
C1011 C1012 C1013
PM@
1U_0603_10V4Z
0.1U_0402_16V4Z

U59D
Part 4 of 5
POWER
NB9M-GS_BGA533
PM@

VDD: J9 J10 J12 J13 L9 M9 M11 M17 N9 N11 N12 N13 N14 N15 N16 N17 N19 P11 P12 P13 P14 P15 P16 P17 R9 R11 R12 R13 R14 R15 R16 R17 T9 T11 T17 U9 U19 W9 W10 W12 W13 W18 W19 VDD
VDD33: A12 B12 C12 D12 E12 F12 VDD33

FBVDDQ: A13 B13 C13 D13 D14 E13 F13 F14 F15 F16 F17 F19 F22 H23 H26 J15 J16 J18 J19 L19 L23 L26 M19 N22 U22 Y22 FBVDDQ
PEX_IOVDDQ: AG6 AF6 AE6 AD6 AC13 AC7 AB17 AB16 AB13 AB9 AB8 AB7 AG7 AF7 AE7 AD8 AD7 AC9 PEX_IOVDDQ
PEX_IOVDD: PEX_IOVDD
PEX_PLLVDD: AF9 +PEX_PLLVDD
VID_PLLVDD: K6 +1.1VS_PLL
SP_PLLVDD: L6
PLLVDD: K5
FB_PLLAVDD: R19 +FB_PLLAVDD
FB_DLLAVDD: T19 +FB_DLLAVDD
DACA_VDD: AG2 +DACA_VDD
DACB_VDD: D7 +DACB_VDD
DACC_VDD: W5 +DACC_VDD
IFPA_IOVDD: V3
IFPB_IOVDD: V2
IFPC_IOVDD: J6
IFPE_IOVDD: H6
IFPAB_PLLVDD: AD5
IFPC_PLLVDD: P6
IFPE_PLLVDD: N6
FB_CAL_PD_VDDQ: B15

PLACE NEAR BGA
+1.8VS
0.022U_0402_16V7K
0.1U_0402_16V4Z
4.7U 6.3V K X5R 0603
C971 C972 C973 C974 C975 C976
PM@
0.022U_0402_16V7K
0.1U_0402_16V4Z
4.7U 6.3V K X5R 0603

PLACE BELOW GPU
FBAVDDQ=2.24A
+1.8VS
4700P_0402_25V7K
4700P_0402_25V7K
1U_0603_10V4Z
C984 C985 C986 C987 C988 C989
PM@
4700P_0402_25V7K
0.022U_0402_16V7K
0.1U_0402_16V4Z
+1.8VS
4700P_0402_25V7K
0.022U_0402_16V7K
1U_0603_10V4Z
C996 C997 C998 C999 C1000
PM@
4700P_0402_25V7K
0.1U_0402_16V4Z

0.1U_0402_16V4Z
0.47U_0402_6.3V6K
C1003 C1004 C1005 C1006
PM@
0.1U_0402_16V4Z
0.47U_0402_6.3V6K
1U_0402_6.3V4Z
C1007
PM@
NEAR BALL

+1.1VS
PEX_IOVDDQ=1.6A
PEX_IOVDD=500mA
PEX_PLLVDD=100mA
10U_0805_10V4Z
C1008 C1009 C1010
PM@
4.7U 6.3V K X5R 0603
10U_0805_10V4Z

+1.8VS
L28
MBK1608121YZF_0603
PM@
4700P_0402_25V7K
470P_0402_50V7K
C1019 C1020 C1021
PM@
4.7U 6.3V K X5R 0603
110mA
NEAR BGA
NEAR BALL
+1.8VS
L31
MBK1608121YZF_0603
PM@
4700P_0402_25V7K
470P_0402_50V7K
C1025 C1026 C1027
PM@
4.7U 6.3V K X5R 0603

+IFPA_IOVDD
+IFPB_IOVDD
+IFPC_IOVDD
12~16mil
10K_0402_5%
R994
PM@
+IFPAB_PLLVDD
+IFPC_PLLVDD
10K_0402_5%
R997
PM@

+1.8VS
MBK1608121YZF_0603
L27
PM@
+1.1VS
0.1U_0402_16V4Z
1U_0402_6.3V6K
C1014 C1015 C1016 C1017 C1018
PM@
0.1U_0402_16V4Z
1U_0402_6.3V6K
1U_0402_6.3V6K
NEAR BALL
PLLVDD=65mA
SP_PLLVDD=25mA
VID_PLLVDD=50mA

12~16mil
+1.8VS
R995
PM@
10K_0402_5%
R996
@
10K_0402_5%
+1.8VS
R998
PM@
30.1_0402_1%

+PEX_PLLVDD
0.1U_0402_16V4Z
10U_0805_10V4Z
L32
MBK1608121YZF_0603
PM@
+1.1VS
C1028 C1029 C1030 C1031
PM@
0.01U_0402_16V7K
1U_0402_6.3V4Z
NEAR BALL
NEAR BGA

+FB_PLLAVDD
0.1U_0402_16V4Z
L30
MBK1608121YZF_0603
PM@
+1.1VS
C1022 C1023 C1024
PM@
0.01U_0402_16V7K
4.7U 6.3V K X5R 0603
+FB_DLLAVDD
0.1U_0402_16V4Z
L34
MBK1608121YZF_0603
PM@
C1032 C1033 C1034
PM@
0.01U_0402_16V7K
4.7U 6.3V K X5R 0603

IFPC_PLLVDD: please add option to support
both 1.8V (for G9X) and 3.3V(for GT21X)

+1.8VS
L35
MBK1608121YZF_0603
55NM_HDMI@
4700P_0402_25V7K
+IFPC_PLLVDD
+3VS
L37
40NM_HDMI@
MBK1608121YZF_0603
C1035
PM_HDMI@
C1036
PM_HDMI@
4.7U 6.3V K X5R 0603
C1036
0 0402 5%
PM_NOHDMI@
+1.1VS
L40
MBK1608121YZF_0603
PM_HDMI@
4700P_0402_25V7K
+IFPC_IOVDD
NEAR BGA
C1042
PM_HDMI@
C1043
PM_HDMI@
C1044
PM_HDMI@
4.7U 6.3V K X5R 0603
470P_0402_50V7K
C1044
0 0402 5%
PM_NOHDMI@
NEAR BALL

260mA
NEAR BGA
+1.8VS
L36
MBK1608121YZF_0603
55NM@
4700P_0402_25V7K
+IFPAB_PLLVDD
NEAR BALL
+1.1VS
L39
40NM@
MBK1608121YZF_0603
4.7U 6.3V K X5R 0603
C1037
PM@
C1038
PM@
IFPAB_PLLVDD: please add option to support
both 1.8V(for G9X) and 1.05V(for GT21X)

R996
37.4_0402_1%
40NM@

+DACA_VDD
4700P_0402_25V7K
4.7U 6.3V K X5R 0603
+3VS
L38
MBK1608121YZF_0603
PM@
C1039 C1040 C1041
PM@
470P_0402_50V7K
110mA

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

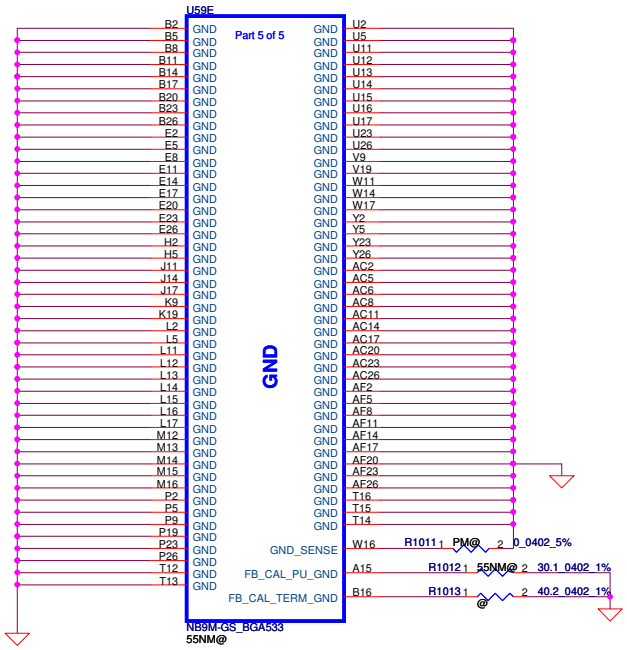
Compal Electronics, Inc.

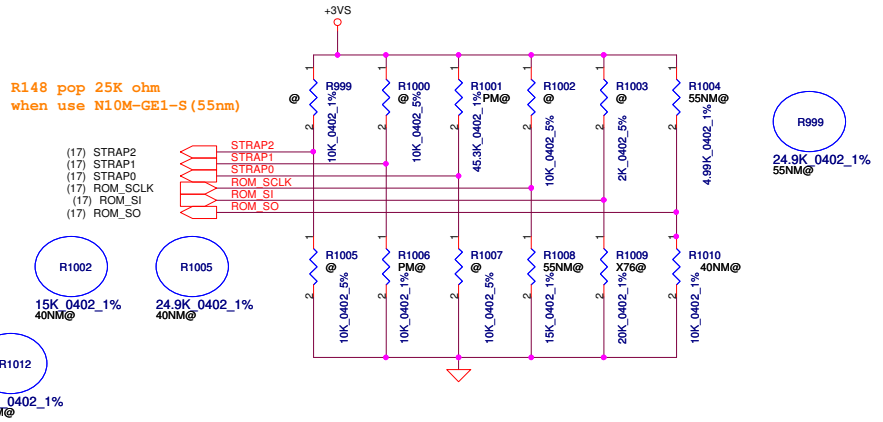
Title: NB10M Power

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 18 of 53

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available





Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)

U59
NB10M-GS-S
40NM@

GB1 Family GPU Strap Options X76

GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K	PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 5K	PD 10K	PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K	PU 45K
GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 10K	PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

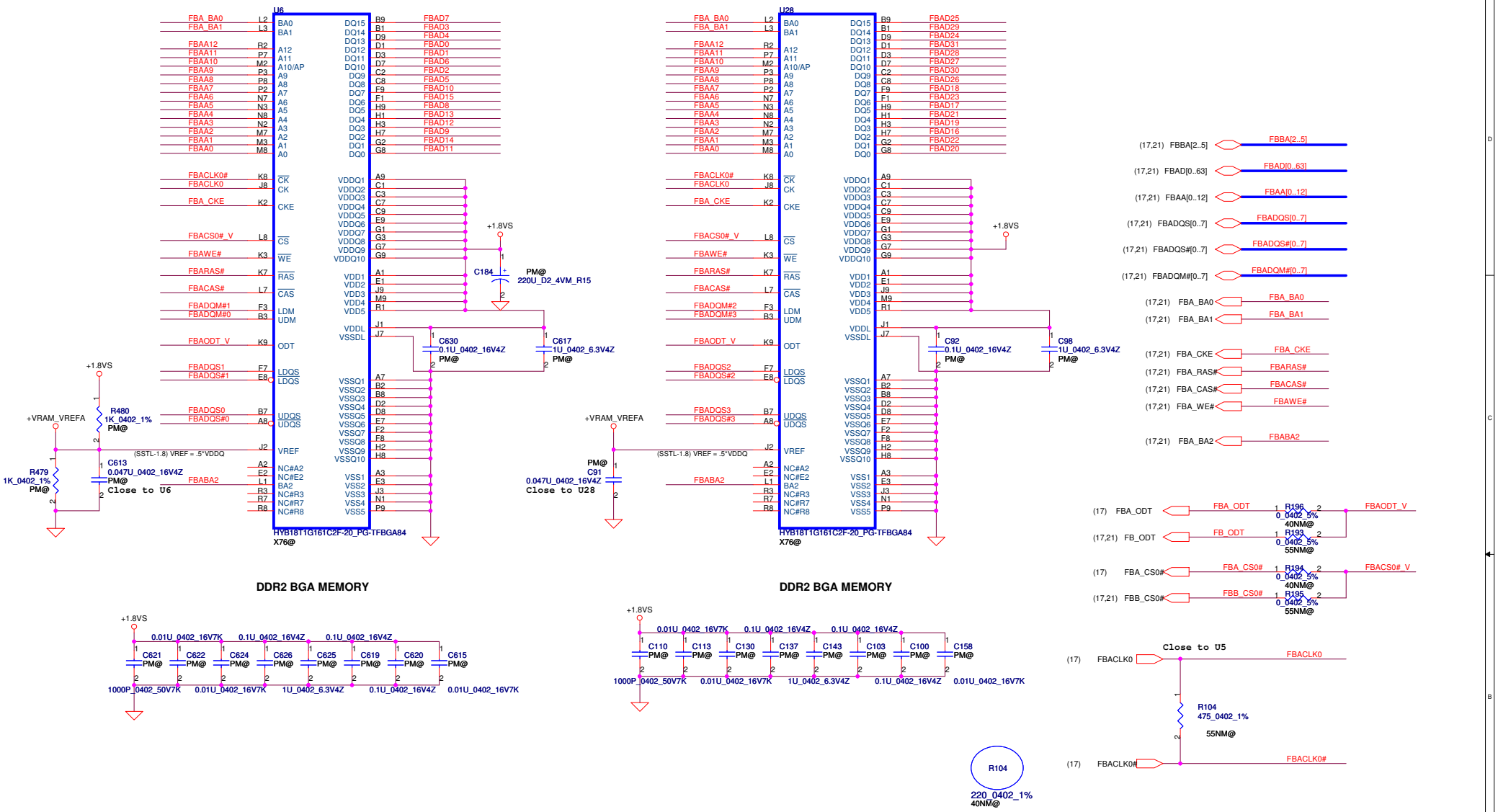
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10M GND & STRAP

Size	Document Number	Rev
B	KIWA5/6 LA-5081P	0.4

Date: Thursday, March 19, 2009 Sheet 19 of 53



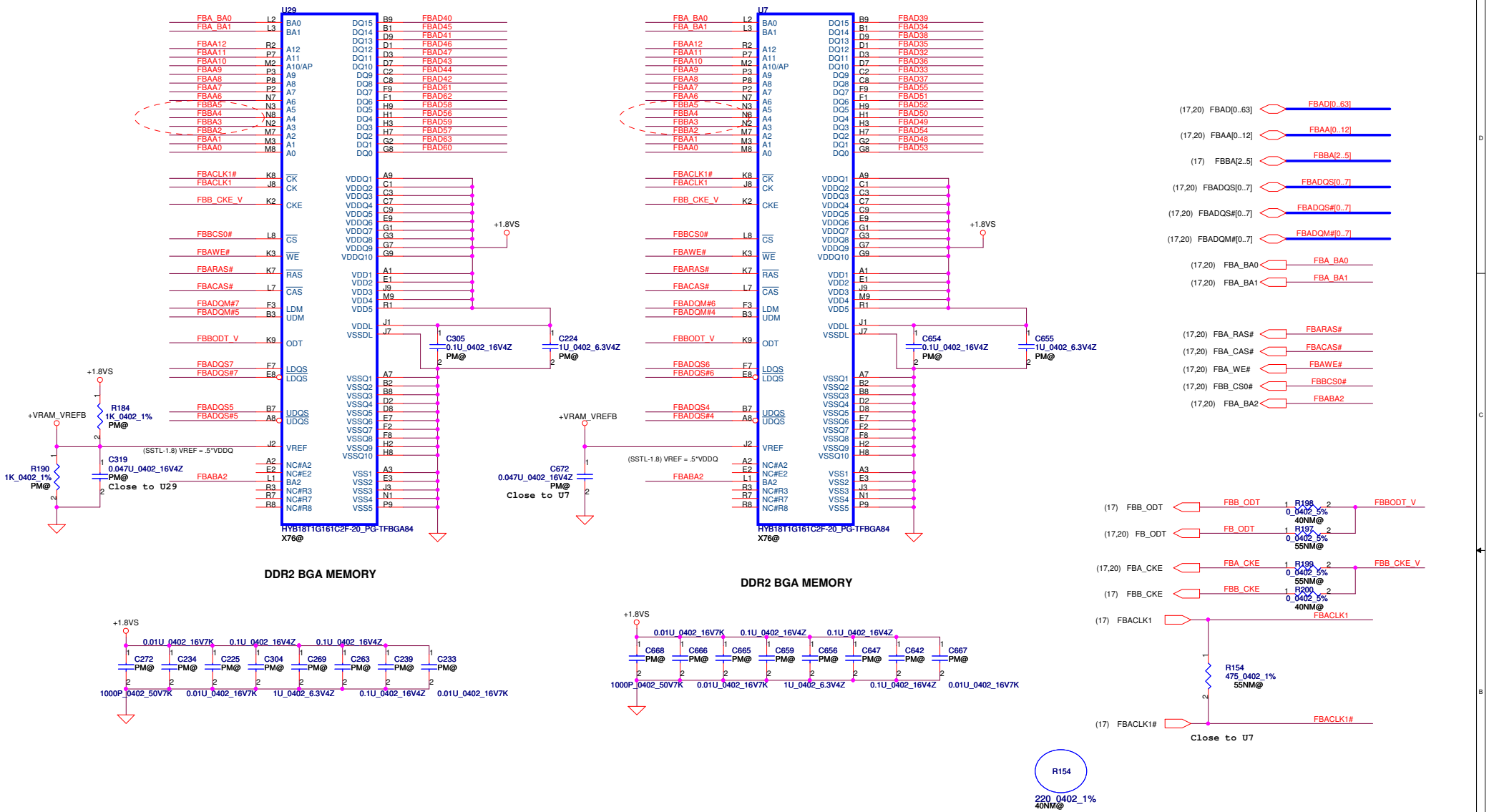
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 20 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDRB**

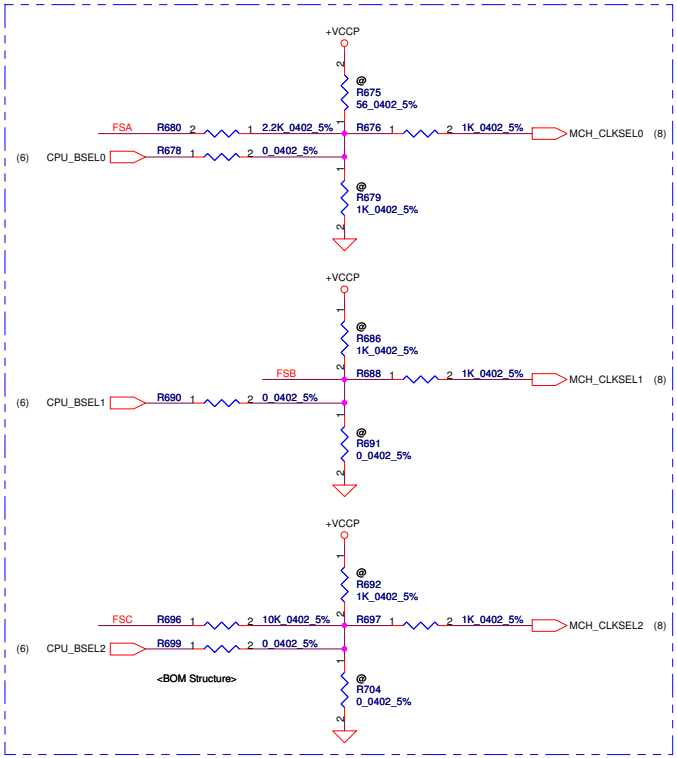
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

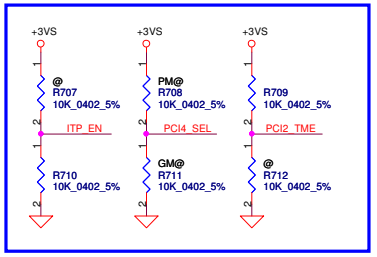
Date: Wednesday, March 18, 2009 | Sheet 21 of 53

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

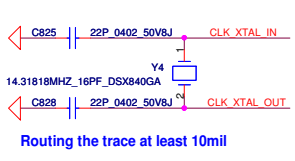
SA000020H00 (ICS : ICS9LPRS387AKLFT)



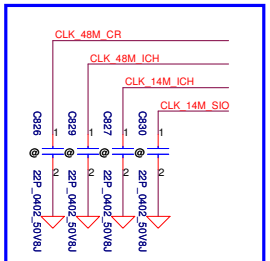


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

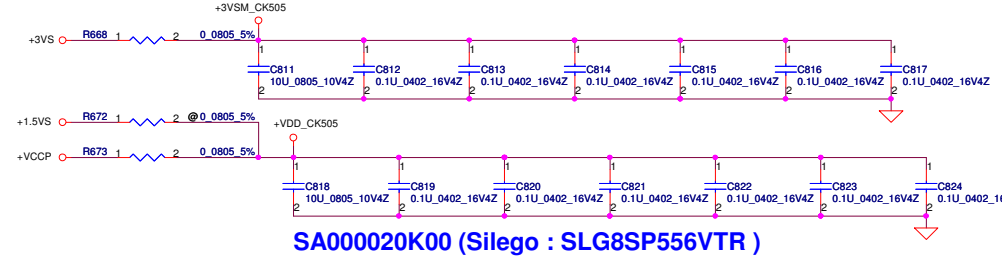
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

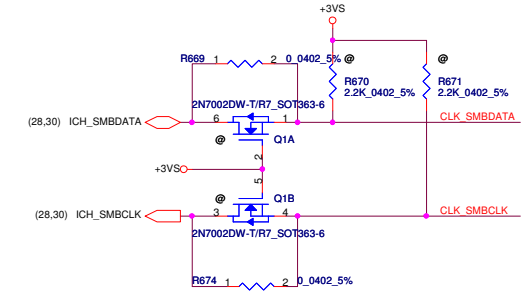


Routing the trace at least 10mil



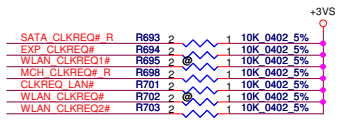
place CAPs near Resistors of U10
For 3G RF noise .





SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: **Clock Generator CK505**

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 22 of 53

10/30 update PS8171 co-lay circuit

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

For 8171

PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PIO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	ASQ1
PIN12	GND	APD
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD

Reserved for CH7318C

1.2k for CH7318C

place those component near JP? for NV request 0515

TMDS pull down (500ohm) resistors for ATI M92-S2 XT

NEAR CONNECTOR

PS8101TQFN48G_QFN48_7X7

KIWB3/B4_LA4551P

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

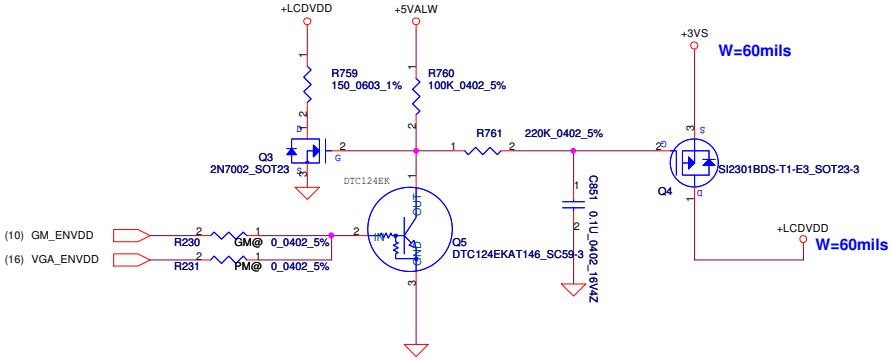
Compal Electronics, Inc.

Title: **Level Shiftter_PS8101T**

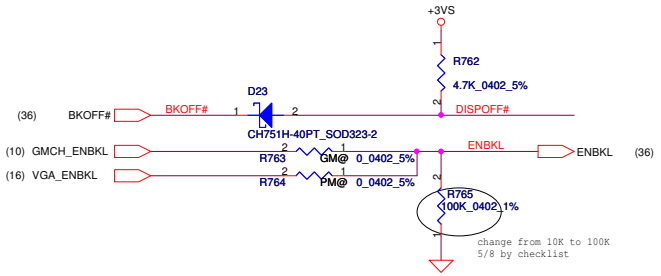
Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

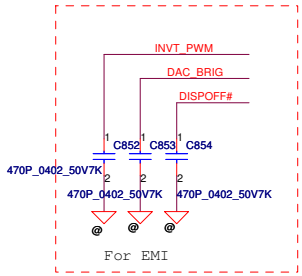
Date: Wednesday, March 18, 2009 | Sheet 23 of 53

LCD POWER CIRCUIT

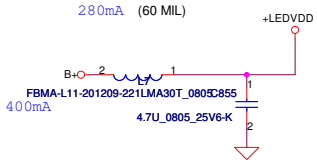


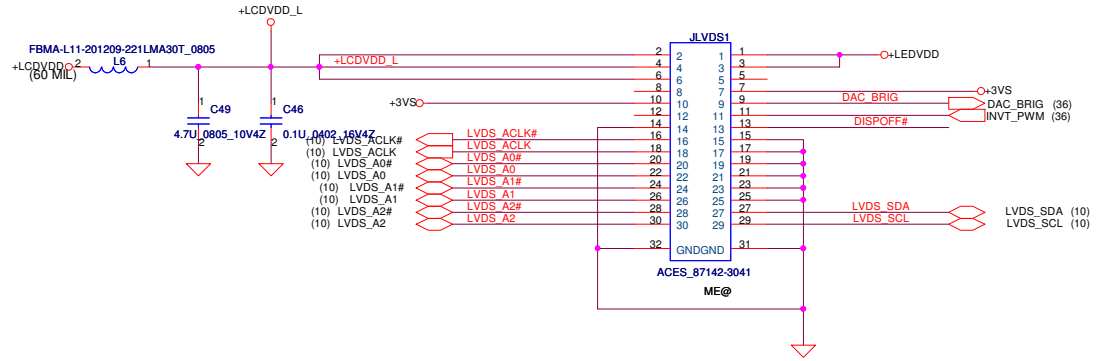
LCD/PANEL BD. Conn. FOR UMA

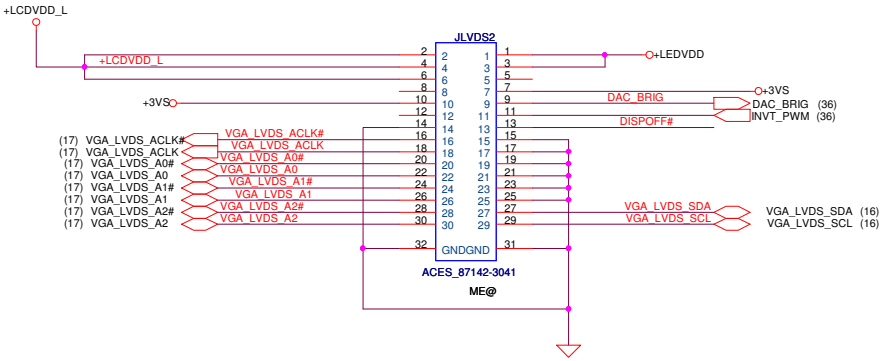




LCD/PANEL BD. Conn. FOR DIS







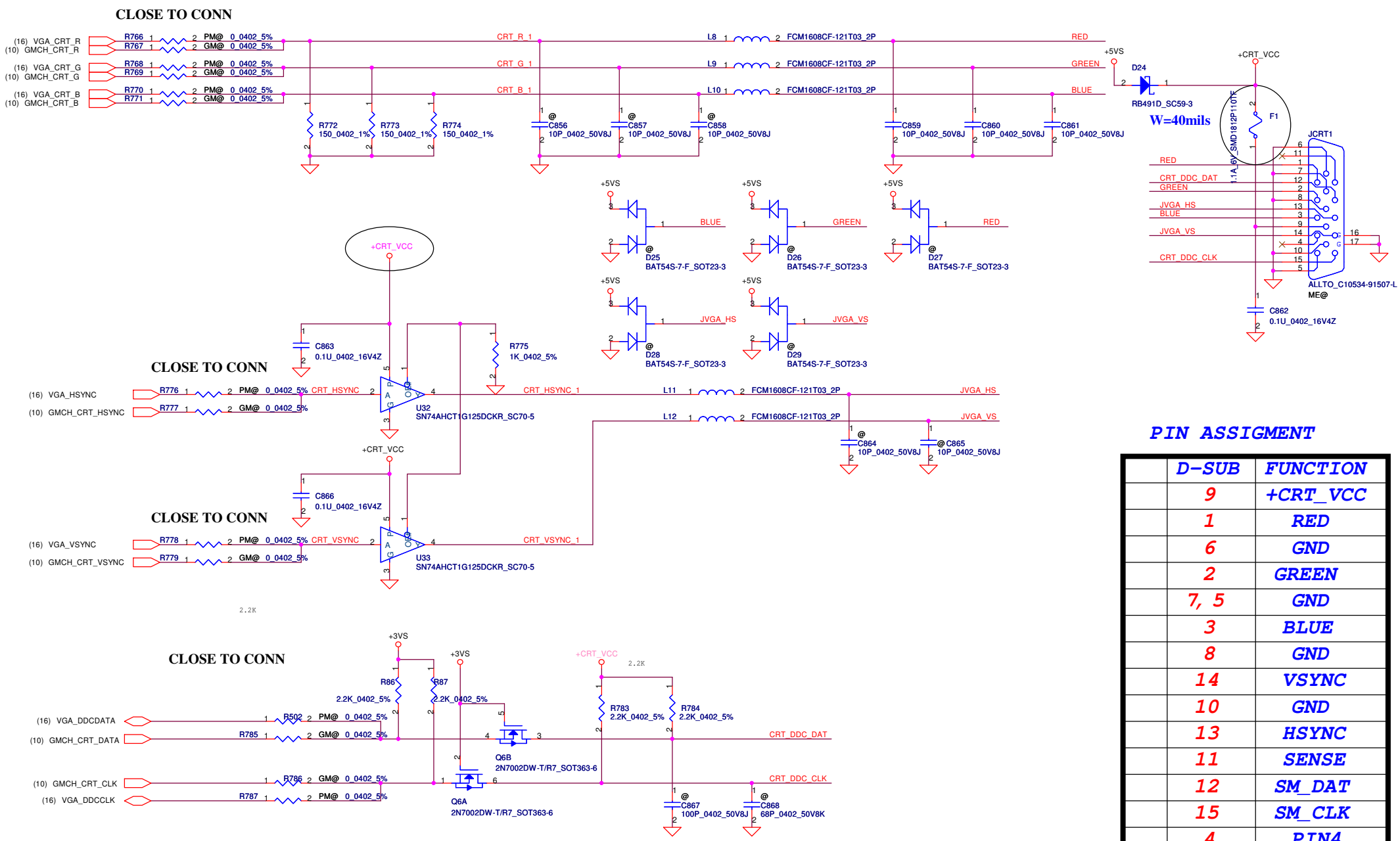
Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 24 of 53

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

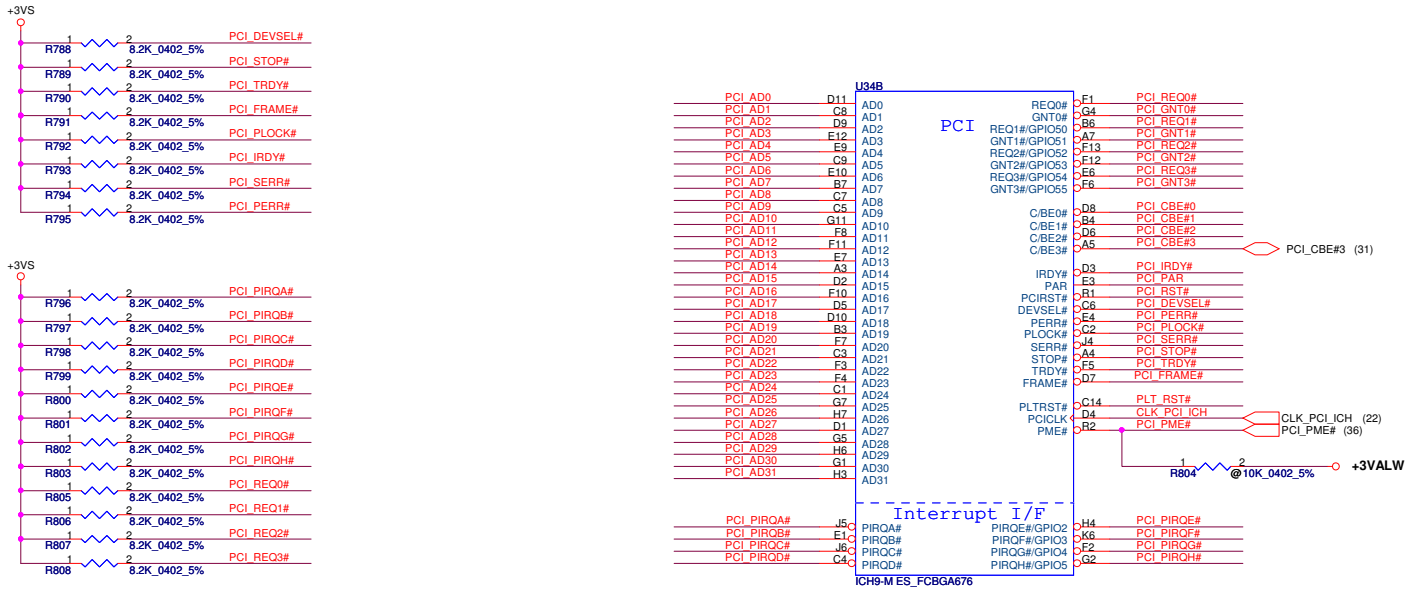
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 25 of 53

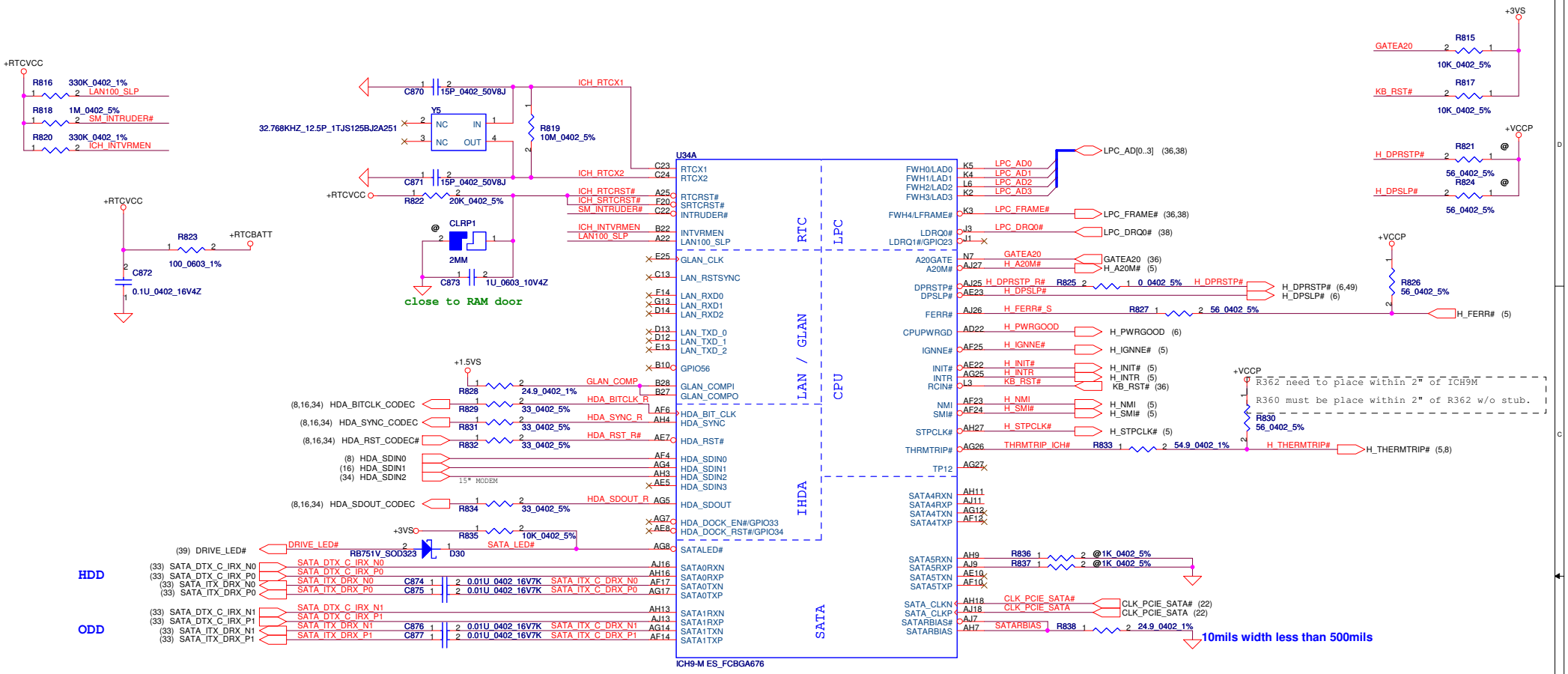


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: ICH9M(1/4)-PCI			
Size	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 26 of 53		



SATA PORT LIST

PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

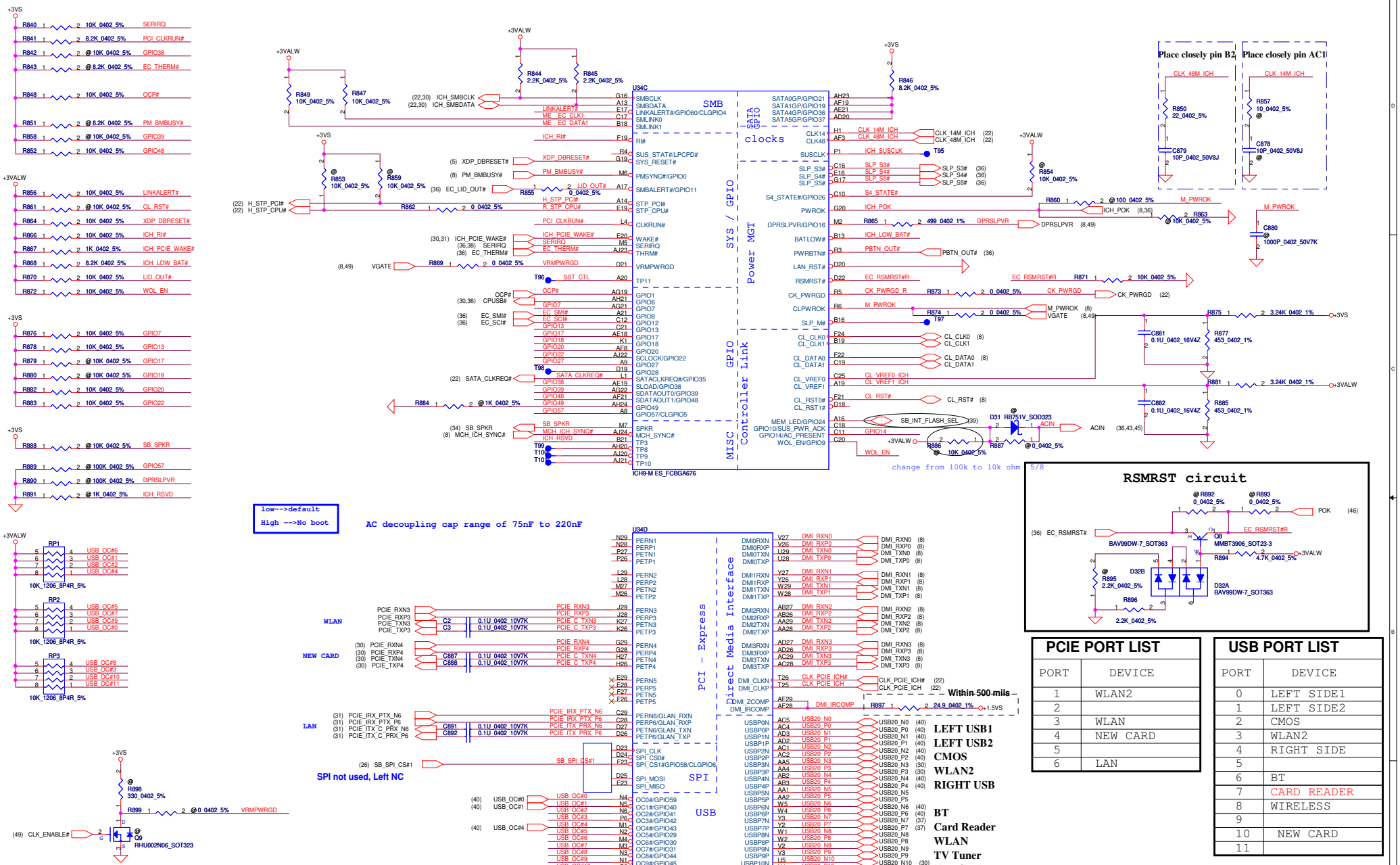
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 27 of 53



PCIE PORT LIST

PORT	DEVICE
1	WLAN2
2	
3	WLAN
4	NEW CARD
5	
6	LAN

USB PORT LIST

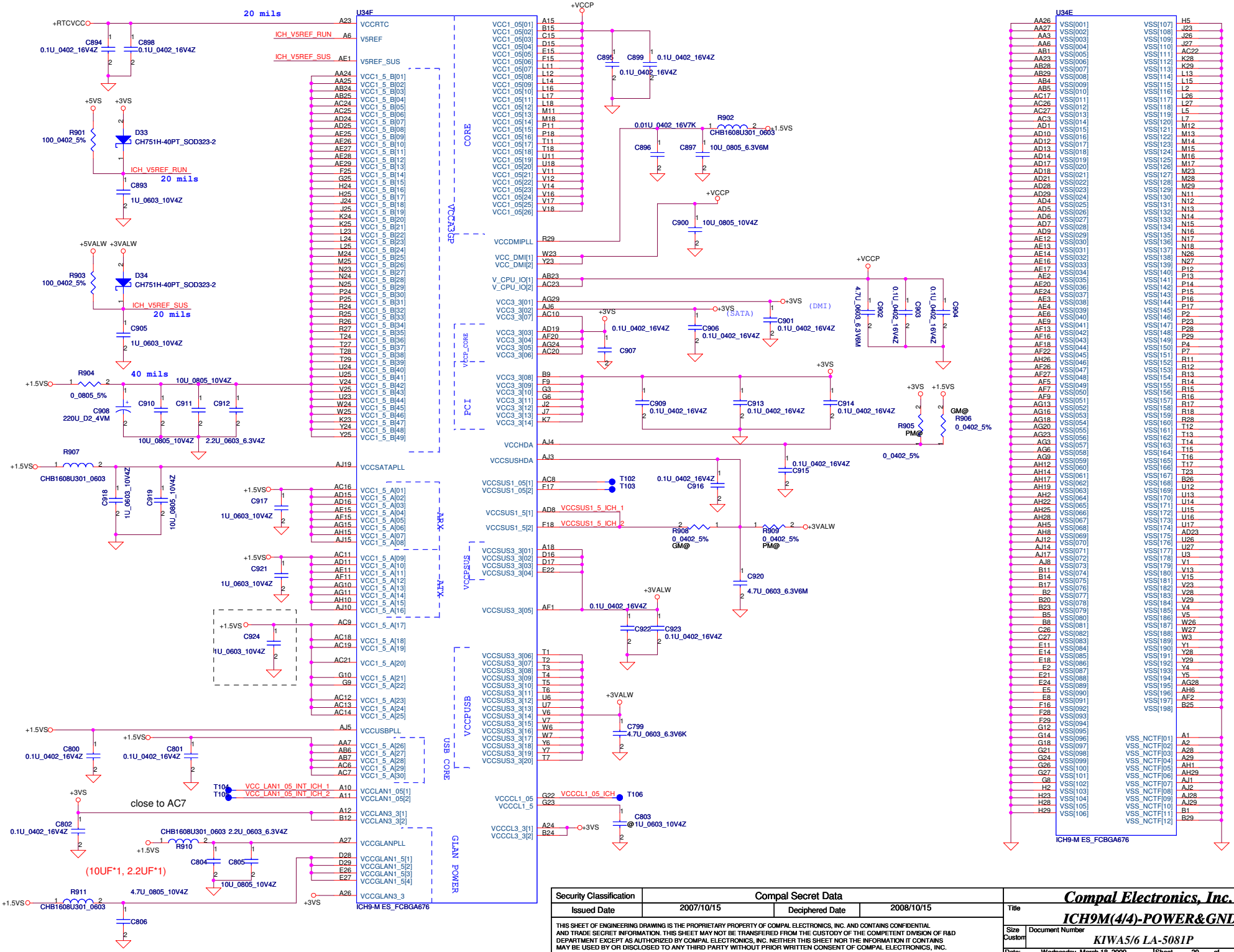
PORT	DEVICE
0	LEFT SIDE1
1	LEFT SIDE2
2	CMOS
3	WLAN2
4	RIGHT SIDE
5	
6	BT
7	CARD READER
8	WIRELESS
9	
10	NEW CARD
11	

Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size: C | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 28 of 53


U34F
ICH9-M ES_FCBGA676
U34E
ICH9-M ES_FCBGA676
20 mils
close to AC7
(10UF*1, 2.2UF*1)
CORE
VCCA3GP
PCI
VCCP_CORE
ATX
VCCPSUS
USB CORE
VCCCPUSB
GLAN POWER
Security Classification
Compal Secret Data
Issued Date
2007/10/15
Deciphered Date
2008/10/15
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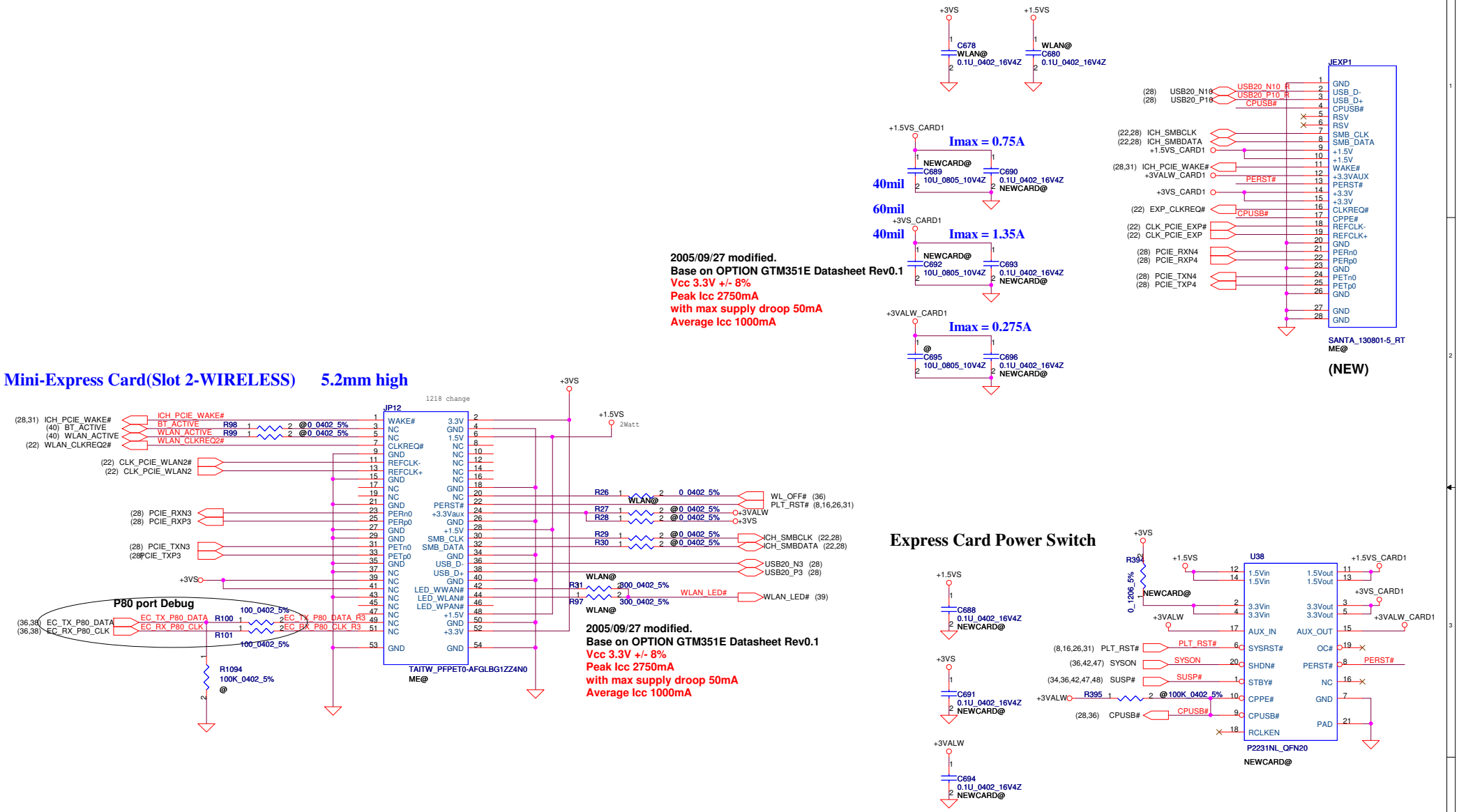
Compal Electronics, Inc.
Title
ICH9M(4/4)-POWER&GND
Size
Custom
Document Number
KIWA5/6 LA-5081P
Rev
0.4
Date:
Wednesday, March 18, 2009
Sheet
29
of
53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	Mini-Card/3G/TV /BT		
Size	Document Number	KIWAX_LA-5082P	Rev 0.4
Date: Wednesday, March 18, 2009	Sheet 30 of 53		

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

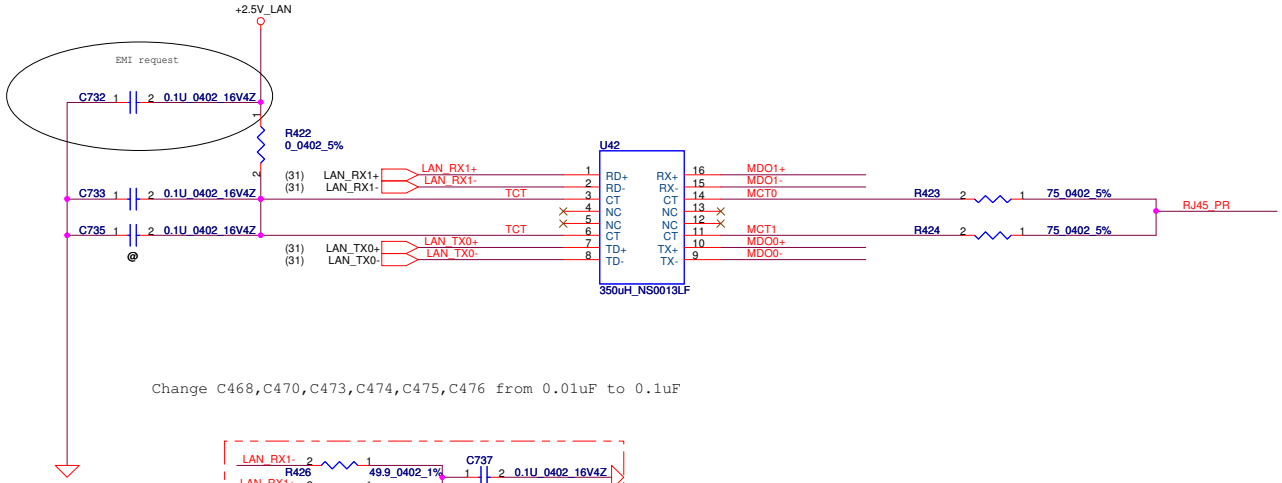
Compal Electronics, Inc.

Title: BCM5787MKML

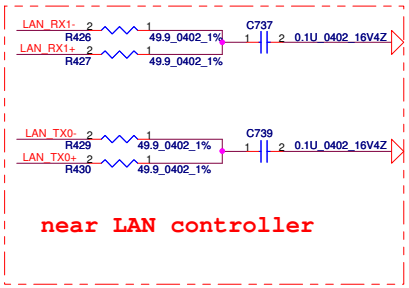
Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

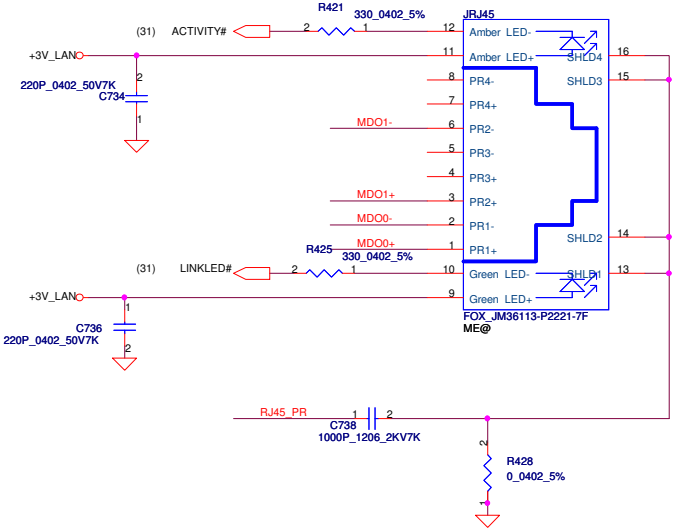
Date: Wednesday, March 18, 2009 | Sheet 31 of 53

RJ45 CONN



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF





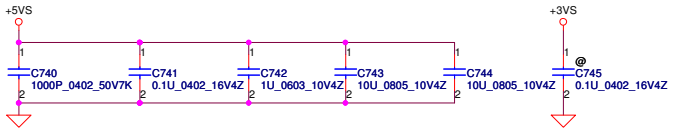
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

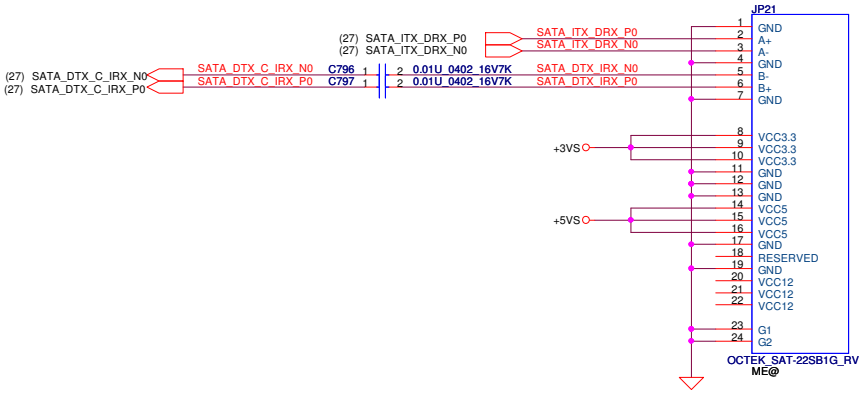
Title: LAN CONTROLLER

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

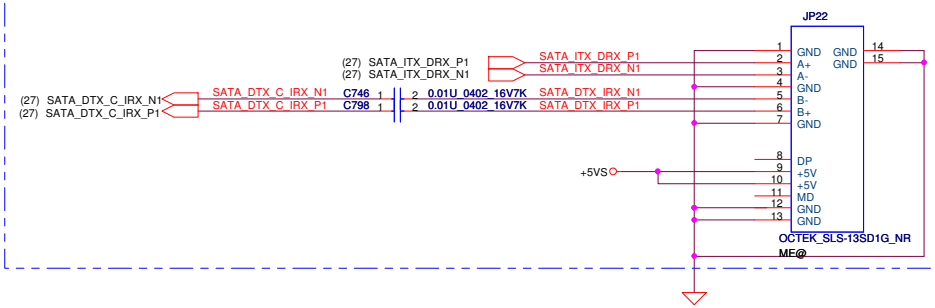
Date: Wednesday, March 18, 2009 Sheet 32 of 53



SATA HDD Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 33 of 53		

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CX20548
AMOM DAA

11/20 update
PC_BEEP dB control

0216_Change value.

CODEC POWER

(3.33V)
250mW

W=40Mil

2.2kohm for MICL + MICR
4.7kohm for MICL or MICR

external MIC
Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

11/20 update

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

DIGITAL ANALOG

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

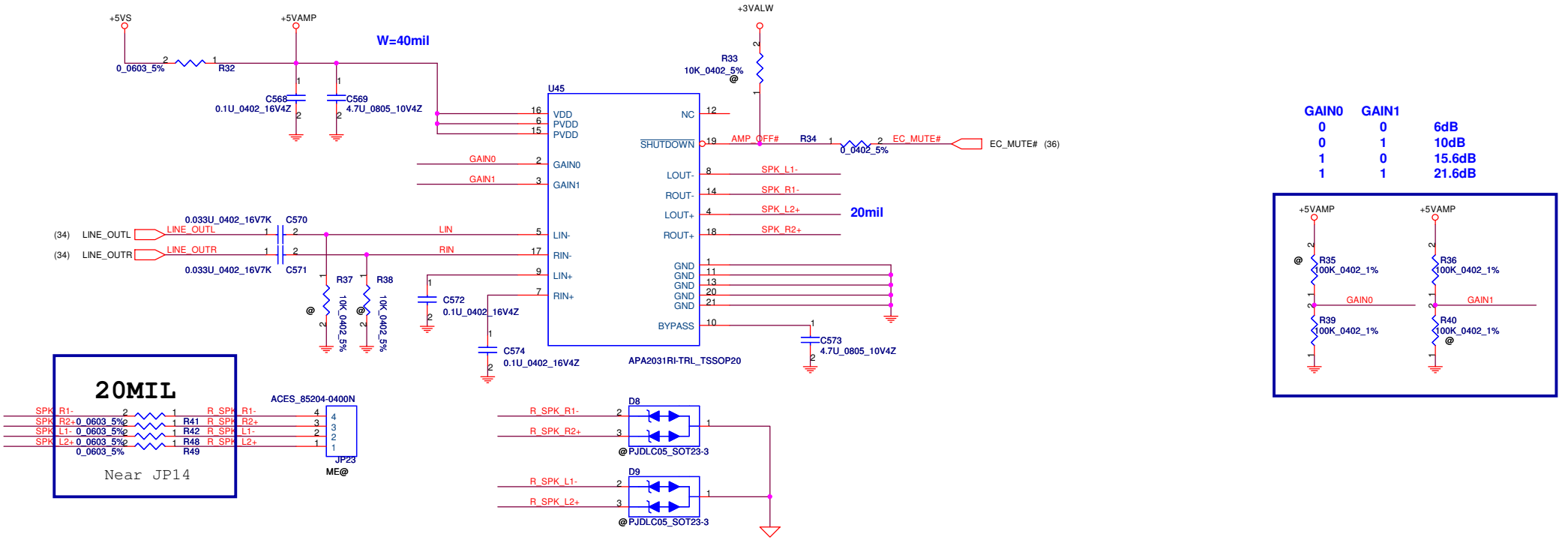
Compal Electronics, Inc.

Title: CX20561-AMOM Codec

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

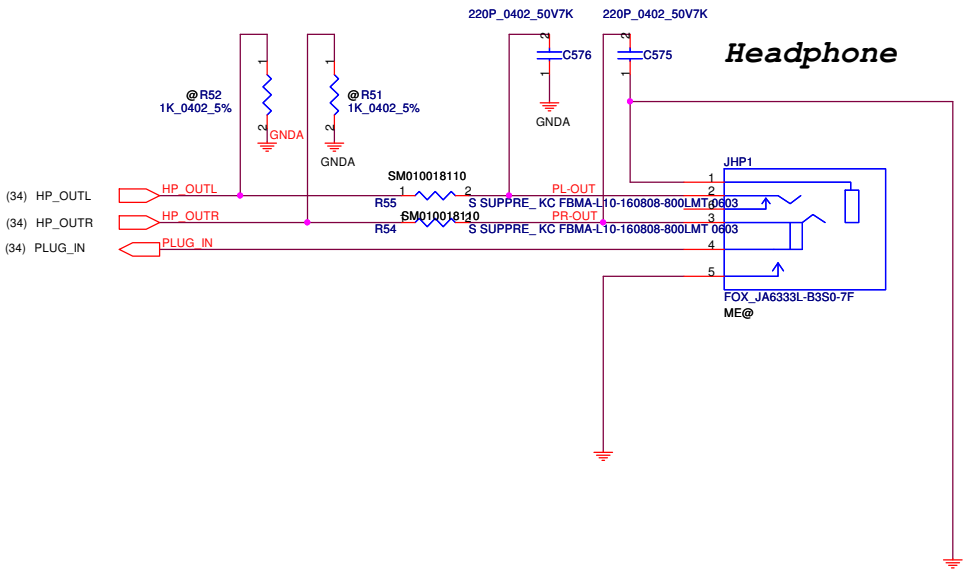
Date: Wednesday, March 18, 2009 | Sheet 34 of 53

Speaker Connector

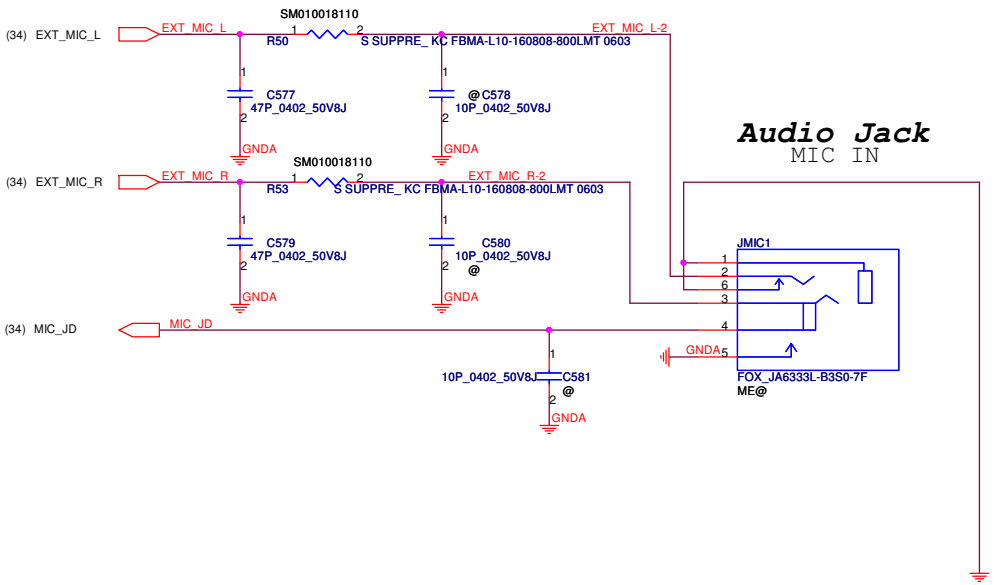


GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Headphone



Audio Jack



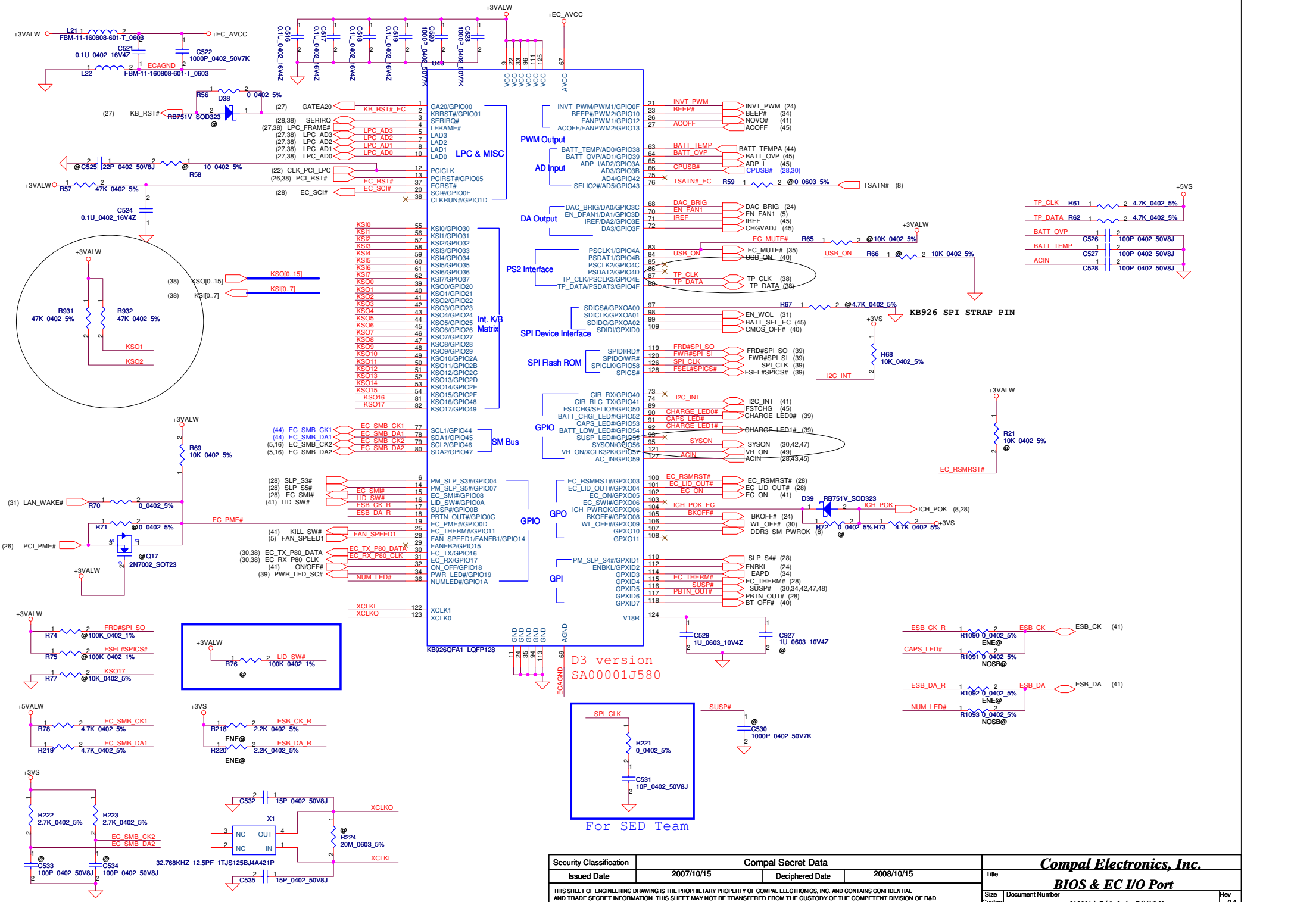
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: AMP,Audio speaker CONN

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 35 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

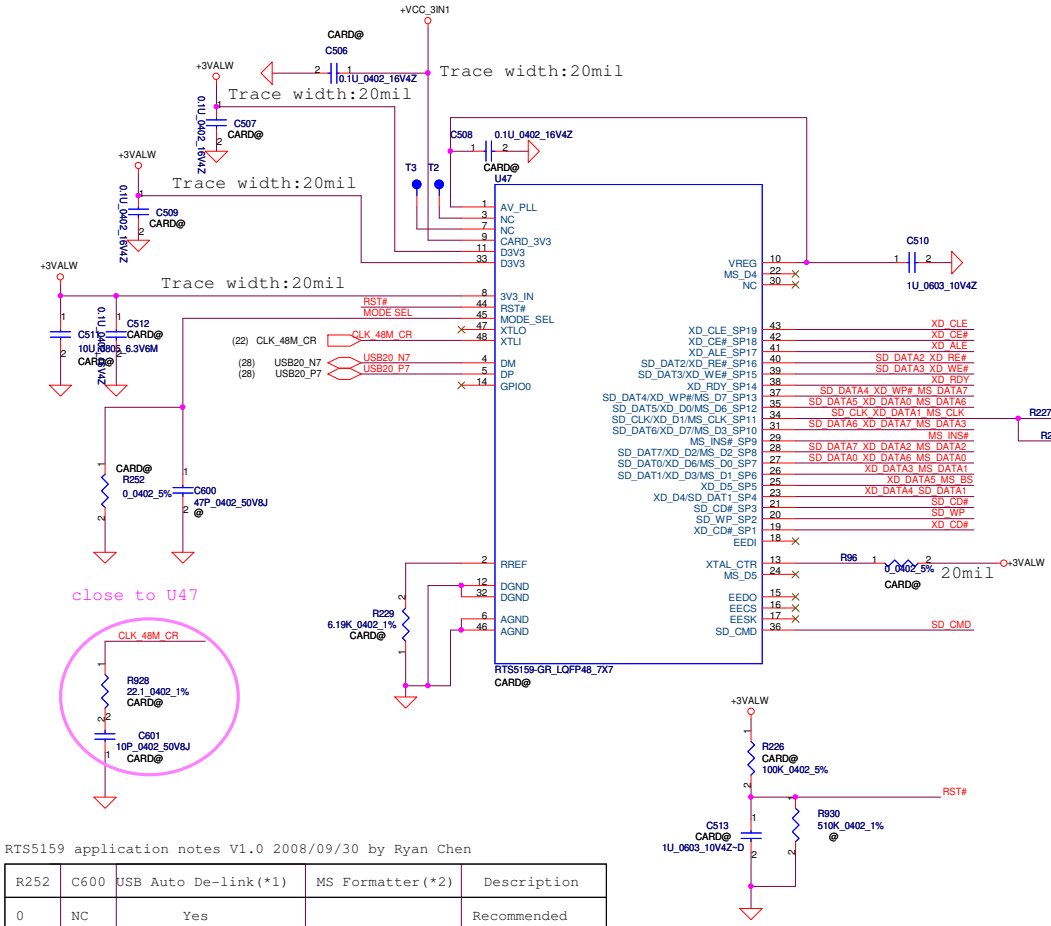
Compal Electronics, Inc.

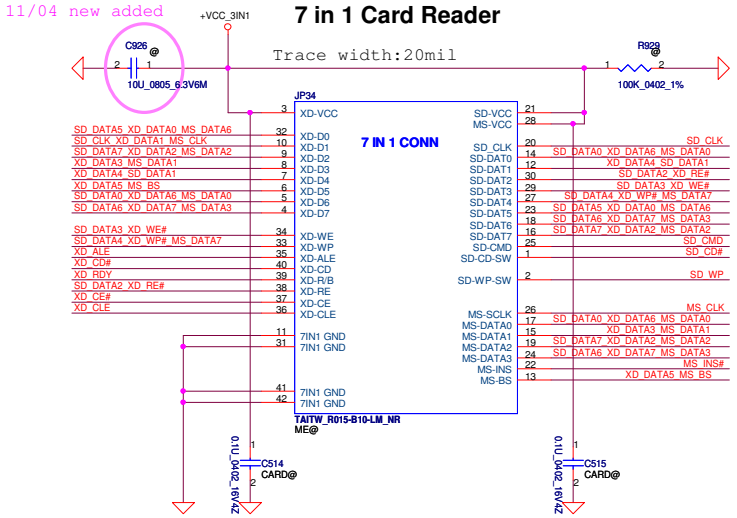
Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 36 of 53

Card reader(XD/SD/MMC/MS/MS-Pro HD SD)





RTS5159 application notes V1.0 2008/09/30 by Ryan Chen

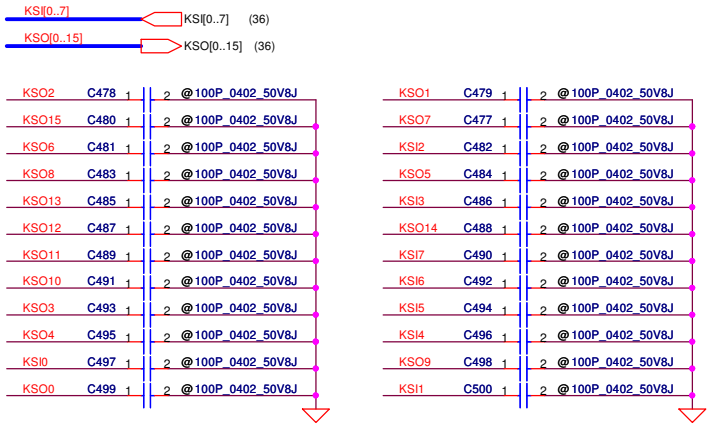
R252	C600	USB Auto De-link(*1)	MS Formatter(*2)	Description
0	NC	Yes		Recommended
NC	47pF	Yes	Yes	
NC	NC			Compatible with RTS5158E
NC	680pF	Yes		LED ON (*3)
10K	180pF			LED ON (*3)
10K	680pF		Yes	

Security Classification	Compal Secret Data		
Issued Date	2008/06/10	Deciphered Date	2008/12/31

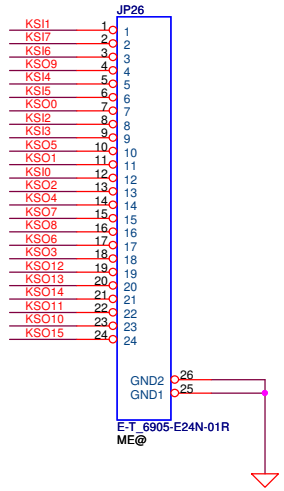
Compal Electronics, Inc.			
Title: USB_CR board			
Size: Custom	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 37 of 53		

Source:SP01000IE00
2nd source:SP01000IF00
30 pin

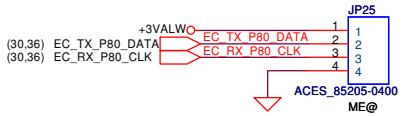
INT_KBD Conn.

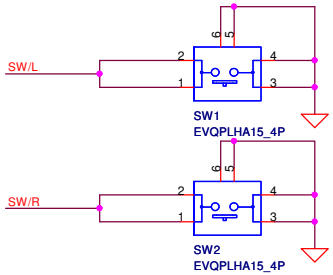


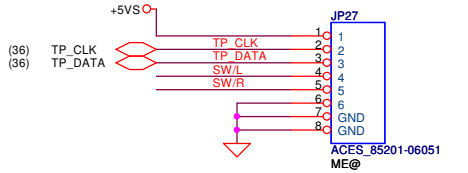
CONN PIN define need double check



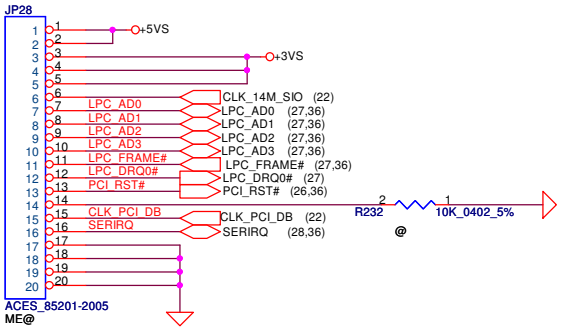
EC DEBUG PORT

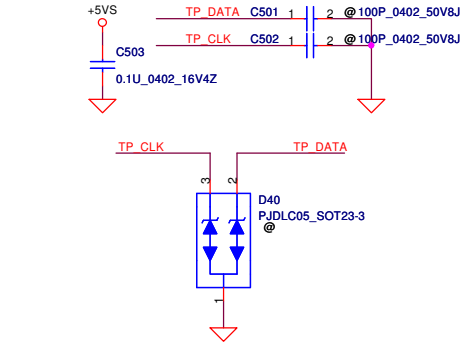






FOR LPC SIO DEBUG PORT

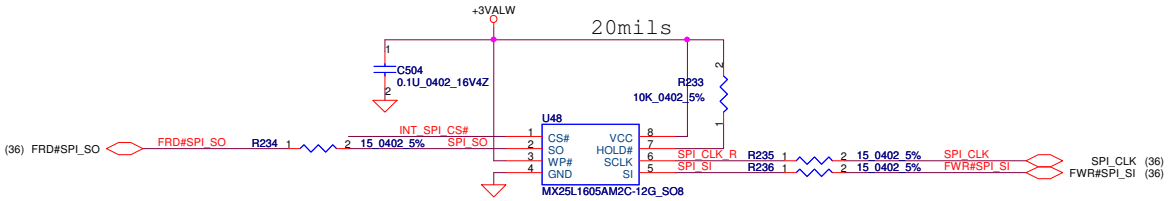


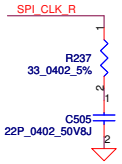


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 38 of 53		

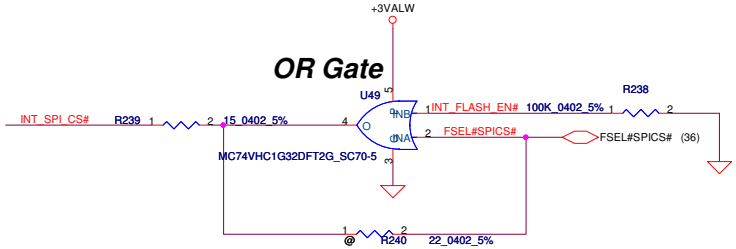
FOR EC 16M SPI ROM

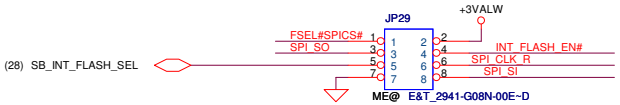




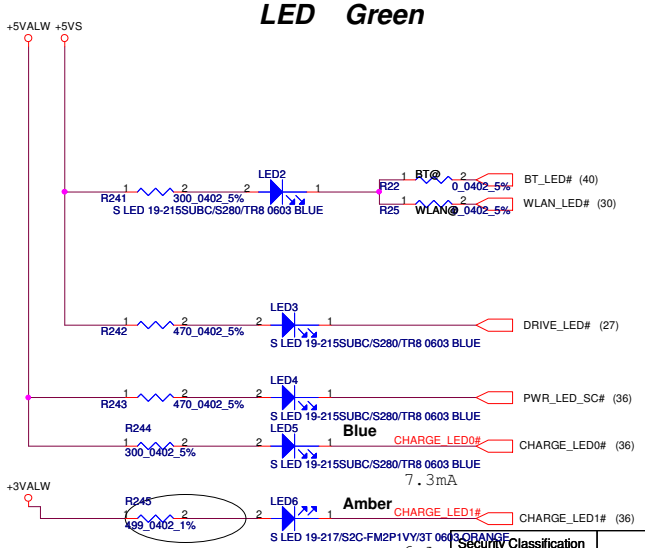
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

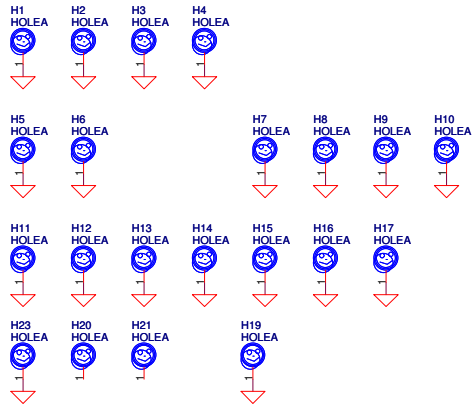
OR Gate





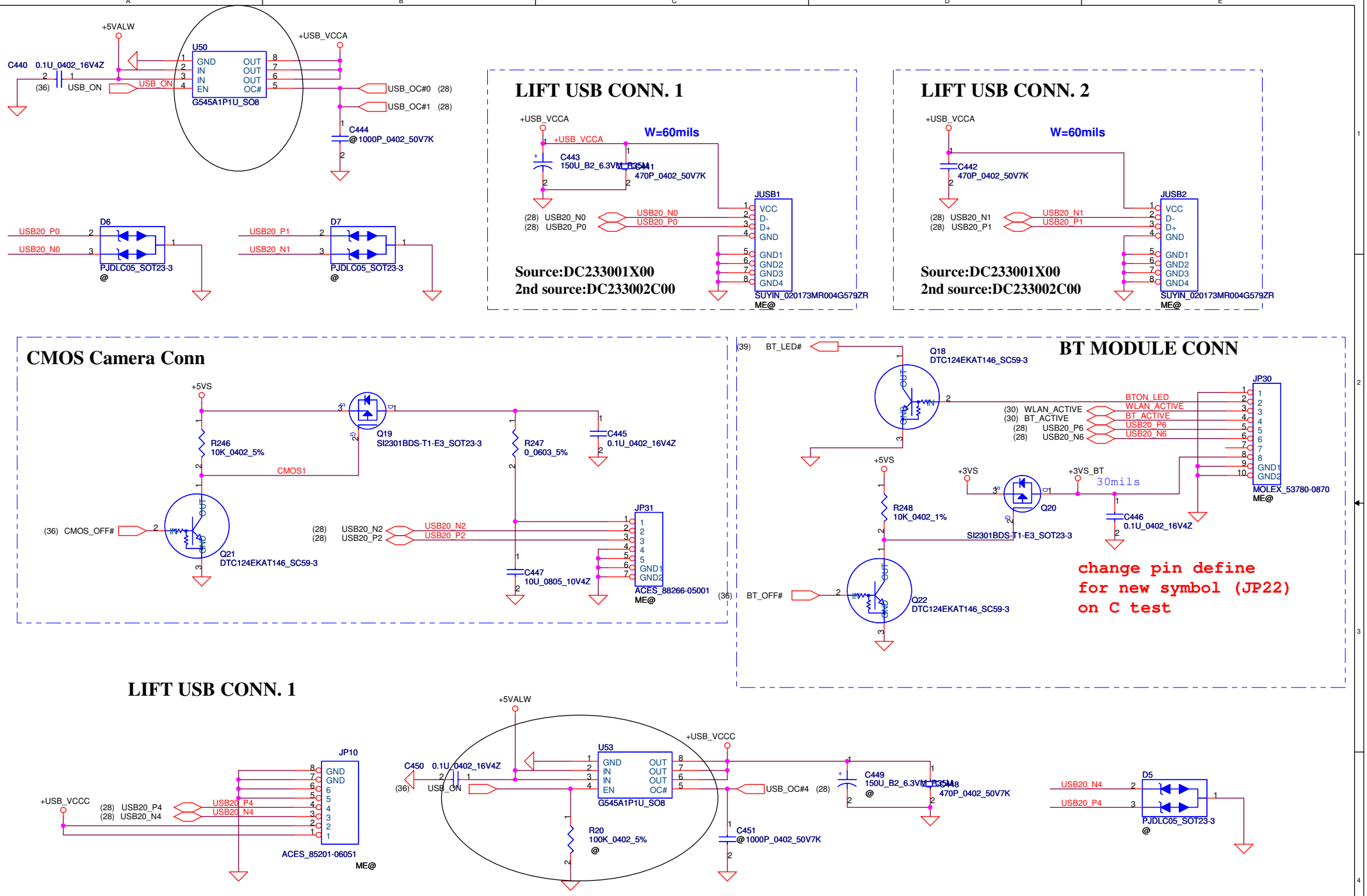
LED Green





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.	
Title	LED/EC SPI ROM
Size B	Document Number KIWA5/6 LA-5081P
Rev	0.4
Date: Wednesday, March 18, 2009	Sheet 39 of 53



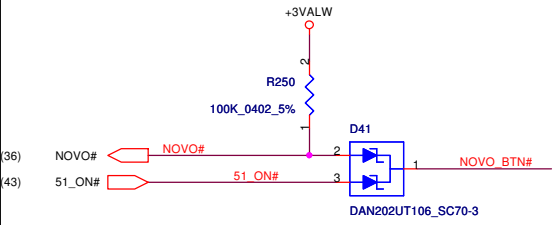
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

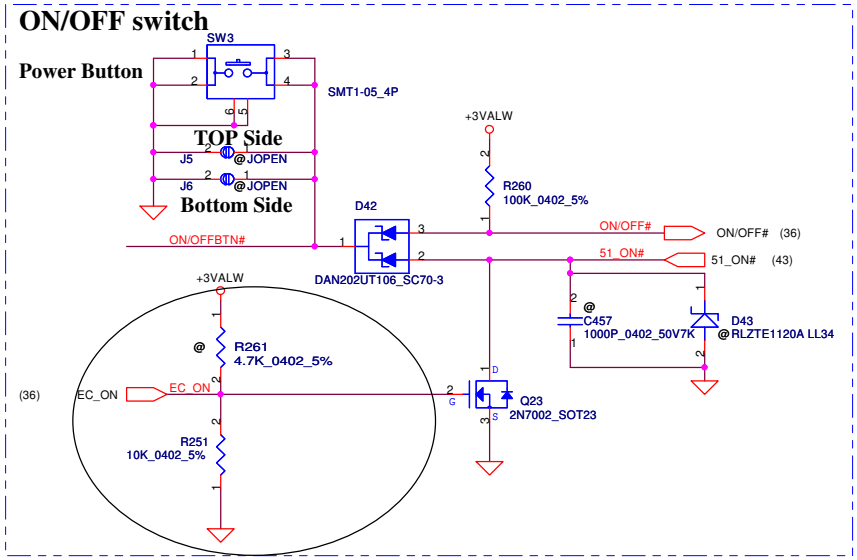
Compal Electronics, Inc.

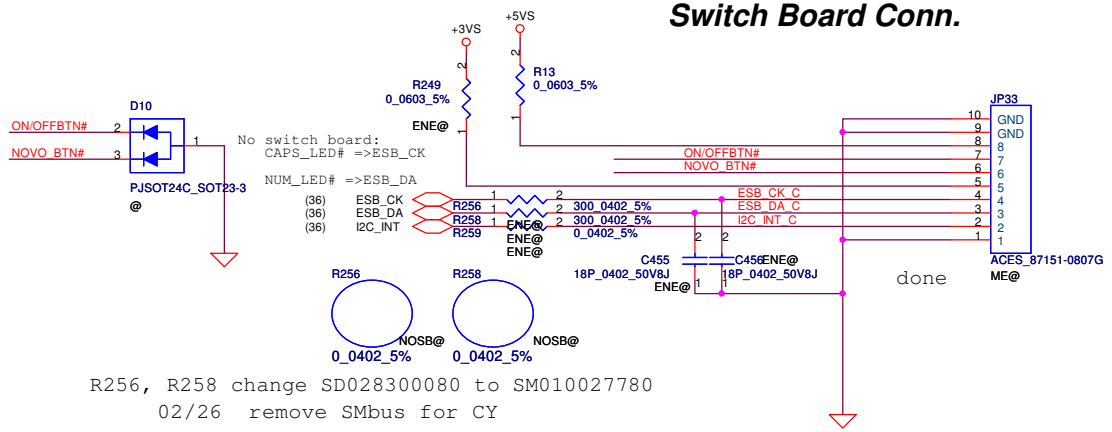
Title: Power OK, Reset and RTC Circuit, TP

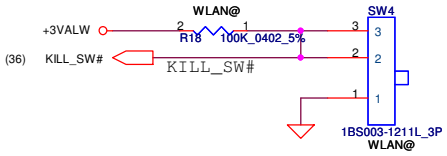
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

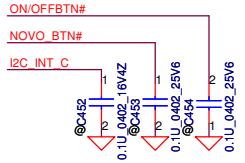
Date: Wednesday, March 18, 2009 Sheet 40 of 53

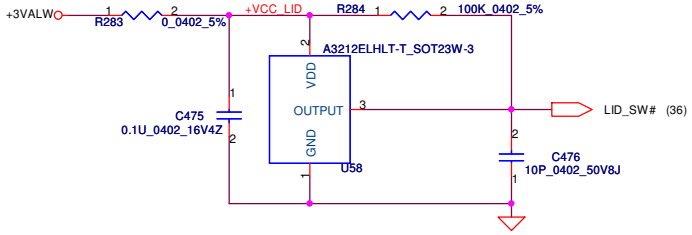








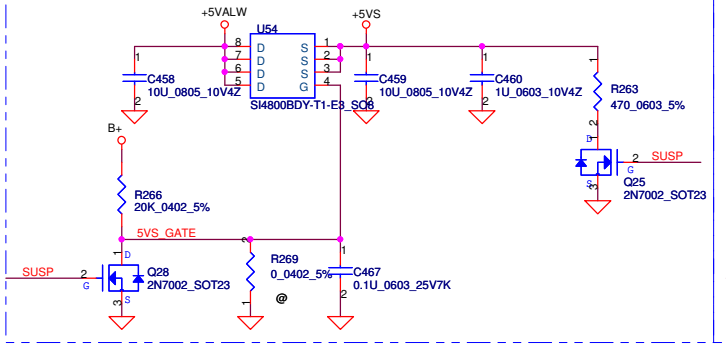




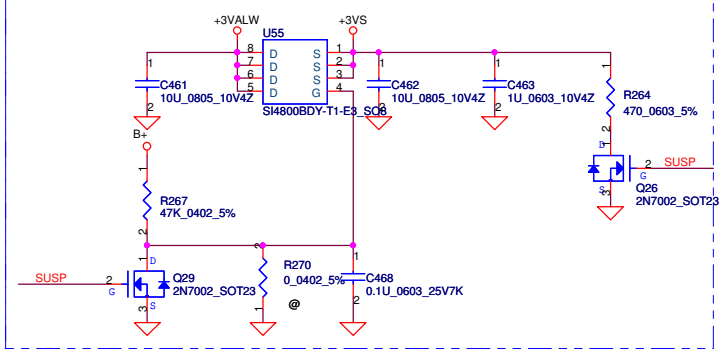
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

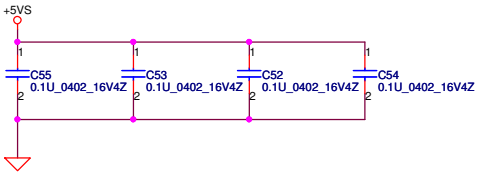
Compal Electronics, Inc.			
Title: Audio Jack & SW connector			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 41 of 53		

+5VALW TO +5VS

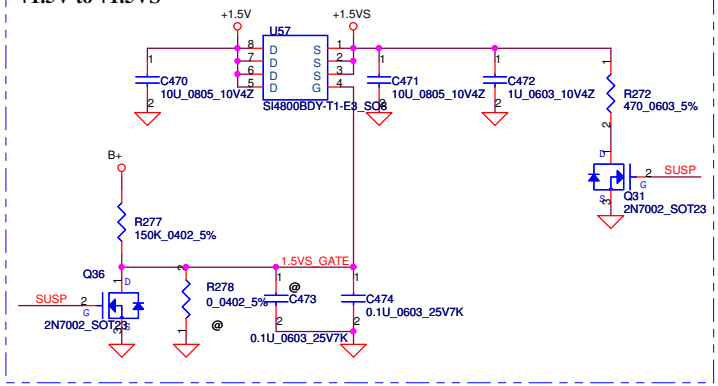


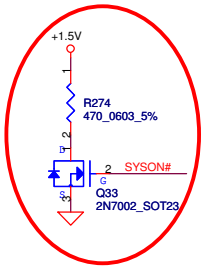
+3VALW TO +3VS

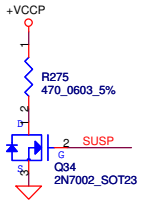


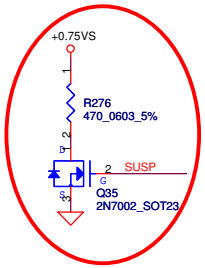


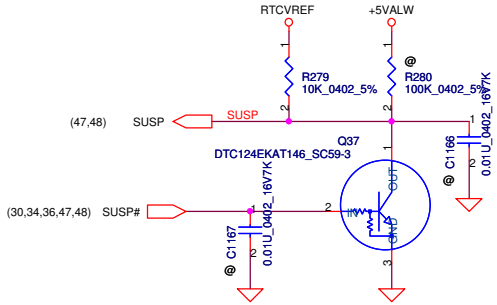
+1.5V to +1.5VS

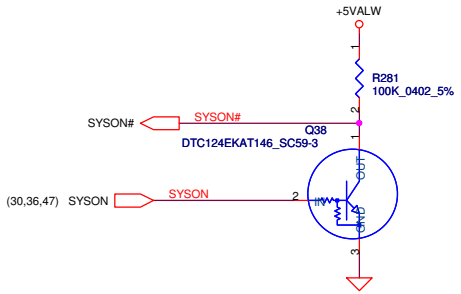












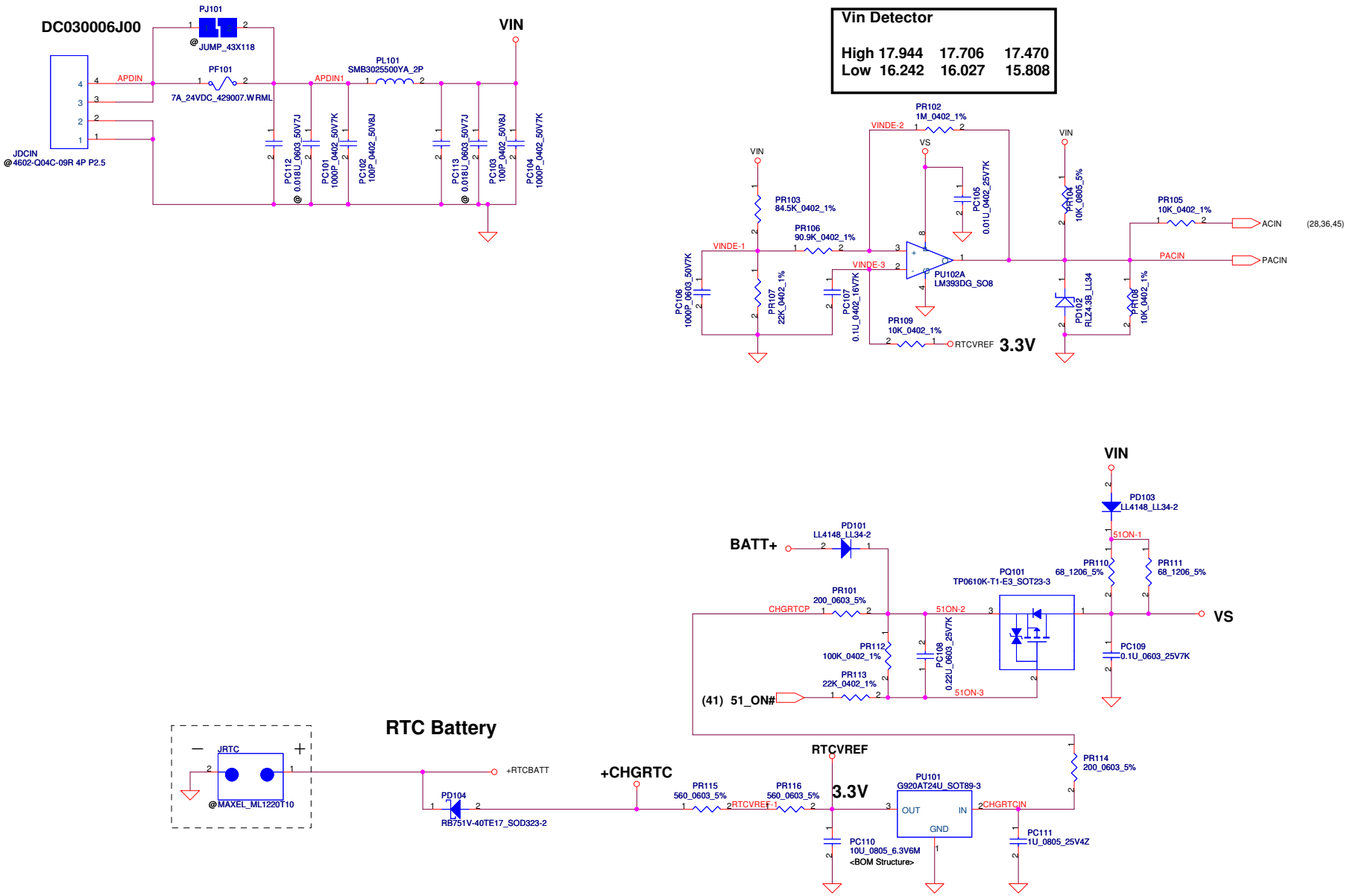
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 42 of 53



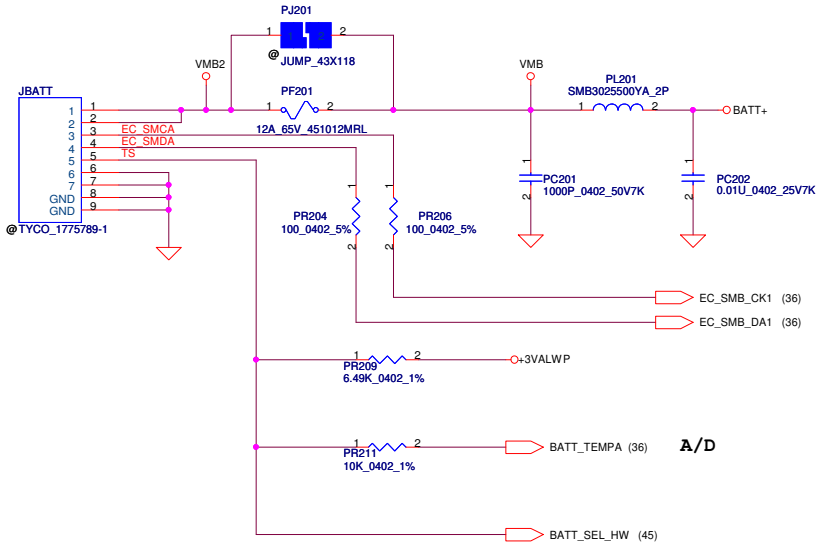
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.4

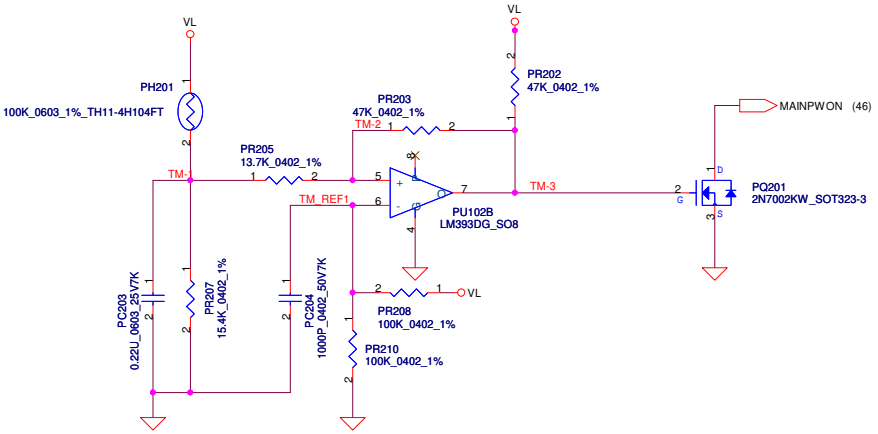
Date: Wednesday, March 18, 2009 | Sheet 43 of 53



PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C



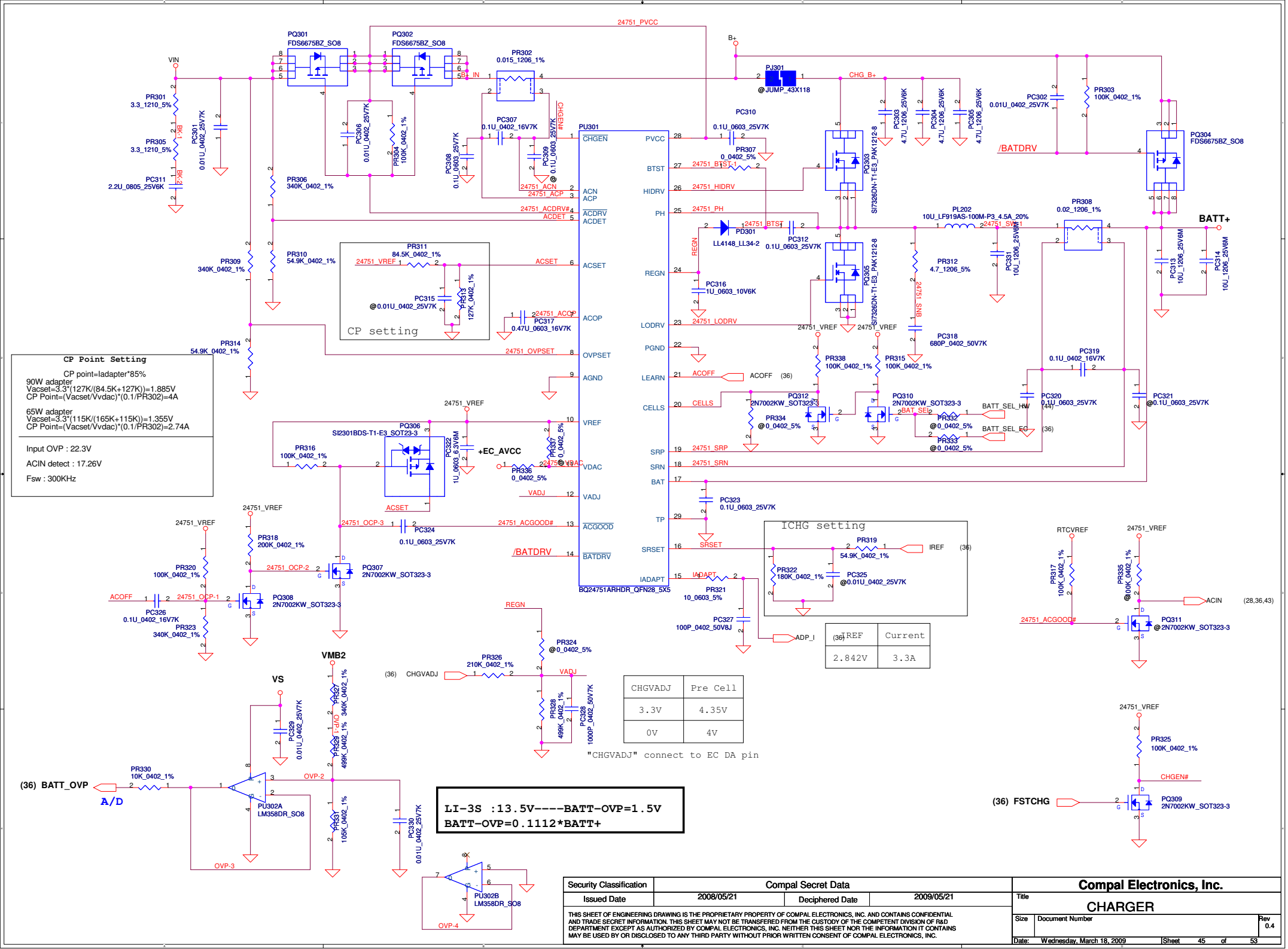
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 44 of 53


CP Point Setting
CP point=ladapter*85%
90W adapter
Vacset=3.3*(127K/(84.5K+127K))=1.885V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=4A
65W adapter
Vacset=3.3*(115K/(165K+115K))=1.355V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=2.74A
Input OVP : 22.3V
ACIN detect : 17.26V
Fsw : 300KHz
CP setting
ICHG setting
IREF Current
2.842V 3.3A
CHGVADJ Pre Cell
3.3V 4.35V
0V 4V
"CHGVADJ" connect to EC DA pin
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+
BQ24751ARHDR_QFN28_5X5
PU301
PQ301 FDS6675BZ_SO8
PQ302 FDS6675BZ_SO8
PQ303 SI7326DN-T1-E3_PAK1212-8
PQ304 FDS6675BZ_SO8
PQ305 SI7326DN-T1-E3_PAK1212-8
PQ306 SI2301BDS-T1-E3_SOT23-3
PQ307 2N7002KW_SOT323-3
PQ308 2N7002KW_SOT323-3
PQ309 2N7002KW_SOT323-3
PQ310 2N7002KW_SOT323-3
PQ311 @2N7002KW_SOT323-3
PU302A LM358DR_SO8
PU302B LM358DR_SO8
PD301 LL4148_LL34-2
PJ301 @JUMP_43X118
PL202 10U_LF919AS-100M-P3_4.5A_20%
VIN
B+
BATT+
24751_PVCC
CHG_B+
/BATDRV
VMB2
VS
(36) BATT_OVP
A/D
(36) FSTCHG
(36) CHGVADJ
ACIN (28,36,43)
RTCVREF
Security Classification Compal Secret Data
Issued Date 2008/05/21 Deciphered Date 2009/05/21
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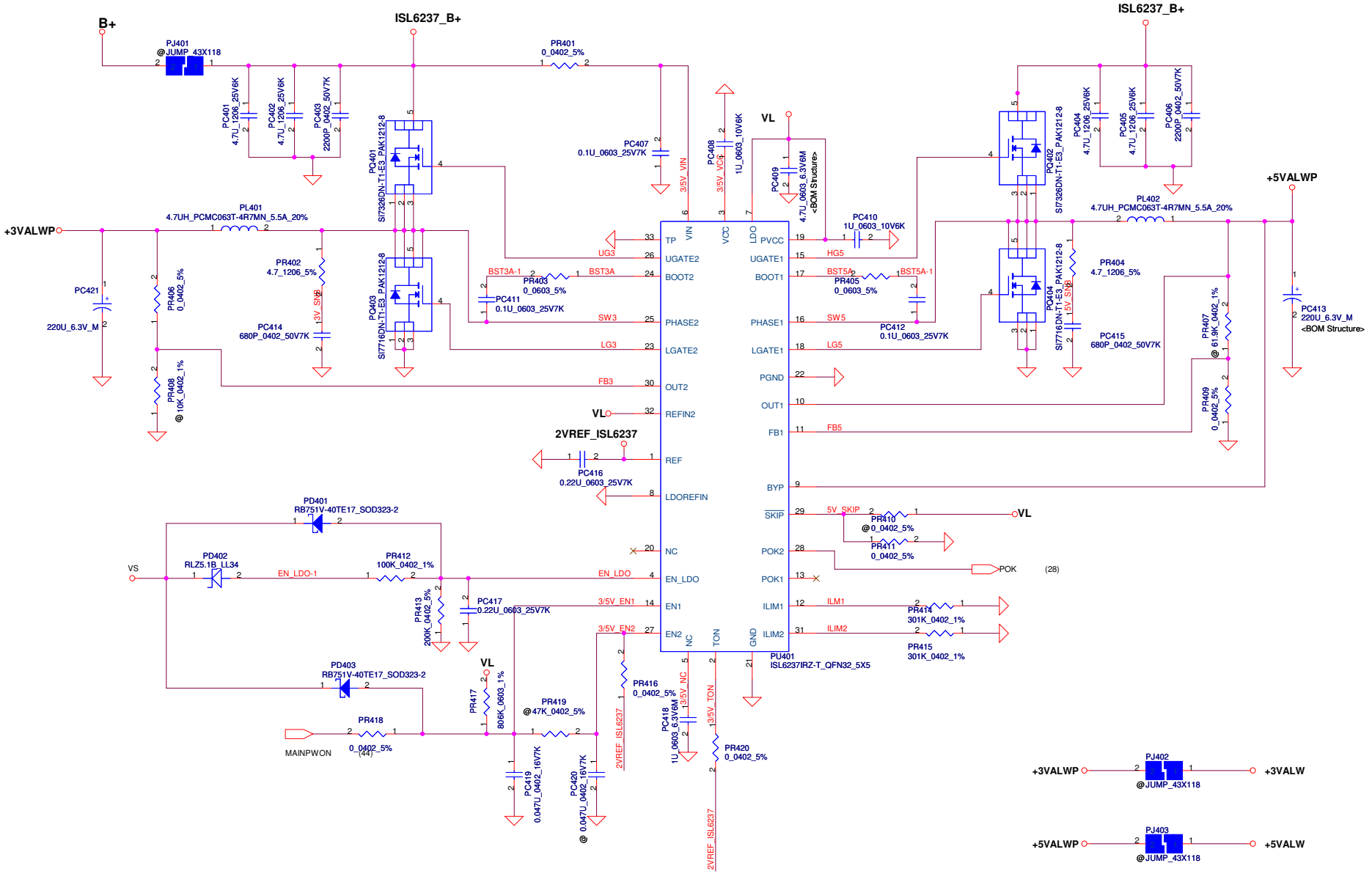
Compal Electronics, Inc.
Title CHARGER
Size Document Number Rev 0.4
Date: Wednesday, March 18, 2009 Sheet 45 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.4

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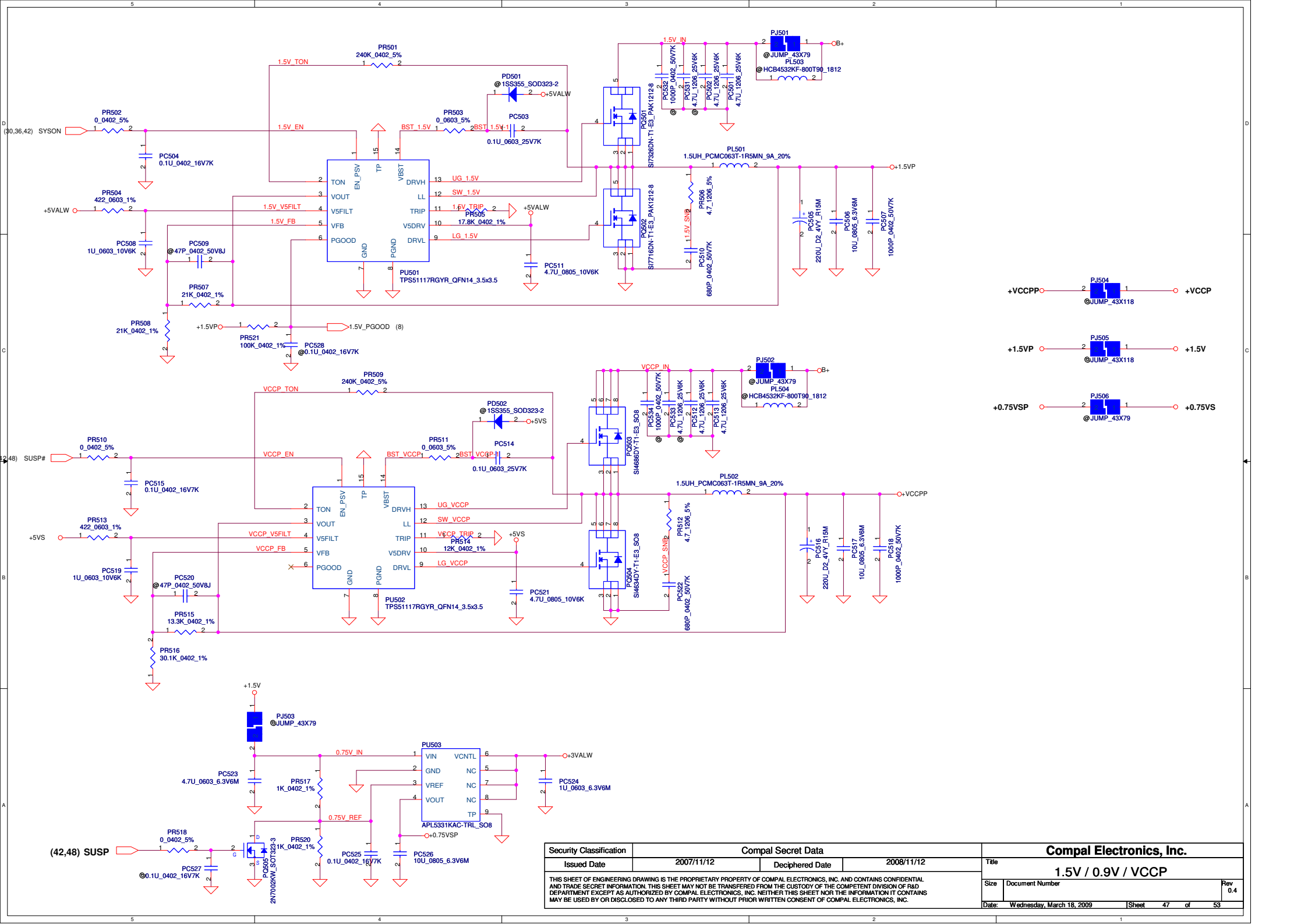


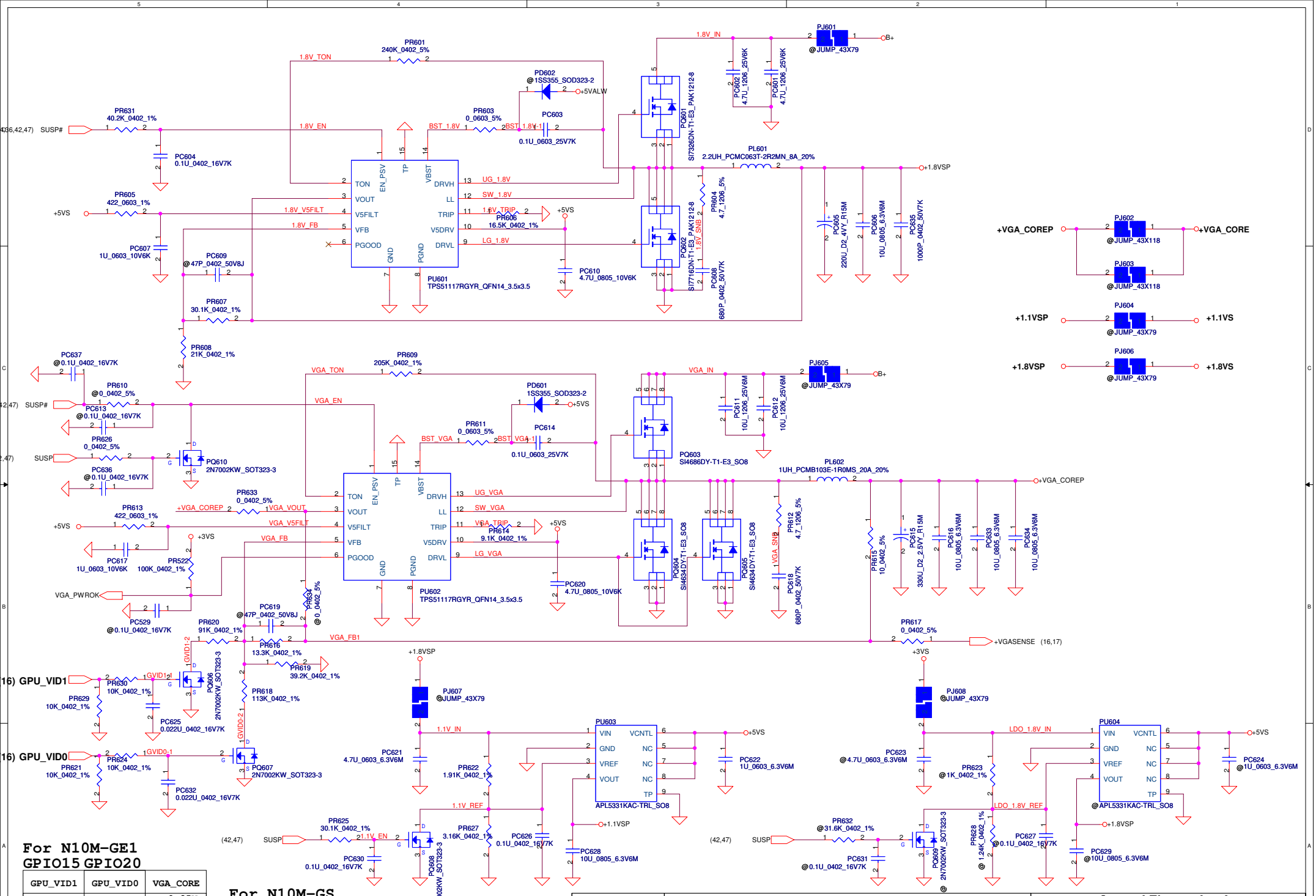
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.5V / 0.9V / VCCP

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 47 of 53



For N10M-GE1
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS

PR616=>9.09K
PR622=>2.21K
PR629,PR630,PC625,PQ606,PR620=>un-pop
PR621,PR624,PC632,PQ607,PR618=>un-pop

Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: VGA_CORE/1.8V/1.1VS

Size	Document Number	Rev
		0.4

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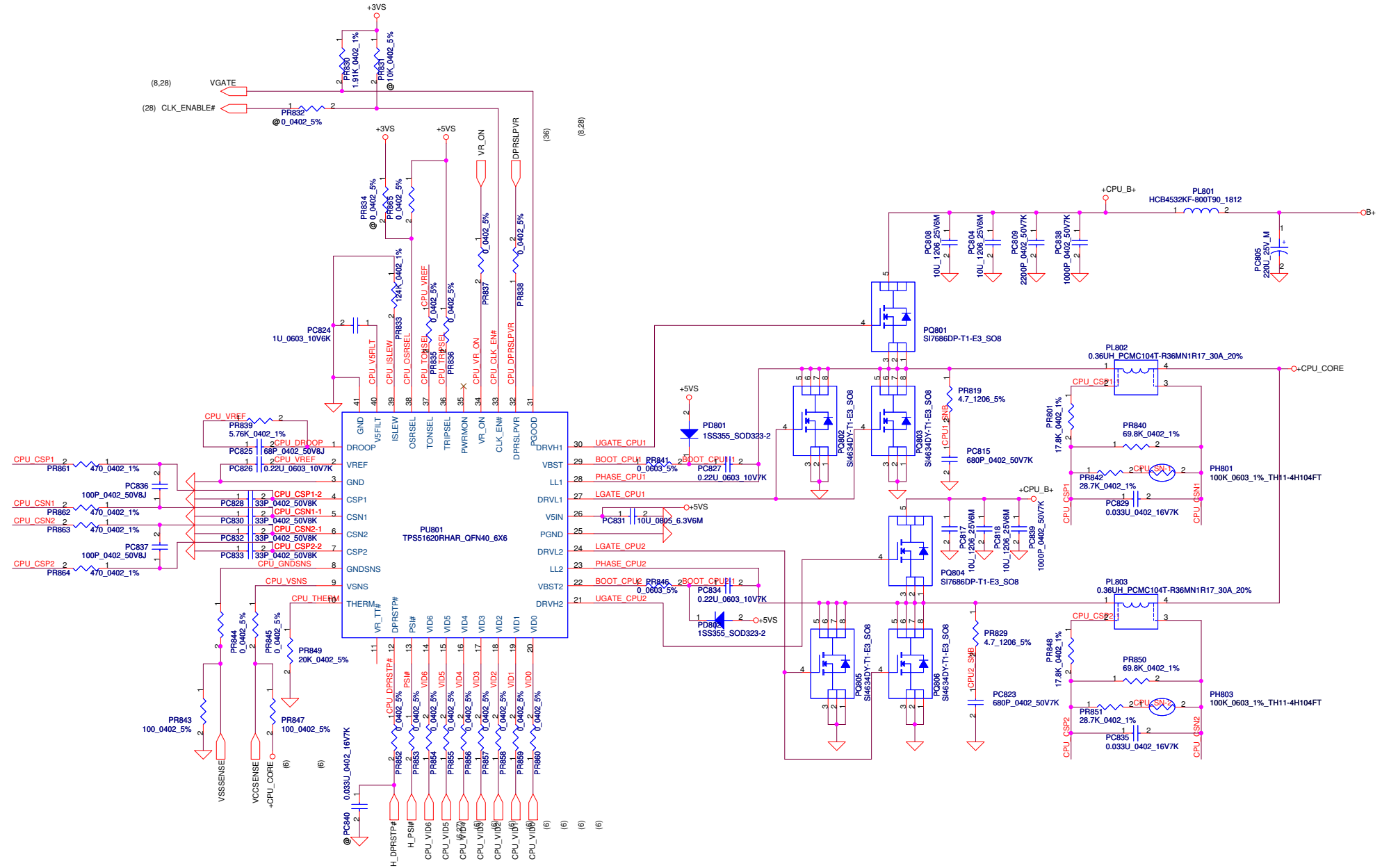

Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.4

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)		
3							
4							
5							
6							
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11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: KIWAX_LA-5082P | Rev: 0.4

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	39	Remove D11, and add R22, R25	
	12/10	36	change PWR_LED_SC# from U46.38 to U46.34	

Compal Electronics, Inc.		
Title: HW PIR		
Size: B	Document Number: KIWAX_LA-5082P	Rev: 0.4
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	39	modify H19 hold size, and change the H5、H6 and H19 hold type.	
		42	add 4 CAPs C52, C53, C54 and C55 for EMI.	
		35	change C572 and C574 footprint from 0603 to 0402.	
		34	add R44 for BEEP# test	
2	1/16	30	Remove one Mini-PCIE function! (Connector Side) Remove component is JP18, R363, R364, R367, R369, R371, R373, R375, R377, R378, R379, R380 and R383 Remove 3G function! Remove component is JP14, D12, R6, C6, C7, R7 and D13	
		28	Remove one Mini-PCIE function!(SB side) Remove component is C884 and C885	

Compal Electronics, Inc.		
Title: HW PIR		
Size: B	Document Number: KIWAX_LA-5082P	Rev: 0.4
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/16	06	add R1089, C1162 and H_DPRSTP#_R	
			add C1163, C1164,and C1165 for EMC request.	
		08	change H_DPRSTP# to H_DPRSTP#_R	
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU	
			R999 change to 24.9K	
		23	add R1095 pull high	
		35	swap HP_OUTL and HP_OUTR	
		36	add R1090, R1091, R1092, R1093	
			CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R	
		41	add R256, R258 Bom configuration	
			Remove CY SMBus	
		42	add C1166, C1167 for EMC request.	
2	3/16	28	change PCIE Port1 to Port3	
		30	change PCIE Port1 to Port3	

Compal Electronics, Inc.		
Title: HW PIR		
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