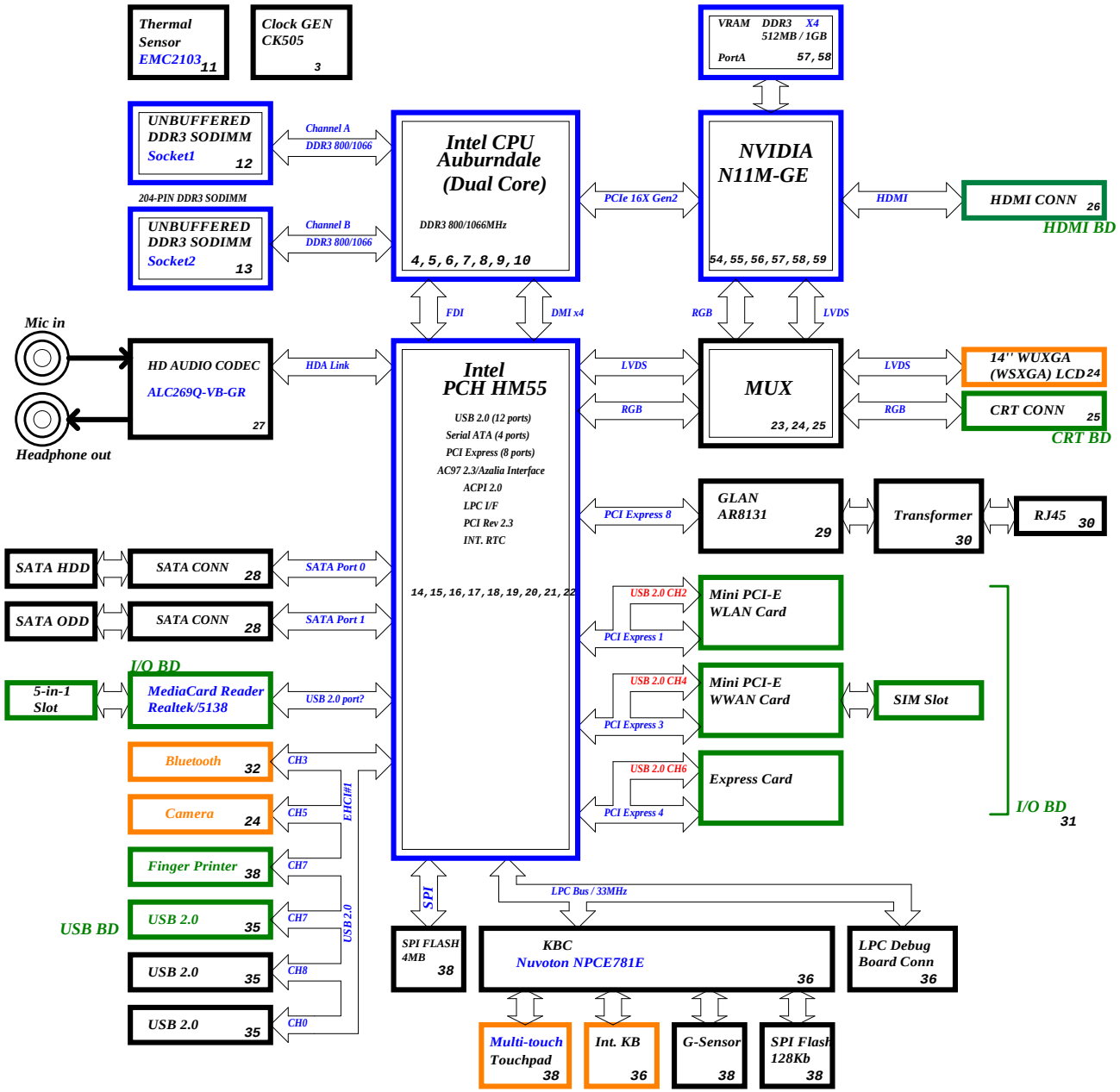
LA46 Switchable Graphics System Schematics

Project Code: 91.4GV01.001
PCB(Raw Card): 09911-1



- USB BD
- I/O BD
- CRT BD
- Power BD
- Finger Printer BD
- HDMI BD
- BT BD
- AV BD

PCB LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Signal

CPU DC/DC ISL62882 38,39

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123 40

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 41

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E 41

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E 42

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025 43

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026 43

INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 44

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC ISL62872 45

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER BQ24745 46

INPUTS	OUTPUTS
DCBATOUT	BT+

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: 01 Block Diagram

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

Date: Wednesday, January 27, 2010 Sheet 1 of 58

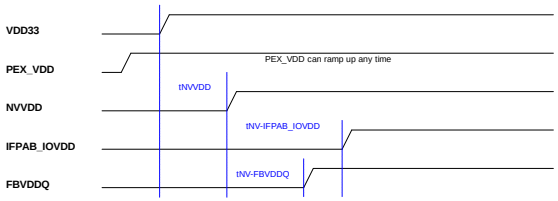
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

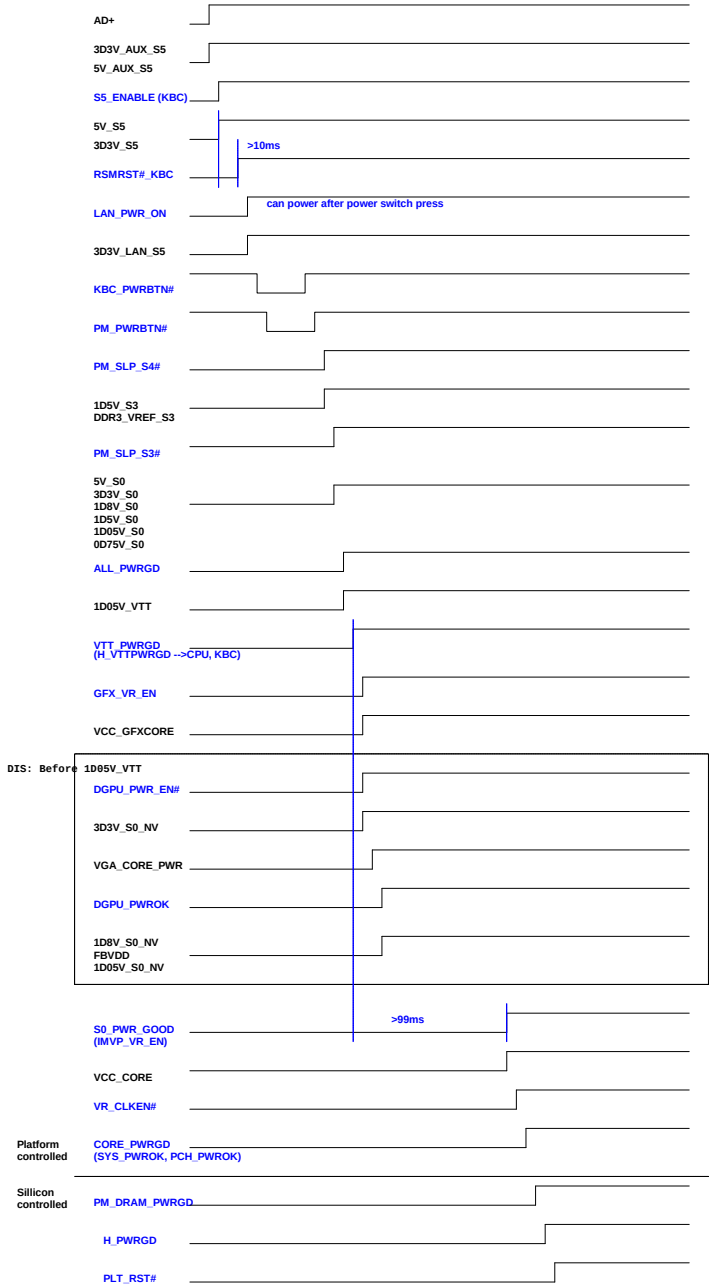
PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence

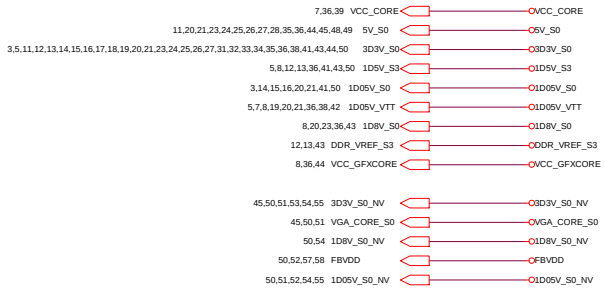


Sequence AC



PLANAR_ID[1..0]

KBC GPIn	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0		
	0	0	LA46 - SA	SA
	0	1	LA46 - SB	SB
	1	0	LA46 - SB	SC
	1	1		-1



<Core Design>

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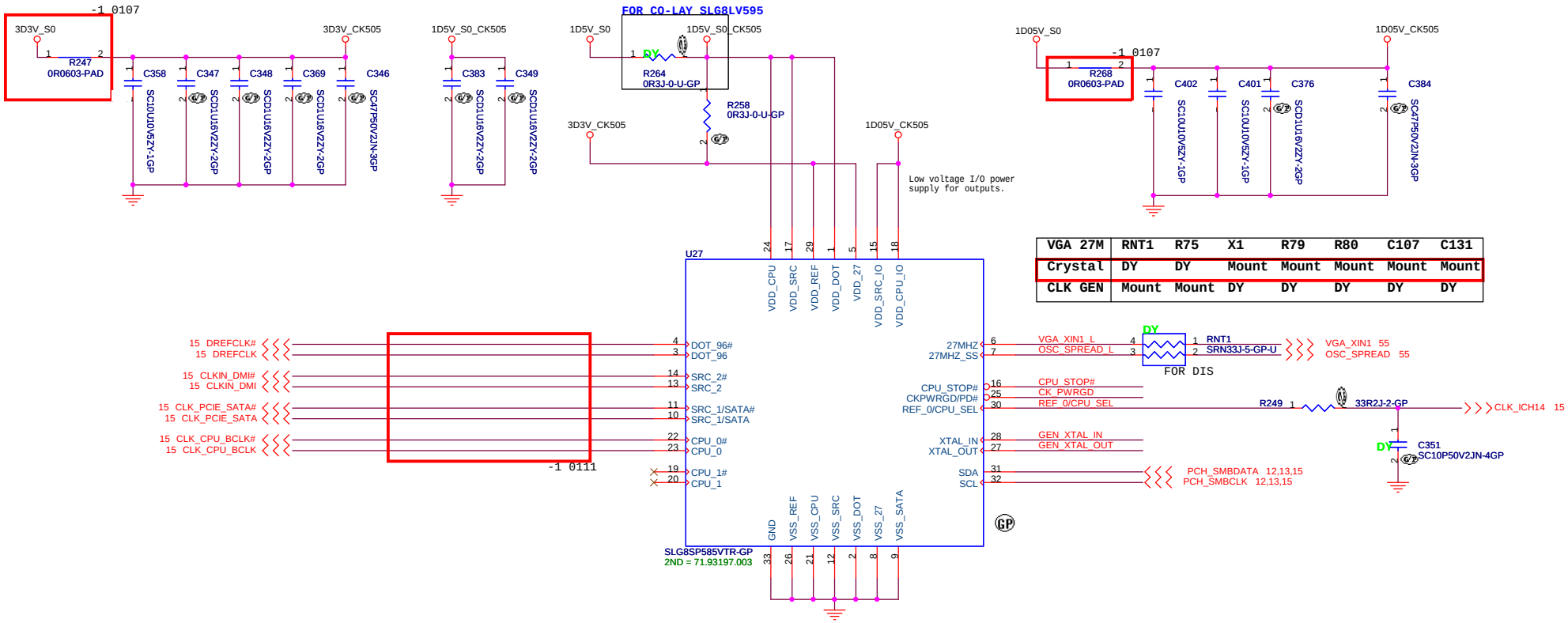
Taipei Hsien 221, Taiwan, R.O.C

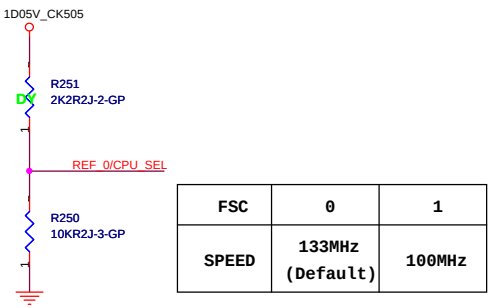
Title: 02_Reference

Size	Document Number	Rev
A2	LA46 MB	-1

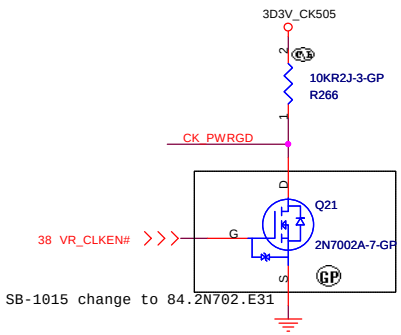
Date: Wednesday, January 27, 2010 Sheet 2 of 58



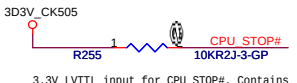
VGA 27M	RNT1	R75	X1	R79	R80	C107	C131
Crystal	DY	DY	Mount	Mount	Mount	Mount	Mount
CLK GEN	Mount	Mount	DY	DY	DY	DY	DY



FSC	0	1
SPEED	133MHz (Default)	100MHz

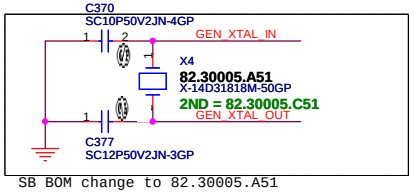


SB-1015 change to 84.2N702.E31



3.3V LVTTL input for CPU_STOP#. Contains internal pull-up resistor.

CL=20pF±0.2pF



SB BOM change to 82.30005.A51

Layout Notes:

Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.

<Core Design>

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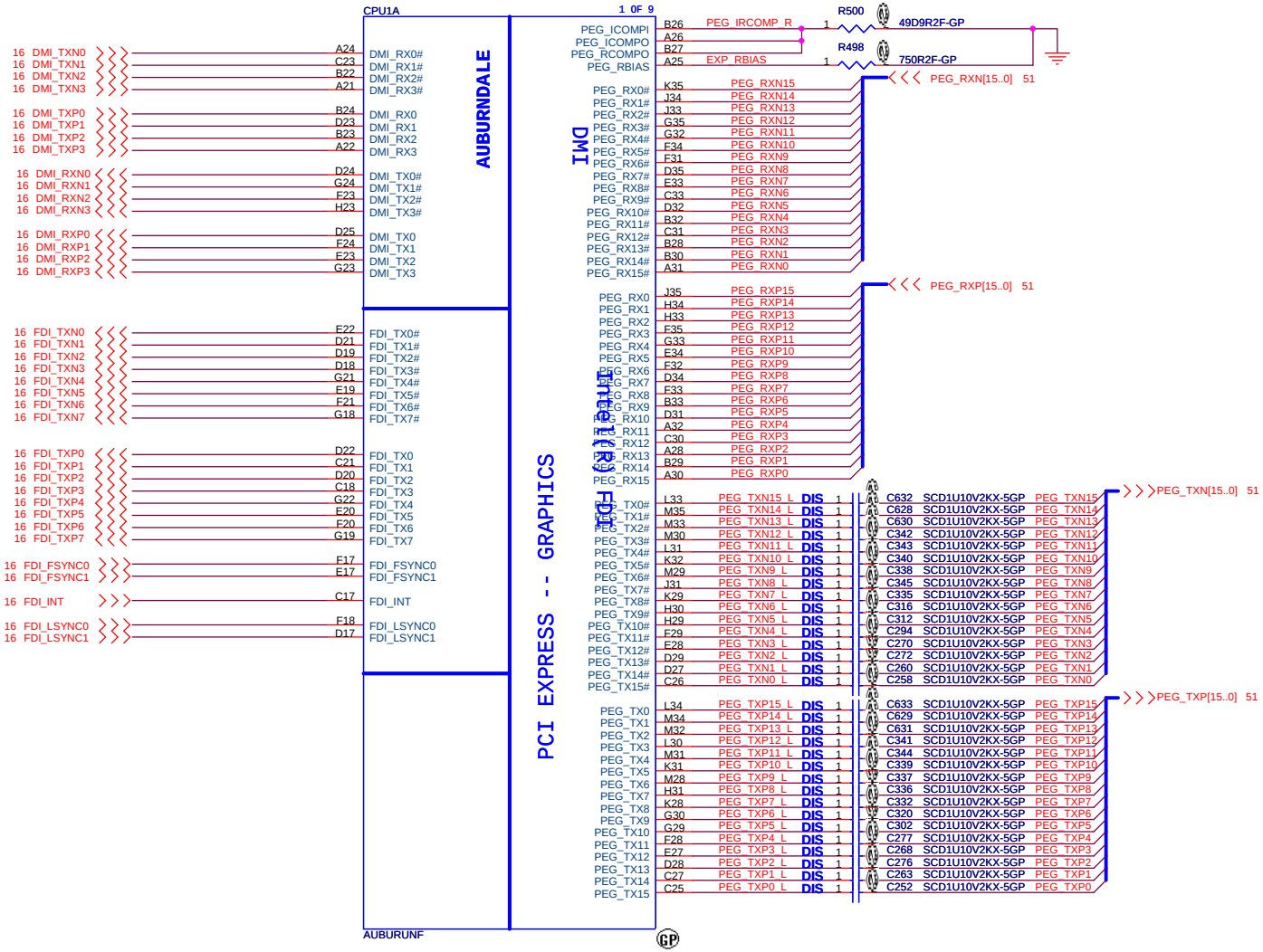
Title: 03_Clock Generator SLG8SP585

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 3 of 58



<Core Design>

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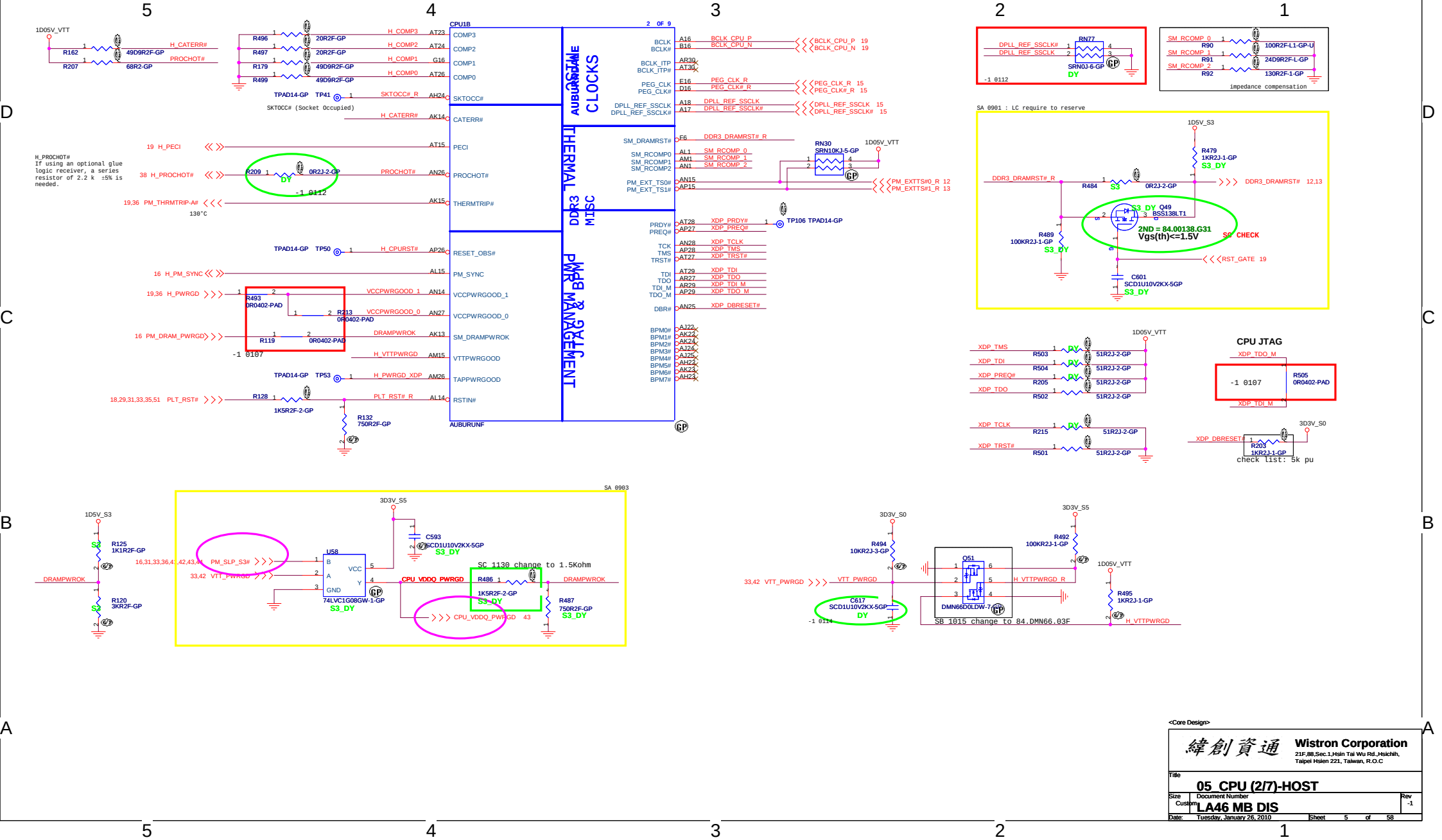
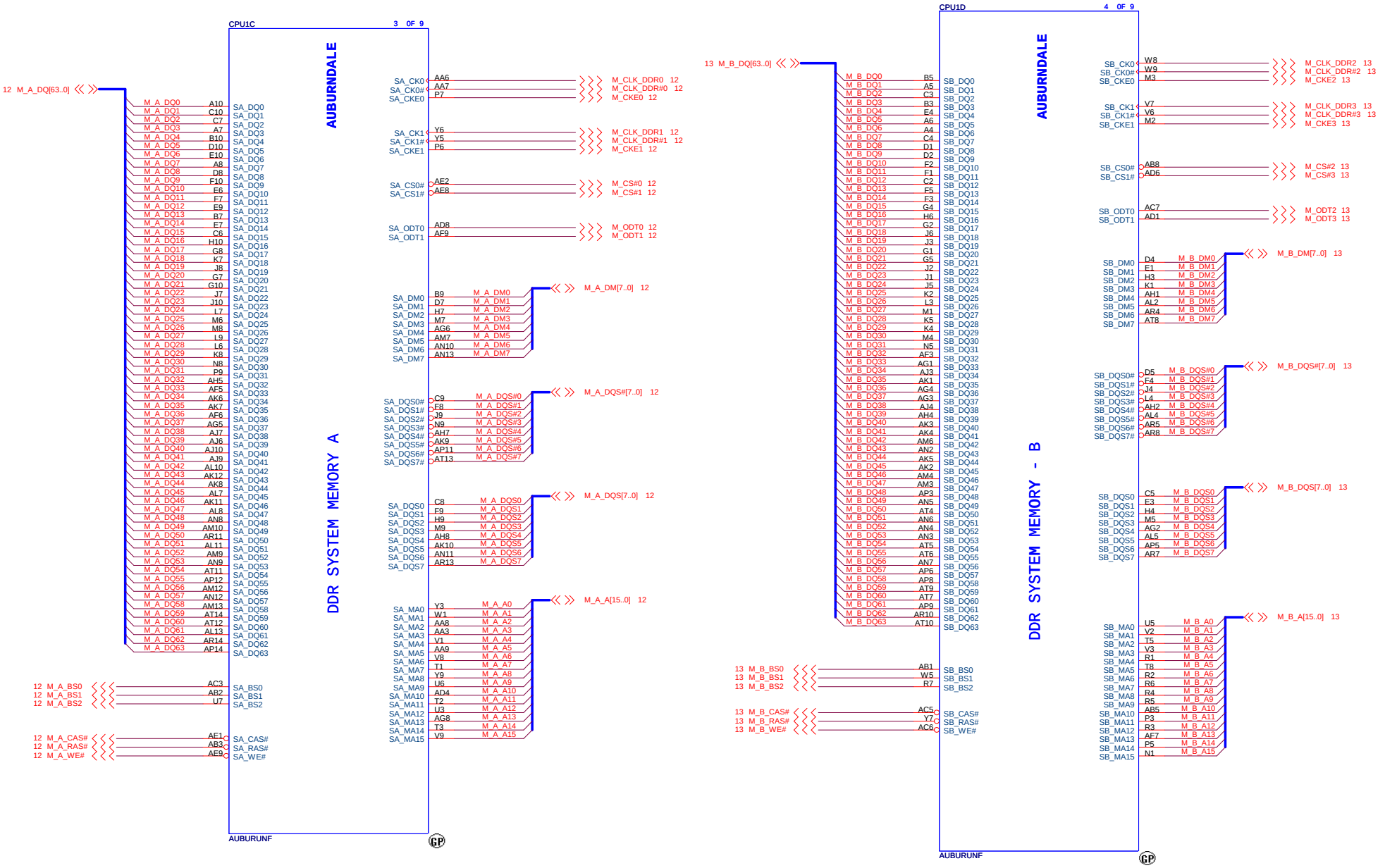
Title
04_CPU (1/7)-PEG / DMI / FDI

Size	Document Number	Rev
A3	LA46 MB DIS	-1

Date: Tuesday, January 26, 2010 Sheet 4 of 58


CPU1B
2 OF 9
AUBURNFME
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
AUBURUNF
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
SA 0901 : LC require to reserve
2ND = 84.00138.G31
Vgs(th)<=1.5V
SG CHECK
CPU JTAG
check list: 5k pu
SA 0903
SC 1130 change to 1.5Kohm
SB 1015 change to 84.DMN66.03F
<Core Design>
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
05_CPU (2/7)-HOST
Size
Custom
Document Number
LA46 MB DIS
Rev
-1
Date: Tuesday, January 26, 2010
Sheet 5 of 58



<Core Design>

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Title: 06_CPU (3/7)-MEM INTERFACE

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

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PROCESSOR CORE POWER

48A -->Arrandale

CPU1F

6 OF 9

AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

SENSE LINES

POWER

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

AUBURUNF

VCC_CORE

C244 C235 C236 C238 C237 C239 — SC10U6D3V3MX-GP

C240 C618 C619 C620 C241 — SC10U6D3V3MX-GP

C267 C251 — SC10U6D3V3MX-GP

C242 C243 C627 C634 C635 — SC10U6D3V3MX-GP

VTT0 — AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

1D05V_VTT

C621 C616 C613 C605 C603 C604 C611 — SC10U6D3V3MX-GP

SA_0917

1D05V_VTT

C636 SCD1U10V2KX-5GP DY

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

VTT0 — AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

1D05V_VTT

C602 SC10U6D3V3MX-GP

C218 SC10U6D3V3MX-GP

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

PSI# — AN33 — PSI# 38

VID0 VID1 VID2 VID3 VID4 VID5 VID6 — AK35 AK33 AK34 AL35 AL33 AM33 AM35 — H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6 — H_VID[6..0] 38

PROC_DPRSLPVR — AM34 — PM_DPRSLPVR 38

VTT_SELECT — G15 — H_VTTVID1 — TP35 TPAD14-GP

Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

VCC_CORE

ISENSE — AN35 — IMVP_IMON 38

R238 100R2F-L1-GP-U

VCC_SENSE VSS_SENSE — AJ34 AJ35 — VCC_SENSE 38 VSS_SENSE 38

R232 100R2F-L1-GP-U

VTT_SENSE VSS_SENSE_VTT — B15 A15 — VTT_SENSE 42

SB 1019 remove test point

<Core Design>

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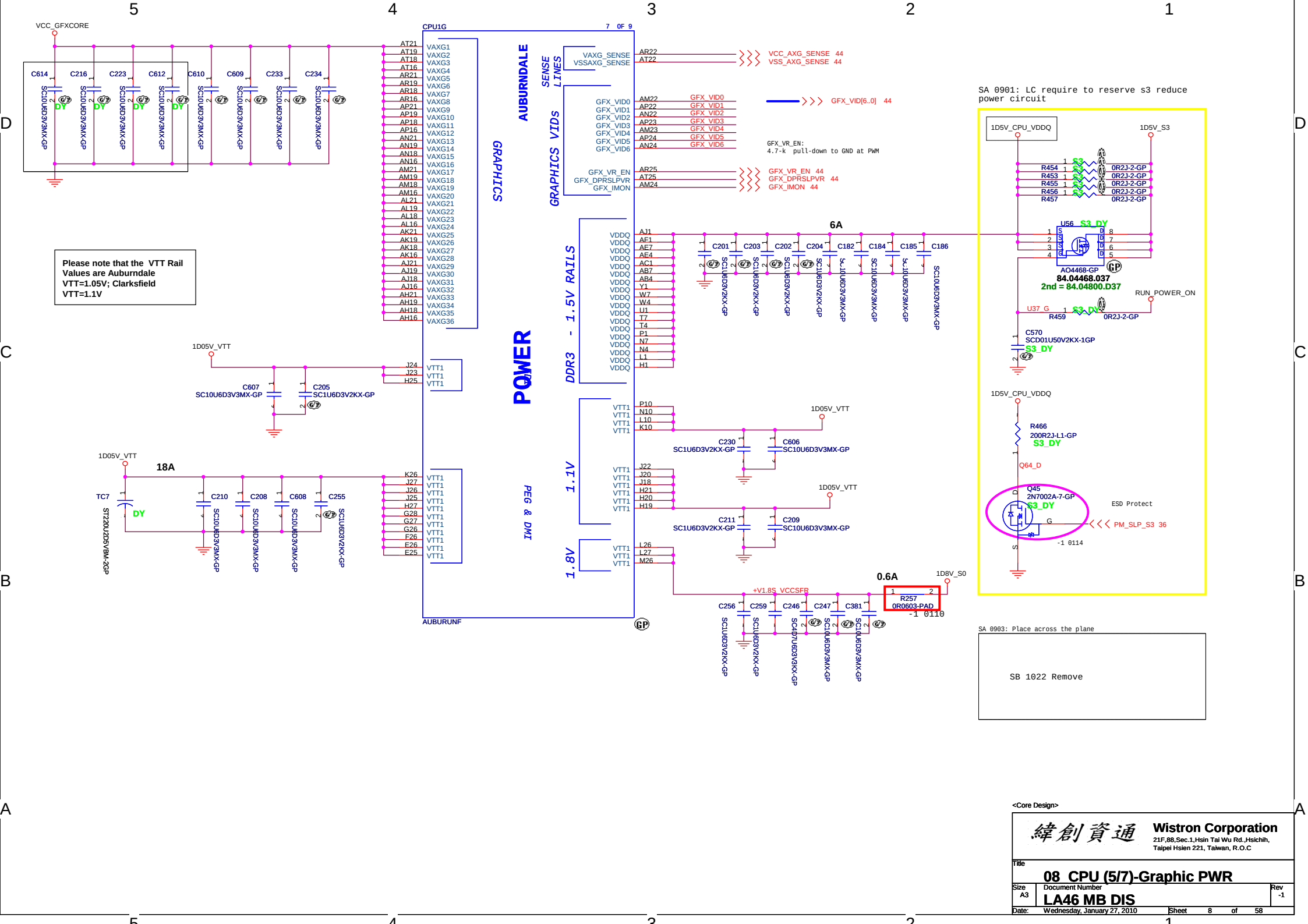
Title: 07_CPU (4/7)-POWER

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 7 of 58



<Core Design>
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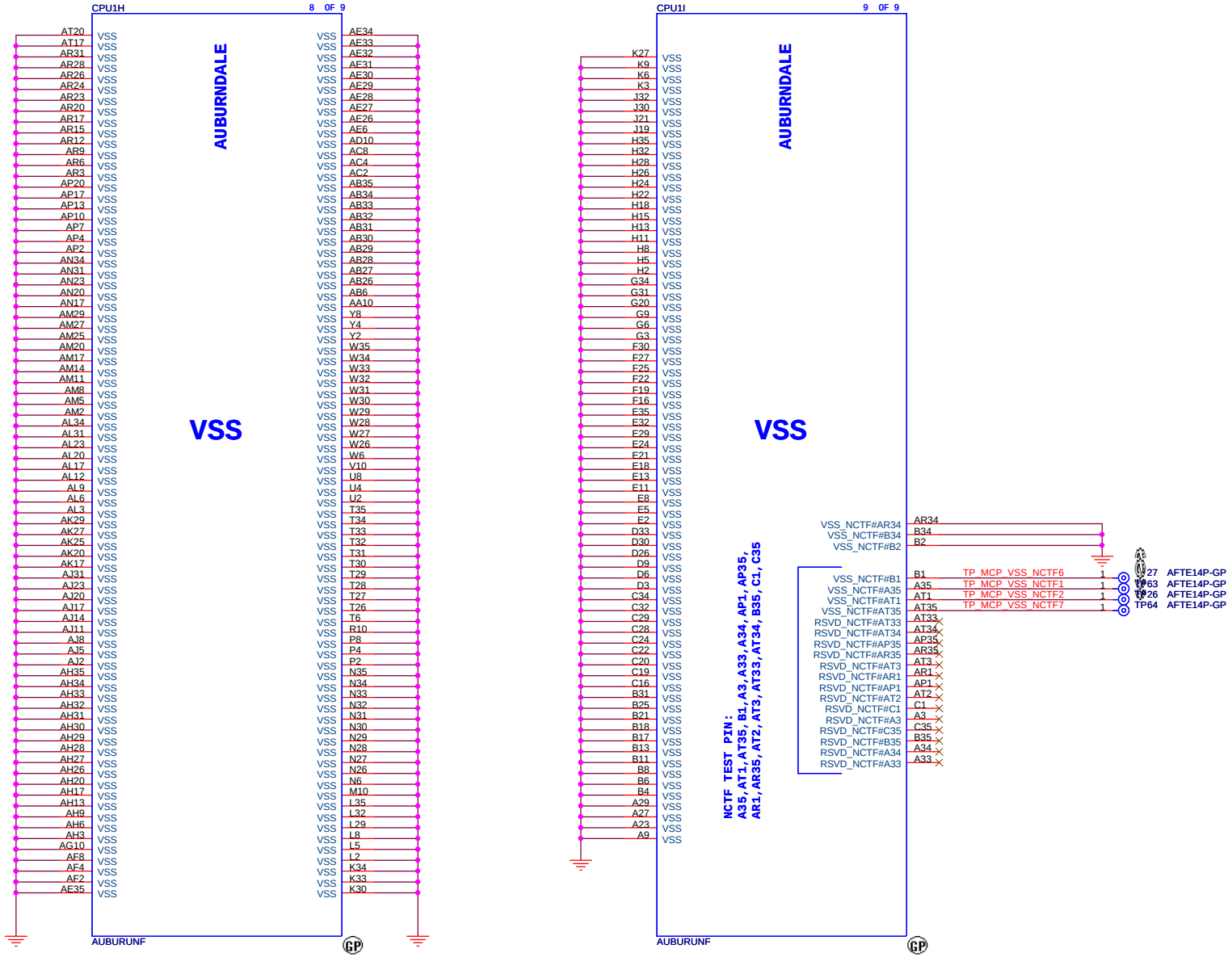
Taipei Hsien 221, Taiwan, R.O.C

Title: 08_CPU (5/7)-Graphic PWR

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 8 of 58



<Core Design>

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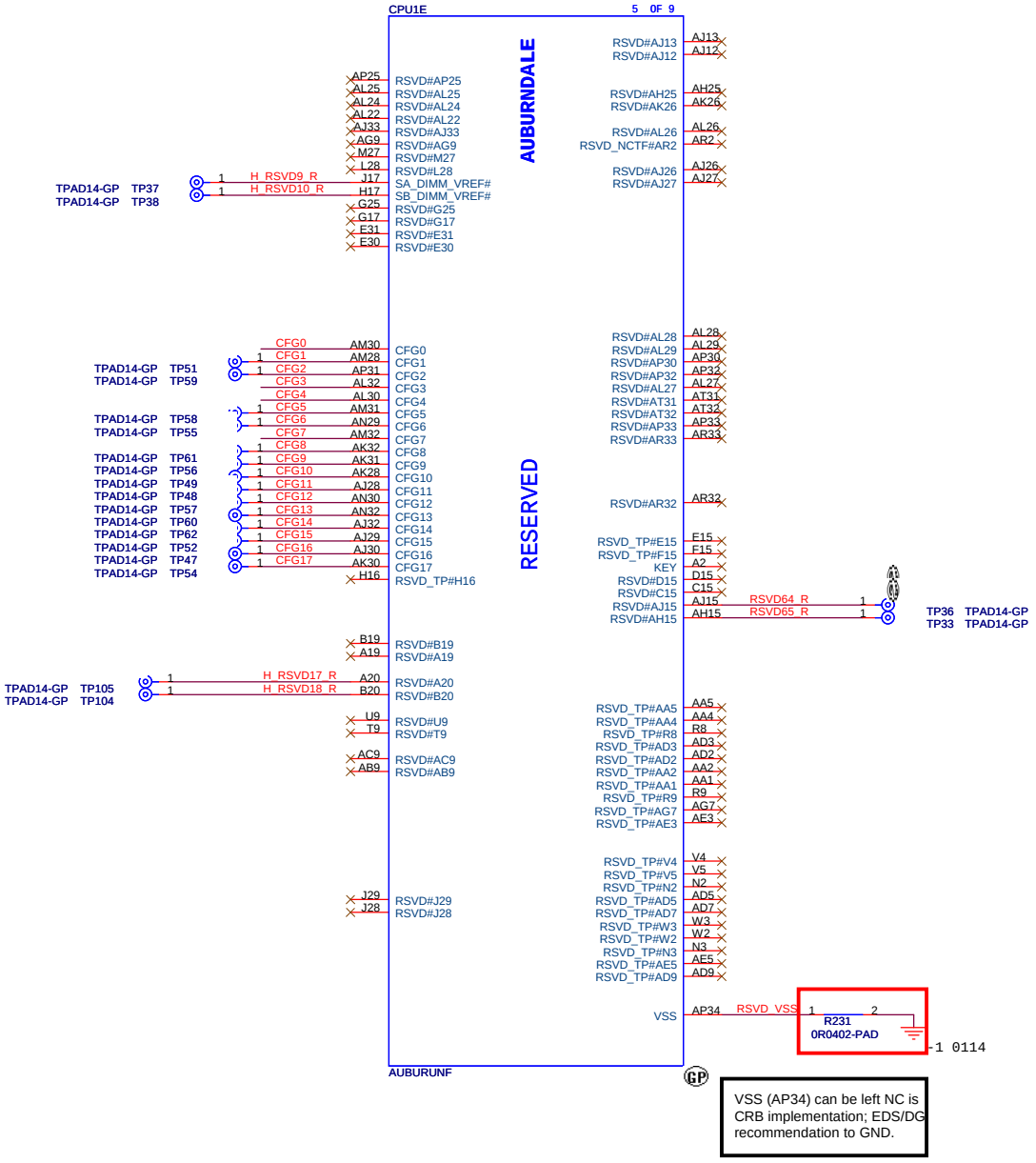
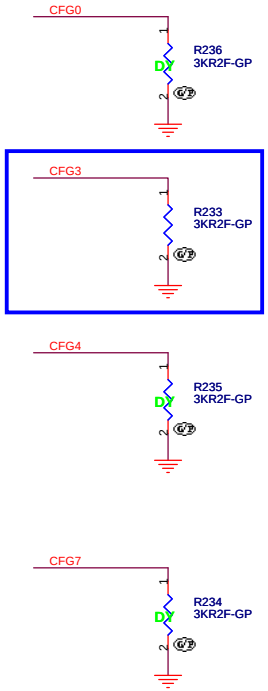
Title: 09_CPU (6/7)-VSS

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 9 of 58



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Core Design>

緯創資通 Wistron Corporation
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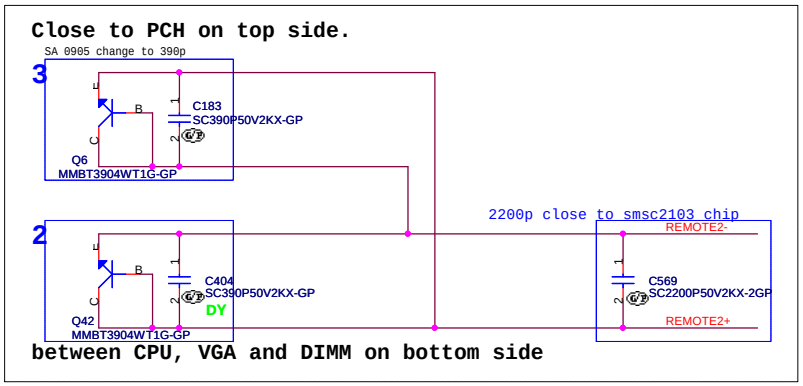
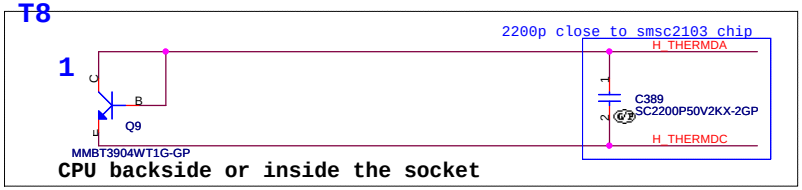
Title: 10_CPU (7/7)-RESERVED

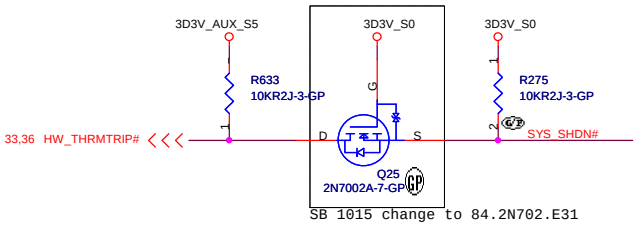
Size	Document Number	Rev
A3	LA46 MB DIS	-1

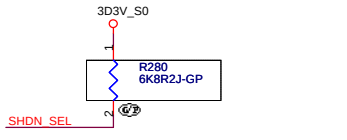
Date: Tuesday, January 26, 2010 Sheet 10 of 58



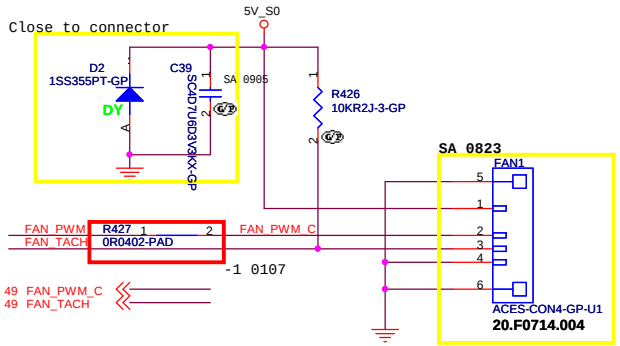


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

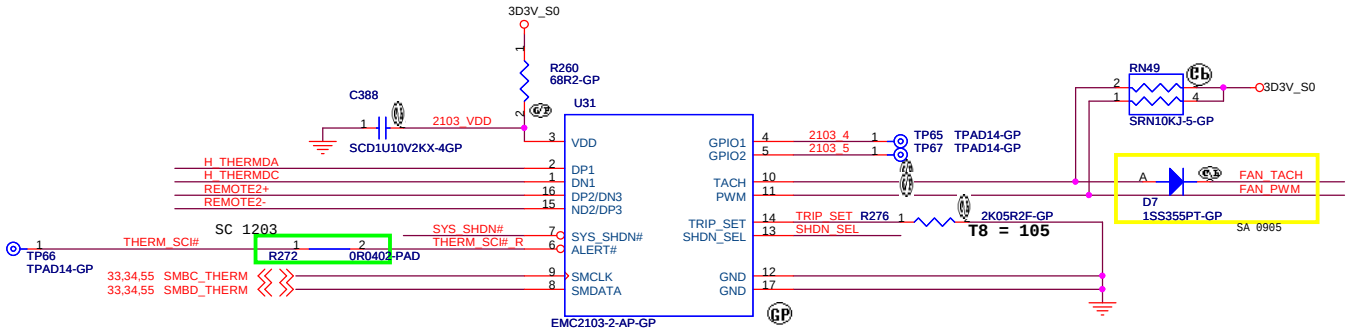




SHDN --> 2N3904 ON External diode



4 WIRE PWM Fan Control circuit



pin6, ALERT# OD
pin7, SYS_SHDN# OD

<Core Design>
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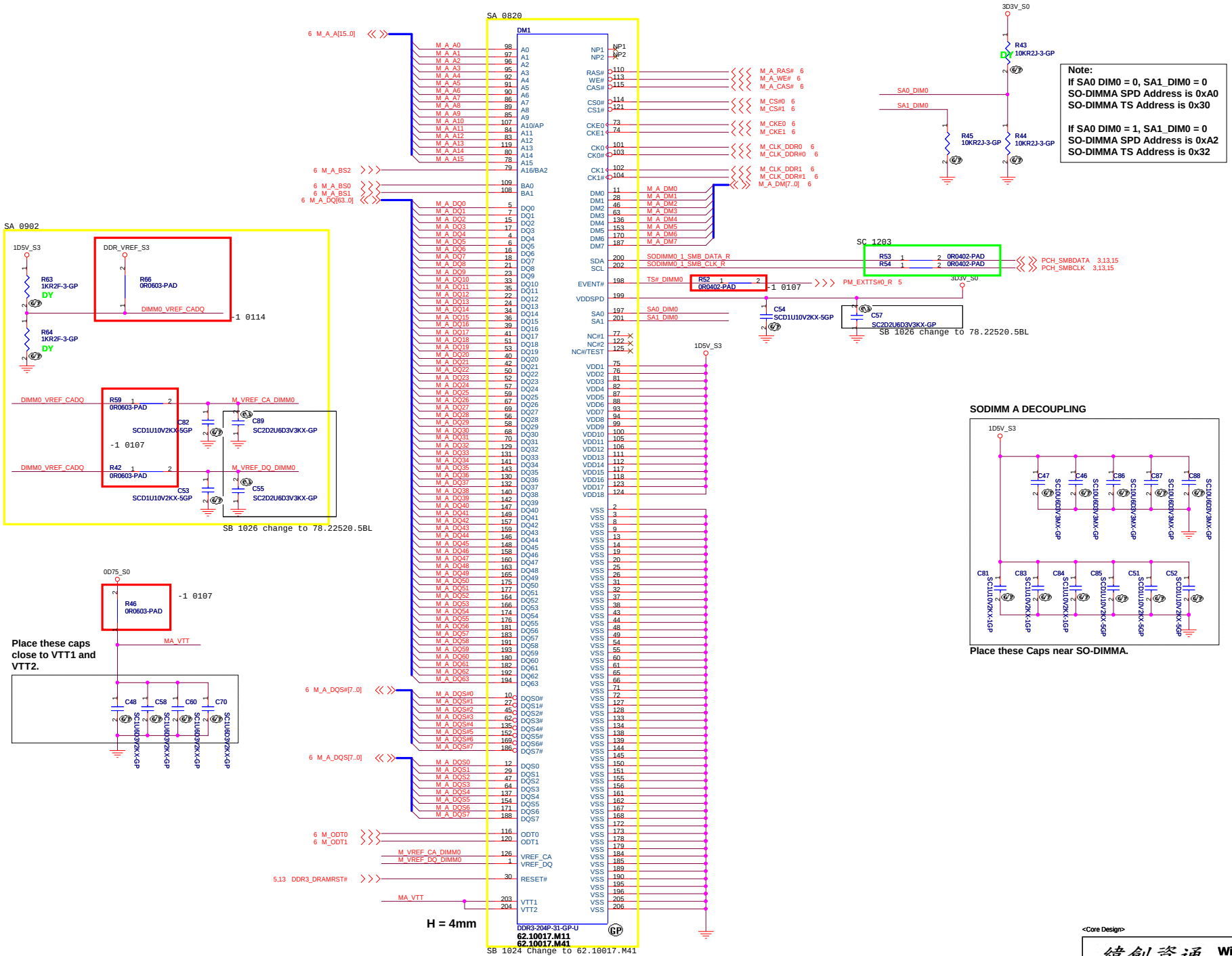
Title: 11 THERMAL SMSC2103

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 11 of 58



<Core Design>

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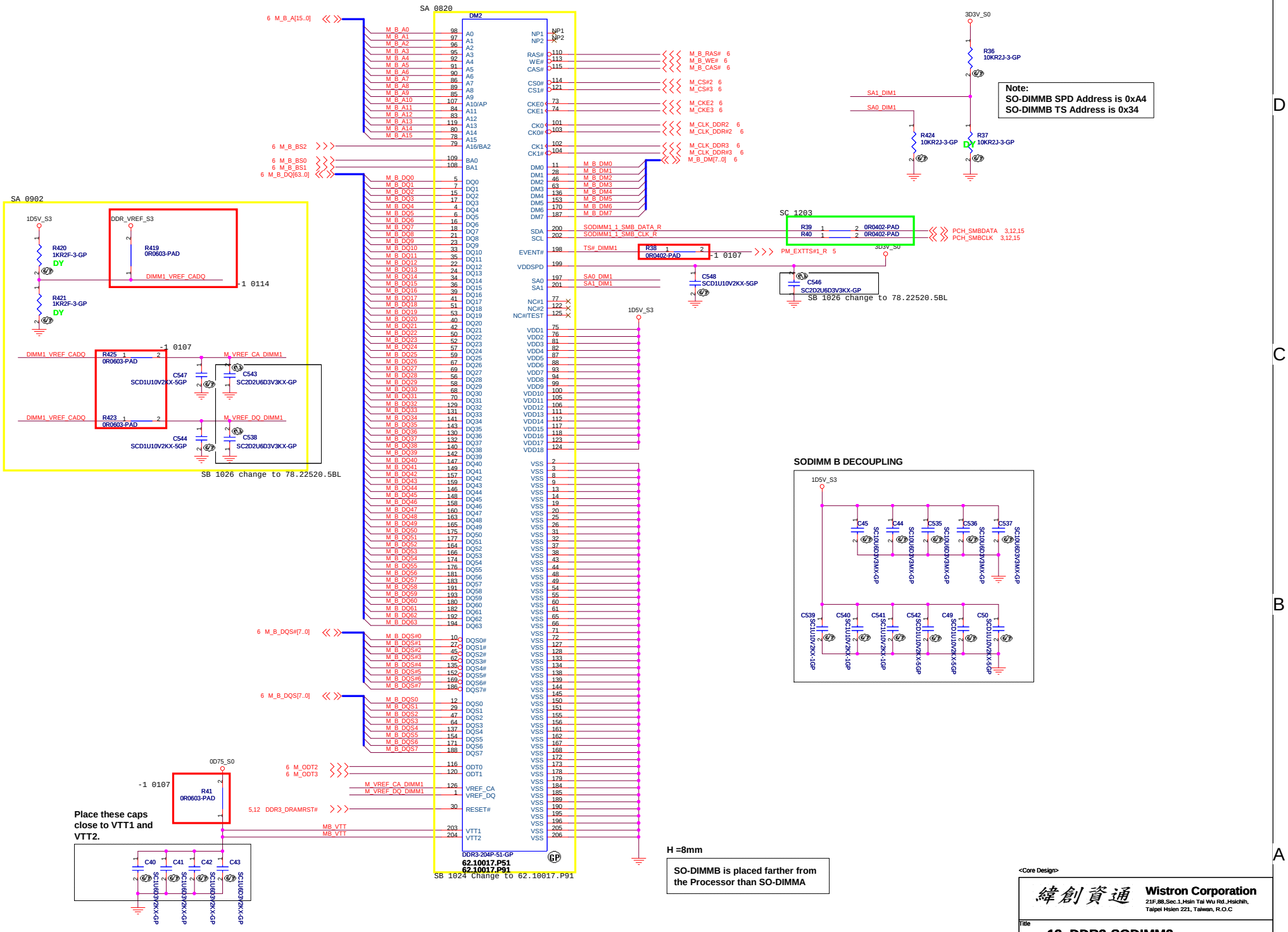
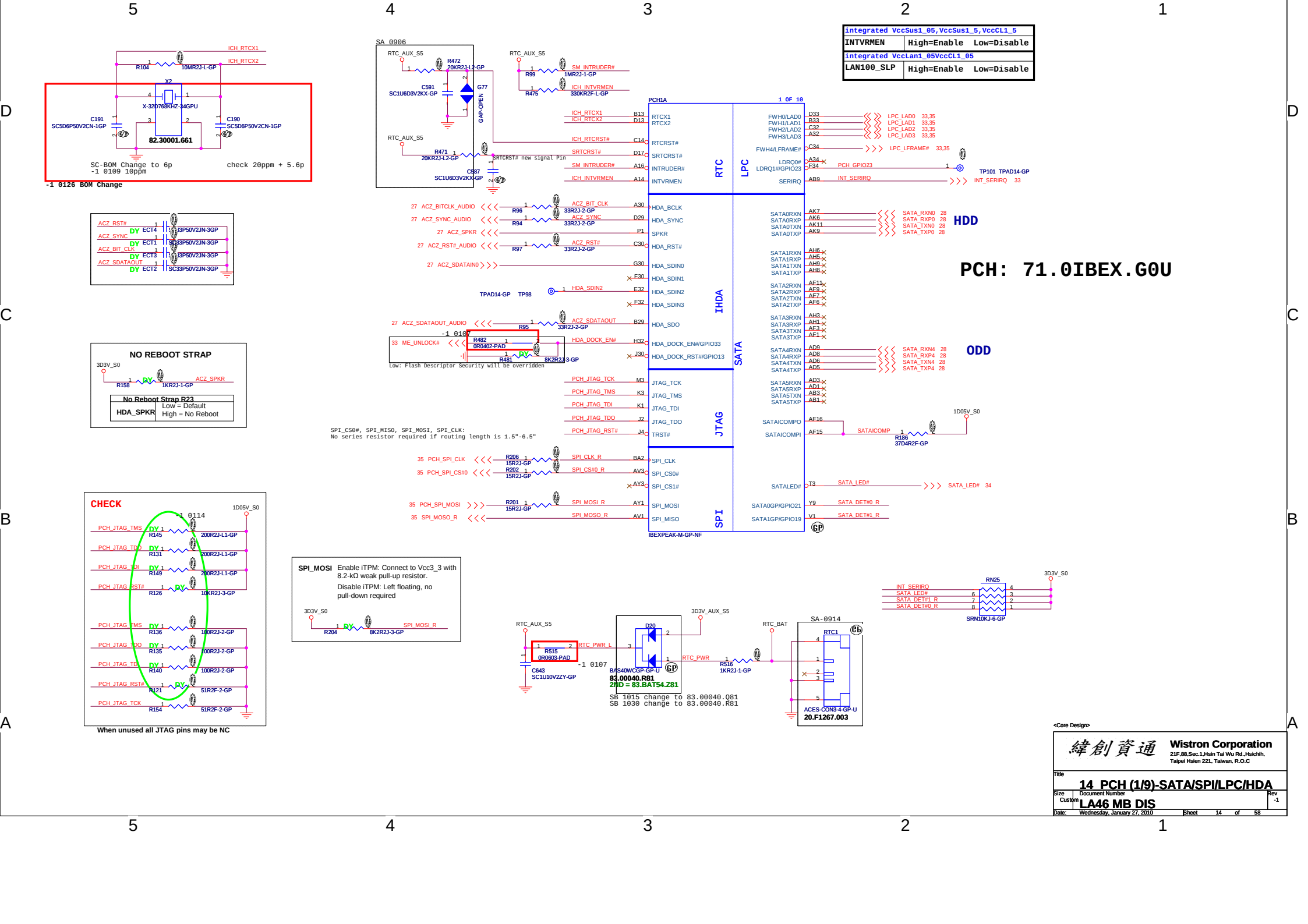
Taipei Hsien 221, Taiwan, R.O.C

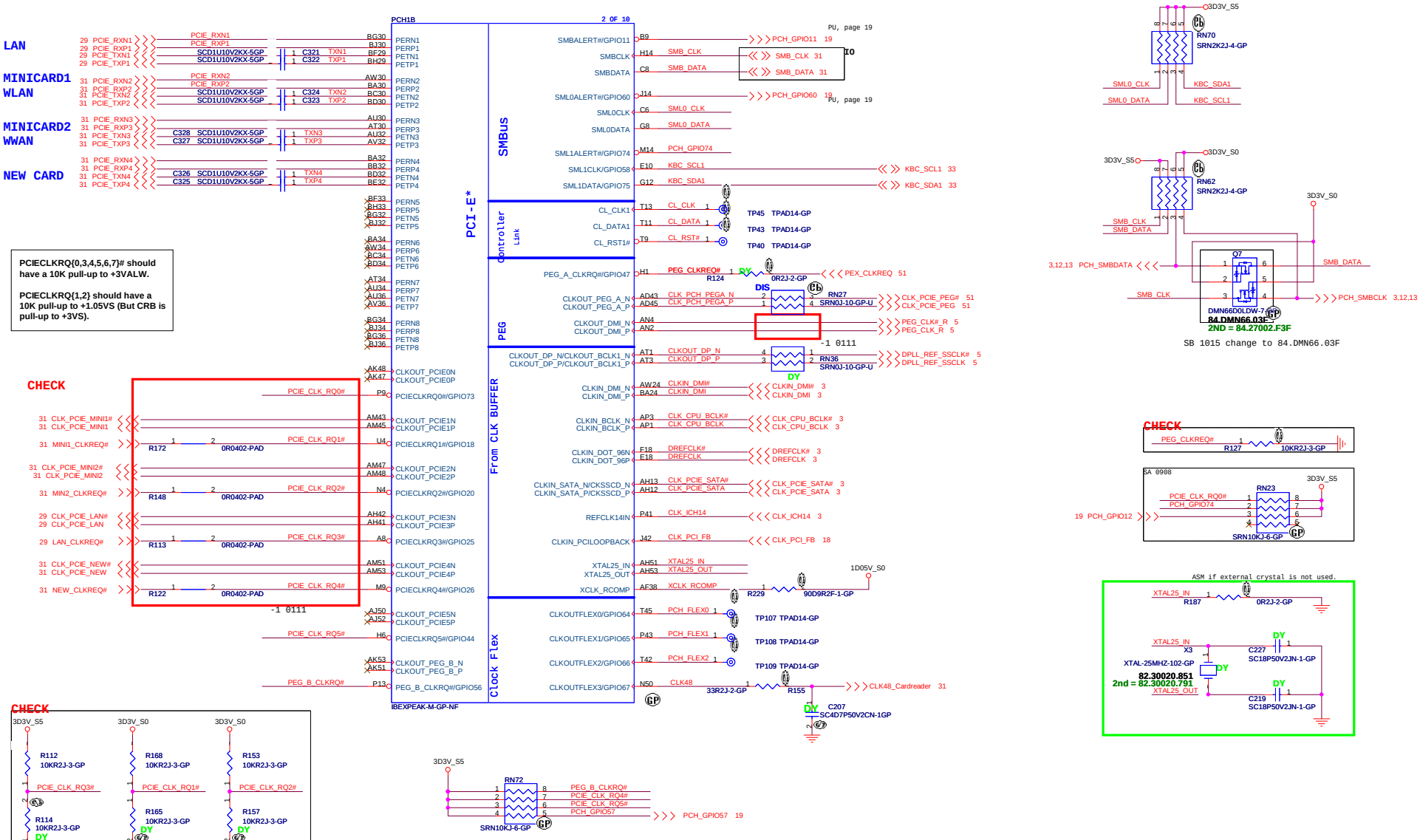
Title: 12_DDR3-SODIMM1

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 12 of 58


SA 0820
DM2
SA 0902
SC 1203
SODIMM B DECOUPLING
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
Place these caps close to VTT1 and VTT2.
H =8mm
SO-DIMMB is placed farther from the Processor than SO-DIMMA
SB 1026 change to 78.22520.5BL
SB 1024 Change to 62.10017.P91
DDR3-204P-51-GP
62.10017.P51
62.10017.P91
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
13_DDR3-SODIMM2
LA46 MB DIS
Wednesday, January 27, 2010


integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
ICH_RTCX1
ICH_RTCX2
R104 10MR2J-L-GP
X2
X-32D768KHZ-34GPU
C191 SC5D6P50V2CN-1GP
C190 SC5D6P50V2CN-1GP
82.30001.661
SC-BOM Change to 6p
-1 0109 10ppm
check 20ppm + 5.6p
-1 0126 BOM Change
SA_0906
RTC_AUX_S5
R472 20KR2J-L2-GP
C591 SC1U6D3V2KX-GP
G77
GAP-OPEN
R471 20KR2J-L2-GP
C587 SC1U6D3V2KX-GP
SRTCRST# new signal Pin
R99 1MR2J-1-GP
R475 330KR2F-L-GP
SM_INTRUDER#
ICH_INTVRMEN
ICH_RTCRST#
SRTCRST#
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
SERIRQ
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LPC_LAD0 33,35
LPC_LAD1 33,35
LPC_LAD2 33,35
LPC_LAD3 33,35
LPC_LFRAME# 33,35
PCH_GPIO23
TP101 TPAD14-GP
INT_SERIRQ 33
ACZ_BIT_CLK
ACZ_SYNC
ACZ_SPKR
ACZ_RST#
ACZ_SDATAOUT
R96 33R2J-2-GP
R94 33R2J-2-GP
R97 33R2J-2-GP
R95 33R2J-2-GP
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO13
TPAD14-GP TP98
R482 0R0402-PAD
R481 8K2R2J-3-GP
-1 0107
Low: Flash Descriptor Security will be overridden
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_RXN0 28
SATA_RXP0 28
SATA_TXN0 28
SATA_TXP0 28
SATA_RXN4 28
SATA_RXP4 28
SATA_TXN4 28
SATA_TXP4 28
HDD
ODD
PCH: 71.0IBEX.G0U
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#
PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
SATAICOMPO
SATAICOMPI
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_LED#
SATA_DET#0_R
SATA_DET#1_R
1D05V_S0
R186 37D4R2F-GP
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
SPI_CLK_R
SPI_CS#0_R
SPI_MOSI_R
SPI_MOSO_R
R206 15R2J-GP
R202 15R2J-GP
R201 15R2J-GP
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
IBEXPEAK-M-GP-NF
ACZ_RST#
ACZ_SYNC
ACZ_BIT_CLK
ACZ_SDATAOUT
ECT4
ECT1
ECT3
ECT2
SC33P50V2JN-3GP
NO REBOOT STRAP
3D3V_S0
R158 1KR2J-1-GP
ACZ_SPKR
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
CHECK
-1 0114
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_RST#
PCH_JTAG_TCK
R145 200R2J-L1-GP
R131 200R2J-L1-GP
R149 200R2J-L1-GP
R126 10KR2J-3-GP
R136 100R2J-2-GP
R135 100R2J-2-GP
R140 100R2J-2-GP
R121 51R2F-2-GP
R154 51R2F-2-GP
When unused all JTAG pins may be NC
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
R204 8K2R2J-3-GP
SPI_MOSI_R
RTC_AUX_S5
R515 0R0603-PAD
C643 SC1U10V2ZY-GP
RTC_PWR_L
D20 BAS40WCGP-GP-U
83.00040.R81
2ND = 83.BAT54.Z81
3D3V_AUX_S5
RTC_PWR
R516 1KR2J-1-GP
RTC_BAT
SA-0914
RTC1
ACES-CON3-4-GP-U
20.F1267.003
SB 1015 change to 83.00040.Q81
SB 1030 change to 83.00040.R81
RN25
SRN10KJ-6-GP
INT_SERIRQ
SATA_LED#
SATA_DET#1_R
SATA_DET#0_R
3D3V_S0
<Core Design>
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
14_PCH (1/9)-SATA/SPI/LPC/HDA
Size Custom
Document Number
LA46 MB DIS
Rev -1
Date: Wednesday, January 27, 2010
Sheet 14 of 58

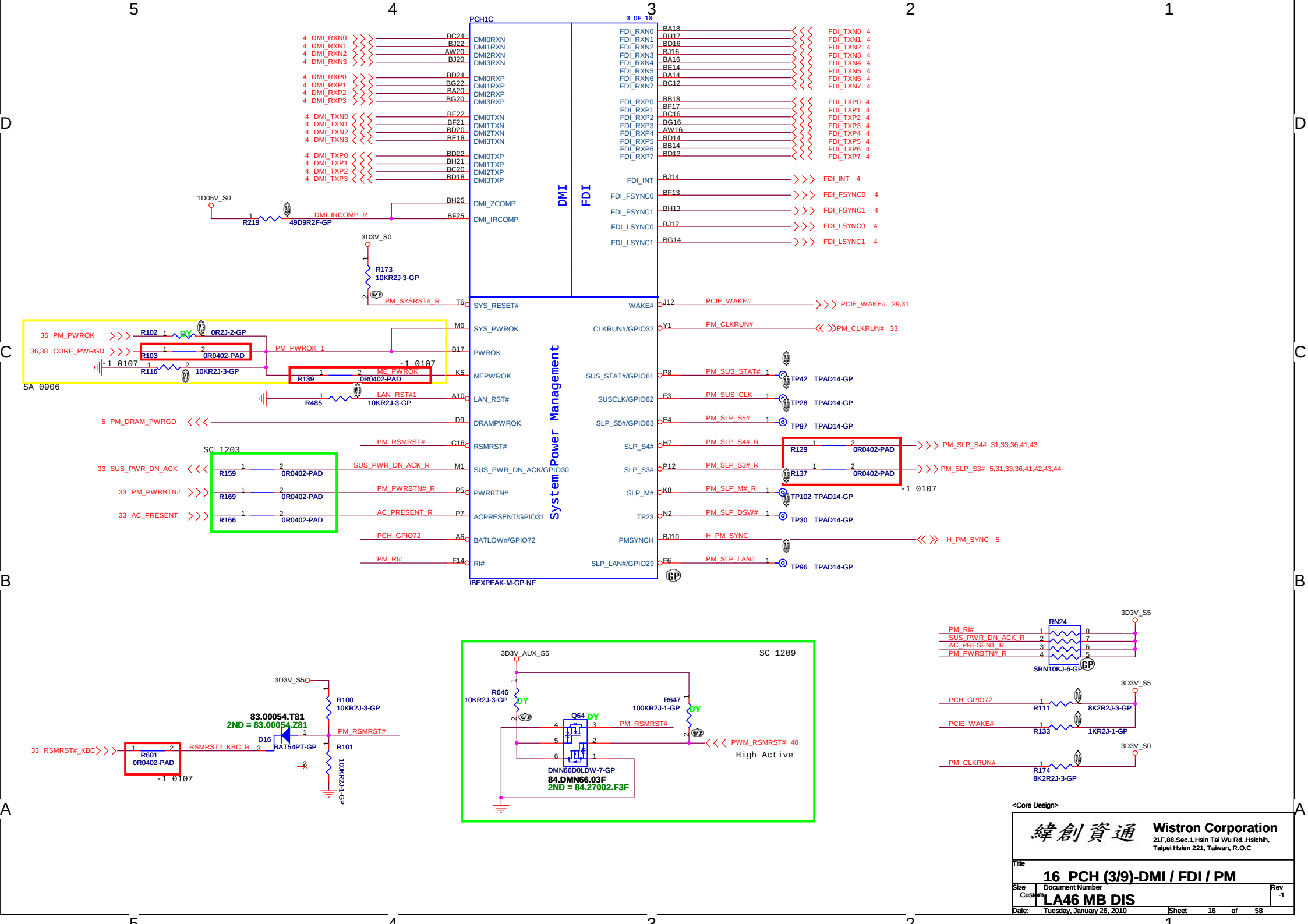


<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 15_PCH (2/9)-PCIE / SMBUS / CLK

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 15 of 58



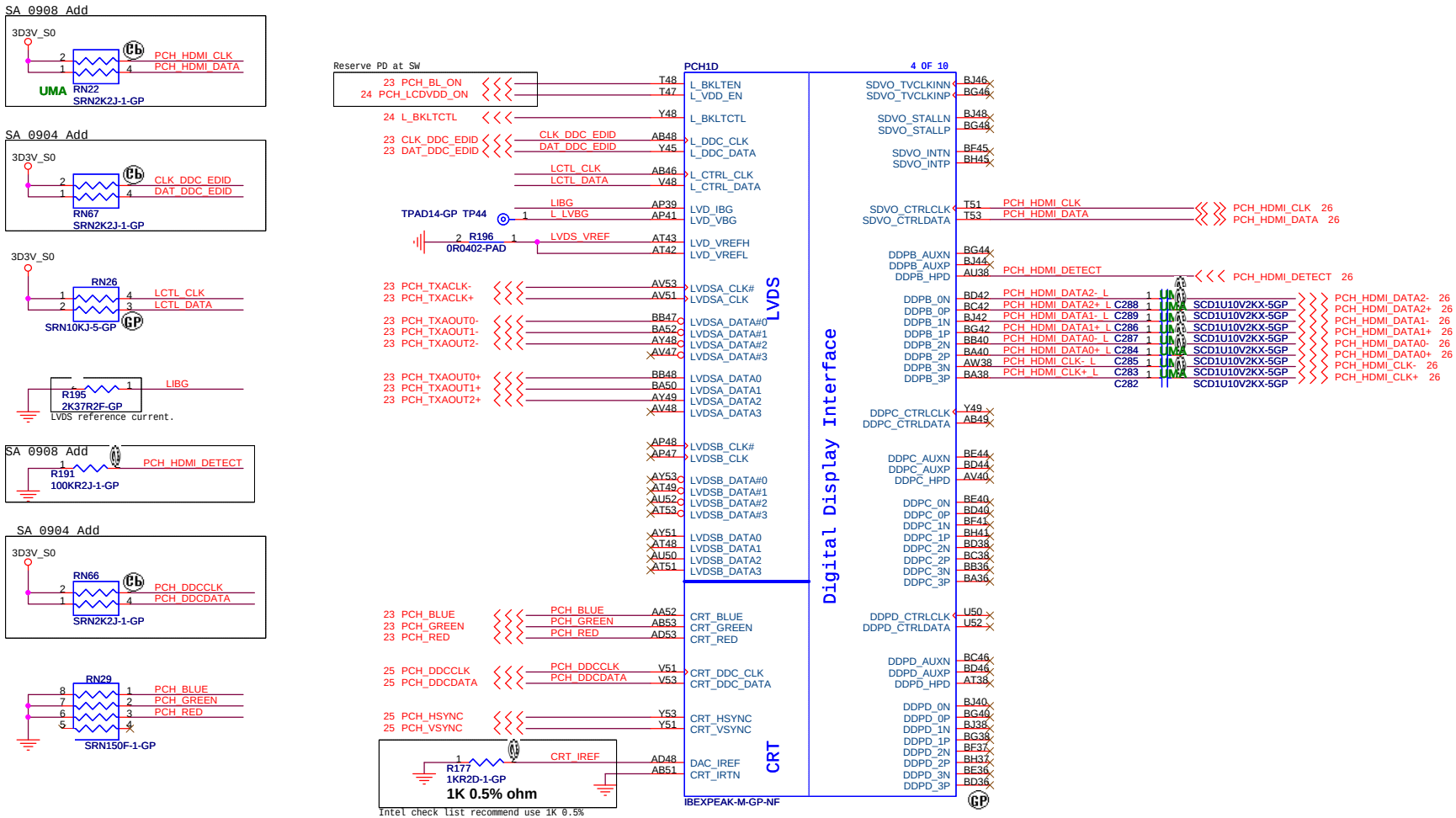
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

<Core Design>

Title: 16_PCH (3/9)-DMI / FDI / PM

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 16 of 58



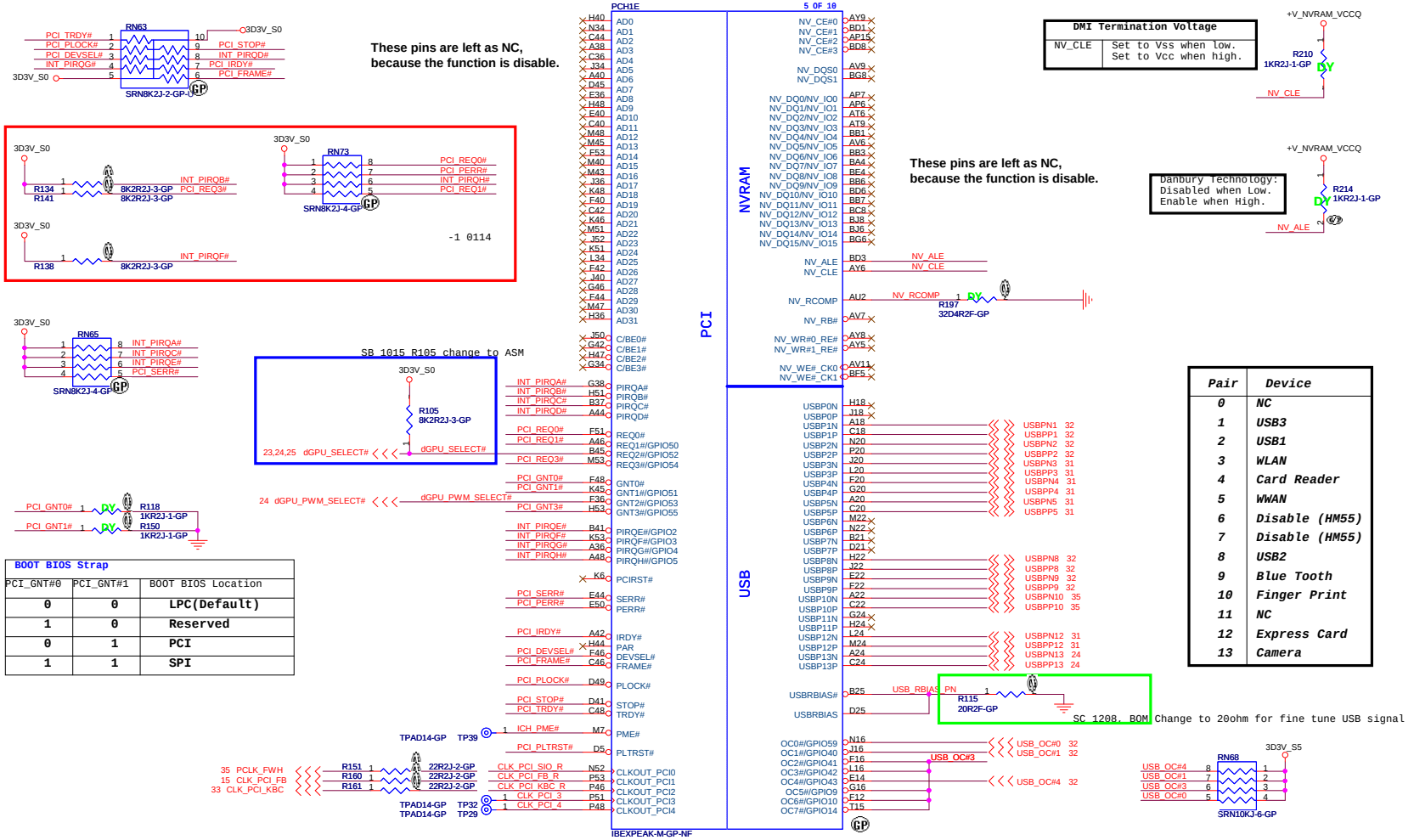
<core_design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 17_PCH (4/9)-LVDS / CRT

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 17 of 58

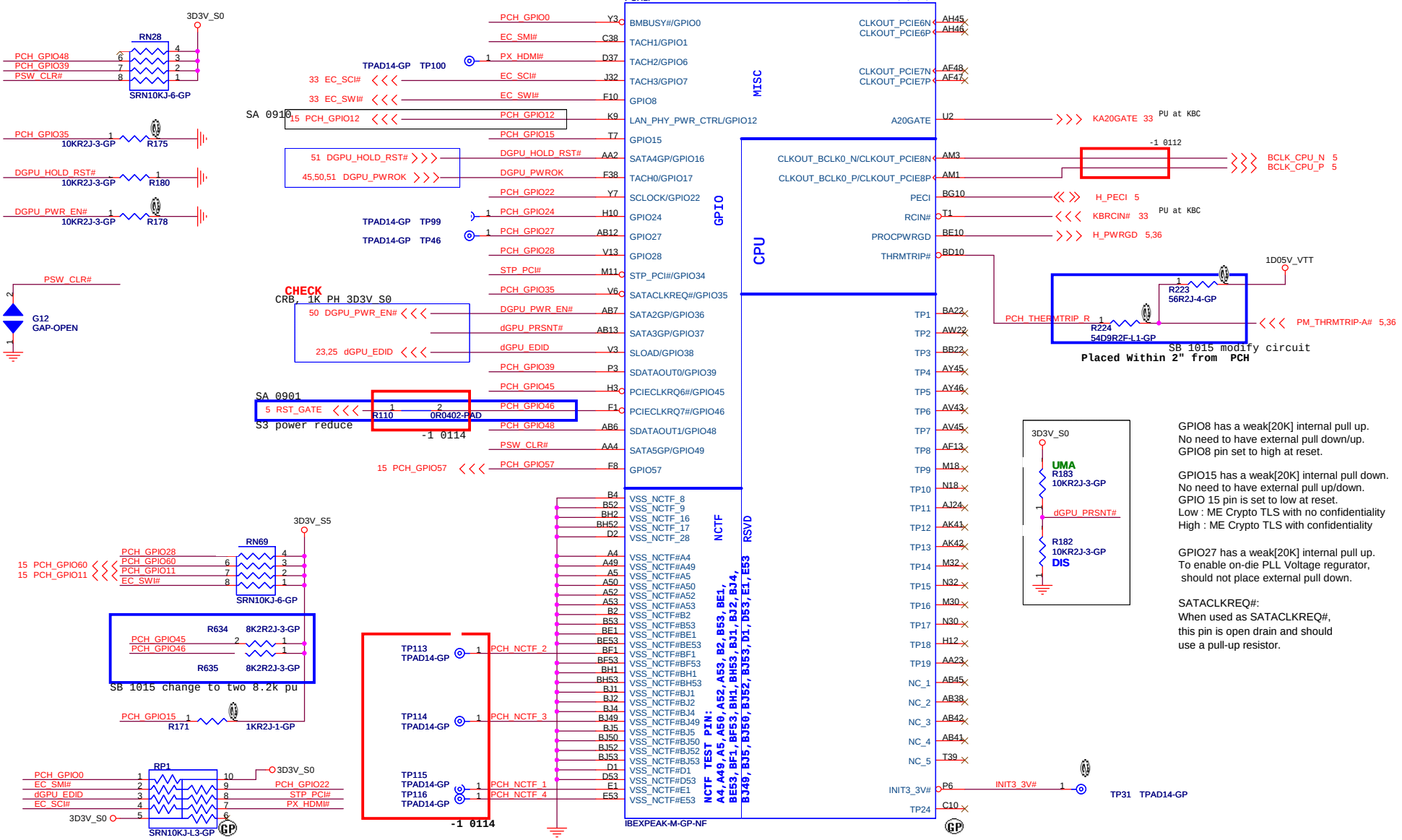


<Core Design>
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 18_PCH (5/9)-PCI / USB

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 18 of 58

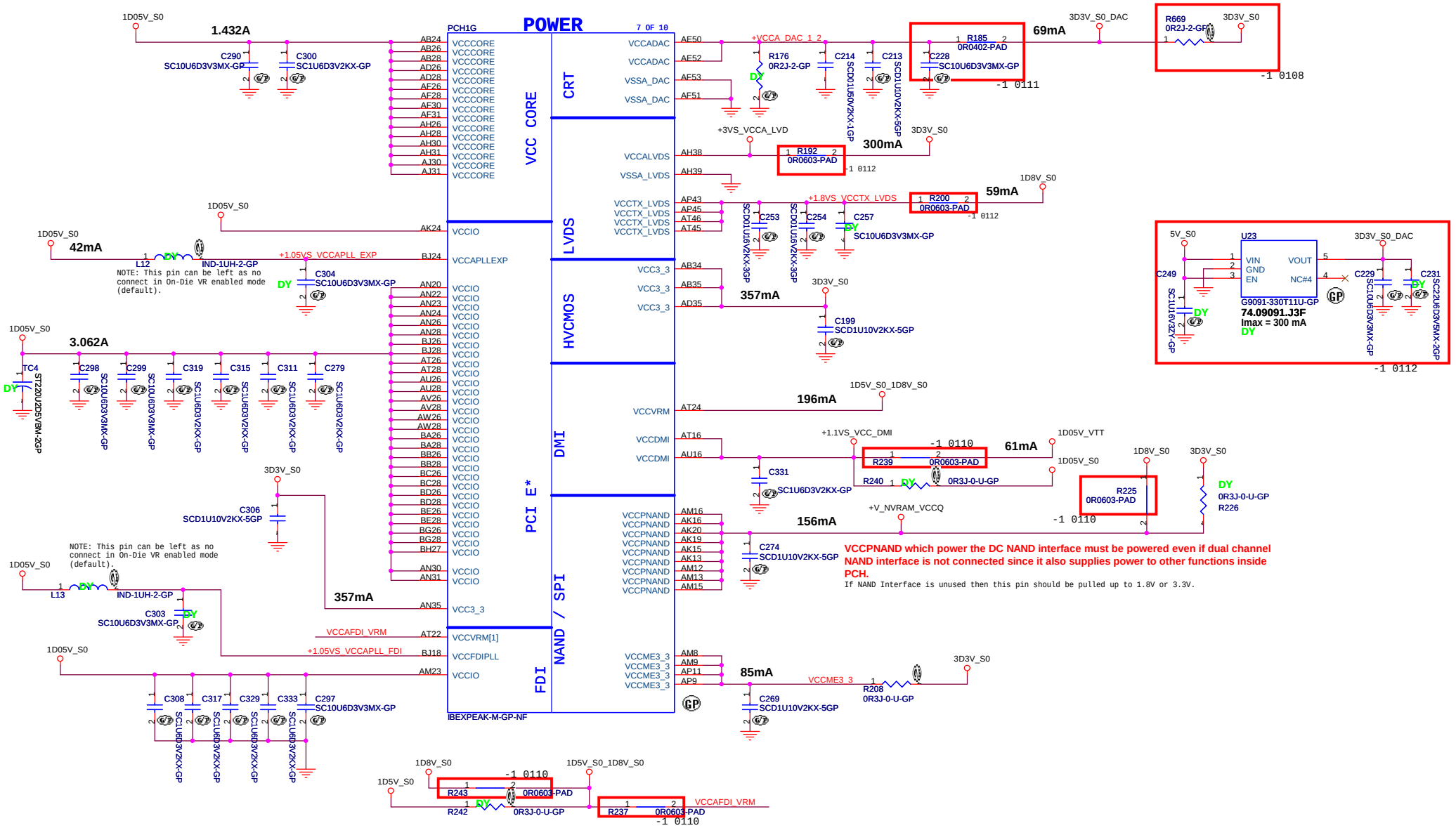


<Core Design>
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 19_PCH (6/9)-GPIO/VSS_NCTF/RSVD

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 19 of 58

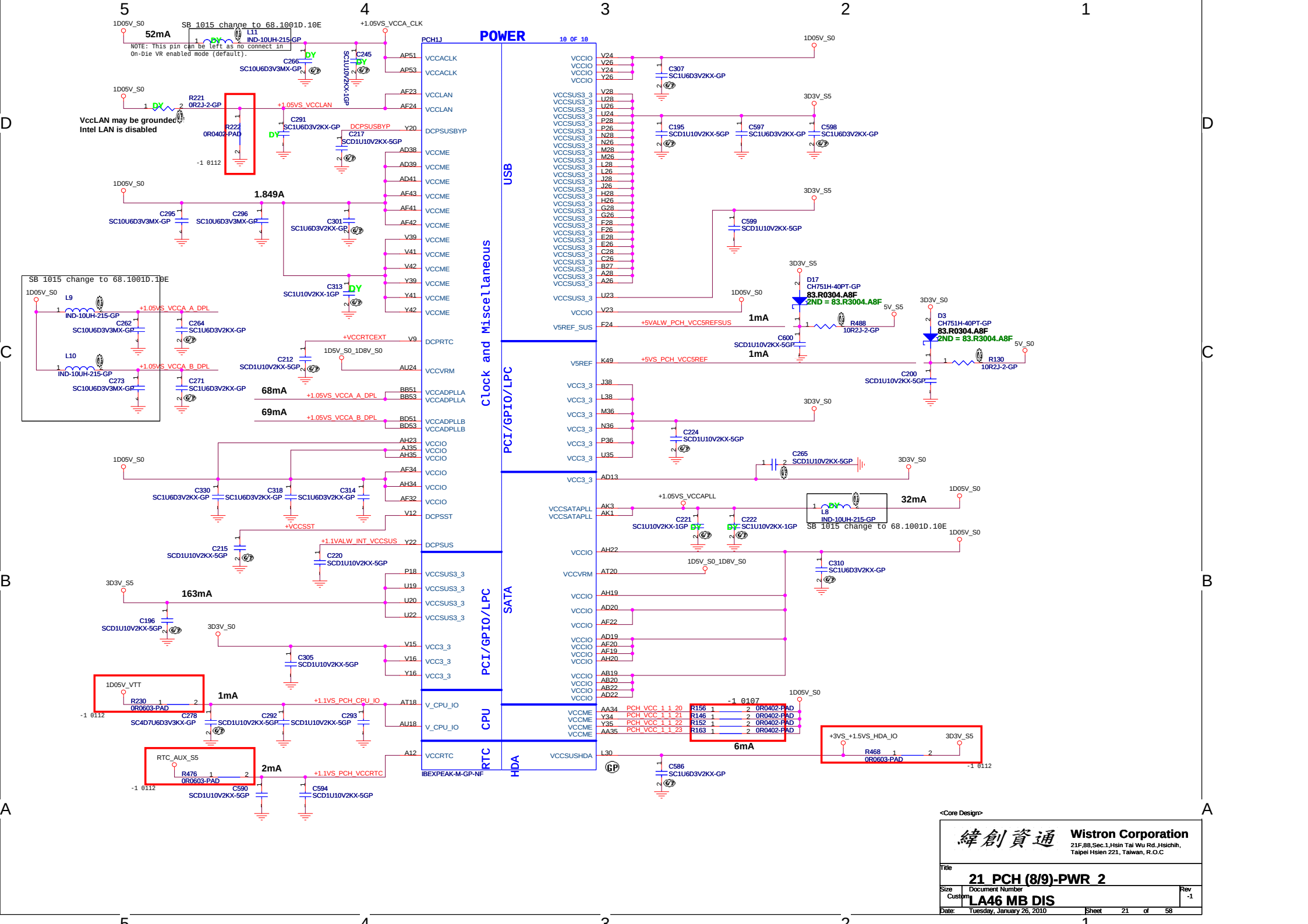


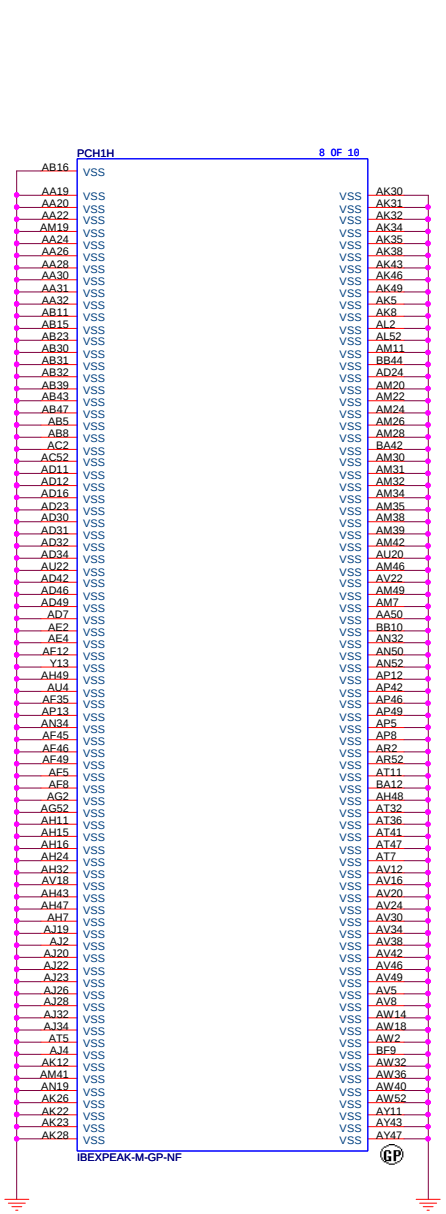
<Core Design>
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

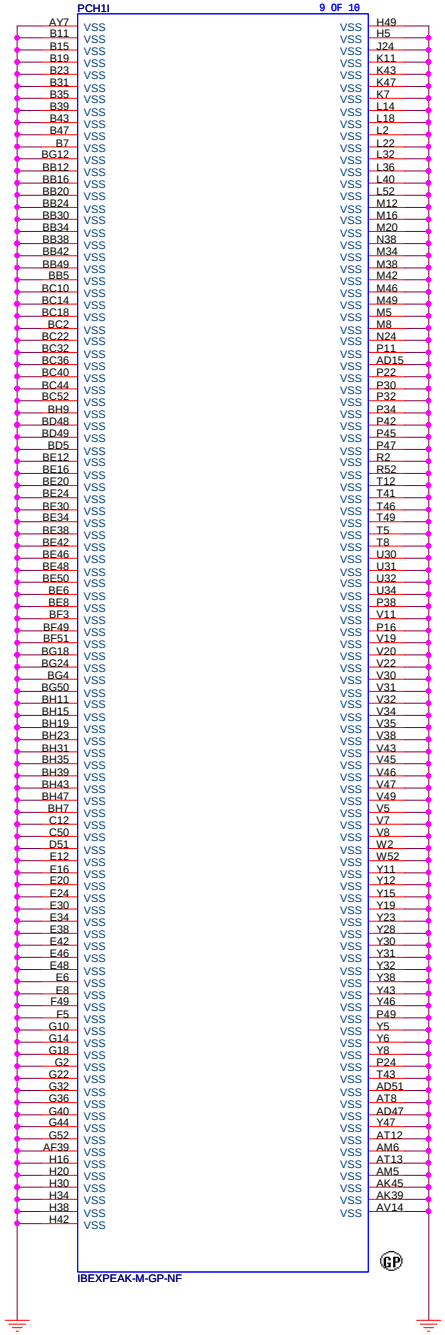
Title: 20_PCH (7/9)-PWR_1

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 20 of 58


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
1mA
68mA
69mA
32mA
6mA
2mA
SB 1015 change to 68.1001D.10E
VccLAN may be grounded
Intel LAN is disabled
IBEXPEAK-M-GP-NF
<Core Design>
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
21_PCH (8/9)-PWR_2
Size
Custom
Document Number
LA46 MB DIS
Rev
-1
Date:
Tuesday, January 26, 2010
Sheet
21
of
58





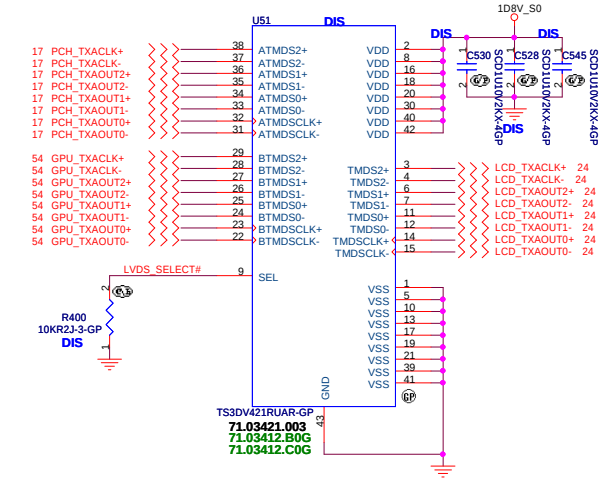
<Core Design>

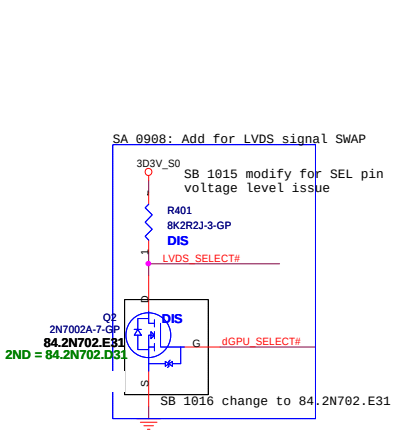
緯創資通 **Wistron Corporation**
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

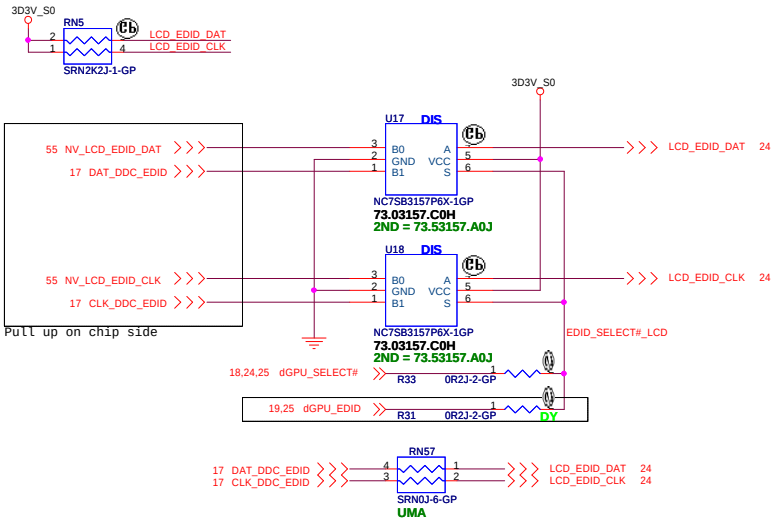
Title: **22_PCH (9/9)-VSS**

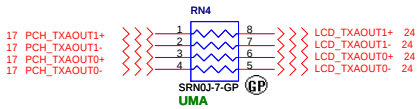
Size	Document Number	Rev
Custom	LA46 MB DIS	-1

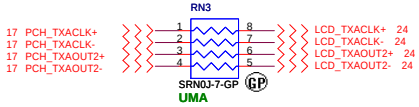
Date: Tuesday, January 26, 2010 Sheet 22 of 58

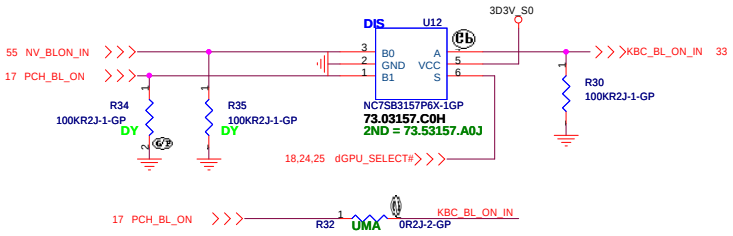


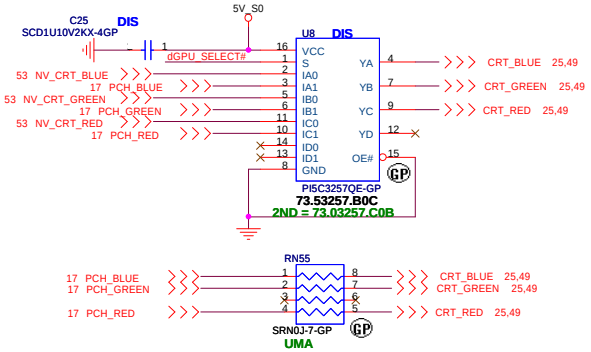












FUNCTION TABLE

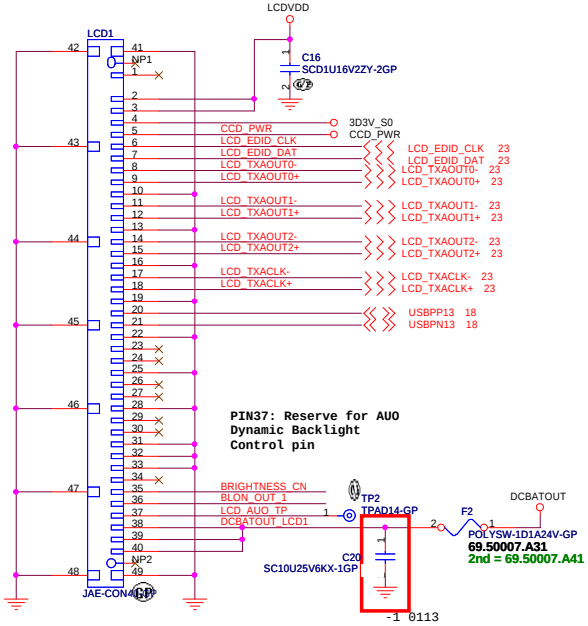
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

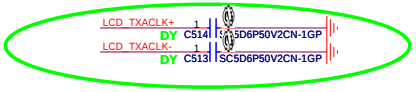
$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

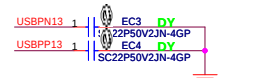
<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

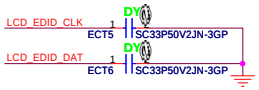
Title: 23_Display MUX
Size: Custom | Document Number: LA46 MB DIS | Rev: -1
Date: Tuesday, January 26, 2010 | Sheet 23 of 58

LCD/INVERTER/CCD CONN

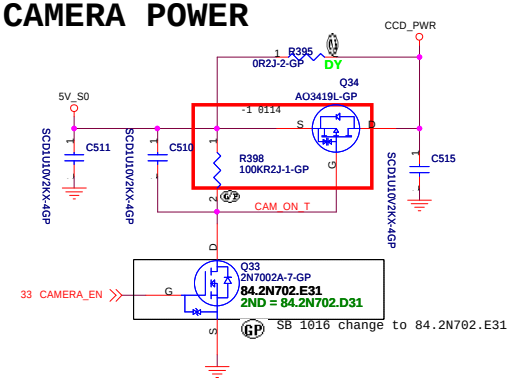


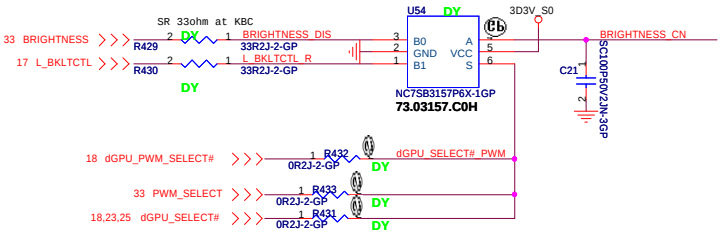


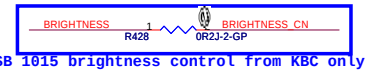


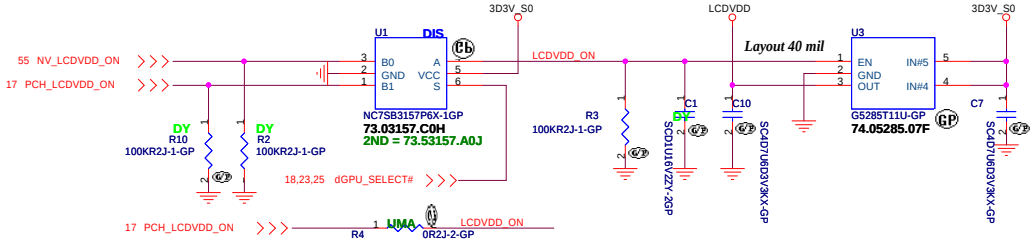


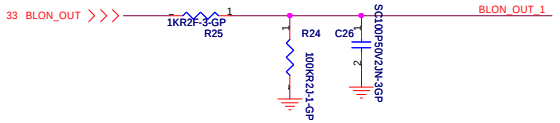
CAMERA POWER











<Core Design>

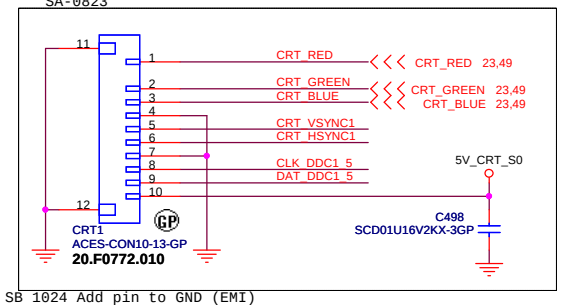
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 24_LCD & CCD

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 24 of 58

SA-0820 Move pi filter to CRT board.
SA-0823

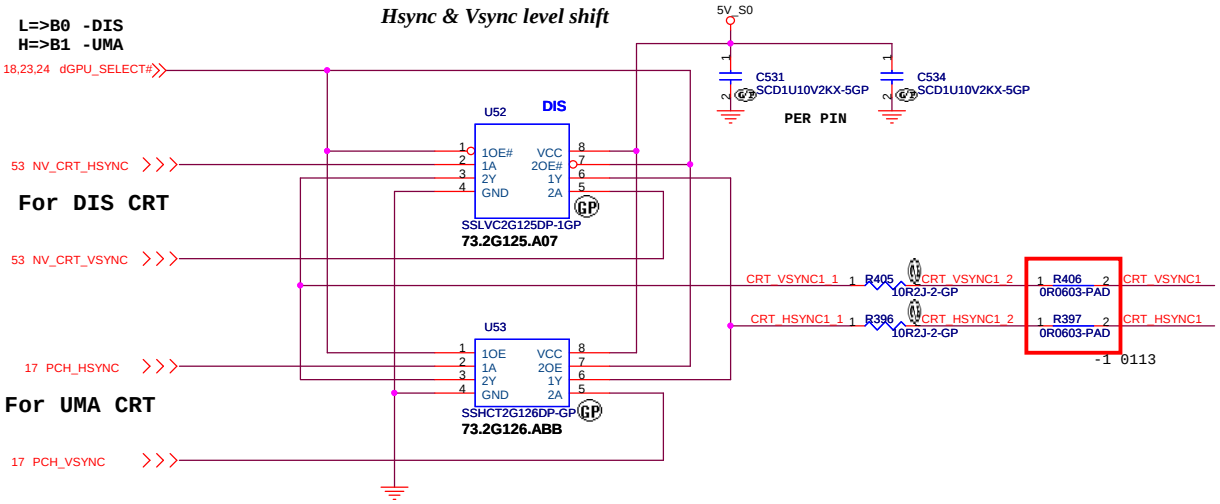


SB 1024 Add pin to GND (EMI)

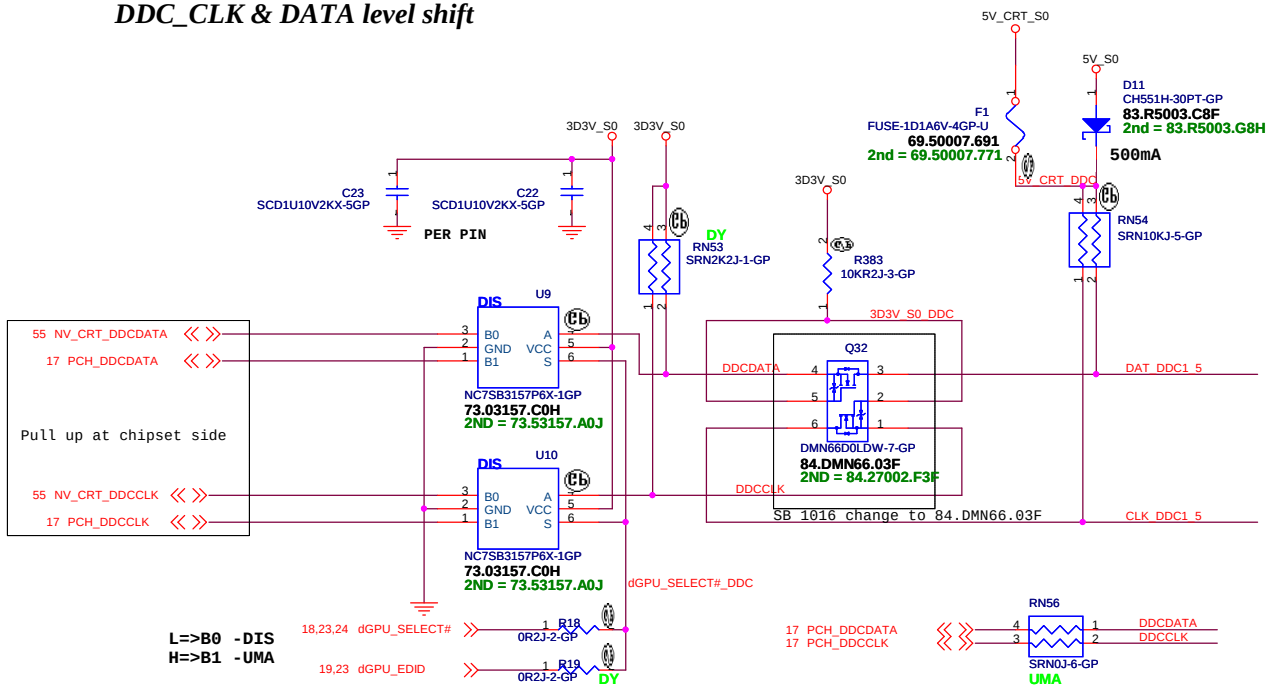
CLK_DDC1_5 → CLK_DDC1_5 49
DAT_DDC1_5 → DAT_DDC1_5 49

CRT_VSYNC1 → CRT_VSYNC1 49
CRT_HSYNC1 → CRT_HSYNC1 49

Hsync & Vsync level shift



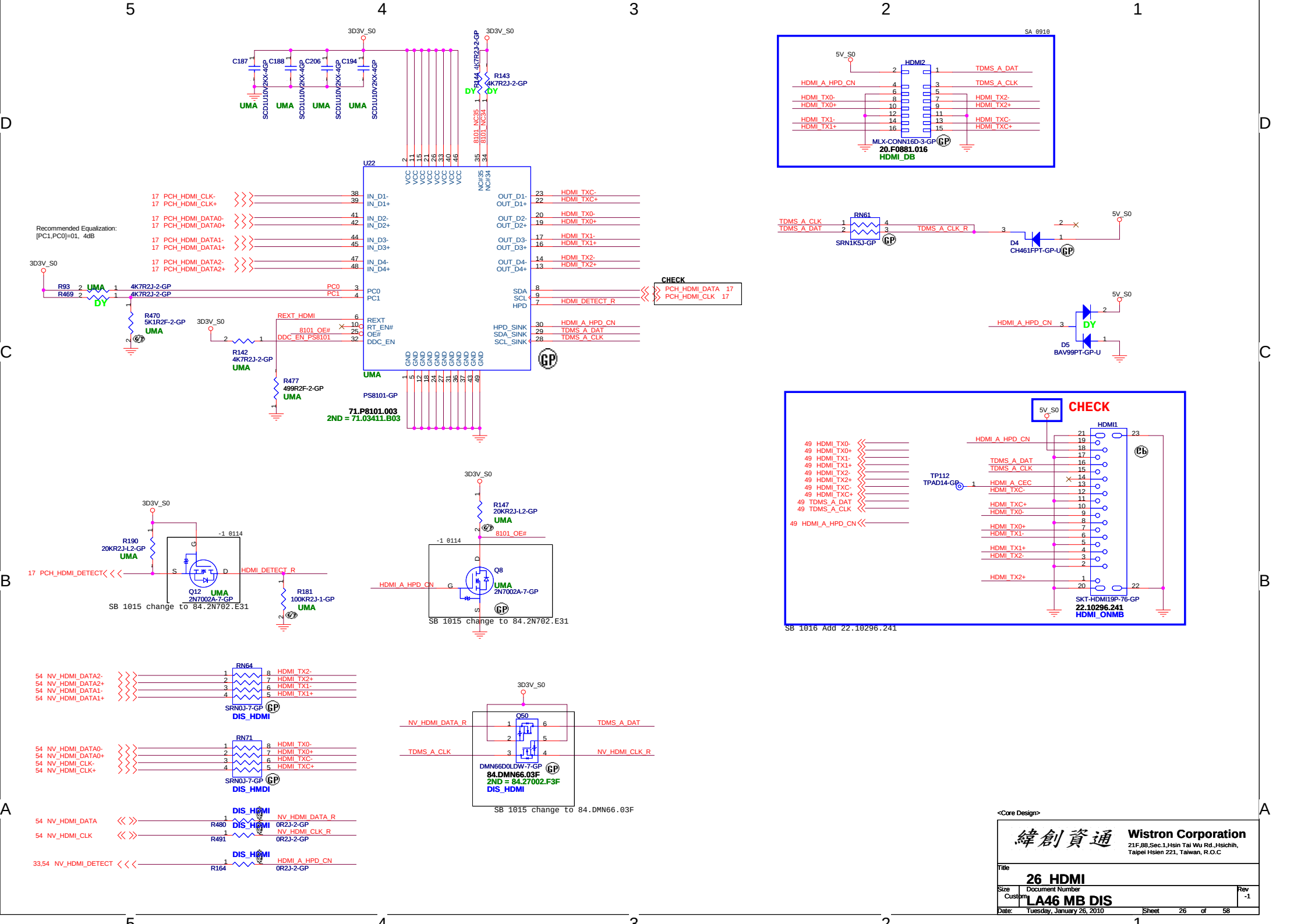
DDC_CLK & DATA level shift



<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 25 CRT
Size: A3
Document Number: LA46 MB DIS
Rev: -1
Date: Tuesday, January 26, 2010
Sheet 25 of 58

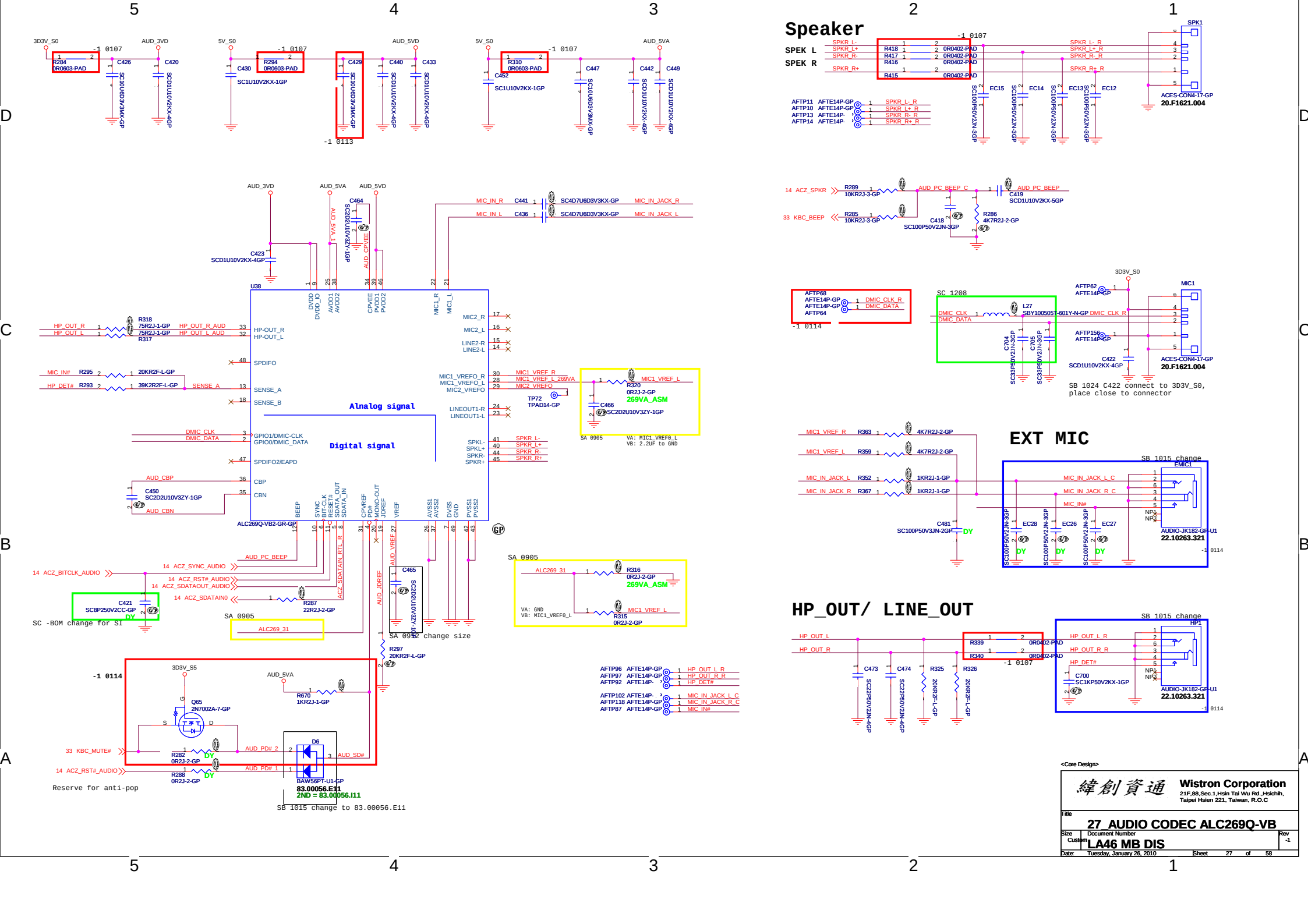


<Core Design>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

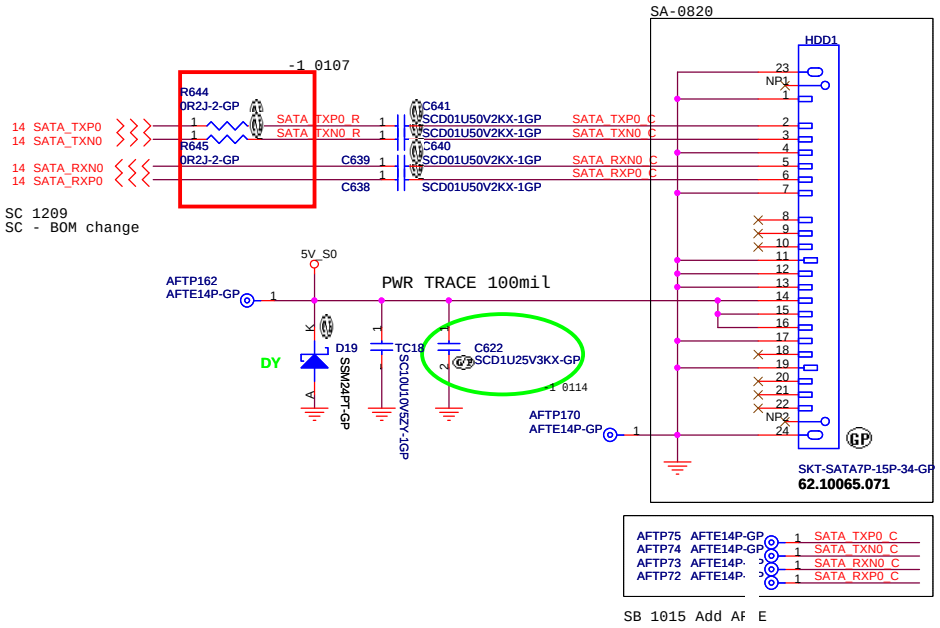
Title: 26 HDMI

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

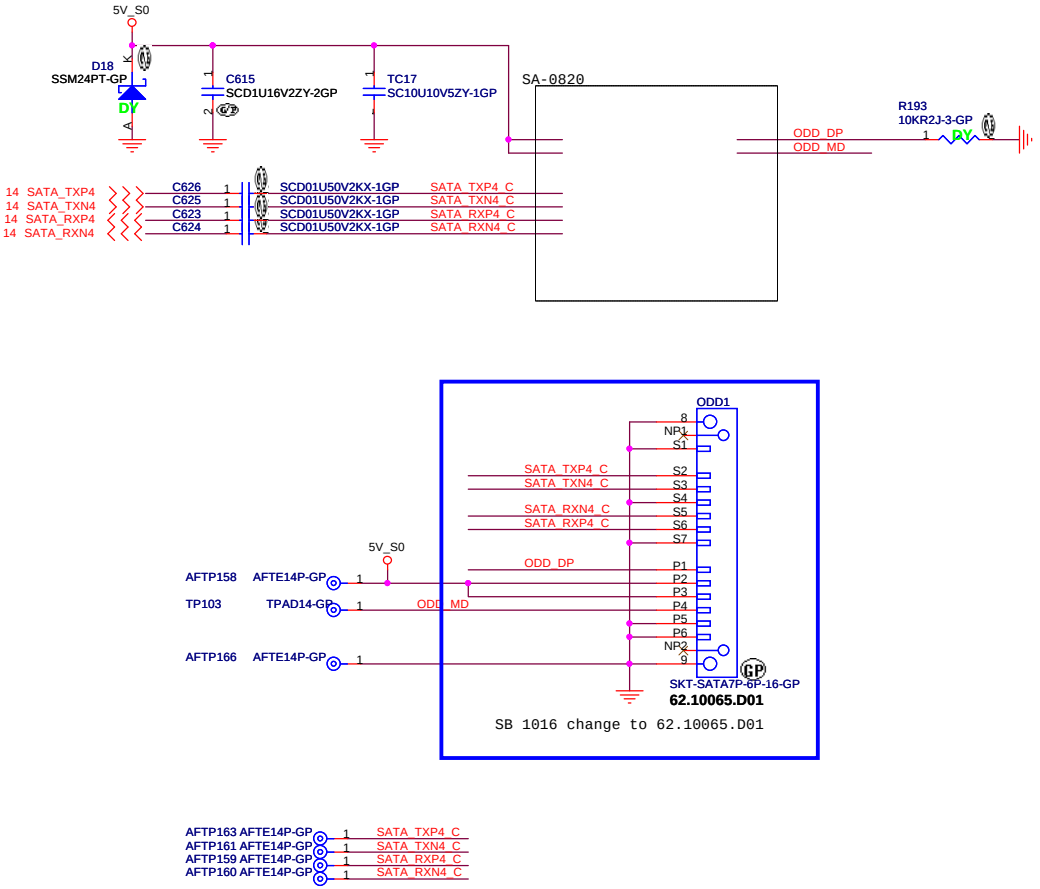
Date: Tuesday, January 26, 2010 | Sheet 26 of 58


Speaker
SPEK L
SPEK R
SPK1
ACES-CON4-17-GP
20.F1621.004
14 ACZ_SPKR
33 KBC_BEEP
AUD_PC_BEEP
MIC1
SB 1024 C422 connect to 3D3V_S0, place close to connector
EXT MIC
EMIC1
AUDIO-JK182-GP-U1
22.10263.321
SB 1015 change
HP_OUT/ LINE_OUT
HP1
U38
ALC269Q-VB2-GR-GP
Alnalog signal
Digital signal
SA 0905
SC -BOM change for SI
SA 0912 change size
Reserve for anti-pop
SB 1015 change to 83.00056.E11
83.00056.E11
2ND = 83.00056.I11
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
27_AUDIO CODEC ALC269Q-VB
LA46 MB DIS
Tuesday, January 26, 2010

SATA Connector



ODD Connector



<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 28 HDD & ODD

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Close to pin16,pin22,pin36,pin39

Close to pin8

Close to pin42

1D1VA_LAN_S5

C382 SCD1U10V2KX-4GP
C379 SCD1U10V2KX-1GP
C365 SCD1U10V2KX-4GP
C414 SCD1U10V2KX-4GP
C367 SCD1U10V2KX-4GP
C399 SCD1U10V2KX-4GP
C413 SCD1U10V2KX-4GP

Close to pin45.pin46

Close to pin28,pin32

1D1VD_LAN_S5

C412 SCD1U10V2KX-1GP
C411 SCD1U10V2KX-4GP
C390 SCD1U10V2KX-4GP
C378 SCD1U10V2KX-4GP

Close to pin15

Close to pin5,pin19,pin25

2D5V_LAN_S5

C368 SCD1U10V2KX-1GP
C366 SCD1U10V2KX-4GP
C374 SCD1U10V2KX-4GP
C372 SCD1U10V2KX-4GP

Close to pin2

3D3V_LAN_S5

C393 SCD1U16D3V3MX-GP
C395 SCD1U10V2KX-1GP

SA 0906

3D3V_LAN_S5

3D3V_S5

C387 SCD1U16Y2X-2GP
C400 SCD1U16Y2X-2GP

-1 0114

R263 0R3J-0-U-GP
Q24 AO3419L-GP
R269 100KR2J-1-GP
LAN_PWR_ON_T
C403 SCD1U10V2KX-1GP
Q23 2N7002A-7-GP
84.2N702.E31
2ND = 84.2N702.D31
33 LAN_PWR_ON

SB ASM by SW require

1D25V_LAN_S5

C373 SCD1U10V2KX-4GP
C371 SC1K50V2KX-1GP
DY

U29
A0 A1 A2 GND VCC WP SCL SDA
LAN_SCLK
LAN_SDATA
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01

3D3V_LAN_S5

C407 SCD1U10V2KX-4GP

Close to LAN AR8131

MDI0- MDI0+ RN45 SRN49D9F-GP MDI0_RC C362 SCD1U10V2KX-4GP
MDI1- MDI1+ RN44 SRN49D9F-GP MDI1_RC C361 SCD1U10V2KX-4GP
MDI2+ MDI2- SRN49D9F-GP RN43 8132_DY MDI2_RC C360 SCD1U10V2KX-4GP 8132_DY
MDI3- MDI3+ RN42 SRN49D9F-GP 8132_DY MDI3_RC C359 SCD1U10V2KX-4GP 8132_DY

for AR8131M apply in the future

LAN_SCLK
LAN_SDATA
DY C396 SCD1U10V2KX-4GP
DY C386 SCD1U10V2KX-4GP

SB 1015, OBS, change to 68.4R750.20C

Close to pin1

L14 IND-4D7UH-192-GP
C398 SC10U6D3V3MX-GP
C397 SCD1U10V2KX-4GP
LX
AVDD_CEN
30 AVDD_CEN
SC 1209
C392 SCD1U10V2KX-4GP

Close to pin6

LAN_XO
LAN_XI
X5 XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
C375 SC15P50V2JN-2-GP
C380 SC15P50V2JN-2-GP

1D1VA_LAN_S5
1D25V_LAN_S5
2D5V_LAN_S5
1D1VD_LAN_S5
3D3V_LAN_S5

-1 0114
R274 0R0402-PAD
Pin42 connect to AVDDL
DO NOT SUPPORT Overclocking

U28
VDD11_REG AVDD_REG AVVDL AVDDL AVDDL AVDDL AVDDL AVDDL
VDDHO AVDDH AVDDH
DVDDL DVDDL DVDD_REG DVDD_REG
LX VDD3V VDD17 VDD25V
SMCLK SMDATA
TESTMODE NO_CONN
TWSI_CLK TWSI_DATA
REFCLKN REFCLKP RX_N RX_P TX_N TX_P
PCIE_RXDN C409 SCD1U10V2KX-5GP
PCIE_RXDP C410 SCD1U10V2KX-5GP
TRXN0 TRXP0 TRXN1 TRXP1 TRXN2 TRXP2 TRXN3 TRXP3 WAKE#
LED2 CLKREQ# LED1 LED0
RBIAS PERST# XTLI XTLO SEL_25_MHZ
GND
AR8131-AL1E-R-GP
71.08131.M02
CO-LAY 71.08132.M01 (10/100)

CLK_PCIE_LAN# 15
CLK_PCIE_LAN 15
PCIE_TXN1 15
PCIE_TXP1 15
PCIE_RXN1 15
PCIE_RXP1 15
MDI0- 30
MDI0+ 30
MDI1- 30
MDI1+ 30
MDI2- 30
MDI2+ 30
MDI3- 30
MDI3+ 30
PCIE_WAKE# 16,31
LAN_CLKREQ# 15
LAN_ACT_LED#
10M/100M/1G_LED#
TP68 TPAD14-GP
LAN_RBIAS R253 2K37R2F-GP
LAN_RST R271 0R0402-PAD
LAN_XI
LAN_XO
SEL_25M
PLT_RST# 5,18,31,33,35,51
-1 0107
C406 SC150P50V2JN-3GP
DY
R262 4K7R2J-2-GP
ASM : 48Mhz
DY : 25Mhz
LAN_ACT_LED# R277 4K7R2J-2-GP
SC 1126

R256 4K7R2J-2-GP
R259 4K7R2J-2-GP
LAN_SCLK
LAN_SDATA
C385 SCD1U10V2KX-4GP DY

SA 0906: Reserve for EEPROM DY

<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 29 LAN AR8131/8132

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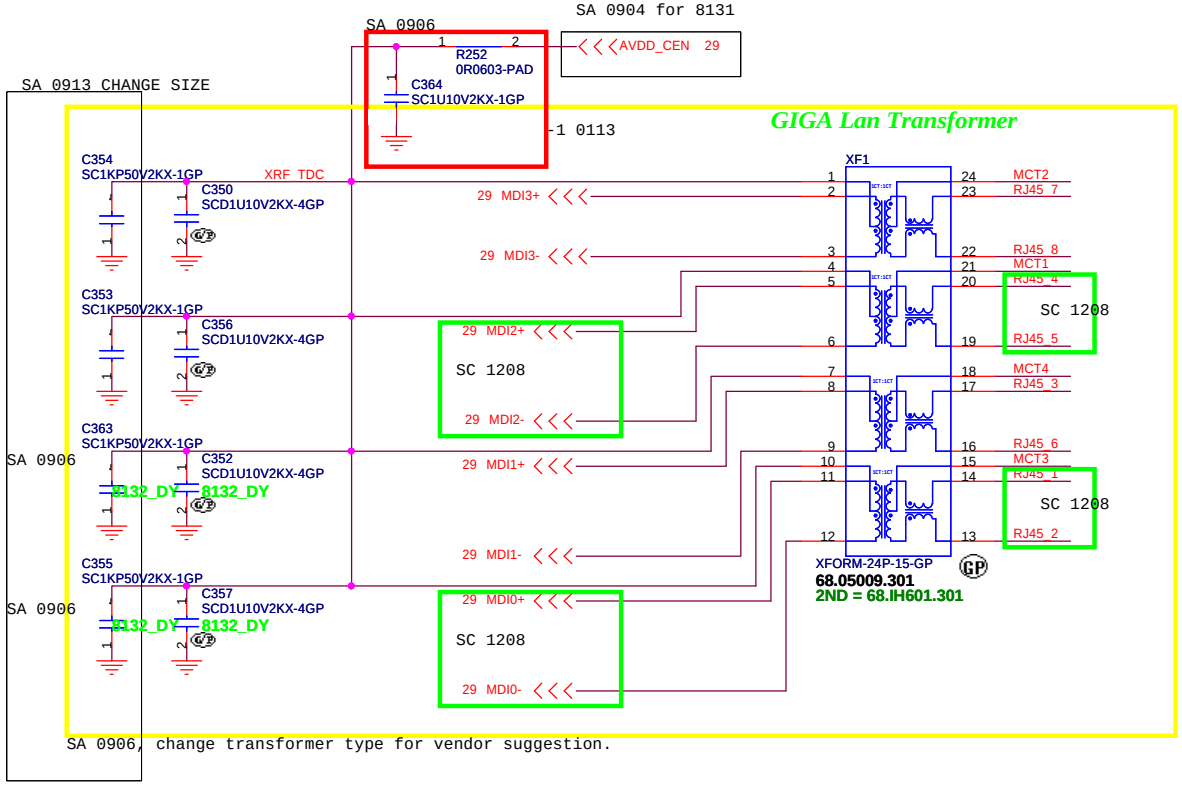
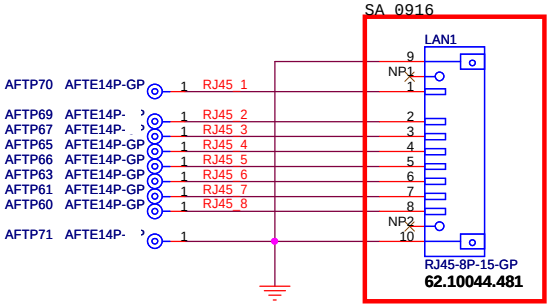
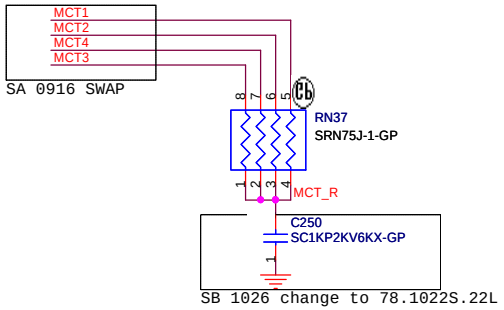
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector







<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 30_LAN CONN

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

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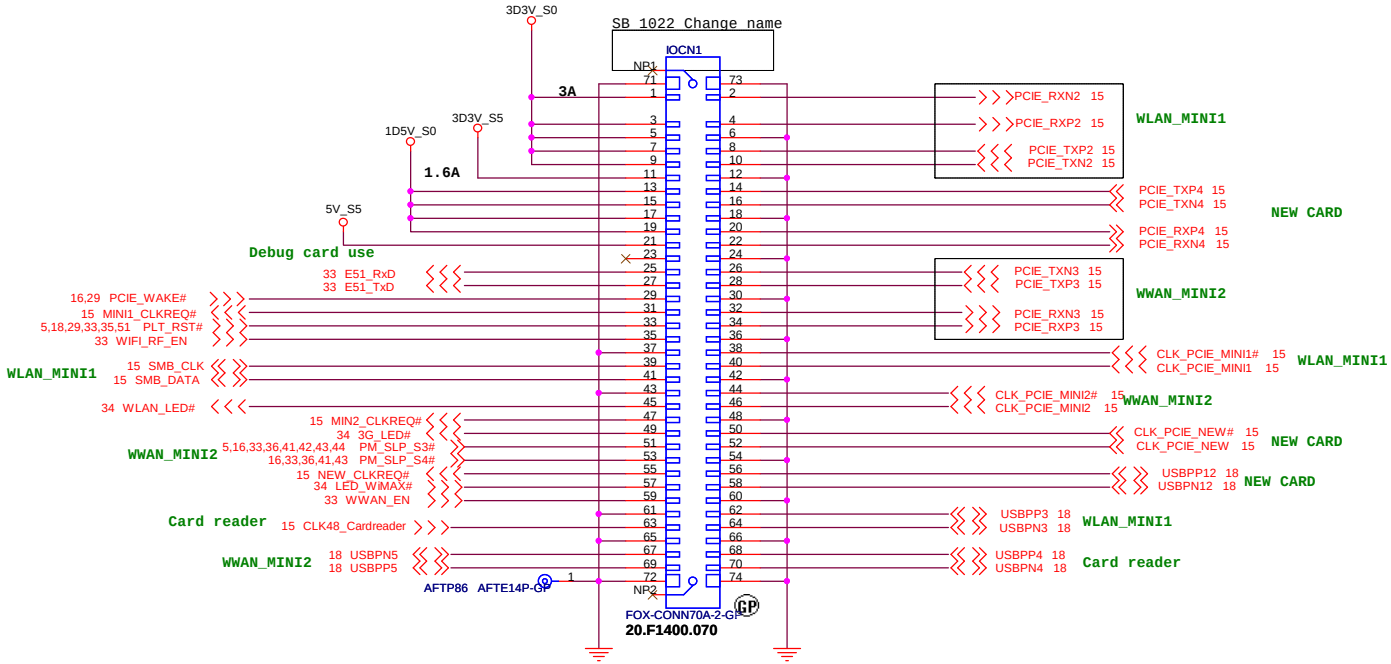

AFTP107 AFTE14P-GP 1 3D3V_S0
AFTP103 AFTE14P- 1 3D3V_S5
AFTP104 AFTE14P-GP 1 1D5V_S0
AFTP99 AFTE14P- 1 5V_S5

AFTP98 AFTE14P-GP 1 E51_RxD
AFTP93 AFTE14P-GP 1 E51_TxD
AFTP91 AFTE14P- 1 PCIE_WAKE#
AFTP84 AFTE14P- 1 MINI1_CLKREQ#
AFTP190 AFTE14P-GP 1 CLK_PCIE_MINI1#
AFTP188 AFTE14P- 1 CLK_PCIE_MINI1
AFTP109 AFTE14P- 1 PCIE_RXN2
AFTP108 AFTE14P- 1 PCIE_RXP2
AFTP105 AFTE14P- 1 PCIE_TXN2
AFTP106 AFTE14P-GP 1 PCIE_TXP2
AFTP185 AFTE14P- 1 PLT_RST#
AFTP184 AFTE14P- 1 WIFI_RF_EN
AFTP182 AFTE14P-GP 1 SMB_CLK
AFTP181 AFTE14P- 1 SMB_DATA
AFTP180 AFTE14P- 1 WLAN_LED#
AFTP178 AFTE14P- 1 MIN2_CLKREQ#
AFTP187 AFTE14P- 1 USBPN3
AFTP189 AFTE14P-GP 1 USBPP3
AFTP177 AFTE14P- 1 CLK_PCIE_MINI2#
AFTP179 AFTE14P- 1 CLK_PCIE_MINI2

AFTP194 AFTE14P-GP 1 USBPP4
AFTP193 AFTE14P-GP 1 USBPN4
AFTP176 AFTE14P-GP 1 CLK48_Cardreader
AFTP101 AFTE14P-GP 1 PCIE_TXP4
AFTP100 AFTE14P- 1 PCIE_TXN4
AFTP95 AFTE14P- 1 PCIE_RXP4
AFTP94 AFTE14P-GP 1 PCIE_RXN4
AFTP174 AFTE14P-GP 1 CLK_PCIE_NEW
AFTP173 AFTE14P- 1 CLK_PCIE_NEW#
AFTP80 AFTE14P- 1 USBPP12
AFTP79 AFTE14P- 1 USBPN12
AFTP81 AFTE14P-GP 1 3G_LED#
AFTP78 AFTE14P- 1 PM_SLP_S3#
AFTP82 AFTE14P- 1 PM_SLP_S4#
AFTP83 AFTE14P- 1 NEW_CLKREQ#
AFTP89 AFTE14P- 1 PCIE_TXN3
AFTP88 AFTE14P-GP 1 PCIE_TXP3
AFTP90 AFTE14P- 1 PCIE_RXN3
AFTP85 AFTE14P- 1 PCIE_RXP3
AFTP192 AFTE14P- 1 USBPN5
AFTP191 AFTE14P- 1 USBPP5
AFTP77 AFTE14P-GP 1 LED_WiMAX#
AFTP76 AFTE14P- 1 WWAN_EN

<Core Design>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 31 IO CONN

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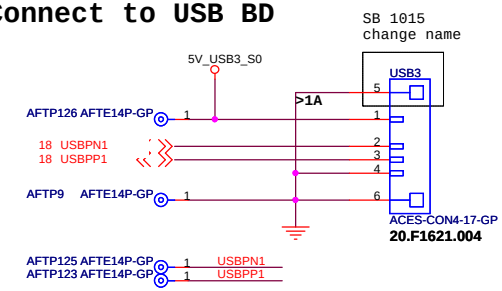
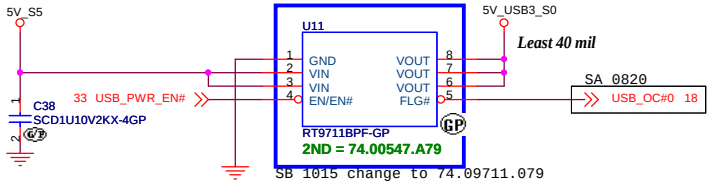
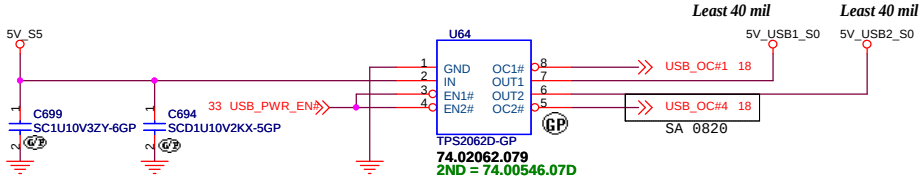
USB3

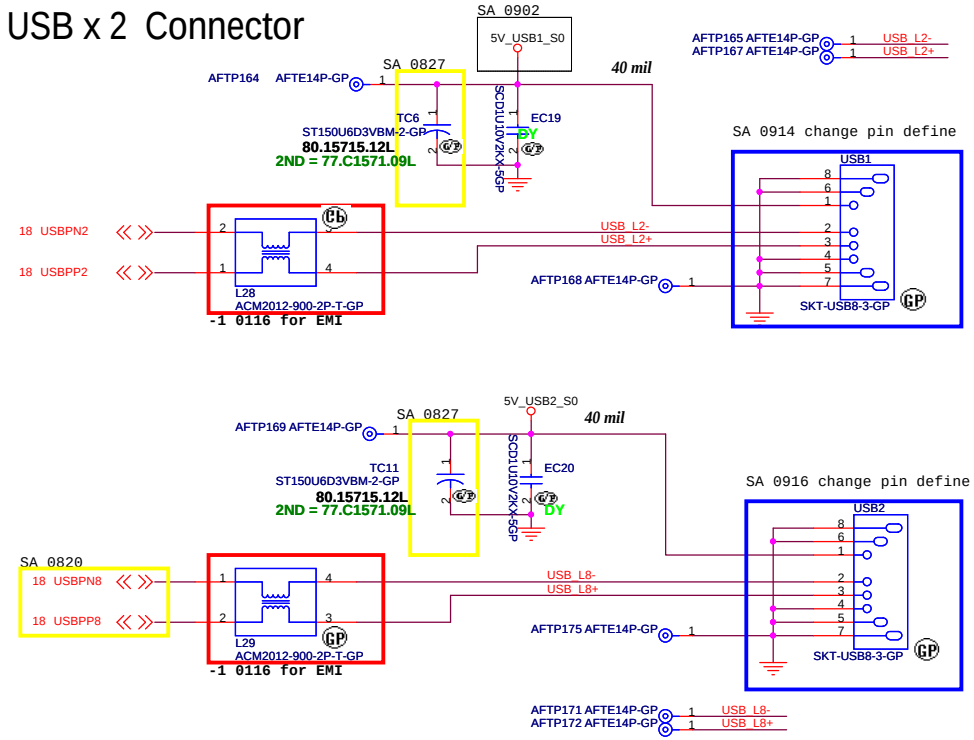
Connect to USB BD



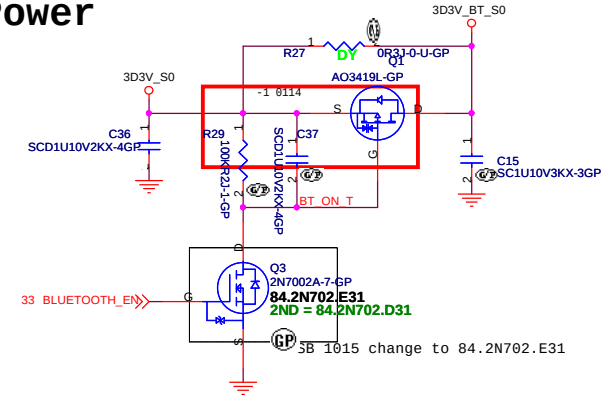




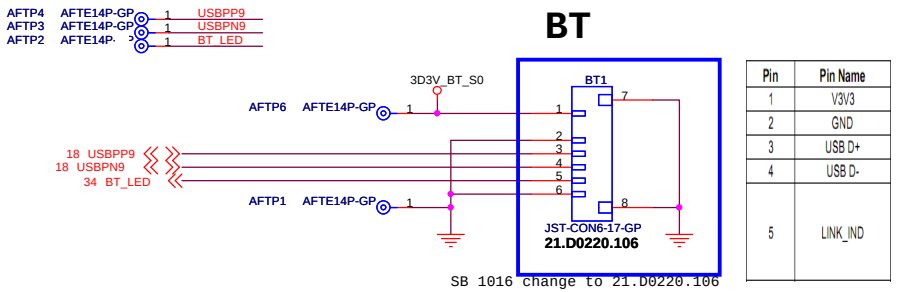
USB x 2 Connector



Bluetooth Power



BT



Pin	Pin Name
1	V3V3
2	GND
3	USB D+
4	USB D-
5	LINK_IND

<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 32 USB & BT

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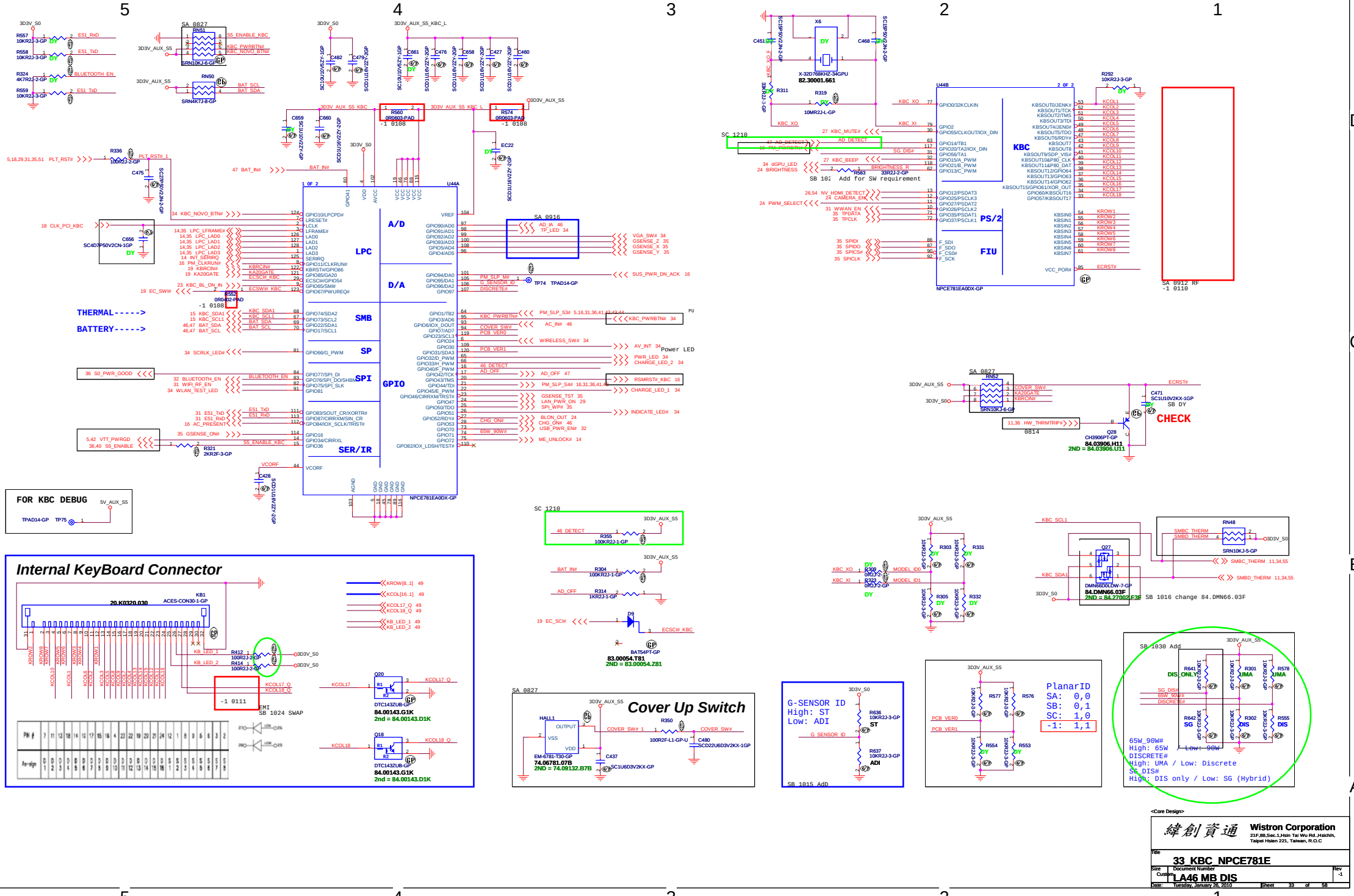
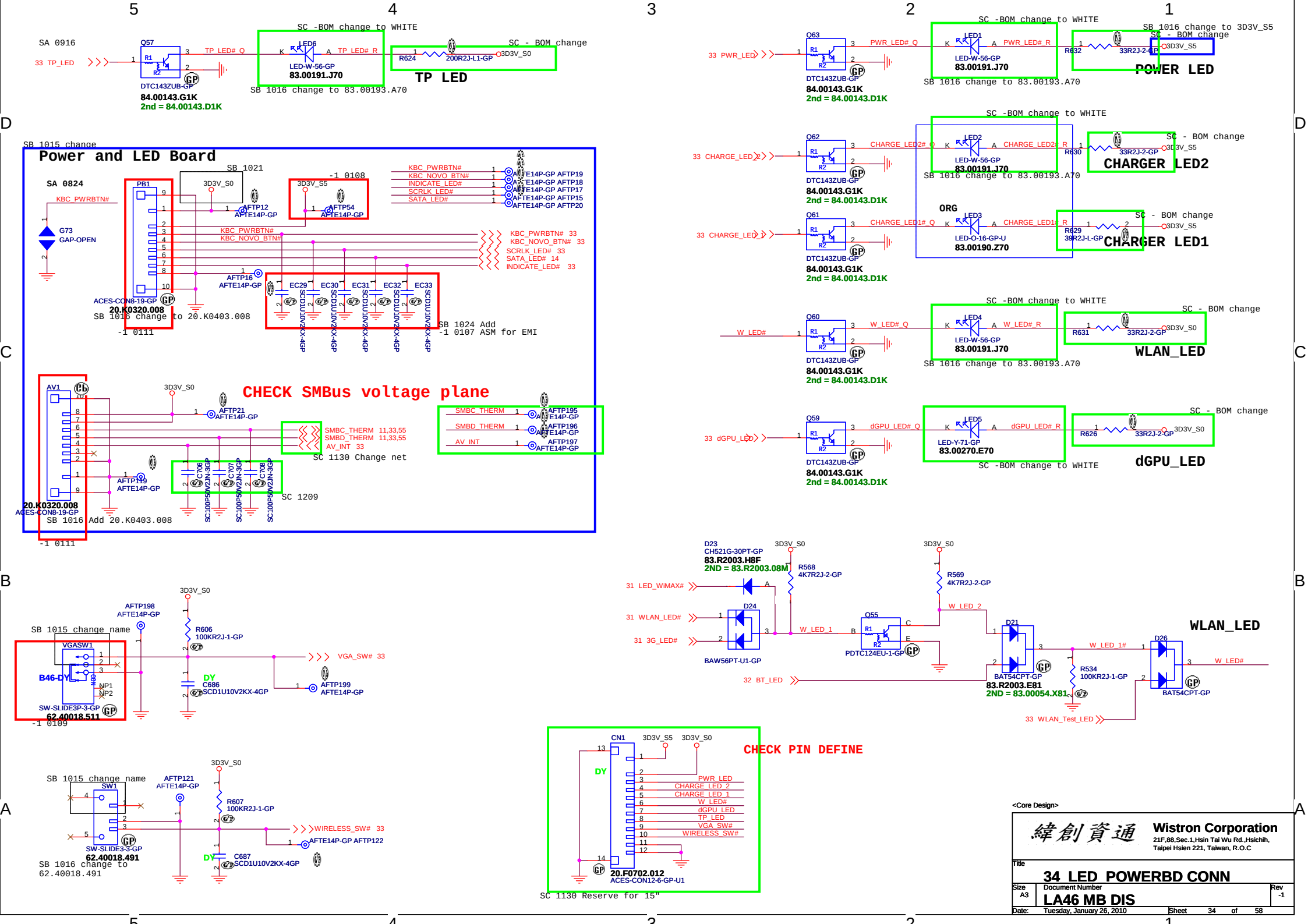

NPCE781EA0DX-GP
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
G-SENSOR ID
High: ST
Low: ADI
PlanarID
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
65W_90W#
High: 65W / Low: 90W
DISCRETE#
High: UMA / Low: Discrete
SG_DIS#
High: DIS only / Low: SG (Hybrid)
CHECK
Wistron Corporation
33_KBC_NPCE781E
LA46 MB DIS


SA 0916
33 TP_LED
Q57
DTC143ZUB-GP
84.00143.G1K
2nd = 84.00143.D1K
TP_LED# Q
TP_LED# R
SC -BOM change to WHITE
LED6
LED-W-56-GP
83.00191.J70
SB 1016 change to 83.00193.A70
R624
200R2J-L1-GP
3D3V_S0
SC - BOM change
TP LED
SB 1015 change
Power and LED Board
SB 1021
SA 0824
PB1
ACES-CON8-19-GP
20.K0320.008
SB 1016 change to 20.K0403.008
-1 0111
-1 0108
KBC_PWRBTN#
KBC_NOVO_BTN#
INDICATE_LED#
SCRLK_LED#
SATA_LED#
G73
GAP-OPEN
AFTP12
AFTP54
AFTP16
EC29
EC30
EC31
EC32
EC33
SCD1U10V2KX-4GP
SB 1024 Add
-1 0107 ASM for EMI
CHECK SMBus voltage plane
AV1
AFTP21
AFTP119
SMBC_THERM 11,33,55
SMBD_THERM 11,33,55
AV_INT 33
SC 1130 Change net
C706
C707
C708
SC100P50V2JN-3GP
SC 1209
SB 1016 Add 20.K0403.008
-1 0111
SMBC_THERM
SMBD_THERM
AV_INT
AFTP195
AFTP196
AFTP197
AFTE14P-GP
Q63
PWR_LED# Q
PWR_LED# R
LED1
LED-W-56-GP
83.00191.J70
R632
33R2J-2-GP
POWER LED
Q62
CHARGE_LED2# Q
CHARGE_LED2# R
LED2
R630
CHARGER LED2
Q61
CHARGE_LED1# Q
CHARGE_LED1# R
LED3
LED-O-16-GP-U
83.00190.Z70
ORG
R629
39R2J-L-GP
CHARGER LED1
Q60
W_LED# Q
W_LED# R
LED4
R631
WLAN_LED
Q59
dGPU_LED# Q
dGPU_LED# R
LED5
LED-Y-71-GP
83.00270.E70
R626
dGPU_LED
DTC143ZUB-GP
84.00143.G1K
2nd = 84.00143.D1K
SB 1016 change to 3D3V_S5
SC - BOM change
SC -BOM change to WHITE
SB 1016 change to 83.00193.A70
D23
CH521G-30PT-GP
83.R2003.H8F
2ND = 83.R2003.08M
D24
BAW56PT-U1-GP
R568
4K7R2J-2-GP
R569
4K7R2J-2-GP
Q55
PDTC124EU-1-GP
D21
BAT54CPT-GP
83.R2003.E81
2ND = 83.00054.X81
D26
R534
100KR2J-1-GP
31 LED_WiMAX#
31 WLAN_LED#
31 3G_LED#
32 BT_LED
W_LED_1
W_LED_2
W_LED_1#
33 WLAN_Test_LED
WLAN_LED
SB 1015 change name
AFTP198
VGASW1
B46-DY
SW-SLIDE3P-3-GP
62.40018.511
-1 0109
R606
100KR2J-1-GP
C686
SCD1U10V2KX-4GP
VGA_SW# 33
AFTP199
SW1
AFTP121
R607
WIRELESS_SW# 33
AFTP122
62.40018.491
SB 1016 change to
62.40018.491
CN1
20.F0702.012
ACES-CON12-6-GP-U1
PWR_LED
CHARGE_LED_2
CHARGE_LED_1
W_LED#
dGPU_LED
TP_LED
VGA_SW#
WIRELESS_SW#
CHECK PIN DEFINE
SC 1130 Reserve for 15"
<Core Design>
緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title
34 LED POWERBD CONN
Size
A3
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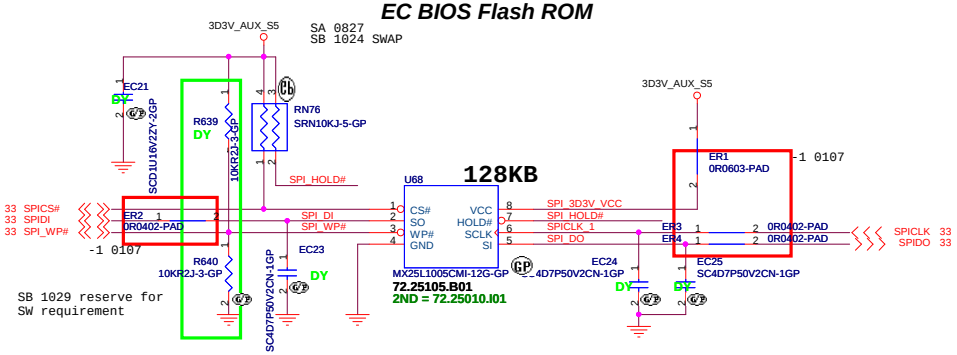
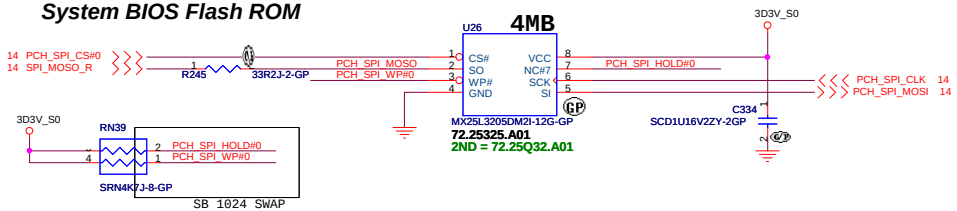
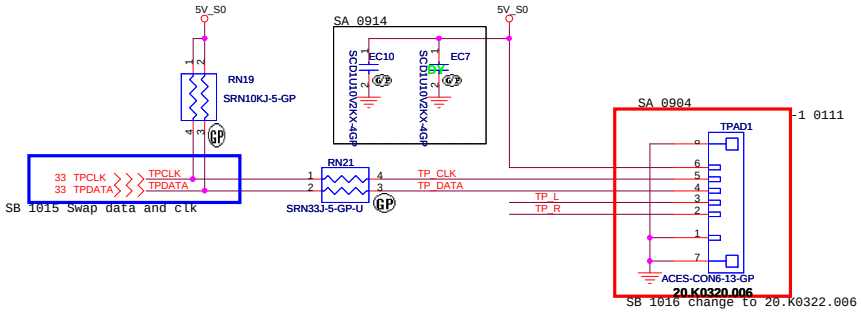
EC BIOS Flash ROM

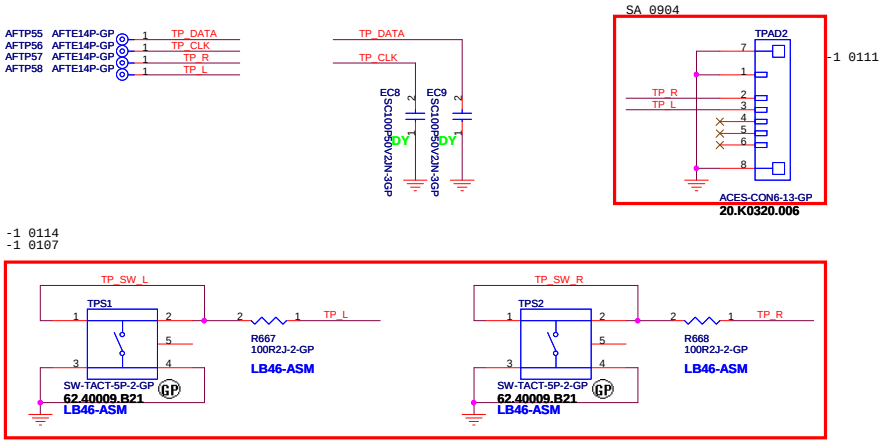


System BIOS Flash ROM

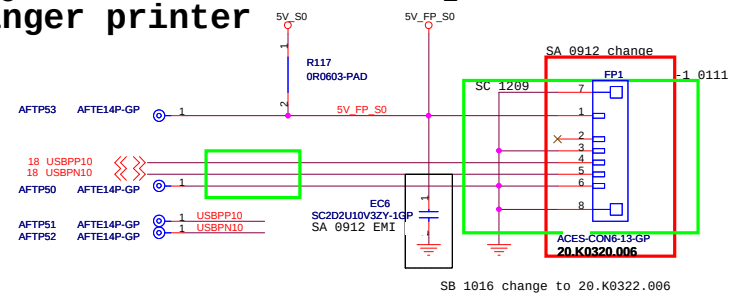


TOUCH PAD

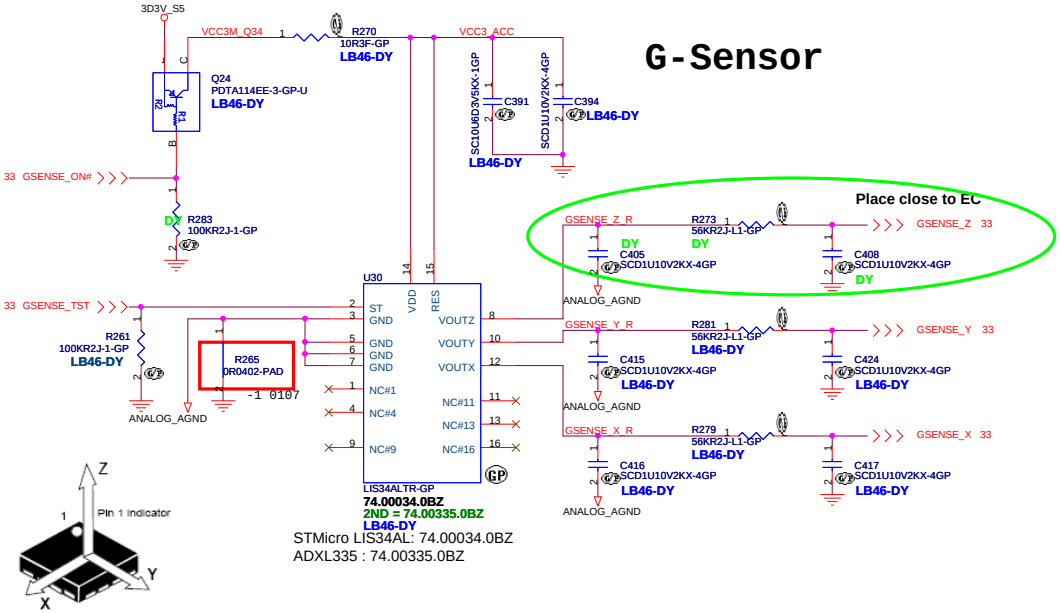




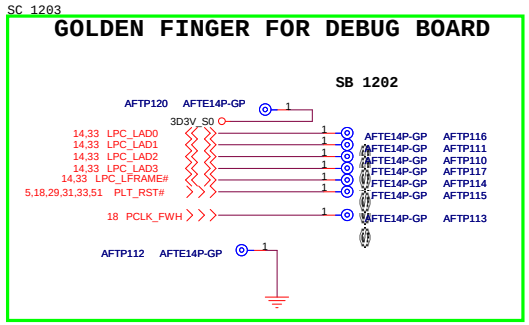
Finger printer



G-Sensor



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 35_BIOS & TP & G-Sensor & FP

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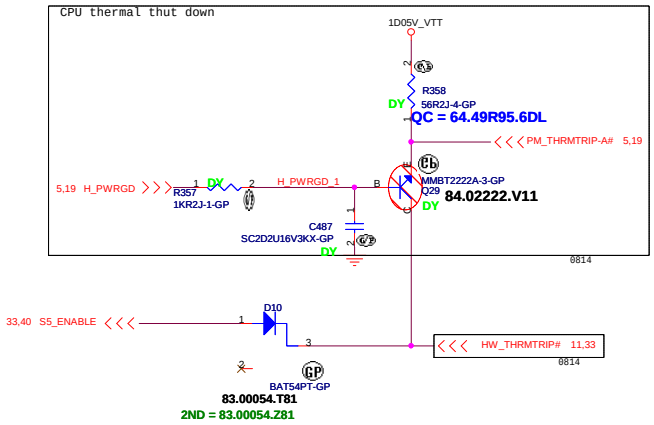
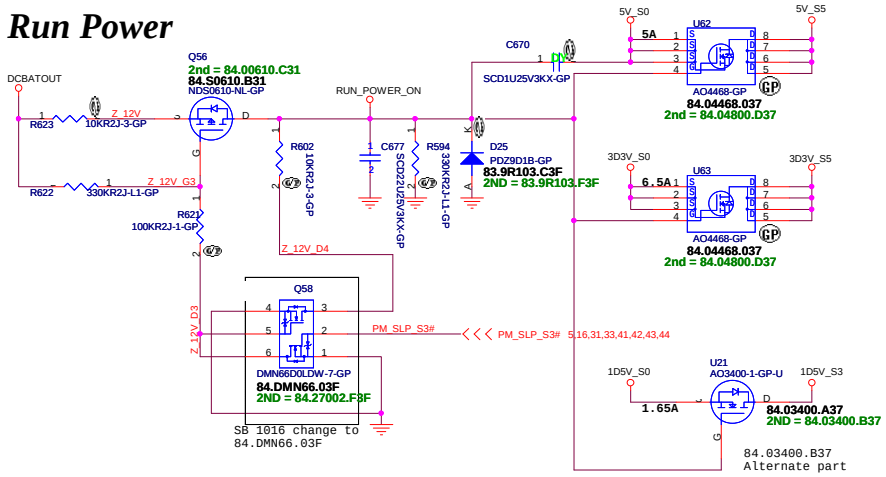
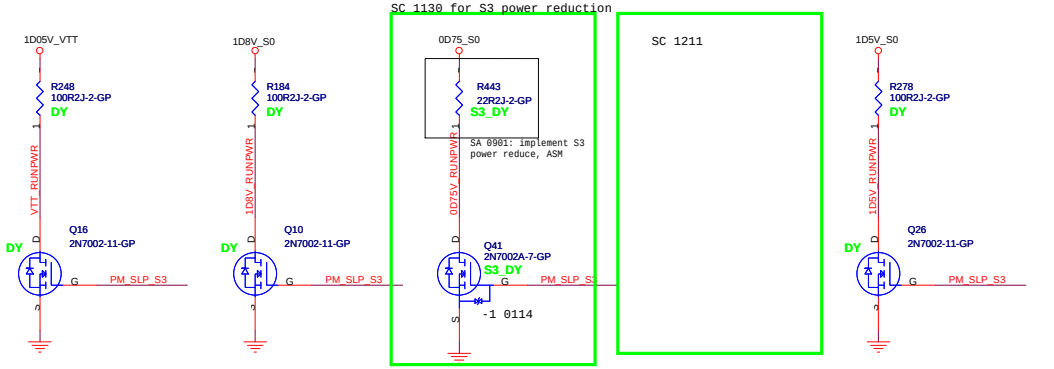
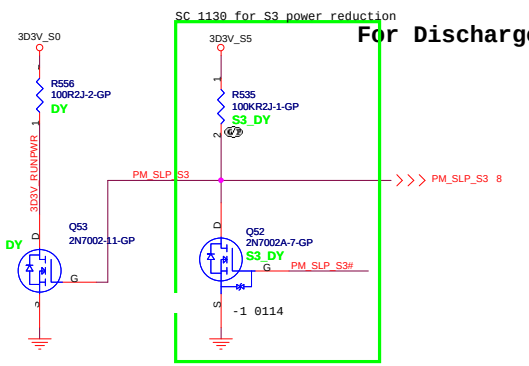
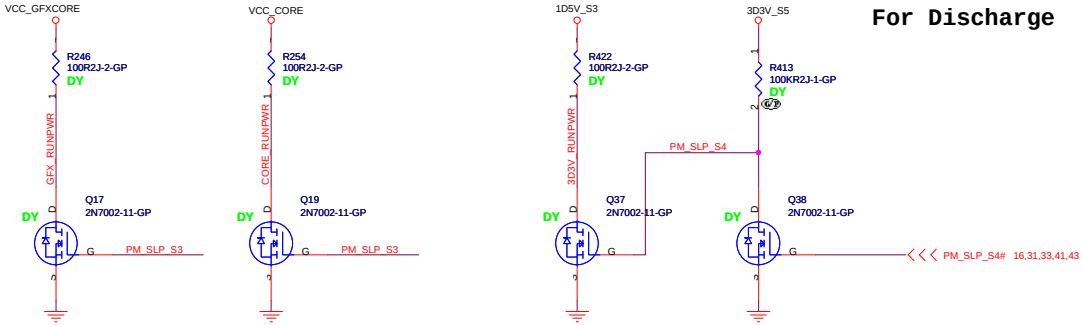


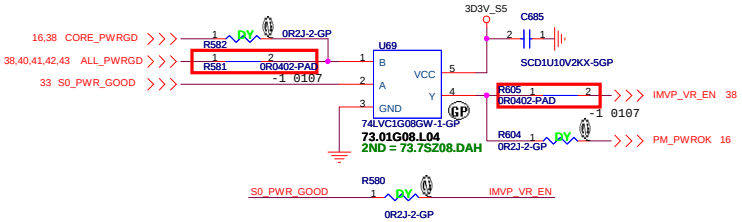








For Discharge



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Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 36_Run PWR

Size	Document Number	Rev
Custom	LA46 MB DIS	-1

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5 4 3 2 1

D D

C C

B B

A A

<Core Design>

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C

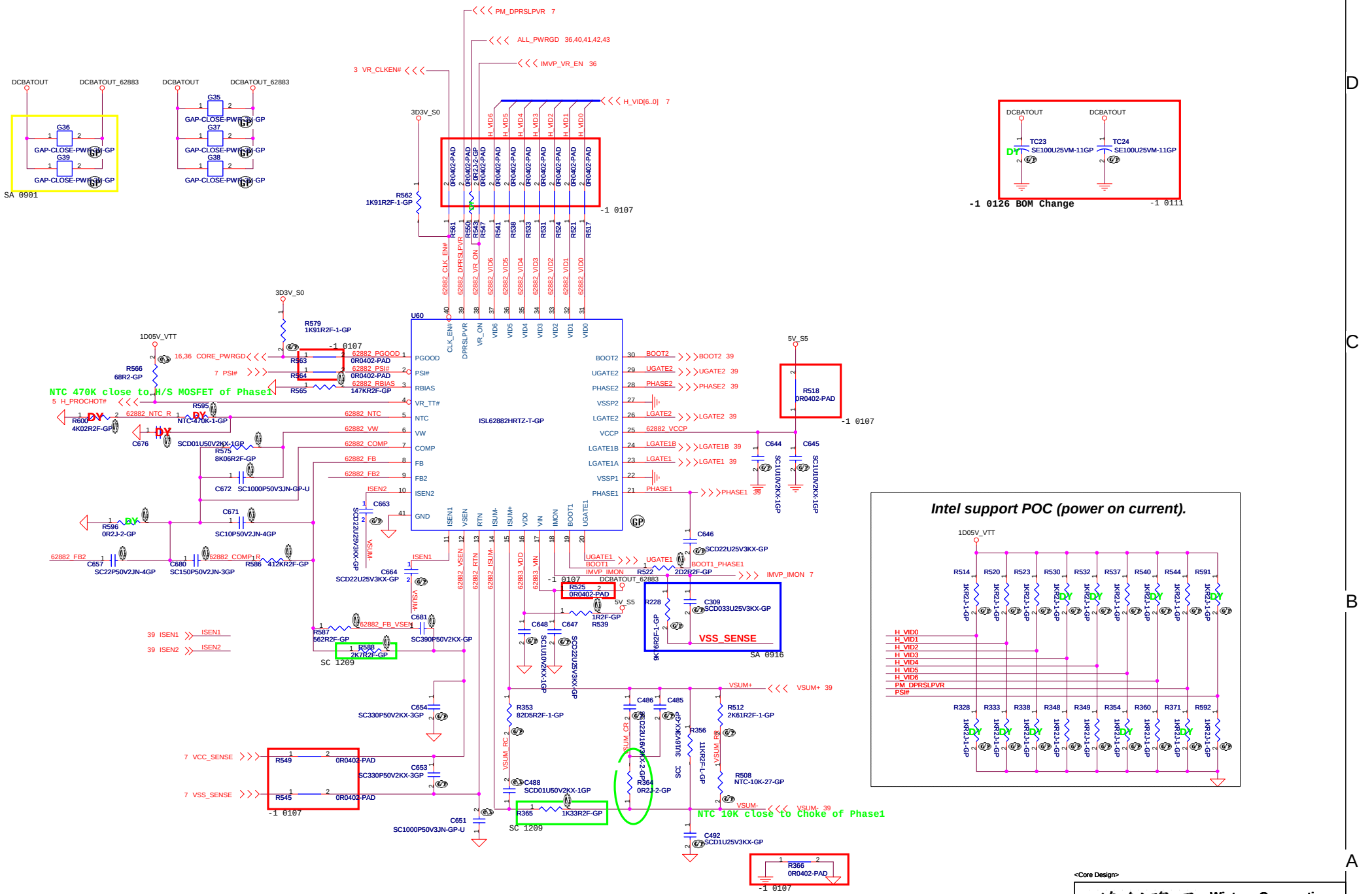
Title

37_BLANK

Size	Document Number	Rev
A3	**LA46 MB**	SA

Date: Tuesday, January 26, 2010 Sheet 37 of 58

5 4 3 2 1



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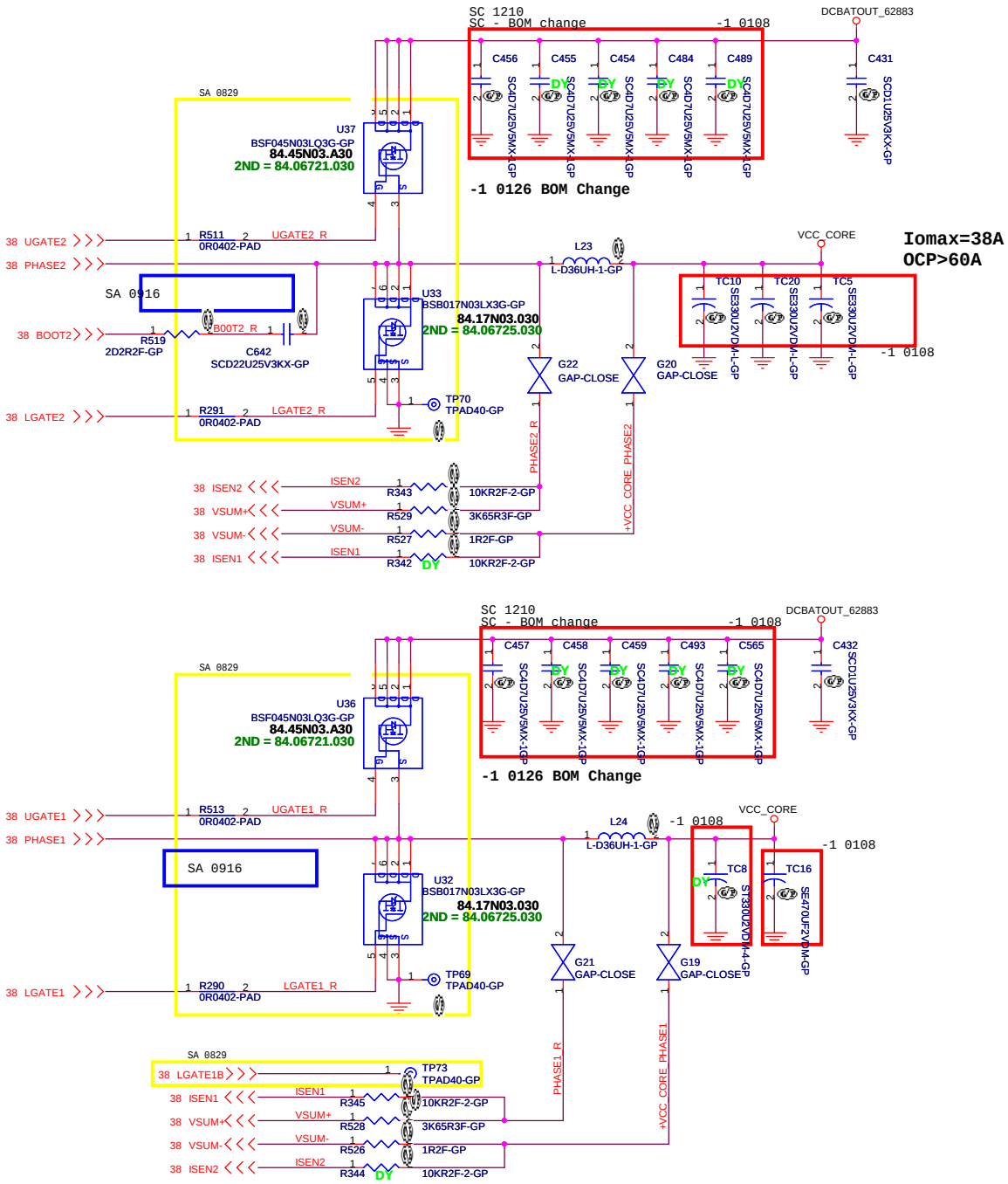
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 38_ISL62882_CPU_CORE (1 of 2)

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 38 of 58



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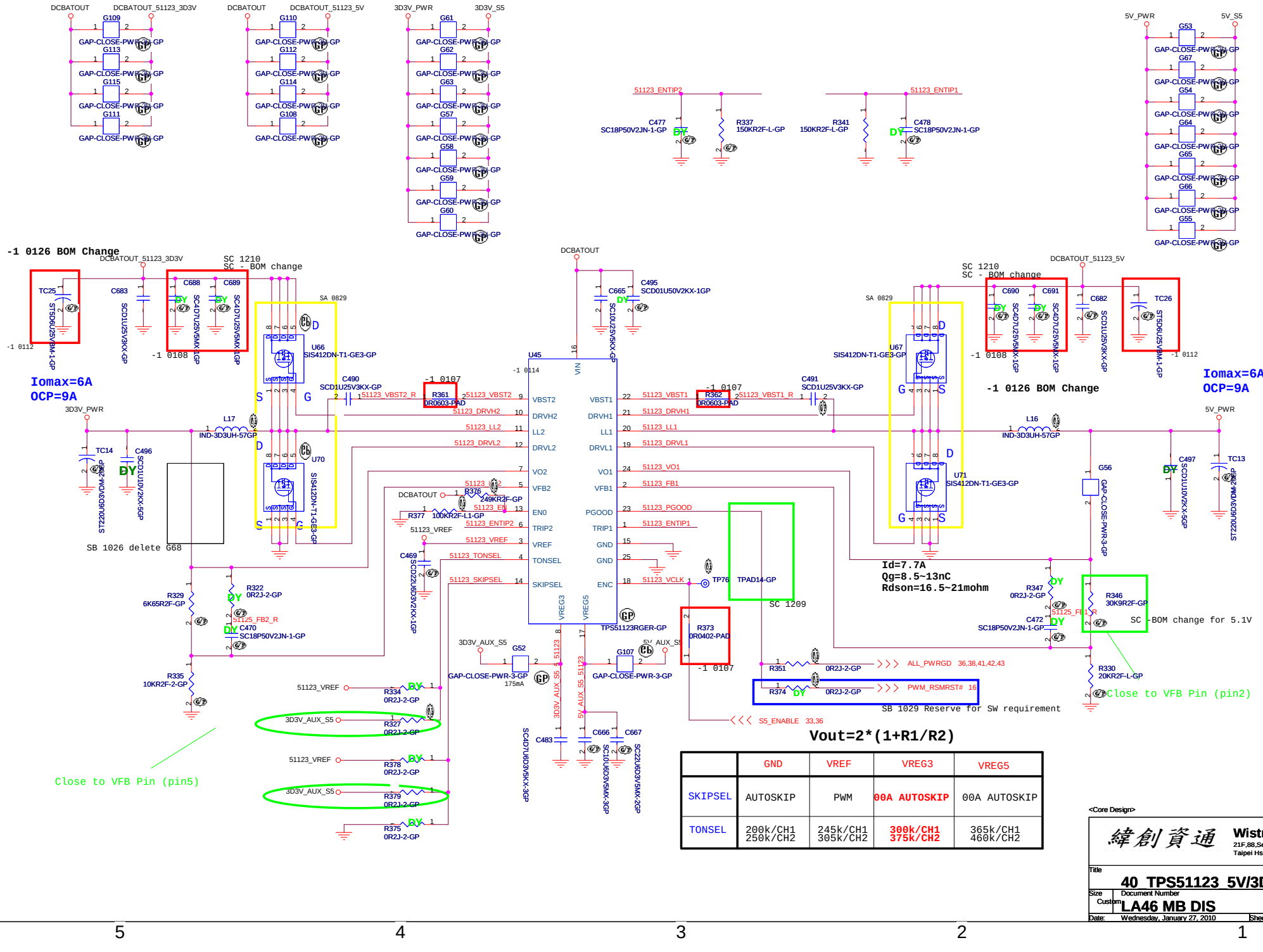
Taipei Hsien 221, Taiwan, R.O.C

Title: 39_ISL62882_CPU_CORE (2 of 2)

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 39 of 58



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TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title: 40_TPS51123_5V/3D3V

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

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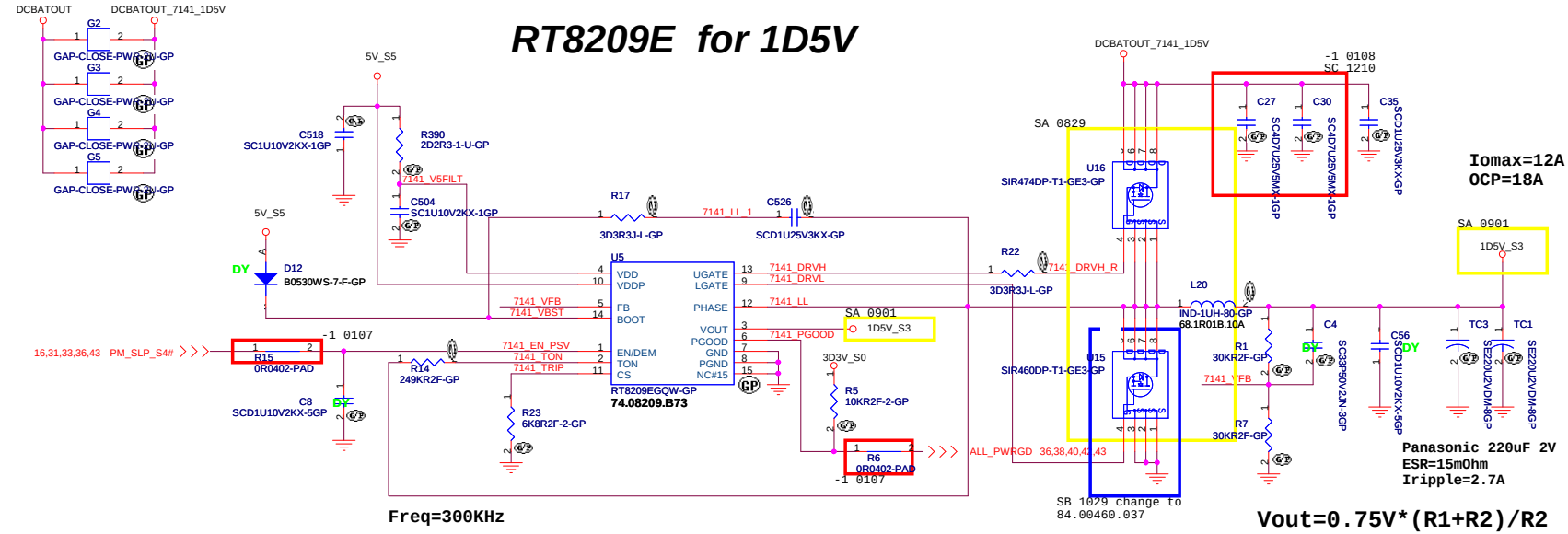
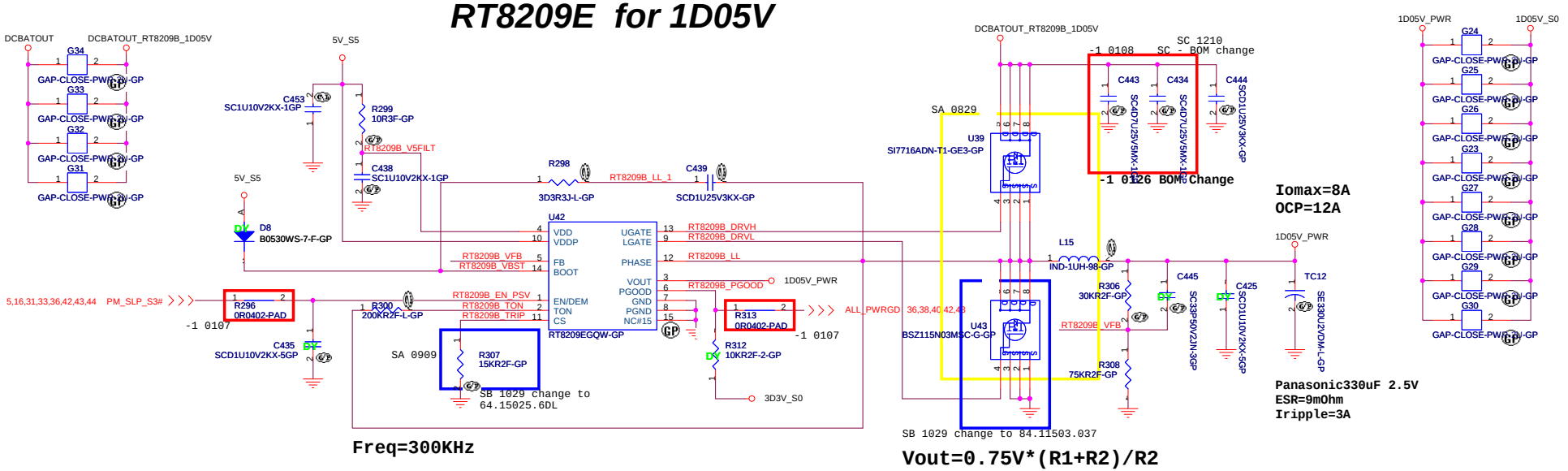
RT8209E for 1D5V



RT8209E for 1D05V



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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 41_RT8209E_1D5V / RT8209E_1D05V

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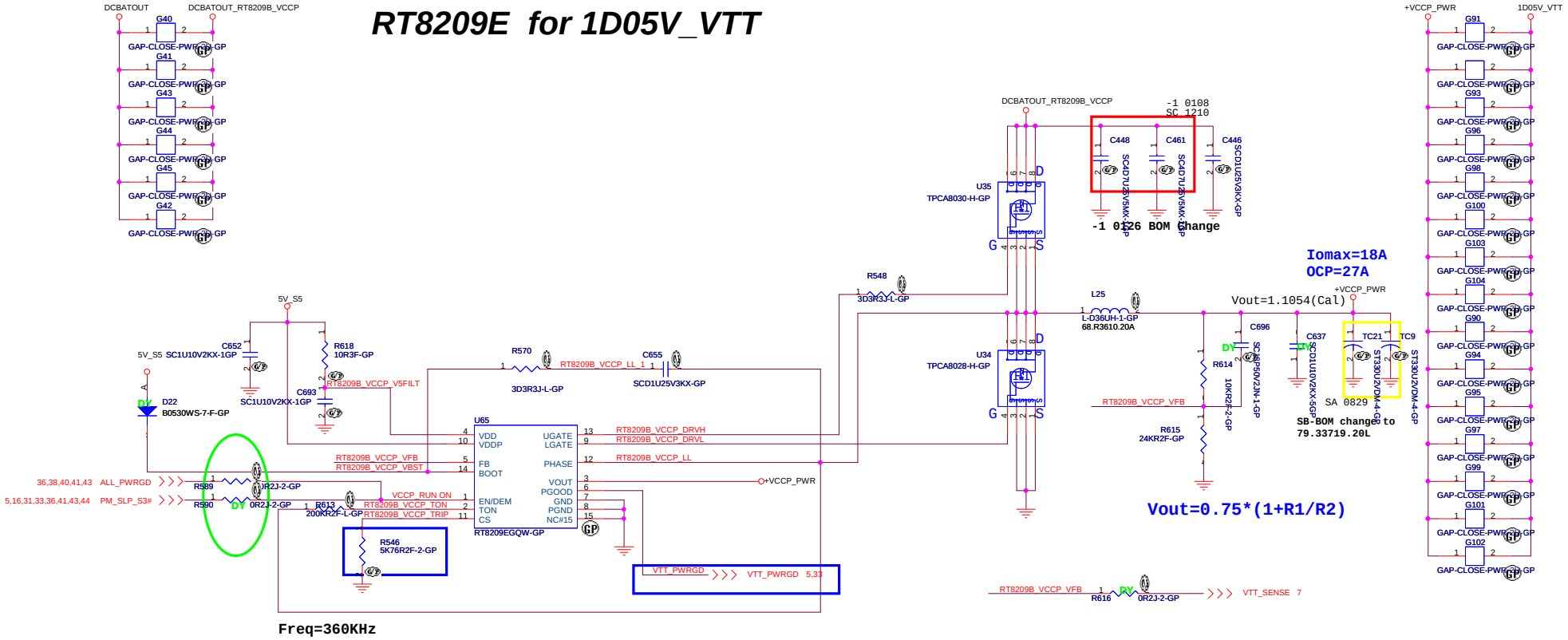
Date: Wednesday, January 27, 2010 | Sheet 41 of 58

RT8209E for 1D05V_VTT



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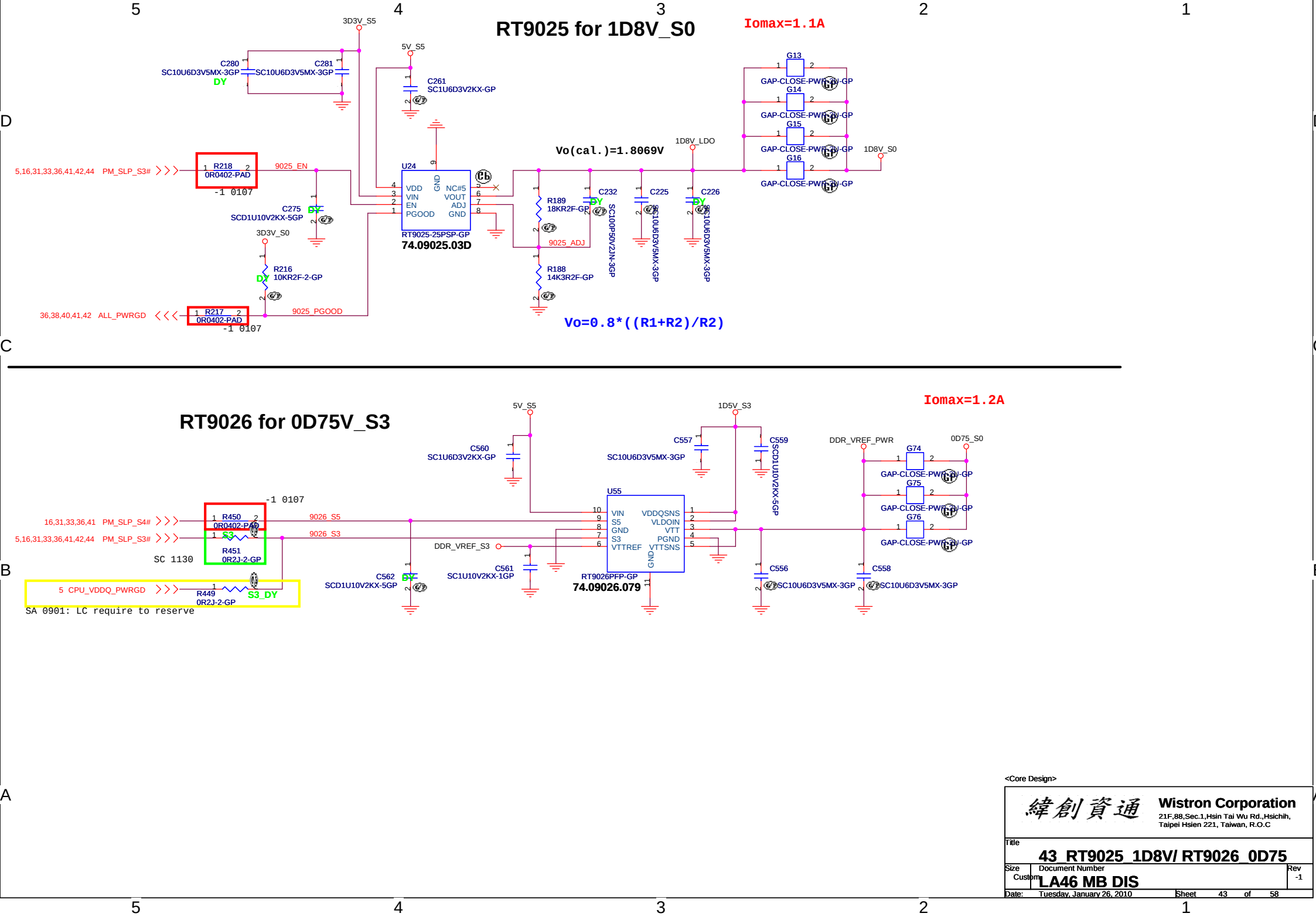
Taipei Hsien 221, Taiwan, R.O.C

Title: 42_RT8209E_1D05V_VTT

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

Date: Wednesday, January 27, 2010 | Sheet 42 of 58



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緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: 43_RT9025_1D8V/ RT9026_0D75

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

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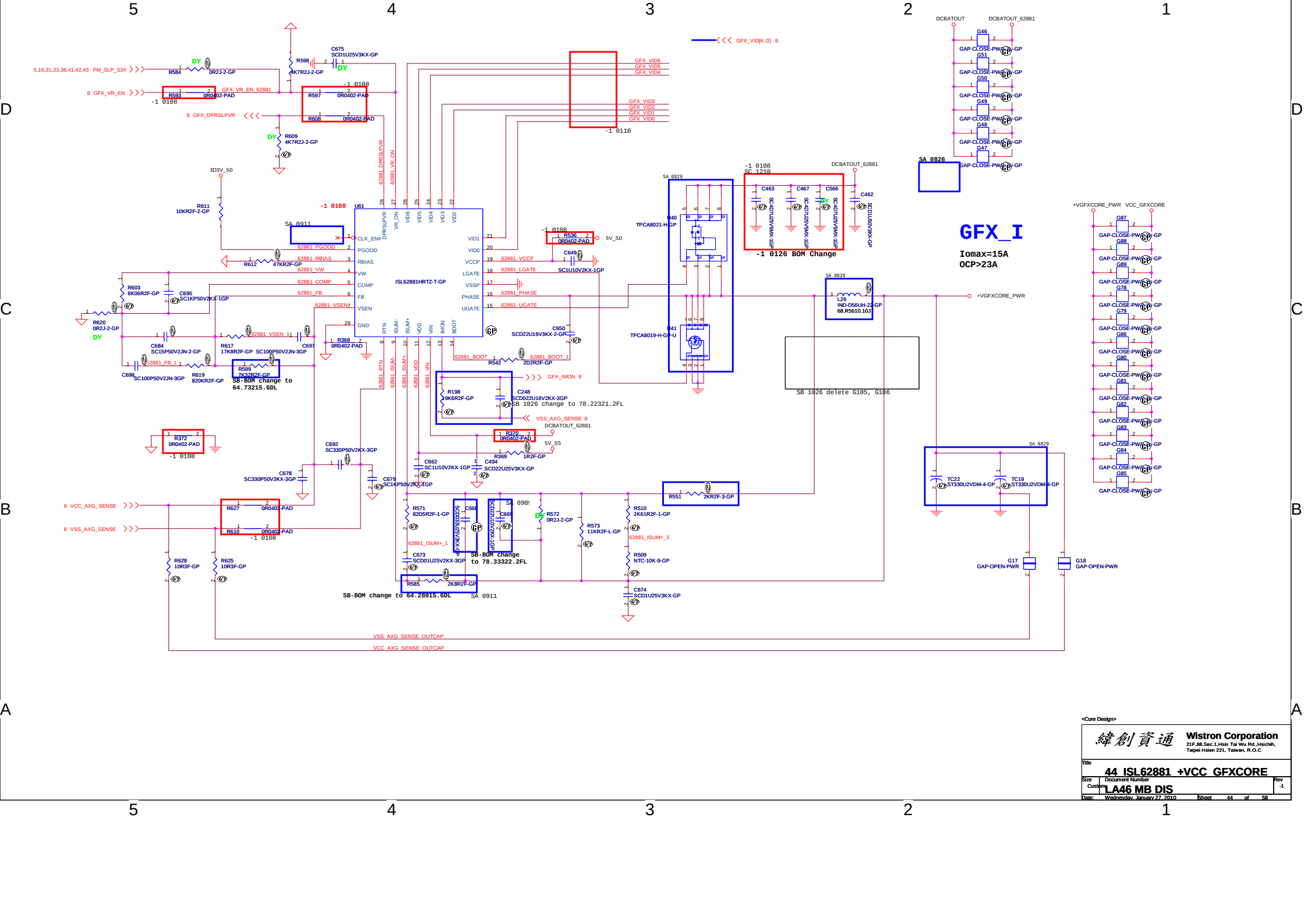
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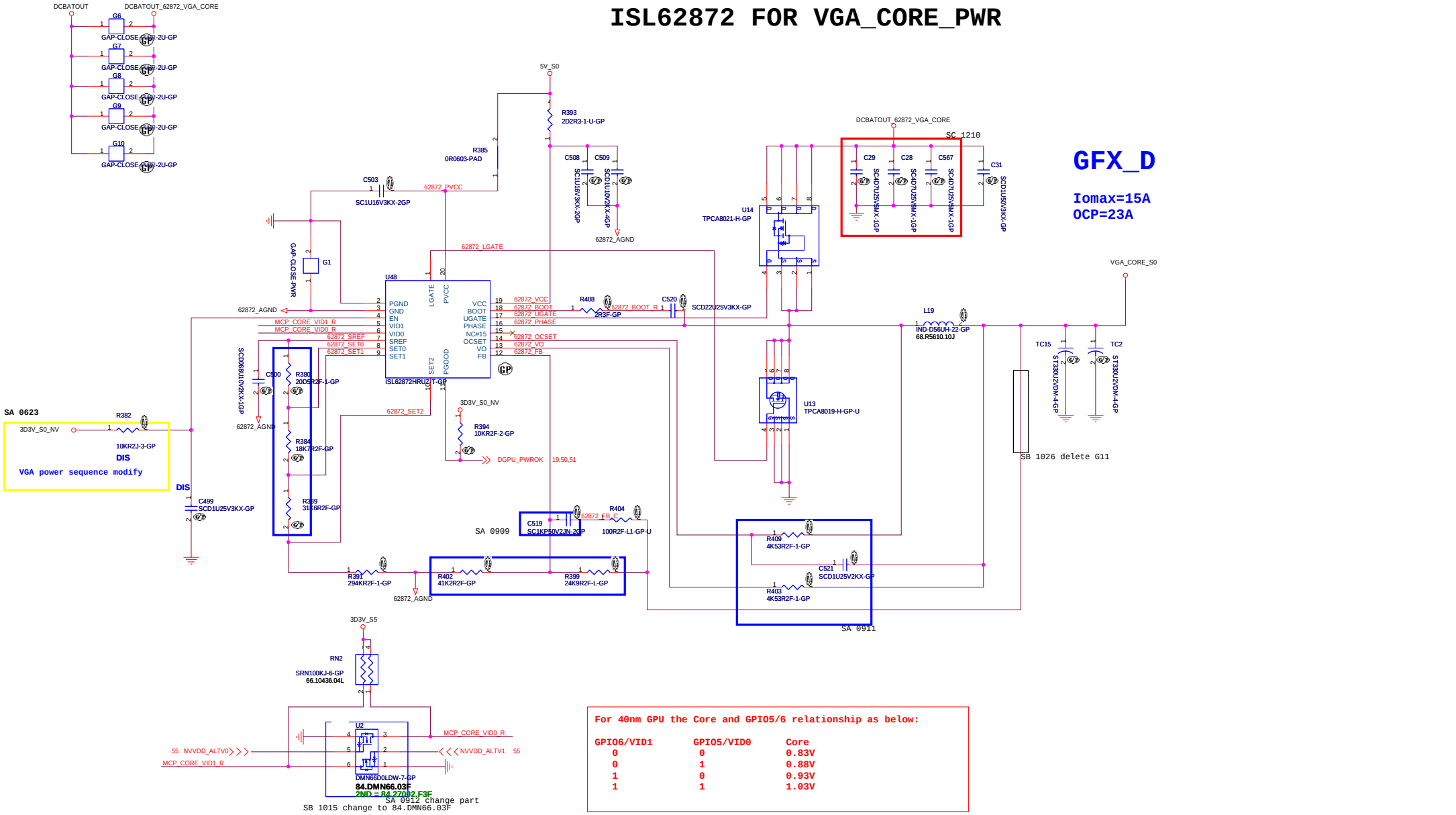
SB 1026 change to 78.22321.2FL
SB 1026 delete G105, G106
SB-BOM change to 78.33322.2FL
SB-BOM change to 64.28015.6DL
-1 0126 BOM Change
SC 1210
+VGFXCORE_PWR
VCC_GFXCORE
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
44_ISL62881_+VCC_GFXCORE
LA46 MB DIS
Wednesday, January 27, 2010

ISL62872 FOR VGA_CORE_PWR



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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title	45_ISL62872_VGA_CORE	
Size: Custom	Document Number: LA46 MB DIS	Rev: -1
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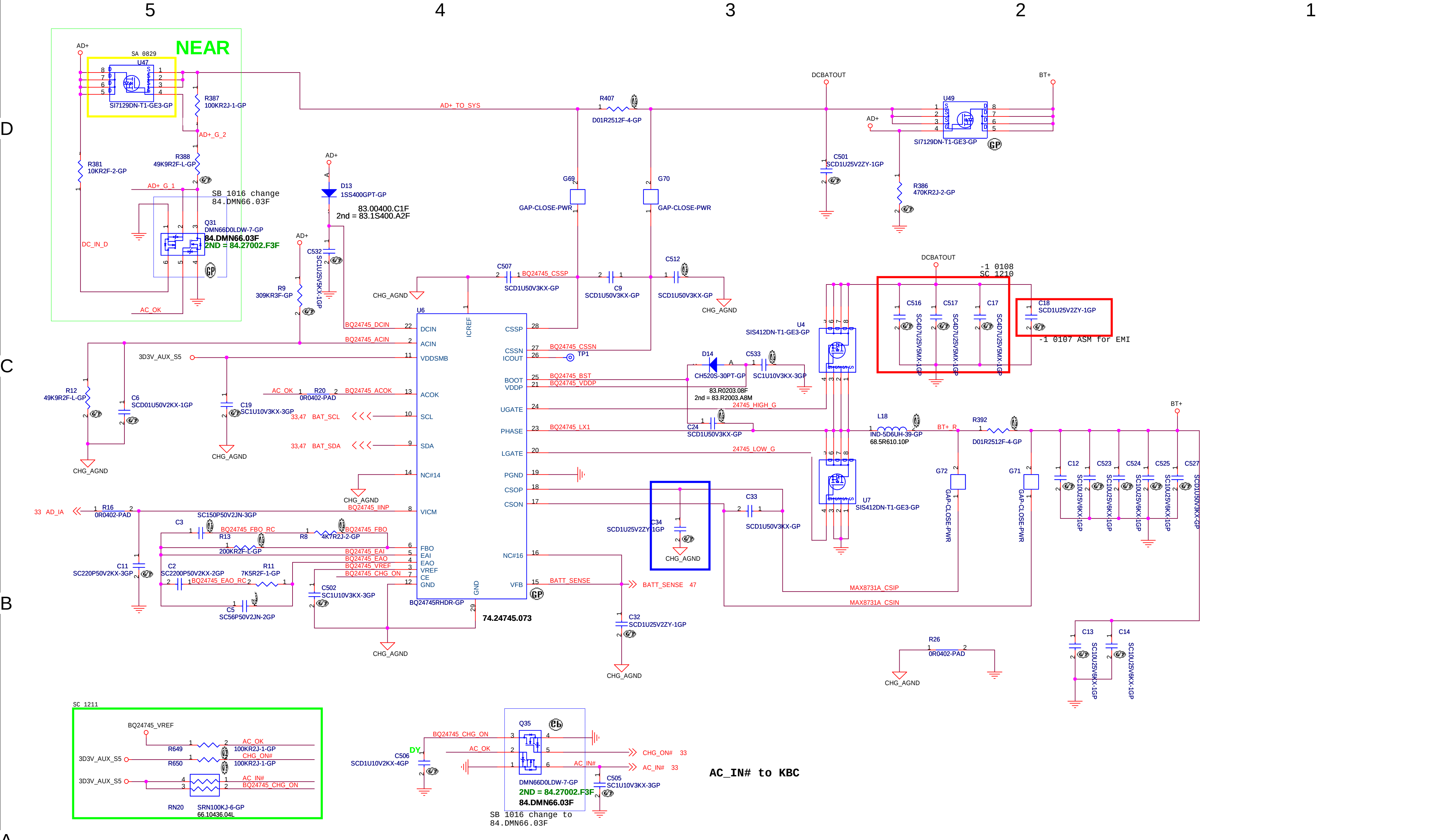

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R387
100KR2J-1-GP
AD+_G_2
R381
10KR2F-2-GP
R388
49K9R2F-L-GP
AD+_G_1
SB 1016 change
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Q31
DMN66D0LDW-7-GP
84.DMN66.03F
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AC_OK
AD+_TO_SYS
R407
D01R2512F-4-GP
D13
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2nd = 83.1S400.A2F
C532
SC1U25V5KX-1GP
R9
309KR3F-GP
G69
GAP-CLOSE-PWR
G70
GAP-CLOSE-PWR
C507
SCD1U50V3KX-GP
C9
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470KR2J-2-GP
BT+
U6
BQ24745RHDR-GP
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ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
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FBO
EAI
EAO
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ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
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CSON
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33,47 BAT_SDA
BQ24745_IINP
33 AD_IA
R16
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C3
R13
200KR2F-L-GP
R8
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BQ24745_EAO
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BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BATT_SENSE
BATT_SENSE 47
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2nd = 83.R2003.A8M
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U7
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C34
SCD1U25V2ZY-1GP
C33
SCD1U50V3KX-GP
C32
SCD1U25V2ZY-1GP
-1 0108
SC 1210
C516
C517
C17
SC4D7U25V5MX-1GP
C18
SCD1U25V2ZY-1GP
-1 0107 ASM for EMI
L18
IND-5D6UH-39-GP
68.5R610.10P
BT+_R
R392
D01R2512F-4-GP
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DY
C506
SCD1U10V2KX-4GP
Q35
DMN66D0LDW-7-GP
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<Core Design>

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21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

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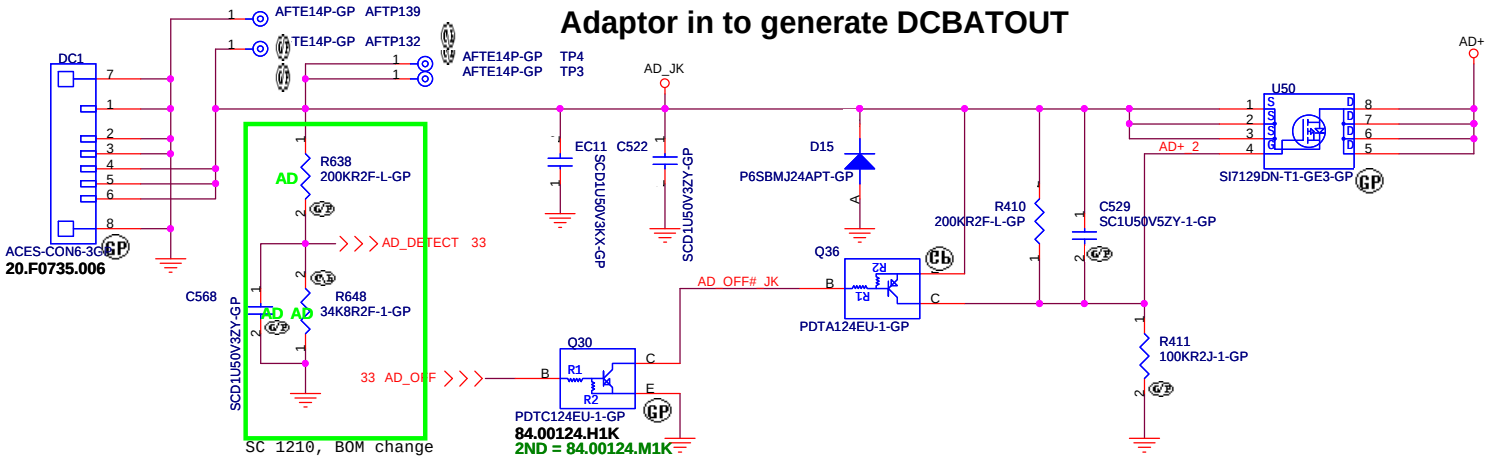
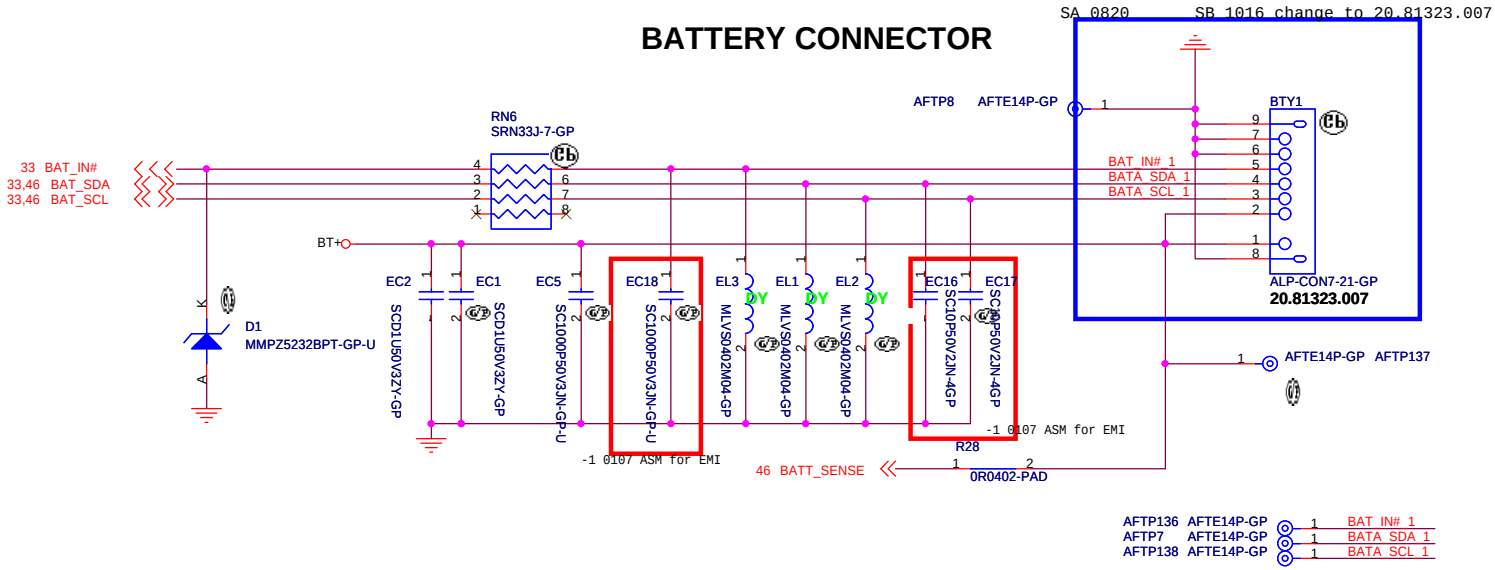
Size: Custom	Document Number: LA46 MB DIS	Rev: -1
Date: Tuesday, January 26, 2010	Sheet 46 of 58	





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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title: 47 AD / BATT CONN

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

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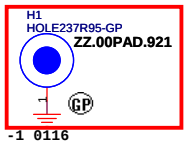

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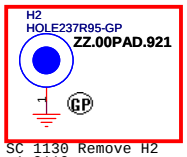

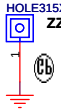

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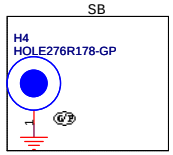

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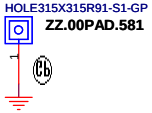

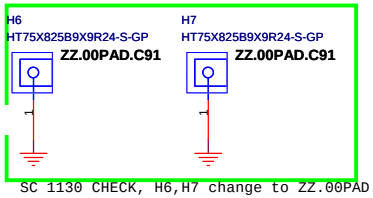

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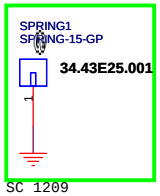

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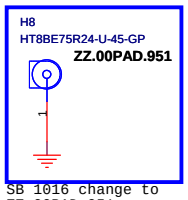

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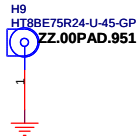

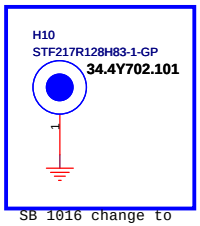

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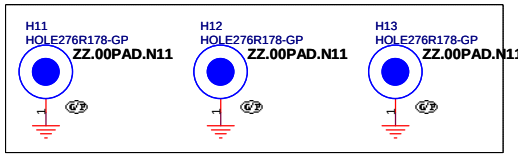

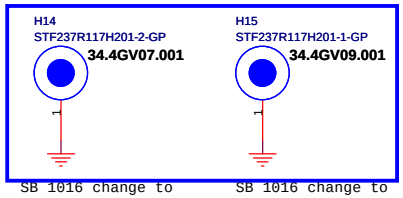

SB 1016 change to
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SB 1016 change to
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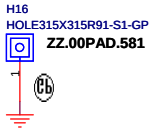

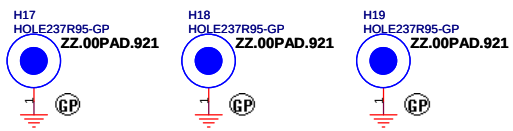

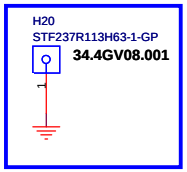

SB 1016 change to
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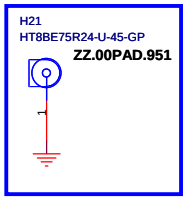

SB 1016 change
to ZZ.00PAD.951

SB 1016 change to
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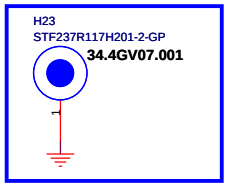
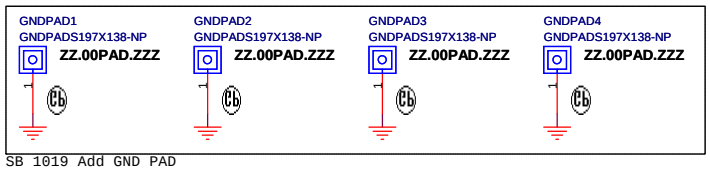
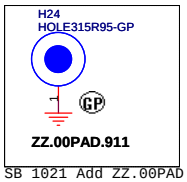


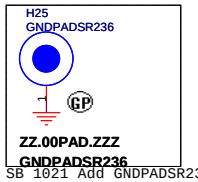
SB 1016 Add 34.4GV07.001



SB 1019 Add GND PAD

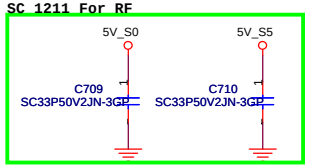


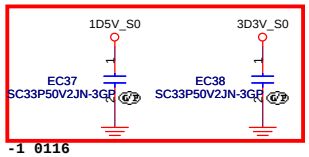
SB 1021 Add ZZ.00PAD.911



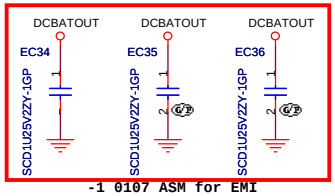
SB 1021 Add GNDPADSR236

SC 1211 For RF





-1 0116



-1 0107 ASM for EMI

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: 48_EMI/Spring/Boss

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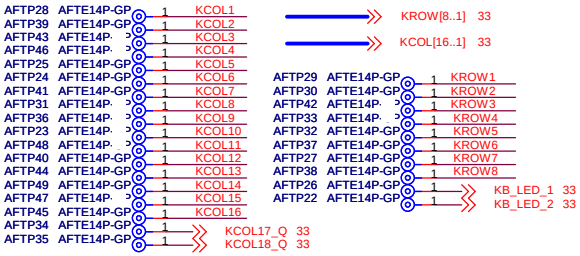
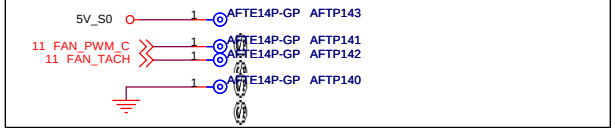
SB_1016_Add_AFTE

Near KB1 Keyboard

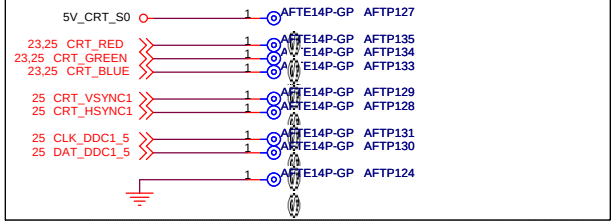


Near FAN1

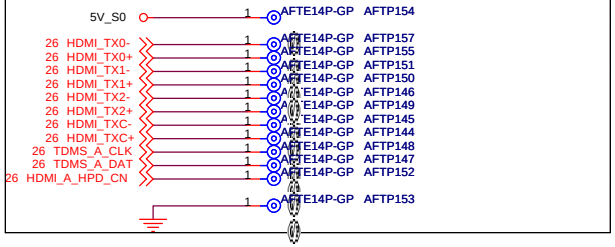


Near RTC1

Near CRT_CN1



Near HDMI_CN1



<Core Design>

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Title: 49_AFTE_TP

Size: A3 | Document Number: LA46 MB DIS | Rev: -1

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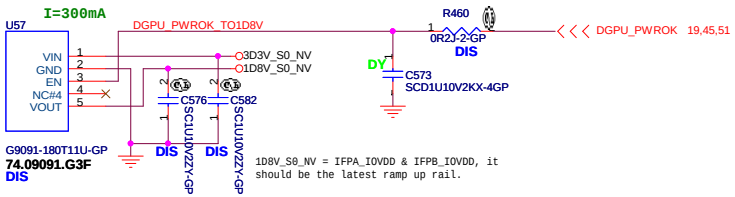
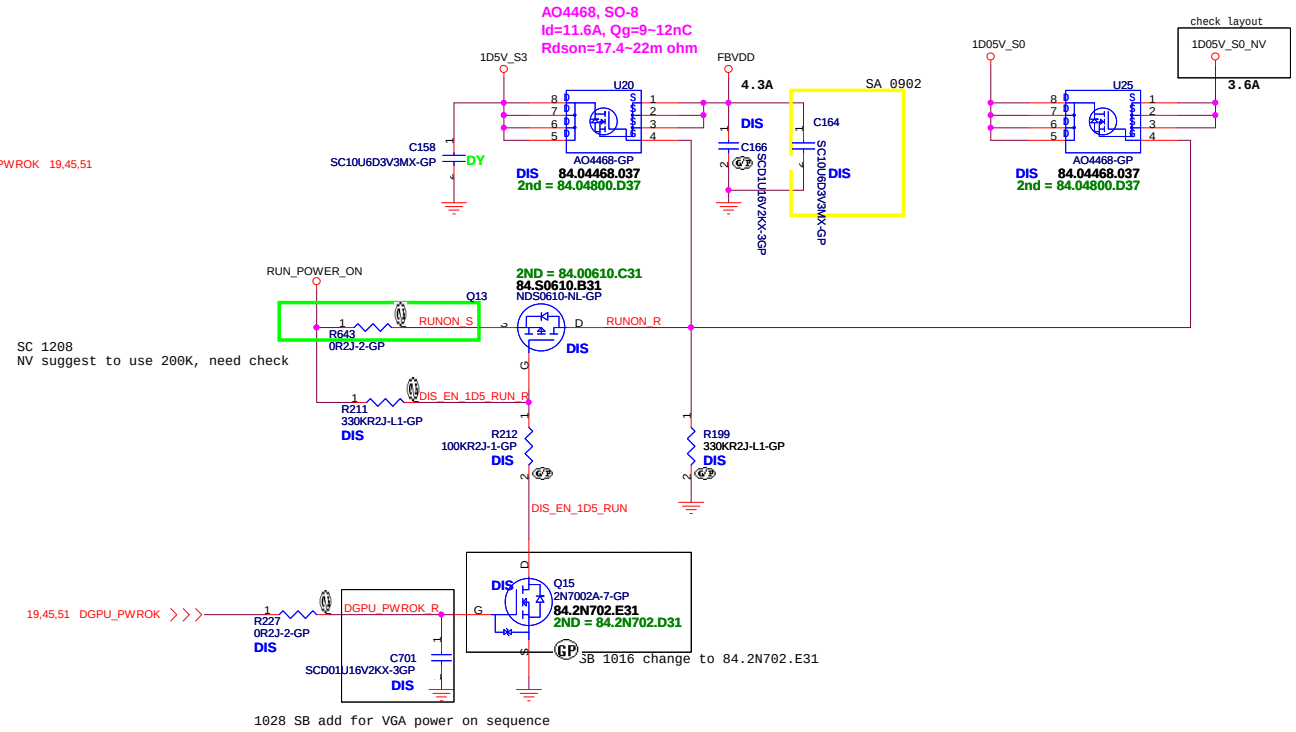
+3VS to 1.8V Transfer

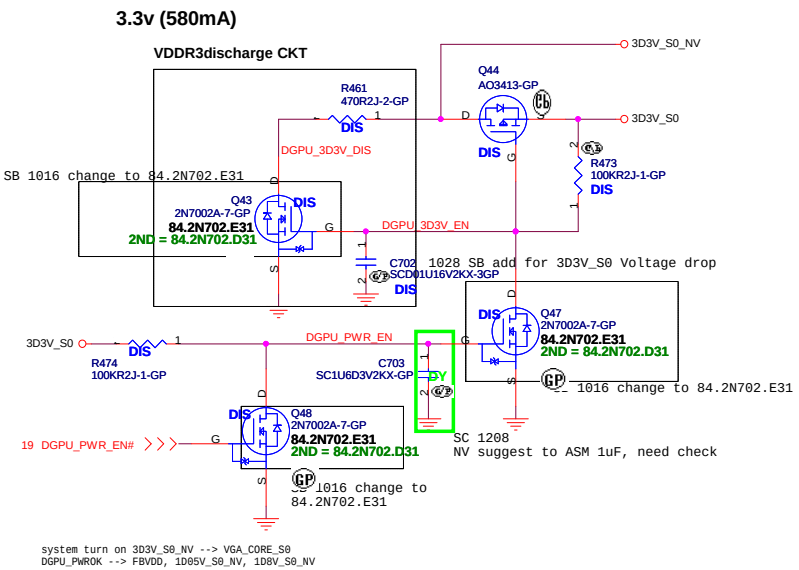


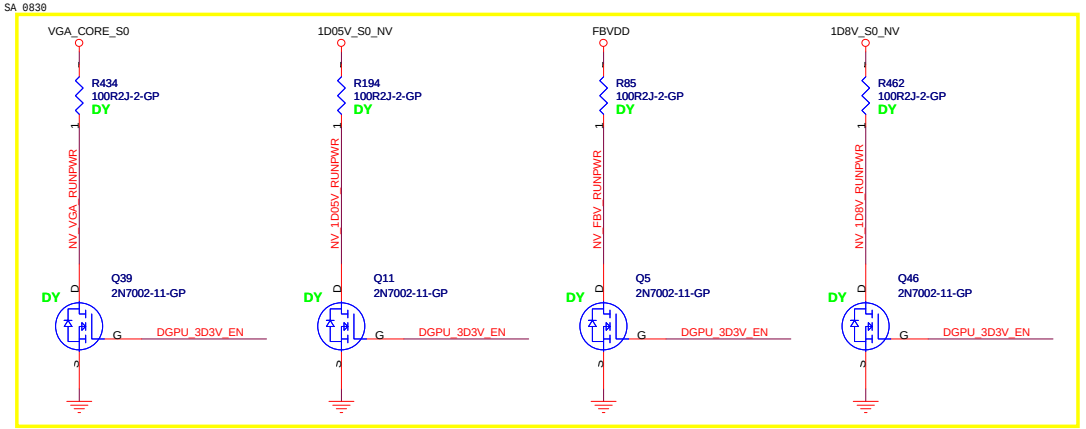
+1.5V to FBVDD Transfer



+1.05V to +1.05V_NV Transfer

+3VS to 3.3V_DELAY Transfer





<Core Design>

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Title: 50_NV power

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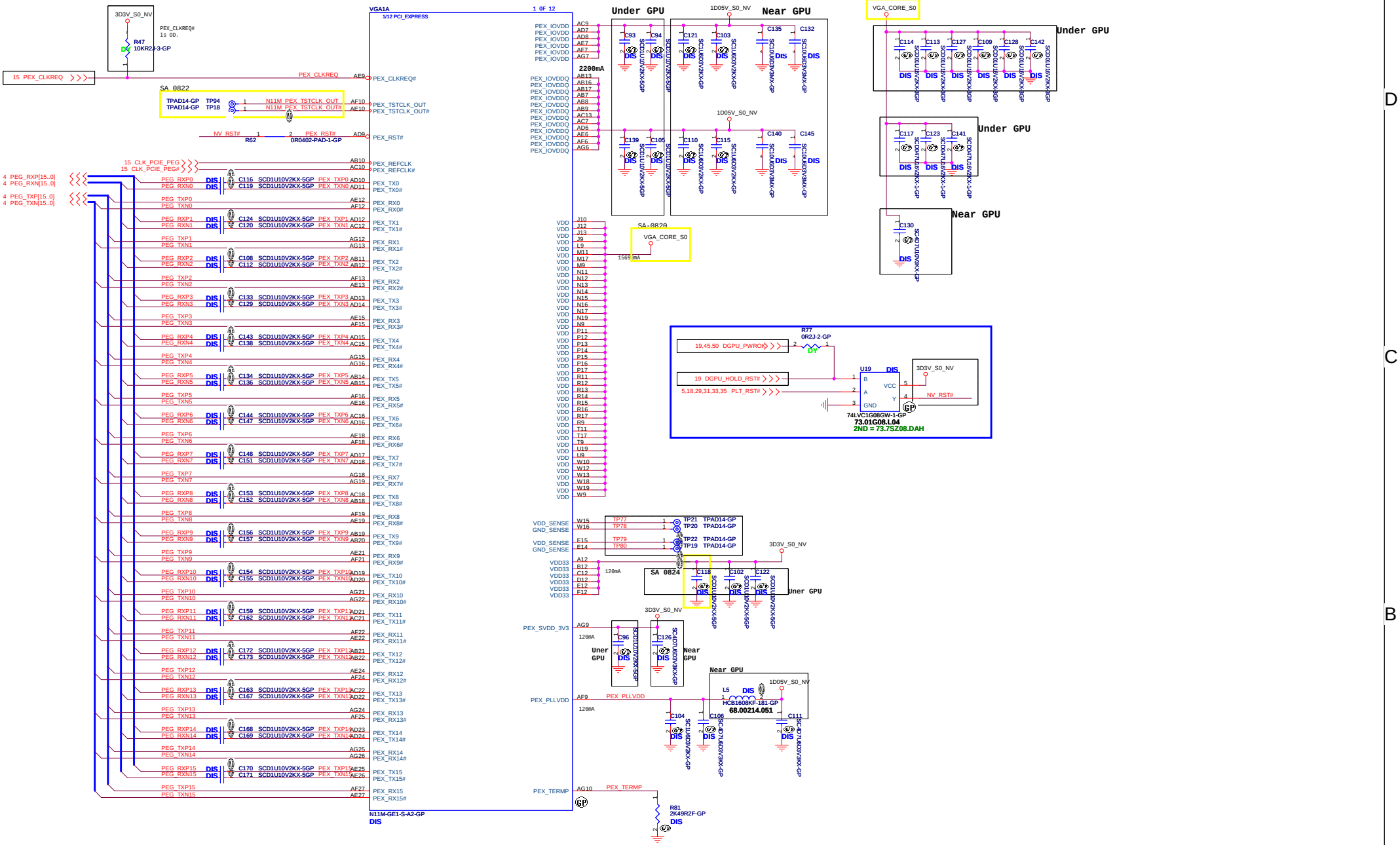
A3? 71.0N11M.C0U



<Core Design>

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Title: 51_N11M(1/6)_PEG

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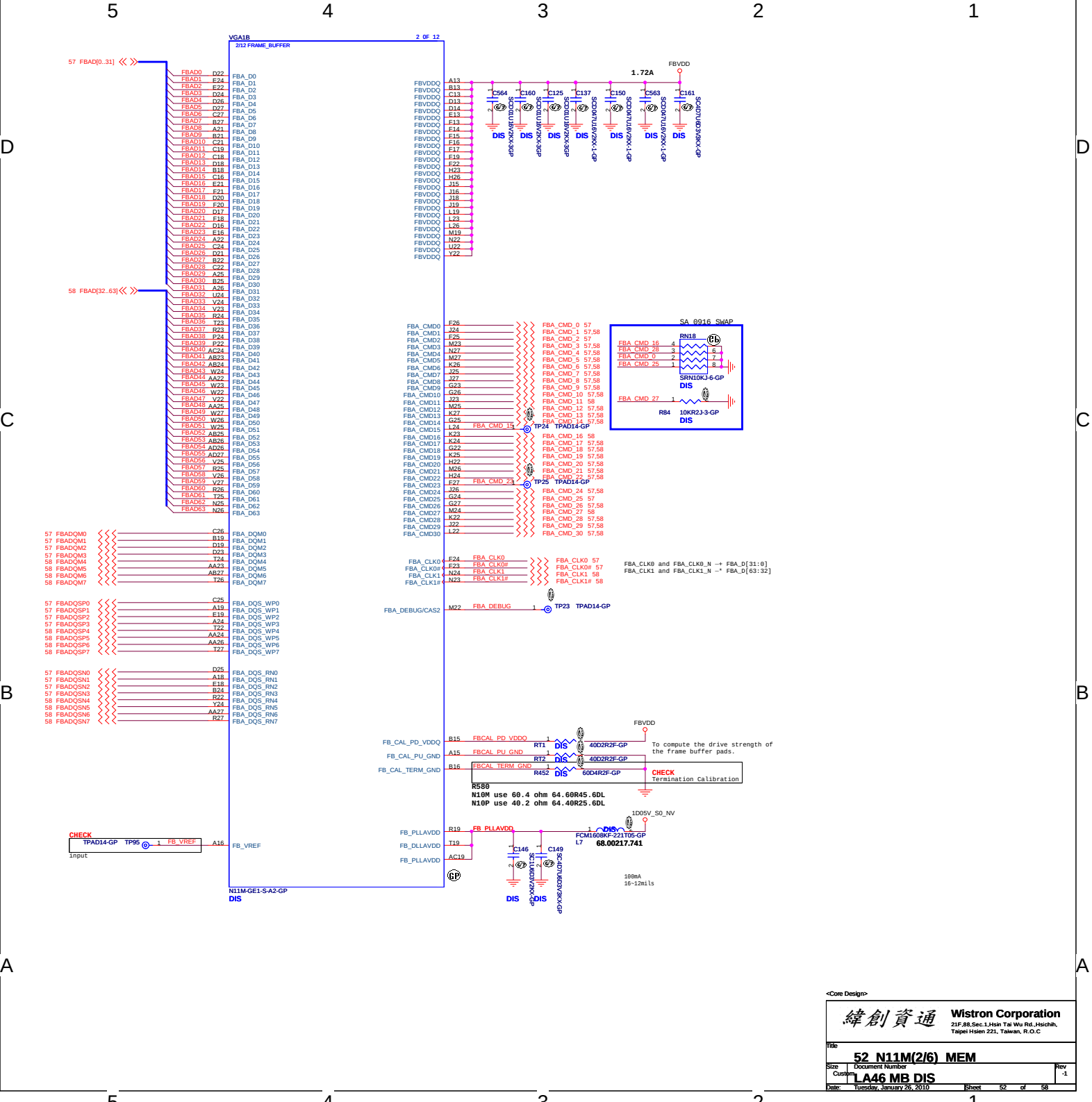

<Core Design>

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Title: 52_N11M(2/6)_MEM

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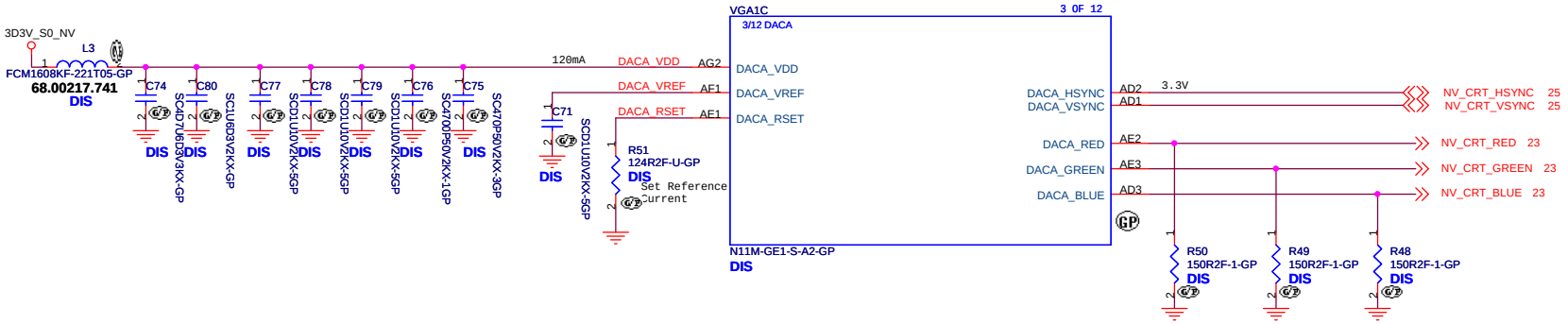

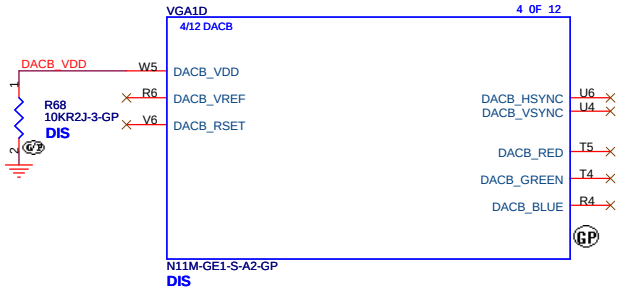

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Title: 53_N11M(3/6)_DAC

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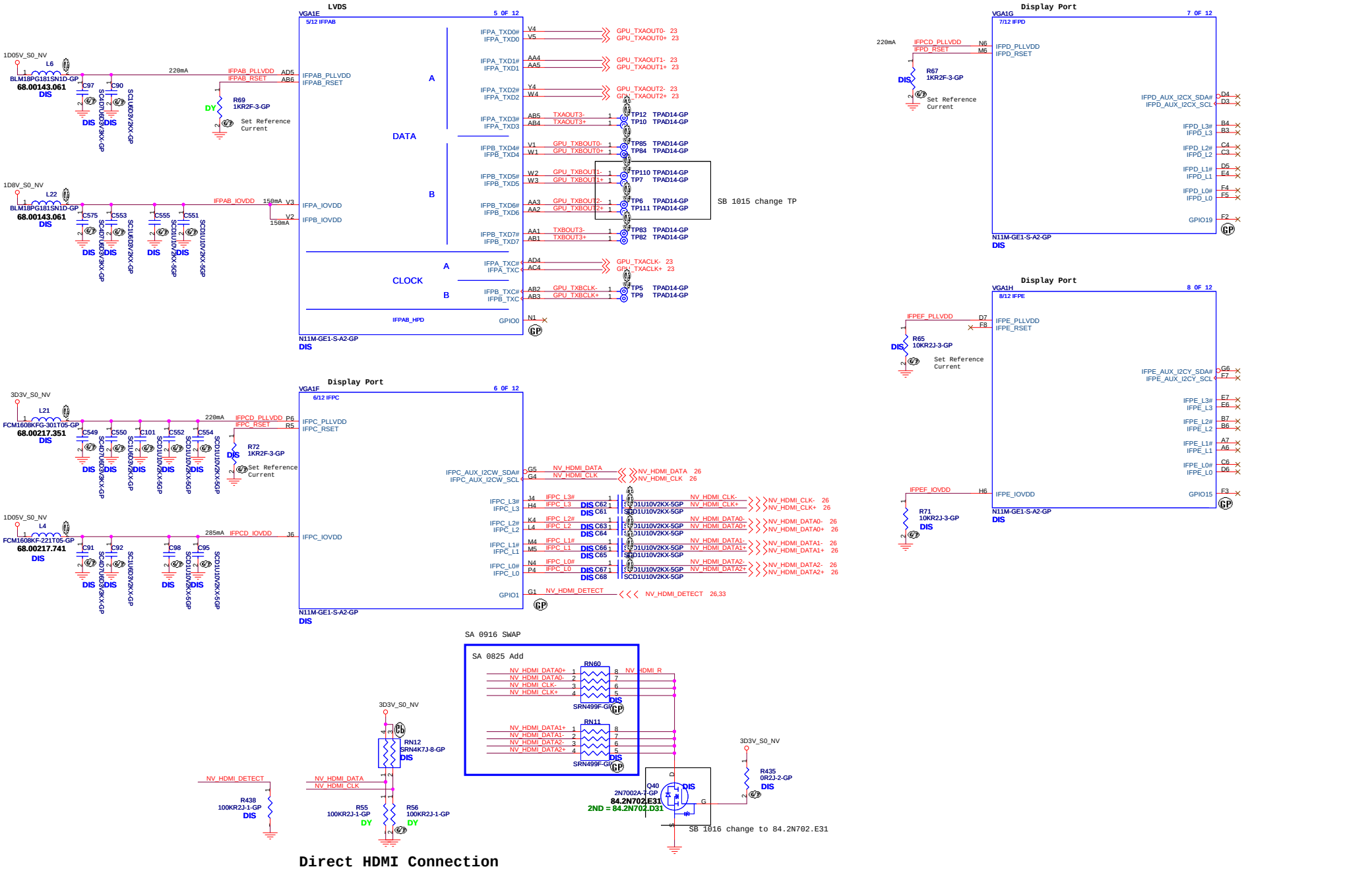

<Core Design>
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Title: 54_N11M(4/6)_IFP

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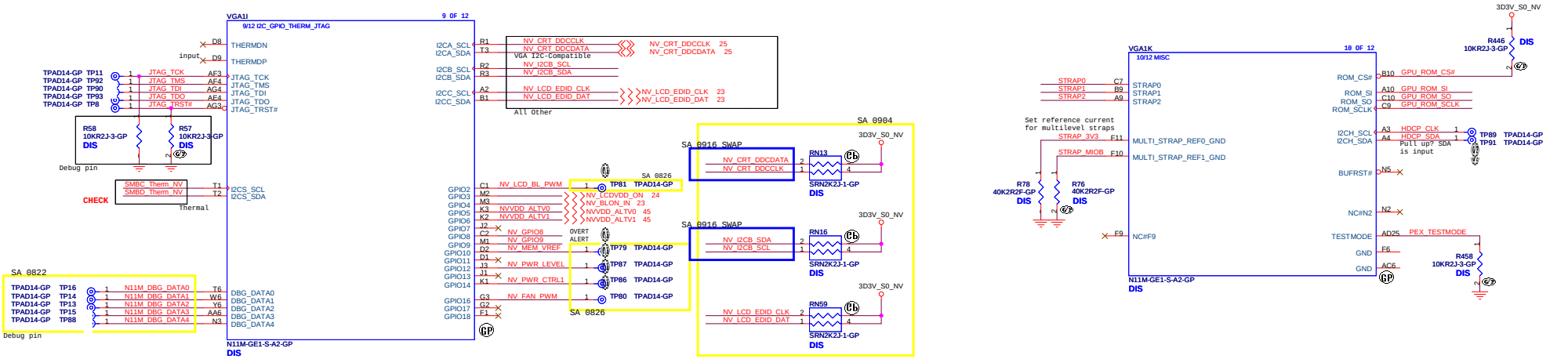
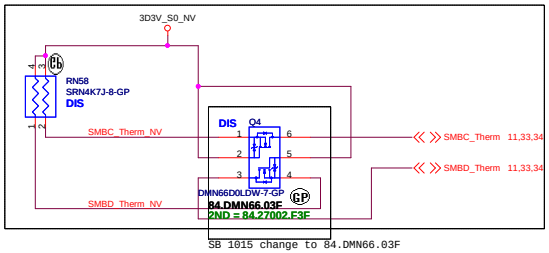
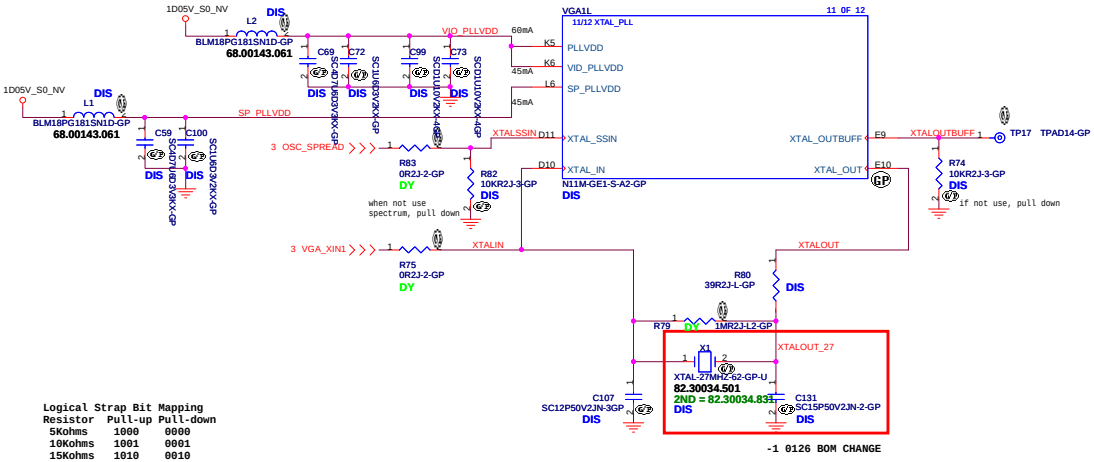






STRAP0

USER[0]=1	DeviceID
USER[1]=1	N11P-LM1(0x0A2B) ?
USER[2]=1	N11M-GE1(0x0A75) 1-0101
USER[3]=1	

STRAP1

3GIO_PADCFG[0]=0	
3GIO_PADCFG[1]=1	
3GIO_PADCFG[2]=1	
3GIO_PADCFG[3]=1	

STRAP2

	N11M-LP1	N11M-GE1
PCI_DEVID[0]=1	[0] 1	1
PCI_DEVID[1]=0	[1] 1	0
PCI_DEVID[2]=1	[2] 0	1
PCI_DEVID[3]=0	[3] 1	0

GPU_ROM_SI

for Hynix VRAM	for Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=0
RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

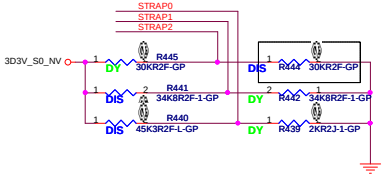
VGA_DEVICE	=1
SMB_ALT_ADDR	=0
FB_0_BAR_SIZE	=0
XCLK_417	=0

GPU_ROM_SCLK

		N11M-LP1	N11M-GE1
PEX_PLL_EN_TERM	=0		
SLOT_CLK_CFG	=1		
SUB_VENDOR	=0		
PCI_DEVID[4]	=1	[4] 0	1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111



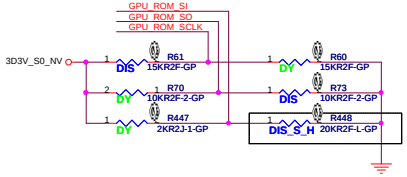


TABLE
KENDO VIDEO MEMORY

	SAMSUNG 0011	HYNIX 0010
R448	20KOHM 64.20025.6DL	15KOHM 64.15025.6DL

<Core Design>

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Title: 55_N11M(5/6)_STRAP/ GPIO

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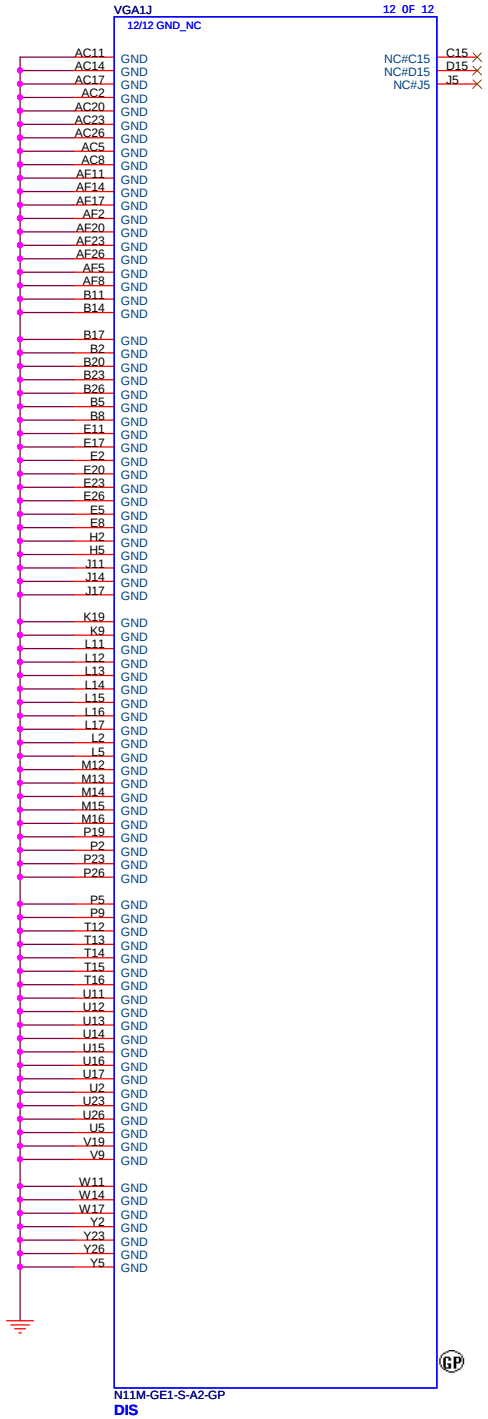

<Core Design>

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Title: 56_N11M(6/6)_GND

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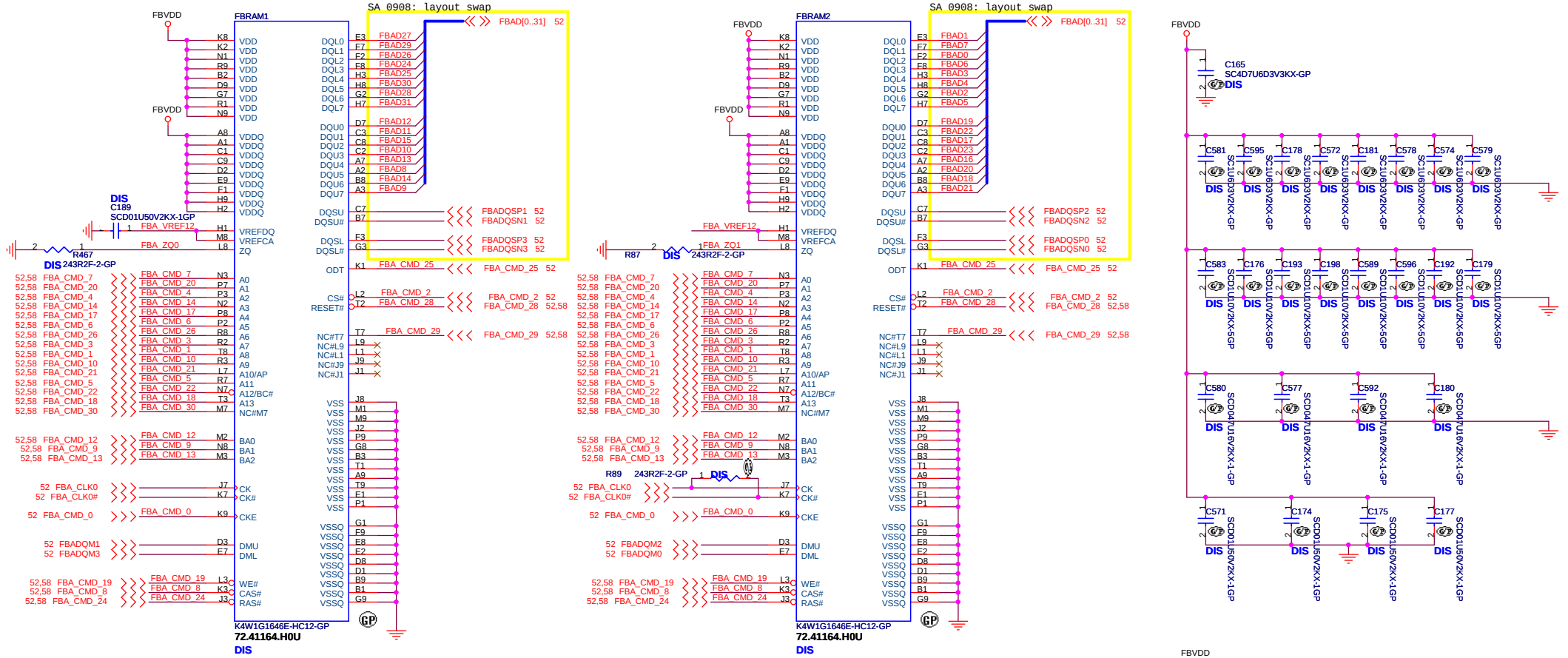
Mode C Command Mapping



2nd: 72.51G63.C0U (IC SDRAM H5TQ1G63BFR-12C FBGA)

SB 1031 change to 78.22520.5BL

<Core Design>

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Title: 57_VRAM(1/2)

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

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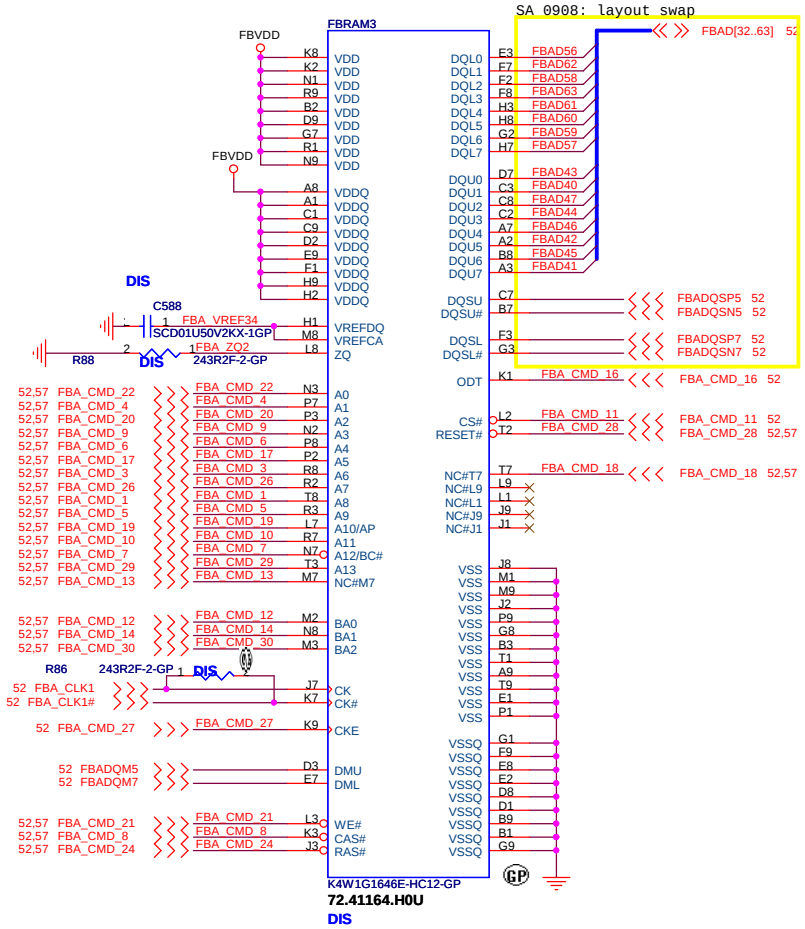

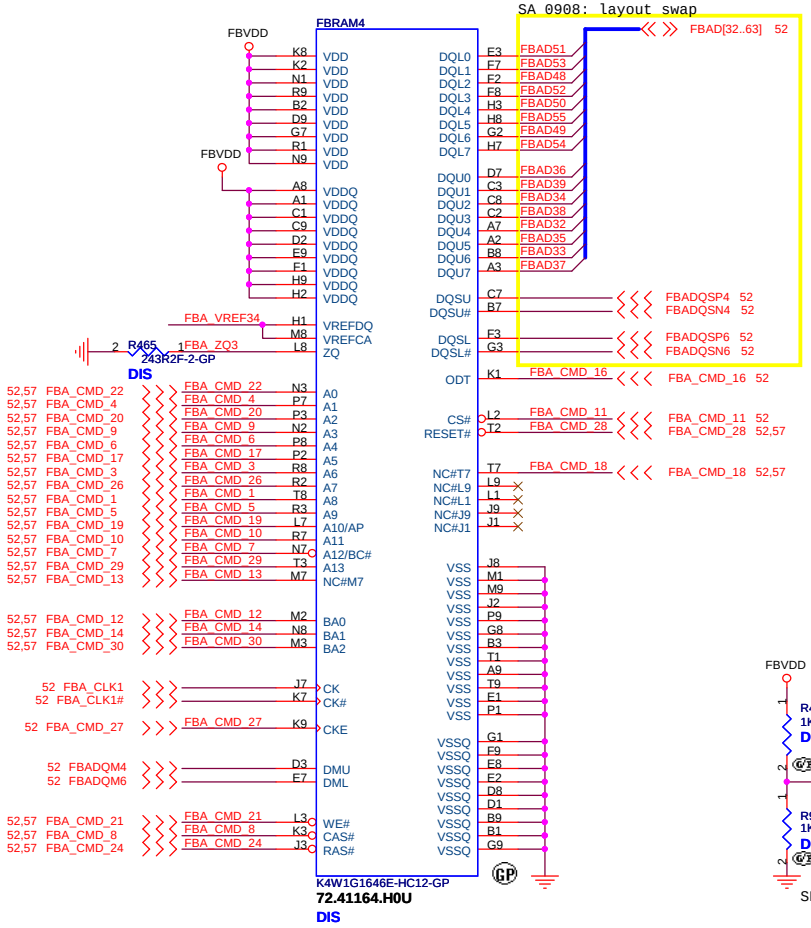

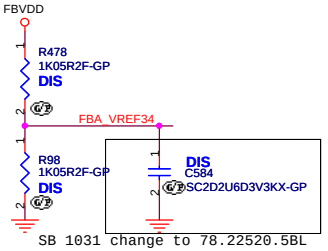

<Core Design>

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Title: 58 VRAM(2/2)

Size: Custom | Document Number: LA46 MB DIS | Rev: -1

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