UMA & Optimus Schematics Document

Sandy Bridge

Intel PCH

2010-08-16

REV : SB

DY :None Installed
UMA:UMA platform installed
OPS:Optimus

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A3	Document Number: LA470	Rev: SB
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Block Diagram (UMA/Optimus co-lay)

Audio BD

POWER BD

Finger Printer BD

IO BD (Cardreader+Audio+USB)

LED BD

USB

##OnMainBoard

VRAM 2GB/1GB/512MB 88,89,90,91

DDR3 800MHz

NVIDIA N12P-GE/GV N12M-GE 83.84,85,86,87

PCIe x 16 (Discrete only)

Intel CPU

Sandy Bridge

DDRIII: 1066/1333/1666 MHz

4,5,6,7,8,9,10

DDRIII 1066/1333/1666 Channel A

DDRIII 1066/1333/1666 Channel B

DDRIII Slot 0 1066/1333/1666 14

DDRIII Slot 1 1066/1333/1666 15

Project code : 91.4KZ01.001
PCB P/N : 48.4KZ01.0SB
Revision : 10250-SB

HDMI 51

LCD 49

CRT 50

HDMI

LVDS

RGB CRT

FDI x 4 x 2 (UMA only)

DMI x 4

Intel PCH Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25

PCIE x 1 → GLAN RTL8111E 31 → RJ45 CONN 55

PCIE x 1/USB2.0 x 1 → Mini-Card WLAN 65

SATA x 1/USB2.0 x 1 → Mini-Card WWAN 66 → SIM 66

USB 2.0 x 3 → MB USB x 3

USB 2.0 x 1/SATA x 1 → E-SATA/USB comb 57

SATA x 2 → HDD 56

SATA x 2 → ODD 56

Bluetooth 63

USB2.0 x 3

CAMERA 49

Finger Print BD

Finger Print 64

I/O BD

SD/MMC+/MS/MS Pro/xD 74

CardReader Realtek RTS5139

USB 2.0 x 1

AZALIA

Internal DMIC

HP1

MIC IN

Azalia CODEC Codec_ALC272 29

2CH SPEAKER

SPI

Flash ROM 4MB 60

LPC Bus

LPC debug port 71

KBC NUVOTON NPCE795G 27

SMBus

G-Sensor 79

Touch PAD 69

Int. KB 69

Thermal EMC2103-2-AP 28

Fan 28

SYSTEM DC/DC RT8208A 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51218 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208A 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8015B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

<Core Design>

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	n

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

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Title: **Table of Content**

Size	Document Number	Rev
A3	LA470	SB

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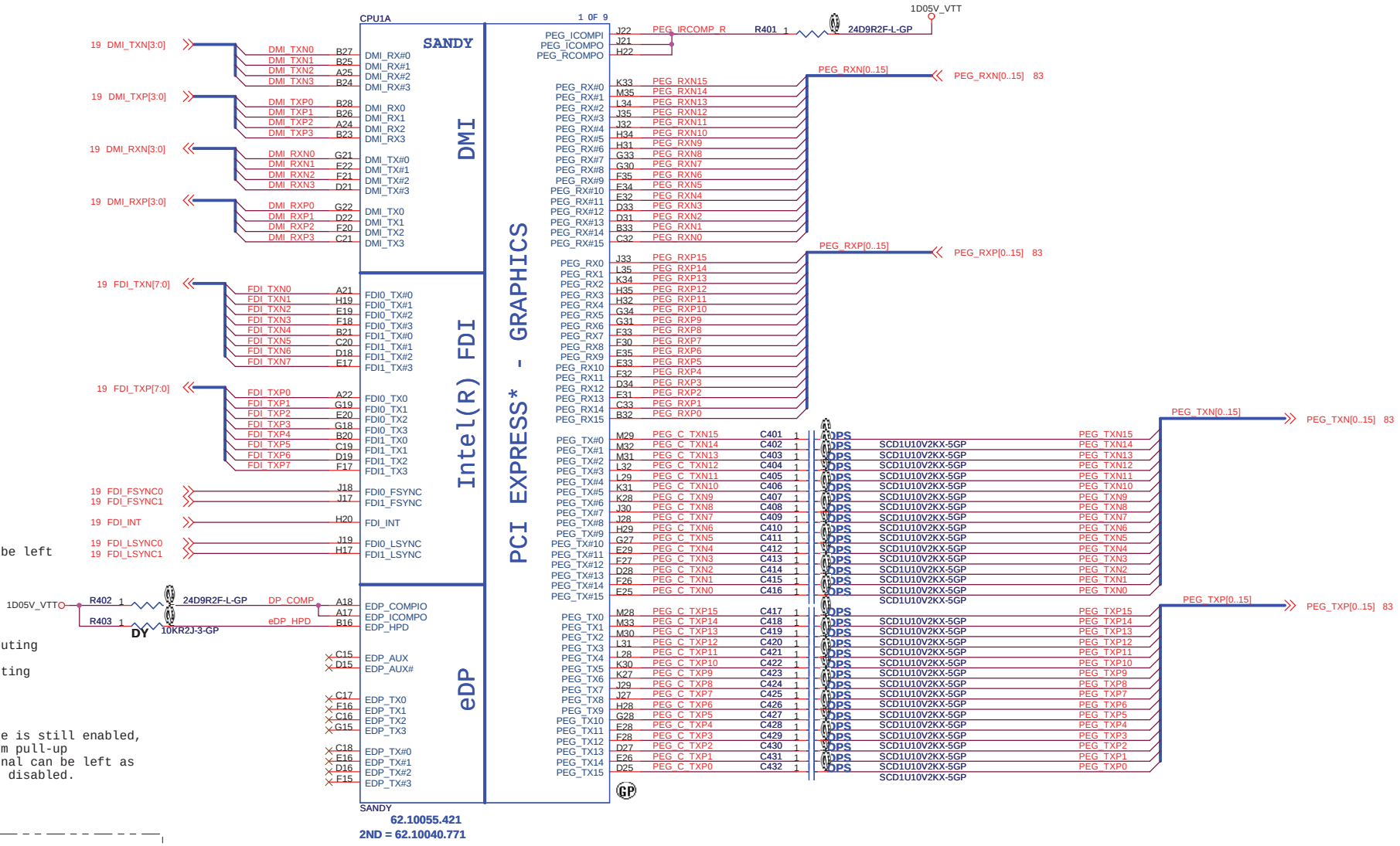
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-k ohm pull-up resistor on the motherboard. This signal can be left as no connect if entire eDP interface is disabled.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
A3	LA470	SB

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SSID = CPU

CPU1B — SANDY — 2 OF 9

MISC: SNB_IVB#, SKTOCC#
THERMAL: CATERR#, PECI, PROCHOT#, THERMTRIP#
PWR MANAGEMENT: PM_SYNC, UNCOREPWRGOOD, SM_DRAMPWROK, RESET#
CLOCKS: BCLK, BCLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#
DDR3 MISC: SM_DRAMRST#, SM_RCOMP0, SM_RCOMP1, SM_RCOMP2
JTAG & BPM: PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO, DBR#, BPM#0–BPM#7

SANDY
62.10055.421
2ND = 62.10040.771

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

SB_0820
SB_0830
SB_0805

<Core Design>

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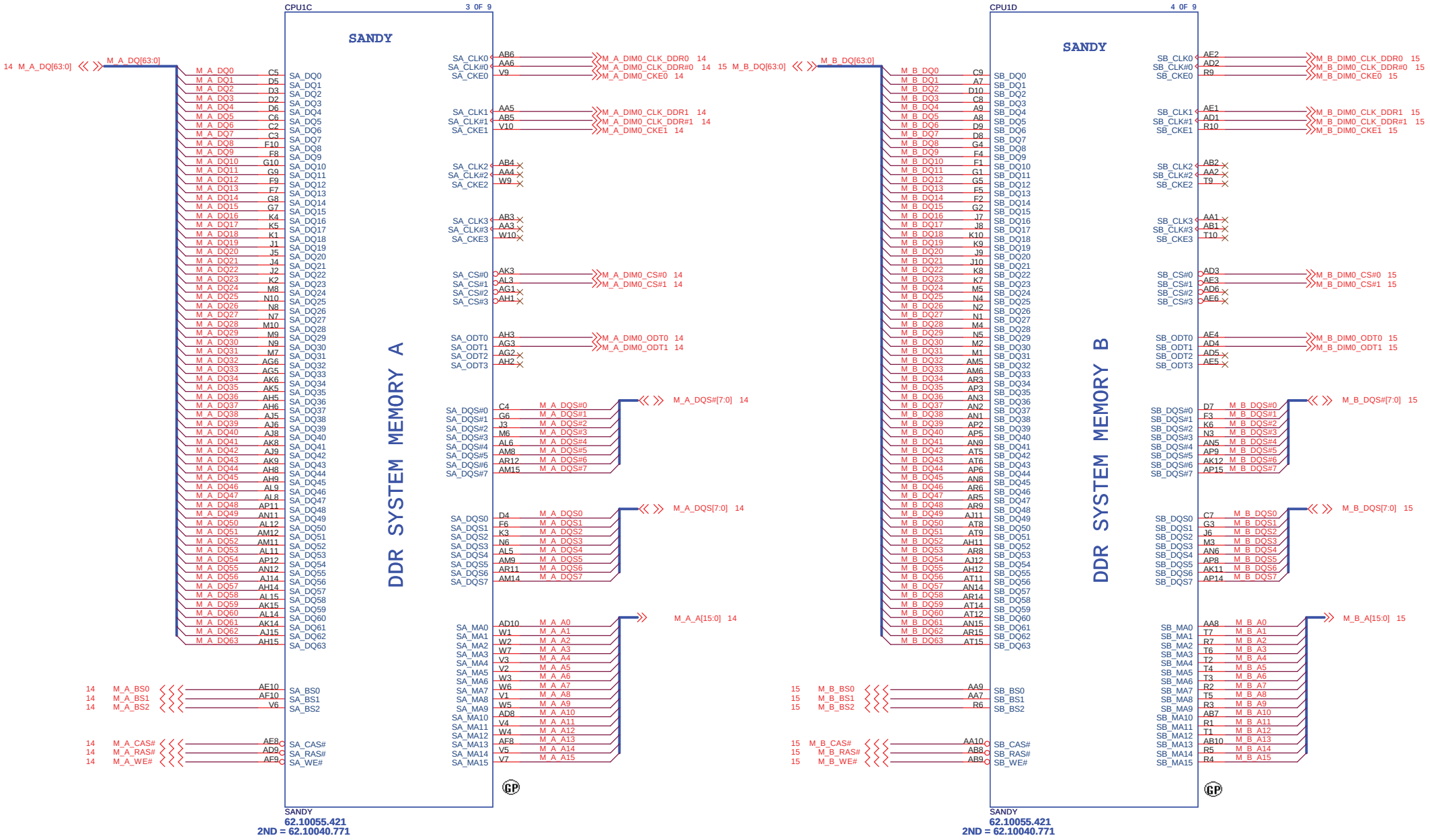
Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 5 of 103

SSID = CPU



<Core Design>

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Title: CPU (DDR)

Size: A3 | Document Number: LA470 | Rev: SB

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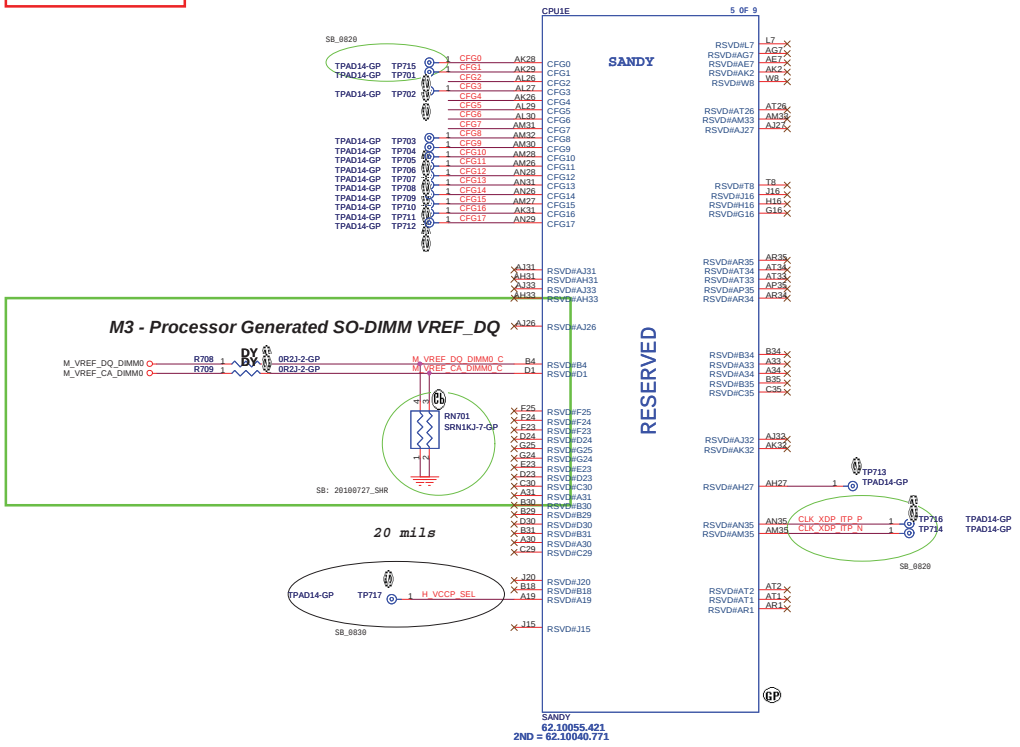
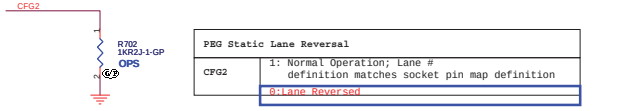
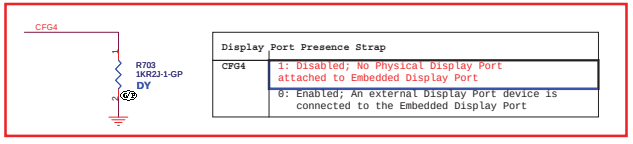
SSID = CPU

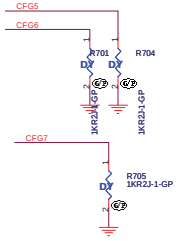




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

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SSID = CPU

POWER

CPU1F

6 OF 9

SANDY

PROCESSOR CORE POWER

53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP
C811 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP
C817 SC10U6D3V5KX-1GP
C818 SC10U6D3V5KX-1GP
C819 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26
AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26
AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26
AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26
AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26
Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26
V35 V34 V33 V32 V31 V30 V29 V28 V27 V26
U35 U34 U33 U32 U31 U30 U29 U28 U27 U26
R35 R34 R33 R32 R31 R30 R29 R28 R27 R26
P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
(all VCC)

PEG AND DDR

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 E12

1D05V_VTT

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 SC10U6D3V5KX-1GP

VCCIO: E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

1D05V_VTT

C812 C813 C814 C829 C830 C842 C843 C844 C845 SC10U6D3V5KX-1GP

VCCIO: J23

CORE SUPPLY

SVID

R804 need to close to CPU

1D05V_VTT

SB_0819

H_CPU_SVIDDAT_R R804 1 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 1 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK_R R805 1 0R2J-2-GP H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT_R R806 1 0R2J-2-GP H_CPU_SVIDDAT 42

SB_0819

SENSE LINES

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE B10 VCCIO_SENSE 45
VSSIO_SENSE A10 VSSIO_SENSE 45

SANDY
62.10055.421
2ND = 62.10040.771

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Title: CPU (VCC_CORE)

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SSID = CPU

POWER

CPU1G

7 0F 9

SANDY

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 SC10U6D3V5KX-1GP
C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 SC10U6D3V5KX-1GP
RC901 SC33P50V2JN-3GP DY

C907 SC10U6D3V5KX-1GP
C908 SC10U6D3V5KX-1GP
C918 SC10U6D3V5KX-1GP
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP
RC902 SC33P50V2JN-3GP DY

SB_0831

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 → VAXG

VAXG_SENSE → AK35
VSSAXG_SENSE → AK34

VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

SM_VREF → AL1

+V_SM_VREF_CNT

+V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ → AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 SC10U6D3V5KX-1GP
C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 SC10U6D3V5KX-1GP

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA → M27 M26 L26 J26 J25 J24 H26 H25

C916 SC10U6D3V5KX-1GP
C915 SC10U6D3V5KX-1GP
C917 SC10U6D3V5KX-1GP
TC903 ST330U2VDM-4-GP DY

0D85V_S0

R902 10R2J-2-GP
R902 need be close to pin H23.

VCCSA_SENSE → H23

VCCSA_SENSE 48

FC_C22 → C22
VCCSA_VID1 → C24

H_FC_C22
VCCSA_SEL

H_FC_C22 48
VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL → B6 A6 A2

C925 SC10U6D3V5KX-1GP
C923 SC10U6D3V5KX-1GP
C922 SC1U10V2KX-1GP
C924 SC1U10V2KX-1GP

SANDY
62.10055.421
2ND = 62.10040.771

Close to CPU

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

<Core Design>

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Title: CPU (VCC_GFXCORE)

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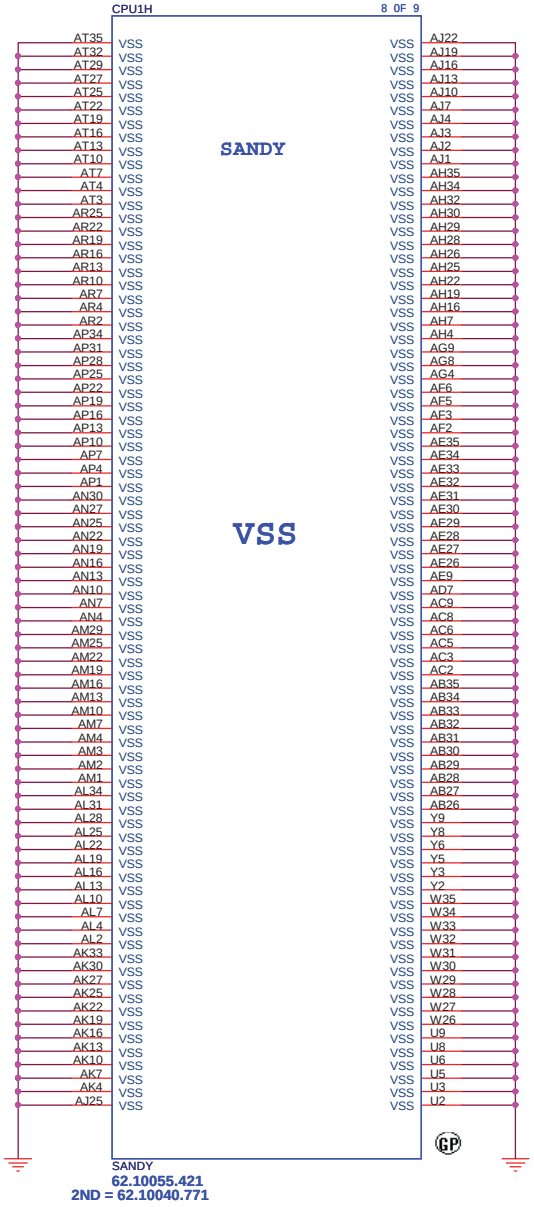
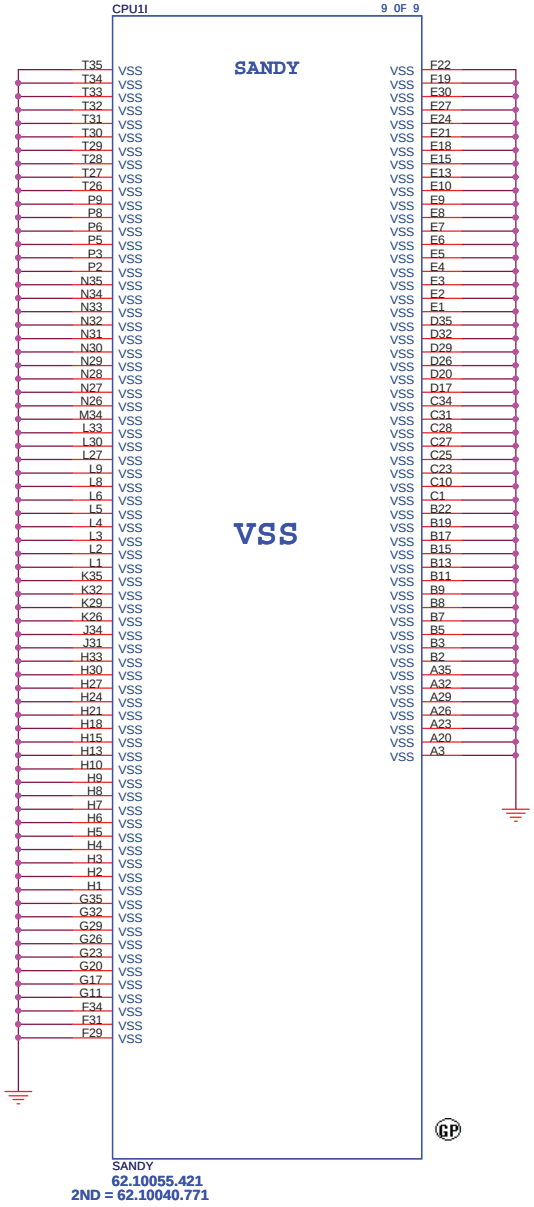
SSID = CPU





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 10 of 103

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

XDP

Size	Document Number	Rev
A3	**LA470**	**SB**

Date: Tuesday, September 07, 2010 Sheet 11 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 12 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 13 of 103

SSID = MEMORY

DM1

DDR3-204P-109-GP
62.10017.X51
2nd = 62.10017.R91
3rd = 62.10017.V61

SB_8819

Place these caps close to VTT1 and VTT2.

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: Custom | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 14 of 103

SSID = MEMORY

DM2

M_B_A[15:0] 6

M_B_BS2 6

M_B_BS0 6
M_B_BS1 6
M_B_DQ[63:0] 6

M_B_DQS#[7:0] 6
M_B_DQS[7:0] 6

M_B_DIM0_ODT0 6
M_B_DIM0_ODT1 6

M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

14,37 DDR3_DRAMRST#

0D75V_S0

M_VREF_CA_DIMM0

C1523 SCD1U10V2KX-5GP
DY C1524 SC2D2U10V3KX-1GP
C1522 SCD1U10V2KX-5GP

Place these caps close to VTT1 and VTT2.

0D75V_S0
DY C1518 SC1U6D3V2KX-GP
C1519 SC1U6D3V2KX-GP
DY C1520 SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6

M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6

M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6

M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6

M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65,66
PCH_SMBCLK 14,20,65,66

TS#_DIMM0_1 14

SA0_DIM1
SA1_DIM1

3D3V_S0
DY C1501 SCD1U10V2KX-5GP
C1502 SC2D2U10V3KX-1GP

1D5V_S3

3D3V_S0
R1501 10KR2J-3-GP
SA1_DIM1
SA0_DIM1
R1502 10KR2J-3-GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SODIMM B DECOUPLING

1D5V_S3
DY C1503 SC10U10V5ZY-1GP
DY C1504 SC10U10V5ZY-1GP
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
DY C1508 SC10U10V5ZY-1GP
C1509 SC10U6D3V5KX-1GP
DY C1510 SC10U6D3V5KX-1GP

C1511 SCD1U10V2KX-5GP
C1512 SCD1U10V2KX-5GP
C1513
C1514 SCD1U10V2KX-5GP

H = 8mm

DDR3-204P-108-GP
62.10017.X41
2nd = 62.10017.M51
3rd = 62.10017.V51

SB_0819

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 15 of 103

(Blanking)

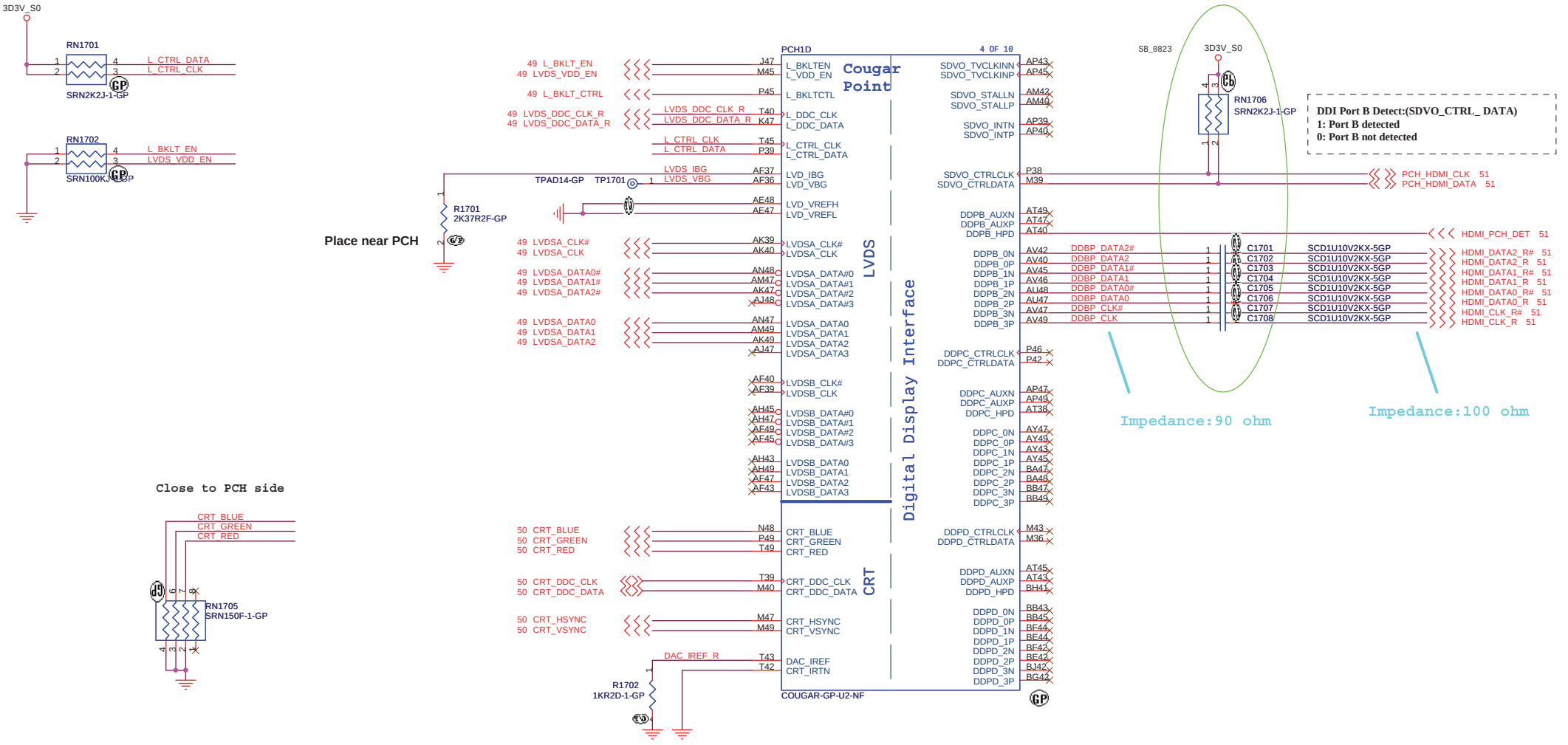
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 16 of 103



<Core Design>

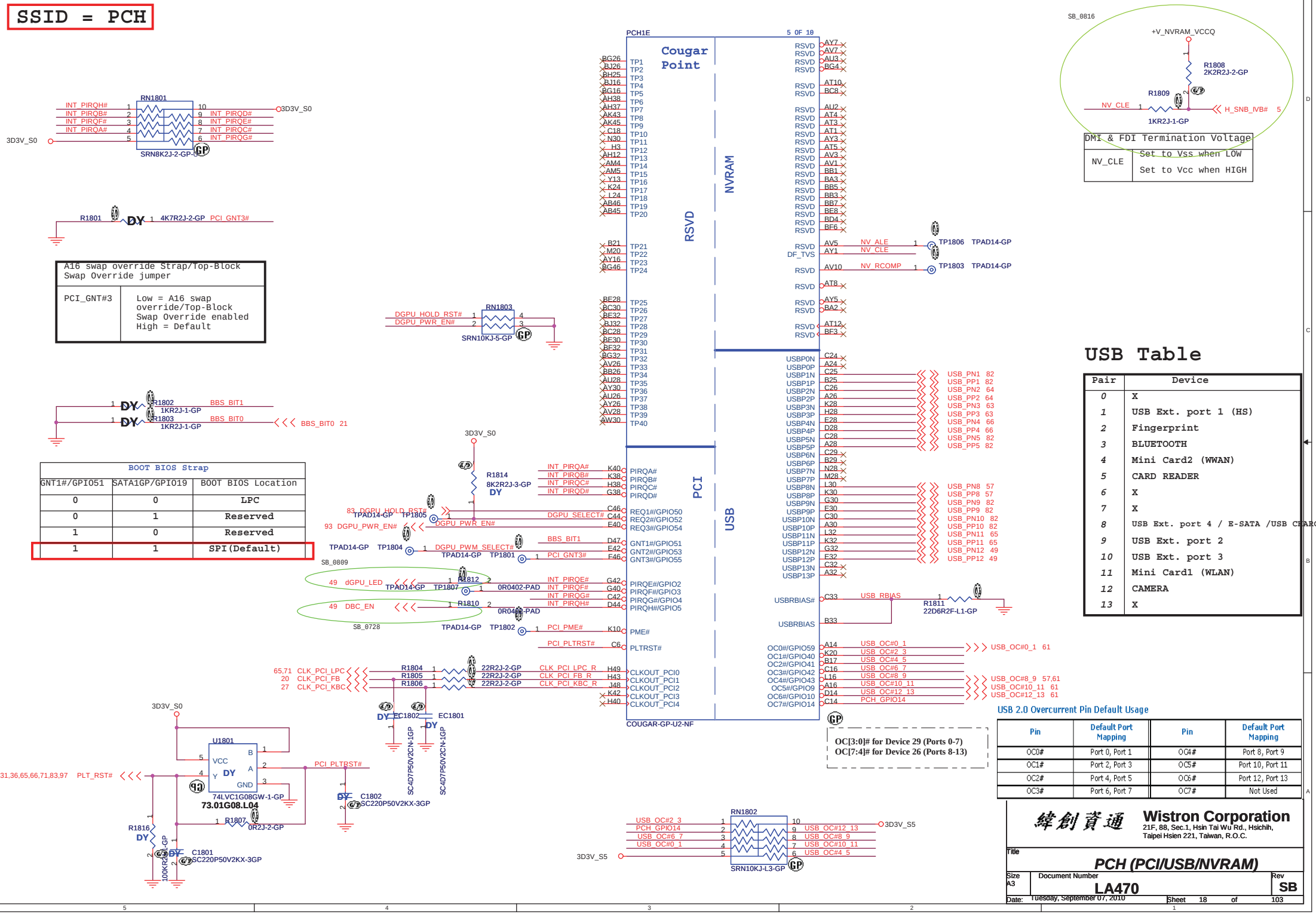
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 17 of 103

SSID = PCH



USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

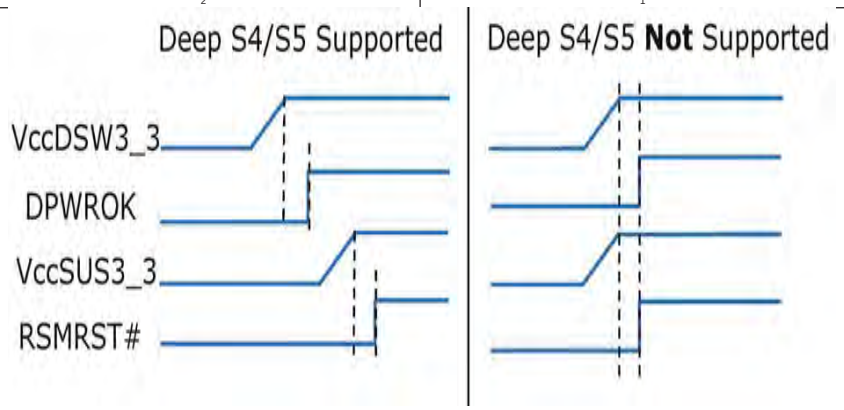
Title: **PCH (PCI/USB/NVRAM)**

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

This signal has an internal pull-up resistor

2nd = 84.DM601.03F

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: LA470 | Rev: SB
Date: Tuesday, September 07, 2010 | Sheet 19 of 103

SSID = PCH

PCH1B

Cougar Point

W-WAN

WLAN

LAN

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

WLAN CLK

LAN CLK

PCIECLKRQ1# and PCIECLKRQ2# support S0 power only

PL 10K FOR Integrated CLOCK GEN mode.

need very close to PCH

CRB: 1K
CHKLT: 10K

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

R2008 and C2008 CO-LAY

2nd = 84.DM601.03F
84.2N702.A3F
2N7002KDW-GP

2nd = 82.30020.791
3rd = 82.30020.A31

<Core Design>

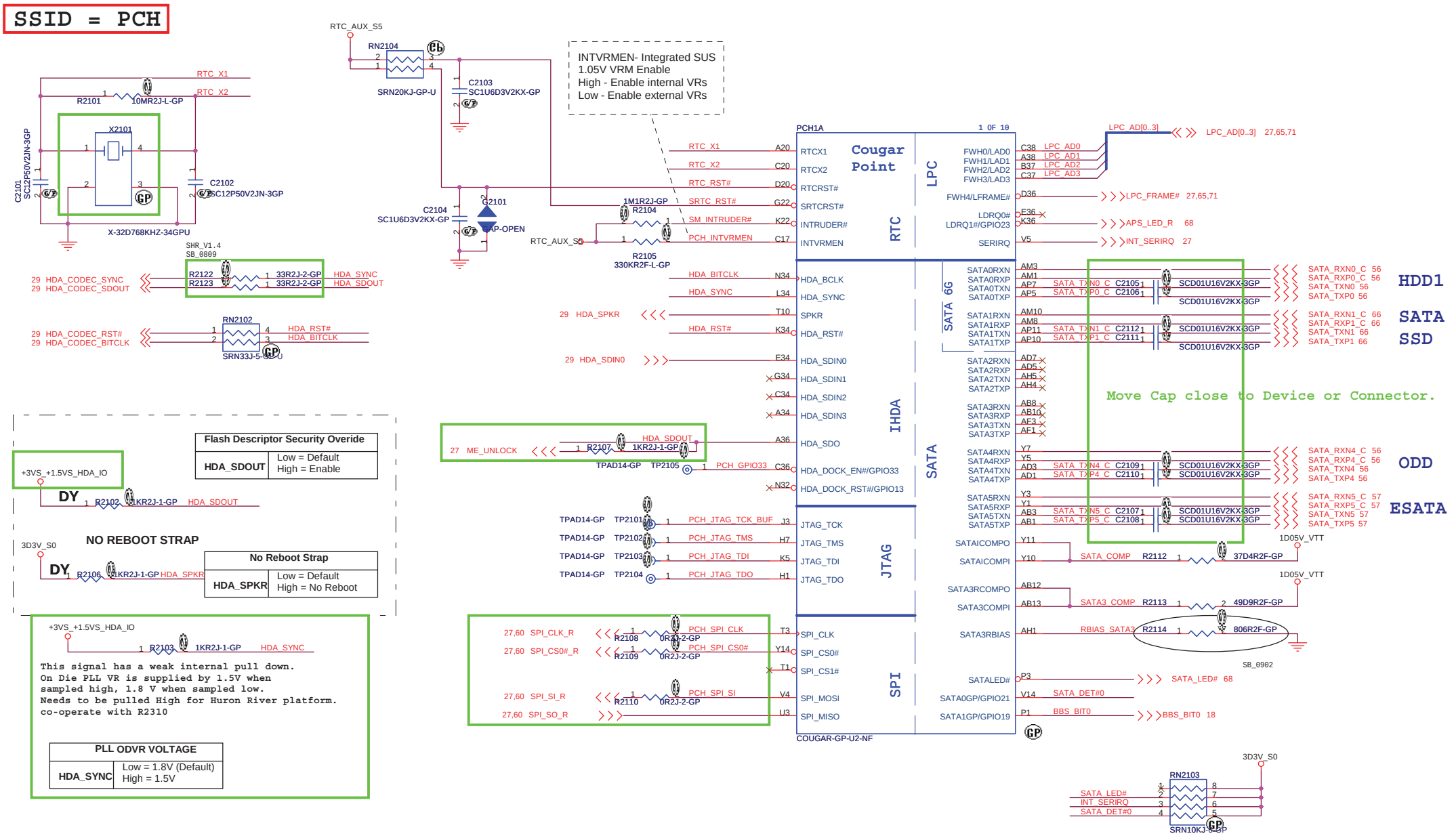
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 20 of 103

SSID = PCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 21 of 103

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

3D3V_S0 — R2202 1 — 200KR2F-L-GP — SATA_ODD_PRSNT#

20100625 V1.2

3D3V_S0 — RN2203 — H_A20GATE, H_RCIN# — SRN10KJ-5-GP

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

3D3V_S0 — R2224 10KR2J-3-GP — PCH_TEMP_ALERT#
PCH_GPIO27 — DY R2223 10KR2J-3-GP
DY R2225 10KR2J-3-GP

3D3V_S0 — RN2201 — PSW_CLR#, DGPU_HPD_INTR#, EC_SMI# — SRN10KJ-8-GP

RN2202 — MFG_MODE, S_GPIO, EC_SCI#, PCH_GPIO22 — SRN10KJ-8-GP
PCH_GPIO48 — R2227 10KR2J-3-GP

3D3V_S5 — RN2205 — PCH_GPIO12, USB3_PWR_ON — SRN10KJ-8-GP

PCH_GPIO15 — R2201 1KR2J-1-GP
PCH_GPIO24 — R2221 10KR2J-3-GP
20100625 V1.2
PLL_ODVR_EN — R2226 10KR2J-3-GP

NC_FP_DET# — R2220 10KR2J-3-GP
20100705

PCH1F — 6 OF 10 — Cougar Point

S_GPIO — R2218 100R2J-2-GP	GPIO0	T7	BMBUSY#/GPIO0
EC_SMI#	GPIO60	A42	TACH1/GPIO1
DGPU_HPD_INTR#	GPIO61	H36	TACH2/GPIO6
27 EC_SCI#	EC_SCI#	E38	TACH3/GPIO7
	ICC_EN#	C10	GPIO8
	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL/GPIO12
	PCH_GPIO15	G2	GPIO15
56 SATA_ODD_PRSNT# — R2213 0R2J-2-GP	PCH_GPIO16	U2	SATA4GP/GPIO16
92,93 DGPU_PWROK — R2228 0R2J-2-GP	DGPU_PWROK	D40	TACH0/GPIO17
49 Color_Engine# — R2229 0R2J-2-GP	PCH_GPIO22	T5	SCLOCK/GPIO22
TPAD14-GP TP2202	PCH_GPIO24	E8	GPIO24/MEM_LED
	PCH_GPIO27	E16	GPIO27
	PLL_ODVR_EN	P8	GPIO28
	PSW_CLR#	K1	STP_PCI#/GPIO34
TPAD14-GP TP2204 — GAP-OPEN G2201	NC_FP_DET#	K4	GPIO35
	DMI_OVRVLTG	V8	SATA2GP/GPIO36
	FDI_OVRVLTG	M5	SATA3GP/GPIO37
	MFG_MODE	N2	SLOAD/GPIO38
	GFX_CRB_DET	M3	SDATAOUT0/GPIO39
TP2209	PCH_GPIO48	V13	SDATAOUT1/GPIO48
	PCH_TEMP_ALERT#	V3	SATA5GP/GPIO49
TPAD14-GP TP2205	USB3_PWR_ON	D6	GPIO57
TPAD14-GP TP2206		A4	NCTF_VSS#A4
TPAD14-GP		A44	NCTF_VSS#A44
		A45	NCTF_VSS#A45
		A46	NCTF_VSS#A46
		A5	NCTF_VSS#A5
		A6	NCTF_VSS#A6
		B3	NCTF_VSS#B3
		B47	NCTF_VSS#B47
		BD1	NCTF_VSS#BD1
		BD49	NCTF_VSS#BD49
TPAD14-GP TP2210		BE1	NCTF_VSS#BE1
TPAD14-GP TP2211		BE49	NCTF_VSS#BE49
TPAD14-GP TP2212		BF1	NCTF_VSS#BF1
		BF49	NCTF_VSS#BF49

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

COUGAR-GP-U2-NF

SB_0811
SHR_V1.5

	TACH4/GPIO68	C40	SATA_ODD_PWRGT 56
	TACH5/GPIO69	B41	UMA_DIS# 20
	TACH6/GPIO70	C41	VRAM_SIZE1
	TACH7/GPIO71	A40	VRAM_SIZE2
	A20GATE	P4	H_A20GATE 27
H_PECI 5,27 — DY R2203 0R2J-2-GP	PECI	AU16	H_PECI_R
	RCIN#	P5	H_RCIN# 27
	PROCPWRGD	AY11	H_CPUPWRGD 5,11,36,97
H_THERMTRIP# 5,36 — R2204 1 390R2J-1-GP	THRMTRIP#	AY10	PCH_THERMTRIP_R
TP2201 TPAD14-GP	INIT3_3V#	T14	INIT3_3V#
	TS_VSS1	AH8	
	TS_VSS2	AK11	
	TS_VSS3	AH10	
	TS_VSS4	AK10	TS_VSS 1 R2219 2 0R0402-PAD
	NC_1	P37	
	NCTF_VSS#BG2	BG2	
	NCTF_VSS#BG48	BG48	
	NCTF_VSS#BH3	BH3	
	NCTF_VSS#BH47	BH47	TP2207 TPAD14-GP
	NCTF_VSS#BJ4	BJ4	
	NCTF_VSS#BJ44	BJ44	
	NCTF_VSS#BJ45	BJ45	TP2208 TPAD14-GP
	NCTF_VSS#BJ46	BJ46	
	NCTF_VSS#BJ5	BJ5	
	NCTF_VSS#BJ6	BJ6	
	NCTF_VSS#C2	C2	
	NCTF_VSS#C48	C48	
	NCTF_VSS#D1	D1	
	NCTF_VSS#D49	D49	
	NCTF_VSS#E1	E1	
	NCTF_VSS#E49	E49	
	NCTF_VSS#F1	F1	
	NCTF_VSS#F49	F49	

3D3V_S0 — R2207 10KR2J-3-GP — DY — FDI_OVRVLTG
R2208 10KR2J-3-GP

3D3V_S0 — R2209 10KR2J-3-GP — DY — DMI_OVRVLTG
R2210 10KR2J-3-GP

ICC_EN# — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2205 10KR2J-3-GP — DY — GFX_CRB_DET
R2206 100KR2J-1-GP

PCH_THERMTRIP_R — R2222 1 — 1D05V_VTT
DY 56R2J-4-GP

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

3D3V_S0 — R2214 2G 10KR2J-3-GP — R2216 1G 10KR2J-3-GP
[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G
VRAM_SIZE1
VRAM_SIZE2
R2215 1G_512M 10KR2J-3-GP — R2217 2G_512M 10KR2J-3-GP

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 R2212 1KR2J-1-GP

<Core Design>

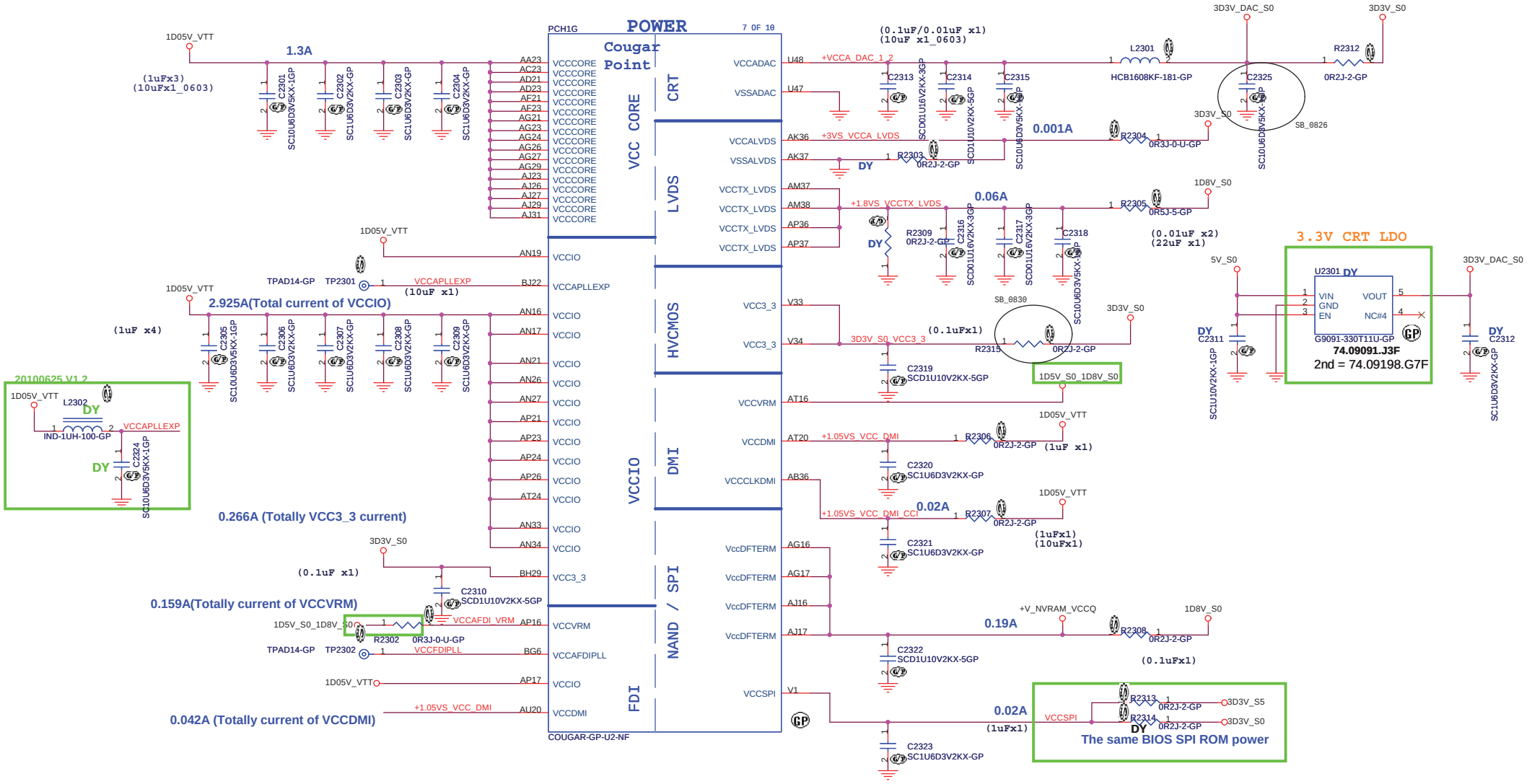
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 22 of 103

SSID = PCH 6A



VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 23 of 103

SSID = PCH

POWER

PCH1J

10 OF 10

Cougar Point

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.08A

0.16A (Totally current of VCCVRM)

0.055A

0.095A

0.01A

6uA

2nd = 68.10090.10B

2nd = 83.R2004.B8F

<Core Design>

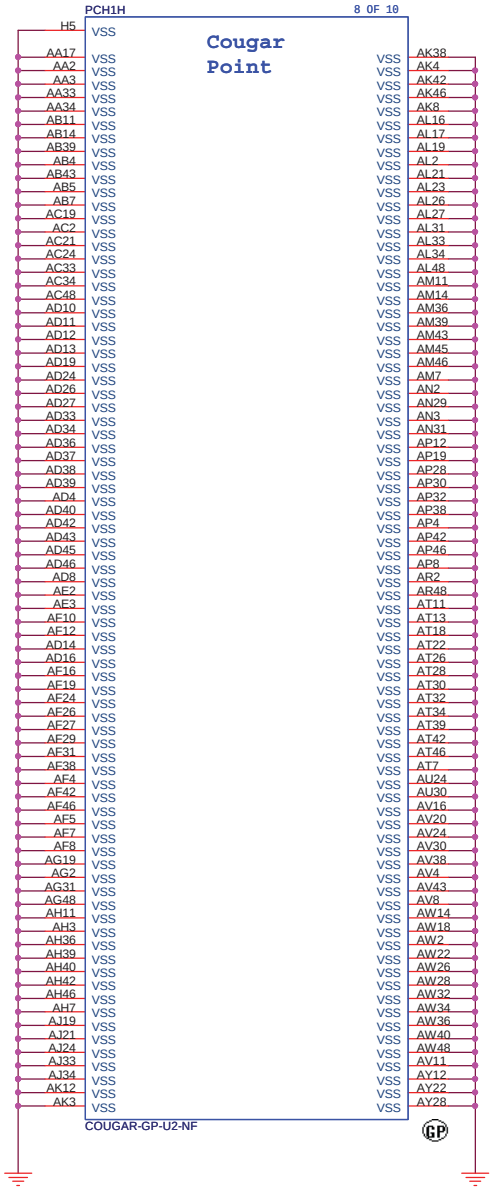
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

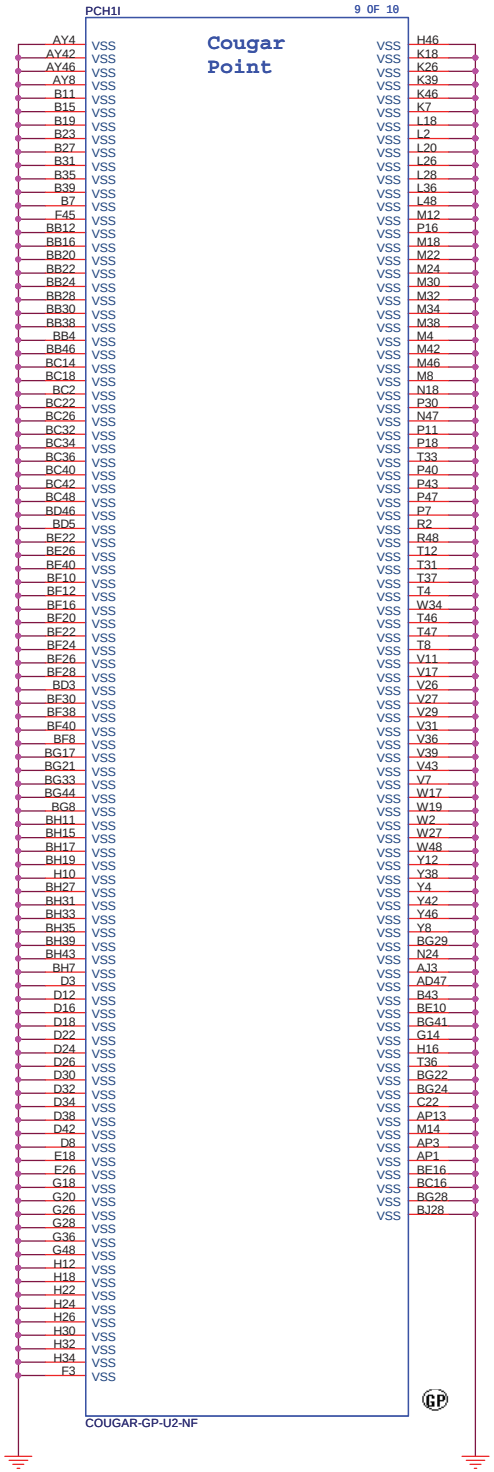
Title: PCH (POWER2)

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 24 of 103

SSID = PCH





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 25 of 103

(Blanking)

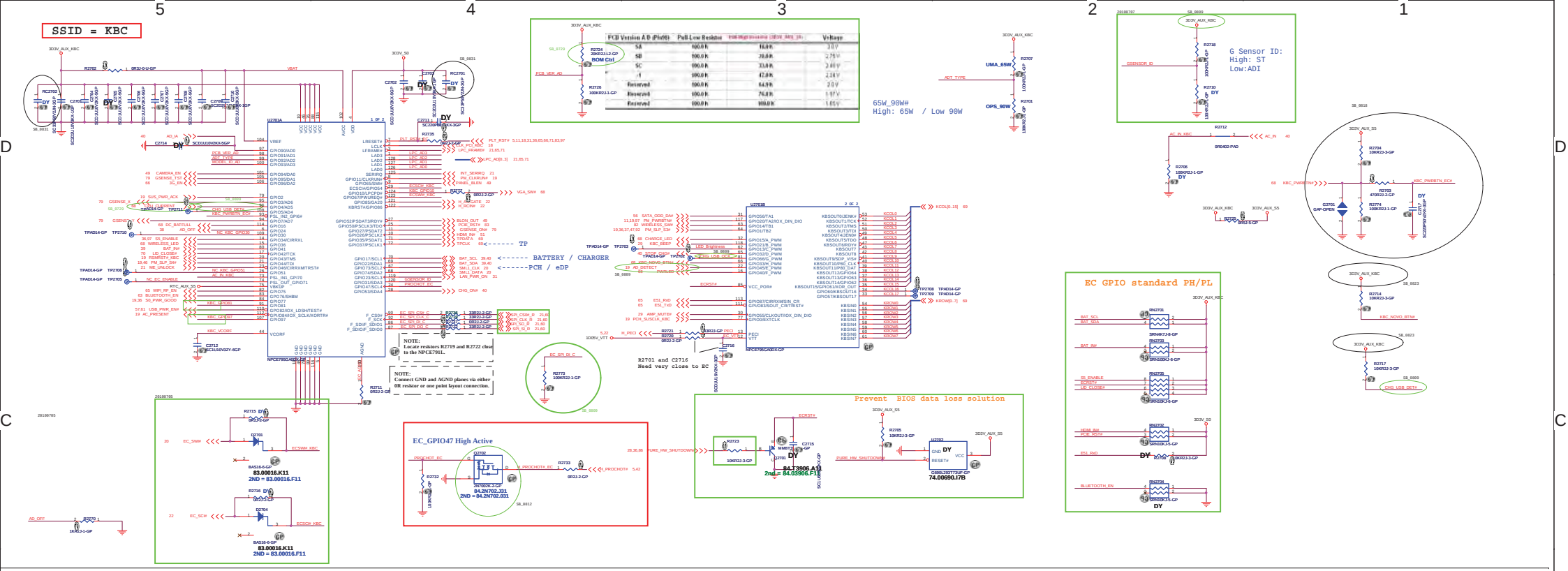
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

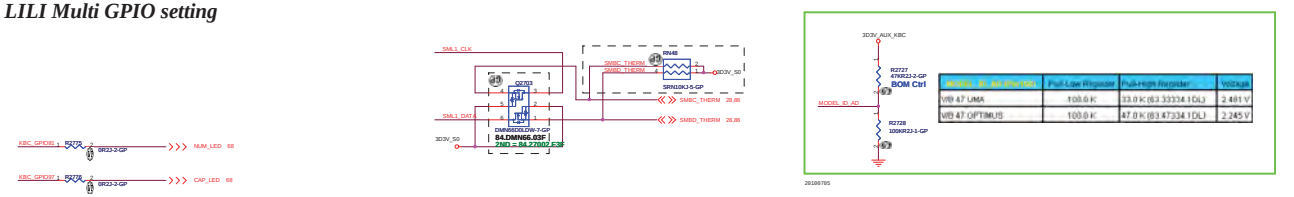
Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 26 of 103



LILI Multi GPIO setting



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

Size: A1 | Document Number: LA470 | Rev: SB

Date: Monday, September 07, 2009 | Sheet 27 of 50

SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA 0905 change to 390p

3

C183 SC390P50V2KX-GP

Q6 MMBT3904WT1G-GP

2200p close to smsc2103 chip

2

C434 SC390P50V2KX-GP

DY

Q42 MMBT3904WT1G-GP

REMOTE2-

REMOTE2+

C569 SC2200P50V2KX-2GP

between CPU, VGA and DIMM on bottom side

T8

1

Q9 MMBT3904WT1G-GP

2200p close to smsc2103 chip

H_THERMDA

C389 SC2200P50V2KX-2GP

H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit

Close to connector

5V_S0

SA 0905

D2801 CH551H-30PT-GP

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

DY

C39 C4D7U6D3V3KX-GP

R2801 0R3J-0-U-GP

R426 10KR2J-3-GP

SB_0819

FAN_TACH

FAN_PWM

5V_S0_FAN

FAN_PWM_C

R427 0R0402-PAD

EC2801 SCI.KP50V2KX-1GP

EC2802 SCI.KP50V2KX-1GP

DY

20100707_EMI

FAN1 ACES-CON4-4-GP

20.F0765.004

2nd = 20.F1808.004

3D3V_S0

R280 6K8R2J-GP

SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0

R260 68R2-GP

C388 SCD1U10V2KX-4GP

2103_VDD

U31

H_THERMDA

H_THERMDC

REMOTE2+

REMOTE2-

SC 1203

THERM_SCI#

THERM_SYS_SHDN#

THERM_SCI#_R

R272 0R0402-PAD

TP66 TPAD14-GP

27,86 SMBC_THERM

27,86 SMBD_THERM

VDD

DP1

DN1

DP2/DN3

ND2/DP3

SYS_SHDN#

ALERT#

SMCLK

SMDATA

GPIO1

GPIO2

TACH

PWM

TRIP_SET

SHDN_SEL

GND

GND

EMC2103-2-AP-GP

2103_4

2103_5

TP65 TPAD14-GP

TP67 TPAD14-GP

TRIP_SET_R276

2K05R2F-GP

T8 = 105

RN49

SRN10KJ-5-GP

3D3V_S0

D2802

CH551H-30PT-GP

FAN_TACH

FAN_PWM

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

83.R5003.C8F

pin6, ALERT# OD

pin7, SYS_SHDN# OD

AFTP2803

AFTP2802

AFTP2801

FAN_PWM_C

FAN_TACH

5V_S0_FAN

SB_0825

3D3V_AUX_S5

D2803 BAT54PT-GP

83.00054.T81

2ND = 83.BAT54.D81

3rd = 83.BAT54.S81

DY

27,36,86 PURE_HW_SHUTDOWN#

R2812 10KR2J-GP

DY

C2811 SCD1U10V2KX-GP

DY

Q2802 2N7002K-2-GP

84.2N702.J31

2ND = 84.2N702.031

SB_0812

THERM_SYS_SHDN#

3D3V_S0

R2809 100KR2J-1-GP

R2810 0R2J-2-GP

DY

R2811 0R2J-2-GP

IMVP_PWRGD 36,42

<Core Design>

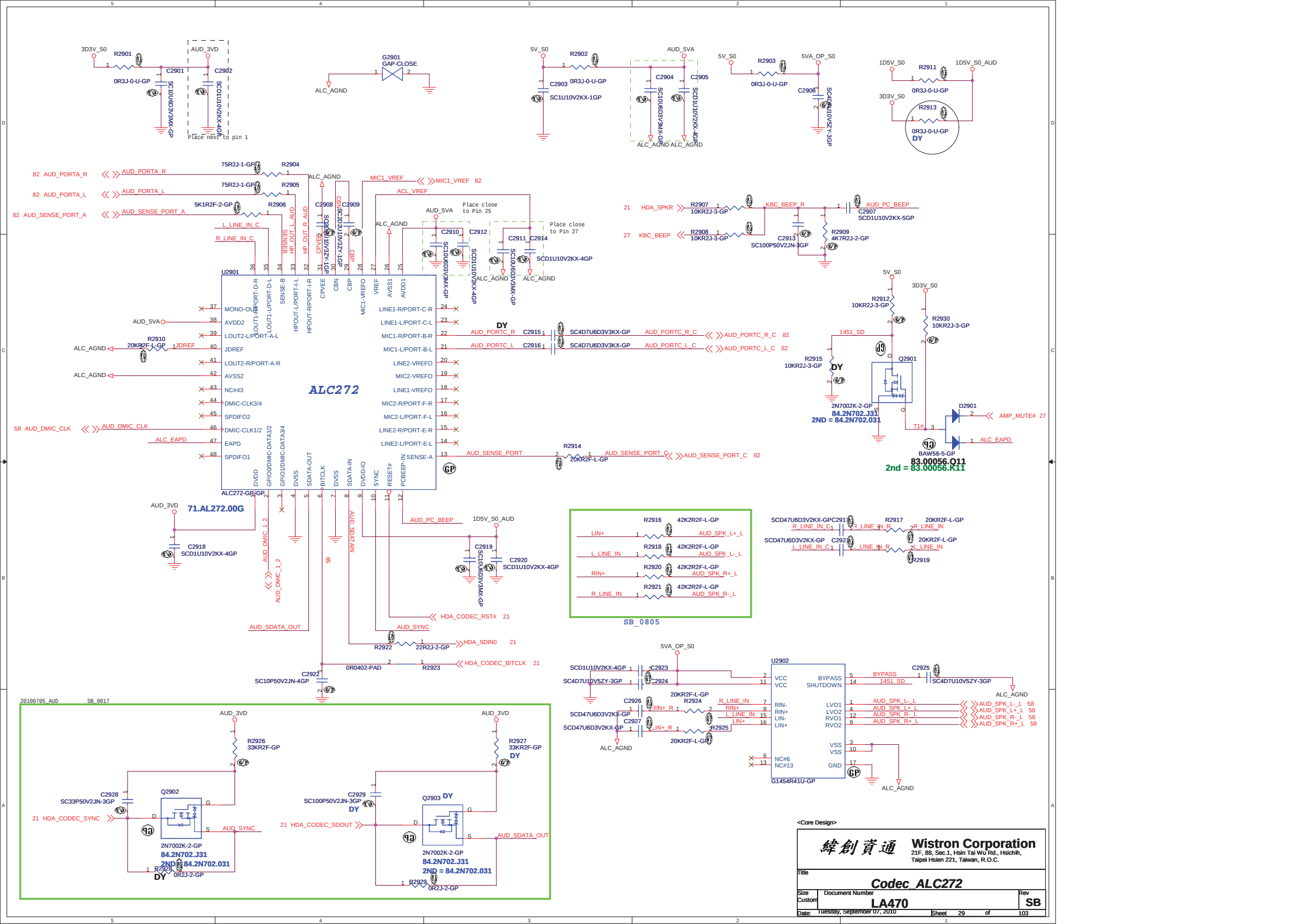
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 28 of 103


ALC272
ALC272-GR-GP
U2901
U2902
G1454R41U-GP
Q2901
Q2902
Q2903
D2901
BAW56-5-GP
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
71.AL272.00G
83.00056.Q11
2nd = 83.00056.K11
SB_0805
20100705_AUD
SB_0817
Place next to pin 1
Place close to Pin 25
Place close to Pin 27
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Codec_ALC272
LA470
Tuesday, September 07, 2010
29
103

<Core Design>

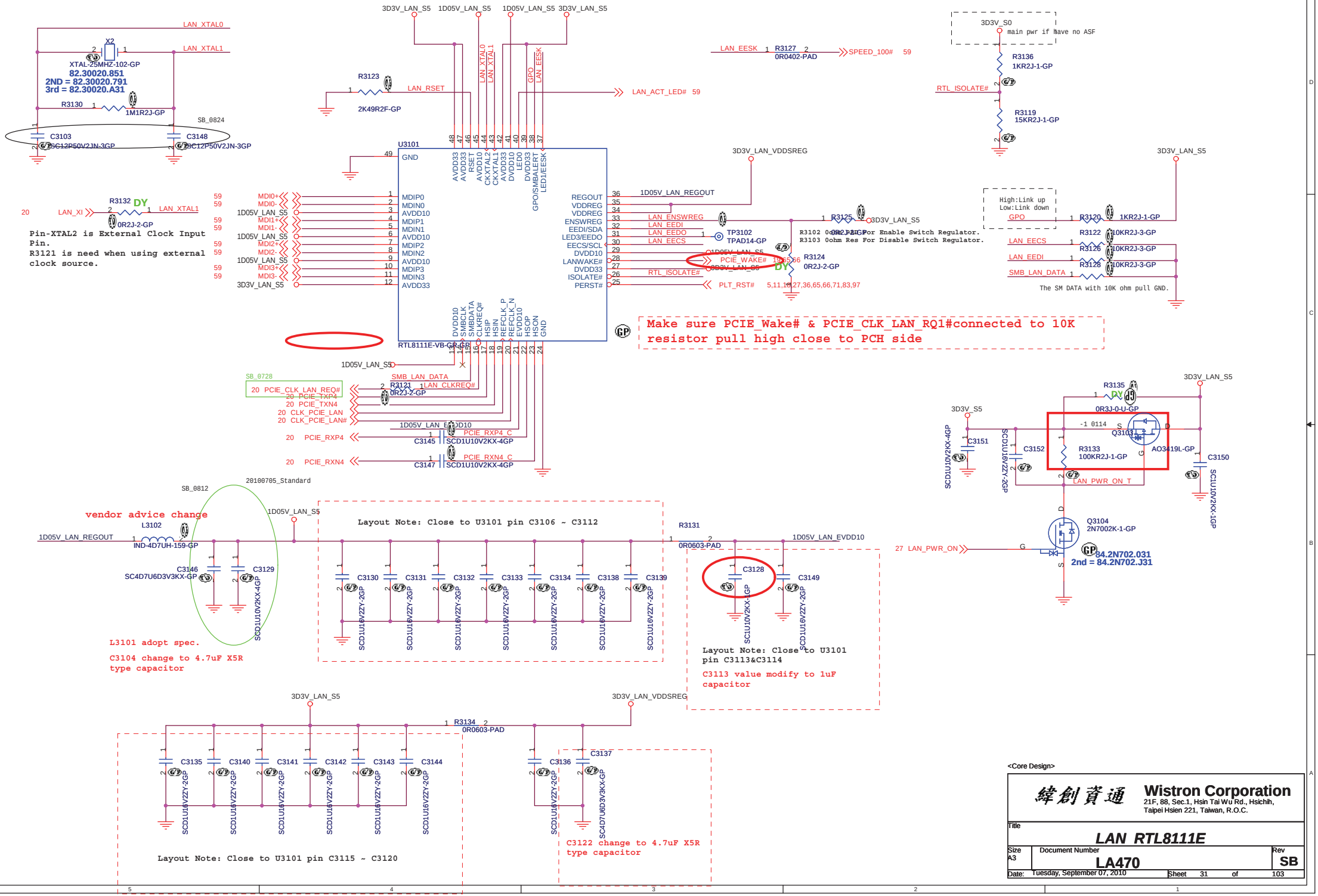
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Audio AMP

Size	Document Number	Rev
A4	**LA470**	**SB**

Date: Tuesday, September 07, 2010 Sheet 30 of 103

25MHz XTAL



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111E

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 31 of 103

<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A3	**LA470**	**SB**

Date: Tuesday, September 07, 2010 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 33 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 34 of 103

<Core Design>

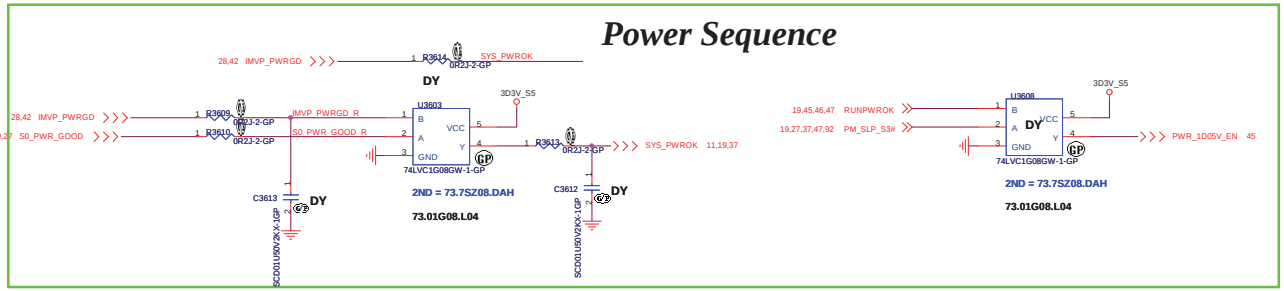
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

Size	Document Number	Rev
A3	LA470	SB

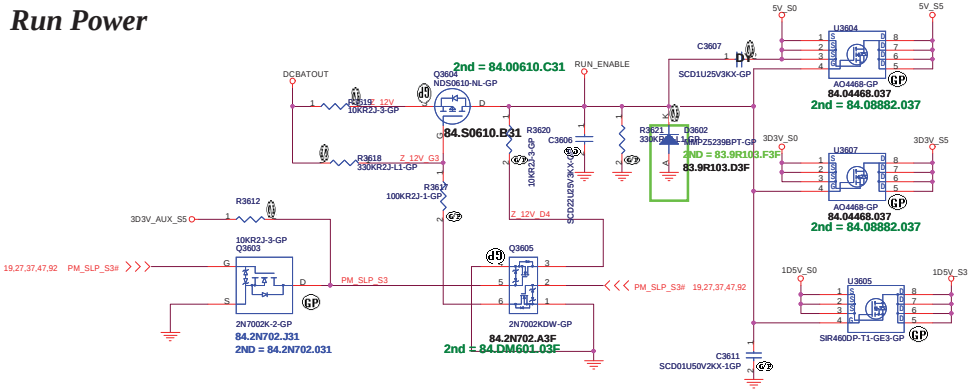
Date: Tuesday, September 07, 2010 Sheet 35 of 103

Power Sequence



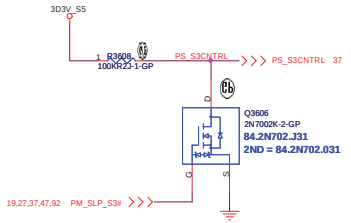
SSID = Reset.Suspend

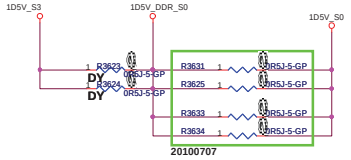
Run Power

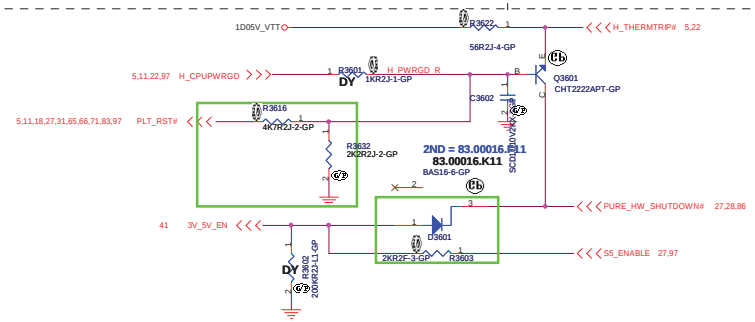


1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A







<Core Design>

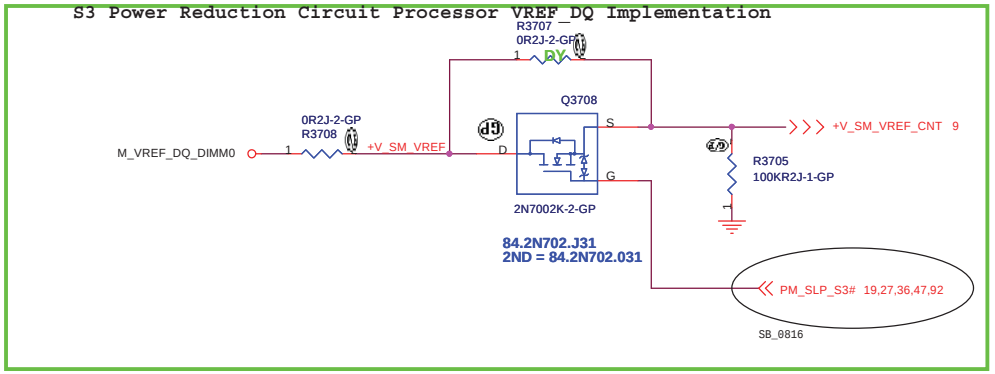
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

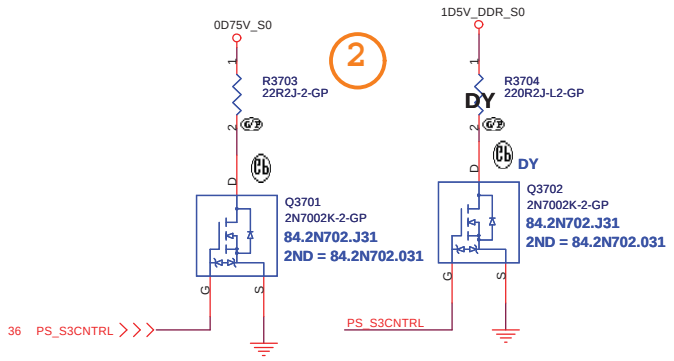
Size	Document Number	Rev
A2	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 36 of 103

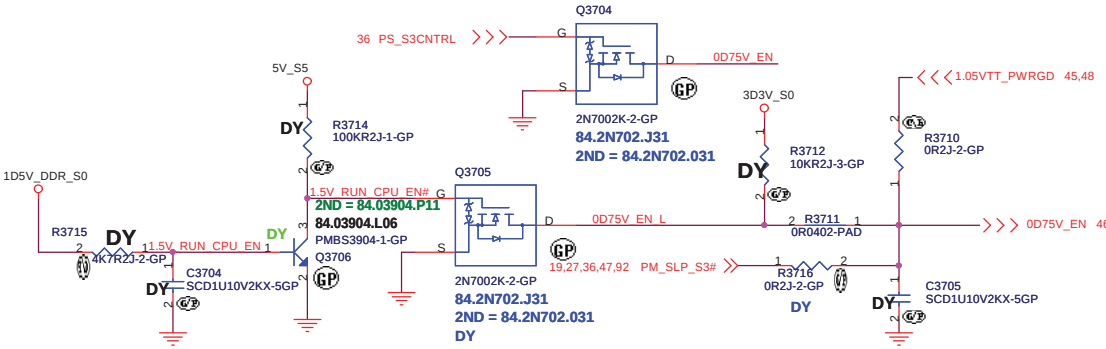
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



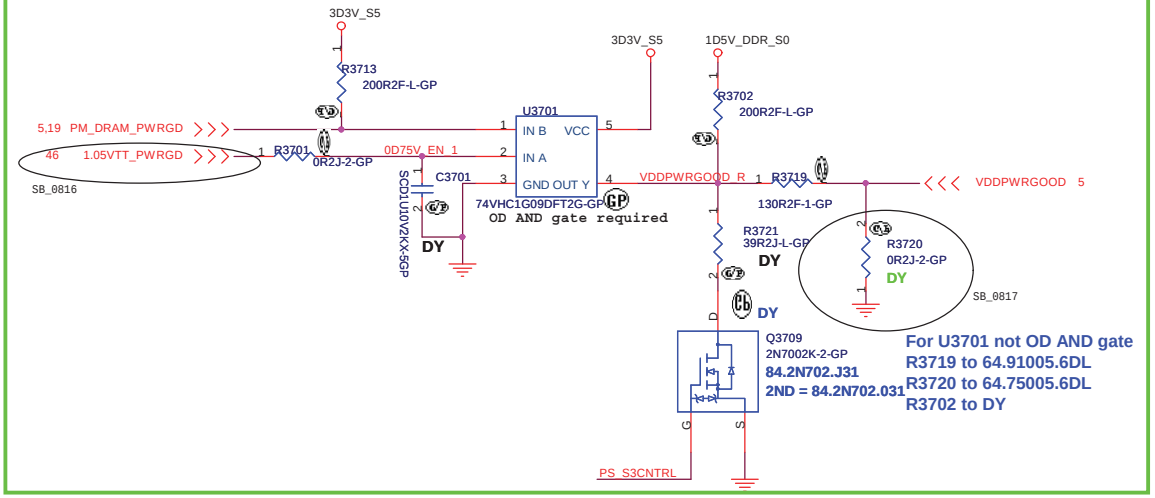
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



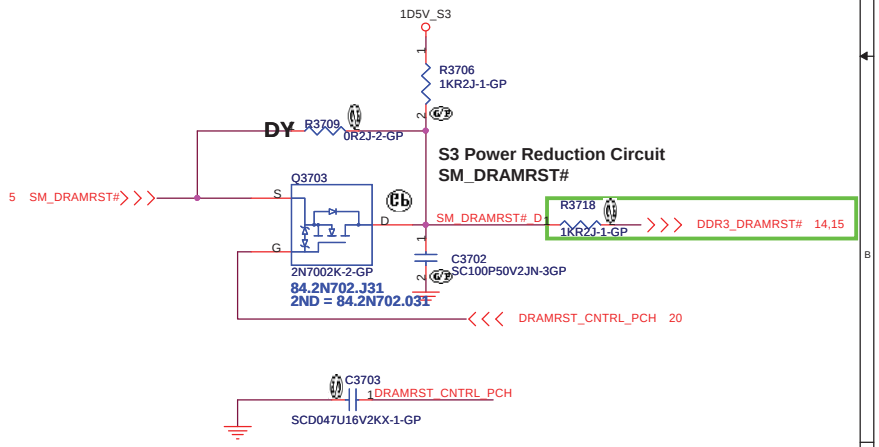
5 S3 Power Reduction X01 20091111



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



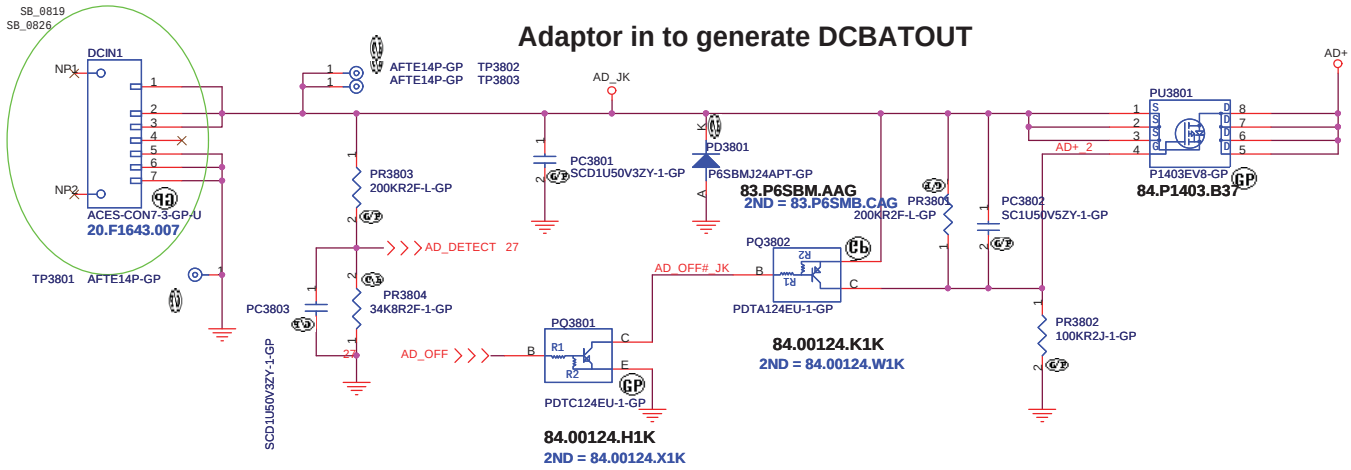
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADAPTER		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 37 of 103	

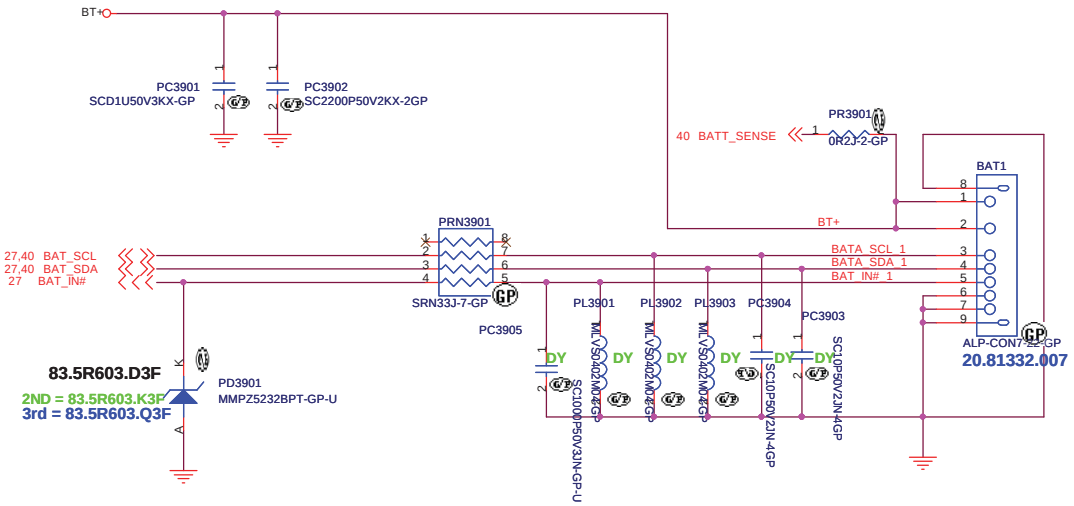
Adaptor in to generate DCBATOUT

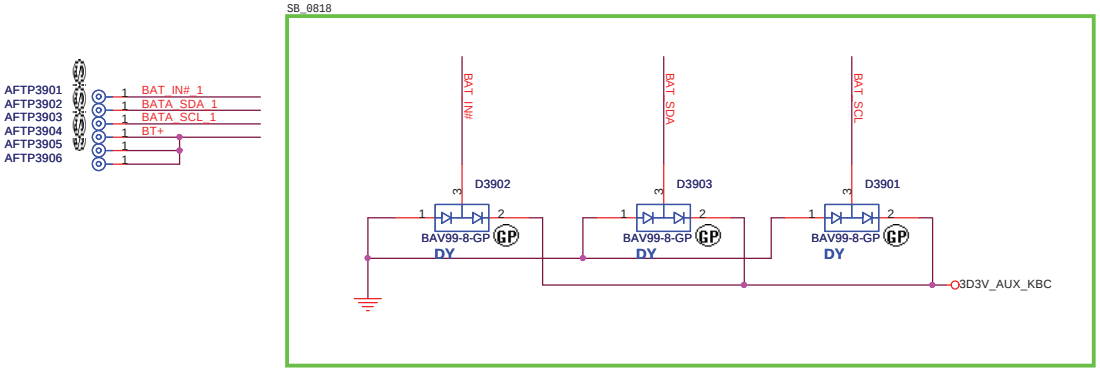


<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN_JACK*		
Size	Document Number: **LA470**	Rev: **SB**
Date: Tuesday, September 07, 2010	Sheet 38 of 103	

BATTERY CONNECTOR





DY ???

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT_CONN	
Size	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 39 of 103	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

20100518 WAYNE

STOP_CHG# connects to KBC

74.24745.073

79.10712.L02

83.R0203.08F
2nd = 83.1R003.I8F

20100518 WAYNE

AC_IN to KBC

<Core Design>

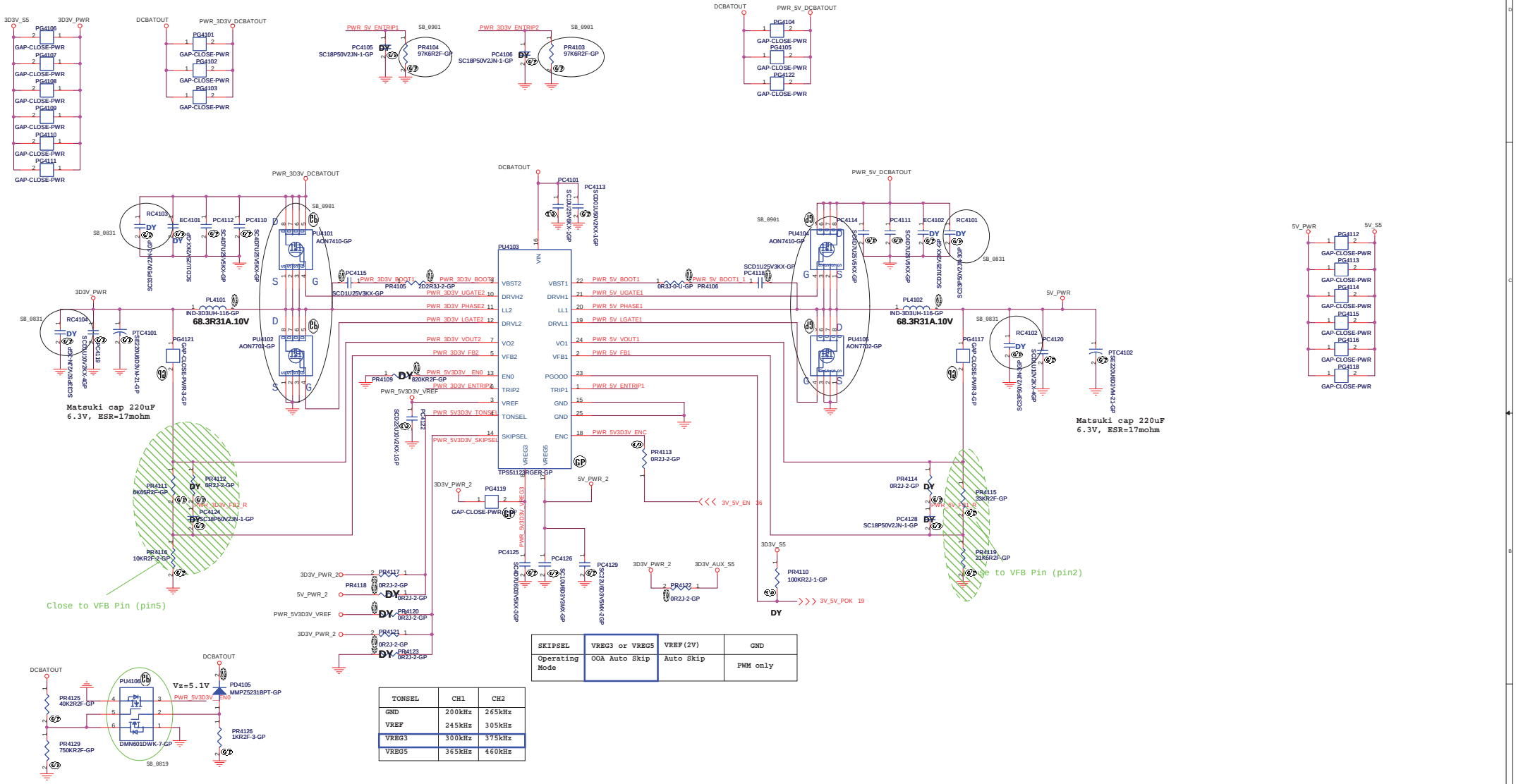
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24745

Size: | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

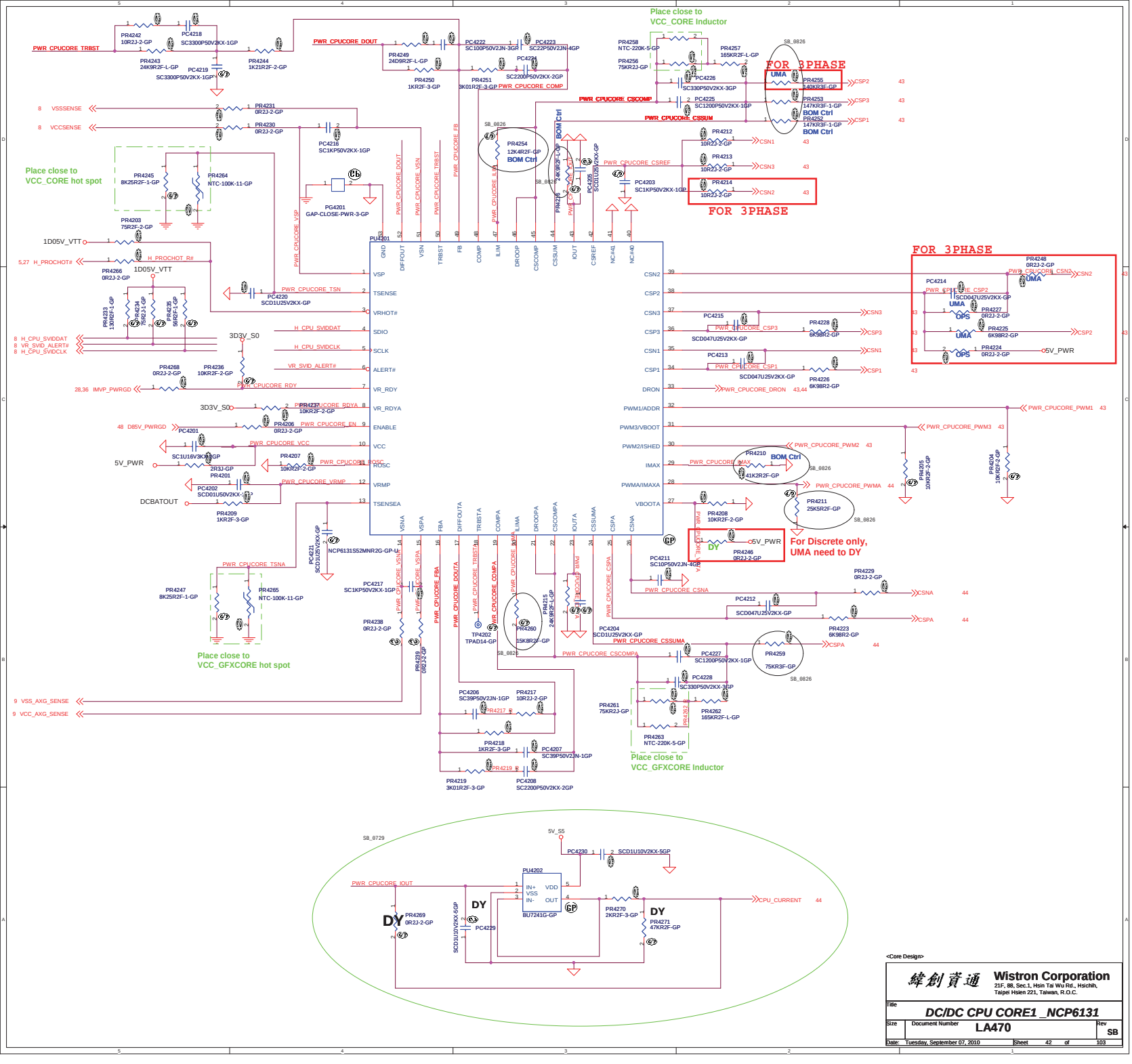
<Core Design>

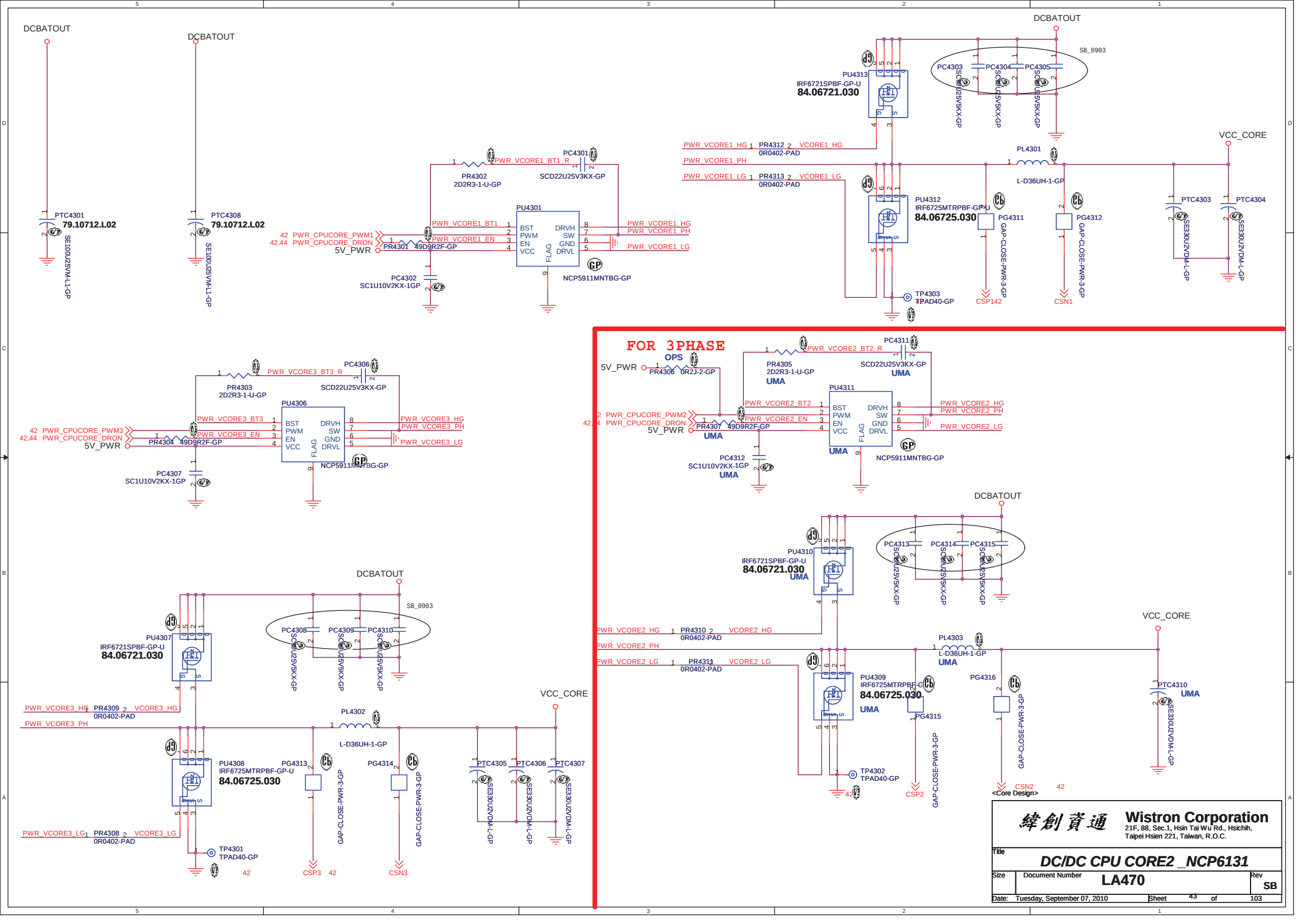
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC 3D3V5V

Size: | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 41 of 103


Place close to VCC_CORE Inductor
FOR 3PHASE
FOR 3PHASE
FOR 3PHASE
Place close to VCC_CORE hot spot
Place close to VCC_GFXCORE hot spot
Place close to VCC_GFXCORE Inductor
For Discrete only, UMA need to DY
PU4201
PU4202
PWR_CPUCORE_DOUT
PWR_CPUCORE_COMP
PWR_CPUCORE_CSCOMP
PWR_CPUCORE_CSSUM
PWR_CPUCORE_CSREF
PWR_CPUCORE_IMAX
PWR_CPUCORE_VSP
PWR_CPUCORE_VSN
PWR_CPUCORE_TRBST
PWR_CPUCORE_FB
PWR_CPUCORE_ILIM
PWR_CPUCORE_DROOP
PWR_CPUCORE_CSCOMP
PWR_CPUCORE_CSSUM
PWR_CPUCORE_IOUT
PWR_CPUCORE_CSREF
PWR_CPUCORE_TSN
PWR_CPUCORE_RDY
PWR_CPUCORE_RDYA
PWR_CPUCORE_EN
PWR_CPUCORE_VCC
PWR_CPUCORE_ROSC
PWR_CPUCORE_VRMP
PWR_CPUCORE_TSNA
PWR_CPUCORE_DIFFOUTA
PWR_CPUCORE_VSNA
PWR_CPUCORE_VSPA
PWR_CPUCORE_TRBSTA
PWR_CPUCORE_COMPA
PWR_CPUCORE_ILIMA
PWR_CPUCORE_IOUTA
PWR_CPUCORE_CSSUMA
PWR_CPUCORE_CSPA
PWR_CPUCORE_CSNA
PWR_CPUCORE_CSCOMPA
PWR_CPUCORE_CSP2
PWR_CPUCORE_CSP3
PWR_CPUCORE_CSP1
PWR_CPUCORE_CSN2
PWR_CPUCORE_PWM1
PWR_CPUCORE_PWM3
PWR_CPUCORE_PWM2
PWR_CPUCORE_PWMA
PWR_CPUCORE_DRON
PWR_CPUCORE_VBOOTA
PWR_CPUCORE_CHECK_VBOOTA
PWR_CPUCORE_TRBST
H_PROCHOT_R#
H_CPU_SVIDDAT
H_CPU_SVIDCLK
VR_SVID_ALERT#
1D05V_VTT
3D3V_S0
5V_PWR
DCBATOUT
VSSSENSE
VCCSENSE
VSS_AXG_SENSE
VCC_AXG_SENSE
CPU_CURRENT
BOM Ctrl
UMA
DY
GP
SB_0826
SB_0729
Core Design
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC CPU CORE1 _NCP6131
Size
Document Number
LA470
Rev
SB
Date: Tuesday, September 07, 2010
Sheet 42 of 103

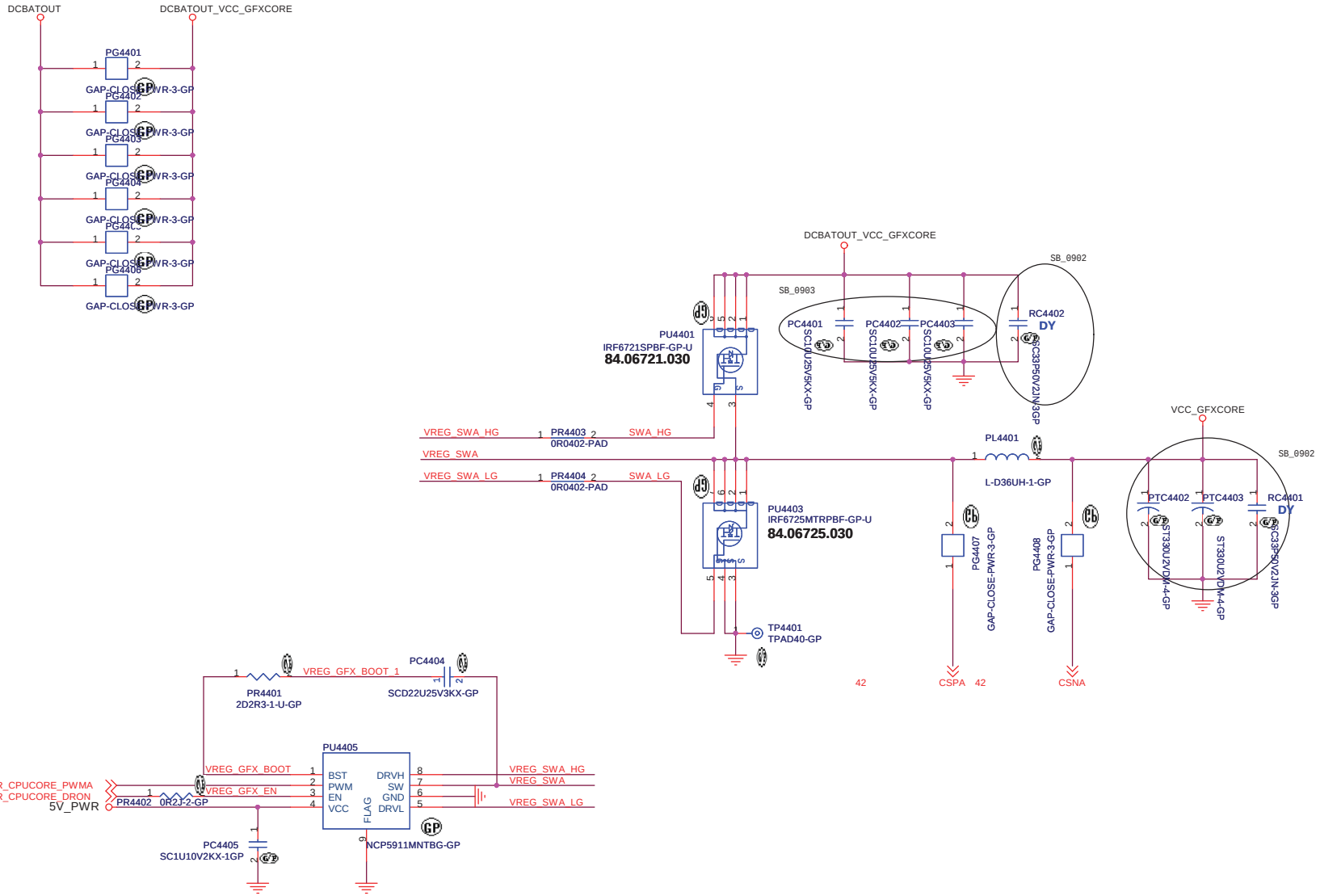


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC CPU CORE2 _NCP6131

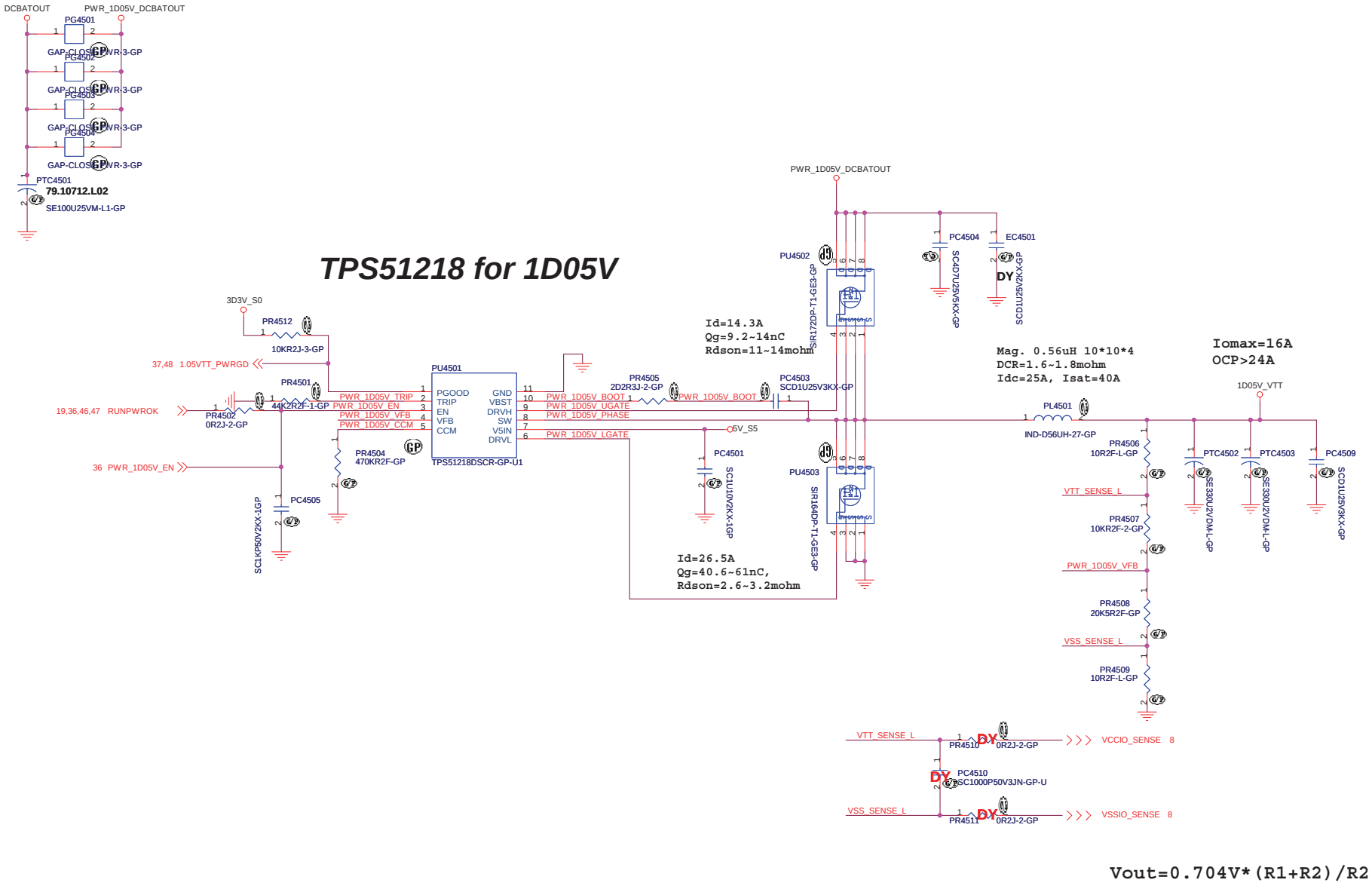
Size	Document Number	Rev
	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 43 of 103



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC/DC CPU CORE3 _NCP6131		
Size	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 44 of 103	



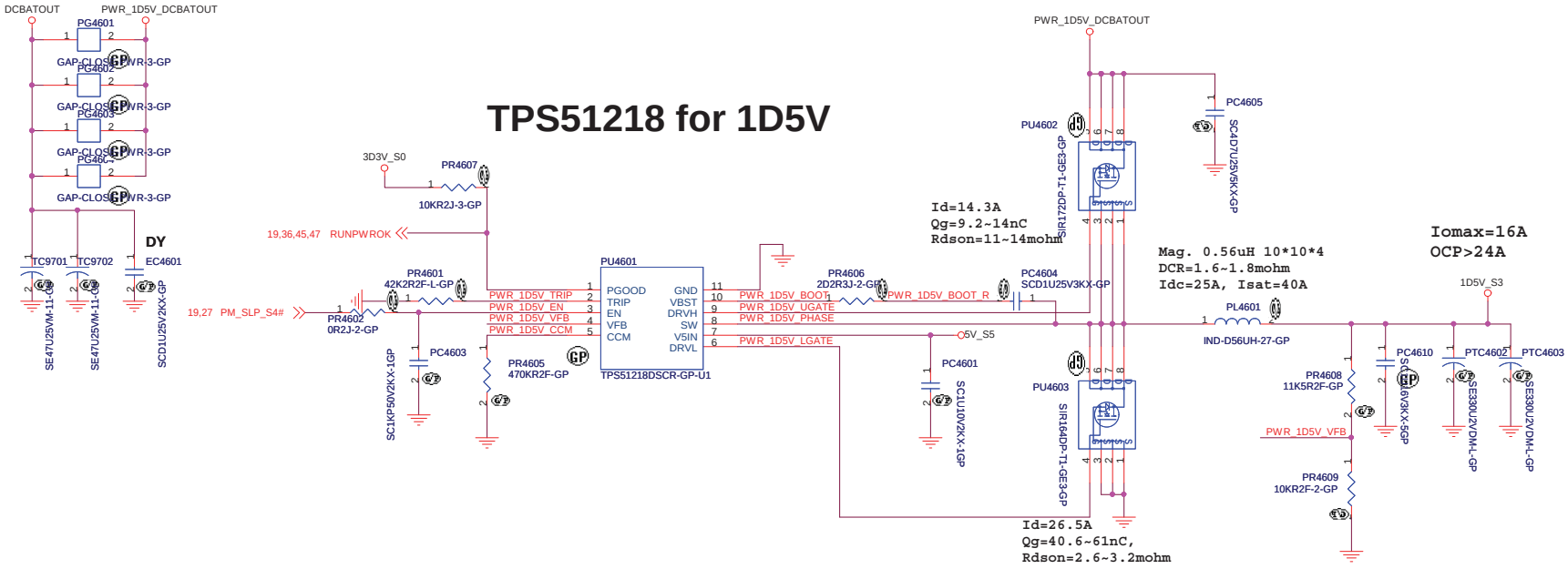
<Core Design>

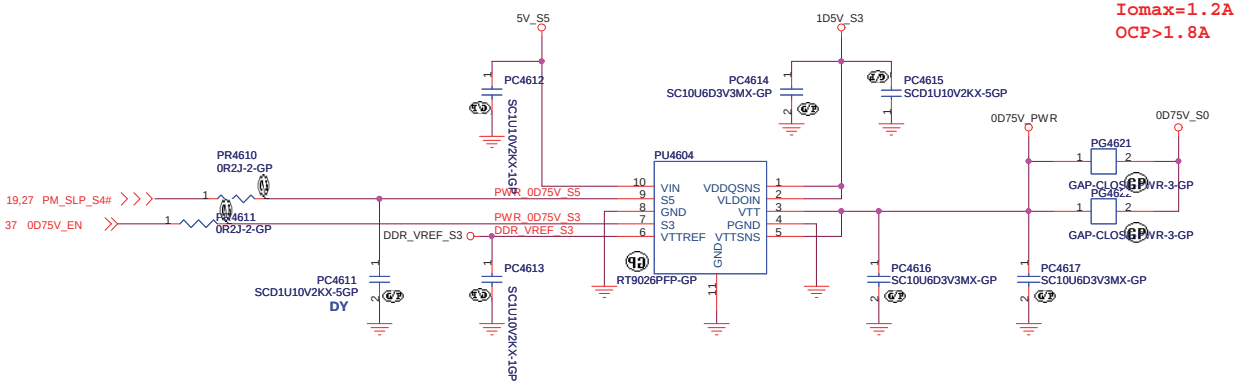
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_1D05V

Size	Document Number	Rev
		SB

Date: Tuesday, September 07, 2010 Sheet 45 of 103





<Core Design>

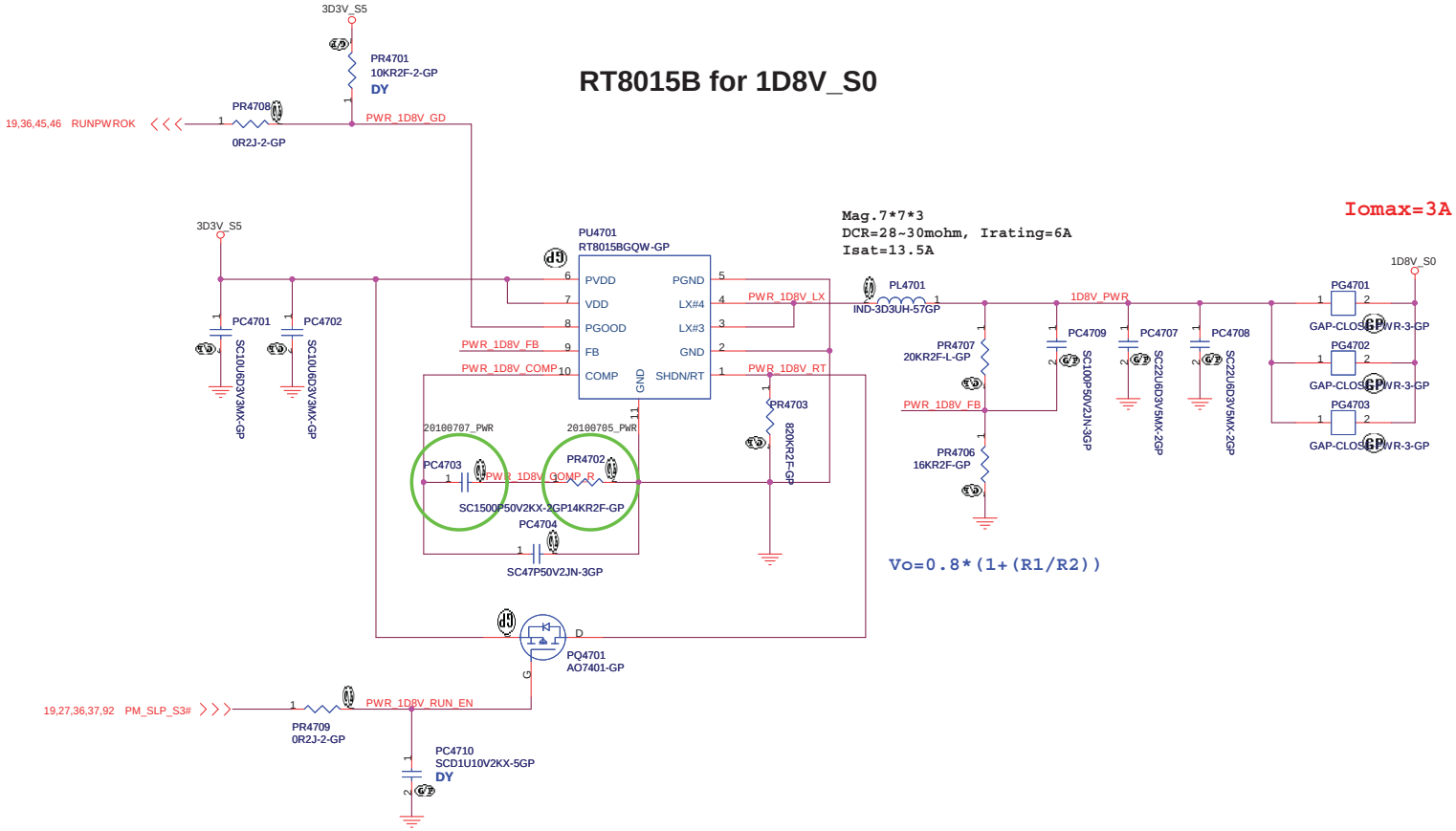
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		SB

Date: Tuesday, September 07, 2010 Sheet 46 of 103

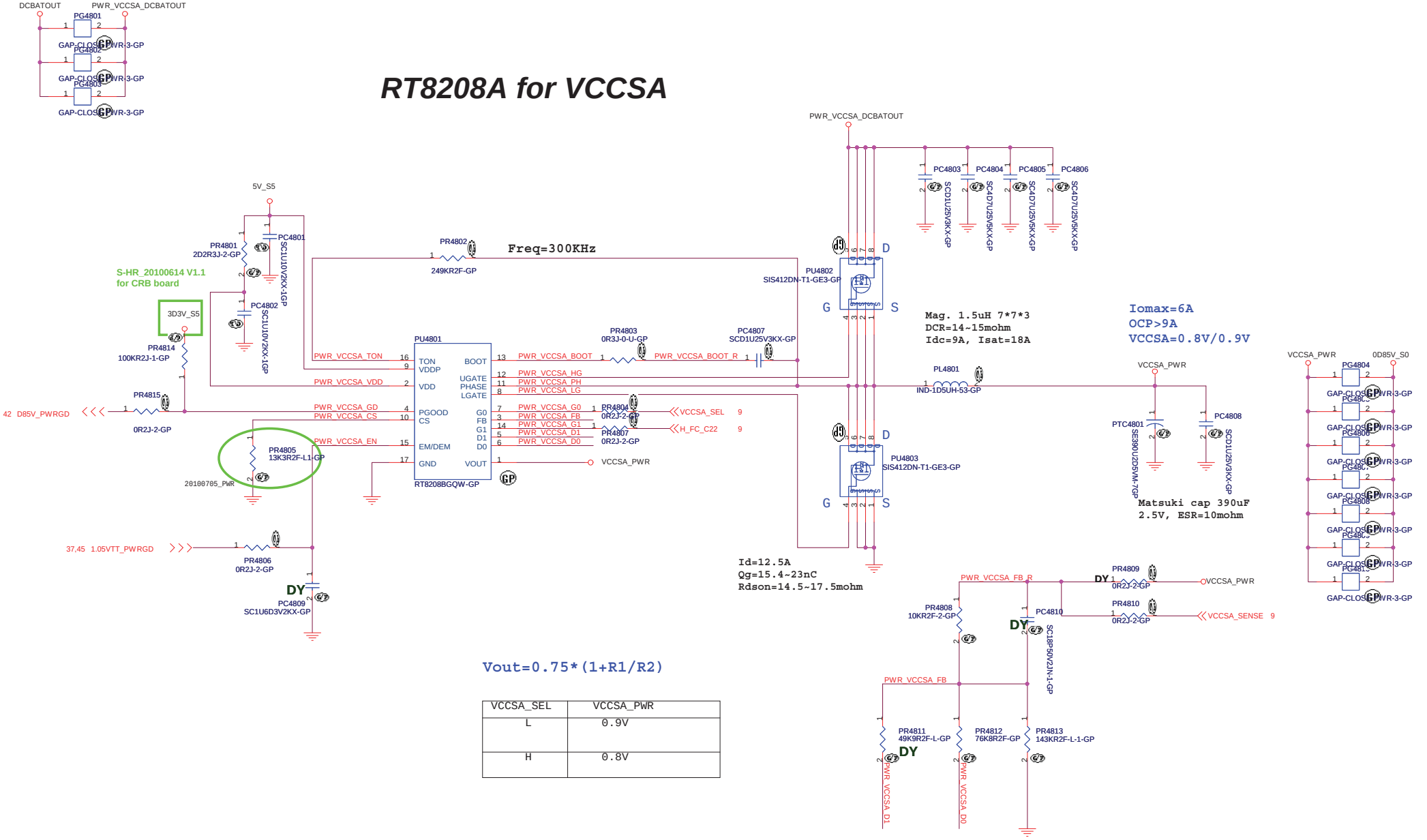
RT8015B for 1D8V_S0



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWM_1D8V_RT8015B		
Size	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 47 of 103	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

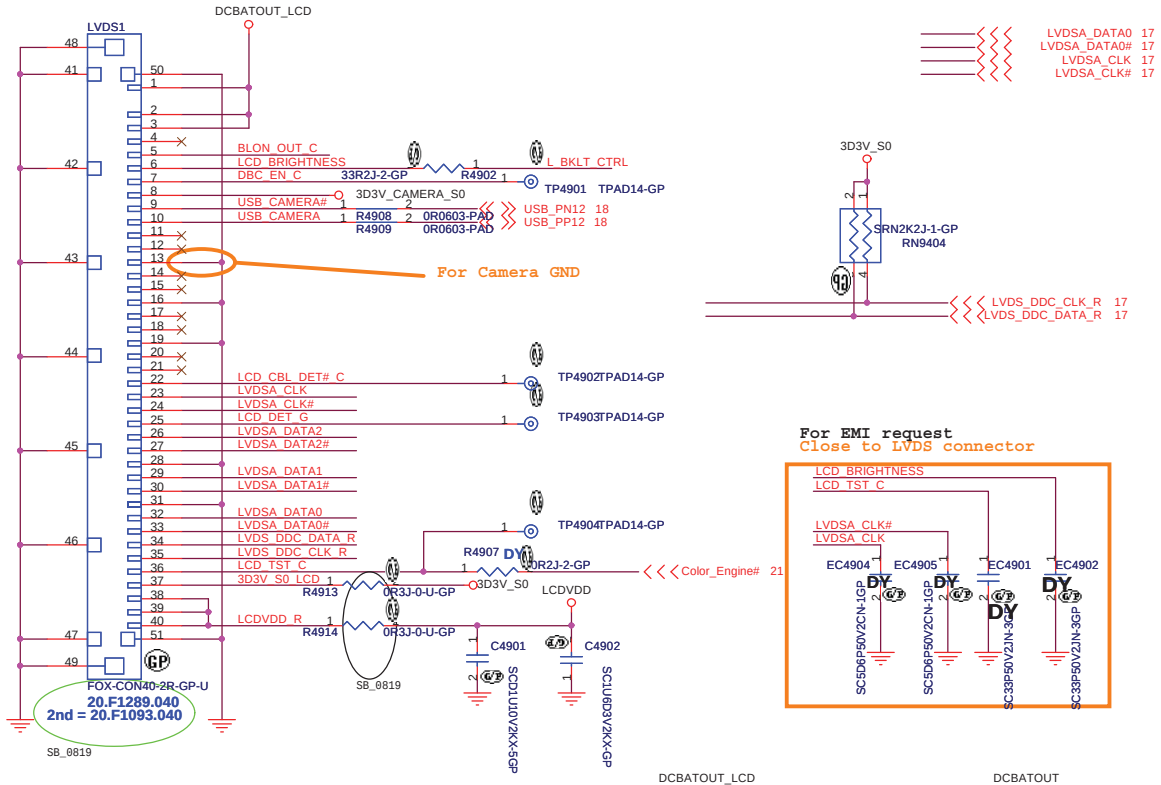
<Core Design>

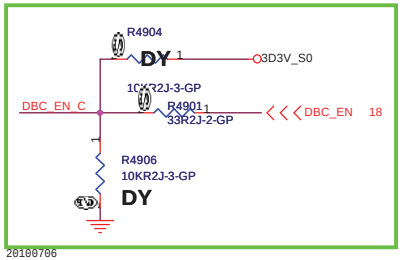
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8208B_VCCSA	
Size	Document Number LA470	Rev SB
Date: Tuesday, September 07, 2010	Sheet 48 of 103	

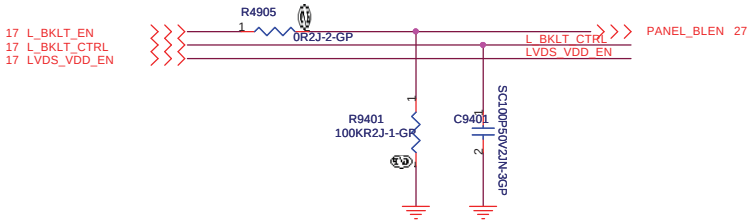
SSID = VIDEO

LVDS CONNECTOR

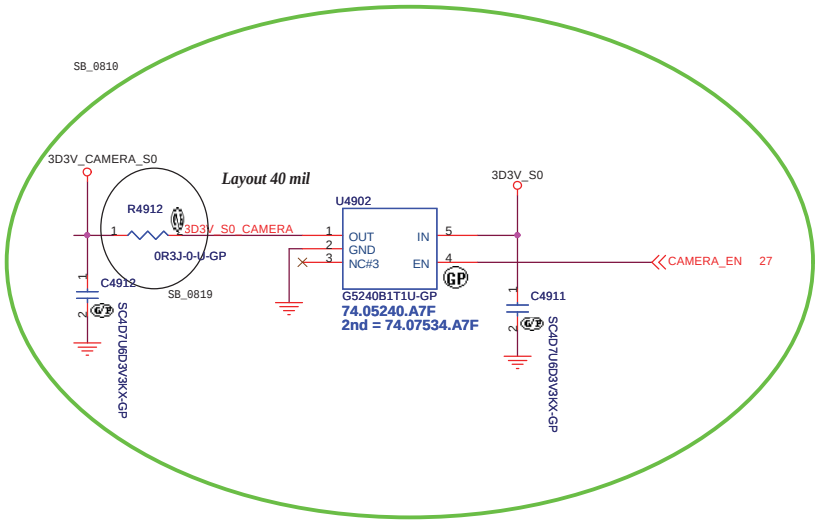




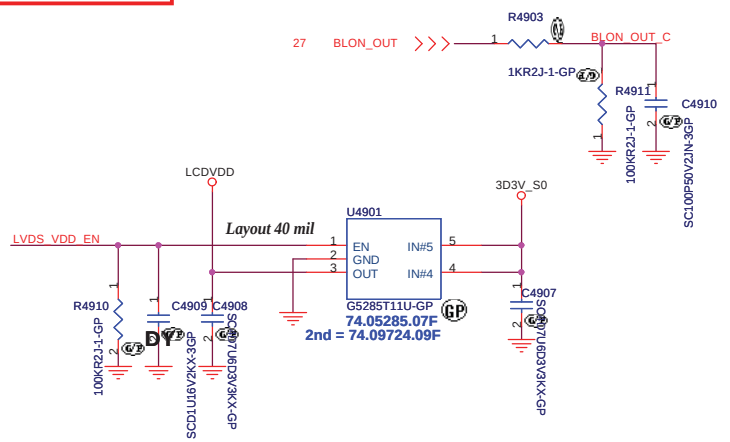
Panel BL brightness/Power En/BL En



CAMERA POWER



SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
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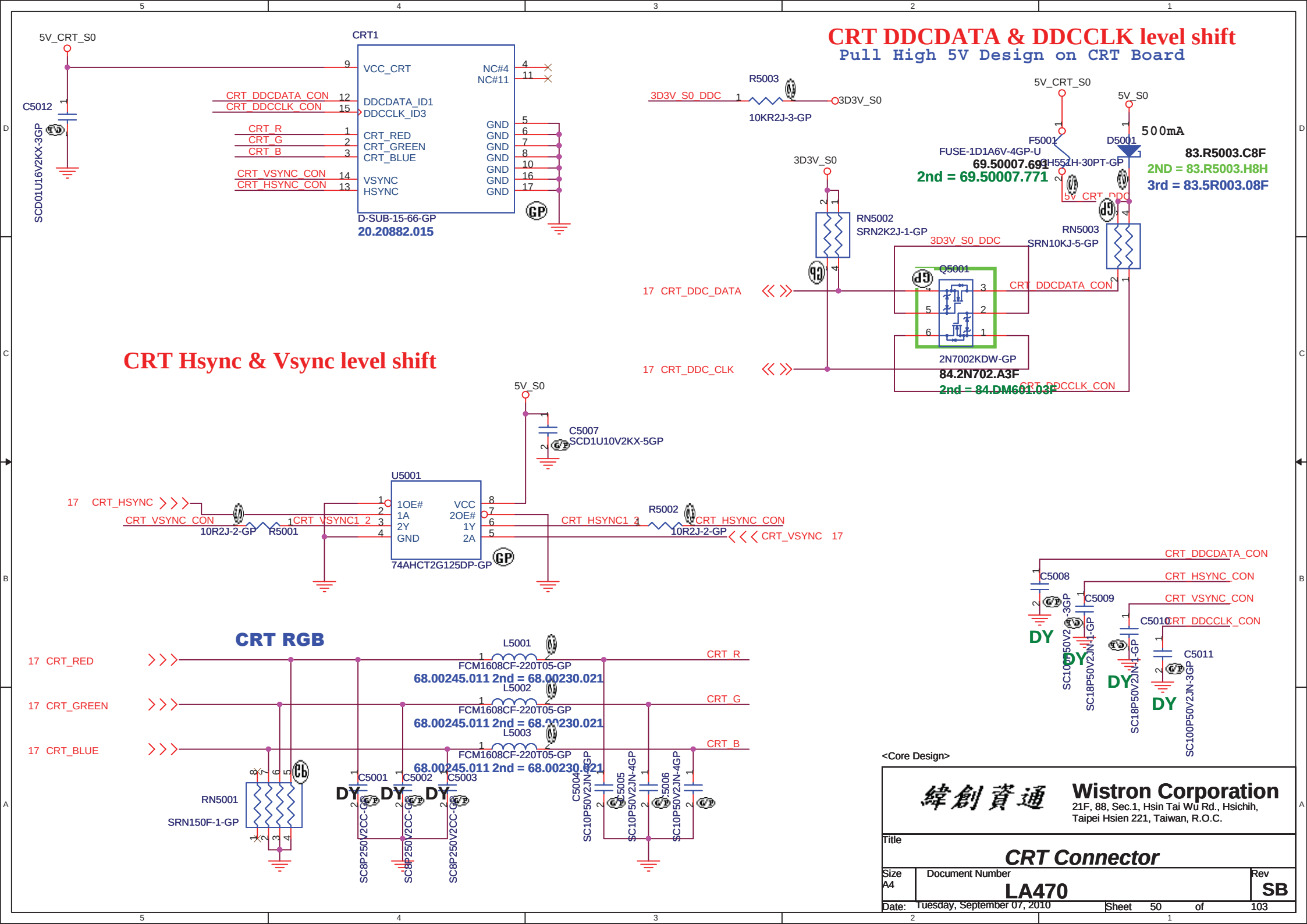
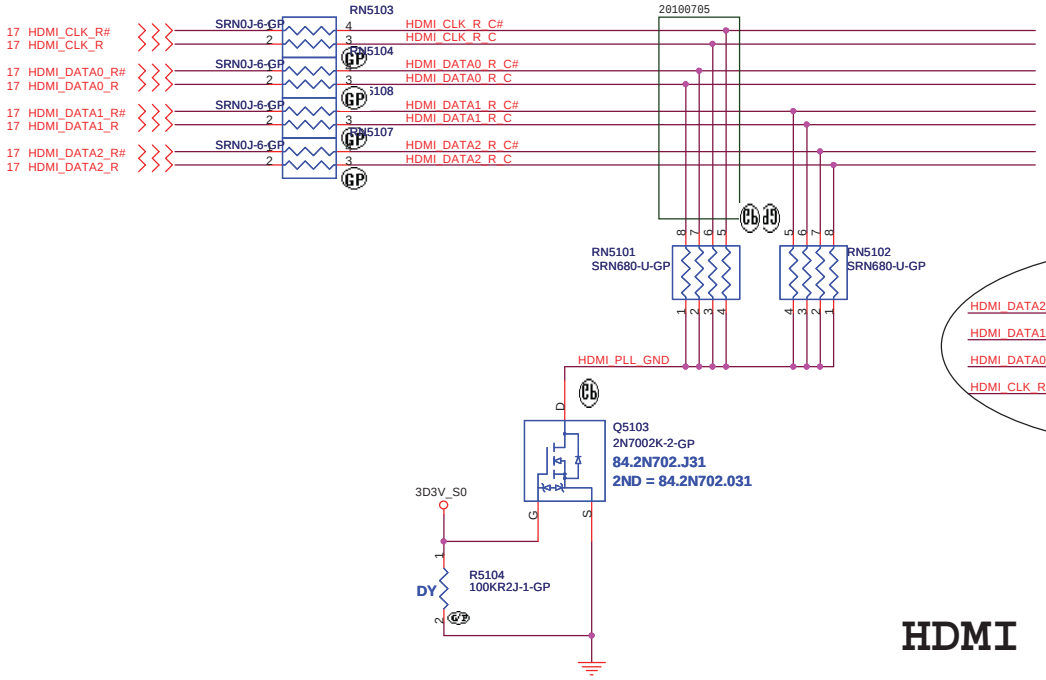

CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board
CRT Hsync & Vsync level shift
CRT RGB
5V_CRT_S0
CRT1
VCC_CRT
NC#4
NC#11
CRT_DDCDATA_CON
CRT_DDCCLK_CON
DDCDATA_ID1
DDCCLK_ID3
CRT_R
CRT_G
CRT_B
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_VSYNC_CON
CRT_HSYNC_CON
VSYNC
HSYNC
GND
D-SUB-15-66-GP
20.20882.015
C5012
SCD01U16V2KX-3GP
R5003
3D3V_S0_DDC
3D3V_S0
10KR2J-3-GP
5V_S0
500mA
F5001
FUSE-1D1A6V-4GP-U
D5001
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
69.50007.691
2nd = 69.50007.771
5V_CRT_DDC
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-5-GP
Q5001
17 CRT_DDC_DATA
17 CRT_DDC_CLK
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
C5007
SCD1U10V2KX-5GP
U5001
1OE#
1A
2Y
GND
VCC
2OE#
1Y
2A
74AHCT2G125DP-GP
17 CRT_HSYNC
17 CRT_VSYNC
10R2J-2-GP
R5001
R5002
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
L5001
L5002
L5003
FCM1608CF-220T05-GP
68.00245.011 2nd = 68.00230.021
RN5001
SRN150F-1-GP
C5001
C5002
C5003
DY
SC8P250V2CC-GP
C5004
C5005
C5006
SC10P50V2JN-4GP
C5008
C5009
C5010
C5011
SC18P50V2JN-1-GP
SC100P50V2JN-3GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
A4
Document Number
LA470
Rev
SB
Date: Tuesday, September 07, 2010
Sheet 50 of 103

SSID = VIDEO

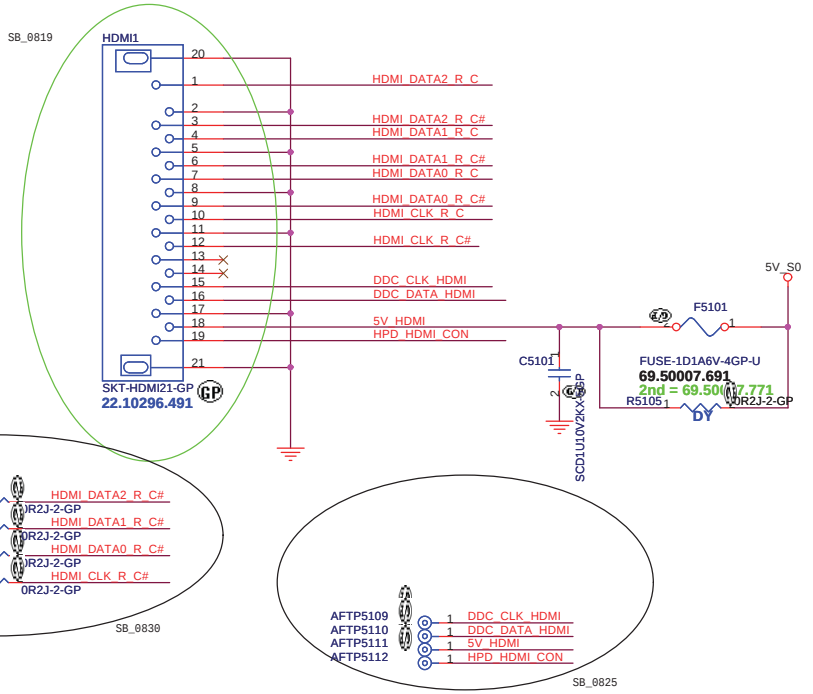
HDMI CONNECTOR

HDMI Passive Level Shifter

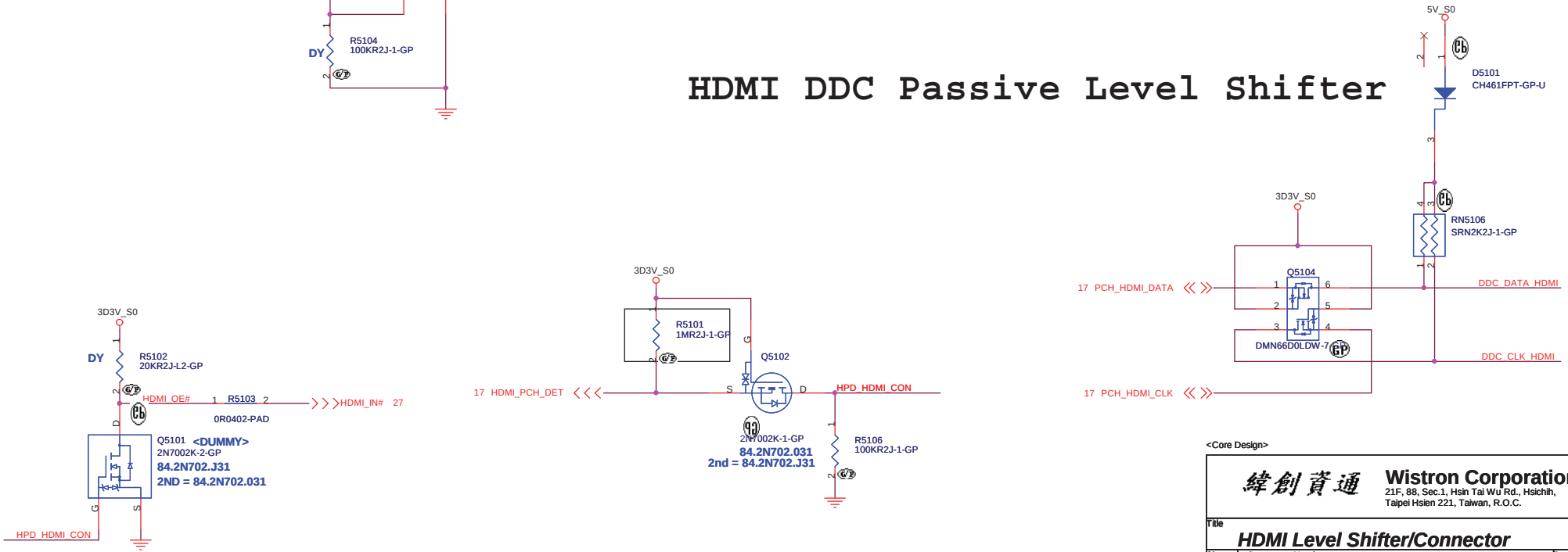
Close to HDMI Connector



HDMI CONN



HDMI DDC Passive Level Shifter



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI Level Shifter/Connector		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 51 of 103	

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size: A3 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 52 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***		
Size: A4	Document Number: **LA470**	Rev: **SB**
Date: Tuesday, September 07, 2010	Sheet 53 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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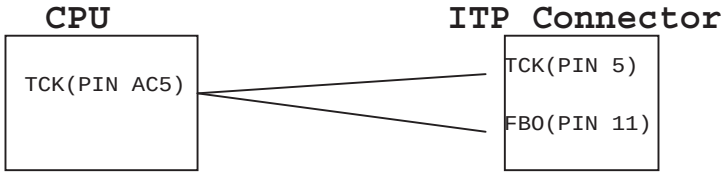
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: LA470	Rev: SB
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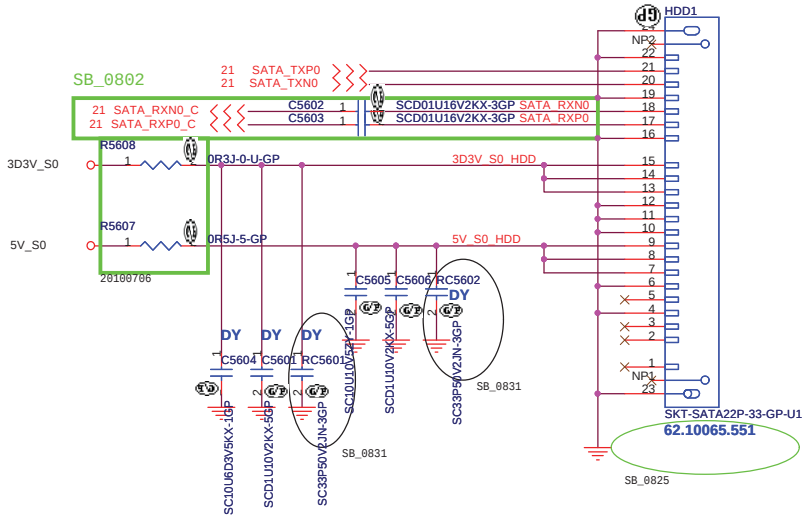
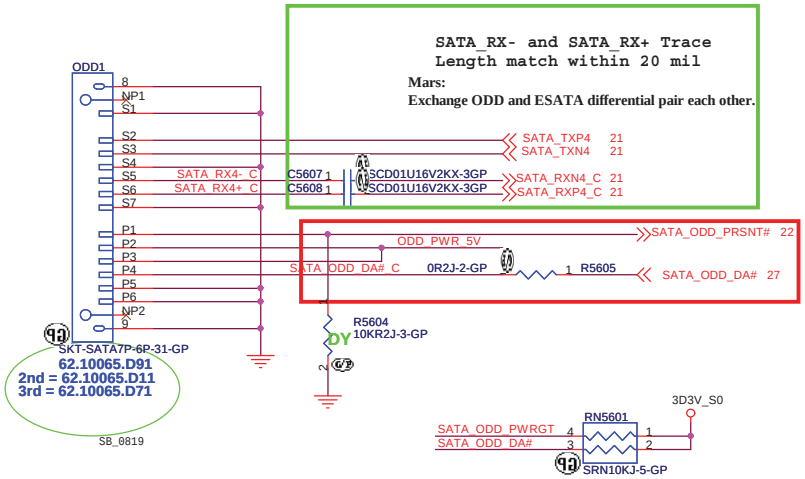
SSID = SATA

SATA HDD Connector

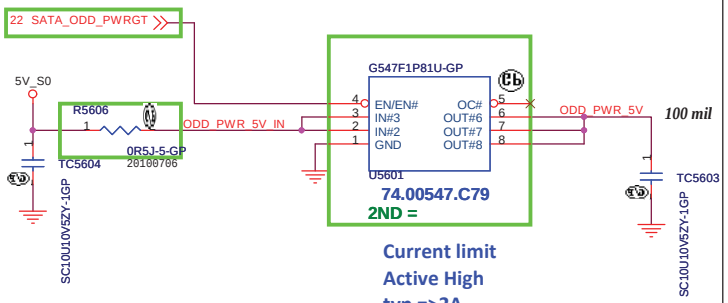


ODD Connector



SUPPORT ZERO SATA ODD

SATA Zero Power ODD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
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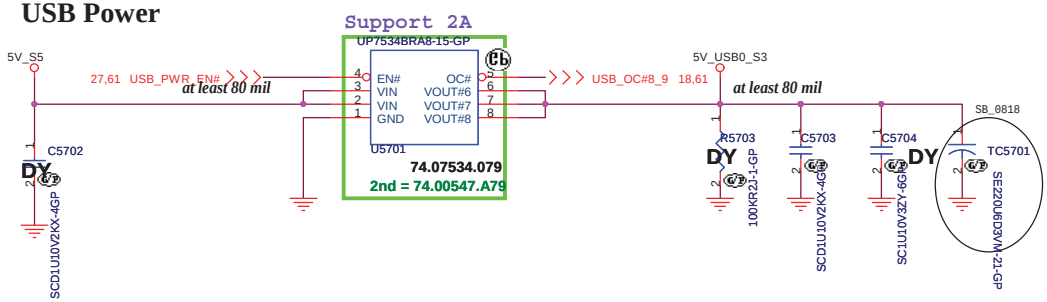
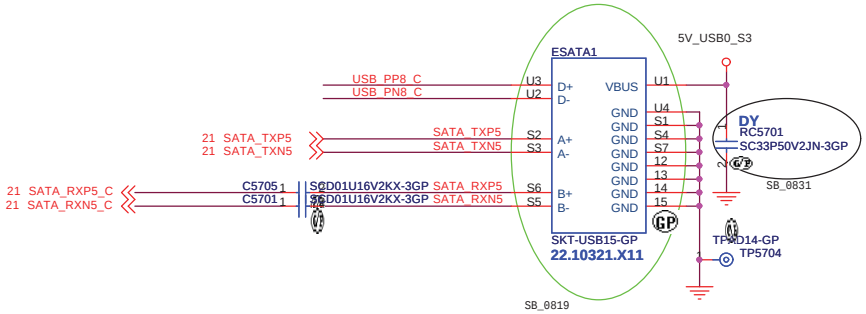
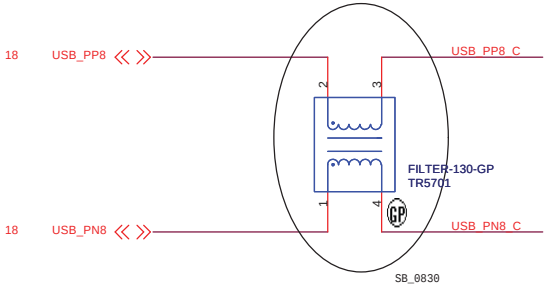
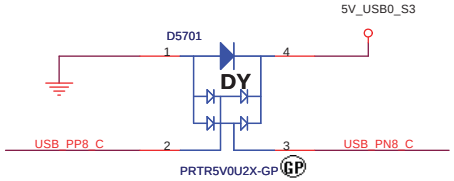
USB Power









<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA

Size	Document Number	Rev
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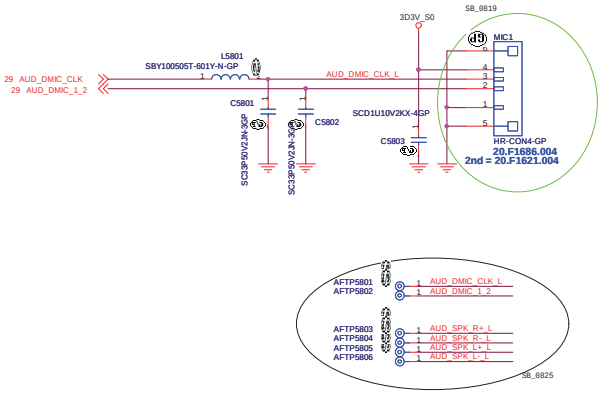
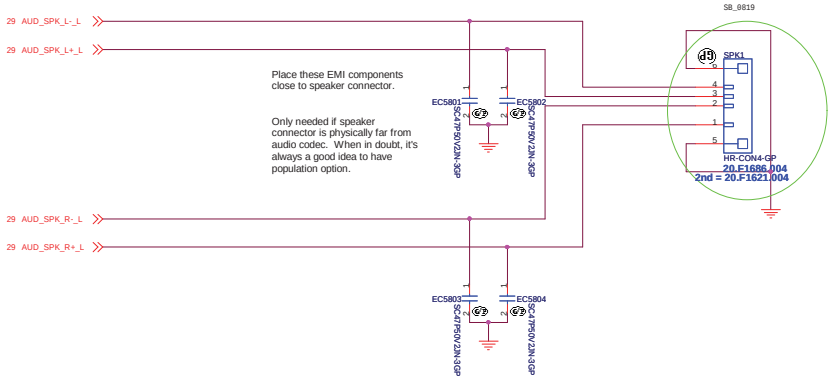


INTERNAL STEREO SPEAKERS

Port G



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MIC/SPEAKER/AUDIO JACK

Size	Document Number	Rev
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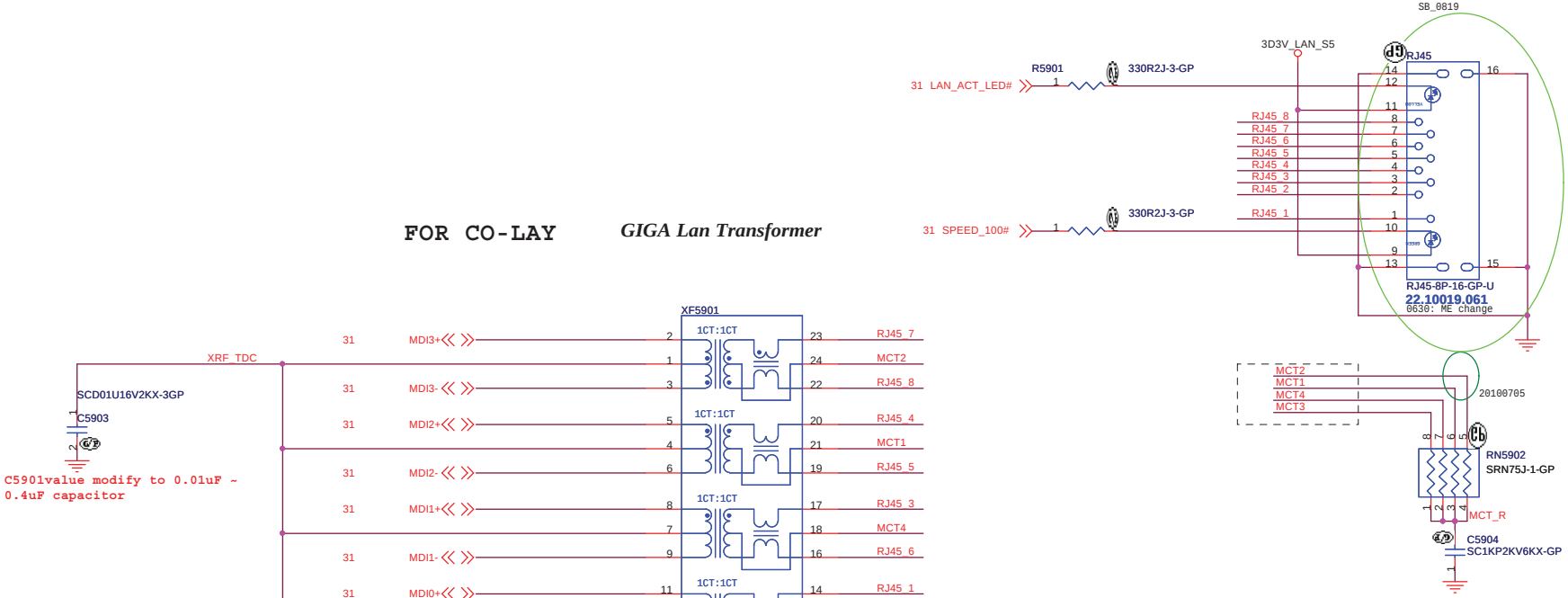
LAN Connector



1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

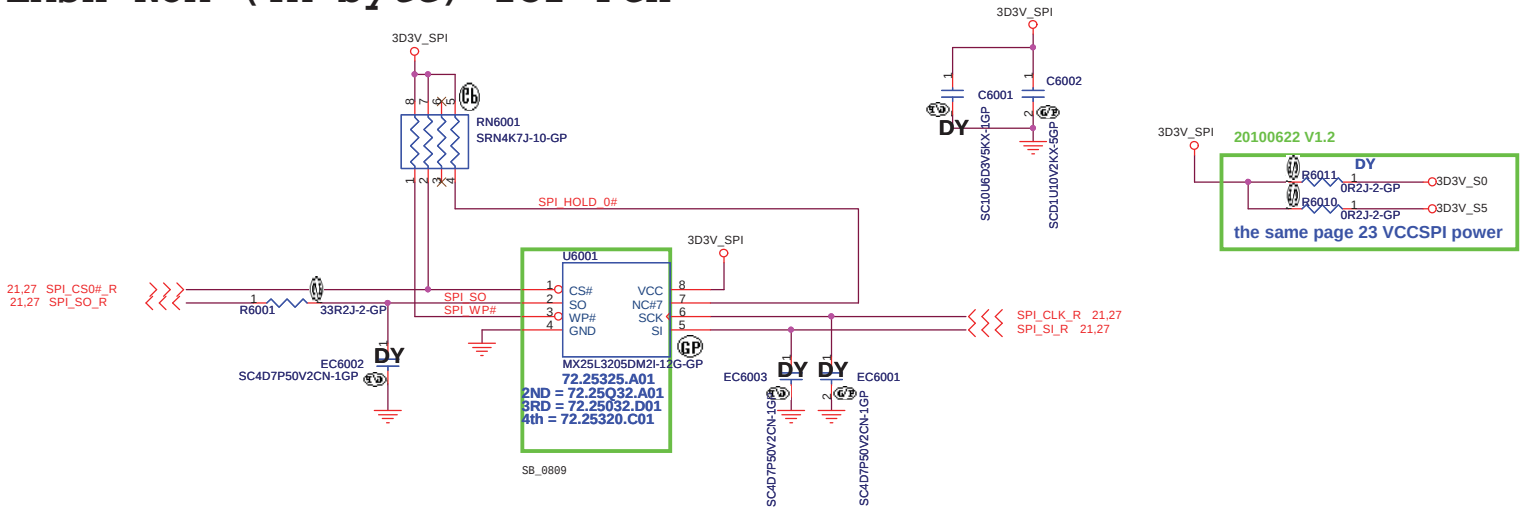
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

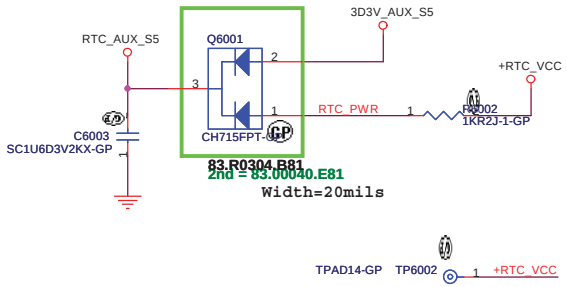
Title: RJ45 / Transformer		
Size: A3	Document Number: LA470	Rev: SB
Date: Tuesday, September 07, 2010	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
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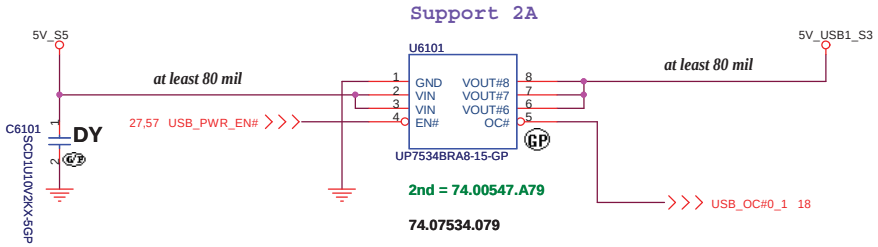
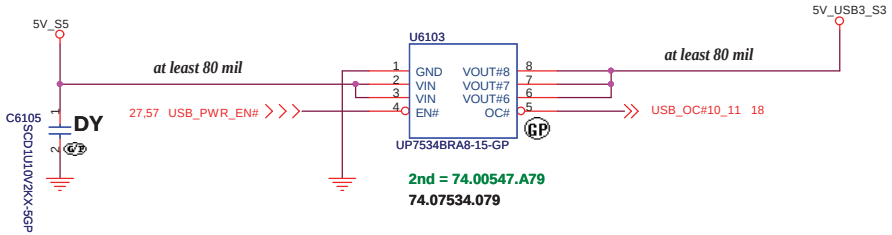
SSID = USB

IO Board USB Power



Sub-USB Board Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

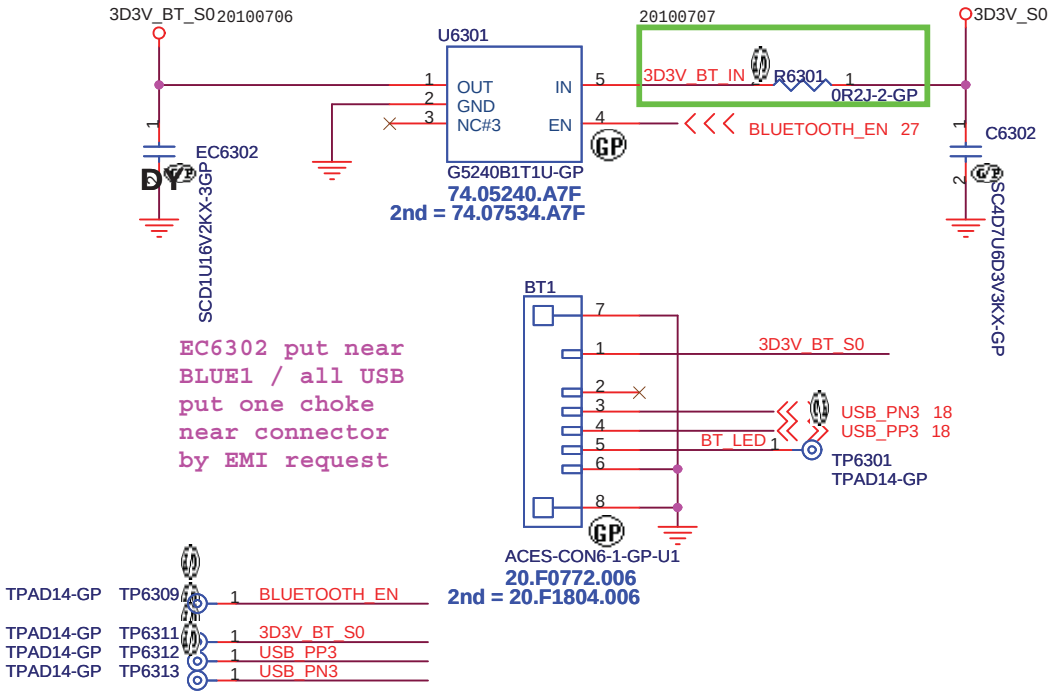
Title: *USB 3.0 Port*

Size	Document Number	Rev
A3	LA470	SB

SSID = User.Interface

Bluetooth Module conn.

Bluetooth Module



<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth**		
Size: A4	Document Number: **LA470**	Rev: **SB**
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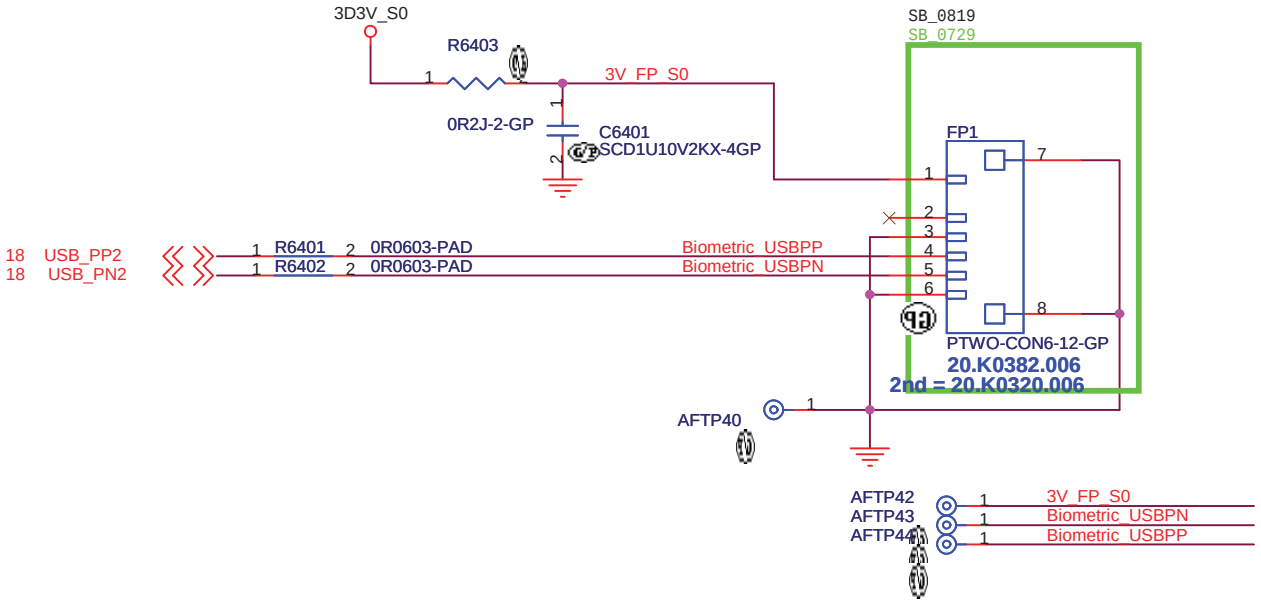
Finger Printer Connector



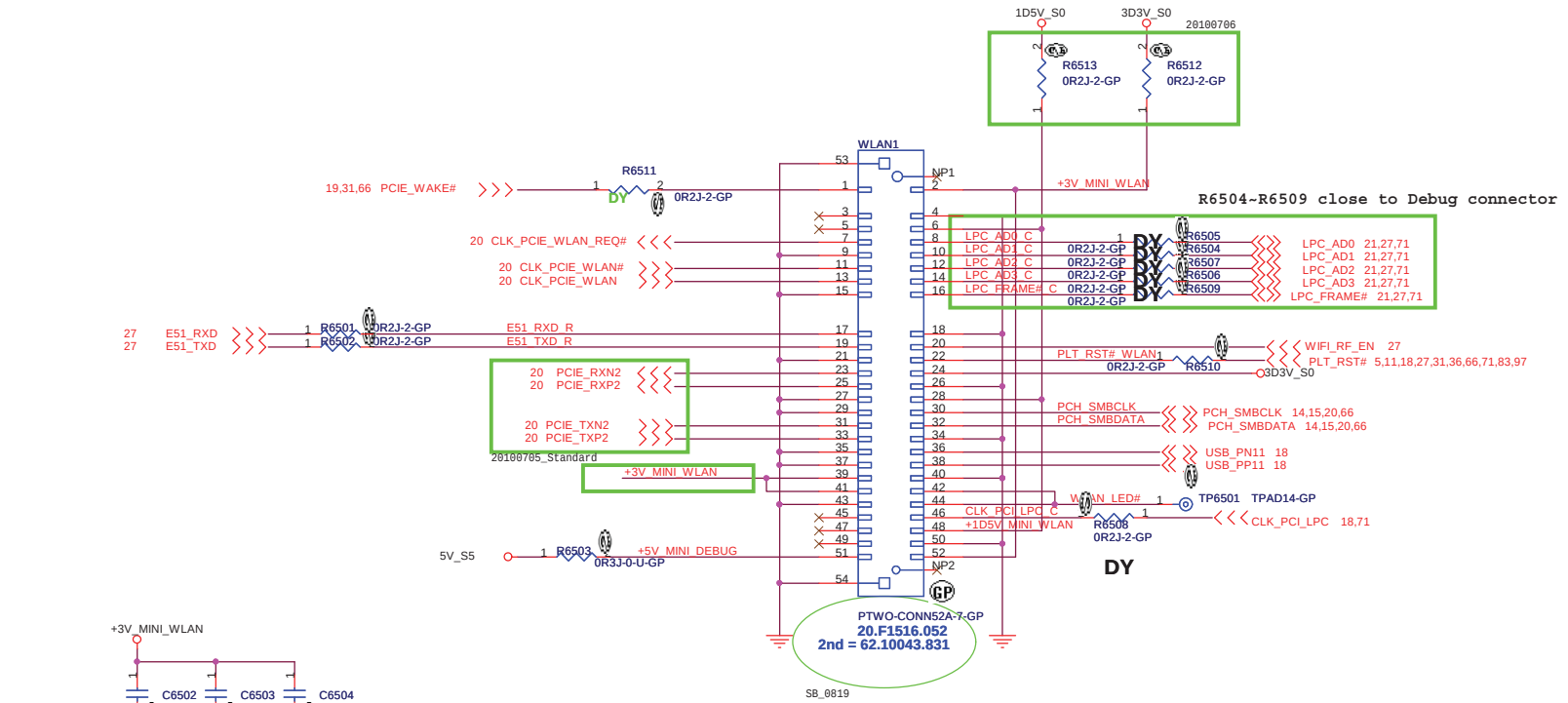
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***		
Size: A4	Document Number: **LA470**	Rev: **SB**
Date: Tuesday, September 07, 2010	Sheet 64 of 103	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
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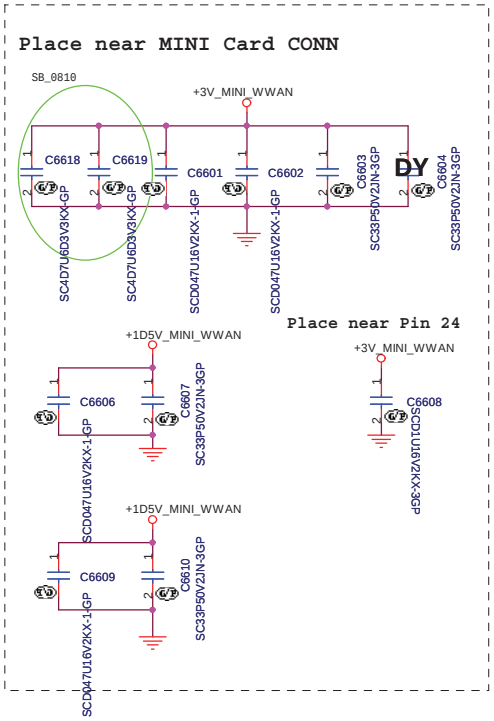
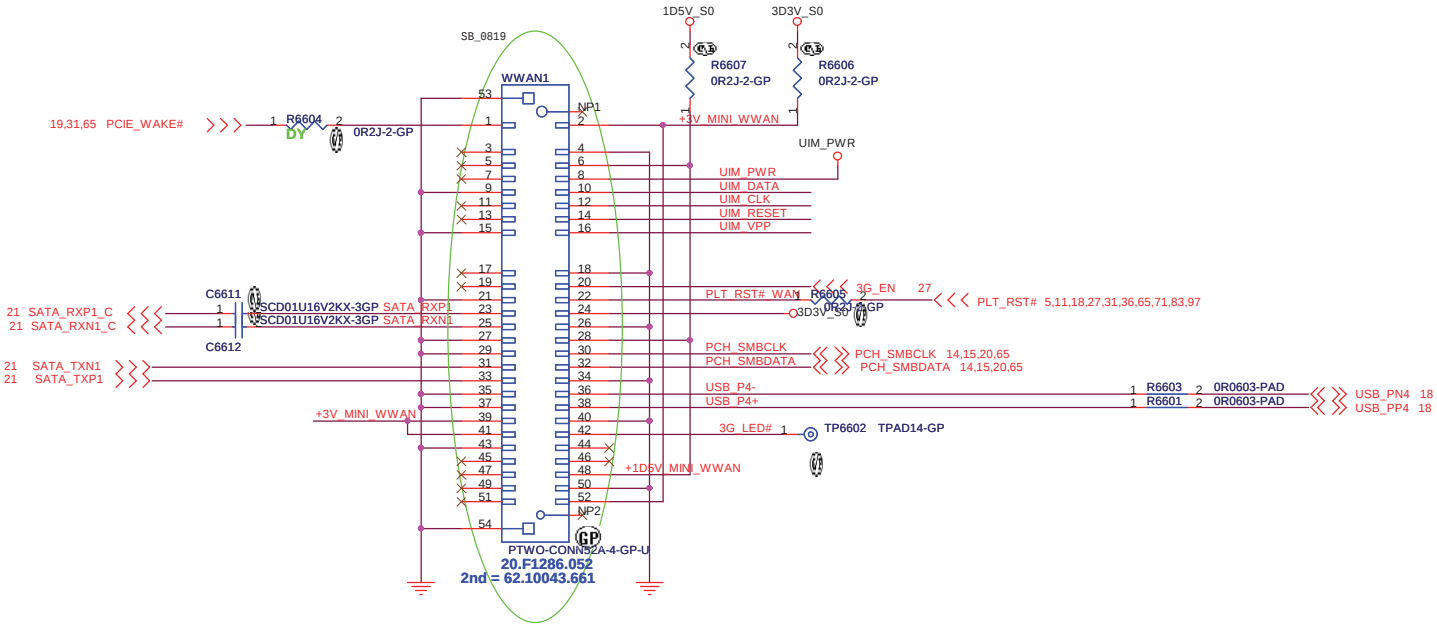
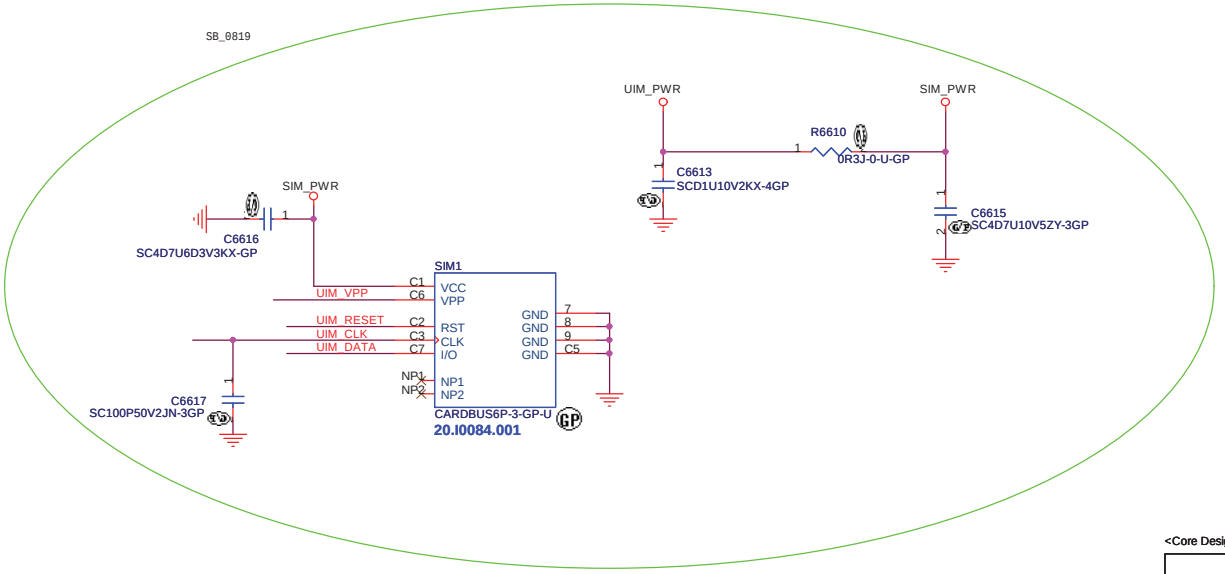
Date: Tuesday, September 07, 2010 Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size	Document Number	Rev
A3	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 66 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

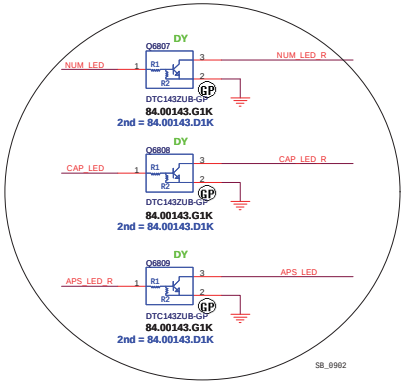
Title: ***Reserved***

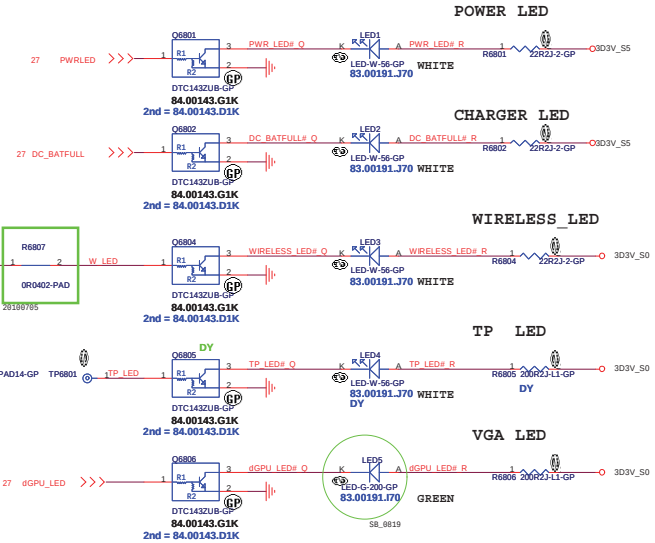
Size	Document Number	Rev
A4	LA470	SB

Date: Tuesday, September 07, 2010 Sheet 67 of 103

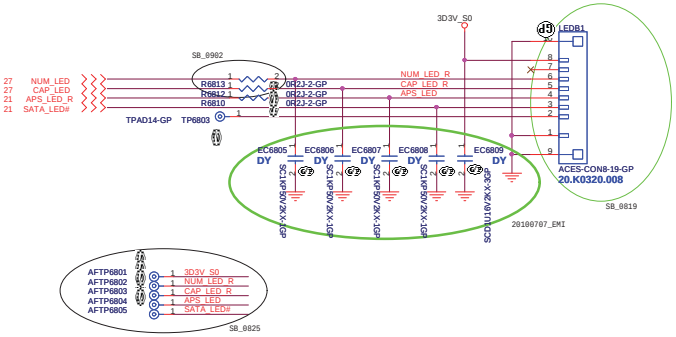
SSID = User.Interface

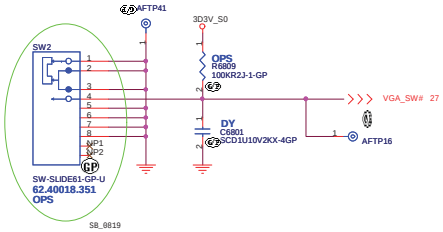
Power button LED

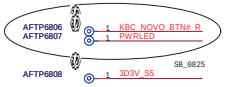




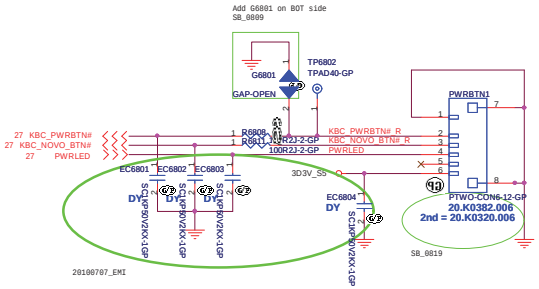
LED Bord CONN.







Power button LED(White)



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

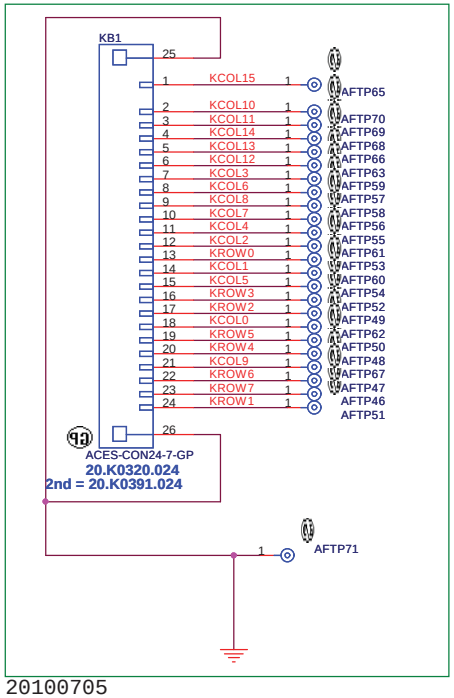
Title: LED Bard/Power Button

Size: A2 | Document Number: LA470 | Rev: SB

Date: Tuesday, September 07, 2010 | Sheet 68 of 103

SSID = KBC

Internal KeyBoard Connector



KROW[0..7] 27

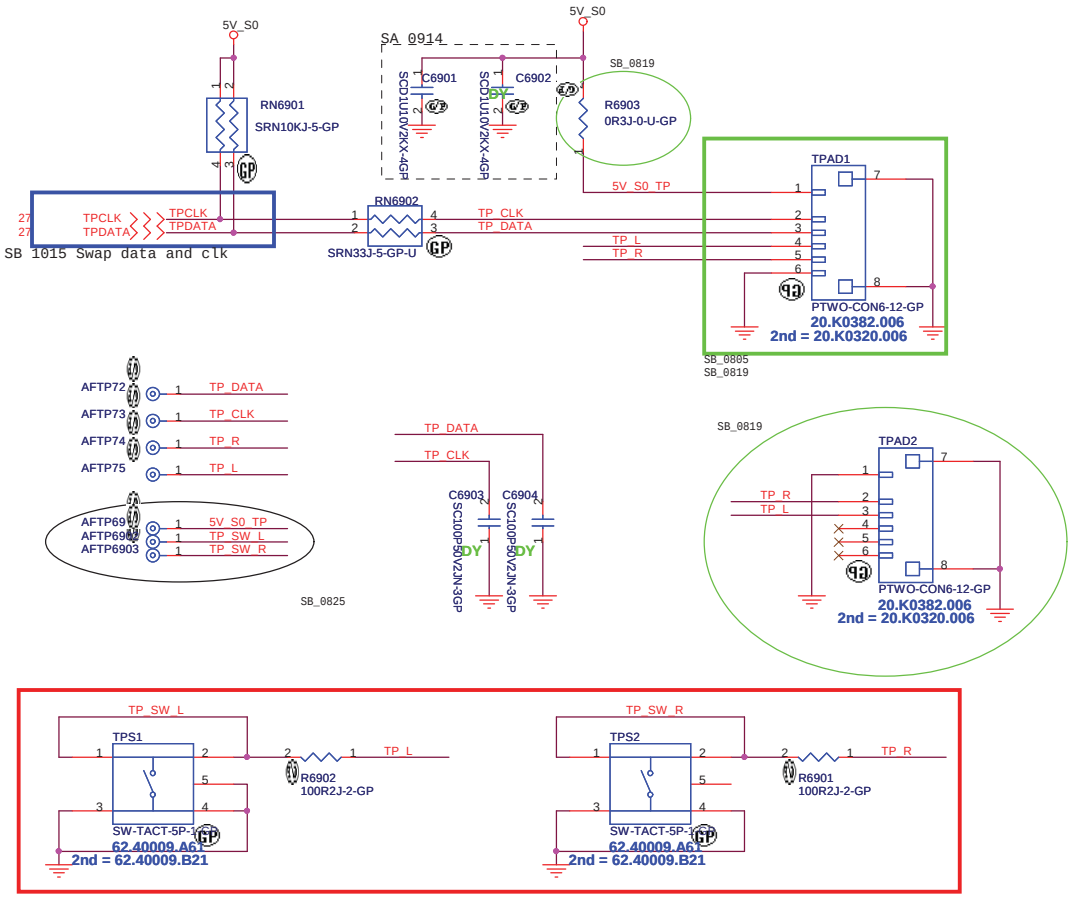
KCOL[0..15] 27

20100705

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Key Board/Touch Pad**
Size: A3	Document Number: **LA470**
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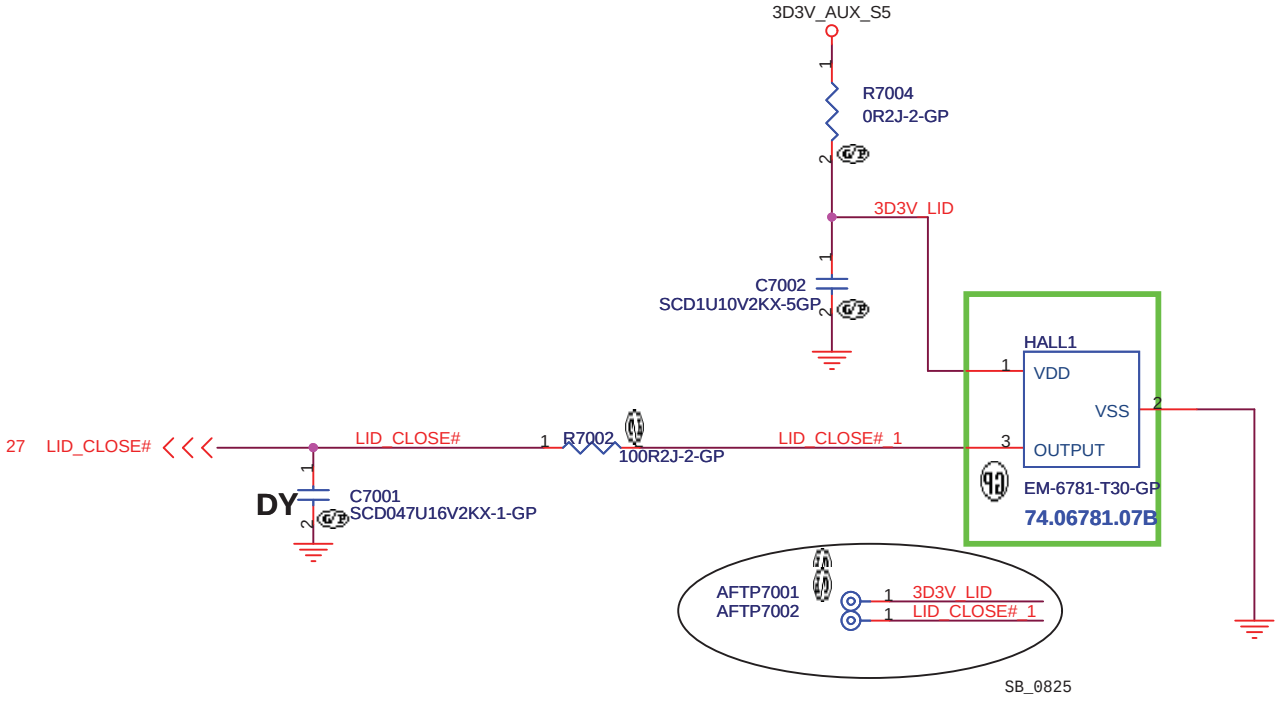

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

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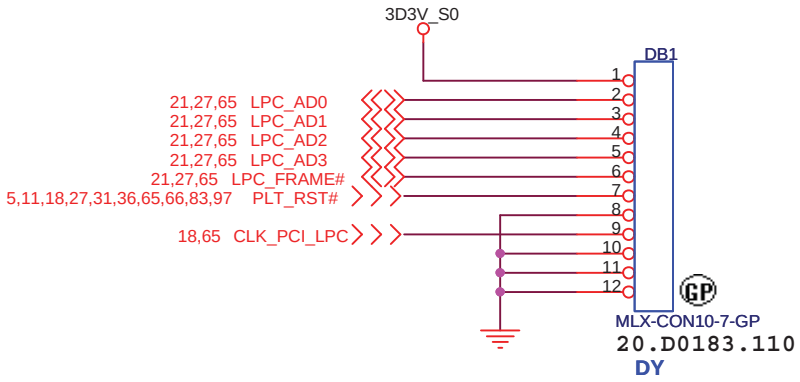

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

New Card

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

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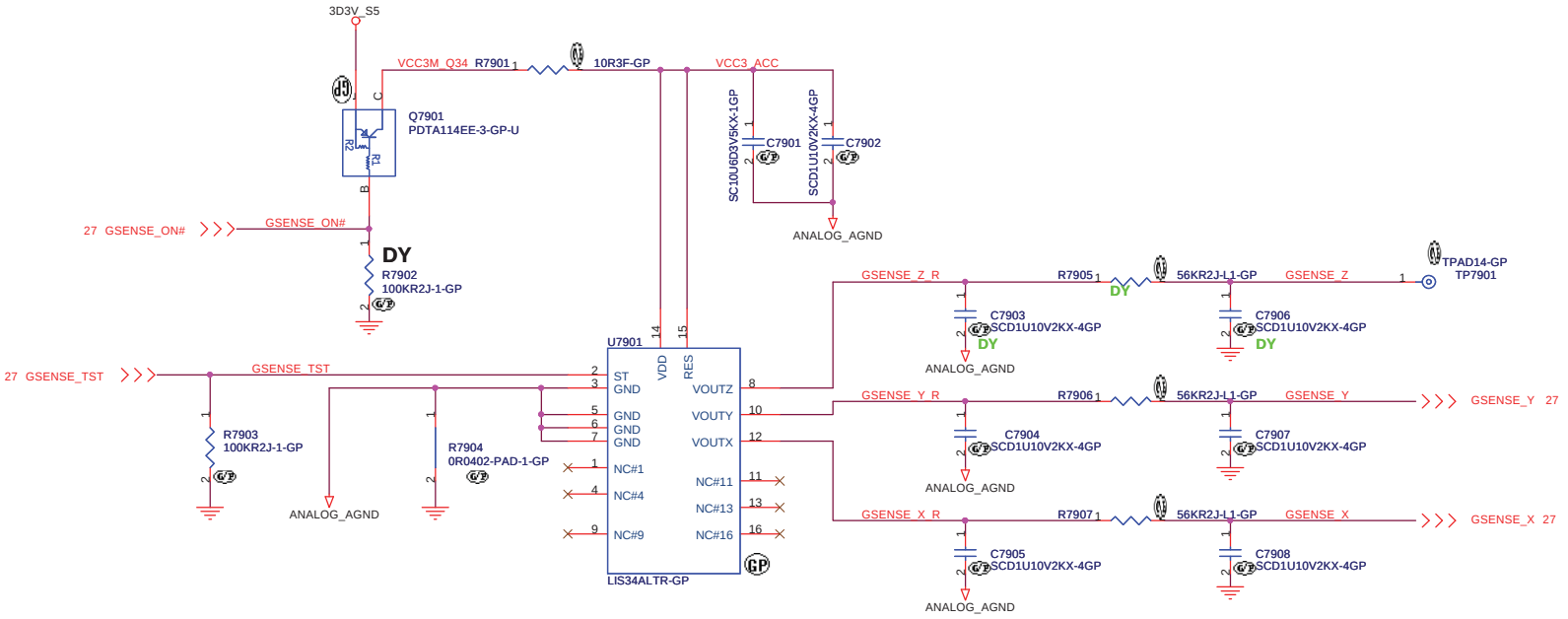
G-Sensor



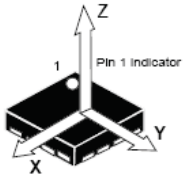
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size: Custom | Document Number: **LA470** | Rev: **SB**

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

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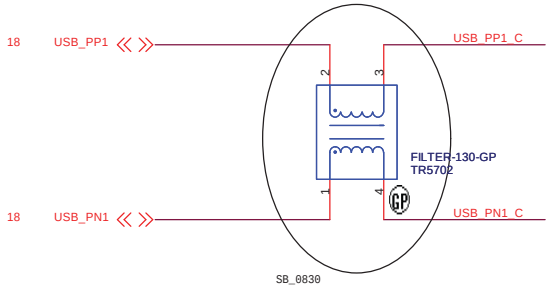
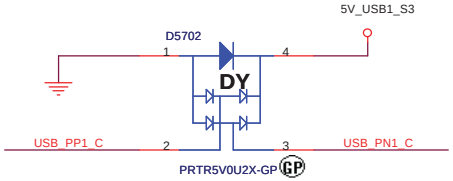
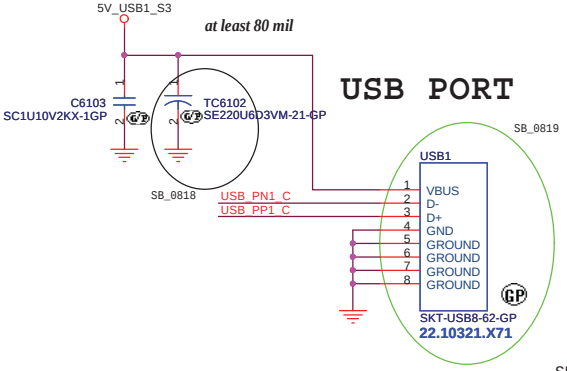
IO Board CONN 80 pin

USB1



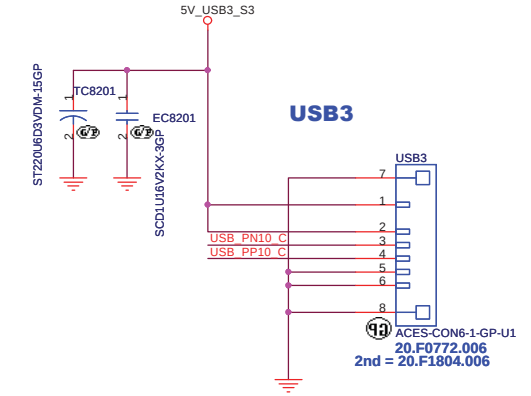




USB PORT

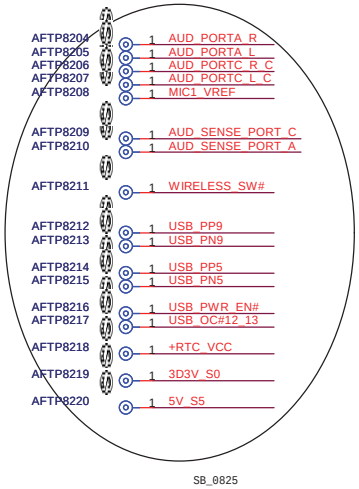
Mars:
Exchange ODD and ESATA differential pair each other.

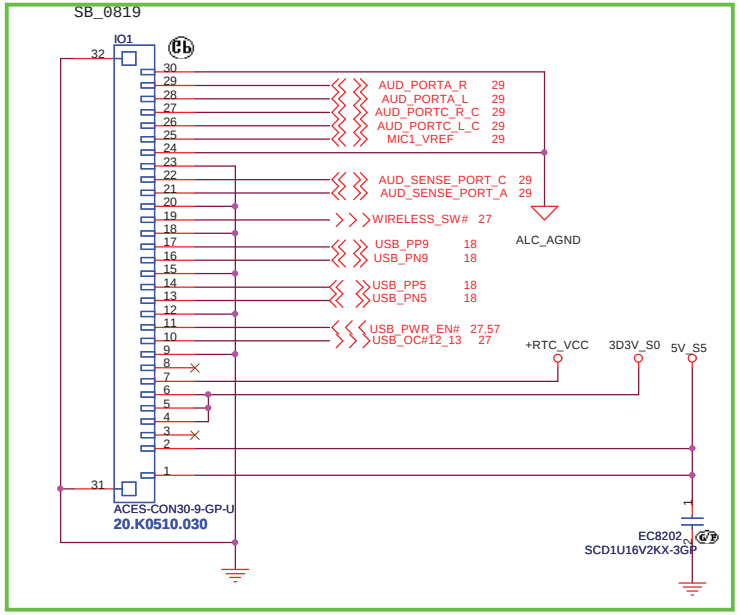
USB Board CONN.

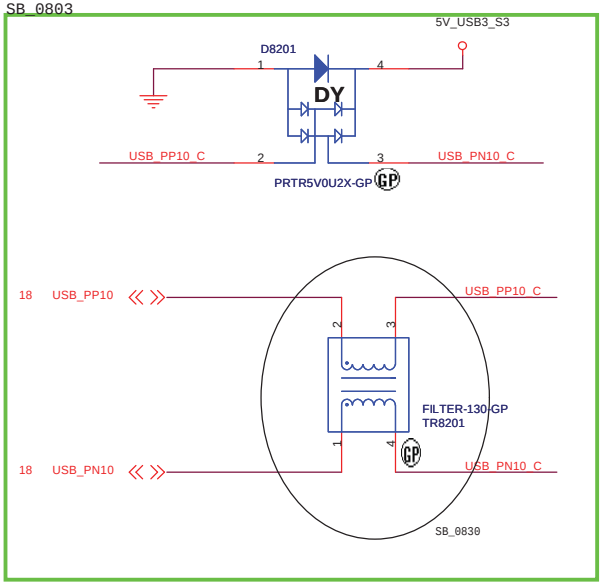


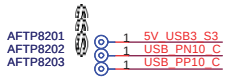
USB3

I/O Board CONN.









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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: IO Board Connector		
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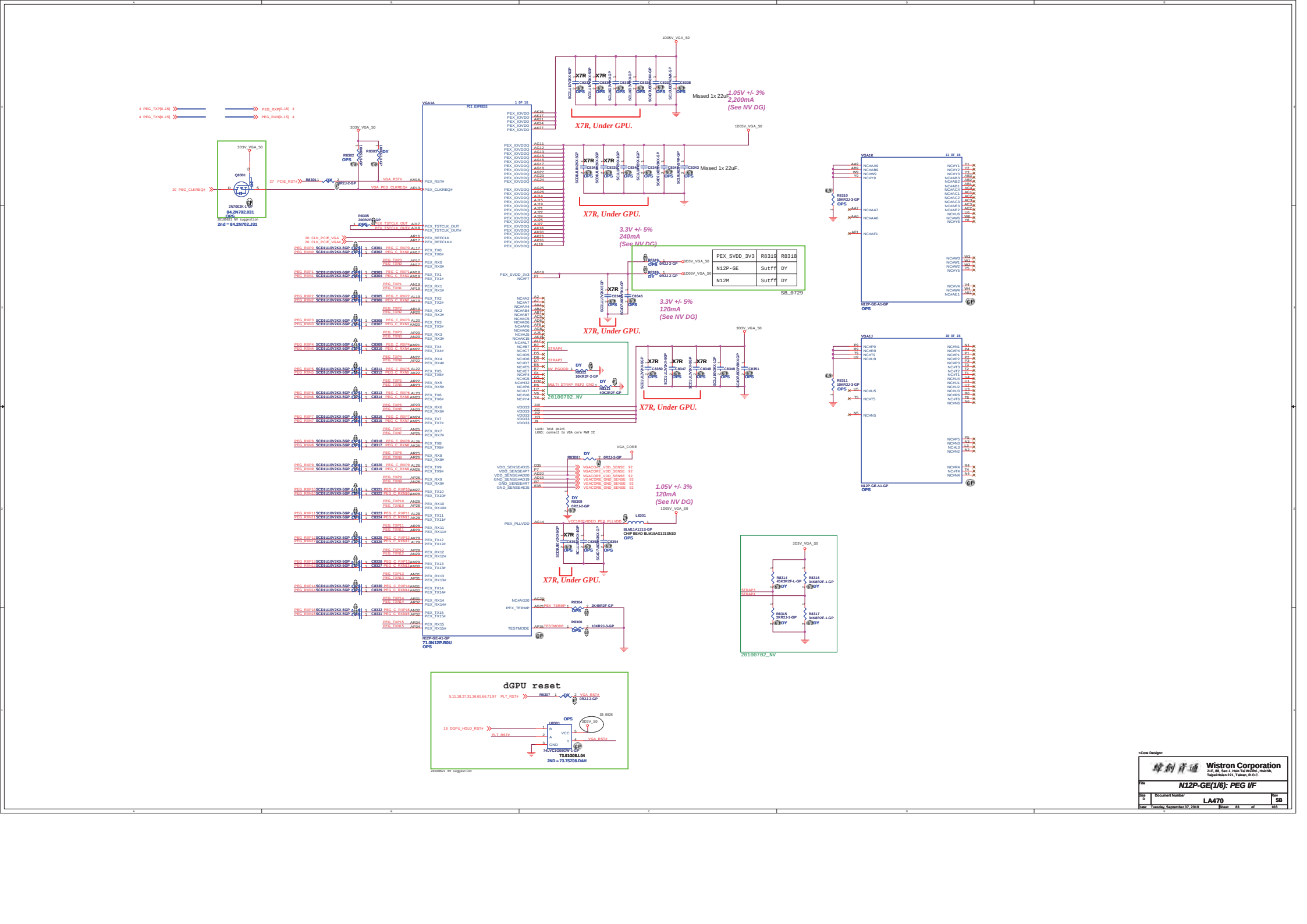

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Wistron Corporation
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Title: N12P-GE(1/6): PEG I/F

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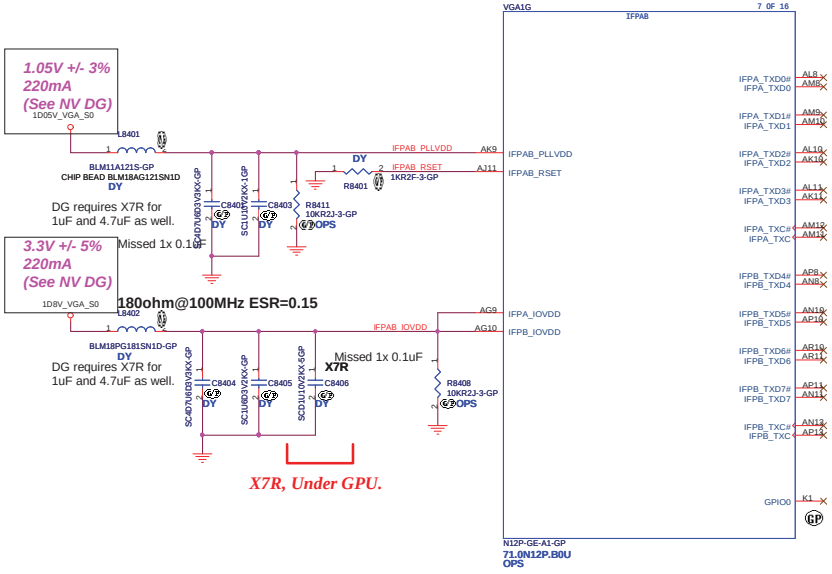
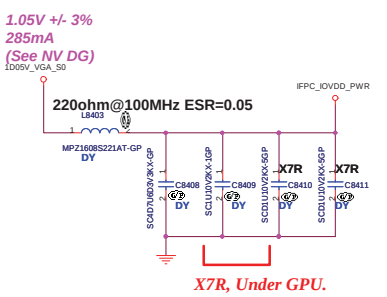
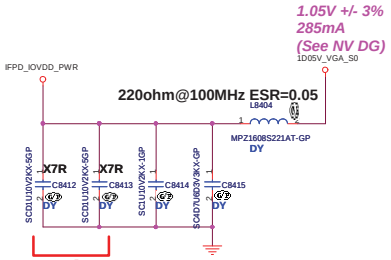
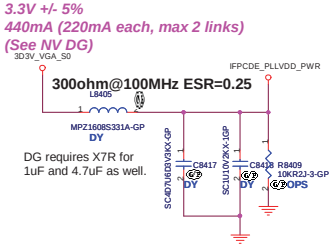
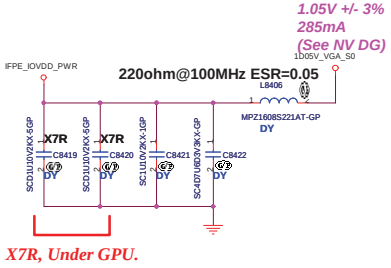
LVDS Interface

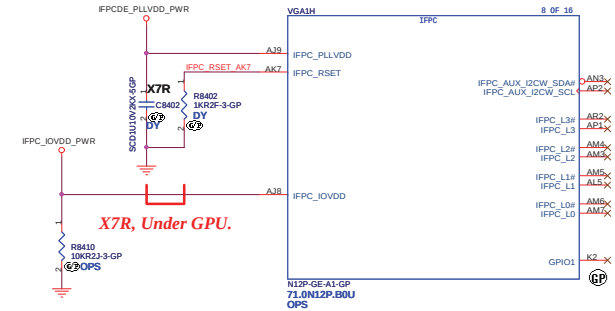




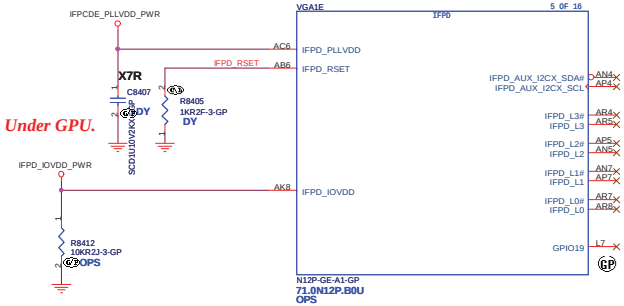


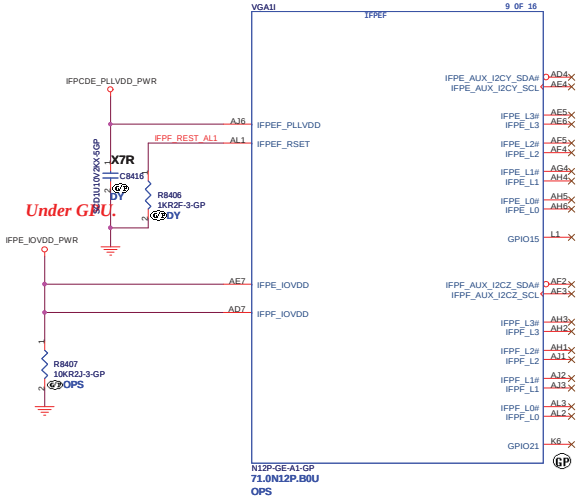






HDMI Interface





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N12P-Q1/Q3 (2/6): DIGITAL OUT***

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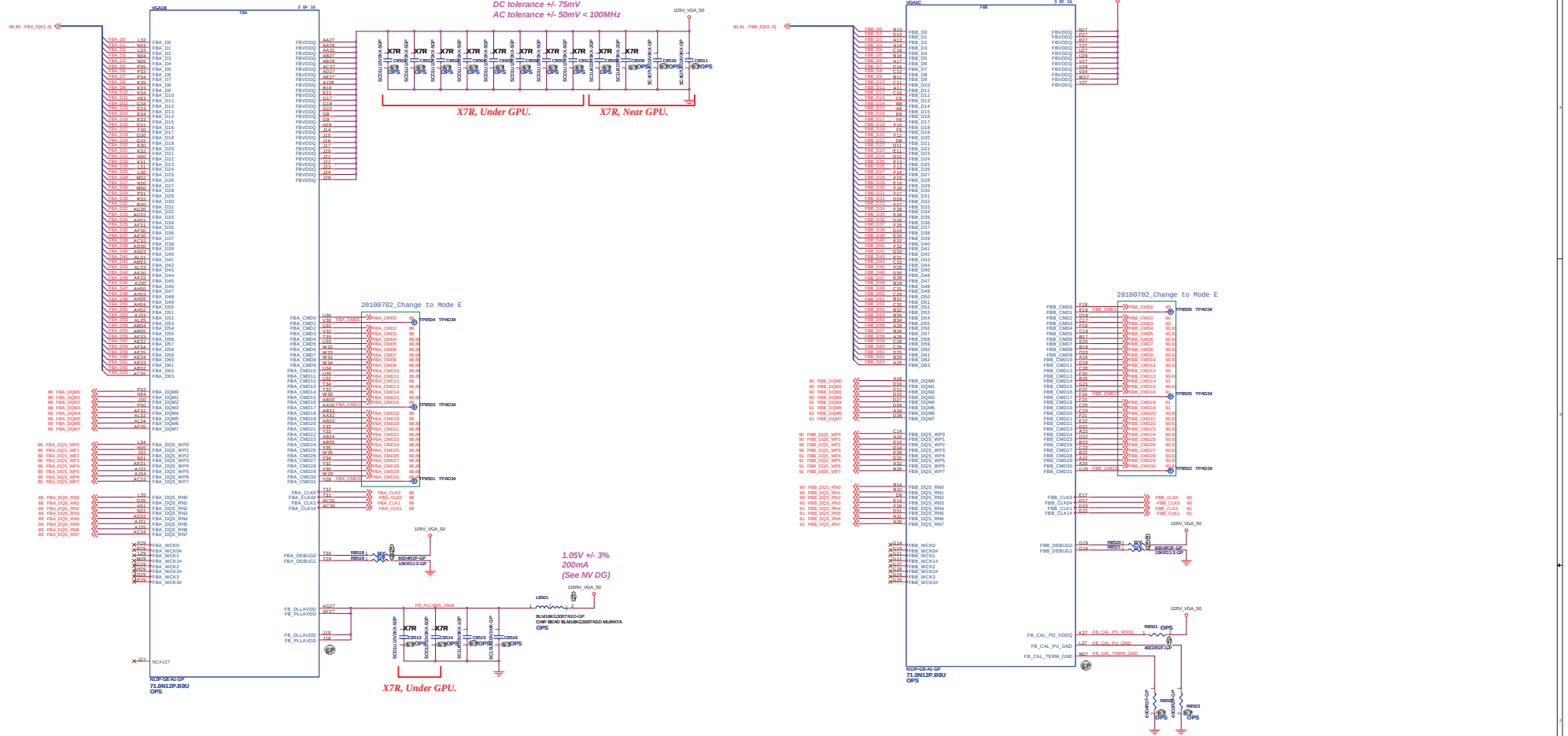
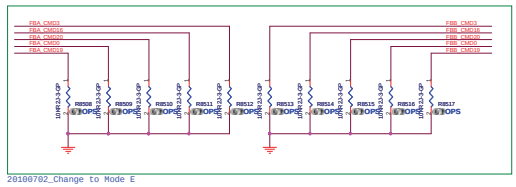
EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz



FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

FBCLK Termination	R8504~R8507
N12P	Sutff 162 ohm 64.16205.GIL
N12M	Sutff 243 ohm 64.24305.GIL

<Core Design>
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *N12P-Q1/Q3 (3/6): VRAM I/F*

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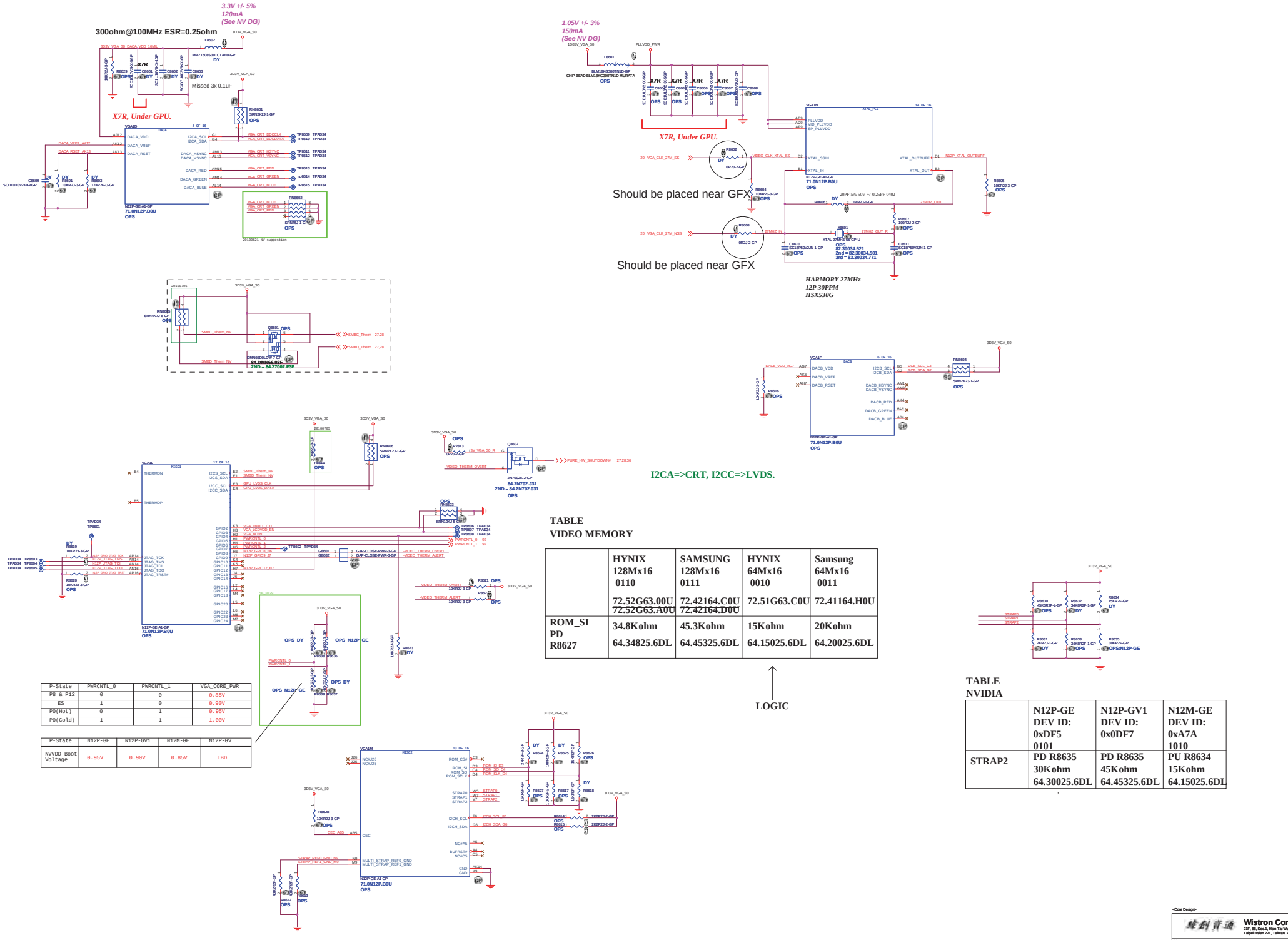

TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
	72.52G63.00U ~~72.52G63.A0U~~	72.42164.C0U ~~72.42164.D0U~~	72.51G63.C0U	72.41164.H0U
ROM_SIPD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

P-State	PWRCNTL_0	PWRCNTL_1	VGA_CORE_PWR
P8 & P12	0	0	0.85V
ES	1	0	0.90V
P0(Hot)	0	1	0.95V
P0(Cold)	1	1	1.00V

P-State	N12P-GE	N12P-GV1	N12M-GE	N12P-GV
NVVDD Boot Voltage	0.95V	0.90V	0.85V	TBD

TABLE
NVIDIA

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV1 DEV ID: 0x0DF7	N12M-GE DEV ID: 0xA7A 1010
STRAP2	PD R8635 30Kohm 64.30025.6DL	PD R8635 45Kohm 64.45325.6DL	PU R8634 15Kohm 64.15025.6DL

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Title: N12P-Q1/Q3 (4/6): GPIO
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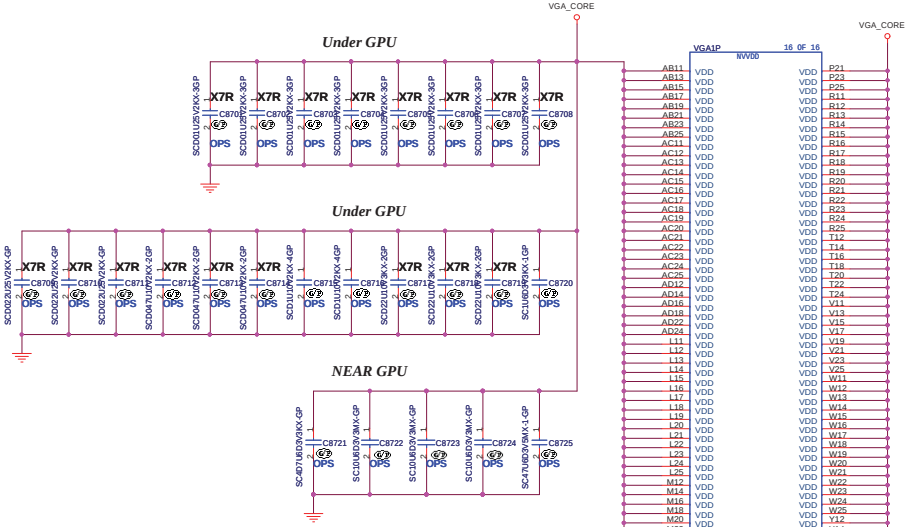

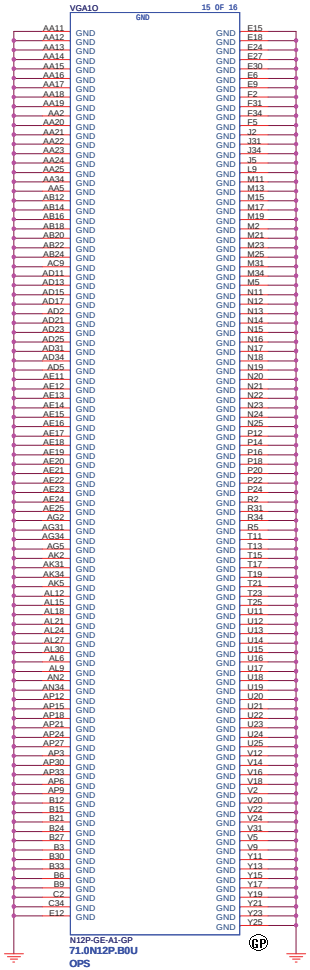

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Taipei Hsien 221, Taiwan, R.O.C.

Title: N12P-Q1/Q3 (5/6): POWER

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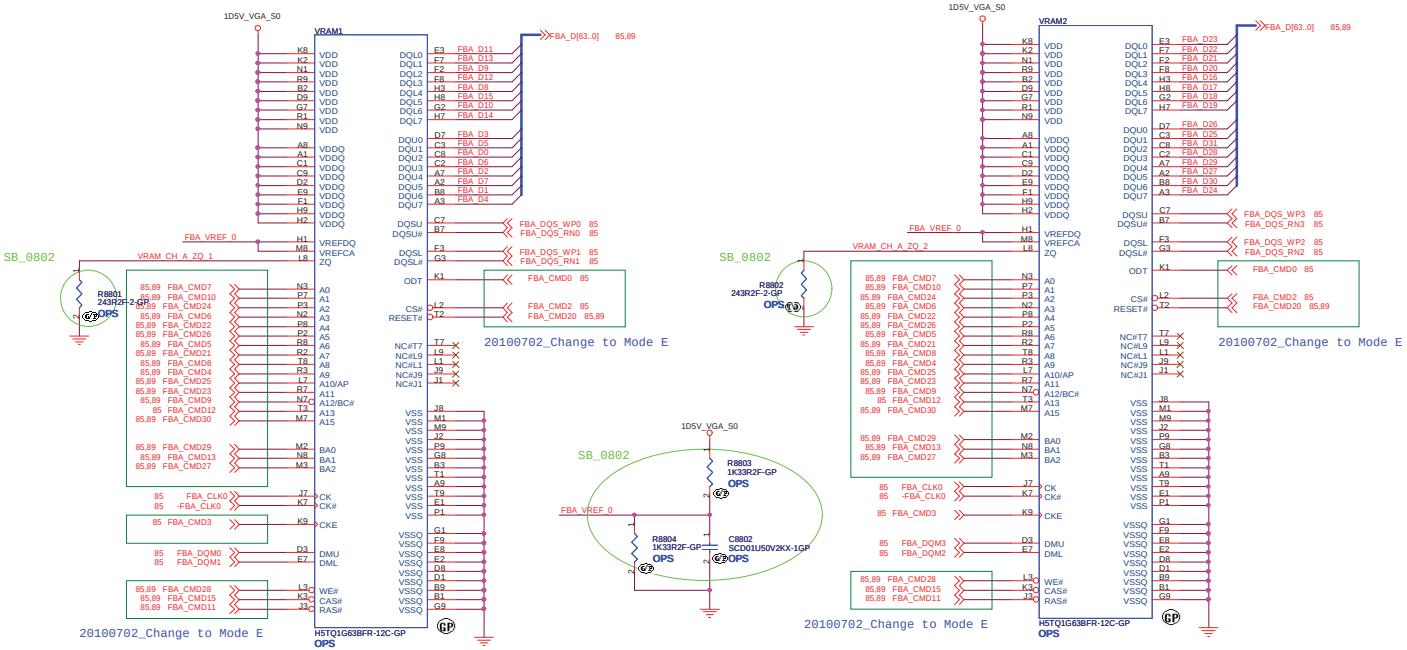
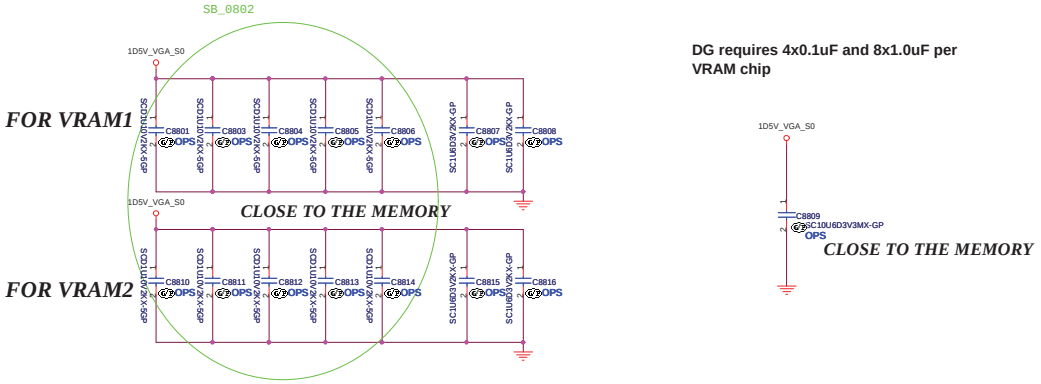


FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip

VIDEO FRAME BUFFER PORT A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-A**

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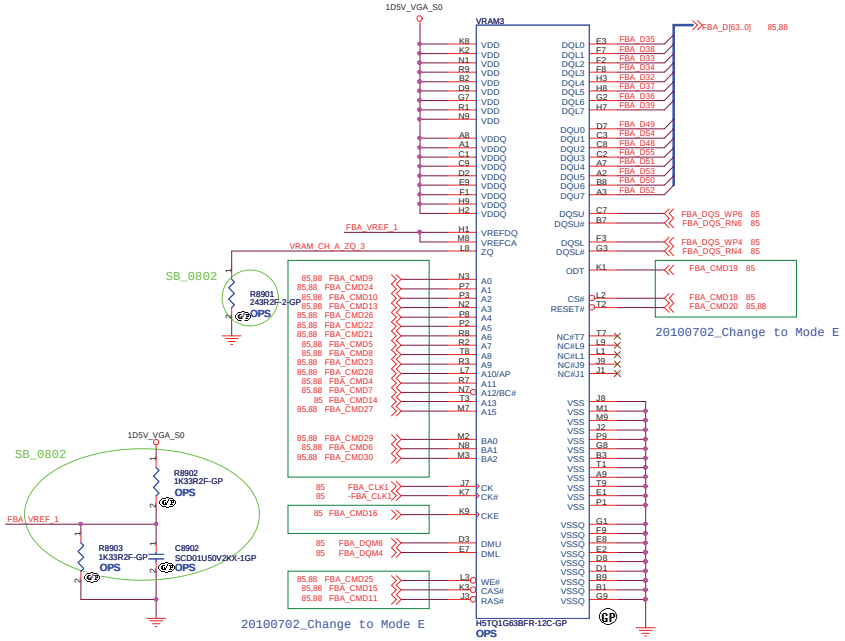
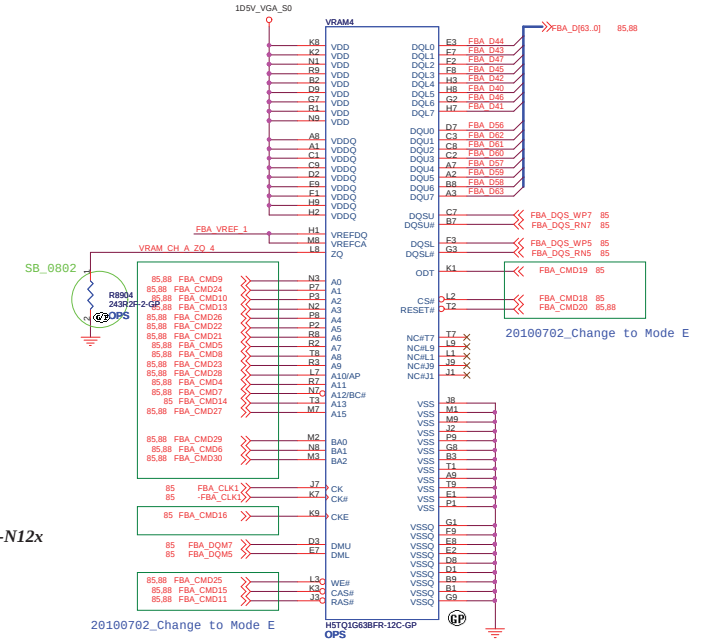
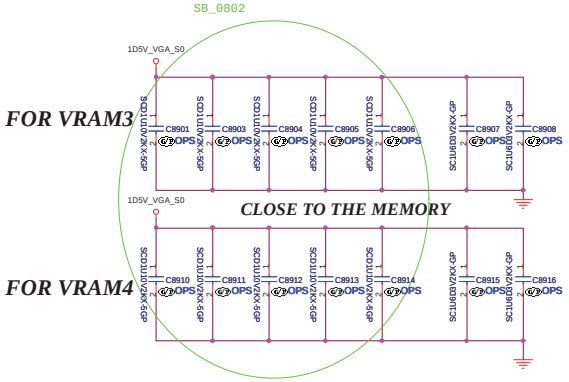




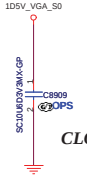
FB CMD mapping Mode D-N12x



FOR VRAM3

CLOSE TO THE MEMORY

FOR VRAM4



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-A

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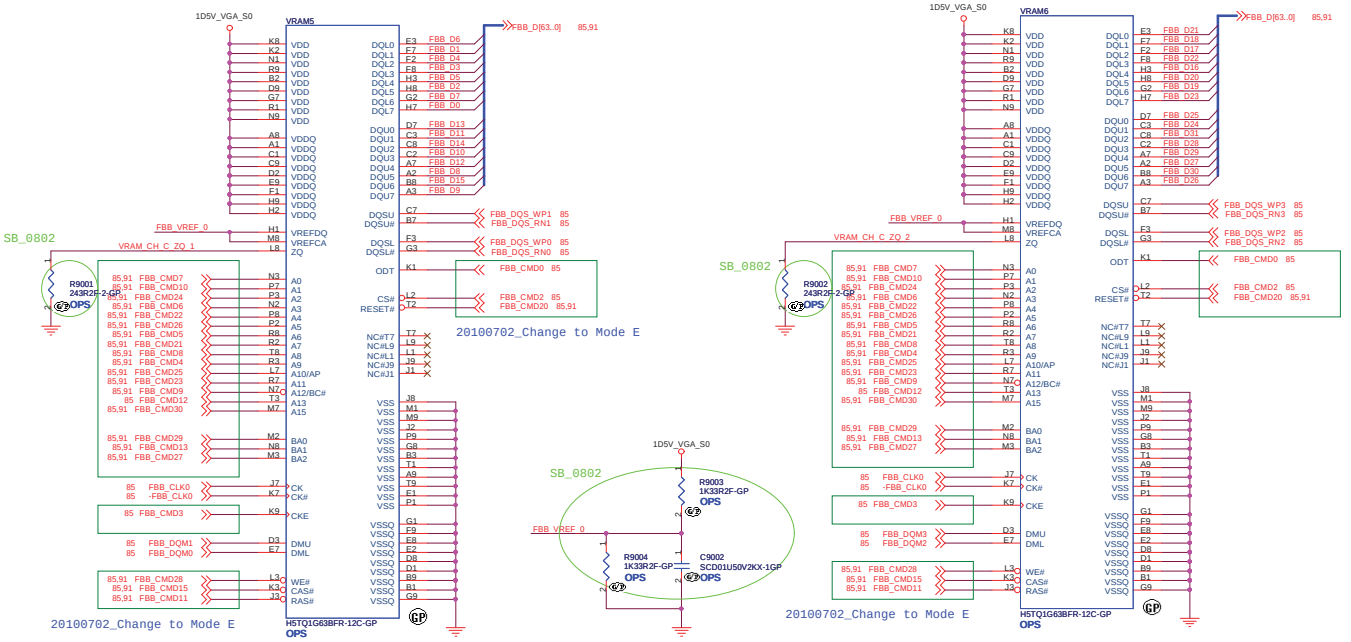
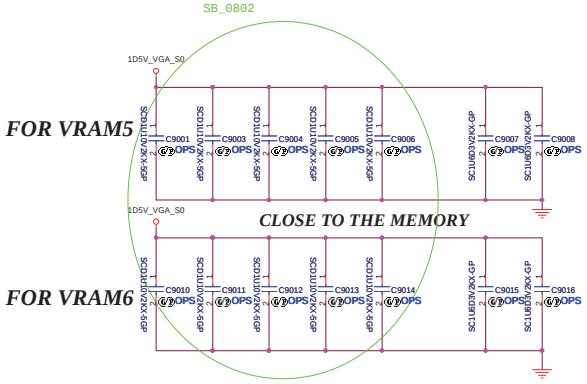
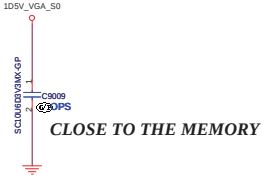




DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM CHANNEL-C***

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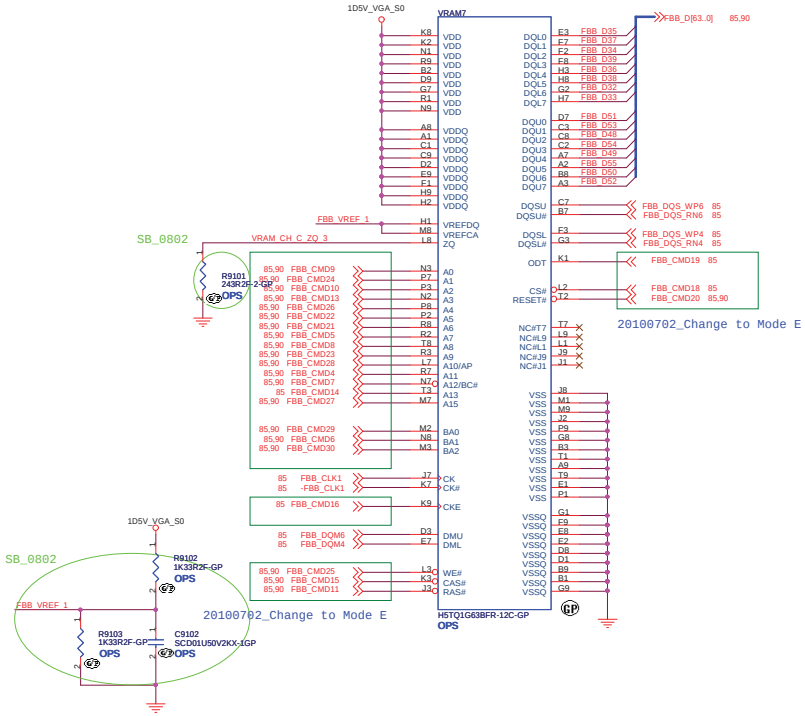

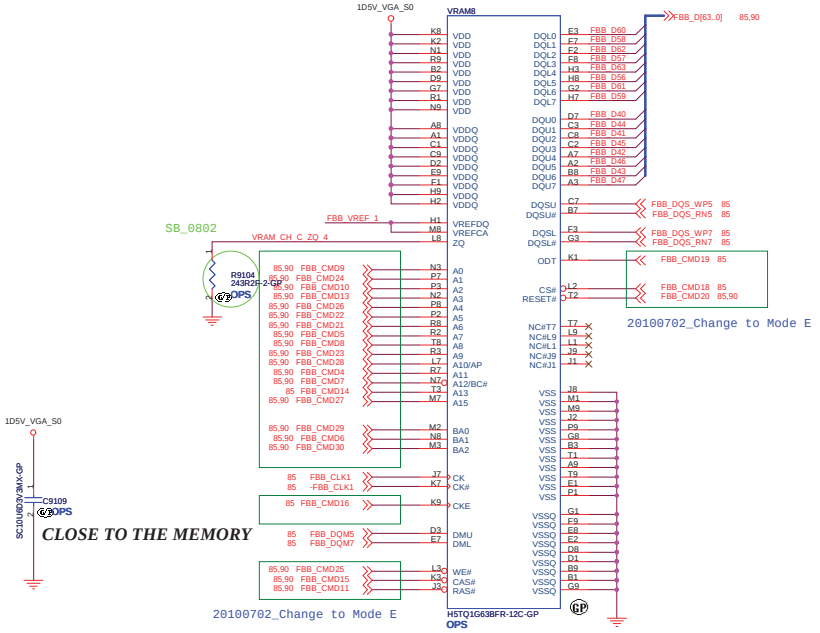

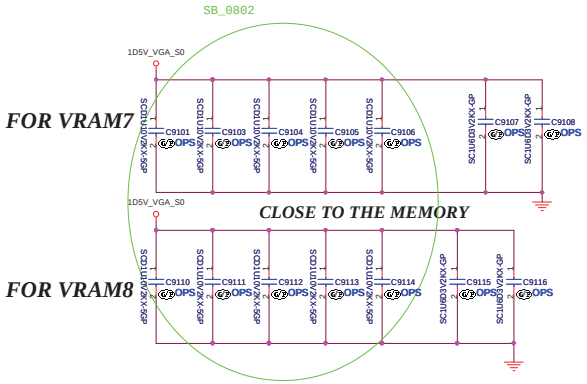

VIDEO FRAME BUFFER PORT C

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM CHANNEL-C**

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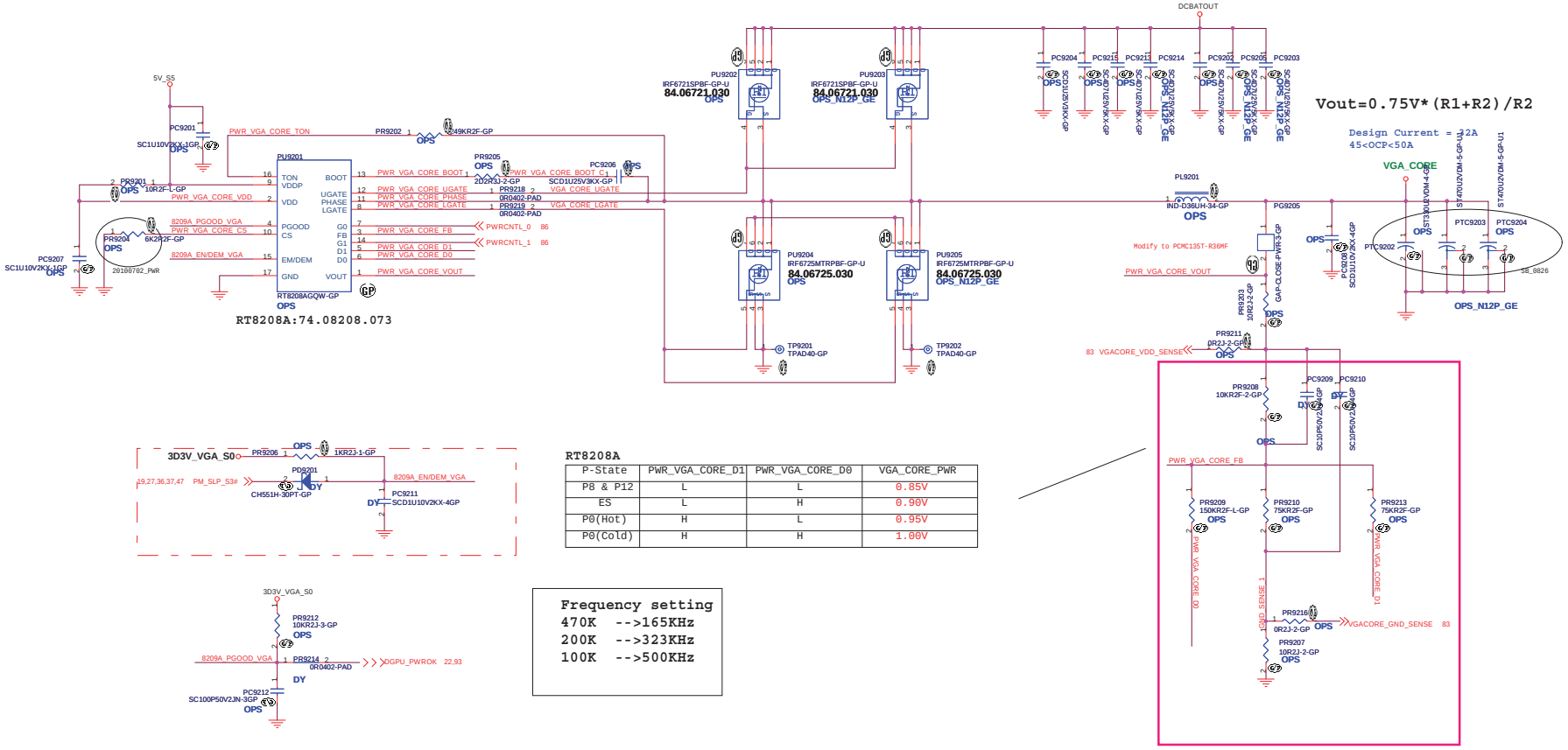
SSID = PWR.Plane.Regulator_GFX



RT8208A

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 & P12	L	L	0.85V
ES	L	H	0.90V
P0(Hot)	H	L	0.95V
P0(Cold)	H	H	1.00V

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

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Title	DC/DC_VGA CORE_RT8208A	
Size	Document Number LA47	Rev SB
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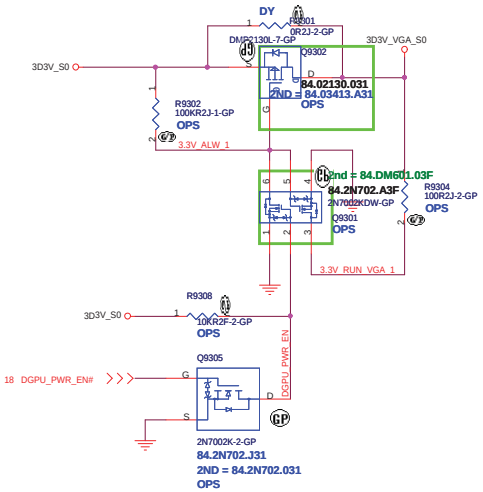
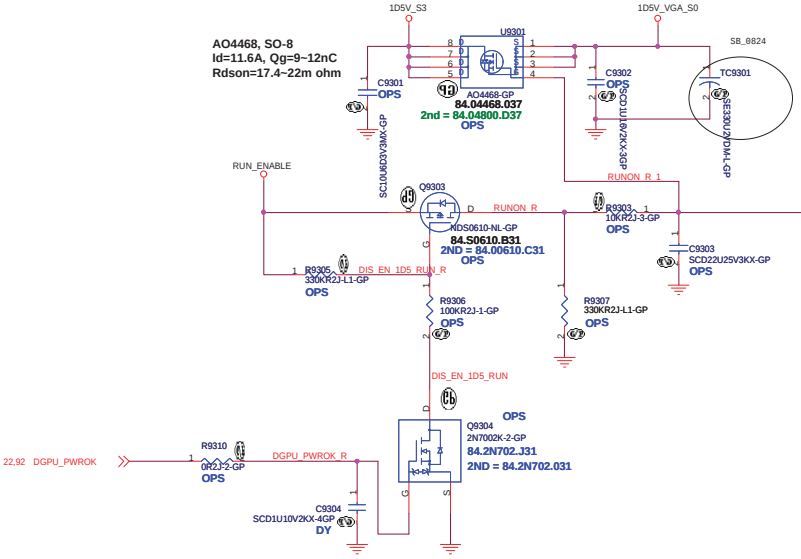
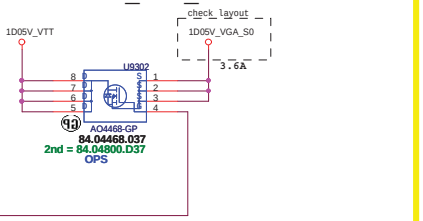
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

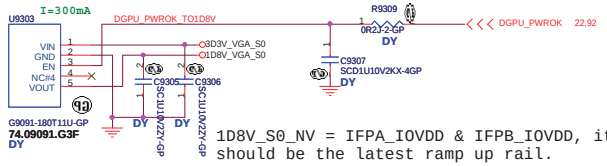


1.05V to 1.05V_VGA_S0 Transfer



20100707

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

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Title: DISCRETE VGA POWER

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Title: *LVDS Switch*

Size	Document Number	Rev
A2	LA470	SB

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Title: CRT_Switch		
Size: A3	Document Number: LA470	Rev: SB
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Title
TOUCH PANEL

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CPU Plate

H1 HOLE276R178-GP — ZZ.00PAD.N11
H2 HOLE276R178-GP — ZZ.00PAD.N11
H3 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H4 STF237R128H42-1-GP — 34.4GD01.001
H5 STF237R128H42-1-GP — 34.4GD01.001

Structure boss

H7 HOLE315X315R91-S1-GP	H8 HOLE315X315R91-S1-GP	H9 HOLE315X315R91-S1-GP	H10 HOLE315X315R91-S1-GP	H11 HOLE315X315R91-S1-GP	H12 HOLE256R115-GP	H13 HOLE256R115-GP	H15 HOLE256R115-GP
ZZ.00PAD.581	ZZ.00PAD.581	ZZ.00PAD.581	ZZ.00PAD.581	ZZ.00PAD.581	ZZ.00PAD.D11	ZZ.00PAD.D11	ZZ.00PAD.D11

MiniPCI Std-Off

H14 STF237R113H115-GP — 34.4V802.101

Check test point

5,11,18,27,31,36,65,66,71,83 PLT_RST#

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
11,19,27 PM_PWRBTN#	AFTP10
5,11,22,36 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12
	AFTP13

Test Point放在Dimm Door打開可量測處

AD+

EC9702 DY SCD1U25V2KX-GP
EC9703 DY SCD1U25V2KX-GP
EC9704 DY SCD1U25V2KX-GP

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Title: UNUSED PARTS/EMI Capacitors

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Title: ***Change History***

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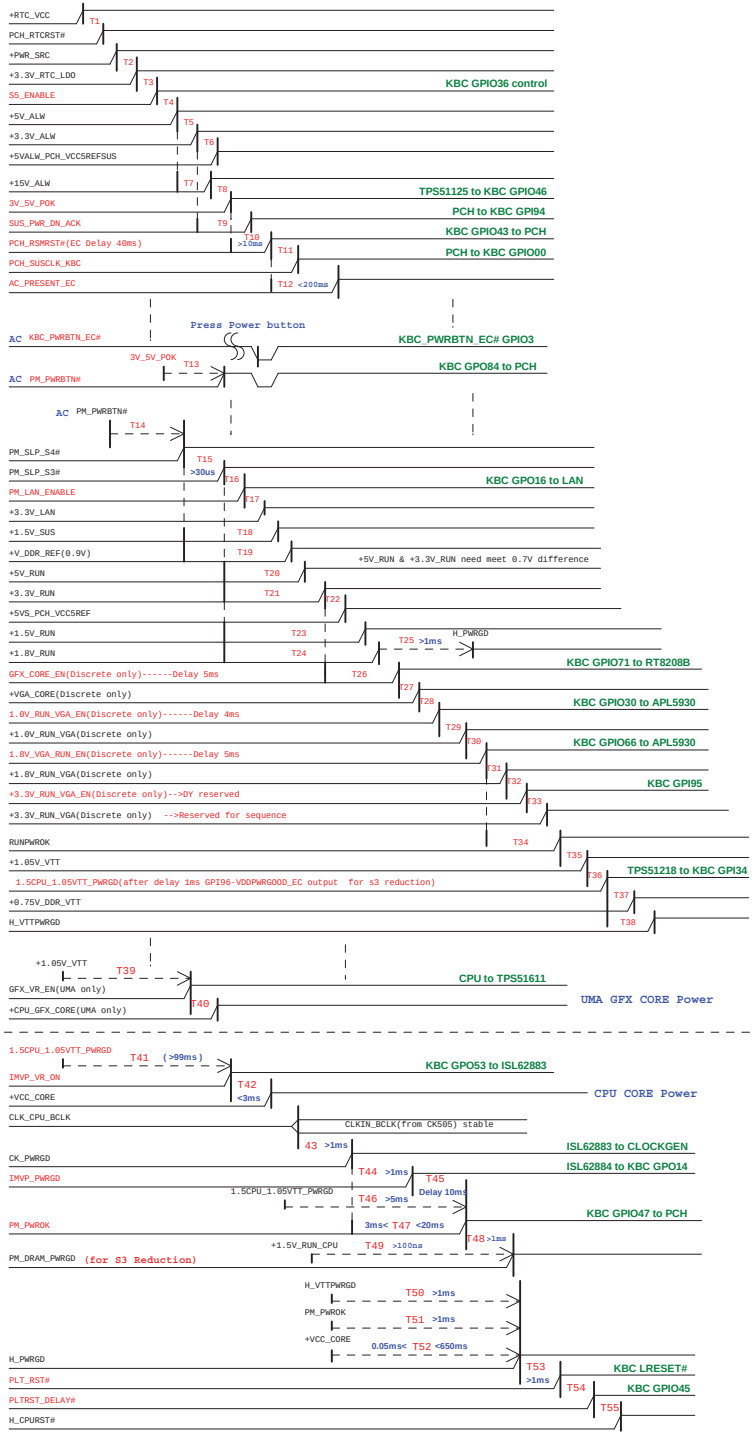
Intel-Power Up Sequence

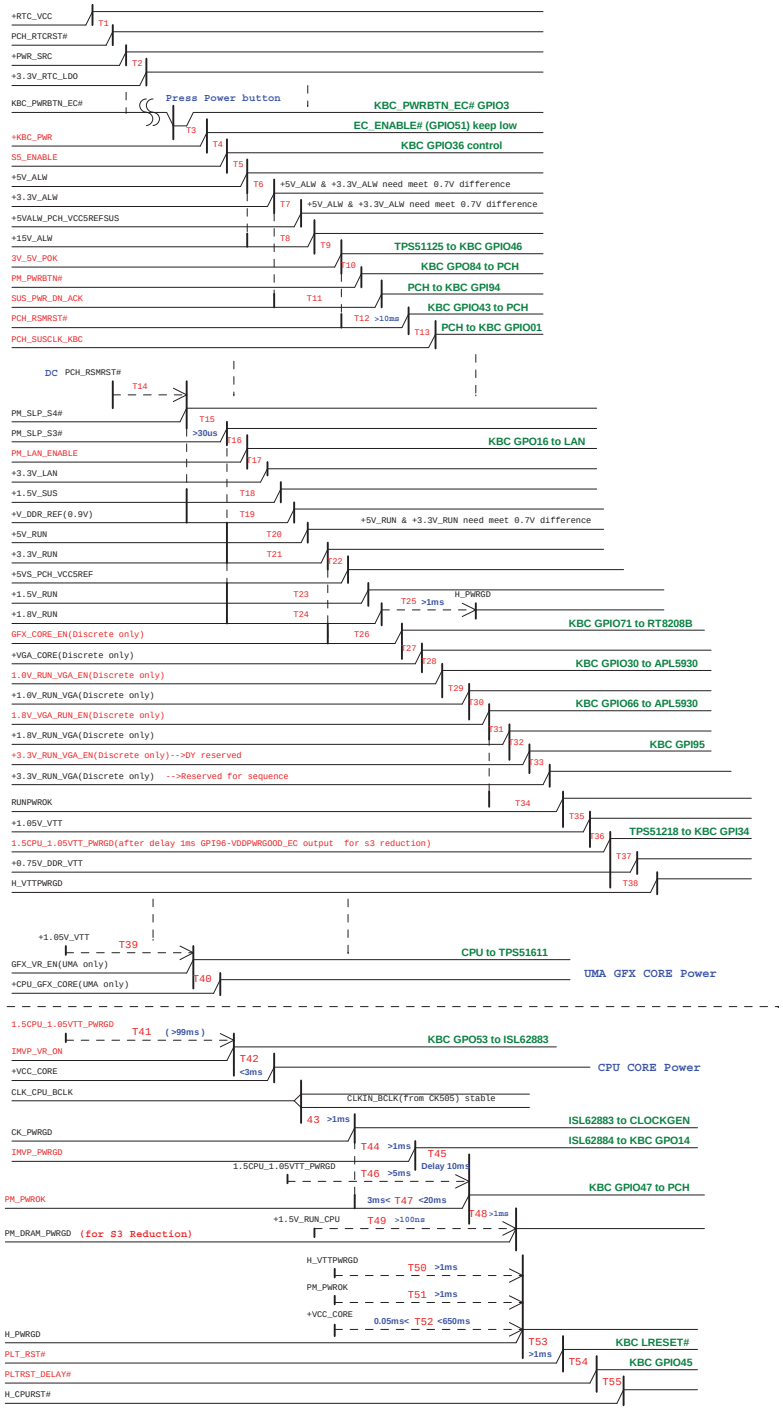
(AC mode)

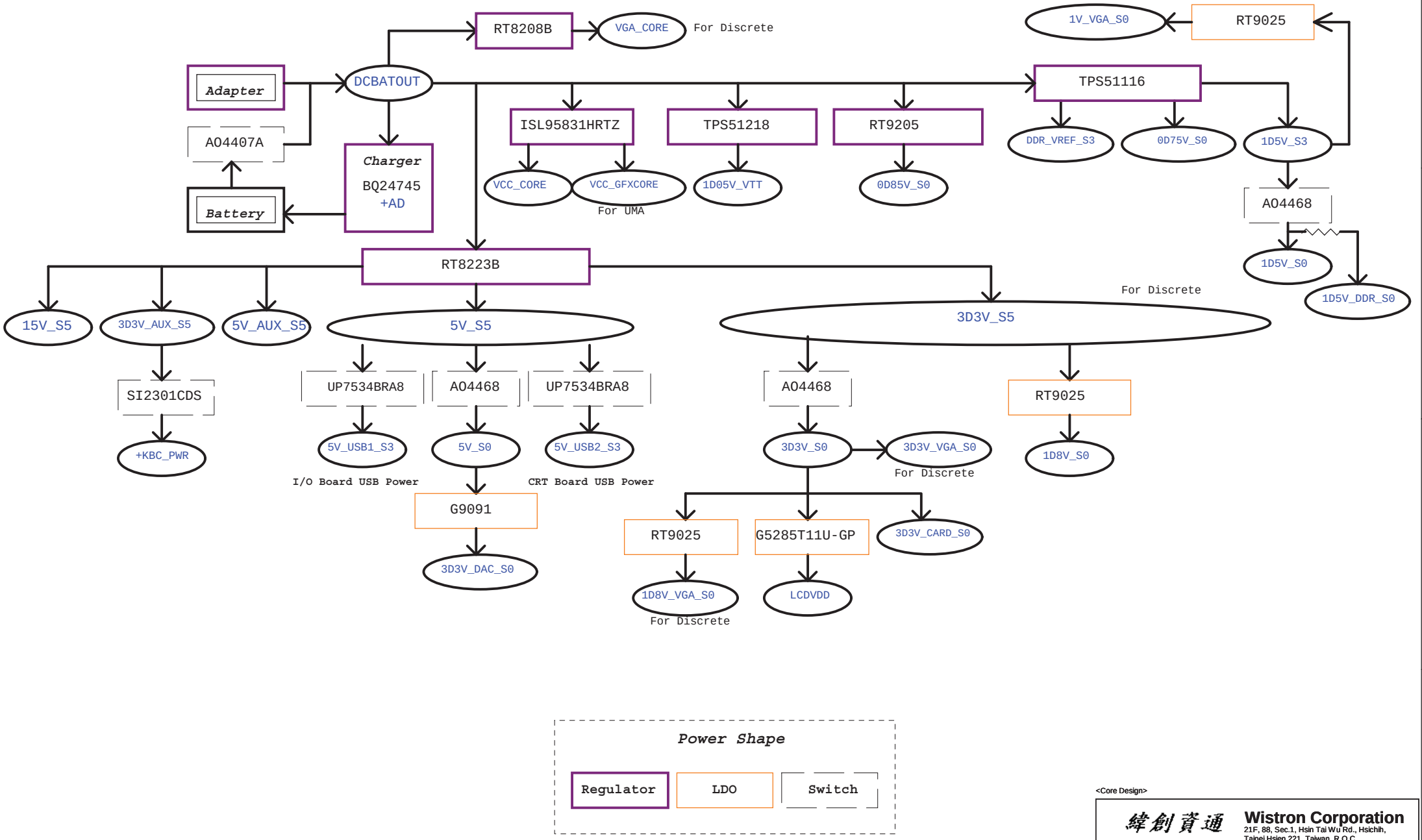
red word: KBC GPIO



(DC mode)

red word: KBC GPIO





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Title: **Power Block Diagram**

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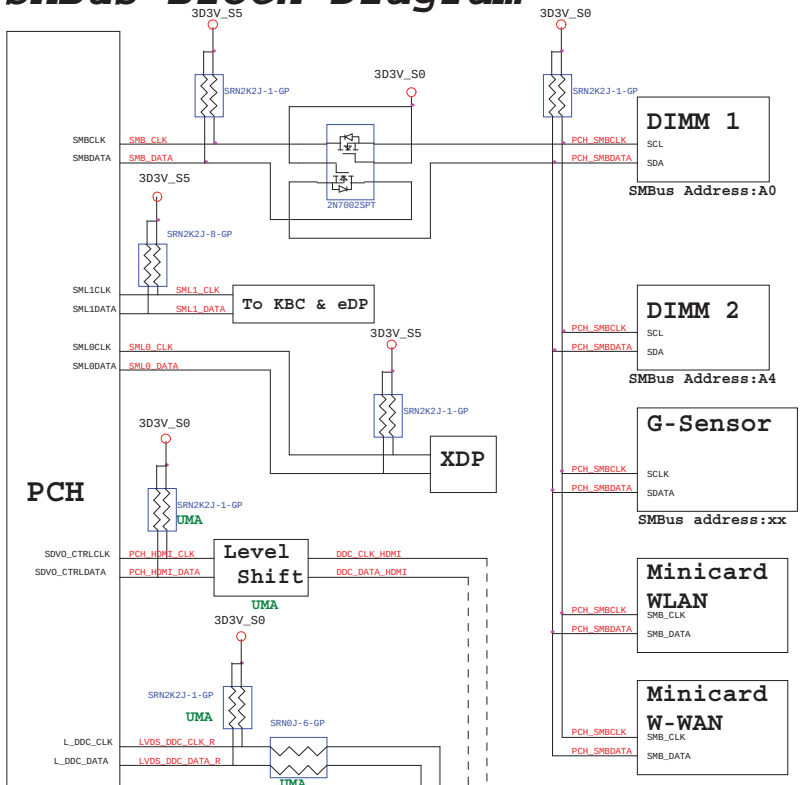
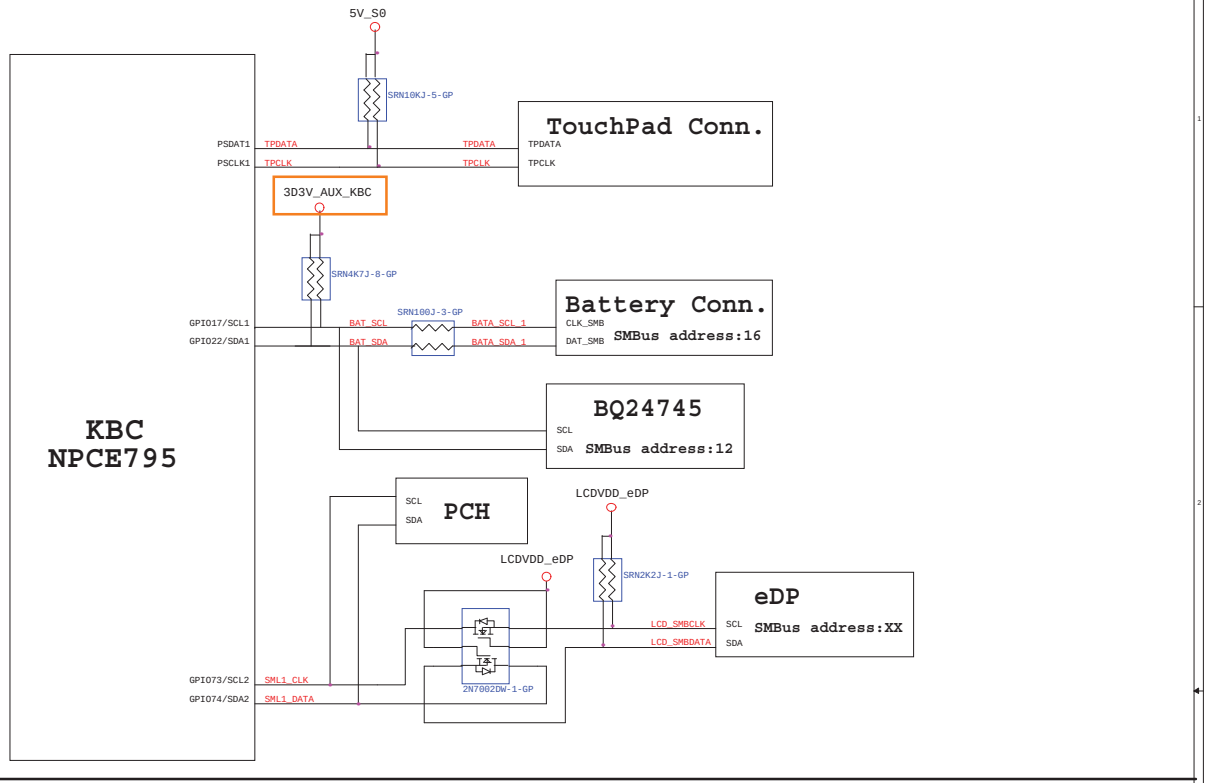
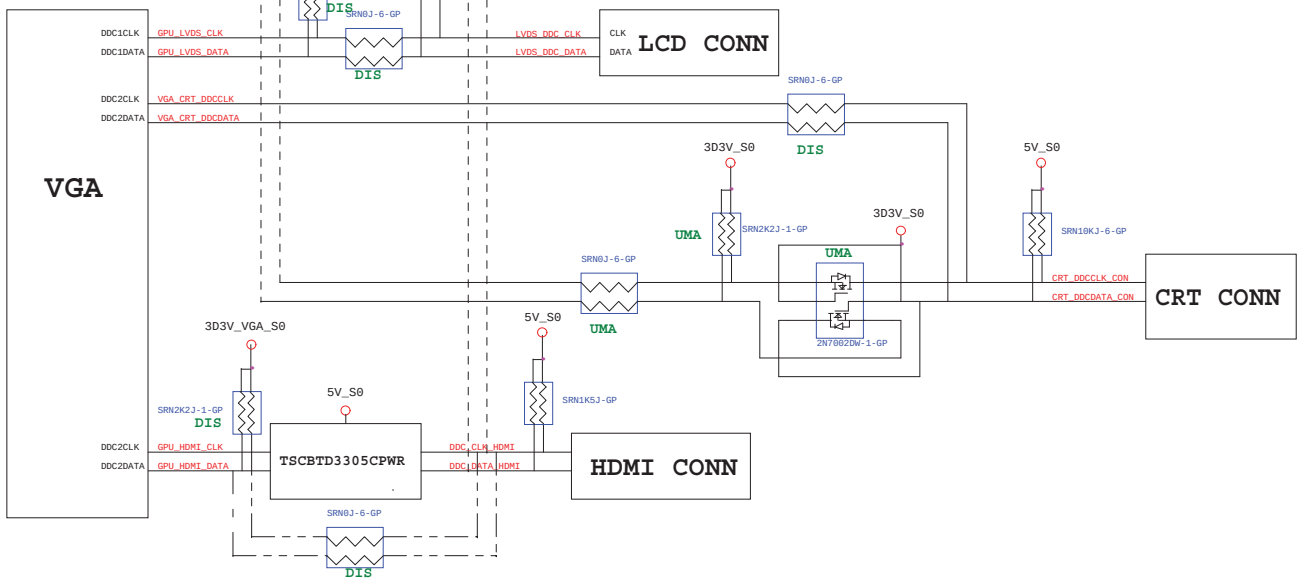
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram

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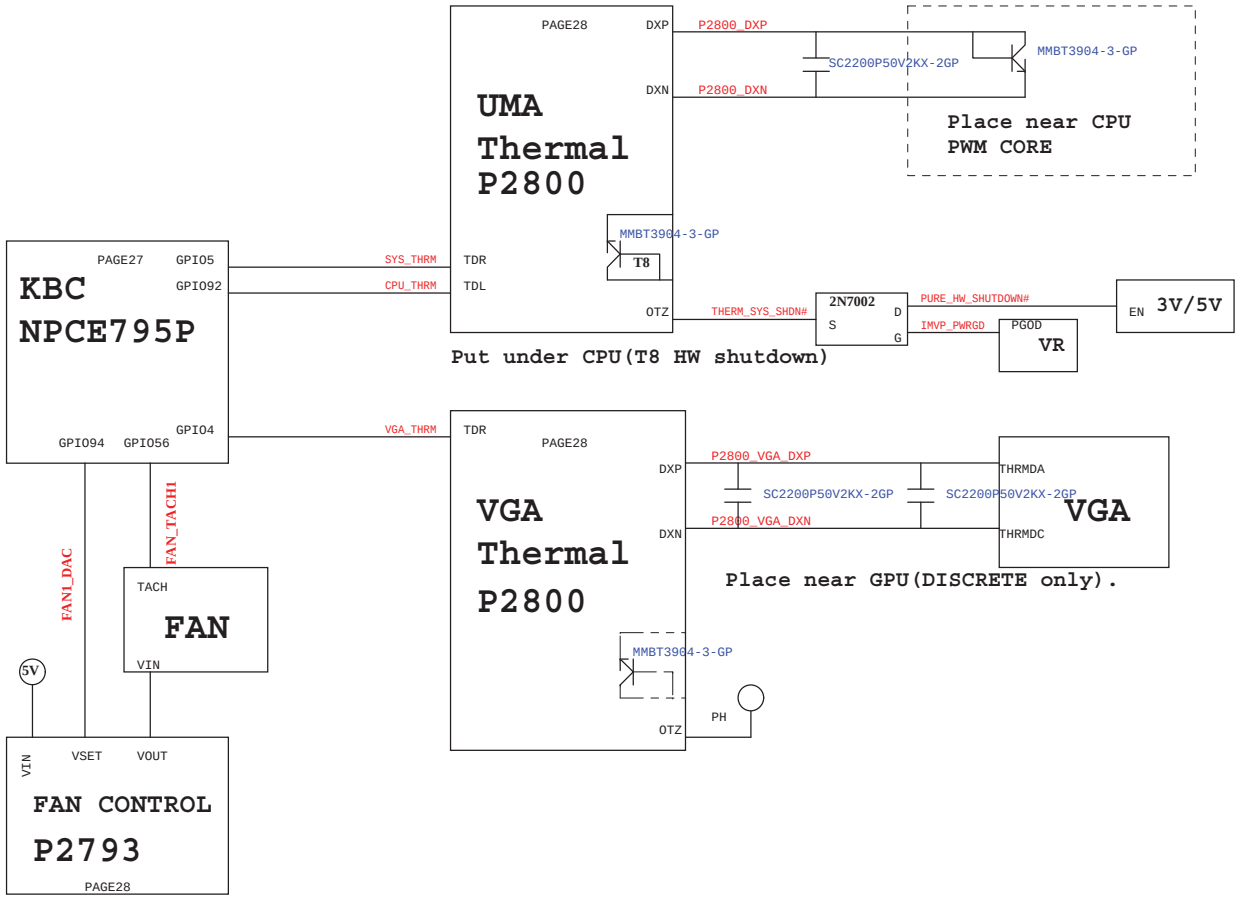
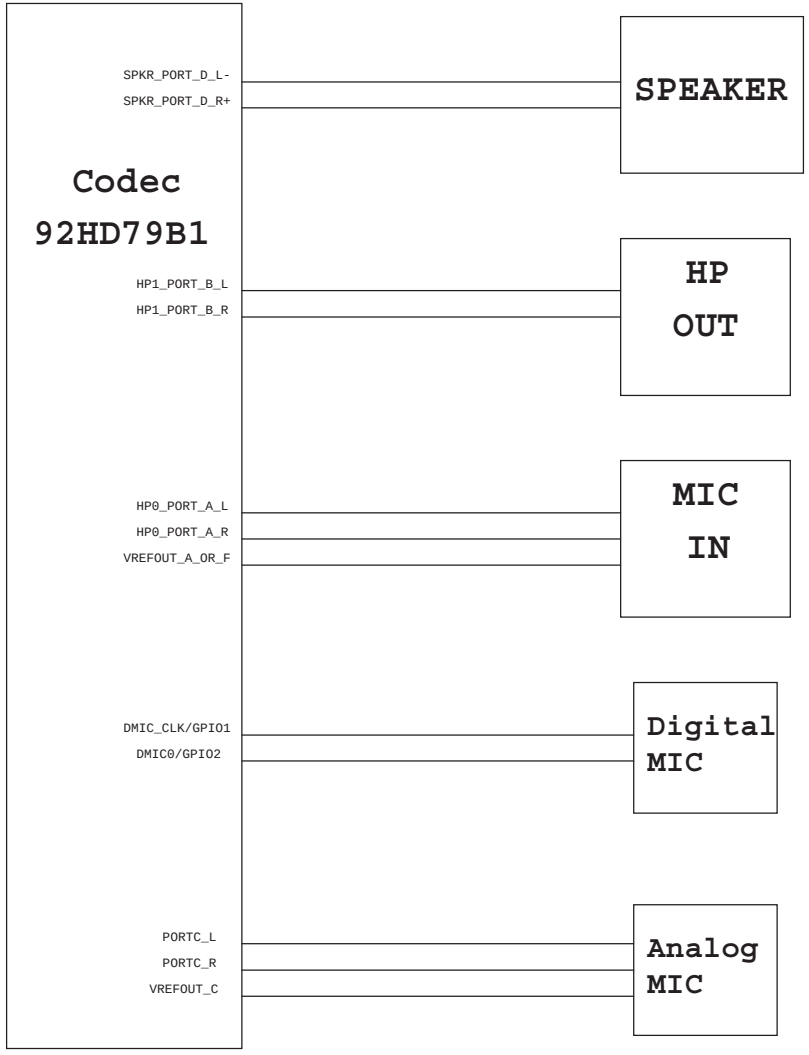
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title: *Change History*

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