

ZZZ1

PCB

DAZ@

ZZZ2

PCB

DAZ@

ZZZ3

SW

DAZ@

ZZZ4

USB

DAZ@

ZZZ5

AUDIO

DAZ@

SE000008600

Compal Confidential

Tanglha Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

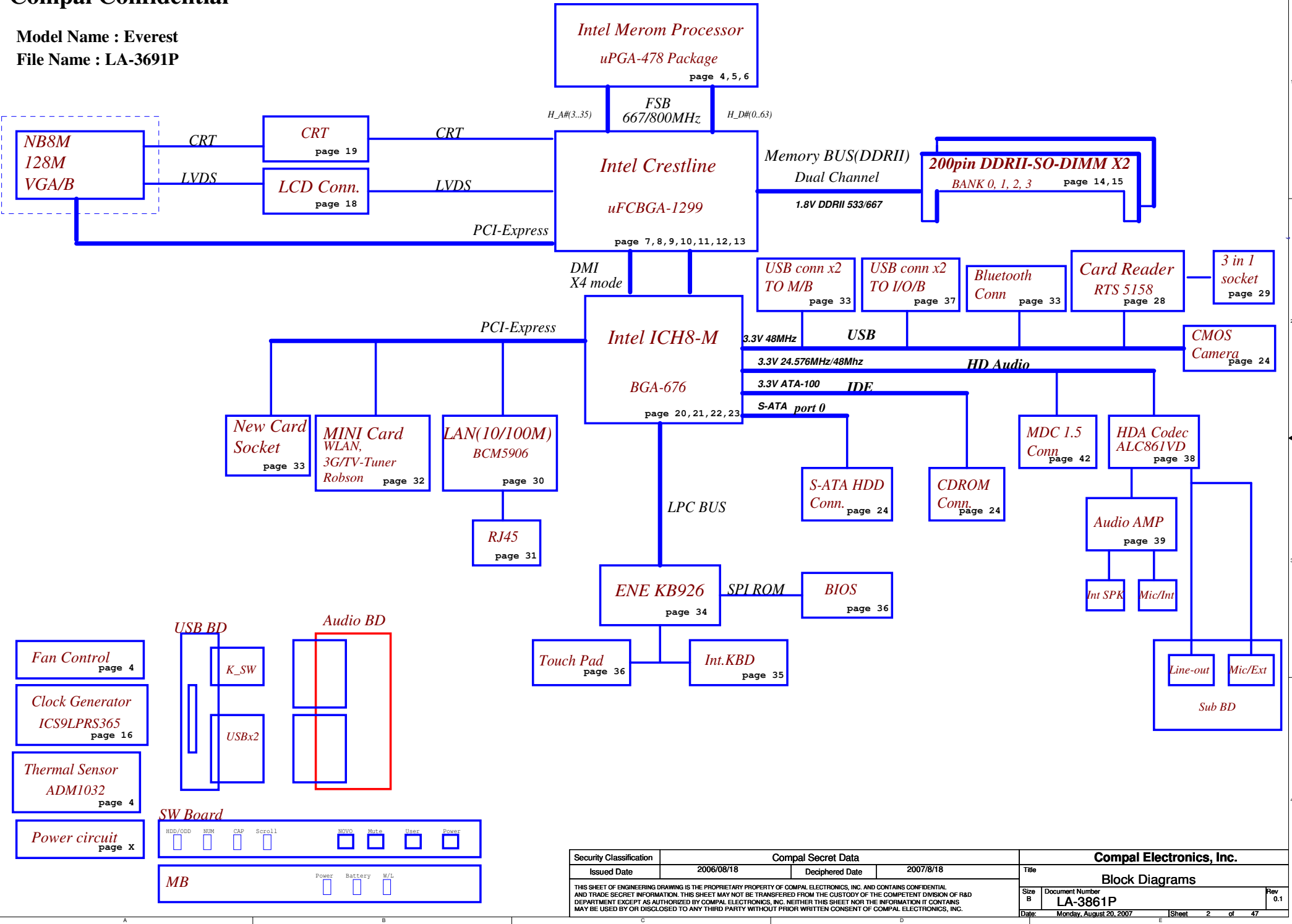
2007-08-16

REV: 1.0

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Compal Confidential

Model Name : Everest
File Name : LA-3691P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0 (R744)	0 (R745)	A-TEST
0 (R744)	1 (R742)	B-TEST
1 (R741)	0 (R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

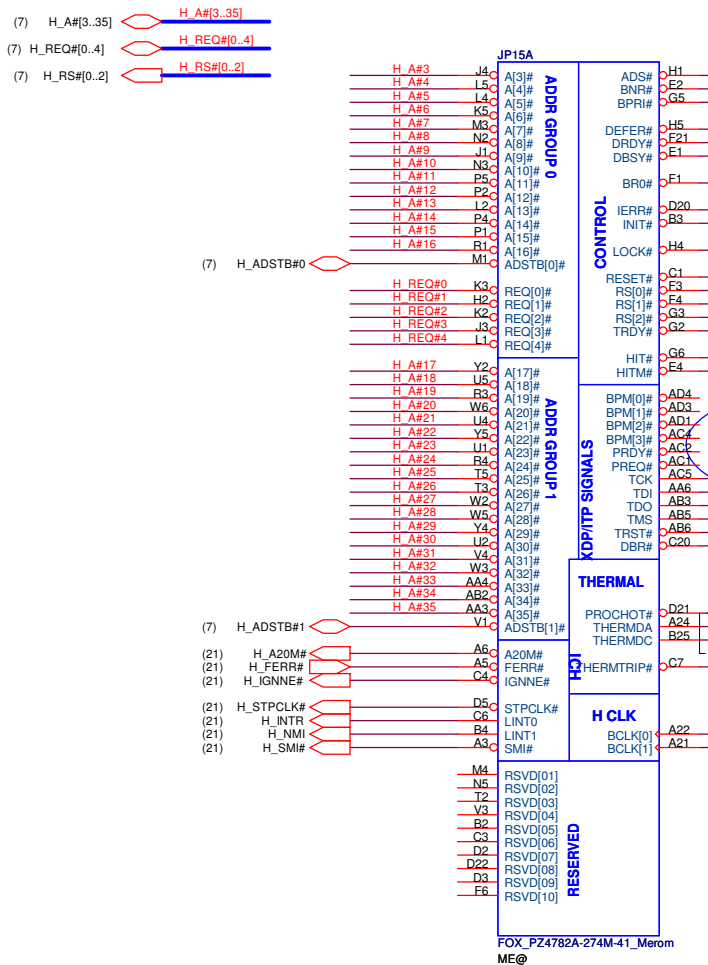
Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

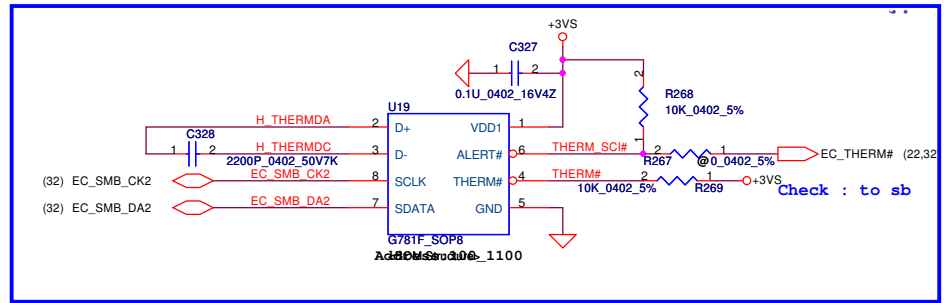
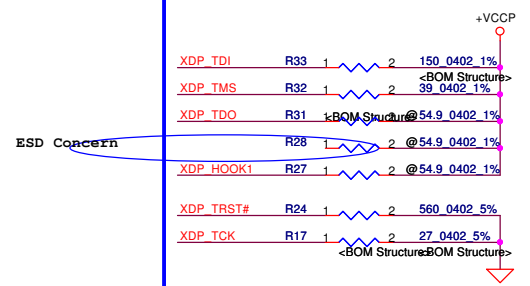
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb



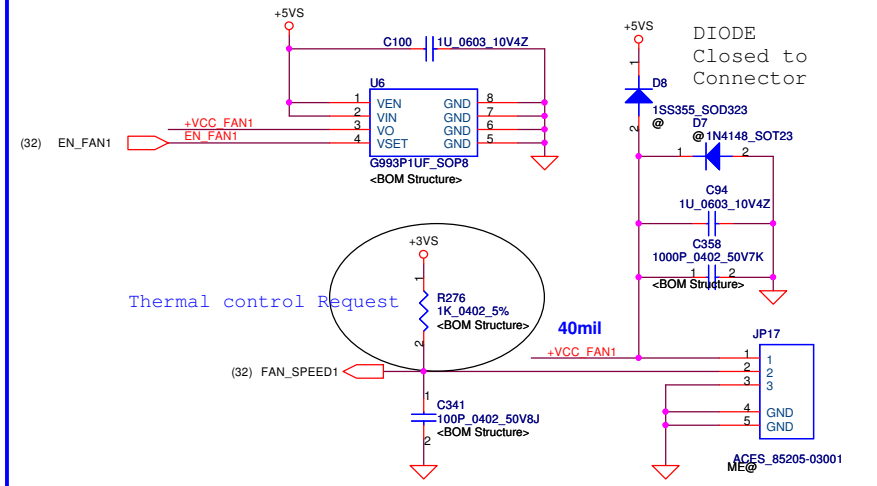
**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

Place close to CPU within 500mil

XDP Reserve

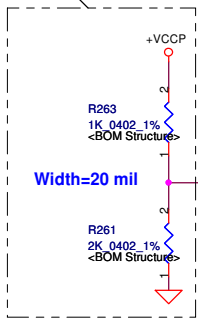


FAN1 Conn



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Close to CPU pin AD26
within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within
0.5" of CPU pin. Trace
should be at least 25
mils away from any other
toggling signal.
COMP[0,2] trace width is
18 mils. COMP[1,3] trace
width is 4 mils.

Length match within 25 mils.
The trace width/space/other is
20/7/25.

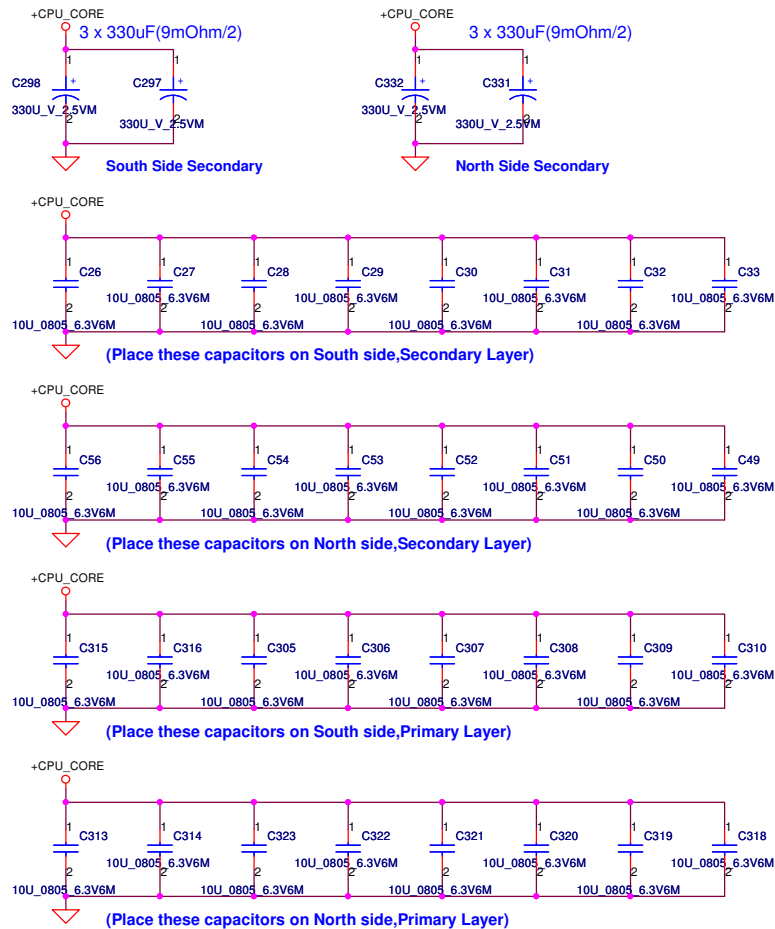
Close to CPU pin
within 500mils.

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JP15D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	A2
M22	VSS[075]	VSS[156]	AF6
M25	VSS[076]	VSS[157]	AF8
N1	VSS[077]	VSS[158]	AF11
N4	VSS[078]	VSS[159]	AF13
N23	VSS[079]	VSS[160]	AF16
N26	VSS[080]	VSS[161]	AF19
P3	VSS[081]	VSS[162]	AF21
		VSS[163]	A25
			AF25

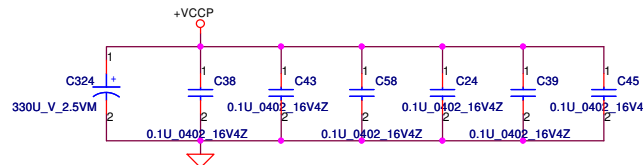
FOX_PZ4782A-274M-41 Merom

ME@

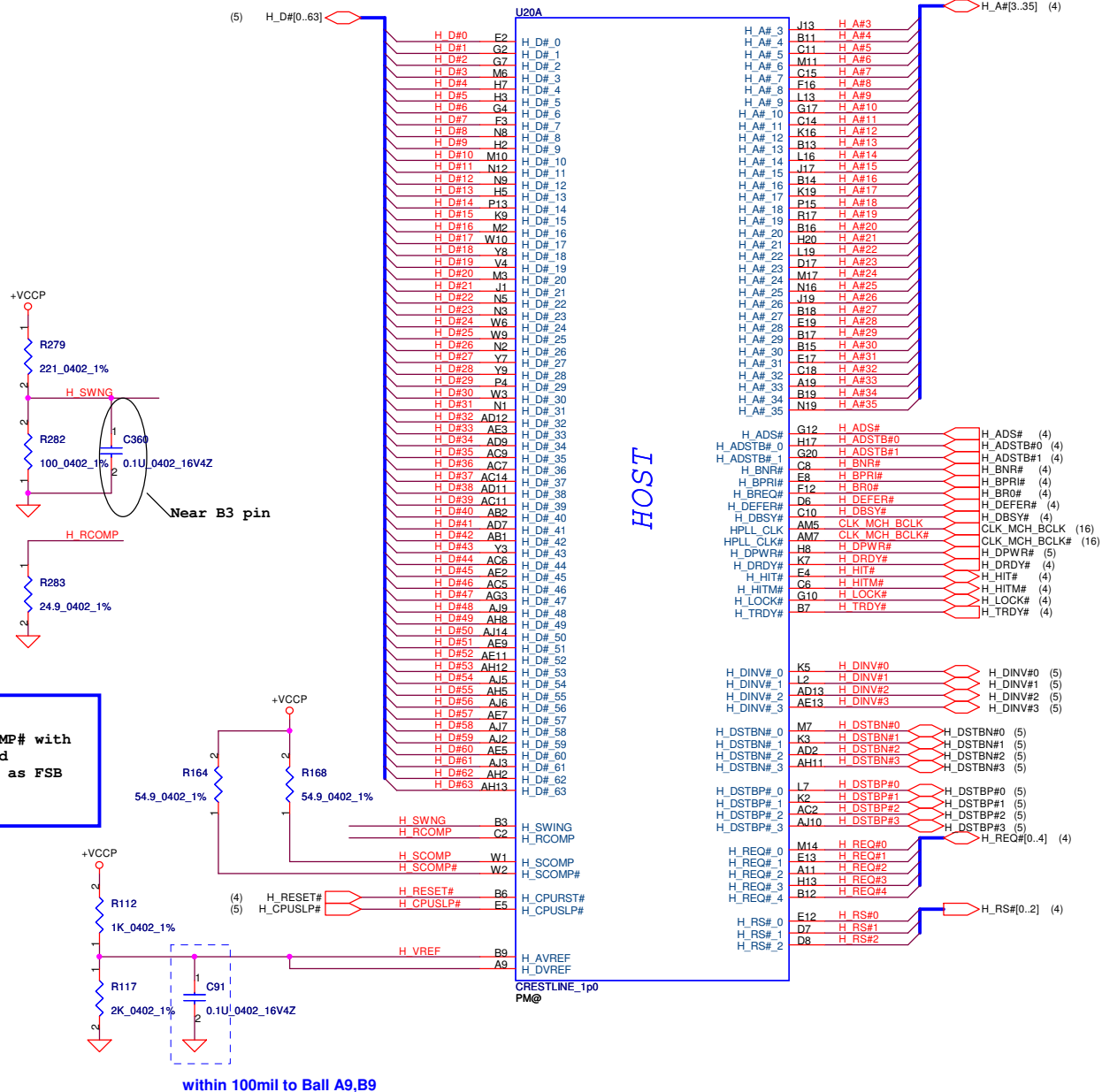


9/25 10U checked. OK for use!

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



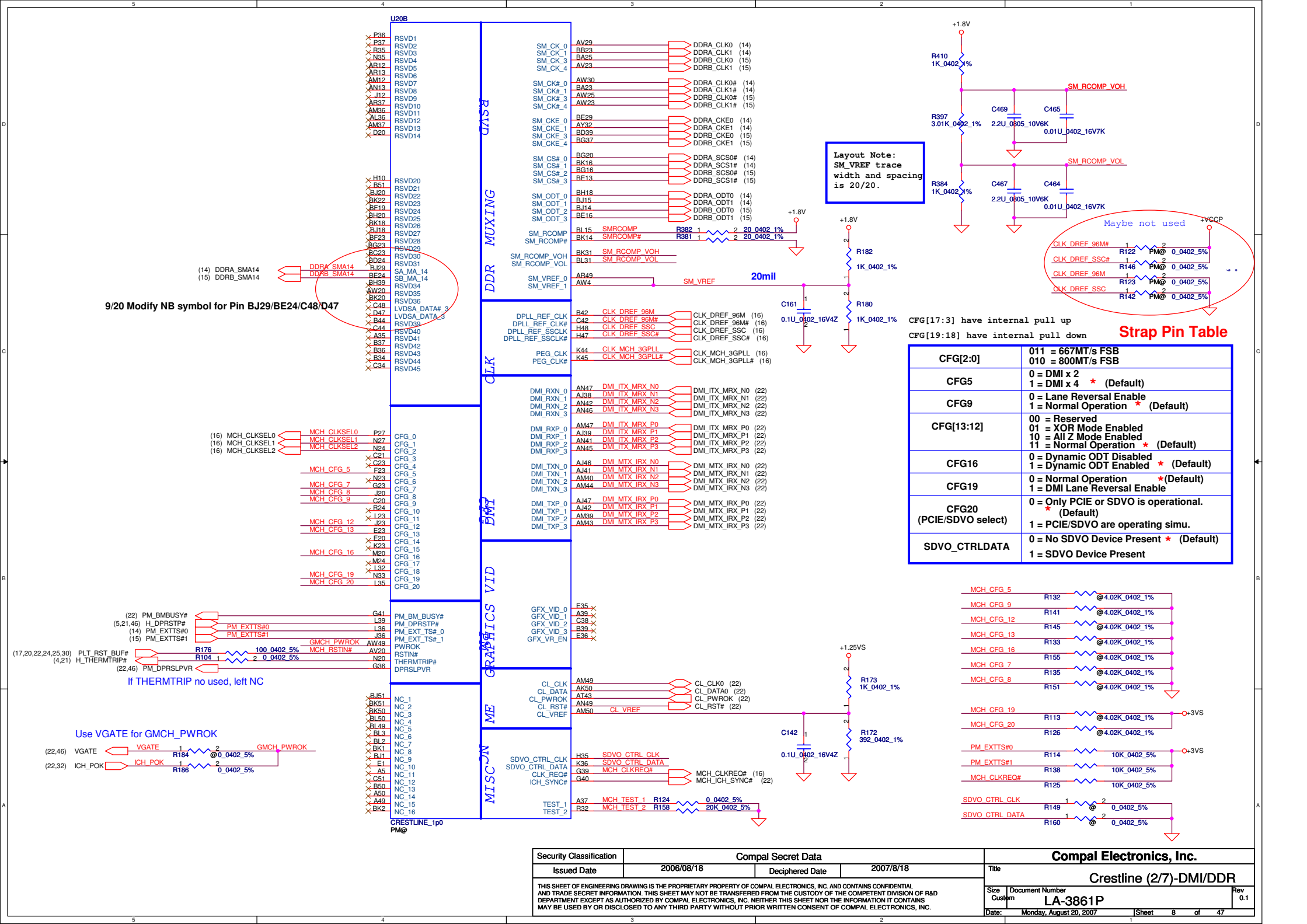
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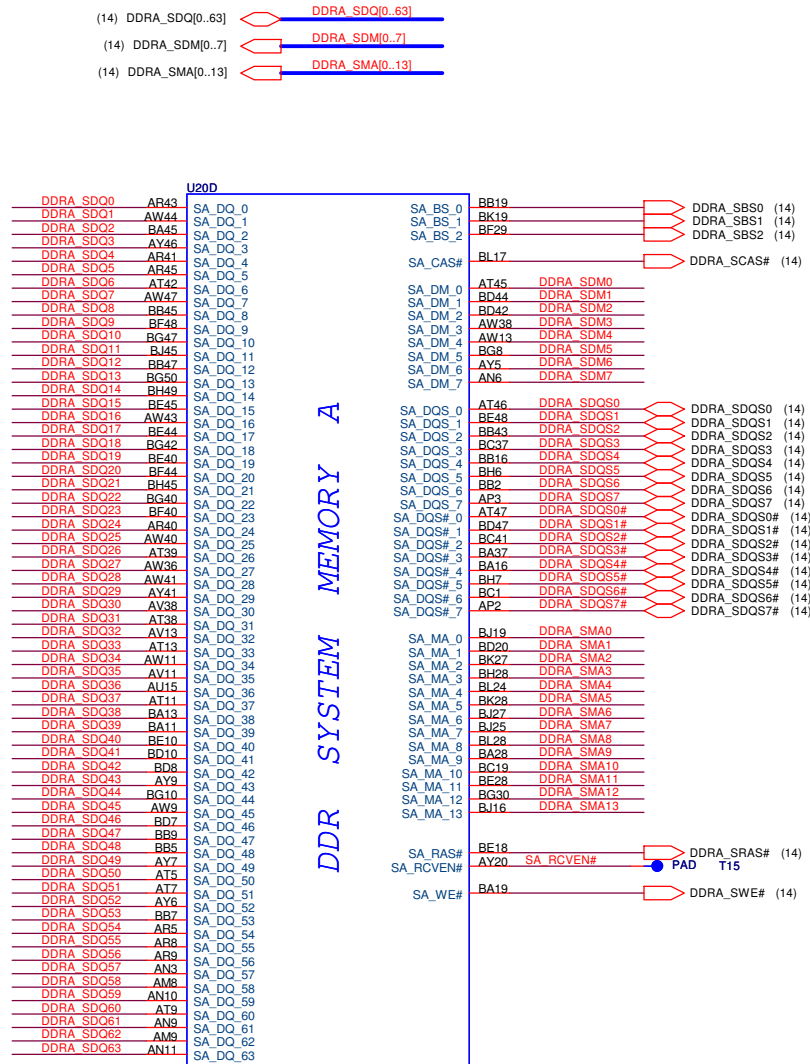


layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

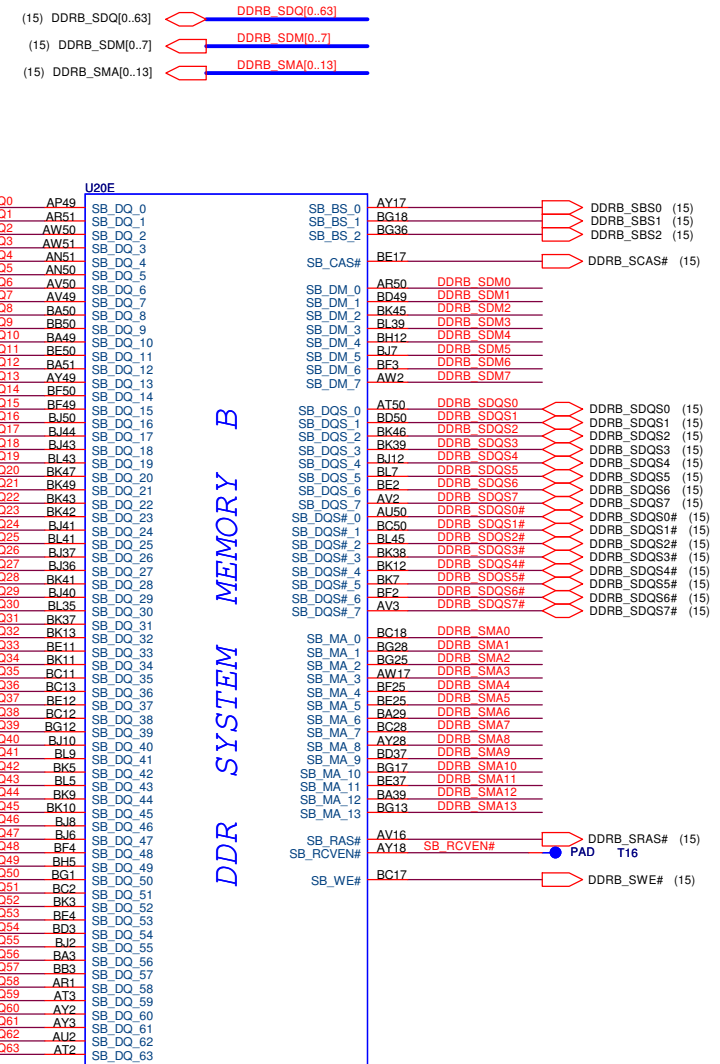
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

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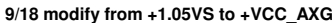


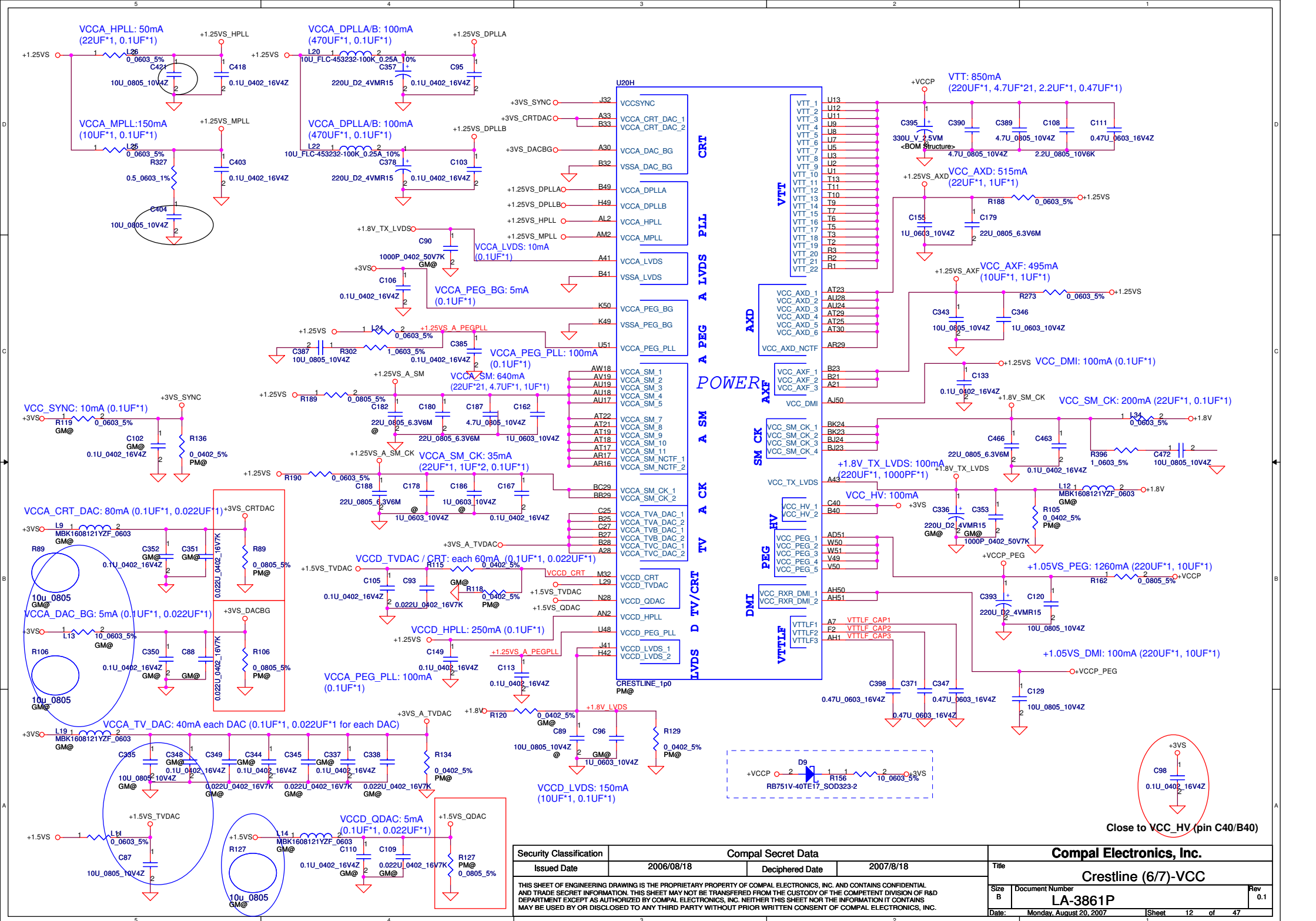


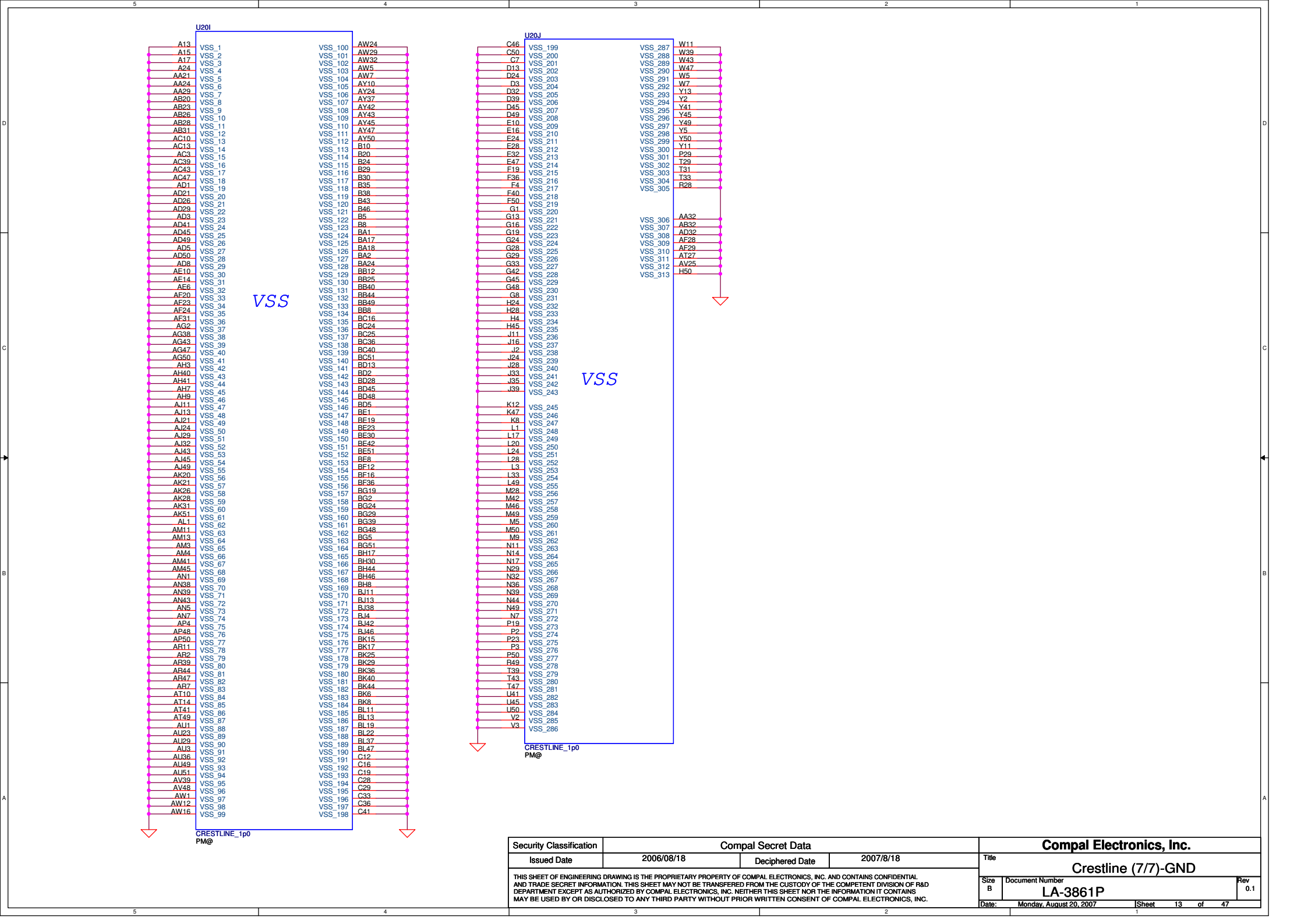
CRESTLINE_1p0
PM@



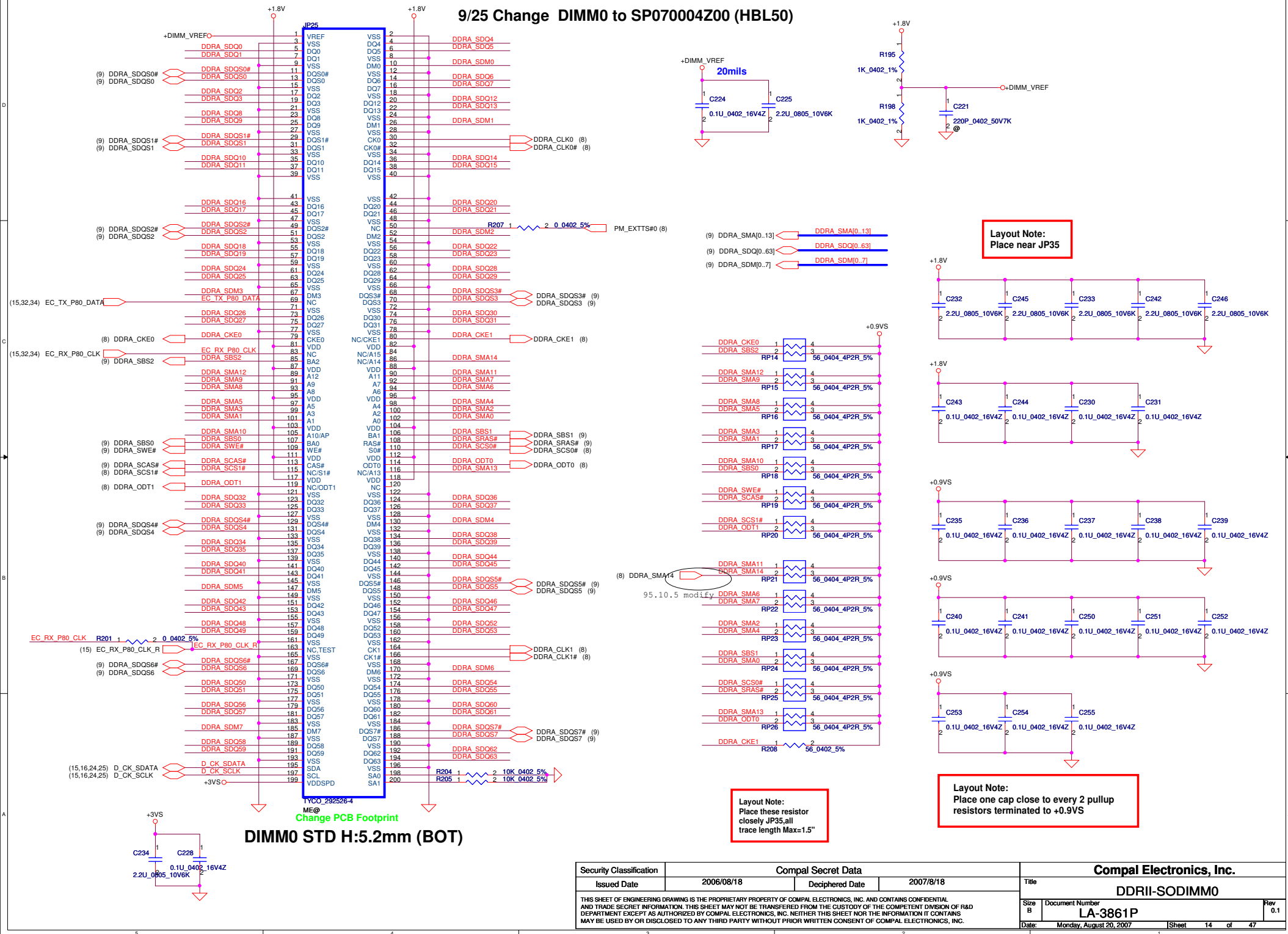
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PM@



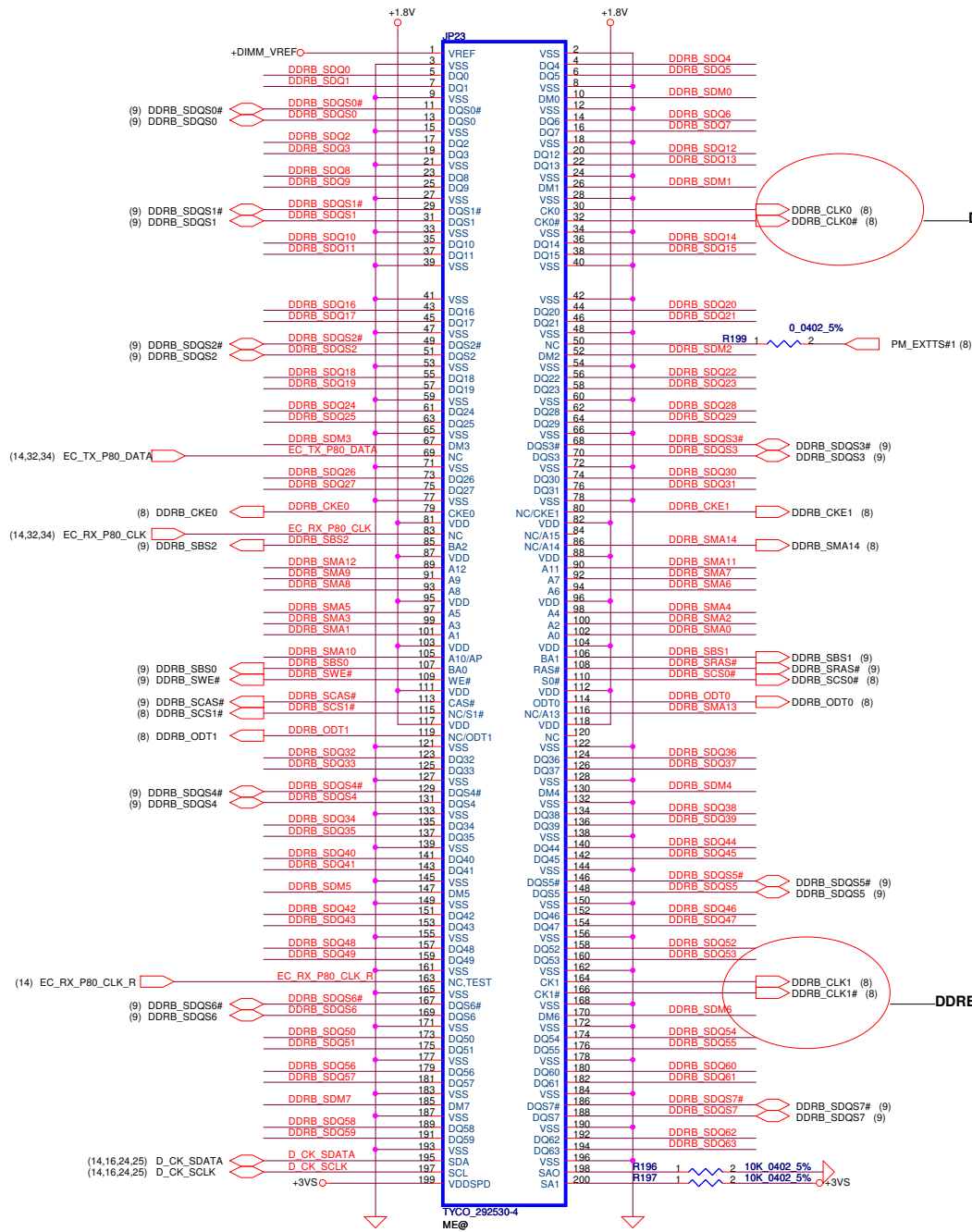




9/25 Change DIMM0 to SP070004Z00 (HBL50)

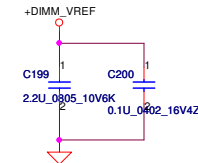


9/25 Change DIMM1 to SP070006F00

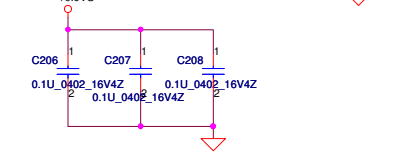
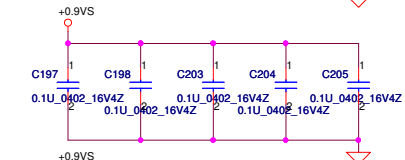
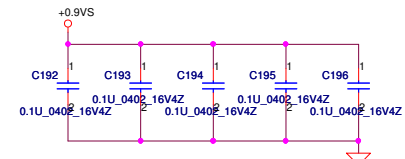
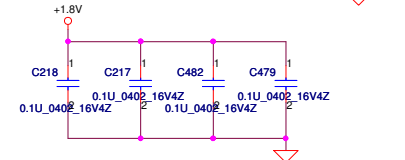
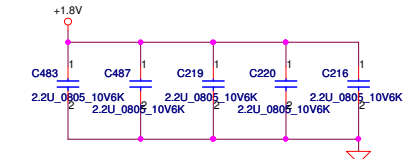


DIMM1 STD H:9.2mm (BOT)

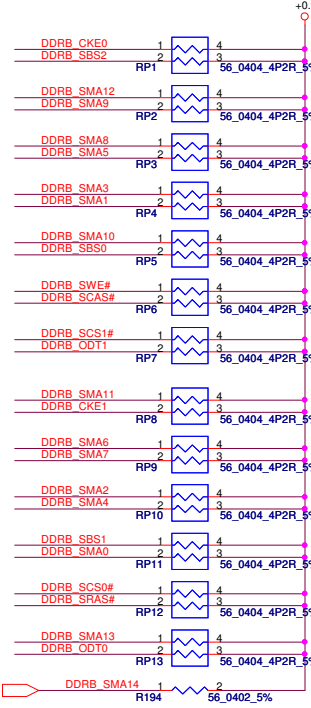
(9) DDRB_SMA[0..13] ← DDRB_SMA[0..13]
(9) DDRB_SDO[0..63] ← DDRB_SDO[0..63]
(9) DDRB_SDM[0..7] ← DDRB_SDM[0..7]



Layout Note:
Place near JP34



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



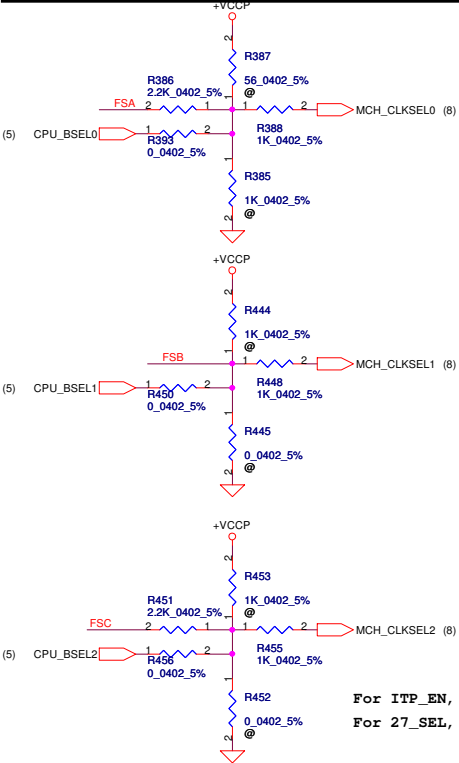
Layout Note:
Place these resistor
closely JP35, all
trace length Max=1.5"

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								Size B			
								Document Number			
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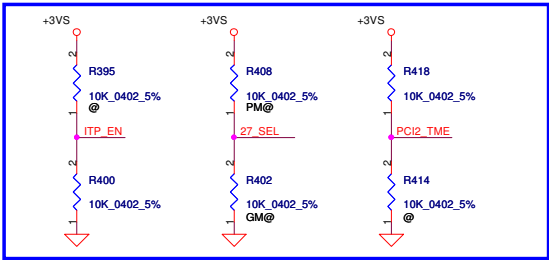
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

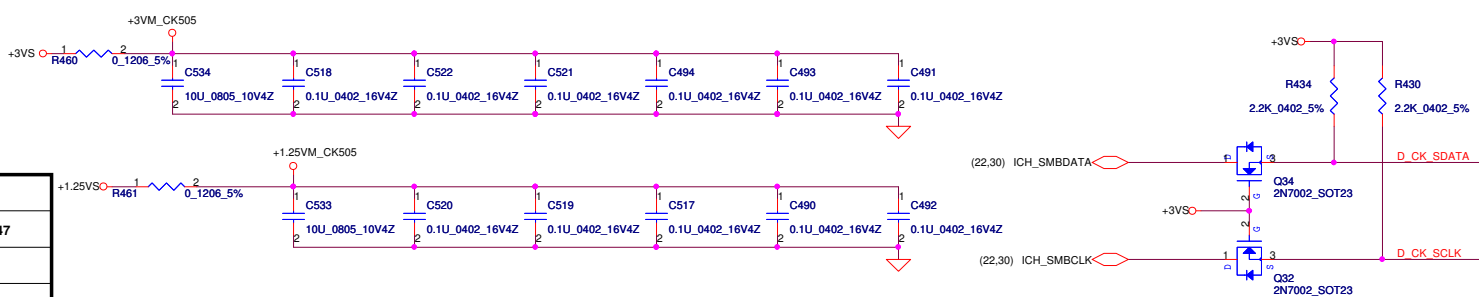
CPU Driven	Stuff						
★(Default)	No Stuff	R401	R408	R417	R430	R438	R447
	Stuff	R401	R417	R447			
667MHz	No Stuff	R408	R430	R438			
	Stuff	R408	R417	R447			
800MHz	No Stuff	R401	R430	R438			
	Stuff	R401	R430	R447			



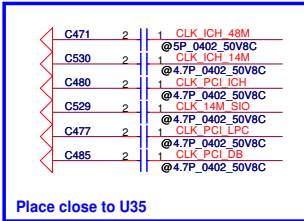
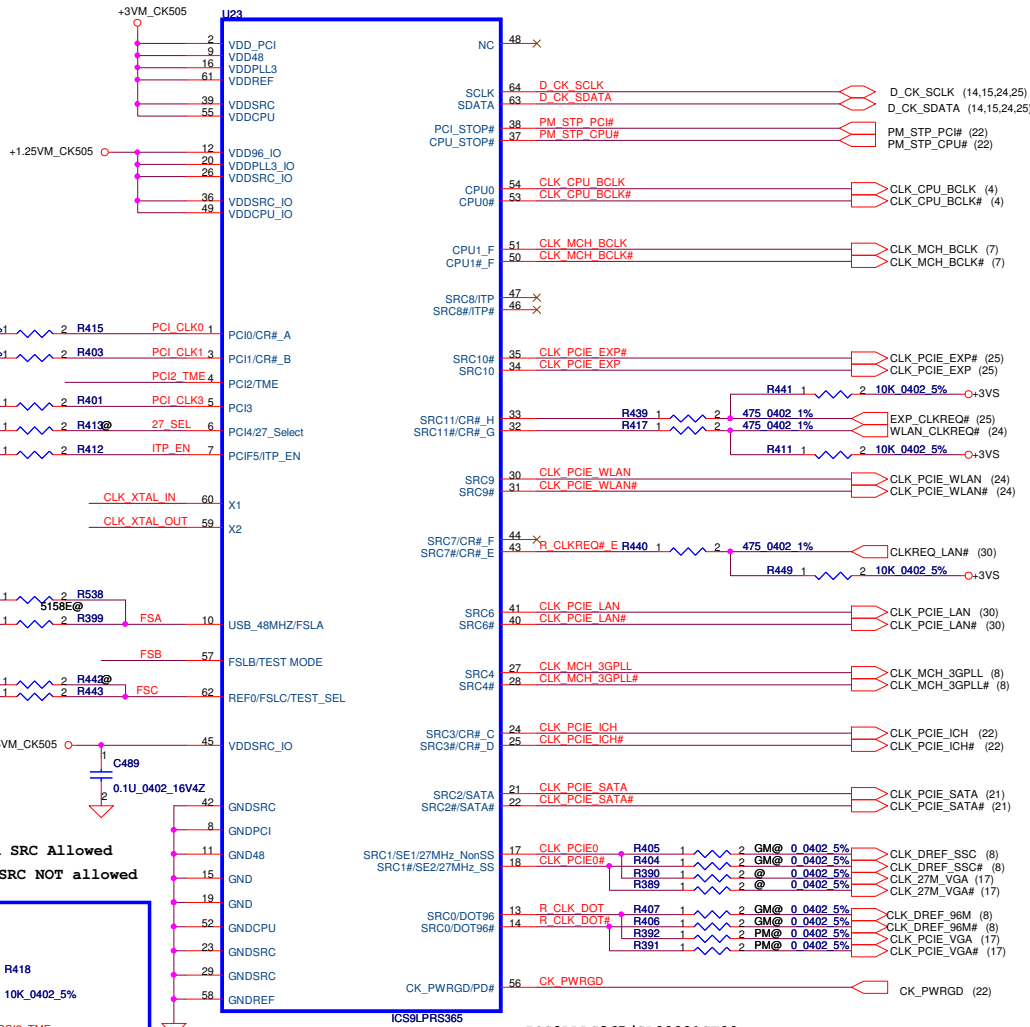
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed



Routing the trace at least 10mil

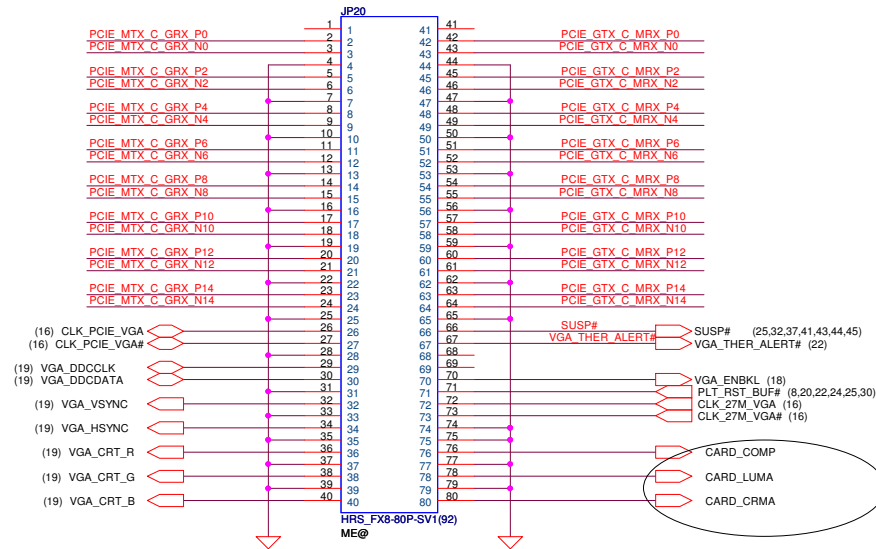
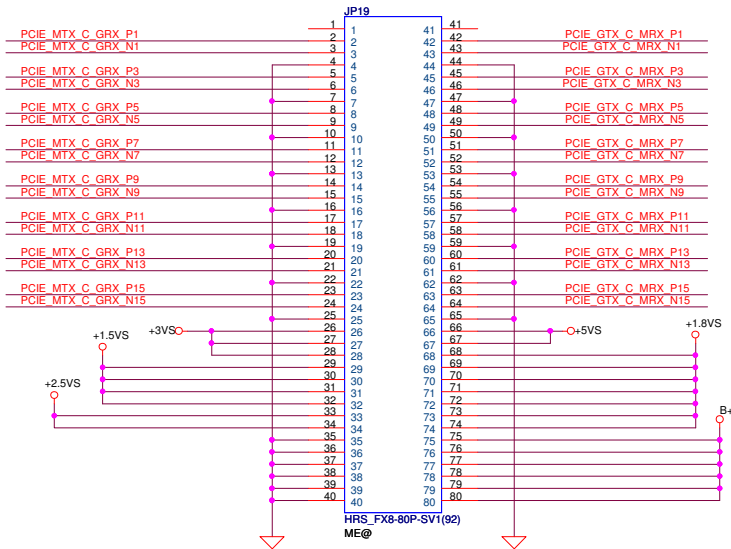


4/16 : Change P/N from SA0001GT10(ICS) to SA00001IJ00 (SILEGO)



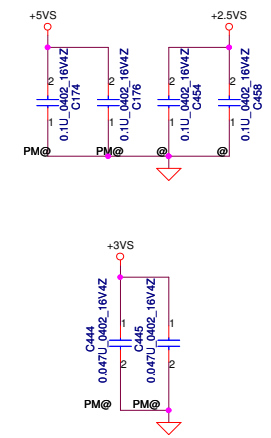
Place close to U35

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MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

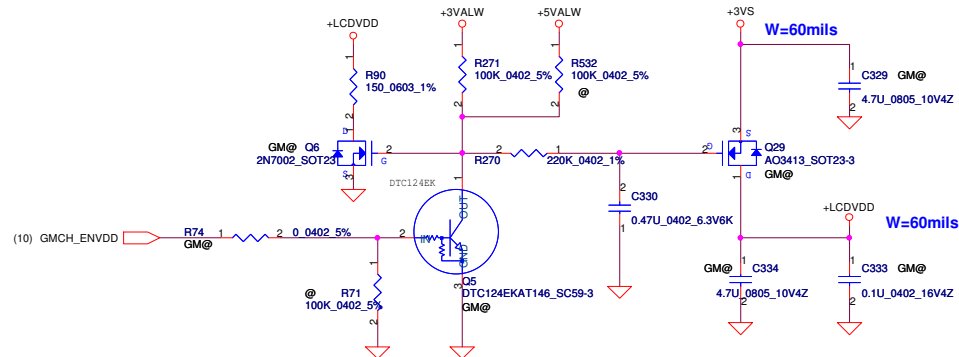
(10) PCIE_MTX_C_GRX_N[0..15] < PCIE_MTX_C_GRX_N[0..15]
(10) PCIE_MTX_C_GRX_P[0..15] < PCIE_MTX_C_GRX_P[0..15]
(10) PCIE_GTX_C_MRX_N[0..15] < PCIE_GTX_C_MRX_N[0..15]
(10) PCIE_GTX_C_MRX_P[0..15] < PCIE_GTX_C_MRX_P[0..15]



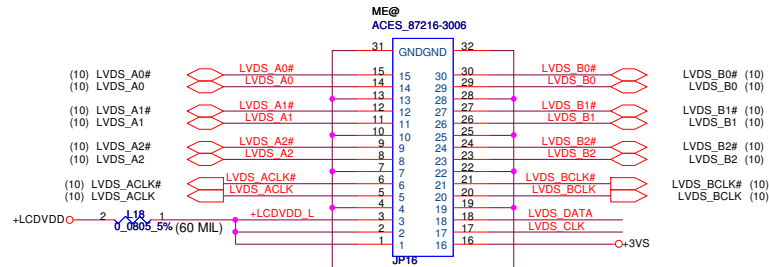
Compal Electronics, Inc.			
VGA/B connector			
Title	Size	Document Number	Rev
	Custon	LA-3861P	0.1
Date	Monday, August 20, 2007	Sheet	17 of 47

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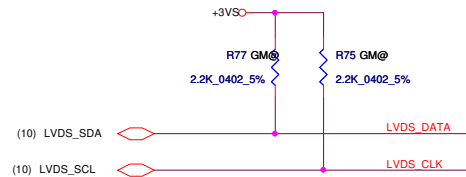
LCD POWER CIRCUIT



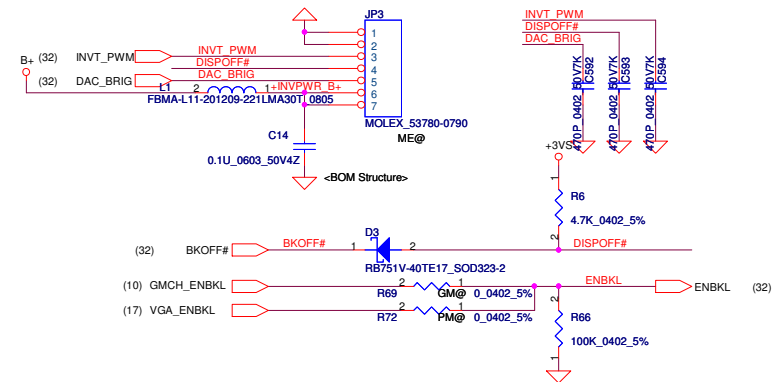
LCD/PANEL BD. Conn.



Follow HEL80's pin definition
Except pin 29



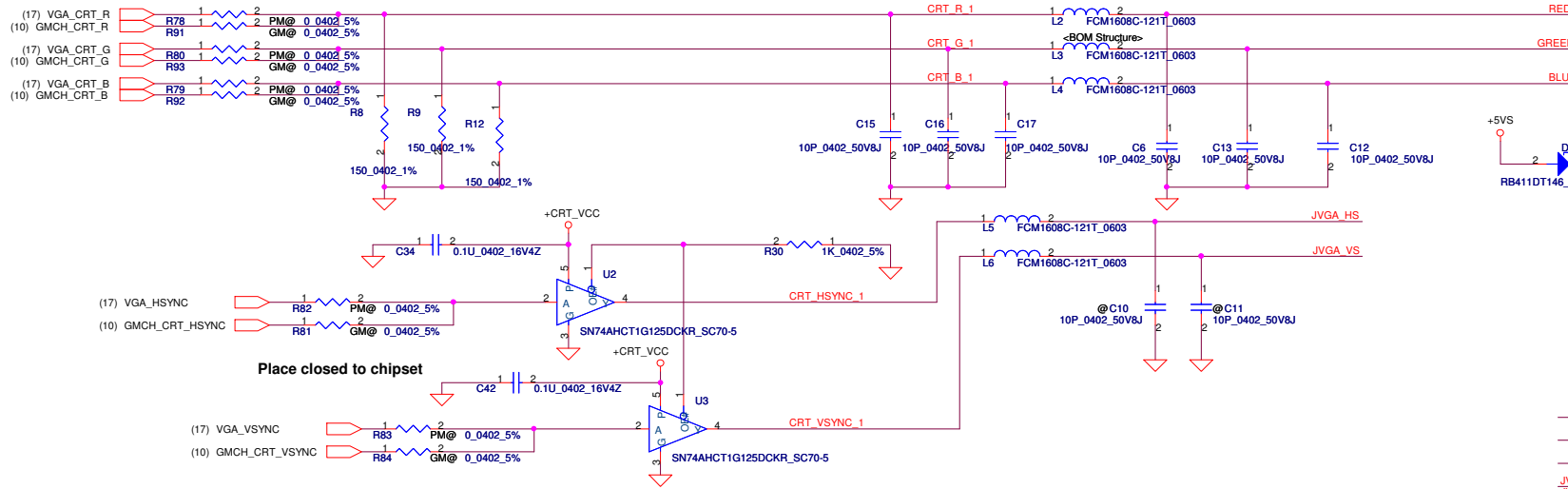
INVERTER Conn.



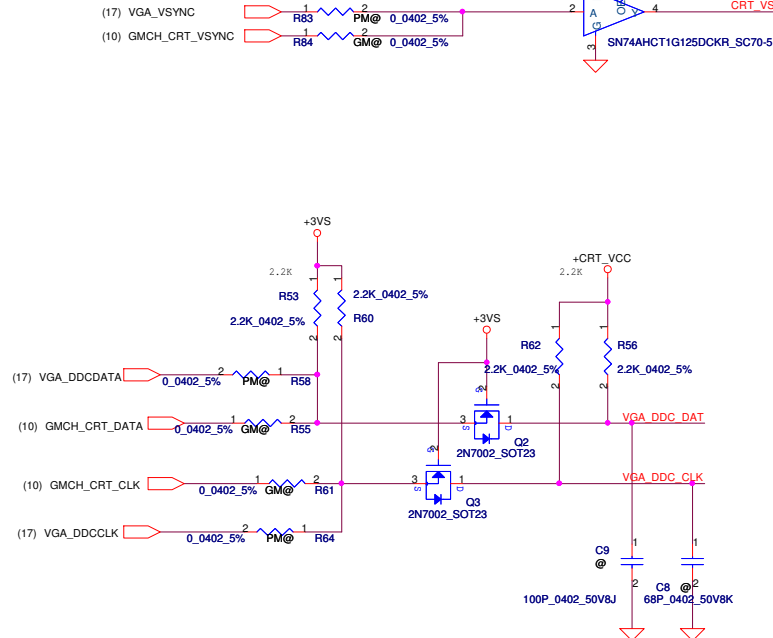
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18				Title			
				Deciphered Date				2007/8/18			
								LVDS & DVI Connector			
								Rev			
								0.1			
								Date			
								Monday, August 20, 2007			
								Sheet			
								18 of 47			

CRT Connector

Place closed to chipset

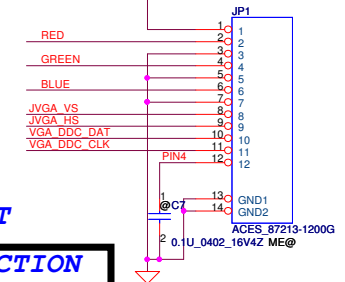


Place closed to chipset

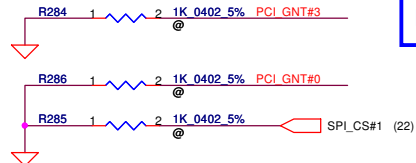
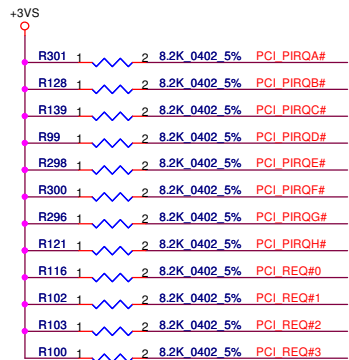
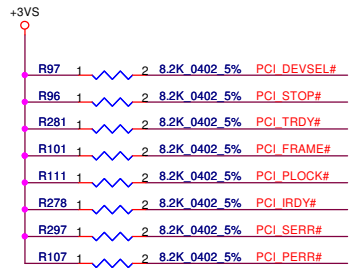


PIN ASSIGNMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSNC
9	10	GND
10	13	HSYNC
11	11	SENSE
12	12	SM_DAT
13	15	SM_CLK
14	4	PIN4



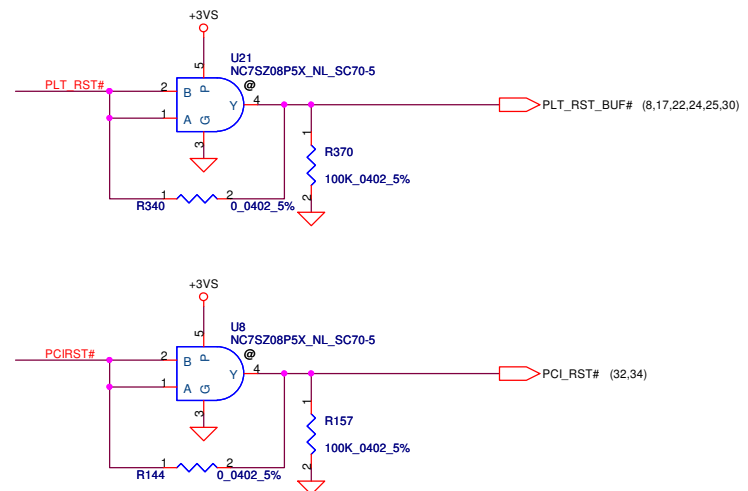
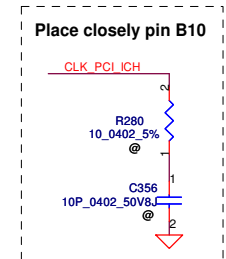
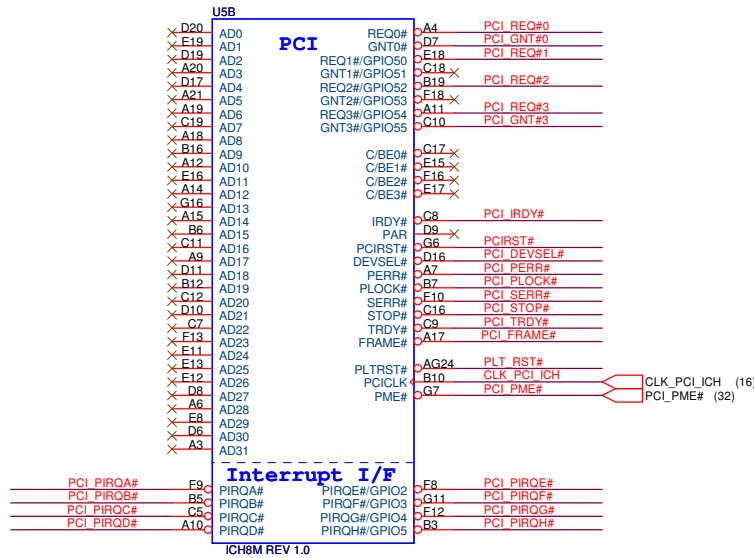
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	CRT & TV-OUT Connector		
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				Date: Monday, August 20, 2007	Sheet 19	of 47

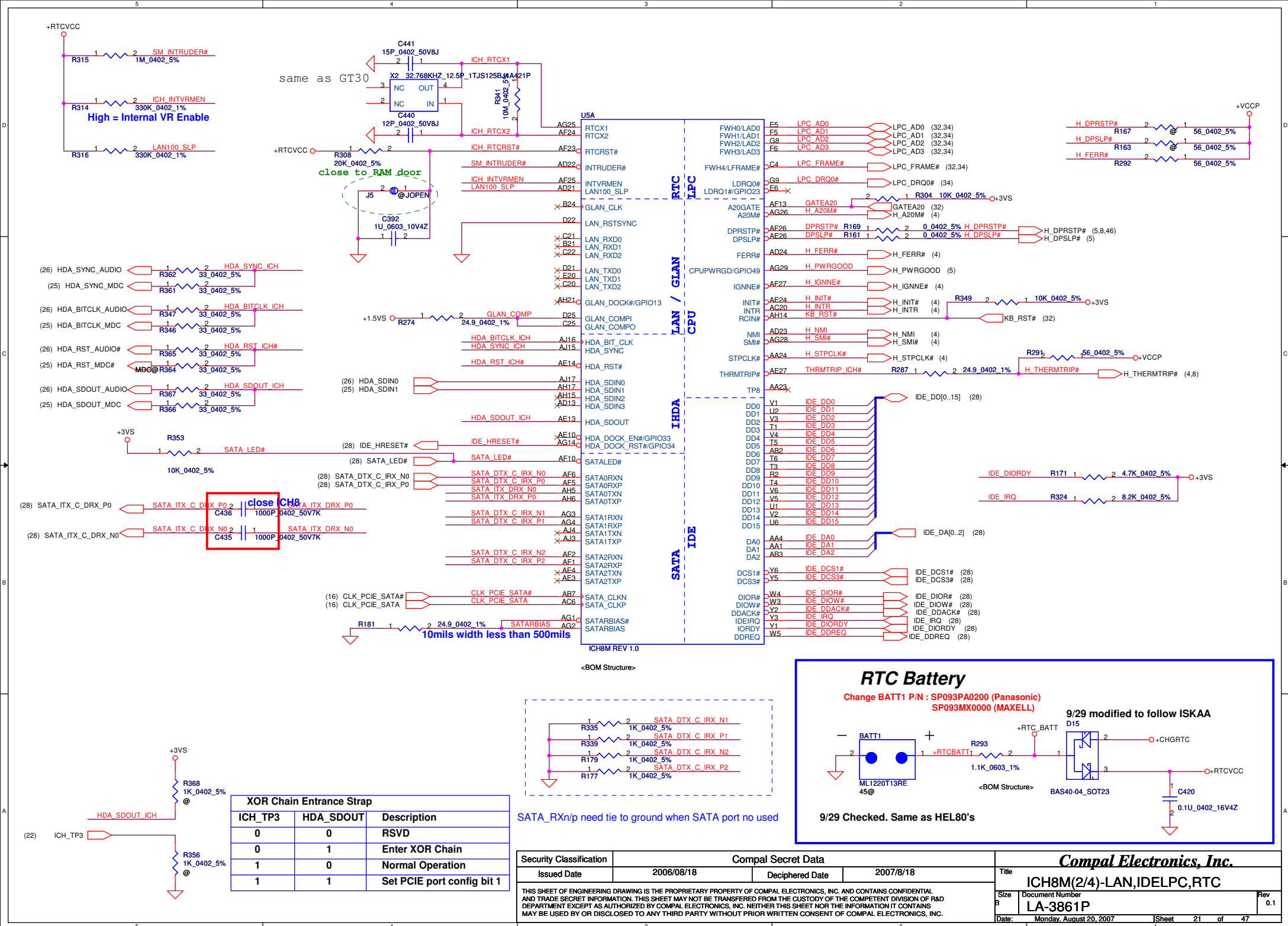


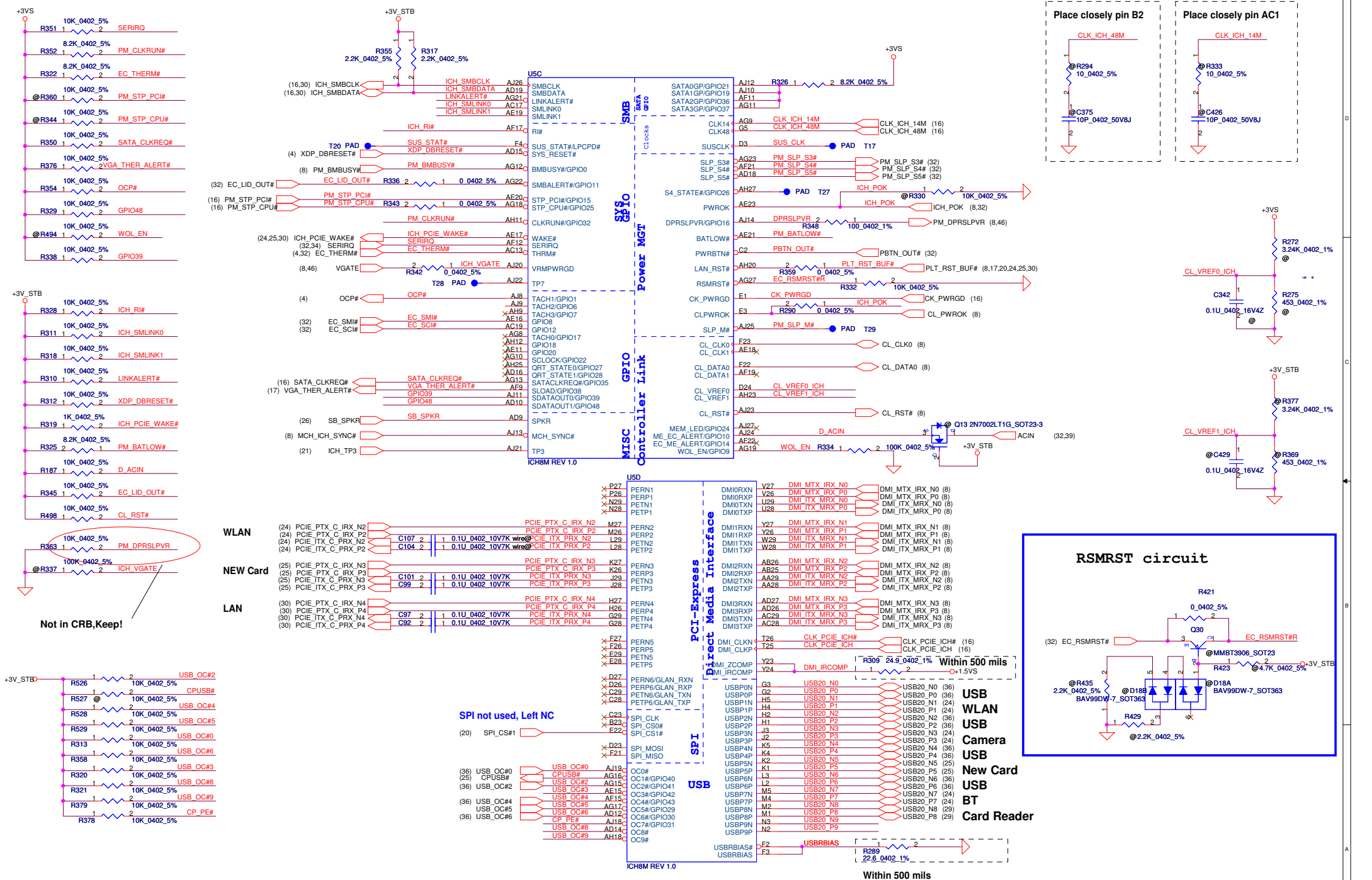
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

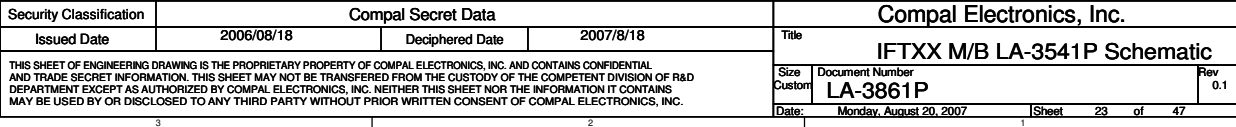
10/17 : Change P/N from SA000010G00 to SA00001JU10
 10/17 : FootPrint : SA000010G00
 BOM : SA00001JU10





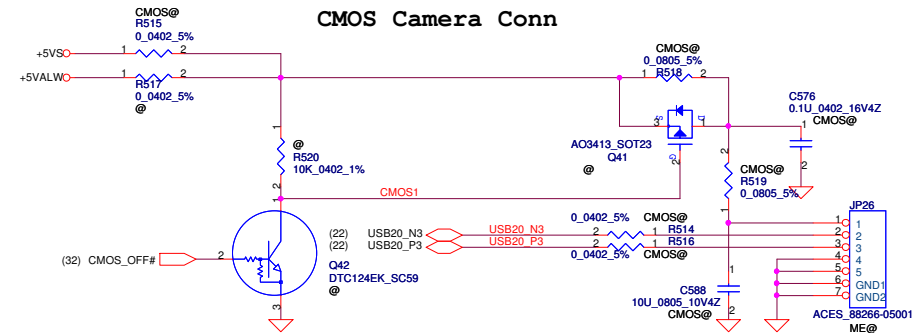
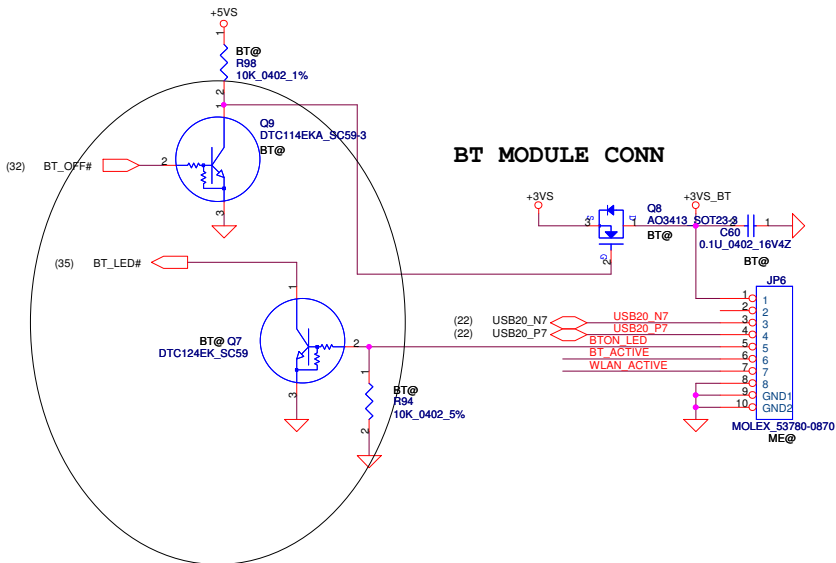
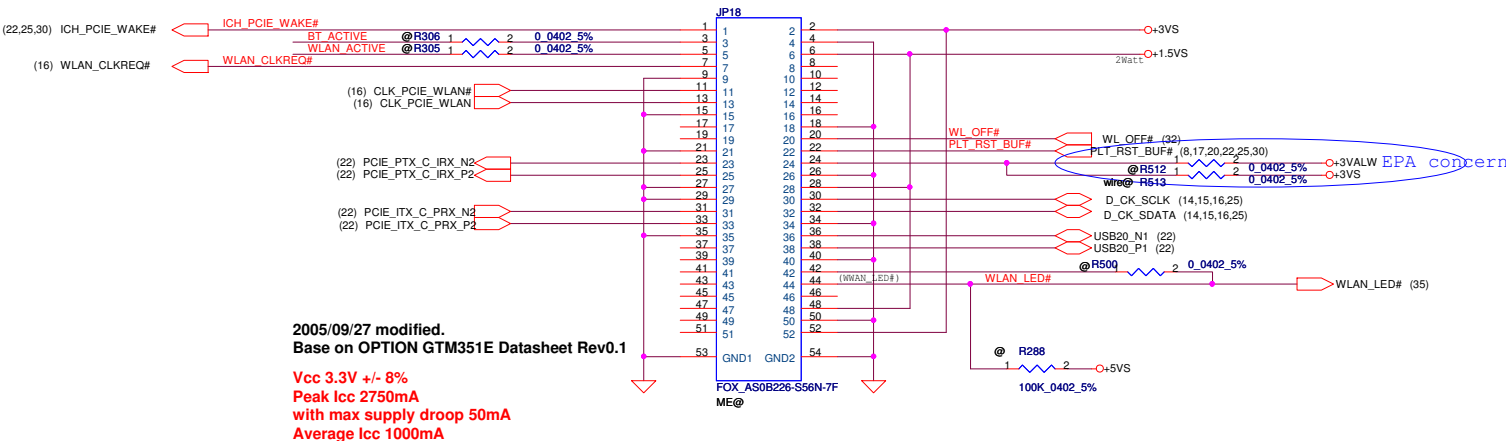
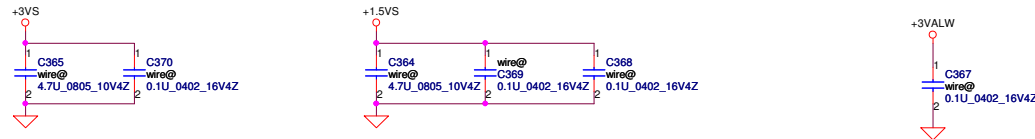


Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2006/08/18	Deciphered Date	2007/8/18	Title			
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					Size	Document Number		Rev
					Customer	LA-3861P		0.1
					Date:	Monday, August 20, 2007	Sheet	22



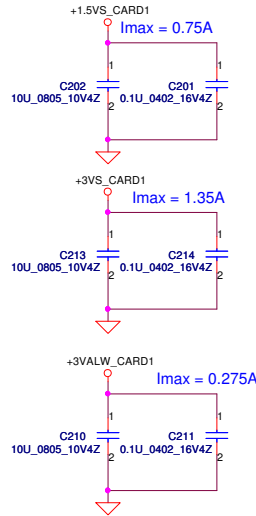
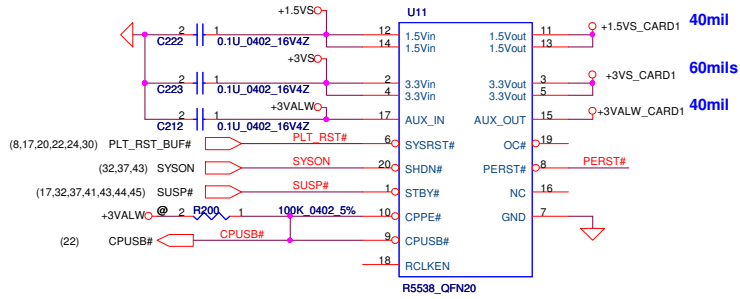
Mini-Express Card for 3G Or TV Tuner

Mini-Express Card for WLAN

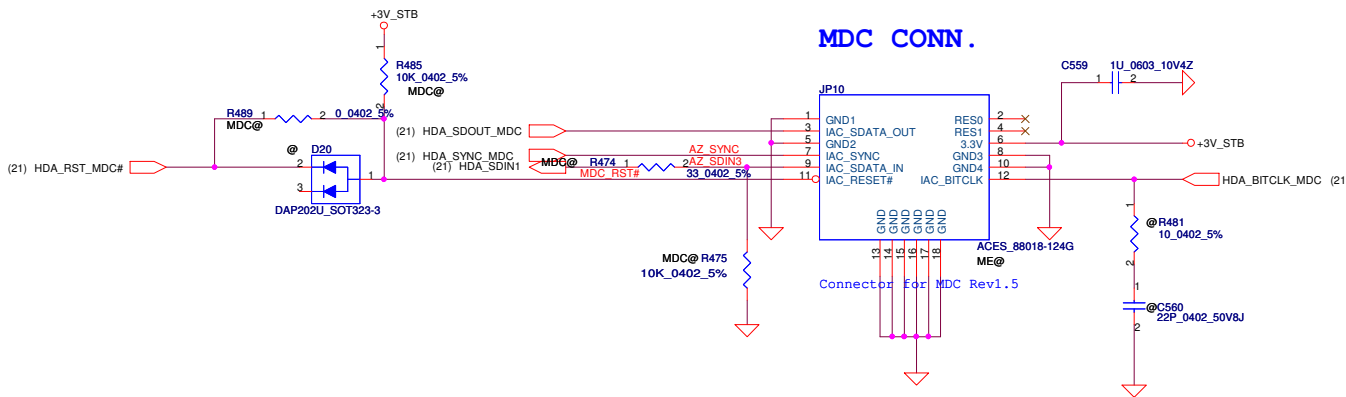
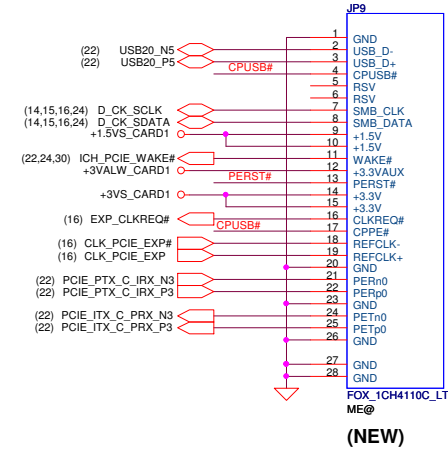


Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/3G/FeliCa/FP	
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Express Card Power Switch

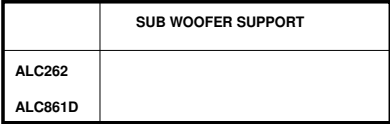


New Card Socket (Left/TOP)



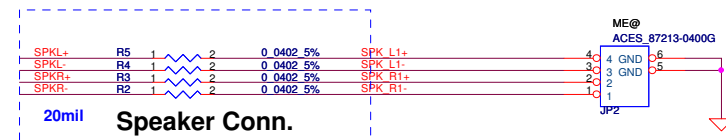
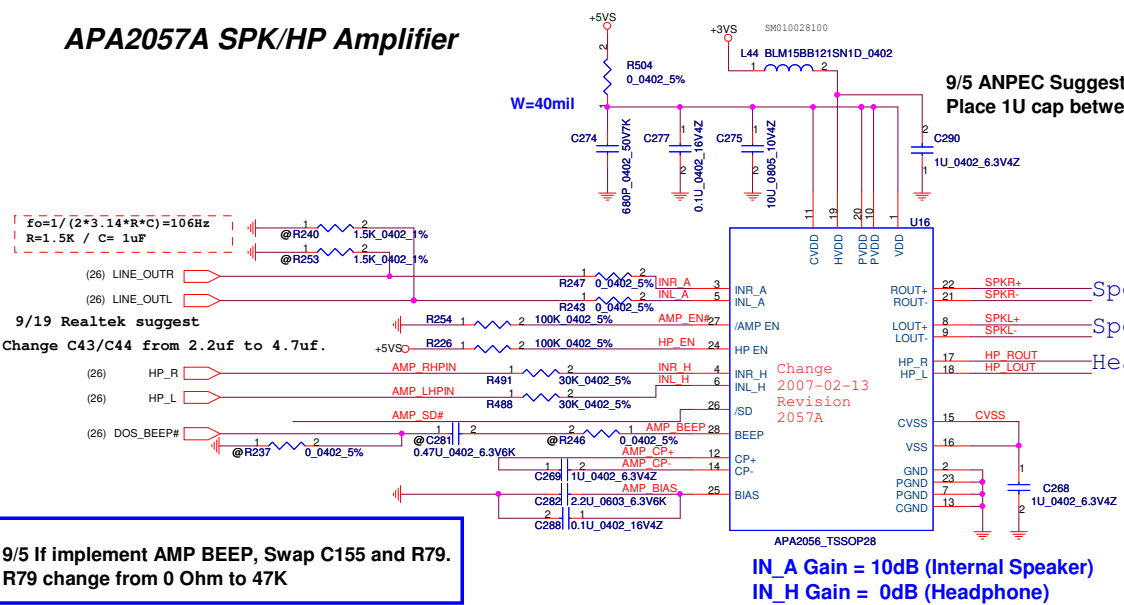
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	NEW CARD & USB Connector
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28.7K for Module Design (VDDA = 4.702



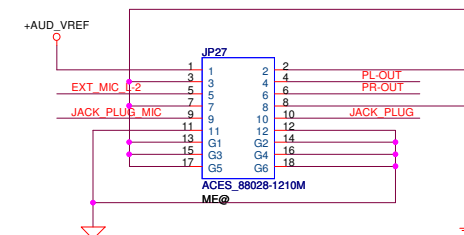
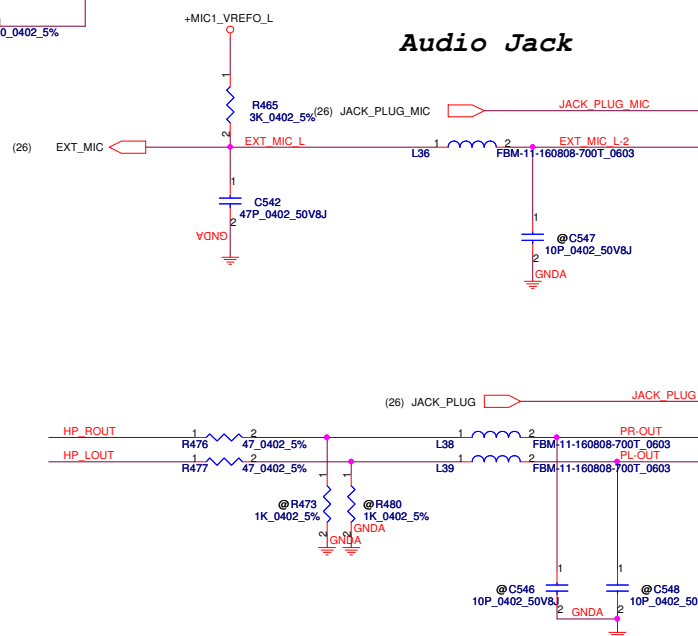
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title ALC861 VD Codec		
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				Date: Monday, August 20, 2007	Sheet 26	of 47

APA2057A SPK/HP Amplifier

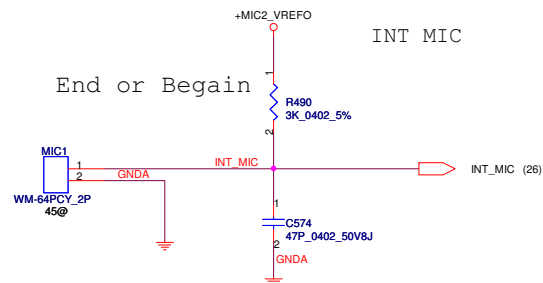


EXT MIC

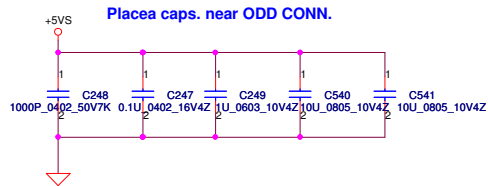
Audio Jack



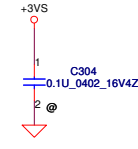
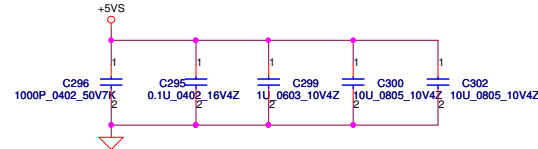
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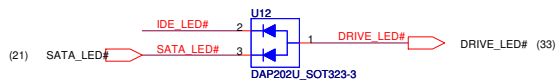
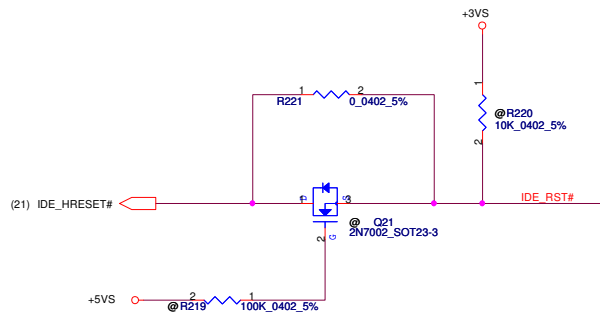
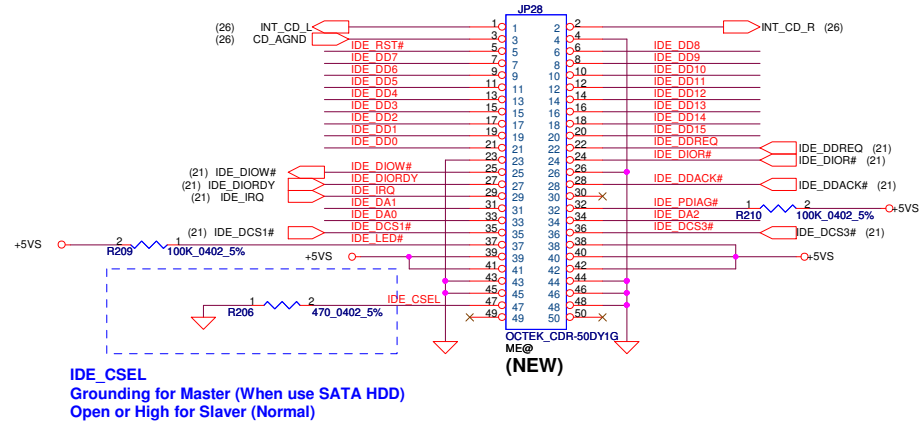
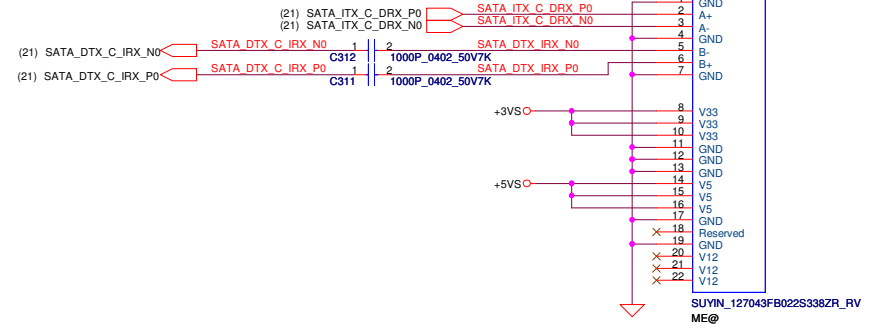
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Issued Date	2006/08/05	Deciphered Date	2007/08/05	AMP/VR/Audio Jack/MIC	
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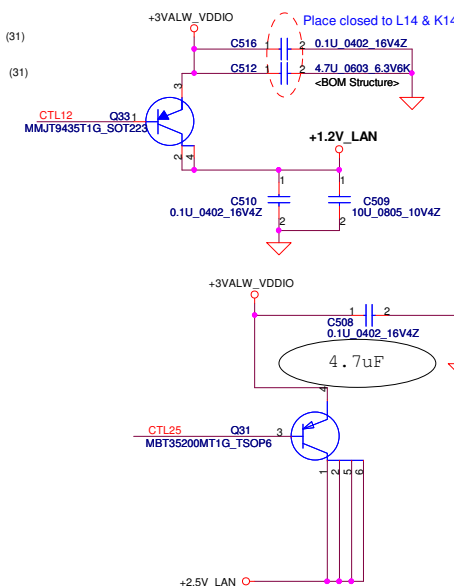
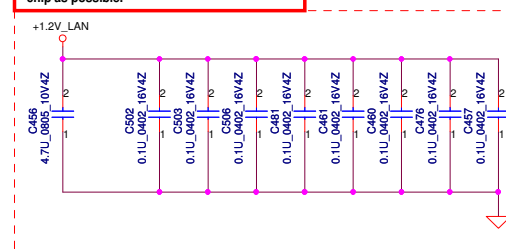
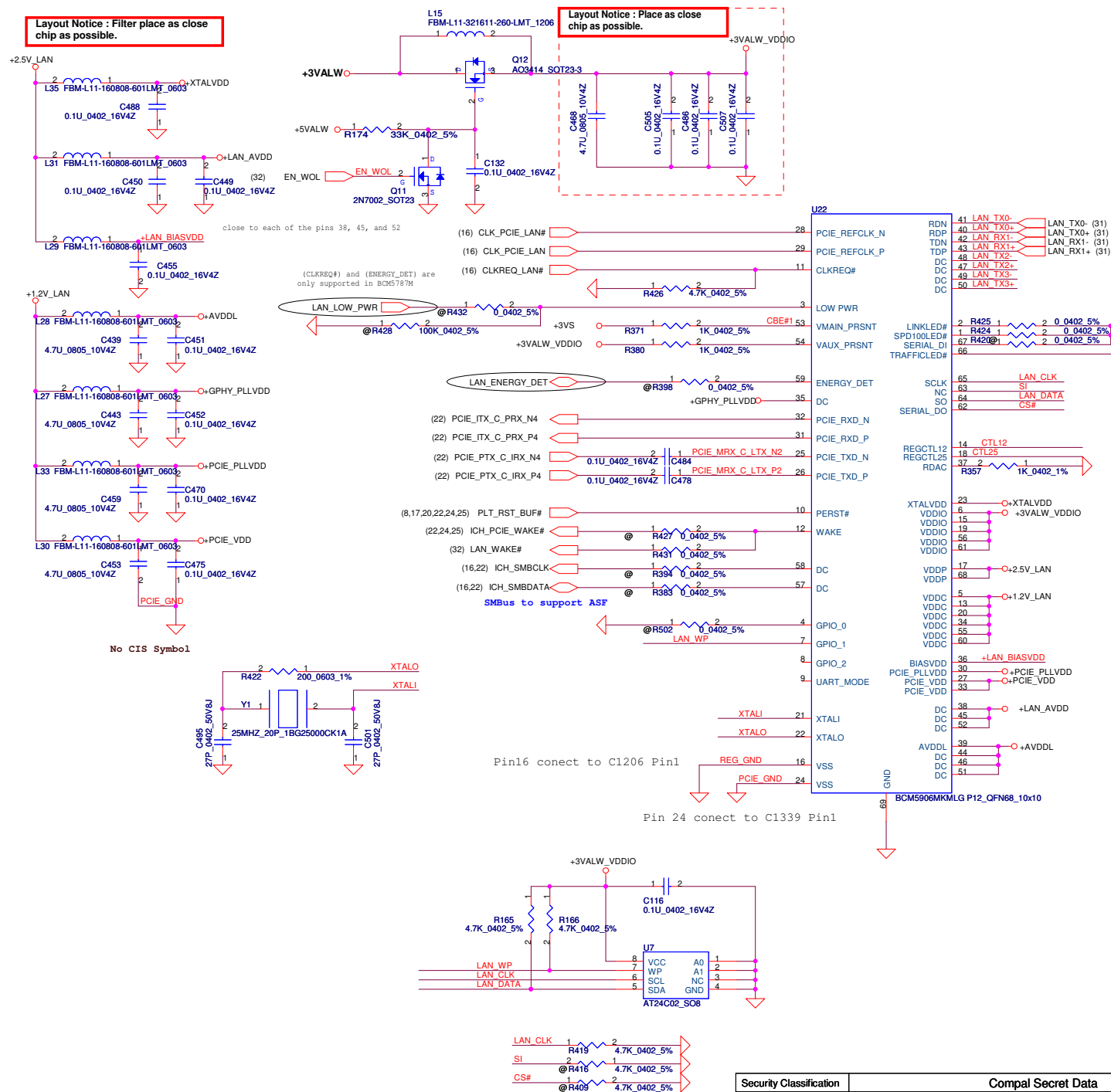
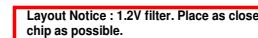
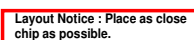
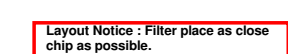
(21) IDE_DD[0..15] IDE_DD[0..15]
 (21) IDE_DA[0..2] IDE_DA[0..2]



SATA HDD Conn.



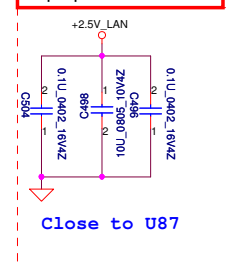
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size B	Document Number	LA-3861P		Rev	0.1
Date:	Monday, August 20, 2007	Sheet	28	of	47



Notice : 4.7u 6.3V capactor Thickness 1.25mm

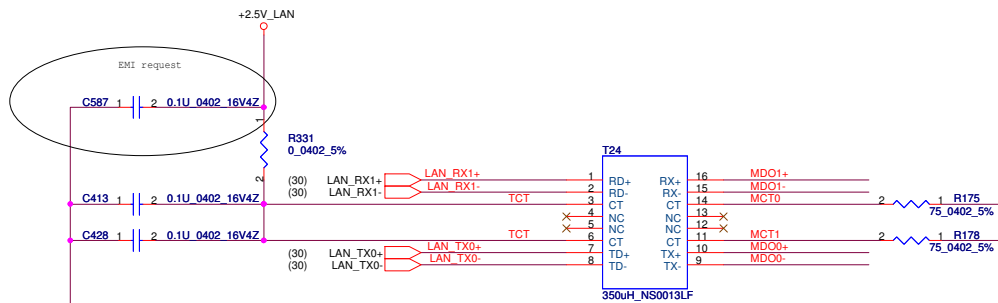
Layout Notice : Filter place as close to chip as possible.

Layout Notice : Place as close to the chip as possible.

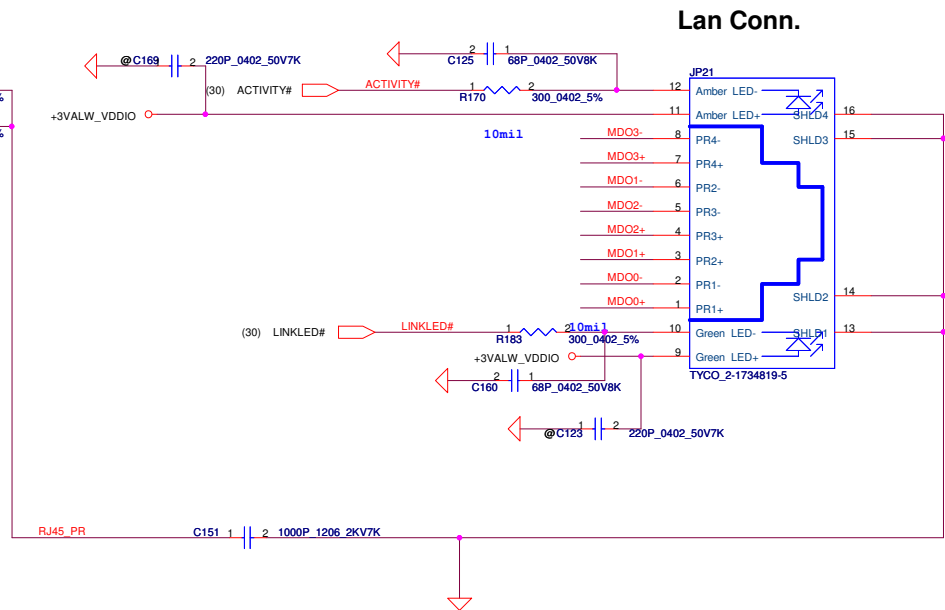
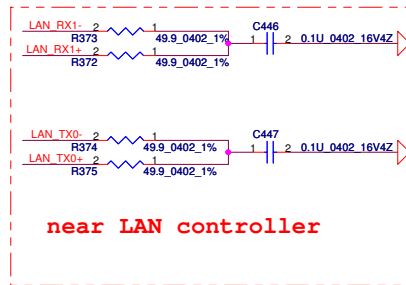


Close to U87

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				Document Number	
				LA-3861P	
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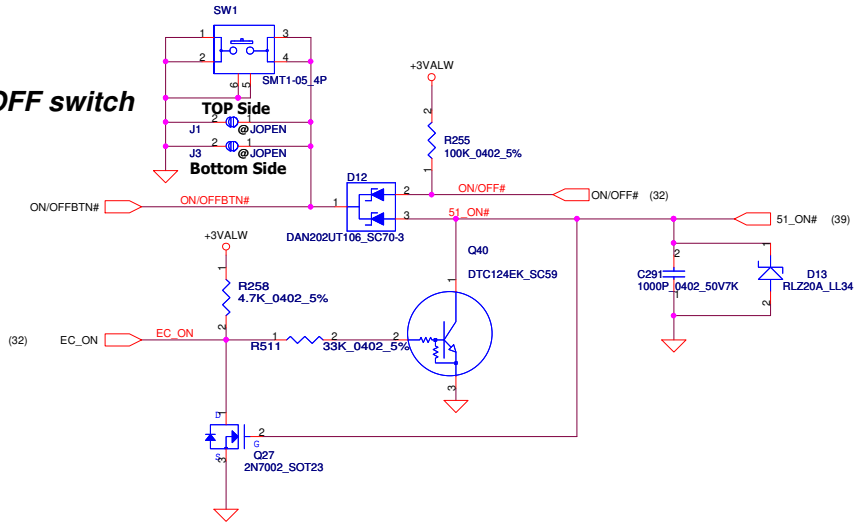
Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



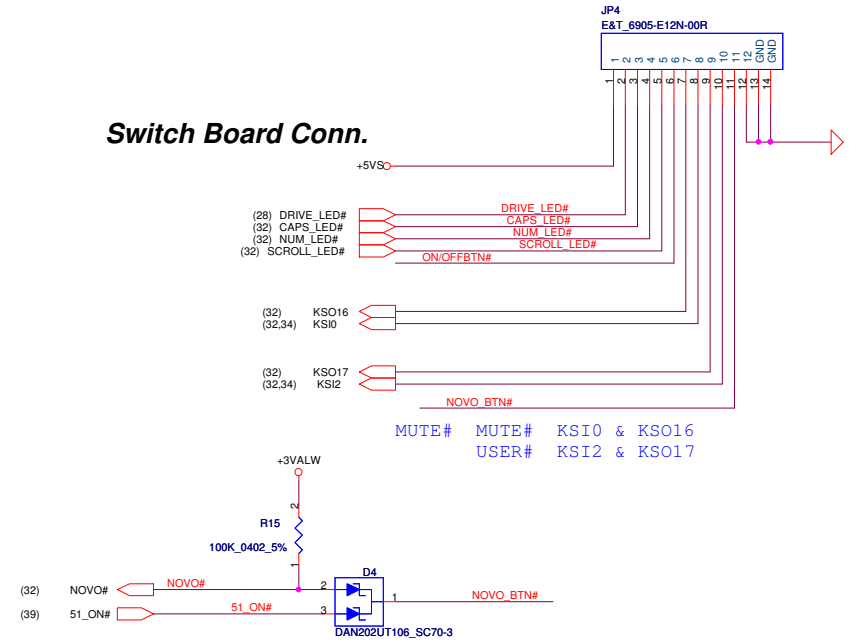
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						Size		Document Number		Rev	
						Custant		LA-3861P		0.1	
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Power Button

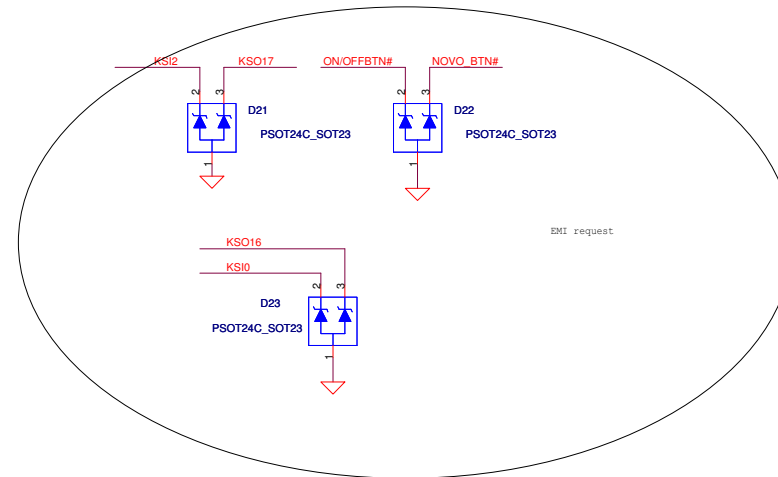
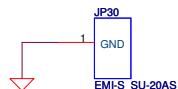
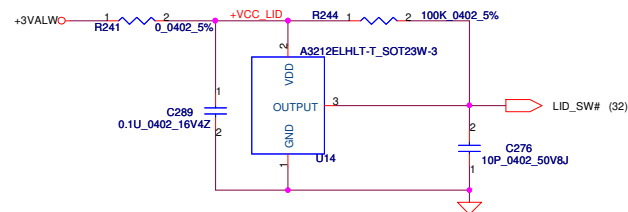
ON/OFF switch



Switch Board Conn.

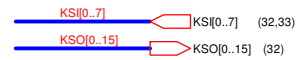


Lid Switch



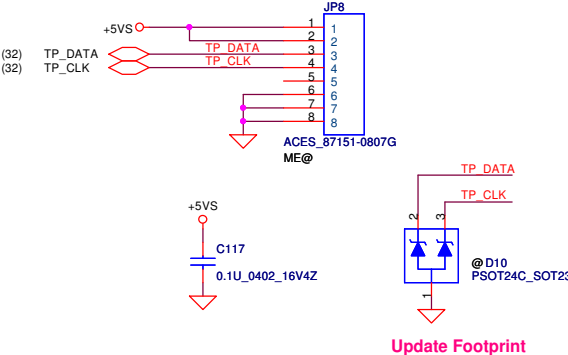
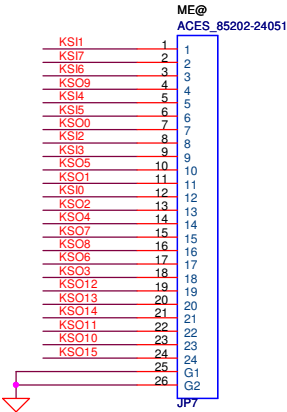
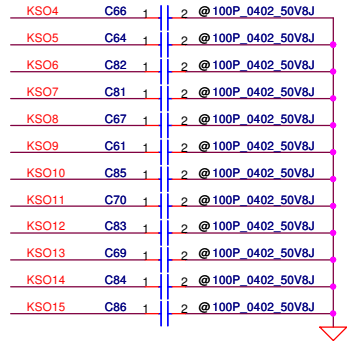
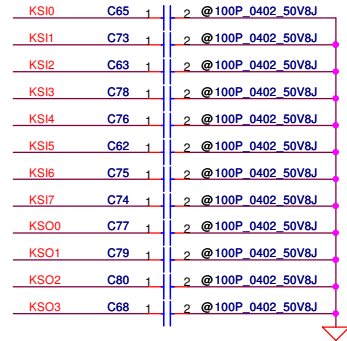
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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title			
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						Size B	Document Number			Rev	
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INT_KBD Conn.

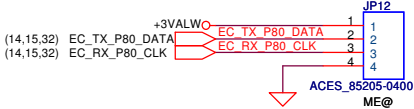


For IHL00

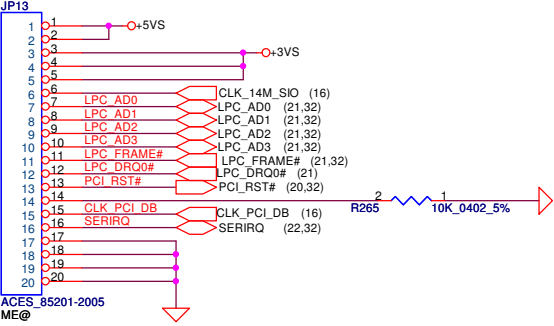
To TP/B Conn.



EC DEBUG PORT

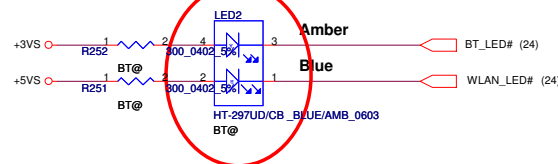
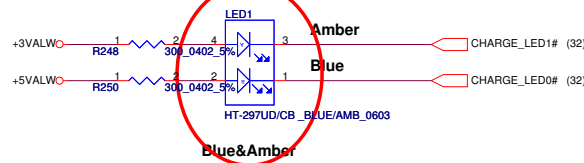
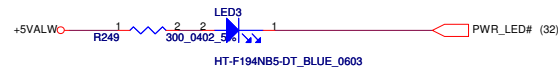


FOR LPC SIO DEBUG PORT



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LED

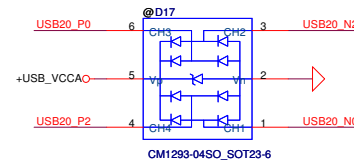
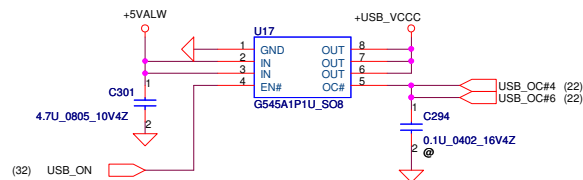
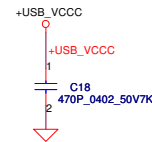
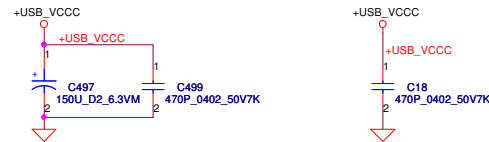
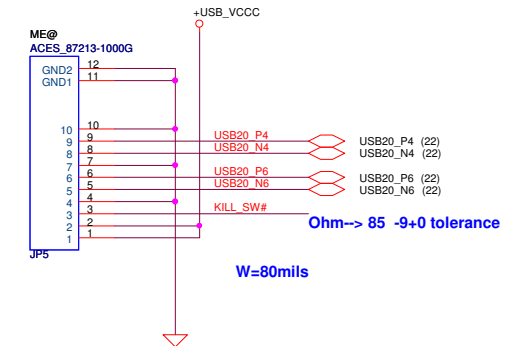
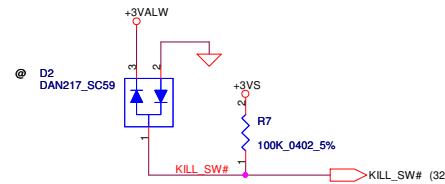


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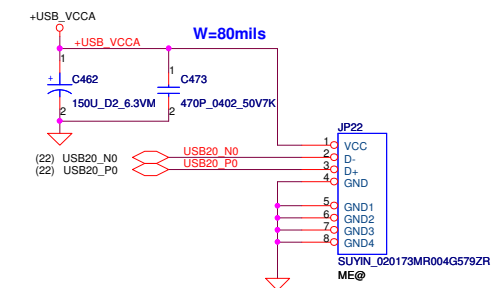
USB Conn.

W=80mils

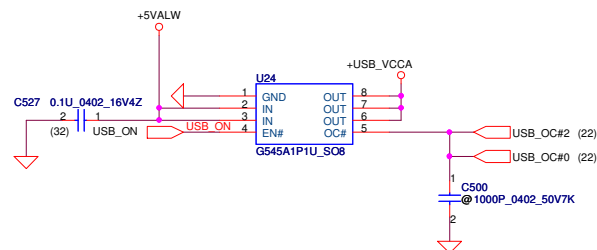
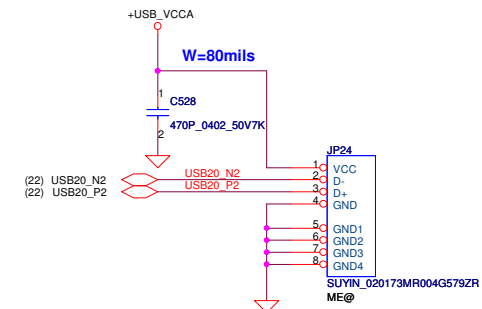
Kill SWITCH



USB CONN. 1

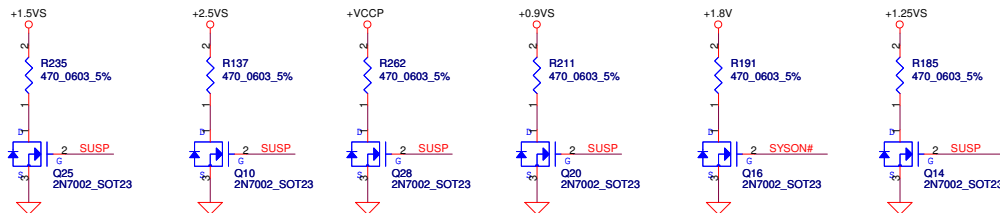
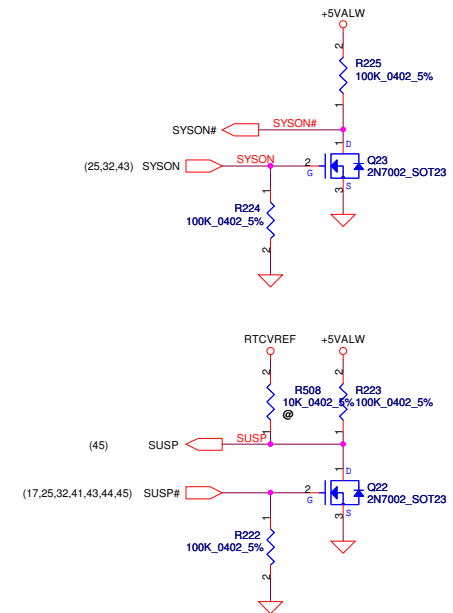
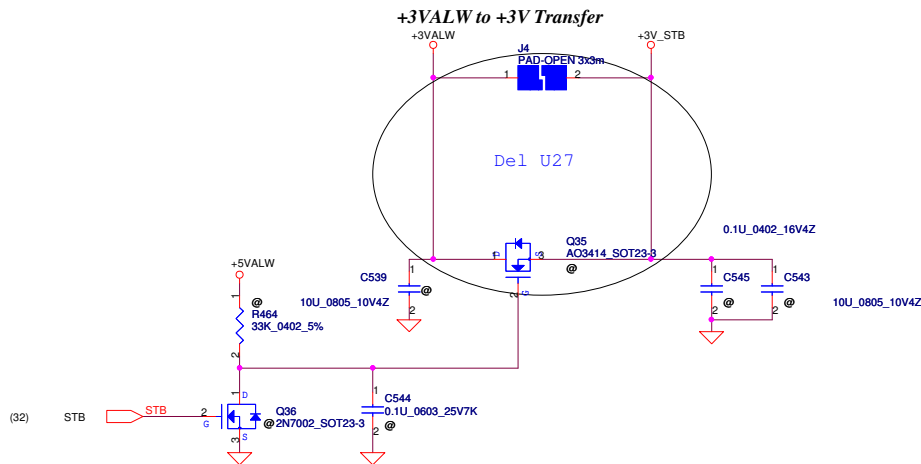
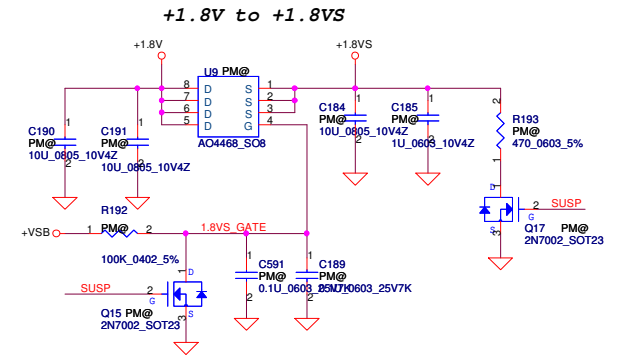
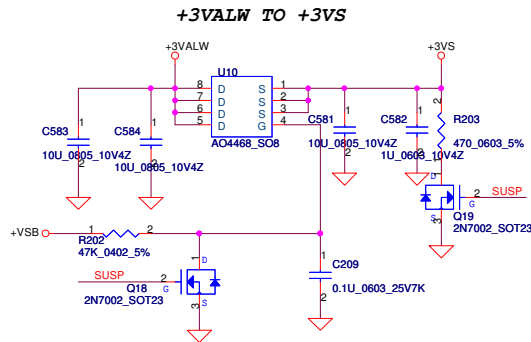
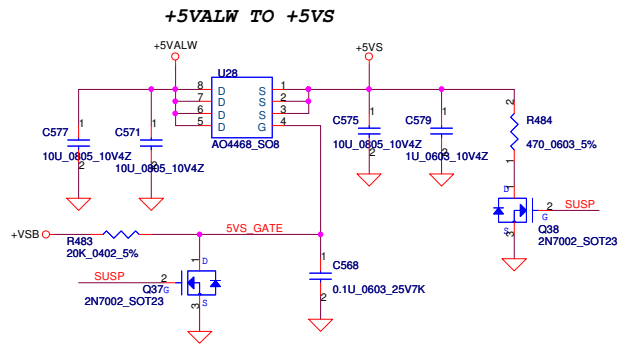


USB CONN. 2

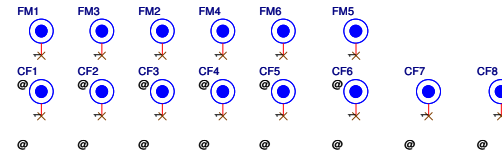
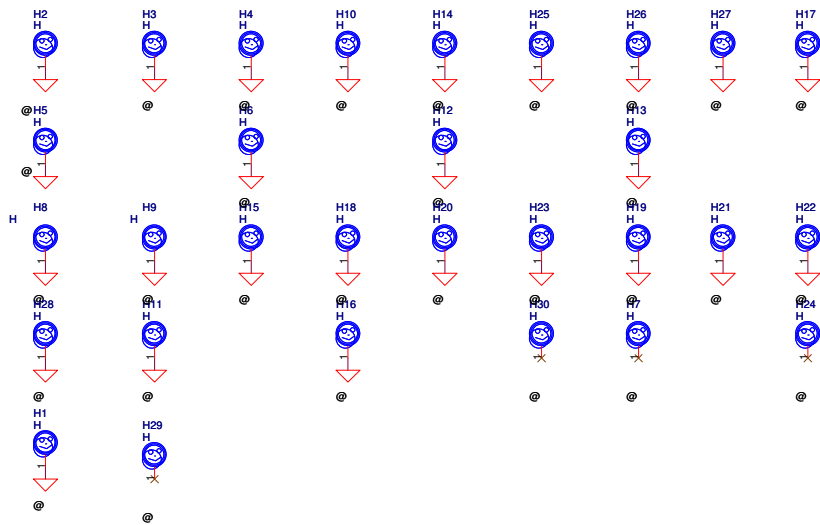


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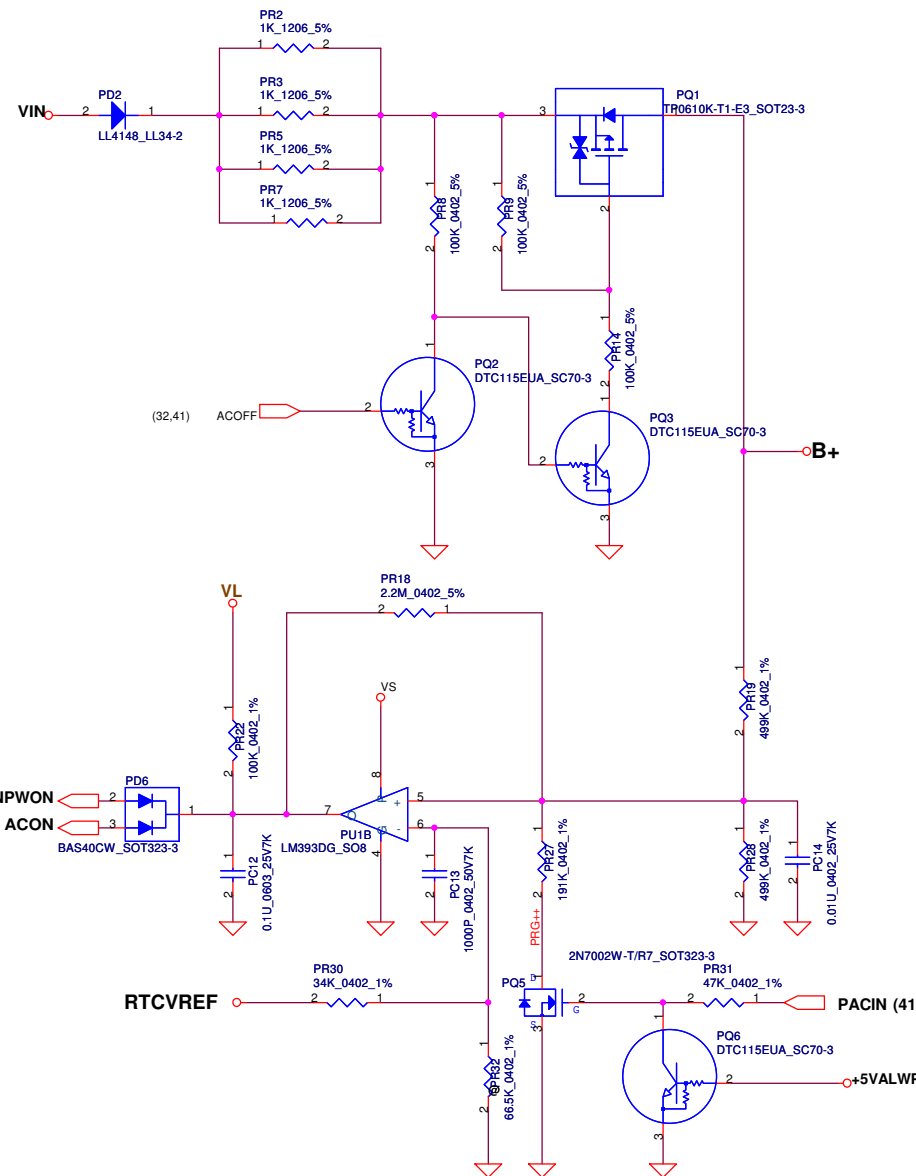


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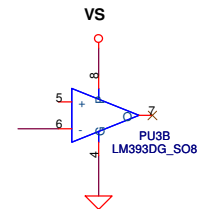


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ACIN				BATT ONLY			
Precharge detector				Precharge detector			
	Min.	typ.	Max.		Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V	H-->L	6.138V	6.214V	6.359V
L-->H	15.562V	15.97V	16.388V	L-->H	7.196V	7.349V	7.505V



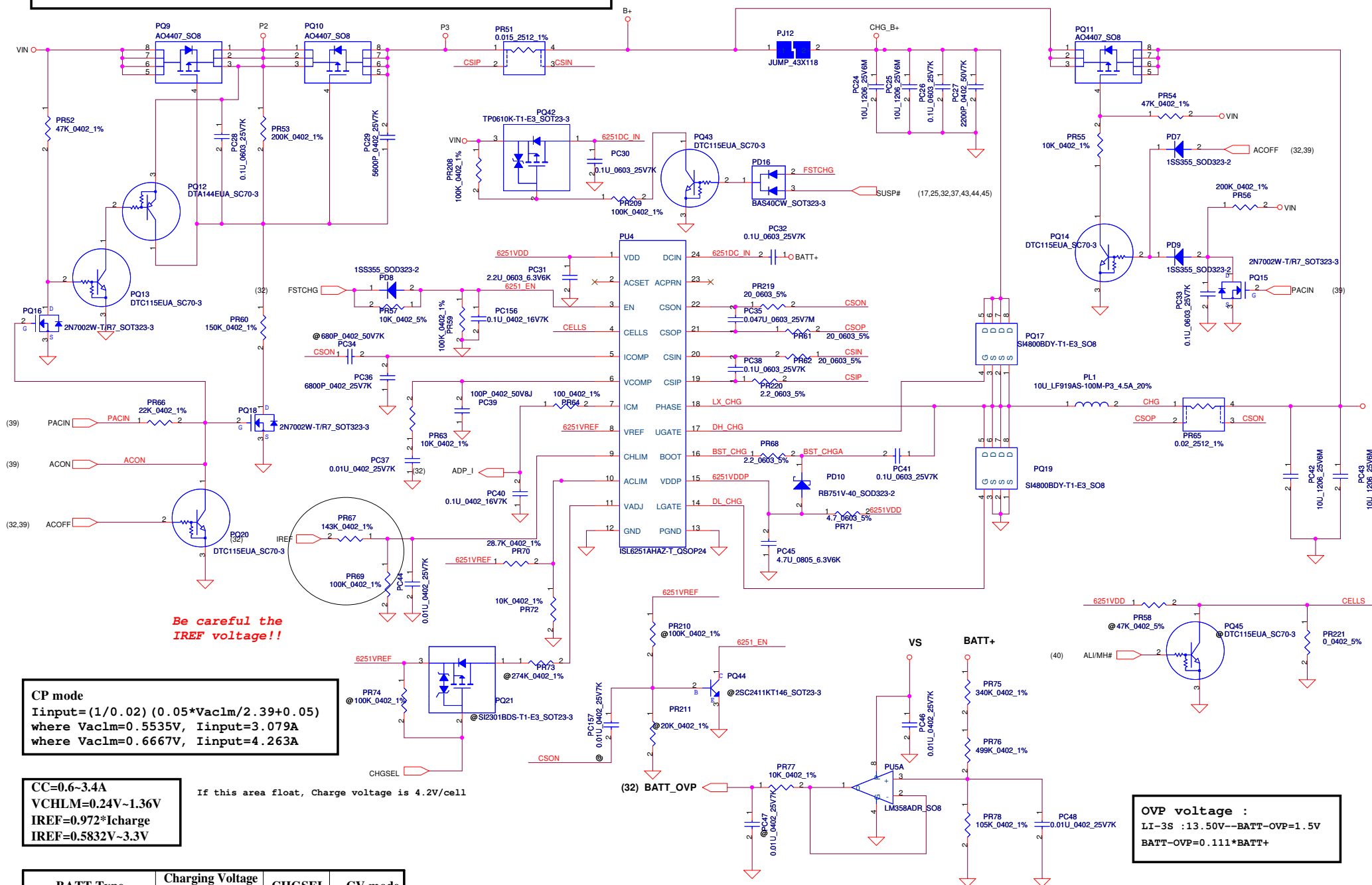
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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR70=39.2K, CP=3.079A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR70=28.7K, CP=4.263A

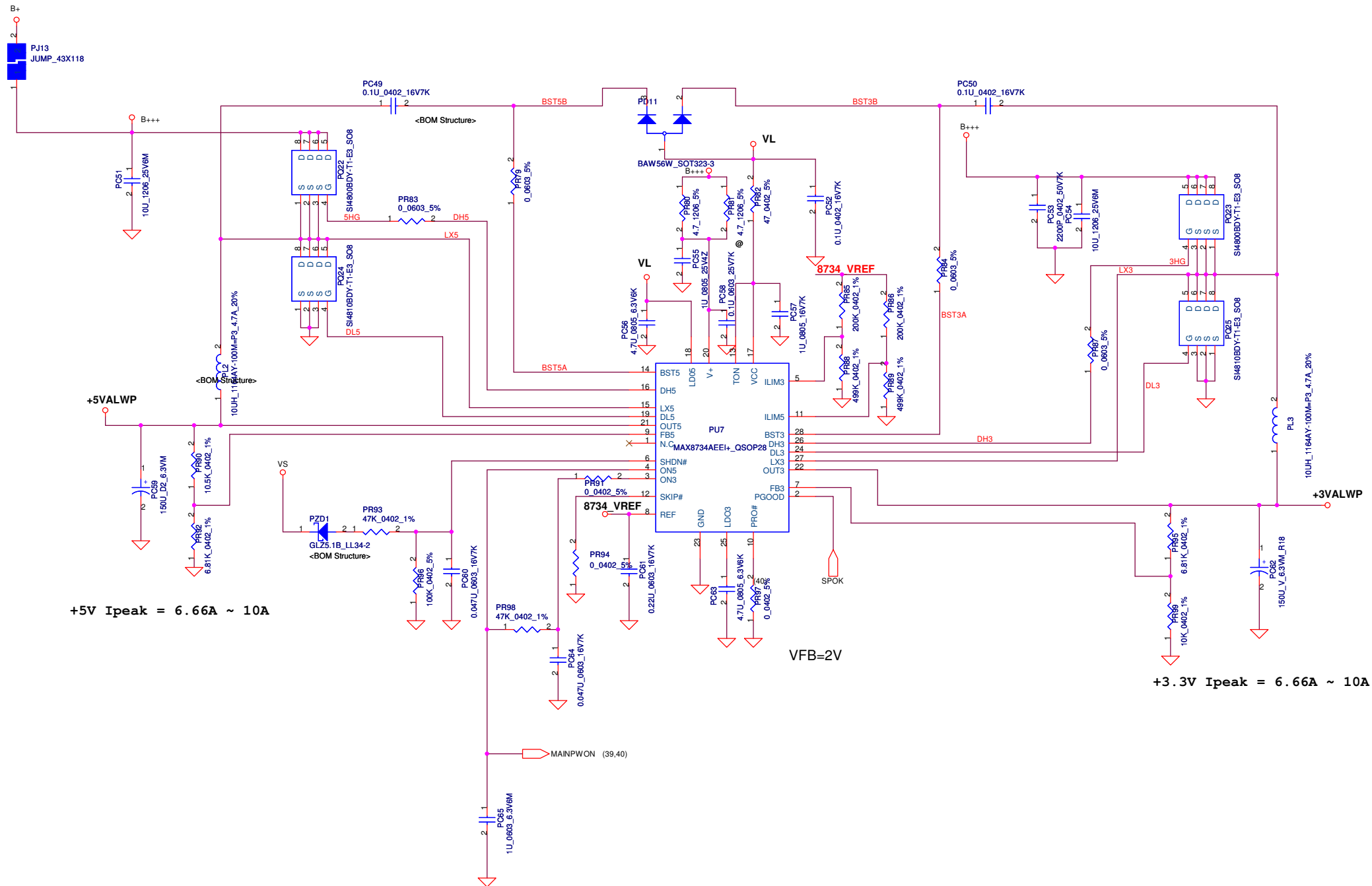
$$ADP_I = 19.9 * I_{\text{adapter}} * R_{\text{sense}}$$



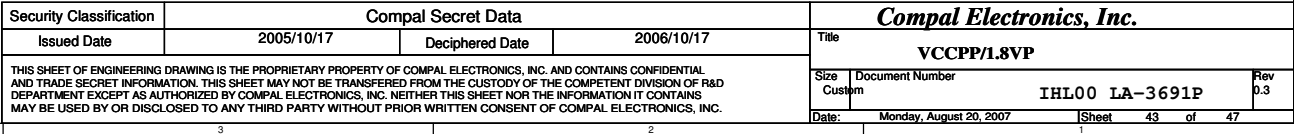
BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

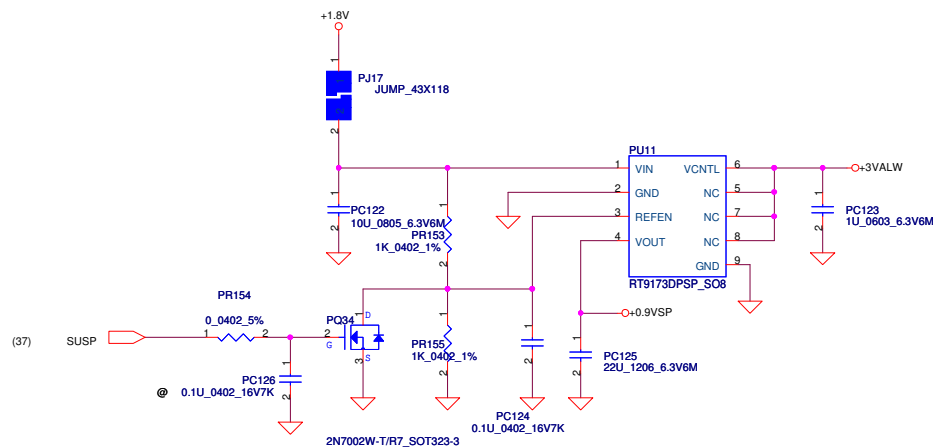
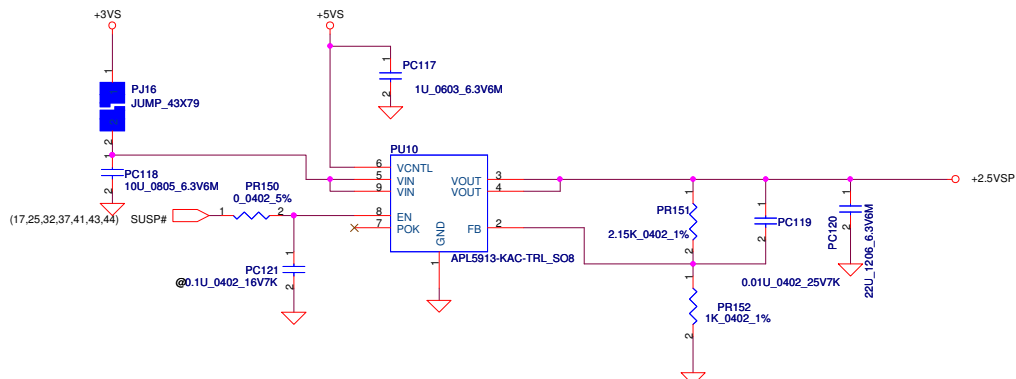
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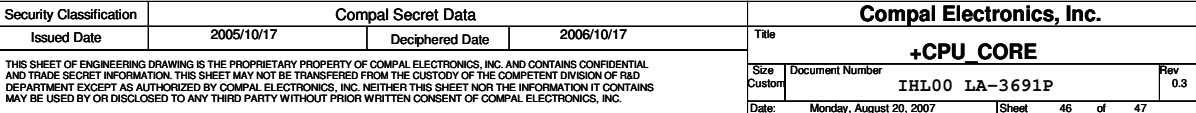


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