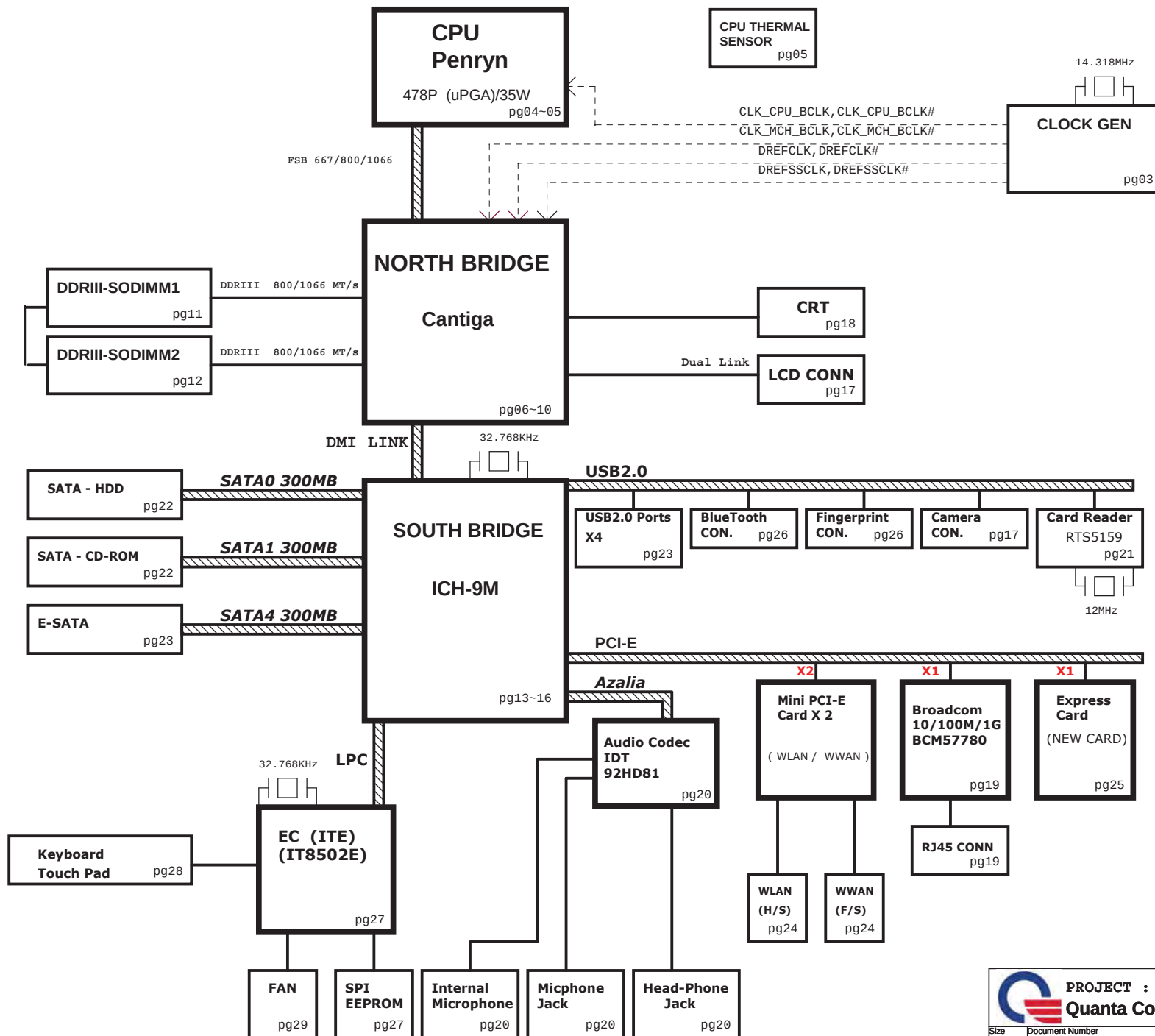
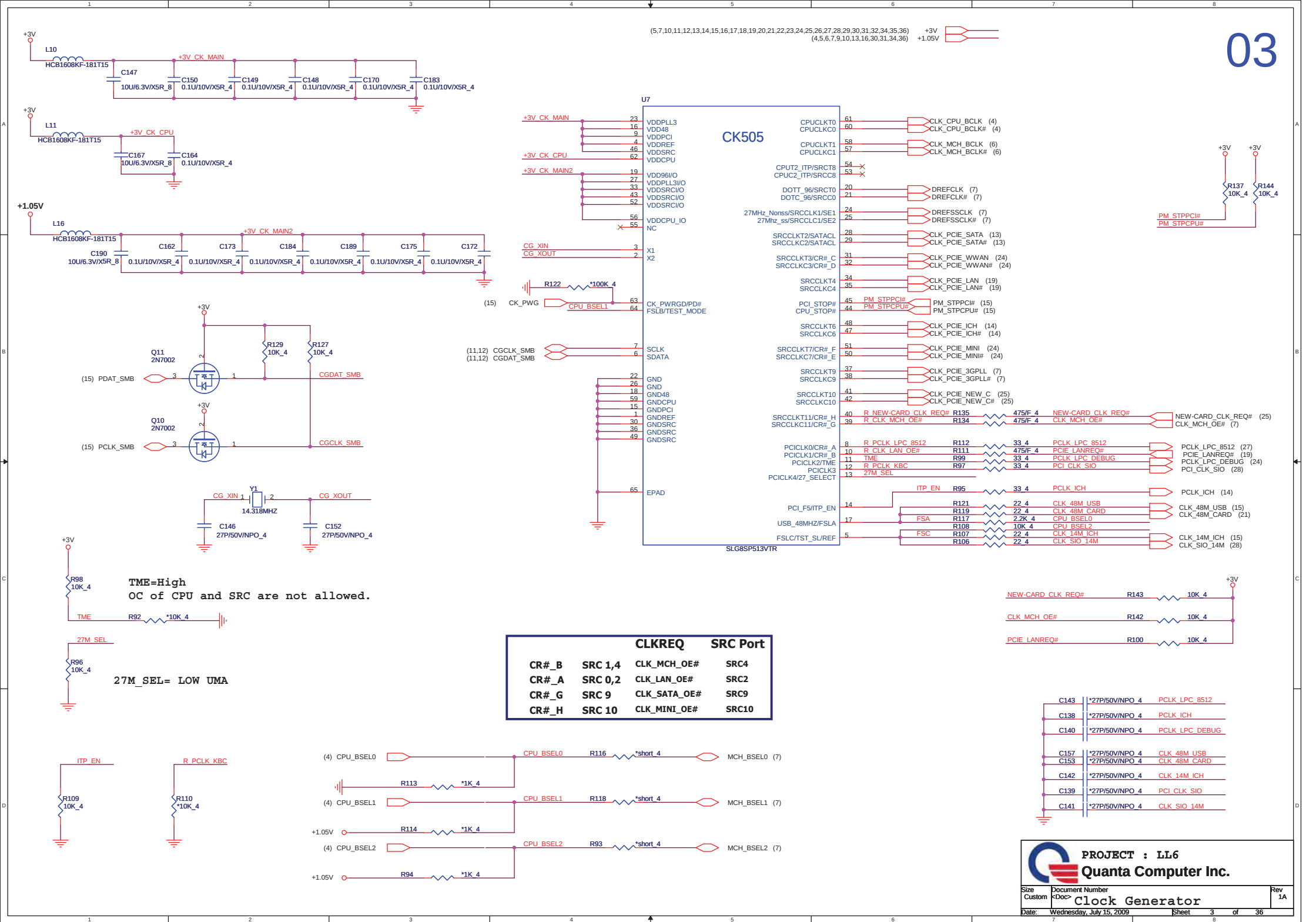


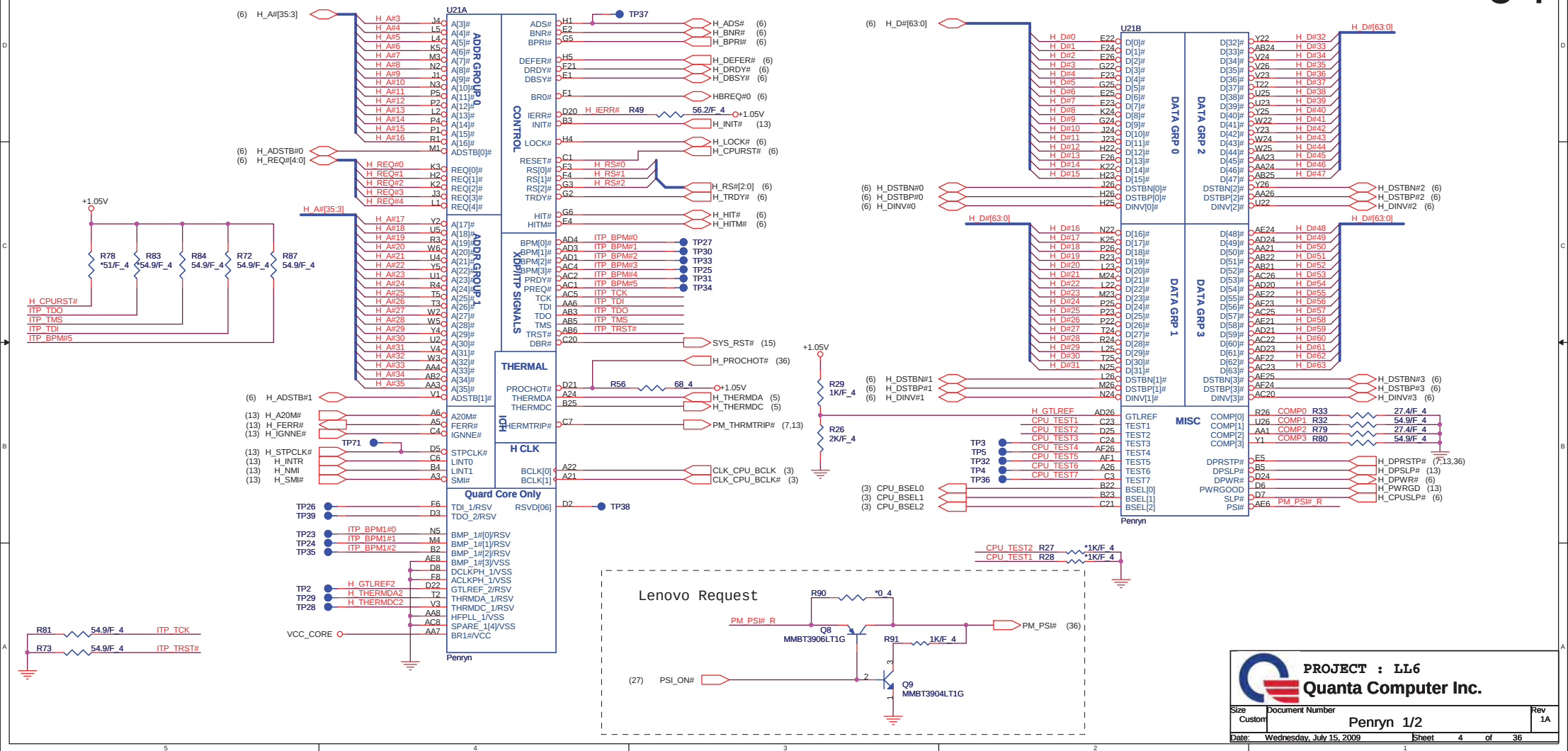
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+19V	18, 33, 34, 35, 36, 37, 38, 39	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	13, 16, 32	RTC		S0~S5
3VPCU	+3.3V	13, 18, 22, 24, 30, 32, 33, 34, 36, 37	8051 POWER		S0~S5
5VPCU	+5V	30, 33, 34, 35, 36, 37, 38	LCD/CHARGE POWER		S0~S5
+15V	+15V	18, 26, 33, 37	LARGE POWER	5VPCU	S0~S5
LANVCC	+3.3V	22, 33	LAN POWER	LAN_ON	
5VSUS	+5V	18, 30, 33, 38	SLP_S5# CTRLD POWER	SUSON	
3VSUS	+3.3V	14, 15, 27, 28, 29, 32, 33, 38	SLP_S5# CTRLD POWER	SUSON	
1.8VSUS	+1.8V	10, 33, 36		SUSON	
1.5VSUS	+1.5V	07, 09, 10, 11, 12, 33, 35	SODIMM POWER CALISTOGA/ICH8 POWER	SUSON	
SMDDR_VREF_DIMM	+0.75V	11, 12	SODIMM POWER		
+5V	+5V	16, 17, 18, 19, 21, 23, 24, 25, 32, 33, 34	SLP_S3# CTRLD POWER	MAINON	
+3V	+3.3V	03, 05, 07, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	SLP_S3# CTRLD POWER	MAINON	
+1.5V	+1.5V	05, 10, 13, 14, 15, 16, 21, 27, 28, 29, 35	CALISTOGA/ICH8 POWER	MAINON	
+1.05V	+1.05V	03, 04, 05, 06, 07, 09, 10, 13, 16, 33, 36, 38	CPU/CALISTOGA/ICH8 POWER	MAINON	
VCC_CORE	+0.7V~+1.77V	04, 05, 33, 38	CPU CORE POWER	VRON	
LCDVCC	+3.3V	18	LCD Power	INT_DISP_ON	
+5VHDD	+5V	23	HDD Power	MAINON	
MBATV	+10V~+17V	32, 34	MAIN BATTERY	D/C#	

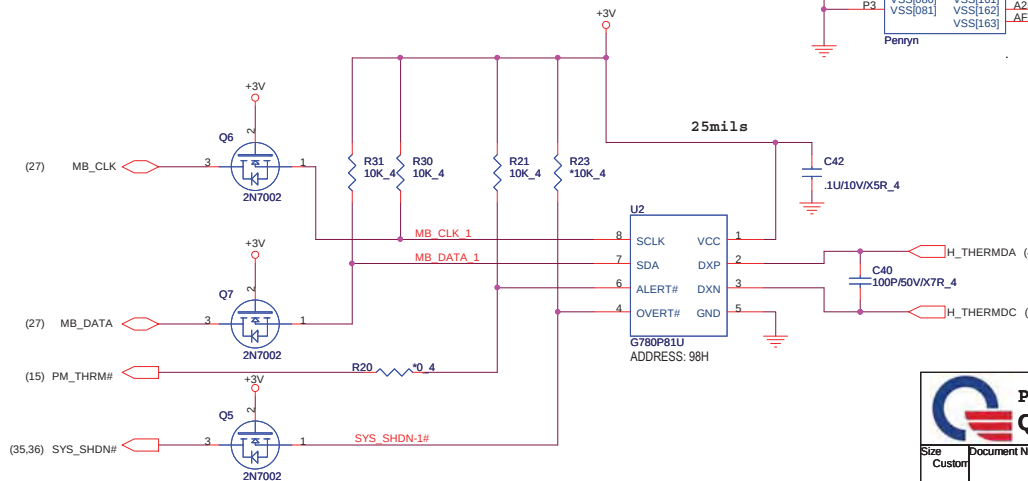
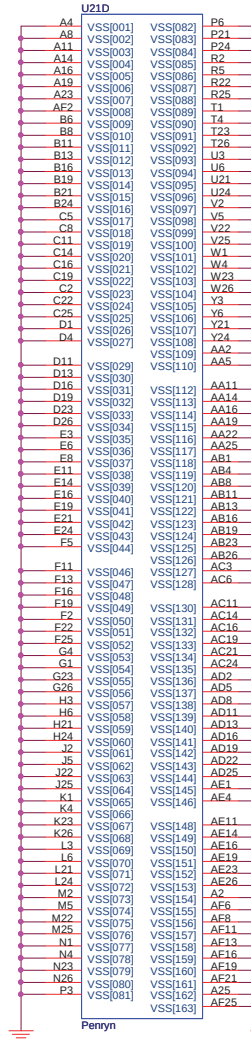
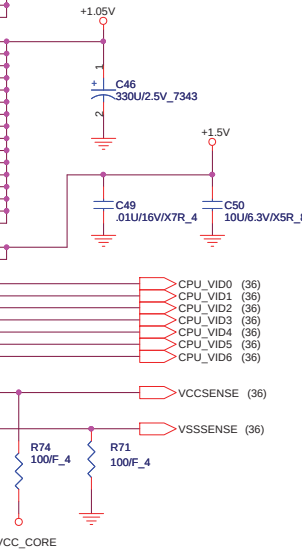
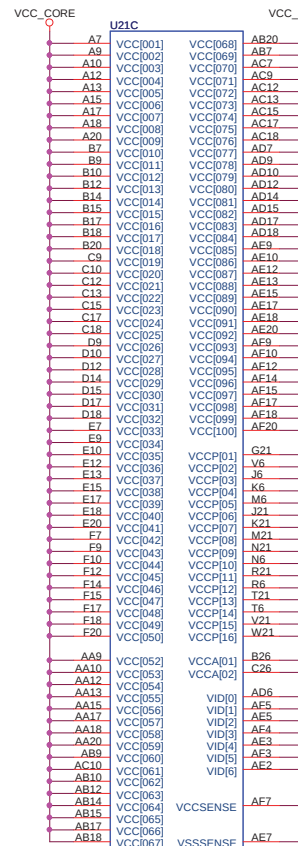
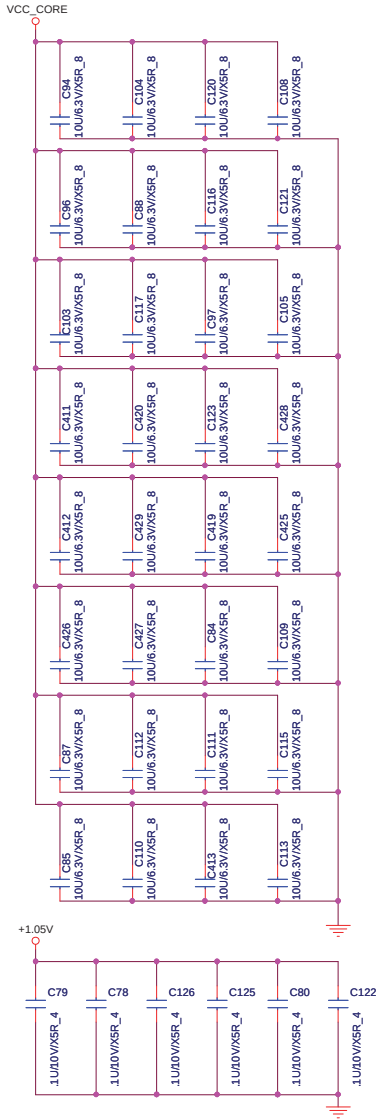


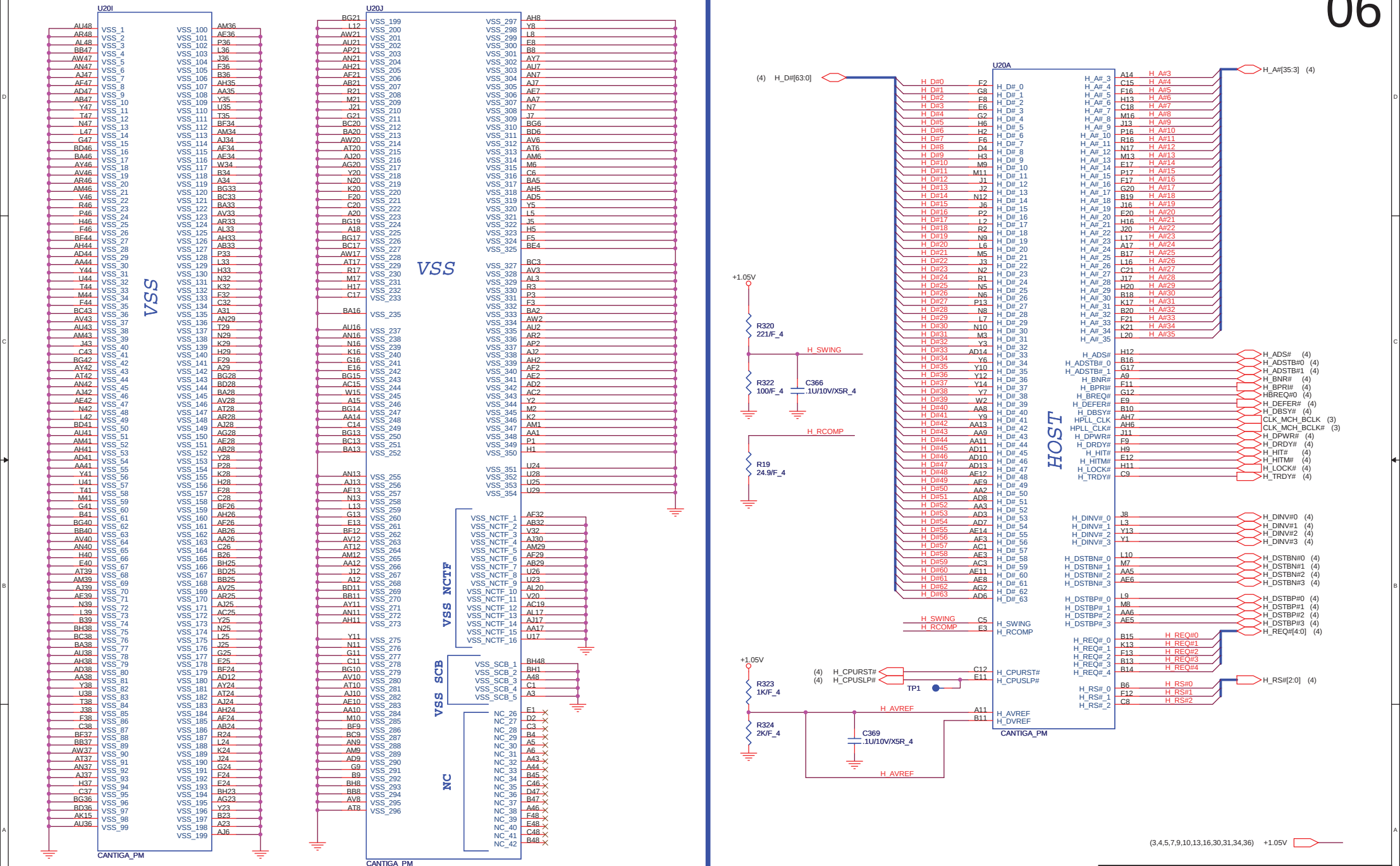


(3,7,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,36)
(3,4,6,7,9,10,13,16,30,31,34,36)
(10,13,14,16,24,25,33)
(4,31,36)

+3V
+1.05V
+1.5V
VCC_CORE

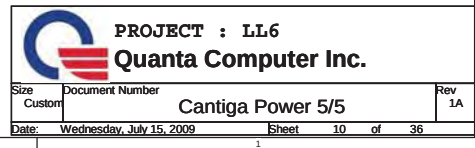
05

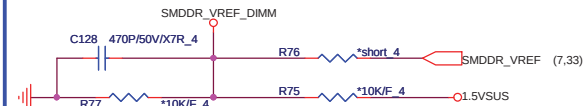
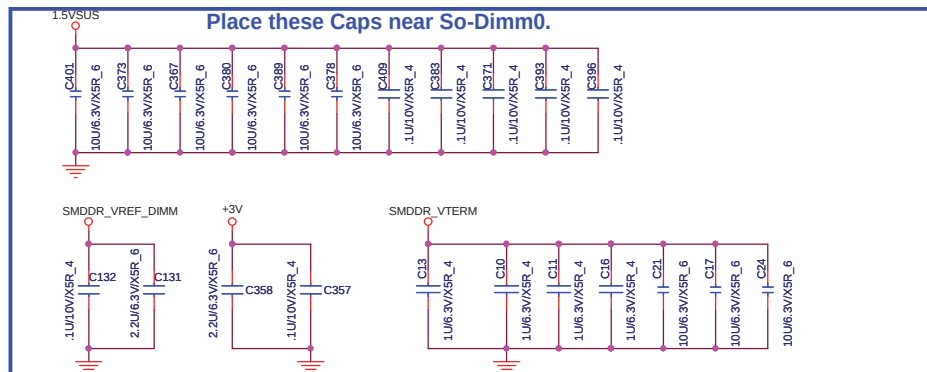
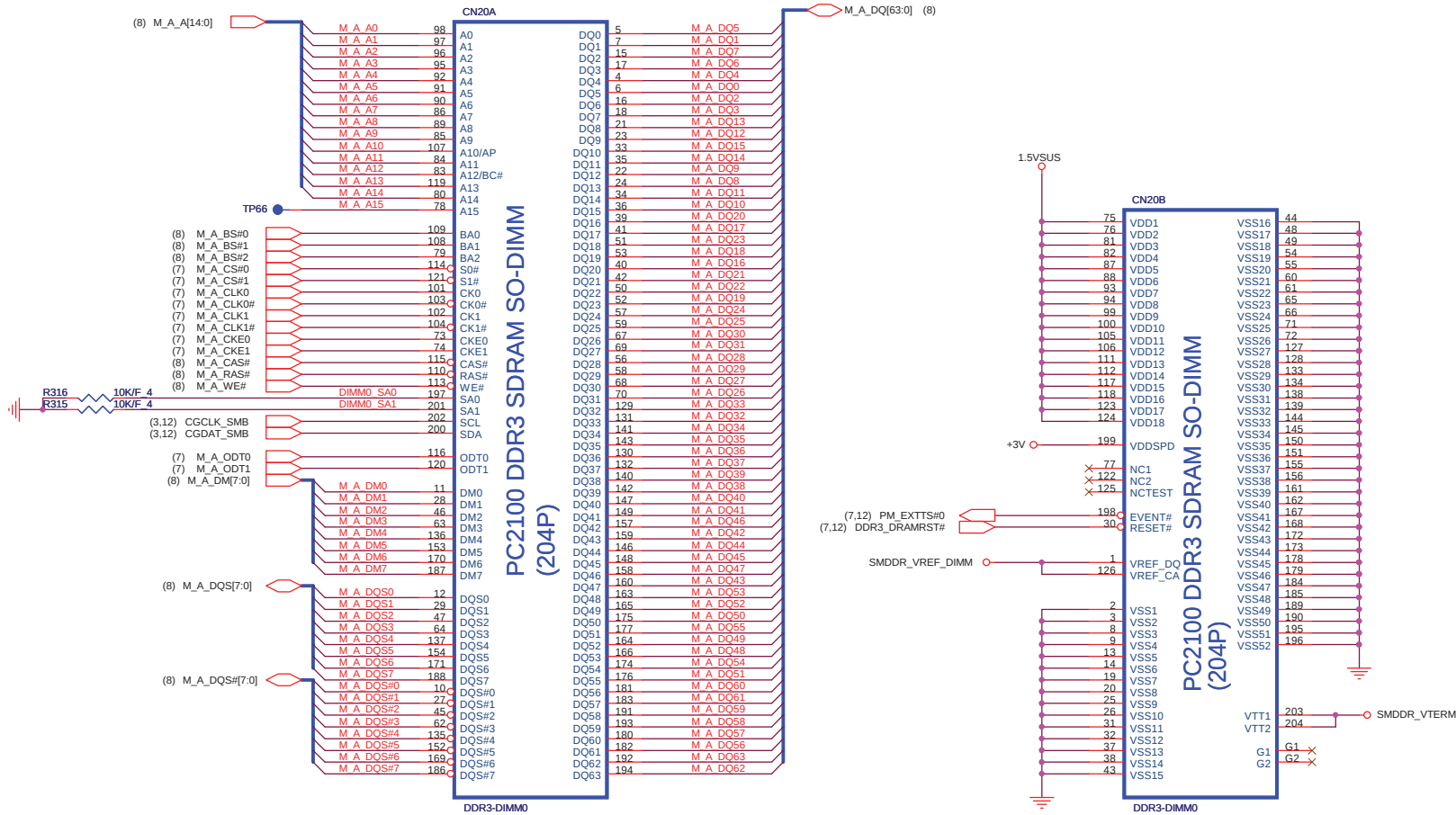


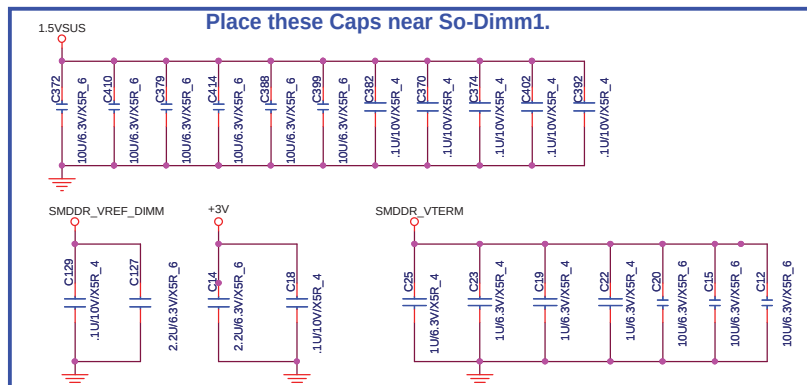
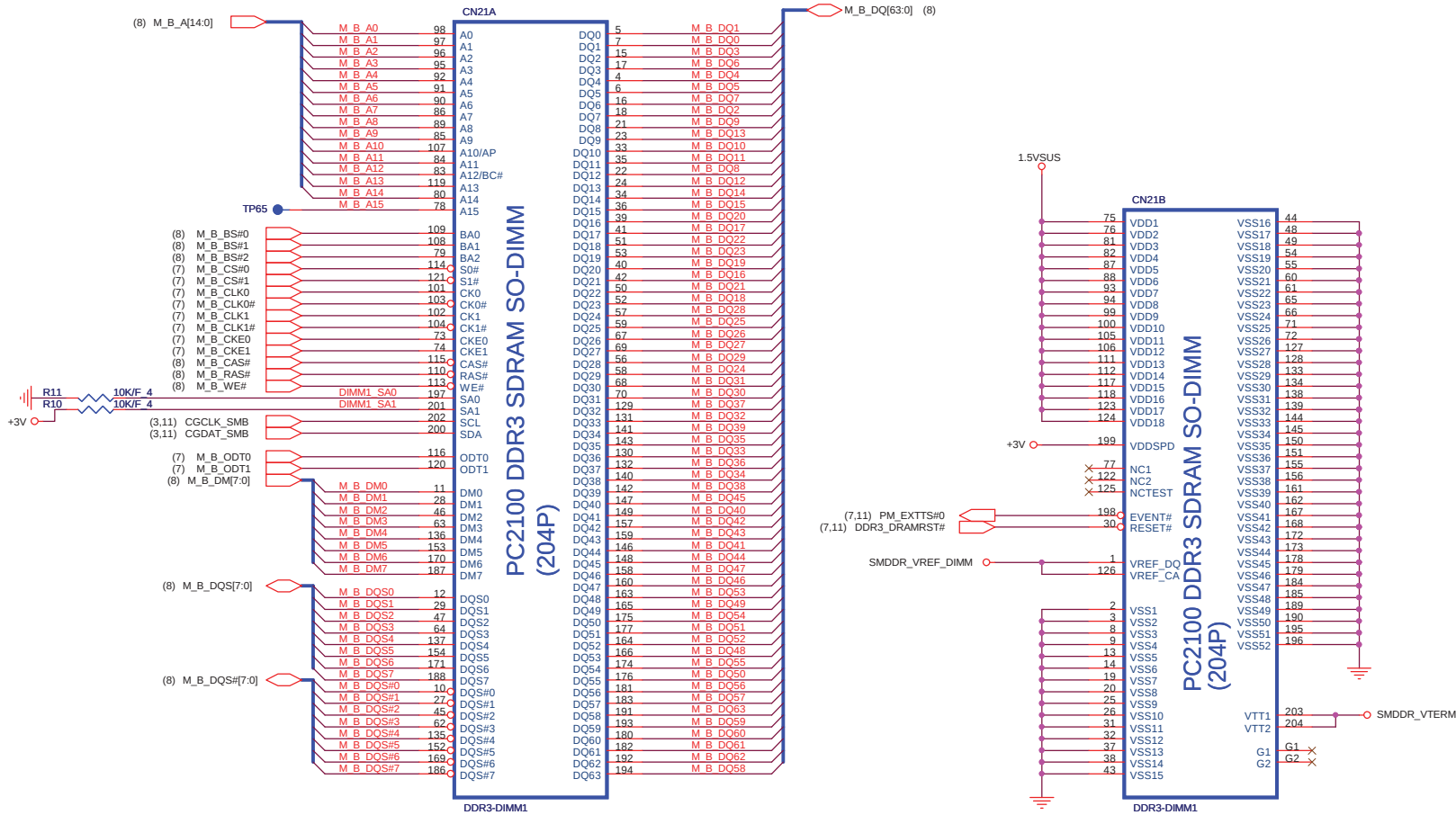


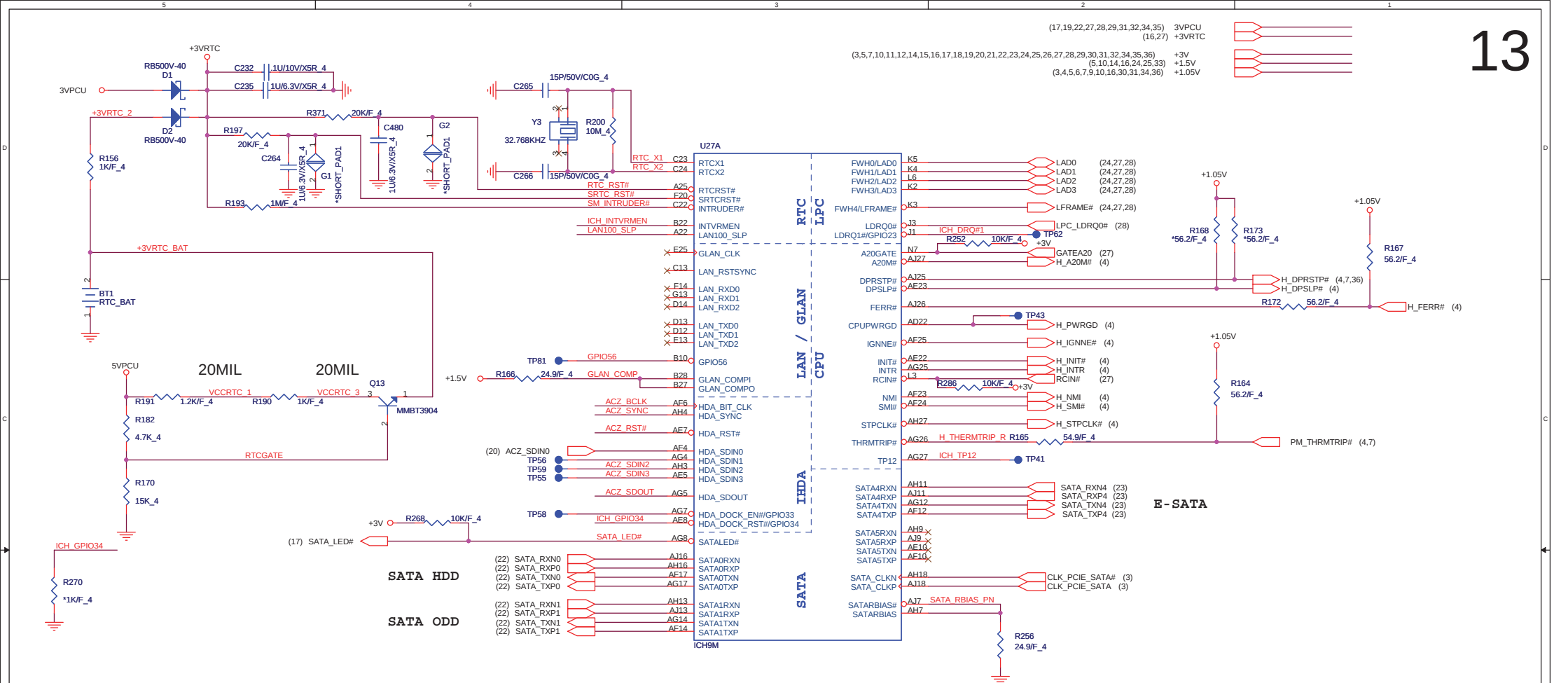
 PROJECT : LL6 Quanta Computer Inc.		
Size Custom	Document Number Cantiga DMI/DISP 2/5	Rev R0
Date: Wednesday, July 15, 2009	Sheet 7 of 36	











SB Strap

ICH9-M Internal VR
Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

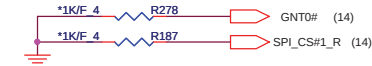
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

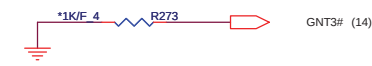
ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

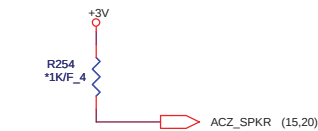
(default)



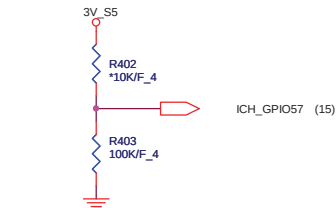
A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default



No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

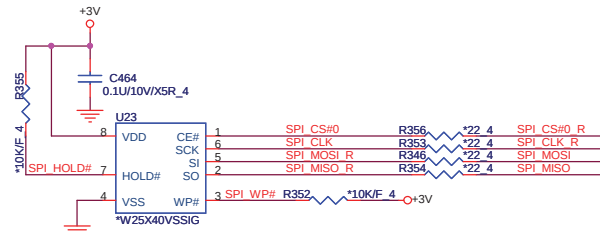
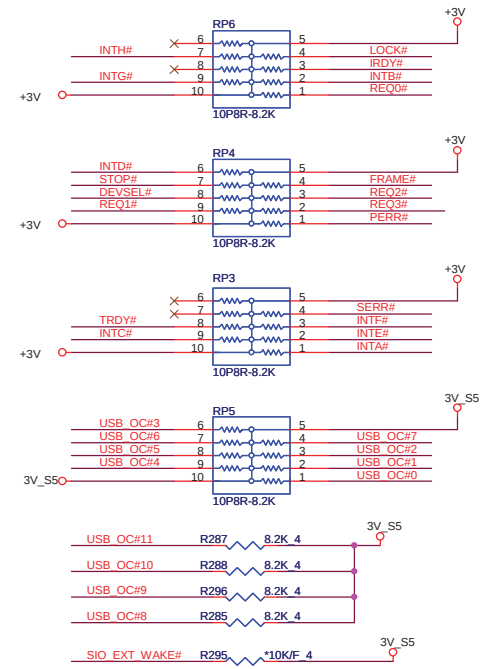


TPM physical presence	
ICH_GPIO57	Low: Default

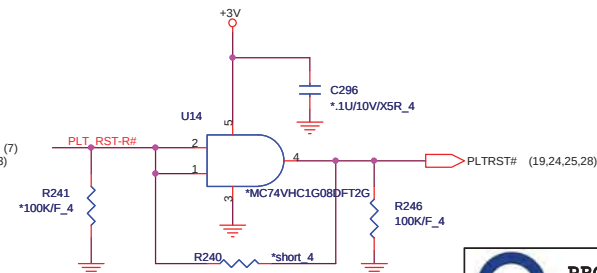
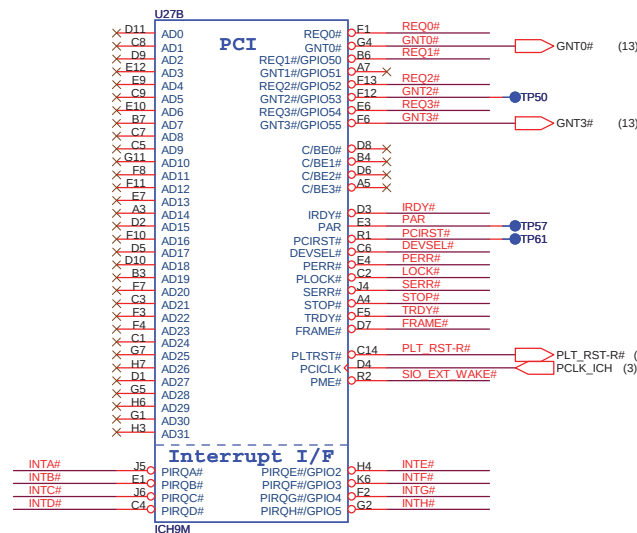


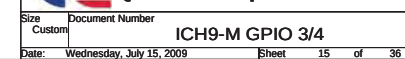
PCIE-LAN

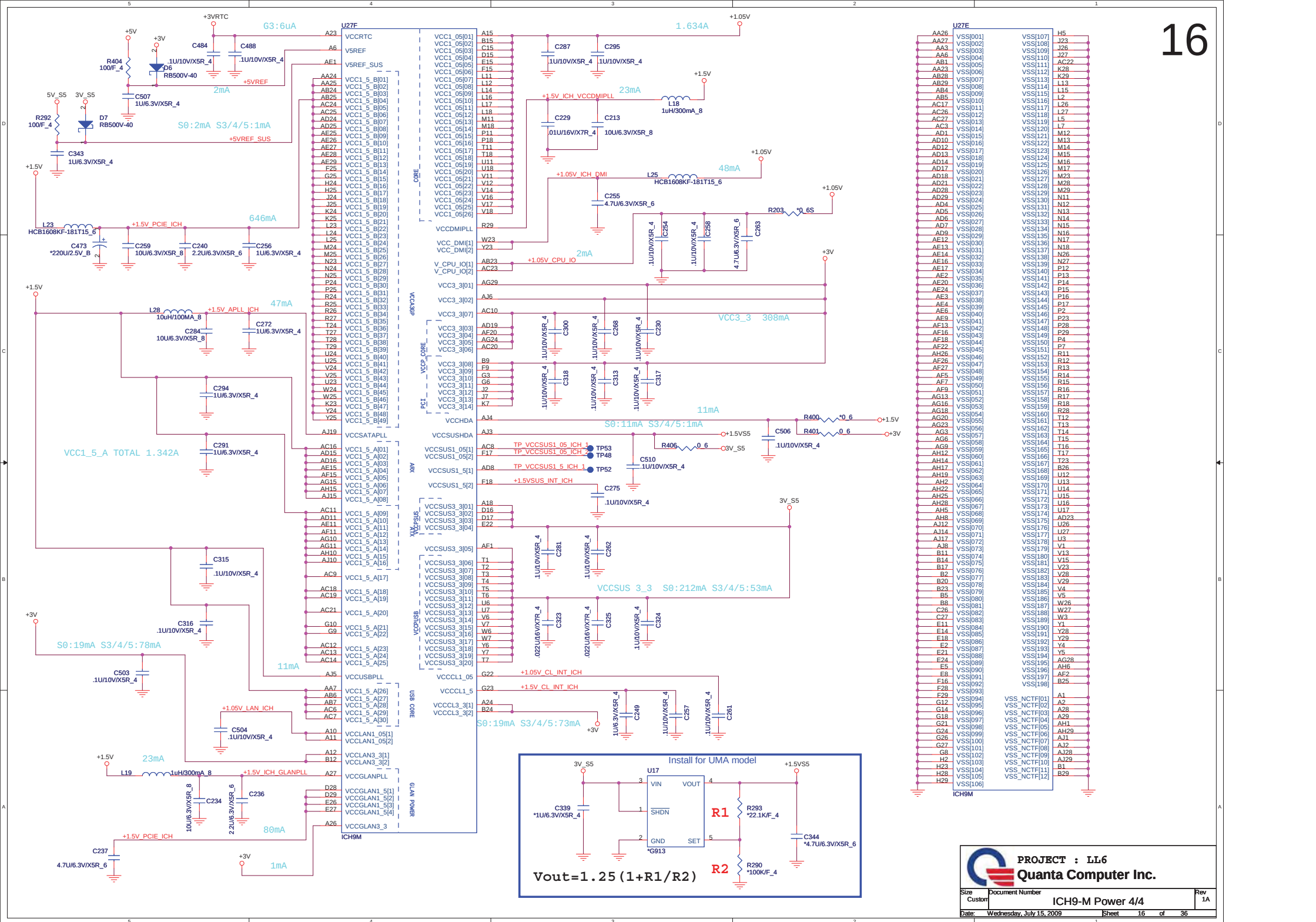
USB Connector 3
USB Connector 4
WLAN Min-Card
WWAN Min-Card



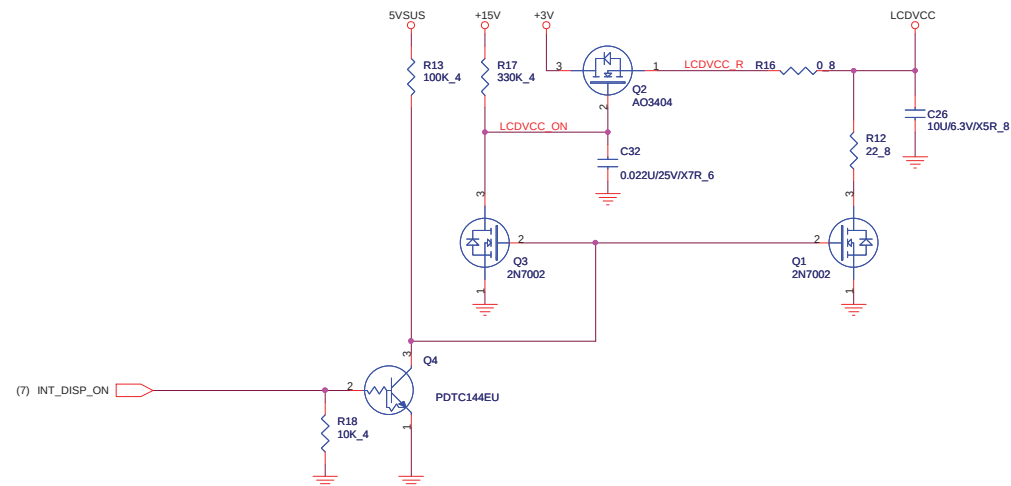
512K byte SPI ROM
For HDCP only



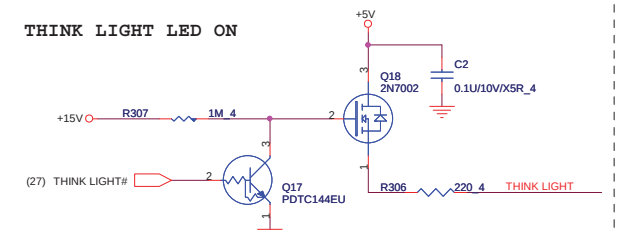
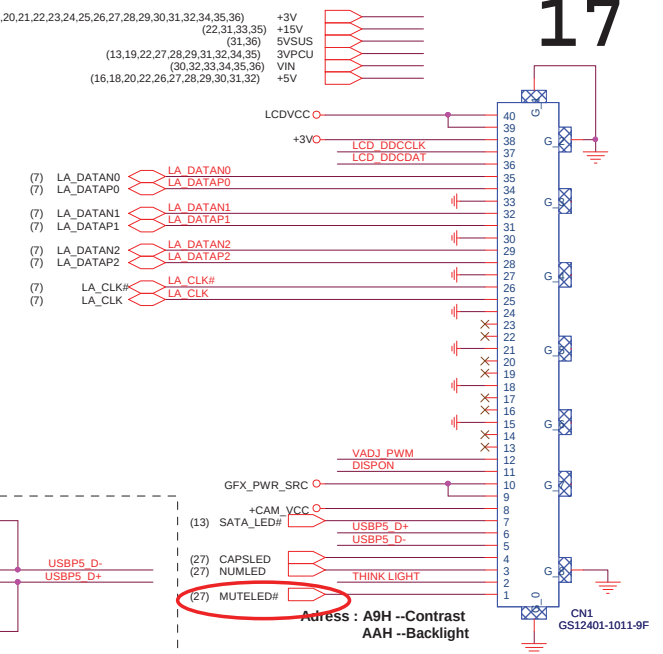
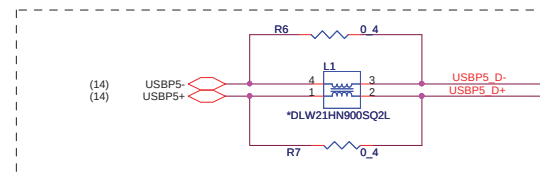
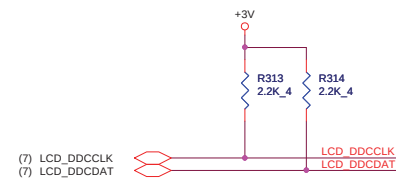
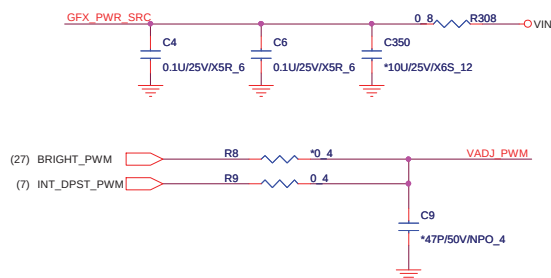
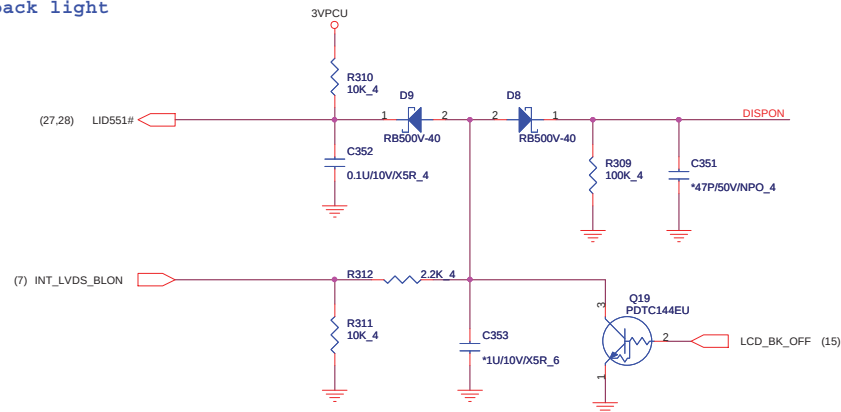




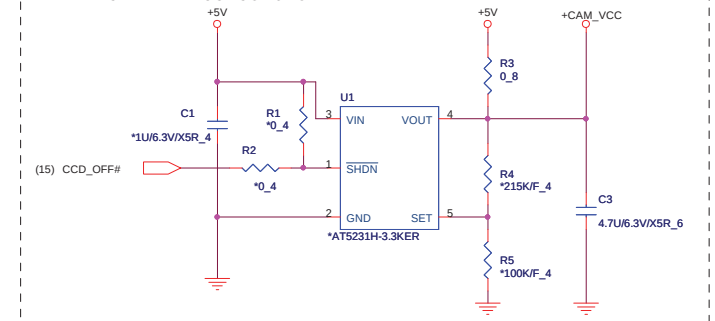
LCD panel control & connector



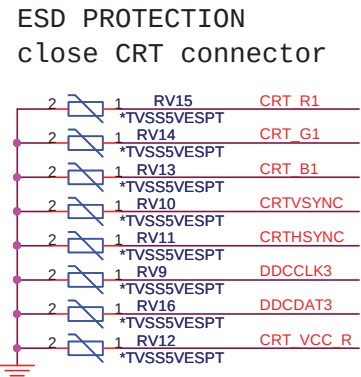
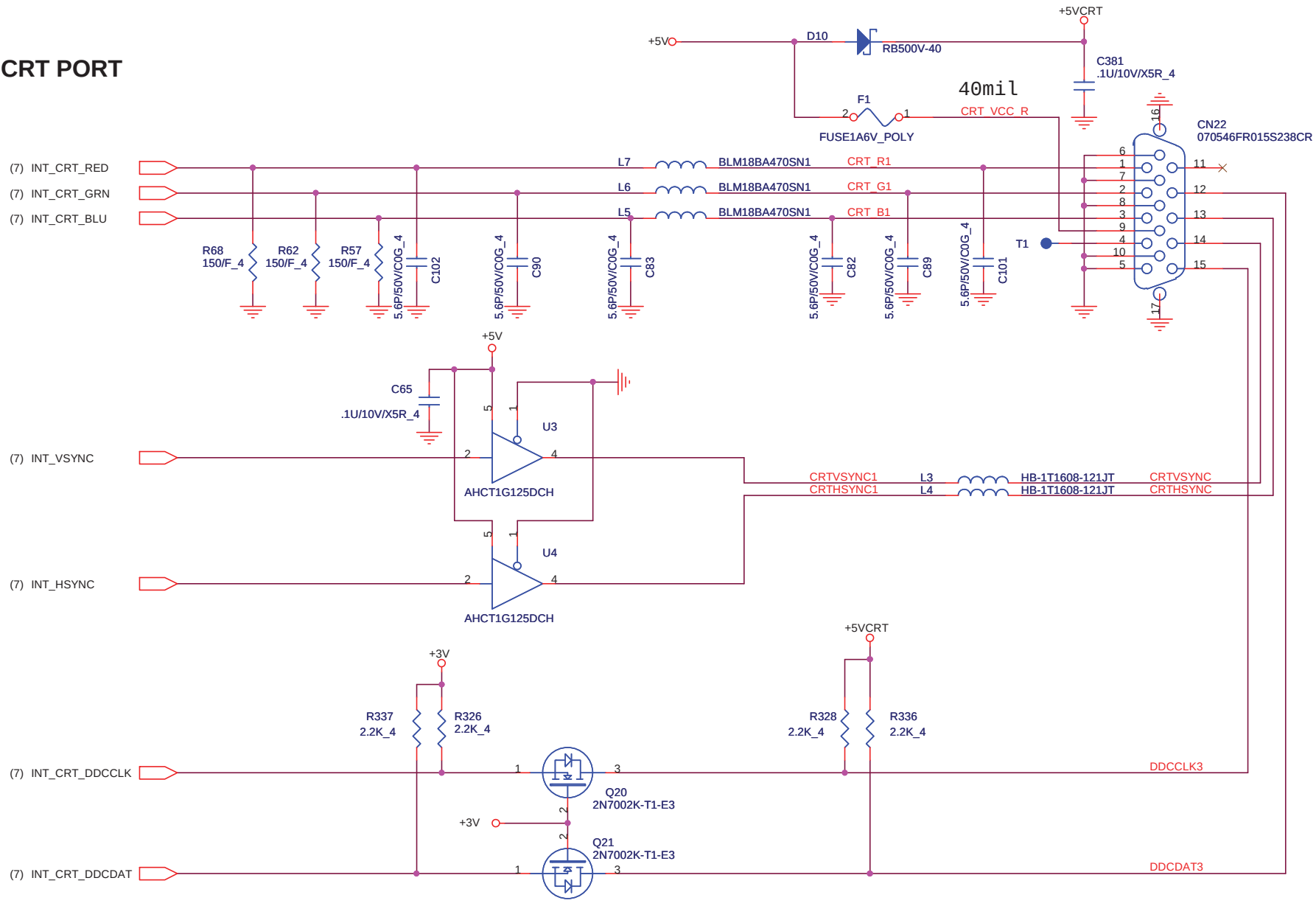
back light

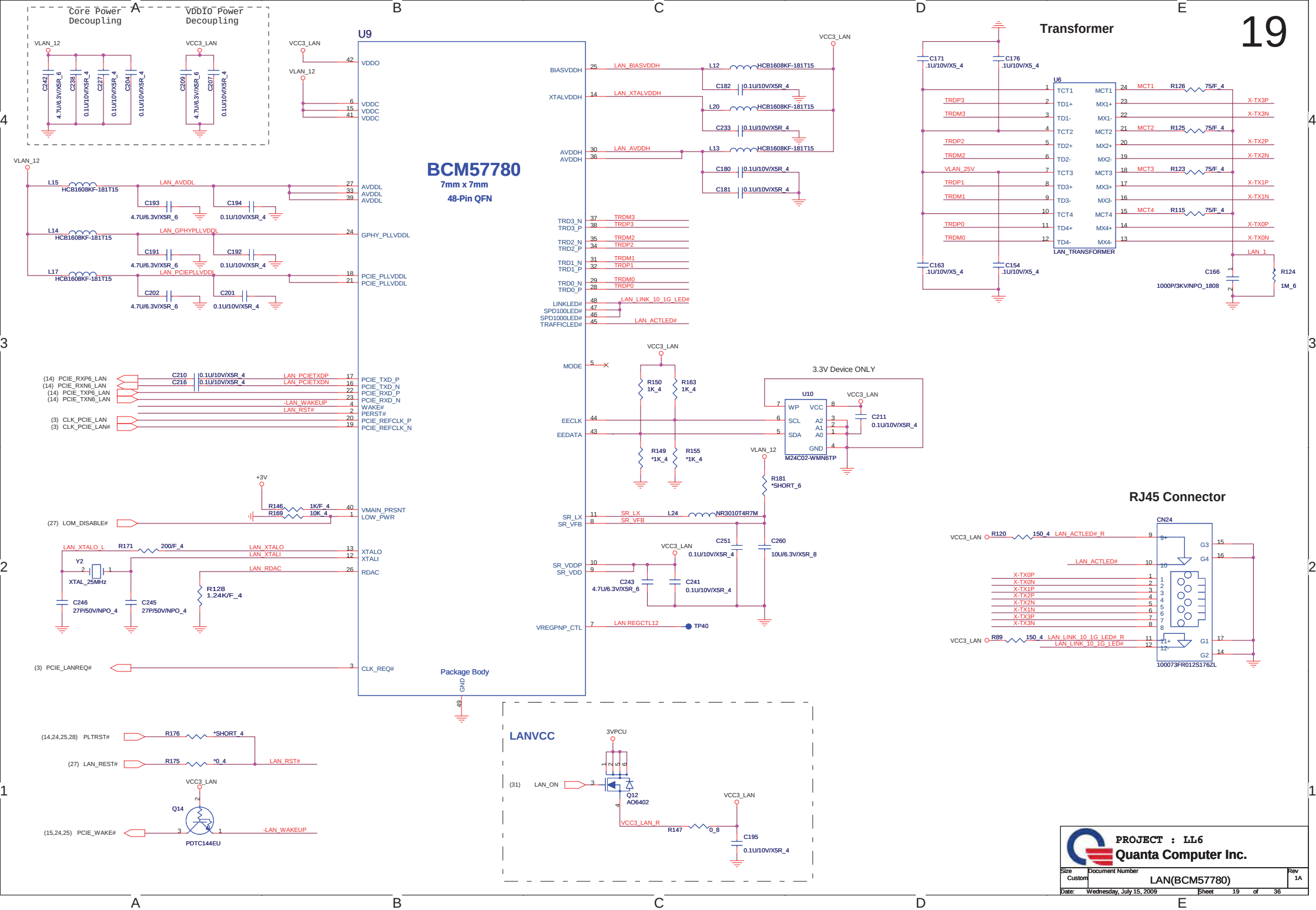


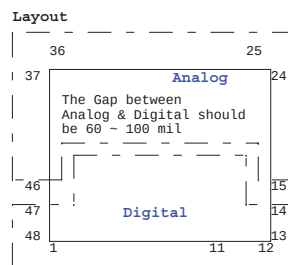
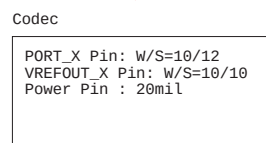
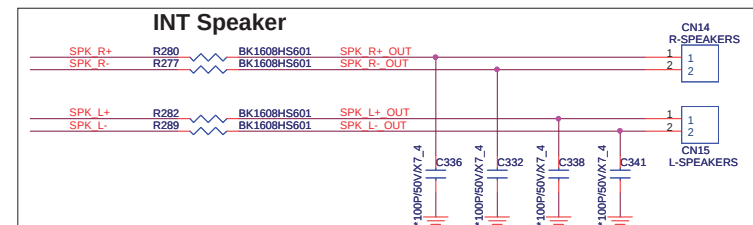
CAMERA VCC Control



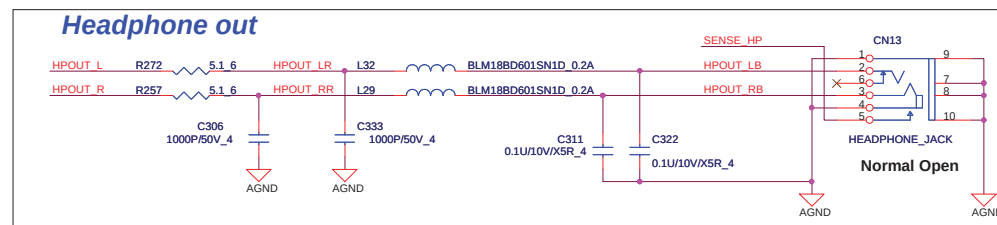
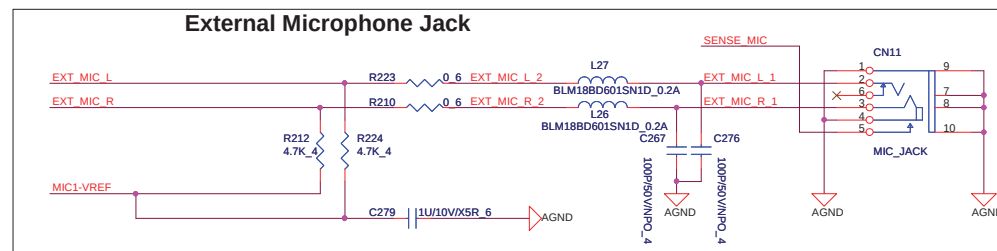
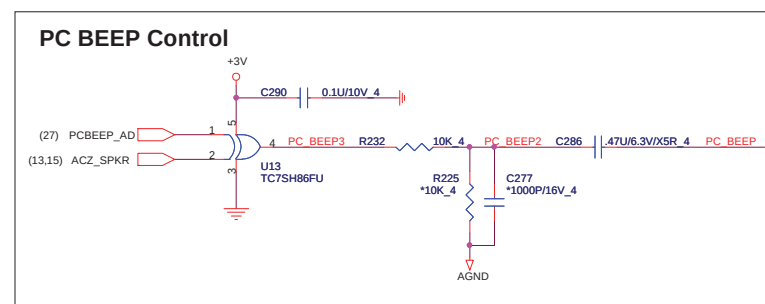
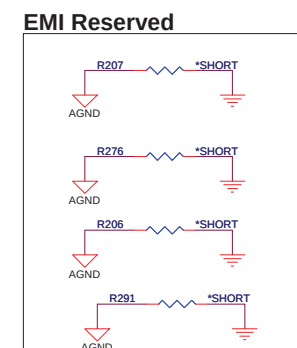
CRT PORT

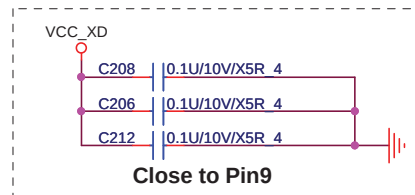






Sense_A	Sense_B	RES
Port_A	Port_E	39.2
Port_B	Port_F	20K





SD/MMC		MS	XD	
SP0				
SP1				
SP2	SD WP			XD CD#
SP3	SD CD#			
SP4	SD DAT1			
SP5		MS BS		XD D4
SP6		MS D1		XD D5
SP7	SD DAT0	MS D0		XD D3
SP8	SD DAT7	MS D2		XD D6
SP9		MS INS#		XD D2
SP10	SD DAT6	MS D3		XD D7
SP11	SD CLK	MS SCLK		XD D1
SP12	SD DAT5			XD D0
SP13	SD DAT4			XD WP#
SP14				XD R/B#
SP15	SD DAT3			XD WE#
SP16	SD DAT2			XD RE#
SP17				XD ALE
SP18				XD CE#
SP19				XD CLE

The diagram shows eight signals (SP7, SP6, SP16, SP5, SP15, SP11, SP10, SP4) with their respective timing traces and labels. Each signal has two traces (R360/R359, R361/R362, R347/R351, R364/R363, R348/R349, R162/R161, R158/R159, R367/R368) and associated labels (MS_DATA0, SD_DATA0, XD-D6, MS_DATA1, XD-D3, SD_DAT2, XD-RE#, MS_BS, XD-D5, SD_DAT3, XD_WE, SD_CLK, MS_CLK, XD-D1, MS_DATA3, XD-D7, XD-D4, SD_DAT1).

SD CARD

SD CARD	Connector	Signal
1	20	MS-10-VSS
2	21	SD-9-DAT2
3	22	SD-8-DAT1
4	23	XD-18-VCC
5	24	XD-17-D7
6	25	XD-16-D6
7	26	XD-15-D5
8	27	XD-14-D4
9	28	XD-13-D3
10	29	XD-12-D2
11	30	XD-11-D1
12	31	XD-10-D0
13	32	XD-9-GND
14	33	XD-8-WP#
15	34	XD-7-WE
16	35	XD-6-ALE
17	36	XD-5-CLE
18	37	XD-4-CE
19	38	XD-3-RE
	39	XD-2-R/B
	40	XD-1-CD
	41	SD-CD/WP GND1
	42	SD-CD/WP GND2

SD CARD

SD-CD
SD-WP
SD-DAT1
MS-DATA0 SD-DAT0
MS-BS
MS-DATA1
SD-CLK MS-CLK
MS-DATA0 SD-DAT0
MS-DATA2 XD-D2
MS-CD#
MS-DATA3
SD-CMD
SD-CLK MS-CLK
SD-DAT3

Connector

20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42

Signal

MS-10-VSS
SD-9-DAT2
SD-8-DAT1
XD-18-VCC
XD-17-D7
XD-16-D6
XD-15-D5
XD-14-D4
XD-13-D3
XD-12-D2
XD-11-D1
XD-10-D0
XD-9-GND
XD-8-WP#
XD-7-WE
XD-6-ALE
XD-5-CLE
XD-4-CE
XD-3-RE
XD-2-R/B
XD-1-CD
SD-CD/WP GND1
SD-CD/WP GND2

Other Labels

C231
*33P/25V_4
VCC_XD
C185
C228
270P/50V/X7R 4
270P/50V/X7R 4
C515
R409
VCC_XD
C481
C479
C483

144-1300302600-42p

C515 4.7U/6.3V/X5R 6
R409 150K/F 4

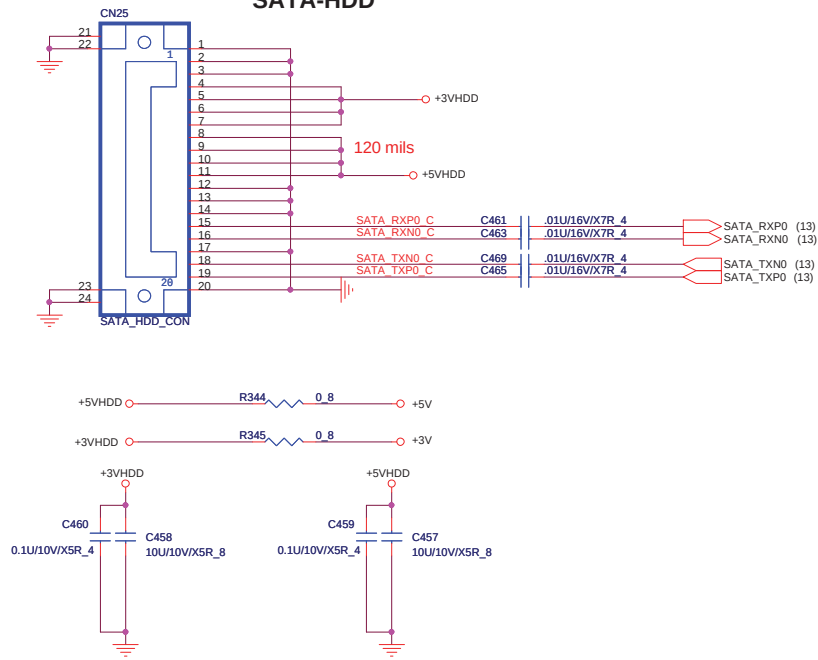
VCC_XD

C481	0.1U/10V/X5R 4
C479	0.1U/10V/X5R 4
C483	0.1U/10V/X5R 4

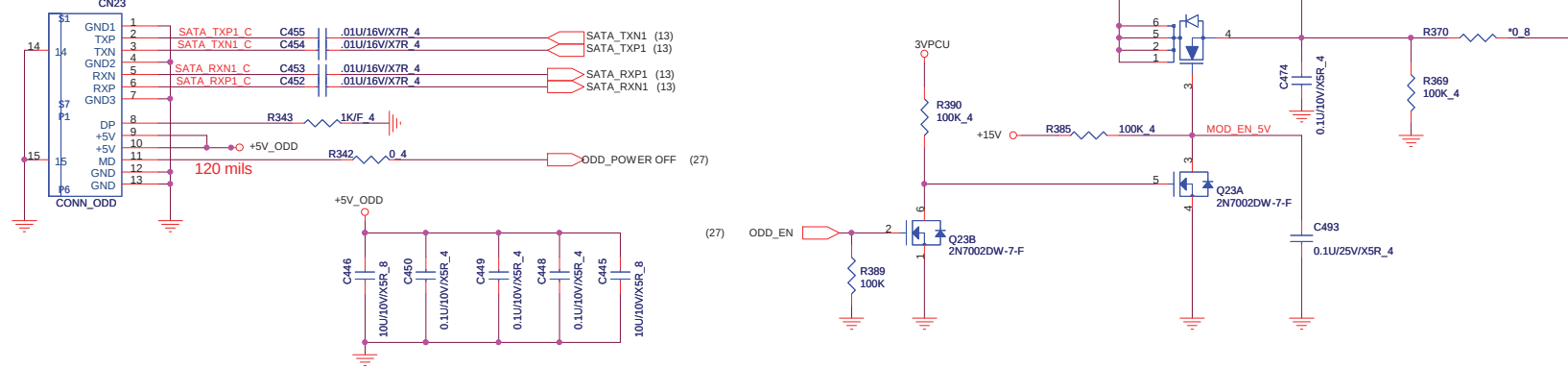
 PROJECT : LL6
Quanta Computer Inc.

Size Custom	Document Number Card Reader (RTS5159)	Rev 1A
Date:	Wednesday, July 15, 2009	Sheet 21 of 36

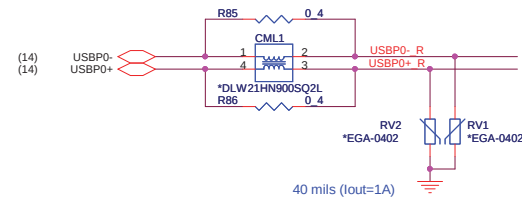
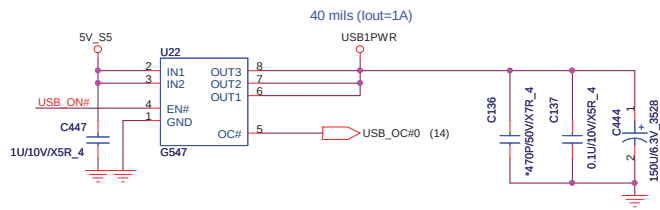
SATA-HDD



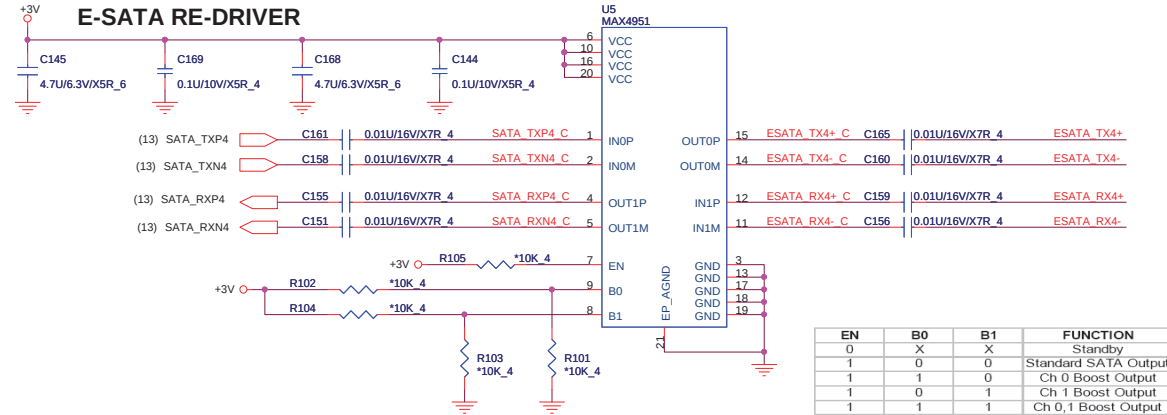
SATA ODD



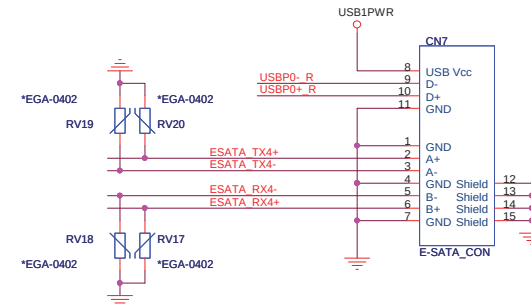
USB 1



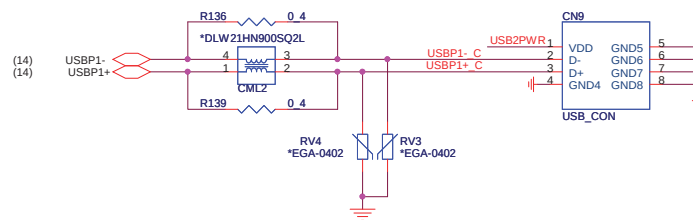
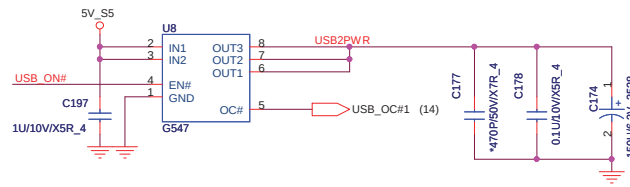
E-SATA RE-DRIVER



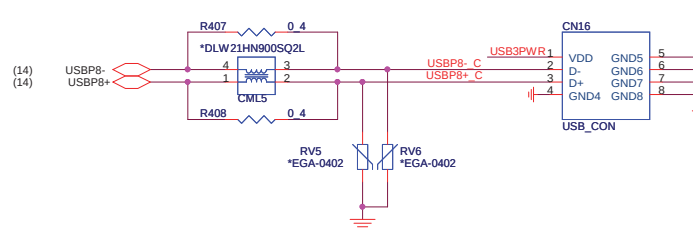
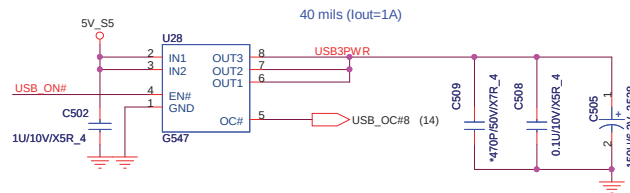
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



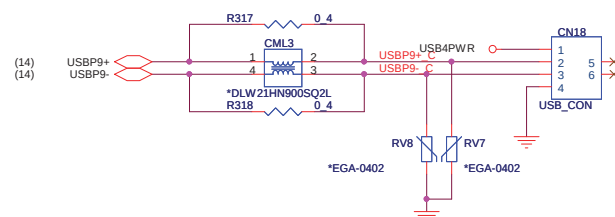
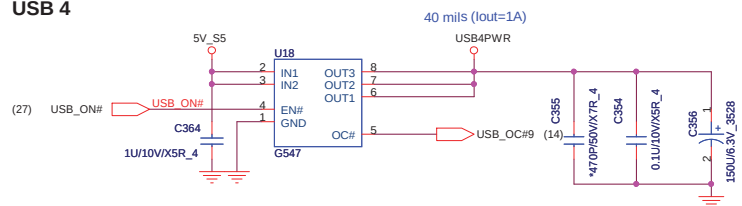
USB 2



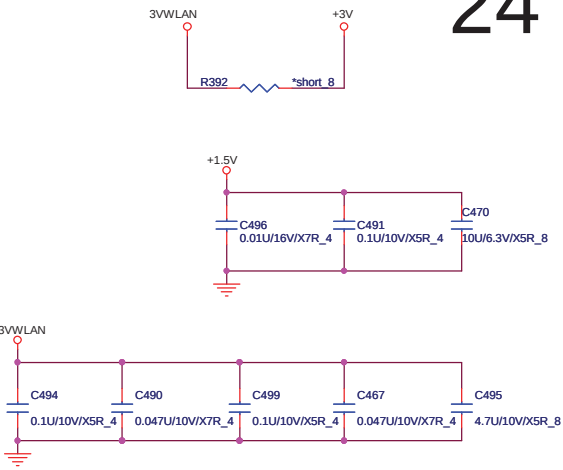
USB 3



USB 4



24



ACS-89911-5204

Pin 1: WAKE#

Pin 2: 3.3V_1

Pin 3: RESERVED_1

Pin 4: GND0

Pin 5: RESERVED_2

Pin 6: 1.5V_1

Pin 7: CLKREQ#

Pin 8: UIM_PWR

Pin 9: GND1

Pin 10: UIM_DATA

Pin 11: REFCLK-

Pin 12: UIM_CLK

Pin 13: REFCLK+

Pin 14: UIM_RESET

Pin 15: GND2

Pin 16: UIM_VPP

Pin 17: UIM_C8

Pin 18: GND3

Pin 19: UIM_C4

Pin 20: W_DISABLE#

Pin 21: PERST#

Pin 22: PERn0

Pin 23: 3.3VAUX1

Pin 24: GND5

Pin 25: PERp0

Pin 26: GND6

Pin 27: 1.5V_2

Pin 28: SMB_CLK

Pin 29: SMB_DATA

Pin 30: GND7

Pin 31: PETn0

Pin 32: SMB_Z

Pin 33: PETp0

Pin 34: GND8

Pin 35: GND9

Pin 36: USB_D-

Pin 37: RESERVED_3

Pin 38: USB_D+

Pin 39: RESERVED_4

Pin 40: GND10

Pin 41: RESERVED_5

Pin 42: LED_WWAN#

Pin 43: RESERVED_6

Pin 44: LED_WLAN#

Pin 45: RESERVED_7

Pin 46: LED_WPAN#

Pin 47: RESERVED_8

Pin 48: 1.5V_3

Pin 49: RESERVED_9

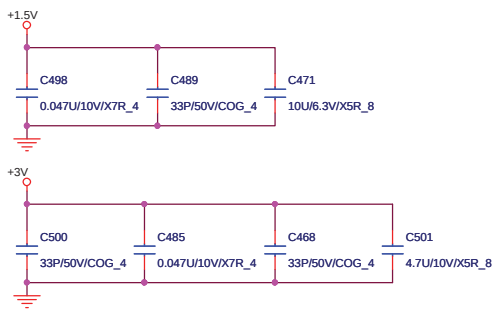
Pin 50: GND11

Pin 51: RESERVED_10

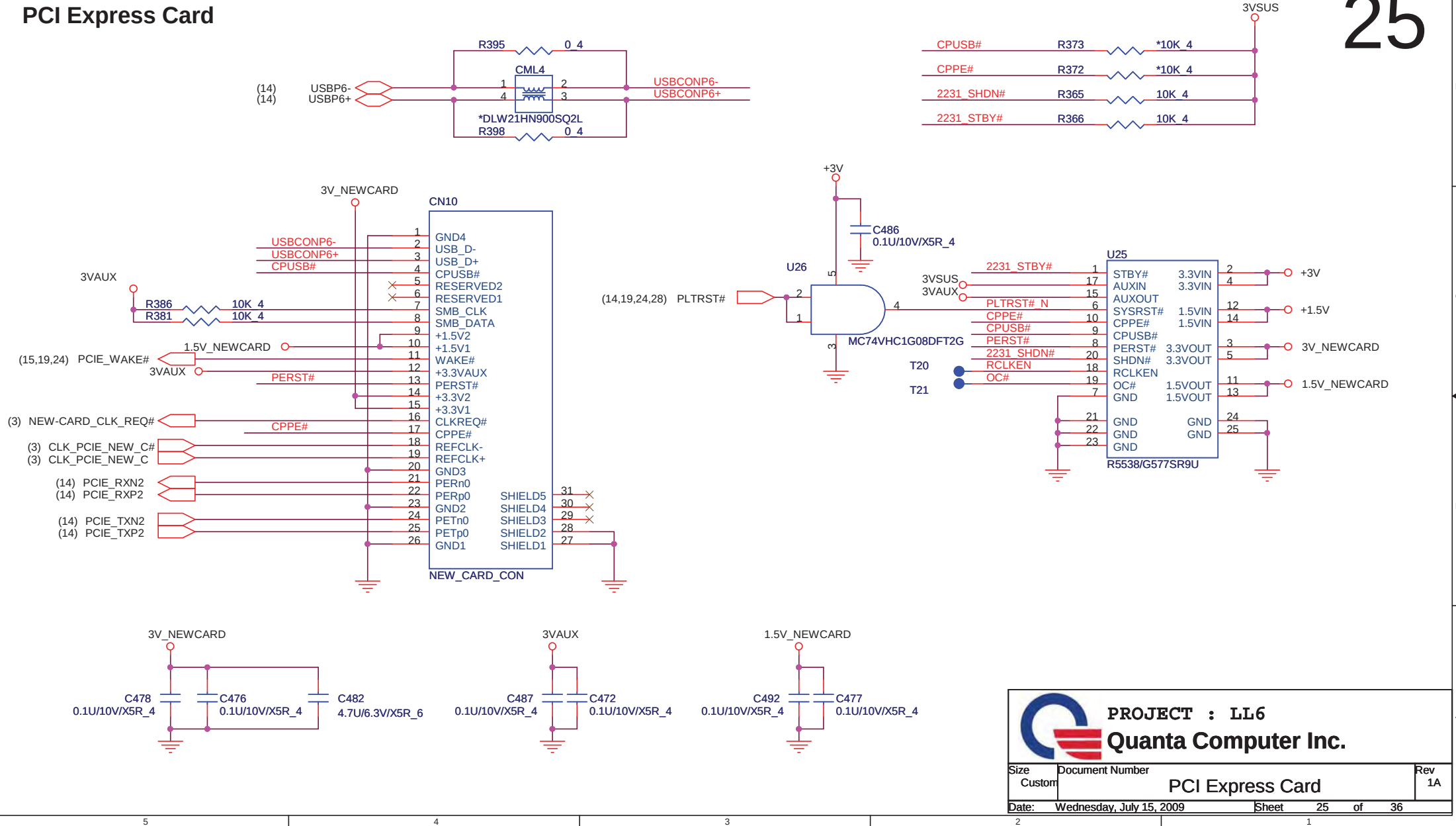
Pin 52: 3.3V_2

Connections:

- Power:** +3V, +1.5V, GND
- Control:** WAKE#, CLKREQ#, PERST#, PERn0, PERp0, PETn0, PETp0, USB_D-, USB_D+, LED_WWAN#, LED_WLAN#, LED_WPAN#
- Data:** UIM_DATA, UIM_CLK, UIM_RESET, UIM_VPP, UIM_C8, UIM_C4, UIM_C9, UIM_C10, UIM_C11, UIM_C12, UIM_C13, UIM_C14, UIM_C15, UIM_C16, UIM_C17, UIM_C18, UIM_C19, UIM_C20, UIM_C21, UIM_C22, UIM_C23, UIM_C24, UIM_C25, UIM_C26, UIM_C27, UIM_C28, UIM_C29, UIM_C30, UIM_C31, UIM_C32, UIM_C33, UIM_C34, UIM_C35, UIM_C36, UIM_C37, UIM_C38, UIM_C39, UIM_C40, UIM_C41, UIM_C42, UIM_C43, UIM_C44, UIM_C45, UIM_C46, UIM_C47, UIM_C48, UIM_C49, UIM_C50, UIM_C51, UIM_C52
- Other:** WWAN_CLKREQ#, CLK_PCIE_WWAN#, CLK_PCIE_WWAN#, PCIE_RXN5, PCIE_RXP5, PCIE_TXN5, PCIE_TXP5, WWAN_OFF#, PLTRST#, USBP11-, USBP11+, WWAN_WLAN_LED#, WWAN_WLAN_LED#



PCI Express Card



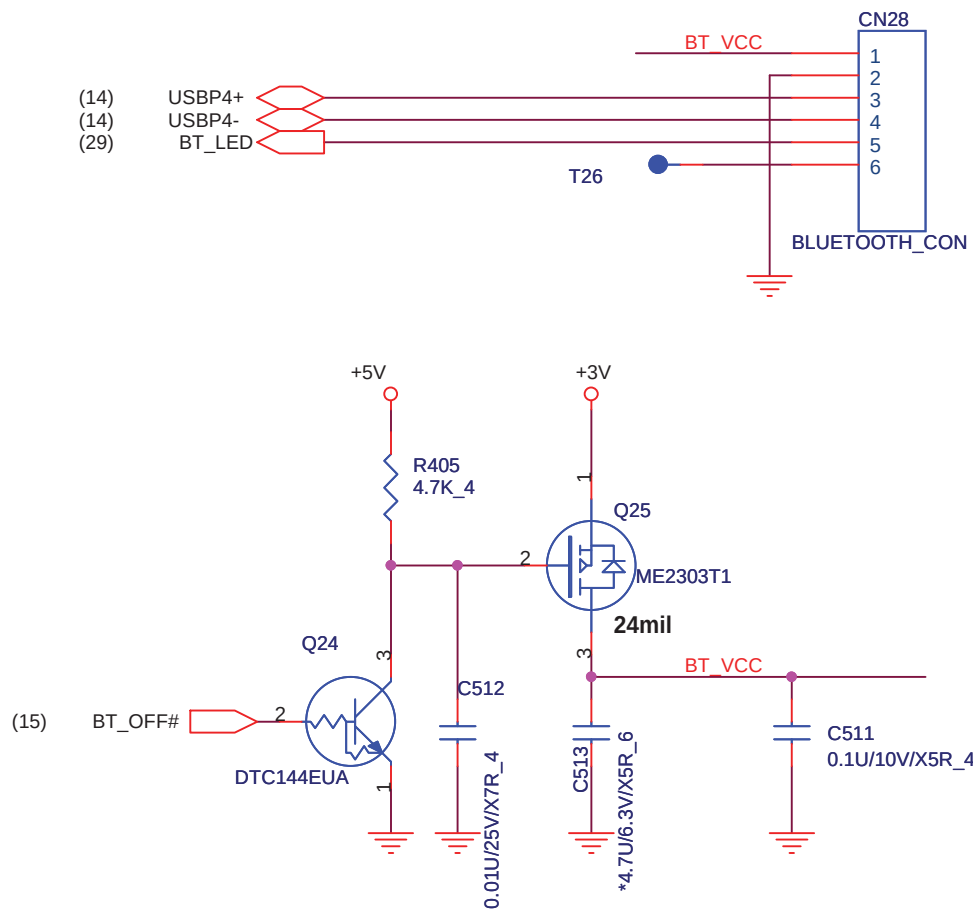


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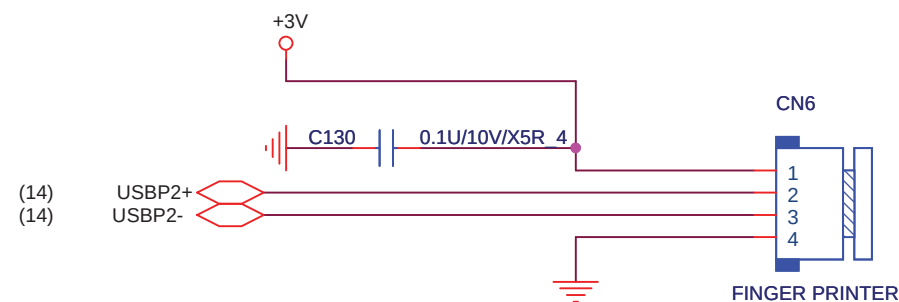
Quanta Computer Inc.

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Custom	PCI Express Card	1A
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BLUETOOTH

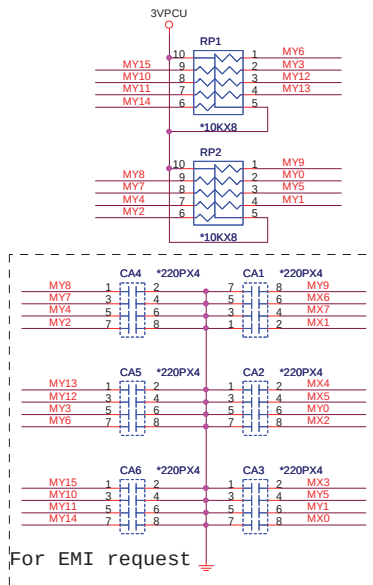


FINGER PRINTER



Input Channel	Output Channel
M1	MY1
M2	MY2
M3	MY3
M4	MY4
M5	MY5
M6	MY6
M7	MY7
M8	MY8
M9	MY9
M10	MY10
M11	MY11
M12	MY12
M13	MY13
M14	MY14
M15	MY15
M16	MY16
M17	MY17
M18	MY18
M19	MY19
M20	MY20
M21	MY21
M22	MY22
M23	MY23
M24	MY24
M25	MY25
M26	MY26
M27	MY27

KB-COIN (85201-24051)



The diagram shows the CPU connector (CN3) with the following connections:

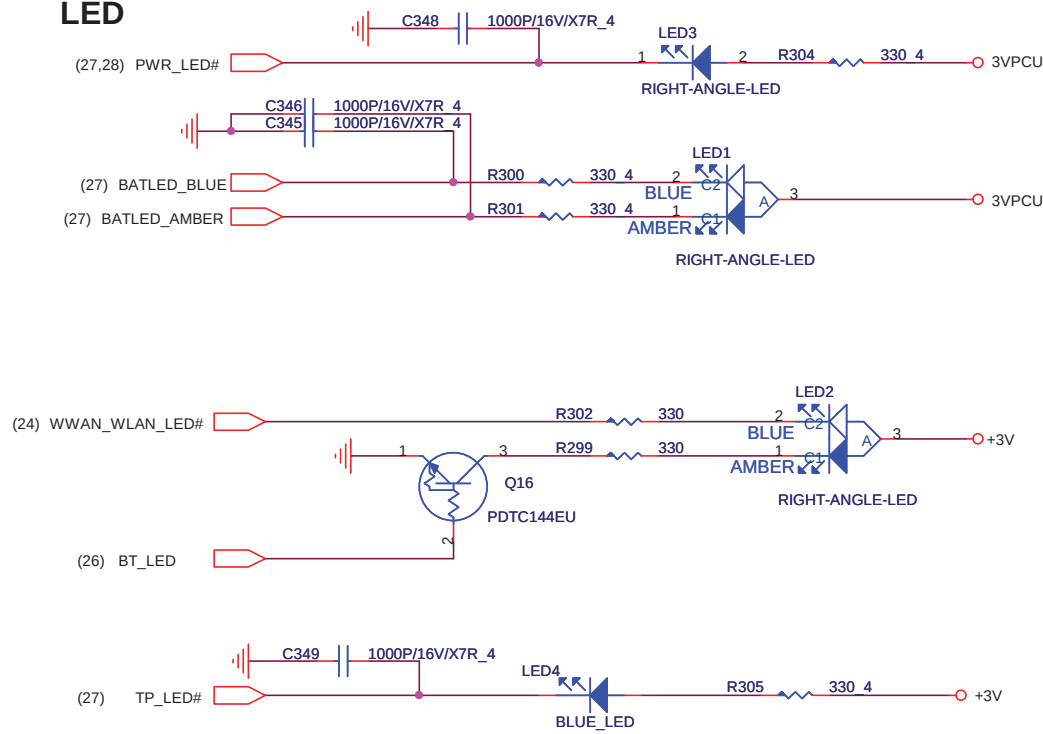
- 3VPCU**: Connected to pin 1 of CN3. A capacitor **C107** is connected between this line and ground. A component **0.1U/10V/X5R_4** is connected between pin 1 and pin 2.
- MY13**: Connected to pin 2 of CN3.
- MX0**: Connected to pin 3 of CN3.
- MX4**: Connected to pin 4 of CN3.
- NOVO_BUTTON#**: Connected to pin 5 of CN3.
- LIDSS1#**: Connected to pin 6 of CN3.
- FUNCTION/B_CON**: Connected to pin 8 of CN3.
- Ground**: Connected to pin 7 of CN3.

[illegible]

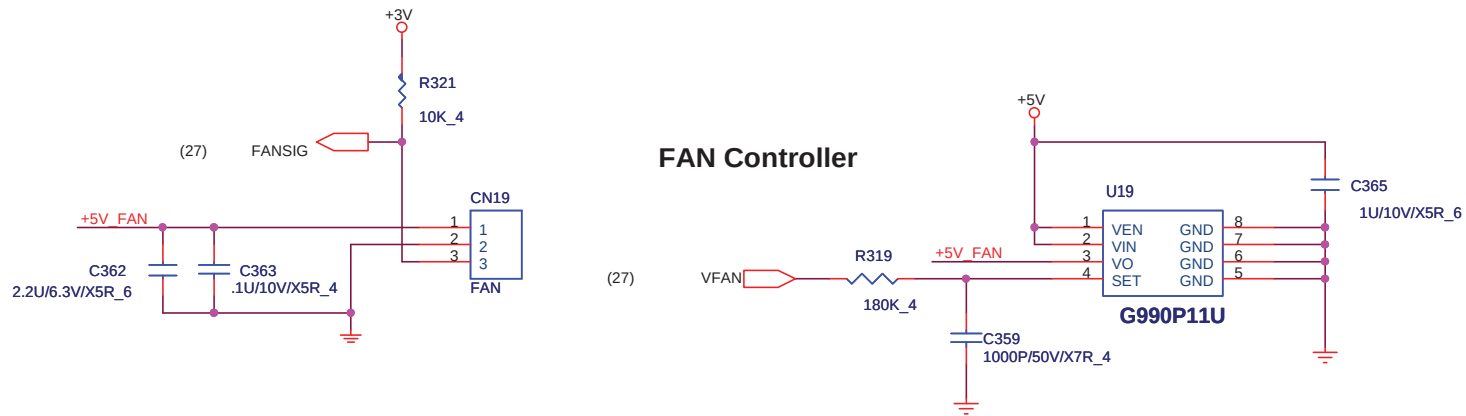
The diagram shows the CN17 connector with pins 1 through 28. The board is labeled 'SIO_BOARD_CON'. The connections are as follows:

- Pin 1: 3V
- Pin 2: 0.1uF/10V/X5R_4
- Pin 3: 0.1uF/10V/X5R_4
- Pin 4: 0.1uF/10V/X5R_4
- Pin 5: 0.1uF/10V/X5R_4
- Pin 6: 0.1uF/10V/X5R_4
- Pin 7: 0.1uF/10V/X5R_4
- Pin 8: 0.1uF/10V/X5R_4
- Pin 9: 0.1uF/10V/X5R_4
- Pin 10: 0.1uF/10V/X5R_4
- Pin 11: 0.1uF/10V/X5R_4
- Pin 12: 0.1uF/10V/X5R_4
- Pin 13: 0.1uF/10V/X5R_4
- Pin 14: 0.1uF/10V/X5R_4
- Pin 15: 0.1uF/10V/X5R_4
- Pin 16: 0.1uF/10V/X5R_4
- Pin 17: 0.1uF/10V/X5R_4
- Pin 18: 0.1uF/10V/X5R_4
- Pin 19: 0.1uF/10V/X5R_4
- Pin 20: 0.1uF/10V/X5R_4
- Pin 21: 0.1uF/10V/X5R_4
- Pin 22: 0.1uF/10V/X5R_4
- Pin 23: 0.1uF/10V/X5R_4
- Pin 24: 0.1uF/10V/X5R_4
- Pin 25: 0.1uF/10V/X5R_4
- Pin 26: 0.1uF/10V/X5R_4
- Pin 27: 0.1uF/10V/X5R_4
- Pin 28: 0.1uF/10V/X5R_4

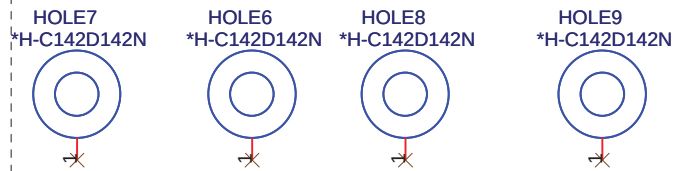
LED



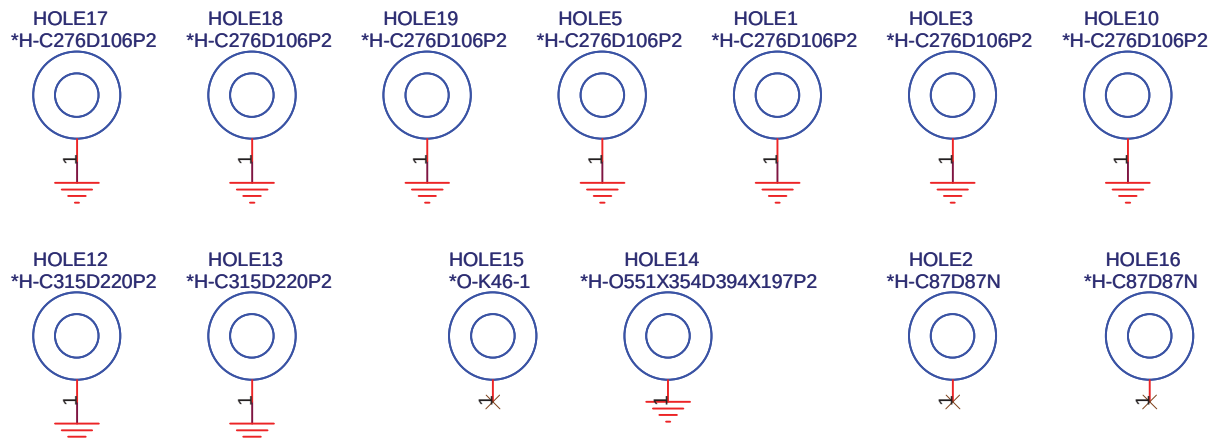
FAN Controller



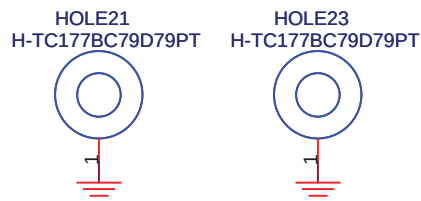
Hole for CPU support



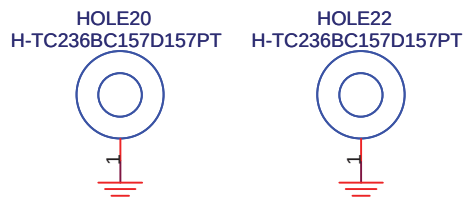
North Bridge nut



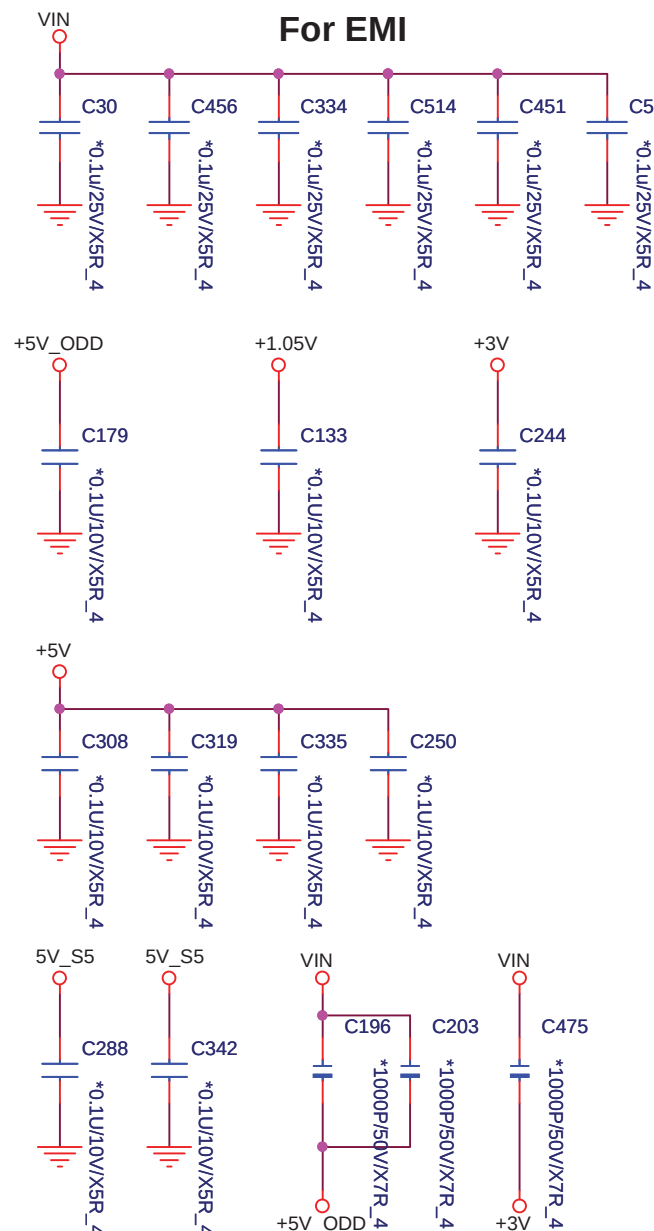
WWAN nut



WLAN nut



For EMI



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+3V, +5V

