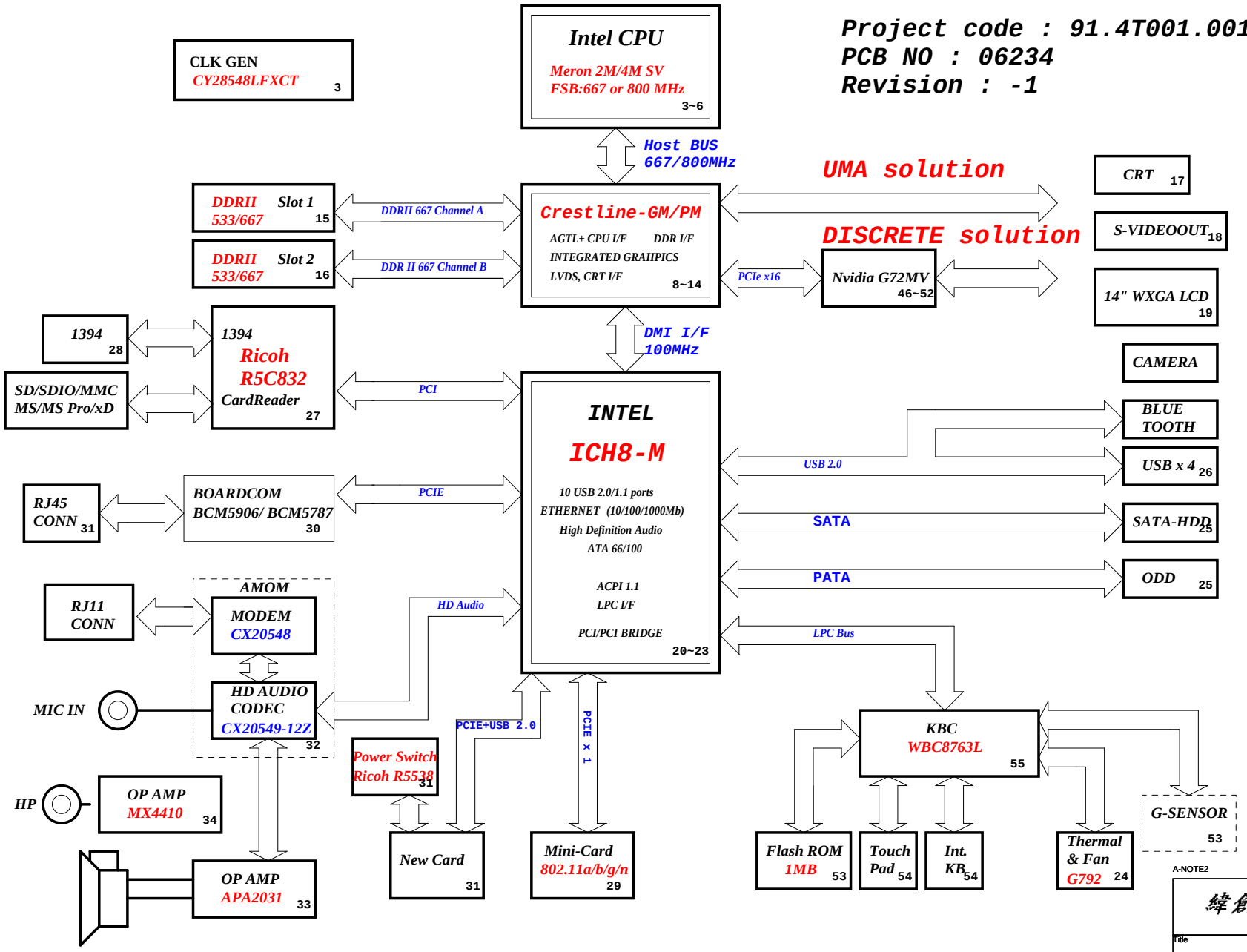
Anote2.0 Block Diagram

Project code : 91.4T001.001
PCB NO : 06234
Revision : -1



SYSTEM DC/DC TPS51120 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3D3V_S5

SYSTEM DC/DC ISL6268CAZ 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51116 40	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 0D9V_S0

CHARGER ISL6255	
INPUTS	OUTPUTS
DCBATOUT	BT+ 20V 3.0A 5V 100mA

CPU DC/DC ISL6262ACRZ 36,37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

PCB LAYER

L1: Signal 1
L2: VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

A-NOTE2

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Title: Block Diagram
Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1
Date: Thursday, March 22, 2007 | Sheet 1 of 56

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	TP3	AZ_DOUT_ICH	Description
0	0		RSVD
0	1		Enter XOR Chain
1	0		Normal Operation(default)
1	1		Set PCIE port config bit1

A16 swap override strap

PCI_GNT#3	
low = A16 swap override enable	
high = default	

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

A-NOTE2

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Title: Table of Content

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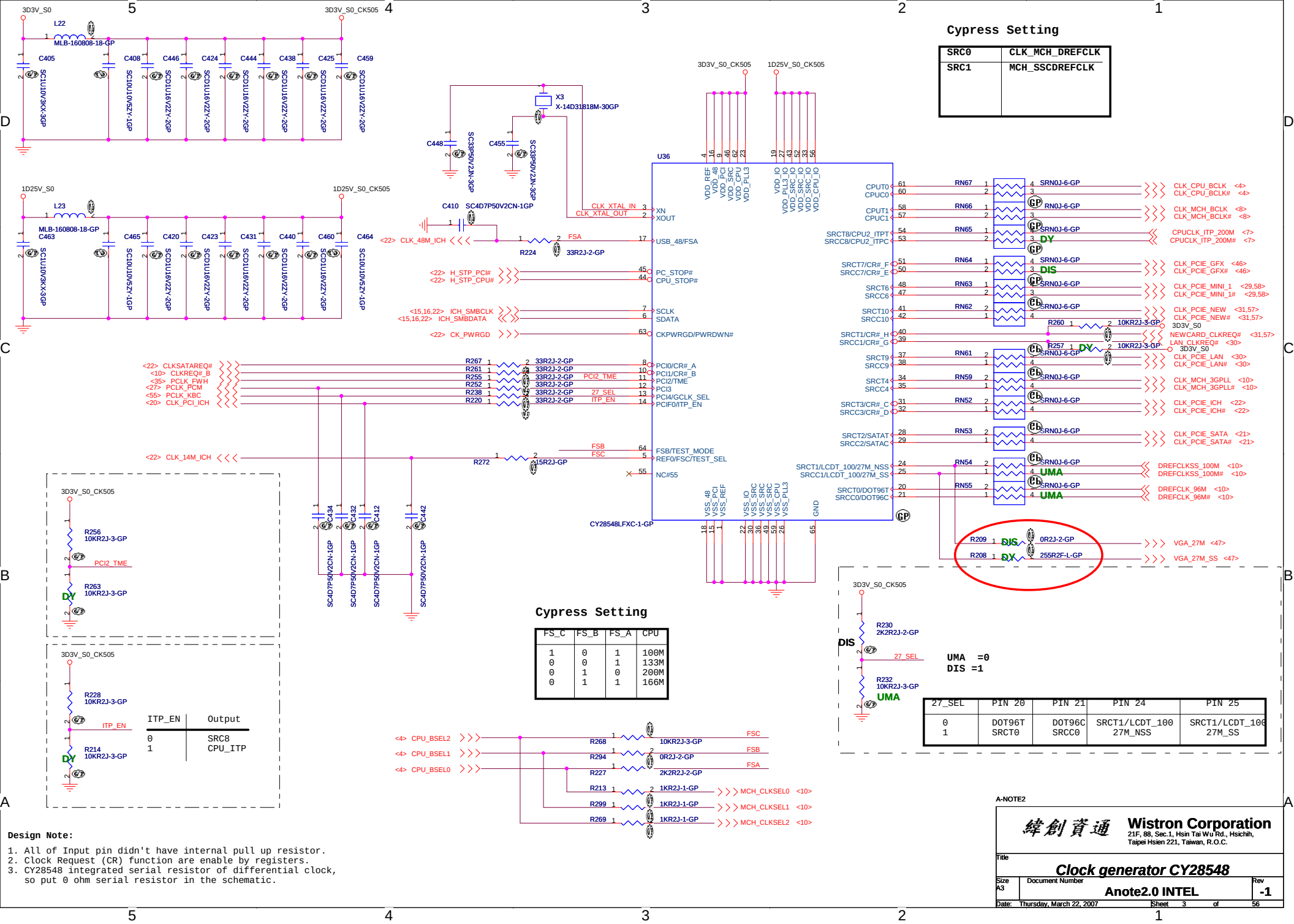

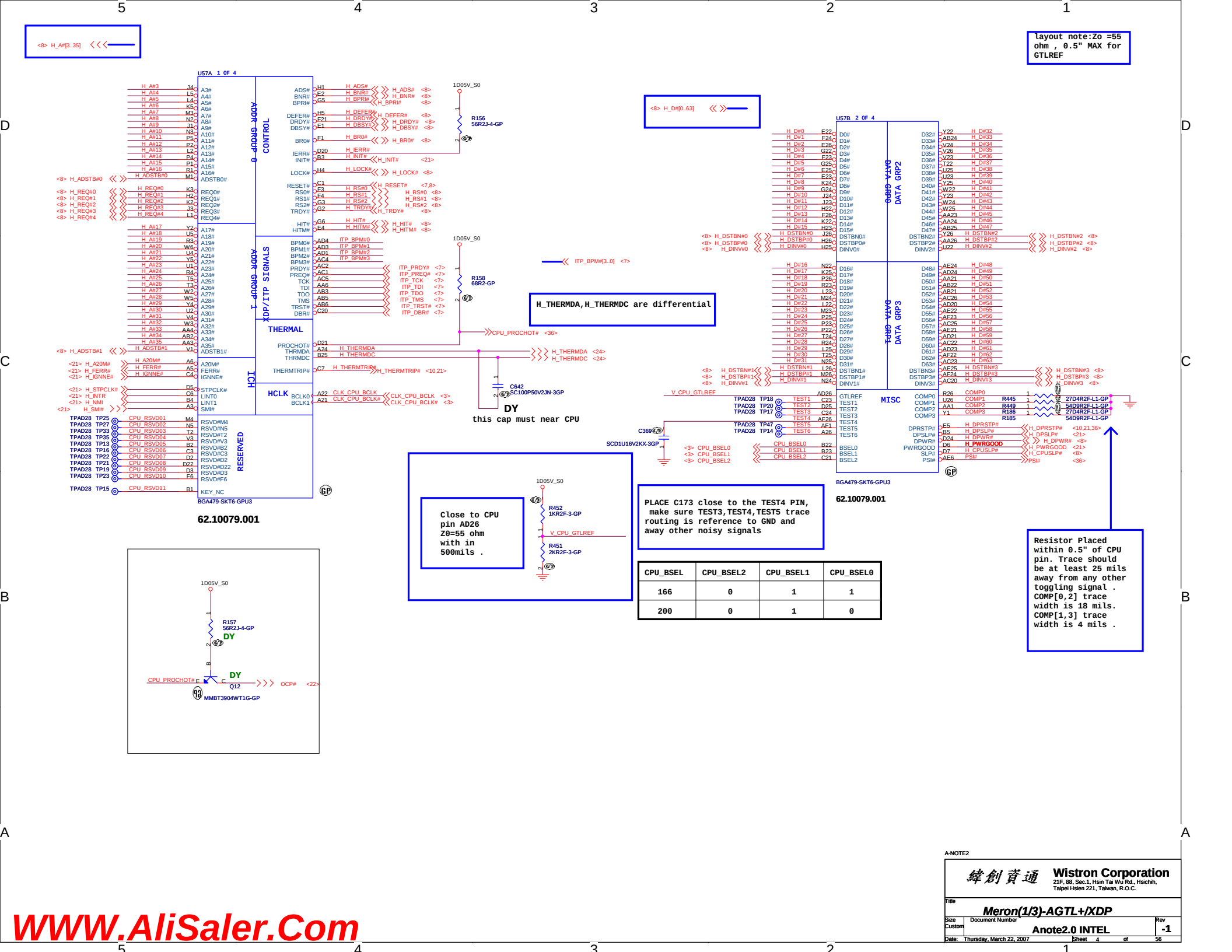
layout note:Zo =55 ohm , 0.5" MAX for GTLREF
H_THERMDA,H_THERMDC are differential
DY
this cap must near CPU
Close to CPU pin AD26 Z0=55 ohm with in 500mils .
PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals
Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .
CPU_BSEL | CPU_BSEL2 | CPU_BSEL1 | CPU_BSEL0
166 | 0 | 1 | 1
200 | 0 | 1 | 0
62.10079.001
BGA479-SKT6-GPU3
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Meron(1/3)-AGTL+/XDP
Anote2.0 INTEL
-1
Thursday, March 22, 2007
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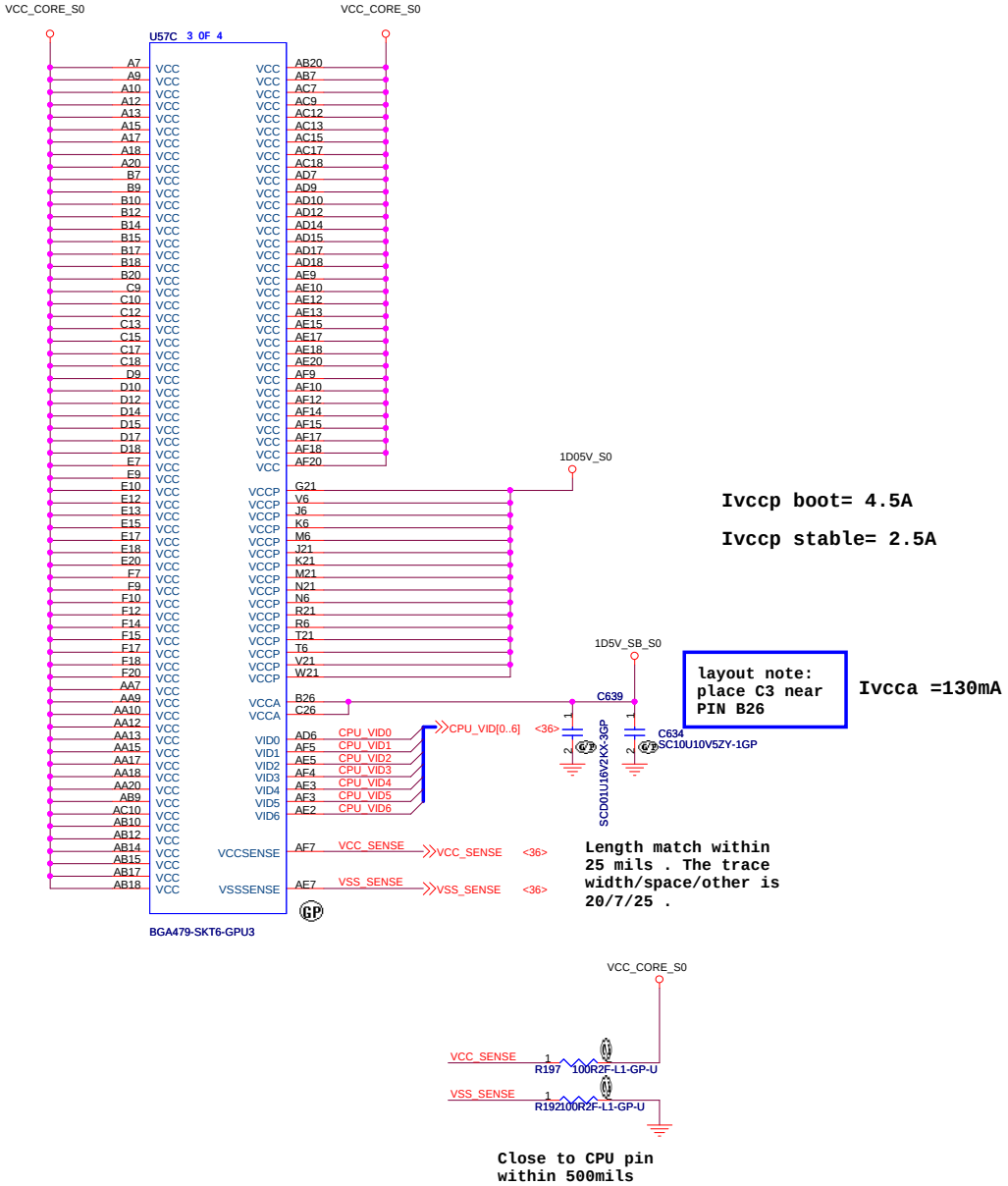

Ivccp boot= 4.5A

Ivccp stable= 2.5A

Ivcca =130mA

layout note: place C3 near PIN B26

Length match within 25 mils . The trace width/space/other is 20/7/25 .

Close to CPU pin within 500mils

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Title: *Meron(2/3)-AGTL+/PWR*

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

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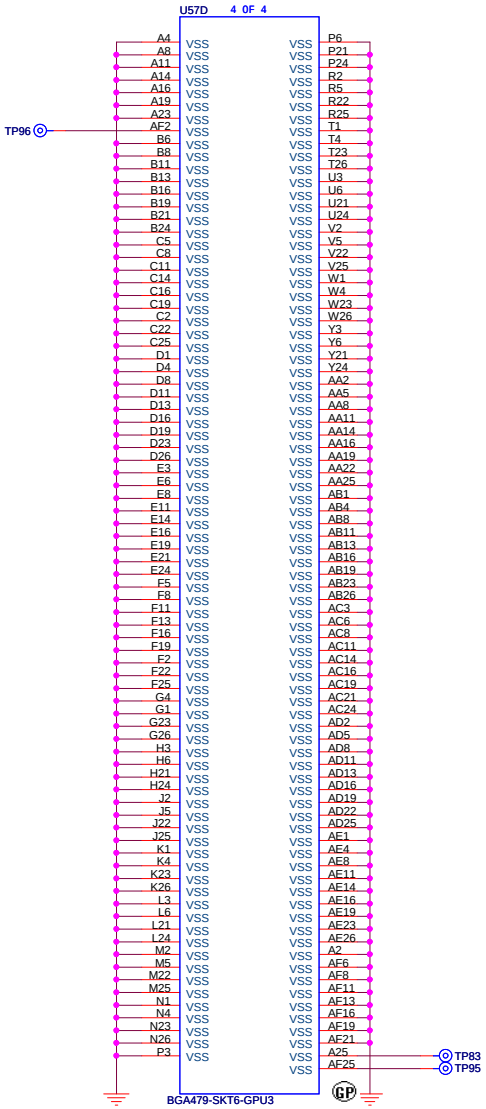

Place these capacitors on L1
(North side ,Secondary Layer)

VCC_CORE_S0

C686 SC10U6D3V5MX-3GP
C675 SC10U6D3V5MX-3GP
C676 SC10U6D3V5MX-3GP
C677 SC10U6D3V5MX-3GP
C678 SC10U6D3V5MX-3GP
C679 SC10U6D3V5MX-3GP
C680 SC10U6D3V5MX-3GP
C261 SC10U6D3V5MX-3GP

Place these capacitors on L1
(North side ,Secondary Layer)

VCC_CORE_S0

C273 SC10U6D3V5MX-3GP
C274 SC10U6D3V5MX-3GP
C260 SC10U6D3V5MX-3GP
C687 SC10U6D3V5MX-3GP
C688 SC10U6D3V5MX-3GP
C683 SC10U6D3V5MX-3GP
C684 SC10U6D3V5MX-3GP
C685 SC10U6D3V5MX-3GP

Mid Frequencd Decoupling

Place these capacitors on L1
(North side ,Secondary Layer)

VCC_CORE_S0

C358 SC10U6D3V5MX-3GP
C340 SC10U6D3V5MX-3GP
C341 SC10U6D3V5MX-3GP
C277 SC10U6D3V5MX-3GP
C276 SC10U6D3V5MX-3GP
C368 SC10U6D3V5MX-3GP
C375 SC10U6D3V5MX-3GP
C360 SC10U6D3V5MX-3GP

DY DY DY DY DY DY DY DY

1D05V_S0

C298 SCD1U16V2KX-3GP
C285 SCD1U16V2KX-3GP
C324 SCD1U16V2KX-3GP
C279 SCD1U16V2KX-3GP
C286 SCD1U16V2KX-3GP
C314 SCD1U16V2KX-3GP

Place these inside socket cavity on L1 (North side Secondary)

A-NOTE2

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Title: ***Meron(3/3)-GND&Bypass***

Size: A3 | Document Number: **Anote2.0 INTEL** | Rev: **-1**

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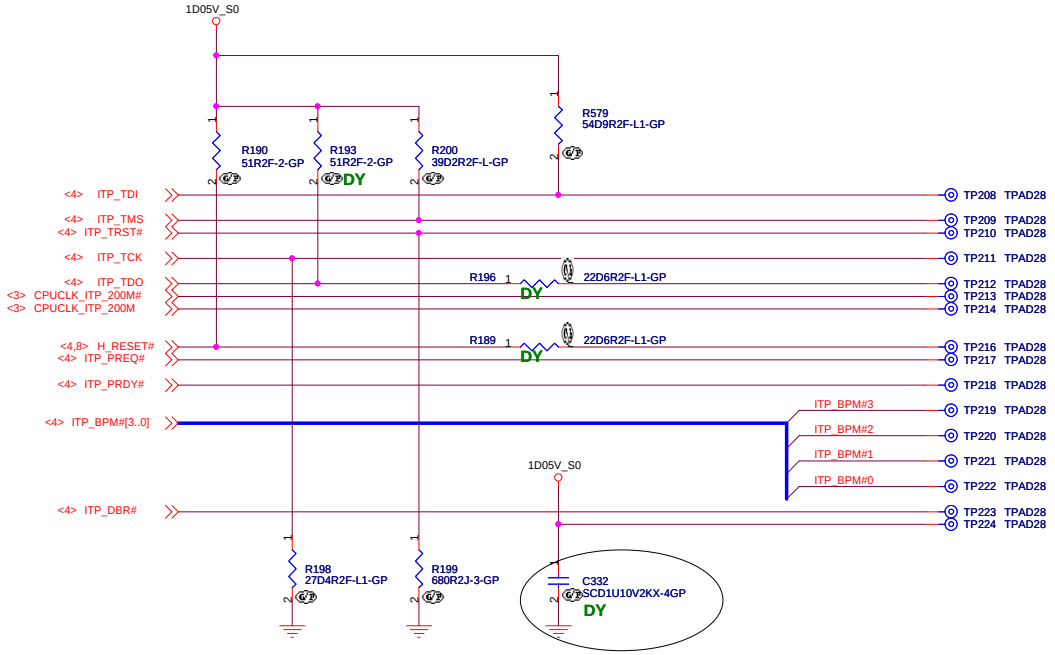
ITP Connector



A-NOTE2

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Title: *Meron(3/3)-GND&Bypass*		
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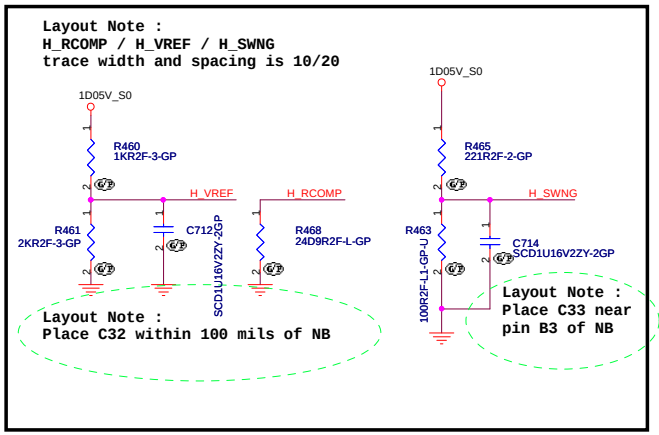
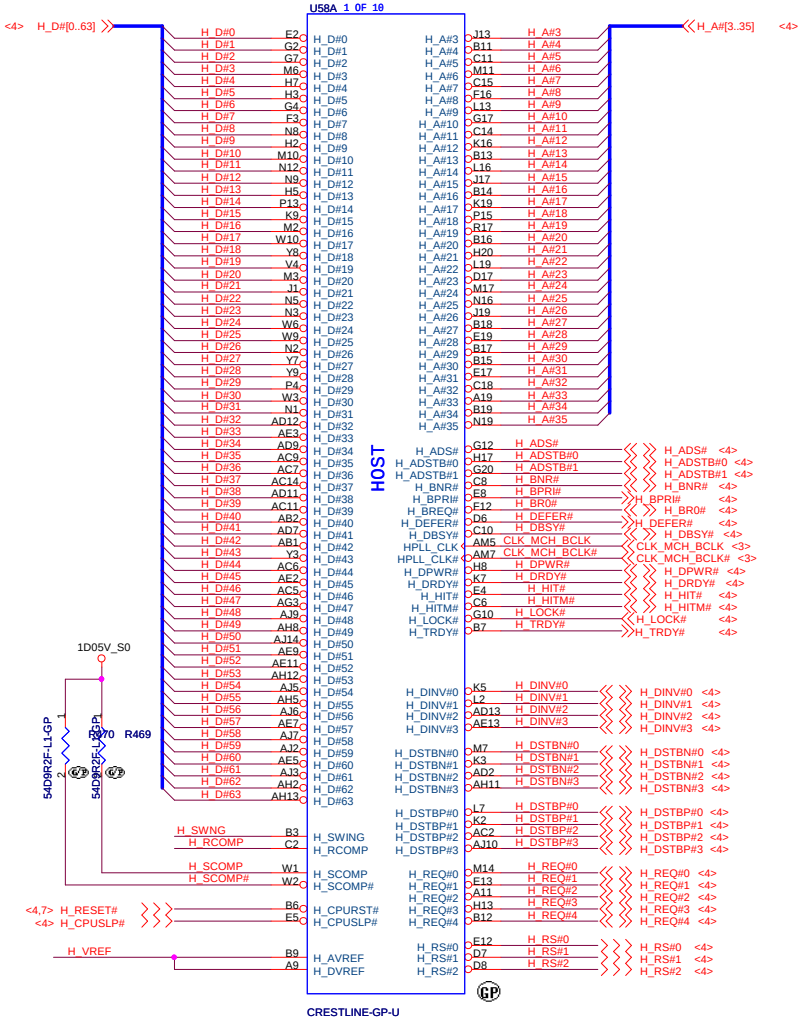
Date: Thursday, March 22, 2007	Sheet 7 of 56	

layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing
and impedance (55 ohm) same as FSB data traces





A-NOTE2

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Title: CRESTLINE(1/7)-AGTL+/DMI/DDR2

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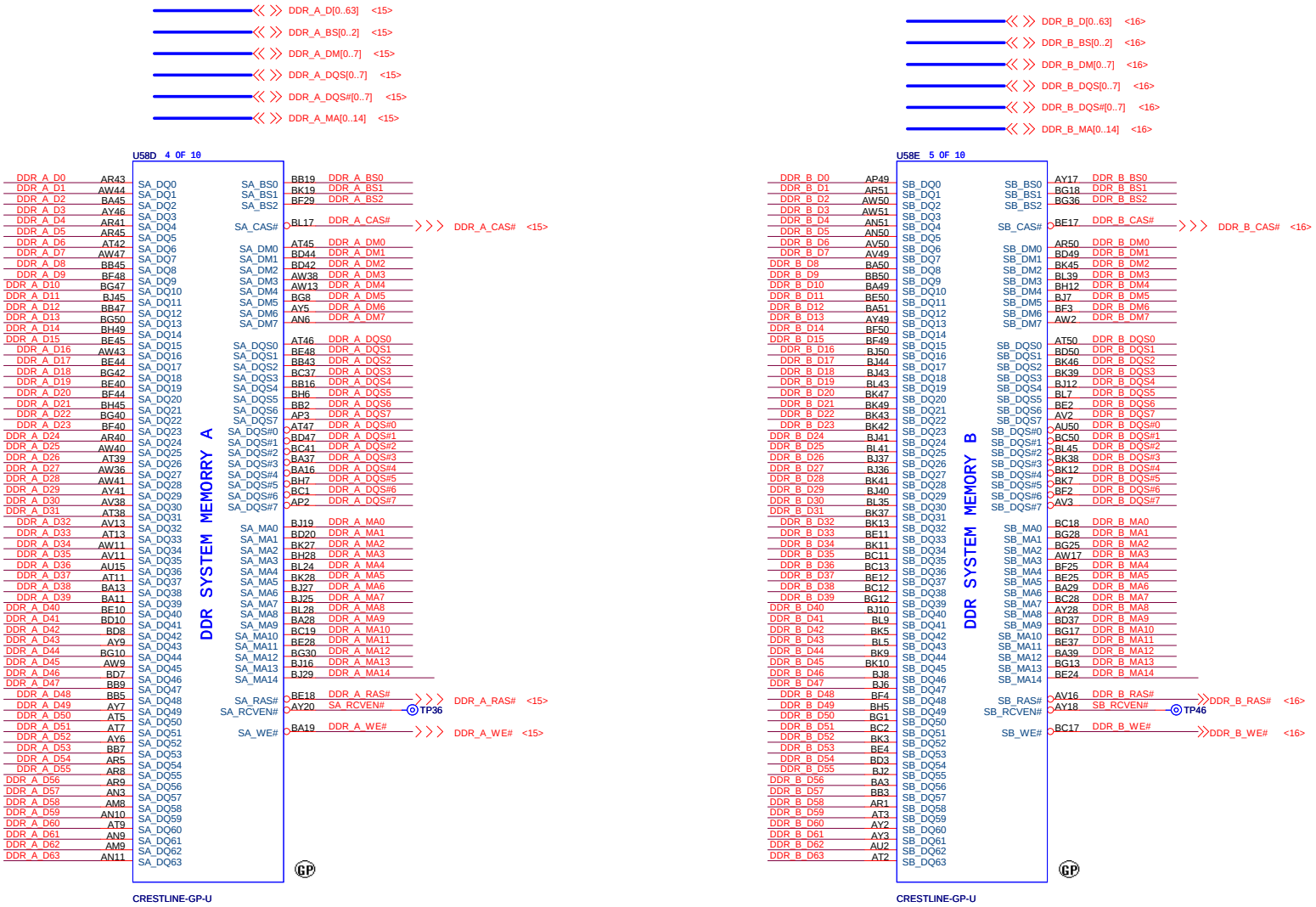

A-NOTE2

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Title: **CRESTLINE(2/7)-DDR2 A/B CH**

Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

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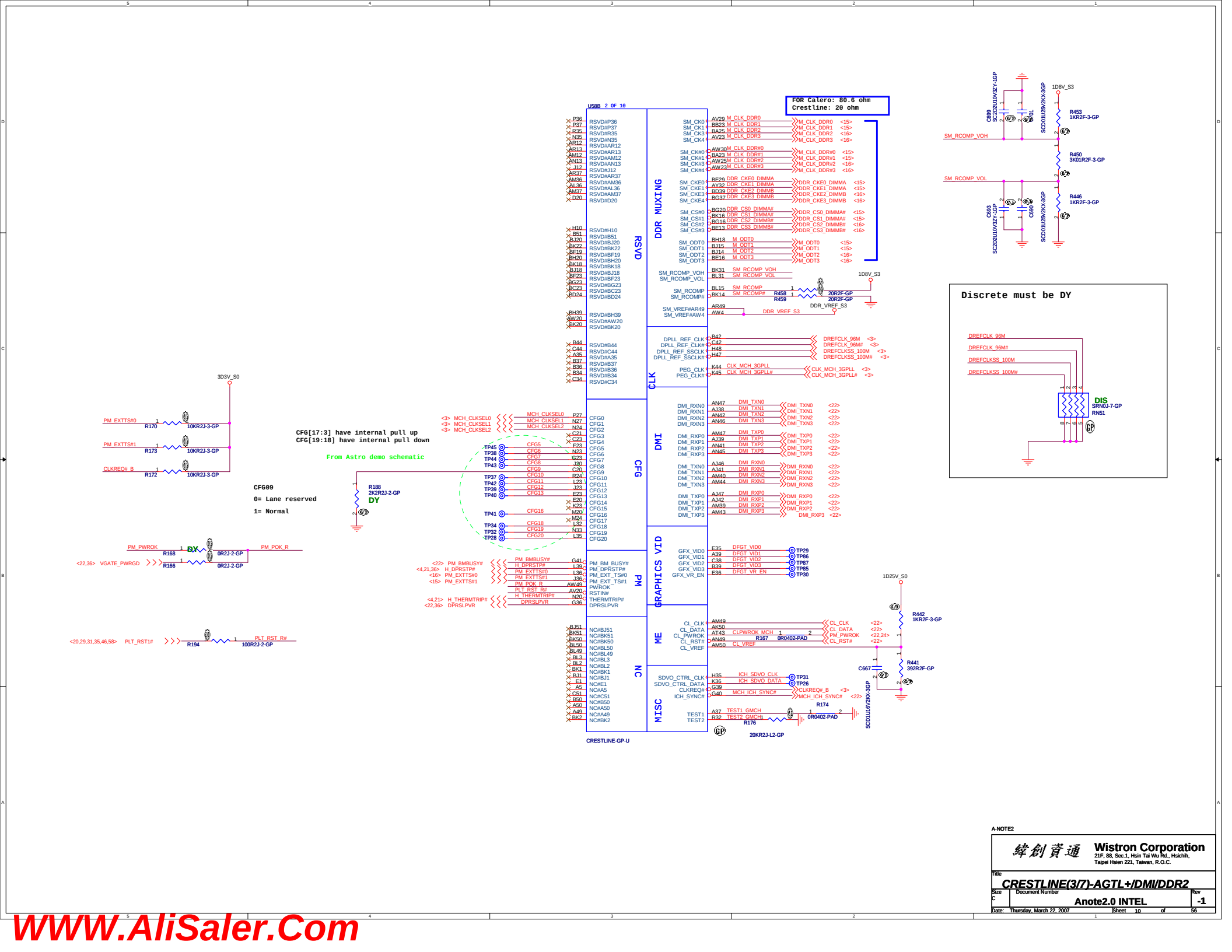
U58B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
FOR Calero: 80.6 ohm
Crestline: 20 ohm
Discrete must be DY
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down
From Astro demo schematic
CFG09
0= Lane reserved
1= Normal
CRESTLINE-GP-U
3D3V_S0
1D8V_S3
1D25V_S0
DDR_VREF_S3
DIS
DY
A-NOTE2
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CRESTLINE(3/7)-AGTL+/DMI/DDR2
Anote2.0 INTEL
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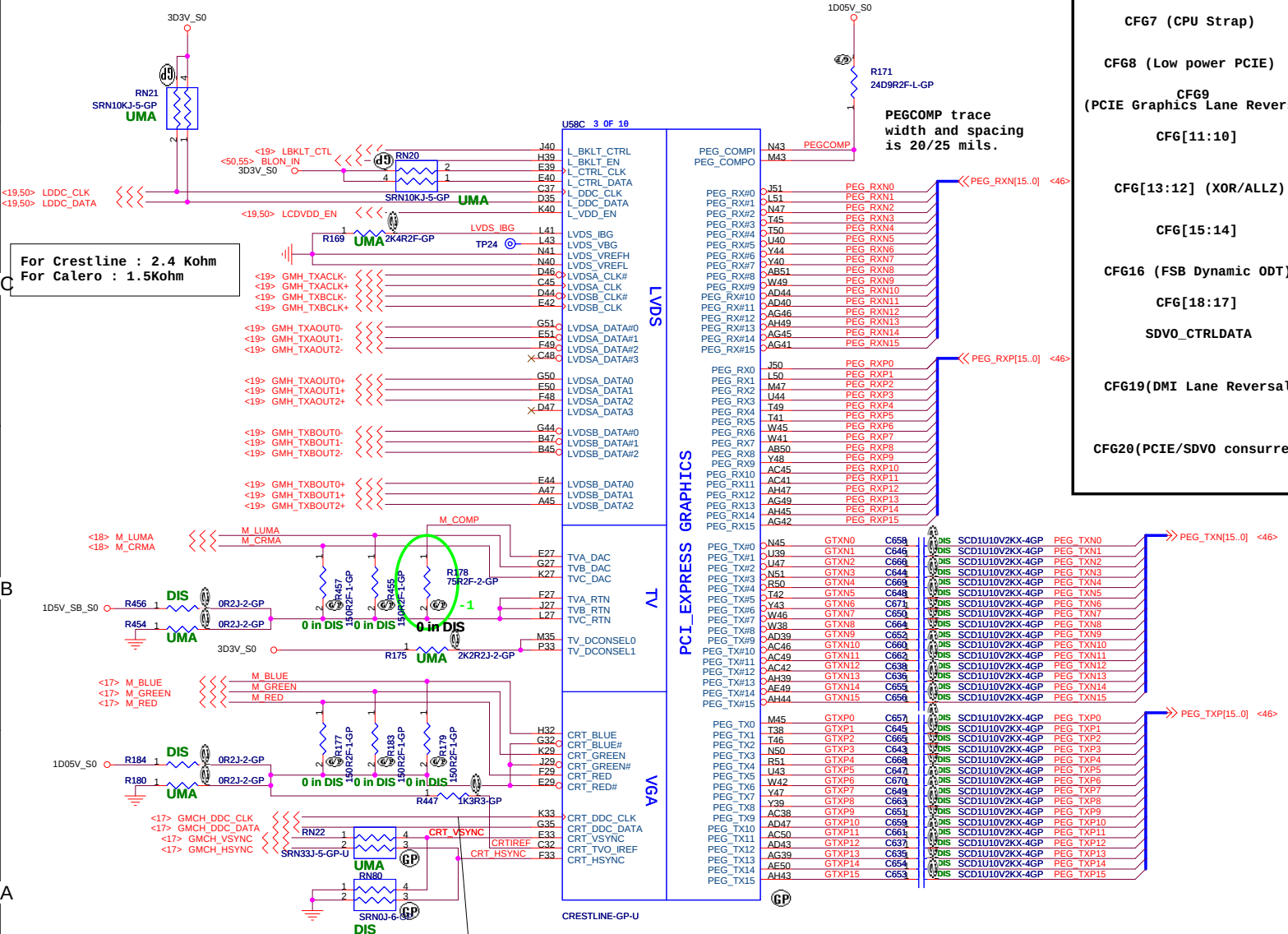
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.



A-NOTE2

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Title: CRESTLINE(4/7)-VGA/LVDS/TV

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A3	Anote2.0 INTEL	-1

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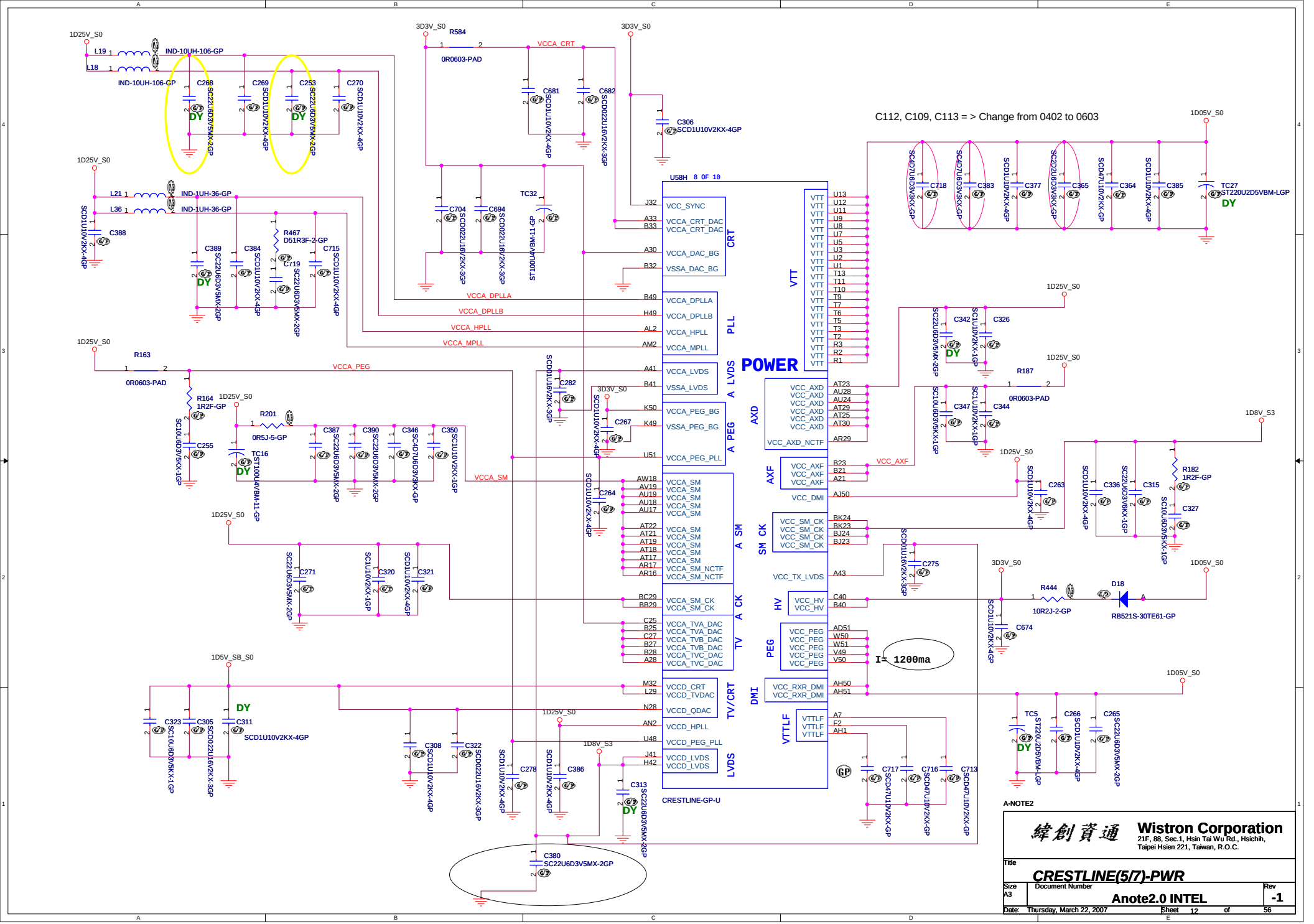

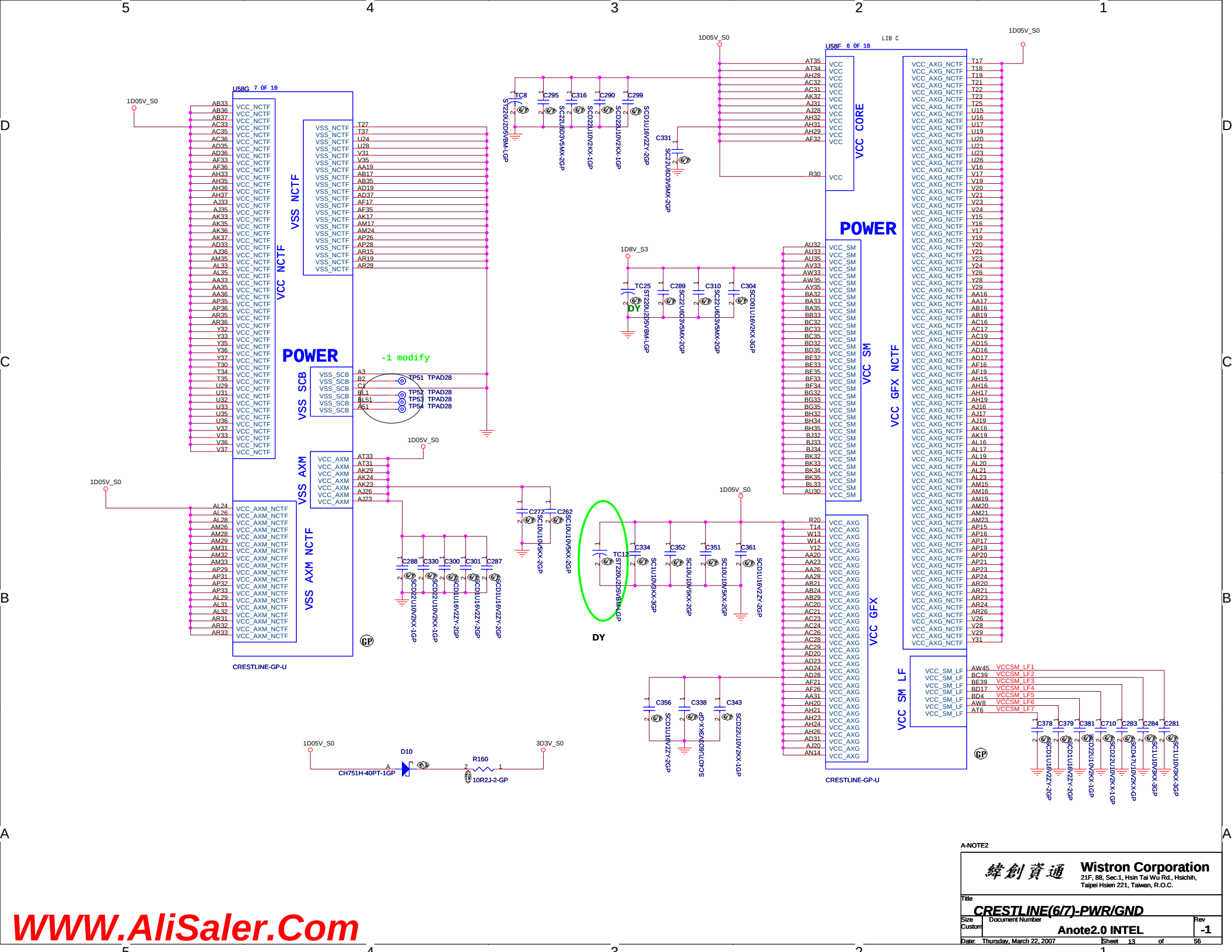

A-NOTE2

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Title: CRESTLINE(6/7)-PWR/GND

Size: Custom | Document Number: Anote2.0 INTEL | Rev: -1

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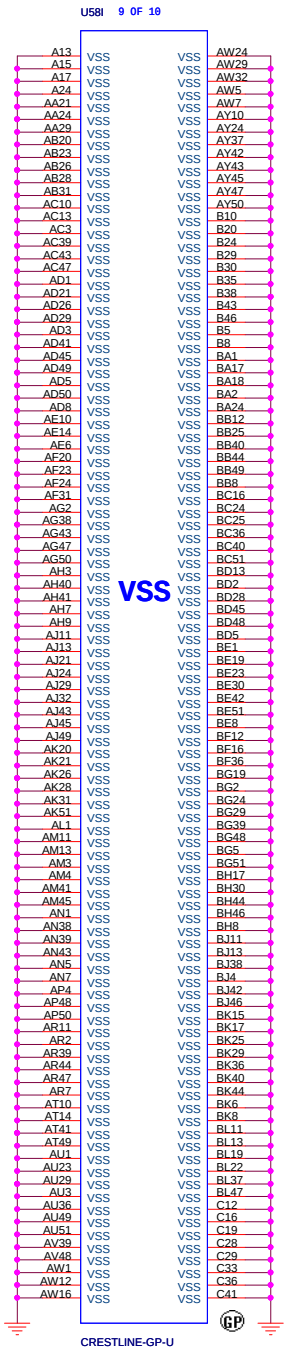

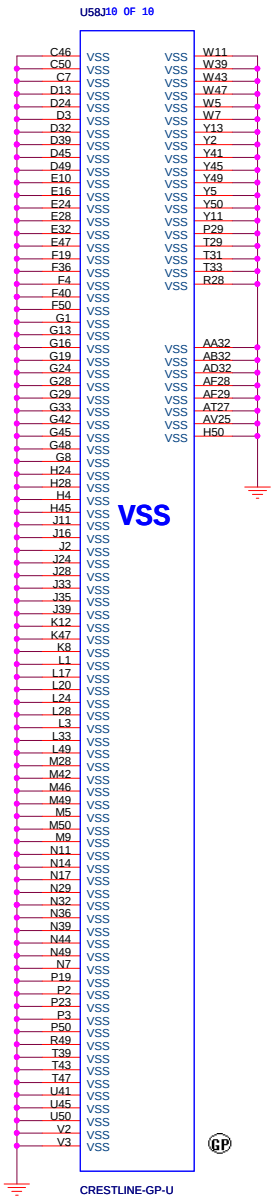

A-NOTE2

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Title: ***CRESTLINE(7/7)-PWR/GND***

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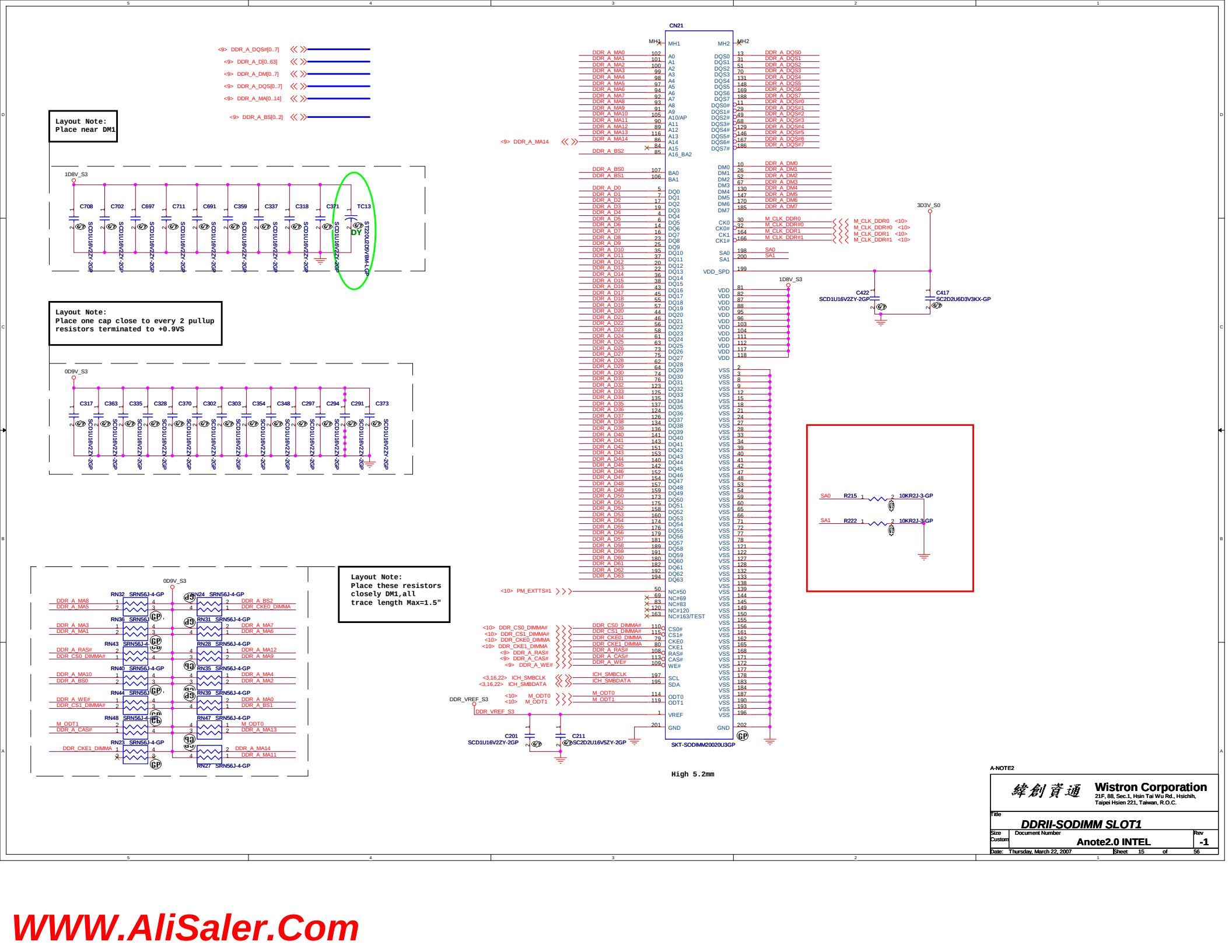

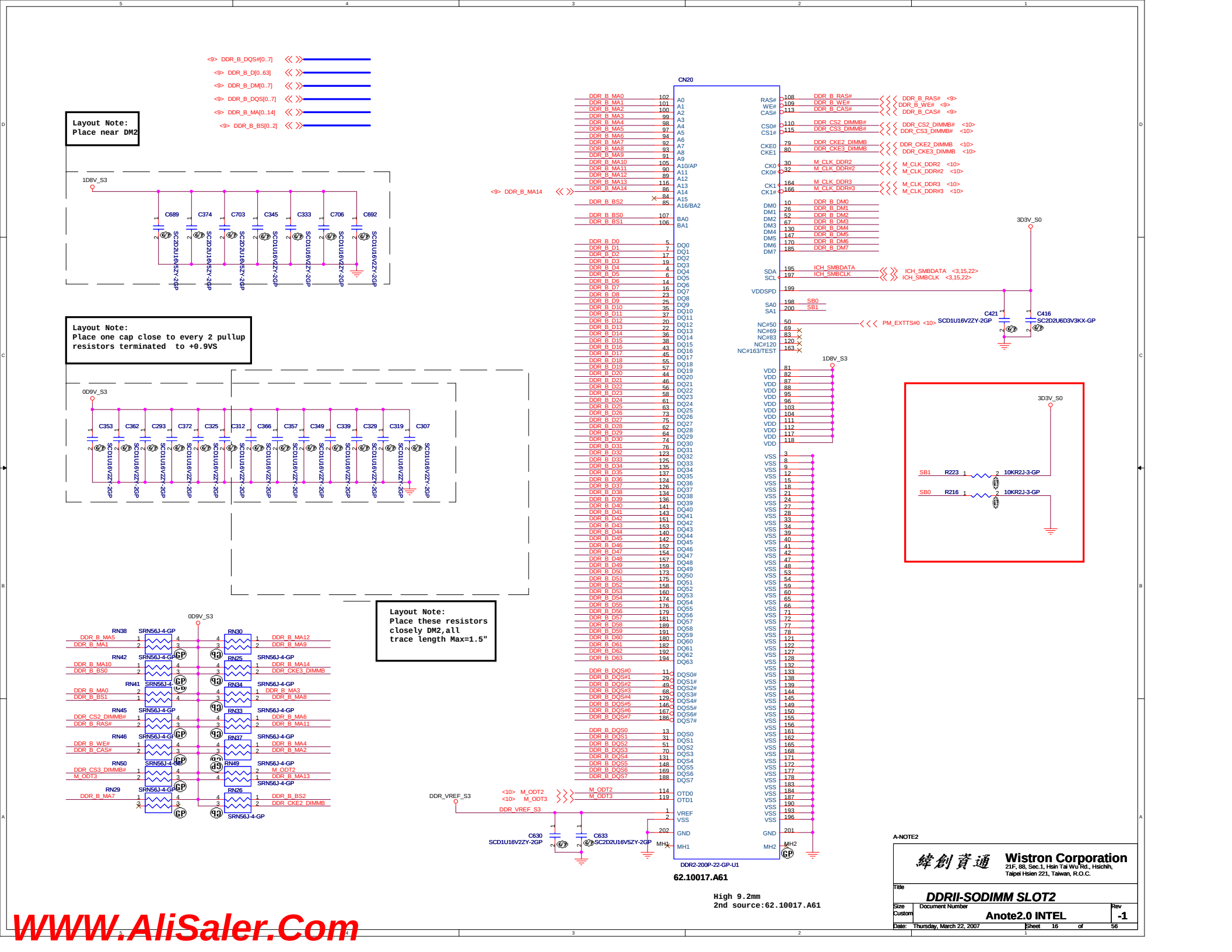
Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
CN20
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
2nd source:62.10017.A61
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DDRII-SODIMM SLOT2
Anote2.0 INTEL
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Thursday, March 22, 2007
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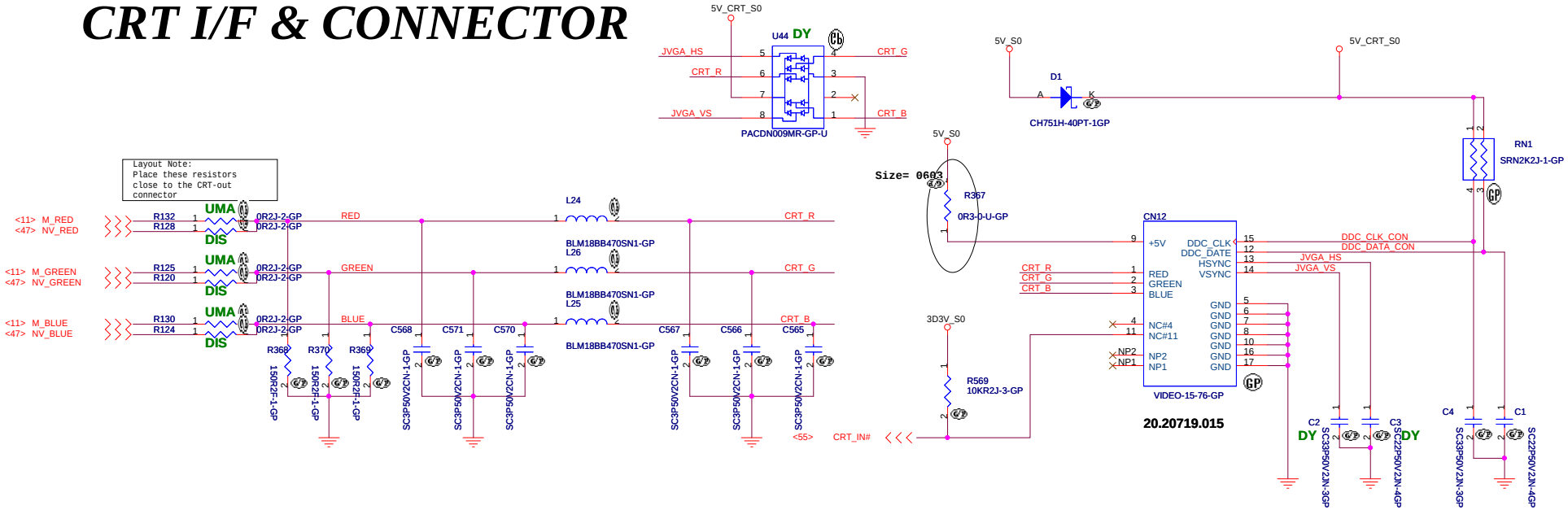
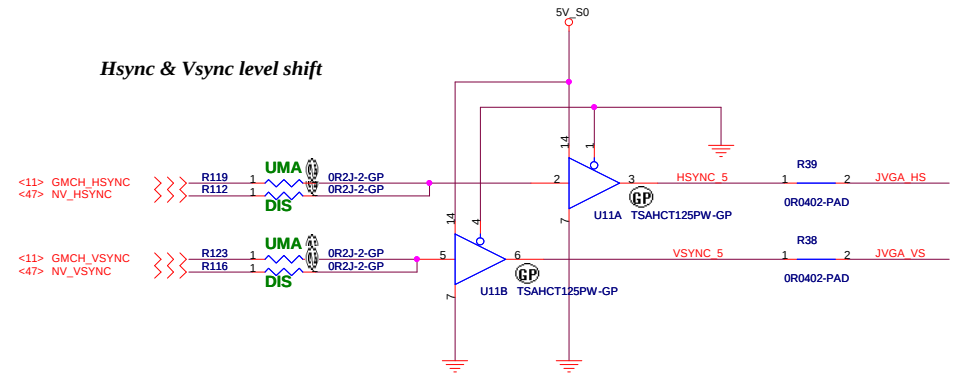
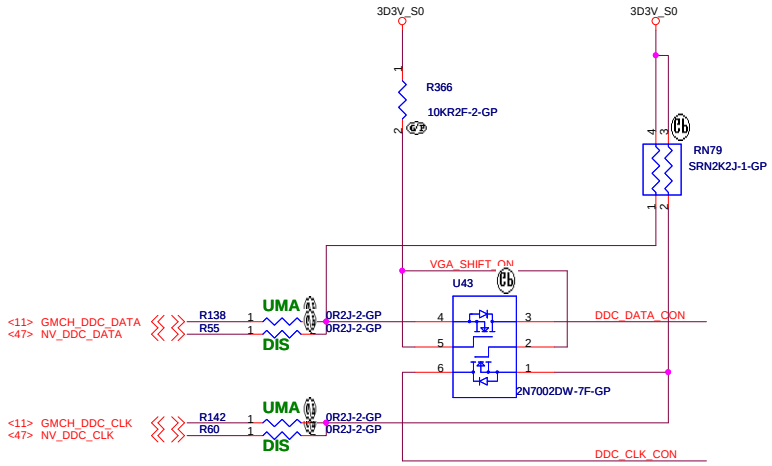
CRT I/F & CONNECTOR



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





A-NOTE2

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Title: CRT Connector

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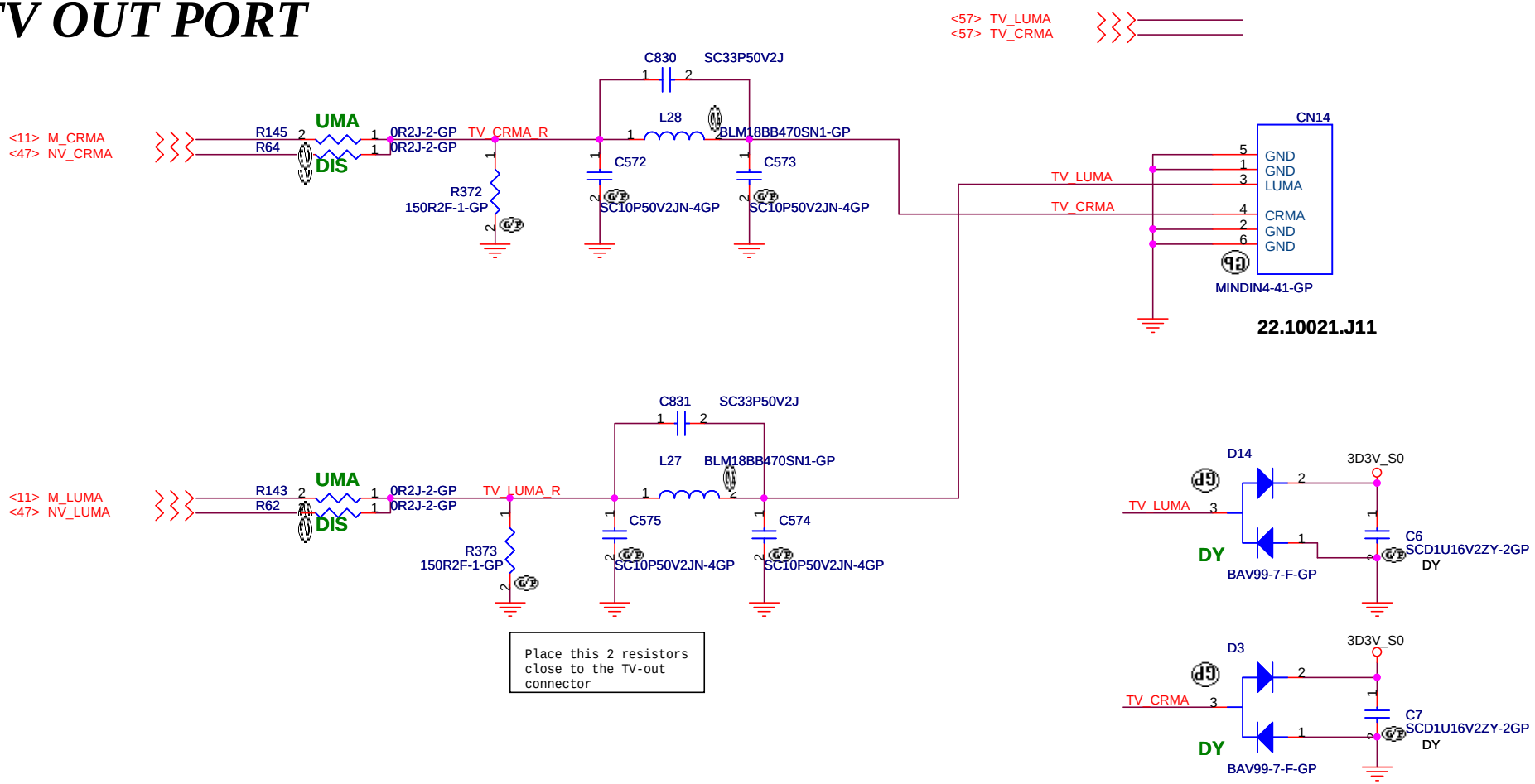
TV OUT PORT



A-NOTE2

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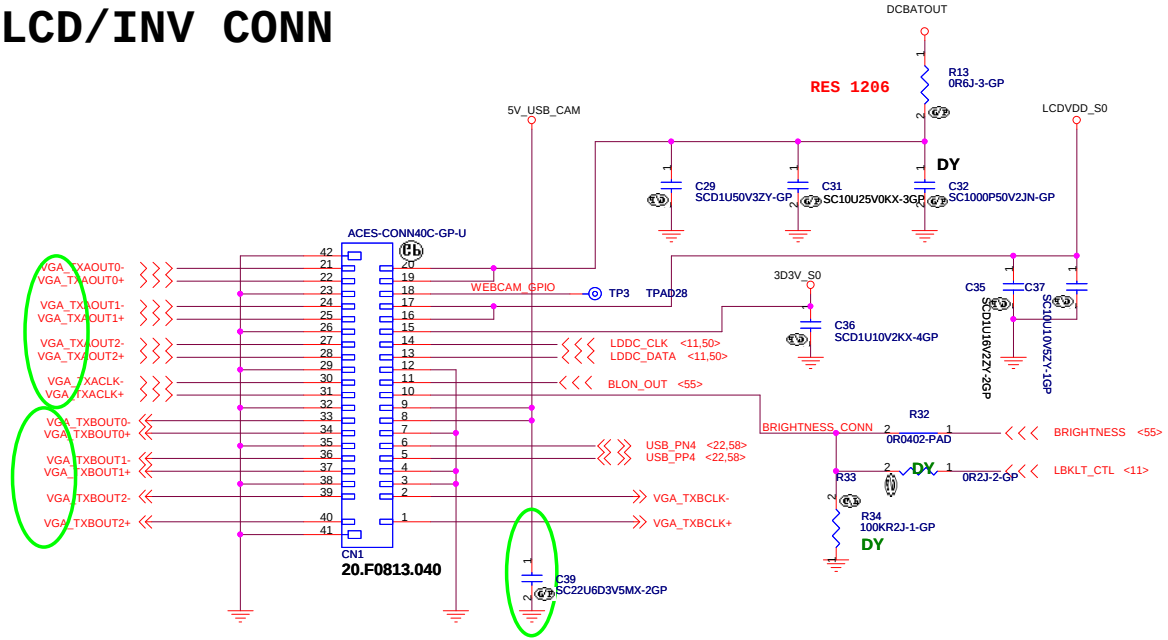
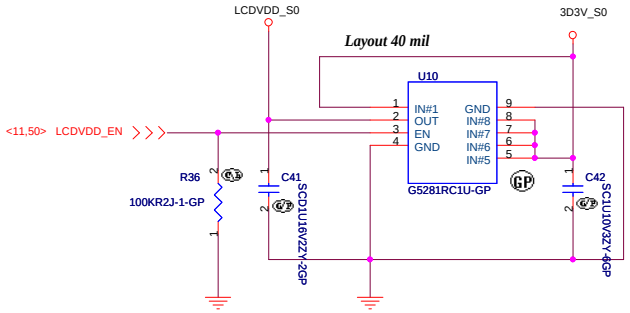
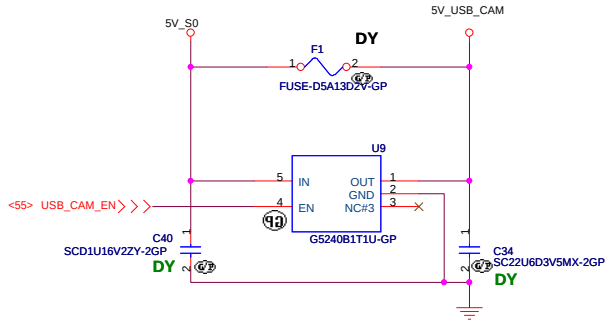
Title	***TV Connector***	
Size A4	Document Number **Anote2.0 INTEL**	Rev **-1**
Date: Thursday, March 22, 2007	Sheet 18 of 56	

LED / INVERTER INTERFACE

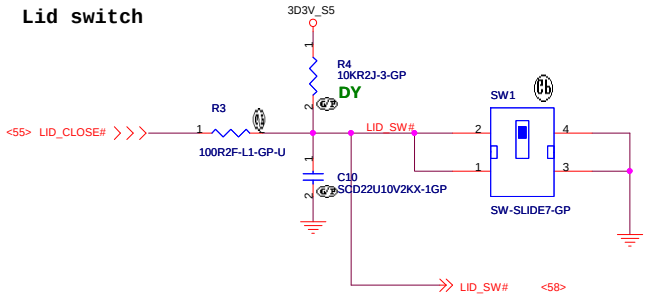
LCD/INV CONN



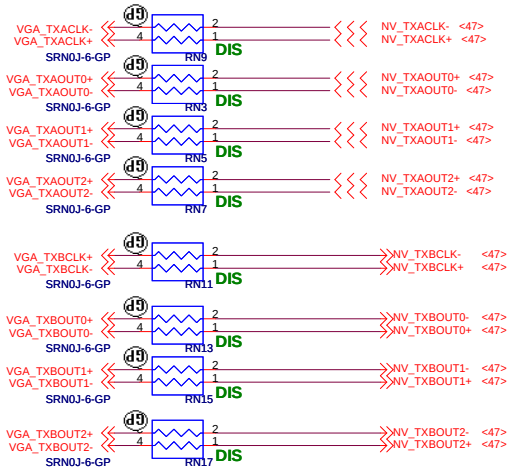




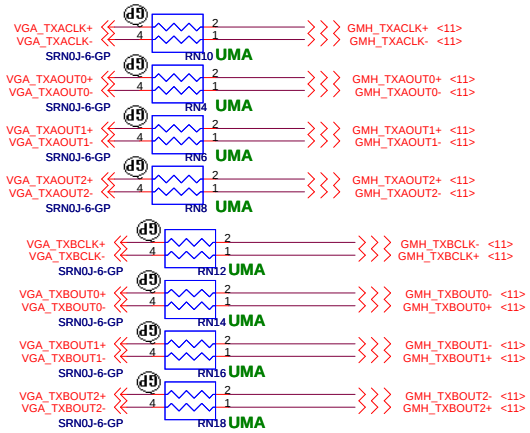
Lid switch



ATI LVDS INTERFACE



UMA LVDS INTERFACE



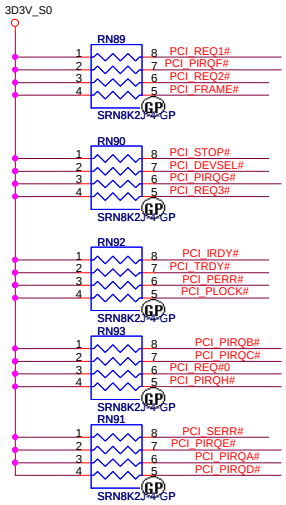
A-NOTE2

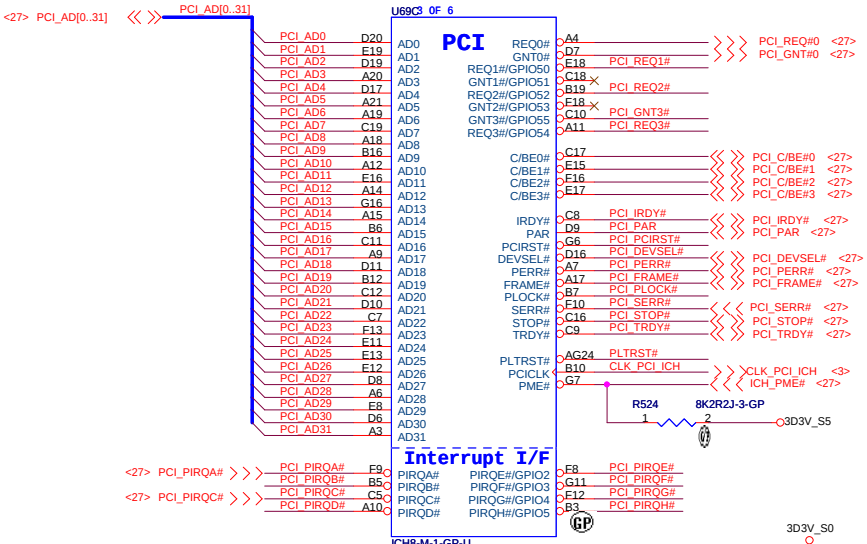
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

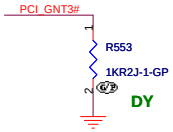
Title: LCD/Inverter Connector

Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

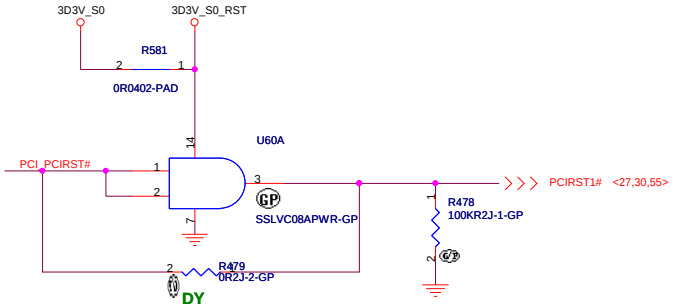
Date: Thursday, March 22, 2007 Sheet 19 of 56

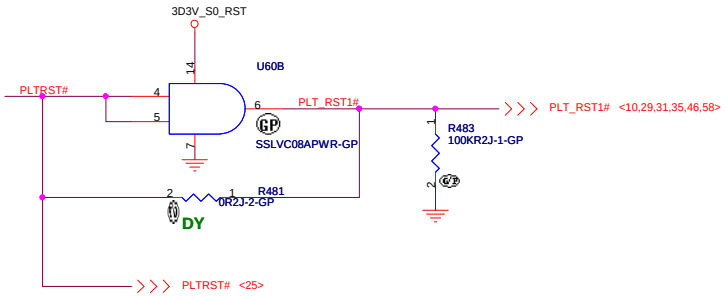




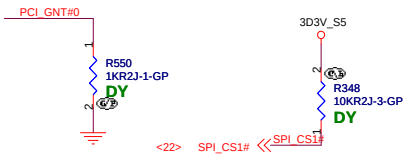


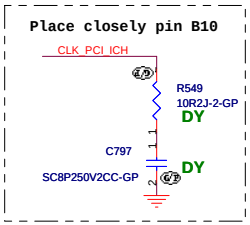
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *





Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





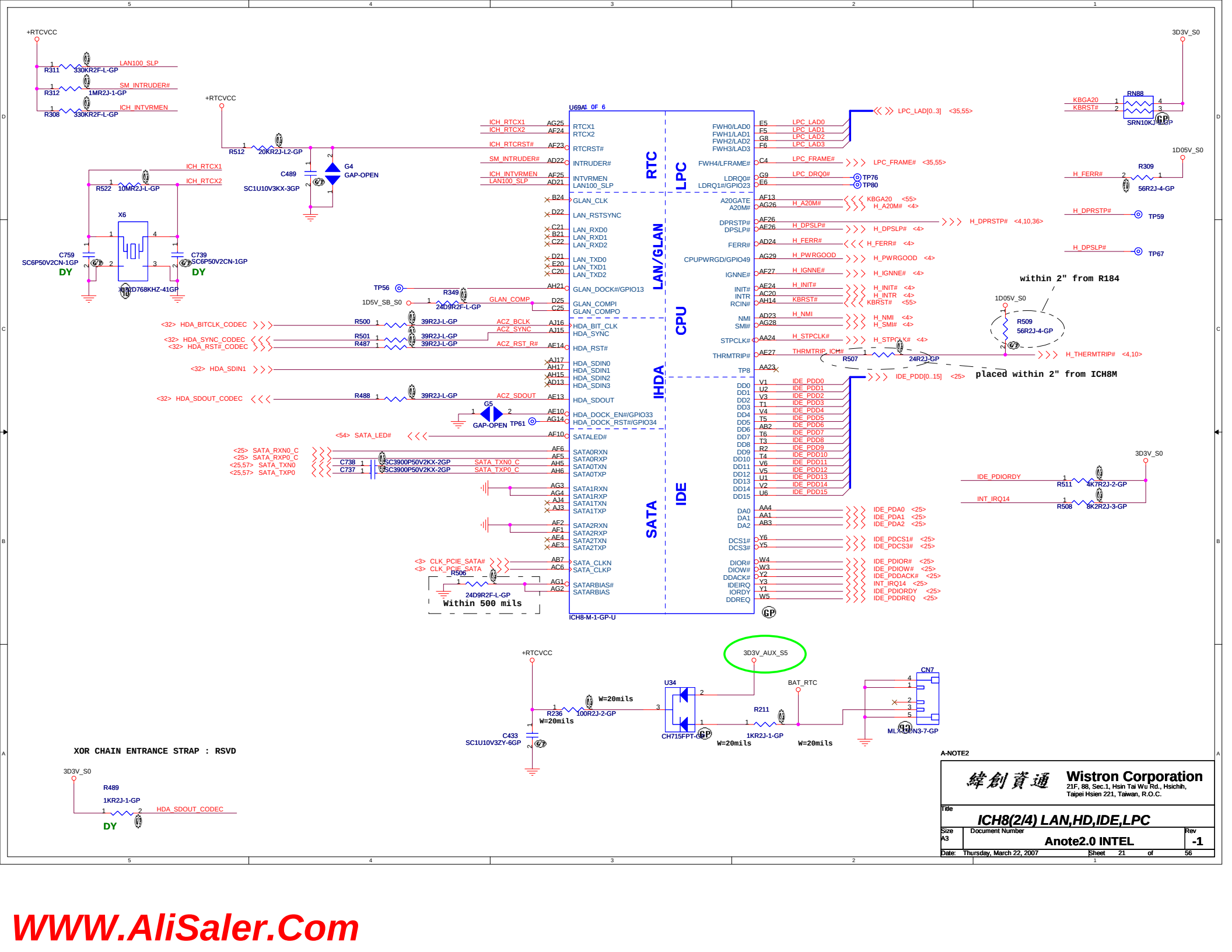
A-NOTE2

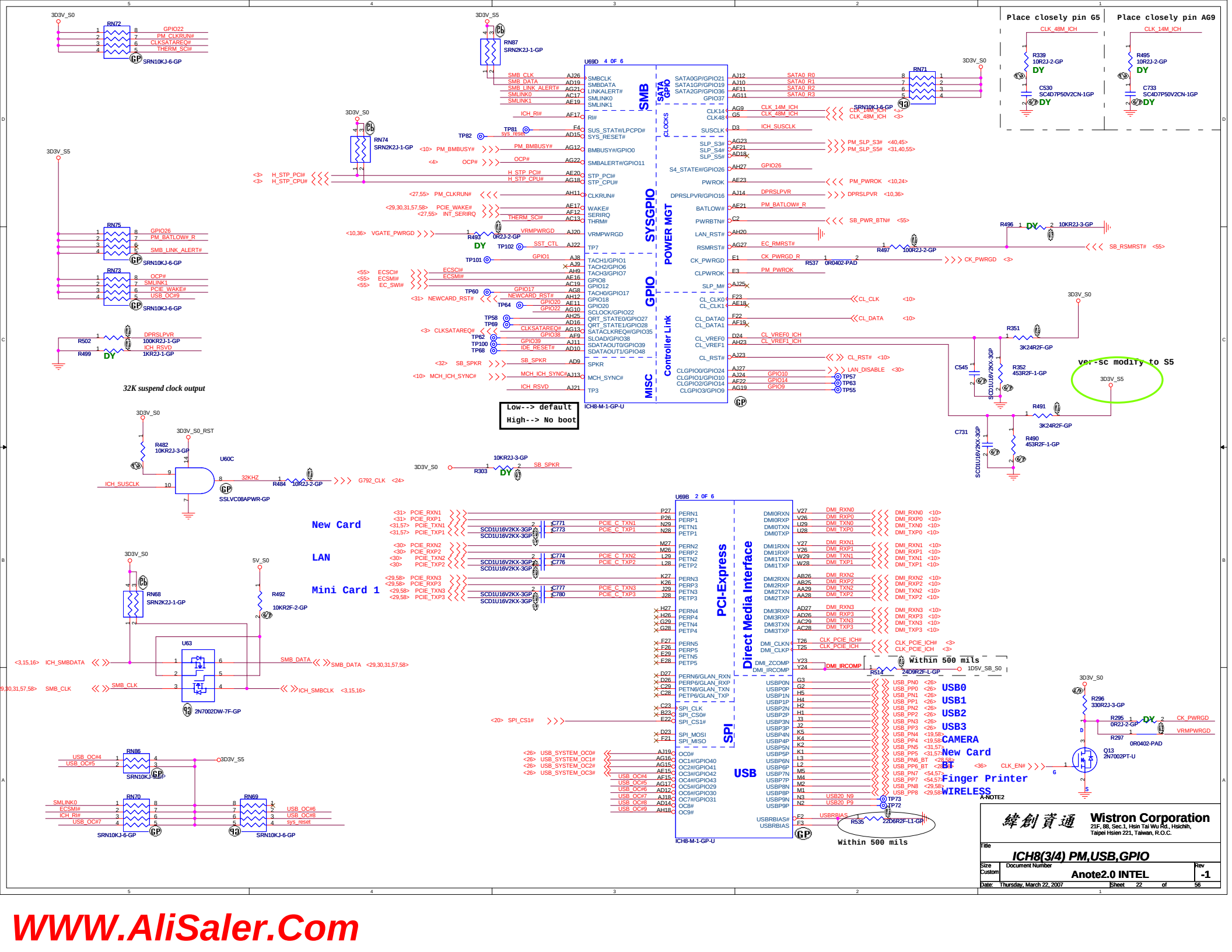
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

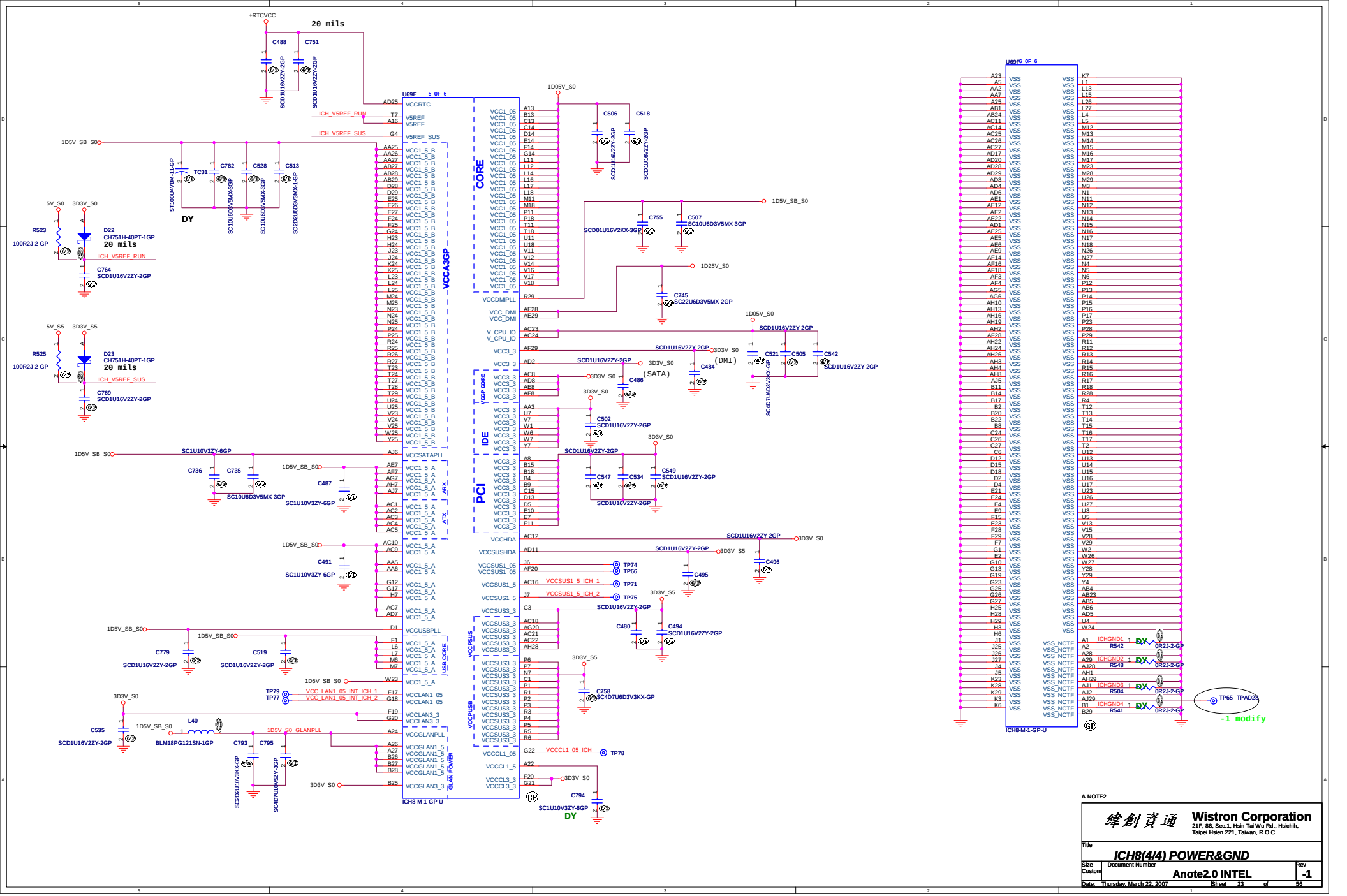
Title: **ICH8(1/4)-PCI/INT**

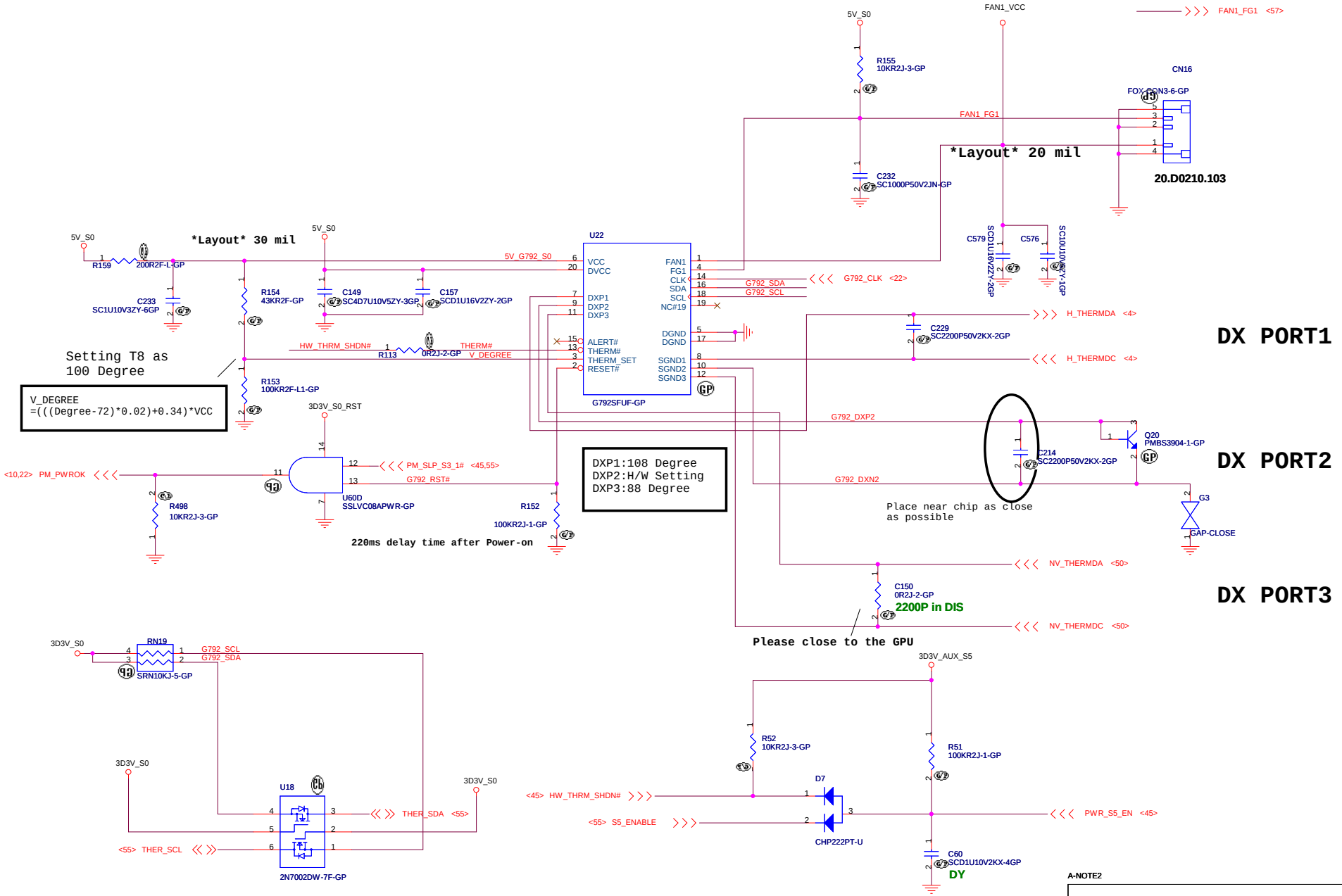
Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 20 of 56





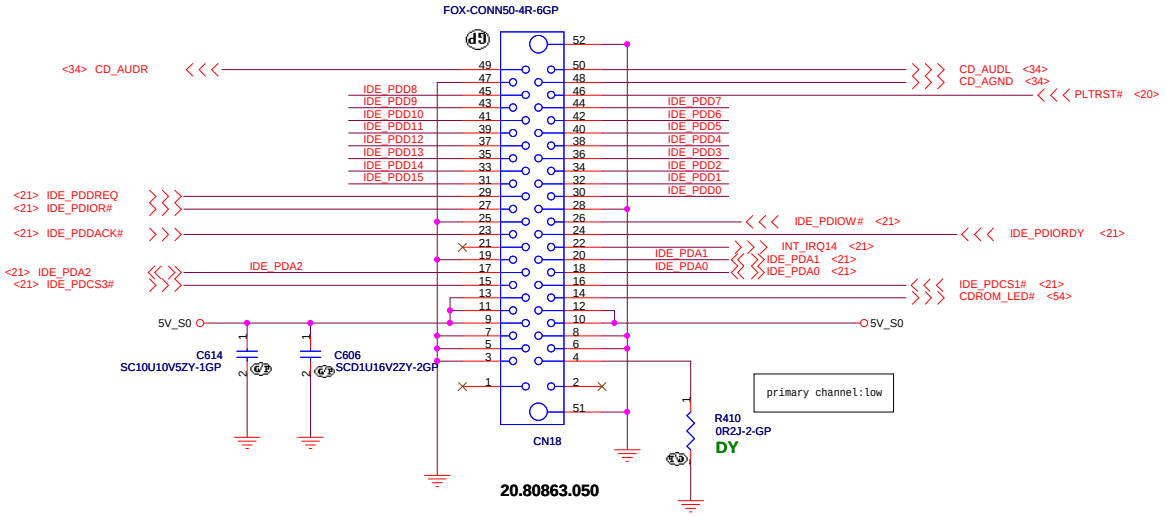




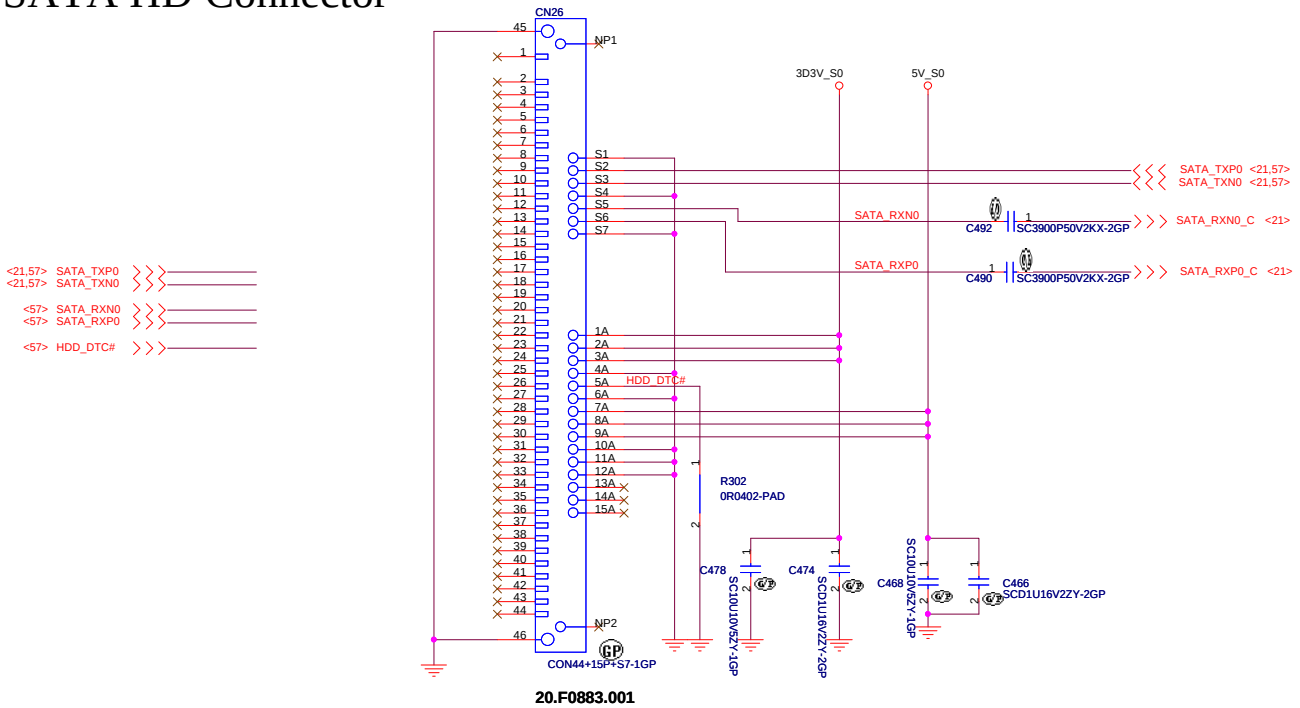
CD-ROM CONNECTOR

Lab1 20.80346.050
Lab2 20.80863.050

IDE_PDD[0..15] <21>



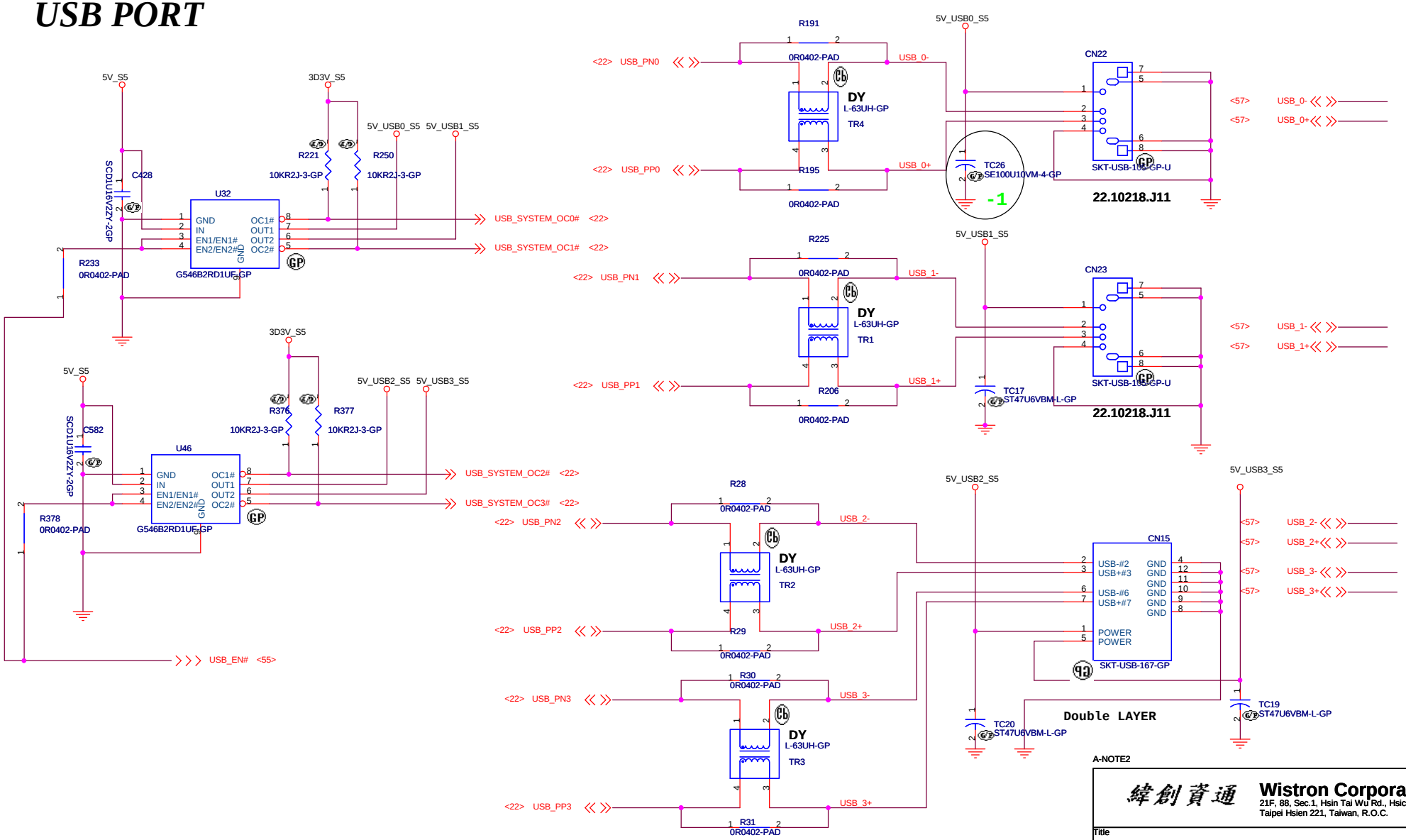
SATA HD Connector



A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HD/CDROM/USB		
Size: A3	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet 25 of 56	

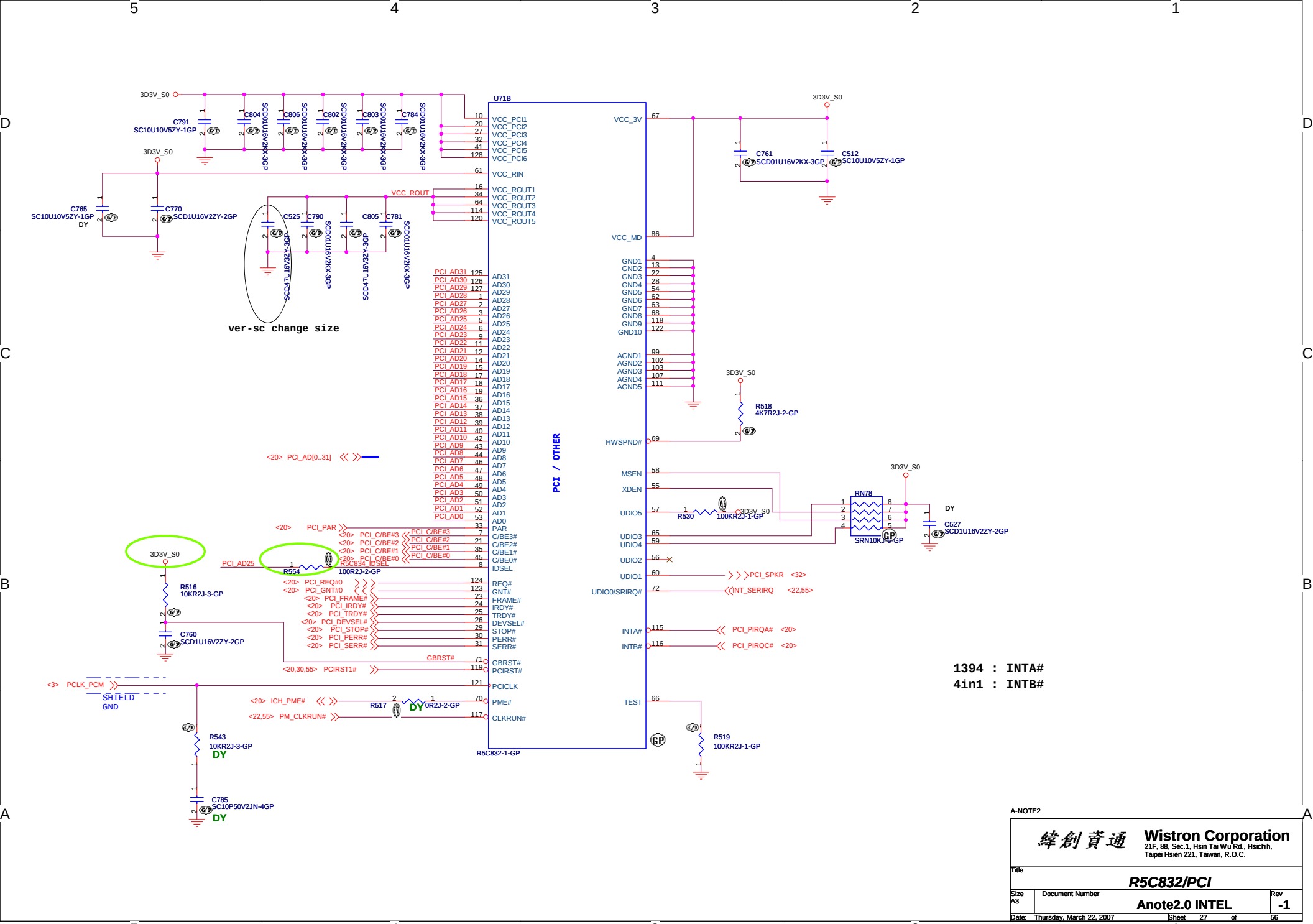
USB PORT

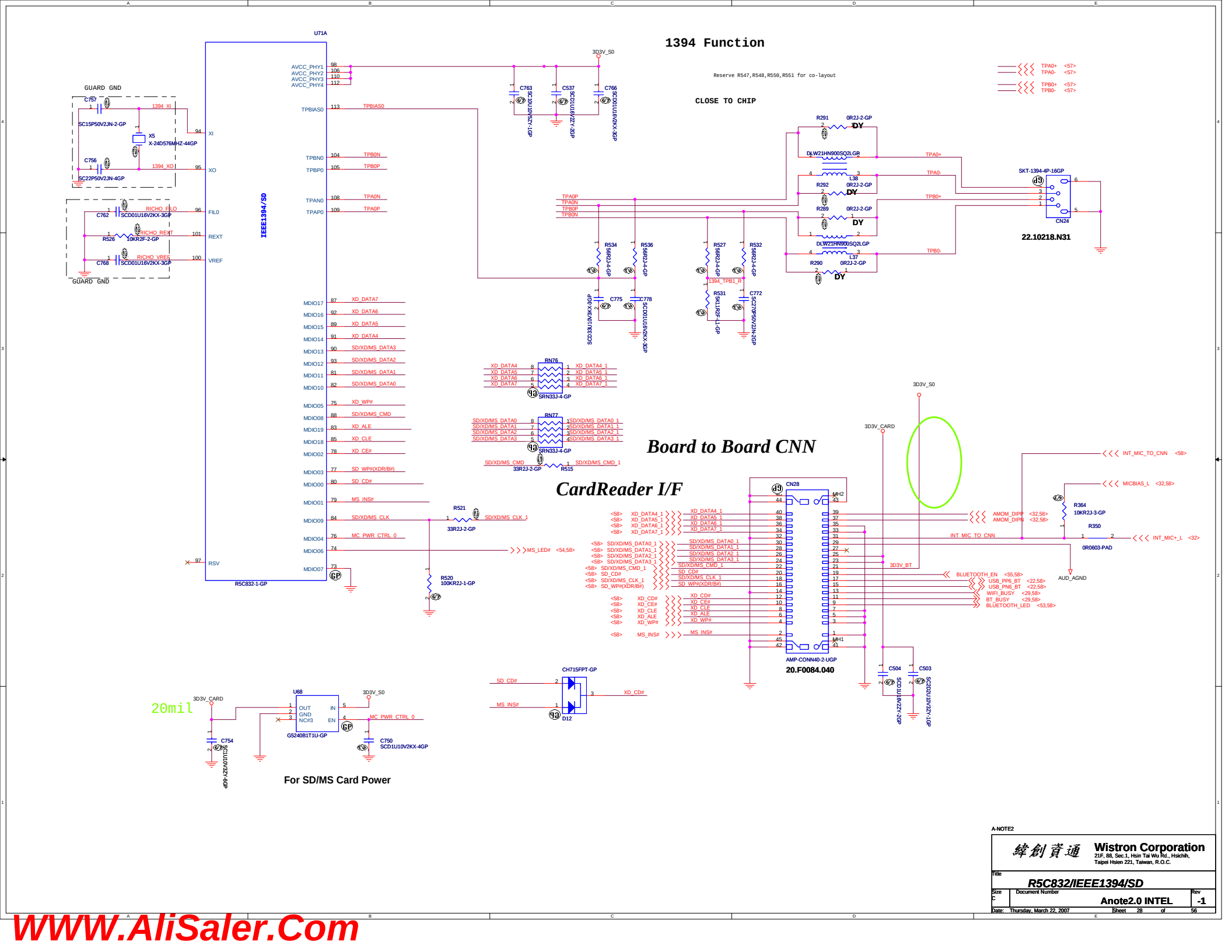


A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**USB I/O**	
Size B	Document Number **Anote2.0 INTEL**	Rev -1
Date: Thursday, March 22, 2007	Sheet 26 of 56	





A-NOTE2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/IEEE1394/SD

Size	Document Number	Rev
C	Anote2.0 INTEL	-1

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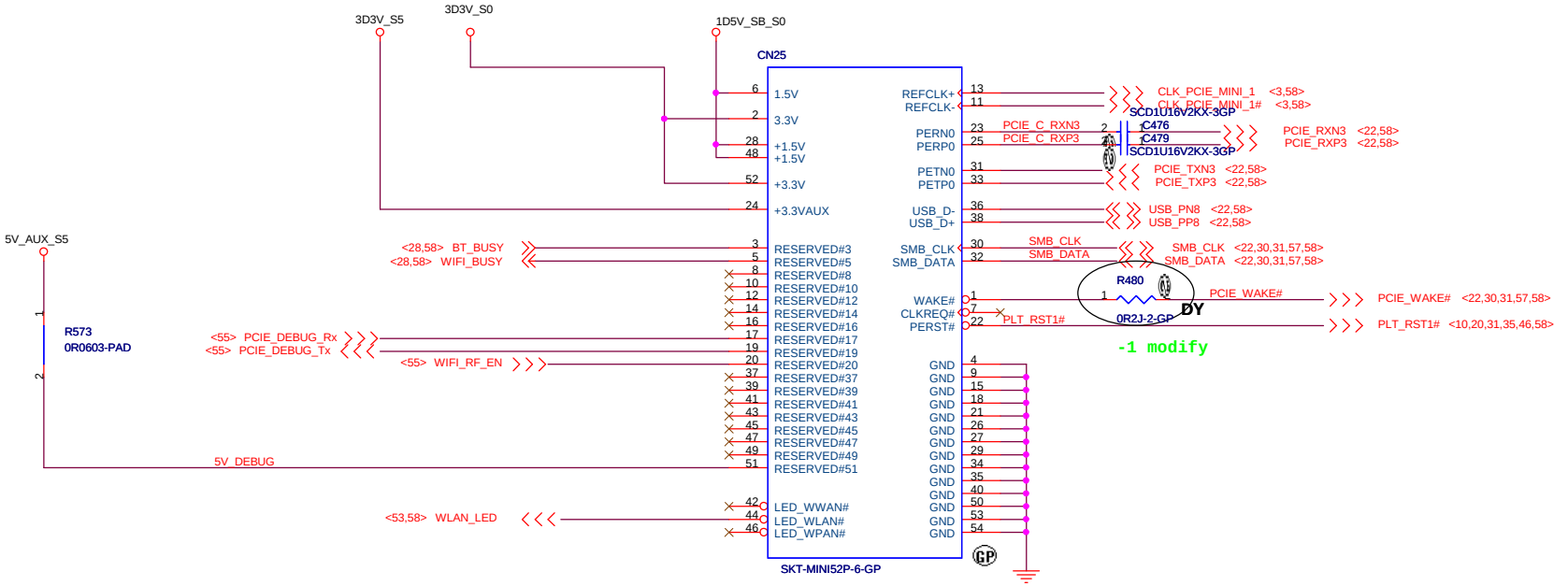
Mini PCI-E Connector

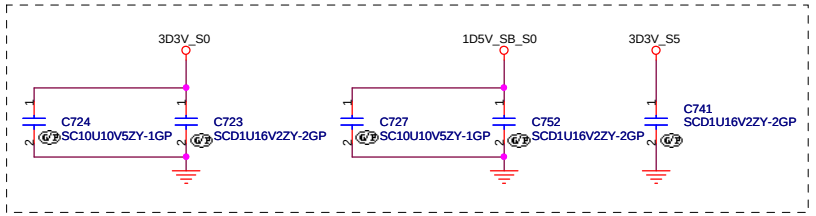
Port-1

Only port-1 support USB



62.10043.261

Note: 9/5 ME updata



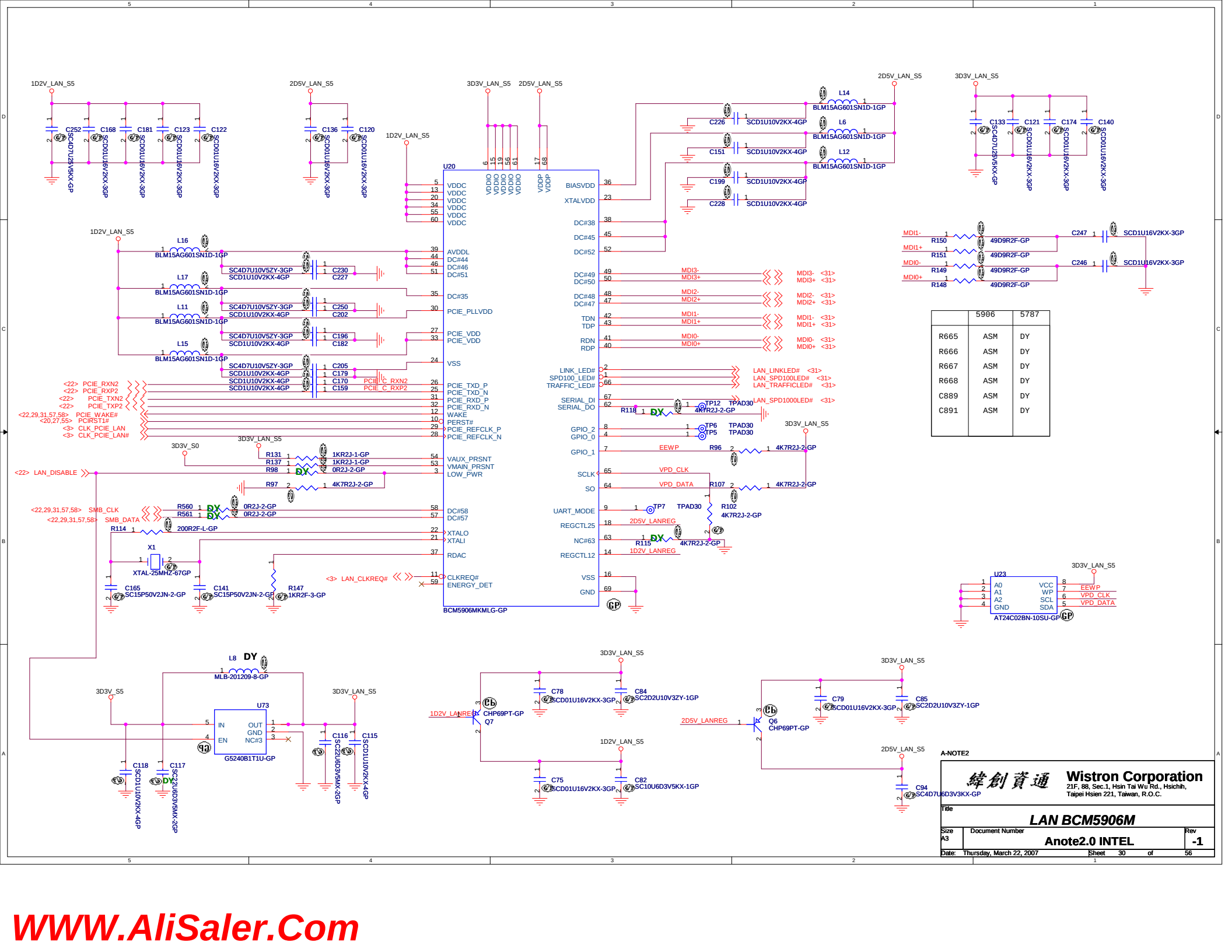
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size: B | Document Number: Anote2.0 INTEL | Rev: -1

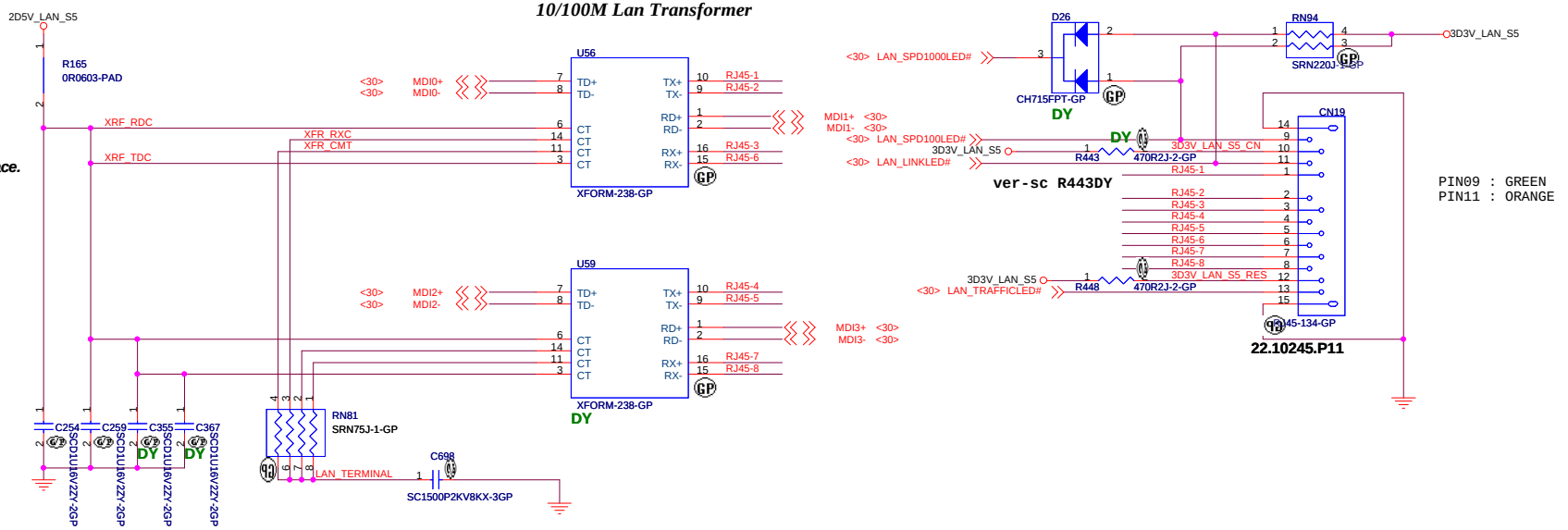
Date: Thursday, March 22, 2007 | Sheet 29 of 56



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

10/100M Lan Transformer

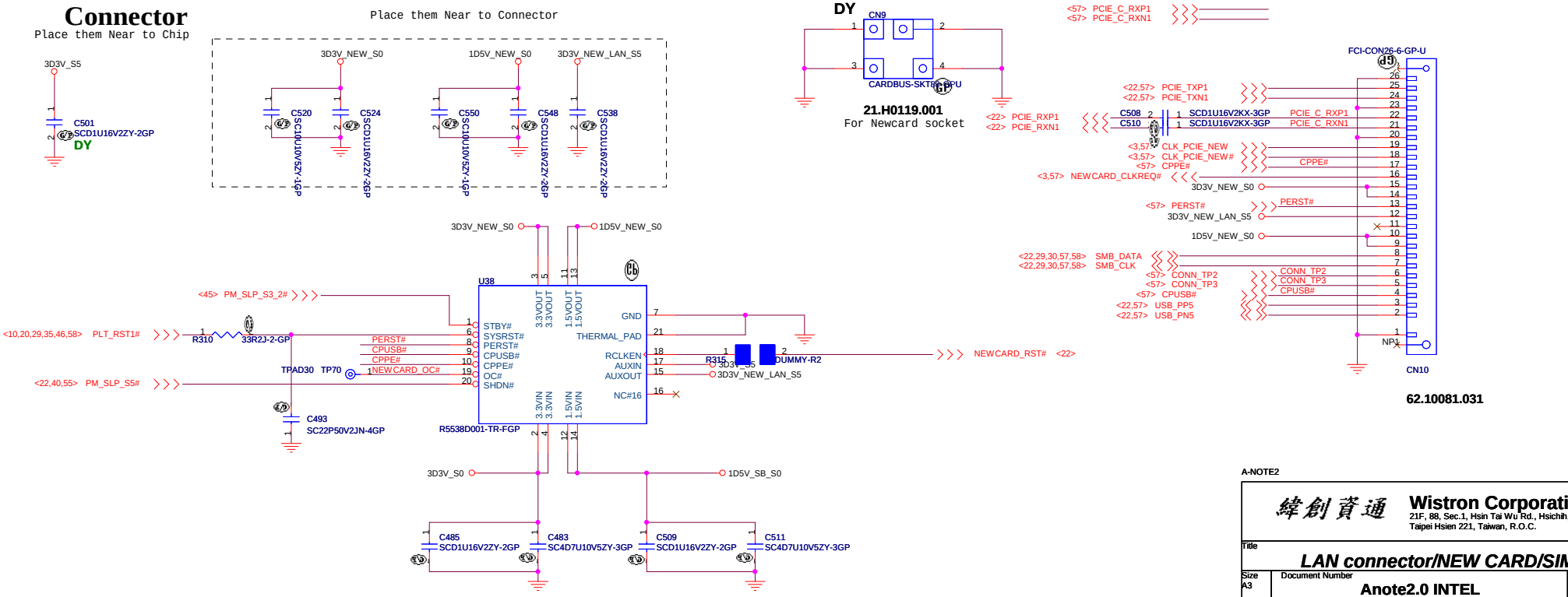
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



NEWCARD Connector

Place them Near to Chip

Place them Near to Connector



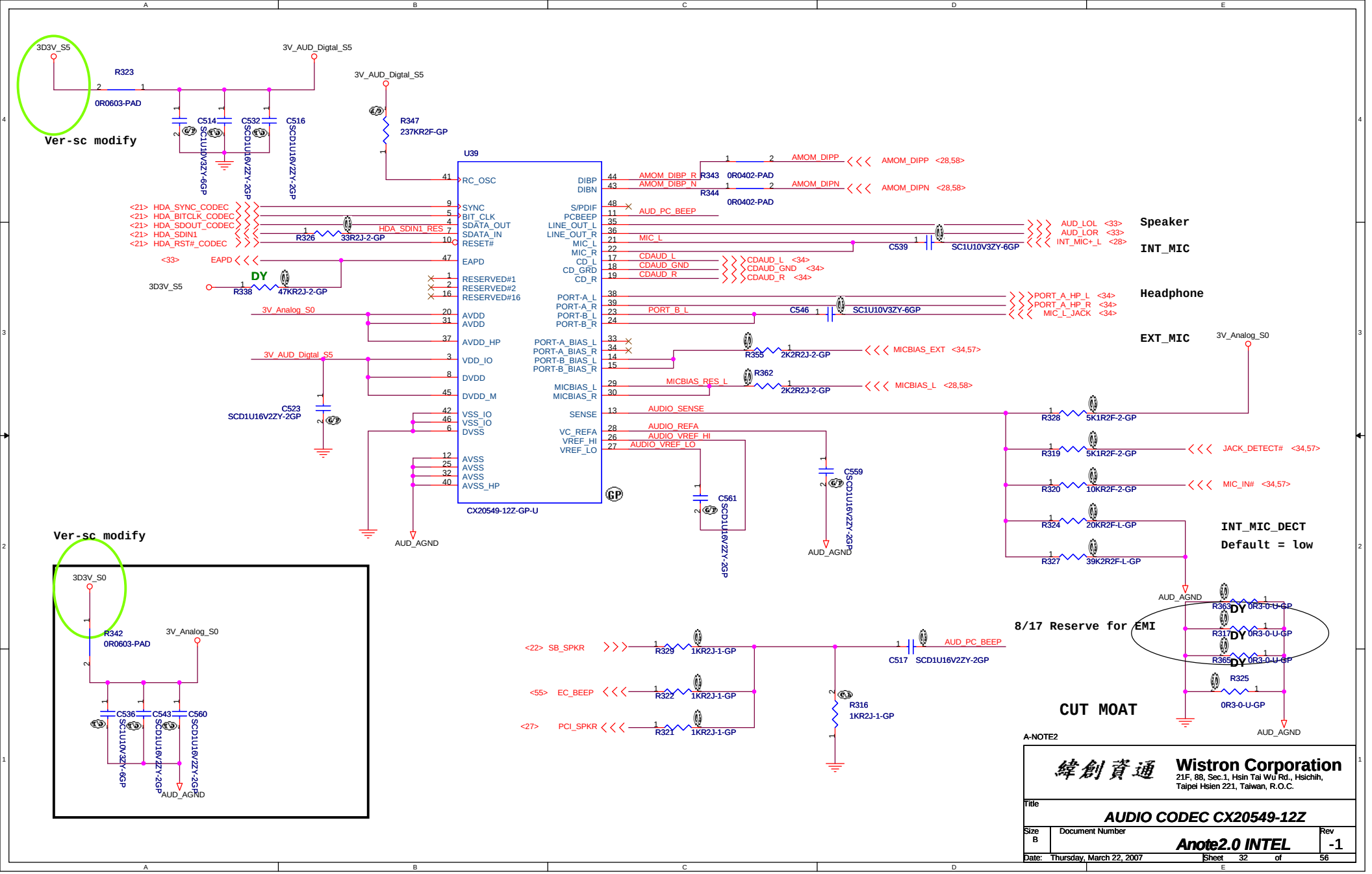
A-NOTE2

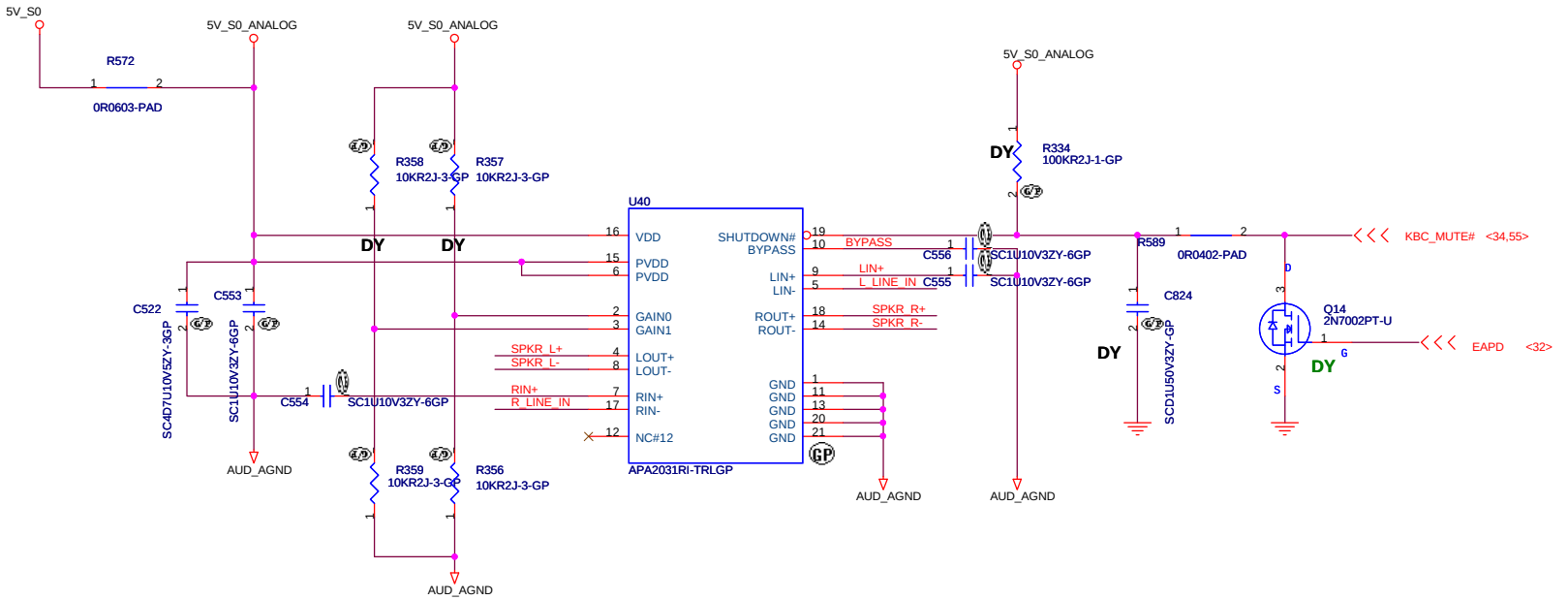
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

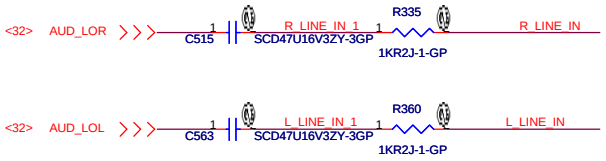
Title: LAN connector/NEW CARD/SIM

Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

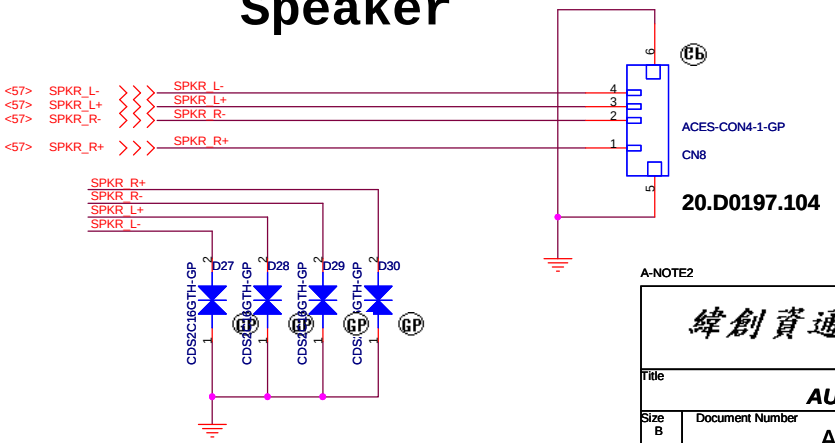
Date: Thursday, March 22, 2007 Sheet 31 of 56





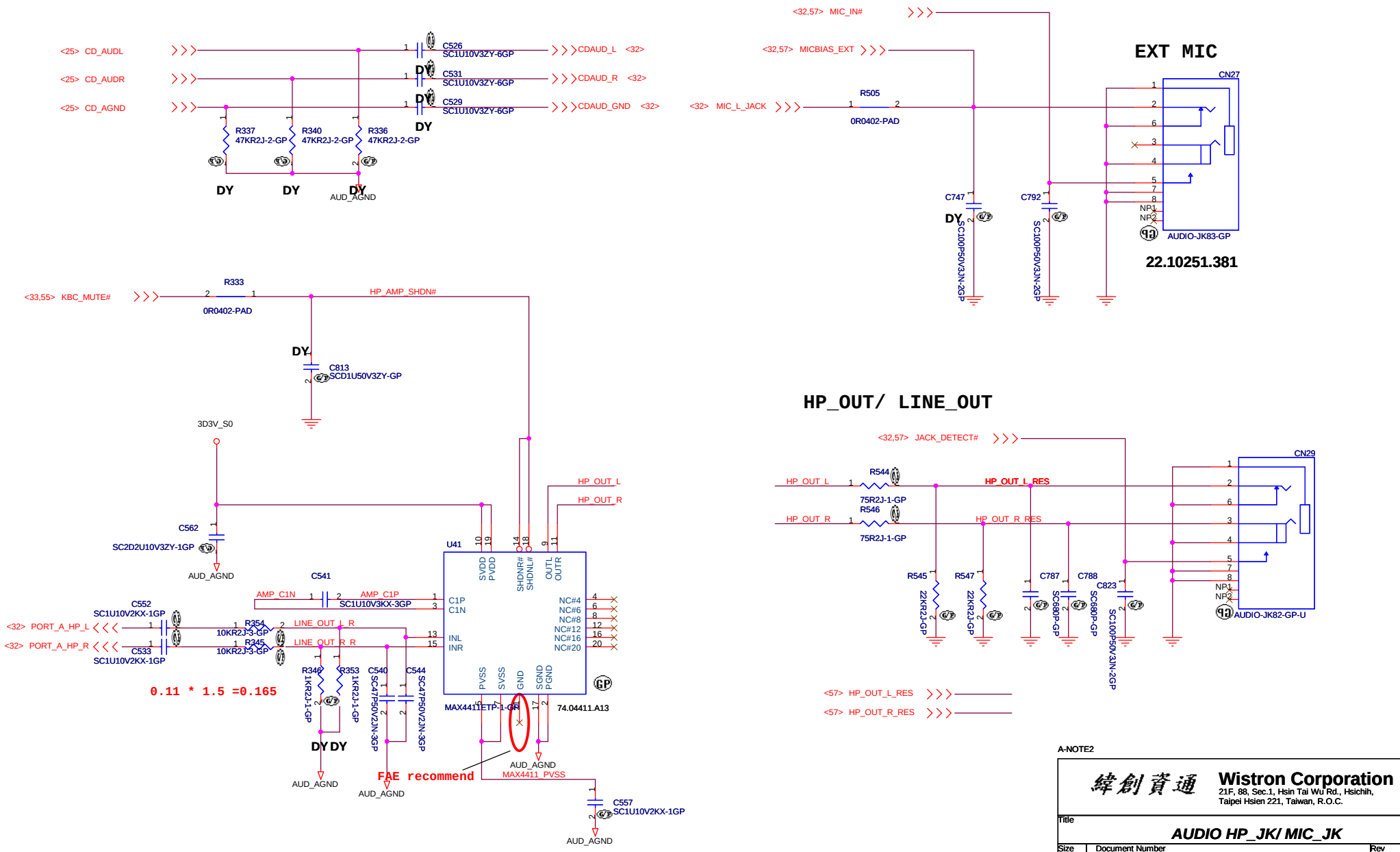


Speaker



A-NOTE2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO AMP/SPEAKER***	
Size: B	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet 33 of 56	

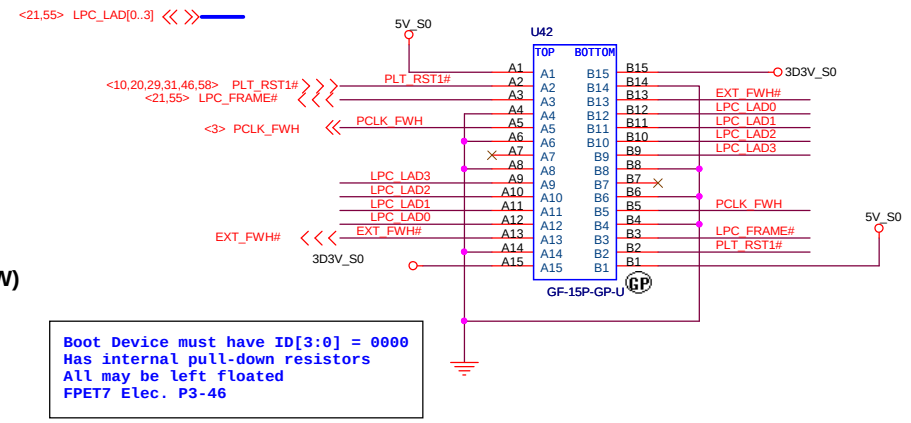


GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

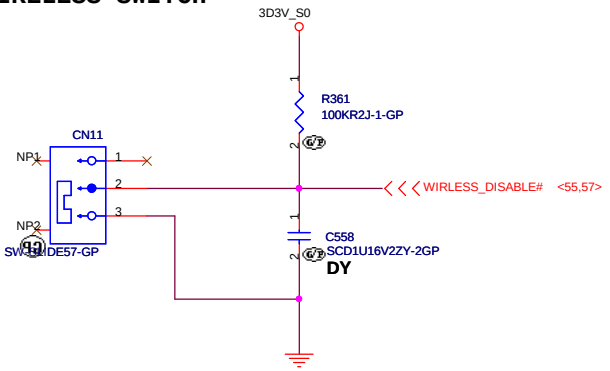
A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

WIRELESS SWITCH



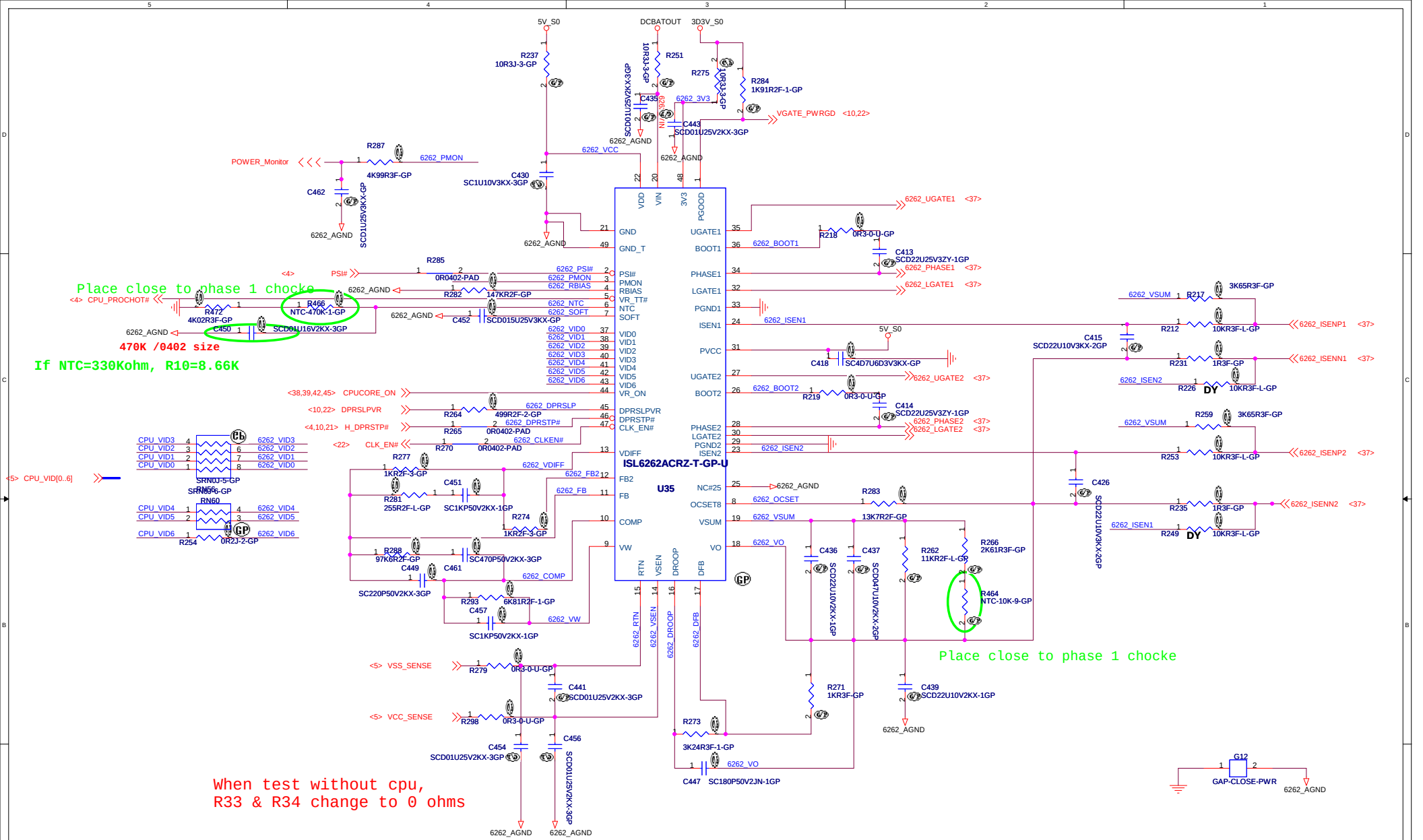
A-NOTE2

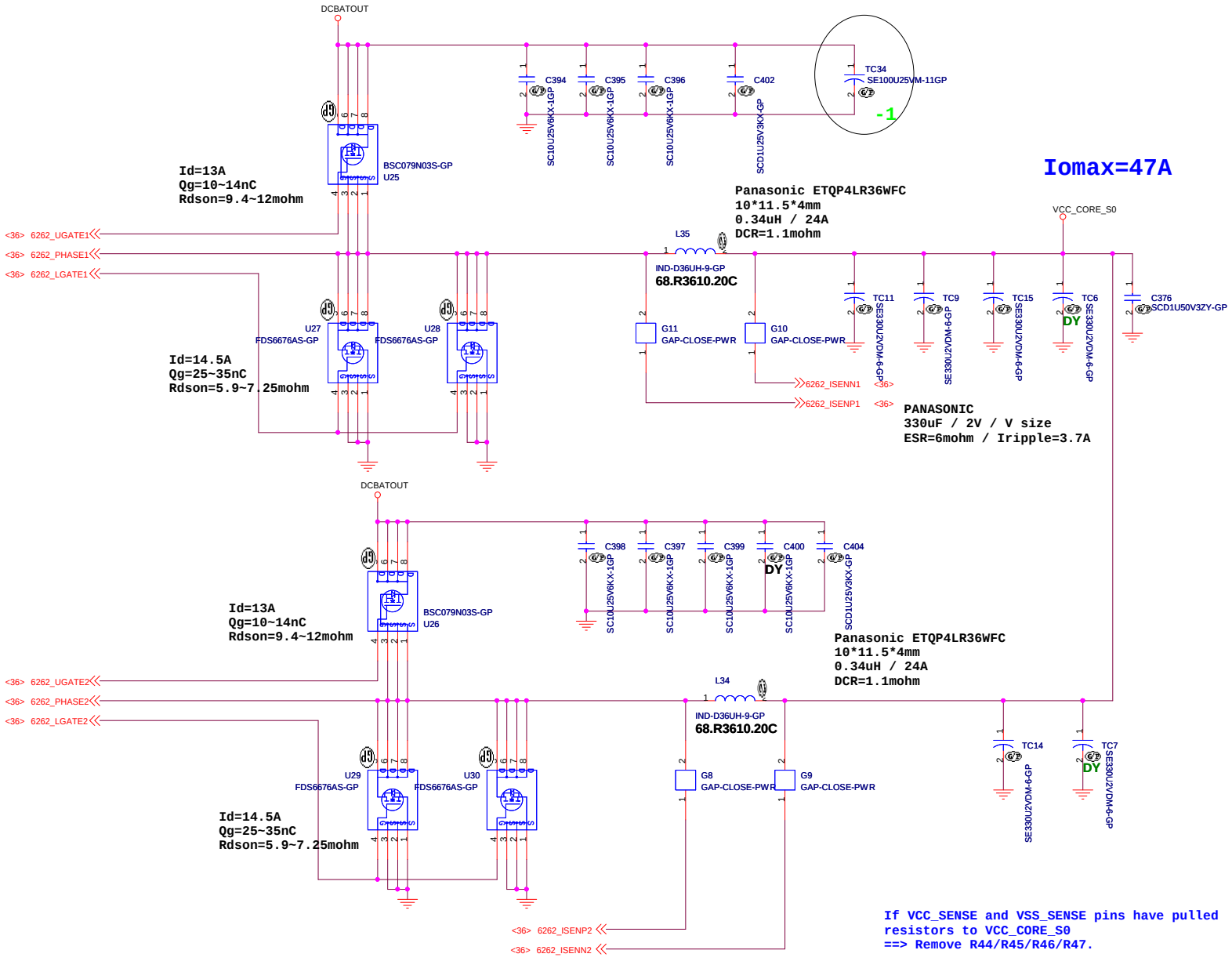
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and Debug

Size: B | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 35 of 56





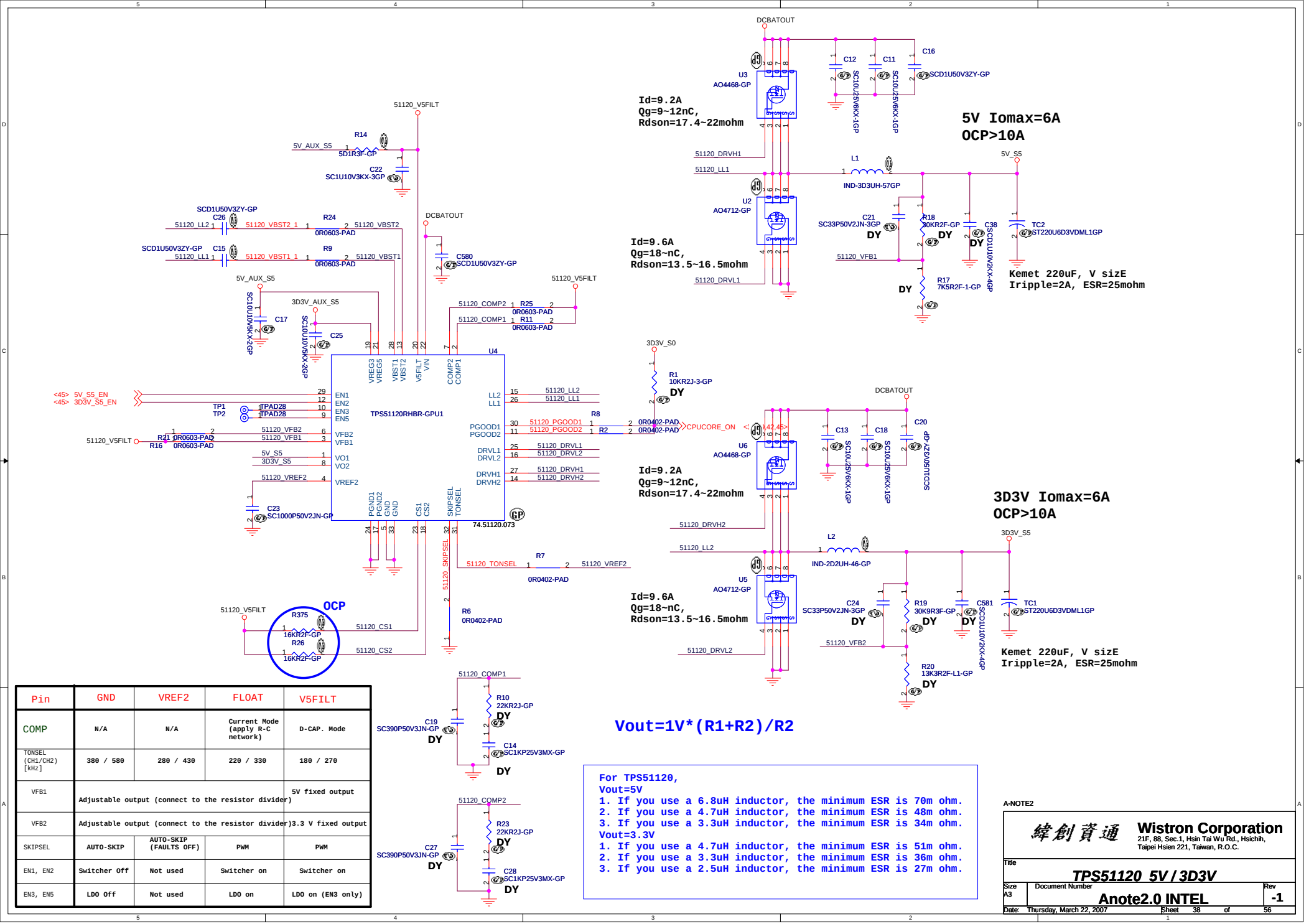
A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VCC_CORE_2*

Size: A3 | Document Number: **Anote2.0 INTEL** | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 37 of 56



Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

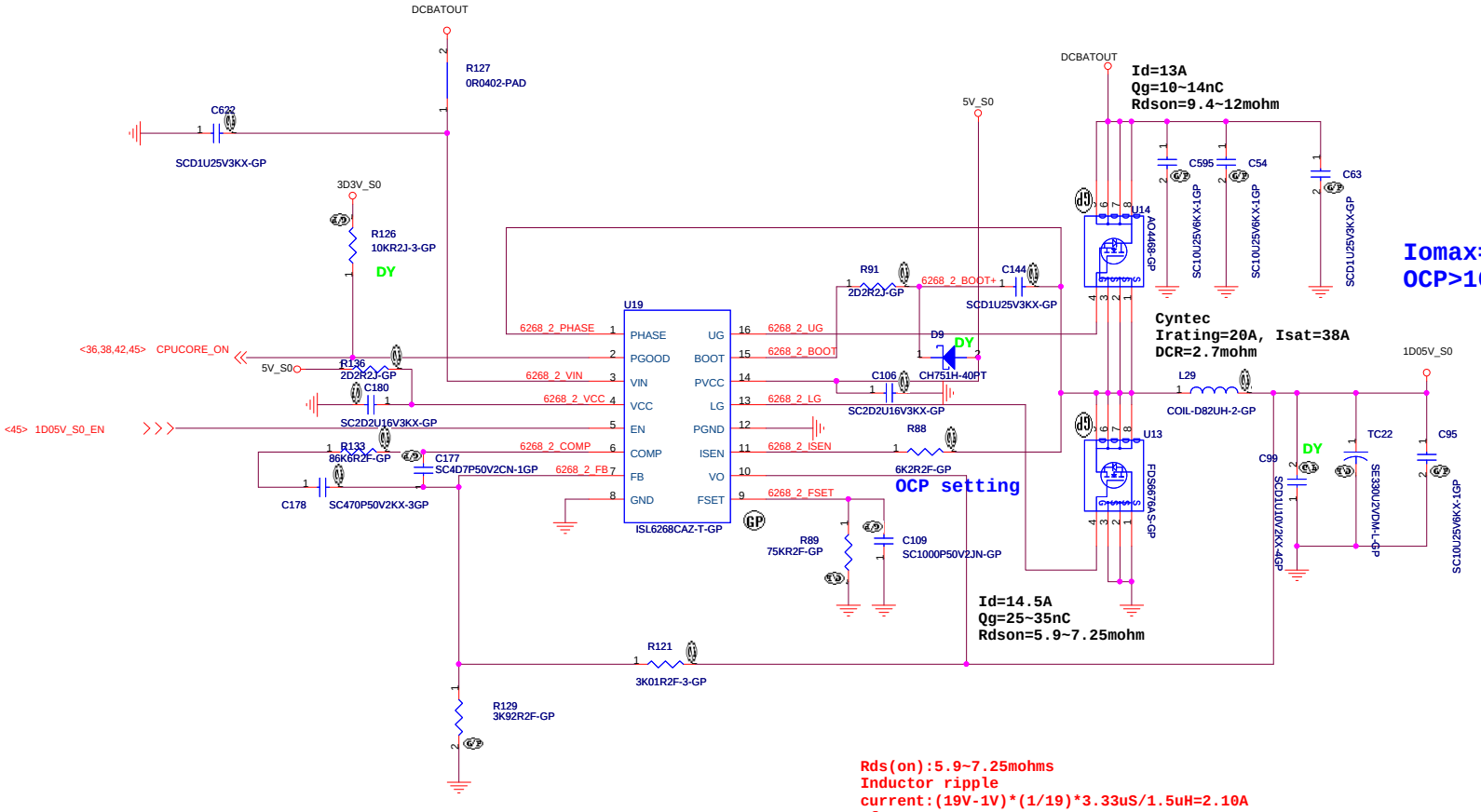
A-NOTE2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 5V / 3D3V

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

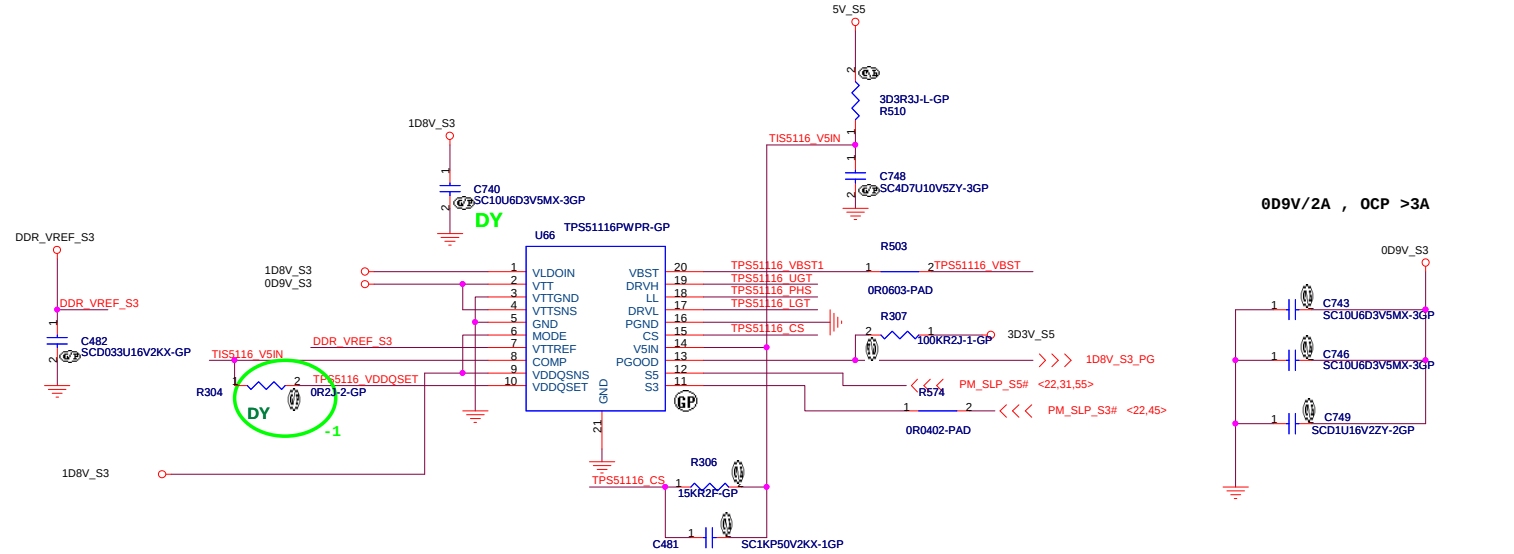
Date: Thursday, March 22, 2007 | Sheet 38 of 56



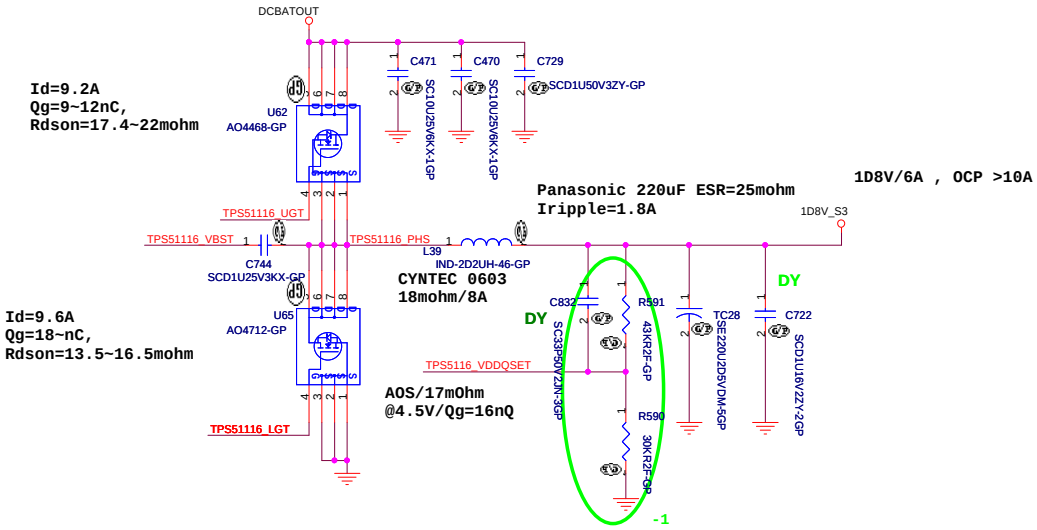
A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D05V_S0_ISL6268		
Size: A3	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet 39 of 56	

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: Anote2.0 INTEL | Rev: -1

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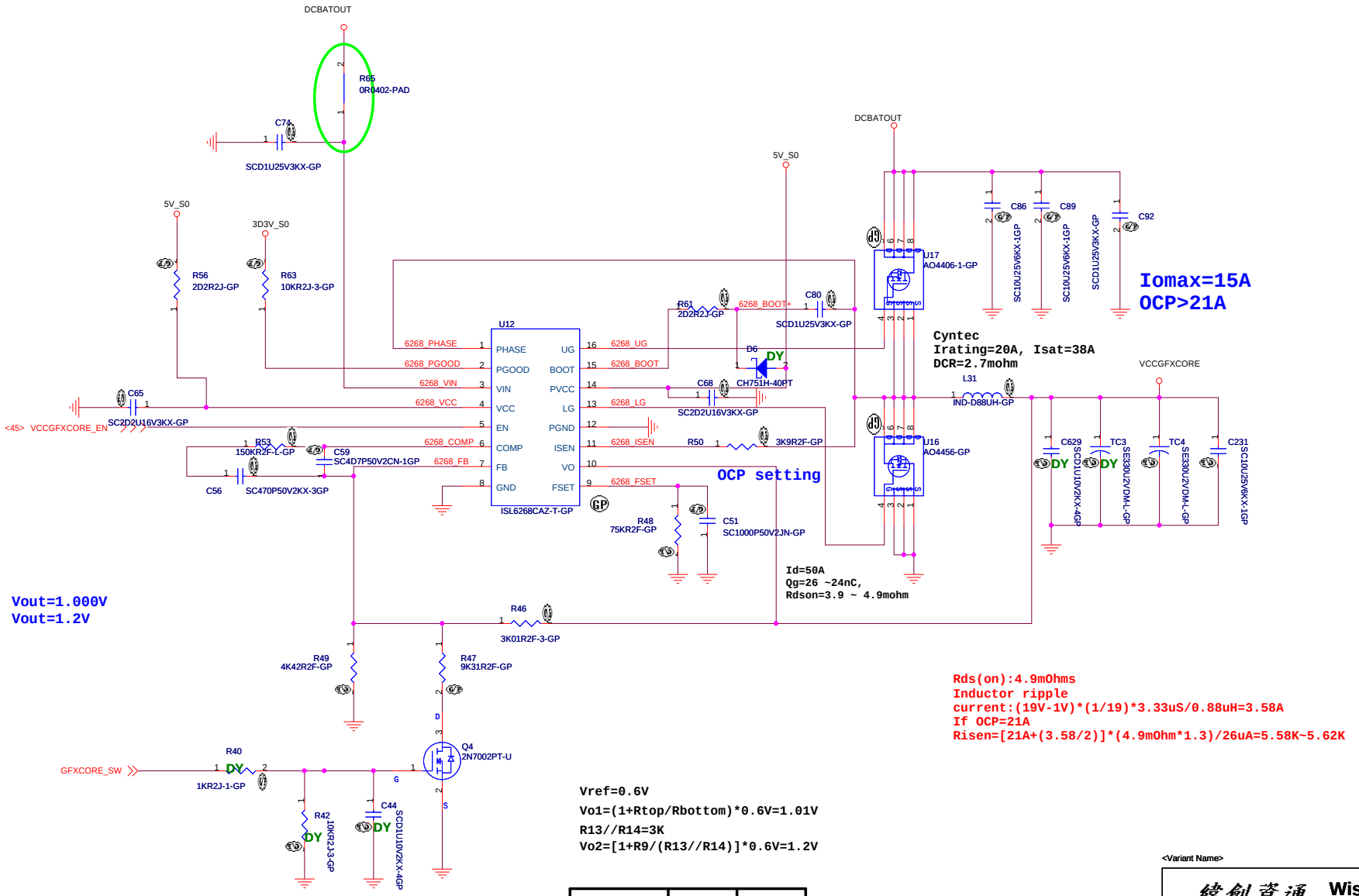
reserve for cost down



Low : Vout=1.000V
High : Vout=1.2V

Rds(on):4.9mOhms
Inductor ripple
current:(19V-1V)*(1/19)*3.33uS/0.88uH=3.58A
If OCP=21A
Risen=[21A+(3.58/2)]*(4.9mOhm*1.3)/26uA=5.58K~5.62K

Vref=0.6V
Vo1=(1+Rtop/Rbottom)*0.6V=1.01V
R13//R14=3K
Vo2=[1+R9/(R13//R14)]*0.6V=1.2V

Vo_Select	Hi	Lo
Vout	1.2V	1.01V

<Variant Name>

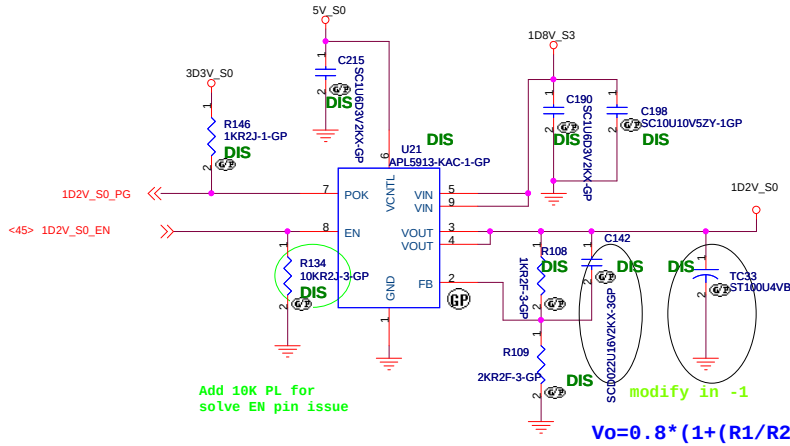
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCGFXCORE(ISL6268)

Size	Document Number	Rev
A3	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 41 of 56

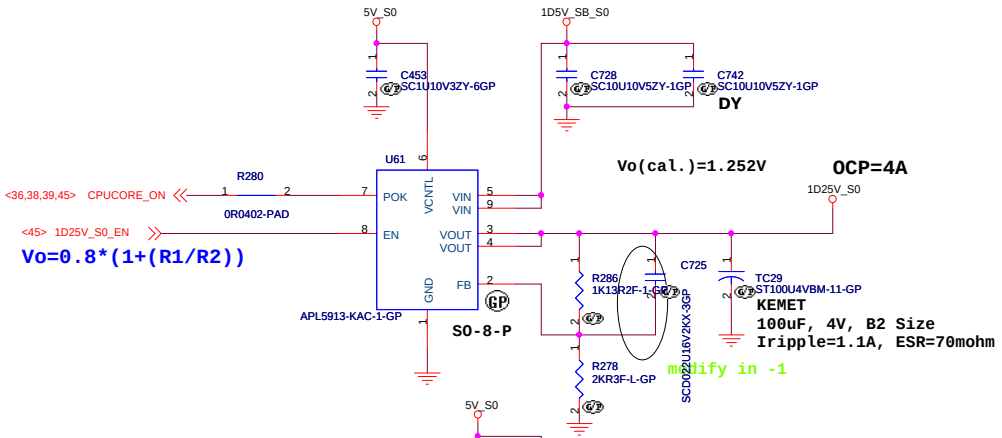
VGA 1.2V Power

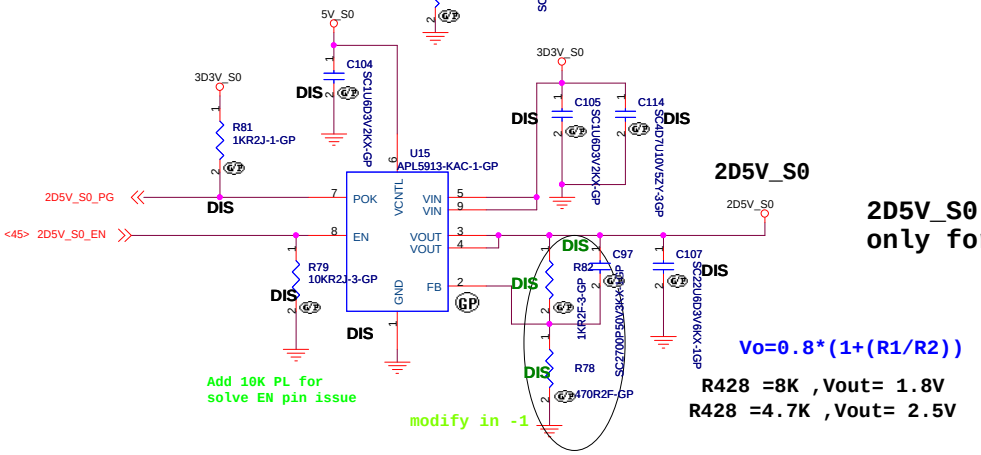


1D5V_NB

PS: SB del

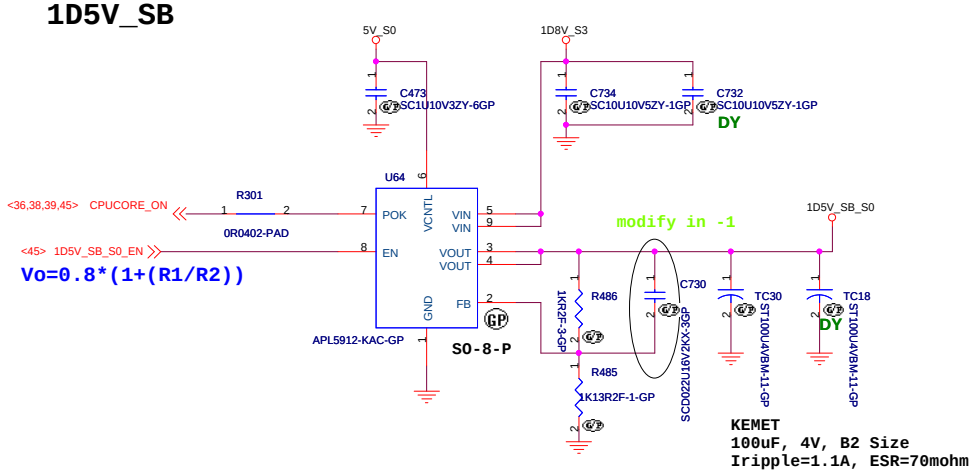
1D25V_S0
Iomax=2.0A





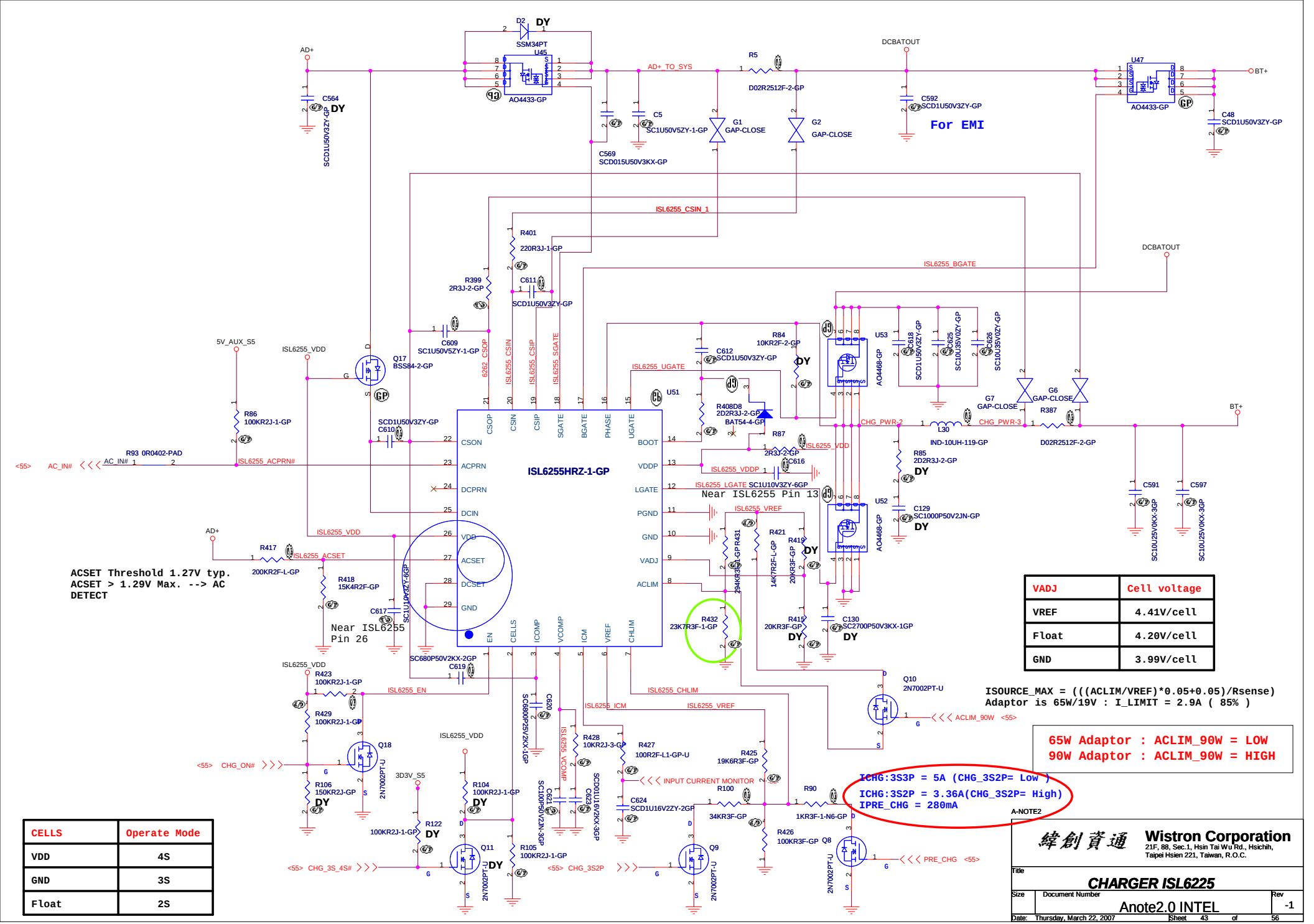
2D5V_S0
only for DISCRETE

1D5V_SB



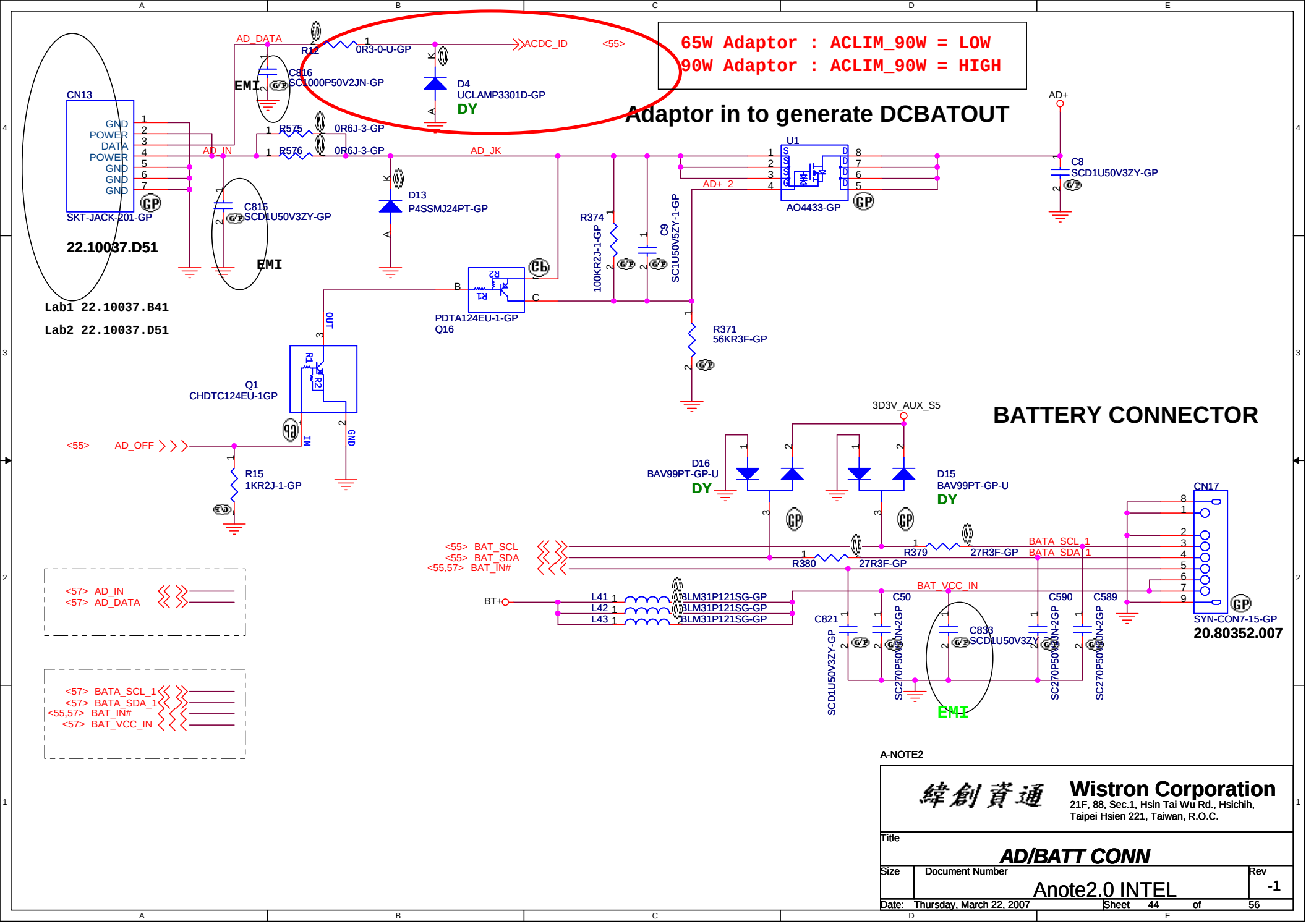
A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *1D2V_VGA/2D5V/1D25V/1D5V LDO*		
Size	Document Number: **Anote2.0 INTEL**	Rev: -1
Date: Thursday, March 22, 2007	Sheet 42 of 56	



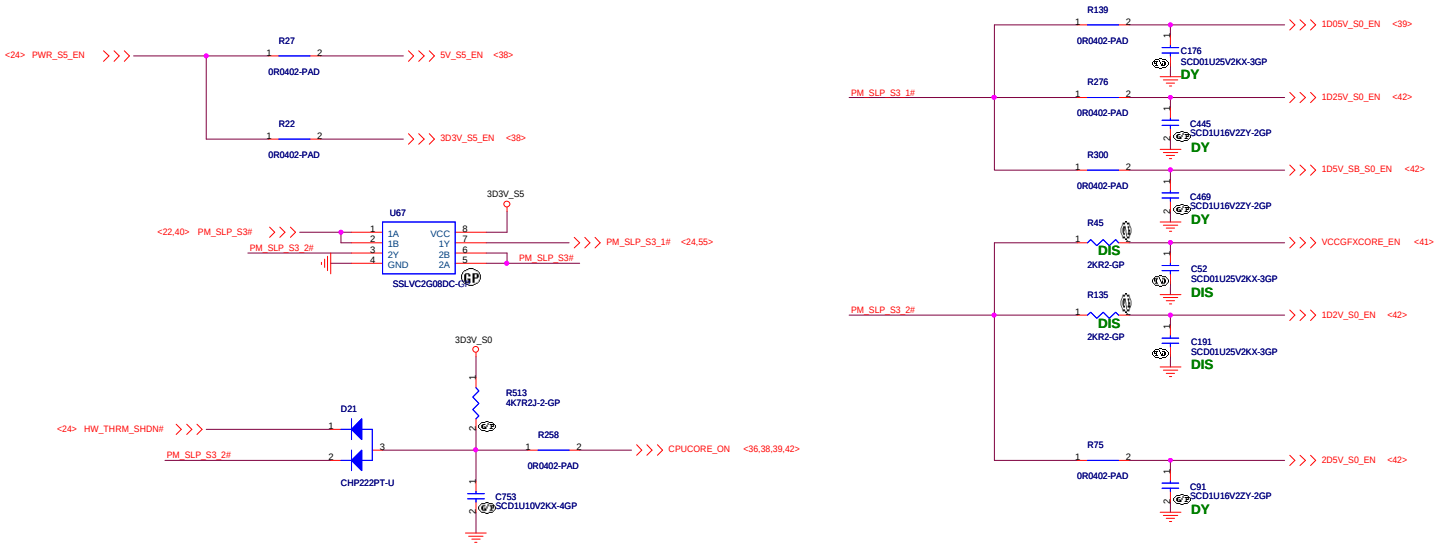
VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

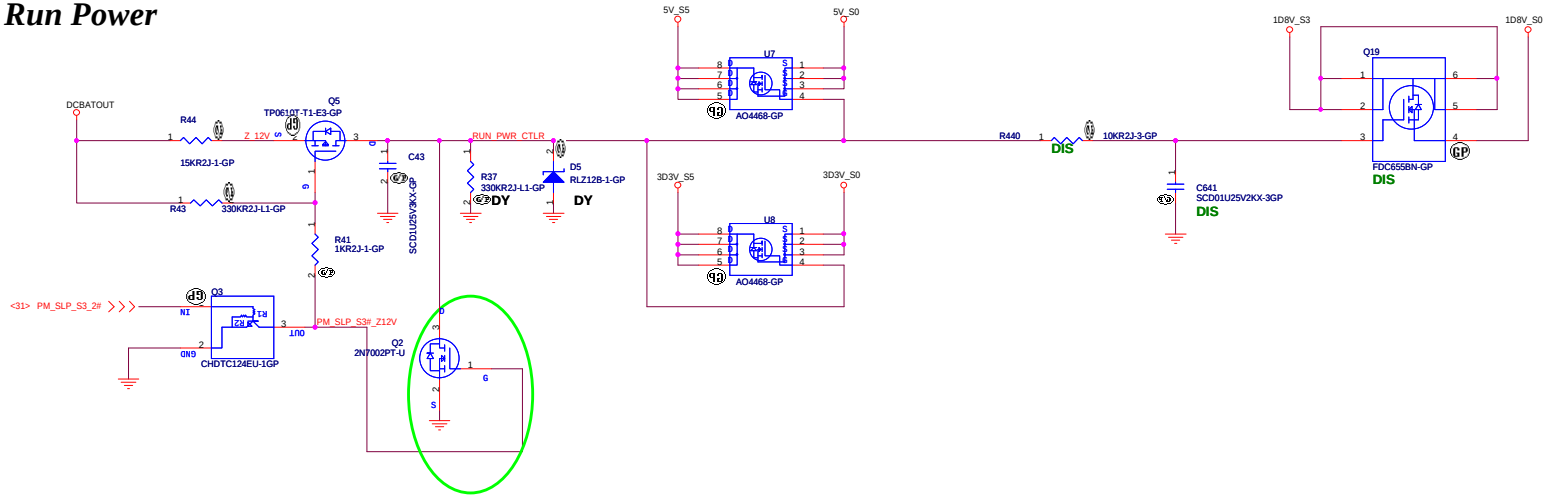


A-NOTE2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size	Document Number Anote2.0 INTEL	Rev -1
Date: Thursday, March 22, 2007	Sheet 44 of 56	



Run Power



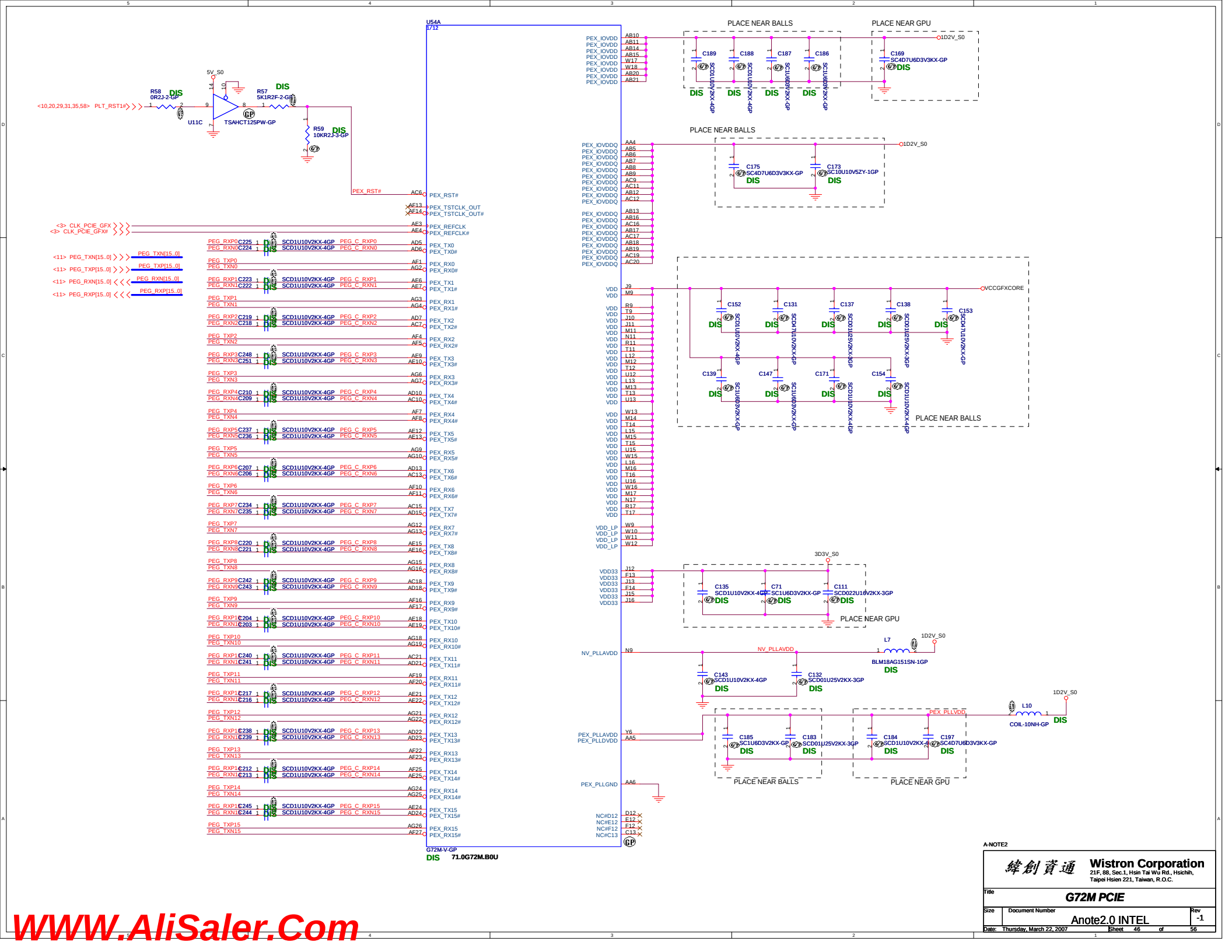
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

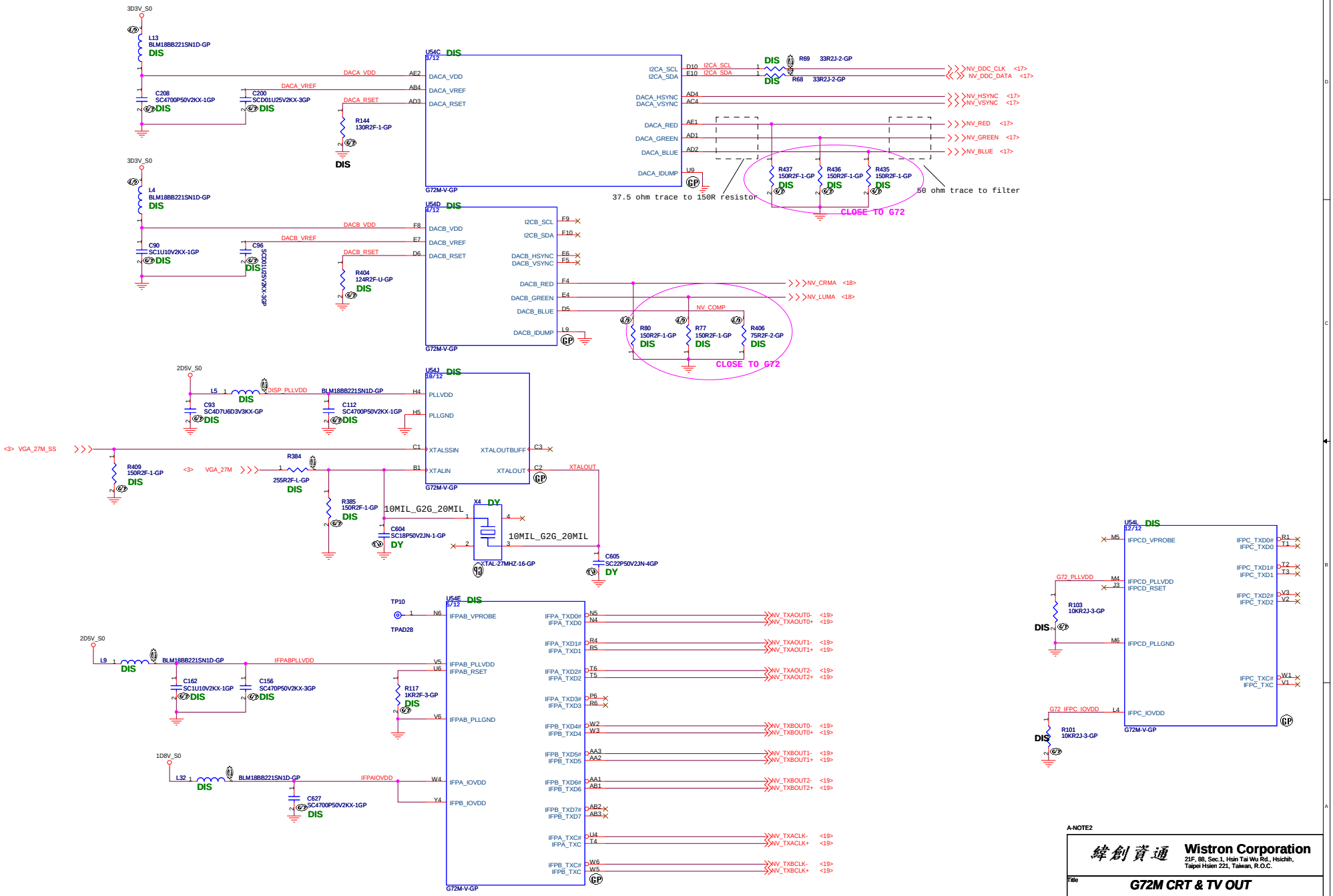
Title: PWRPLANE&RESET LOGIC

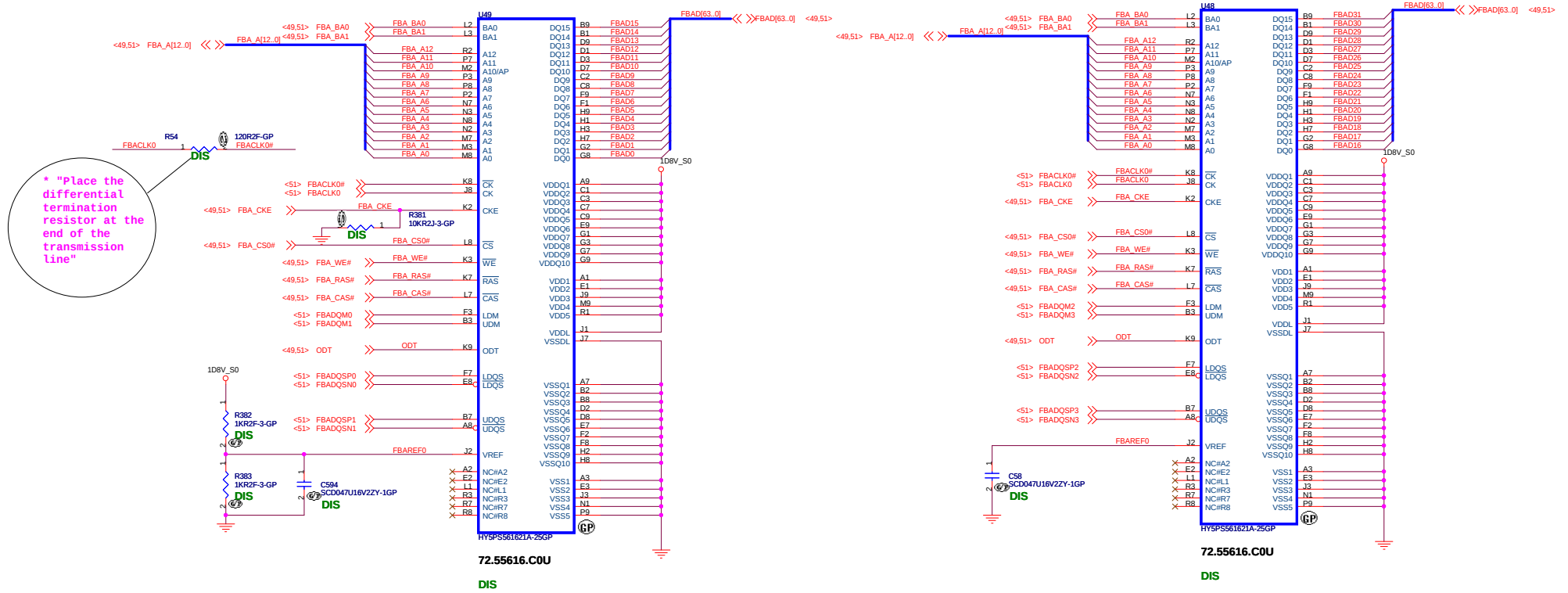
Size	Document Number	Rev
C	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 45 of 56

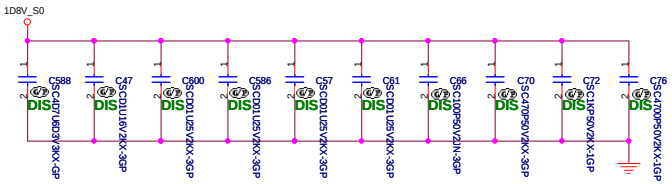


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G72M PCIE
Size	Document Number: Anote2.0 INTEL
Rev	-1
Date: Thursday, March 22, 2007	Sheet 46 of 56

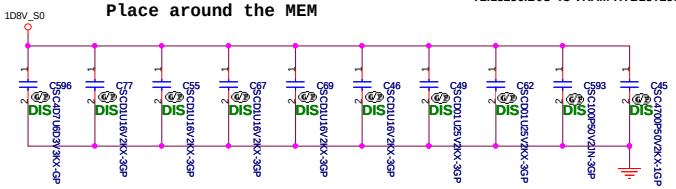




Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)

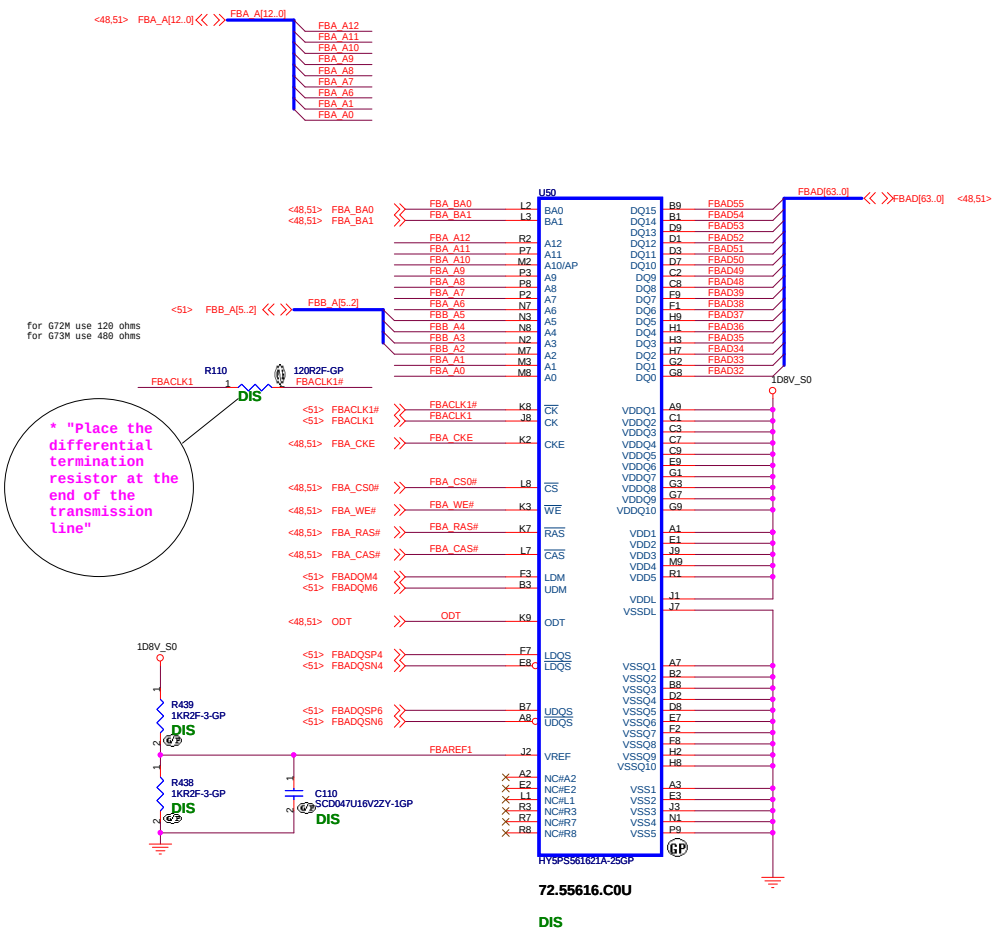
A-NOTE2

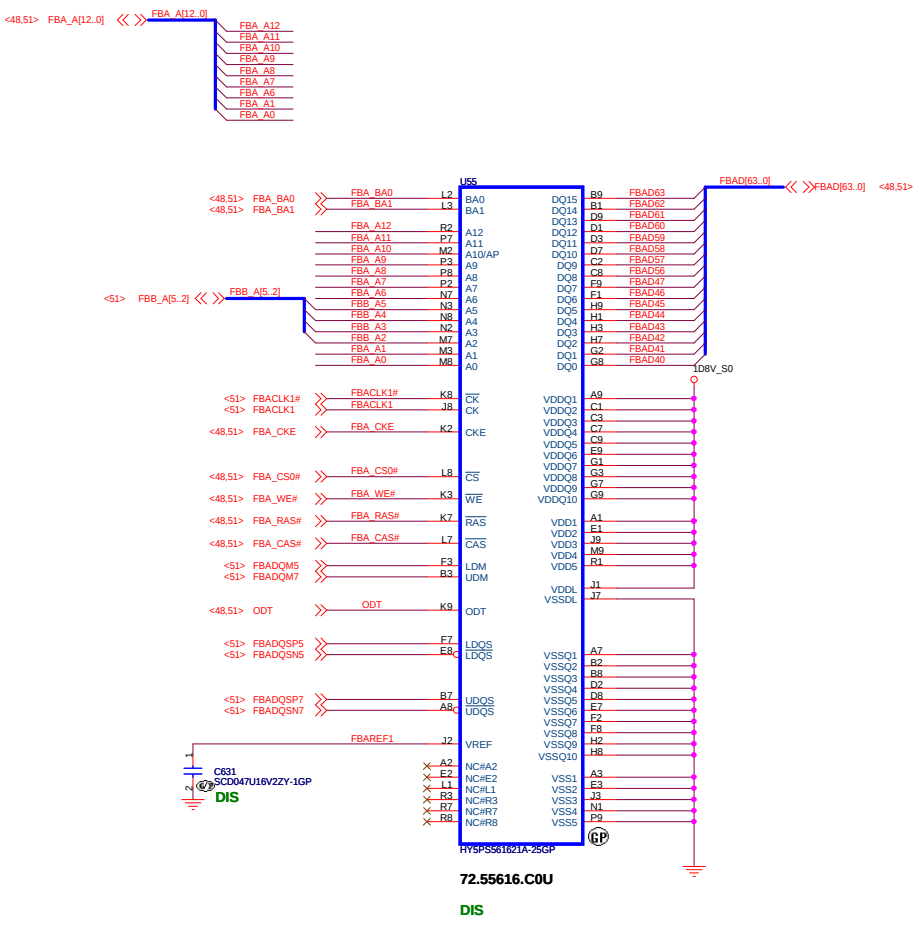
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M VRAM (1ST 1/2)

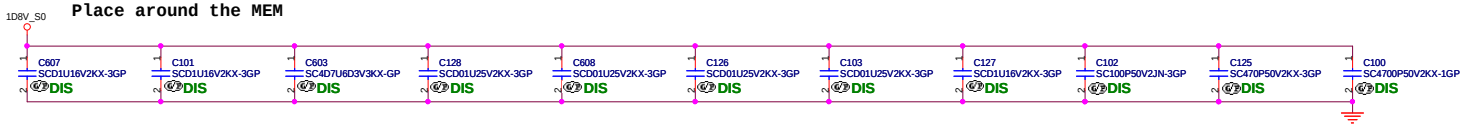
Size	Document Number	Rev
	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 48 of 56

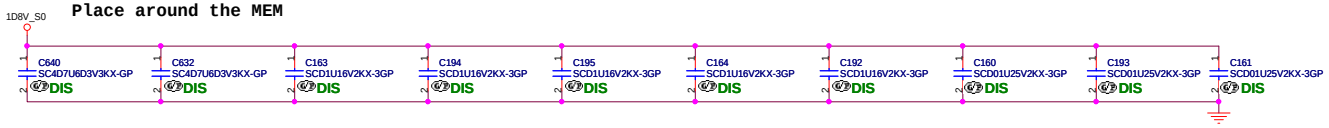




Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



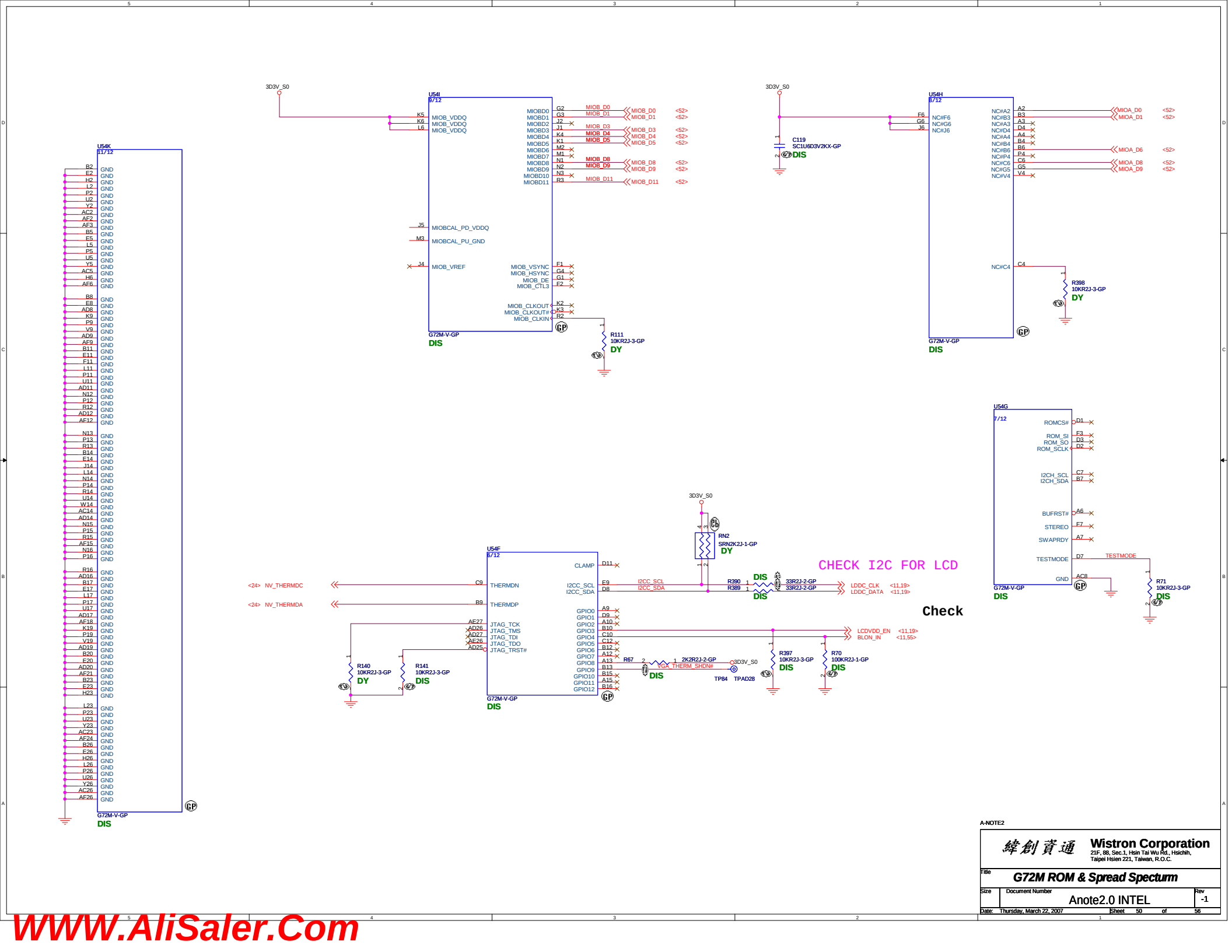
A-NOTE2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M VRAM (1ST 2/2)

Size	Document Number	Rev
	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 49 of 56



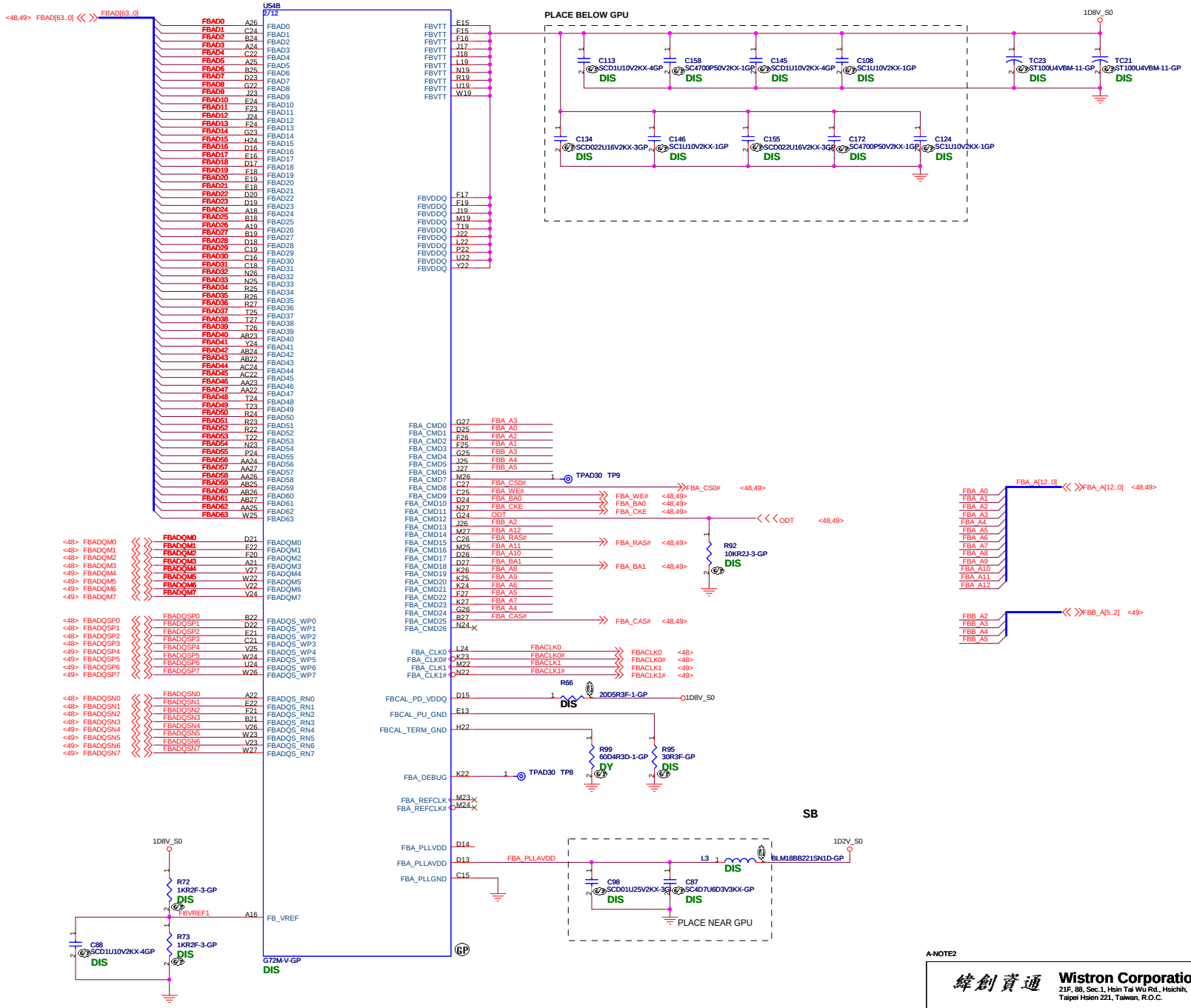
A-NOTE2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M ROM & Spread Specturm

Size	Document Number	Rev
	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 50 of 56



A-NOTE2

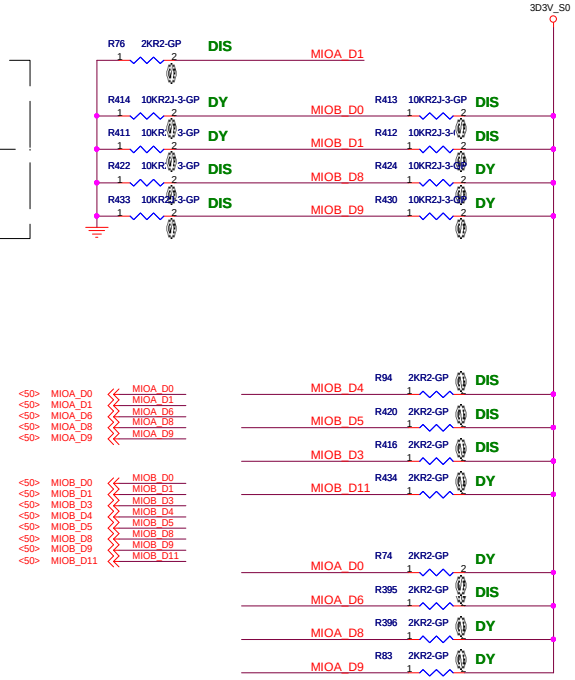
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G72M MEMORY IF 1	
Size	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet 51 of 56	

STRAPS, Mechanical Parts

Check

Hynix256MB :	R825_0	R824_1	R822_1	R820_1
Hynix128MB :	R825_0	R823_0	R822_1	R820_1
Hynix64MB :	R826_1	R823_0	R822_1	R820_1
Infineon256MB :	R825_0	R824_1	R822_1	R819_0
Infineon128MB :	R825_0	R823_0	R822_1	R819_0
Infineon64MB :	R826_1	R823_0	R822_1	R819_0



Bit	Signal	Values
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS

For MEM strapping, Please use below table:

RAM_CFG[9.8.1.0] RAM_CFG[3..0]	Config	FB Bus Width	Definitions
0000			
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100			
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

MIOB_D4:	PCI_DEVID_0	
MIOB_D5:	PCI_DEVID_1	1000 (default 0x00FC)
MIOB_D3:	PCI_DEVID_2	
MIOB_D11:	PCI_DEVID_3	0111 G72MV **G72MZ=6,G73=8**

MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6:	3GIO_PADCFG_LUT_ADDR[0]	
MIOA_D8:	3GIO_PADCFG_LUT_ADDR[1]	
MIOA_D9:	3GIO_PADCFG_LUT_ADDR[2]	001 DEFAULT

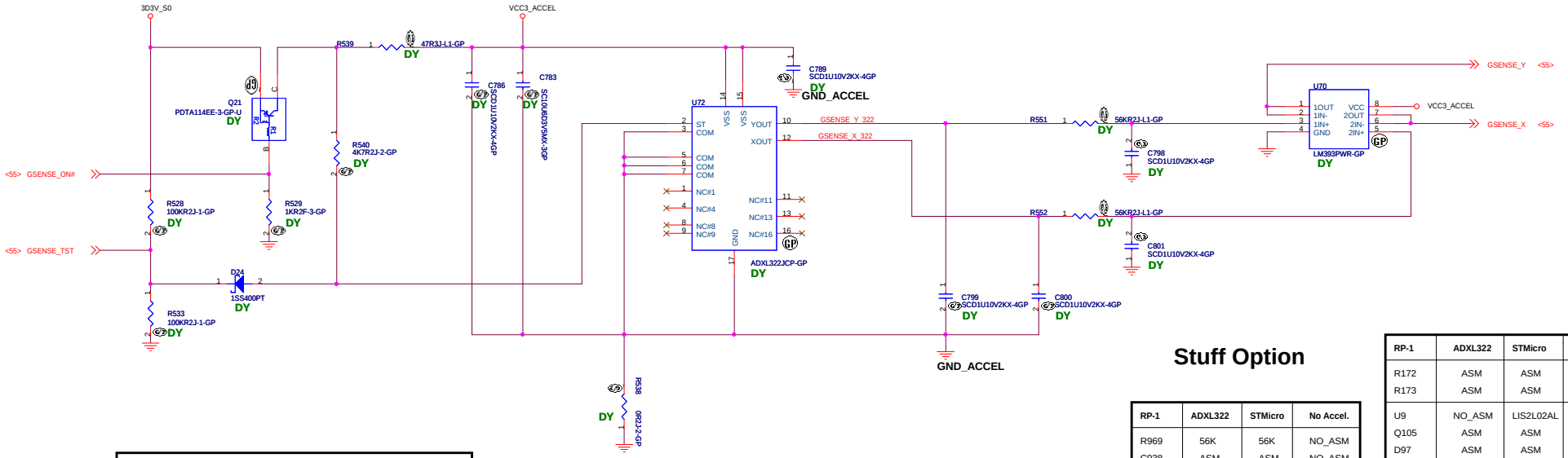
A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G72M STRAPPING***

Size	Document Number	Rev
	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 52 of 56



Stuff Option

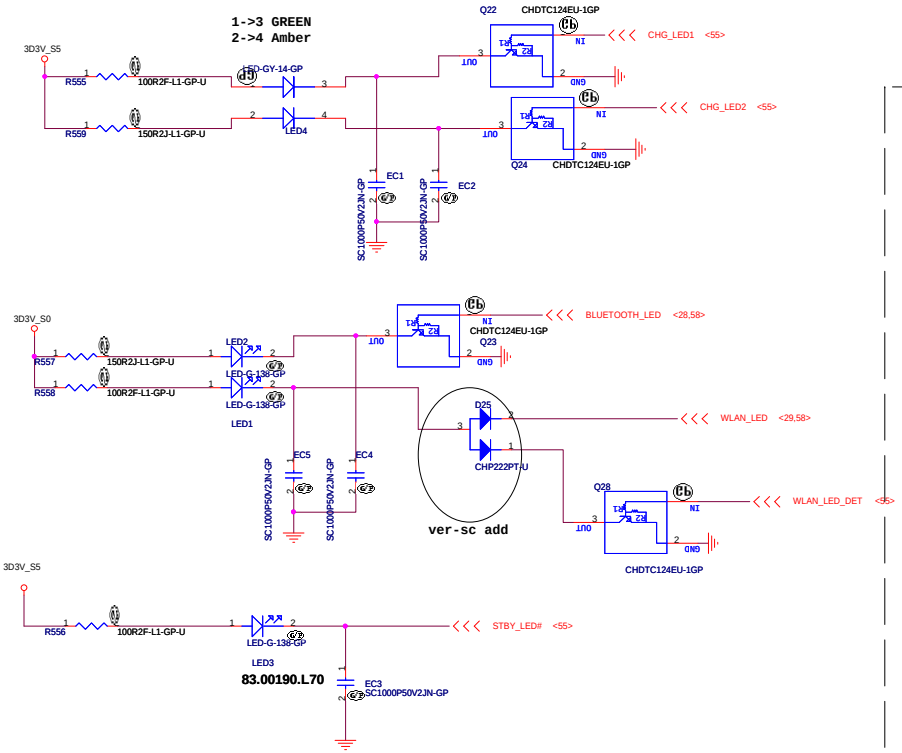
RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

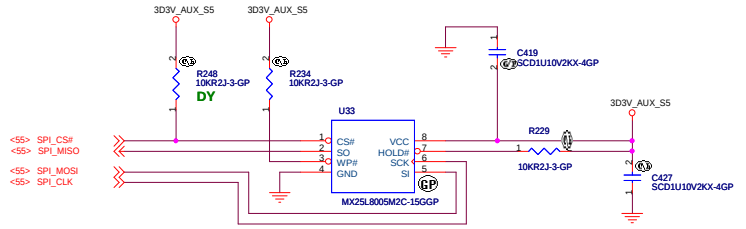
A-note 2.0 LED's Location and Sequence

Left side — Right side

WLAN Bluetooth Battery Suspend



SPI ROM for System & KBC



1. MXIC MX25L8005M2C
2. WINBOND W25X80
3. SST 8Mbit72.25080.G01

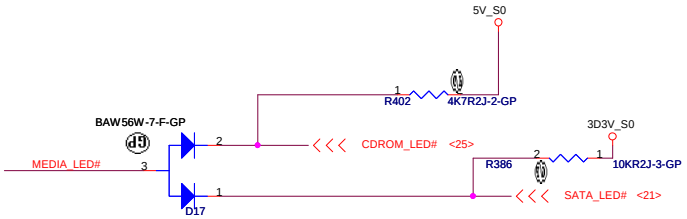
A-NOTE2

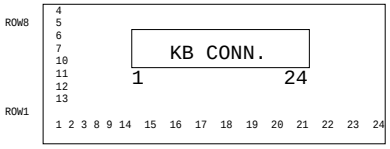
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G-sensor / SPI / LEDs

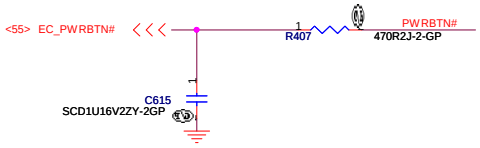
Size: C | Document Number: Anote2.0 INTEL | Rev: -1

Date: Thursday, March 22, 2007 | Sheet 53 of 56

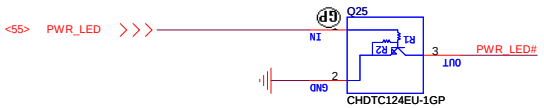


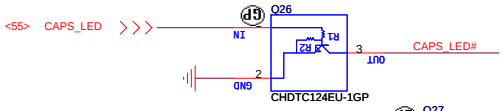


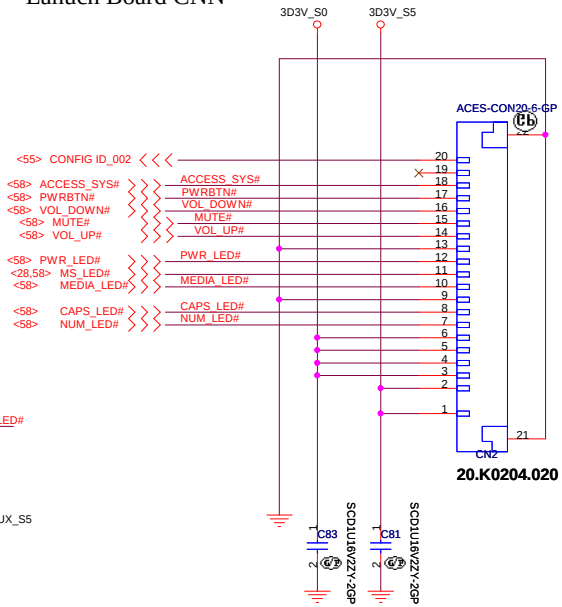
Internal KeyBoard Connector

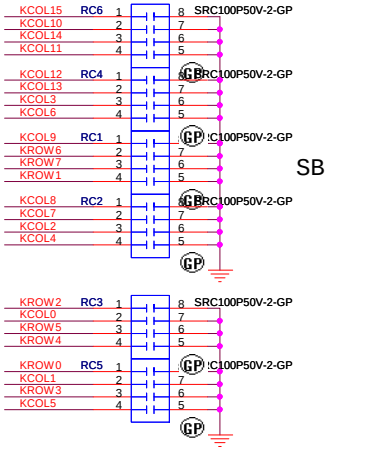


Lanuch Board CNN

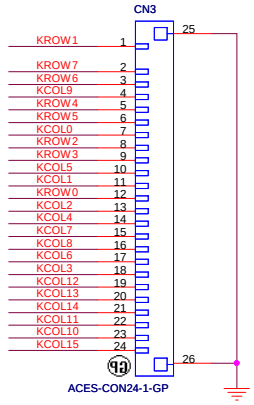






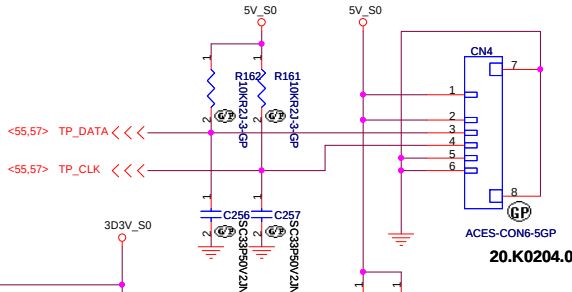


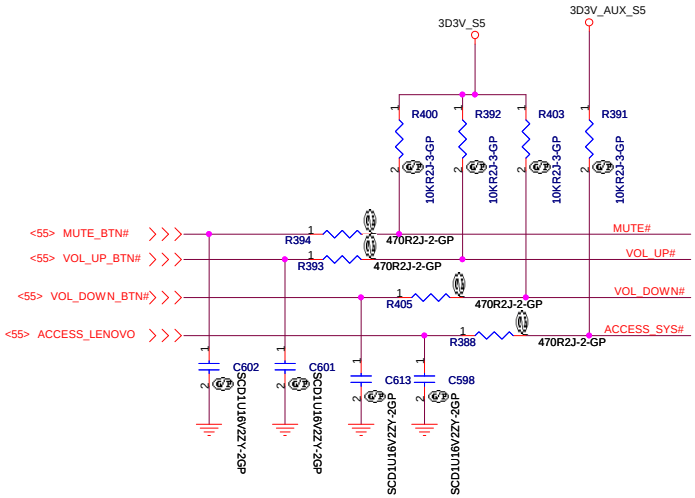
SB



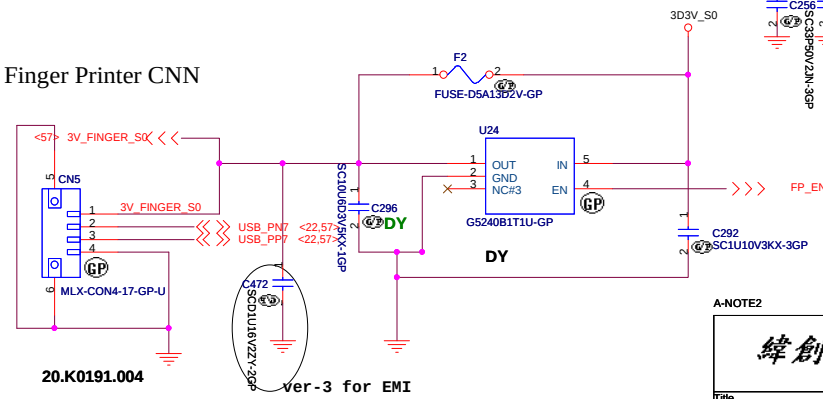
LAB2 20.K0204.020

TouchPad Connector



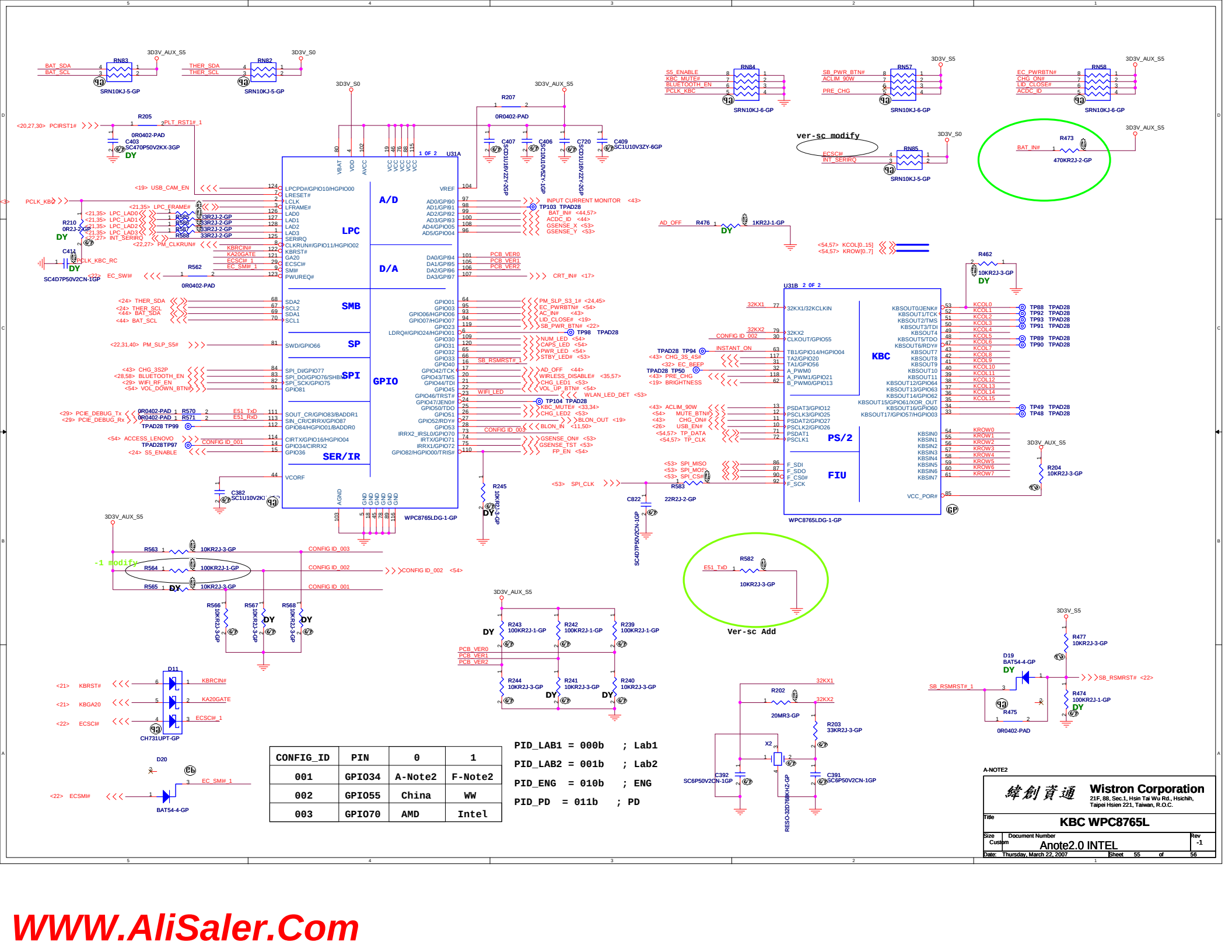


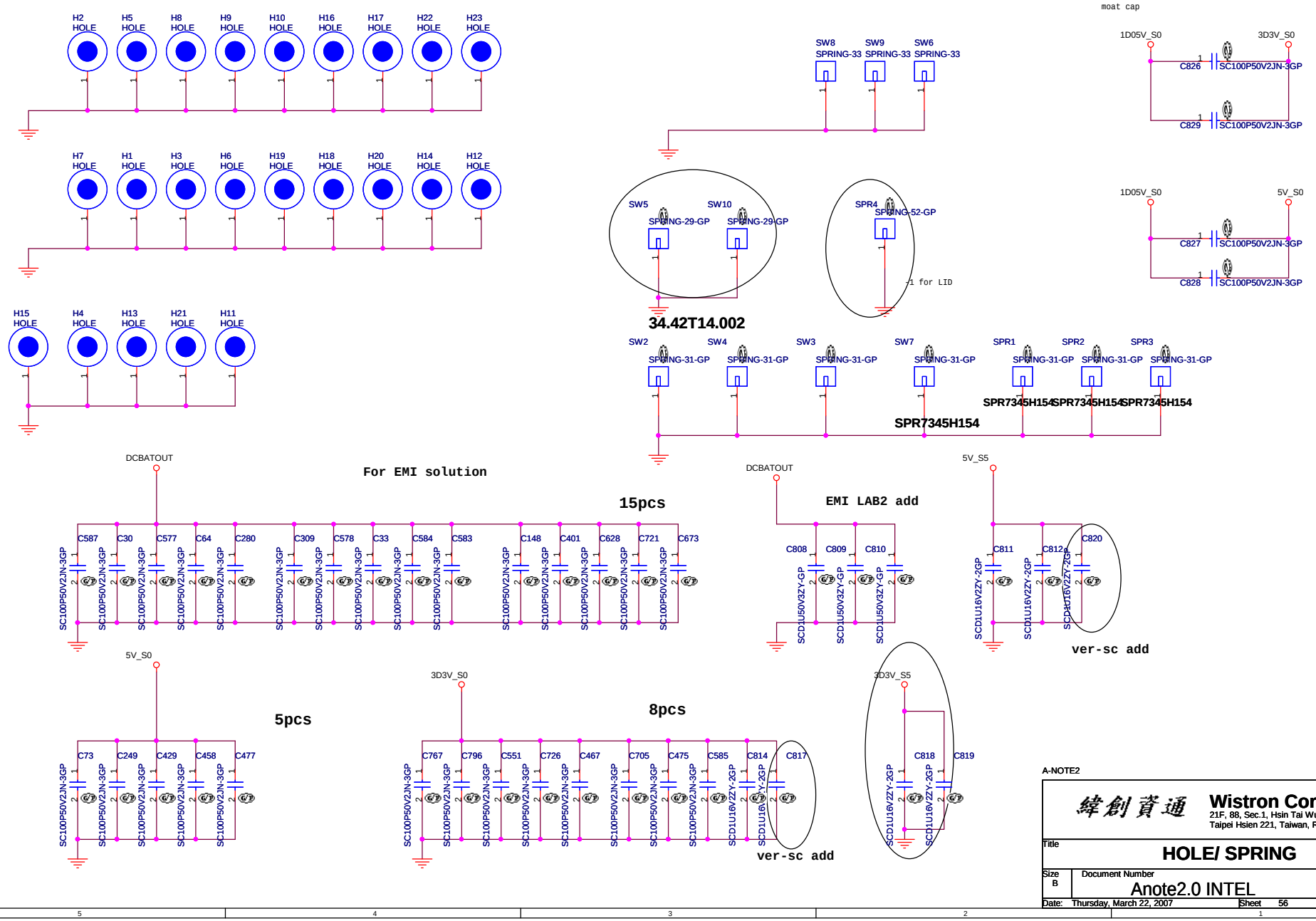
Finger Printer CNN

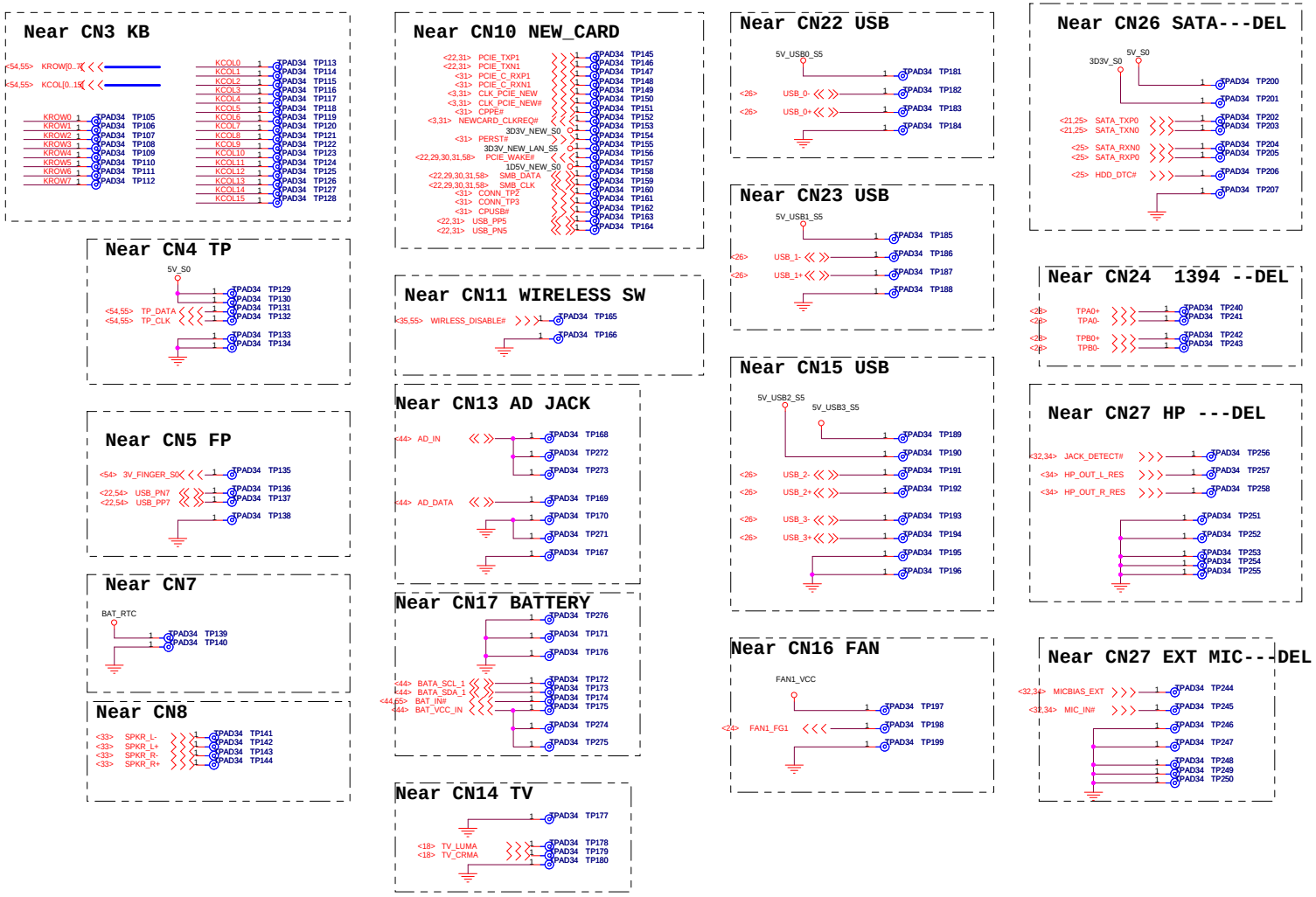


A-NOTE2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Keyboard /Touch Pad***	
Size A3	Document Number **Anote2.0 INTEL**	Rev -1
Date: Thursday, March 22, 2007	Sheet 54 of 56	

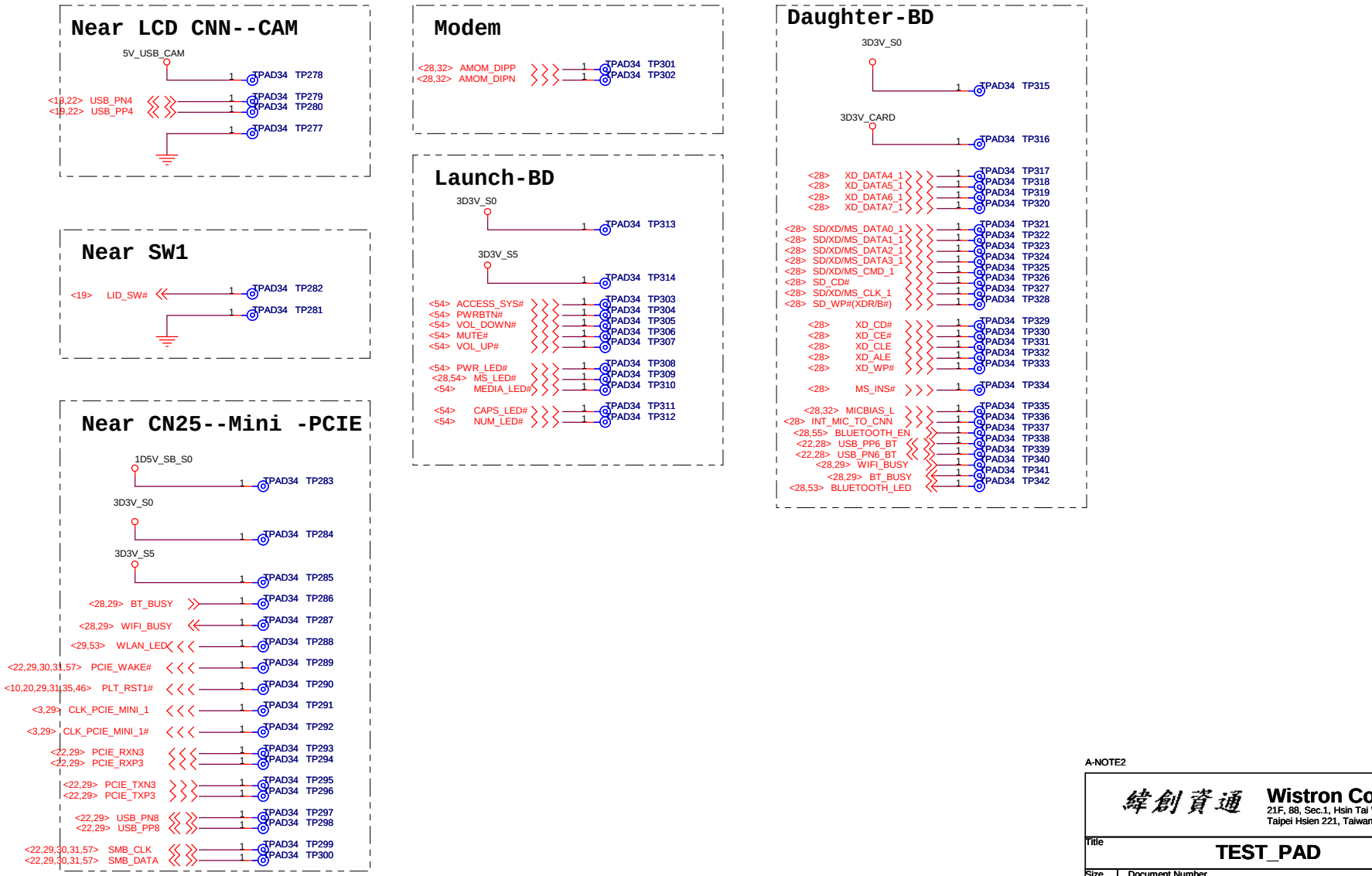

U31A
WPC8765LDG-1-GP
U31B 2 OF 2
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
PS/2
FIU
KBC
ver-sc modify
Ver-Sc Add
-1 modify
CONFIG_ID
PIN
0
1
001
GPIO34
A-Note2
F-Note2
002
GPIO55
China
WW
003
GPIO70
AMD
Intel
PID_LAB1 = 000b ; Lab1
PID_LAB2 = 001b ; Lab2
PID_ENG = 010b ; ENG
PID_PD = 011b ; PD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8765L
Anote2.0 INTEL
Thursday, March 22, 2007
Sheet 55 of 56
WWW.AliSaler.Com





A-NOTE2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TEST_PAD		
Size: C	Document Number: Anote2.0 INTEL	Rev: -1
Date: Thursday, March 22, 2007	Sheet 57 of 57	



A-NOTE2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TEST_PAD**

Size	Document Number	Rev
B	Anote2.0 INTEL	-1

Date: Thursday, March 22, 2007 Sheet 58 of 58