

Compal Confidential

JFWXX Schematics Document

Intel Merom Processor with SiSM672MX + DDRII + SiS968 + SiS307LV

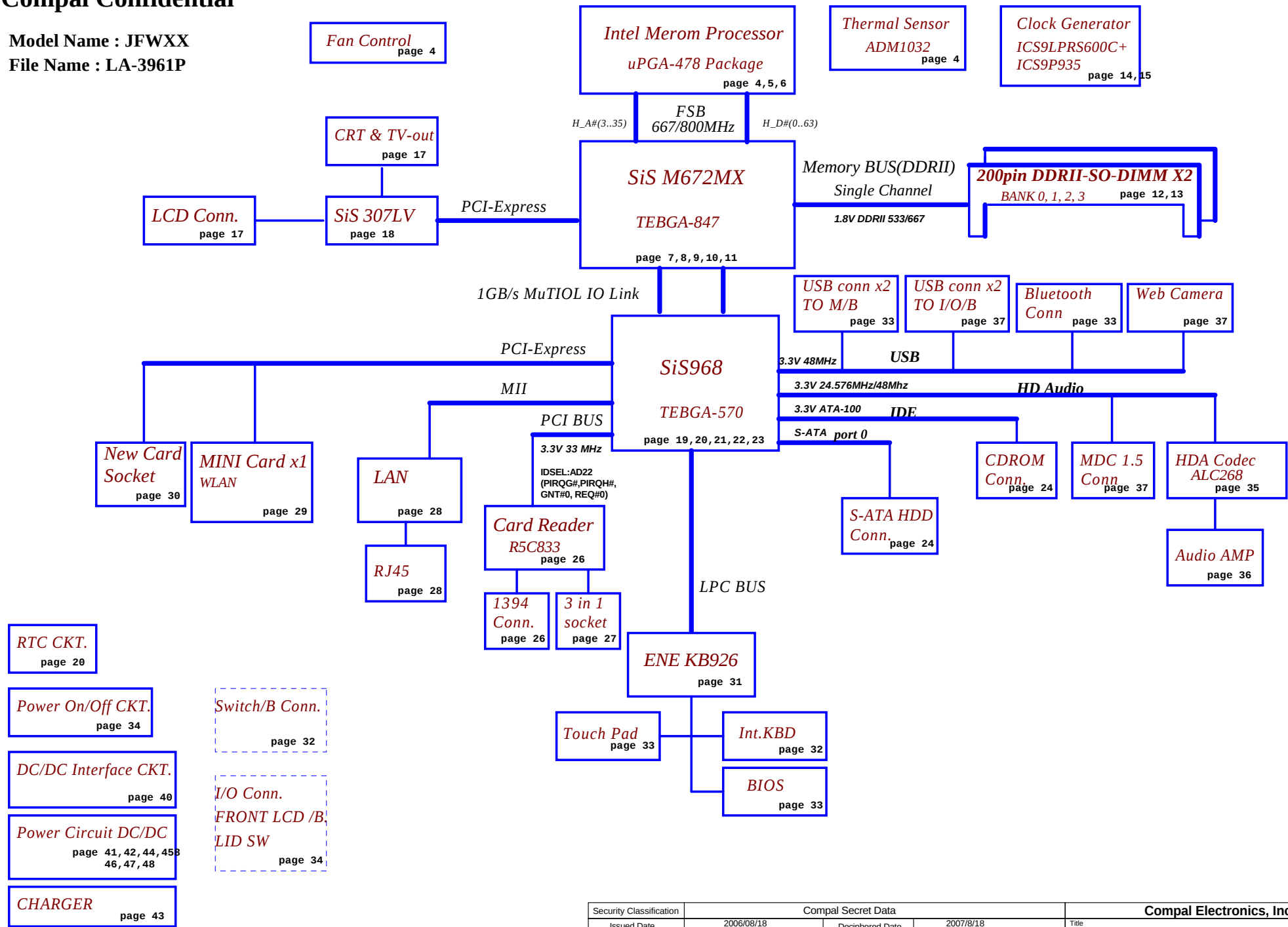
2007 - 09 - 06

REV: 0.3

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Model Name : JFWXX
File Name : LA-3961P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID
14W	R424 (Pull low)
15W	NA (Internal Pull High)

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

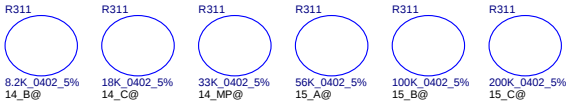
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Ra~ R312

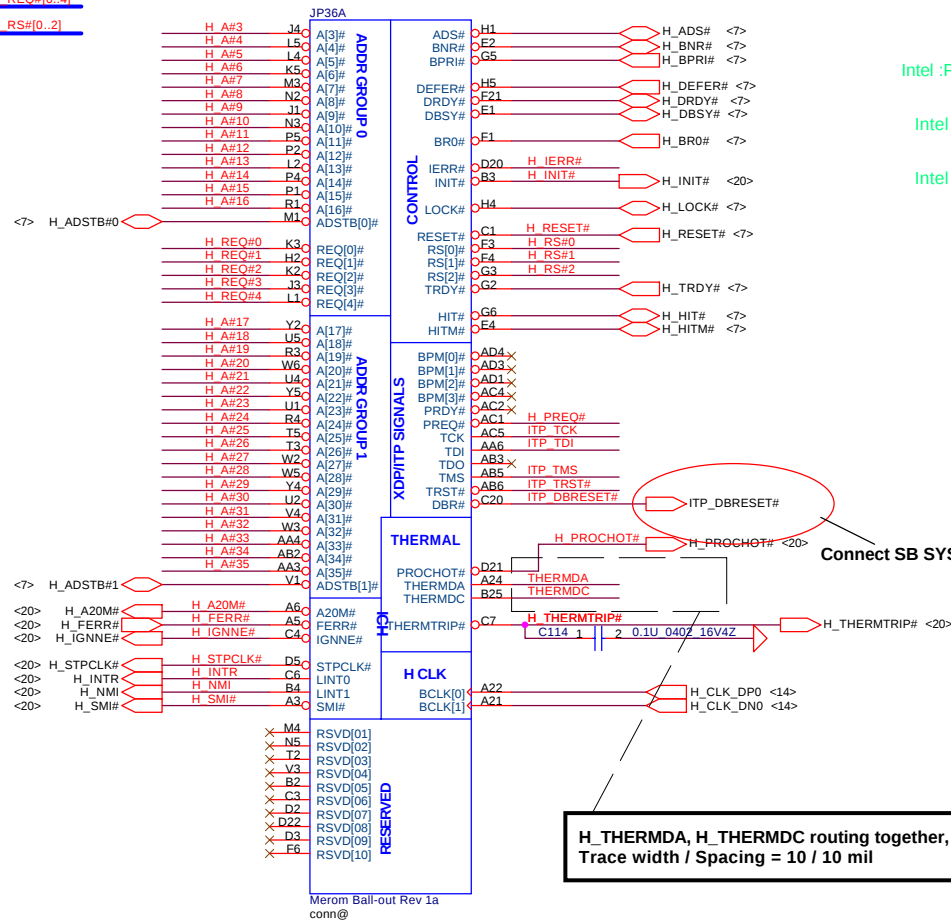
Rb~ R311



Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	Rb BOM Structure
0	0	0 V	0 V	0 V	14_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	14_B@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	14_C@ ✓
3	33K +/- 5%	0.721 V	0.819 V	0.926 V	14_MP@
4	56K +/- 5%	1.054 V	1.185 V	1.325 V	15_A@
5	100K +/- 5%	1.489 V	1.650 V	1.819 V	15_B@
6	200K +/- 5%	2.019 V	2.200 V	2.386 V	15_C@ ✓
7	NC	3.135V	3.300 V	3.465 V	15_MP@

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<7> H_A# [3..35] H_A# [3..35]
<7> H_REQ# [0..4] H_REQ# [0..4]
<7> H_RS# [0..2] H_RS# [0..2]



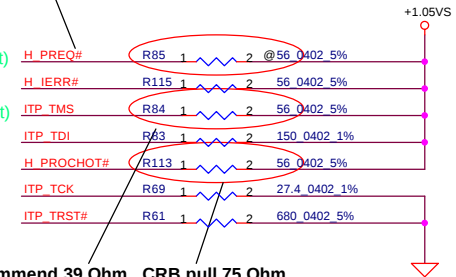
Trace length must short

Place close to CPU within 500mil

Intel :Pull-up 56ohm (Un-Mount) SIS : Pull-up 56ohm (Mount)

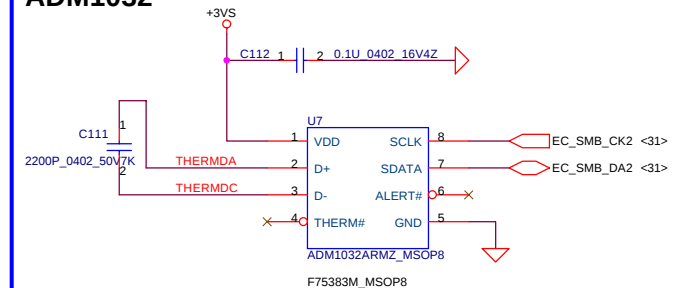
Intel :Pull-up 56ohm (Mount) SIS : Pull-up 54.9ohm (Mount)

Intel :Pull-up 56ohm (Mount) SIS : Pull-up 75ohm (Mount)

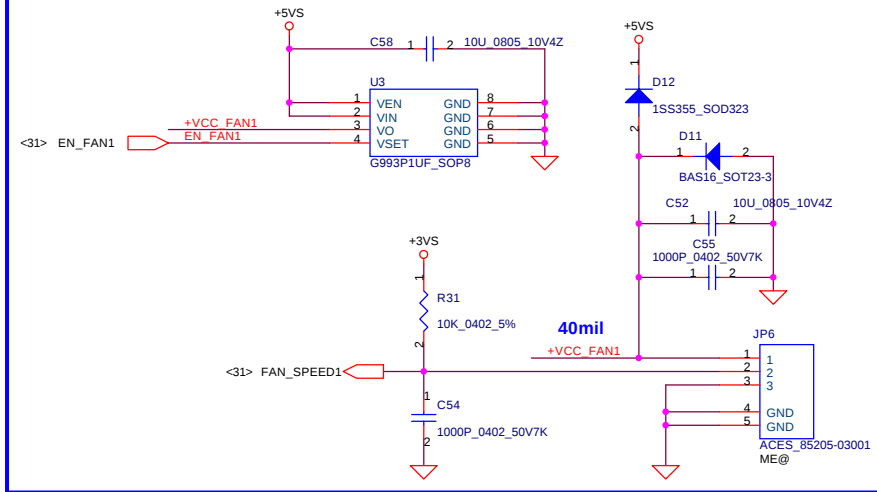


Checklist recommend 39 Ohm CRB pull 75 Ohm

ADM1032



FAN1 Conn

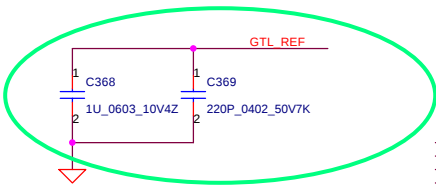


H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

CPU to SB interface

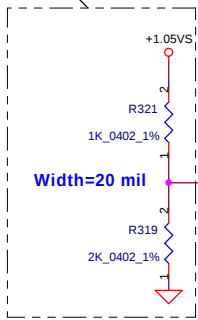


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SIS Recommend

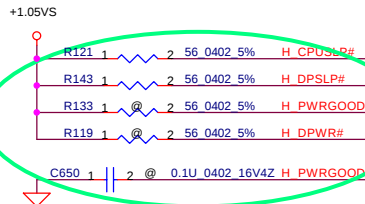
Close to CPU pin AD26 within 500mils.



Width=20 mil

Layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0



Intel :Don't Pull-up SiS : Pull-up 56ohm (Mount)

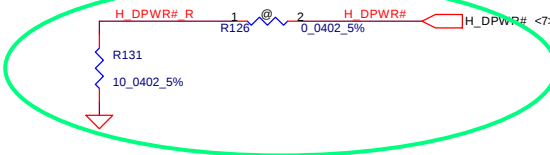
Intel :Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

Intel :Don't Pull-up (Connecte to ICH) SiS : Pull-up 56ohm (Un-Mount)

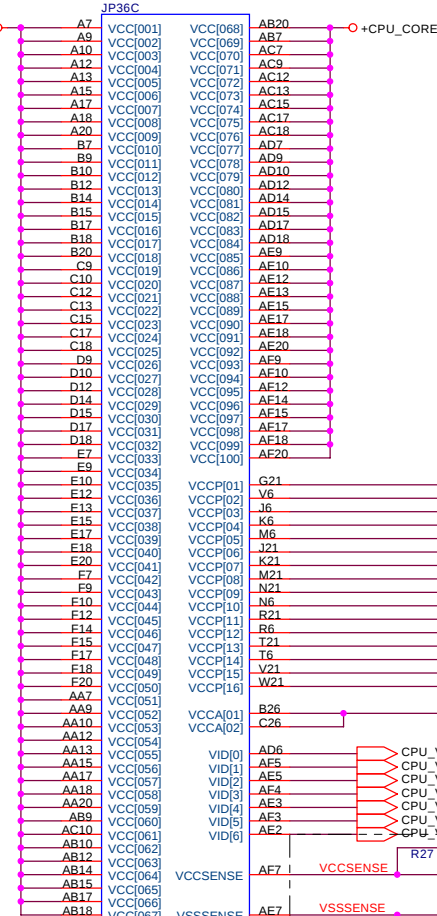
Intel :Don't Pull-up SiS : Pull-up 56ohm (Un-Mount)

Intel :Don't Pull-down SiS :Pull-down Cap (Un-Mount)

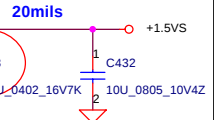
SIS Recommend



Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Place this cap more close to B26/C26 rather than 10UF

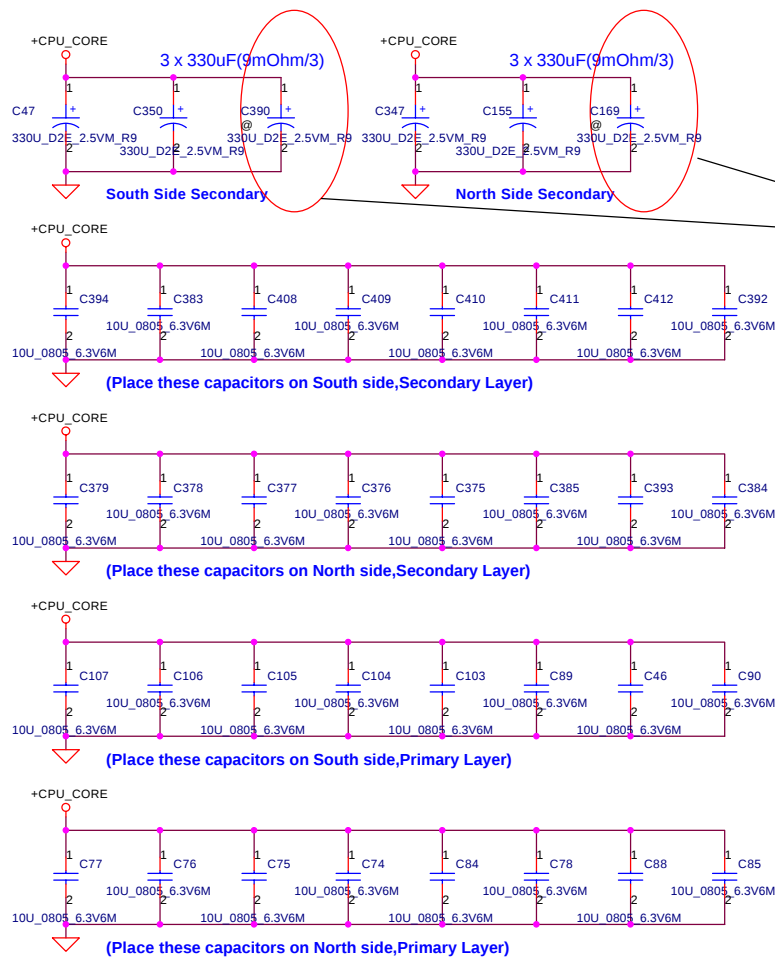
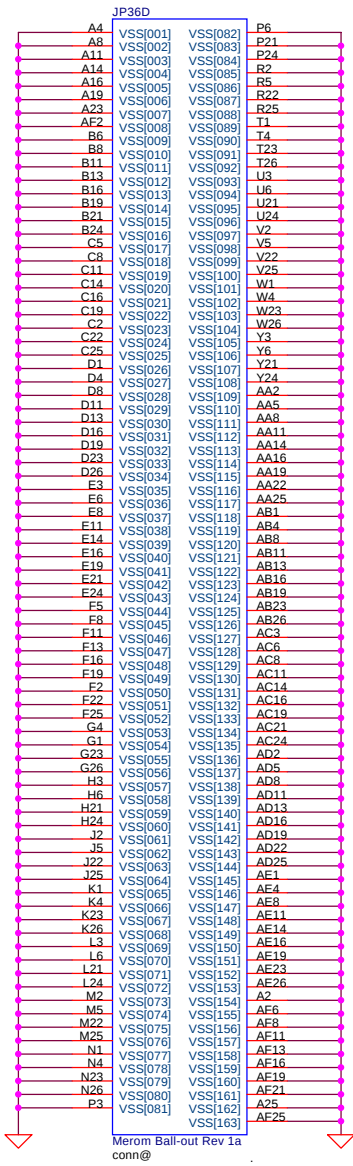


20mils

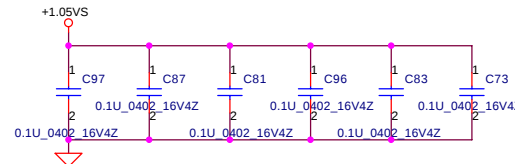
Length match within 25 mils. The trace width/space/other is 20/7/25.

Close to CPU pin within 500mils.

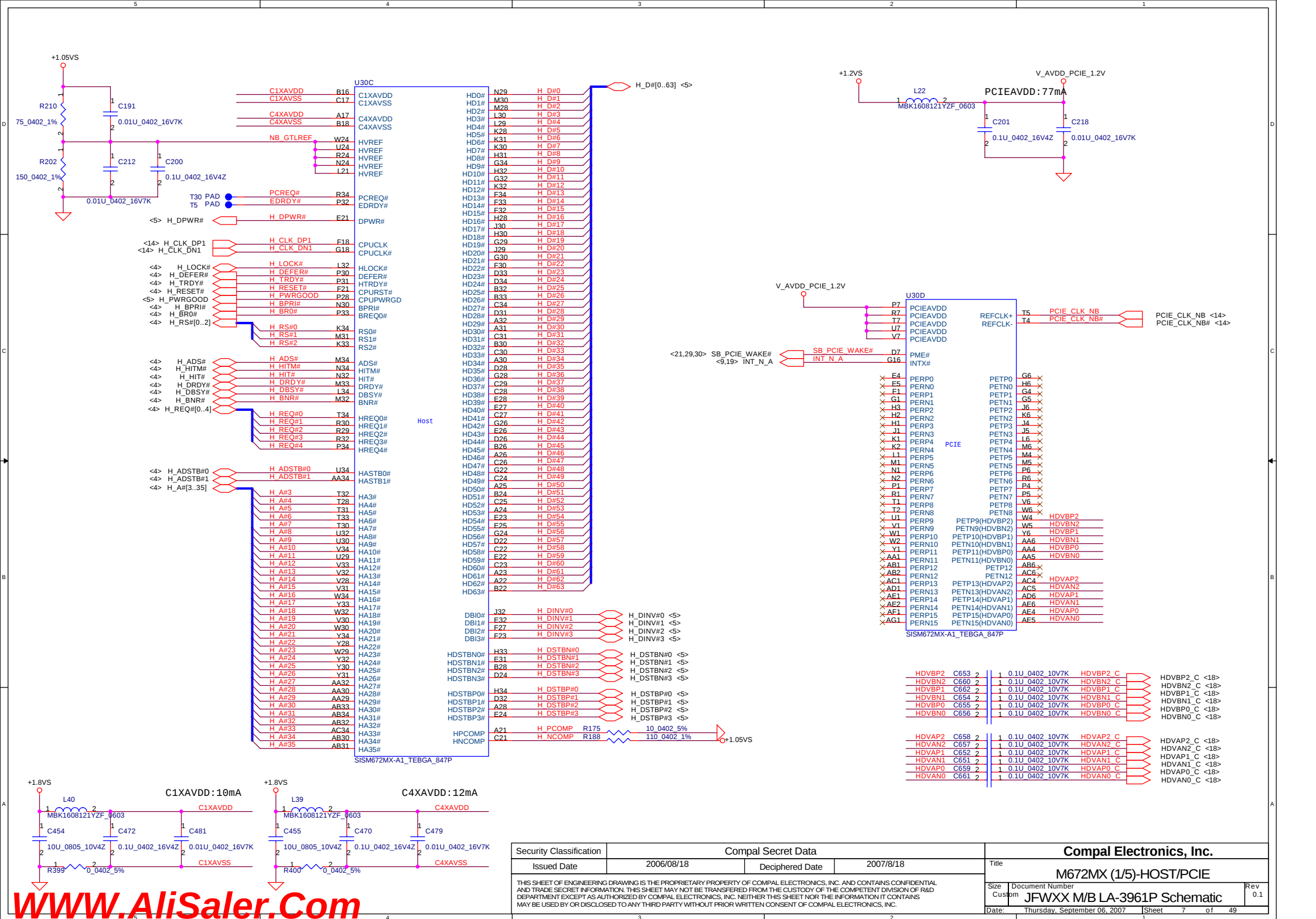
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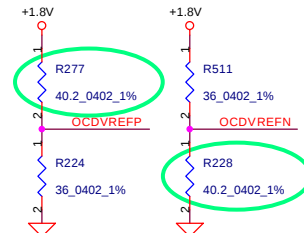
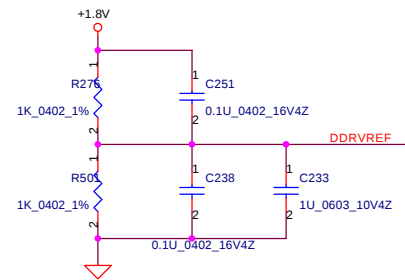
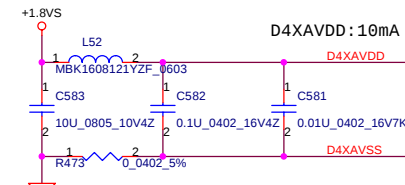
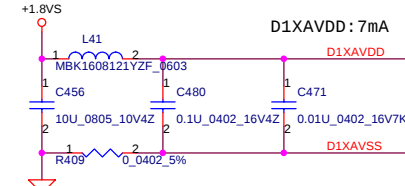
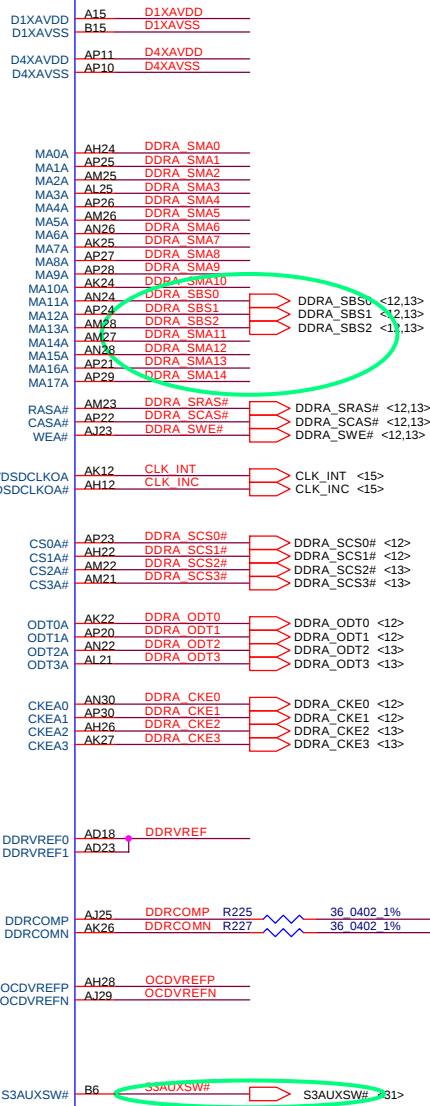


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



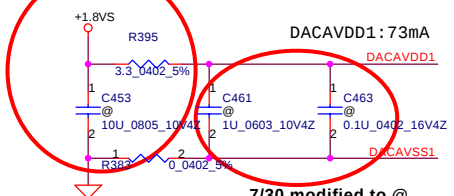
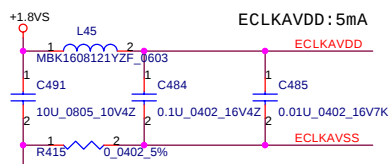
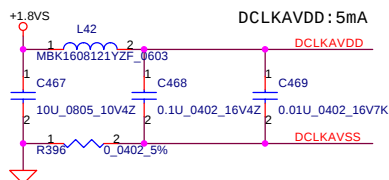
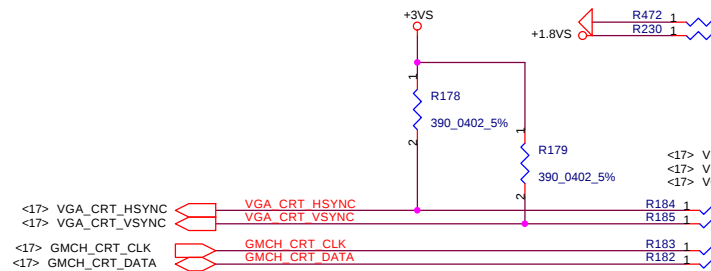
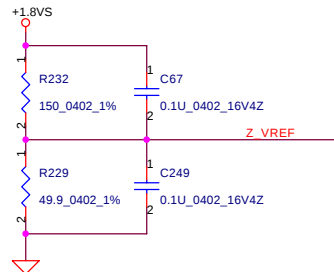
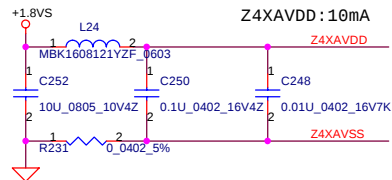
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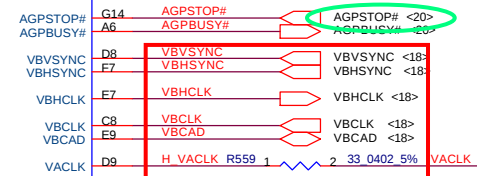
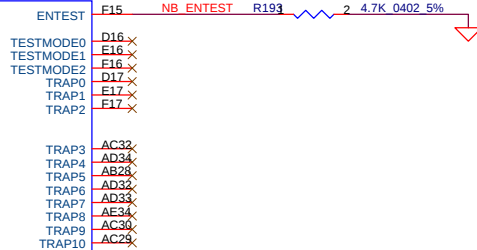
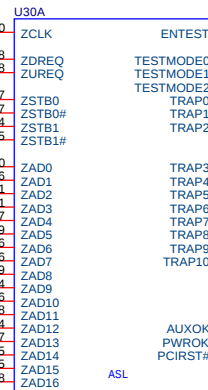
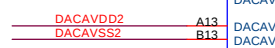
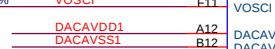
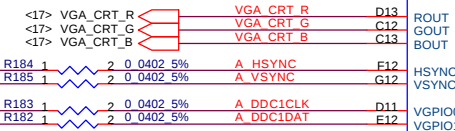
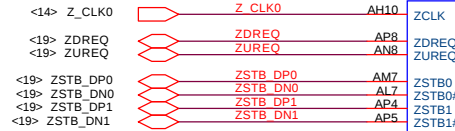
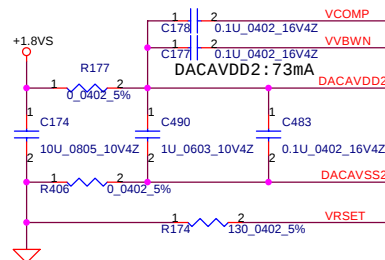
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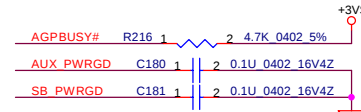


DACAVDD1 Spec.
Voltage : 1.5V +/- 5%
Current : 100mA

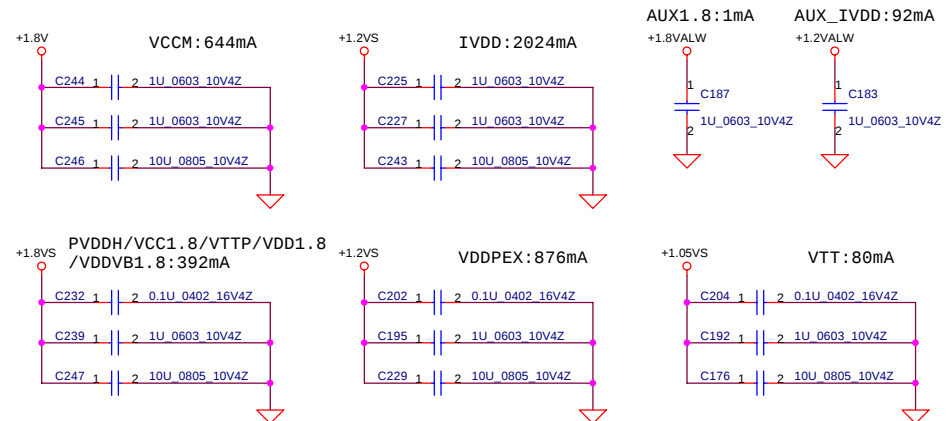
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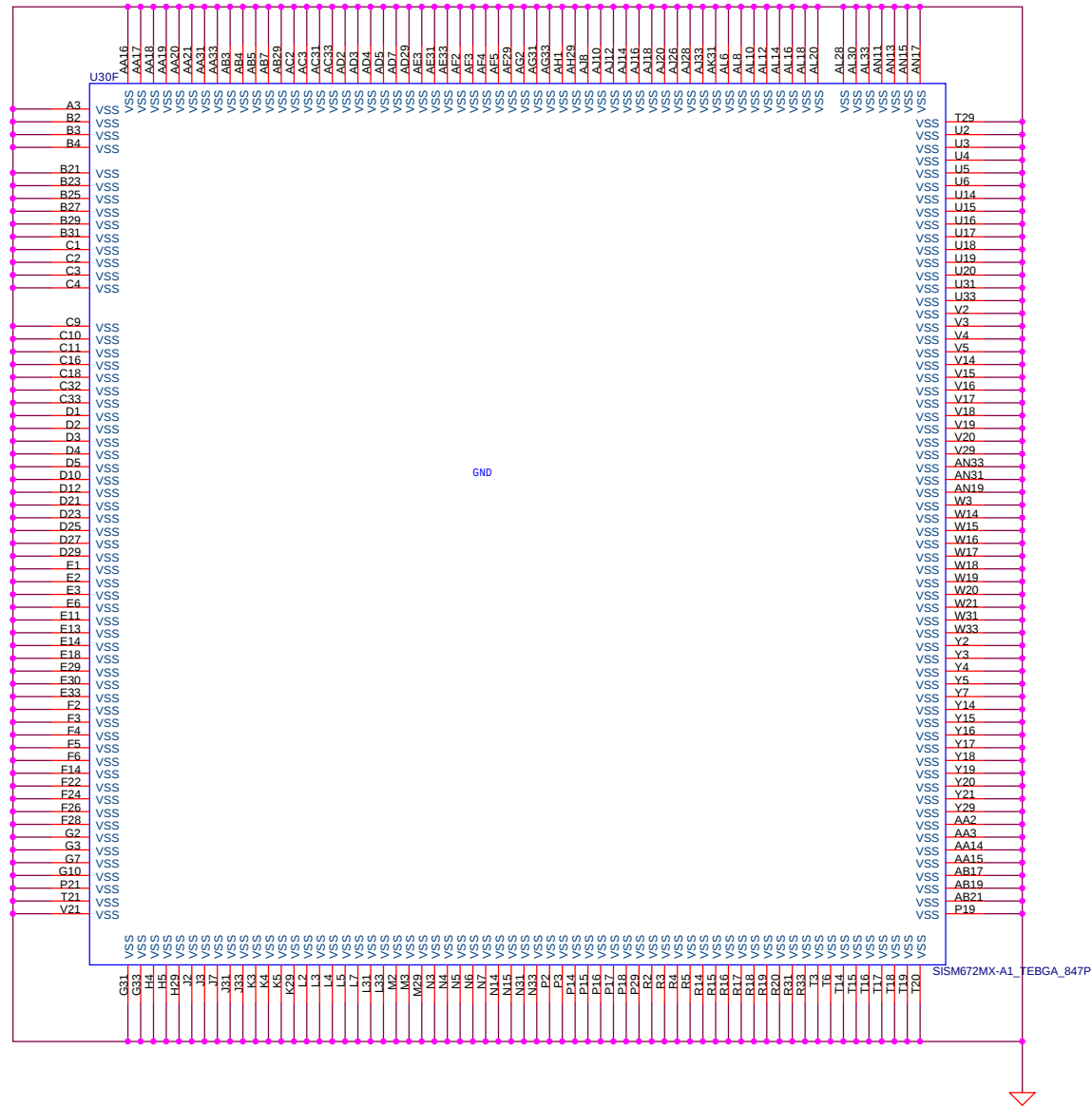
For S1S VB 307 use only



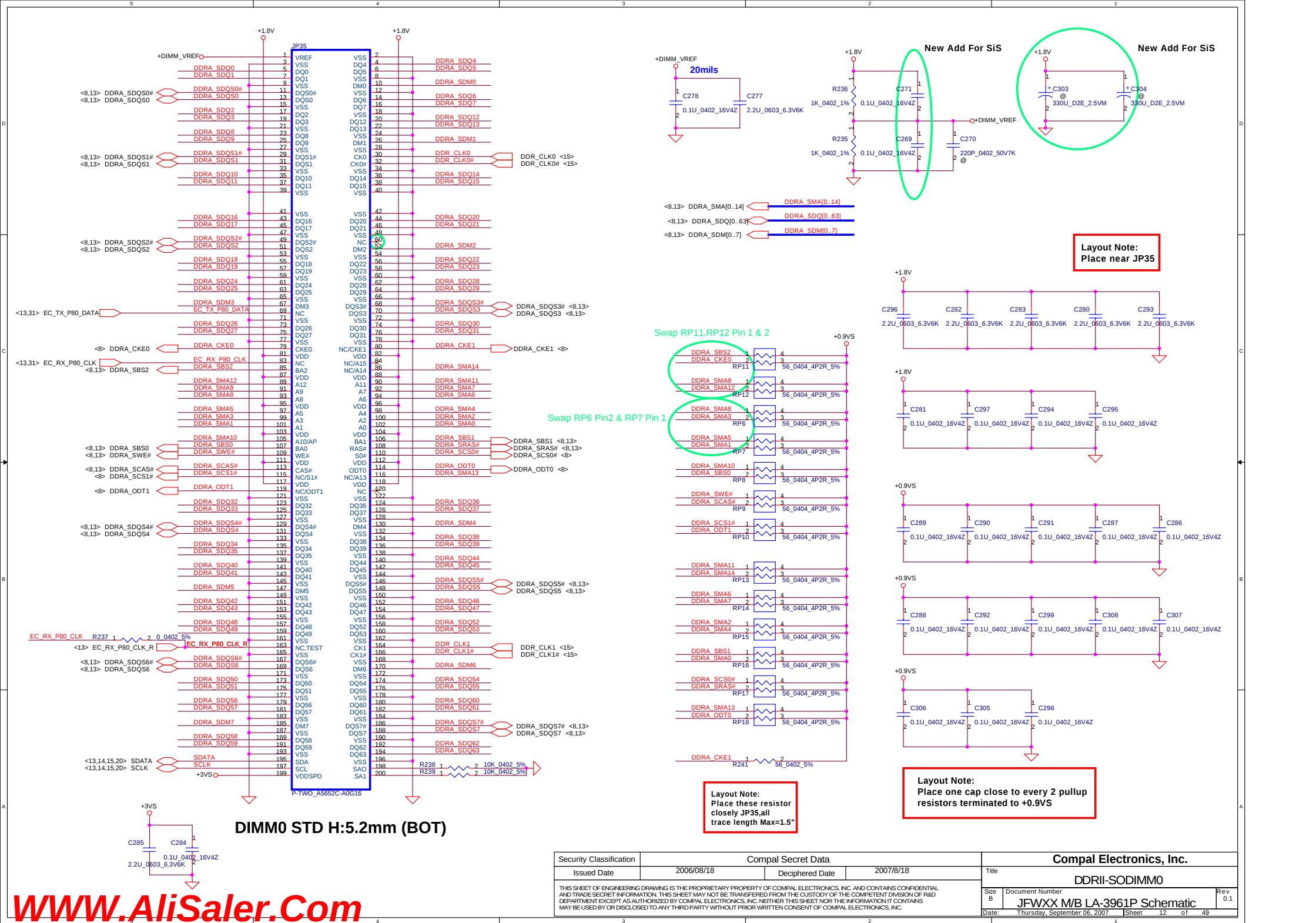
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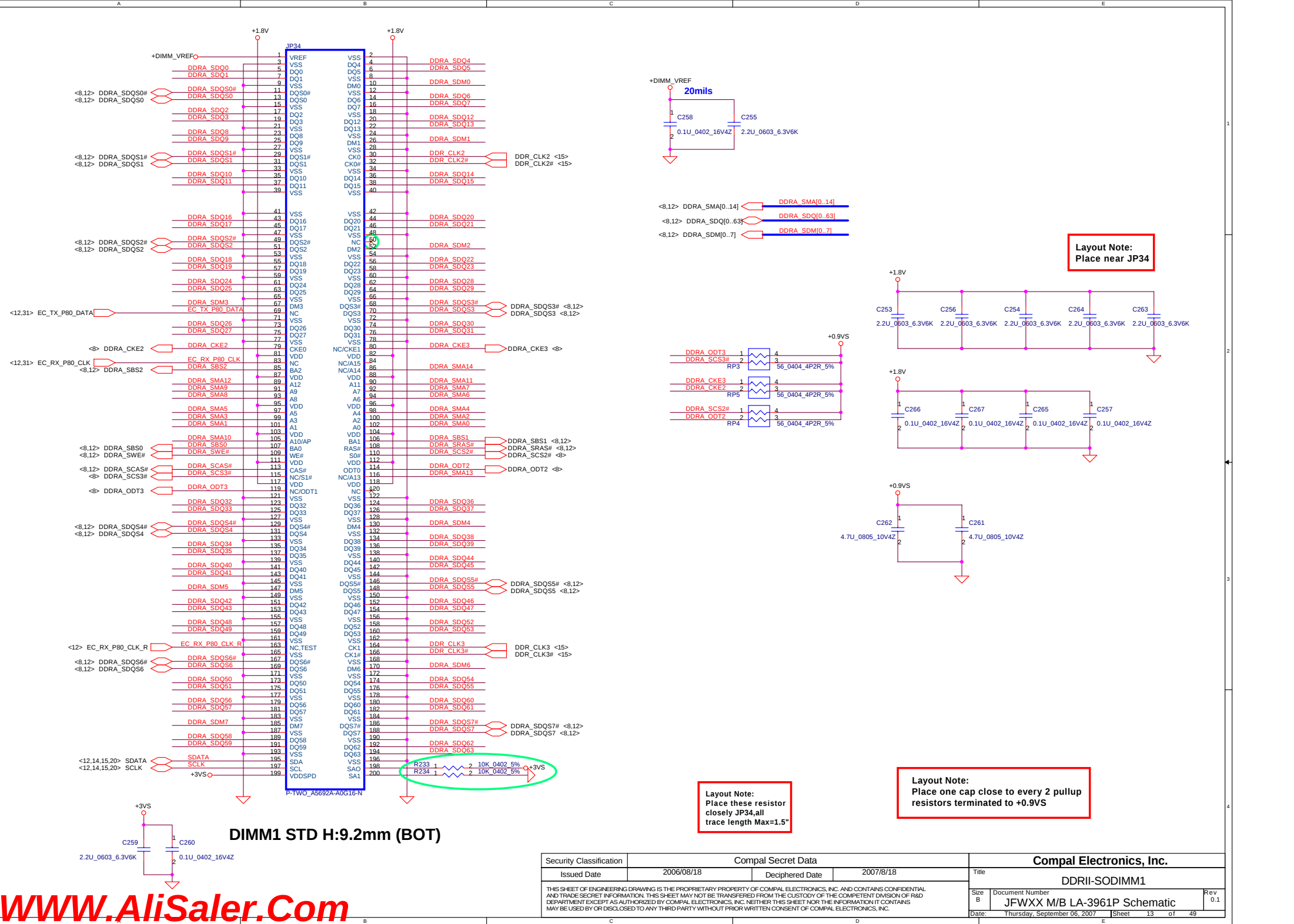


The image displays six circuit diagrams arranged in a 2x3 grid, illustrating different capacitor configurations for a 1.8V supply. Each diagram shows a 1.8V input connected to a series of capacitors (C230, C231, C235, C223, C237, C236) in parallel, which are then connected to ground. The capacitors are labeled with their values: 0.1uF, 1uF, and 4.7uF. The diagrams are arranged in a 2x3 grid. The top row shows configurations for +1.8V, +1.2VS, +1.8VALW, and +1.2VALW. The bottom row shows configurations for +1.8VS, +1.2VS, and +1.05VS.

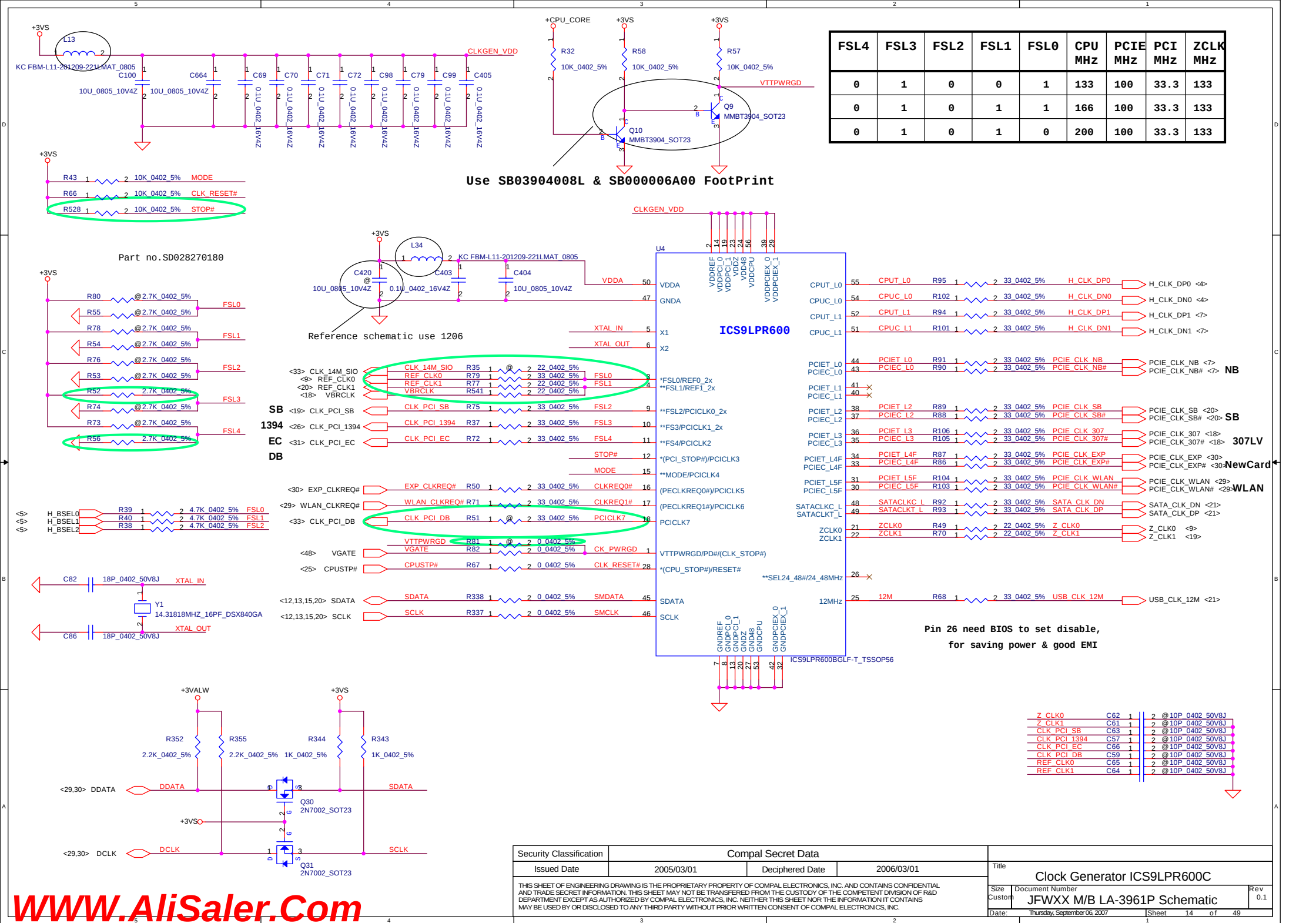


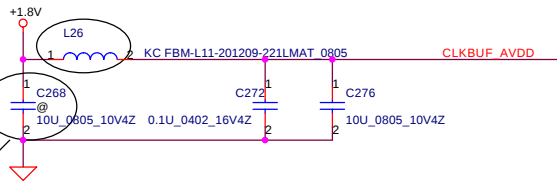
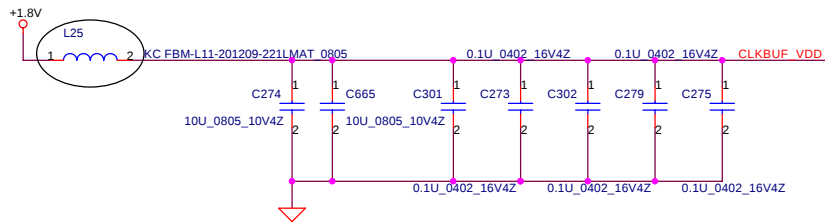
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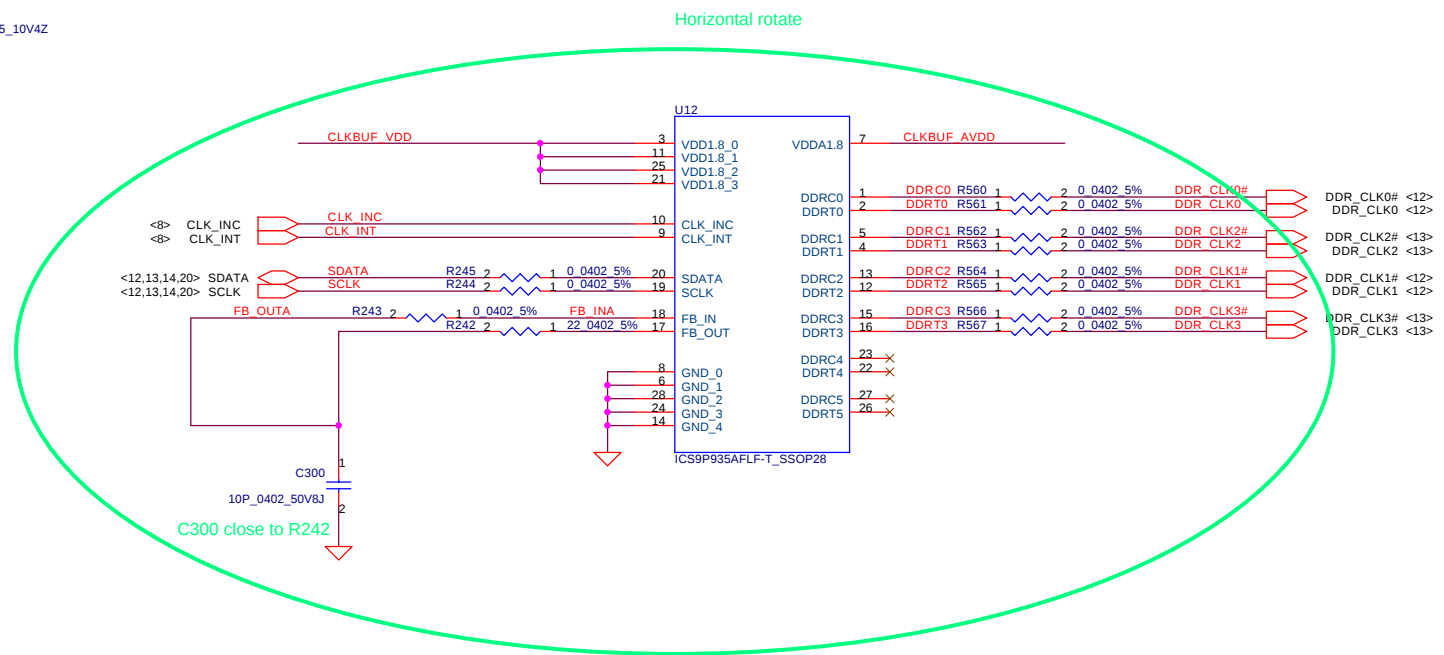


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								JFWXX M/B LA-3961P Schematic			
								Rev 0.1			
				Date: Thursday, September 06, 2007				Sheet 13 of 49			



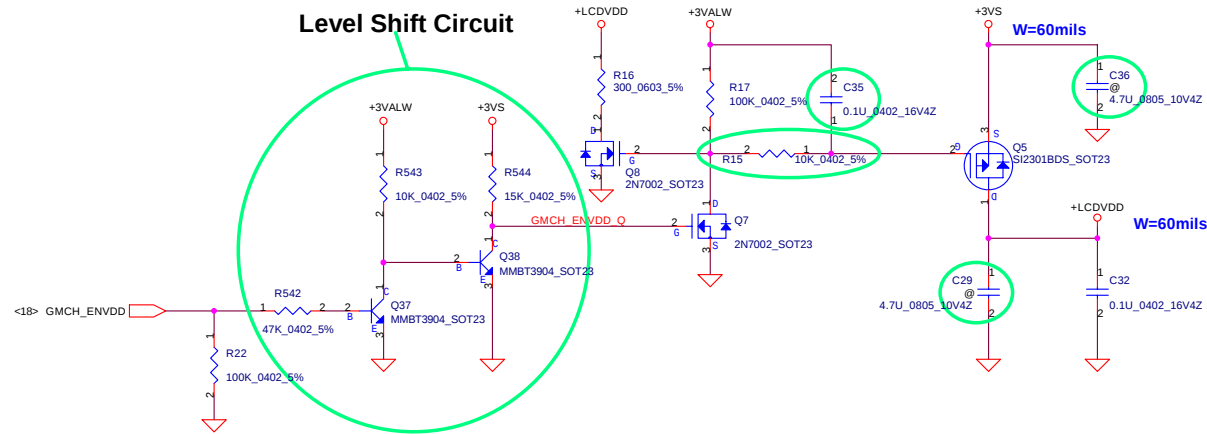


Reference schematic use 1206

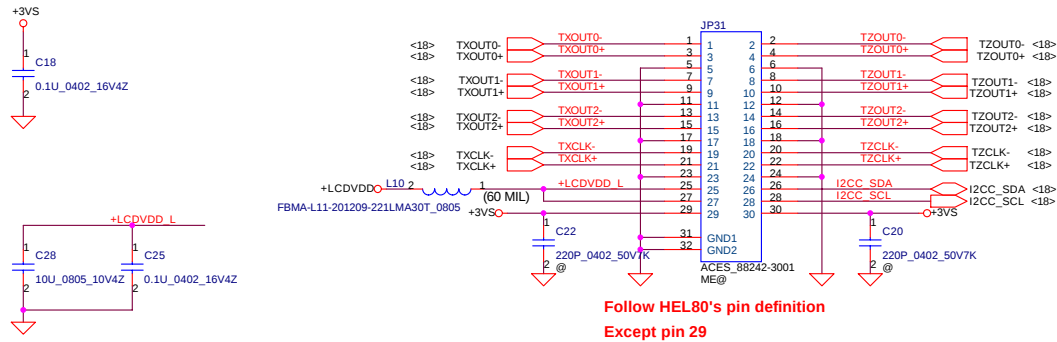


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				Date: Thursday, September 06, 2007	Sheet 15 of 49

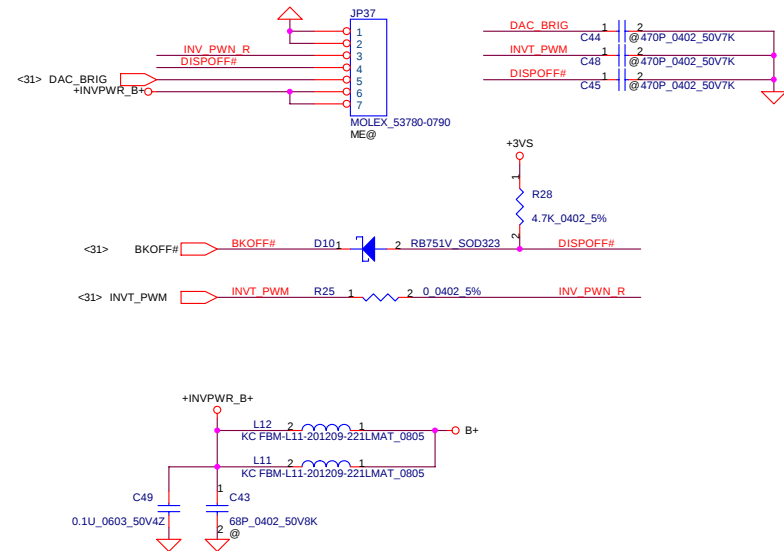
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

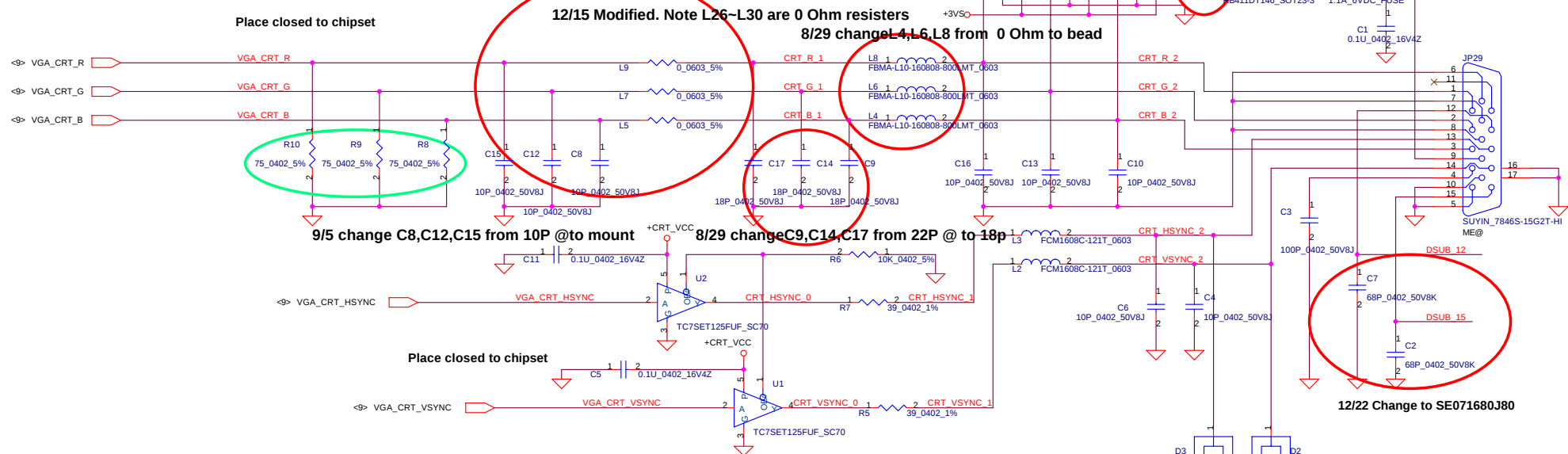
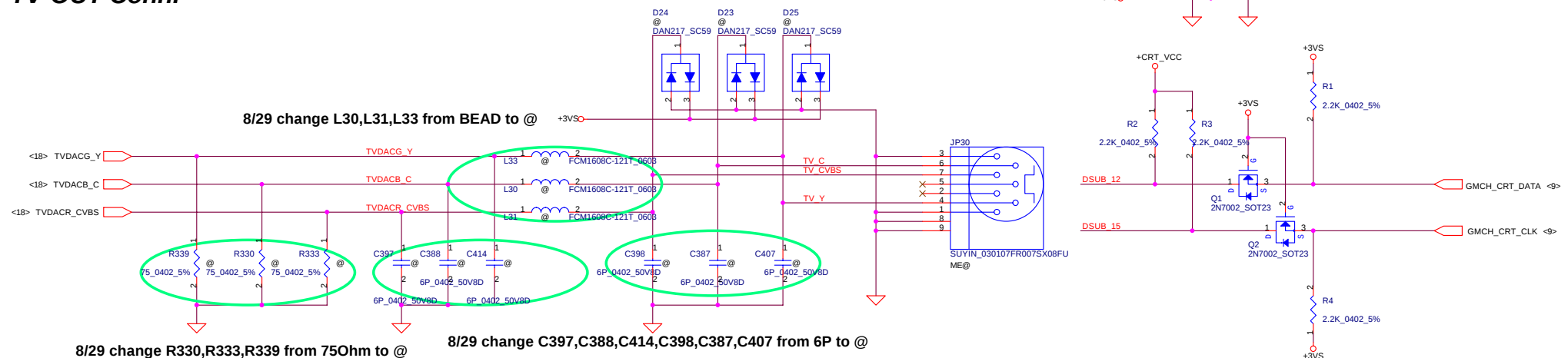


INVERTER Conn.

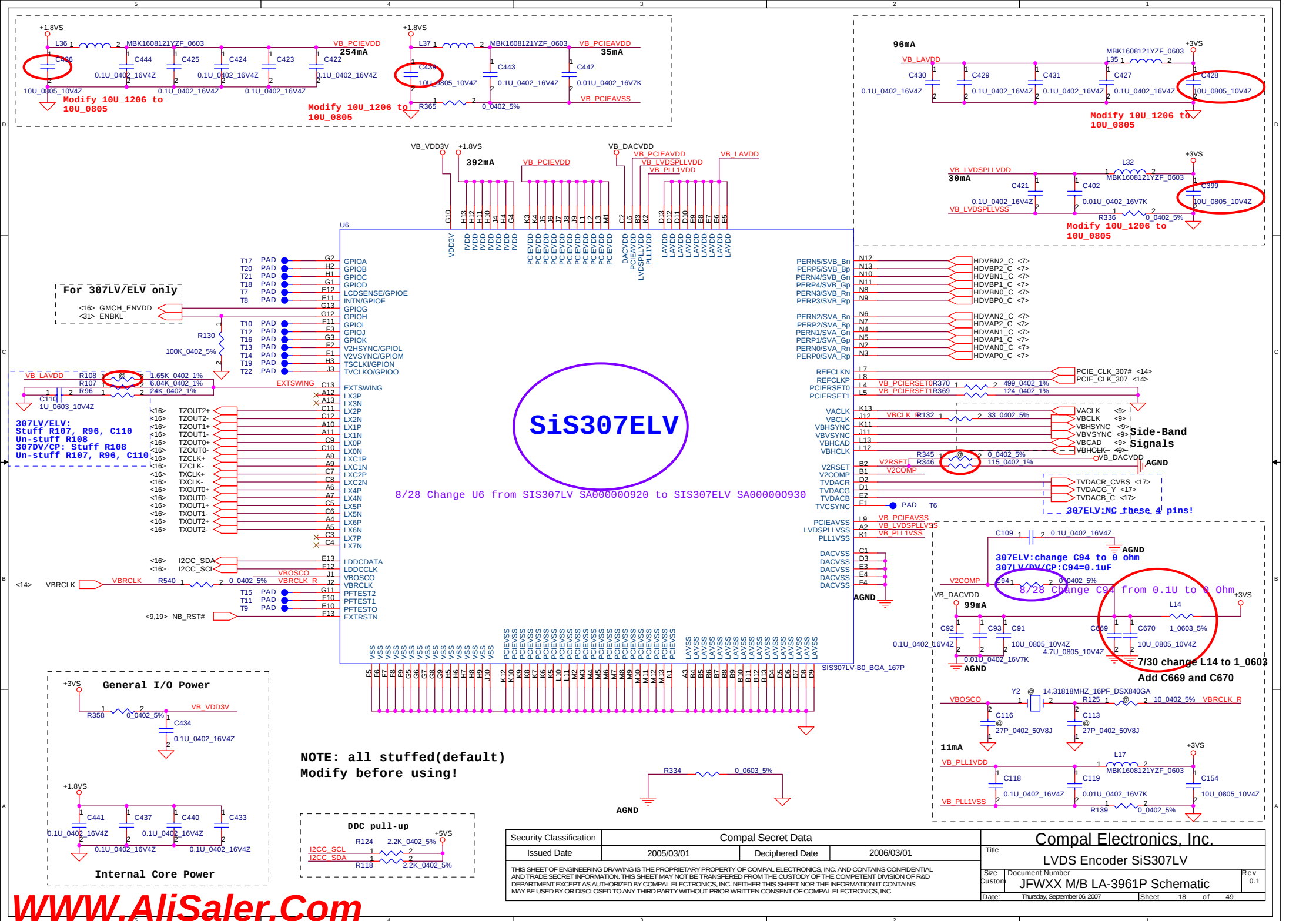


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Size B	Document Number	JFWXX M/B LA-3961P Schematic			Rev	0.1
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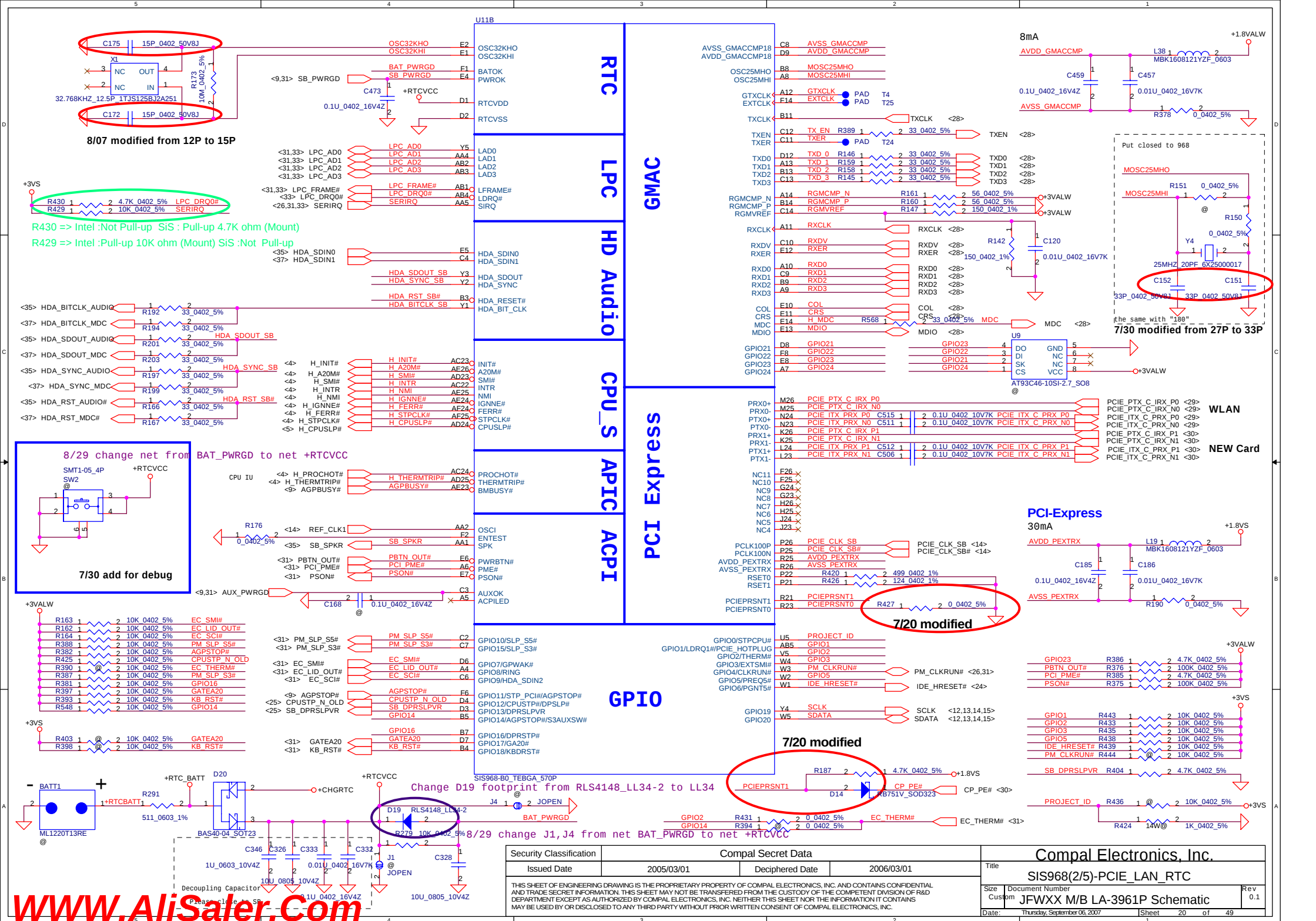
CRT Connector

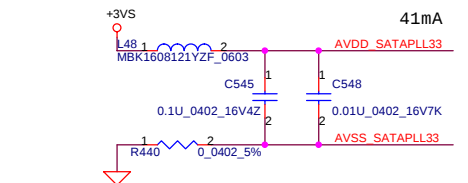
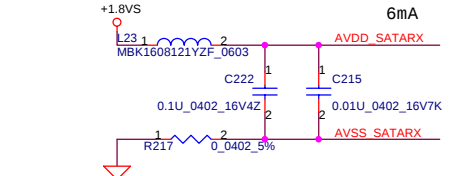
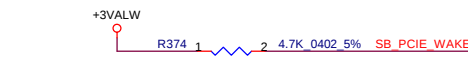
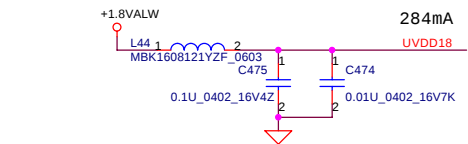
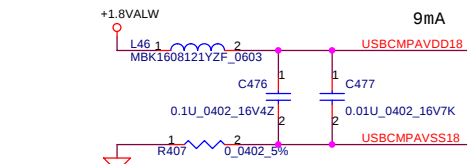
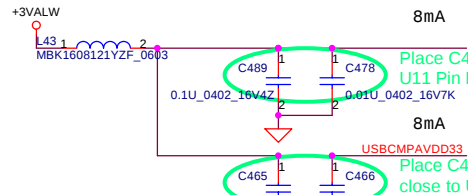
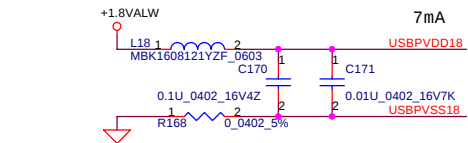
**TV-OUT Conn.**

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				JFWXXX M/B LA-3961P Schematic		
				Date:	Thursday, September 06, 2007	Sheet 17 of 49

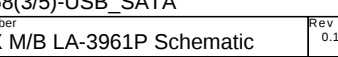
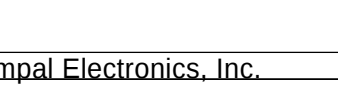
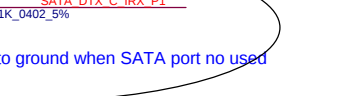
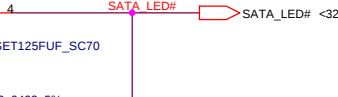
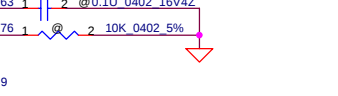
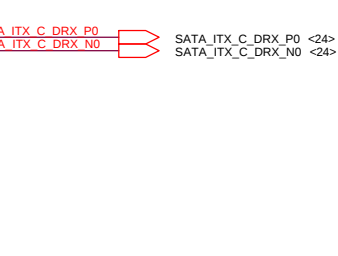
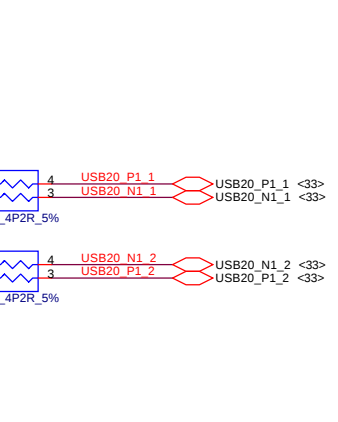
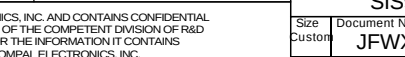
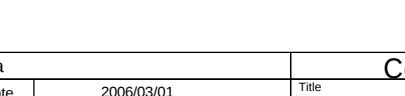
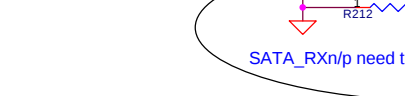
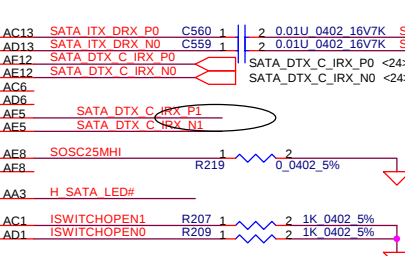
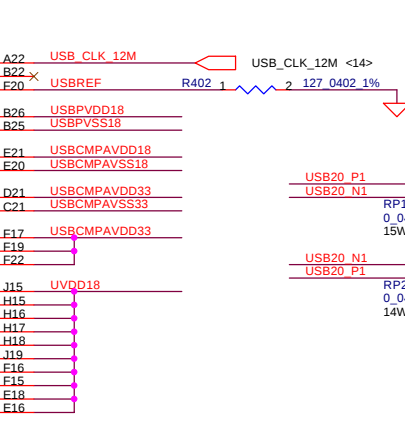
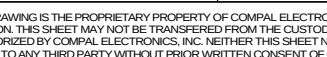
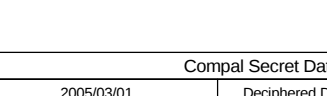
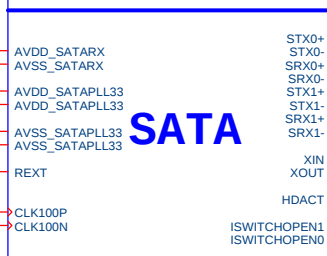
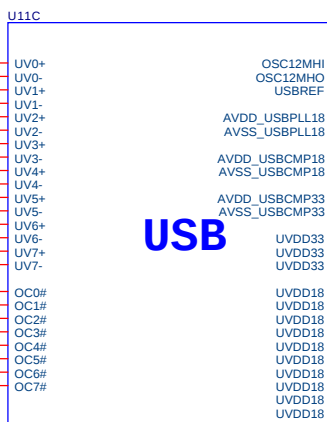
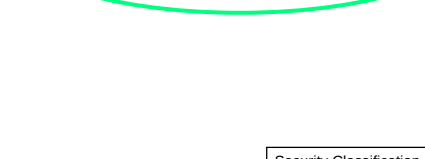
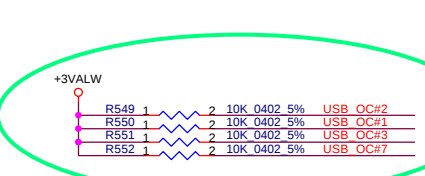
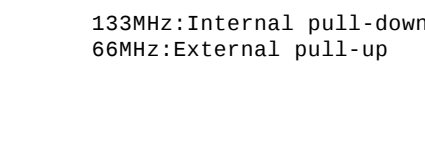
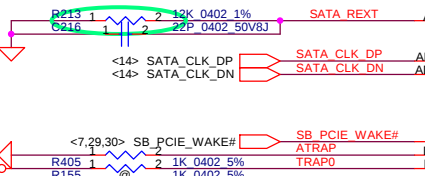
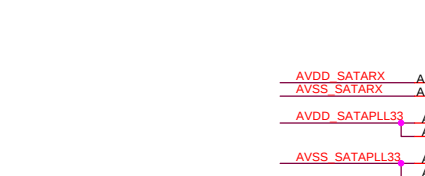
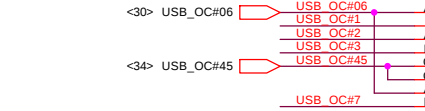




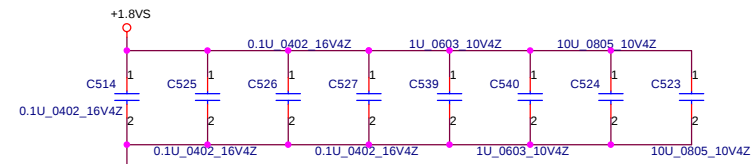
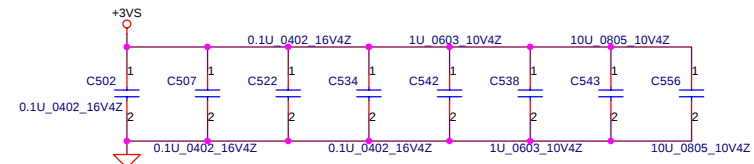
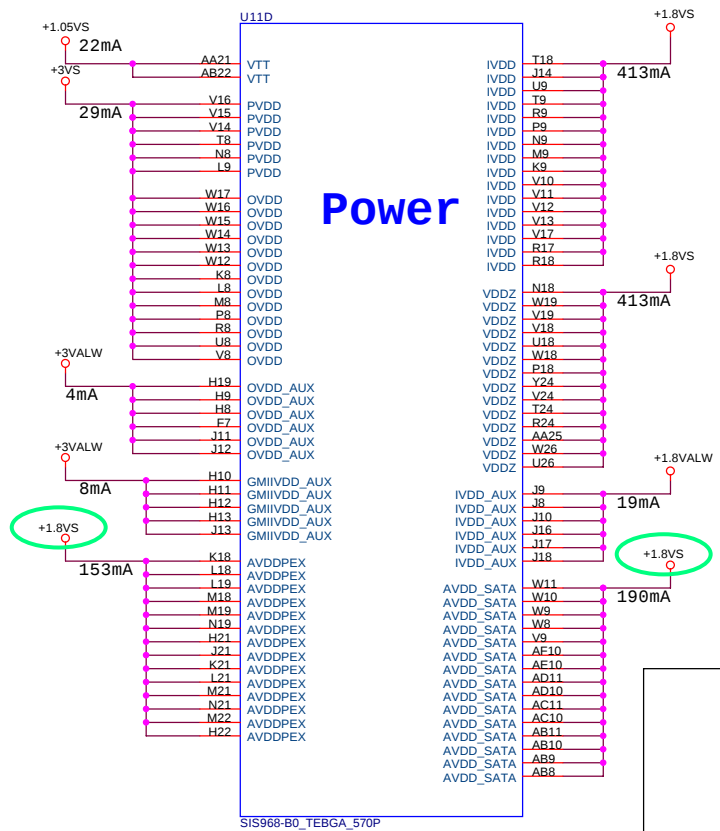




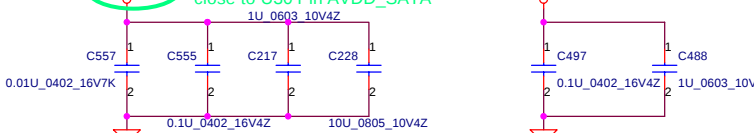
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New Card
WLAN
USB
USB
CAMERA



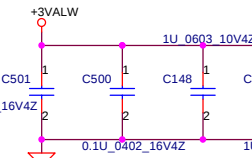
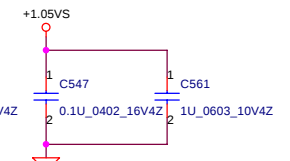
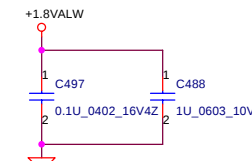
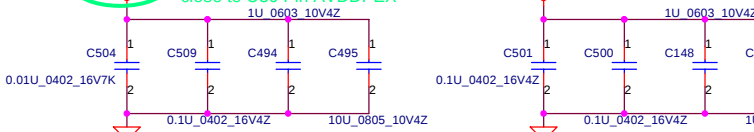
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				Custom	JFWXX M/B LA-3961P Schematic	0.1			
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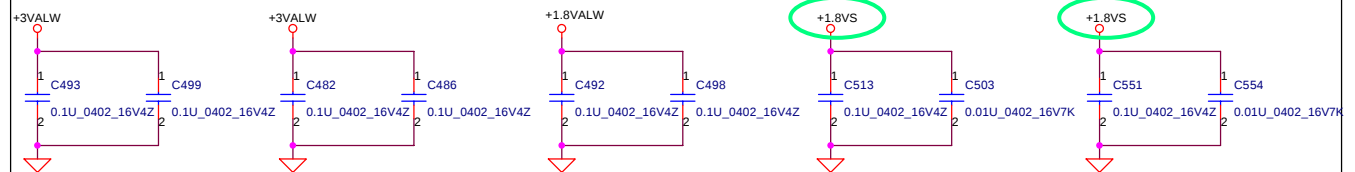
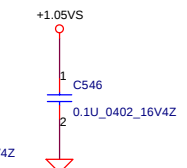
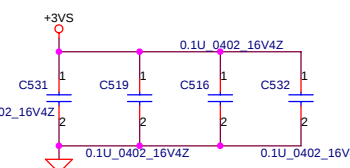
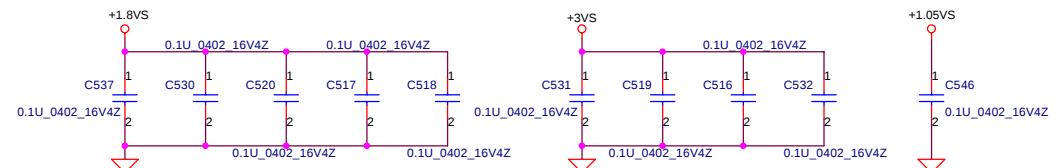
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C557,C555,C217,C228,C551,C554
close to U30 Pin AVDD_SATA



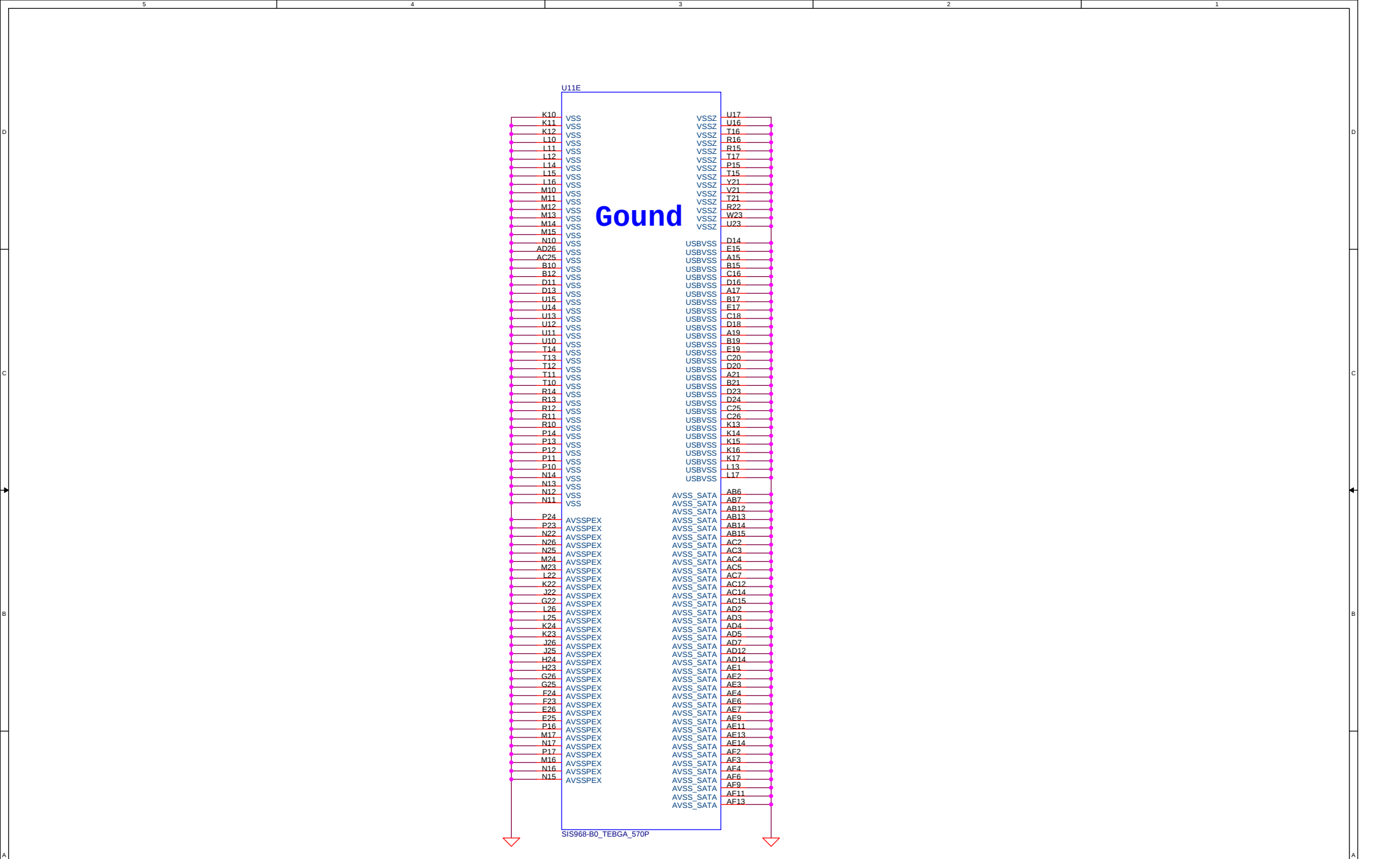
+1.8VS
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close to U30 Pin AVDDPEX



Put under 968 solder side

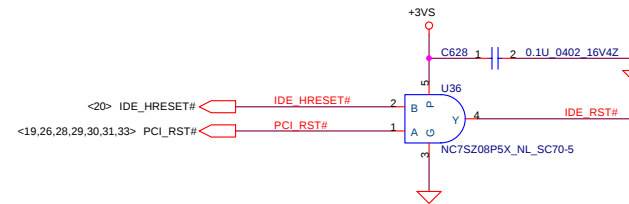
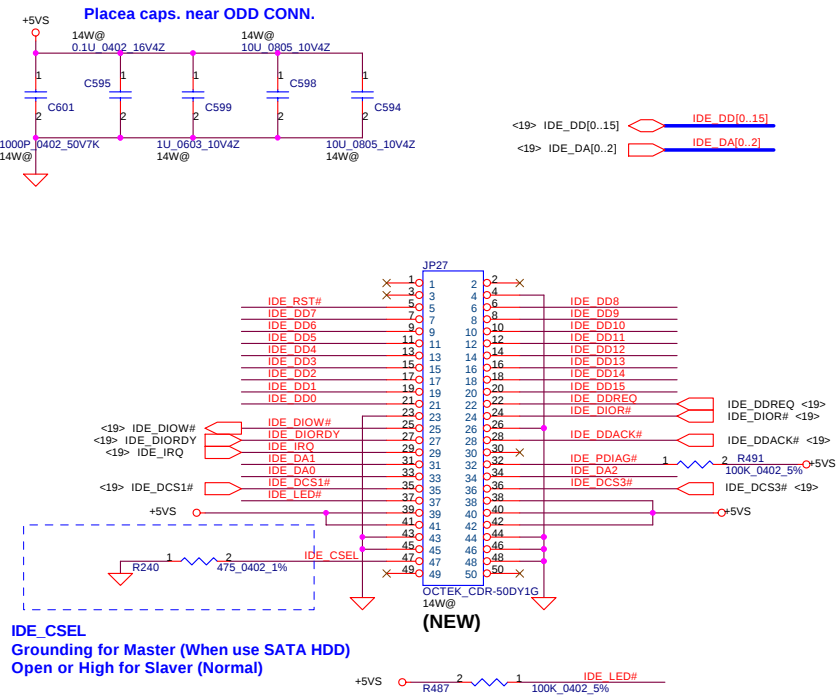


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Size		Document Number		Rev	
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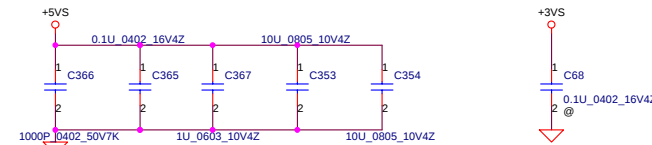


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								Size		Document Number		Rev	
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								Date:		Thursday, September 06, 2007		Sheet 23 of 49	

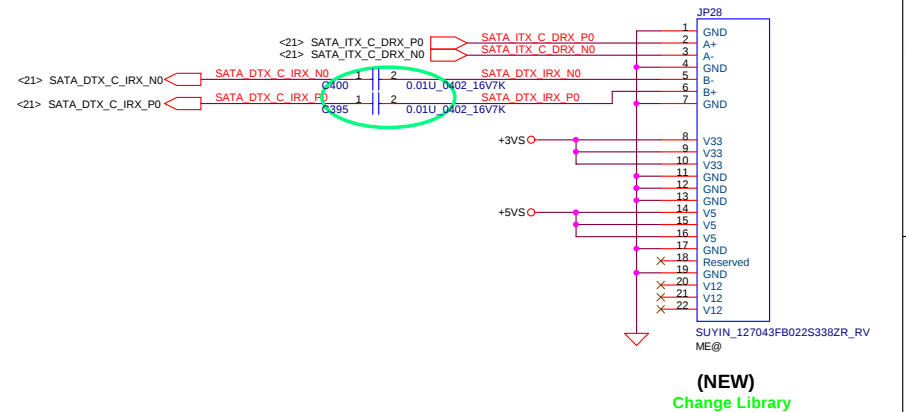
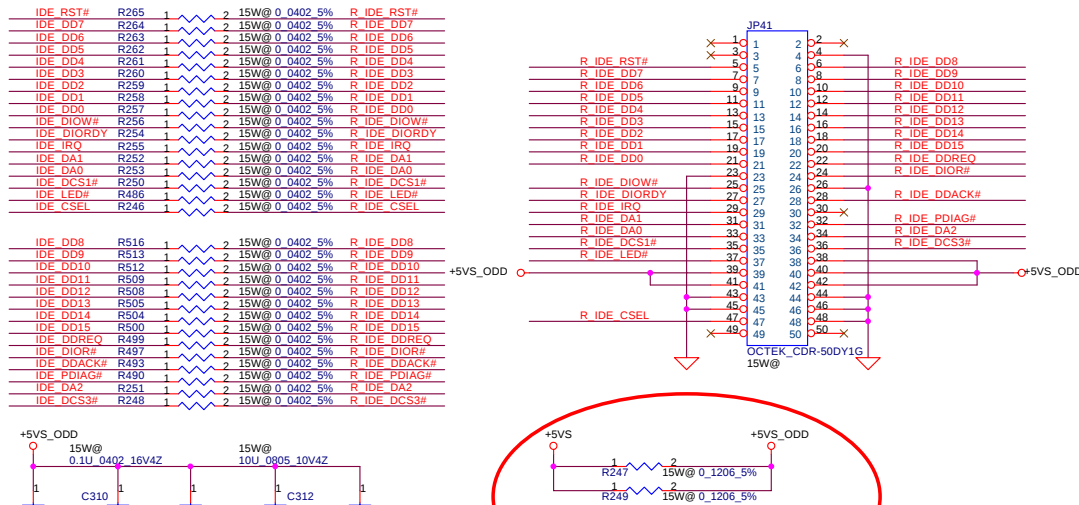
14W ODD Conn.



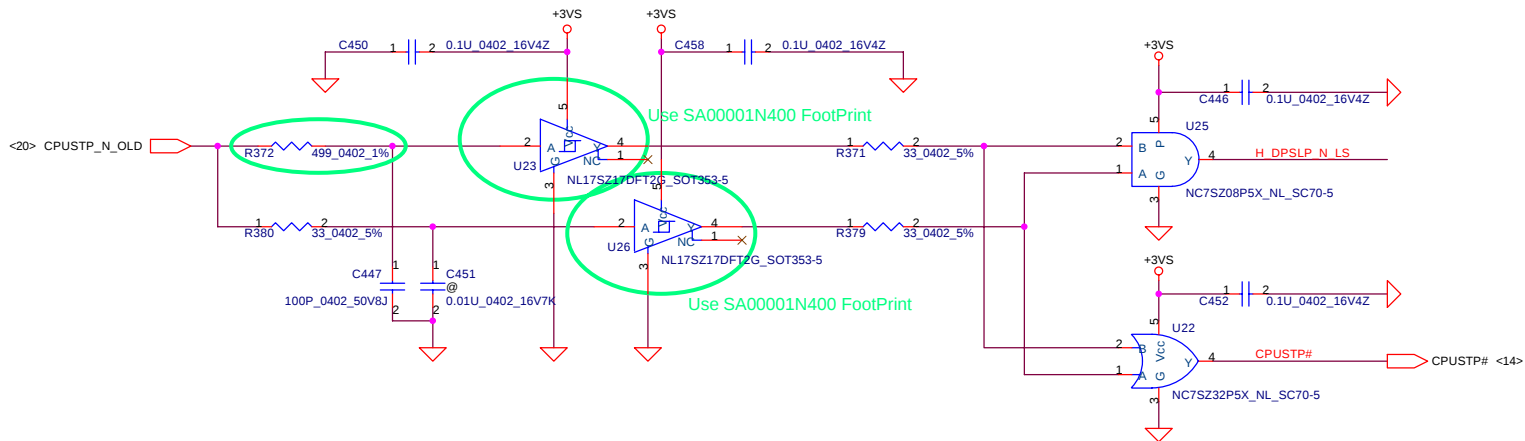
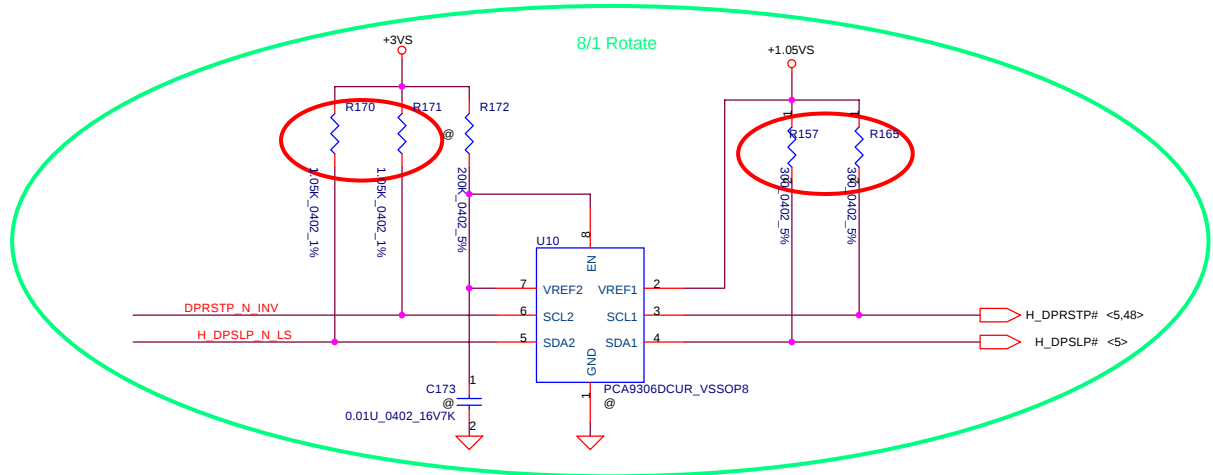
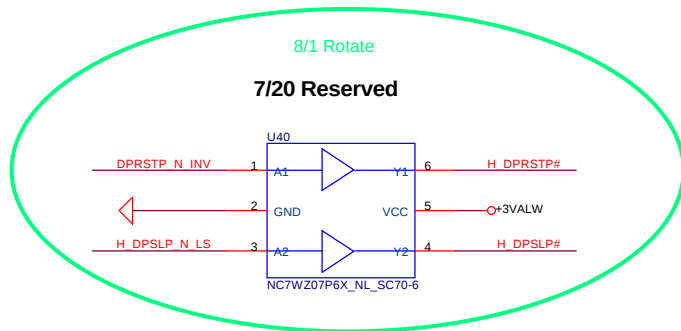
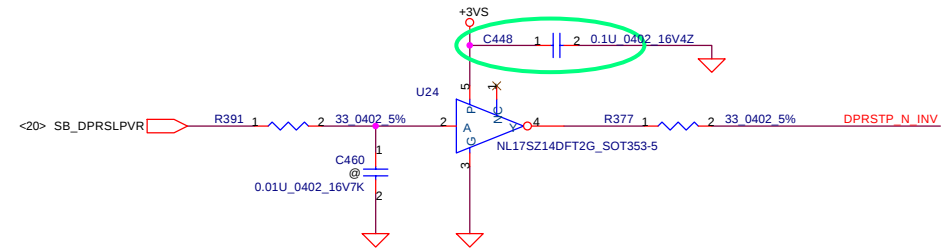
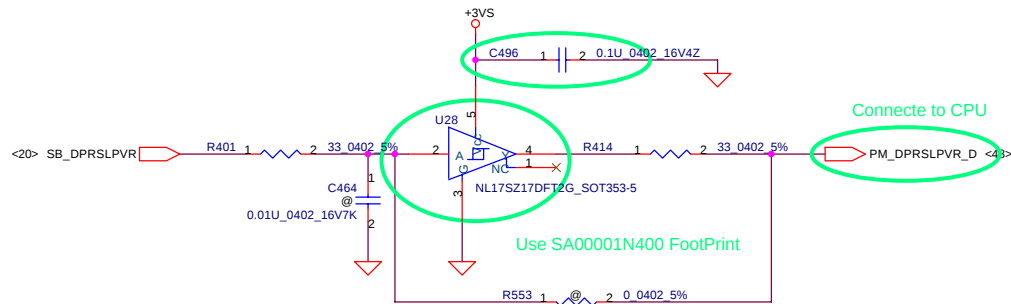
SATA HDD Conn.



15W ODD Conn.

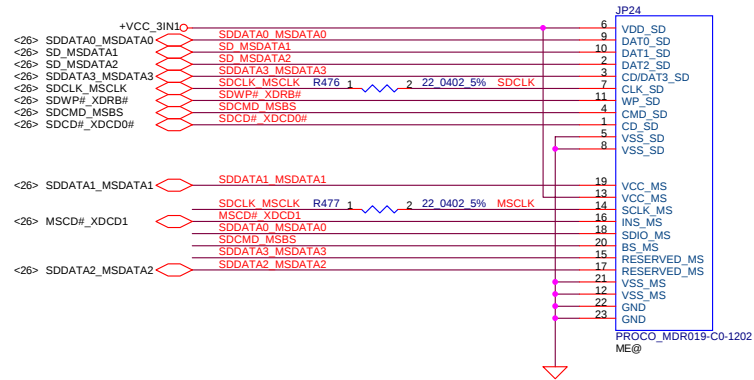


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Size	Document Number	JFWXX M/B LA-3961P Schematic		Rev	
B				0.1	
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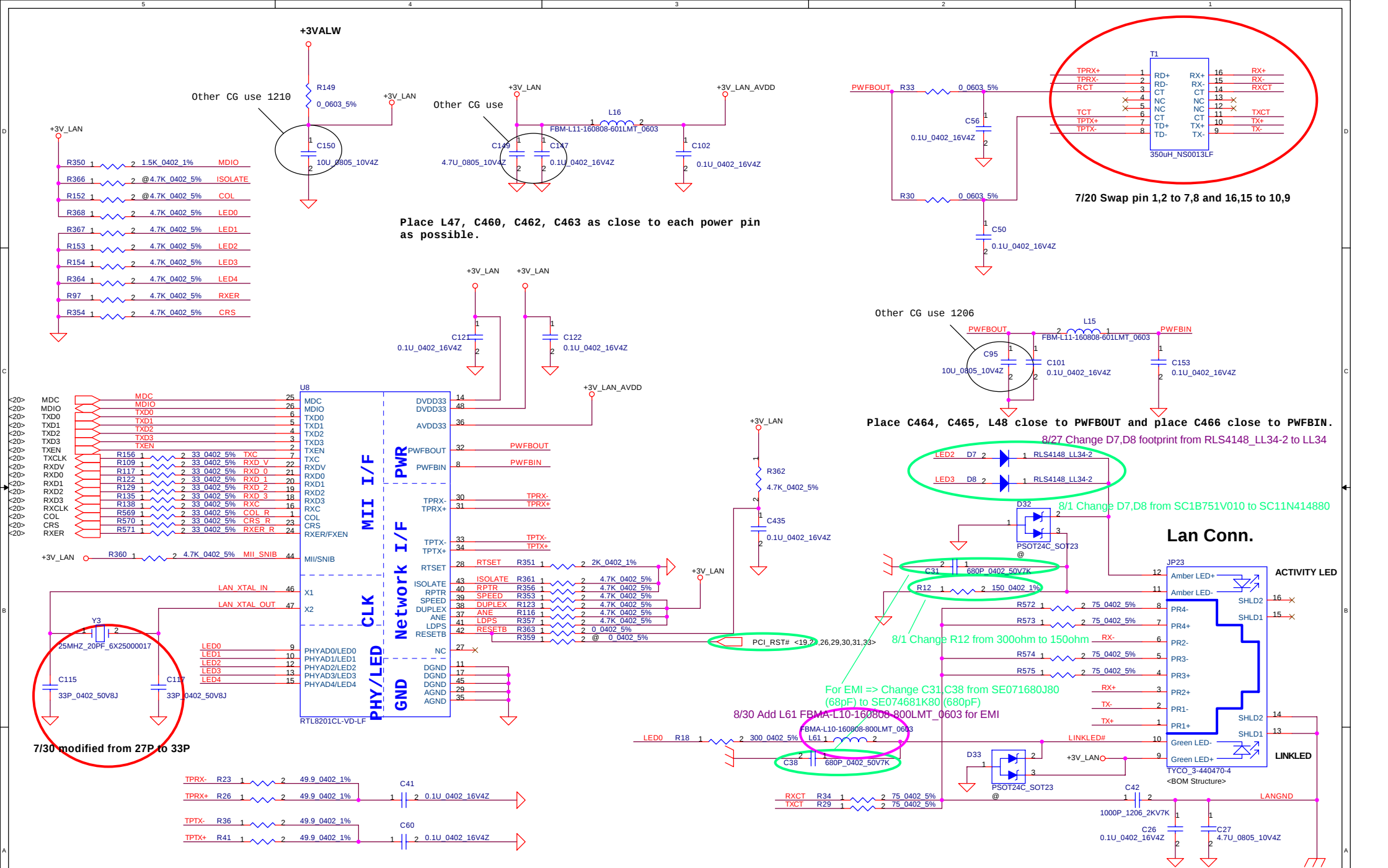


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Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title <Title>
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3 in 1 Card Reader



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				Date: Thursday, September 06, 2007	Sheet 27 of 49

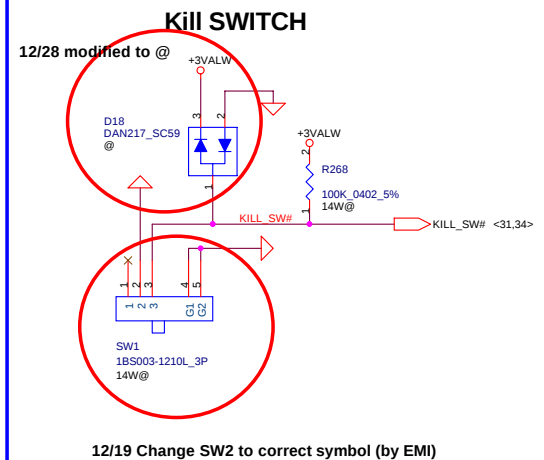
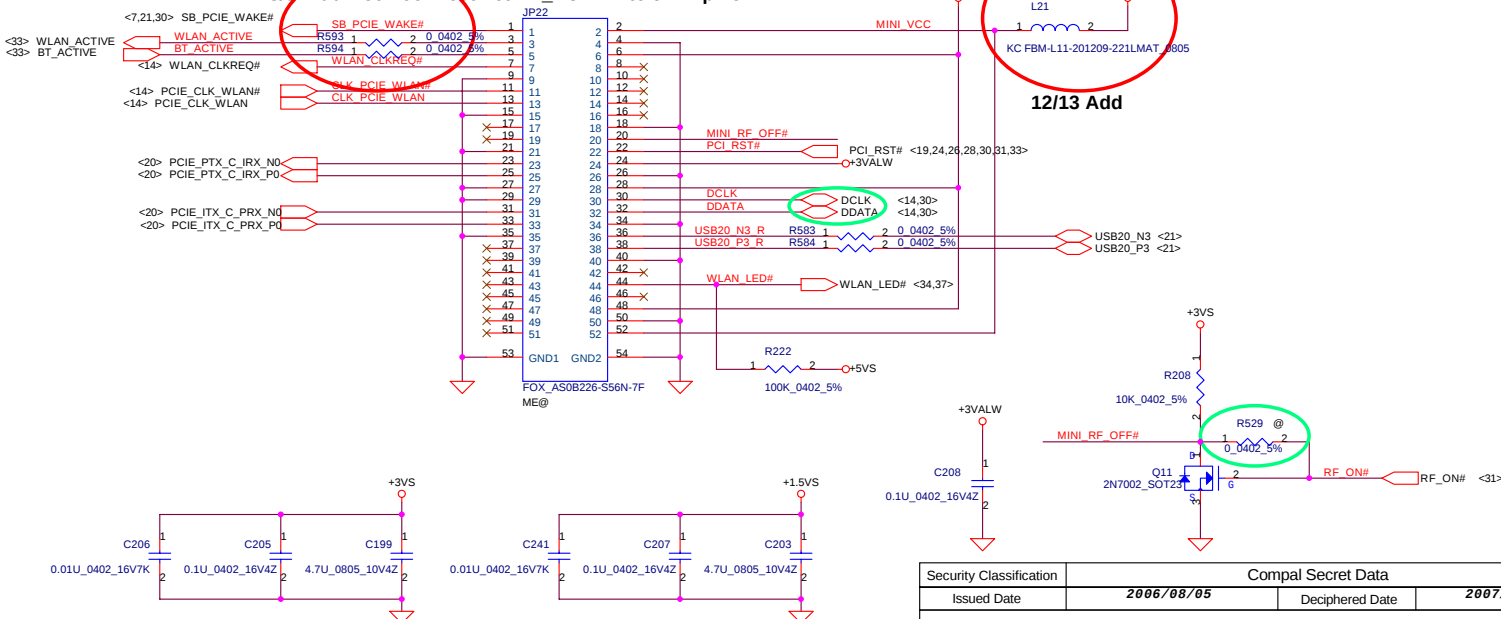


LED0 LED1 LED2 LED3 LED4
Link Dupx 10Act 100Act COL

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		JFWXX M/B LA-3961P Schematic	
Custom		Date		Thursday, September 06, 2007	
		Sheet		28 of 49	

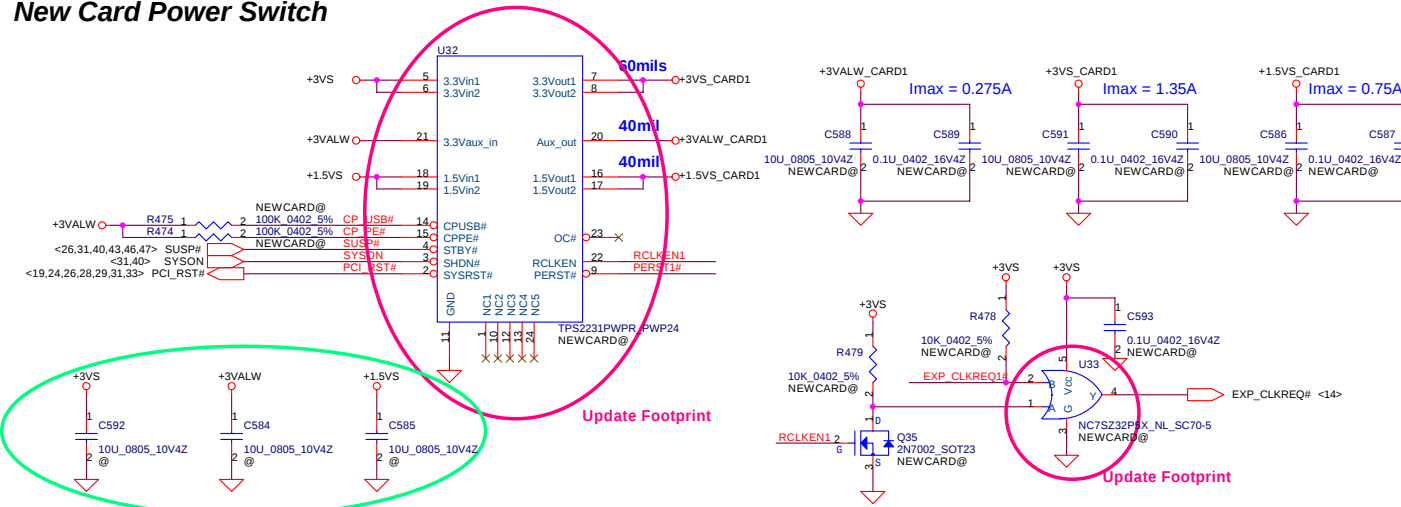
Mini-Express Card for WLAN

8/31 Add R593 connect net WLAN_ACTIVE to JP22 pin3
8/31 Add R594 connect net BT_ACTIVE to JP22 pin5

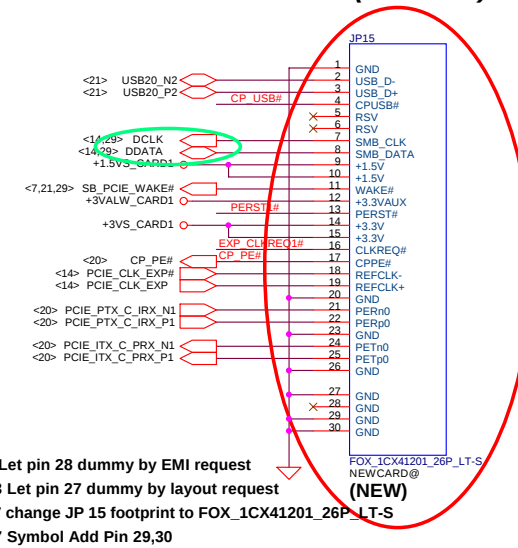


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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/Kill SW	
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				JFWXX	M/B LA-3961P Schematic
				Date:	Thursday, September 06, 2007
				Sheet	29 of 49
				Rev	0.1

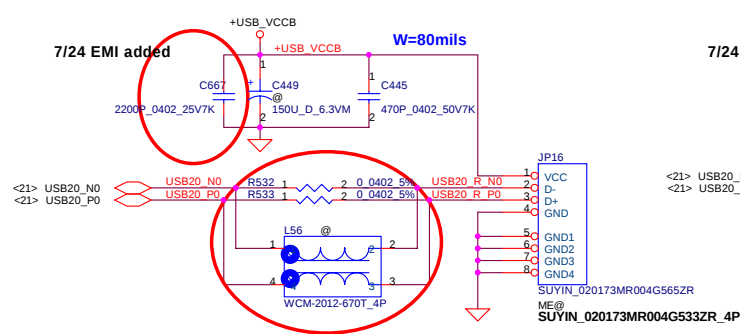
New Card Power Switch



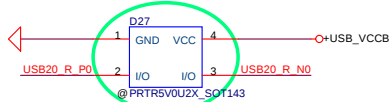
New Card Socket (Left/TOP)



USB CONN. 1

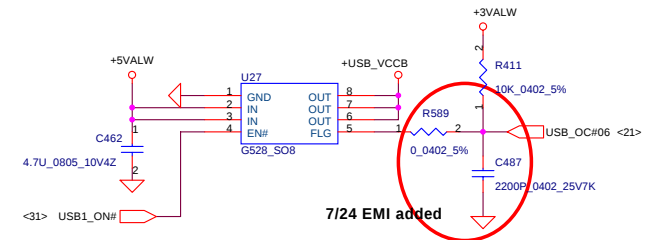
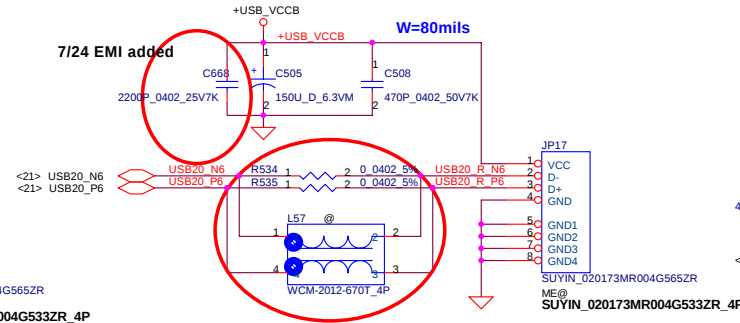


For EMI => Add R532,R533,R534,R535 (SD028000080) ,L56,L57 (SM070000I00)
7/30 change L56,57 to SM070000K00 by EMI request

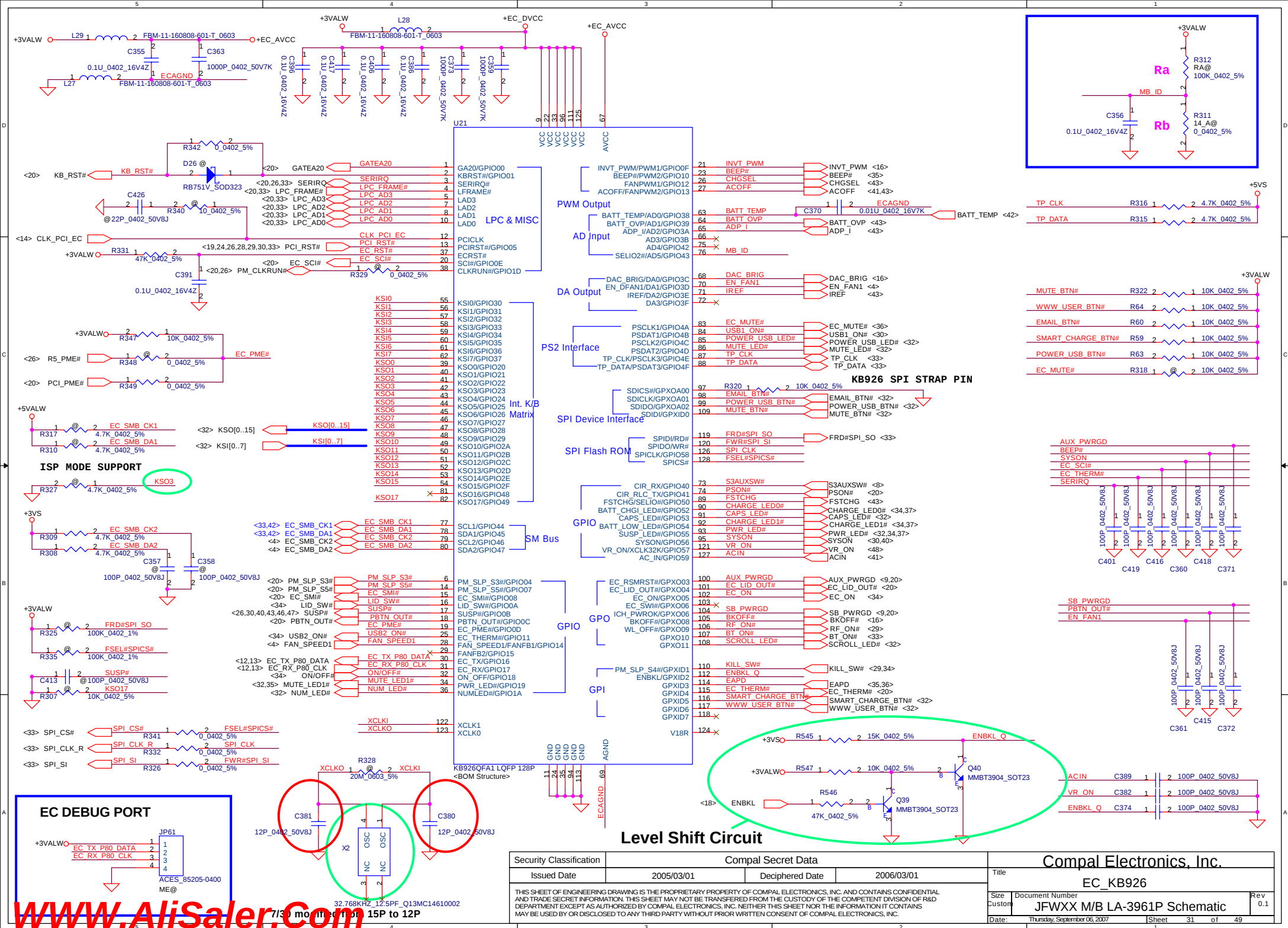


For EMI => Change D27,D28 from SC300000100 to SC300000P00

USB CONN. 2

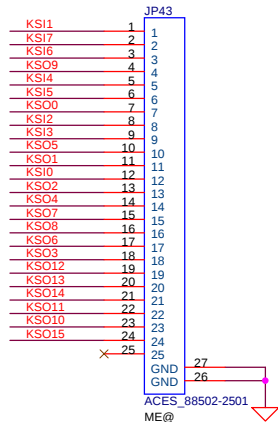


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title NewCard & USB Connector		
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				JFWXX M/B LA-3961P Schematic		
				Date: Thursday, September 06, 2007	Sheet 30 of 49	

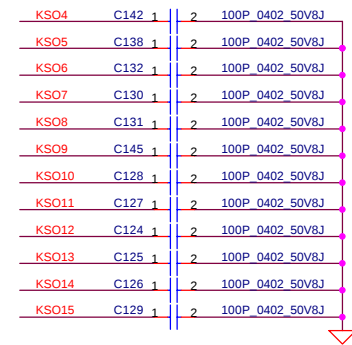
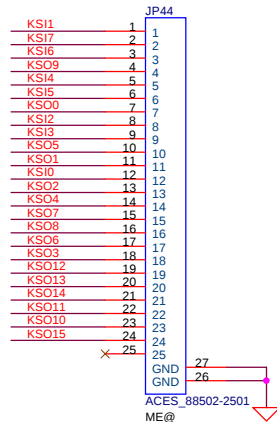


INT_KBD Conn.

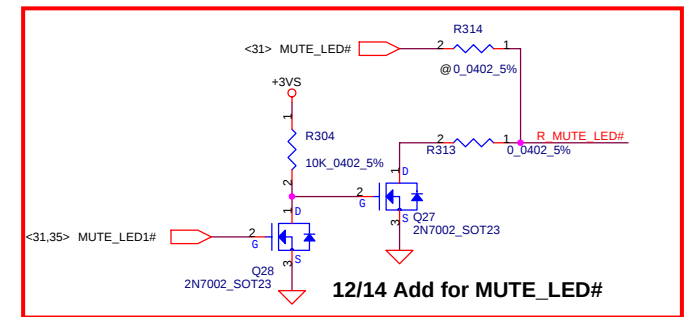
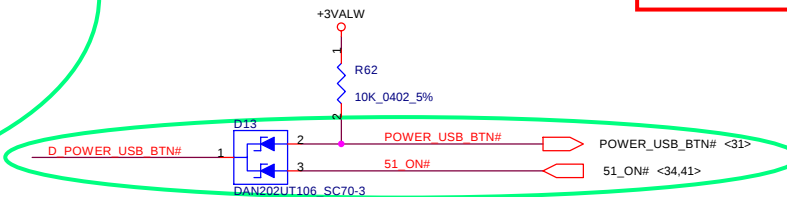
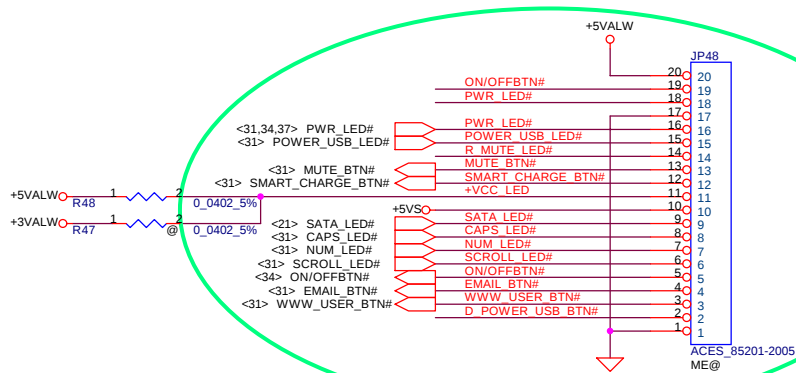
For JFW91



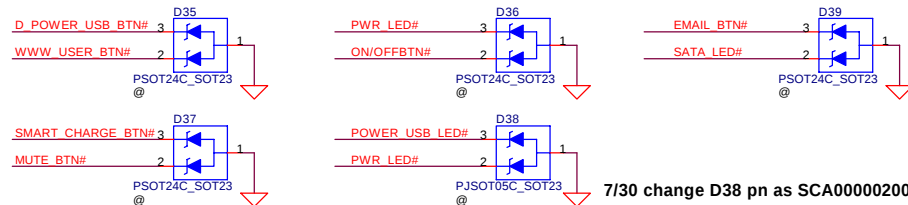
For JFW01



Switch Board Conn.



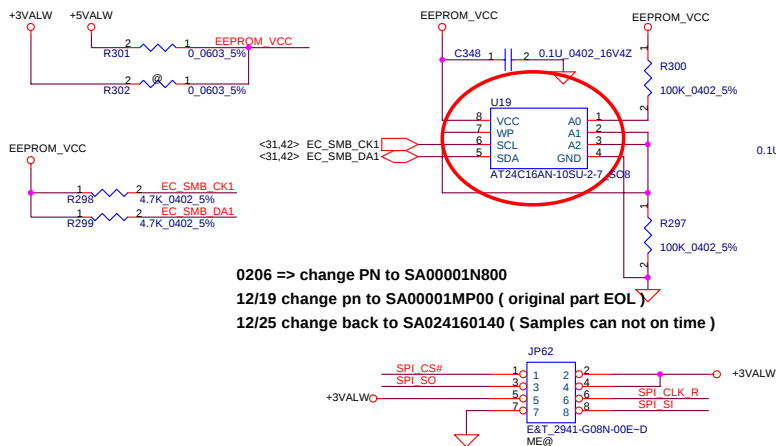
7/30 EMI added



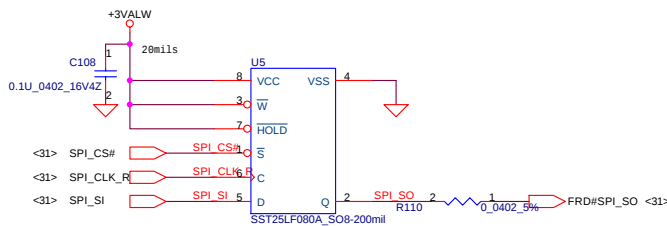
7/30 change D38 pn as SCA00000200

8/1 Change D38 value PSOT24C_SOT23 from to PJSOT05C_SOT23 , Add D39

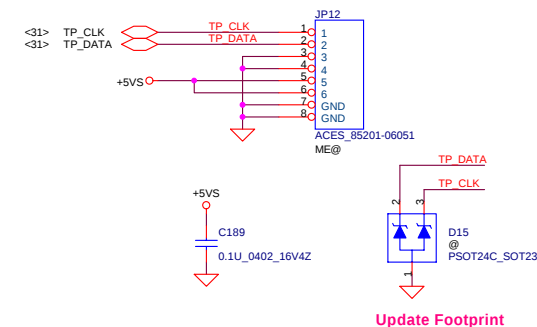
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Size	Document Number	JFWXX M/B LA-3961P Schematic		Rev	
Date	Thursday, September 06, 2007	Sheet	32	of	49



8M SPI ROM



To TP/B Conn.

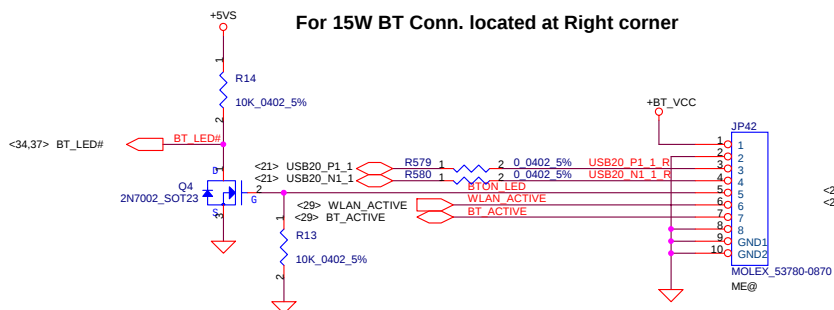


Bluetooth Conn.

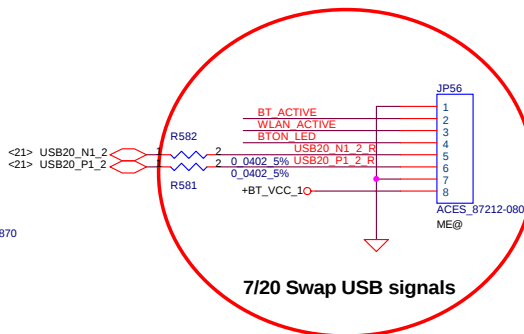
Need to check BT pin definition again!

9/20 modified this block

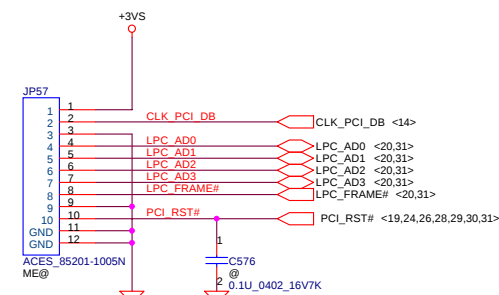
For 15W BT Conn. located at Right corner



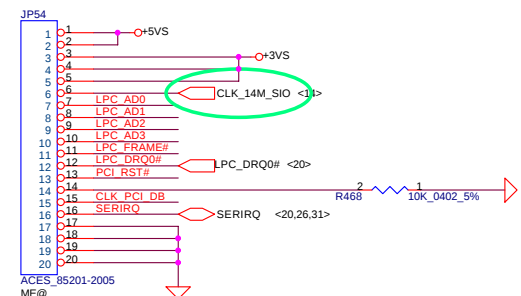
For 14W BT Conn. located at Left corner



FOR LPC DEBUG PORT

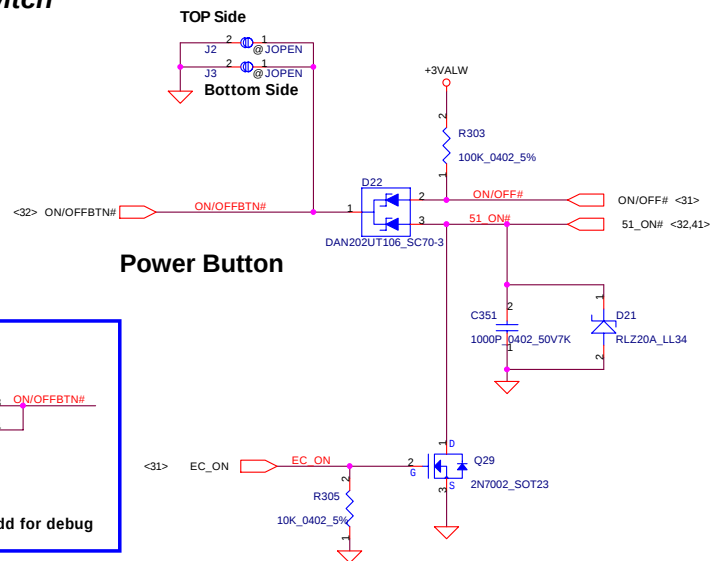


FOR LPC SIO DEBUG PORT

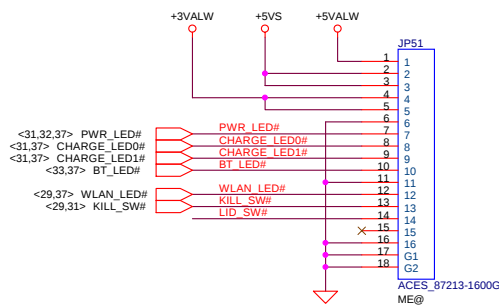


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Size	B	Document Number	JFWXX M/B LA-3961P Schematic	Rev	0.1	
Date:	Thursday, September 06, 2007	Sheet	33	of	49	

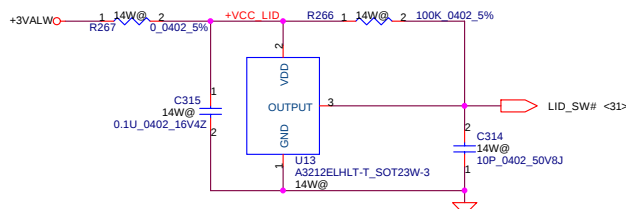
ON/OFF switch



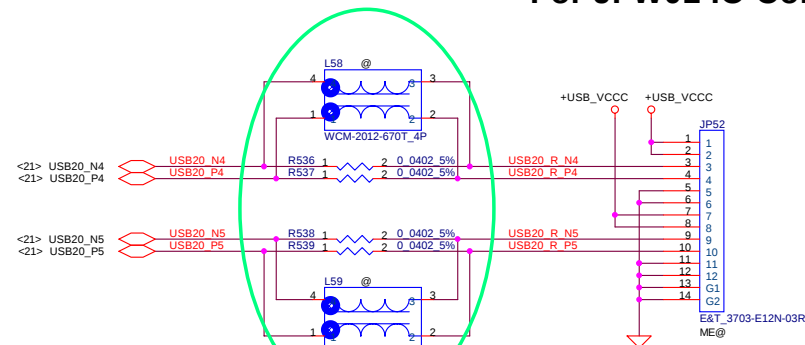
Front LED Board



Lid Switch



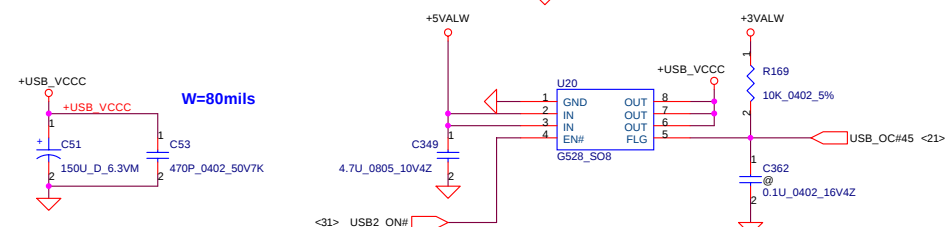
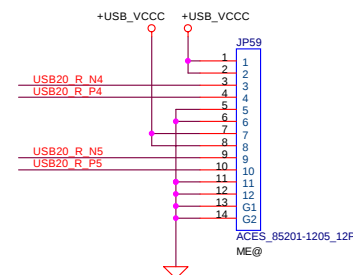
For JFW01 IO Conn.



For EMI => Add R536,R537,R538,R539 (SD028000080) ,L58,L59 (SM070000I00)
Swap L58,L59 Pin 1 & Pin 4 , Pin 2 & Pin 3

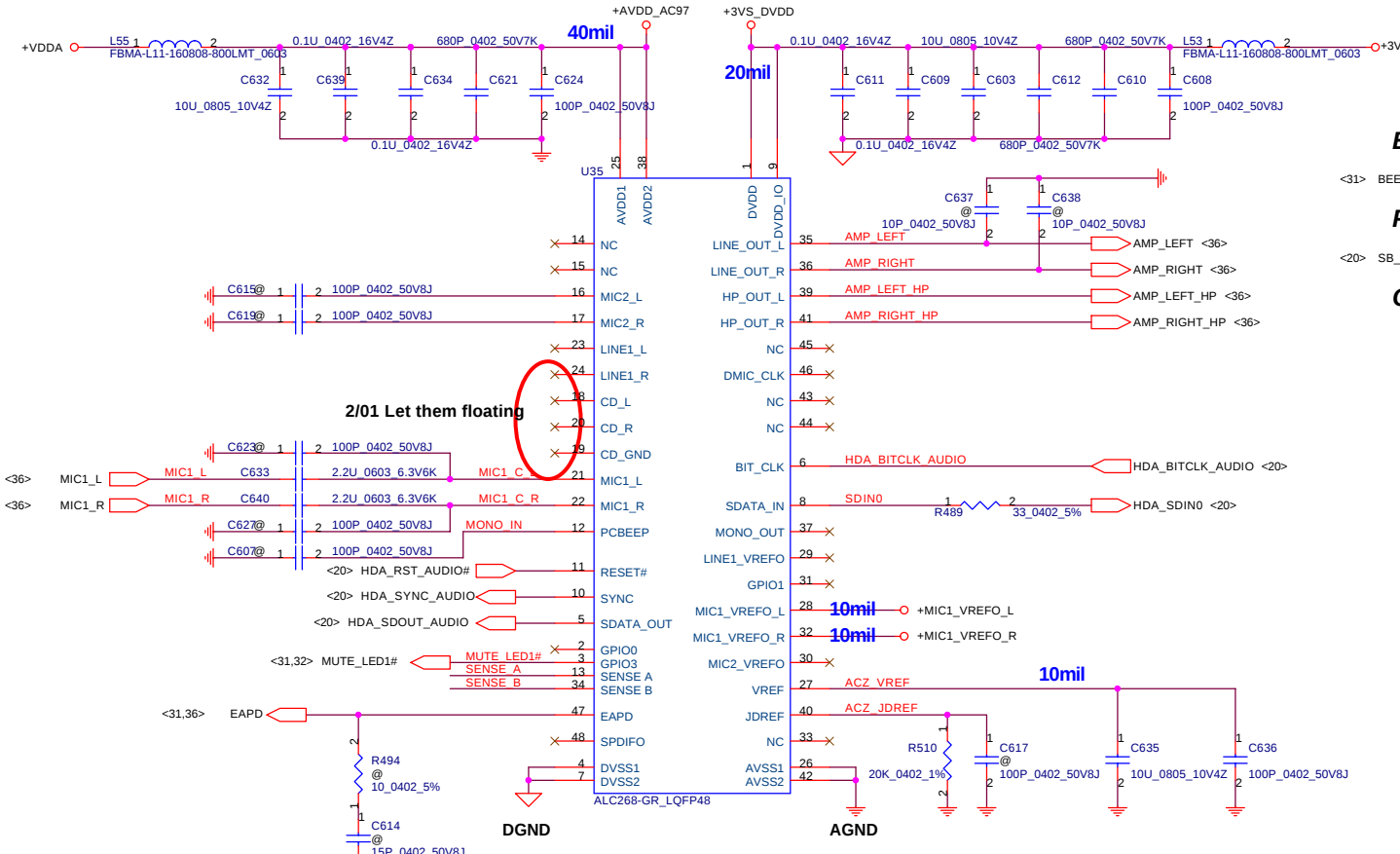
7/30 change L58,59 to SM070000K00 by EMI request

For JFW91 IO Conn.



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				PWROK/LID/Front/IO Board				
				Size	Document Number		Rev	
				B		JFWXX M/B LA-3961P Schematic		0.1
				Date:		Thursday, September 06, 2007		Sheet

HD Audio Codec

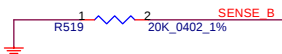


2/01 Let them floating

SENSE FOR Ext. Mic.



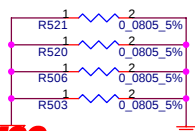
SENSE FOR Solo Int. Mic.



SENSE FOR HP

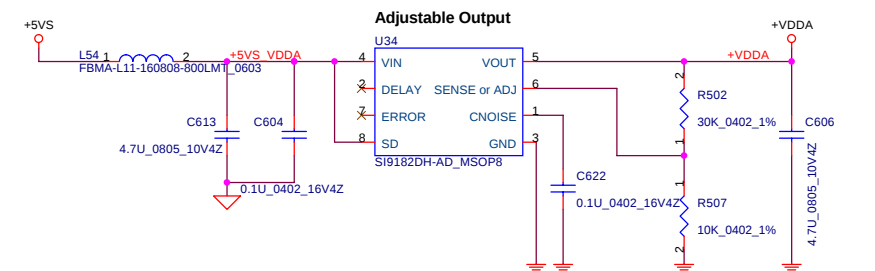


Moat Bridge



Sense Pin	Impedance	Codec Signals	Funncion
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
SENSE B	5.1K	PORT-D (PIN 35, 36)	LINE Out
	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Regulator for CODEC



9/22 Update footprint, Need to check

EC Bleep

PCI Bleep

CardBus Bleep

Need Update Footprint

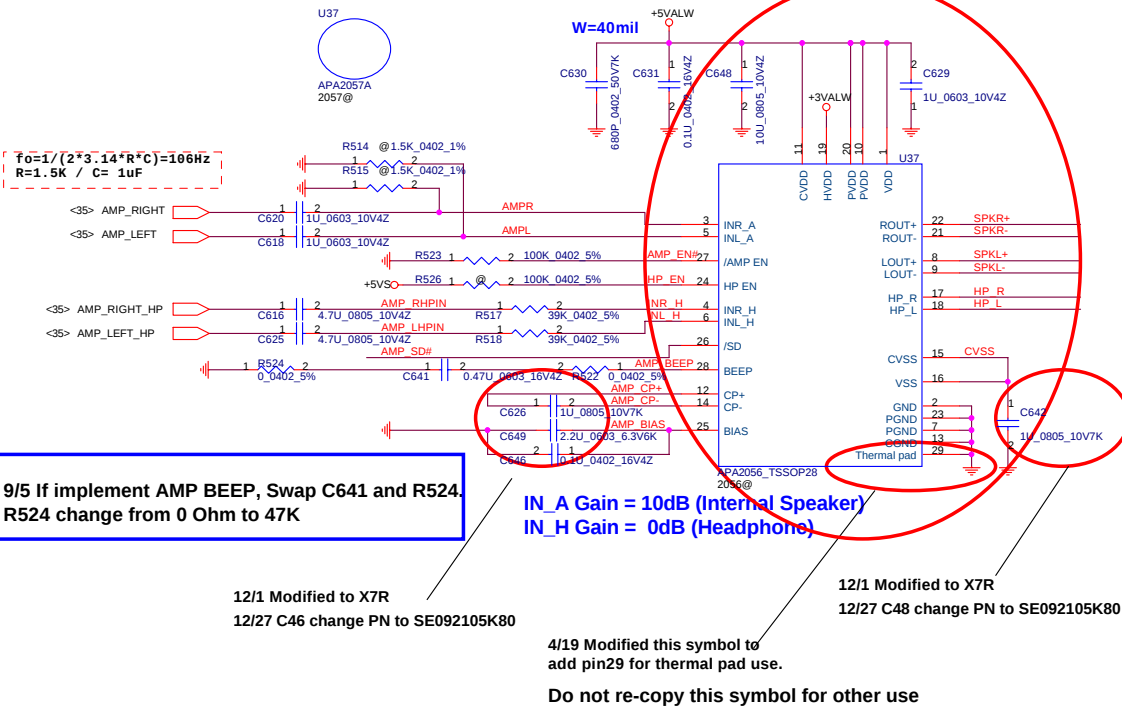
9/19 Realtek suggest And bypass schematic.

7/20 modified

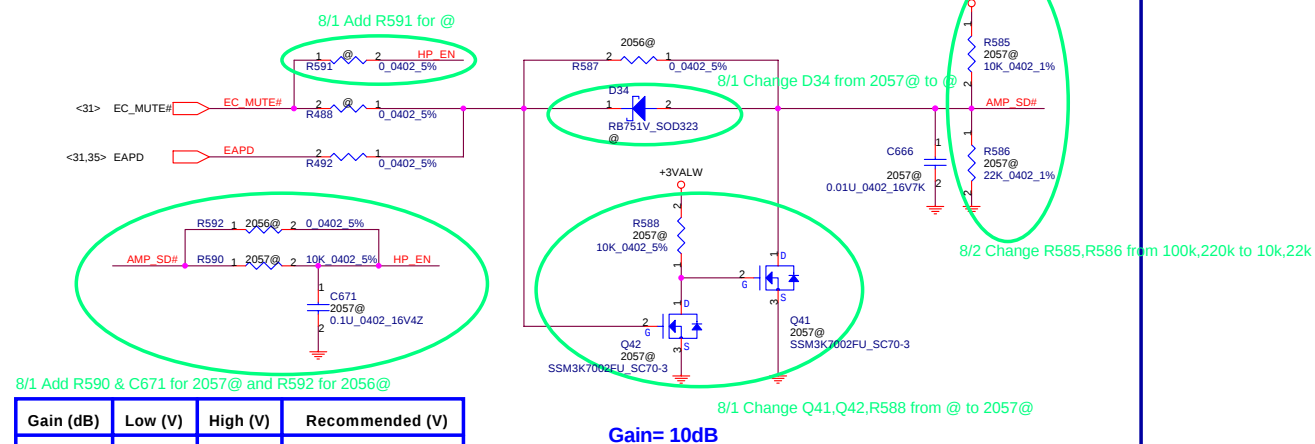
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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	HD Audio Codec ALC268
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APA2056 SPK/HP Amplifier

7/20 Add U37 for APA2057A SA00001QD00



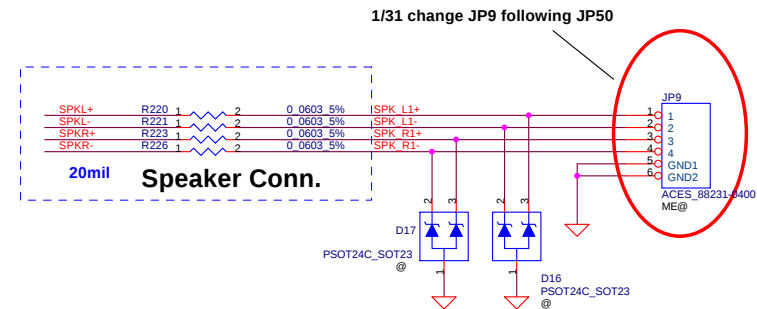
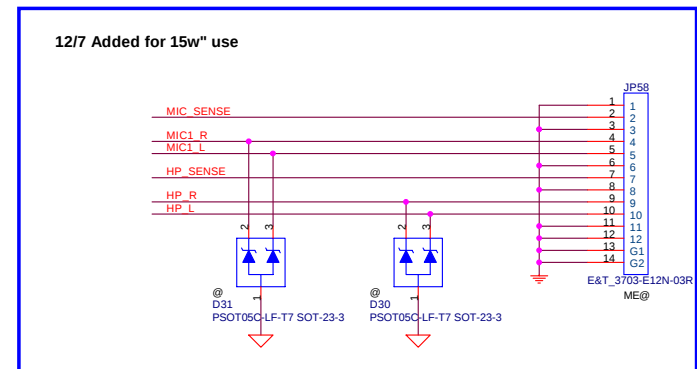
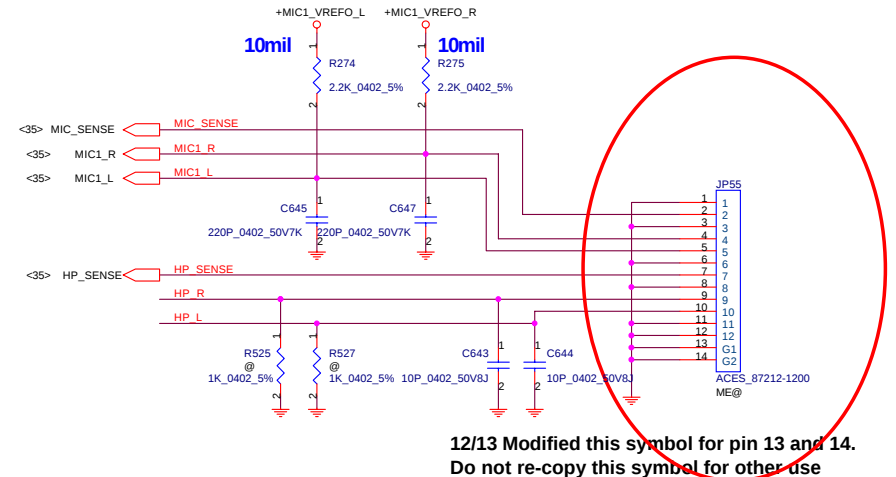
7/20 Add below circuit for APA2057 gain tuning use



Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

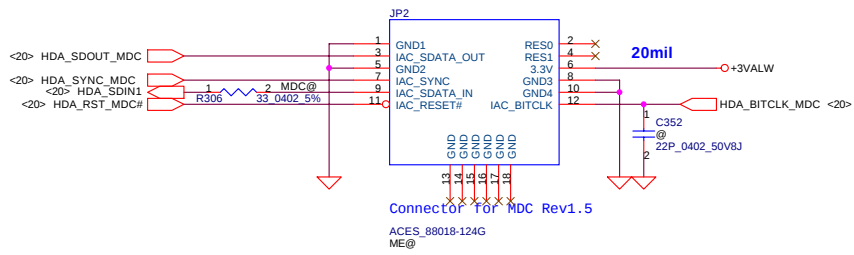
+5VALW assume equal 5.1V

10dB = 5.1 x 220 / 320 = 3.5

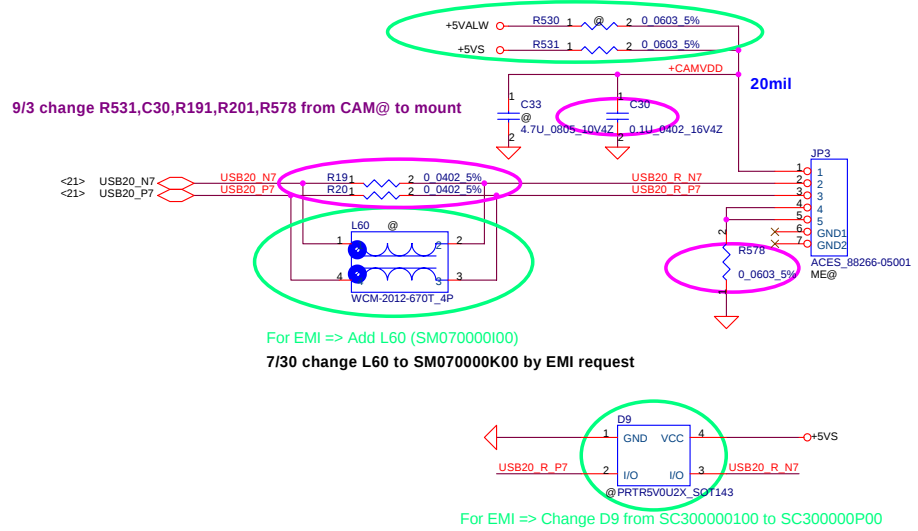


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				Custom	LA-3541P
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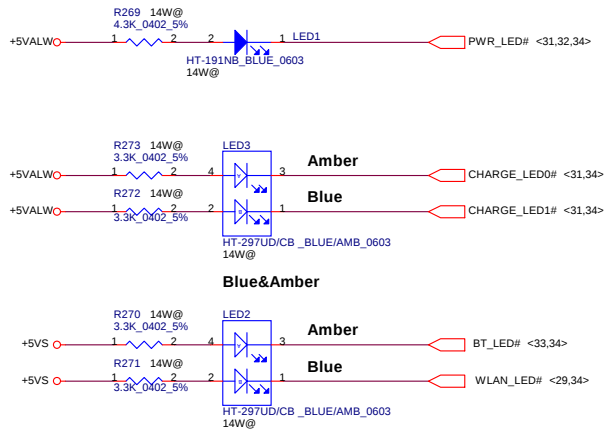
MDC Conn.



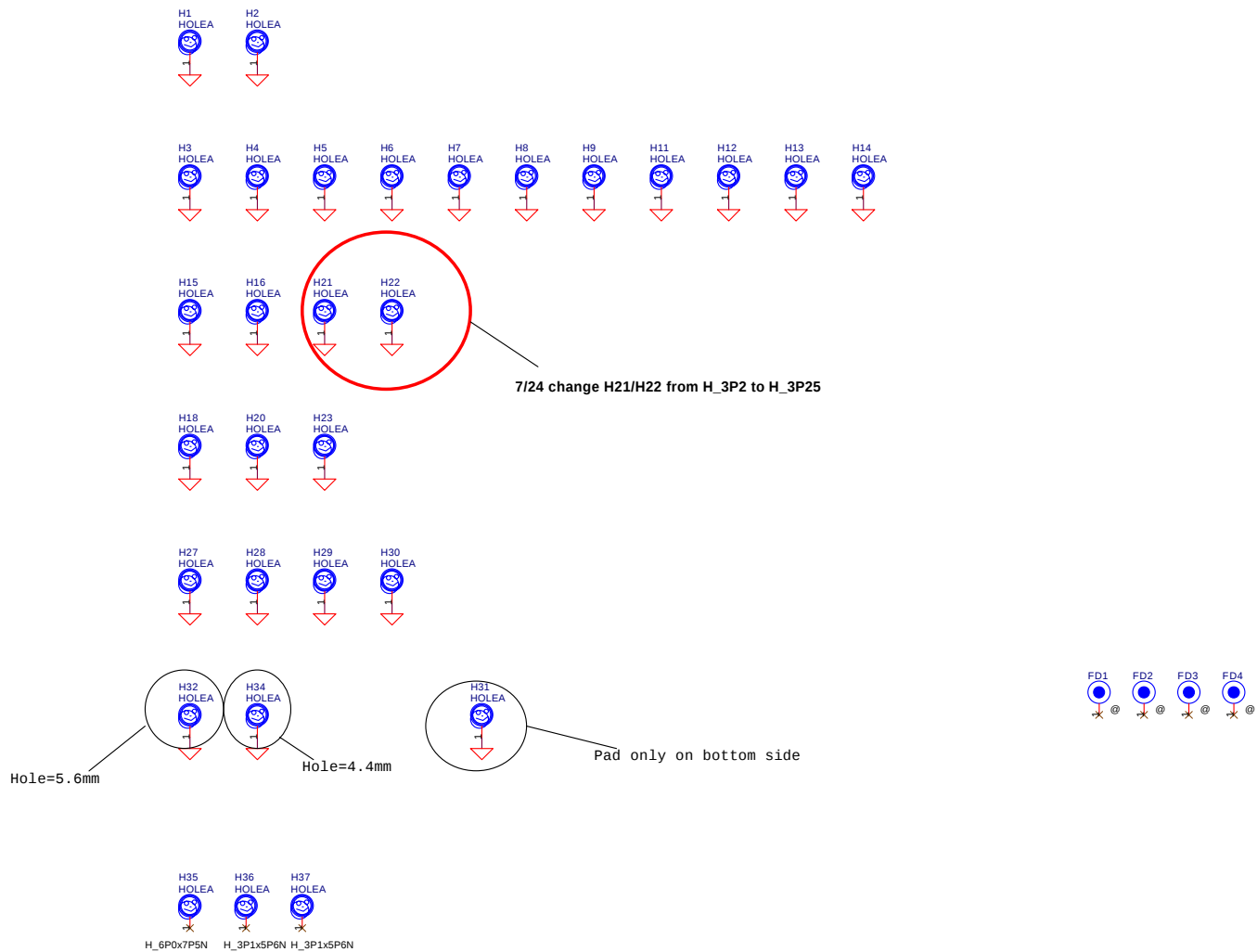
Camera Conn



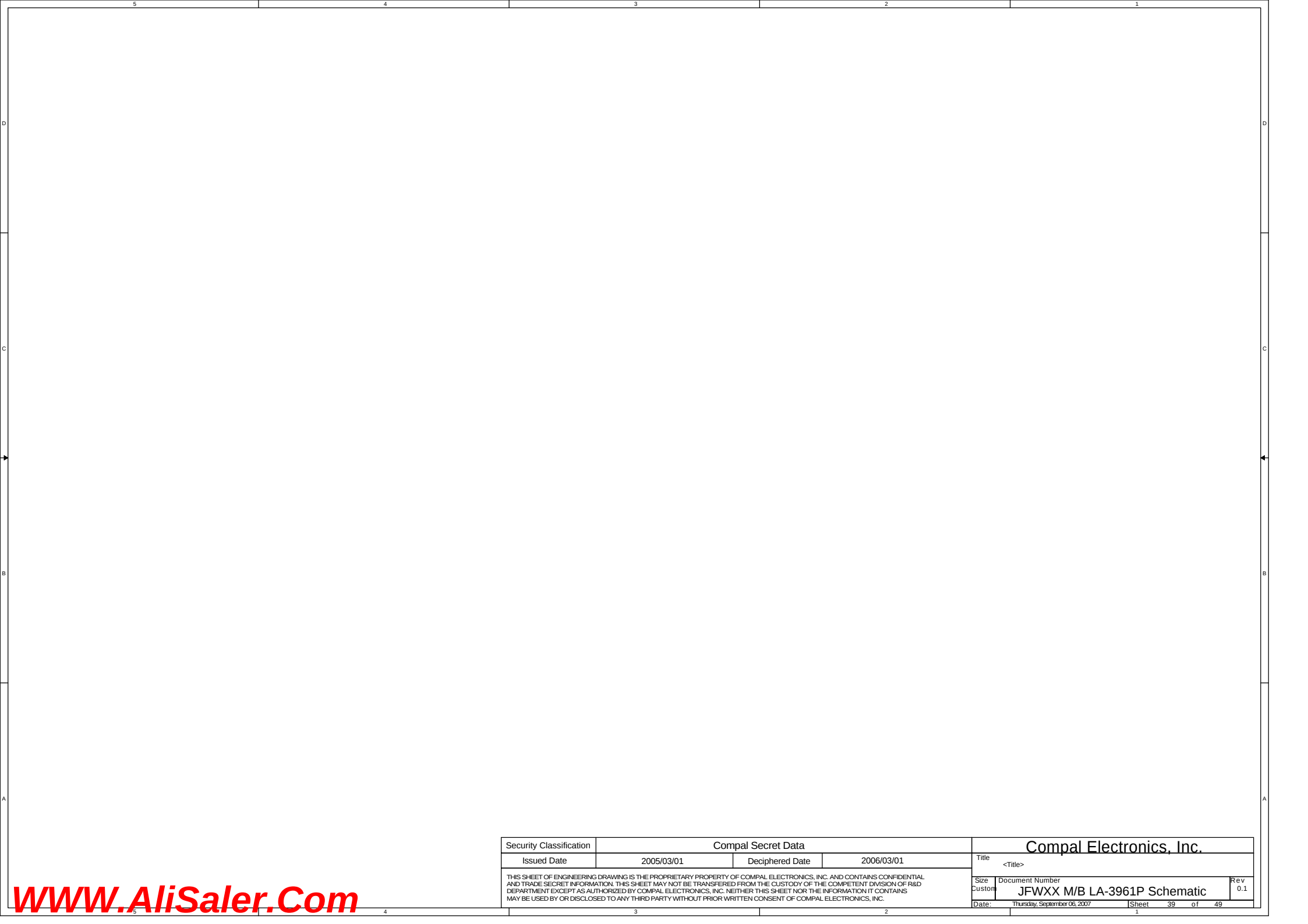
LED



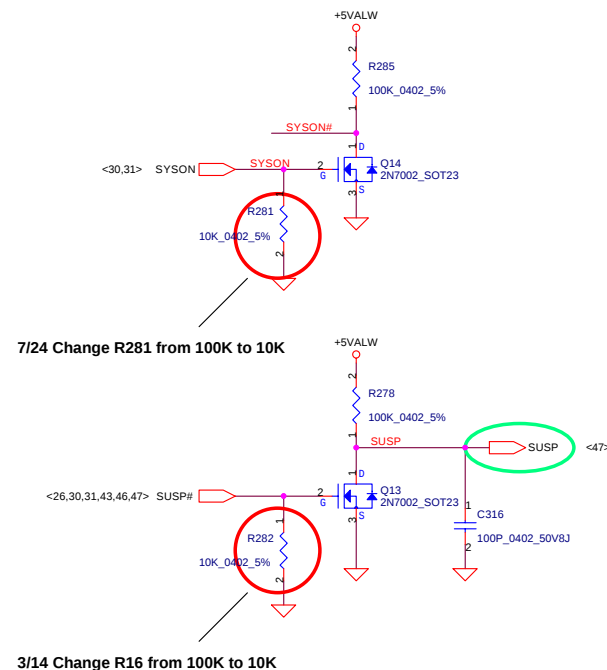
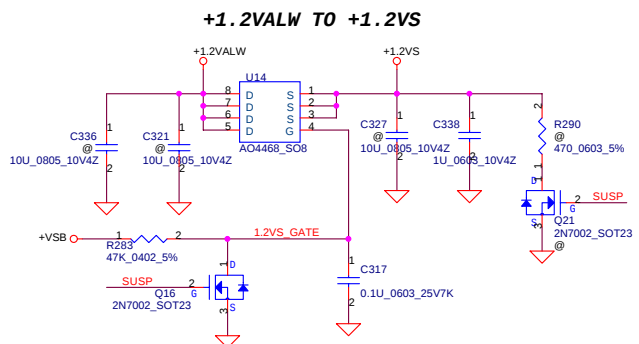
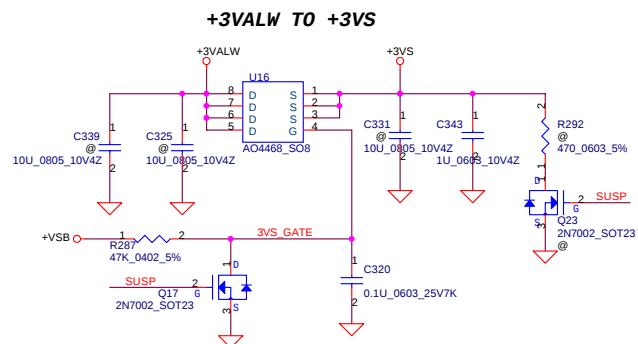
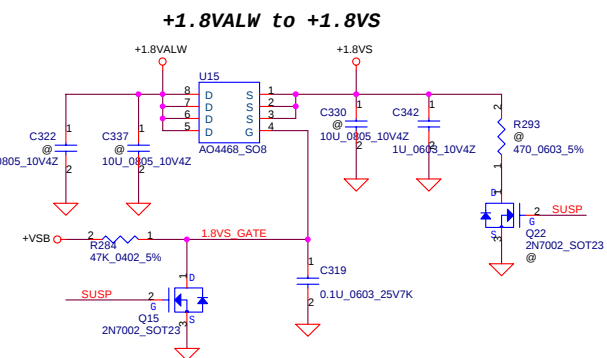
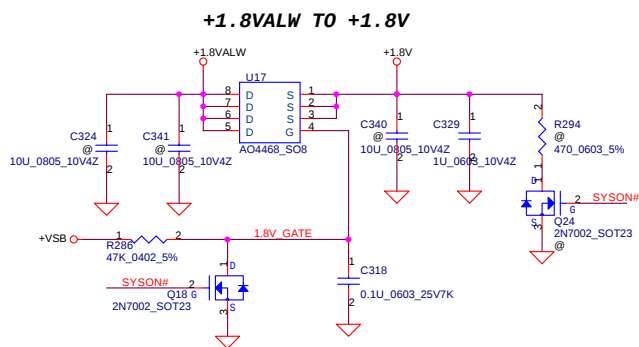
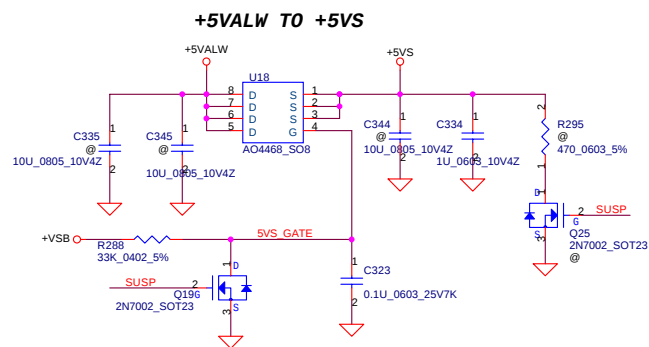
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Issued Date				2006/08/18		Deciphered Date		2007/8/18		Title	
										LED/MDC/CAMERA	
										JFWXX M/B LA-3961P Schematic	
										Rev 0.1	
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Size B	Document Number JFWXX M/B LA-3961P Schematic			Rev 0.1	
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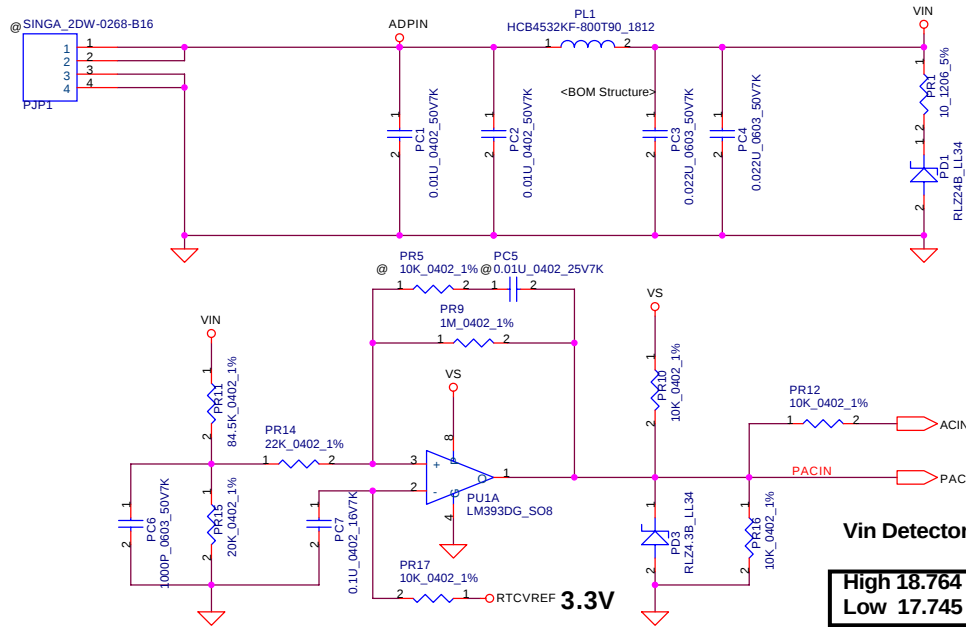


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	DC Interface	
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DC301001Y00



Vin Detector

High	18.764	17.901	17.063
Low	17.745	16.9	16.03

ACIN

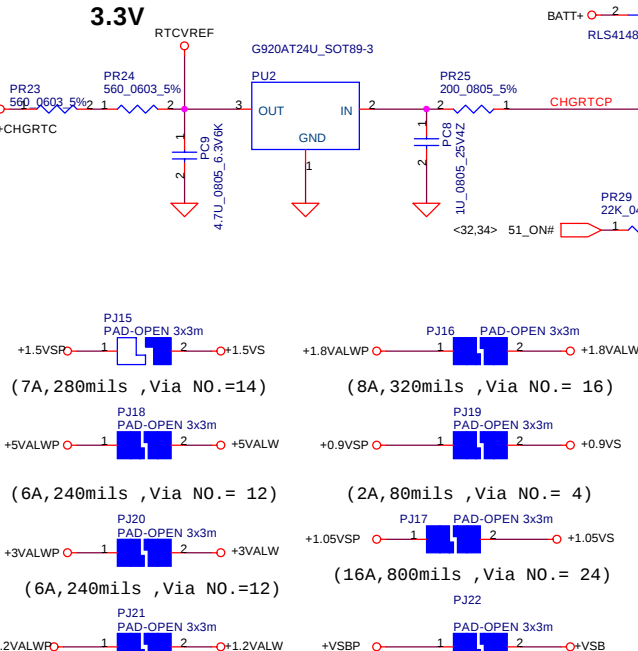
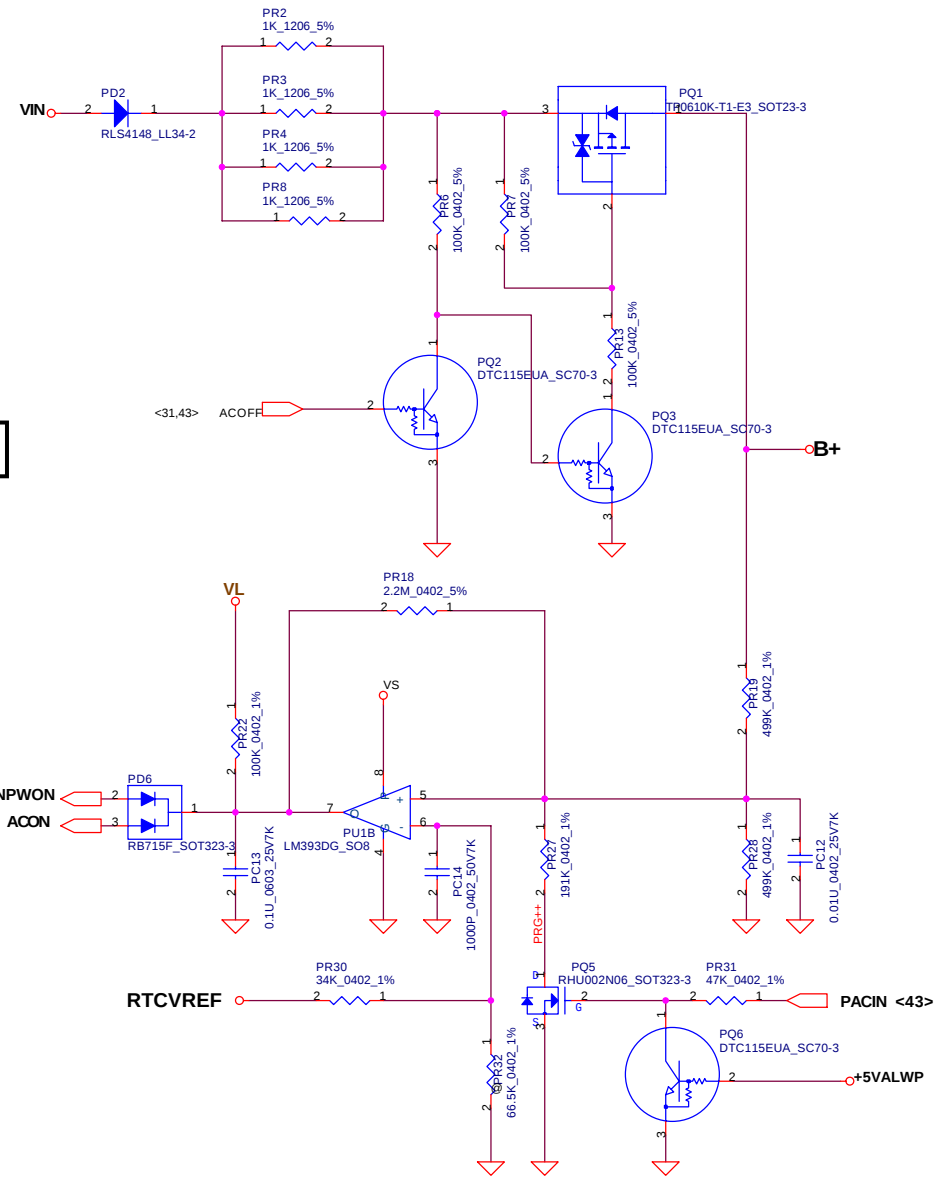
Precharge detector

	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

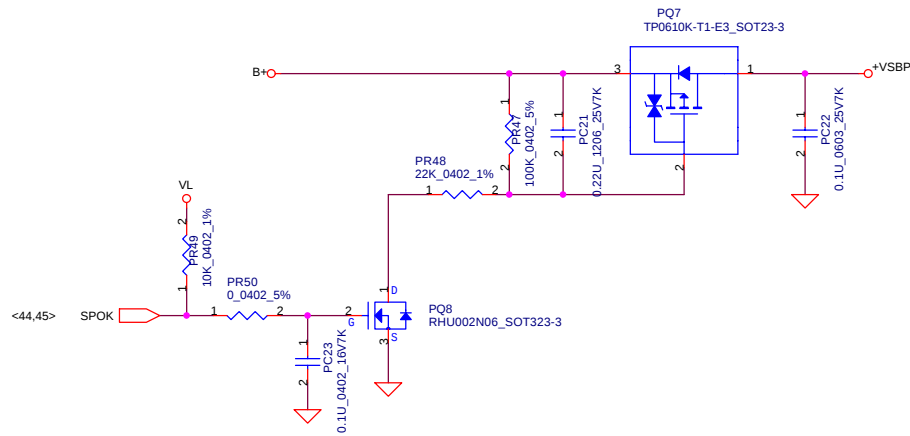
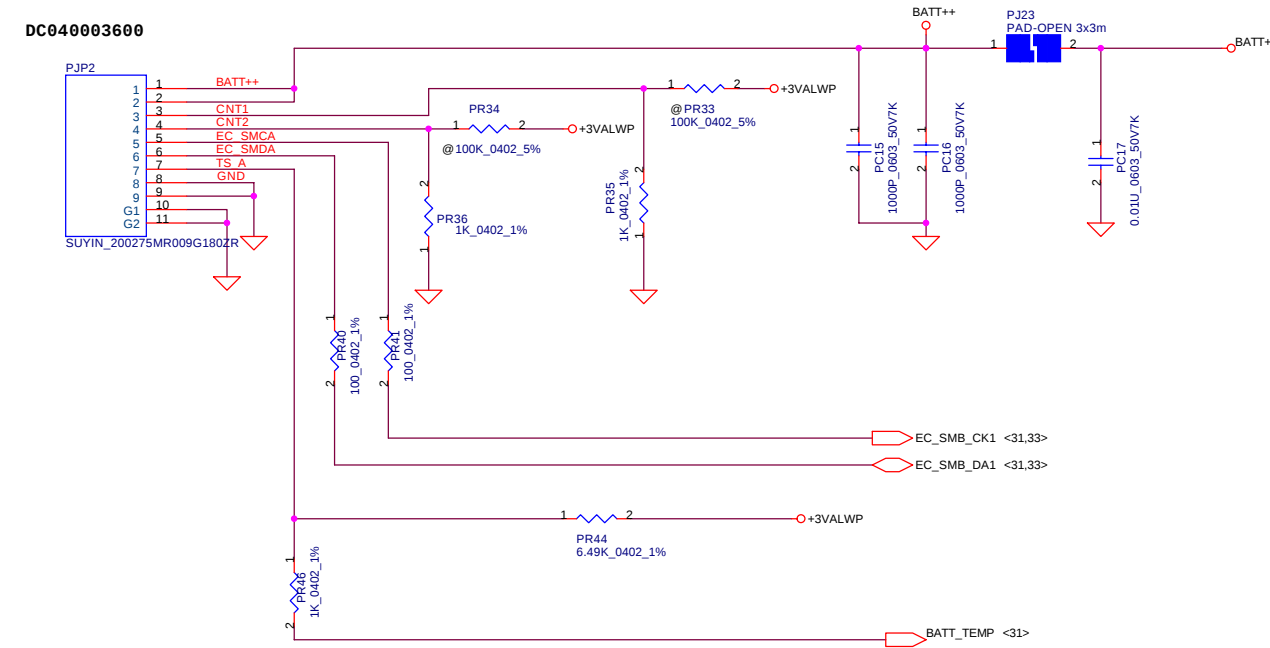
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



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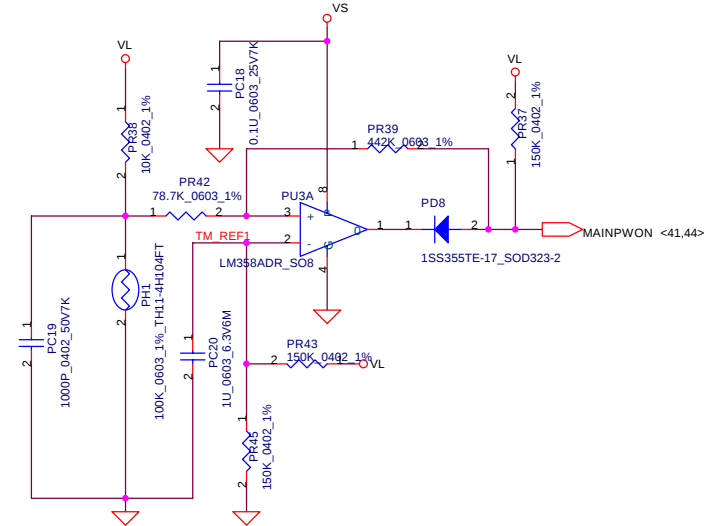
WWW.AliSaler.Com

DC040003600



2/16 Change to 89 degree C for thermal request

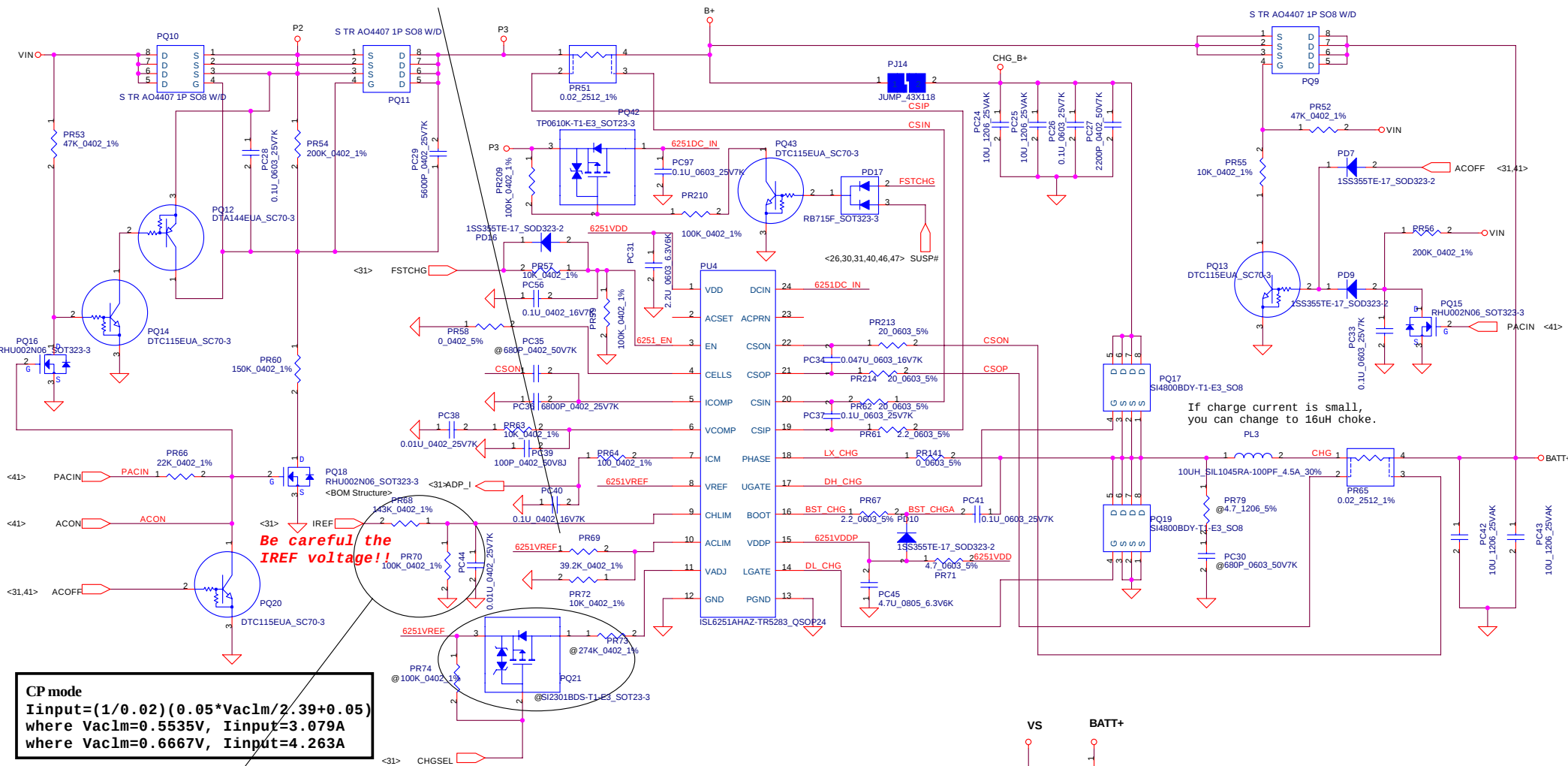
PH1 under CPU bottom side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR74=39.2K, CP=3.079A

ADP_I = 19.9*Iadapter*Rsense



Be careful the IREF voltage!!

If this area float, Charge voltage is 4.2V/cell

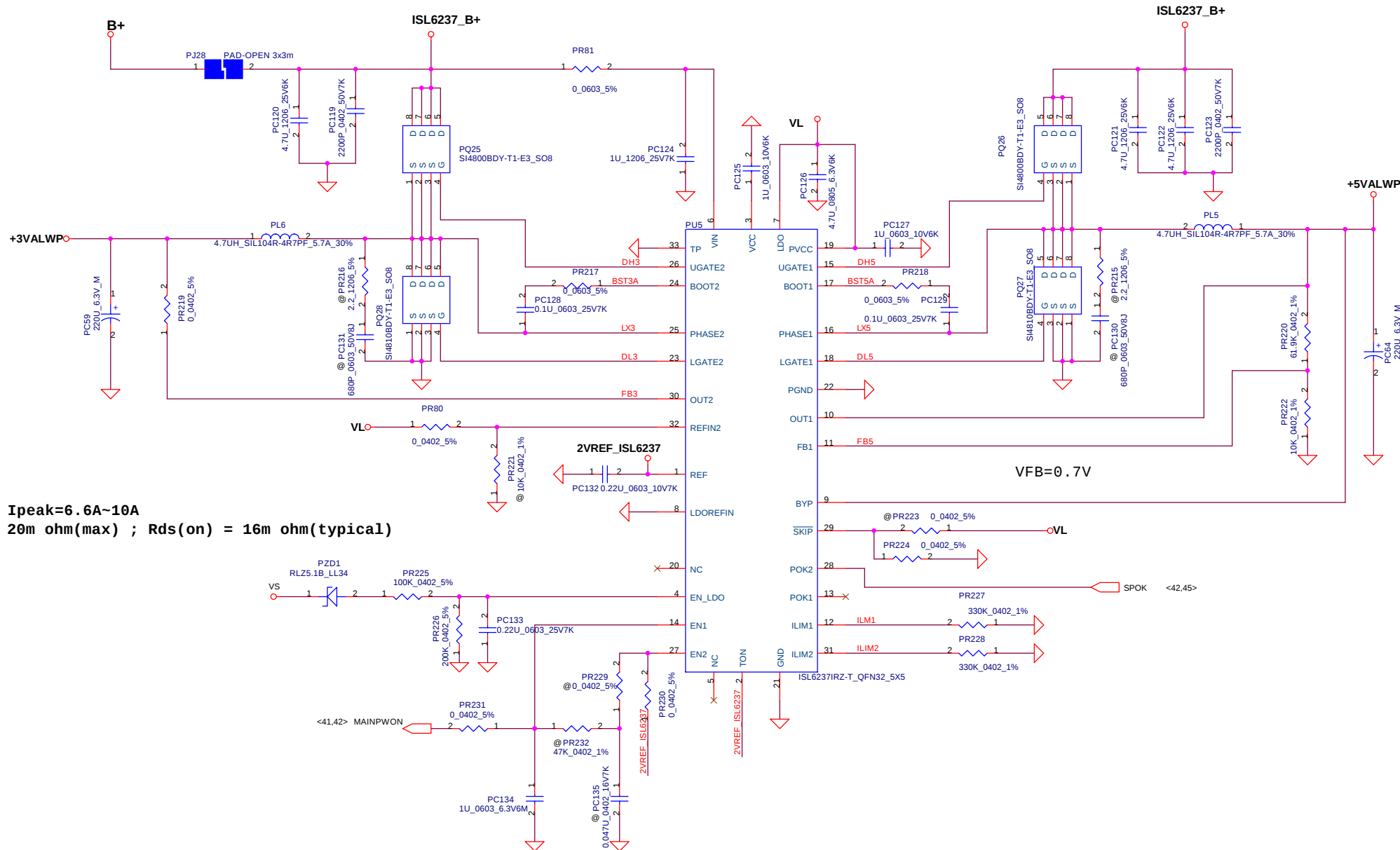
CP mode
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 \cdot I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

If charge current is small, you can change to 16uH choke.

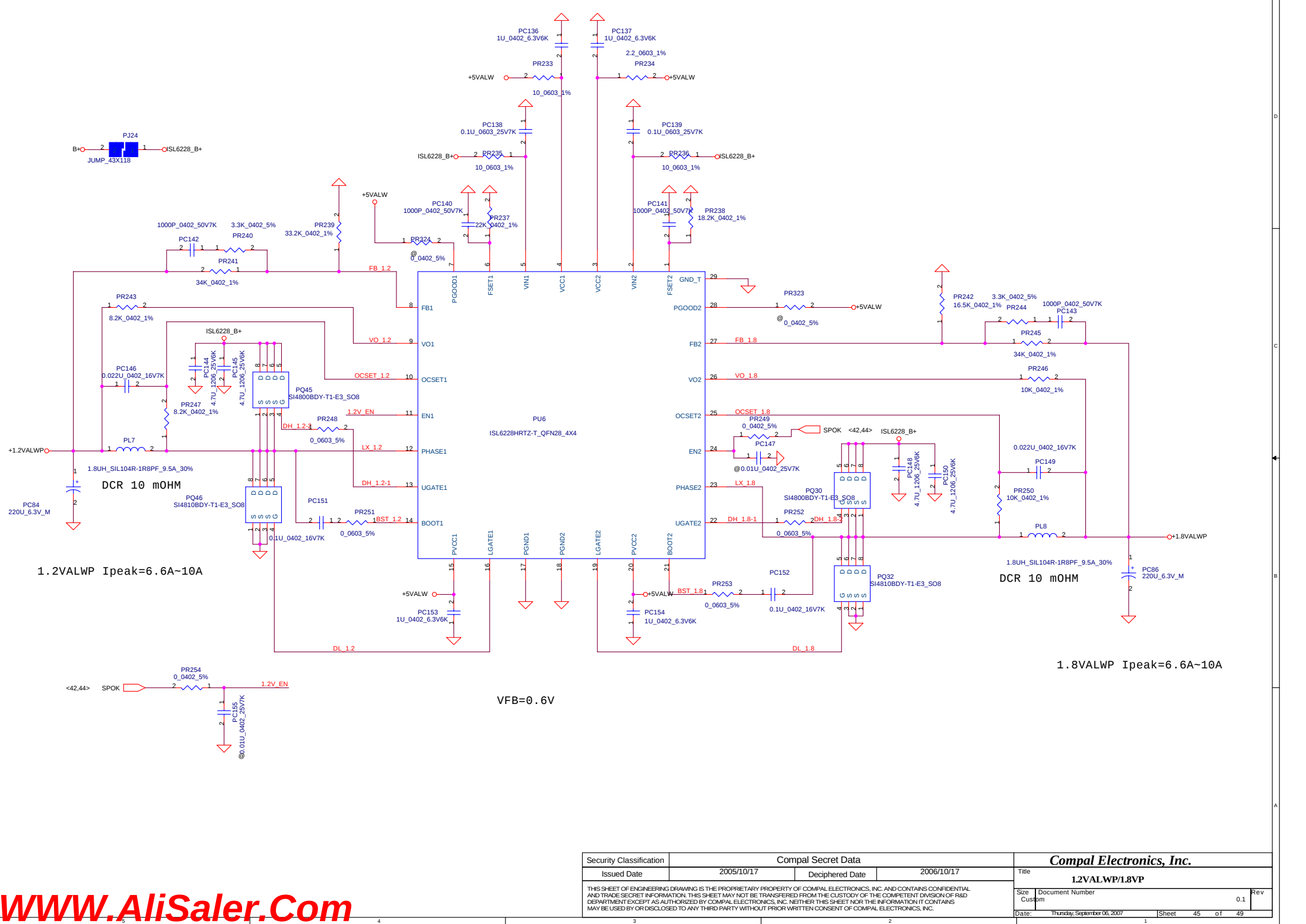
OVP voltage :
 LI-3S : 13.50V -- BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+



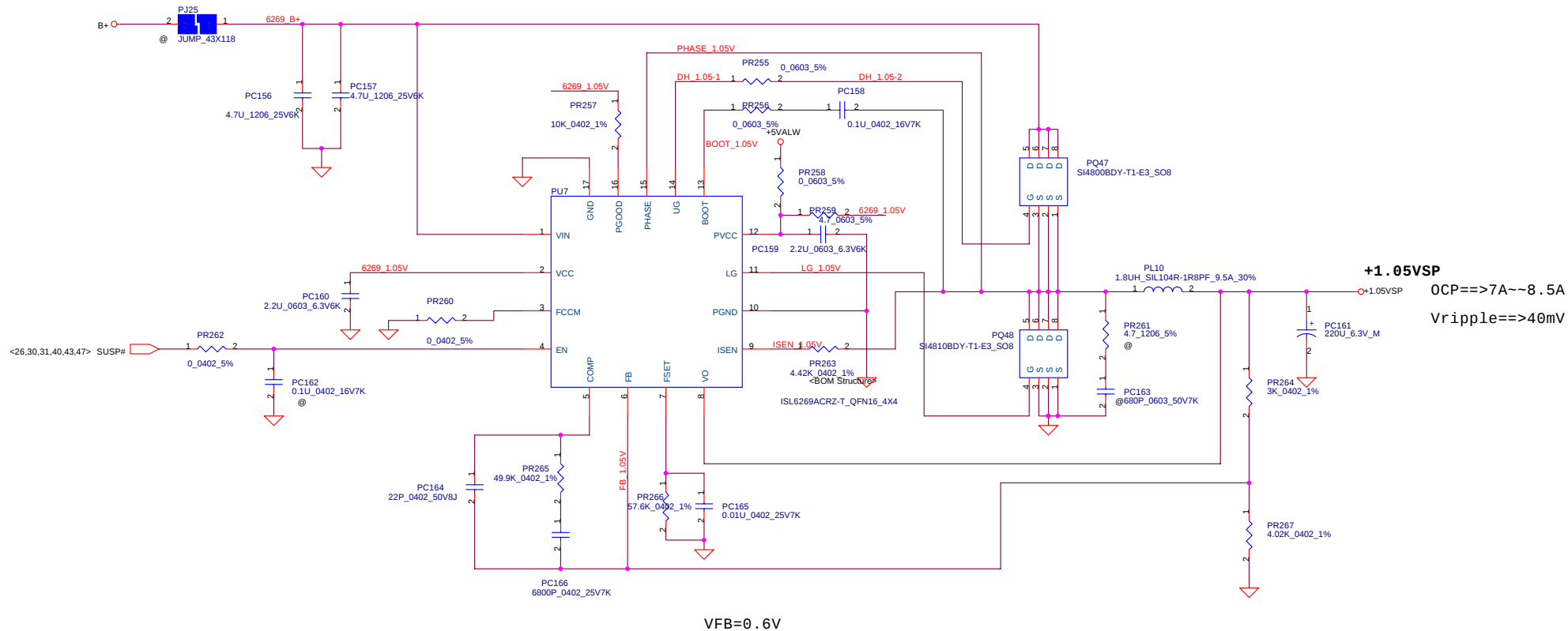
3.3VALWP Ipeak=6.6A~10A
Rds(on) = 20m ohm(max) ; Rds(on) = 16m ohm(typical)

5VALWP Ipeak=6.6A~10A
Rds(on) = 20m ohm(max) ; Rds(on) = 16m ohm(typical)

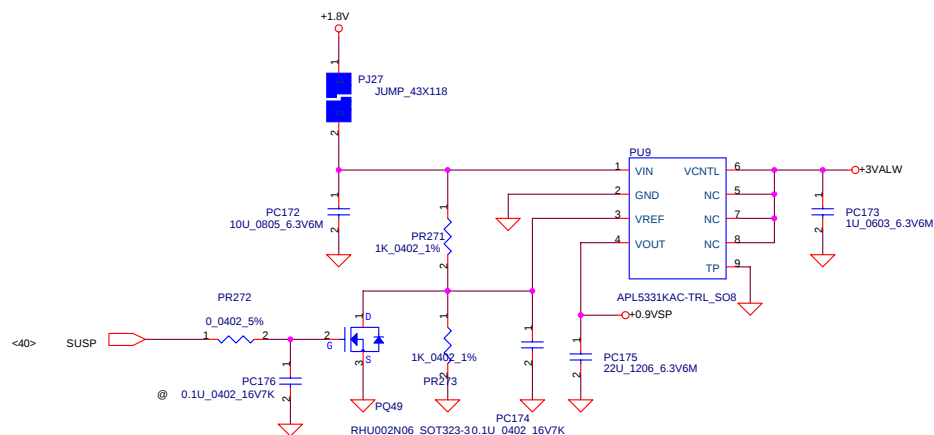
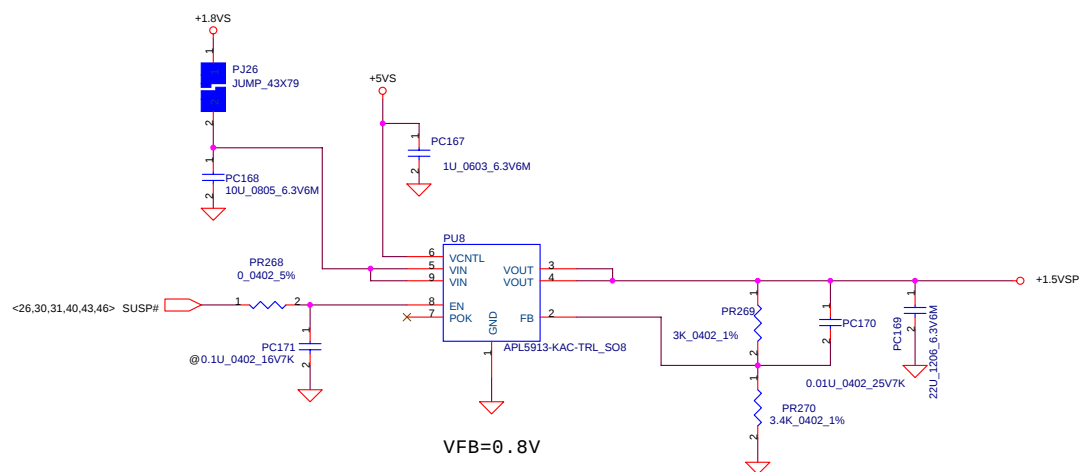
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Size		Document Number		Rev							
Custom								0.1			
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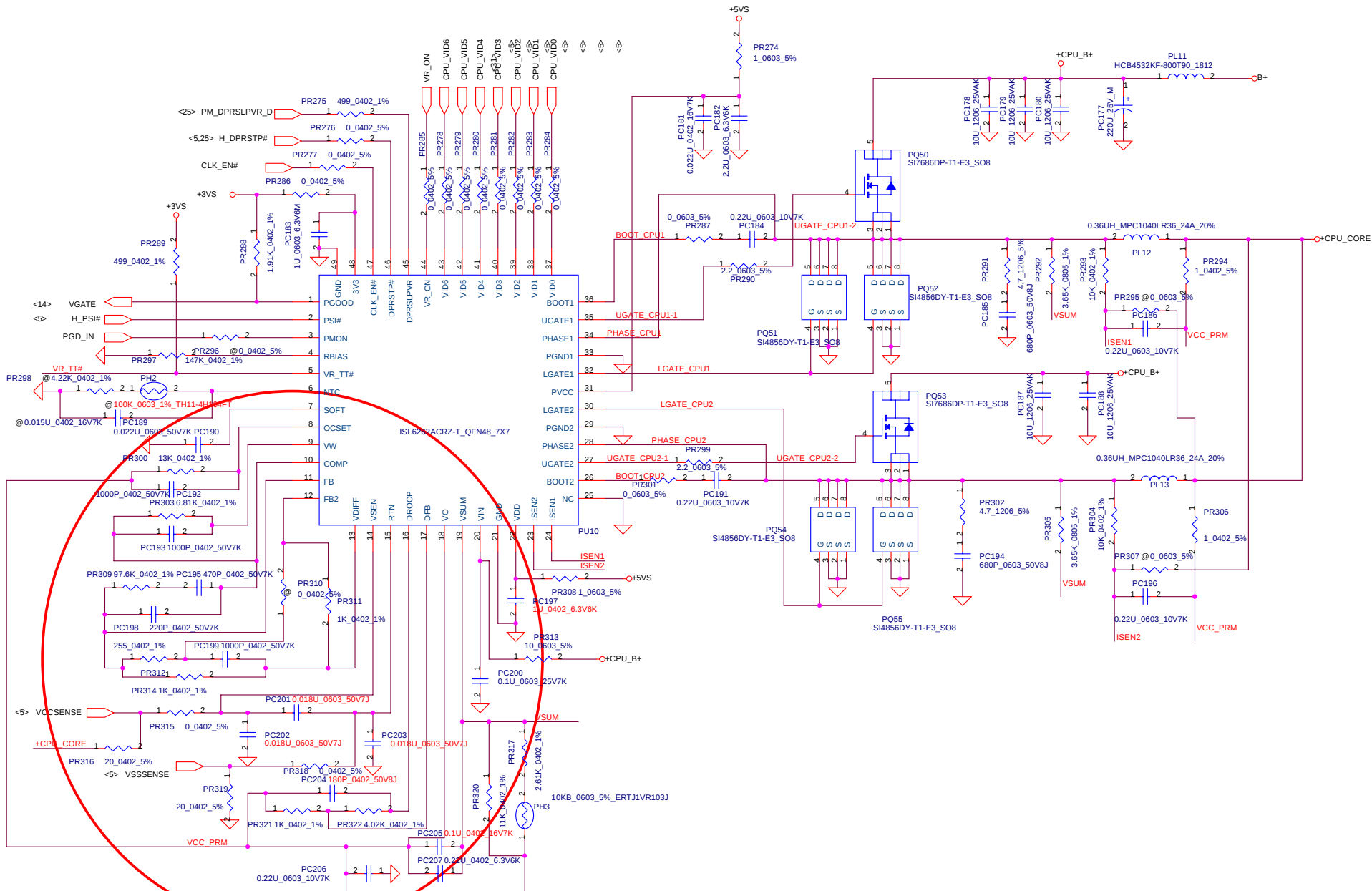


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