

Compal Confidential

Gx00/Gx00 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

AMD Mars XT / SUN Pro

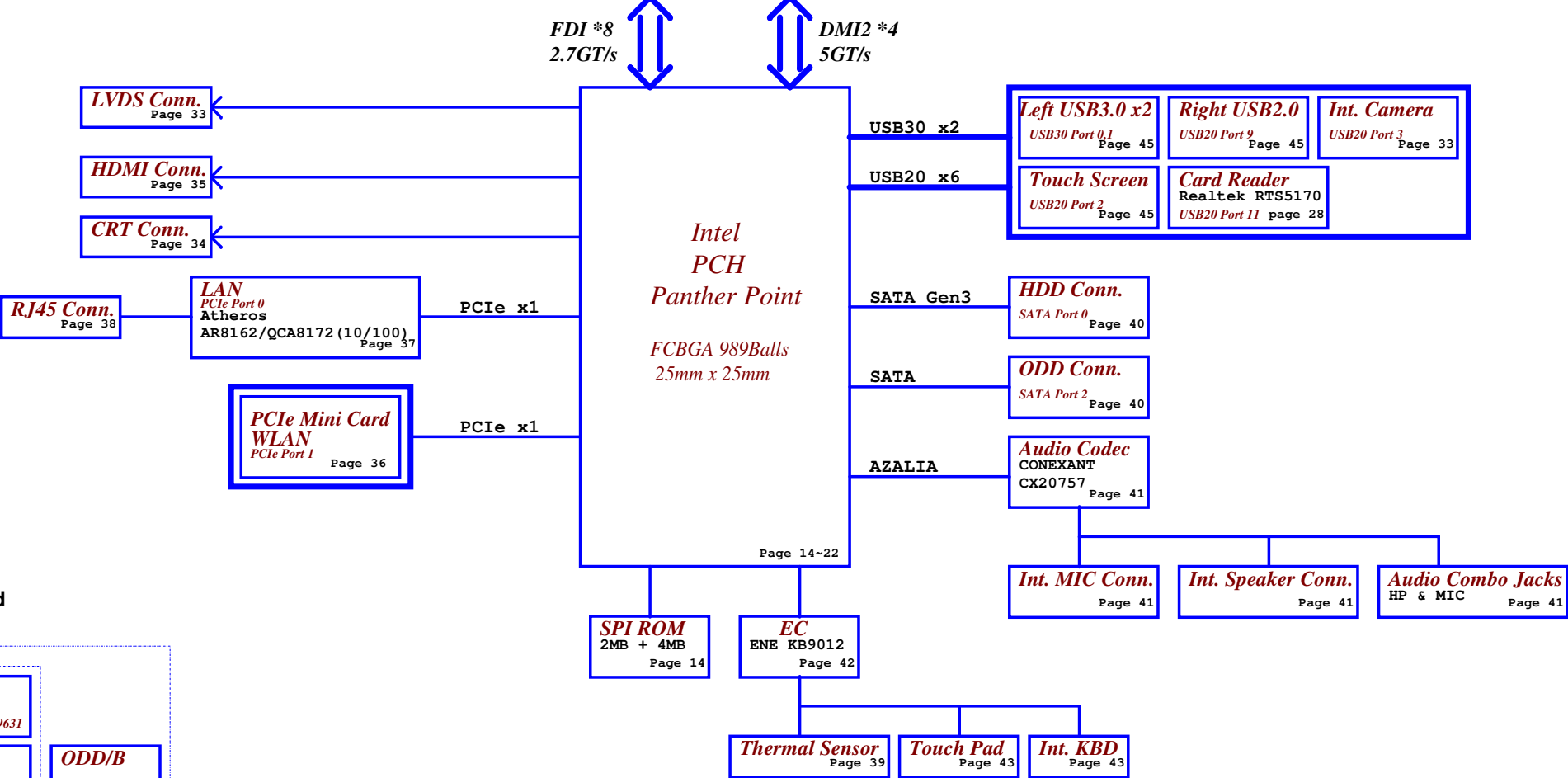
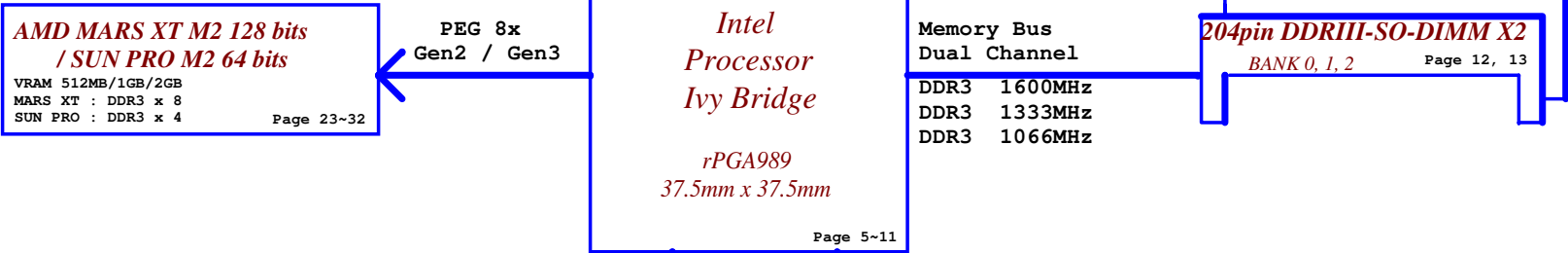
2013-02-27

LA-9631P

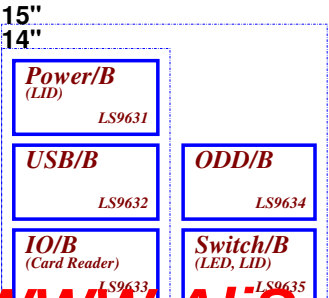
REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY CUSTOMER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9631P	Rev 1.0
				Date: Wednesday, February 27, 2013	Sheet 1 of 60	

Chief River



Sub-borad



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	MB Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9631P
				Date	Wednesday, February 27, 2013
				Sheet	2 of 60
				Rev	1.0

Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	×
S5 S4/AC		○	○	×	×
S5 S4/ Battery only		○	×	×	×
S5 S4/AC & Battery don't exist		×	×	×	×

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V
R694	100K +/- 1%

Board ID / SKU ID Table for AD channel

Board ID	R695	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD	
0	0	0 V	0 V	0 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
EHCI2		7	
	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76, HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011x	Thermal Sensor	0100 1100

EC SM Bus2 address

PCH SM Bus address

Device	Address	Device	Address
DDR_JDIMM1	1010 000x A0h	Internal thermal sensor	0100 0001 41h
DDR_JDIMM2	1010 010x A4h		

AMD-GPU SM Bus address

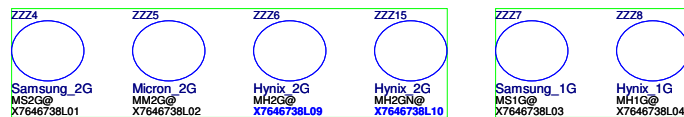
SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	×	√	×	×	×	×	×
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	×	×	×	×	×	×	×
SMB_EC_DA2	+3VS	+3VGS					+3VS	+3VALW
PCH_SMBCLK	PCH	×	×	×	√	√	×	×
PCH_SMBDATA	+3VALW				+3VS	+3VS		
PCH_SML0CLK	PCH	×	×	×	×	×	×	×
PCH_SML0DATA	+3VALW							
SML1CLK	PCH	×	×	×	×	×	×	×
SML1DATA	+3VALW	+3VGS		√			+3VS	

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Notes List
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-9631P	1.0
				Date	Wednesday, February 27, 2013
				Sheet	3 of 60

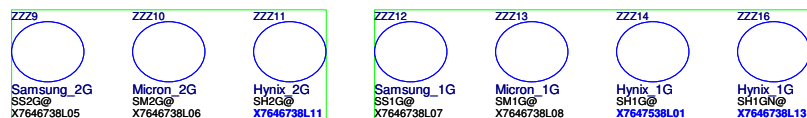
Mars XT VRAM STRAP

		X76@					X76@	
	Vendor	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd	
	UV9, UV8, UV7, UV8 UV9, UV10, UV11, UV12					RV20	RV27	
2GBytes	ZZZ4 MS2G@ Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	0	NC	4.75K	
2GBytes	ZZZ5 MM2G@ Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K	
2GBytes	ZZZ6 MH2G@ Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C	2	0	1	0	4.53K	2K	
1GBytes	ZZZ7 MS1G@ Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	3	0	1	1	6.98K	4.99K	
2GBytes	ZZZ15 MH2GN@ Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	4	1	0	0	4.53K	4.99K	
1GBytes	ZZZ8 MH1G@ Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	7	1	1	1	4.75K	NC	



Sun PRO VRAM STRAP

		X76@					X76@	
	Vendor	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd	
	UV9, UV10, UV11, UV12					RV20	RV27	
2GBytes	ZZZ9 SS2G@ Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	0	NC	4.75K	
2GBytes	ZZZ10 SM2G@ Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-107G:E	1	0	0	1	8.45K	2K	
2GBytes	ZZZ11 SH2G@ Hynix 4096Mbits SA00006DG00 256Mx16 H5TQ4G63MFR-11C	2	0	1	0	4.53K	2K	
1GBytes	ZZZ12 SS1G@ Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	3	0	1	1	6.98K	4.99K	
1GBytes	ZZZ16 SH1GN@ Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	4	1	0	0	4.53K	4.99K	
1GBytes	ZZZ13 SM1G@ Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	6	1	1	0	3.4K	10K	
1GBytes	ZZZ14 SH1G@ Hynix 2048Mbits SA000065300 128M16 H5TQ2G63DFR-N0C	7	1	1	1	4.75K	NC	



Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(3.3VGS)

PCIE_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

PERSTb

REFCLK

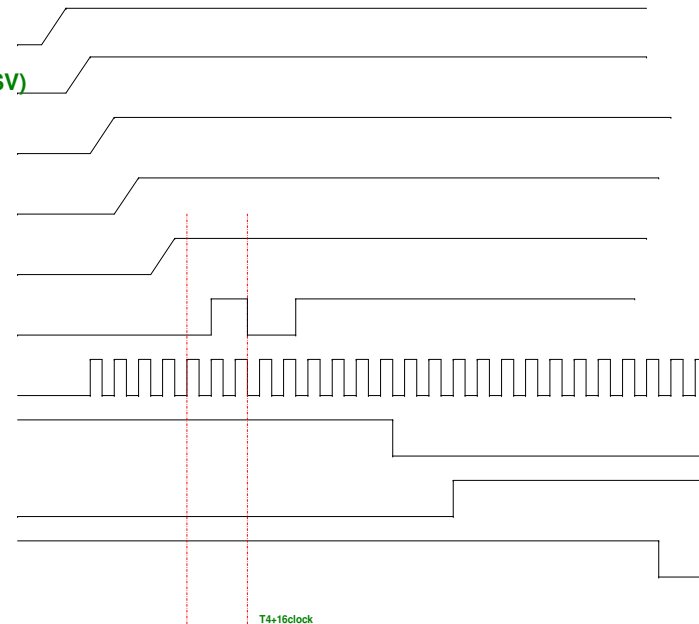
Straps Reset

Straps Valid

Global ASIC Reset

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-9631P	1.0
				Date	Wednesday, February 27, 2013
				Sheet	4 of 60



14" DIS PCB_LA9631P
DA6000WO000
PCB 0N1 LA-9631P REV0 M/B DIS 3



15" DIS PCB_LA9631P
DA6000WO100
PCB 0N2 LA-9631P REV0 M/B DIS 5

PEG_ICOMPI and RCOMPO signals should be
shorted and routed
with - max length = 500 mils - typical
impedance = 43 mohms
PEG_ICOMPO signals should be routed with -
max length = 500 mils
- typical impedance = 14.5 mohms

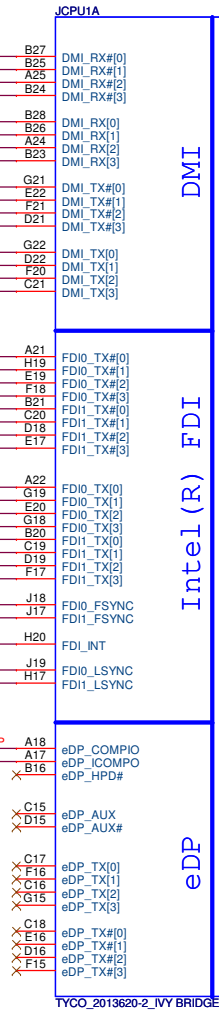
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	---

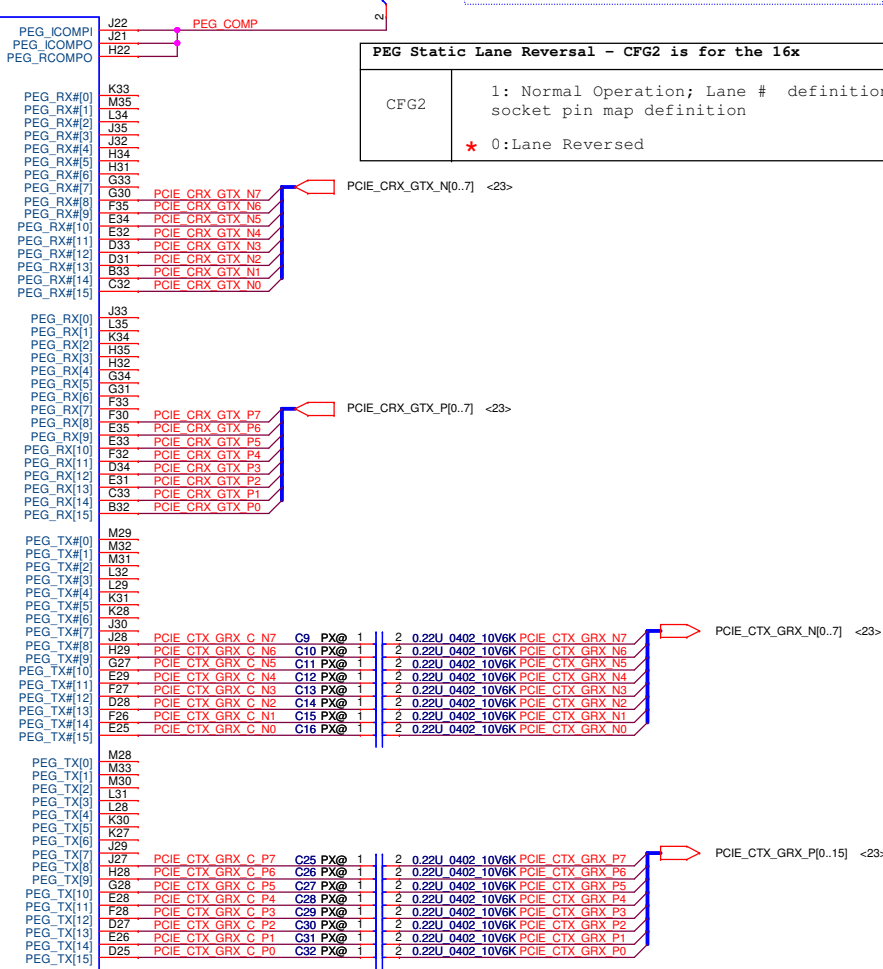
eDP_COMPIO and ICOMPO signals
should be shorted near balls
and routed with typical
impedance <25 mohms

+V1.05S_VCCP
24.9_0402_1%

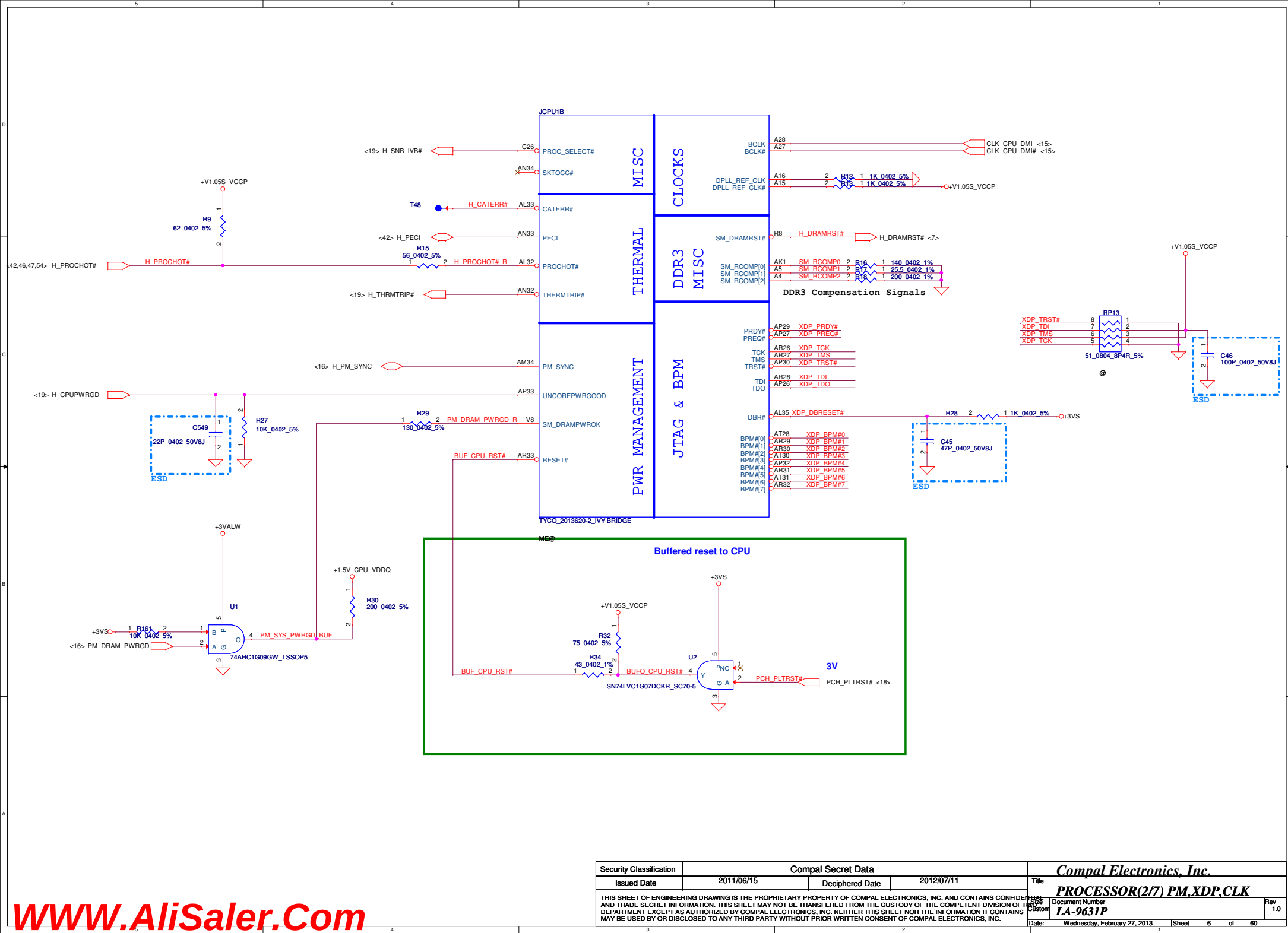
EDP_COMP
eDP_HPD



PCI EXPRESS* - GRAPHICS



Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2011/06/15		Deciphered Date		2012/07/11		Title					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								PROCESSOR(1/7) DMI,FDI,PEG					
								Size		Document Number		Rev	
								Custom		LA-9631P		1.0	
Date:								Wednesday, February 27, 2013		Sheet 5 of 60			



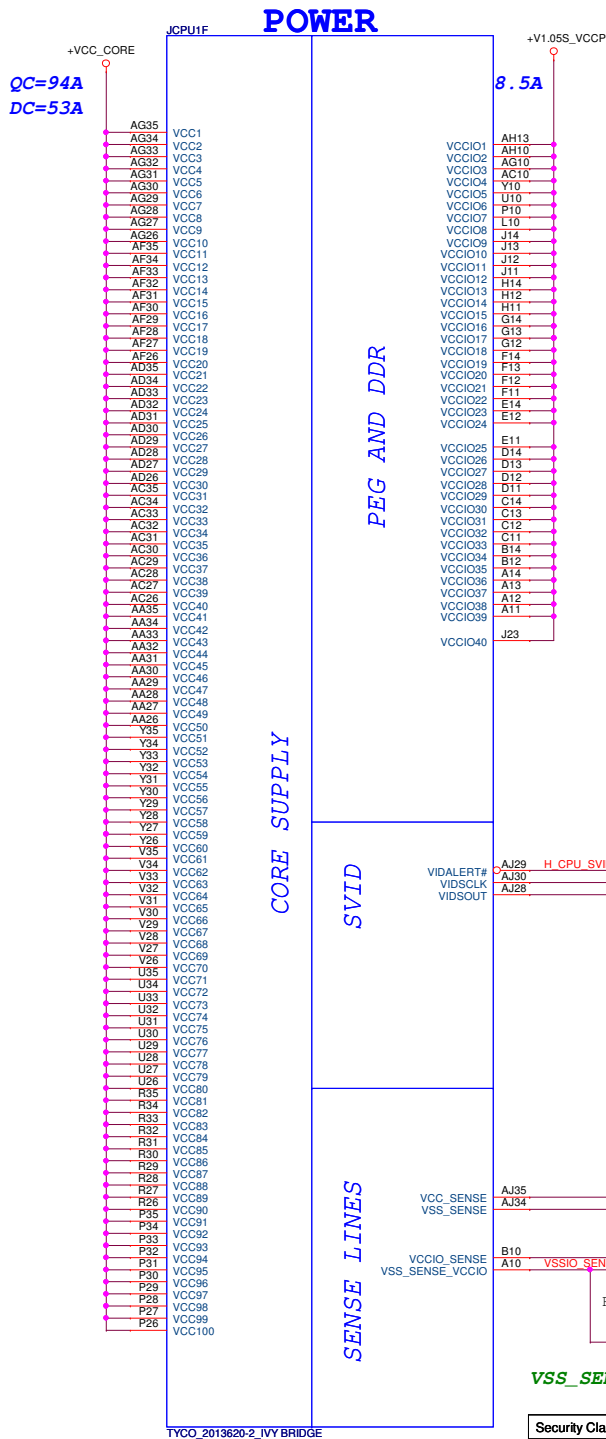
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed

CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	---

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled
----------	---

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---





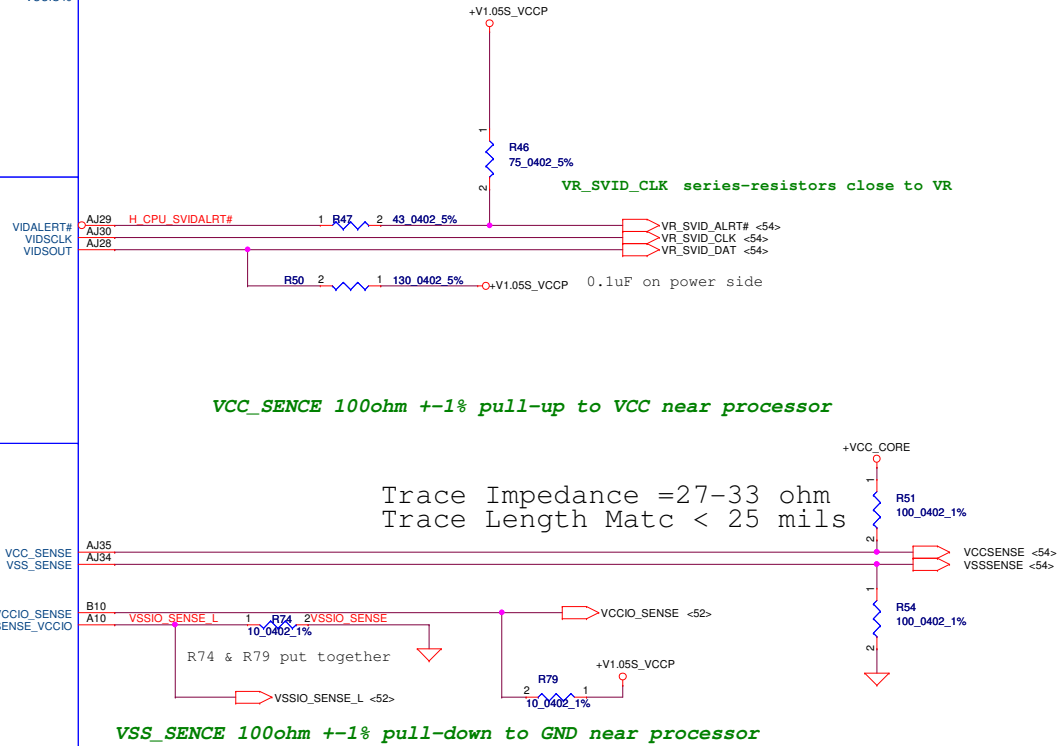
POWER

PEG AND DDR

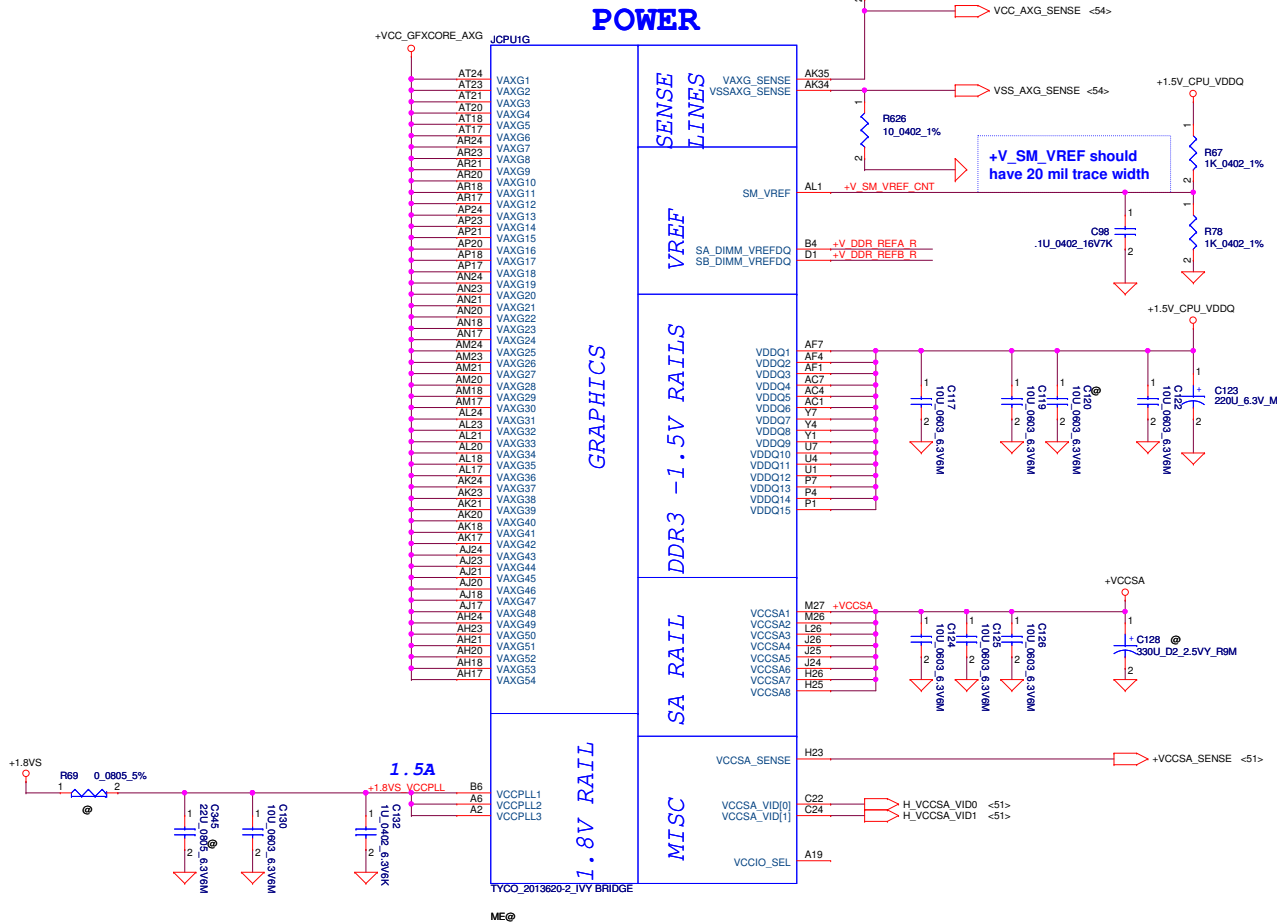
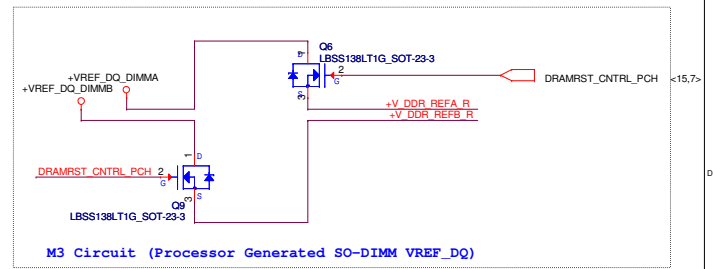
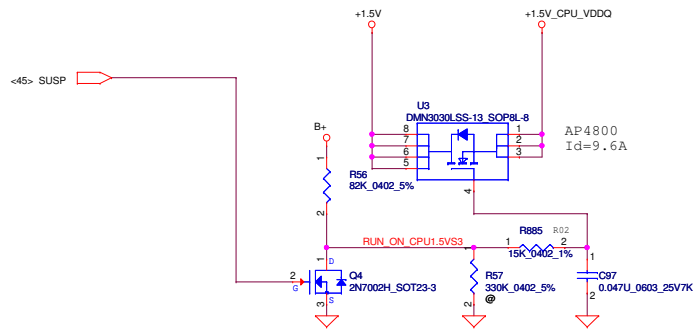
CORE SUPPLY

SVID

SENSE LINES

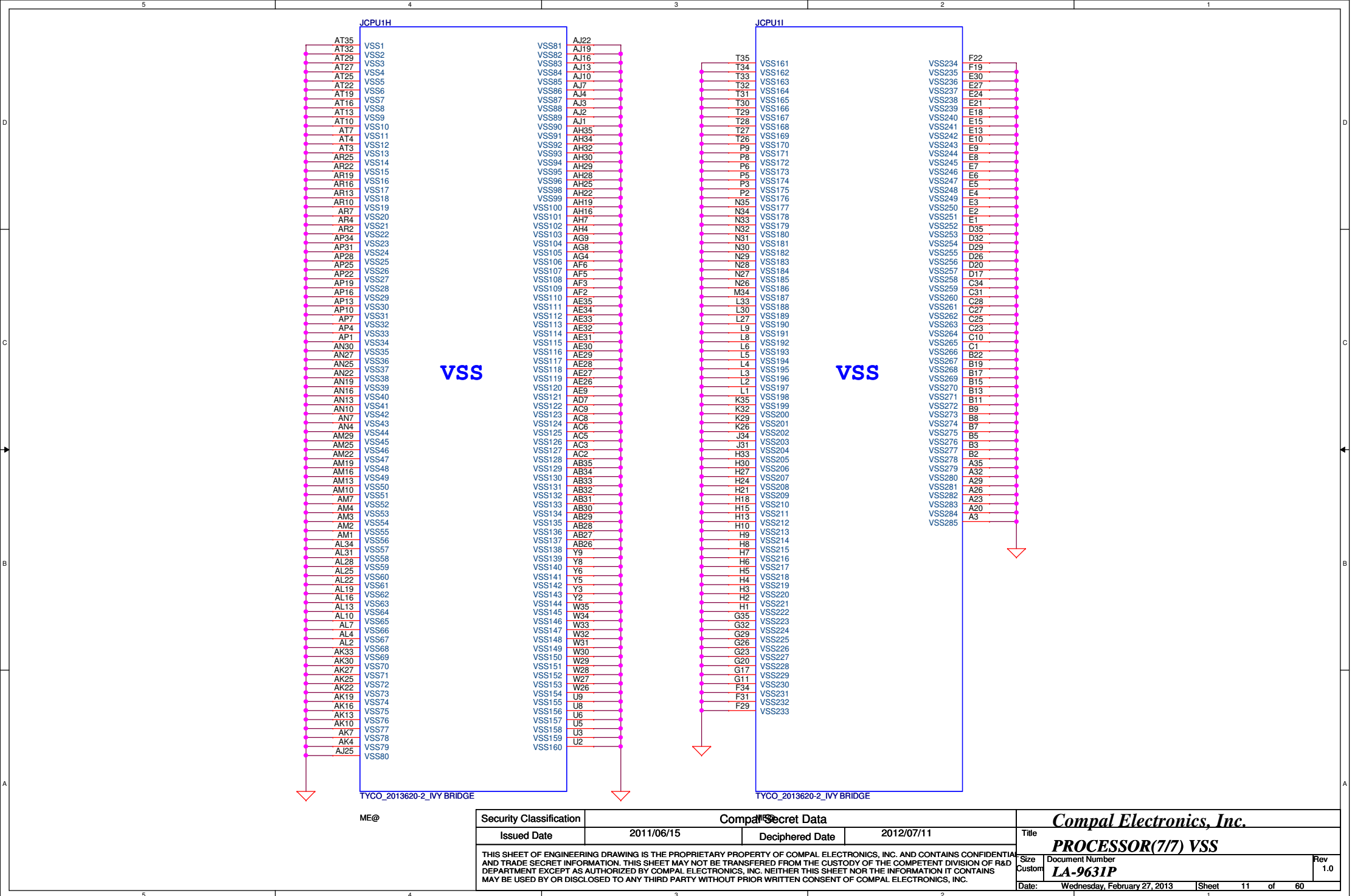


Security Classification			Compal Secret Data			Title		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Rev	1.0	PROCESSOR(5/7) PWR,BYPASS		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Document Number	LA-9631P	Rev 1.0
						Date	Wednesday, February 27, 2013	Sheet 9 of 60

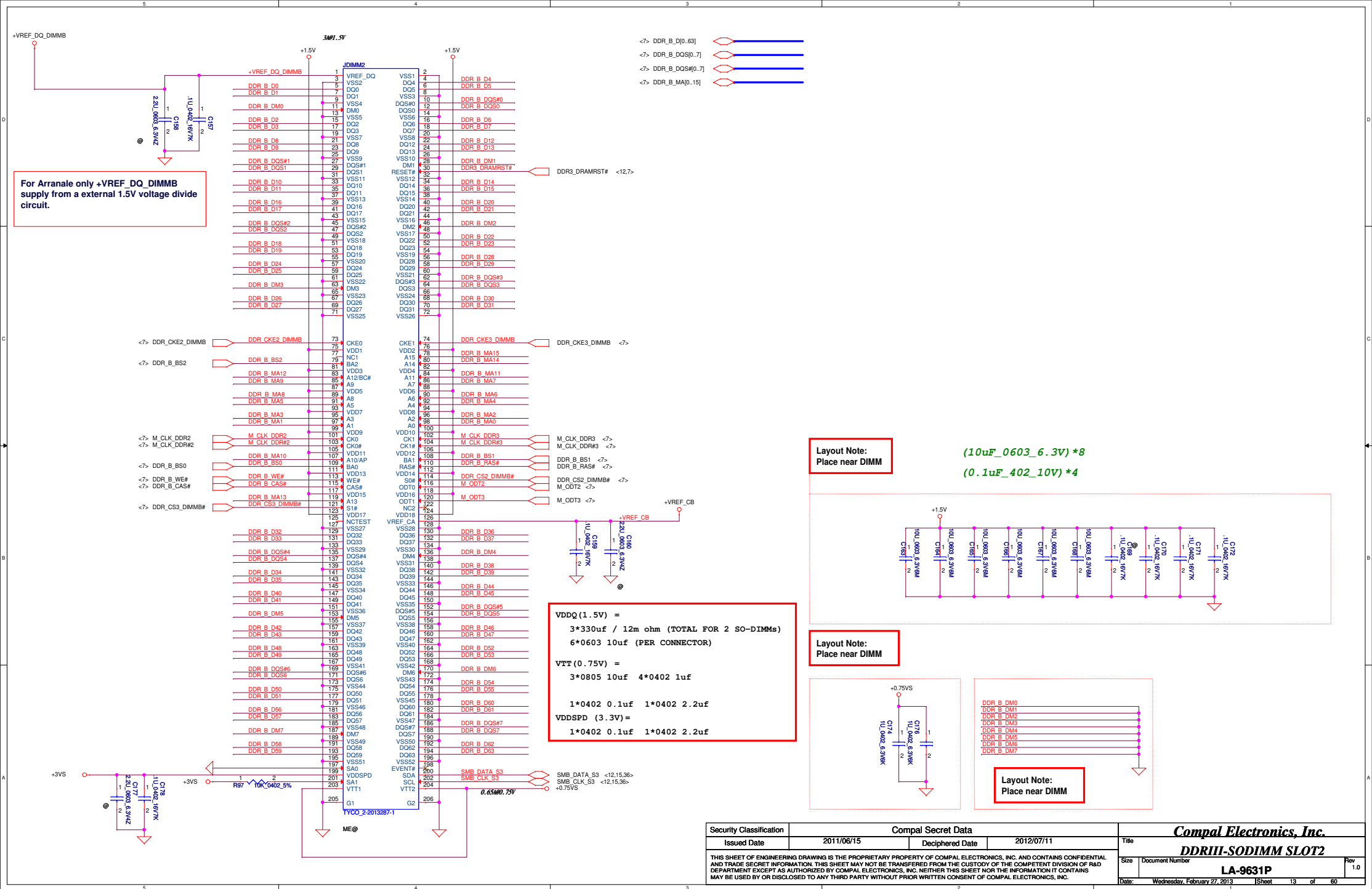


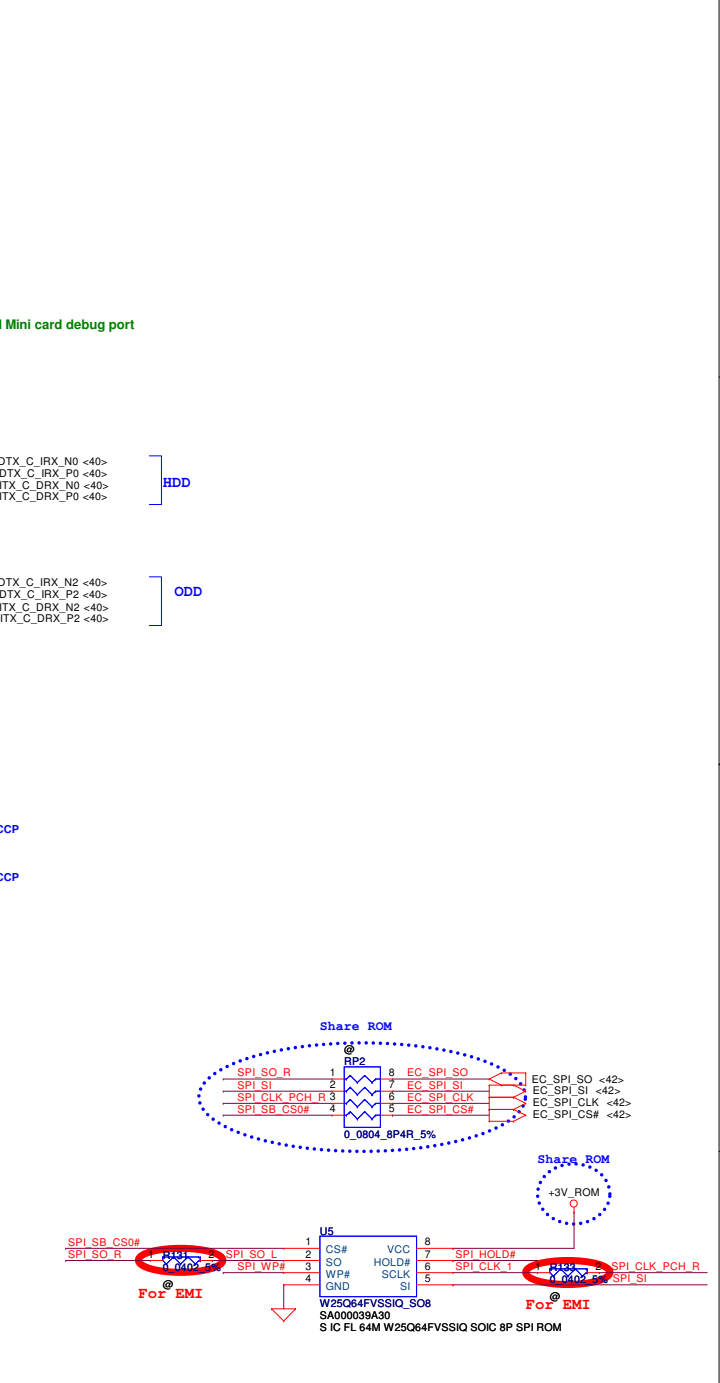
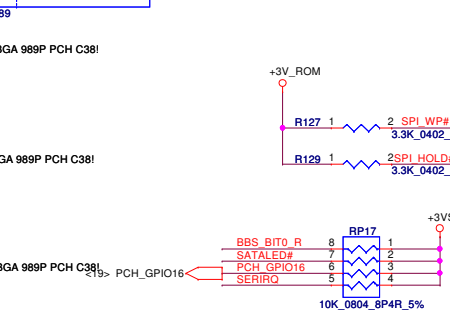
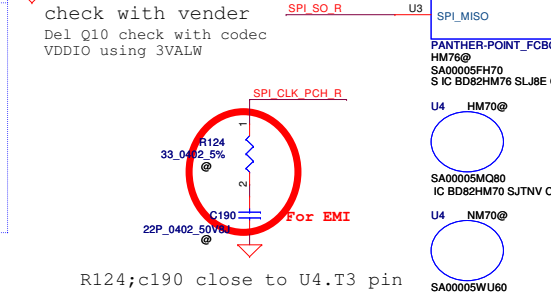
IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0
Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

Security Classification	Compal Secret Data			Title
Issued Date	2011/06/15	Deciphered Date	2012/07/11	PROCESSOR(6/7) PWR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 1.0
Date: Wednesday, February 27, 2013				Sheet 10 of 60

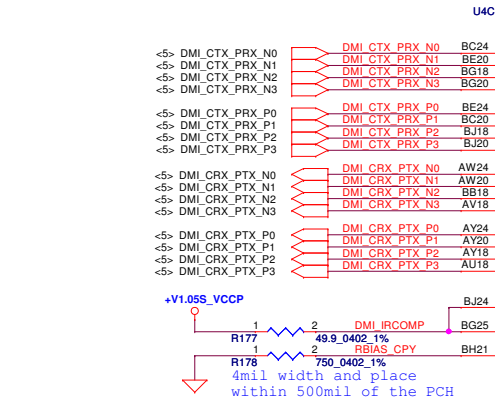
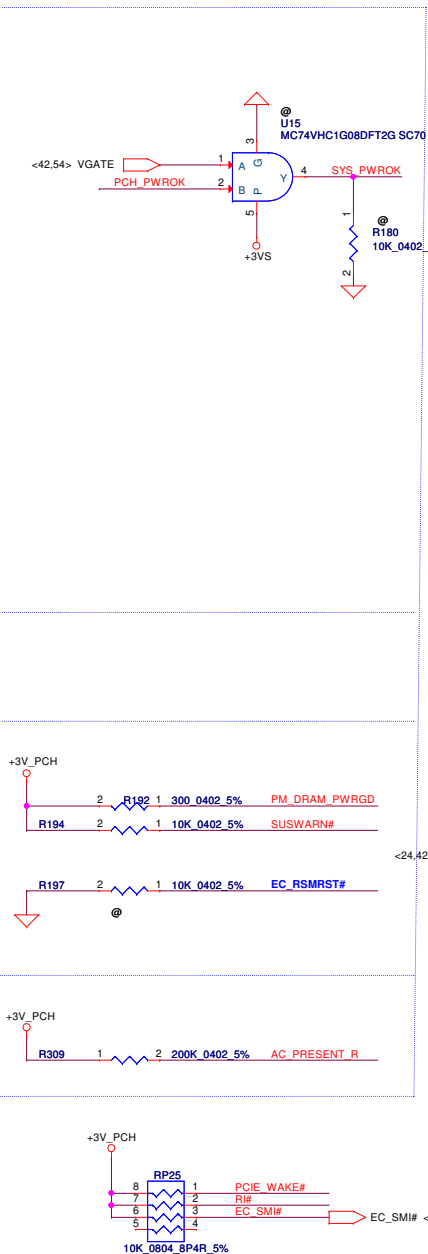




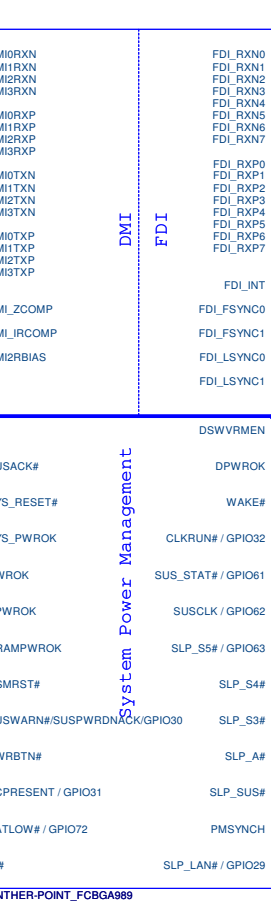
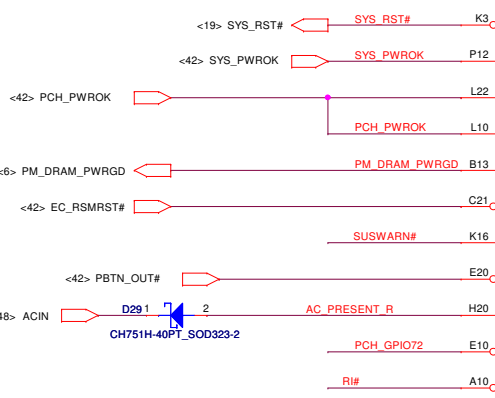




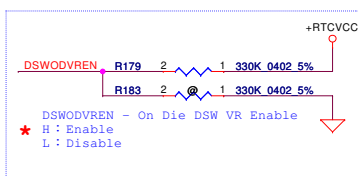
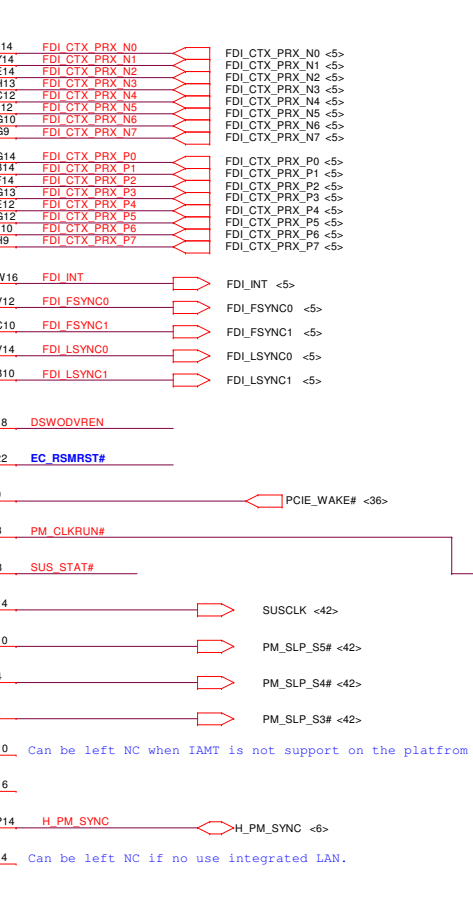
Security Classification		Compal Secret Data		Compal Electronics, Inc. PCH (I/O) SATA, HDA, SPI, LPC, XDP	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Rev 1.0
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-9631P	Rev 1.0
				Date: Wednesday, March 06, 2013	Sheet 14 of 60

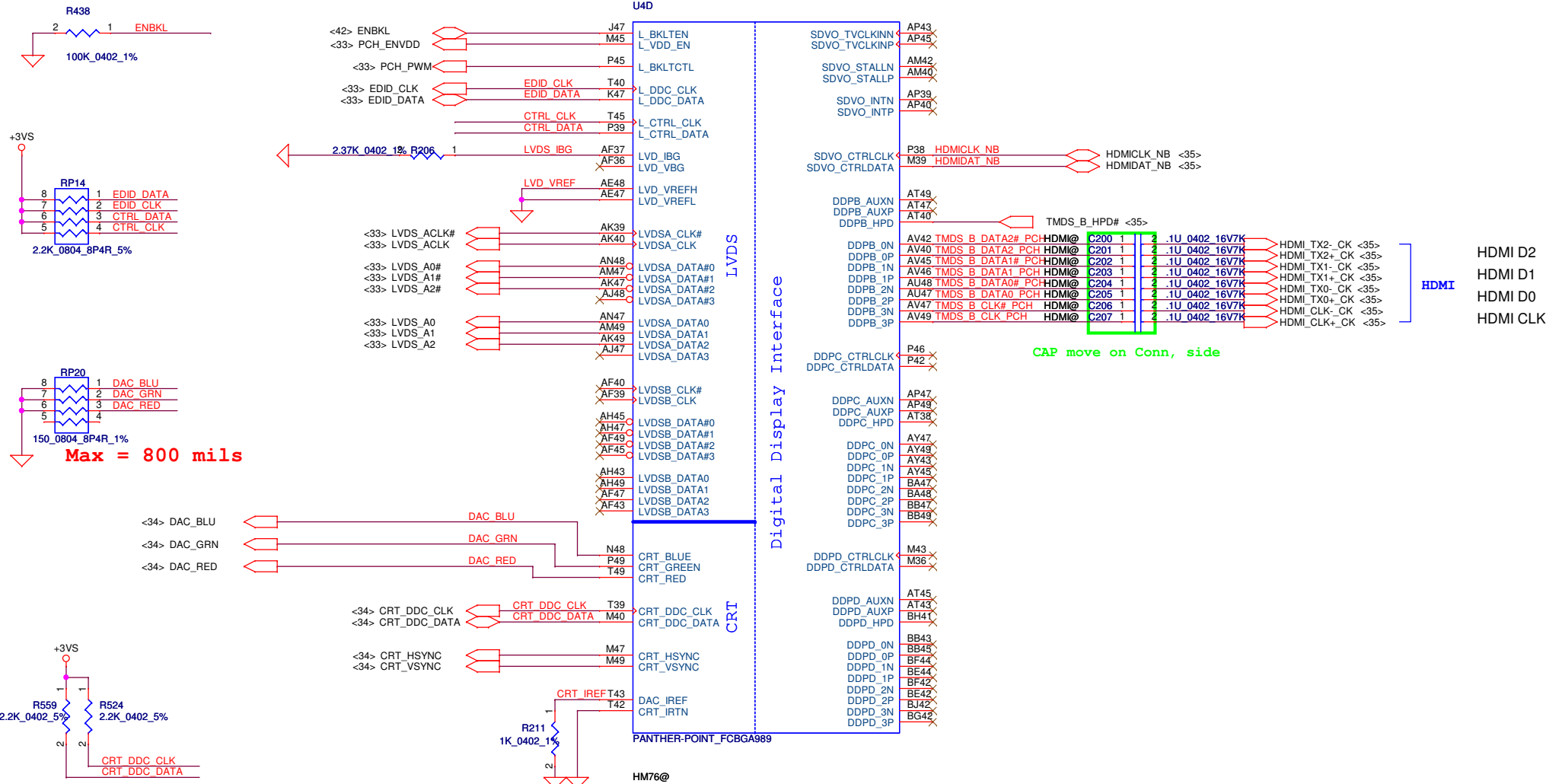


SUSACK# is only used on platform that support the Deep Sx state.



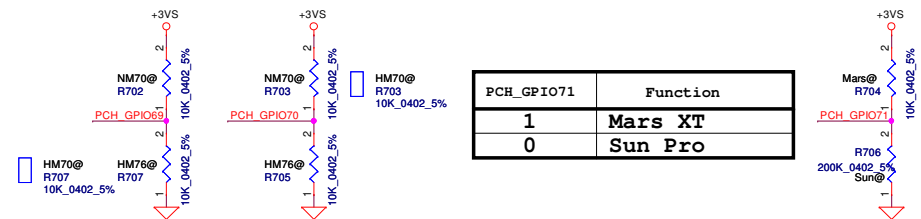
HM76@



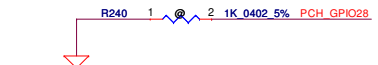


Security Classification		Compal Secret Data									
Issued Date		2011/06/15		Deciphered Date		2012/07/11		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								PCH (4/9) LVDS,CRT,DP,HDMI			
								Document Number		Rev	
								LA-9631P		1.0	
								Date:		Wednesday, February 27, 2013	
								Sheet		17 of 60	

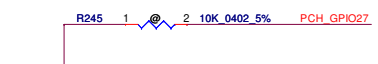
PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76



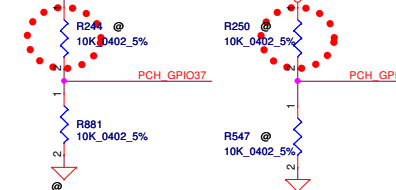
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



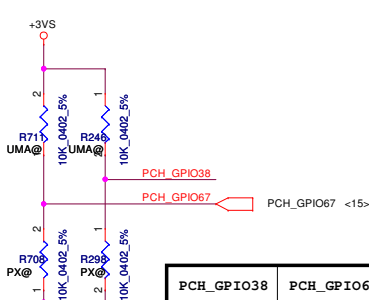
★ PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



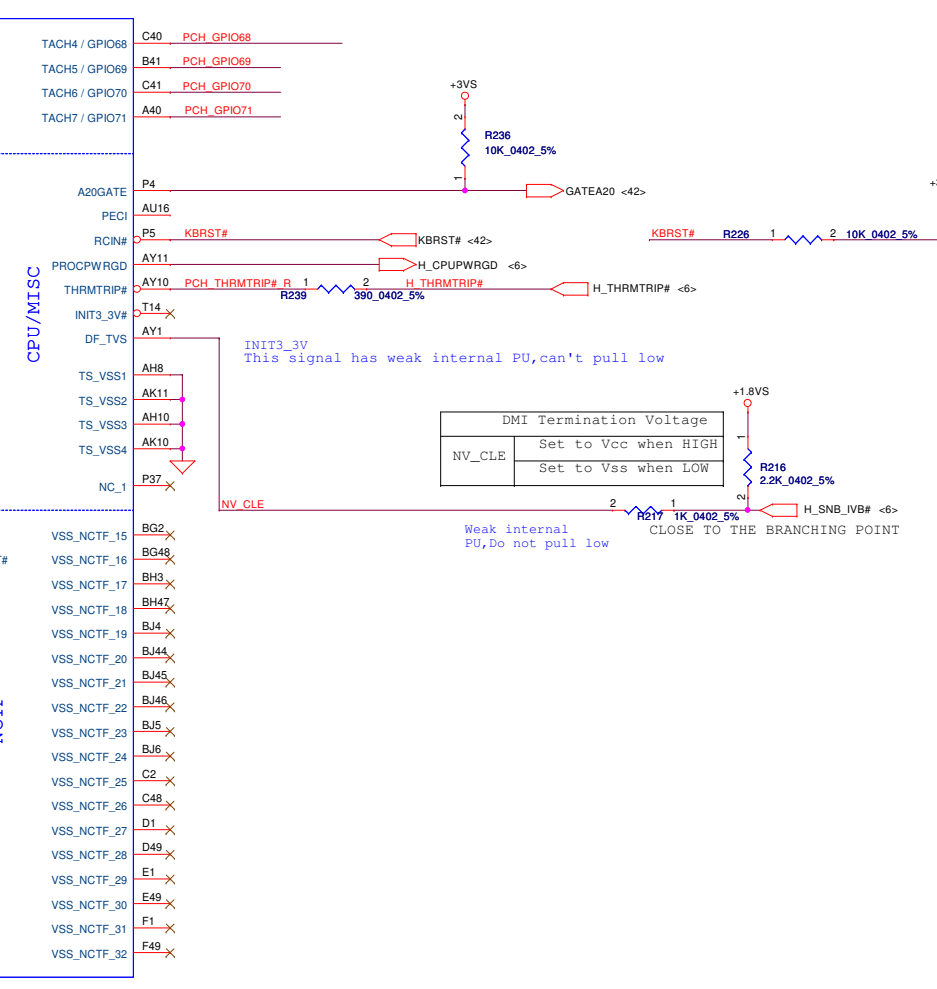
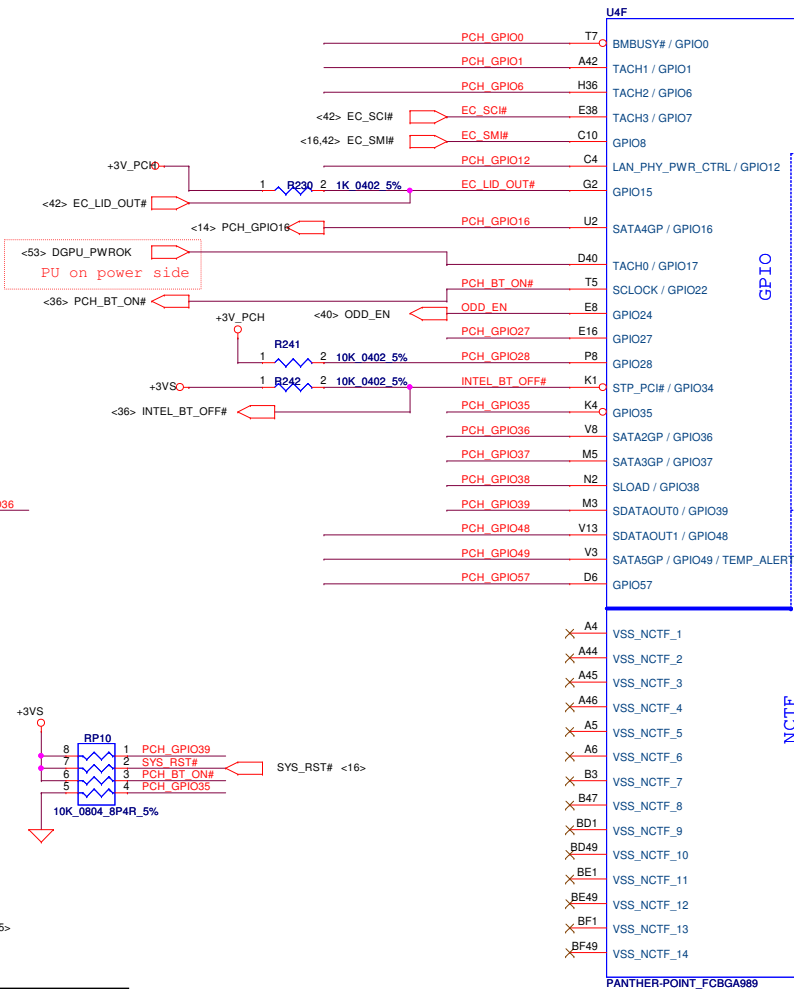
GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.



BIOS Request SKU ID

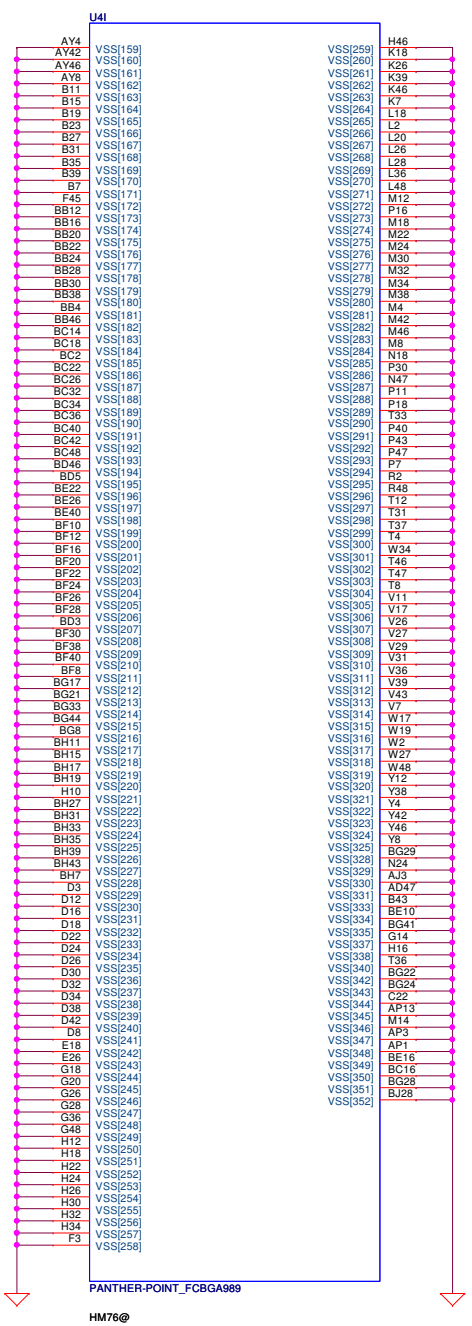
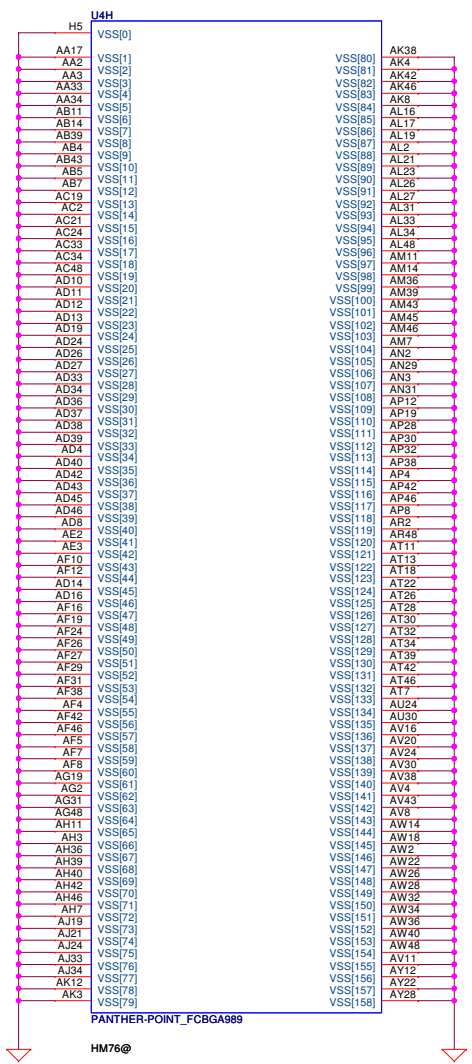


PCH_GPIO38	PCH_GPIO67	Function
0	0	SG(Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA



Security Classification	Compal Secret Data			Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Custom	LA-9631P
Date: Wednesday, February 27, 2013				Sheet	19 of 60

Compal Electronics, Inc.



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2011/06/15		Deciphered Date		2012/07/11		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								PCH (9/9) VSS			
								Document Number		Rev	
								LA-9631P		1.0	
								Date: Wednesday, February 27, 2013		Sheet 22 of 60	

<5> PCIE_CTX_GRX_P[7..0] PCIE_CTX_GRX_P[7..0]
<5> PCIE_CTX_GRX_N[7..0] PCIE_CTX_GRX_N[7..0]

UV1A

PART 1 OF 9

PCIE_CRX_GTX_P[7..0] PCIE_CRX_GTX_P[7..0] <5>
PCIE_CRX_GTX_N[7..0] PCIE_CRX_GTX_N[7..0] <5>

PCIE_CTX_GRX_P0 AA38 PCIE_RX0P
PCIE_CTX_GRX_N0 Y37 PCIE_RX0N
PCIE_CTX_GRX_P1 Y35 PCIE_RX1P
PCIE_CTX_GRX_N1 W36 PCIE_RX1N
PCIE_CTX_GRX_P2 W38 PCIE_RX2P
PCIE_CTX_GRX_N2 V37 PCIE_RX2N
PCIE_CTX_GRX_P3 V35 PCIE_RX3P
PCIE_CTX_GRX_N3 U36 PCIE_RX3N
PCIE_CTX_GRX_P4 U38 PCIE_RX4P
PCIE_CTX_GRX_N4 T37 PCIE_RX4N
PCIE_CTX_GRX_P5 T35 PCIE_RX5P
PCIE_CTX_GRX_N5 R36 PCIE_RX5N
PCIE_CTX_GRX_P6 R38 PCIE_RX6P
PCIE_CTX_GRX_N6 P37 PCIE_RX6N
PCIE_CTX_GRX_P7 P35 PCIE_RX7P
PCIE_CTX_GRX_N7 N36 PCIE_RX7N

PCI EXPRESS INTERFACE

PCIE_TX0P Y33 PCIE_CRX_C GTX_P0 0.22U 0402 10V6K 1 2 CV1 PX@ PCIE_CRX_GTX_P0
PCIE_TX0N Y32 PCIE_CRX_C GTX_N0 0.22U 0402 10V6K 1 2 CV2 PX@ PCIE_CRX_GTX_N0
PCIE_TX1P W33 PCIE_CRX_C GTX_P1 0.22U 0402 10V6K 1 2 CV3 PX@ PCIE_CRX_GTX_P1
PCIE_TX1N W32 PCIE_CRX_C GTX_N1 0.22U 0402 10V6K 1 2 CV4 PX@ PCIE_CRX_GTX_N1
PCIE_TX2P U33 PCIE_CRX_C GTX_P2 0.22U 0402 10V6K 1 2 CV5 PX@ PCIE_CRX_GTX_P2
PCIE_TX2N U32 PCIE_CRX_C GTX_N2 0.22U 0402 10V6K 1 2 CV6 PX@ PCIE_CRX_GTX_N2
PCIE_TX3P U30 PCIE_CRX_C GTX_P3 0.22U 0402 10V6K 1 2 CV7 PX@ PCIE_CRX_GTX_P3
PCIE_TX3N U29 PCIE_CRX_C GTX_N3 0.22U 0402 10V6K 1 2 CV8 PX@ PCIE_CRX_GTX_N3
PCIE_TX4P T33 PCIE_CRX_C GTX_P4 0.22U 0402 10V6K 1 2 CV9 PX@ PCIE_CRX_GTX_P4
PCIE_TX4N T32 PCIE_CRX_C GTX_N4 0.22U 0402 10V6K 1 2 CV10 PX@ PCIE_CRX_GTX_N4
PCIE_TX5P T30 PCIE_CRX_C GTX_P5 0.22U 0402 10V6K 1 2 CV11 PX@ PCIE_CRX_GTX_P5
PCIE_TX5N T29 PCIE_CRX_C GTX_N5 0.22U 0402 10V6K 1 2 CV12 PX@ PCIE_CRX_GTX_N5
PCIE_TX6P P33 PCIE_CRX_C GTX_P6 0.22U 0402 10V6K 1 2 CV13 PX@ PCIE_CRX_GTX_P6
PCIE_TX6N P32 PCIE_CRX_C GTX_N6 0.22U 0402 10V6K 1 2 CV14 PX@ PCIE_CRX_GTX_N6
PCIE_TX7P P30 PCIE_CRX_C GTX_P7 0.22U 0402 10V6K 1 2 CV15 PX@ PCIE_CRX_GTX_P7
PCIE_TX7N P29 PCIE_CRX_C GTX_N7 0.22U 0402 10V6K 1 2 CV16 PX@ PCIE_CRX_GTX_N7

N33
N32
N30
N29
L33
L32
L30
L29
K33
K32
J33
J32
K30
K29
H33
H32

CLOCK

<15> CLK_PCIE_VGA# CLK_PCIE_VGA# AB35 PCIE_REFCLKP
<15> CLK_PCIE_VGA# CLK_PCIE_VGA# AA36 PCIE_REFCLKN

RV2 2 PX@ 1 AH16
1K_0402_5% TEST_PG
GPU_RST# AA30 PERSTB

Mars@ MARS XT M2 FCBGA 962
SA0000081J60
S IC 216-0842000 A0 MARS XT M2 BGA C38!

UV1 Sun@

SUN PRO M2 C38
SA000008BA20
S IC 216-0841000 A0 SUN PRO M2 BGA C38!

CALIBRATION

PCIE_CALR_TX Y30 RV1 1 PX@ 2 1.69K 0402 1% +0.95VGS
PCIE_CALR_RX Y29 RV3 1 PX@ 2 1K 0402 1% +0.95VGS

LVDS Interface

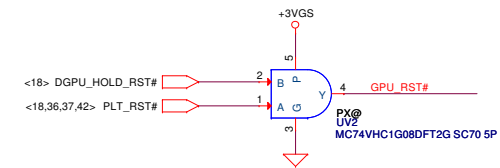
UV1D

PART 7 OF 9

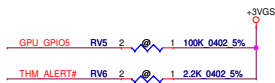
LVDS CONTROL

RSVD/VARY_BL AK27
RSVD/DIGON AJ27
TXCBP_DPB3P AK35
TXCBM_DPB3N AL36
TX3P_DPB2P AJ38
TX3M_DPB2N AK37
TX4P_DPB1P AH35
TX4M_DPB1N AJ36
TX5P_DPB0P AG38
TX5M_DPB0N AH37
NC#AF35 AF35
NC#AG36 AG36
TXCAP_DPA3P AP34
TXCAM_DPA3N AR34
TX0P_DPA2P AW37
TX0M_DPA2N AU35
TX1P_DPA1P AR37
TX1M_DPA1N AU39
TX2P_DPA0P AP35
TX2M_DPA0N AR35
NC AN36
NC AP37

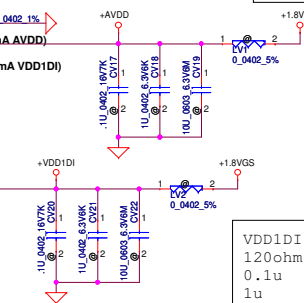
Mars@ MARS XT M2 FCBGA 962



Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/06/15		Deciphered Date		2012/07/11		Title	
								AT1 MarsXTX M2 PCIE/LVDS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Document Number	Rev
								LA-9631P	1.0
Date: Wednesday, March 06, 2013								Sheet	23 of 60



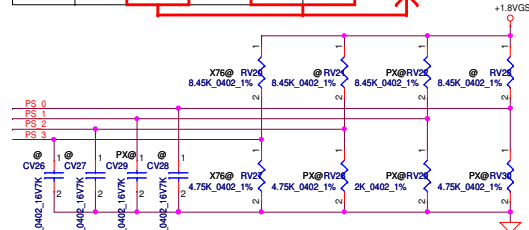
AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	11	000	NC	NC	4.75K
PS_1[5:1]	01	001	82nF	8.45K	2K
PS_2[5:1]	11	000	NC	NC	4.75K
PS_3[5:1]	11	XXXX	NC	X	X



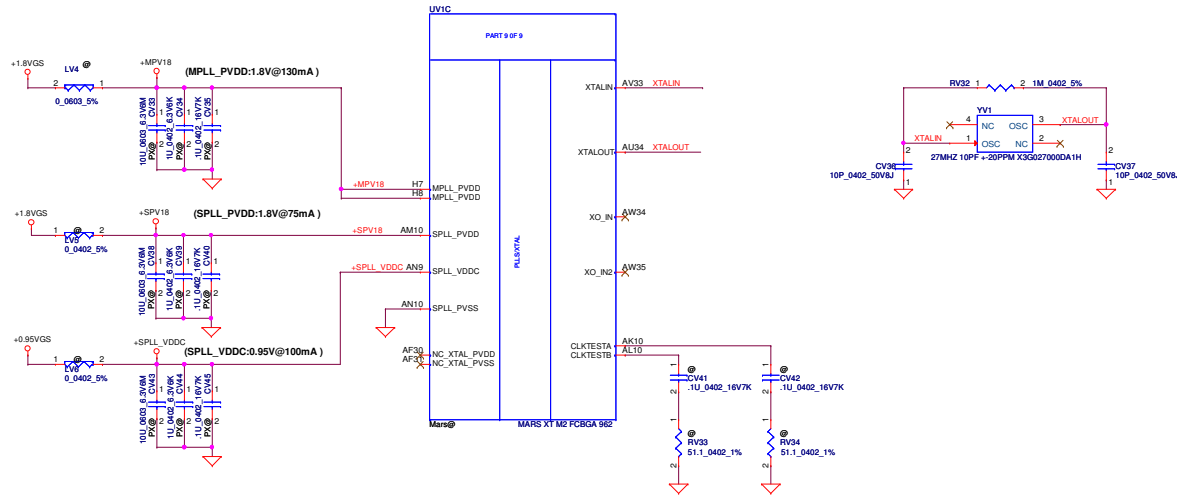
Place CLOSE VGA CHIP

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	ATI MarsXTX M2 Main MSIC
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size C	Document Number
					LA-9631P
				Date:	Wednesday, February 27, 2013
				Sheet	24 of 60

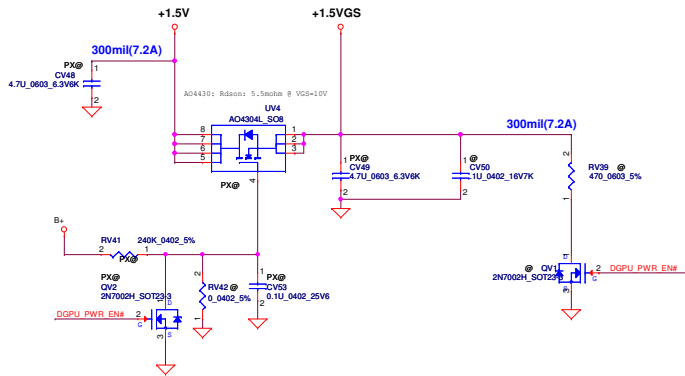
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

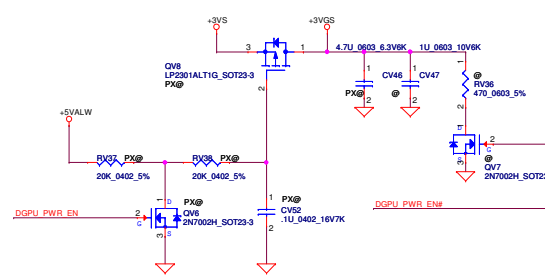
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



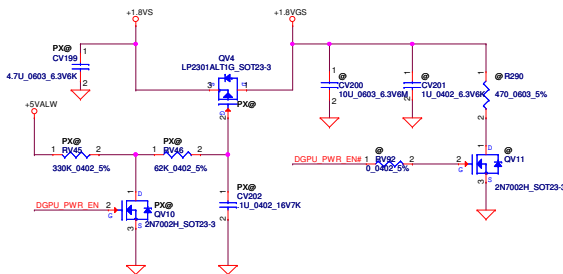
+1.5V to +1.5VGS



+3VS to +3VGS

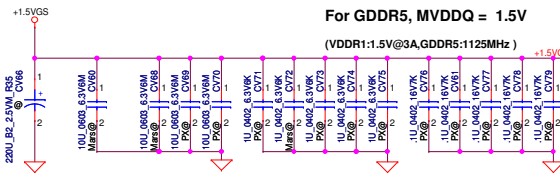


+1.8VS to +1.8VGS



Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date
2012/07/11		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		
Title	ATI MarsXTX M2 BACO POWER	Rev
Sheet	LA-9631P	1.0
Date	Wednesday, February 27, 2013	Sheet
28	d	80



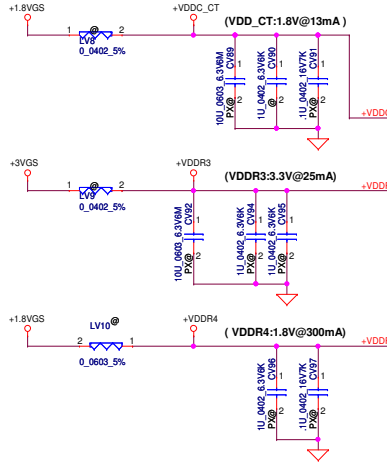


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

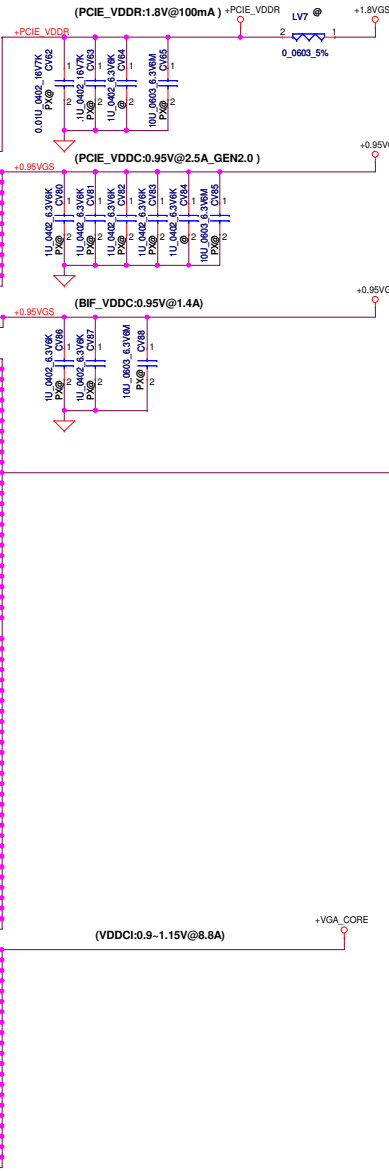
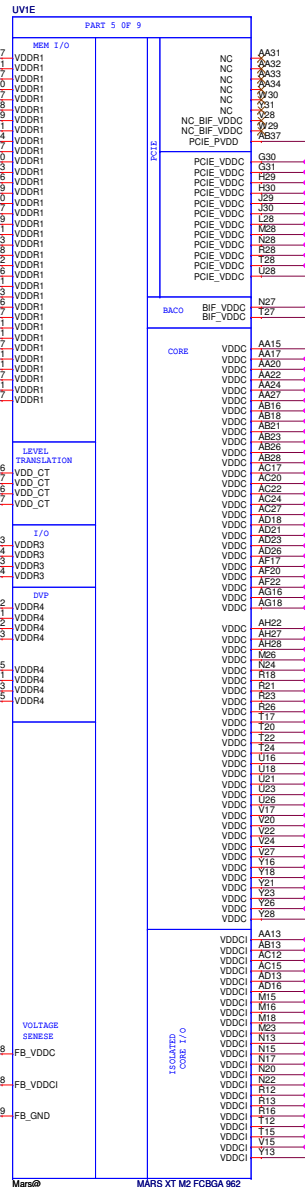
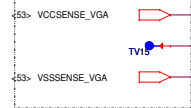
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



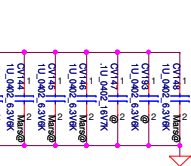
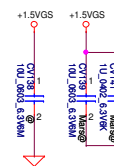
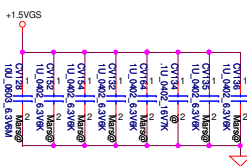
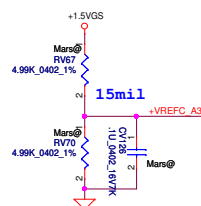
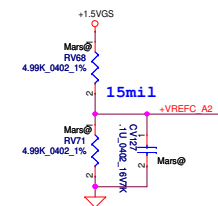
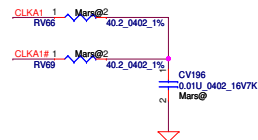
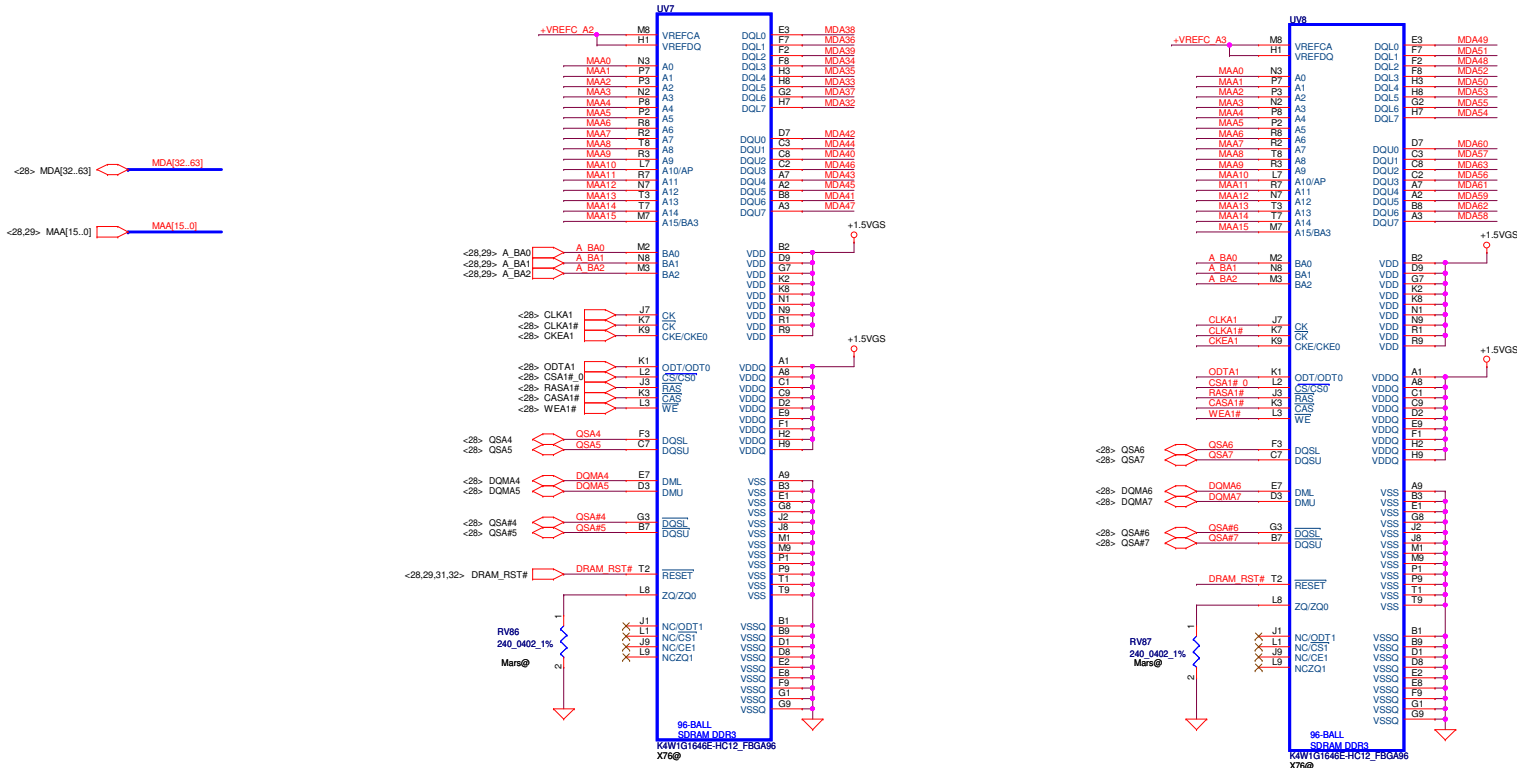
Route as differential pair



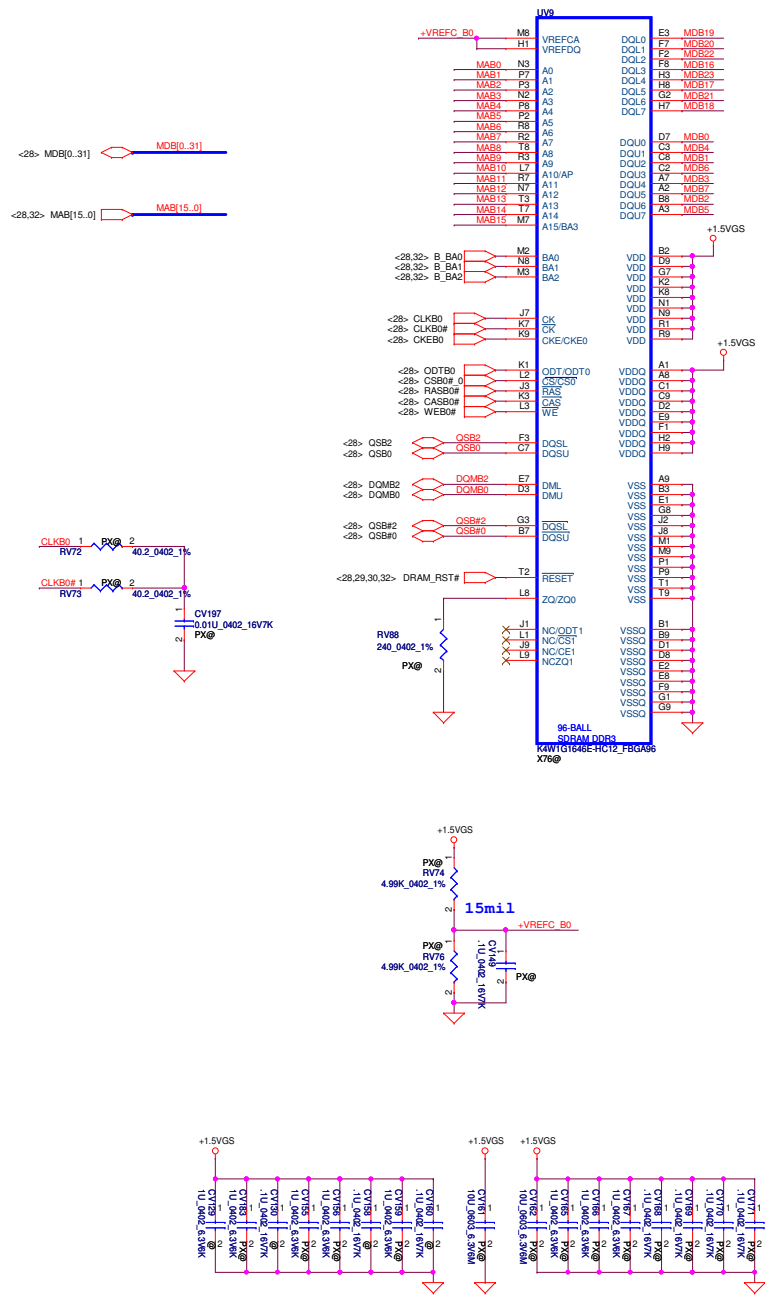
PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

VGA_CORE Cap in power side sheet



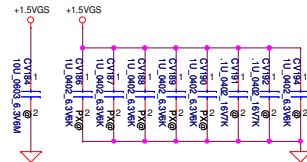
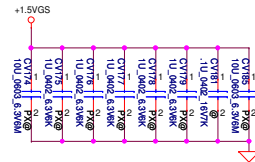
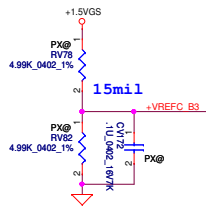
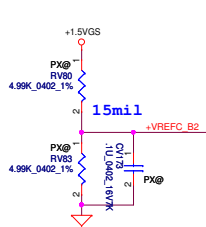
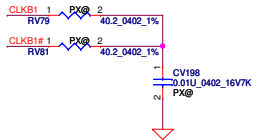
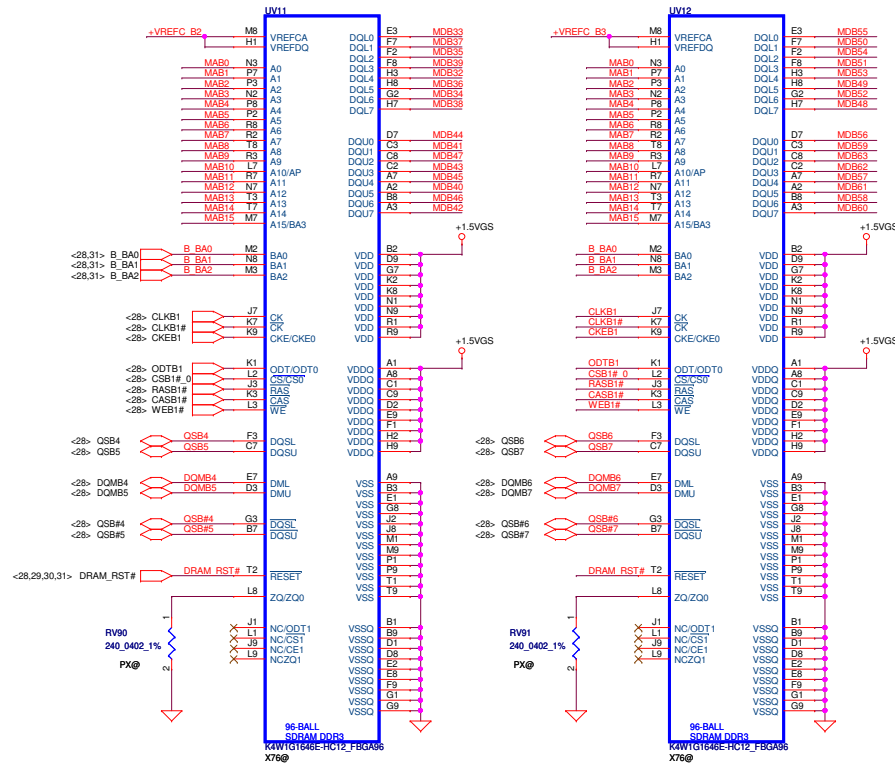
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	ATI Whistler M2 VRAM A	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 1.0
Size C	Document Number LA-9631P	Date: Wednesday, February 27, 2013	Sheet 30 of 60		



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				ATI Whistler M2 VRAM B
Size C	Document Number LA-9631P	Date: Wednesday, February 27, 2013	Sheet 31 of 60	Rev 1.0

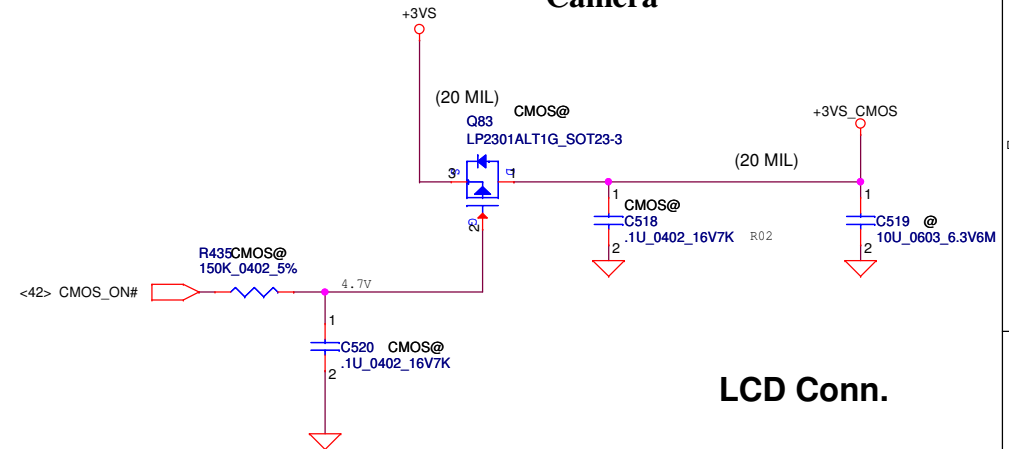
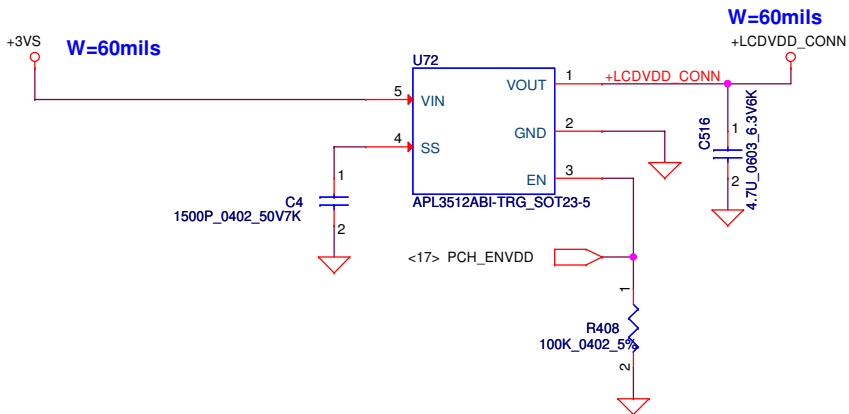
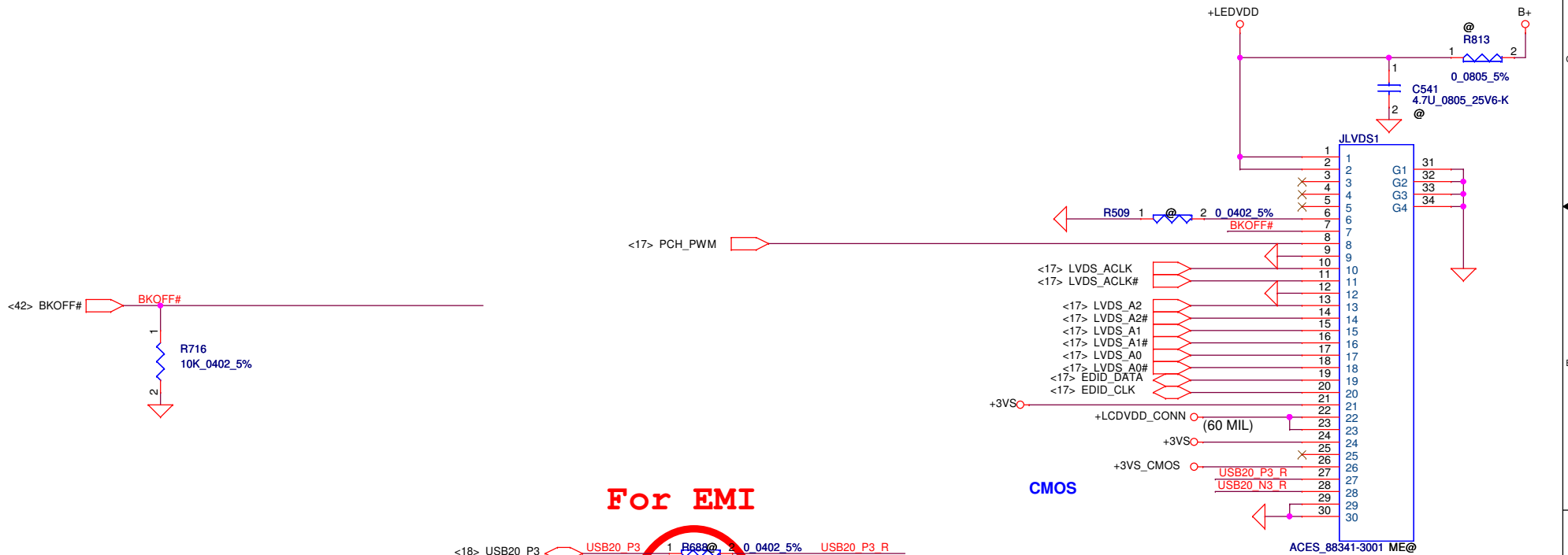
<28> MDB[32..63] MDB[0..31]

<28,31> MA[15..0] MA[15..0]

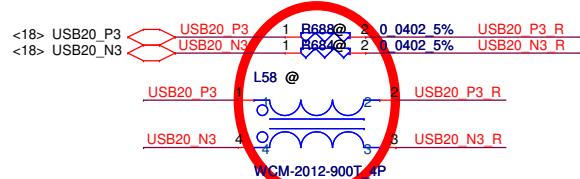


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				ATI Whistler M2 VRAM A
Size	Document Number	Rev		
C	LA-9631P	1.0		
Date:	Wednesday, February 27, 2013	Sheet	32	of 60

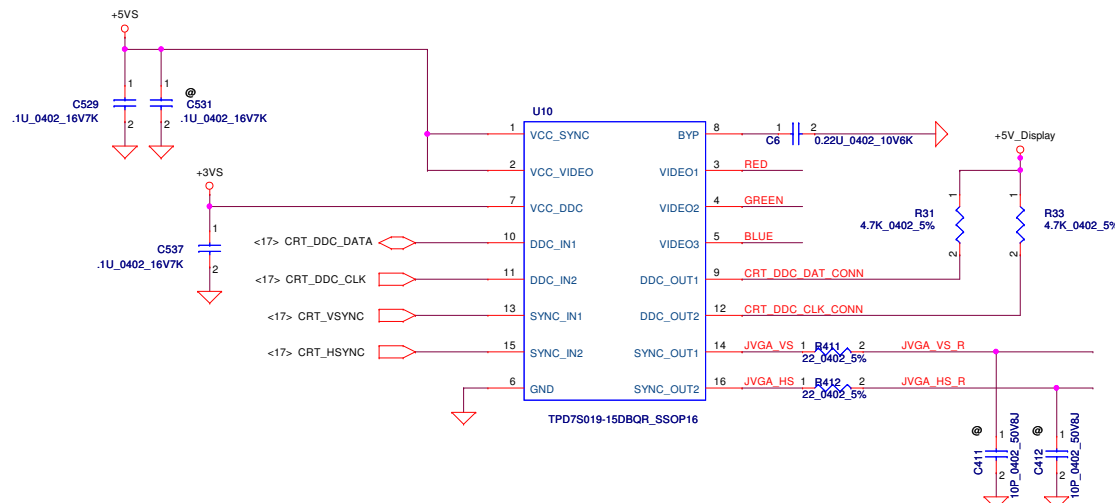
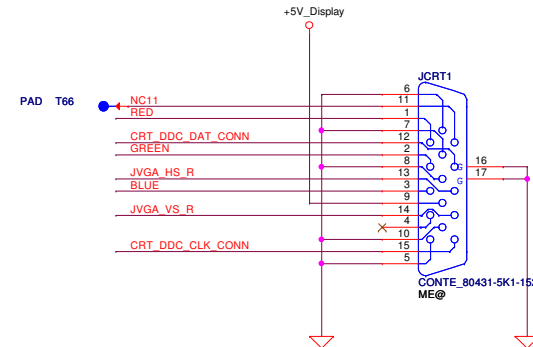
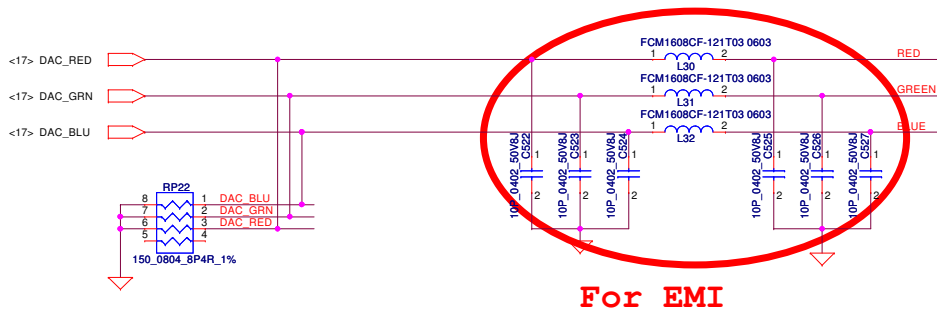
LCD POWER CIRCUIT

**LCD Conn.**

For EMI

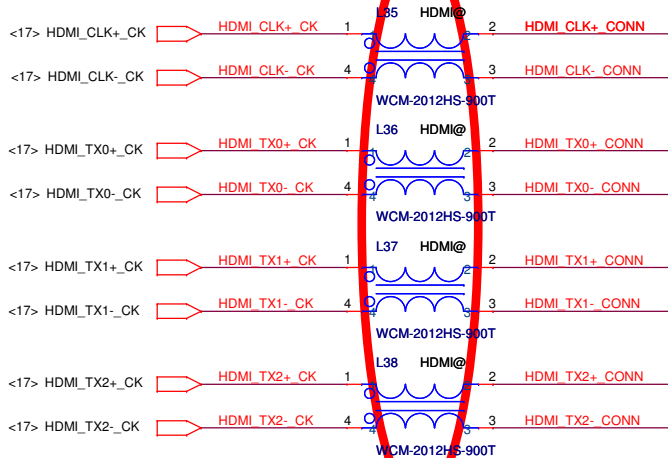


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LVDS/CAMERA		
				Size	Document Number	Rev
				Custom	LA-9631P	1.0
				Date:	Wednesday, February 27, 2013	Sheet 33 of 60

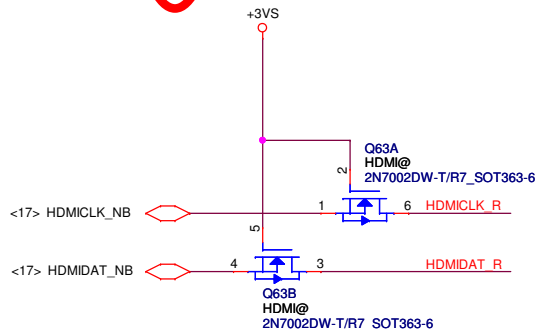
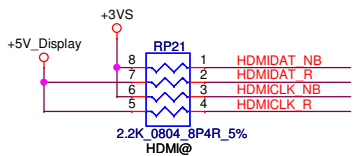


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF PRODUCT DEVELOPMENT AND DESIGN TO ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-9631P	1.0
				Date: Wednesday, February 27, 2013	Sheet 34 of 60

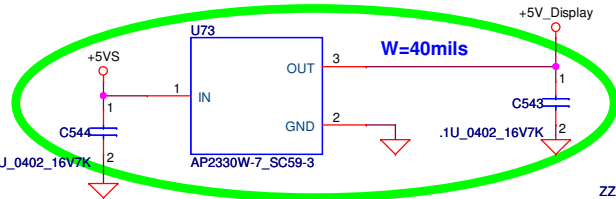
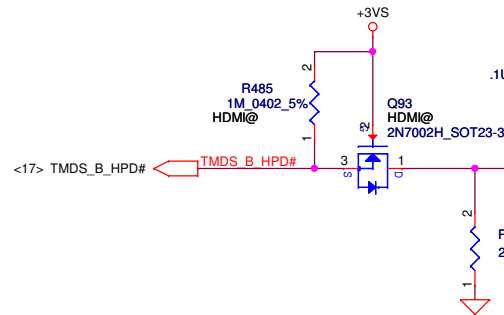
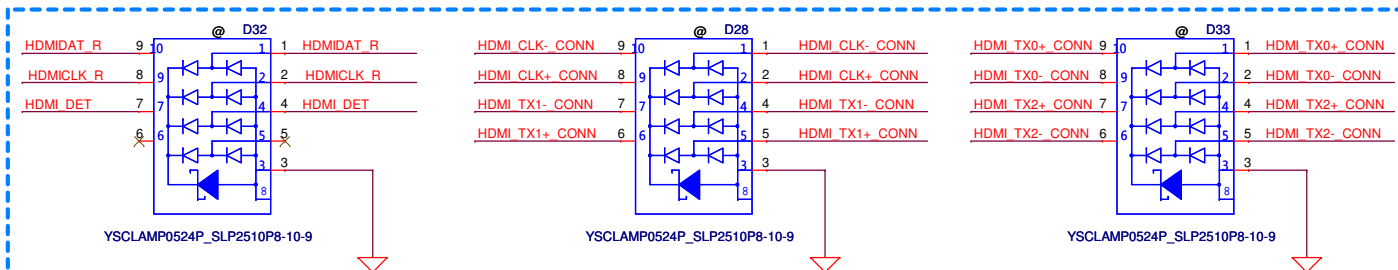
For EMI



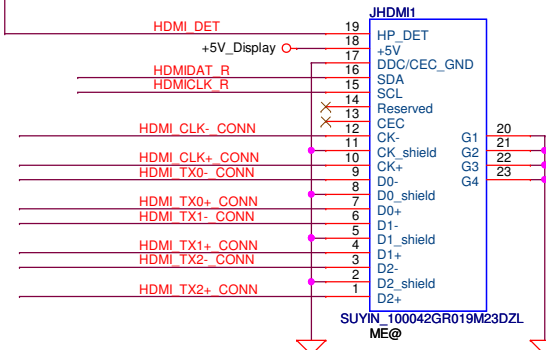
Pull up R for PCH OR VGA SIDE



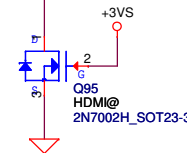
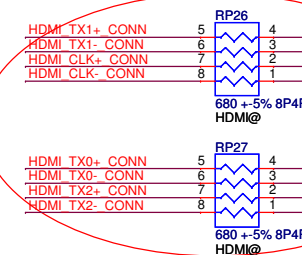
ESD



For CRT and HDMI

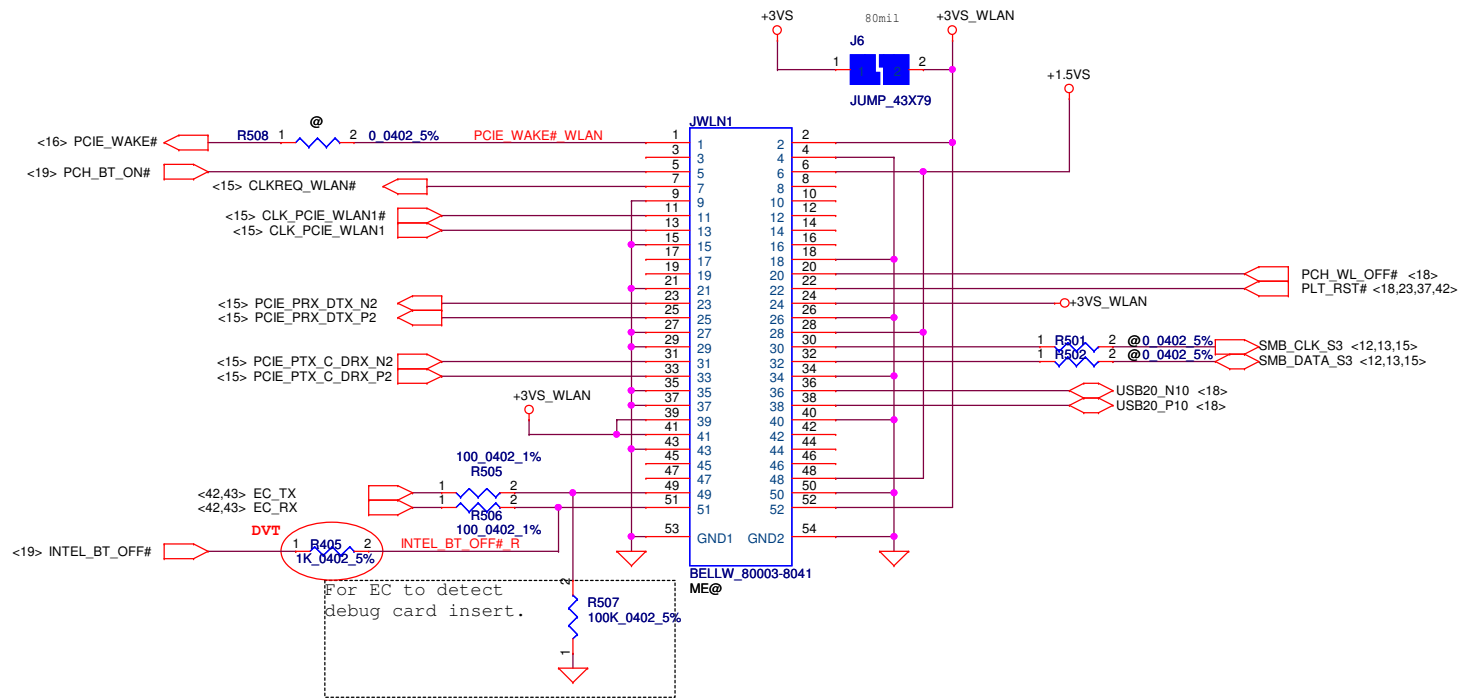


DVT



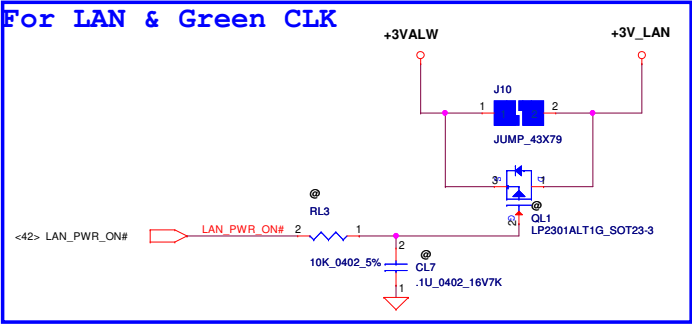
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	HDMI CONN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-9631P	Rev 1.0
				Date: Wednesday, February 27, 2013	Sheet 35 of 60

Mini Card for WLAN/WiMAX(Half)

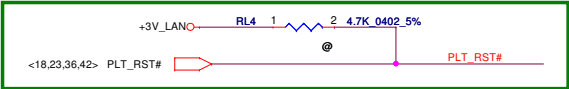


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-9631P	Rev 1.0
Date: Wednesday, February 27, 2013				Sheet 36	of 60

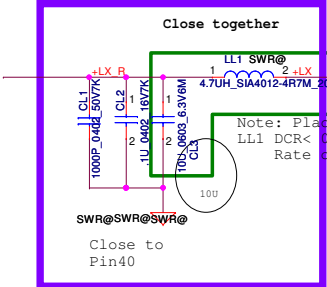
For LAN & Green CLK



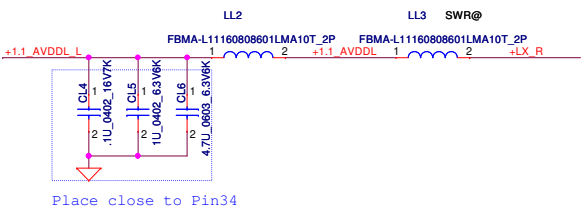
Vendor recommend reseve the
PU resistor close LAN chip



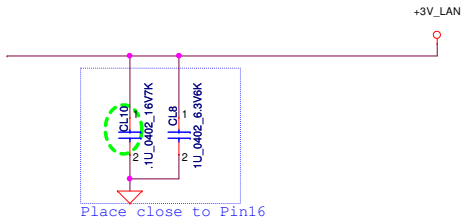
UL1 8172@
QCA8172-BL3A-R
SA000065410
S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL



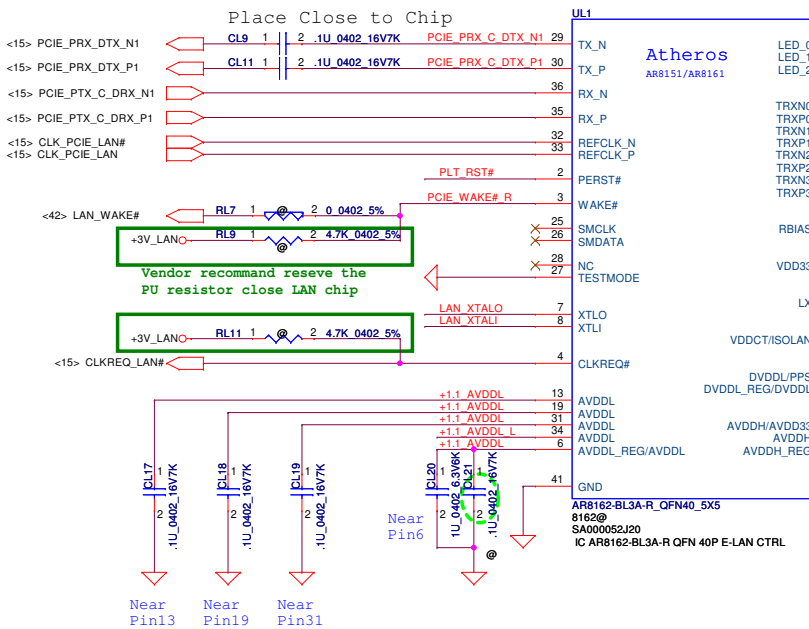
Note: Place Close to LAN chip
LL1 DCR< 0.15 ohm
Rate current > 1A



Place close to Pin34

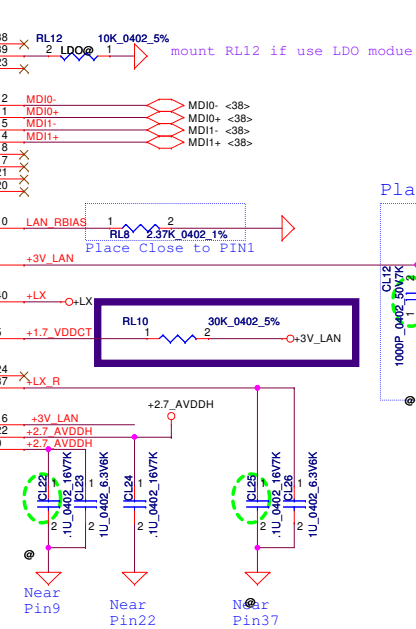


don't @ (could be B C cost done)



Vendor recommend reseve the
PU resistor close LAN chip

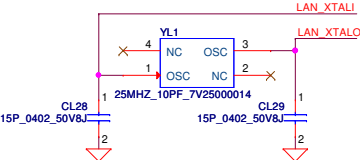
Near Pin13
Near Pin19
Near Pin31



Near Pin9

Near Pin22

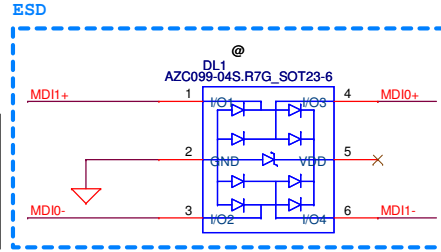
Near Pin37



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LAN-AR8162/8172
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size Custom	Document Number	LA-9631P	Rev 1.0
Date: Wednesday, February 27, 2013		Sheet	37	of	60

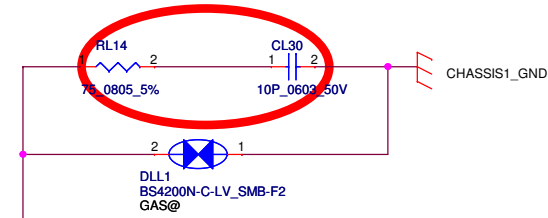
DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

Place Close to TL1



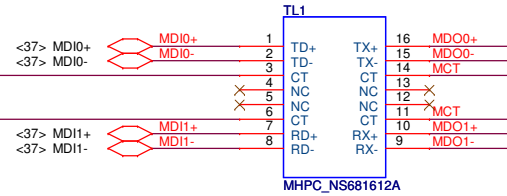
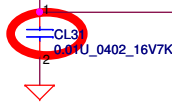
Reserve gas tube for EMI go rural solution

For EMI

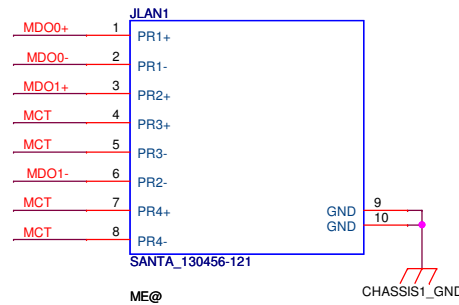
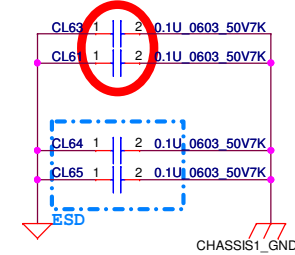


Place Close to TL1

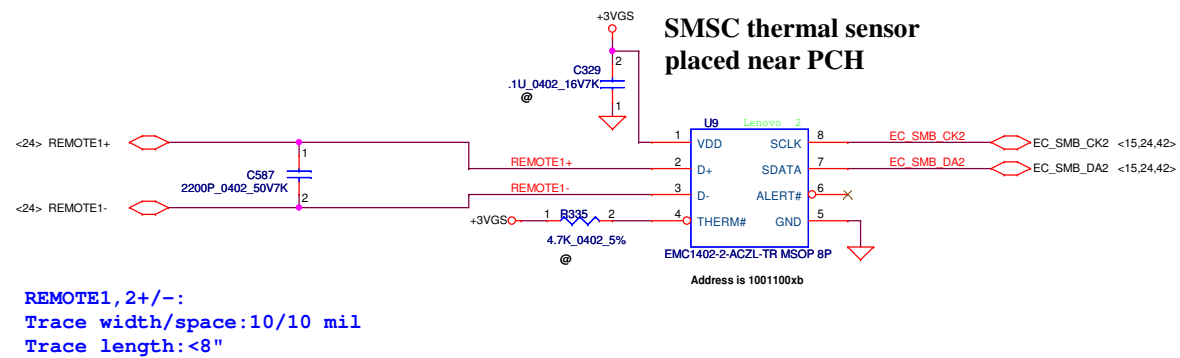
For EMI



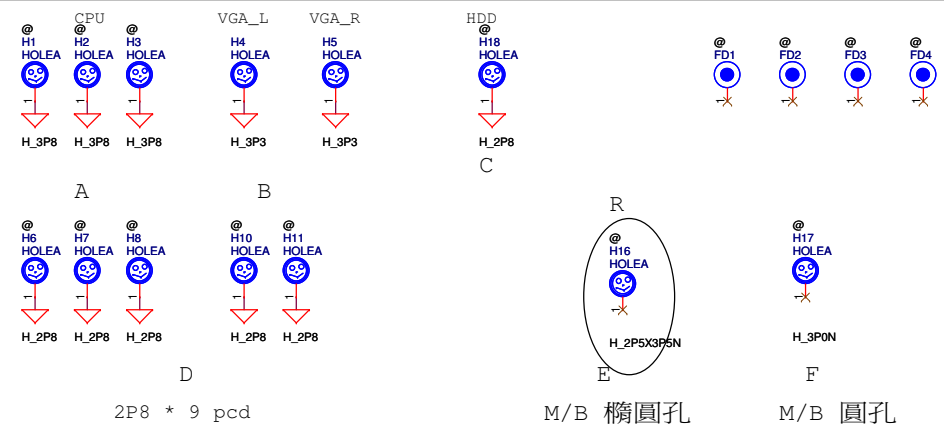
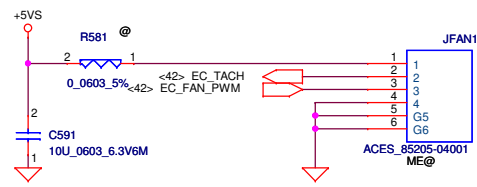
For EMI



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LAN_Transformer
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date	Wednesday, February 27, 2013
				Sheet	38 of 60
				Rev	1.0
				LA-9631P	

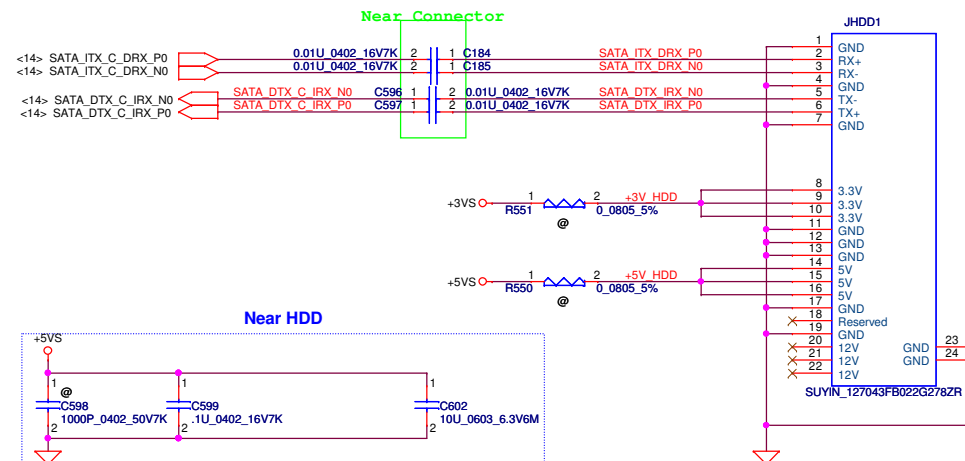


FAN1 Conn

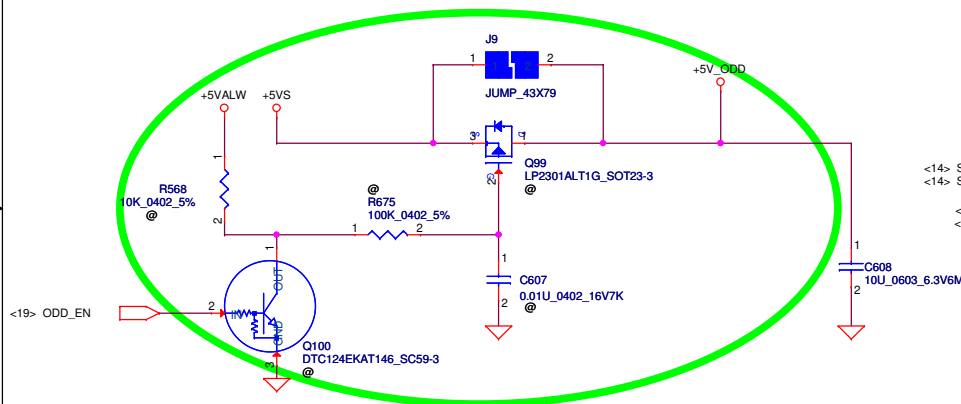


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Fintek-Thermal IC/FAN/screw	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-9631P	1.0
				Date: Wednesday, February 27, 2013	Sheet 39 of 60	

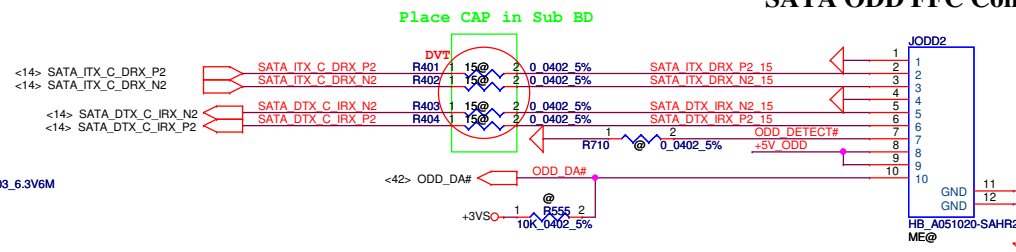
SATA HDD Conn.



ODD Power Control

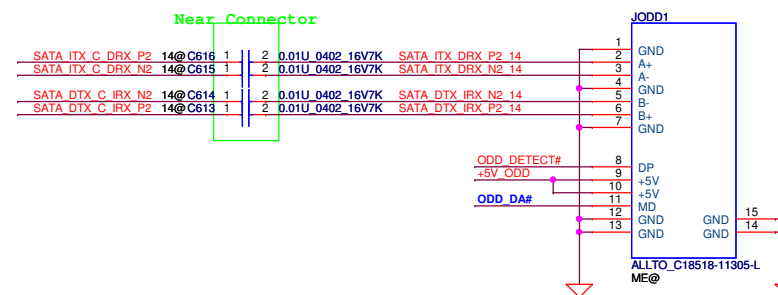


FOR 15" SATA ODD FFC Conn.



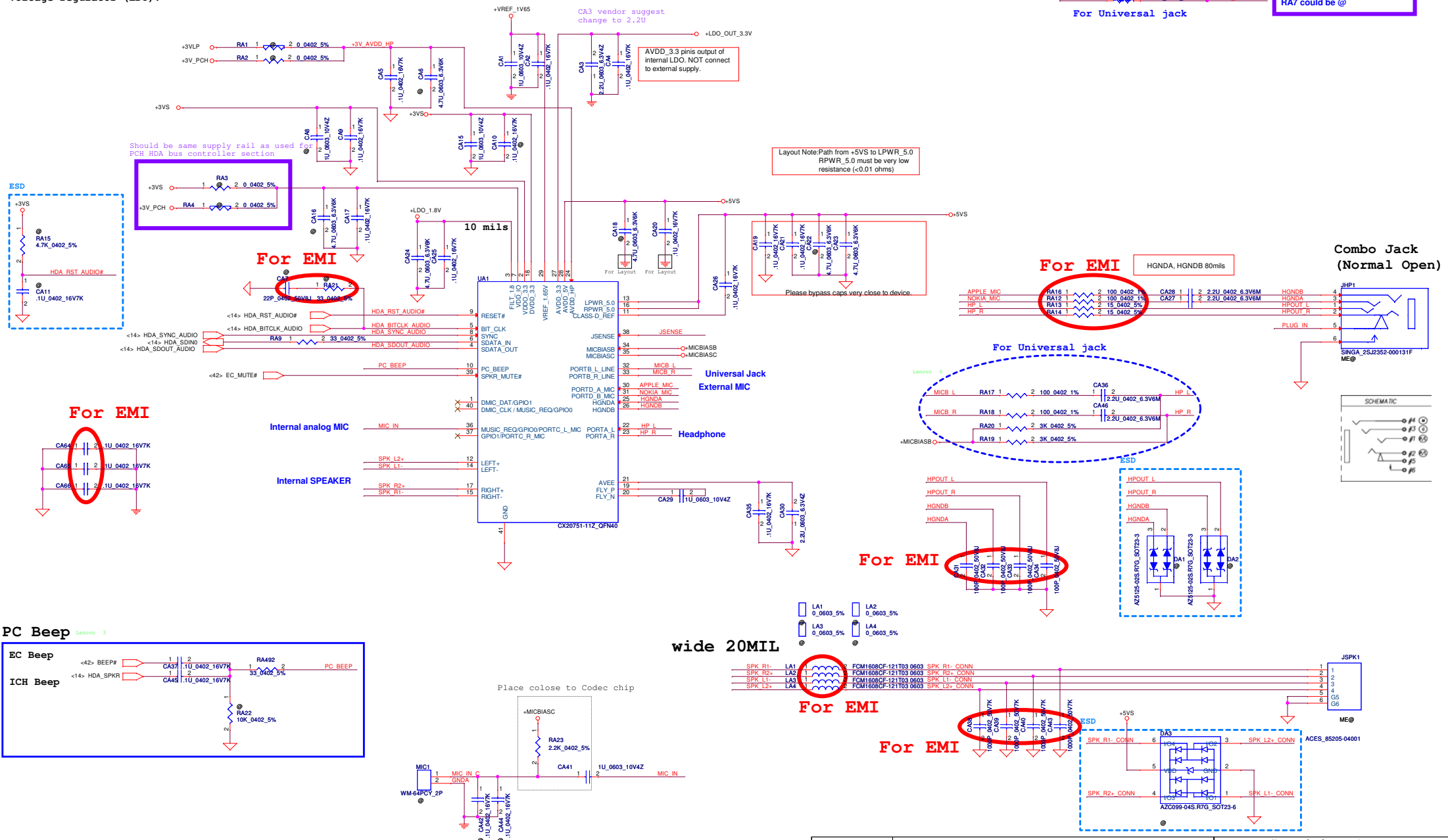
Co-lay

FOR 14" SATA ODD Conn.

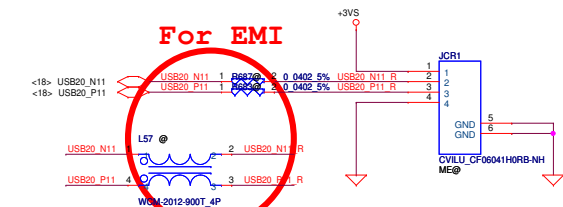
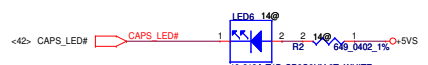
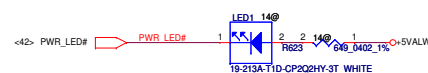
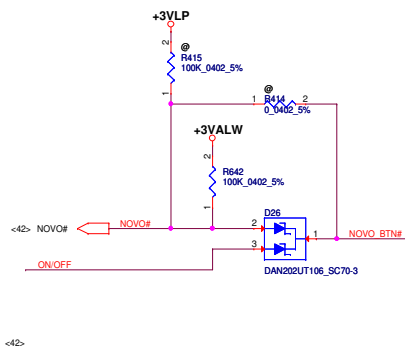
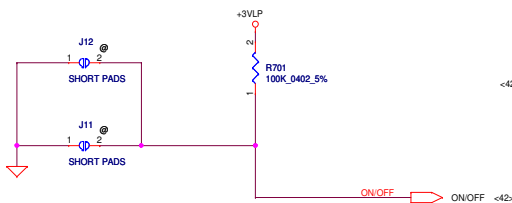
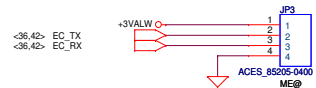


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	HDD/ODD/BT Connector	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-9631P	1.0
				Date:	Wednesday, February 27, 2013	Sheet 40 of 60

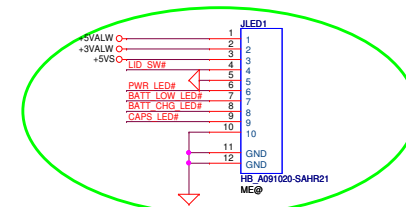
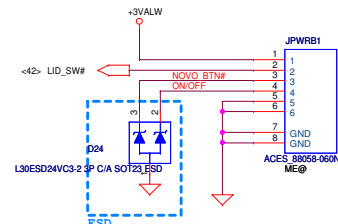
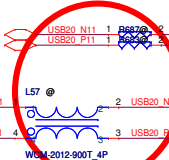
CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



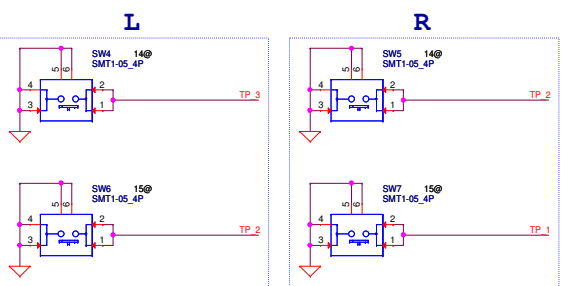
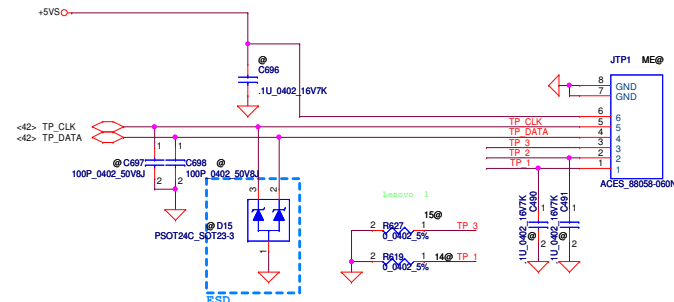
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> Title CX20751 Codec	
Issued Date 2011/06/15		Deciphered Date 2012/07/11		Size Custom Document Number LA-9631P	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date: Tuesday, March 05, 2013 Sheet 41 of 60	



For EMI

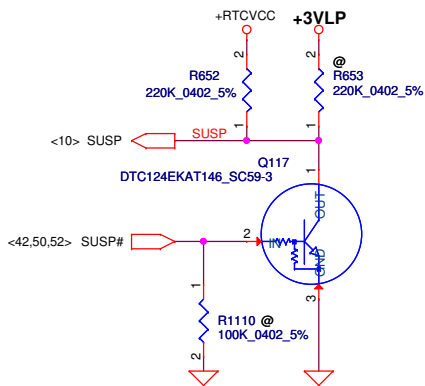
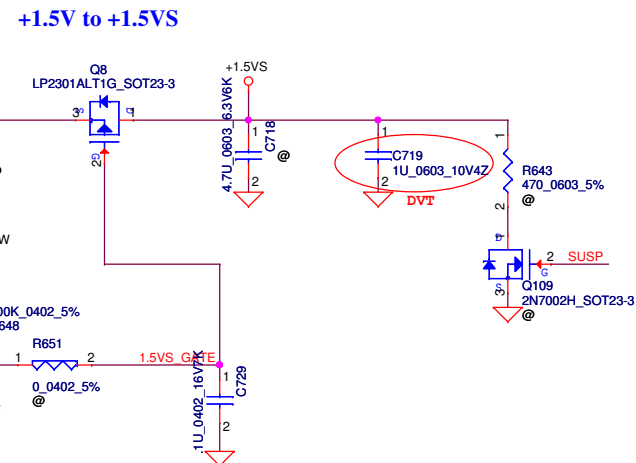
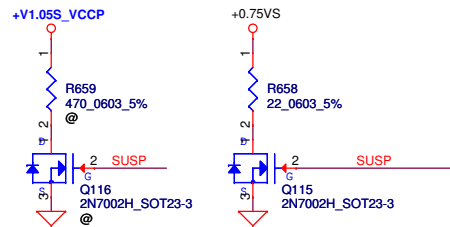
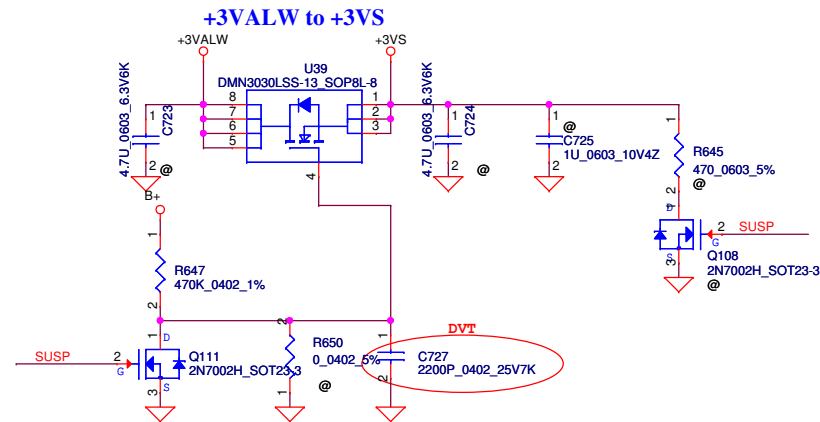
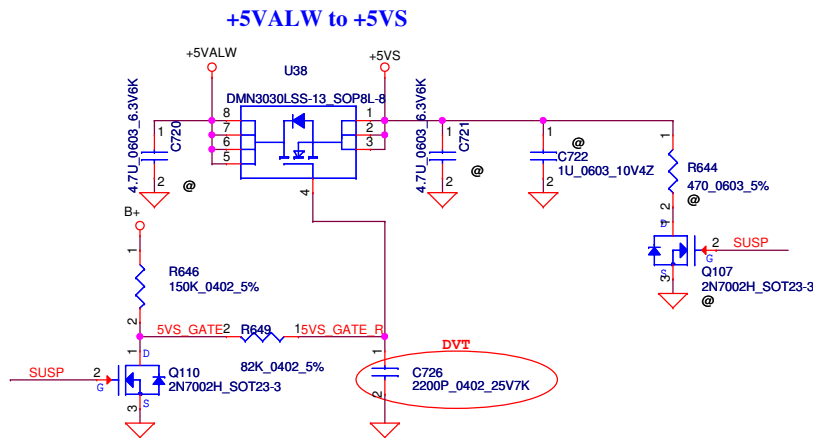


For 15"

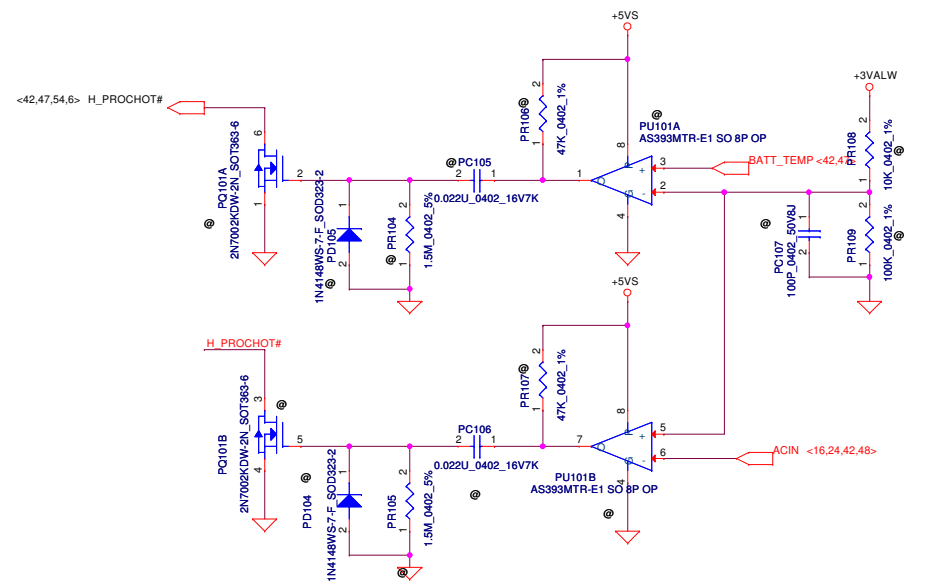
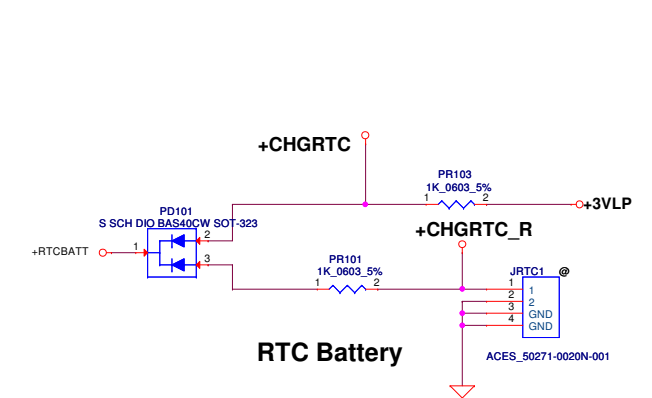
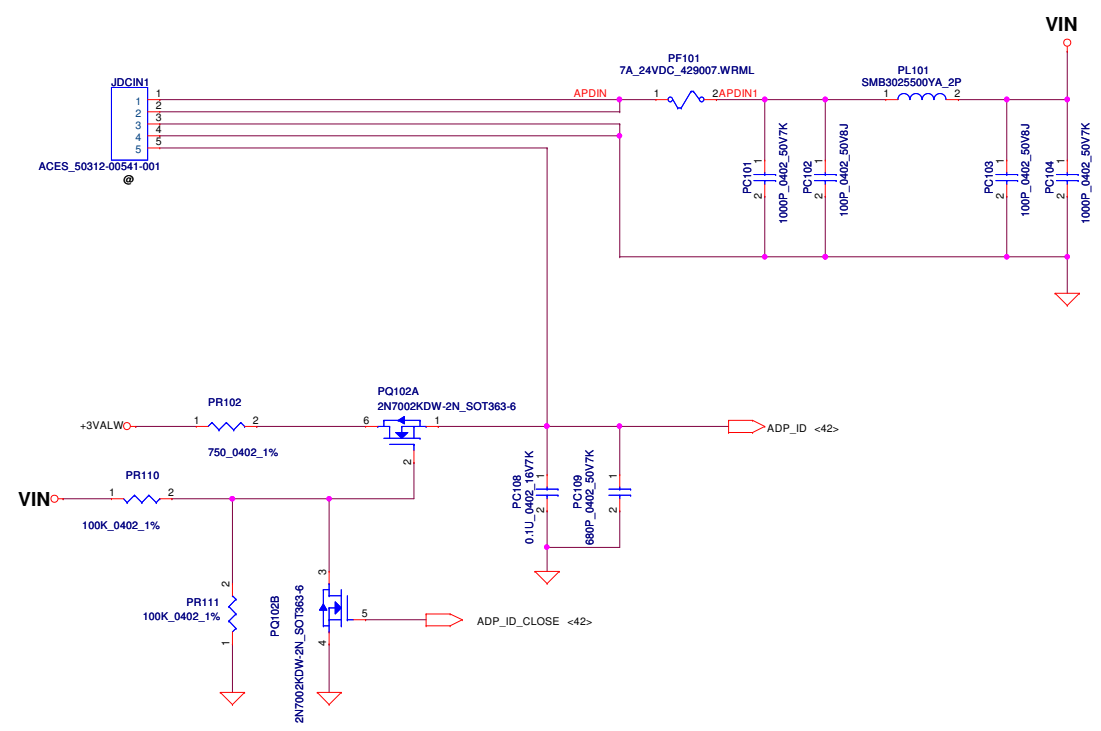


15/17"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND



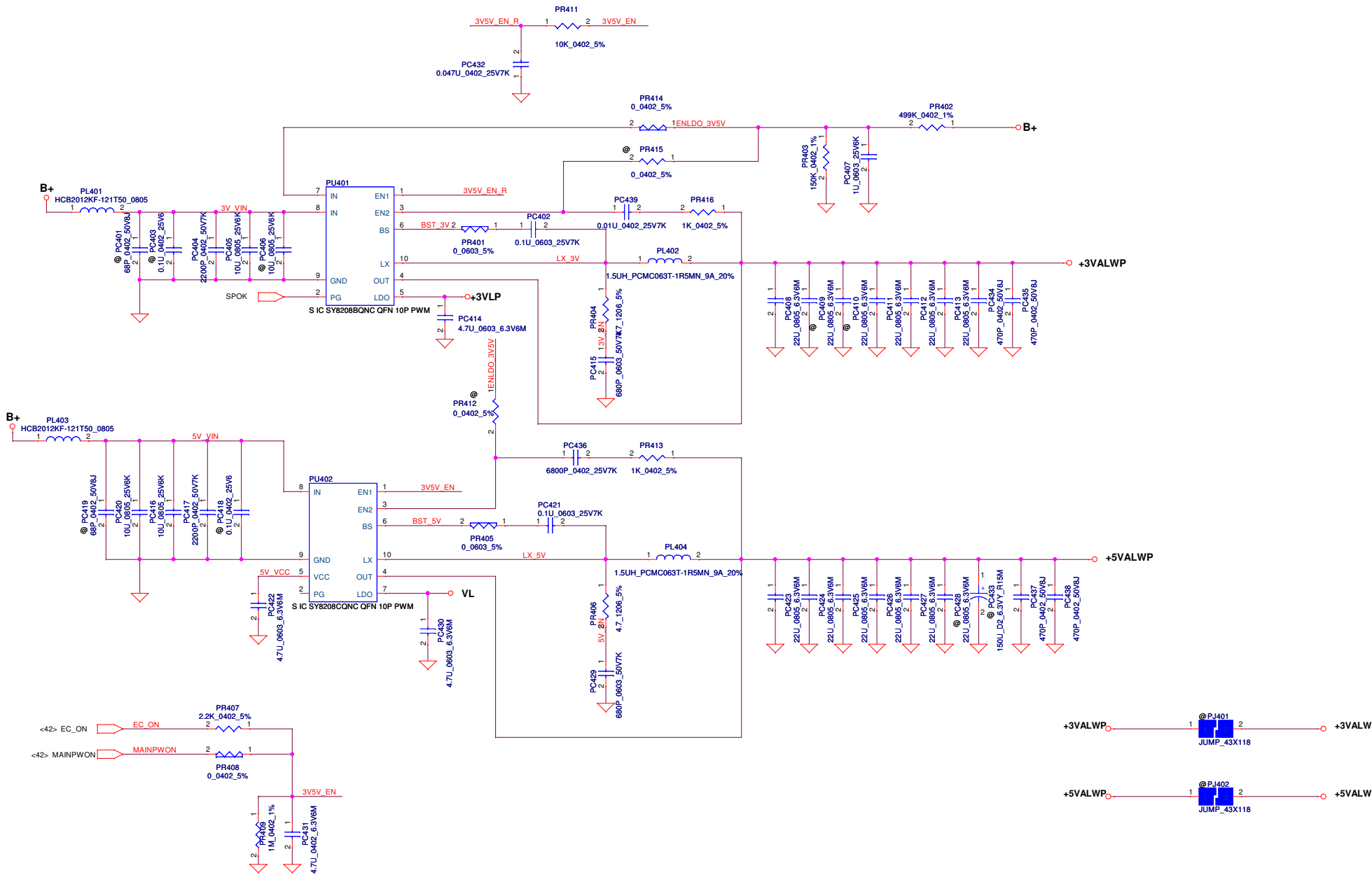
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9631P
				Rev	1.0
				Date:	Wednesday, February 27, 2013
				Sheet	45 of 60



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIELD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR DCIN / RTC Battery	
				Document Number	Rev
				Gx00	1.0
				Date:	Wednesday, February 27, 2013
				Sheet	46 of 60



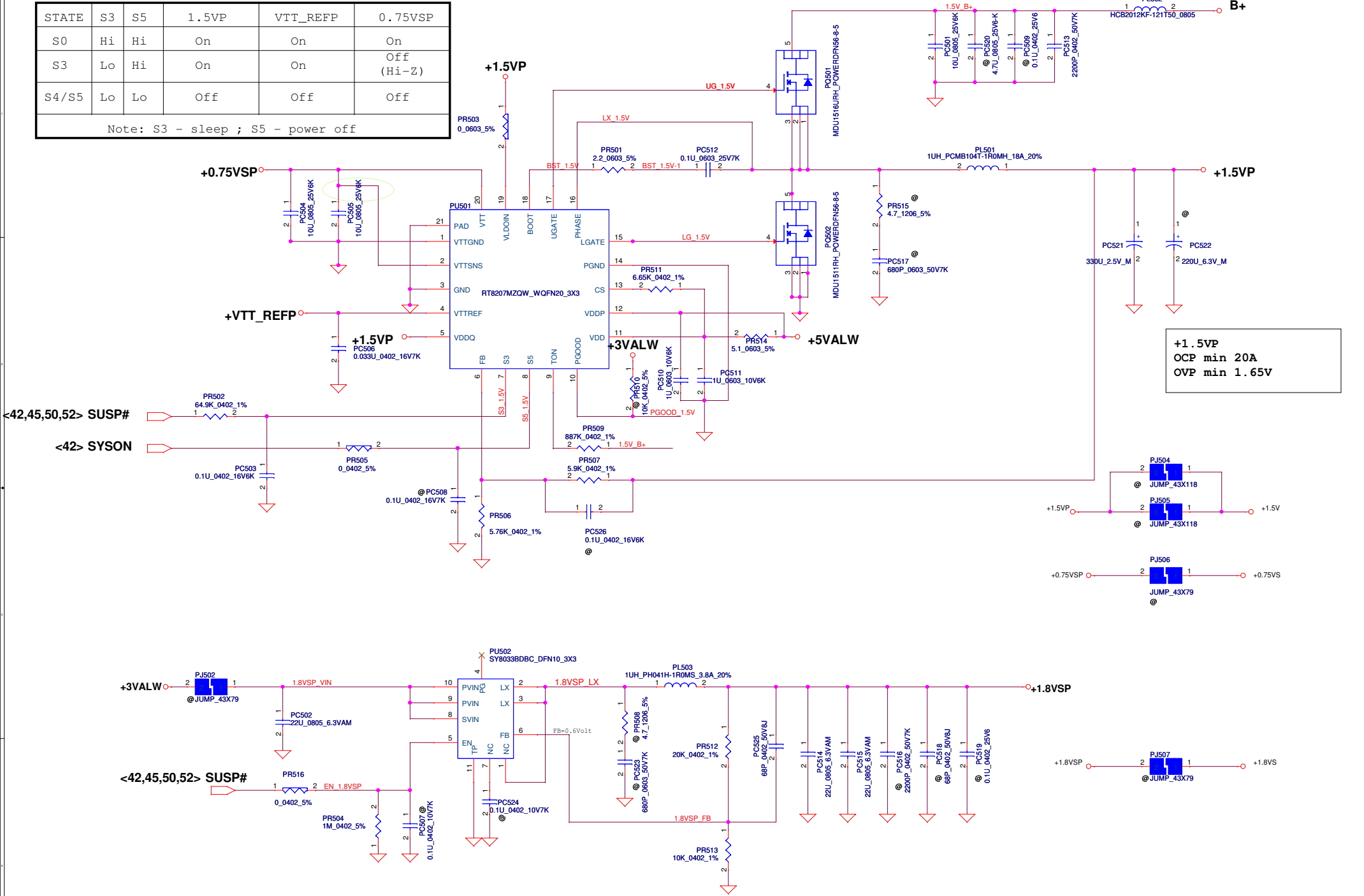
Date:	Wednesday, February 27, 2013	Sheet	48	of	60
-------	------------------------------	-------	----	----	----



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FRONTRON CORPORATION EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				Gx00-CR
				Rev
				1.0
				Date
				Wednesday, February 27, 2013
				Sheet
				49 of 60

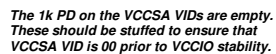
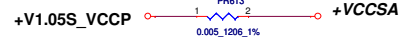
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



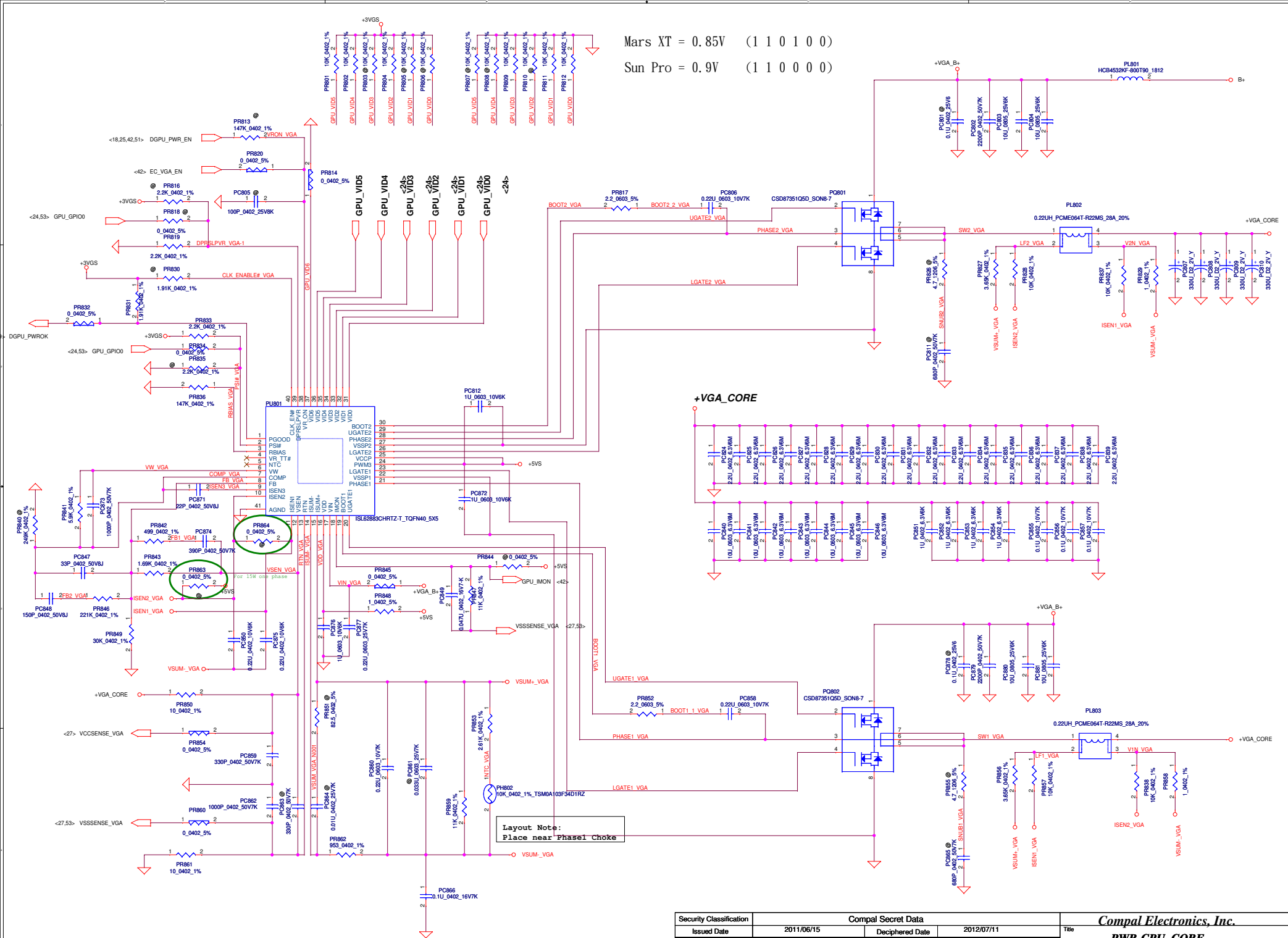
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	+1.5VP/+1.8VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	Gx00-CR
				Date	Wednesday, February 27, 2013
				Sheet	50 of 60
				Rev	1.0

output voltage adjustable network

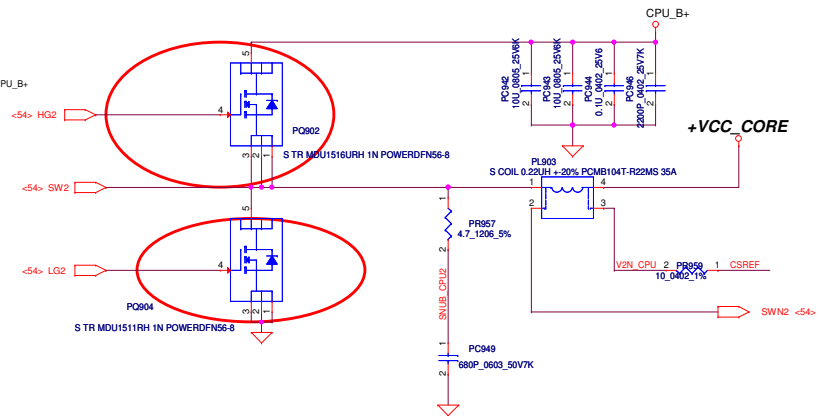
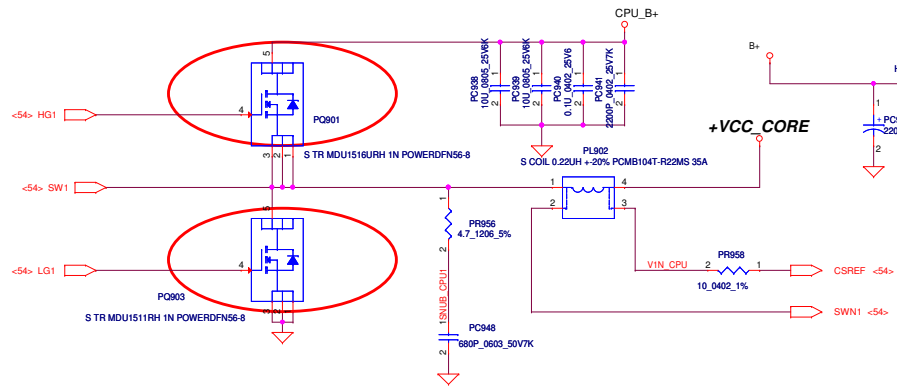


Mars XT = 0.85V (1 1 0 1 0 0)

Sun Pro = 0.9V (1 1 0 0 0 0)

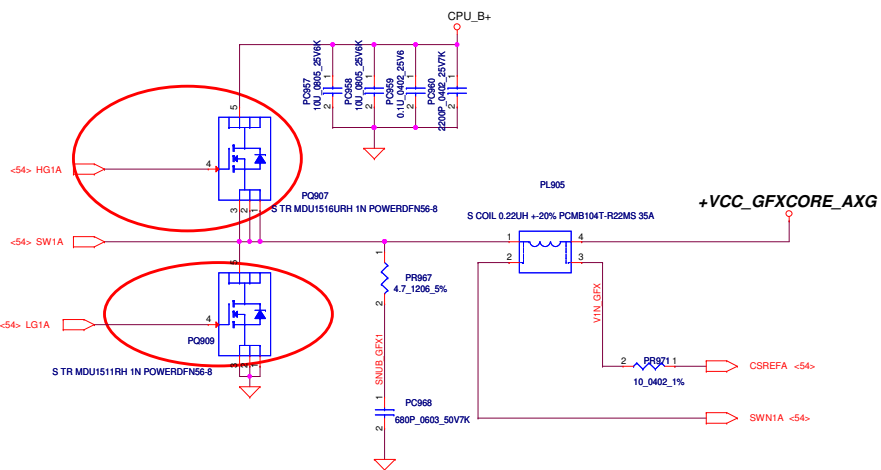


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Document Number	Gx00-CR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date	Wednesday, February 27, 2013
				Sheet	53 of 60



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP=110A

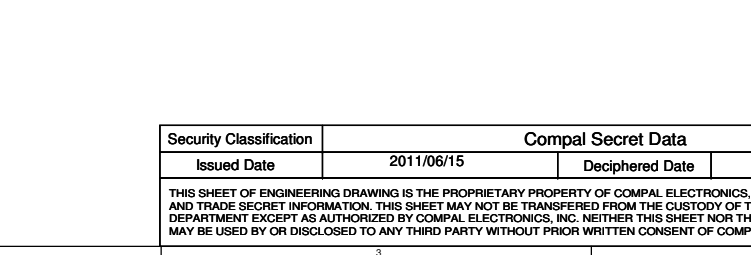
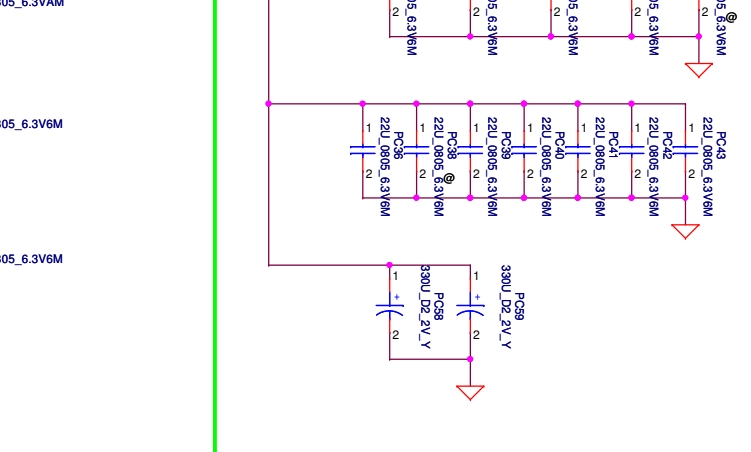
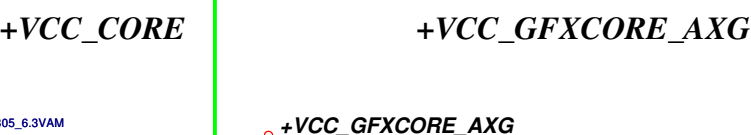
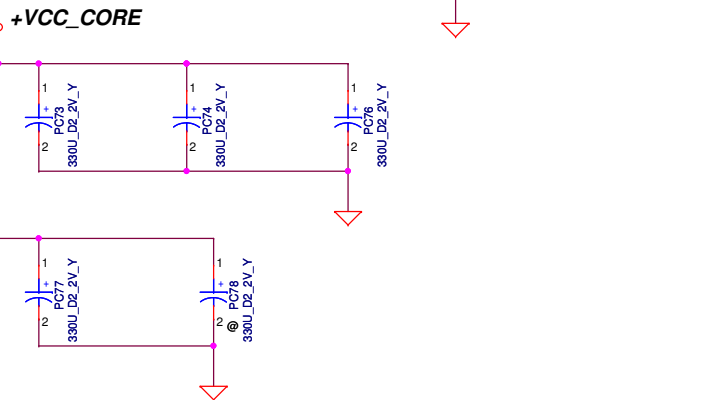
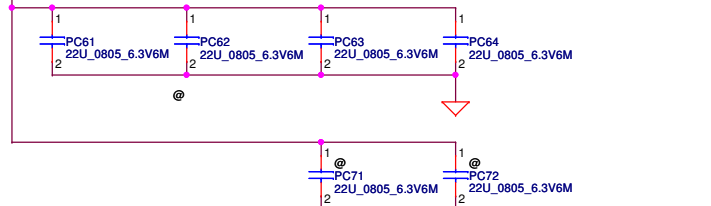
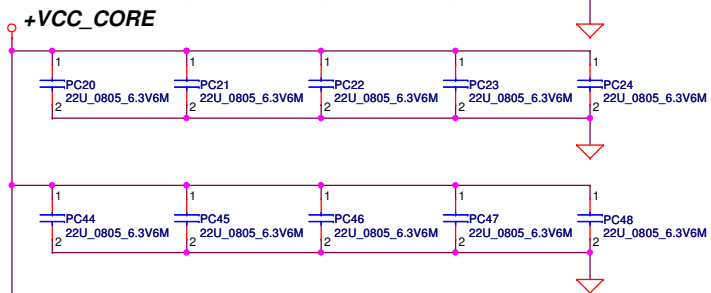
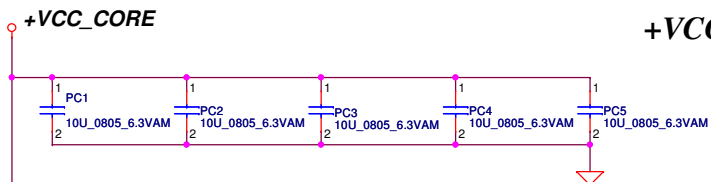
DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP=65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP=55A

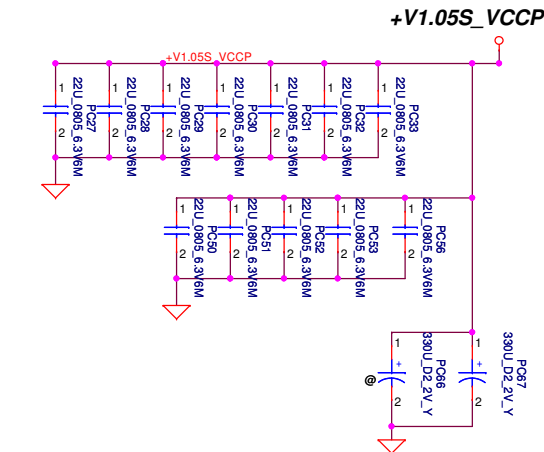
DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP=40A

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PWR-CPU CORE
Size	Document Number	Gx00-CR		Rev
C		1.0		
Date:	Wednesday, February 27, 2013	Sheet	55	of 60



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/06/15				Deciphered Date			
2012/07/11				Title				PWR - PROCESSOR DECOUPLING			
Size				Document Number				LA-9631P			
Date				Wednesday, February 27, 2013				Sheet 56 of 60			

VIWGP/R PWR PIR List

Item	Page	MODIFICATION LIST	PURPOSE	EVT TO DVT
1	P. 46	Add PR102, PC108, PC109	For ADP_ID pin detect	
2	P. 47	Add PR225, PR227, PR228, PQ206, PQ207, PQ208	For protect adapter function	
3	P. 49	Add PR410, PC433	For 3VALWP/5VALWP sequence	
4	P. 49	Add PC434, PC435, PC436, PC437	For EMI solution	
5	P. 49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple	
6	P. 50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence	
7	P. 51	Add PC637	For +0.95VGSP sequence	
8	P. 54	Change PC907, PR912, PR927, PC928	For CPU Transient Compensation	

9	P. 48	Add PR326 and PQ314	For battery health function	PVT TO PVT2
10	P. 49	Add PR411, PC432	To delay +3VALW enable. PR411 change to 10K and PC432 change to 0.047uF	
11	P. 49	Change PC439 from 4700P to 10nF , PC436 from 47nF to 6.8nF	Adjust +3VALW and +5VALW rising time.	
12	P. 51	Add PR614	For Celeron CPU SA_PGOOD	
13				
14				
15				
16				
17				
18				
19				
20				
21				
22				
23				

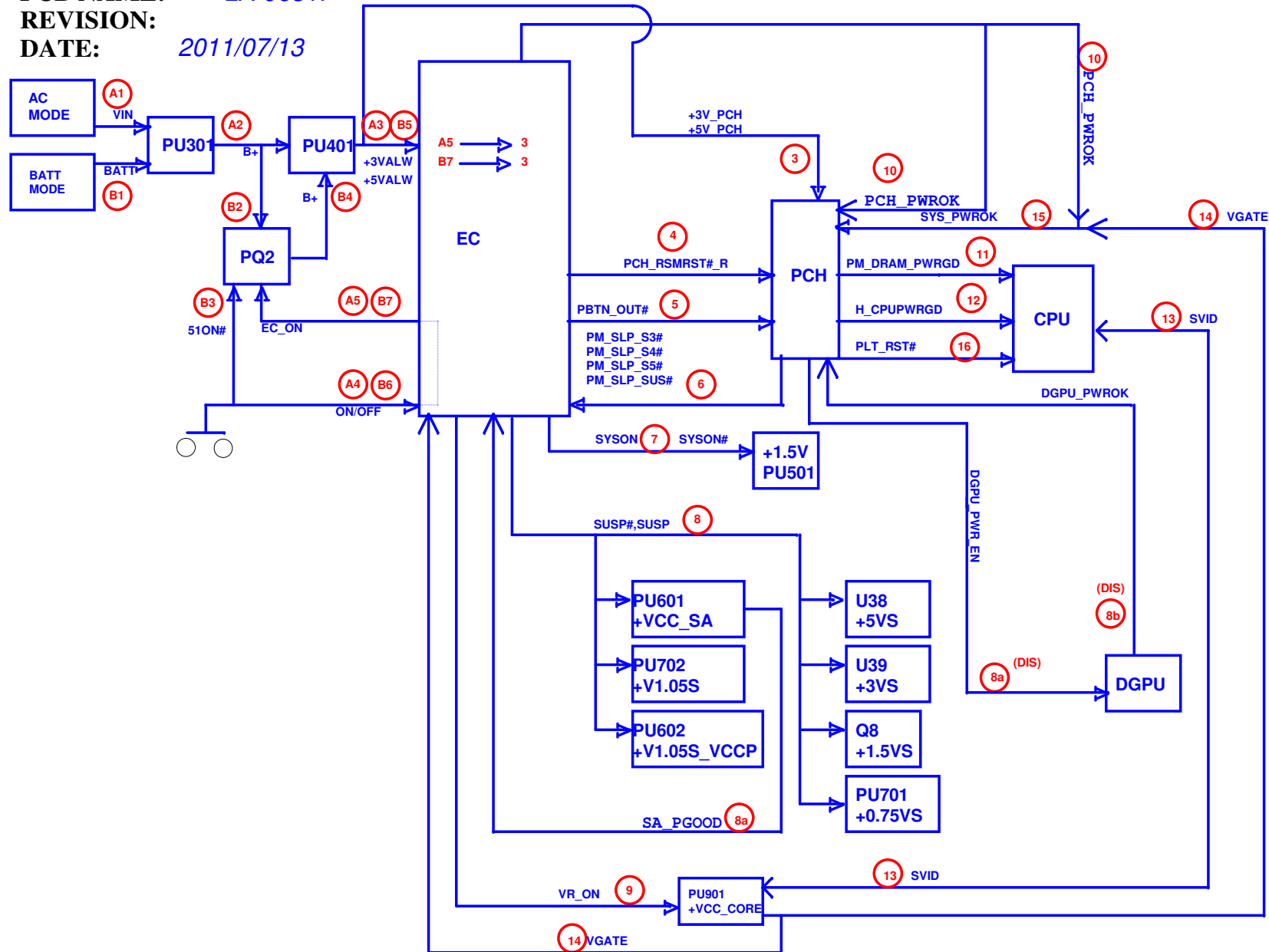
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*

PCB NAME: *LA-9631P*

REVISION:

DATE: *2011/07/13*



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Power sequence
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIELD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-9631P
				Date	Wednesday, February 27, 2013
				Sheet	58 of 60
				Rev	1.0

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	EVT TO DVT
1	P. 46	Change C726, C727 to 2.2nF	For Sequence	
2	P. 36	Add R405	For Intel Combo Card	
3	P. 35	Delete RP19. Add RP26, RP27	Because ME modify MIC location	
4	P. 14	Add R406, R407, R408, R409	Reserve for improvement factory processes	
5	P. 42	Add EC_SPI_S0, EC_SPI_S1, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes	
6	P. 42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes	
7	P. 42	Reserve R410	Reserve Pull-high for GPIO	
8	P. 5-32	Change footprint of JCPU1, U4, UV1, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	For Lenovo rule	
9	P. 25	Change RV41 to 240K. Change CV53 to 0.1uF	For VGA sequence	
10	P. 21	Add Q21, R40, C237, R225, C243	Reserve for power consumption	
11	P. 34	Add R411, R412, C411, C412	Reserve for EMI	
12	P. 25	Change CV36, CV37 to 8.2pF	For Crystal fine-tune	
13	P. 42	Add ADP_65 to EC Pin.21	For adapter protection	
14	P. 42	Add ADP_90 to EC Pin.68	For adapter protection	
15	P. 42	Add ADP_135 to EC Pin.85	For adapter protection	
16	P. 42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design	
17	P. 42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design	
18	P. 42	Add ADP_ID to EC Pin.66	For adapter	
19	P. 42	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design	
20	P. 42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design	
21	P. 42	Add VGATE to EC Pin.74	Reserve for sequence	
22	P. 42	Add SYS_PWROK to EC Pin.86	Reserve for sequence	
23	P. 42	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design	
24	P. 42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design	
25	P. 42	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design	

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 40	Delete R416, Add J9	No need Zero ODD Function
2	P. 36	Reserve R508	For leakage current issue of Atheros WLAN
3	P. 33	Add R509	protect BKOFF# damage
4	P. 42	Reserve R416	Reserve +3VLP power rail to EC
5	P. 42	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P. 42	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC.
7	P. 14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P. 14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P. 41	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P. 42	Reserve resistance in EC for share ROM.	Follow common design
3	P. 51	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU