

Compal Confidential

DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

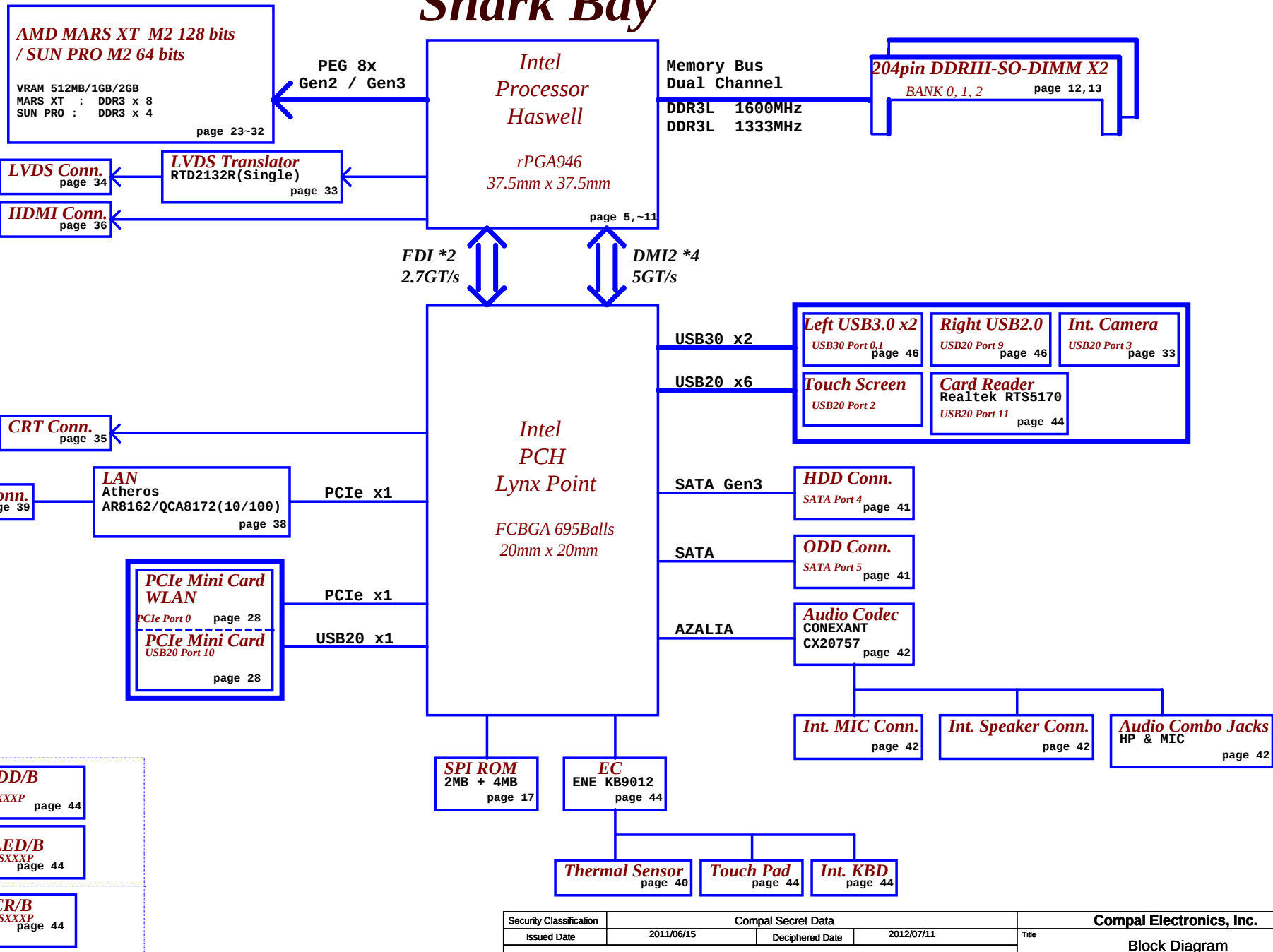
2013-02-27

LA-9641P

REV: 0.3

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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	Cover Page
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Shark Bay



Voltage Rails

power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS
				+VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
State				
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor	1001_100xb

PCH SM Bus address

AMD-GPU SM Bus address

Device	Address	Device	Address
DDR DIMM1 ChannelA	0xA0	Internal thermal sensor	1000_001xb
DDR DIMM2 ChannelB	0xA4		

Device	Address
RTD2132R	1101 010Xb

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	X	X
SMB_EC_DA2	+3VALW							+3VS	+3VS
SMBCLK	PCH	X	X	X	V	V	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SMLCLK	PCH	X	X	X	X	X	X	X	X
SMLDATA	+3VALW								
SMLCLK	PCH	V	X	V	X	X	V	X	V
SMLDATA	+3VALW	+3VS		+3VS			+3VS		+3VS

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
EHCI2	UHCI4	7	
		8	
	UHCI5	9	Right USB2.0
		10	WLAN
	UHCI6	11	Card reader
		12	
		13	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%	Board ID / SKU ID Table for AD channel				
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Porject	Phase
0	0	0 V	0 V	0 V	6-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	6-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	6-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	6-series	EVT

BOM Structure Table

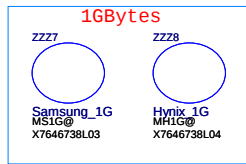
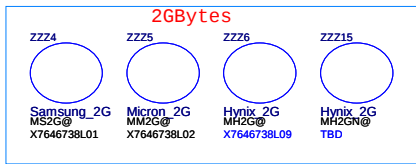
BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Cameara	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
Righ side USB	RUSB@
Zero ODD circuit	ZODD@
Share ROM	SROM@
Non-share ROM	NOSROM@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

VRAM BOM STRUCTURE Refer P4. VGA NOTE

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Mars XT VRAM STRAP

	X76@ Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ4 MS2G@	Samsung 2048Mbits SA0000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
ZZZ5 MM2G@	Micron 2048Mbits SA0000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@	Hynix 2048Mbits SA0000065300 H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
ZZZ7 MS1G@	Samsung 1028Mbits SA000004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
ZZZ8 MH1G@	Hynix 1024Mbits SA0000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC
ZZZ15 MH2GN@	Hynix 2048Mbits SA000006H400 128Mx16 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K



Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

VDDR3(3.3VGS)

PCIE_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD_CT(1.8V)

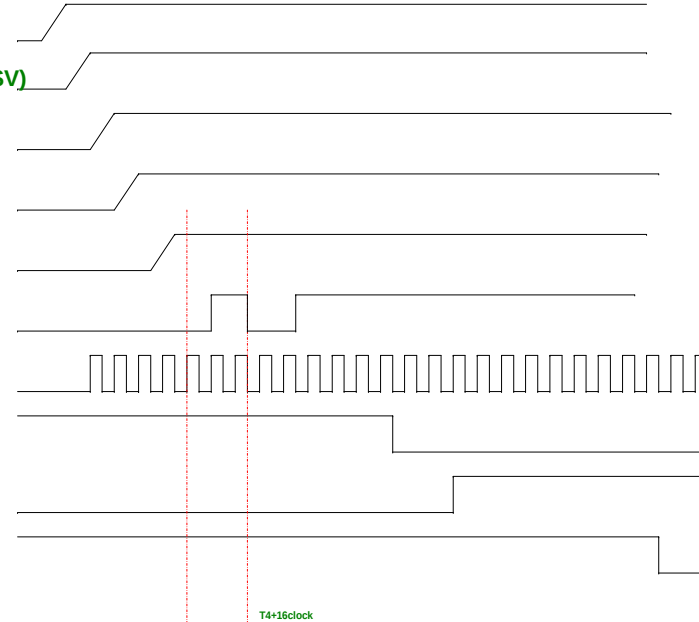
PERSTb

REFCLK

Straps Reset

Straps Valid

Global ASIC Reset

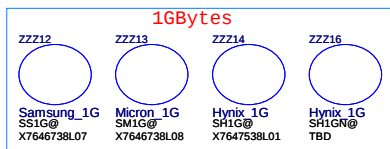
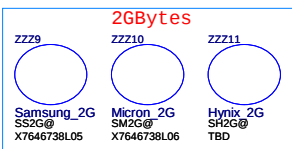


R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

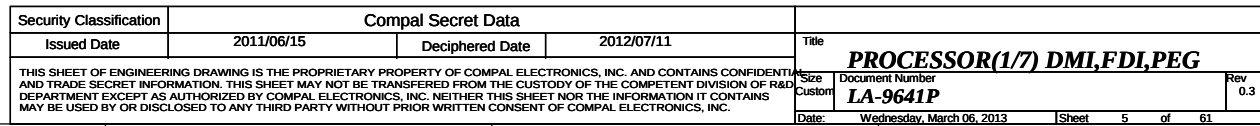
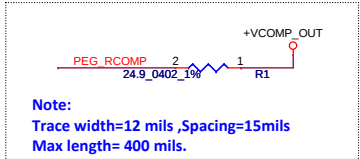
Note: 0402 1% resistors are required.

Sun PRO VRAM STRAP

	X76@ Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ9 SS2G@	Samsung 4096Mbits SA0000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
ZZZ10 SM2G@	Micron 4096Mbits SA0000065D00 256Mx16/1866 MT41K256M16HA-109G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@	Hynix 4096Mbits SA000006DG00 256Mx16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@	Samsung 2048Mbits SA0000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
ZZZ13 SM1G@	Micron 2048Mbits SA0000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@	Hynix 2048Mbits SA0000065300 H5TQ2G63DFR-N0C	1	1	1	4.75K	NC
	Hynix 2048Mbits SA000006H400 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K



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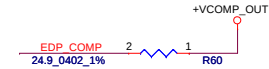


HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

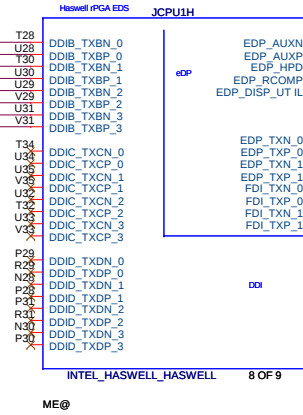
Place on connector side

COMPENSATION PU FOR eDP

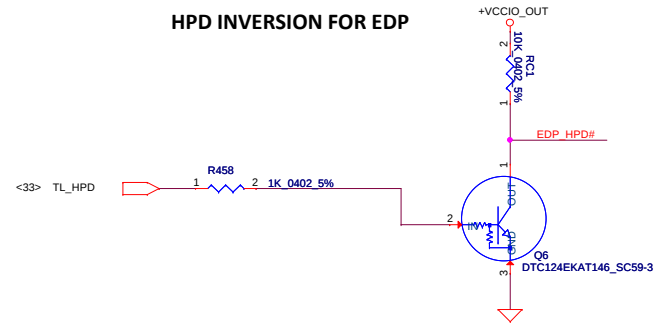


Note:

Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.



HPD INVERSION FOR EDP

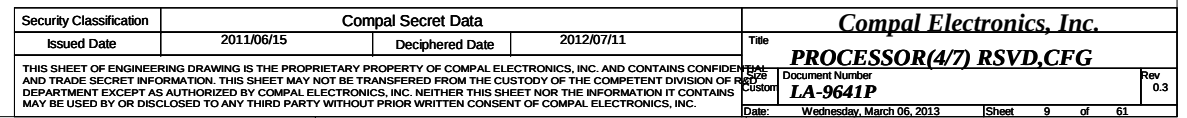


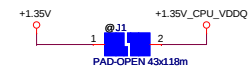
HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

A schematic diagram showing a resistor labeled R62 with a value of 1K_0402_1%. The resistor is connected between a pin labeled CFG2 and a ground symbol (a triangle pointing down). The pins are numbered 1 and 2.

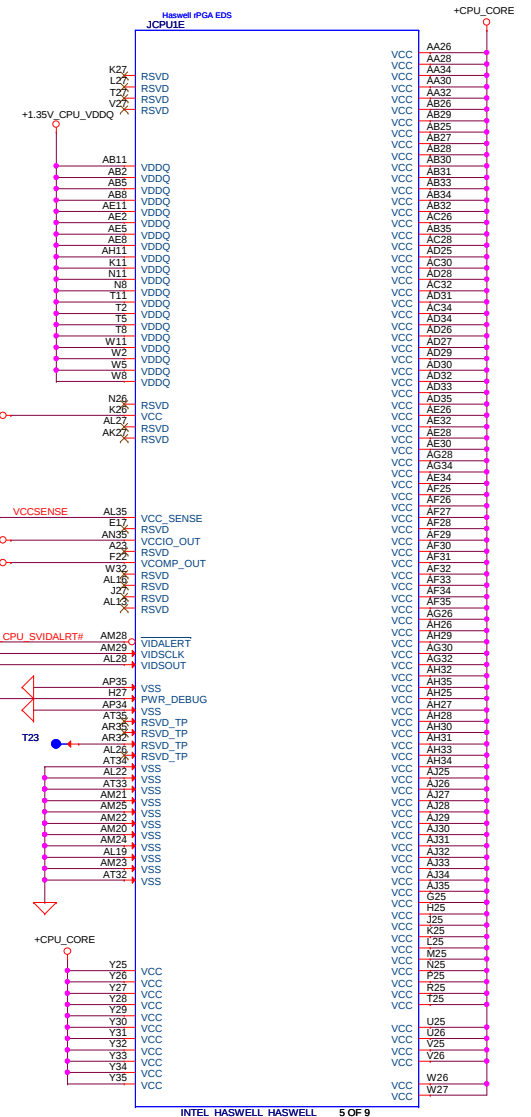
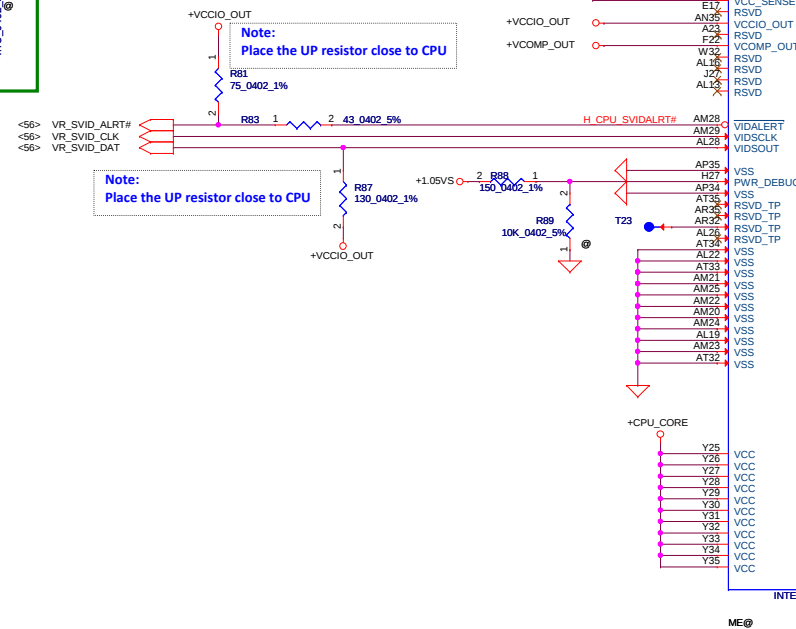
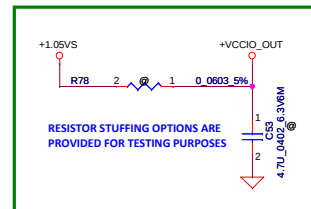
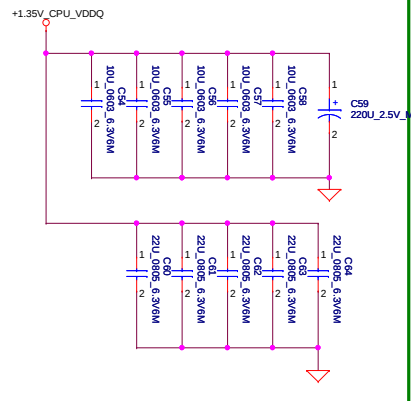
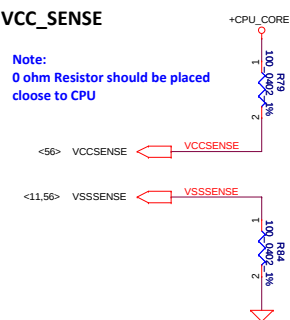
A schematic diagram showing a resistor labeled R63 with a value of 1K_0402_1%. The resistor is connected between a pin labeled CFG4 and a ground symbol.

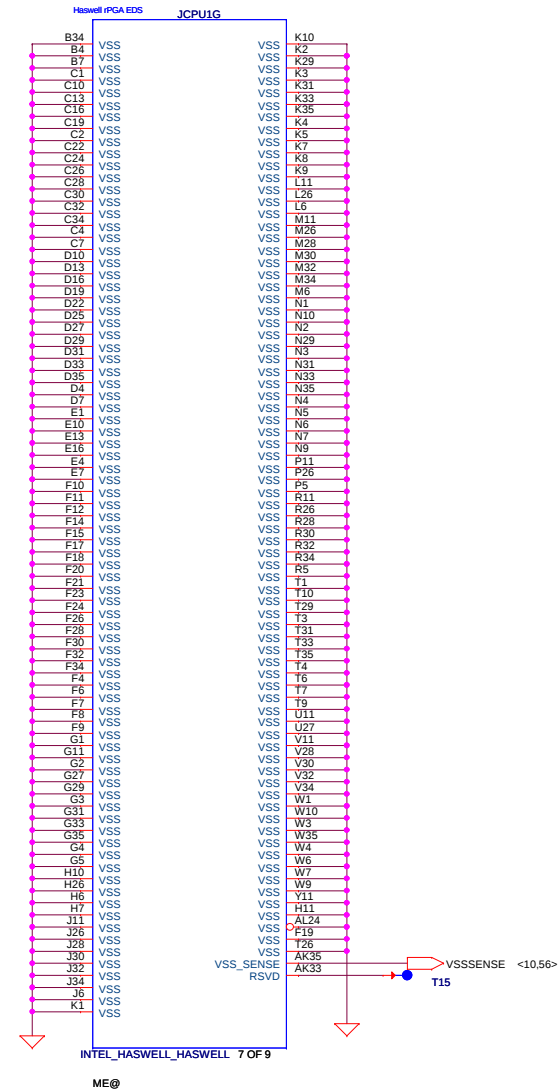
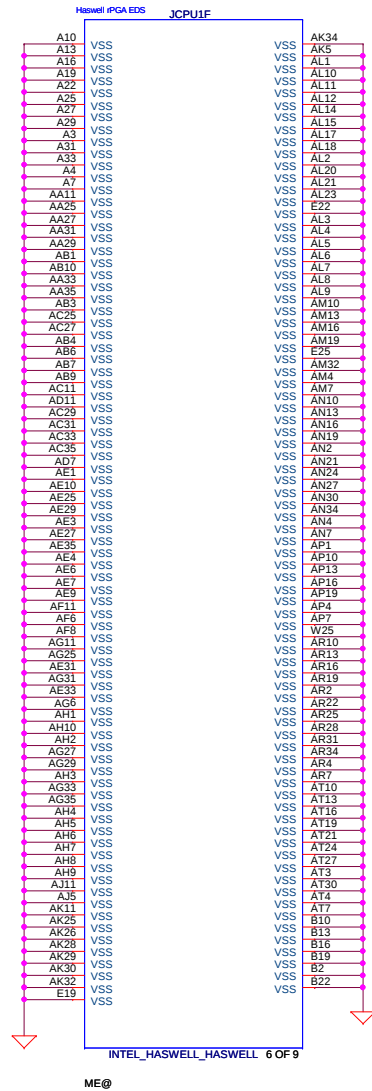
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





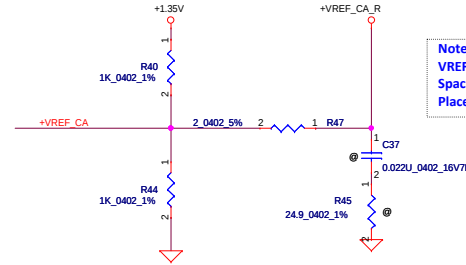
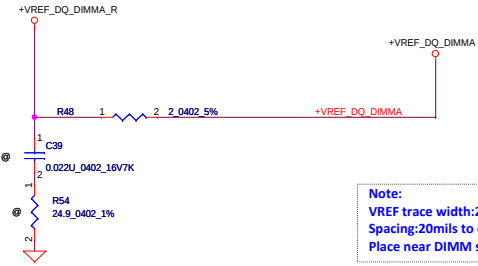
Note:
0 ohm Resistor should be placed
close to CPU



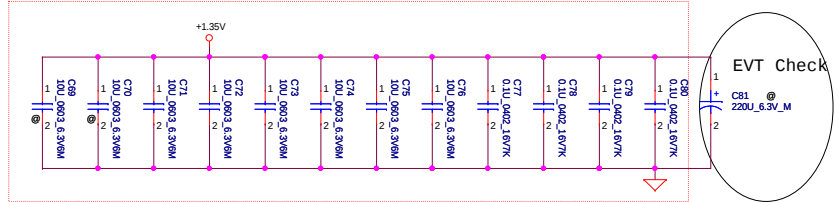




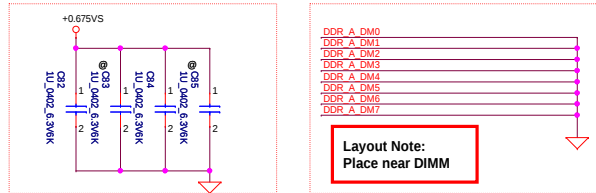
<7> DDR_A_D[0..63]
 <7> DDR_A_DQS[0..7]
 <7> DDR_A_DQS#0..7
 <7> DDR_A_MA[0..15]



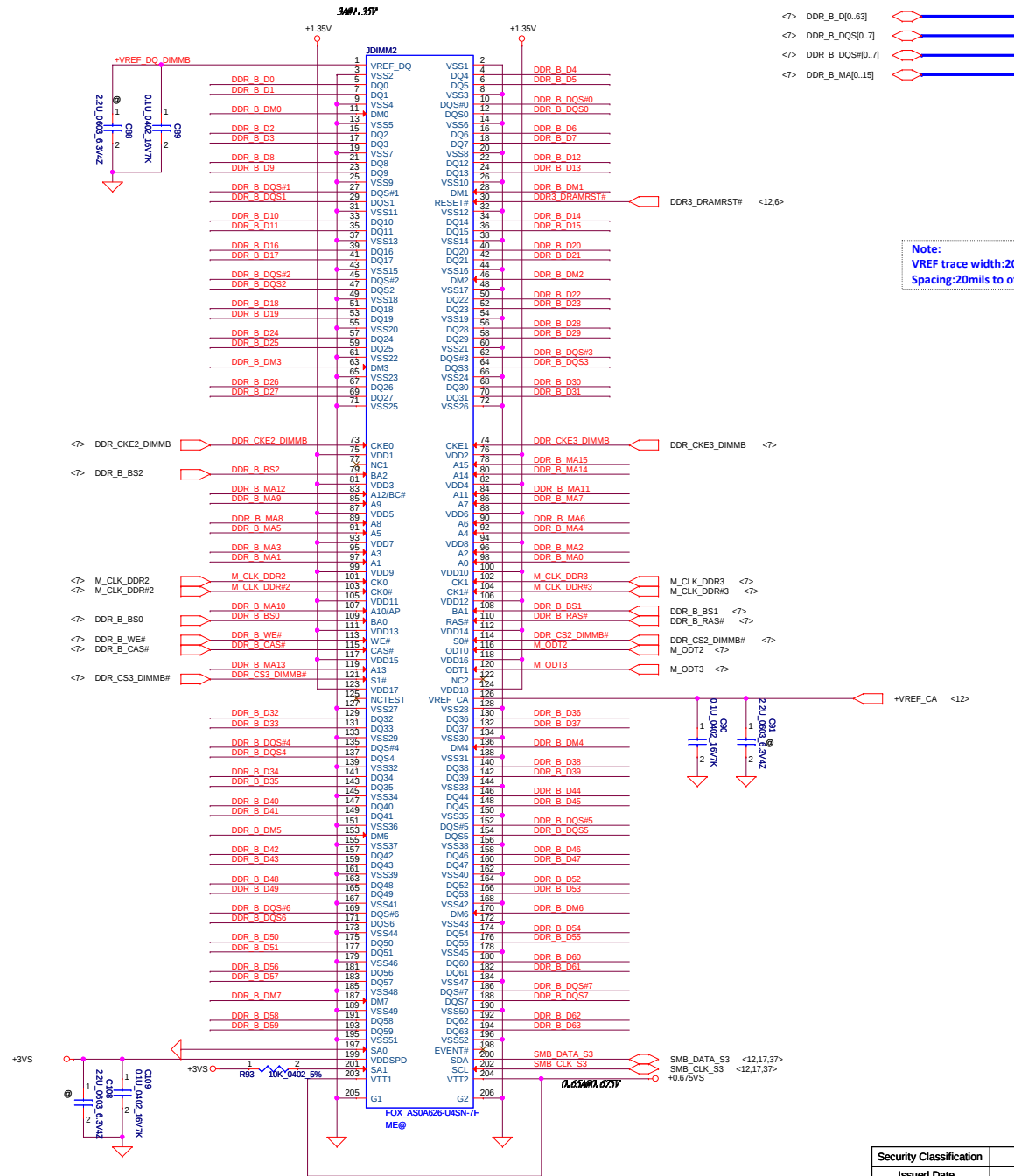
Layout Note:
 Place near DIMM



Layout Note:
 Place near DIMM



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Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes

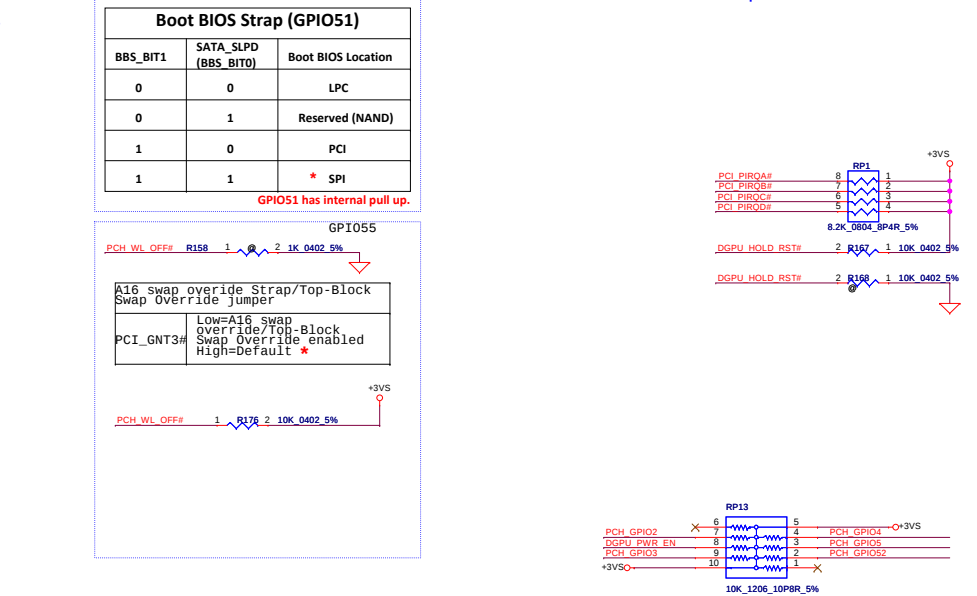
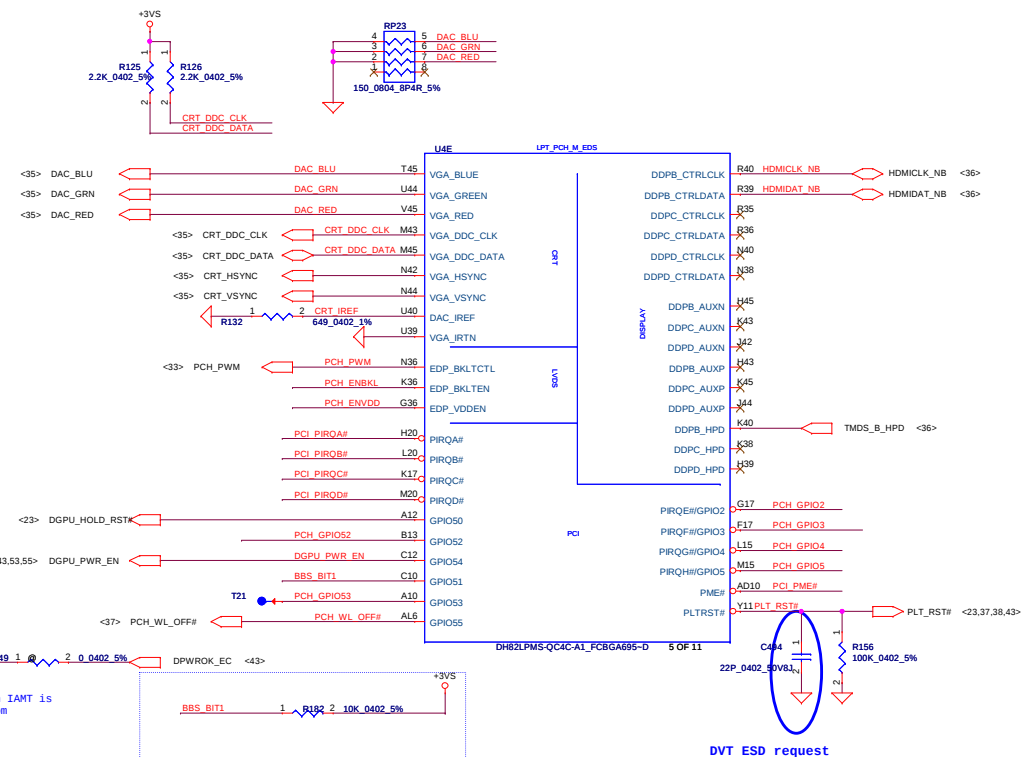
Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

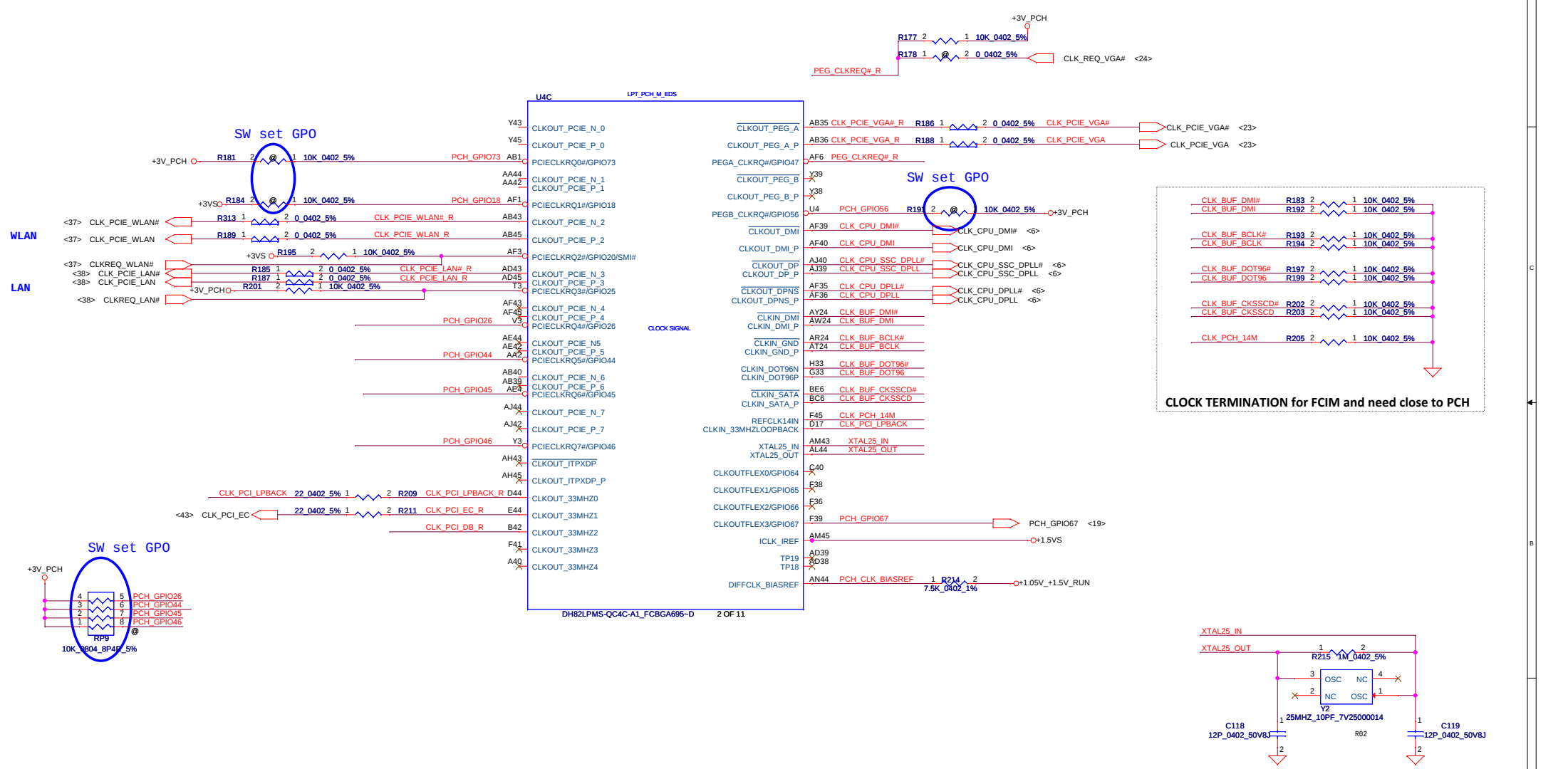
Layout Note:
Place near DIMM

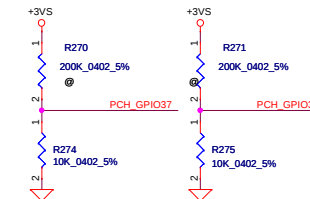
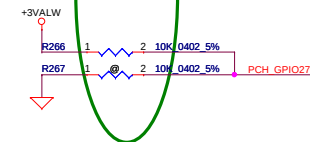
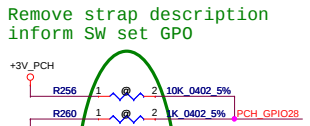
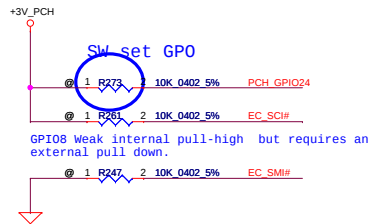
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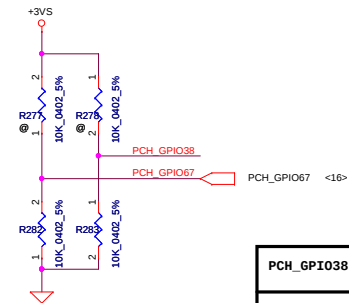


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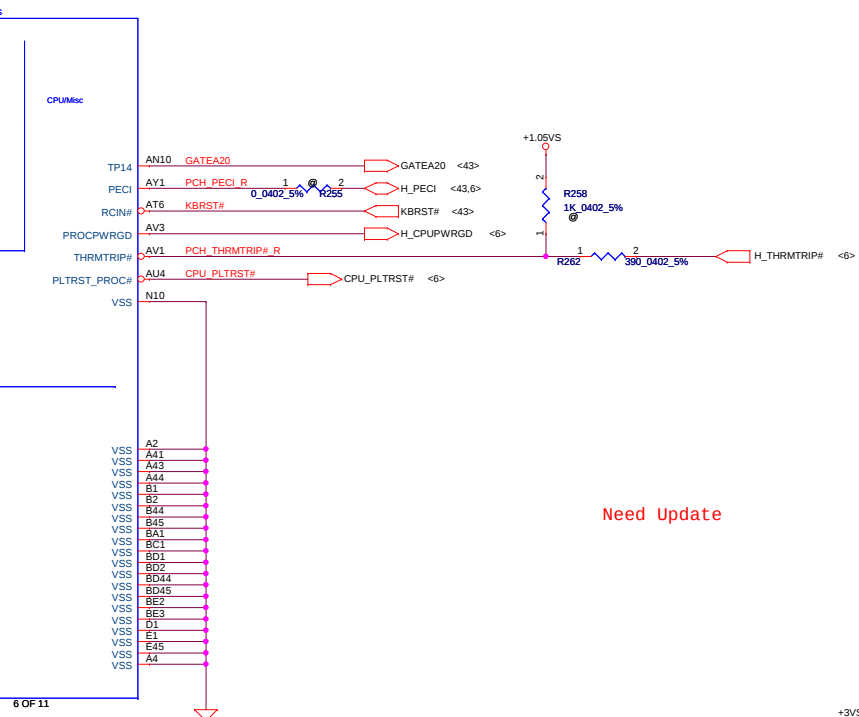
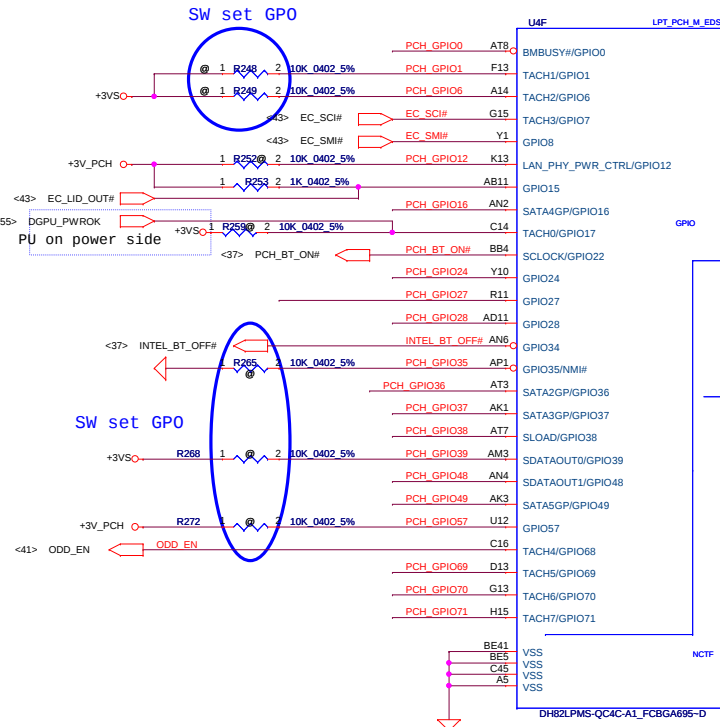
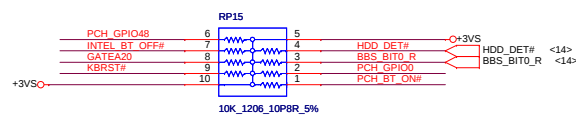




BIOS Request SKU ID

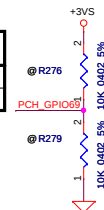


PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	DIS
1	1	UMA

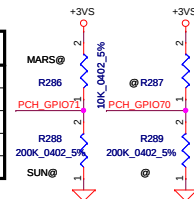


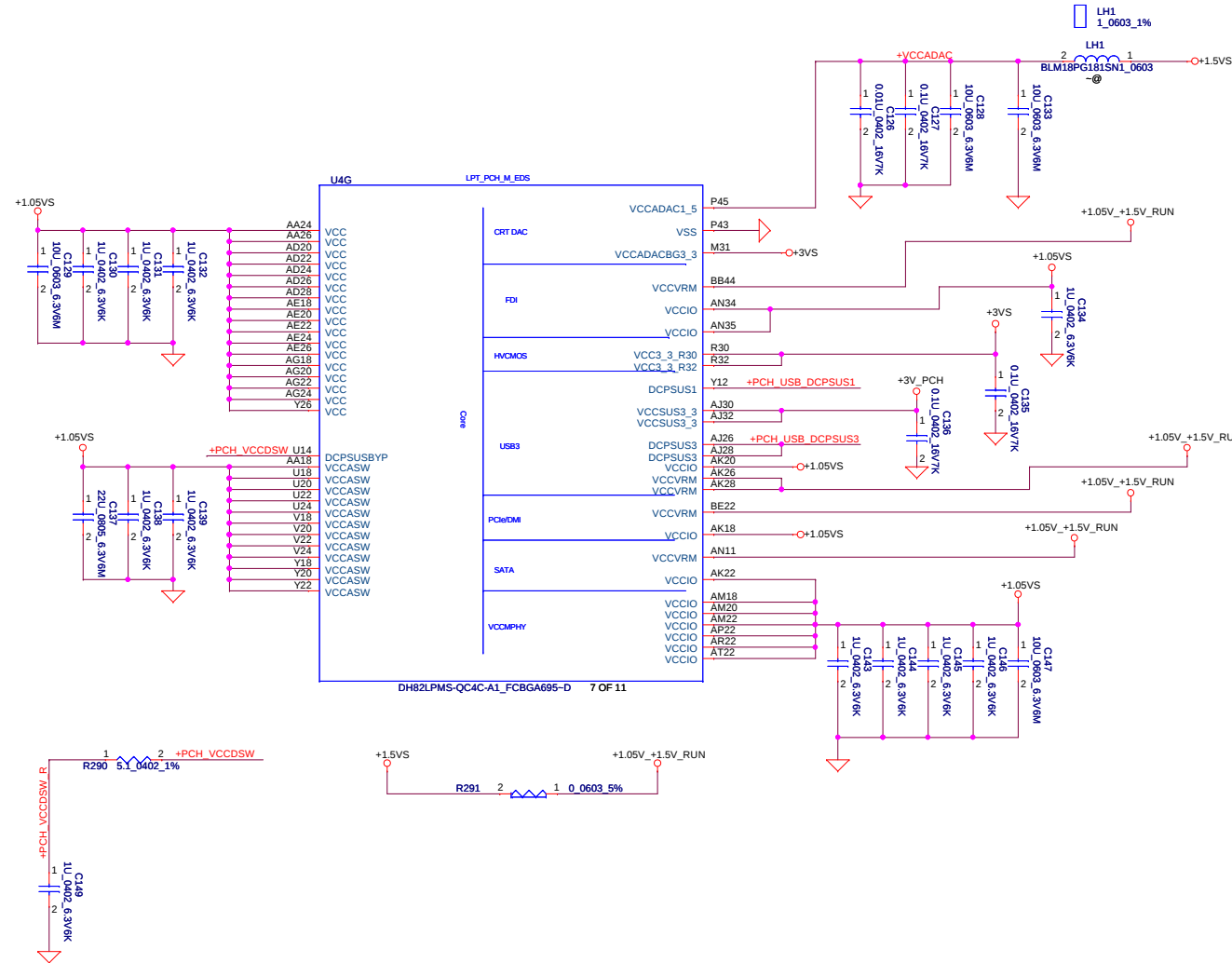
Need Update

PCH_GPIO69	Function
0	
1	

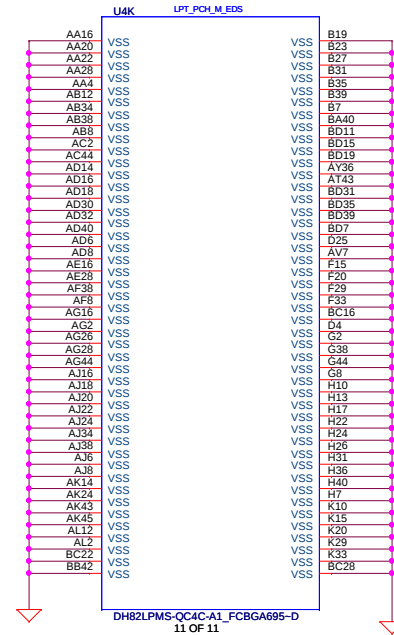
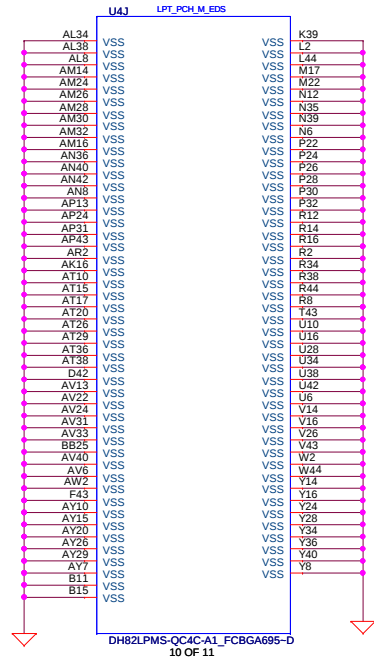


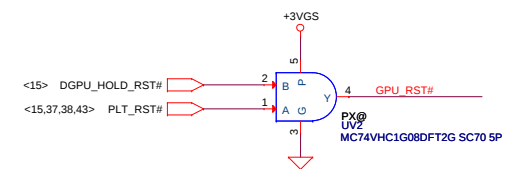
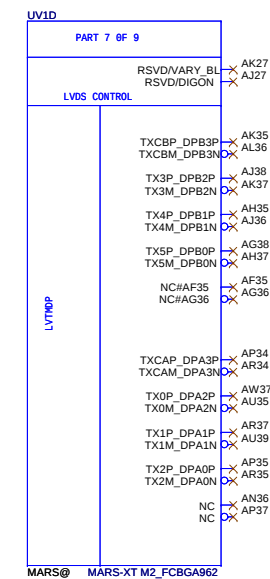
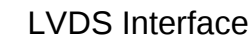
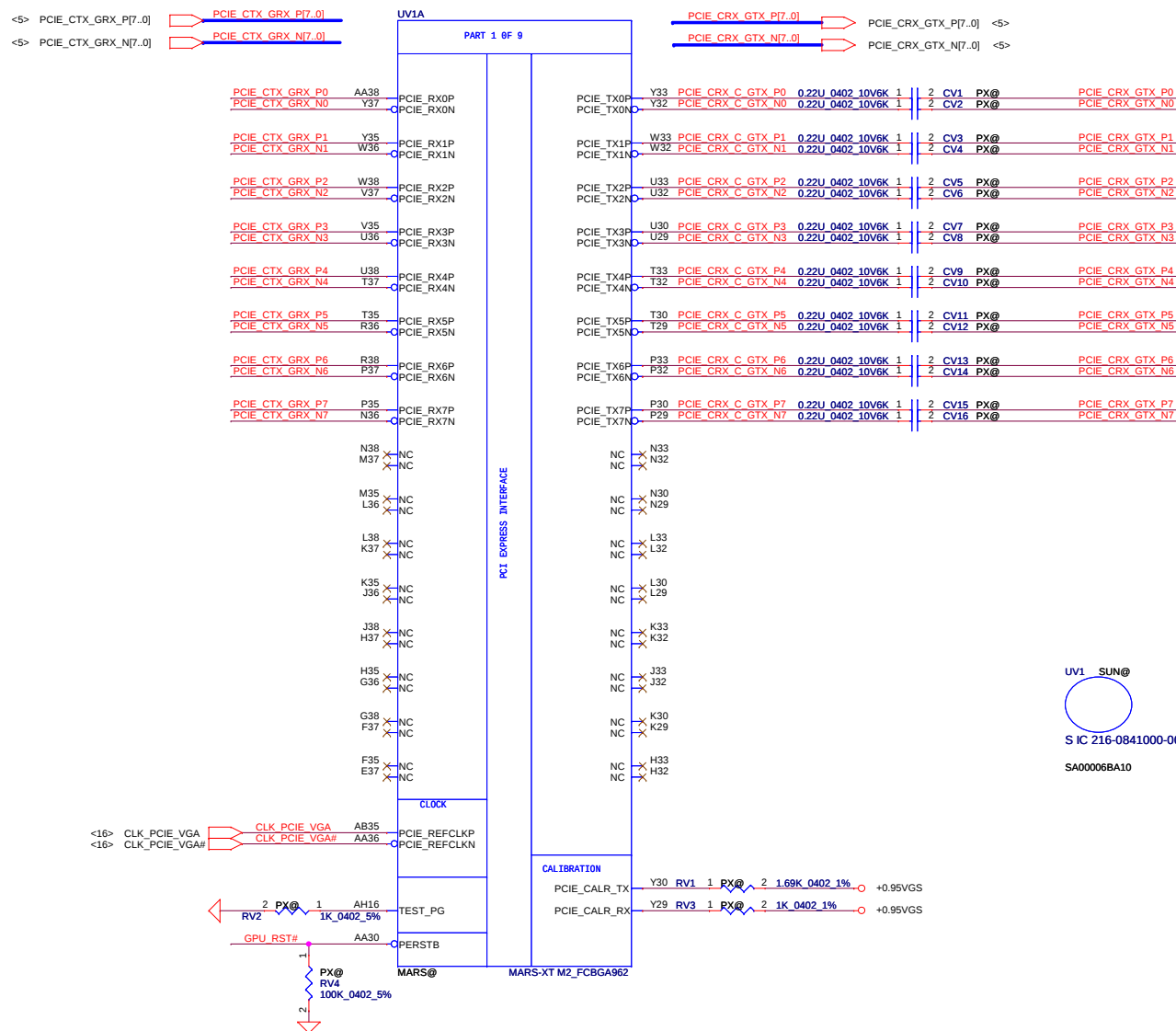
PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	SUN PRO
1	Mars XT



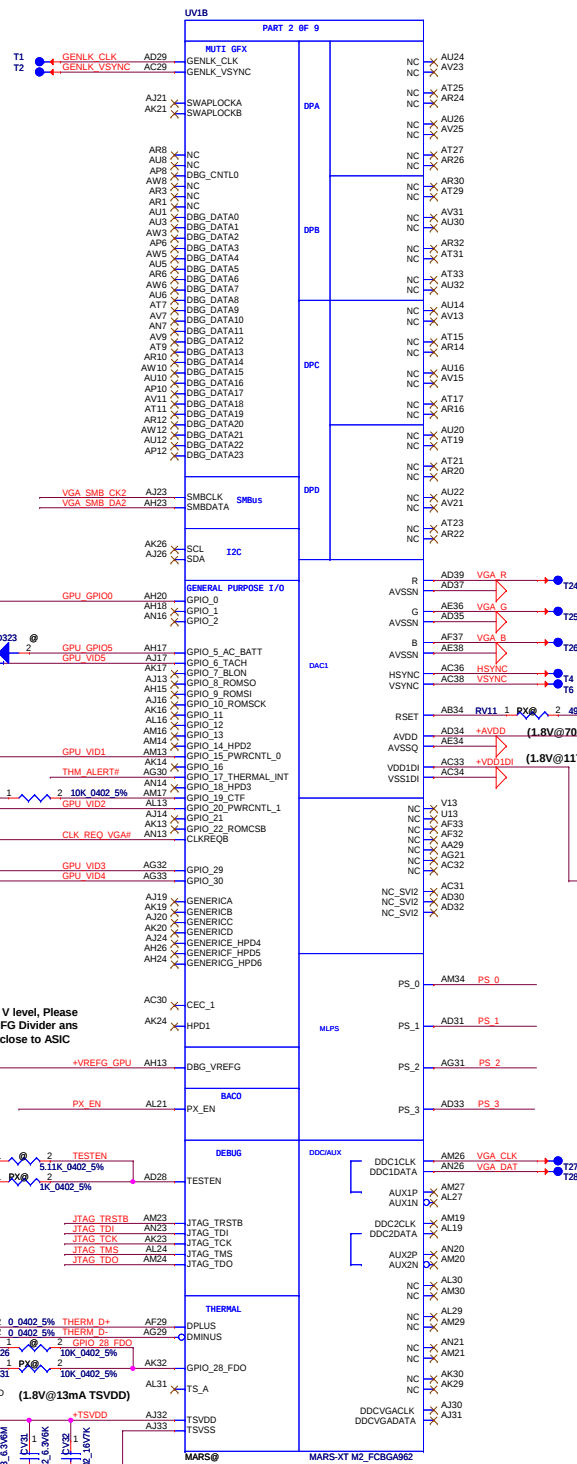


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A





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STRAPS



AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

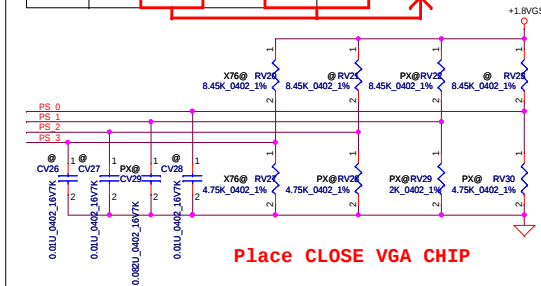
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	PS_1[4]	Transmitter Power Savings Enable 0.50m Tx output swing 1.Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0.Tx de-emphasis disabled 1.Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Seymour and should be strapped to 0) 0.GEN3 not support at power-on 1.GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0.VGA controller capacity enabled 1.VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100- 512Kbit M2SP05A (ST) 101- 1Mbit M2SP10A (ST) 101- 2Mbit M2SP20 (ST) 101- 4Mbit M2SP40 (ST) 101- 8Mbit M2SP80 (ST) 100- 512Kbit Pm2SLV010 (Chingis) 101- 1Mbit Pm2SLV010 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0.Disabled 1.Enabled	0
AUD[1]	NA	00- No audio function 01- Audio for DP only 10- Audio for DP and HDMI if dongle is detected 11- Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	NOT ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whisper/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_1[5:1]	0 1	0 0 1	82 nF	8.45K	2K
PS_2[5:1]	1 0	0 0 0	10 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

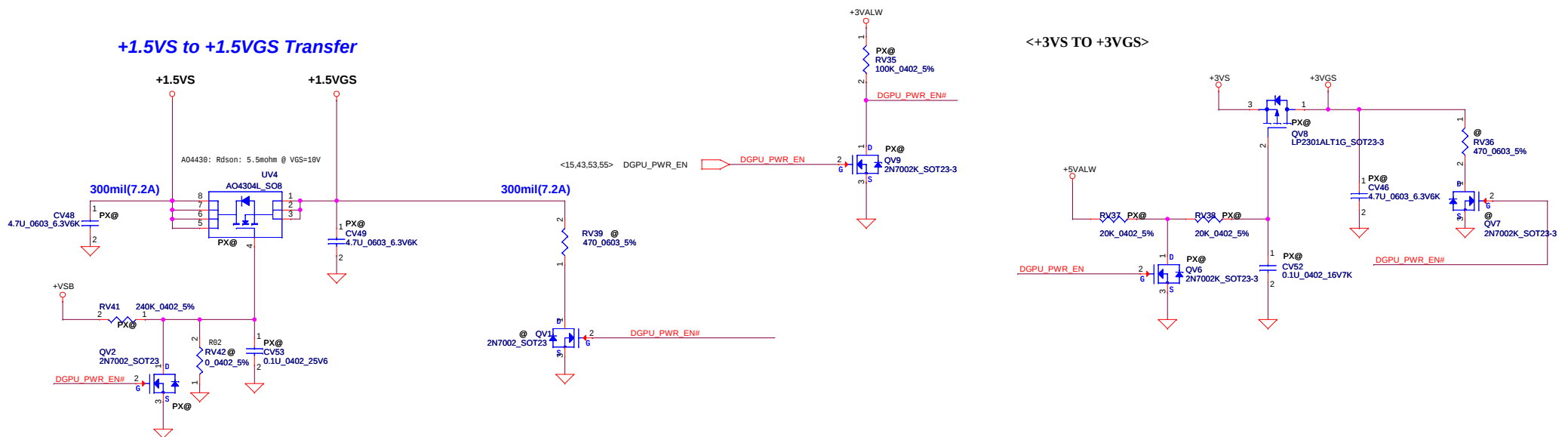
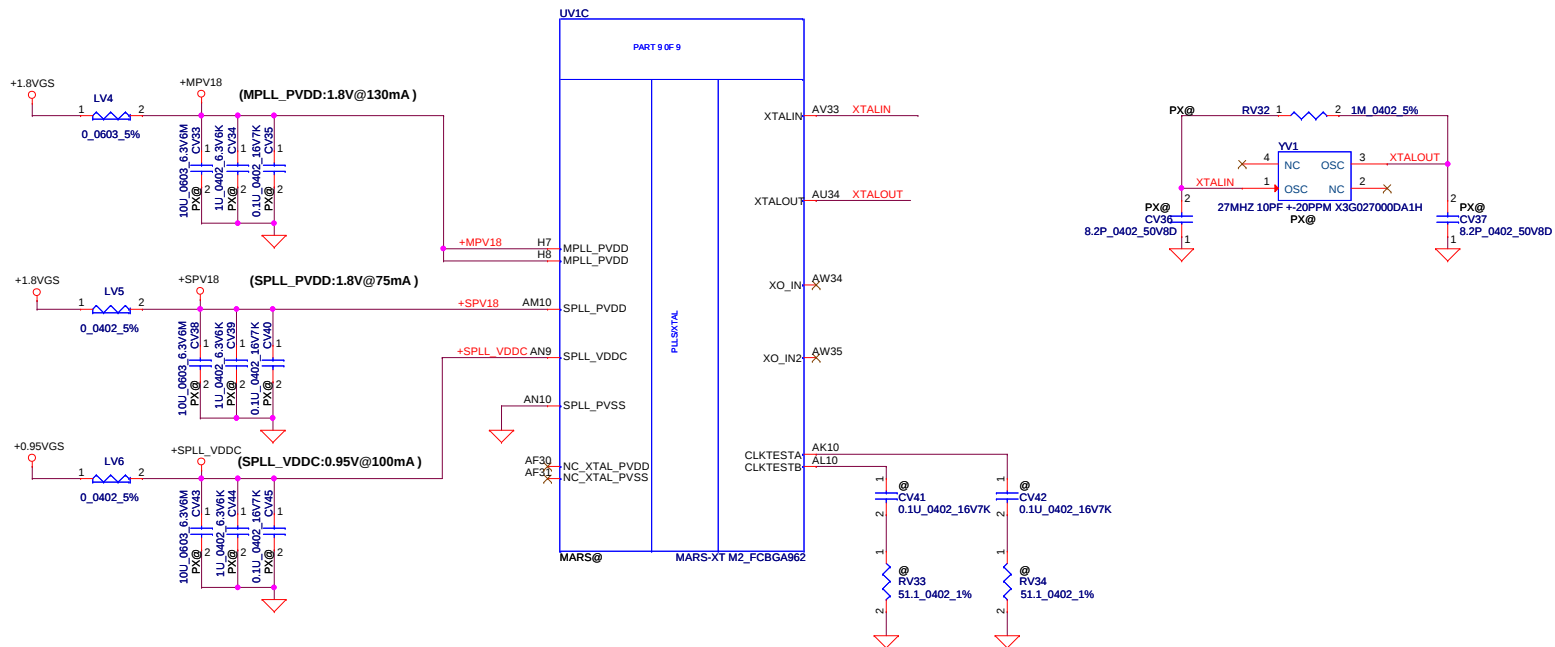
Mapping to VRAM type please refer to page 4



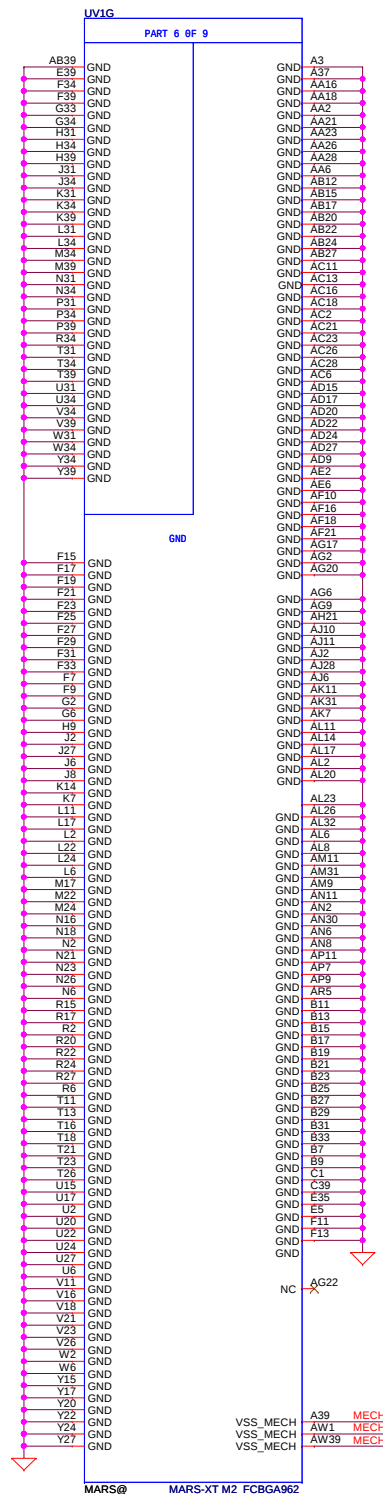
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

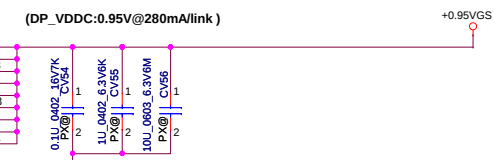
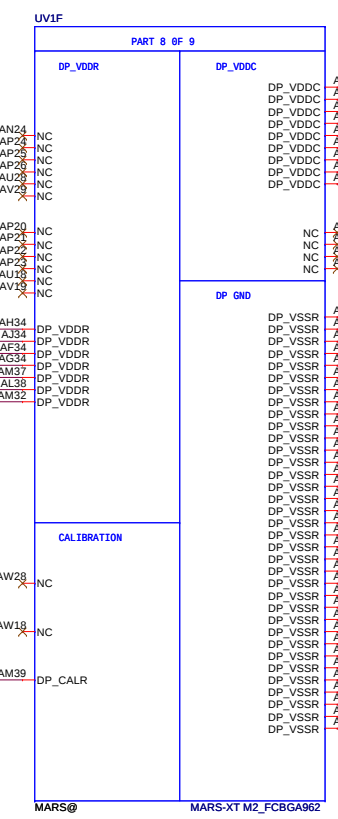
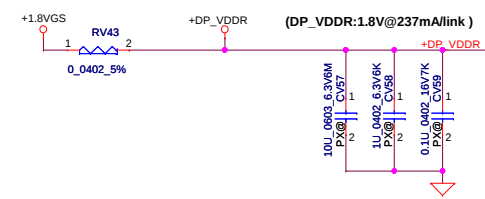
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



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				Custom	LA8642P M/B	0.3
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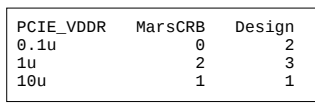
DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



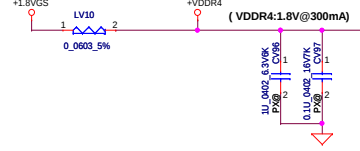
DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

VSS_MECH A39 MECH#1 TV12 PAD
VSS_MECH AW1 MECH#2 TV13 PAD
VSS_MECH AW39 MECH#3 TV14 PAD

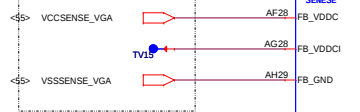
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						Part Number		Document Number		Rev	
						Custom		LA8642P M/B		0.3	
						Date:		Wednesday, March 06, 2013		Sheet 26 of 61	



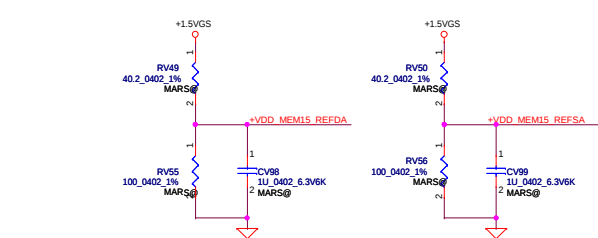
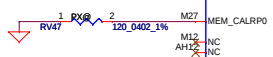
VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



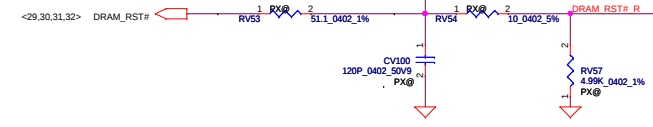
Route as differential pair



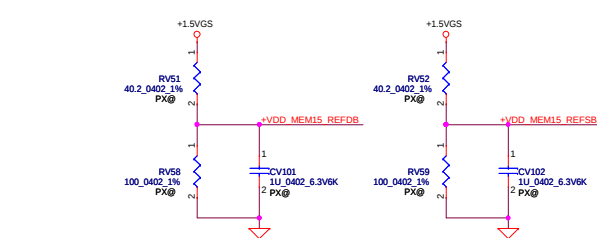
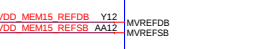
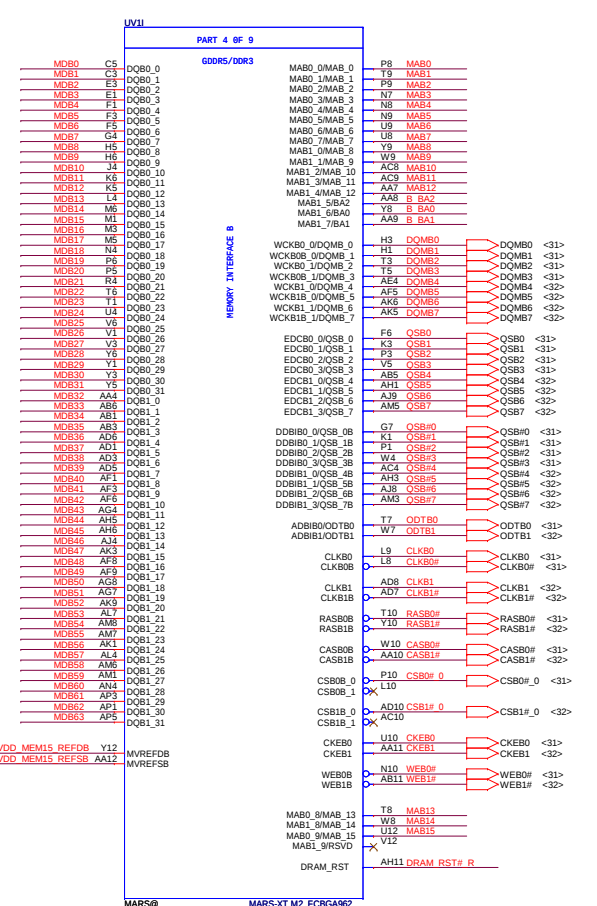
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				Size		Document Number		Rev	
				C		LA8642P M/B		0.3	
				Date:		Wednesday, March 06, 2013		Sheet 27 of 61	



Ball to RV57 < 1"
 CV100 to RV57 < 200 mil
 CV100 to RV53 < 1"



DRAM_RST# is a daisy-chain net that connects to all VRAM
 This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.
 Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2



<28> MDA[0..31]

<28..30> MAA[15..0]

CLKA0_1 MARS@ 40.2_0402_1%

CLKA0#_1 MARS@ 40.2_0402_1%

CV195 0.01u 0402_16V7K MARS@

CV196 0.01u 0402_16V7K MARS@

CV197 0.01u 0402_16V7K MARS@

CV198 0.01u 0402_16V7K MARS@

CV199 0.01u 0402_16V7K MARS@

CV200 0.01u 0402_16V7K MARS@

CV201 0.01u 0402_16V7K MARS@

CV202 0.01u 0402_16V7K MARS@

CV203 0.01u 0402_16V7K MARS@

CV204 0.01u 0402_16V7K MARS@

CV205 0.01u 0402_16V7K MARS@

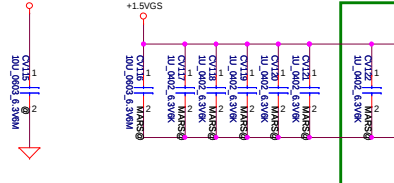
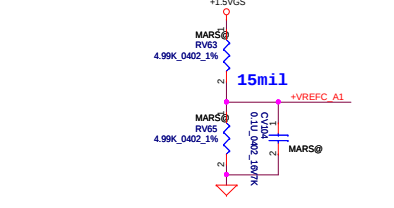
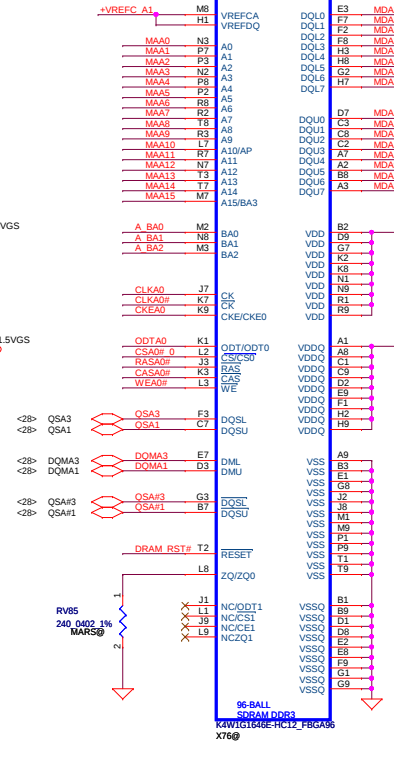
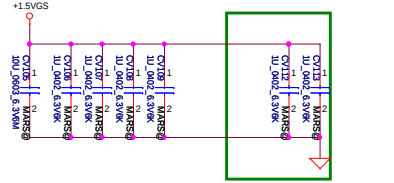
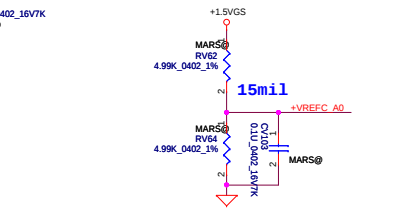
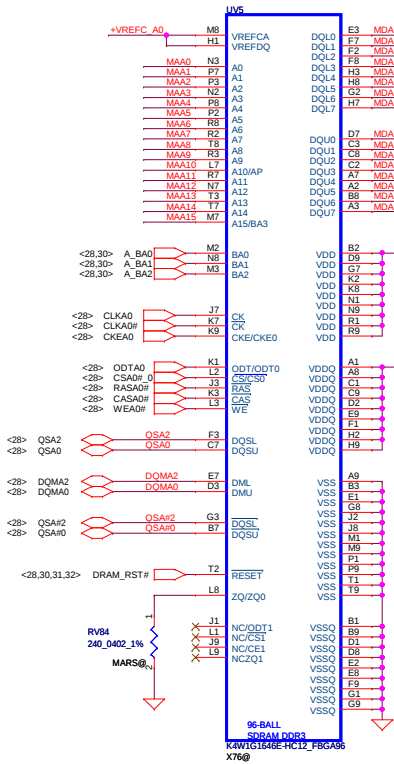
CV206 0.01u 0402_16V7K MARS@

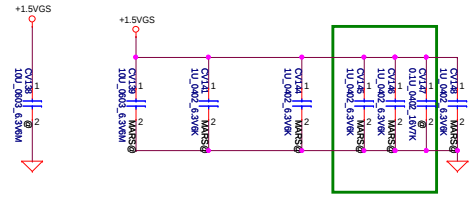
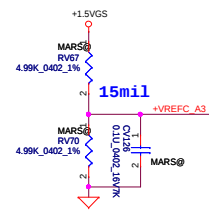
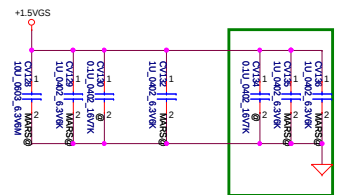
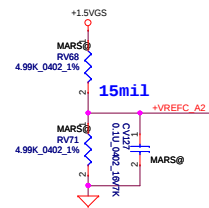
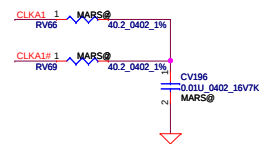
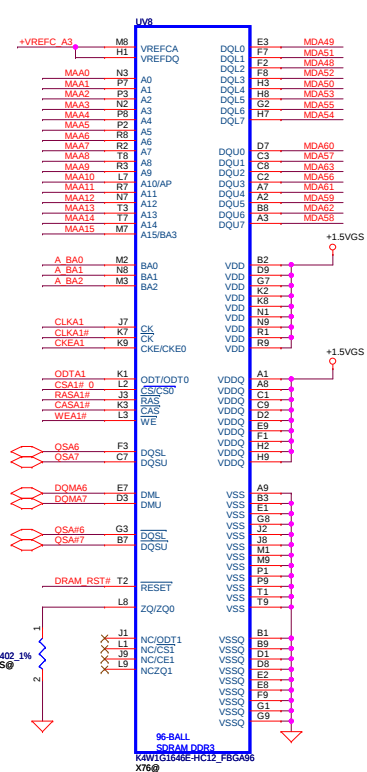
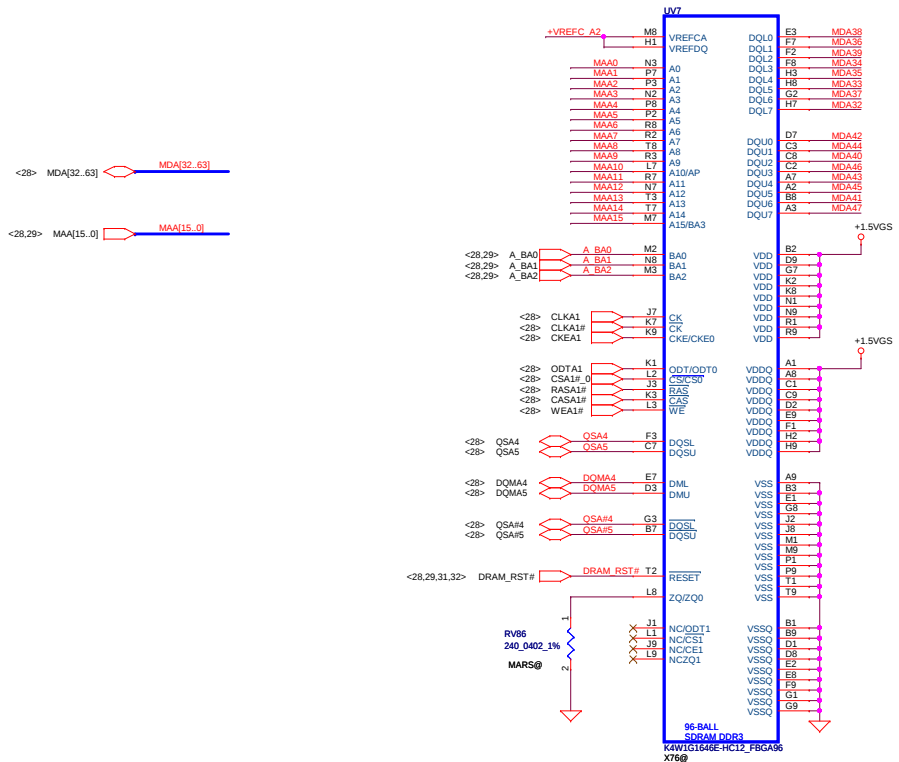
CV207 0.01u 0402_16V7K MARS@

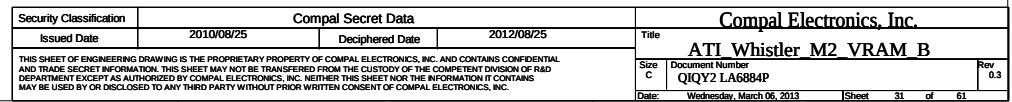
CV208 0.01u 0402_16V7K MARS@

CV209 0.01u 0402_16V7K MARS@

CV210 0.01u 0402_16V7K MARS@

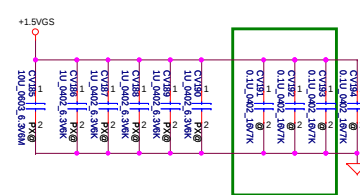
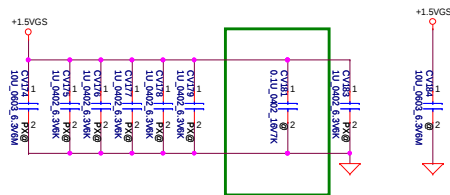
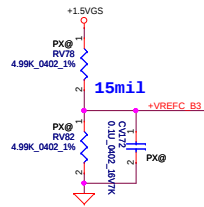
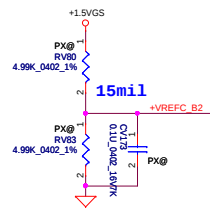
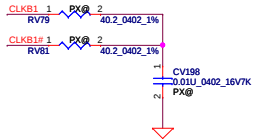
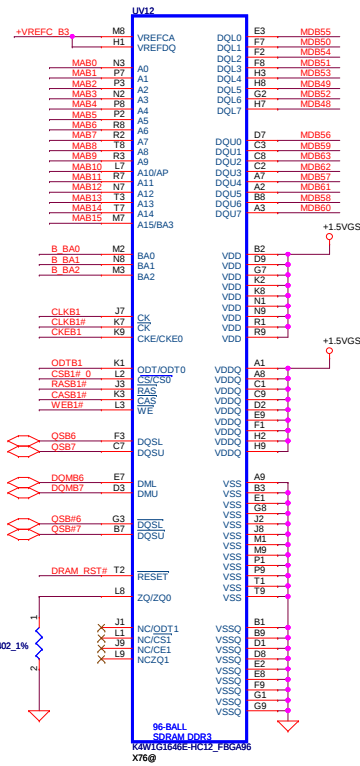
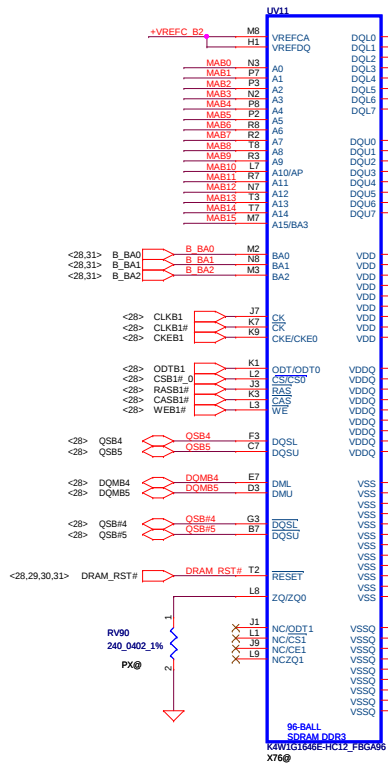






<28> MDB[32..63]

<28.31> MAB[15..0]

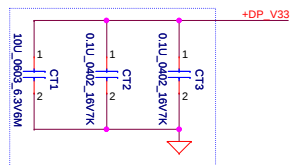




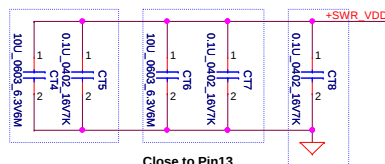
RTD2132R LDO MODE



Close to Pin3

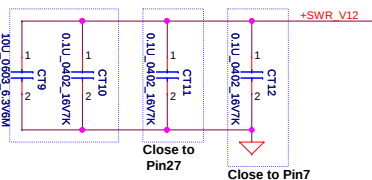


Close to pin11



Close to Pin13

Close to LT3



Close to Pin27

Close to Pin7

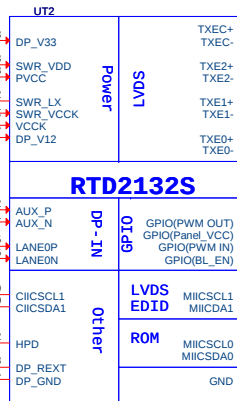
 EDP_CPU_AUX
 EDP_CPU_AUX#
 EDP_CPU_LANE_P0
 EDP_CPU_LANE_N0

C190 1 2 0.1u 0402 16V7K
C191 1 2 0.1u 0402 16V7K
C192 1 2 0.1u 0402 16V7K
C193 1 2 0.1u 0402 16V7K

EDP_CPU_AUX R
EDP_CPU_AUX# R
EDP_CPU_LANE_P0 R
EDP_CPU_LANE_N0 R

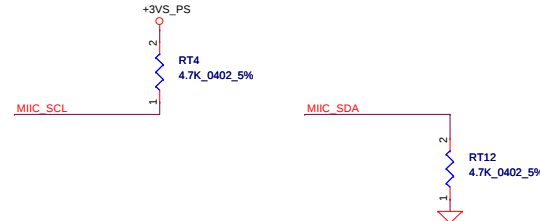
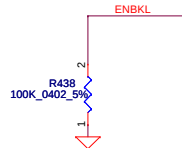
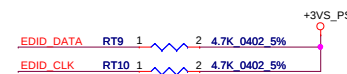
<17,24,40,43> EC_SMB_CK2
<17,24,40,43> EC_SMB_DA2

 TL_HPD



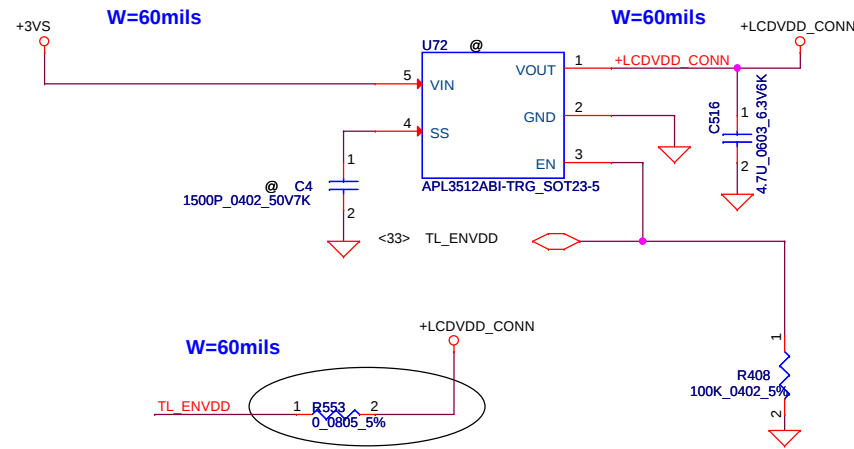
TL_ENVDD need 60 mil if use for LVDS power on R version

ADD TP on trace or via

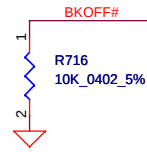


MIIC_SCL \ MIIC_SDA	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

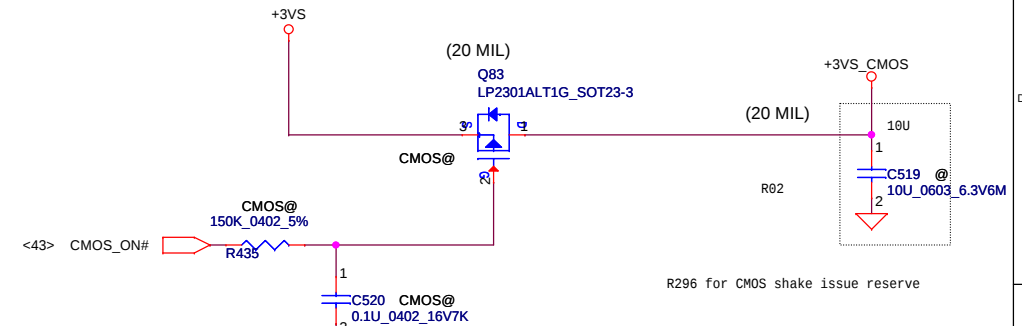
LCD POWER CIRCUIT



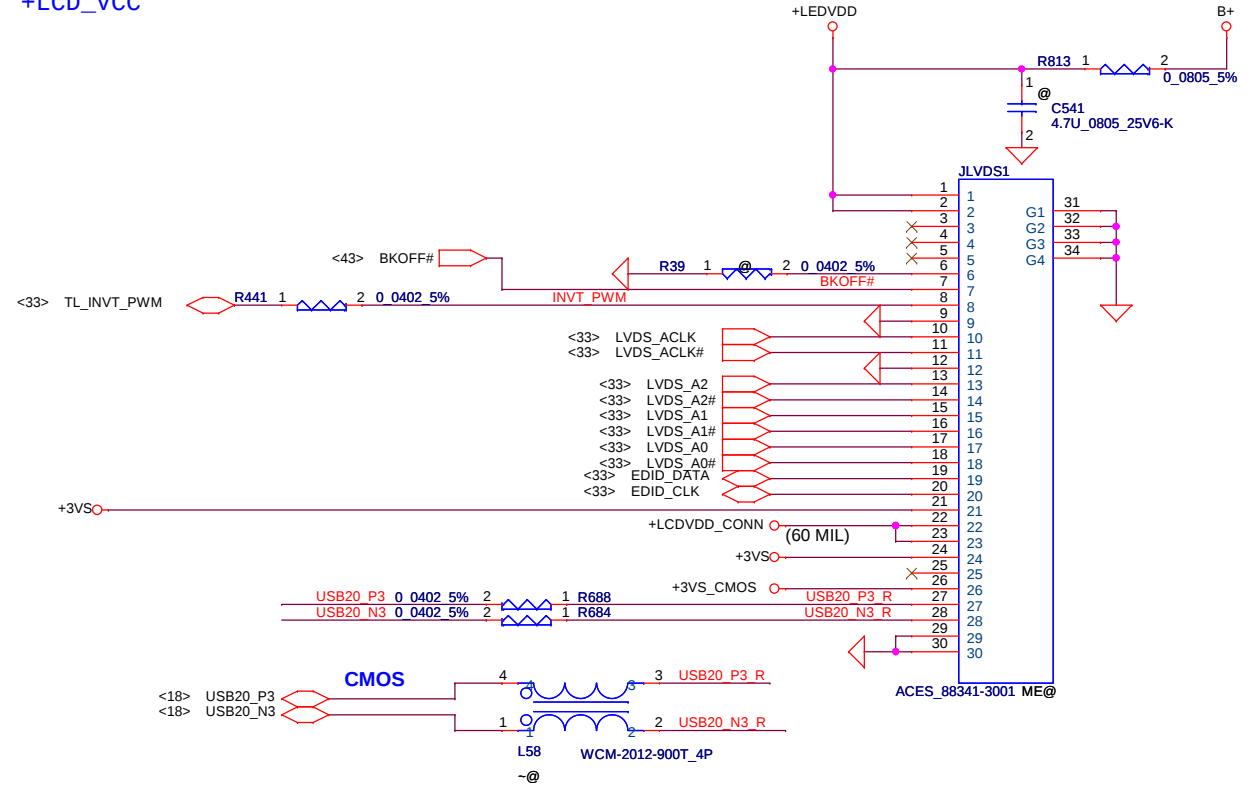
RTD2132R Internal load switch for +LCD_VCC



CMOS Camera

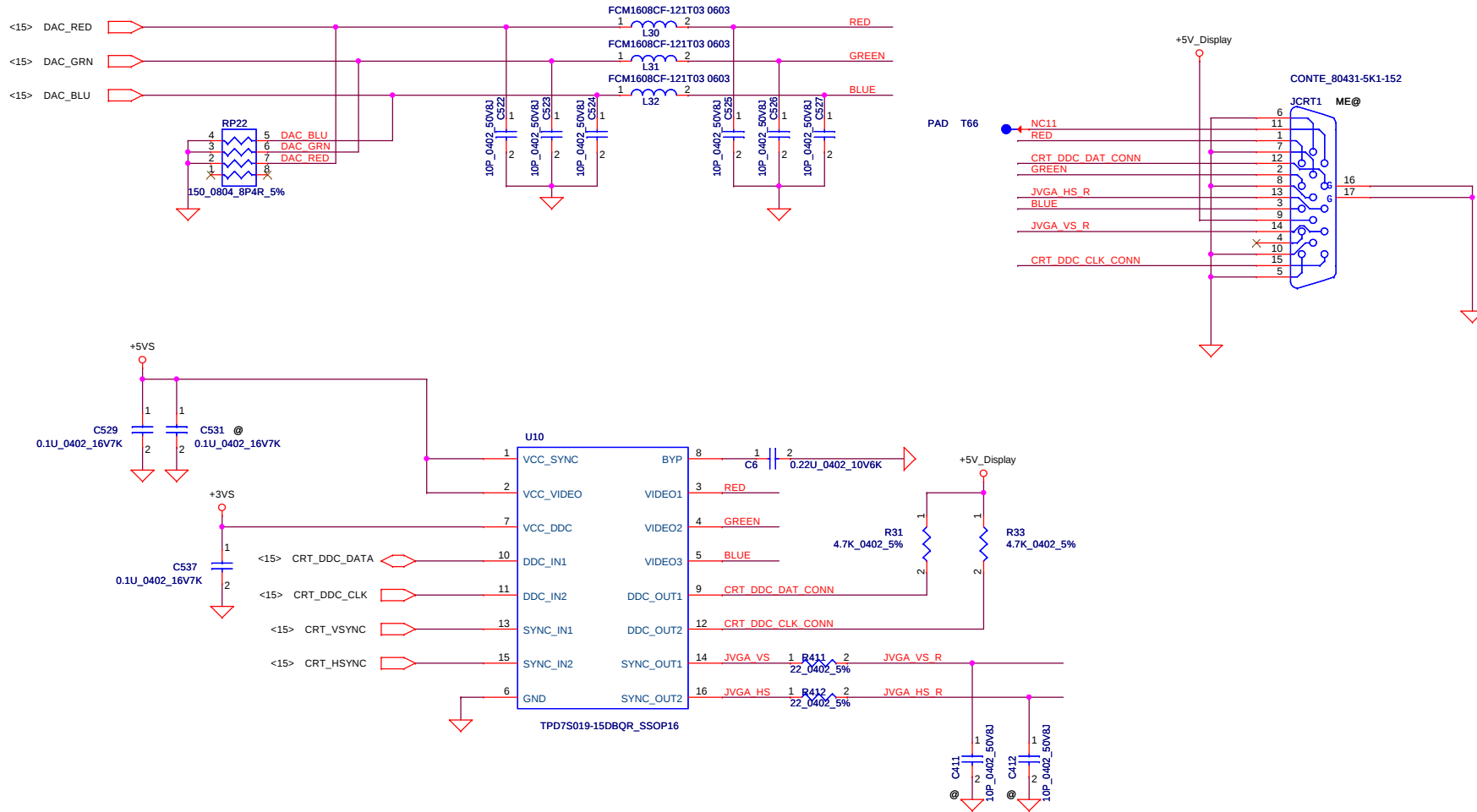


VGA LCD/PANEL BD. Conn.

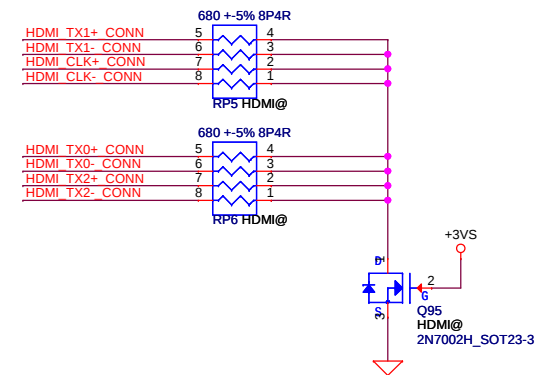
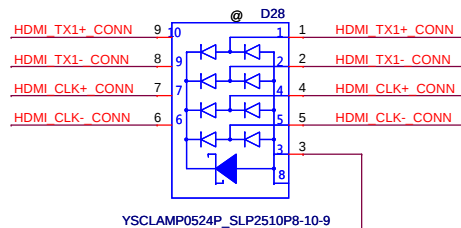


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				Custom	0.3
				Date:	Wednesday, March 06, 2013
				Sheet	34 of 61

CRT Connector

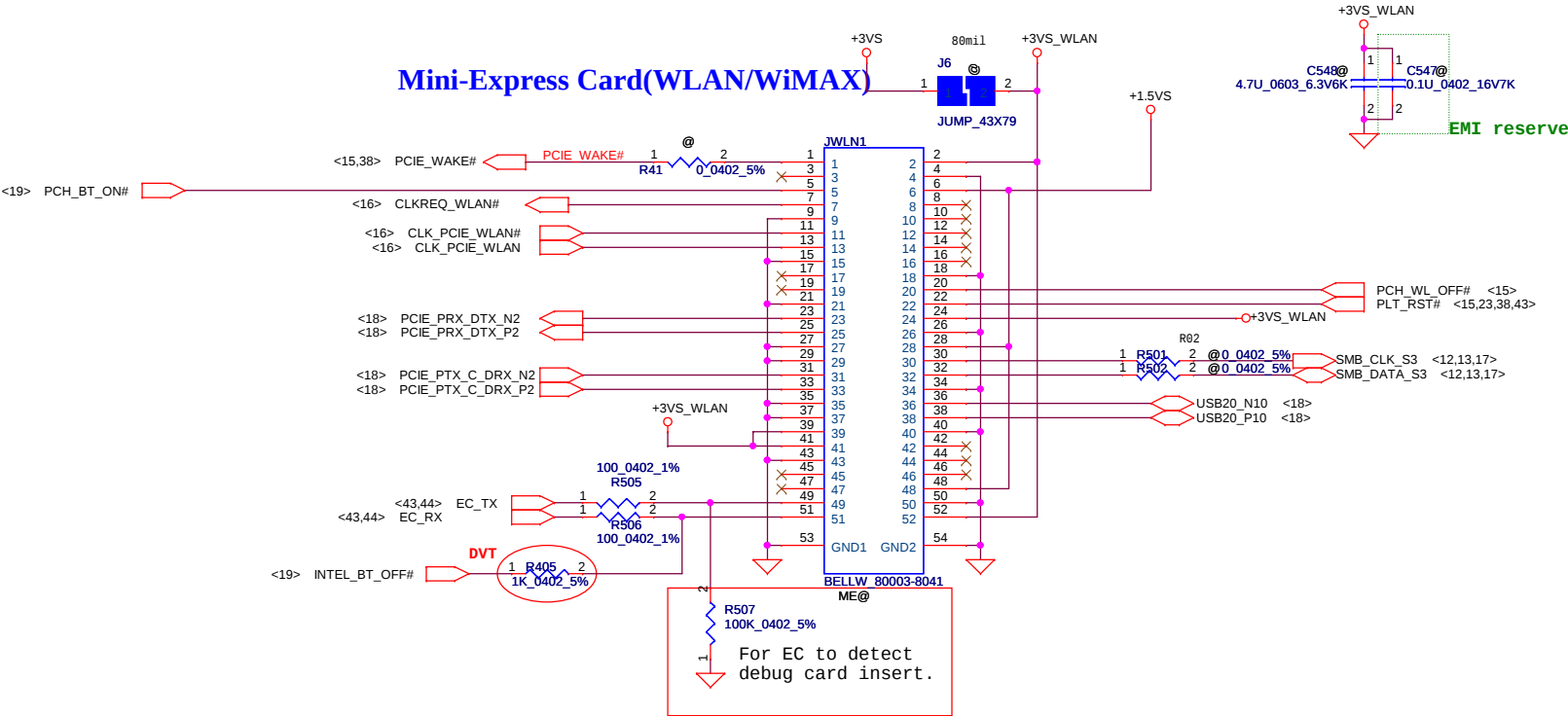


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Size	Custom	Document Number	LA-9641P	Rev	0.3
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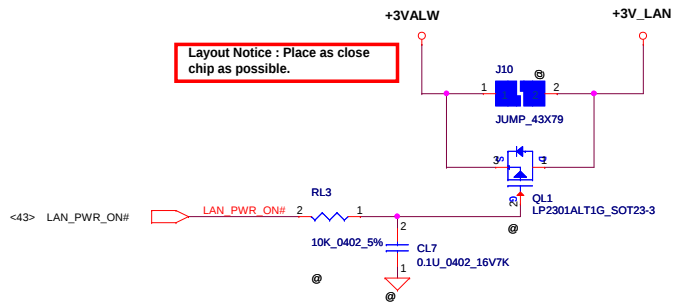


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				A	LA-9641P	0.3
				Date:	Wednesday, March 06, 2013	Sheet 36 of 61

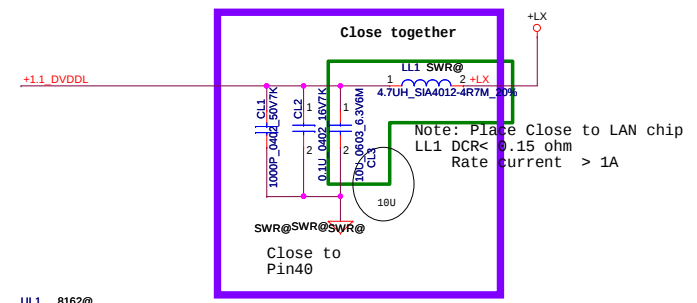
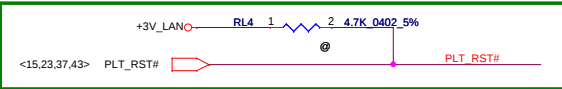
Mini-Express Card for WLAN/WiMAX(Half)



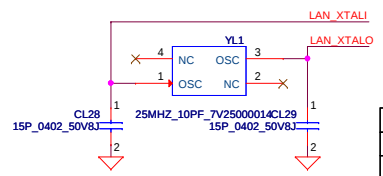
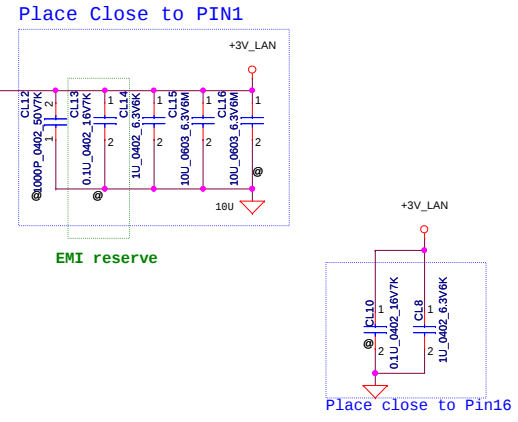
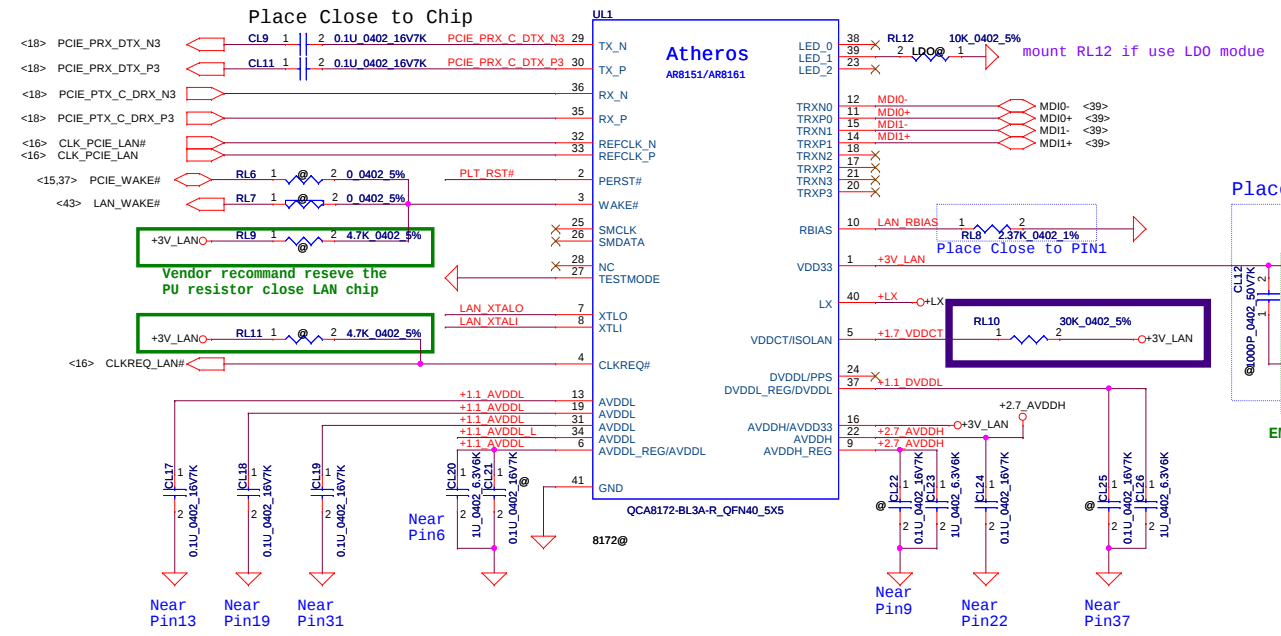
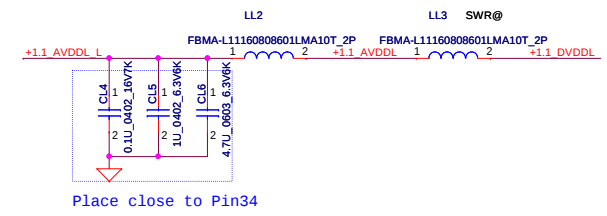
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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Vendor recommend reseve the PU resistor close LAN chip



SA000065410 S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL
SA000052J20 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL



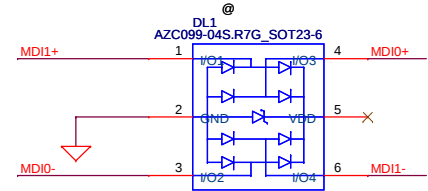
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	LAN-AR8162/8172
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				Date	Wednesday, March 06, 2013
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Place Close to TL1

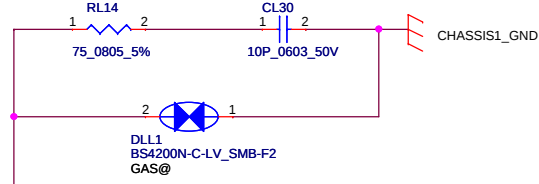
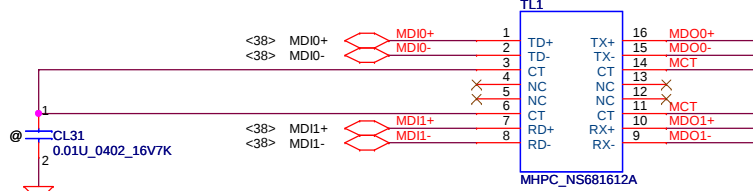
DL1

1'S PN:SC300001G00

2'S PN:SC300002E00

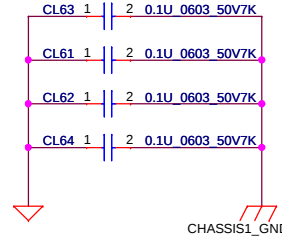
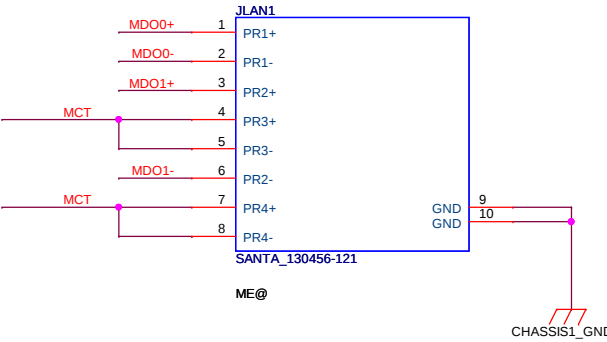


Reserve gas tube for EMI go rural solution

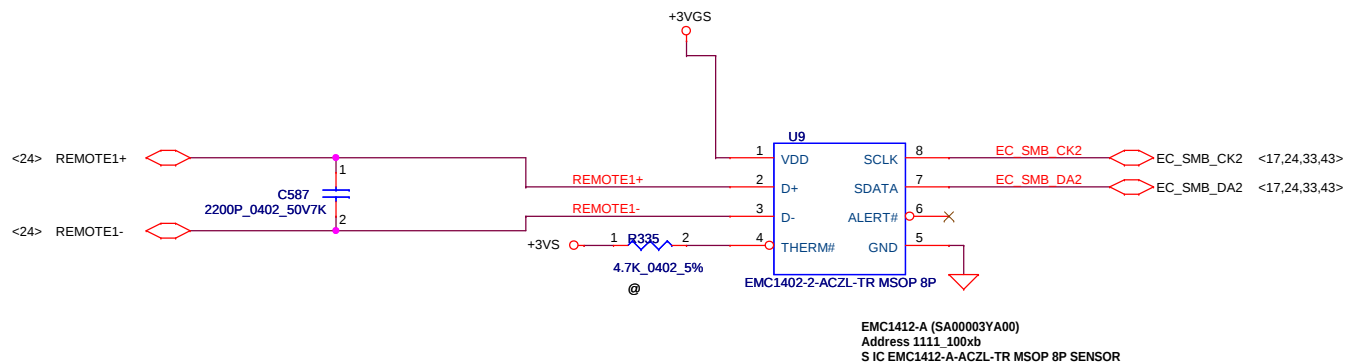


Place Close to TL1

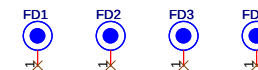
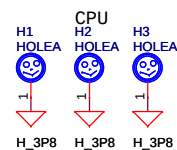
Need check Symbol1



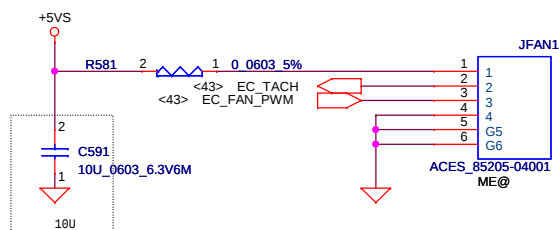
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn

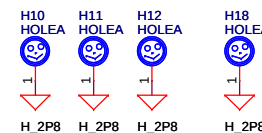
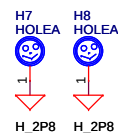


A

B

M/B 橢圓孔

M/B 圓孔



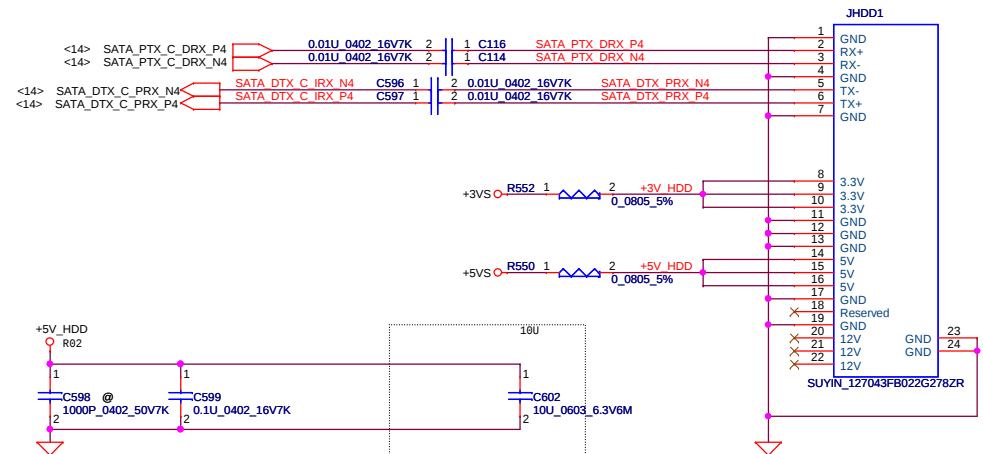
2P8 * 7 pcd

D

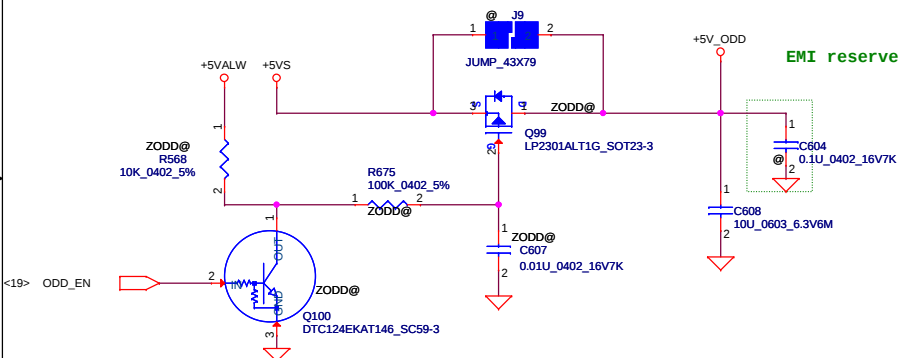
E

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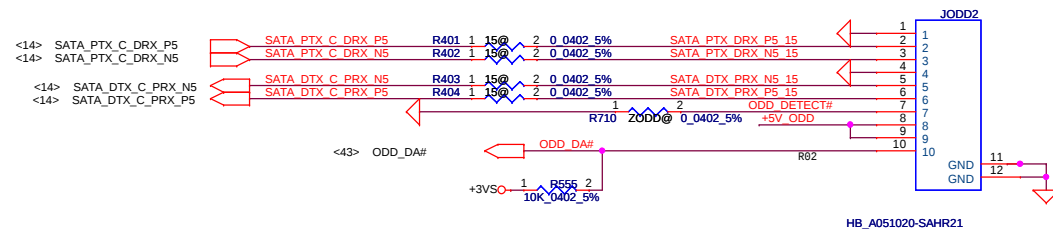
SATA HDD Conn.



ODD Power Control

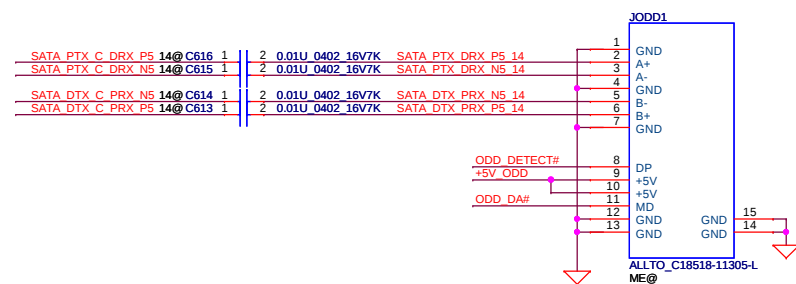


FOR 15" SATA ODD FFC Conn.



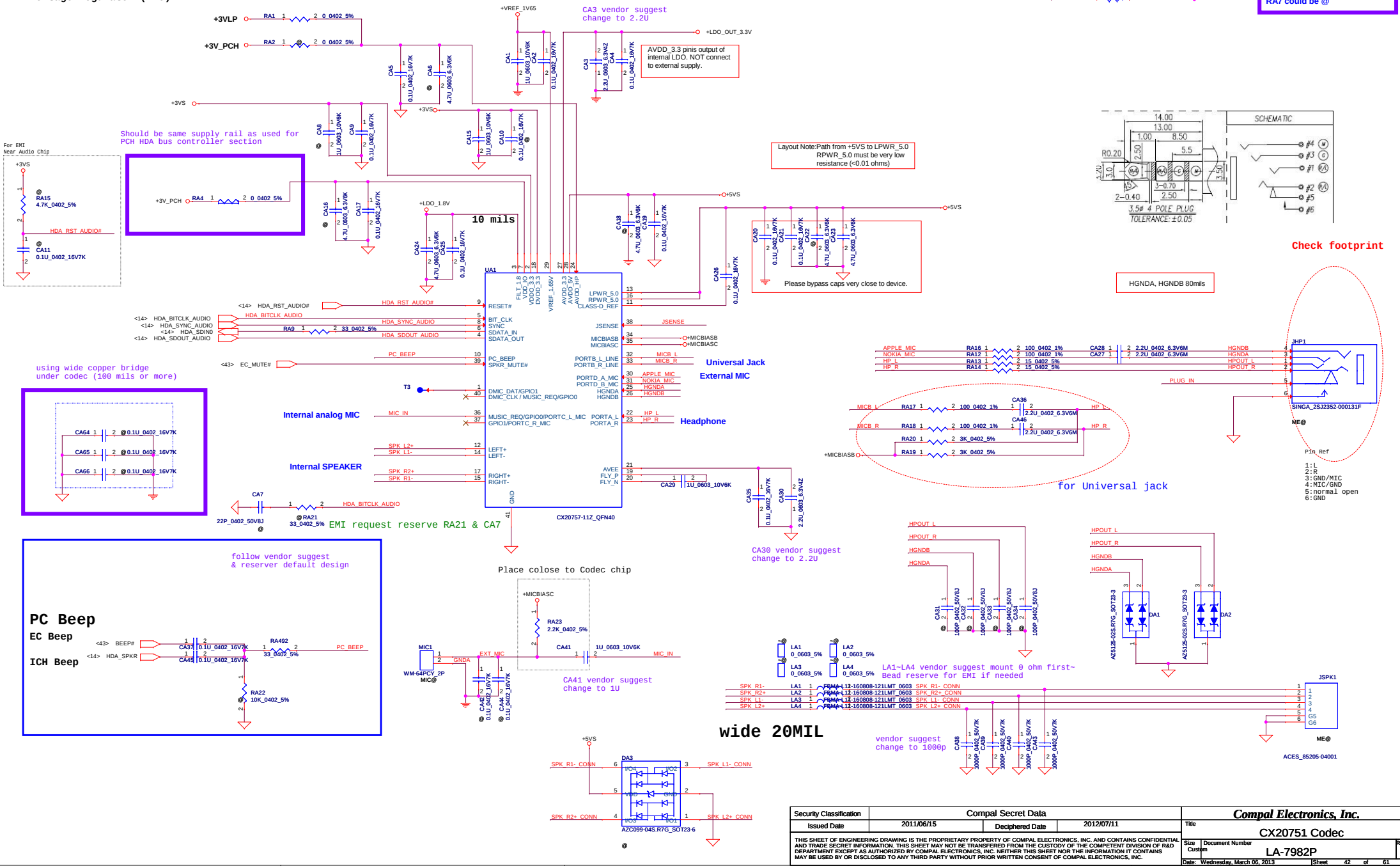
Co-lay

FOR 14" SATA ODD Conn.

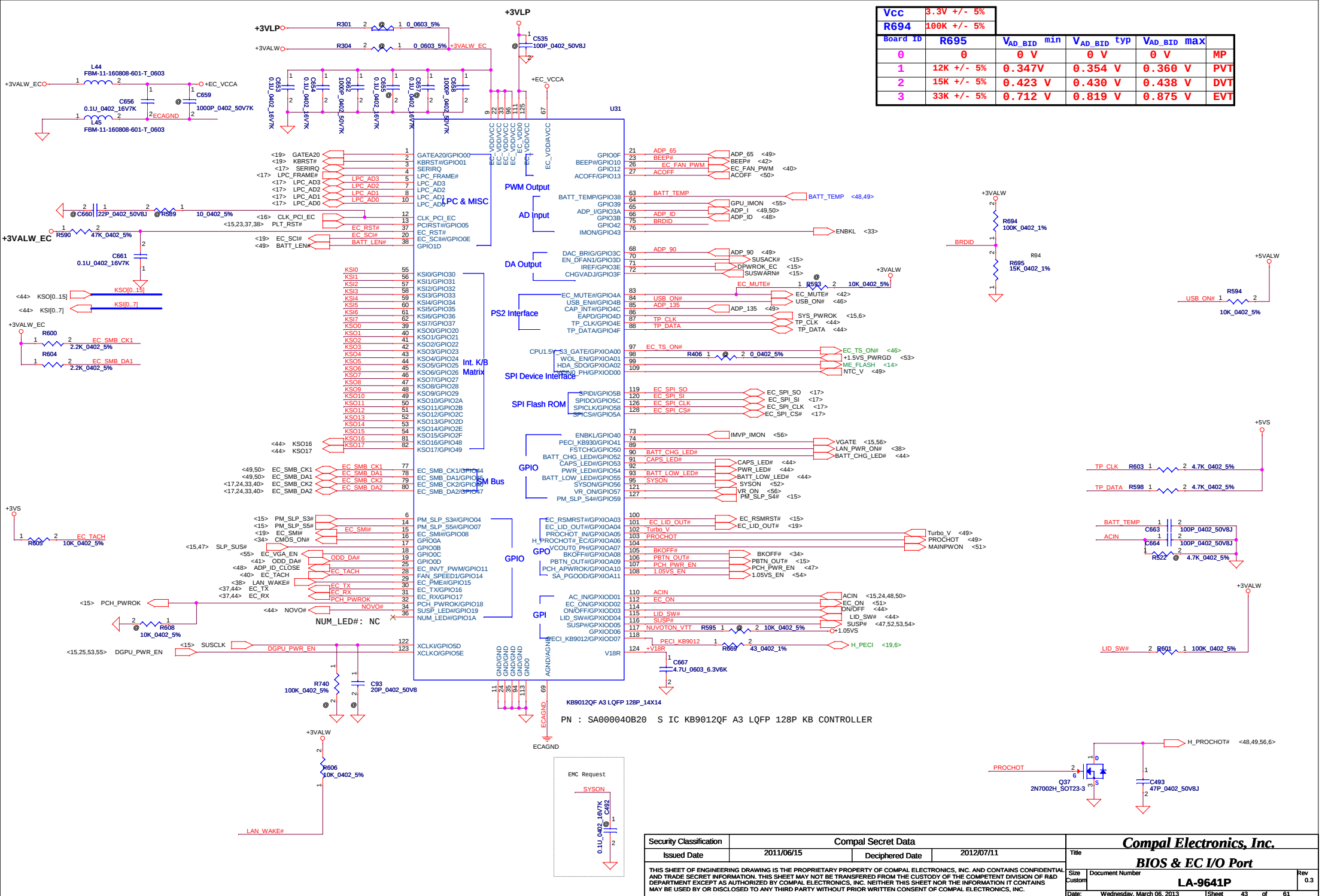


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				Custom	0.3
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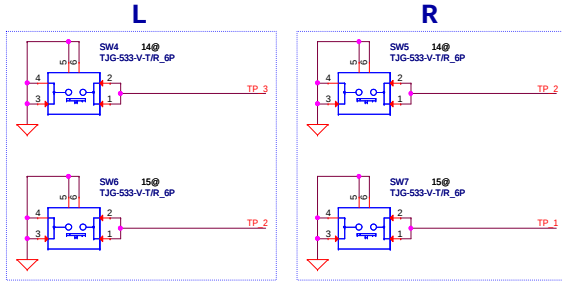
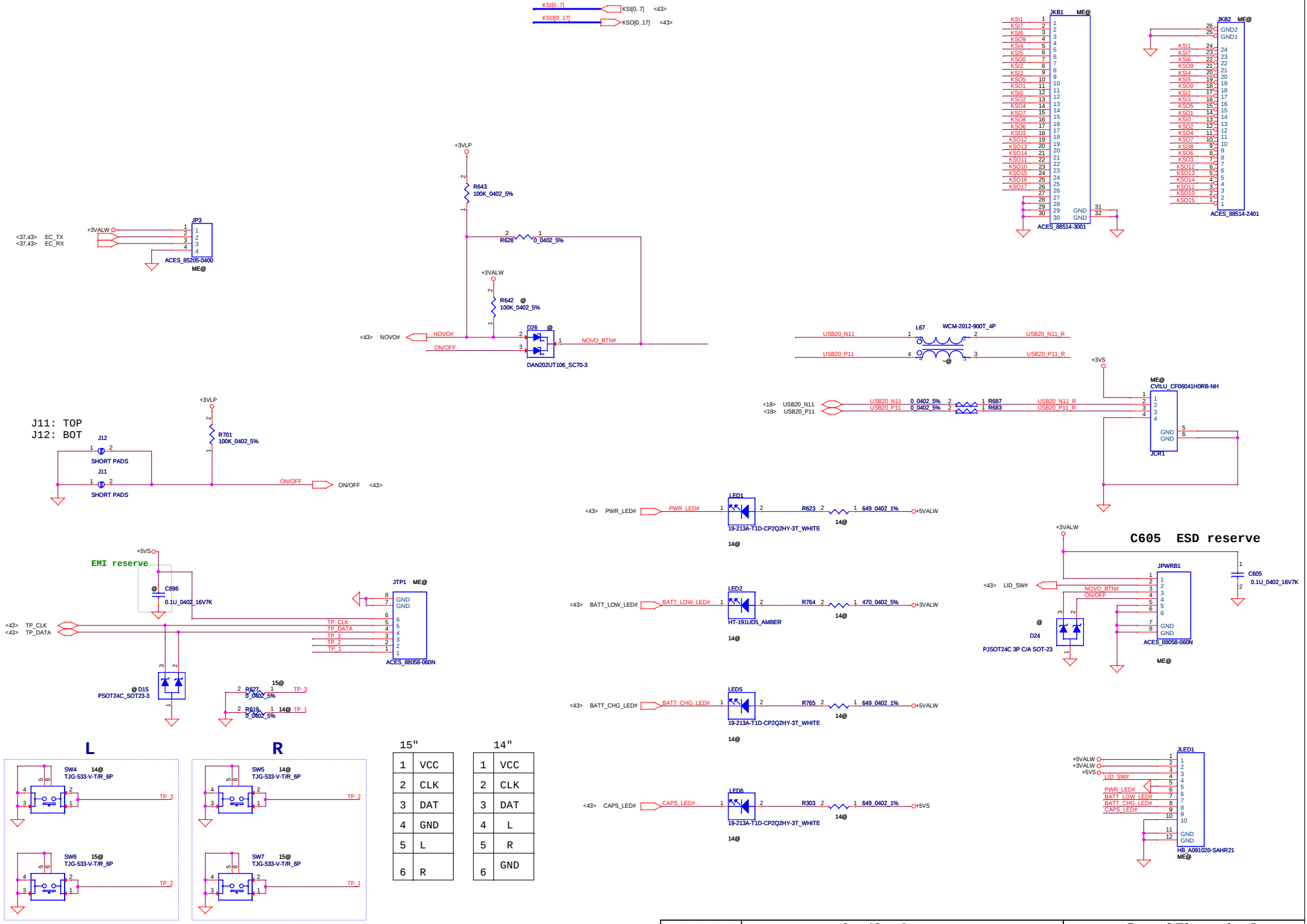
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



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				Custom	LA-9641P	0.3
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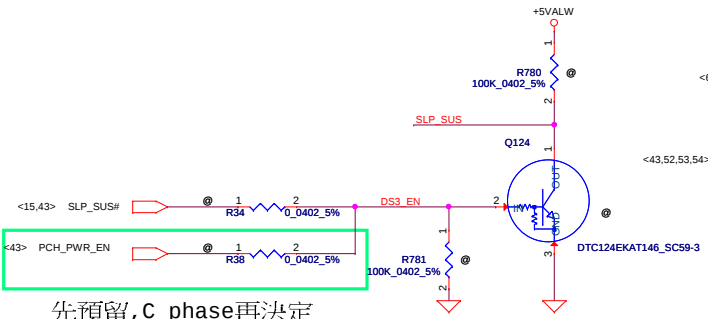
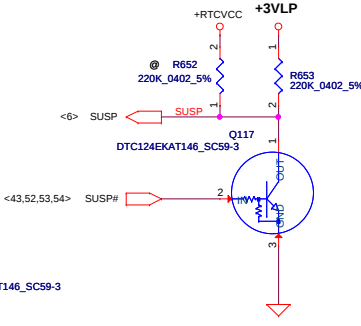
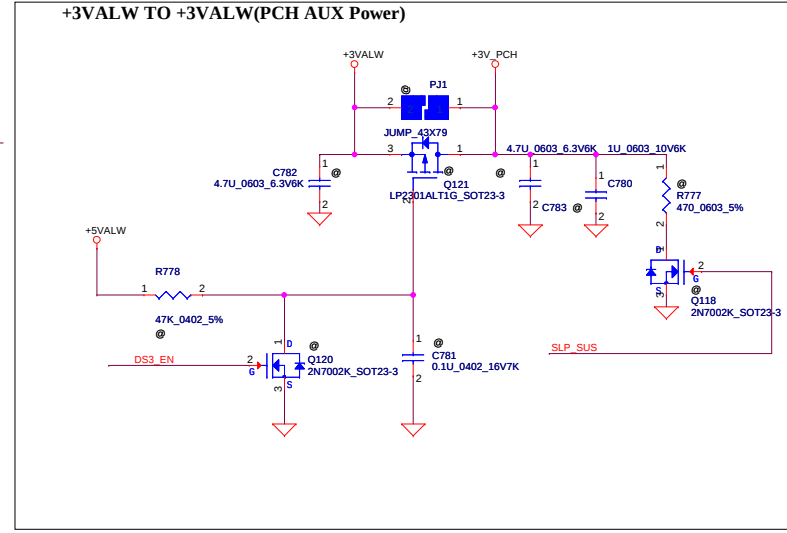
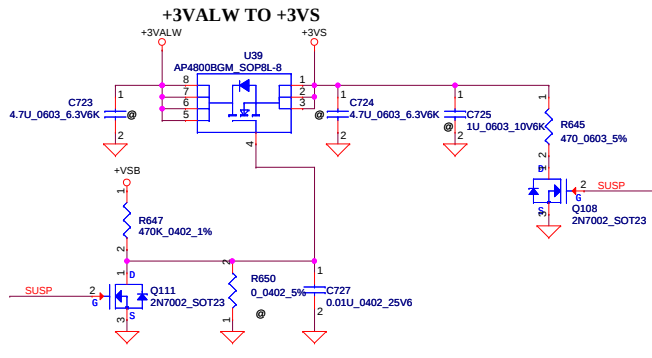
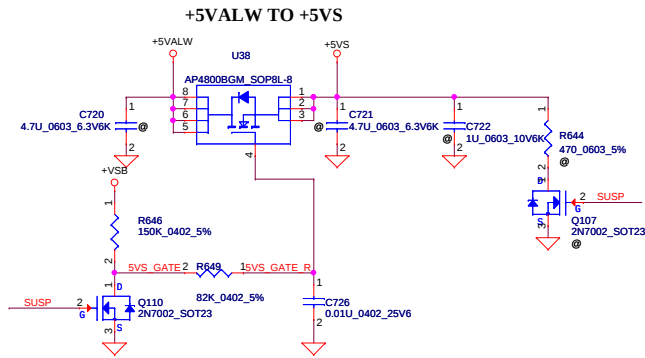
15"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND

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								USB ext. ports			
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						Date		Wednesday, March 06, 2013		Sheet	

1

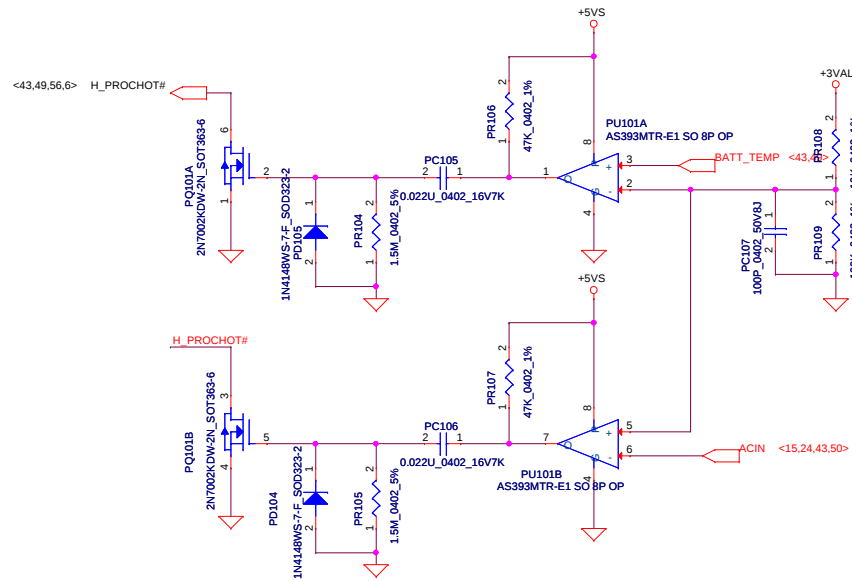
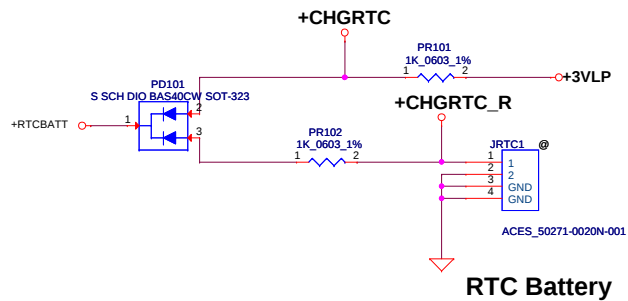
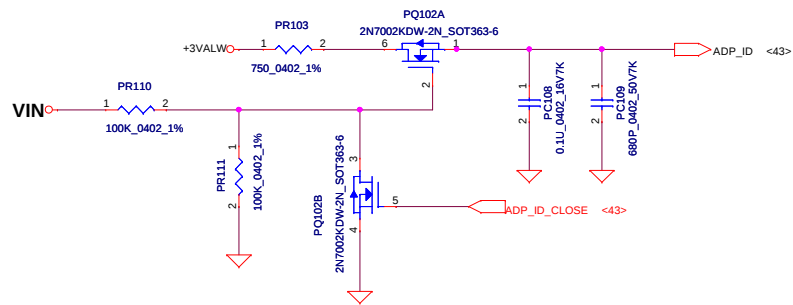
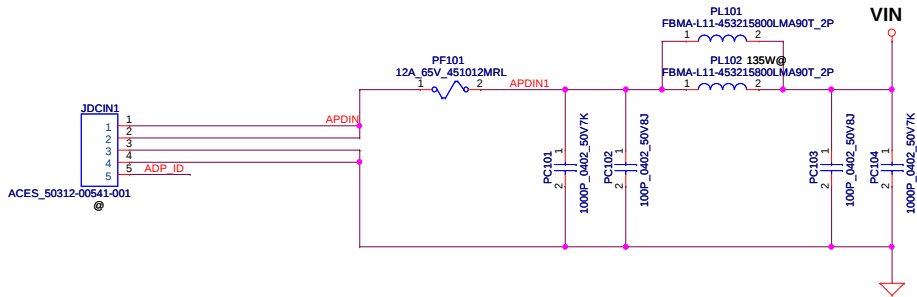


I.

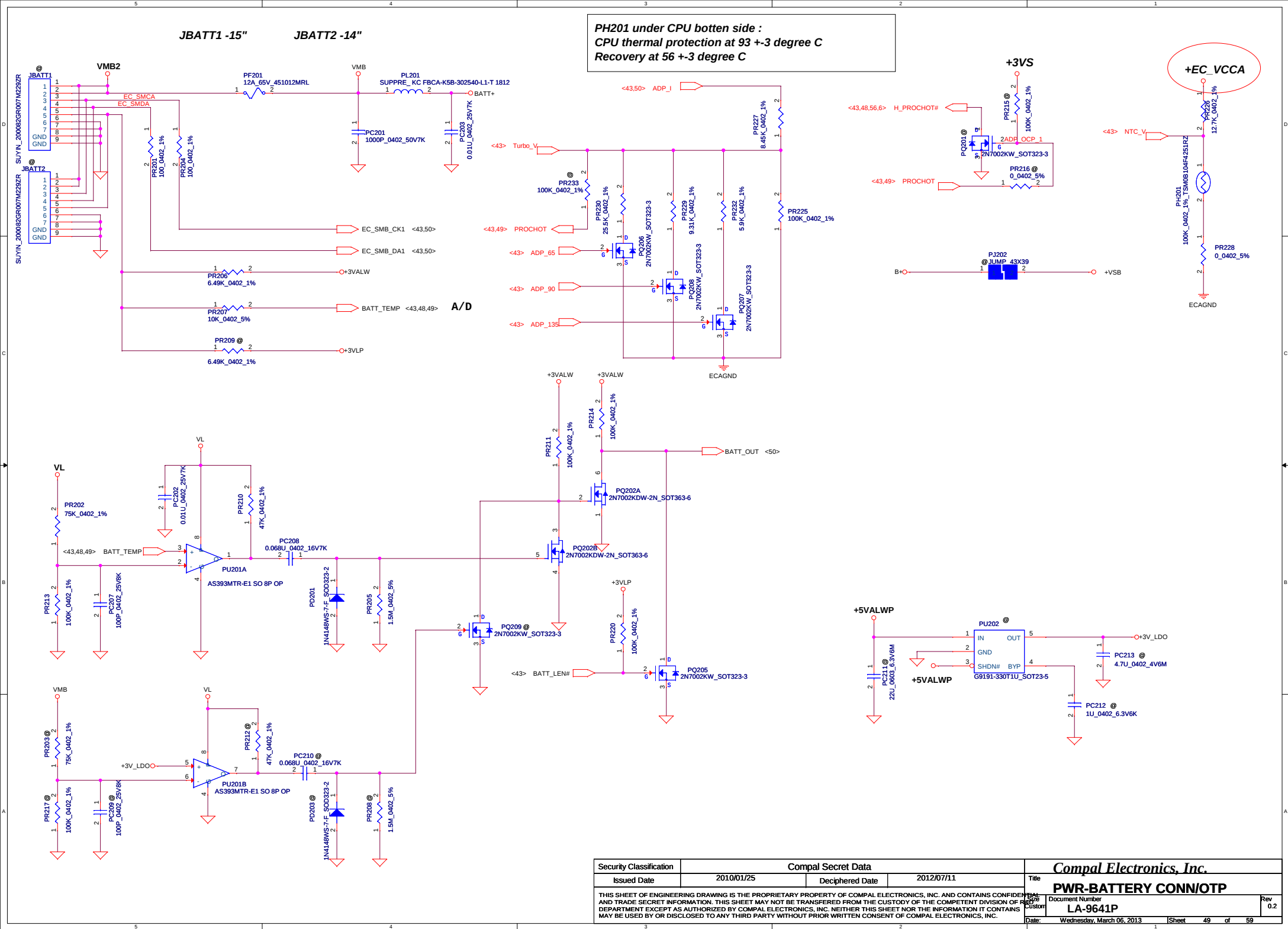


先預留,C phase再決定

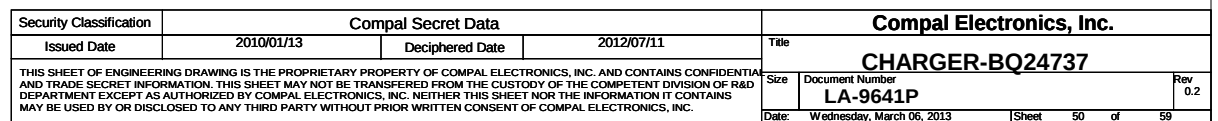
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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Size	Custom	Document Number	LA-9641P	Rev	0.3
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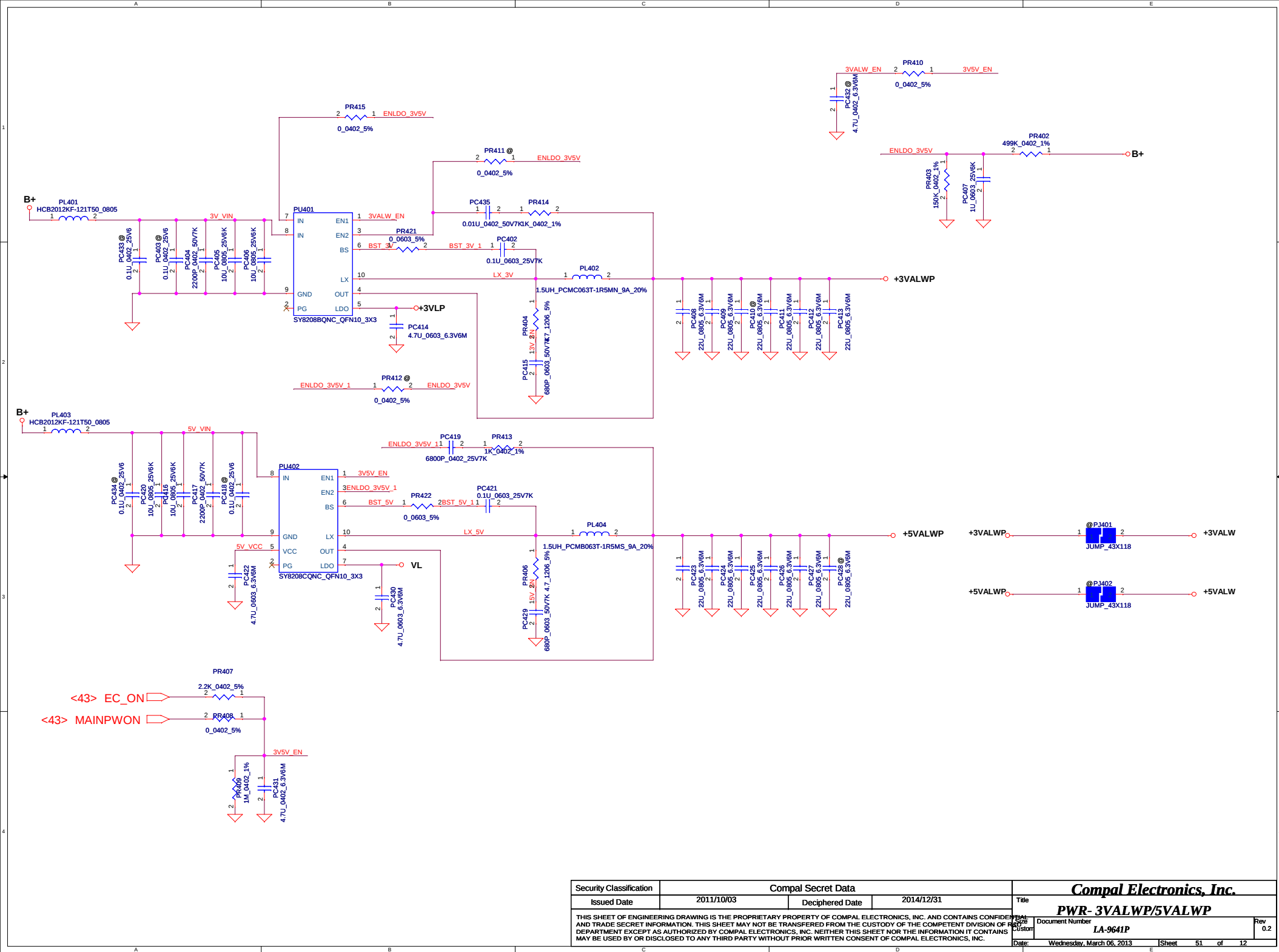


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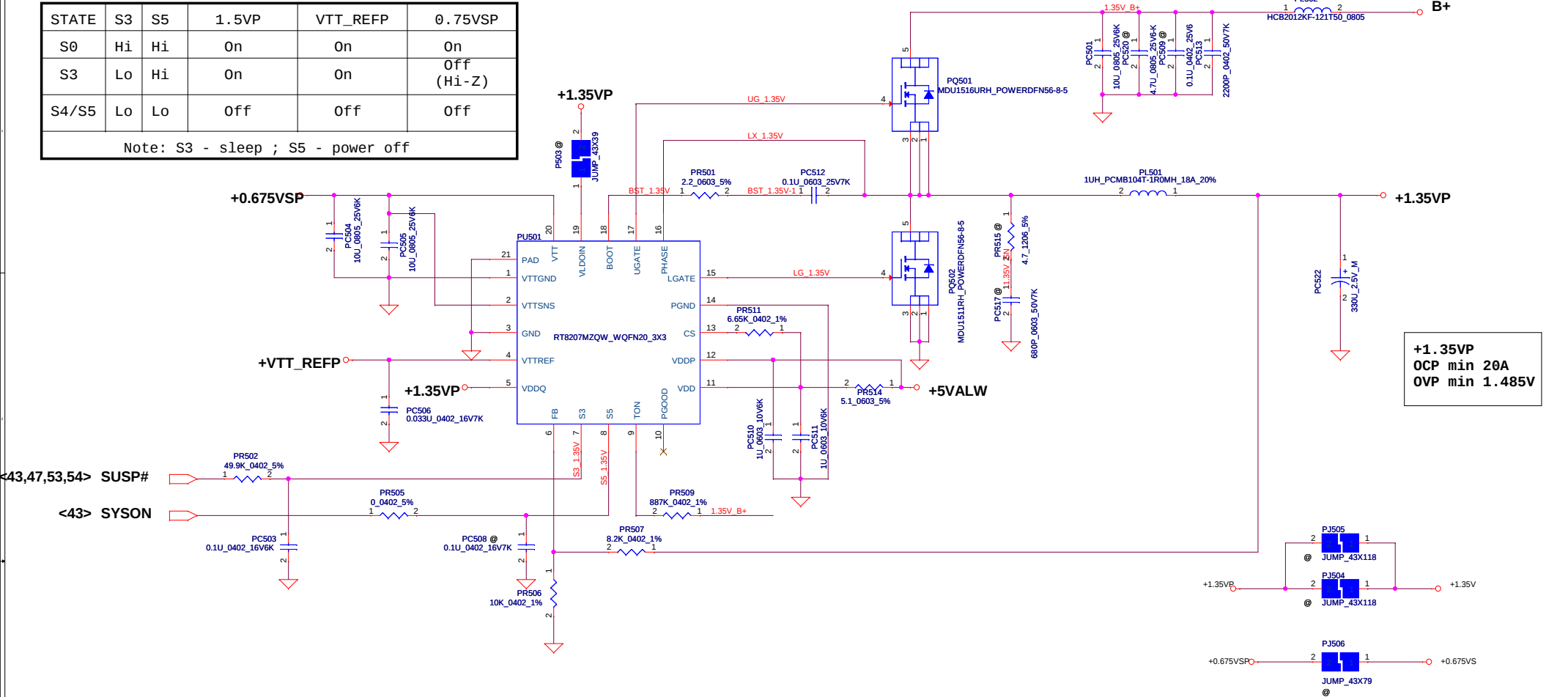
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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title Doc Number Revis Date	Date Wednesday, March 06, 2013	Rev 0.2
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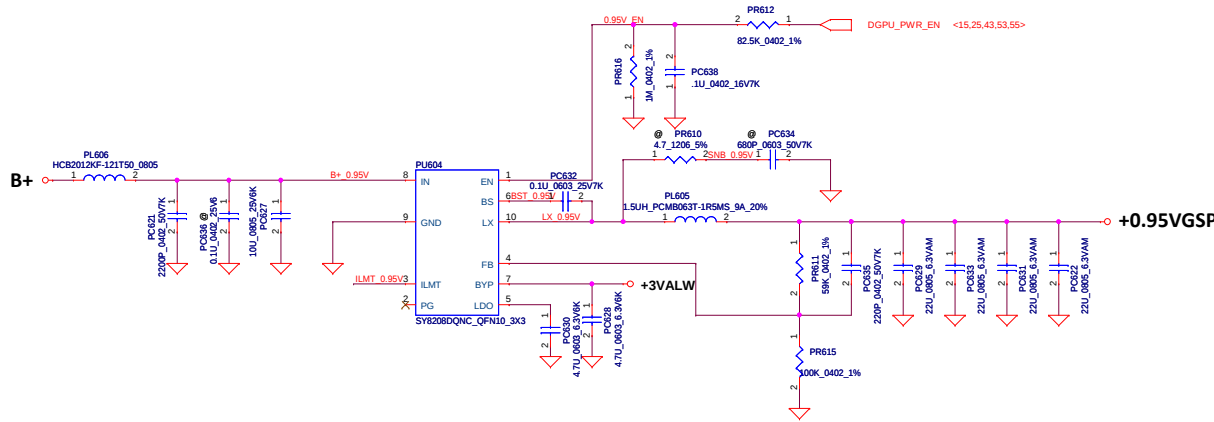
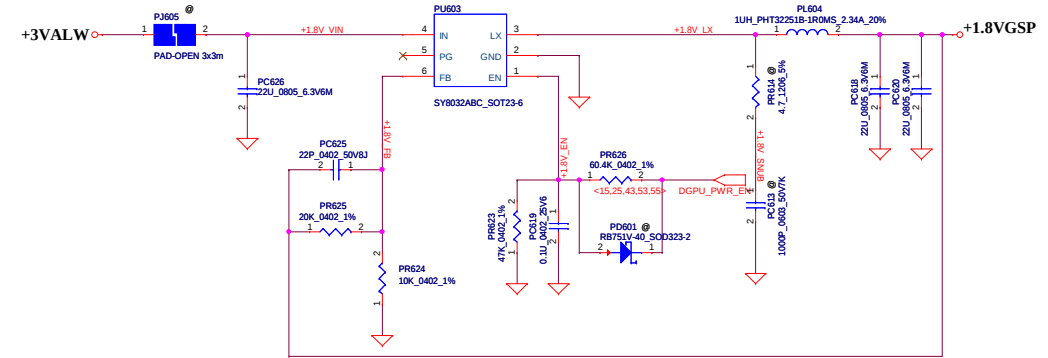
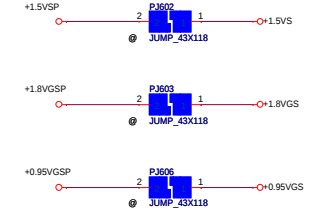
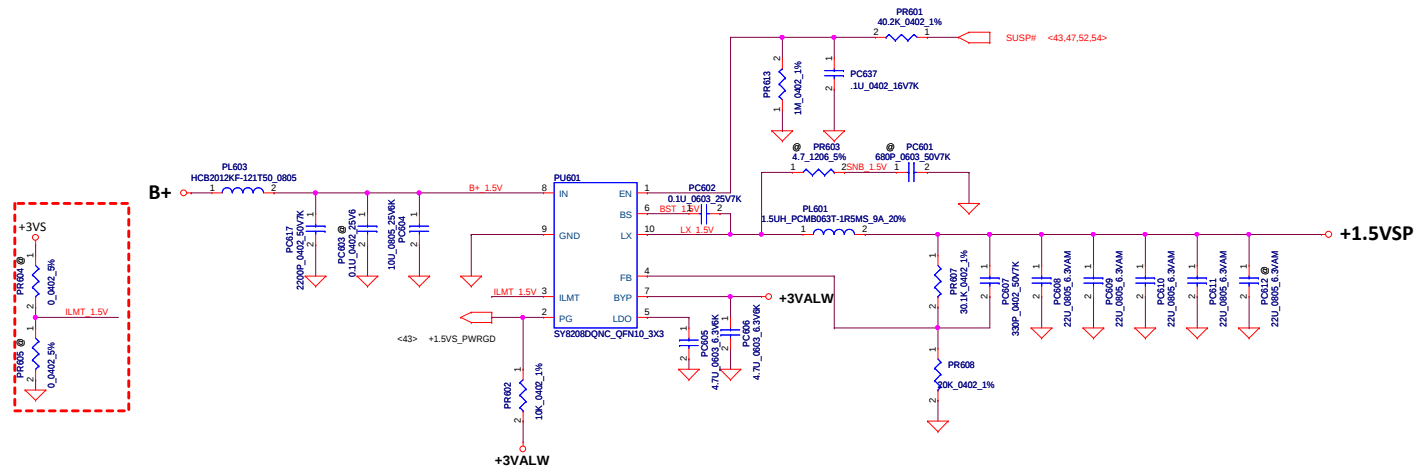


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C		D		Date:	Wednesday, March 06, 2013	Sheet 51 of 12

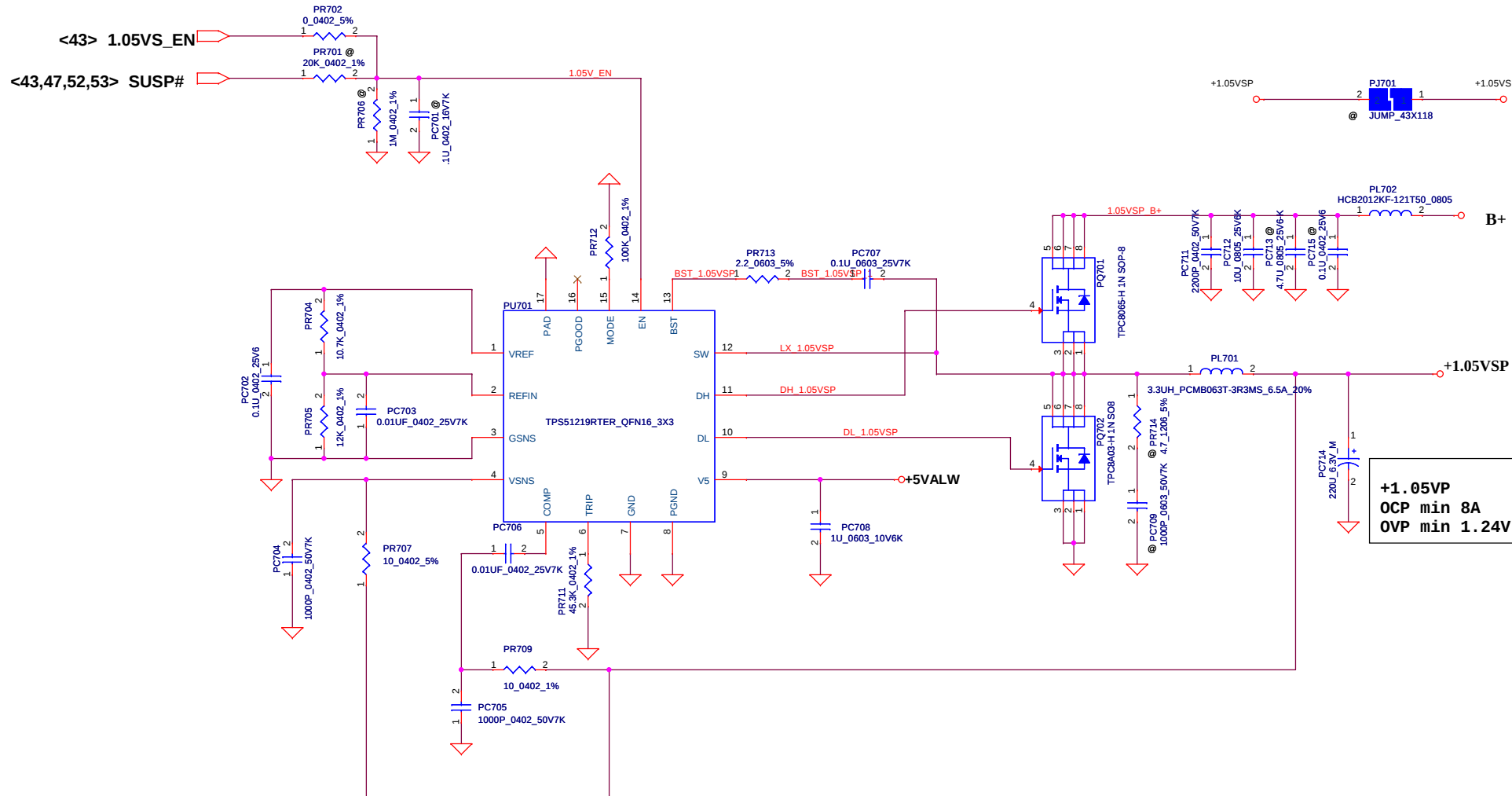
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



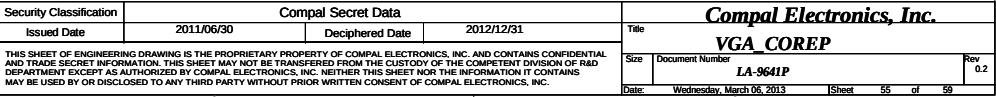
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				Sheet 52 of 59	

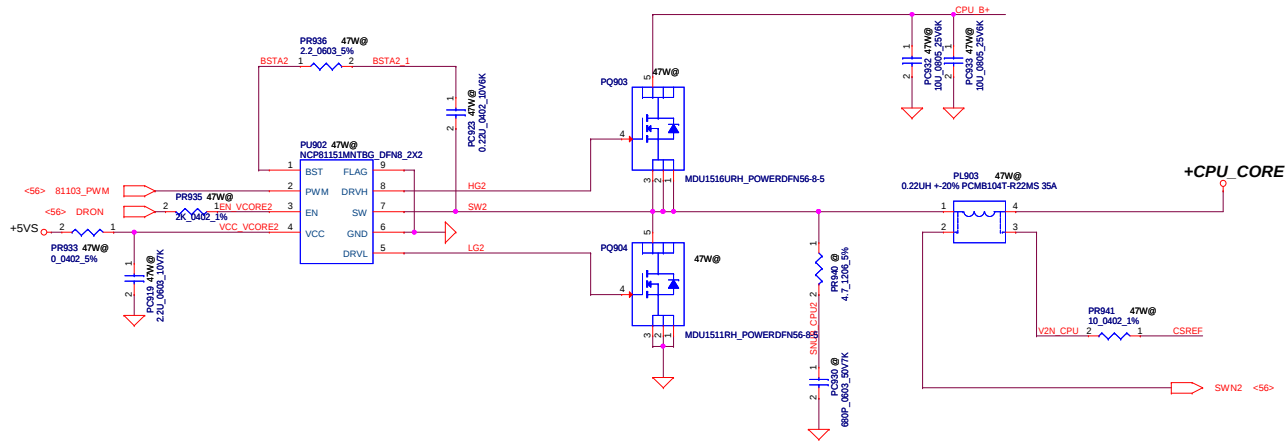
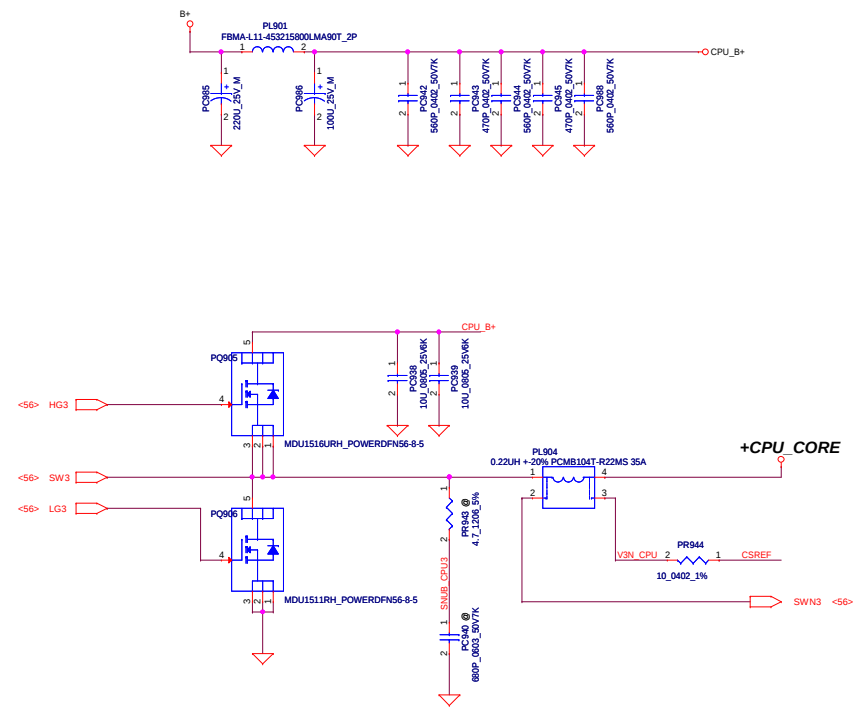
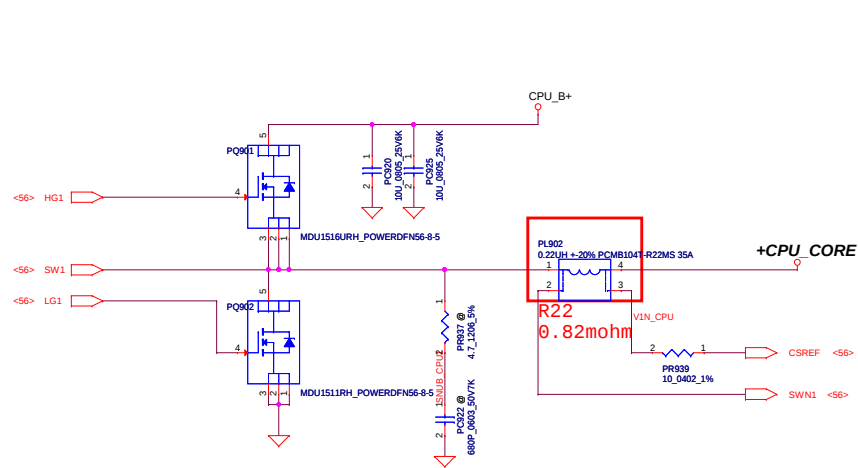


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Size	Document Number	Rev	0.2	
C	LA-9641P			
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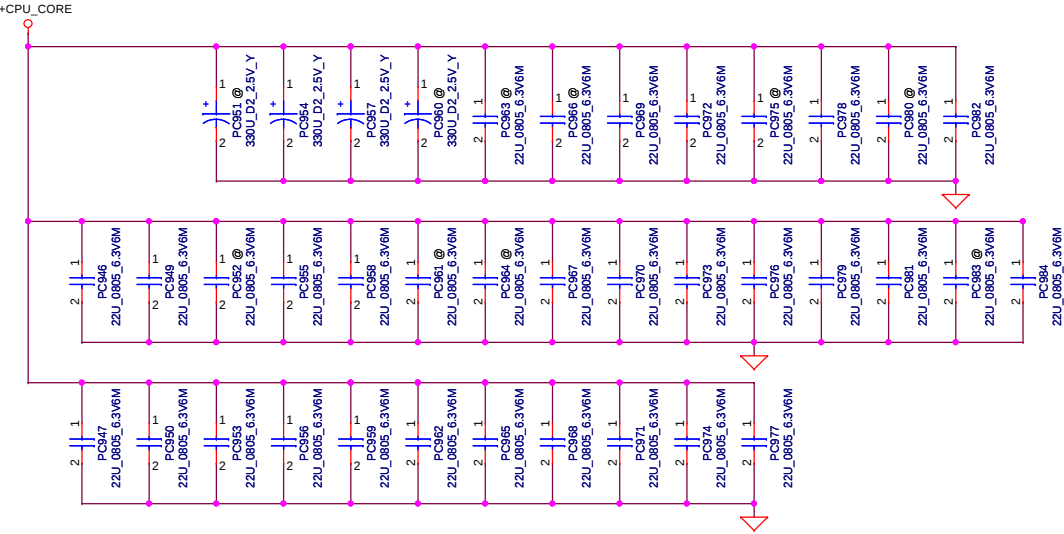


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+CPU_CORE 3 X 330u/9m(47W) 2X330u/9m(37W)
34 X 22u/0805 34 X 22u/0805



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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adapter ID selection circuit	48 49	Add PR103,PR110,PR111,PQ102,PC108,PC109 Add PR227,PR230,PR229,PR232,PR225,PQ206,PQ208,PQ207	2012.11.28	DVT
2	Delete reserve circuit B+ to VSB	49	Delete PR217,PR218,PR219,PC204,PQ203,PR223,PR224,PC205,PQ204,PC206	2012.11.28	DVT
3	Pop Snubber by EMI request	50	PR323,PC320	2012.11.28	DVT
4	To reduce Ripple	51	PC411,PC426 and change PL404 to 3.3uH	2012.11.28	DVT
5	Reserve enable signal by HW request	51	Add PR410,PC432	2012.11.28	DVT
6	Add boost resistor by EMI request	51	Add PR421,PR422	2012.11.28	DVT
7	Reserve feedback signal for IC application	51	Add PR413,PC419	2012.11.28	DVT
8	To reduce Ripple	53	Change PL601and PL605 to 1.5uH	2012.11.28	DVT
9	Delete reserve circuit	53	Delete PC623,PU602,PC624,PR619,PR620,PR622,PC614,PR627,PL602,PR613,PC612,PC615,PC616	2012.11.28	DVT
10	To reduce Ripple	54	Change PL601and PL701 to 3.3uH	2012.11.28	DVT
11	Reserve enable signal by HW request	54	Add PR702	2012.11.28	DVT
12	Pop Snubber by EMI request	55	PR826,PC811,PR855,PC865	2012.11.28	DVT
13	Add input MLCC by EMI request	57	Add PC943,PC944,PC945,PC988	2012.11.28	DVT
14	Reserve battery detective circuit	49 50	Add PR2003,PR217,PC209,PR212,PC210,PD203,PR208,PQ209,PC211,PU202,PC212,PC213 Add PQ314,PR311(Pop)	2013.03.03	PVT
15	Reserve capacitor by EMI request	50	Add PC318,PC319	2013.03.03	PVT
16	Reduce Component	51	Delete PD401	2013.03.03	PVT
17	Reserve 1.5VSP Power Good by HW request	53	Add PR602	2013.03.03	PVT
18	Reserve bridge resistor by EMI request	55	Add PR948,PC989		

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				Document Number	
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Item	Reason for change	PG#	Modify List	Date	Phase
1	USE singal 8M ROM for BIOS		Change U8 to SA000039A30 8MB ROM Del U7, R239, R234, R235, R233, R236	12/25	DVT
2	POWER NEW AC Connector		U31.21--> ADP_65 U31.68 change from EC_WL_OFF# to ADP_90 U31.85 change from EC_TS_ON#to ADP_135 U31.66 change from BRDID_1 to ADP_ID	12/25	DVT
3	Change XDP pull down Resistor to R pack		Del R18, R21, R23 / Add RP19	12/25	DVT
4	Update Lenovo BGA footprint		UV1, U4, UV5, UV6, UV7, UV8, UV9, UV10, UV11, UV12	12/25	DVT
5	Move 15" ODD CAP to Small Board		ChangeC605 to R401/ChangeC606 to R402/ ChangeC618 to R403/ChangeC617 to R404	12/25	DVT
6	WLAN Control change to PCH		PCH_GPI055--> PCH_WL_OFF# PCH_GPI022-->PCH_BT_ON# PCH_GPI034-->INTEL_BT_OFF#	12/25	DVT
7	POP TL_ENVDD PULL DOWN		POP R408	12/25	DVT
8	Change HDMI LV from 10P8R to 8R4R X2		Del RP19 ADD RP5, RP6	12/25	DVT
9	Update EC GPIO		NOVO# change form pin 26 to 34 EC_FAN_PWM change form pin 34 to 26 ENBKL change form pin 73 to 76 IMVP_IMON change form pin 76 to 73 DGPU_PWR_EN change form pin 107 to 123	12/25	DVT
10	VGA sequence		+1.5VGS : RV41 --> 240K / CV53 --> 0.1U	12/25	DVT
11	EC Board ID		Change R695 to 15K	12/25	DVT
12	Change ODD connector symbol		J0DD1->ALLT0_C18518-11305-L_13P-T	12/25	DVT
13	Update Crystal cap Value by vendor suggestion		C111/ C112 --> 15p CV36/CV37-->8.2p	12/25	DVT
14	Reserve for EMI		ADD R411, R412, C411, C412	12/25	DVT
15	Change PCIE port and clock connection by SW request		LAN-->Port 3 / WLAN--> Port2	12/25	DVT
16	Reserve R301		Reserve +3VLP power rail to EC	12/25	DVT
17	Change EC_RST# power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
18	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
19					
20					
21					
22					

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Add resistor to switch audio power from +3VS to +3VLP and +3VALW.		Add RA1,RA2	02/18	PVT
2	Reconnect HDD +3VS power rail.		Add R-short R552.	02/18	PVT
3	Modify LED current limiting resistor value.		Modify : R623,R765,R303	02/18	PVT
4	Add parallel resistor to separate BIOS and EC.		Add RP2	02/18	PVT
5	Add a Capacitor to connect CHASSIS_GND and GND by EMI request.		Add CL64	02/18	PVT
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