

ZZZ1



PCB
14*DAZ@

ZZZ2



LA-7011P
14*DA@

ZZZ3



LS-7011P
14*DA@

ZZZ4



LS-7013P
14*DA@

ZZZ5



LS-7014P
14*DA@

Compal Confidential

Schematics Document

PAW10

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

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				Date: Friday, December 24, 2010	Rev 1.0
				Sheet 1 of 41	

Clock Generator
SLG8SP556VTR

page16

Mobile Penryn

uPGA-478 CPU

page4, 5, 6

For 14"
LS-7011P 4PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

For 15"
LS-7012P 8PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

H_A#(3..35)
H_D#(0..63)



FSB
667/800MHz

CRT Connector

page21

LVDS
Connector

page22

Intel Cantiga GMCH

GM45

uFCBGA 1329

page 7, 8, 9, 10, 11, 12, 13



Dual Channel
DDR3-667/800(1.5V)

DDR3-SO-DIMM X2

BANK 0, 1, 2, 3

page 14,15

up to 4G

DMI *4



C-Link

**Wire Less Mini
card Slot 1**

page23

6*PCL-E BUS

Intel ICH9-M

page 17, 18, 19, 20

**SPI ROM
BIOS**

LPC BUS

EC

ENE KB926 E0

page27

AR8151/8152

10/100/Giga LAN

page24

RJ45 CONN

page25

Int.KBD

page32

**SPI ROM
BIOS**

page28

Touch Pad

page32

AZALIA

Audio Codec
CONEXTAN
CX20671

page26

2Channel Speaker

page26

Analog MIC_Int

page26

14*USB2.0

CMOS Camera

page22

BlueTooth CONN

page30

USB CONN X1(Right)

page29

USB PORT X1(Left)

page29

USB PORT X1(Left)

page29

Audio Jack SB CONN
HP X 1+
MIC_Ext X1

page30

Card Reader RTS5139

SATA HDD CONN

page28

SATA ODD CONN

page32

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				Date	Rev
				Friday, December 24, 2010	1.0
				Sheet 2 of 41	

DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Thermal
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
DDR SO-DIMM	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

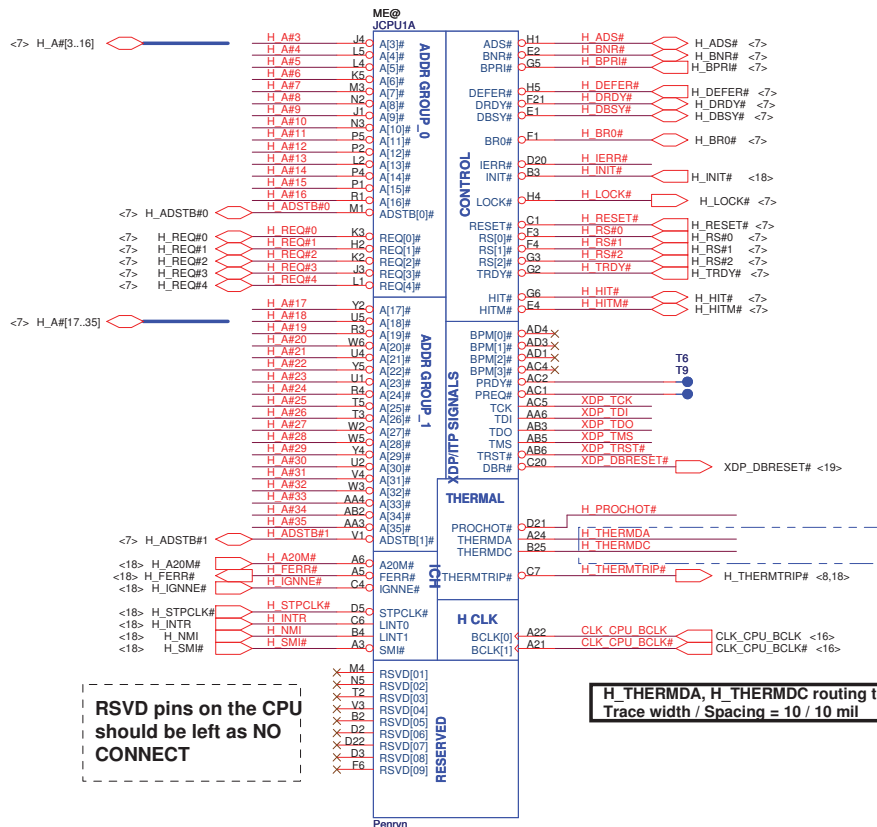
Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

PCIE PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

USB PORT LIST

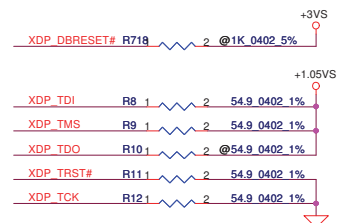
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT (ESATA)
8	
9	
10	
11	
12	
13	



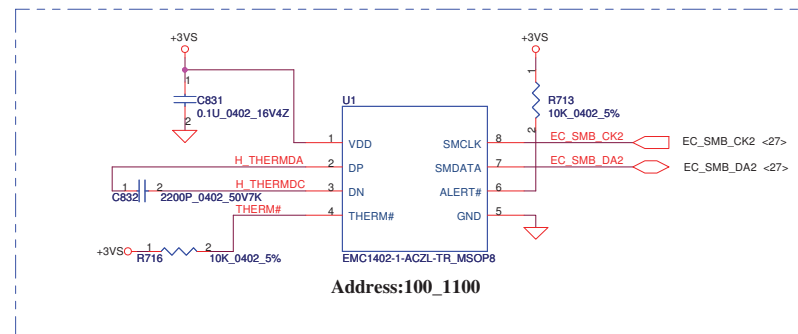
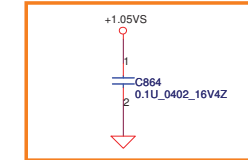
RSVD pins on the CPU should be left as NO CONNECT

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

SDP Reserve for debug , Please close to CPU side

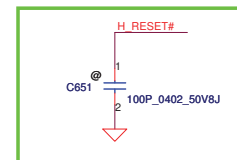


PVT ESD solution. Please close to R715



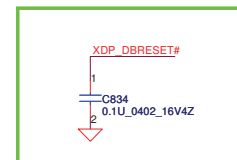
Address:100_1100

10/01 Add for reduce noise



Place closely pin C1

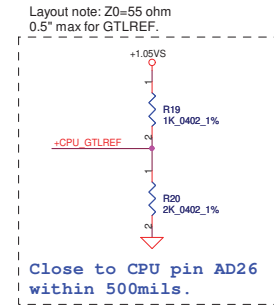
09/16 Add C834 For ESD



Place closely pin C20

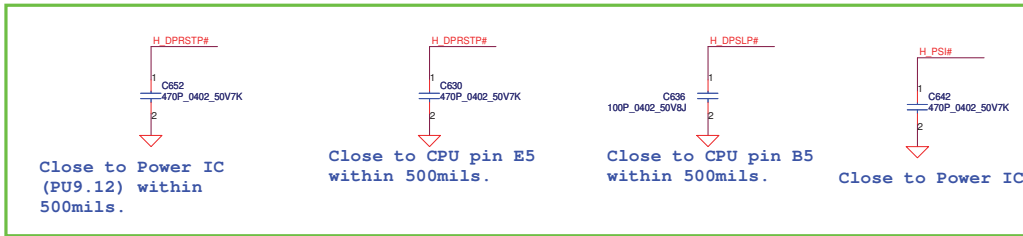
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				Customer	LA7011P
				Date	Friday, December 24, 2010
				Sheet	4 of 41
				Rev	1.0

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

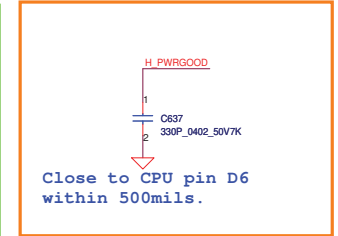


TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

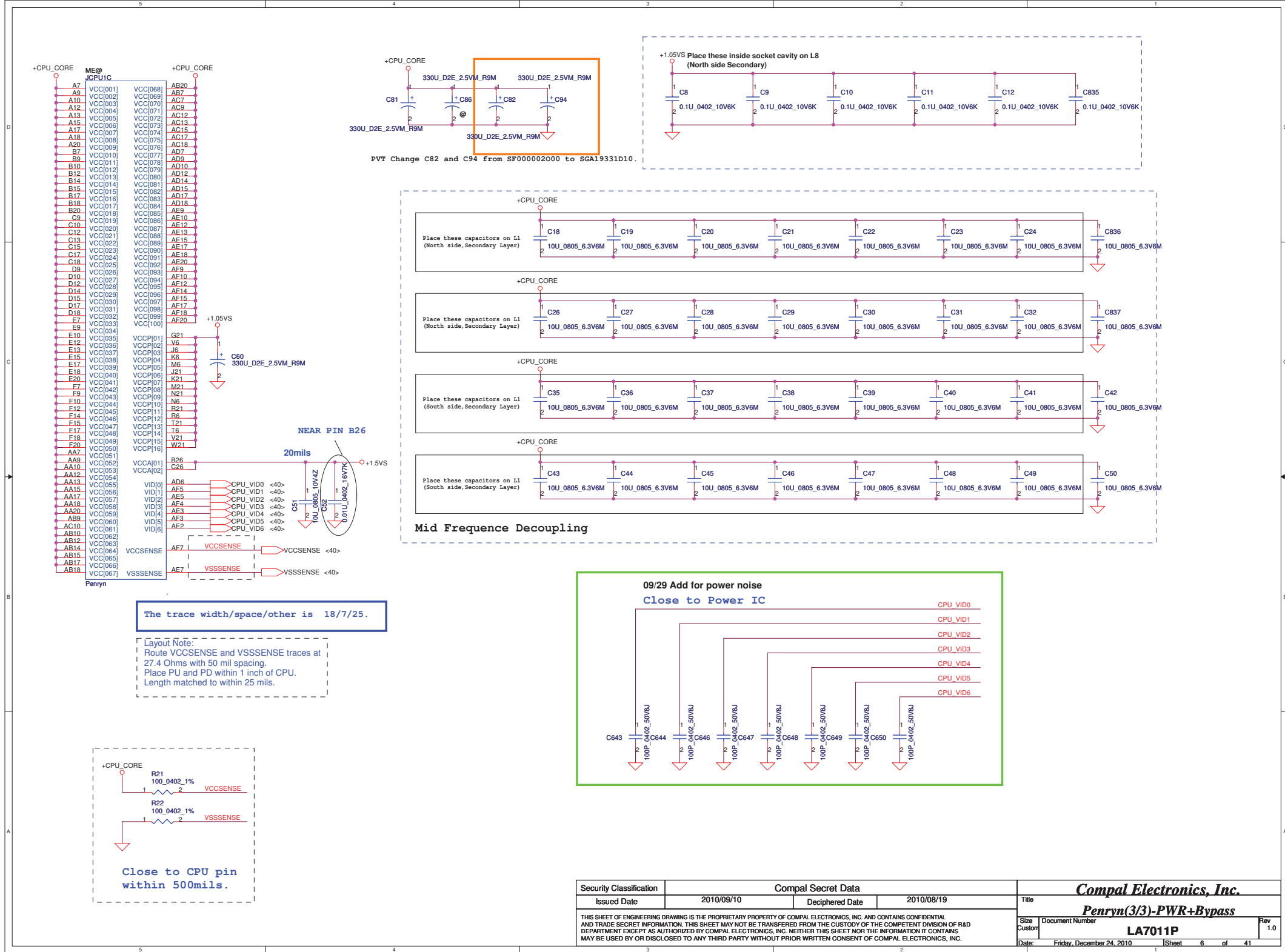
09/29 Add for power noise

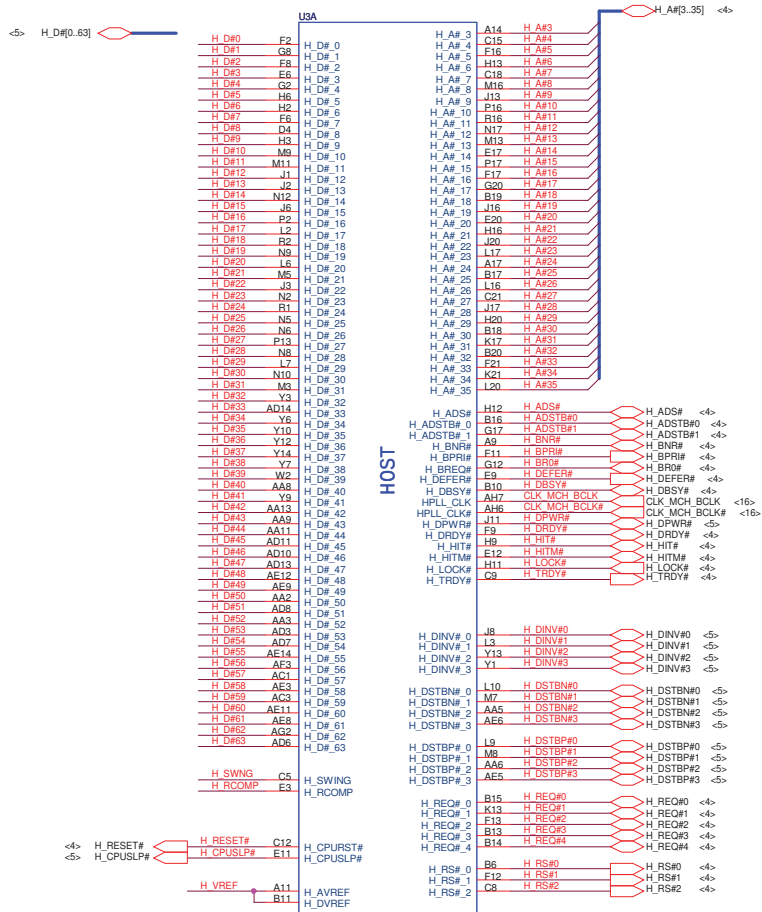


PVT for ESD solution

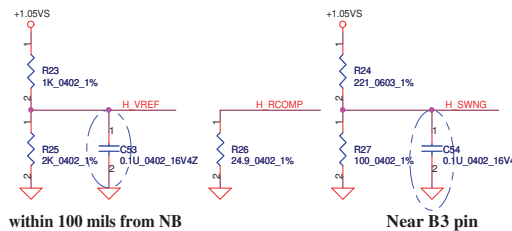


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Size	Custom	Document Number	LA7011P	Rev	1.0
Date	Friday, December 24, 2010	Sheet	5	of	41

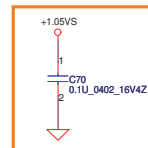




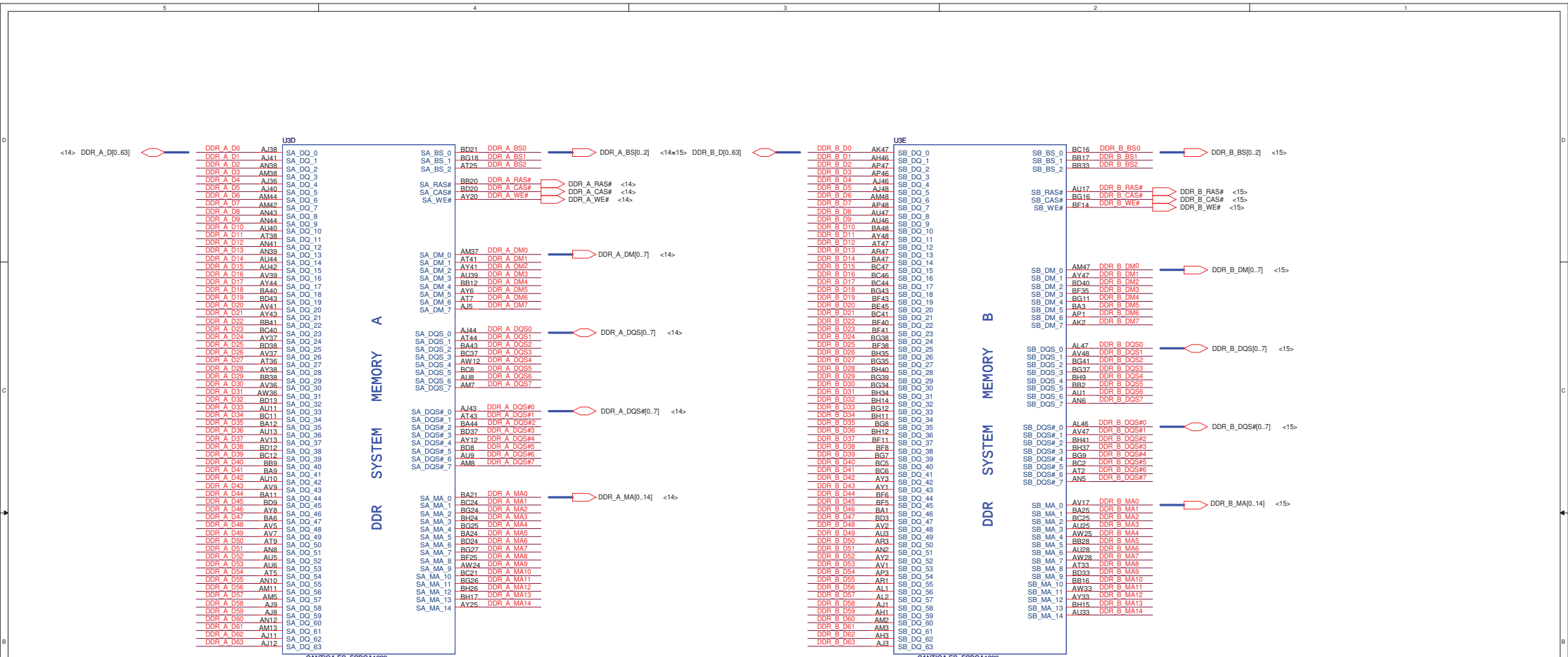
Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



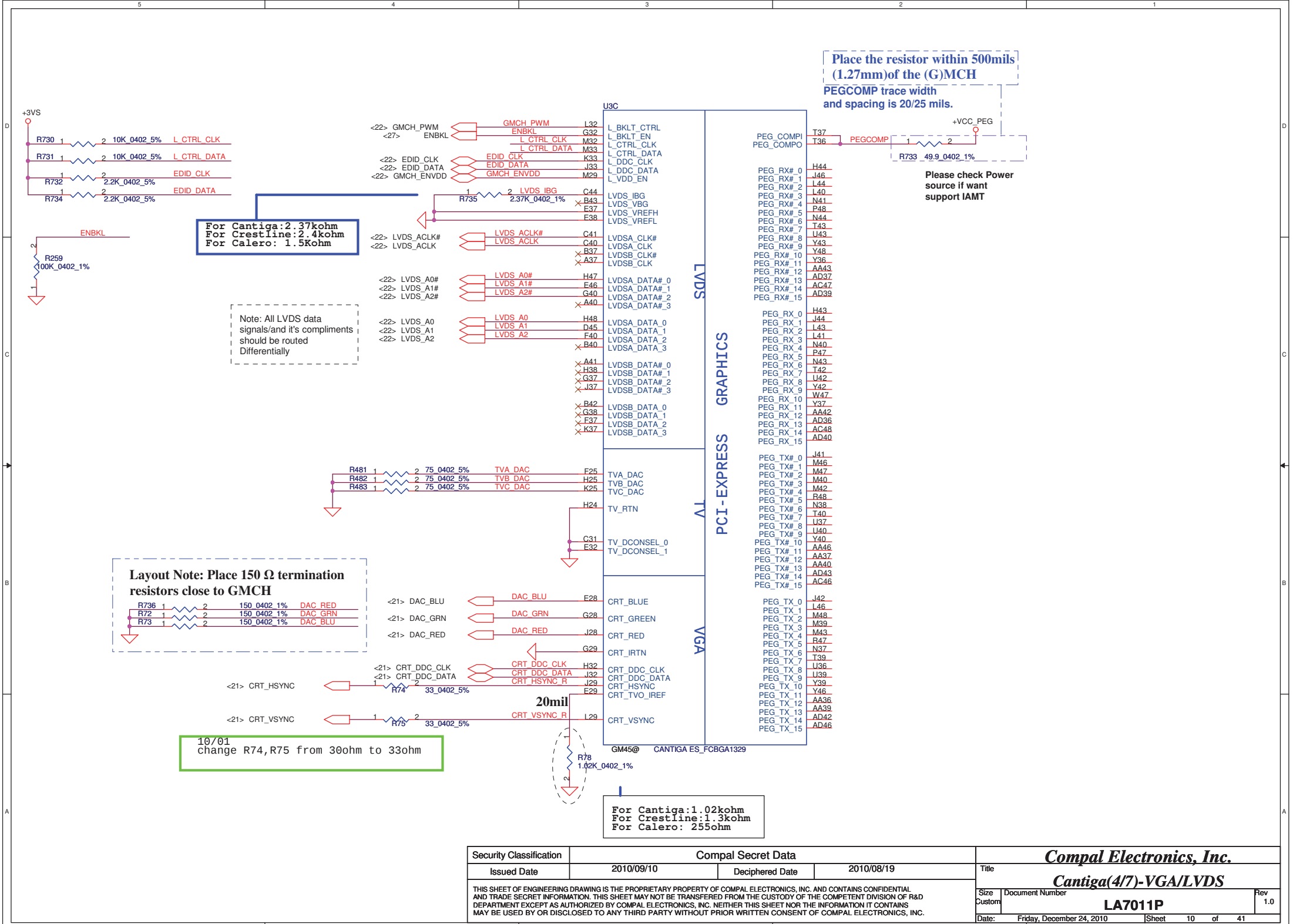
PVT ESD solution.
Please close to R23



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				LA7011P	
				Date: Friday, December 24, 2010	Sheet 7 of 41



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				LA7011P	
				Date	Friday, December 24, 2010
				Sheet	9 of 41



Place the resistor within 500mils
(1.27mm) of the (G)MCH
PEGCOMP trace width
and spacing is 20/25 mils.

Please check Power
source if want
support IAMT

For Cantiga: 2.37kohm
For Crestline: 2.4kohm
For Calero: 1.5kohm

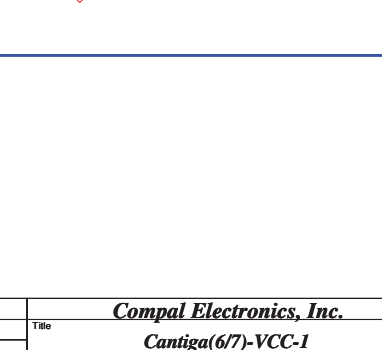
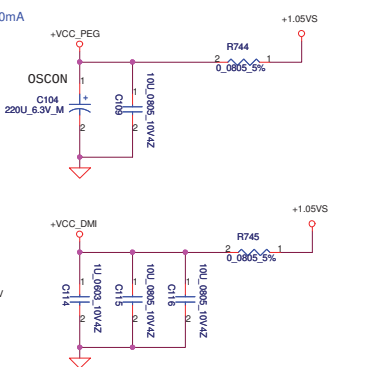
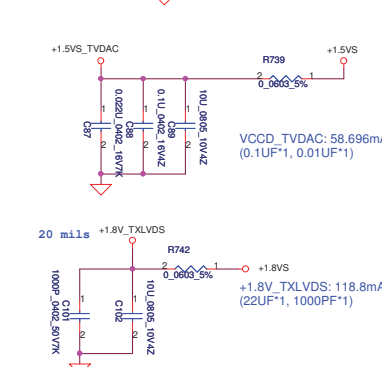
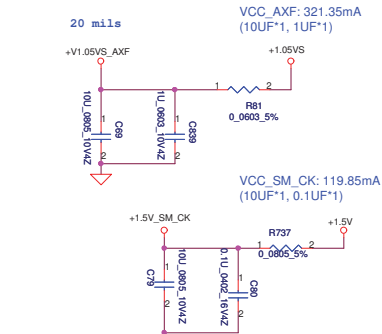
Note: All LVDS data
signals/and it's compliments
should be routed
Differentially

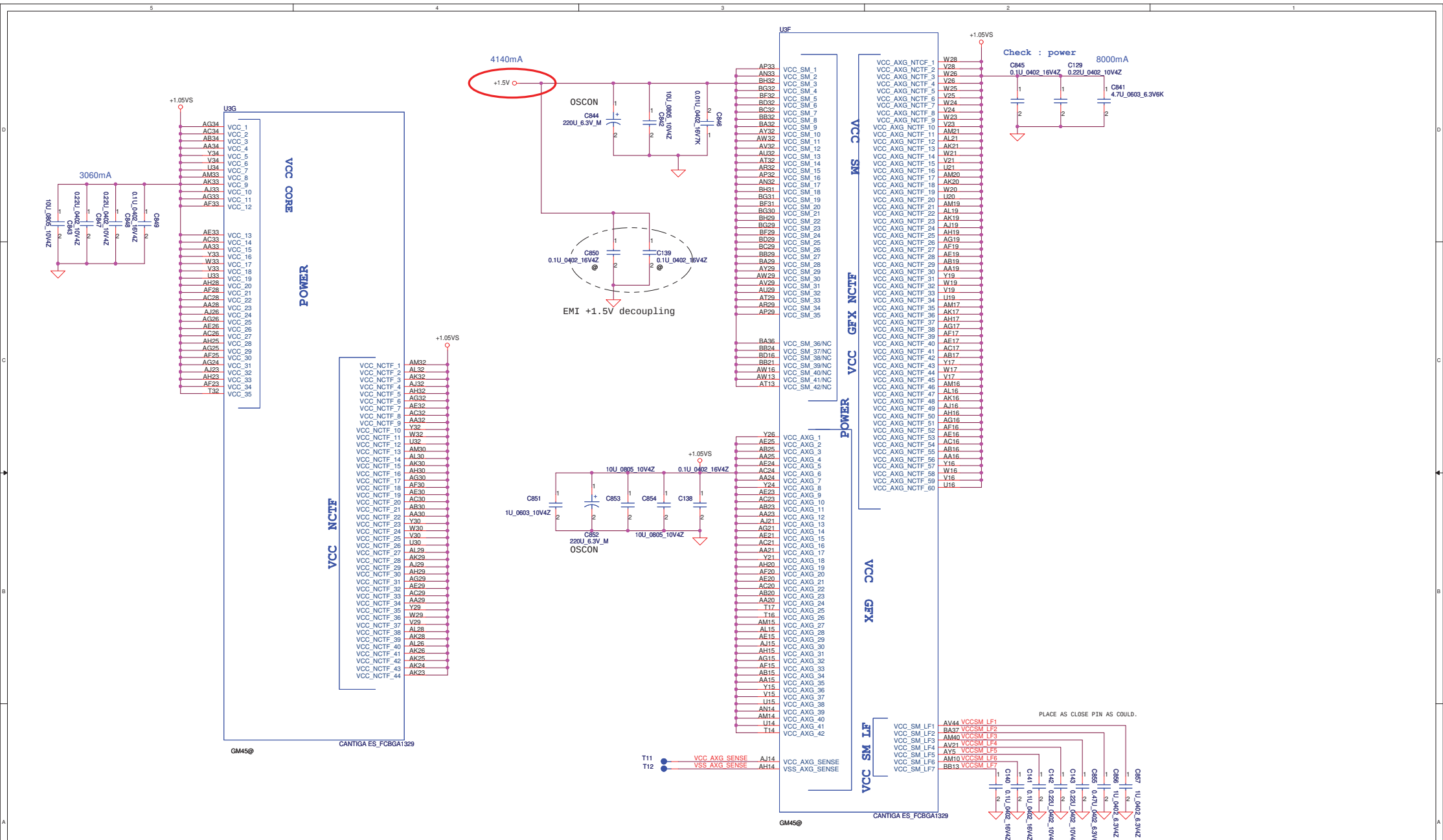
Layout Note: Place 150 Ω termination
resistors close to GMCH

10/01
change R74,R75 from 30ohm to 33ohm

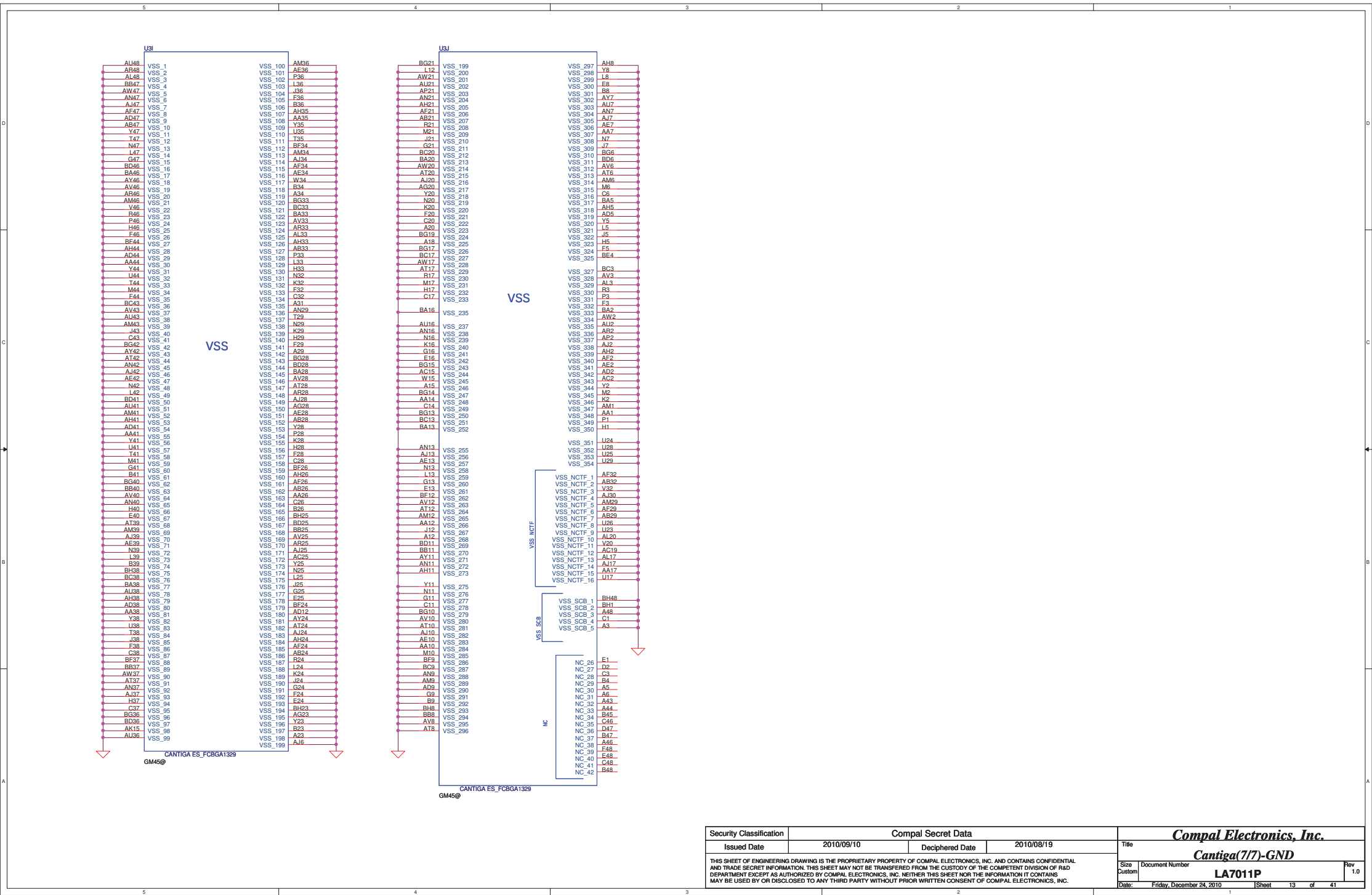
For Cantiga: 1.02kohm
For Crestline: 1.3kohm
For Calero: 255ohm

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Size Custom	Document Number	LA7011P			Rev 1.0
Date:	Friday, December 24, 2010	Sheet	10	of	41

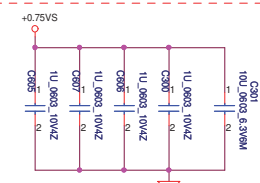




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Date:		Friday, December 24, 2010		Sheet		12		of		41	

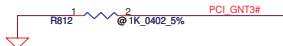
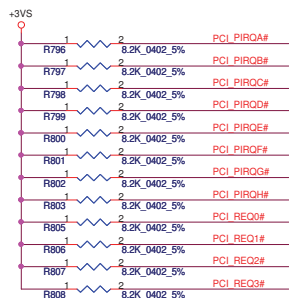
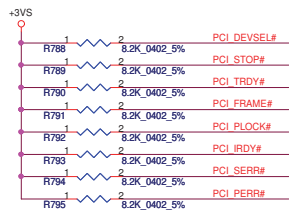


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Custom	LA7011P				1.0
Date:		Friday, December 24, 2010		Sheet	13 of 41

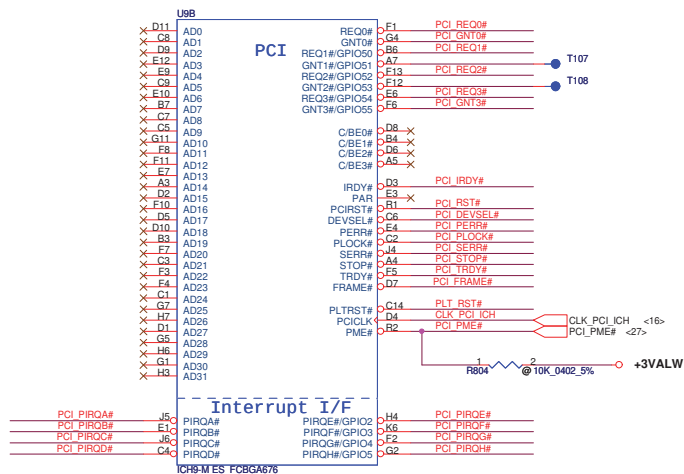




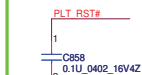
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				Cust	LA7011P	1.0	
				Date:	Friday, December 24, 2010	Sheet	15 of 41
2				1			



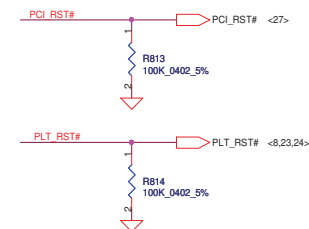
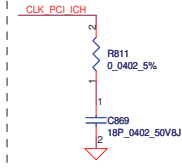
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



09/16 Add C858 For ESD
Place closely pin C14

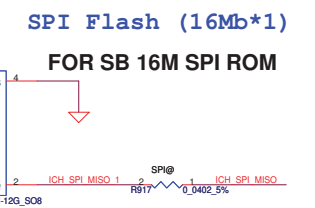
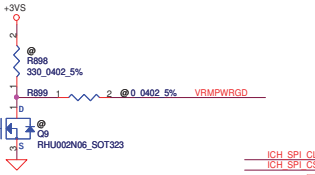
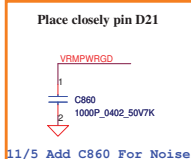
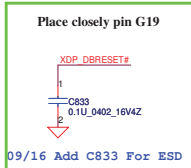
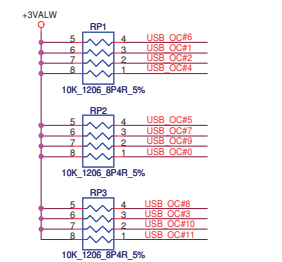
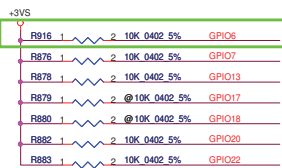
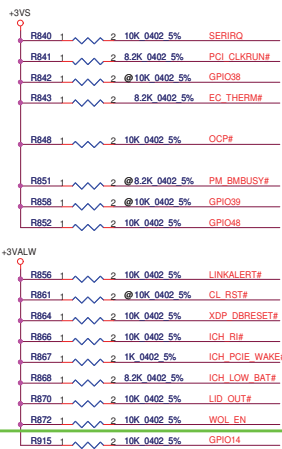


Place closely pin D4

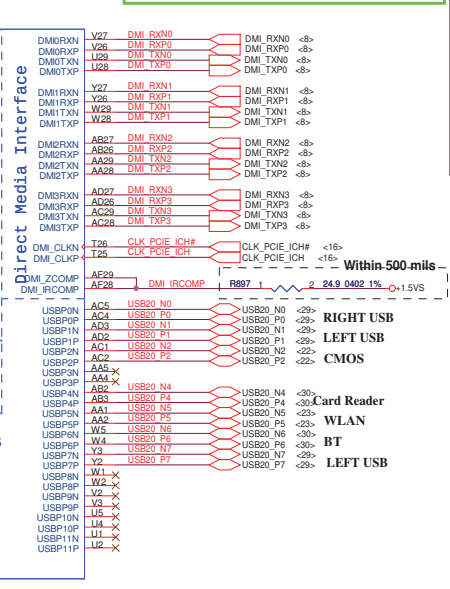
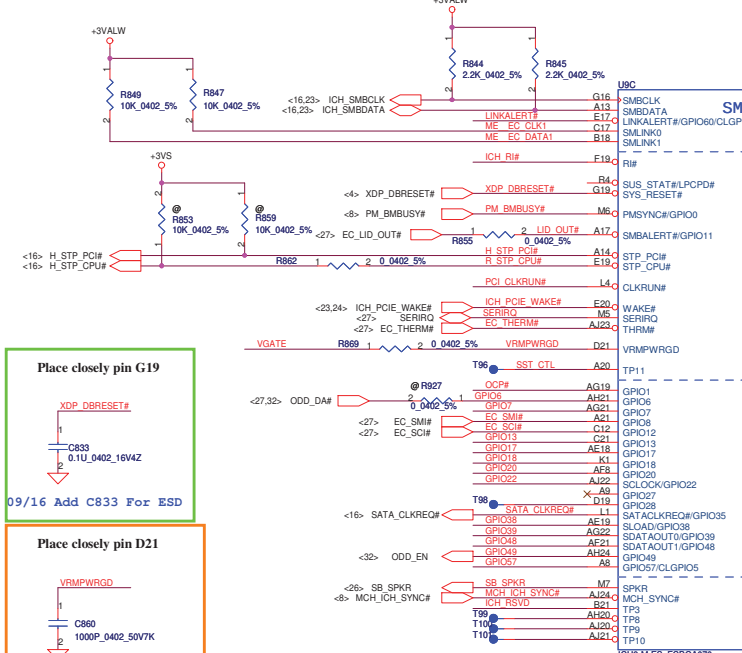


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

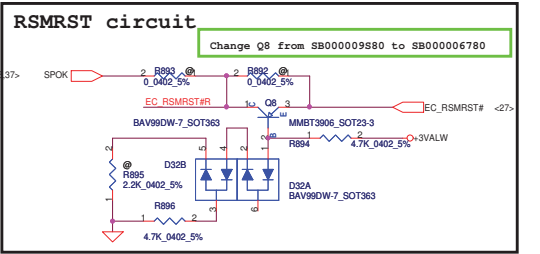
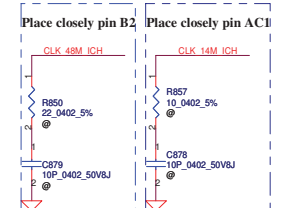
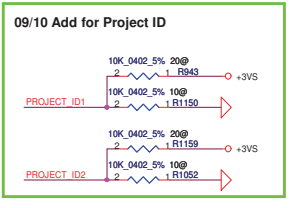
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Size	Custom	Document Number	LA7011P	Rev 1.0
Date:	Friday, December 24, 2010	Sheet	17	of 41



Change U33 footprint from WIESO_G6179-100000_8P to MX25L1606EM2I-12G_S08 0920
Change Value from MX25L8005M2C-15G SOP 8P to MX25L1606EM2I-12G_S08 0920

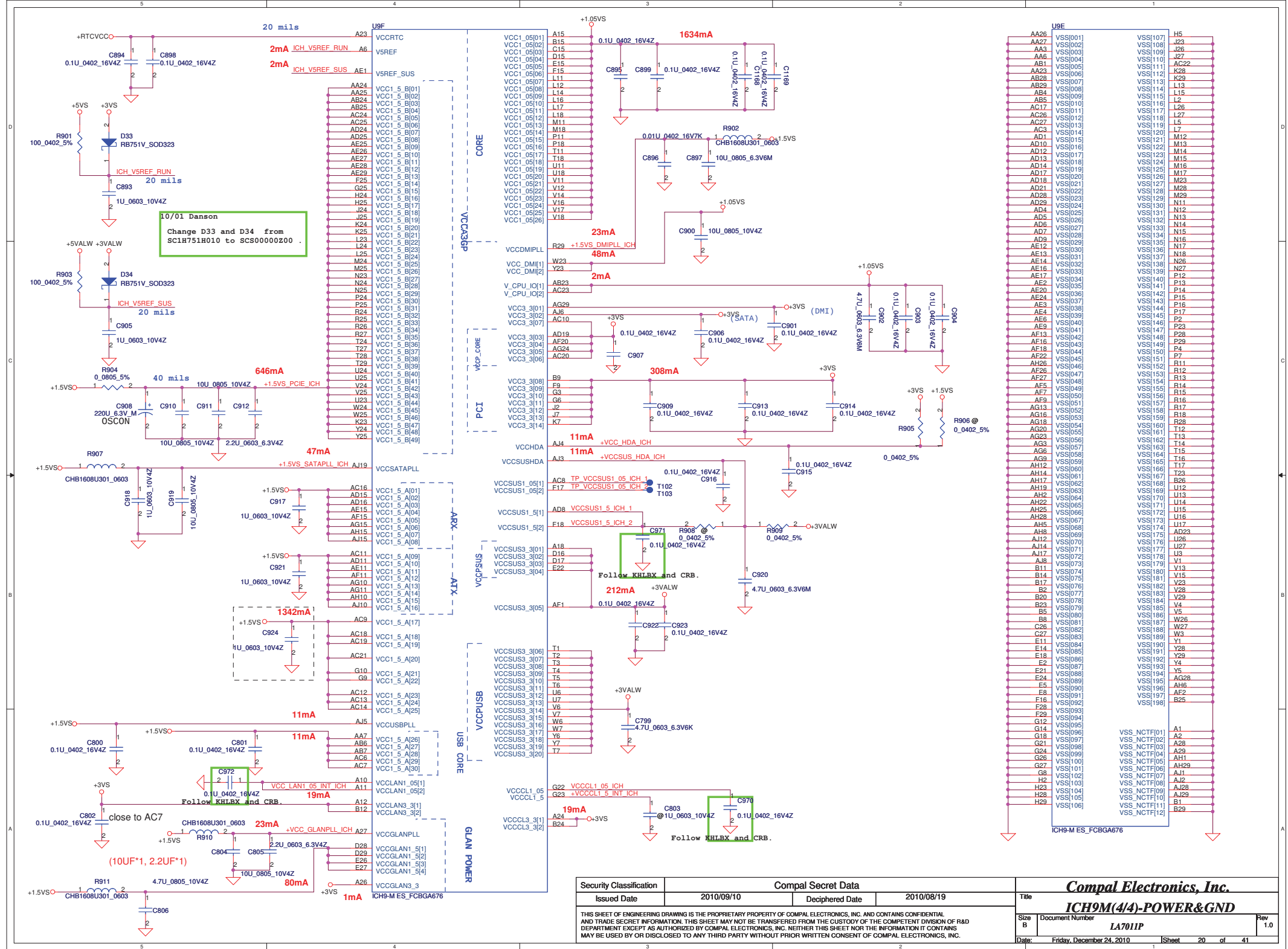


Change U26 P/N from SA00000X100 to SA000041N00 0915

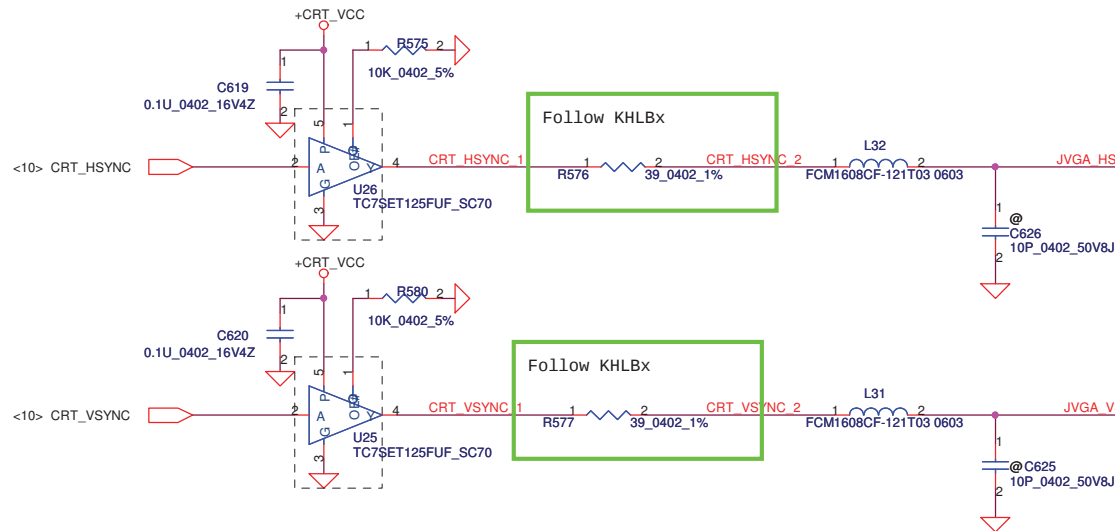
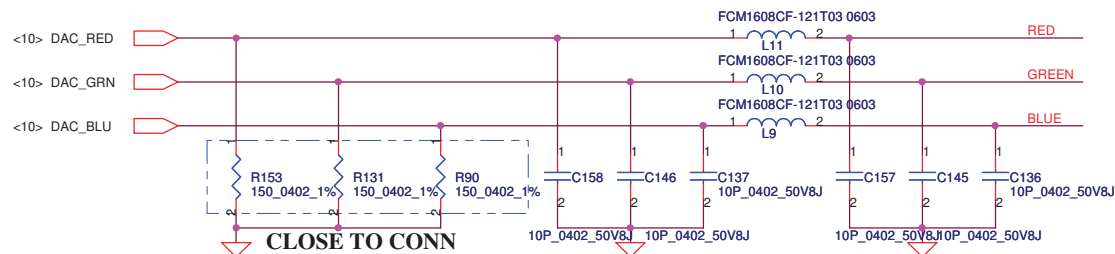
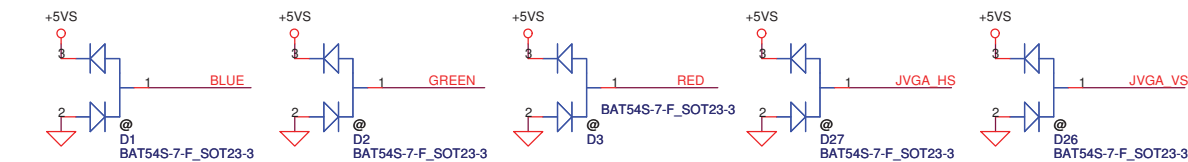


PORT	DEVICE
1	LAN
2	WLAN
3	CMOS
4	CARD READER
5	WIRELESS
6	BT
7	LEFT SIDE
8	RIGHT SIDE
9	CMOS
10	CMOS
11	CMOS

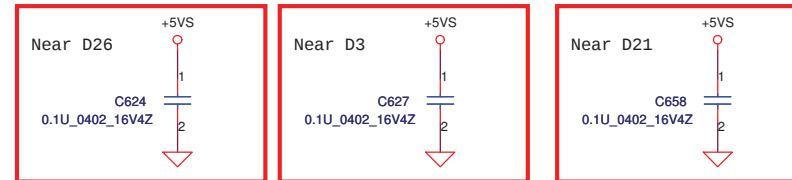
PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	CARD READER
4	WIRELESS
5	BT
6	LEFT SIDE
7	RIGHT SIDE
8	CMOS
9	CMOS
10	CMOS
11	CMOS



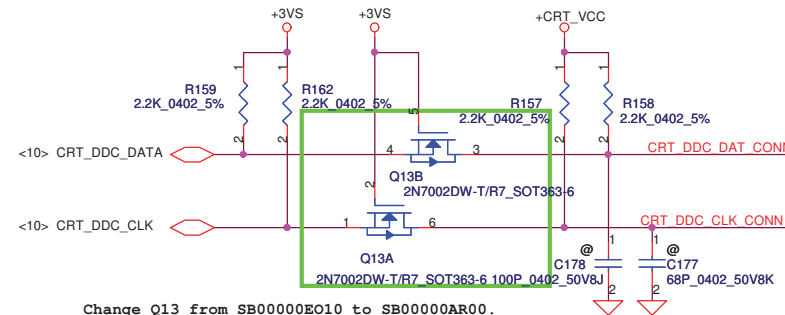
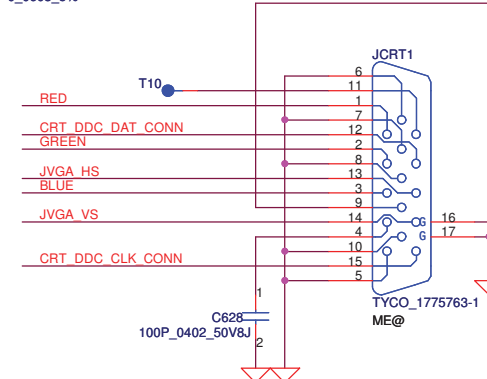
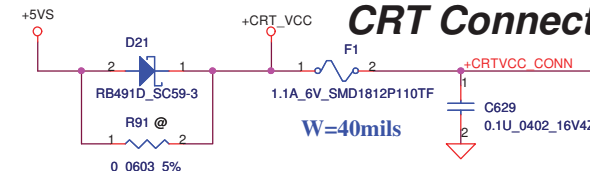
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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					LA7011P
				Rev	1.0
3 1 2				Date:	Friday, December 24, 2010
				Sheet	20 of 41



Pre MP ADD for ESD solution

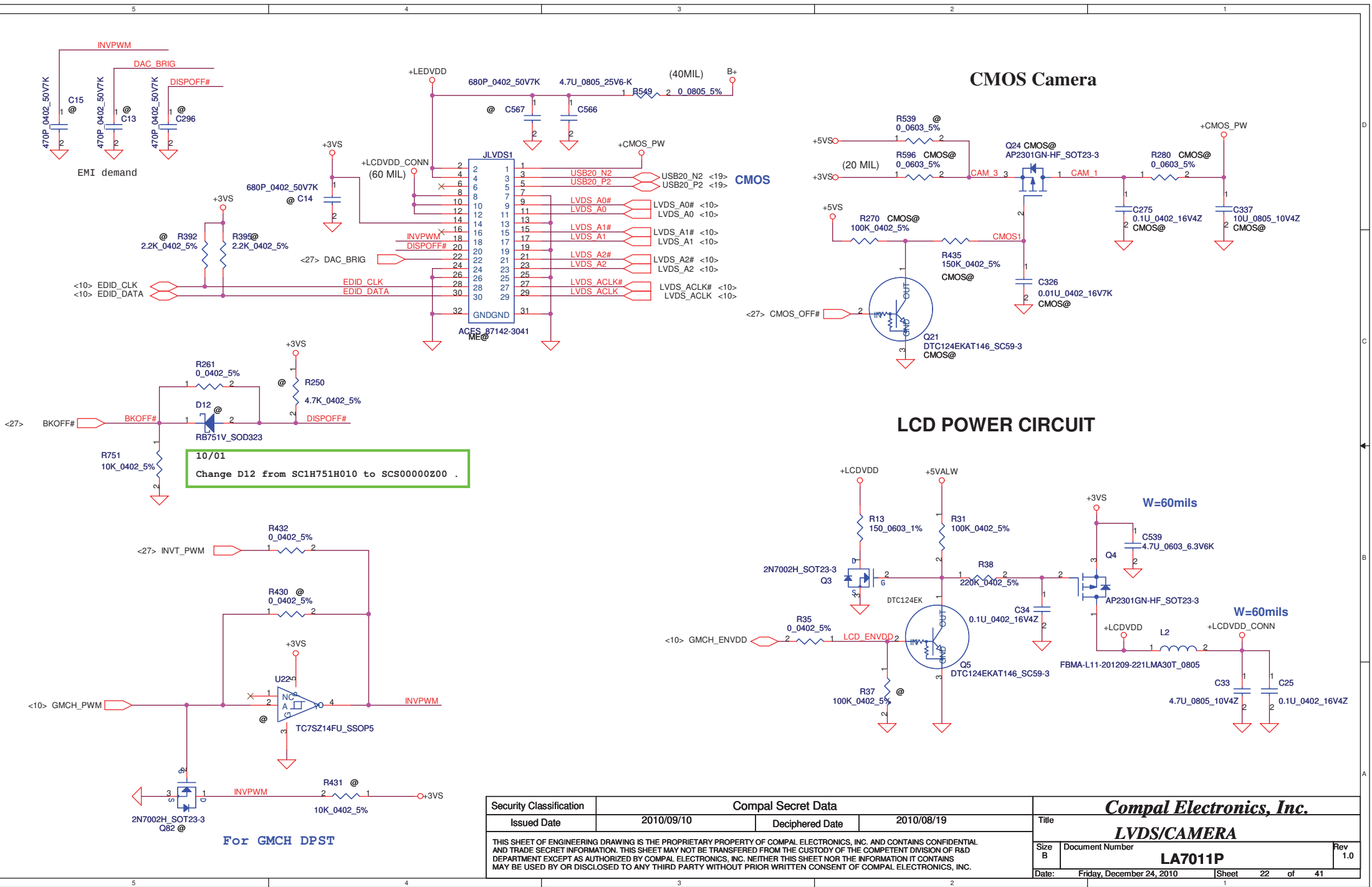


CRT Connector



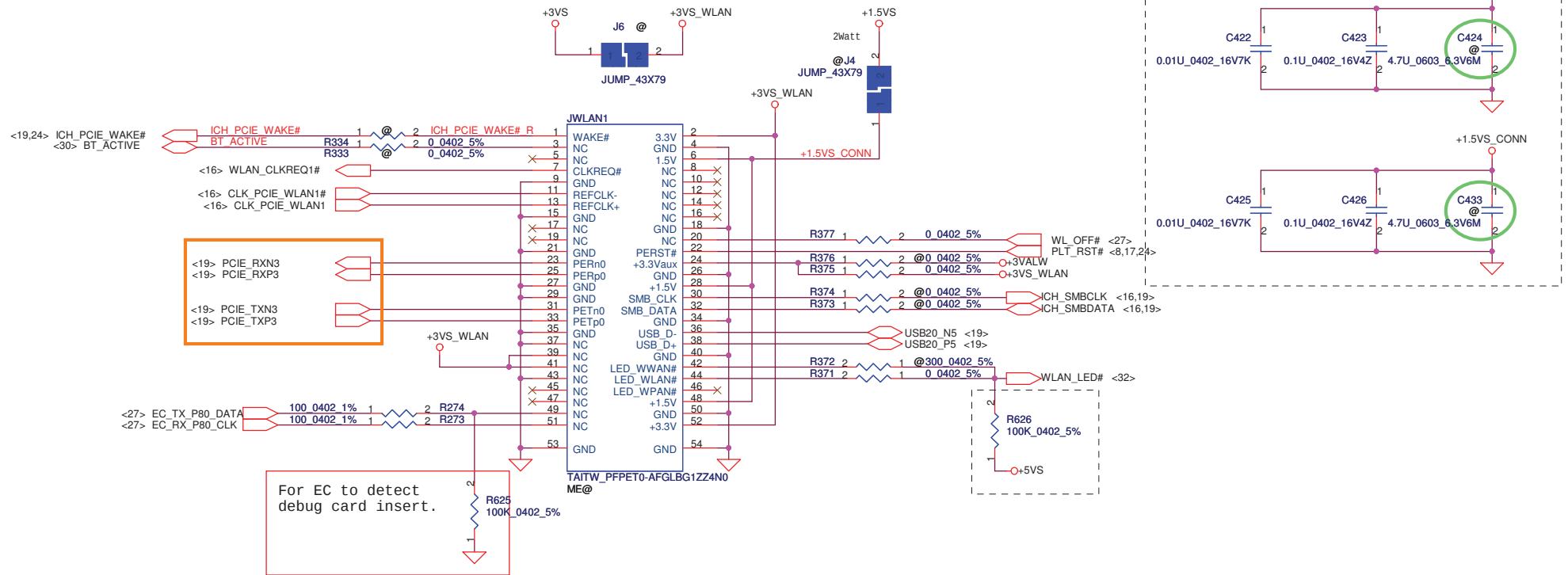
Change Q13 from SB00000EO10 to SB00000AR00.

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						Size B	Document Number			LA7011P		Rev 1.0	
						Date:		Friday, December 24, 2010		Sheet	21	of	41



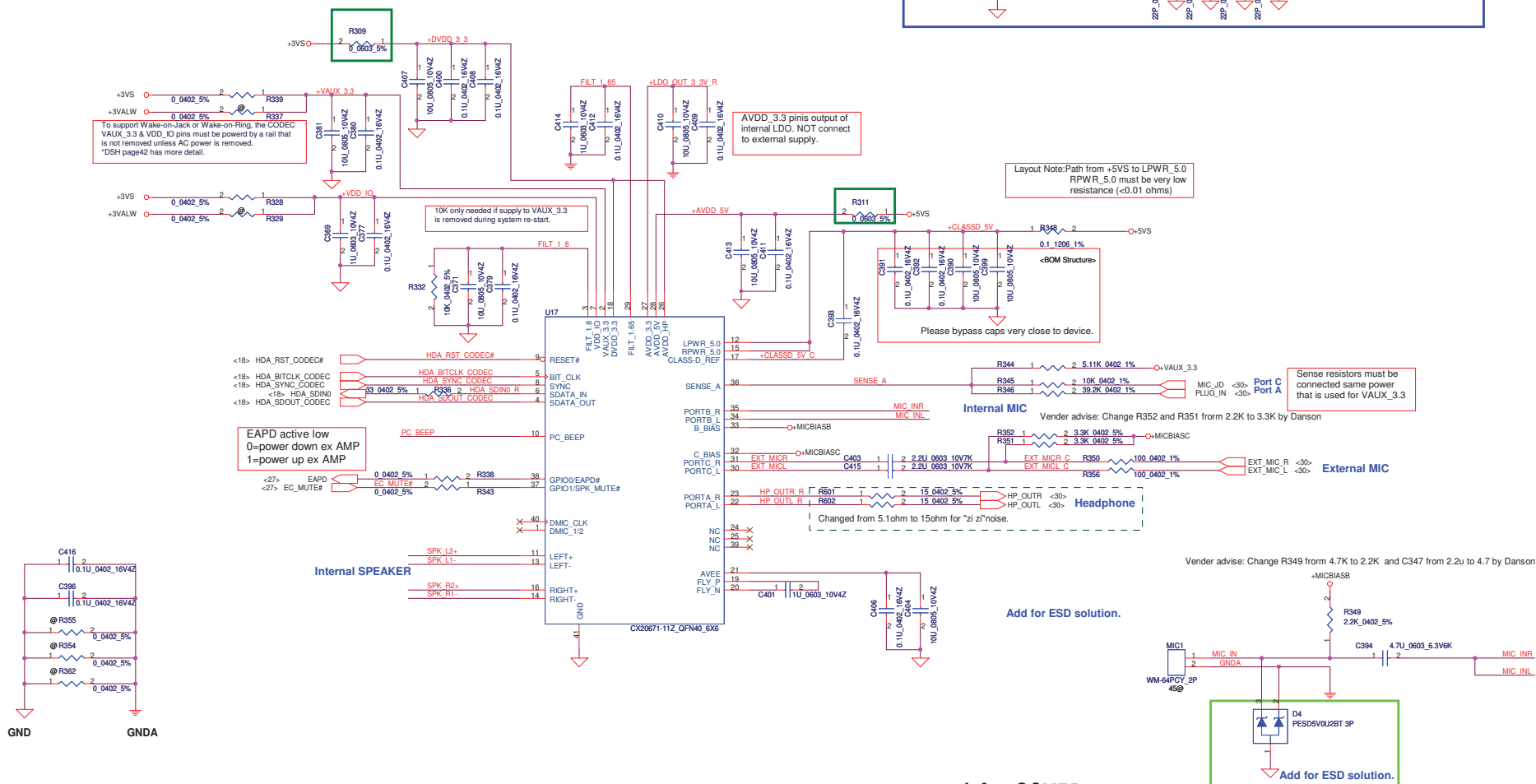
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				Date:	Friday, December 24, 2010
				Sheet	22 of 41

Mini-Express Card for WLAN(Half)

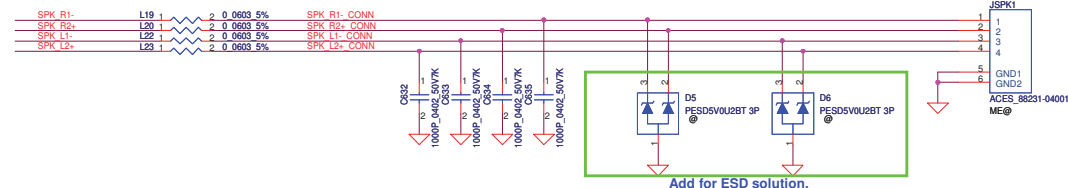
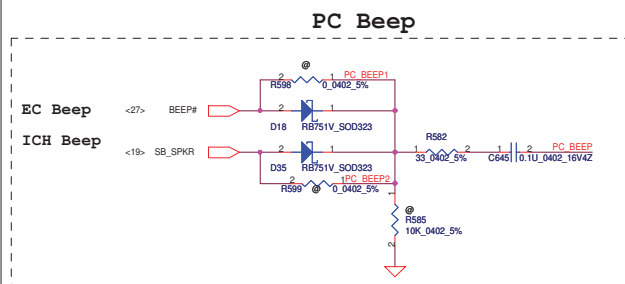


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				Document Number	1.0
				LA7011P	
				Date:	Friday, December 24, 2010
				Sheet	23 of 41

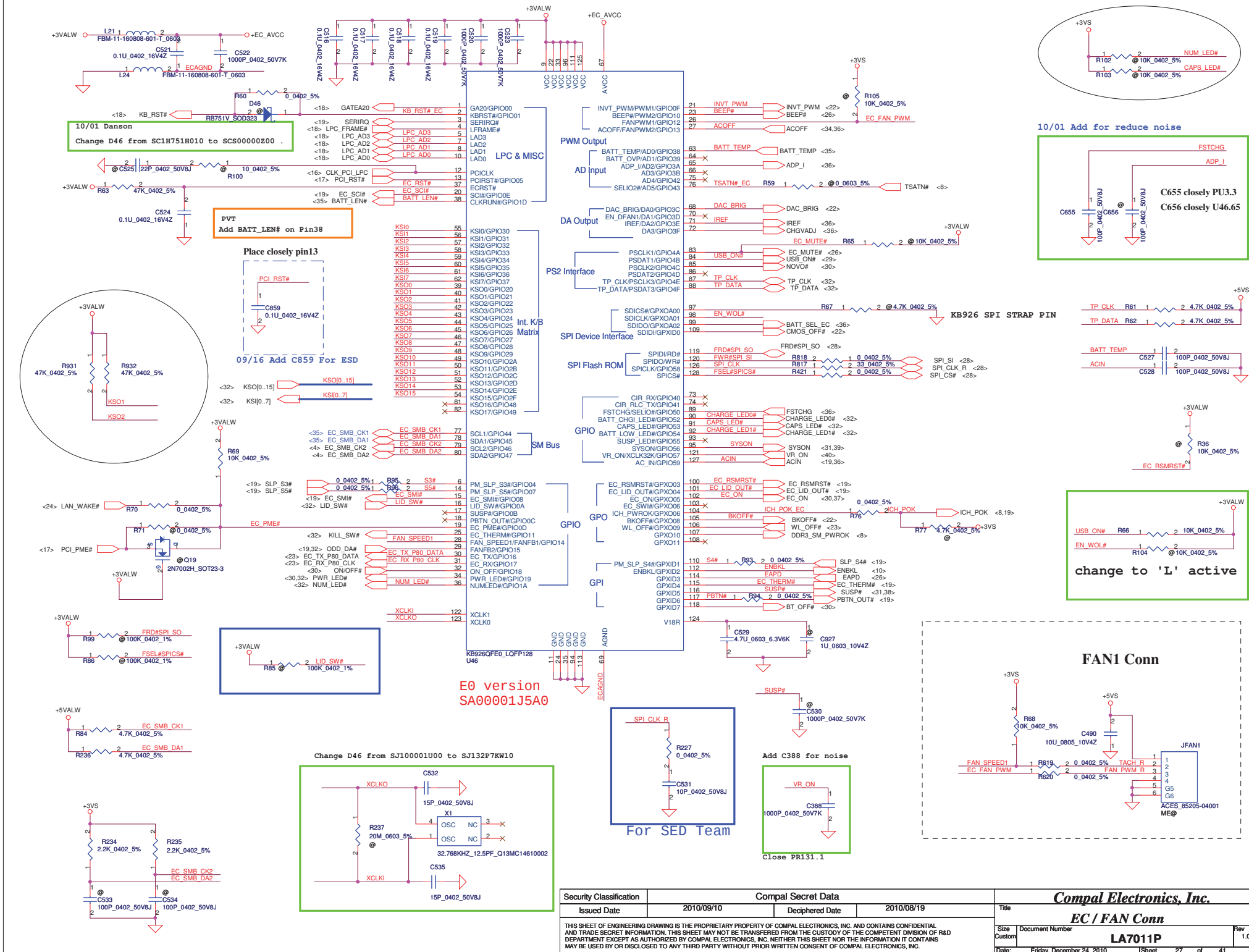
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



wide 20MIL



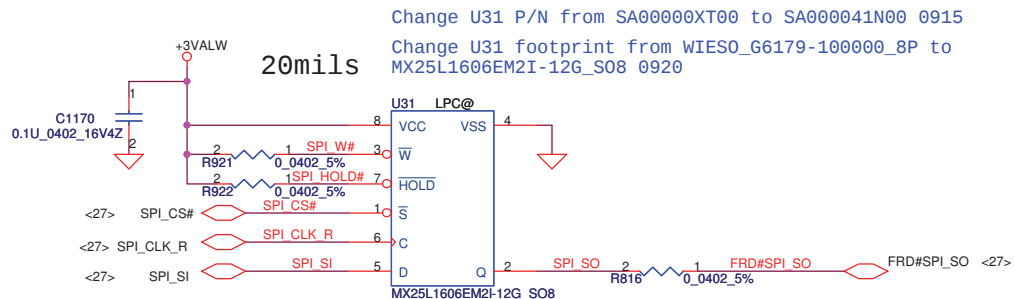
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>							
Issued Date		2010/09/10	Deciphered Date		2010/08/19	Title					
						CX20671 Codec					
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							Size	Document Number		New	
									LA7011P		
Date		Friday, December 24, 2010		Sheet	26	of 41					



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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title EC / FAN Conn		
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				Date: Friday, December 24, 2010 Sheet 27 of 41		

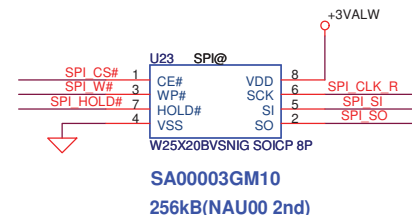
SPI Flash (16Mb*1)

FOR EC 16M SPI ROM

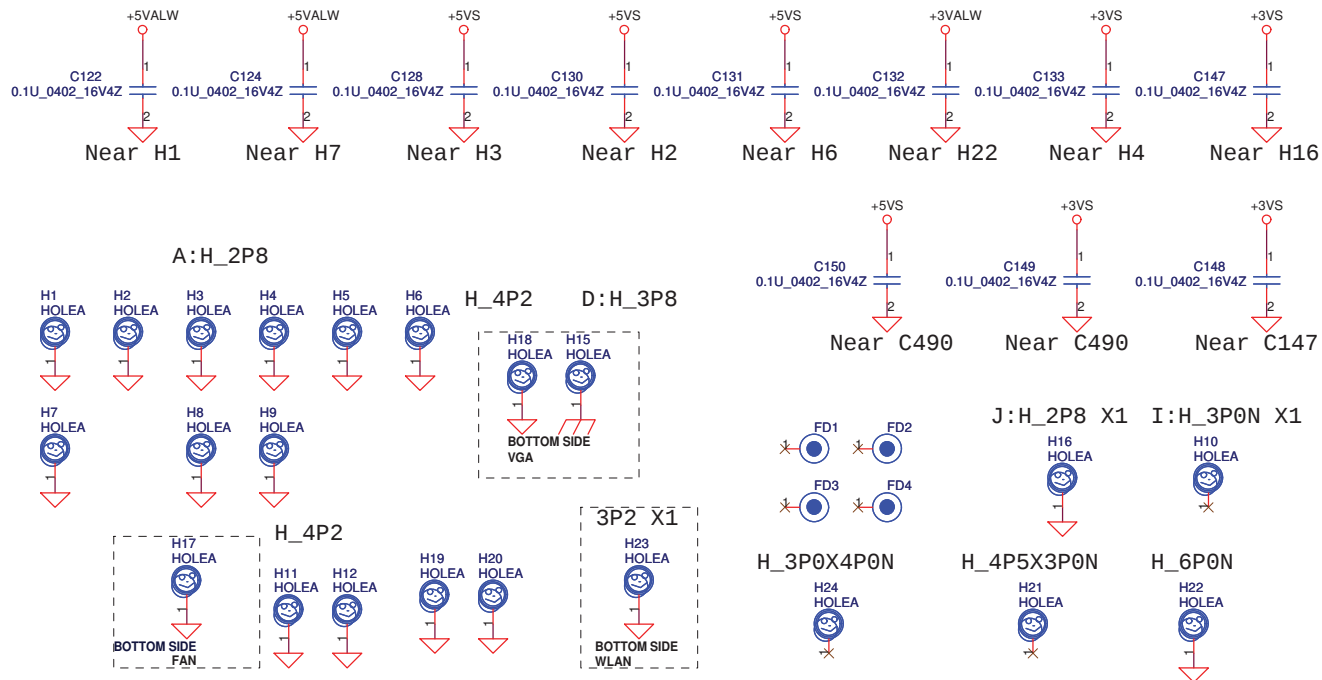
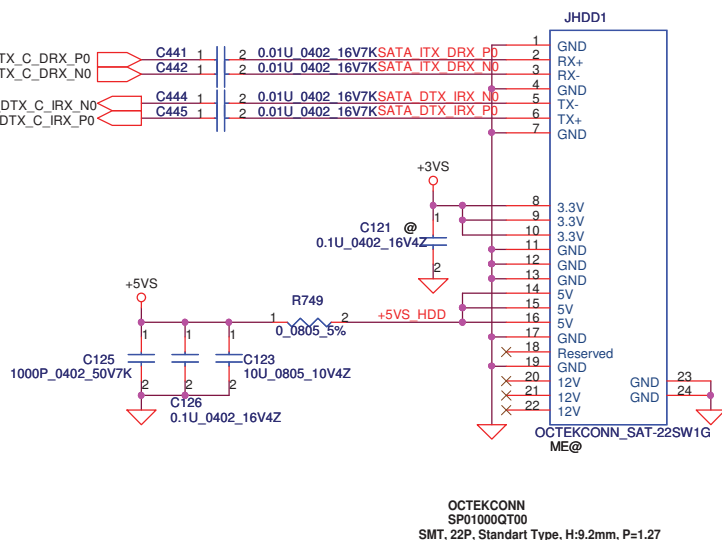


FOR EC 256K SPI ROM (NONShare ROM)

2010/09/24 Add U23 for NONShare SPI ROM.

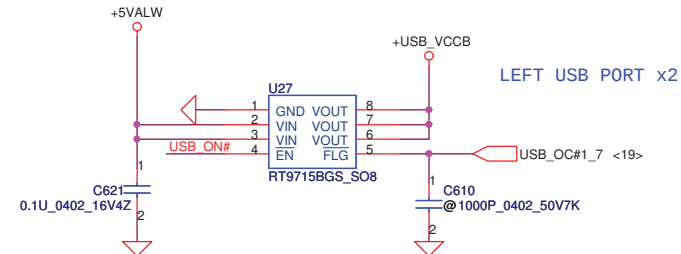
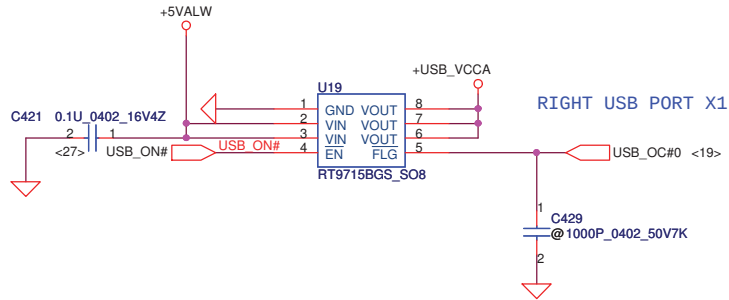


SATA HDD Conn.

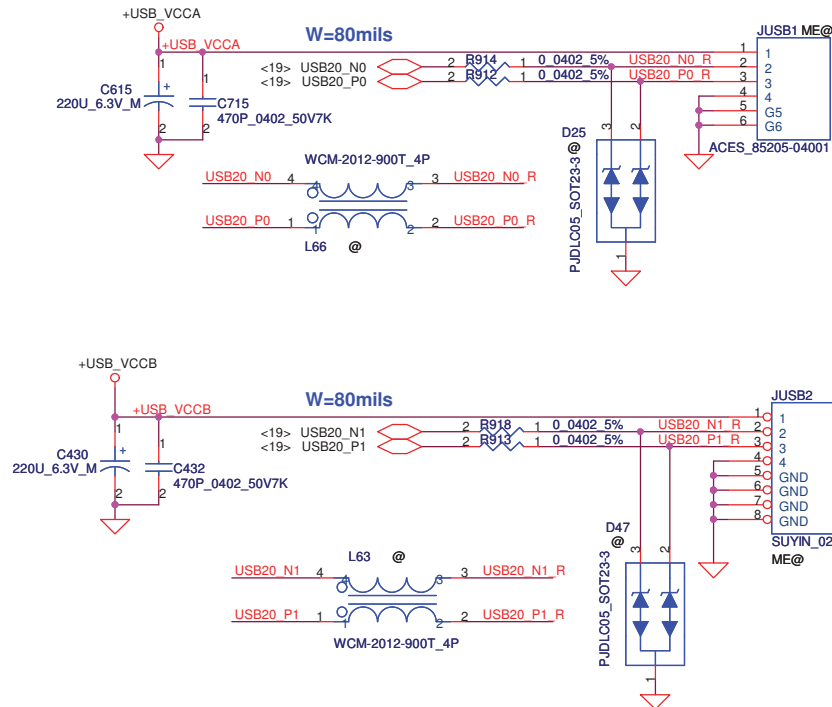
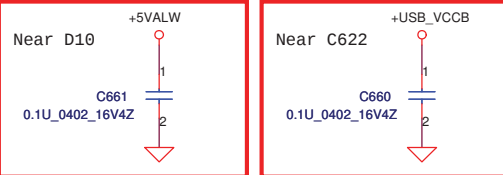


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				Size B	Document Number
				LA7011P	
Date: Friday, December 24, 2010		Sheet 28 of 41		Rev 1.0	

PVT Change U19 and U27 part number from SA000039E00 to SA00002XX00



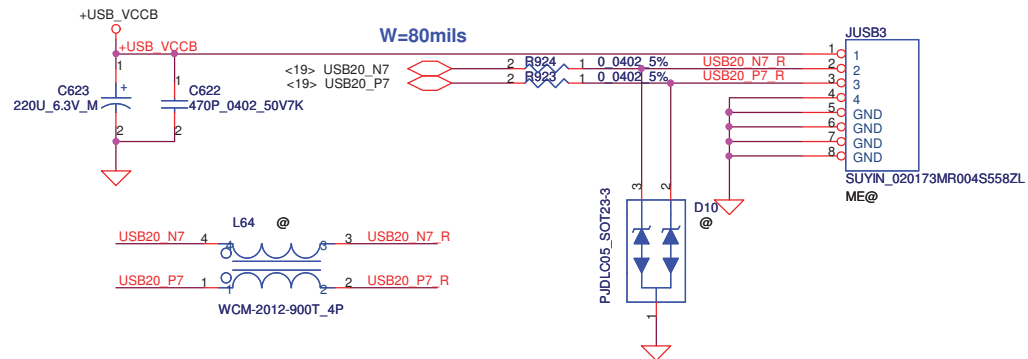
Pre MP ADD for ESD solution



Right USB Conn.

Left USB Conn.

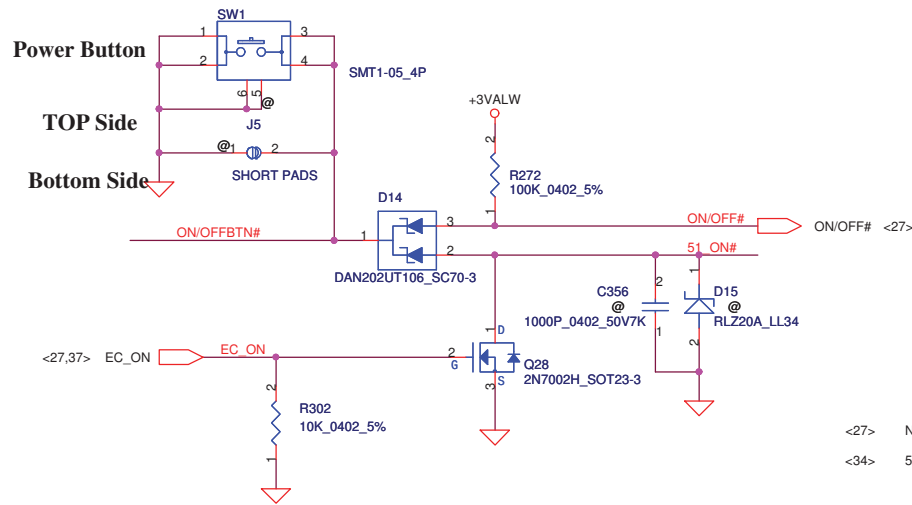
Change JUSB3 connector from ESATA to USB



Left2 USB Conn.

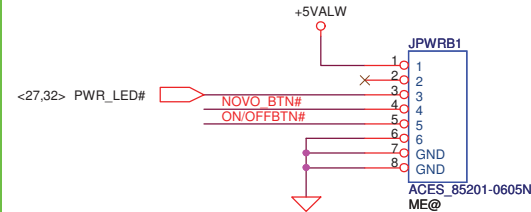
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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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Size B	Document Number	LA7011P		Rev 1.0	
Date:	Friday, December 24, 2010	Sheet	29	of	41

ON/OFF switch



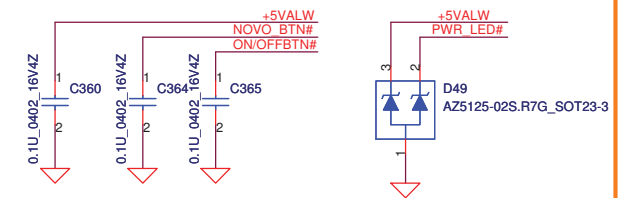
10/11 Change JPWRB1 P/N from SP010009010 to SP01000LB00

Add C359 to PWR_LED# for ESD solution.

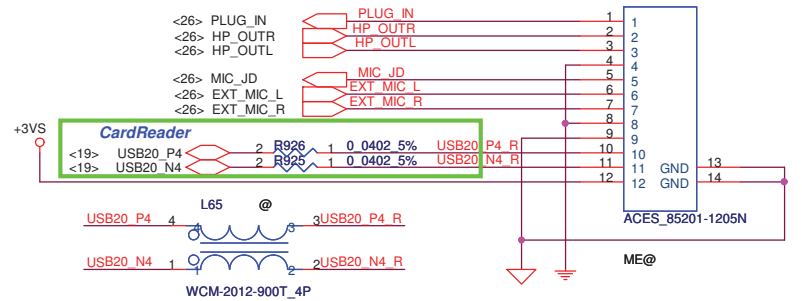


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

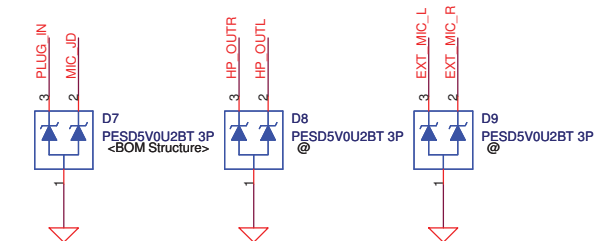
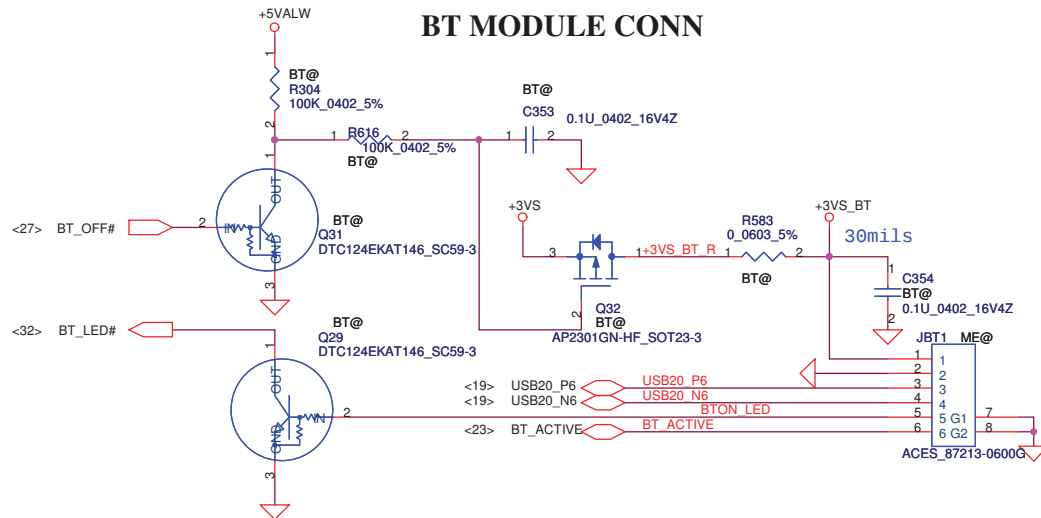
PVT ESD solution.



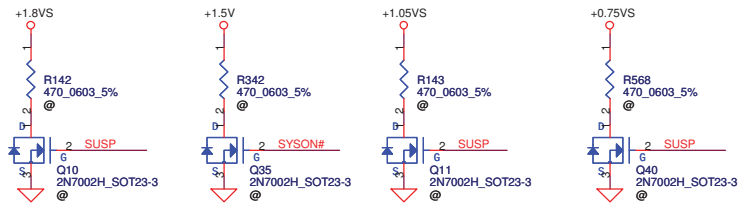
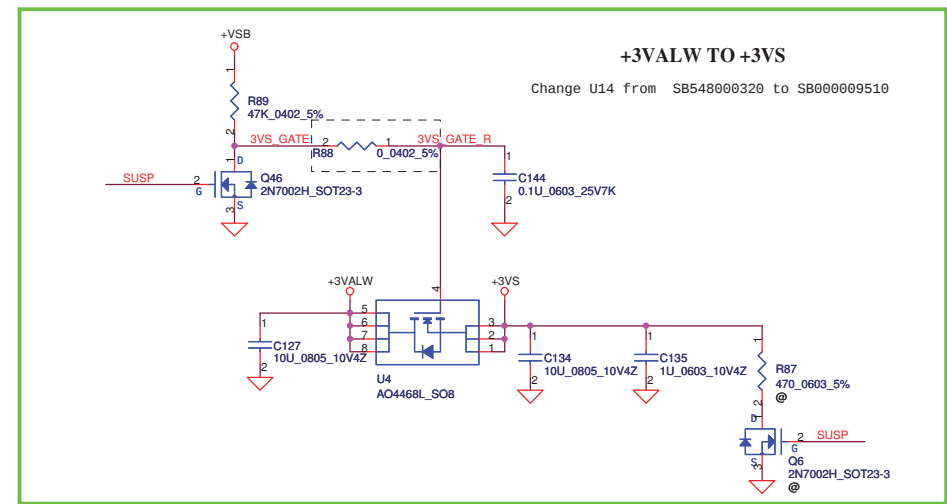
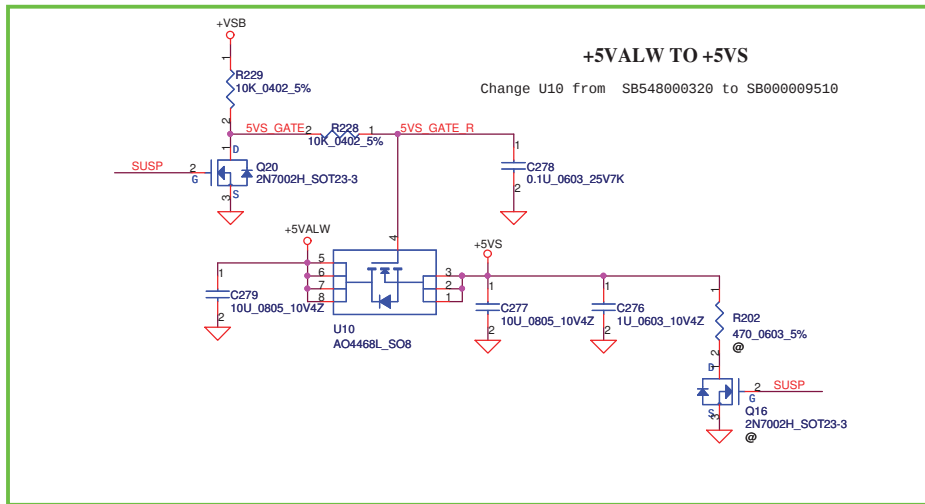
Card Reader/Audio Jack SB CONN



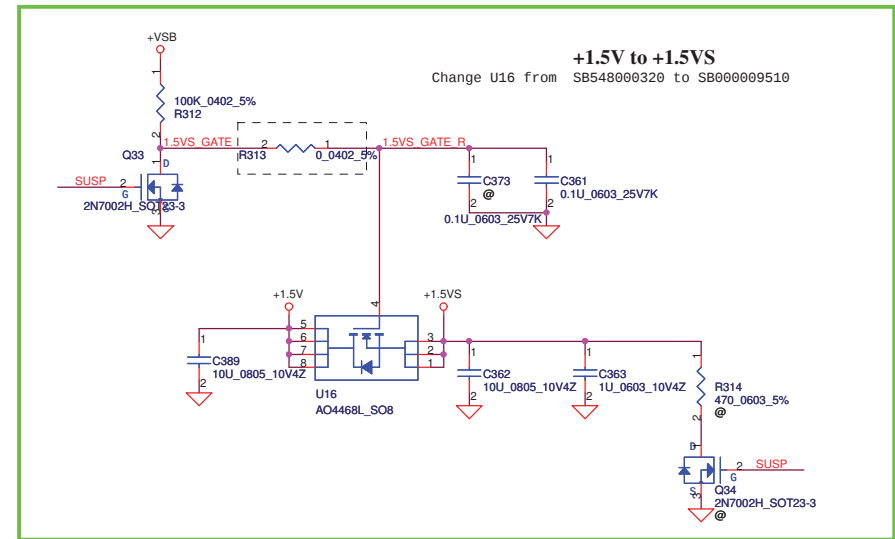
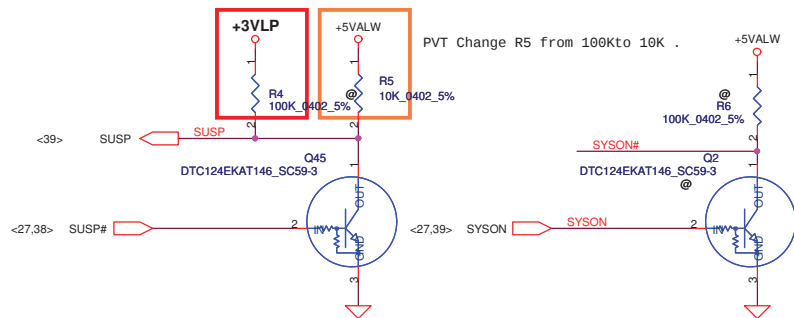
BT MODULE CONN



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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	Audio Jack & SW & BT Conn.
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				LA7011P	
				Date: Friday, December 24, 2010	Sheet 30 of 41

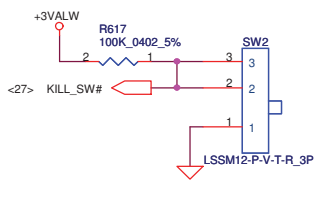


Pre MP Change SUSP pull high from +5VALW to +3VLP



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Size	Custom	Document Number	LA7011P	Rev	1.0
Date:	Friday, December 24, 2010	Sheet	31	of	41

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON



LED1

White

<27,30> PWR_LED#

LED1 5V 300_0402_5%

19-213A-T1D-CP202HY-3T_WHITE

LED2

Orange

BATT_LOW_LED#

<27> CHARGE_LED1#

LED2 3V 300_0402_5%

White

BATT_CHG_LED#

<27> CHARGE_LED0#

LED2 5V 470_0402_5%

18-225A-S2T3D-C01-3T_ORG-WHITE

LED3

White

<23> WLAN_LED#

LED3 5V 300_0402_5%

19-213A-T1D-CP202HY-3T_WHITE

LED4

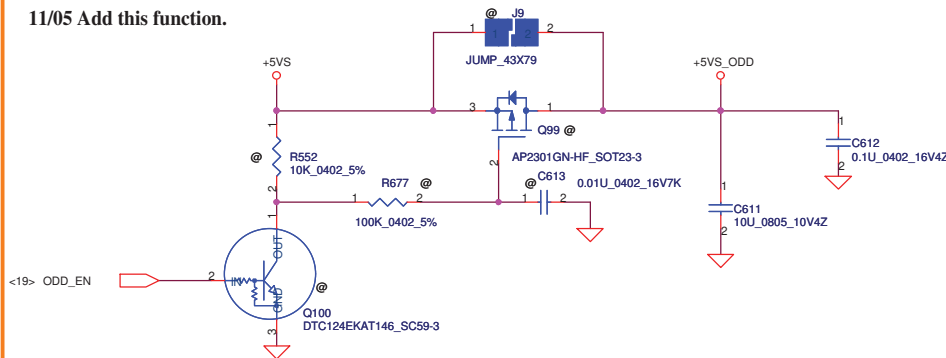
White

<18> HDD_LED#

LED4 5V 300_0402_5%

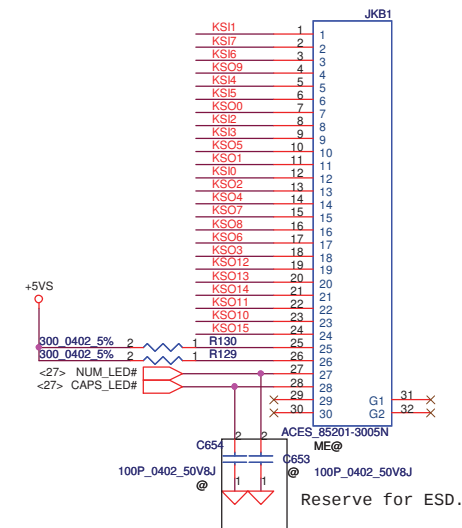
19-213A-T1D-CP202HY-3T_WHITE

11/05 Add this function.



<27>		KS[0..7]	KSIO[0..7]			
<27>		KSQ[0..15]	KSQIO[0..15]			
100P	0402	50V8J	2	1	C721	KSQ0
100P	0402	50V8J	2	1	C722	KS01
100P	0402	50V8J	2	1	C723	KS02
100P	0402	50V8J	2	1	C724	KS03
100P	0402	50V8J	2	1	C725	KS04
100P	0402	50V8J	2	1	C726	KS05
100P	0402	50V8J	2	1	C727	KS06
100P	0402	50V8J	2	1	C728	KS07
100P	0402	50V8J	2	1	C729	KS08
100P	0402	50V8J	2	1	C730	KS09
100P	0402	50V8J	2	1	C731	KS010
100P	0402	50V8J	2	1	C732	KS011
100P	0402	50V8J	2	1	C733	KS012
100P	0402	50V8J	2	1	C734	KS013
100P	0402	50V8J	2	1	C735	KS014
100P	0402	50V8J	2	1	C736	KS015
100P	0402	50V8J	2	1	C737	KSIO
100P	0402	50V8J	2	1	C738	KSII
100P	0402	50V8J	2	1	C739	KSIZ
100P	0402	50V8J	2	1	C740	KSIS
100P	0402	50V8J	2	1	C741	KSIA
100P	0402	50V8J	2	1	C742	KSIS
100P	0402	50V8J	2	1	C743	KSIE
100P	0402	50V8J	2	1	C744	KSIT

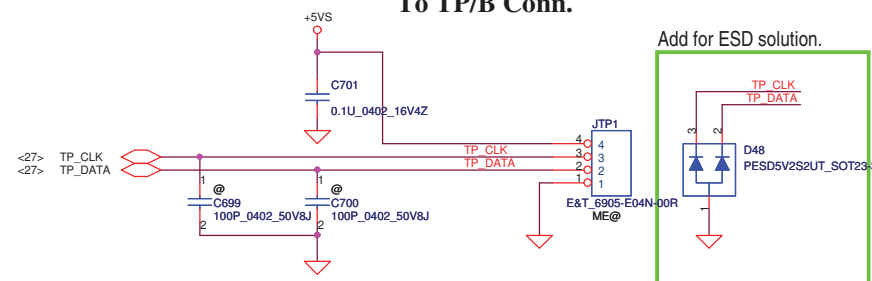
Reserve for ESD.



Reserve for ESD.

check connector & pin define.

CONN PIN define need double check



The schematic diagram illustrates the internal wiring of a SATA to SATA-Express adapter. It shows the connection between SATA signals and SATA-Express signals through various resistors and capacitors.

Top Section (SATA Signals):

- SATA_1TX_C_DRX_P1** and **SATA_1TX_C_DRX_N1** are connected to **C428** and **C431** (10k capacitors).
- SATA_DTX_C_IRX_N1** and **SATA_DTX_C_IRX_P1** are connected to **C437** and **C439** (10k capacitors).
- These signals are connected to the SATA controller pins: **0.01U_0402_16V7K SATA_1TX_DRX_P1**, **0.01U_0402_16V7K SATA_1TX_DRX_N1**, **0.01U_0402_16V7K SATA_DTX_IRX_N1**, and **0.01U_0402_16V7K SATA_DTX_IRX_P1**.

Bottom Section (SATA-Express Signals):

- ODD_DA#** is connected to **R717** (0.0402 5% resistor) and **R554** (0.0402 5% resistor).
- ODD_DETECT#** is connected to **R554** and **R555** (0.0402 5% resistor).
- +3VSD** is connected to **R555** and **10K_0402_5%** resistor.
- The signals are connected to the SATA-Express controller pins: **8 DP+**, **9 +5V**, **10 +5V**, **11 MD**, **12 GND**, and **13 GND**.

Right Side (SATA-Express Connector):

- The connector pins are labeled: **GND**, **A+**, **A-**, **GND**, **B-**, **B+**, **GND**, **DP+**, **+5V**, **+5V**, **MD**, **GND**, **GND**.
- The connector is labeled **OCTEK_SLS-13SB1G_RV** and **ME@**.

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KB/TP/LID/KLL/ODD/LED FOR 14

Document Number

LA7011P

Date:

Friday, December 24, 2010

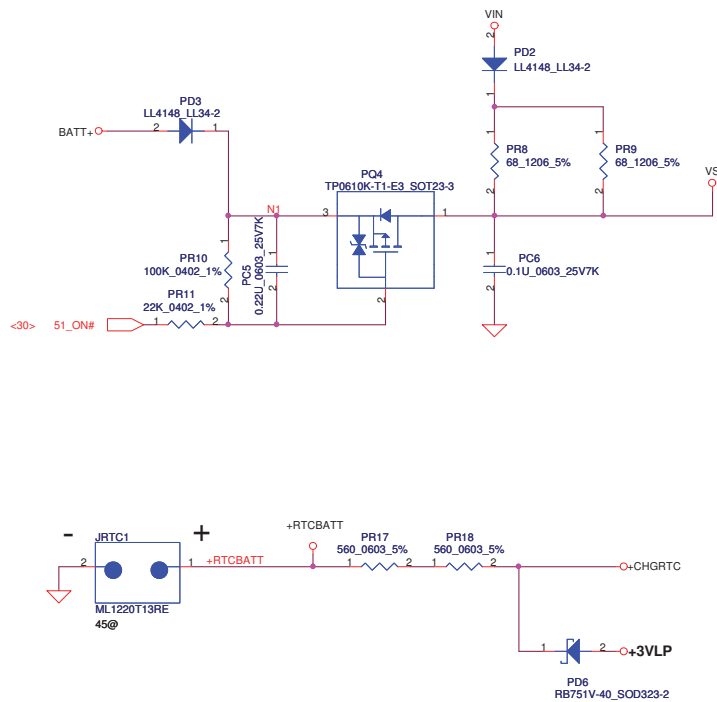
Sheet 32 of 41

Version change list (P.I.R. List)

Page 1 of 1 for HW

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
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				Size	Document Number	Rev
				Custom	LA7011P	1.0
Date: Friday, December 24, 2010				Sheet	33 of 41	

[illegible]

The schematic diagram illustrates the internal circuitry of the T1-E3_SOT23-3 device, divided into two main functional blocks: PreCHG and MAINPWON.

PreCHG Section:

- VIN Input:** Connected to a voltage divider network consisting of resistors PR1 (1K_1206_5%), PR2 (1K_1206_5%), PR3 (1K_1206_5%), and PR6 (1K_1206_5%).
- PD1:** A diode (LL4148_LL34-2) connected in series with the voltage divider.
- PQ1:** A MOSFET (TP0610K-T1-E3_SOT23-3) used for charging, controlled by a gate driver circuit.
- Gate Driver:** Includes a diode PD2 (PDTCT115EU_SOT323-3) and a MOSFET PQ2 (PDTCT115EU_SOT323-3).
- ACOFF Input:** Connected to a diode PD4 (RB715F_SOT323-3) and a MOSFET PQ3 (PDTCT115EU_SOT323-3).
- B+ Output:** The output of the PreCHG section.

MAINPWON Section:

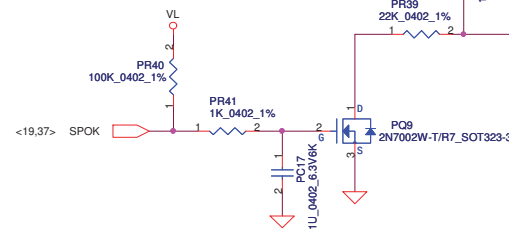
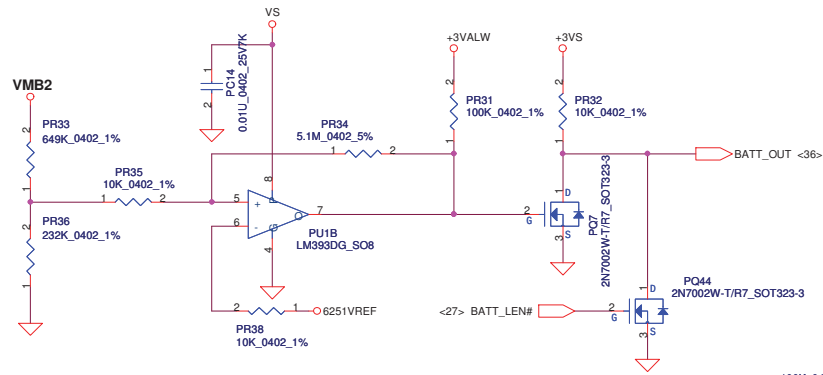
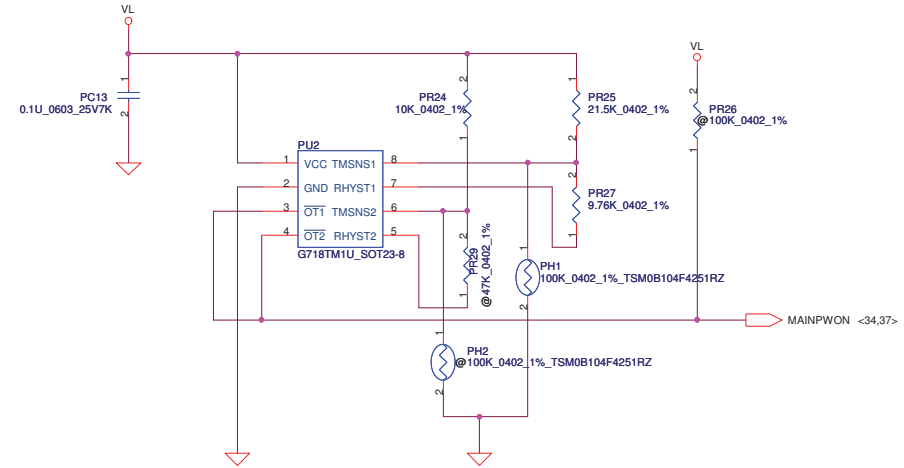
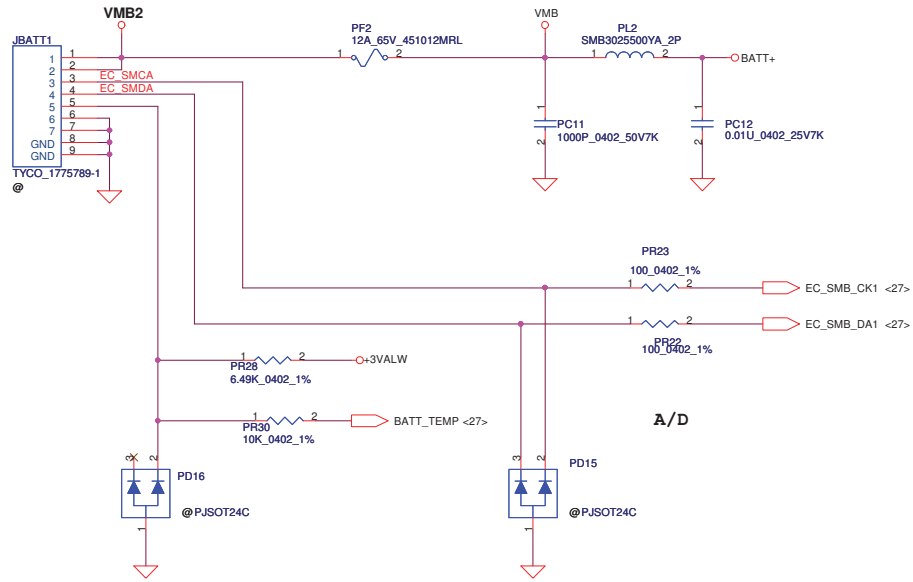
- VL Input:** Connected to a diode PD5 (RB715F_SOT323-3) and a MOSFET PQ5 (2N7002W-T/R7_SOT323-3).
- VS Input:** Connected to a diode PD7 (PDTCT115EU_SOT323-3) and a MOSFET PQ6 (PDTCT115EU_SOT323-3).
- ACON Input:** Connected to a diode PD5 (RB715F_SOT323-3) and a MOSFET PQ5 (2N7002W-T/R7_SOT323-3).
- PC8:** A capacitor (0.1U_0603_25V7K) connected to the VS input.
- PC9:** A capacitor (0.1U_0603_25V7K) connected to the VS input.
- PC10:** A capacitor (0.1U_0603_25V7K) connected to the VS input.
- PR12:** A resistor (2.2M_0402_5%) connected to the VS input.
- PR19:** A resistor (34K_0402_1%) connected to the VS input.
- PR21:** A resistor (6.5K_0402_1%) connected to the VS input.
- PR23:** A resistor (47K_0402_1%) connected to the VS input.
- PACIN Input:** Connected to a diode PD5 (RB715F_SOT323-3) and a MOSFET PQ5 (2N7002W-T/R7_SOT323-3).
- +5VALW Output:** The output of the MAINPWON section.

	Precharge detector		
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

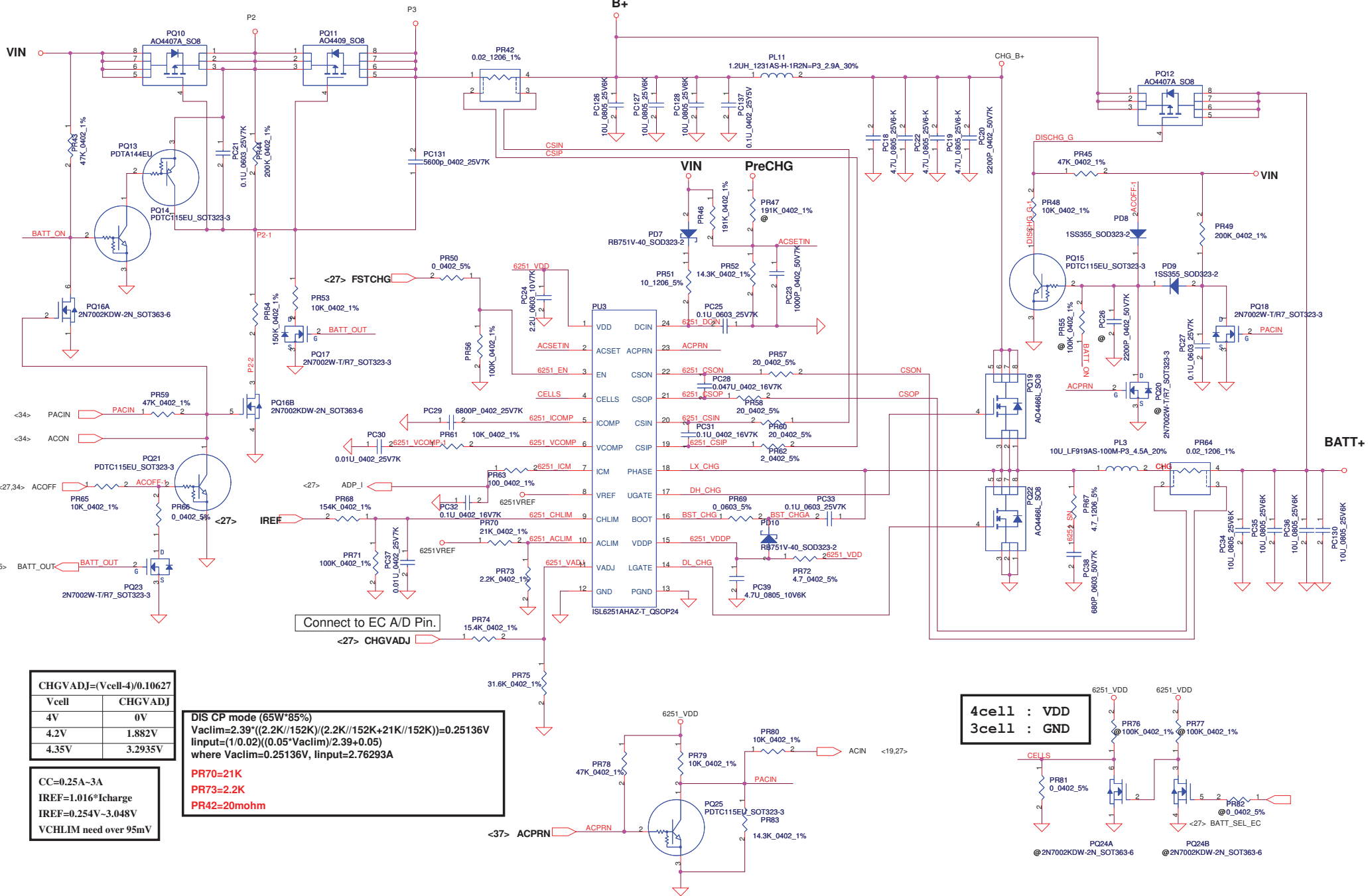
	Precharge detector		
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

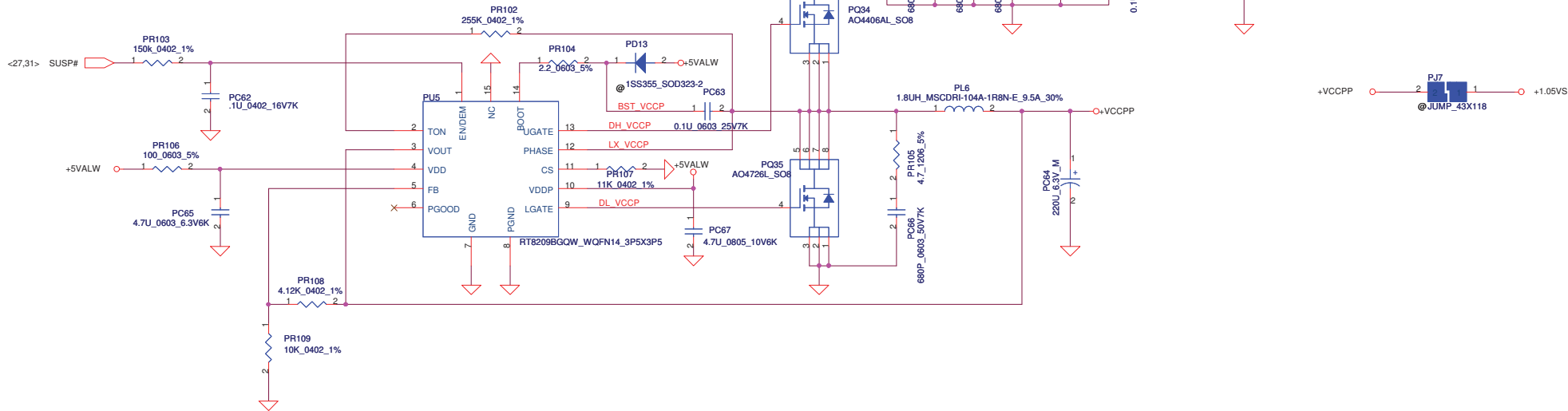
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				Size Customer	Document Number
				Date:	Friday, December 24, 2010
				Sheet	34 of 41

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

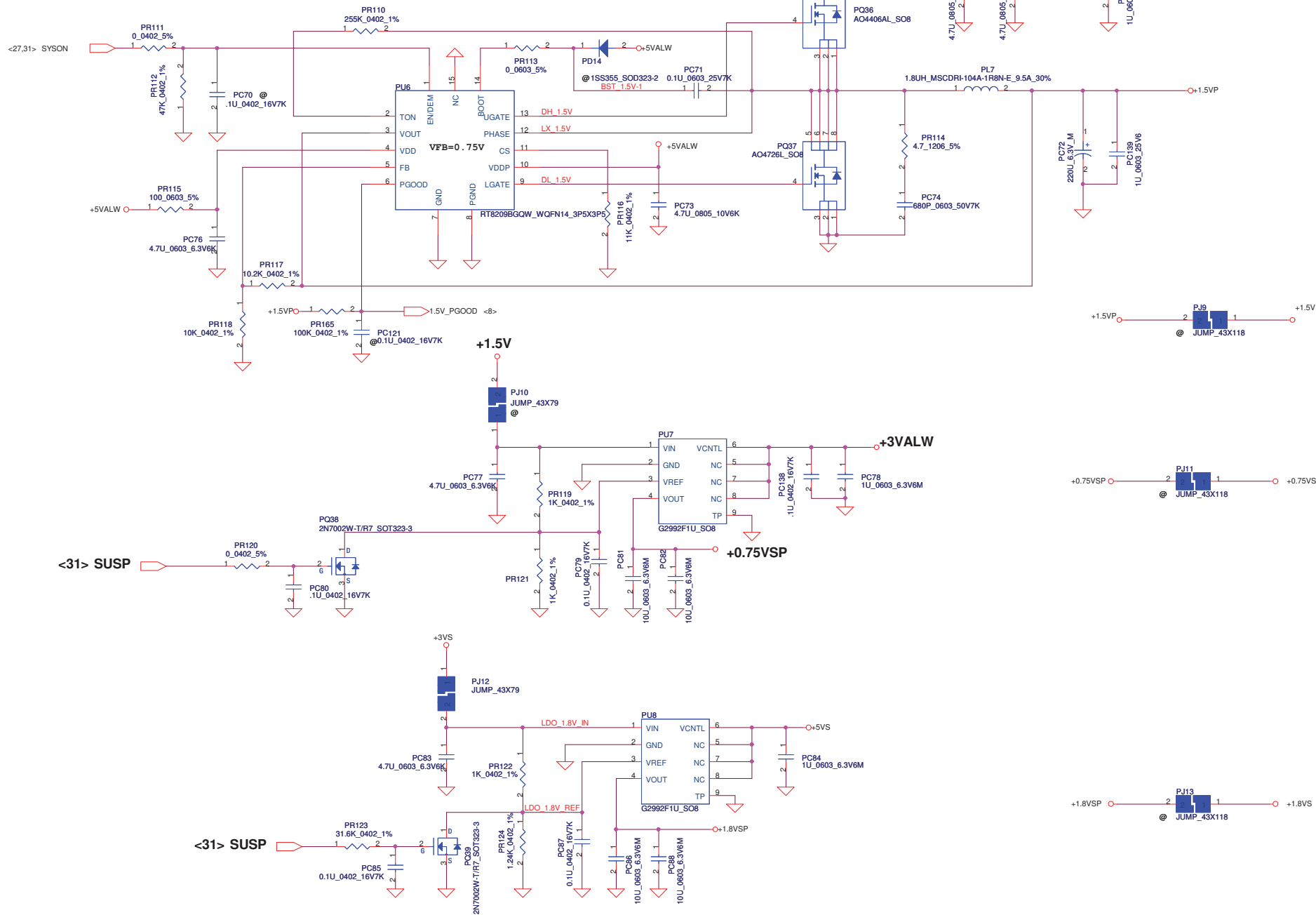


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Size				Document Number				Rev			
Date				Friday, December 24, 2010				Sheet 35 of 41			





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Size	Document Number	Rev		1.0	
Date:	Friday, December 24, 2010	Sheet	38 of 41		



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								Document Number			
								Date			
								Friday, December 24, 2010			
								Sheet			
								39 of 41			
								Rev			
								1.0			

Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damaged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transistor, the design margin of PQ11 is not enough.	Add PQ44
p39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

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				Date:	Friday, December 24, 2010
				Sheet	41 of 41