

ZZZ1

PCB
15'DAZ@

ZZZ2

LA-7012P
15'DA@

ZZZ3

LS-7012P
15'DA@

ZZZ4

LS-7013P
15'DA@

ZZZ5

LS-7014P
15'DA@

Compal Confidential

Schematics Document

PAW20

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	Cover Sheet
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Clock Generator
SLG8SP556VTR

page16

Mobile Penryn

uPGA-478 CPU

page4, 5, 6

For 14"
LS-7011P 4PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

For 15"
LS-7012P 8PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

H_A#(3..35)
H_D#(0..63)



FSB
667/800MHz

CRT Connector

page21

LVDS
Connector

page22

Intel Cantiga GMCH

GM45

uFCBGA 1329

page 7, 8, 9, 10, 11, 12, 13



Dual Channel
DDR3-667/800(1.5V)

DDR3-SO-DIMM X2

BANK 0, 1, 2, 3

page 14,15

up to 4G

DMI *4



C-Link



2Channel Speaker
page26

Analog MIC_Int
page26

**Wire Less Mini
card Slot 1**

page23

6*PCL-E BUS

Intel ICH9-M

page 17,18,19,20

**SPI ROM
BIOS**

LPC BUS



EC

ENE KB926 E0

page27

AR8151/8152

10/100/Giga LAN

page24

RJ45 CONN

page25

AZALIA

14*USB2.0

6*SATA serial

Audio Codec
CONEXTAN
CX20671

page26

CMOS Camera

page22

BlueTooth CONN

page30

USB CONN X1(Right)

page29

USB PORT X1(Left)

page29

USB PORT X1(Left)

page29

Audio Jack SB CONN
HP X 1+
MIC_Ext X1
Card Reader RTS5139

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SATA HDD CONN

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SATA ODD CONN

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Touch Pad

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Int.KBD

page32

**SPI ROM
BIOS**

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DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Thermal
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
DDR SO-DIMM	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

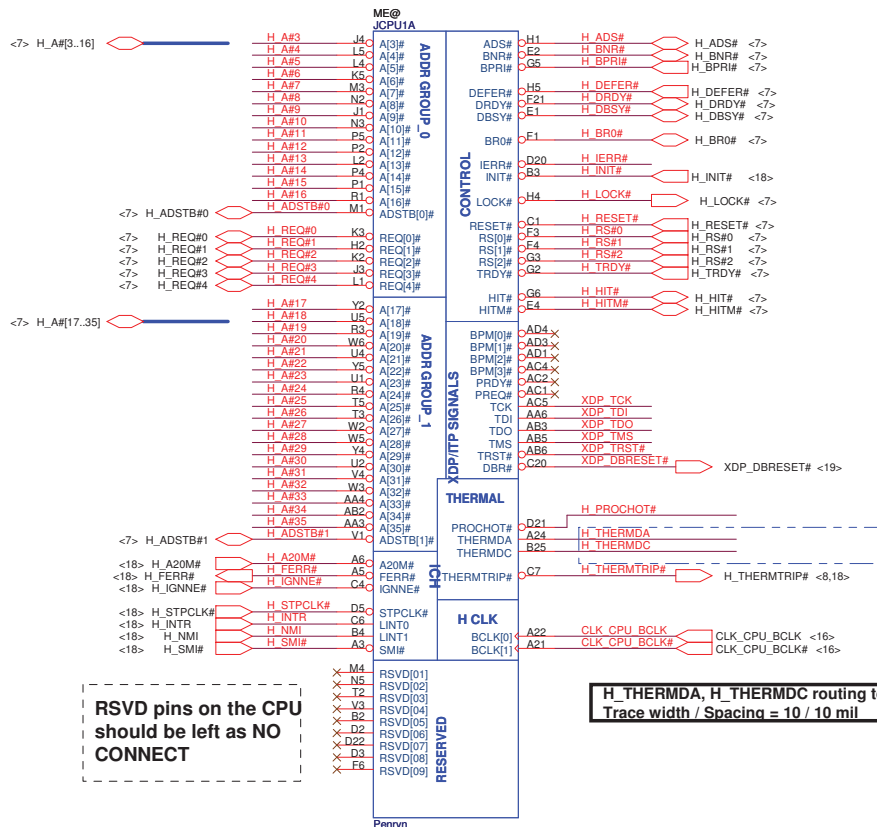
Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

PCIE PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

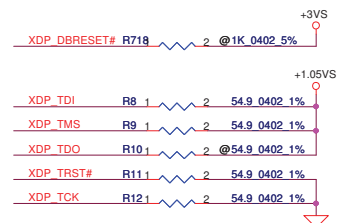
USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT (ESATA)
8	
9	
10	
11	
12	
13	

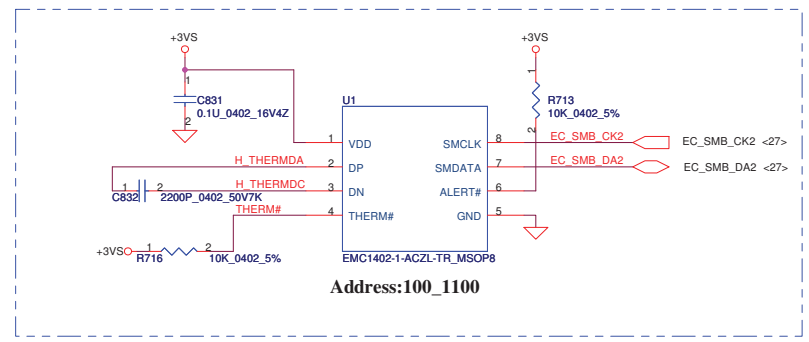
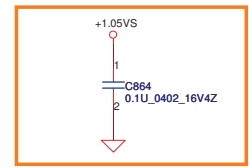


**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

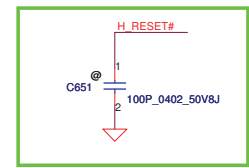
SDP Reserve for debug , Please close to CPU side



**PVT ESD solution.
Please close to R715**

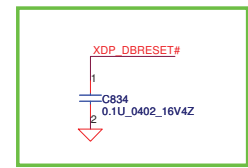


10/01 Add for reduce noise



Place closely pin C1

09/16 Add C834 For ESD



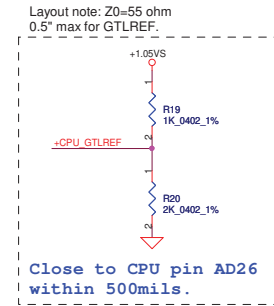
Place closely pin C20

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Compal Electronics, Inc.
Penryn(1/3)-AGTL+THM,FAN

LA7012P

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

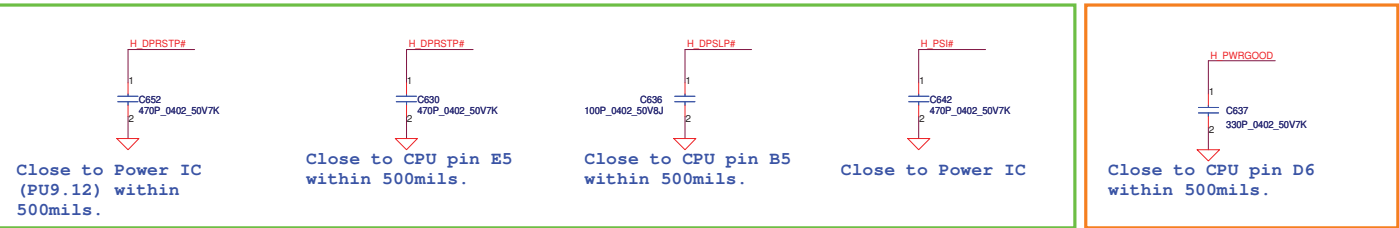


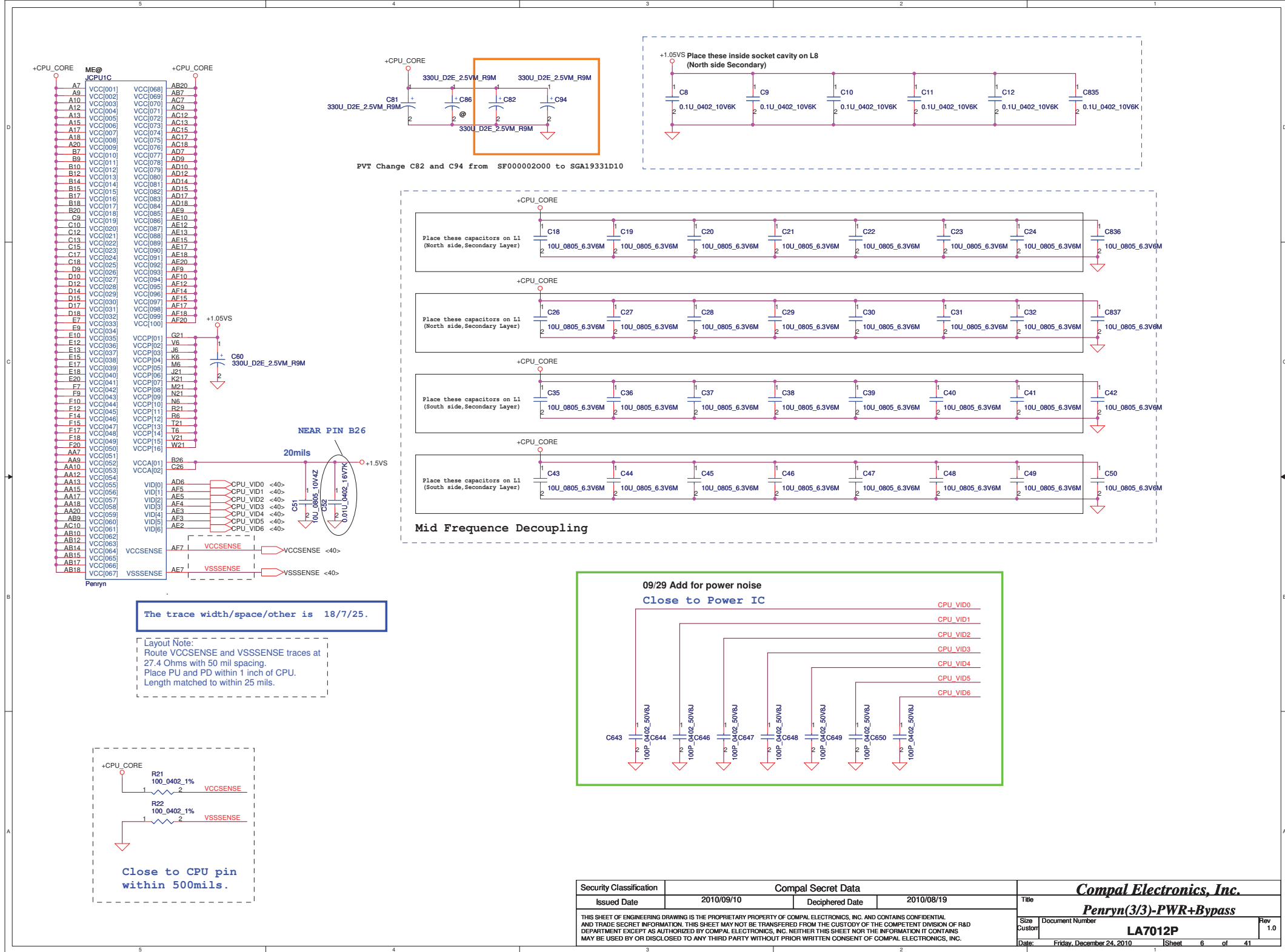
TRACE CLOSELY CPU < 0.5"

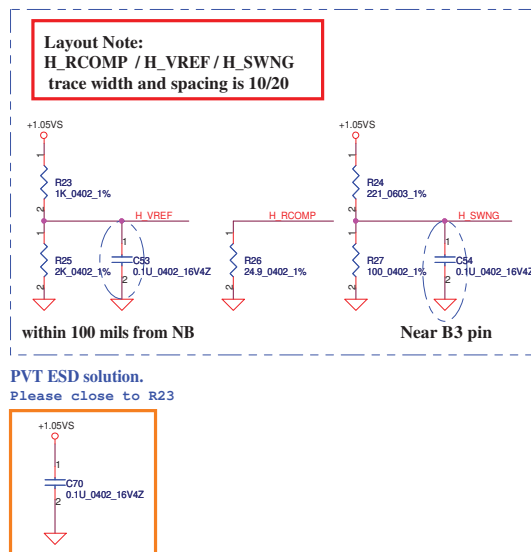
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

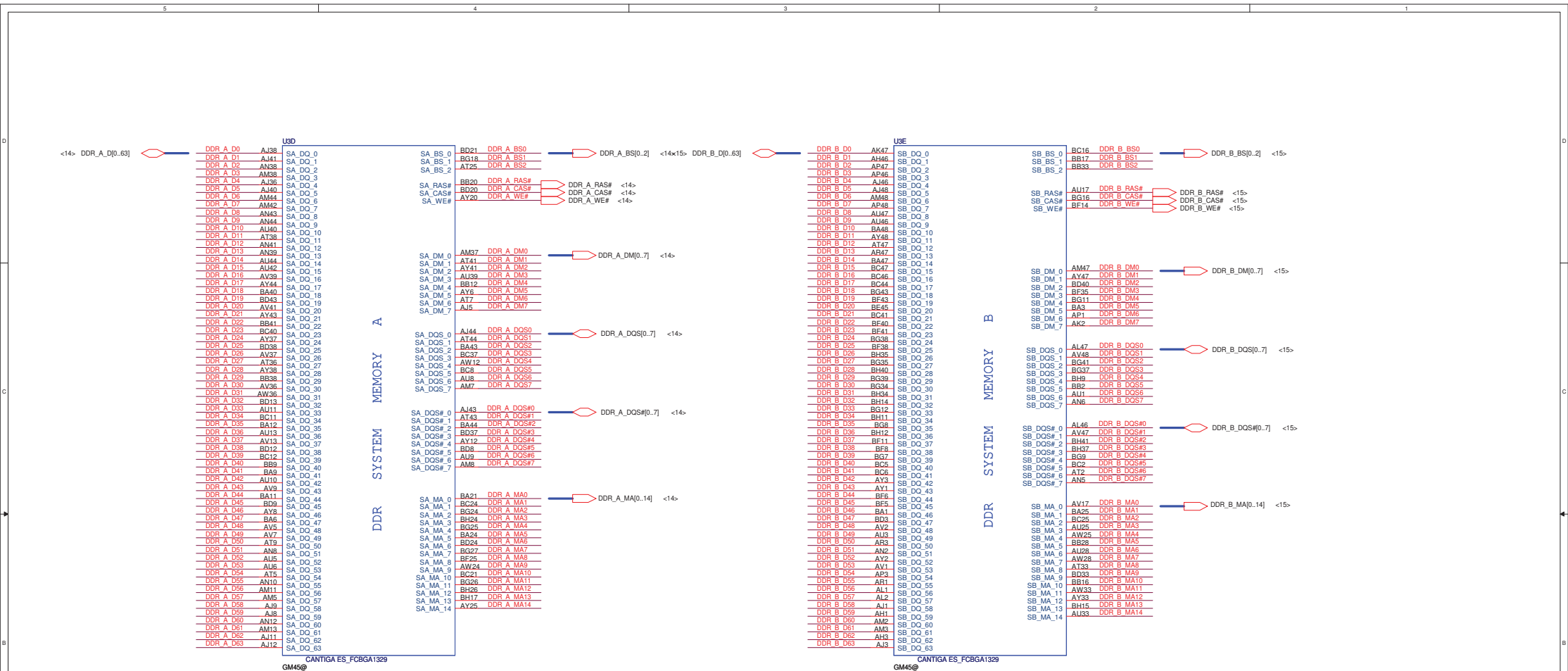
09/29 Add for power noise

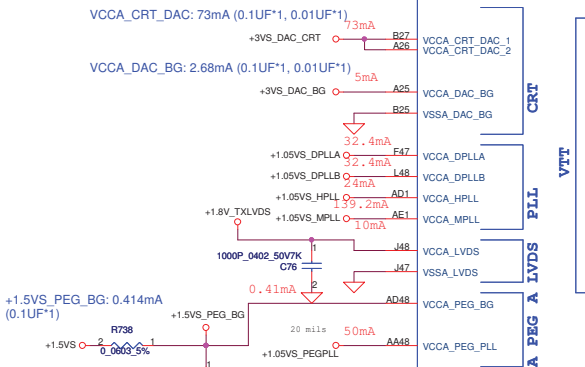
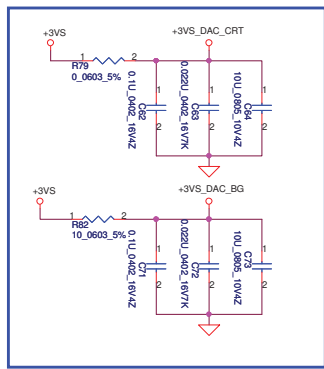






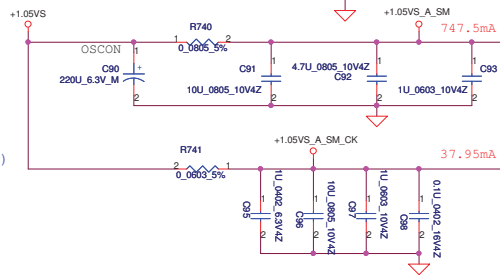
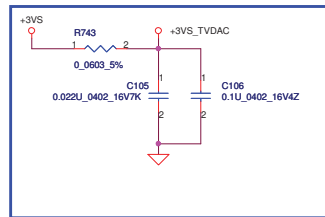
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VCCA_SM:720mA
(22UF*2, 4.7UF*1, 1UF*1)

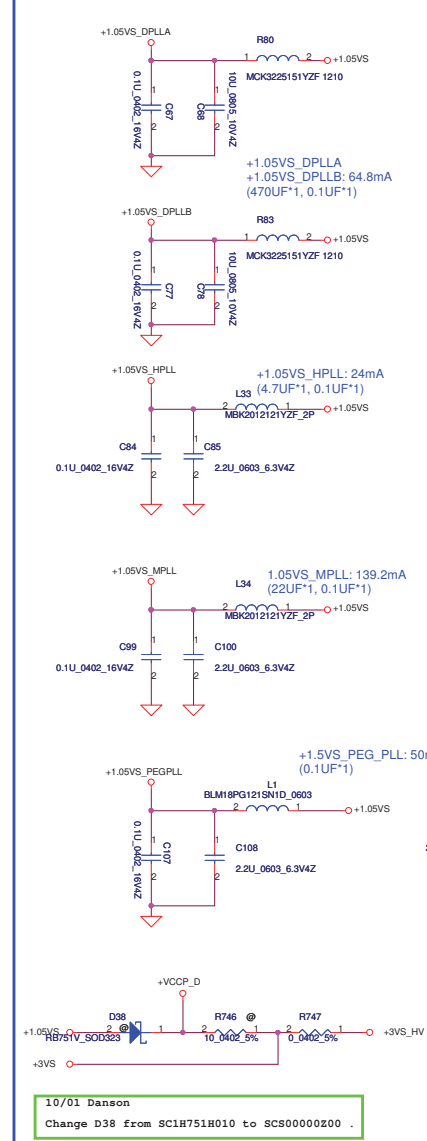
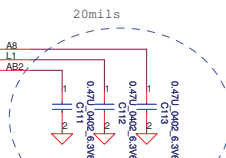
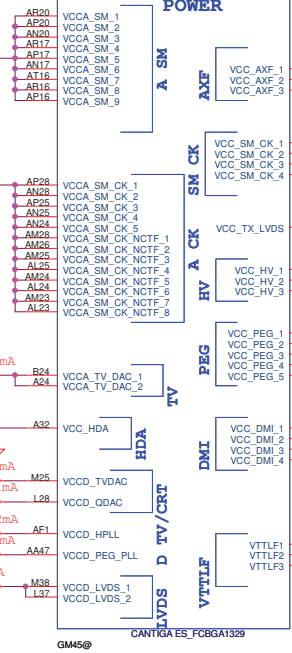
VCCA_SM_CK:220mA
(22UF*1, 2.2UF*1, 0.1UF*1)



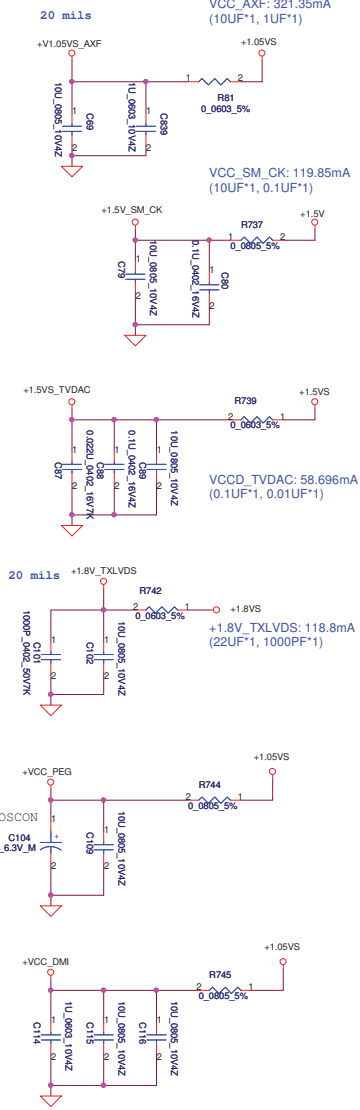
+3VS_TV_DAC: 40mA
(0.1UF*1, 0.01UF*1 for each DAC)

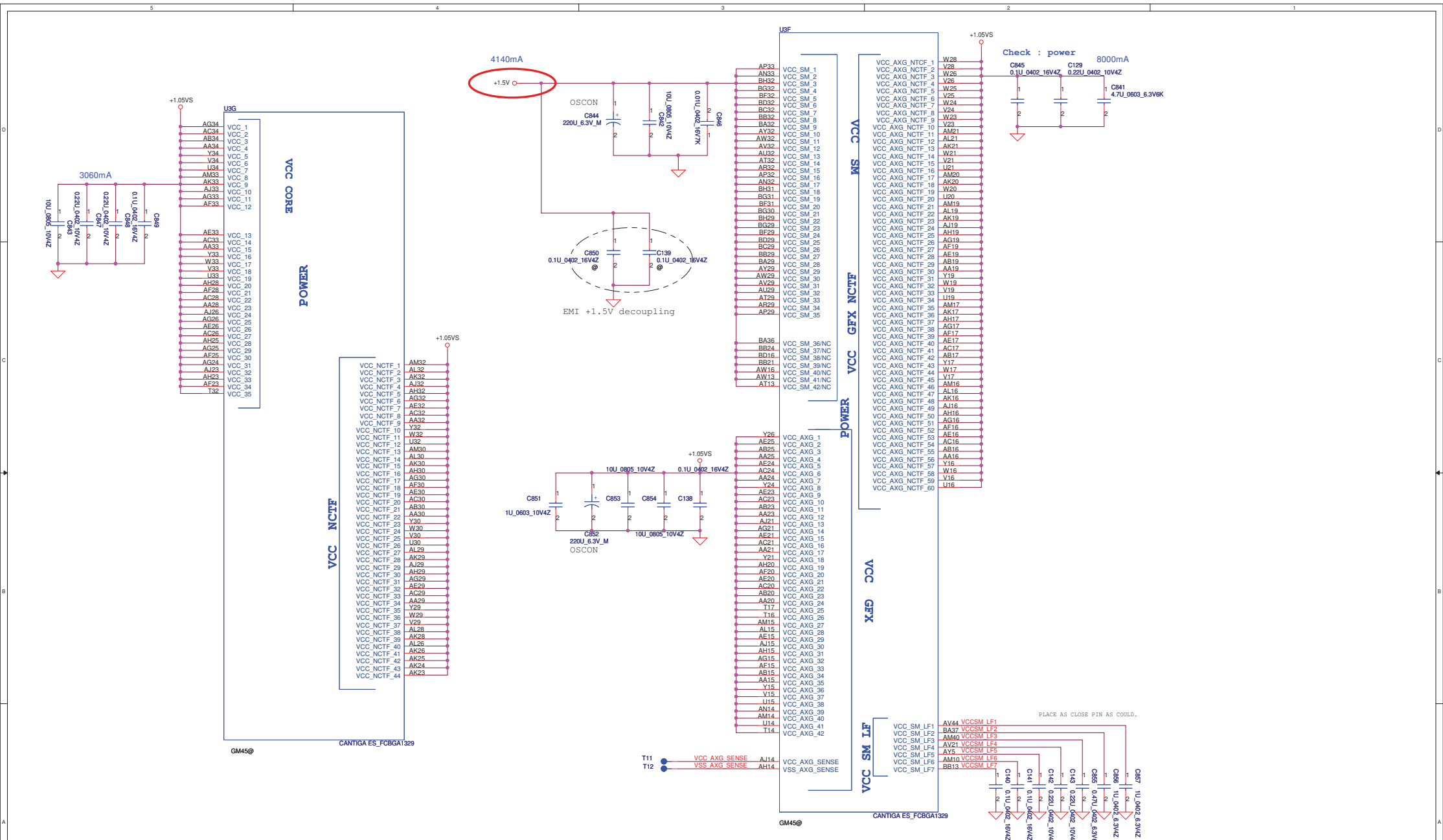
+1.5VS_TV_DAC: 48.363mA
(0.1UF*1, 0.01UF*1)

+1.8V_LVDS: 60.311111mA
(1UF*1)

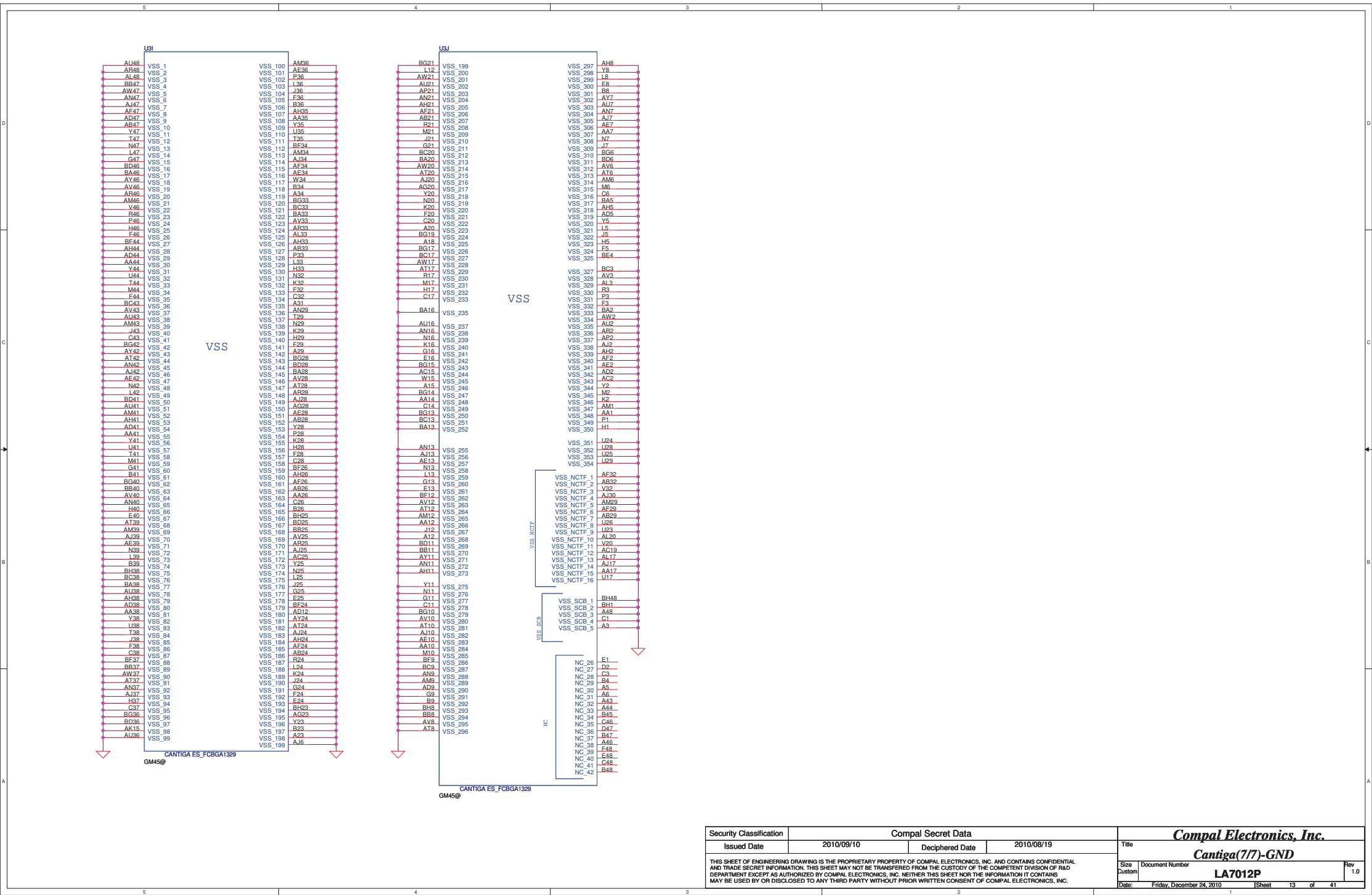


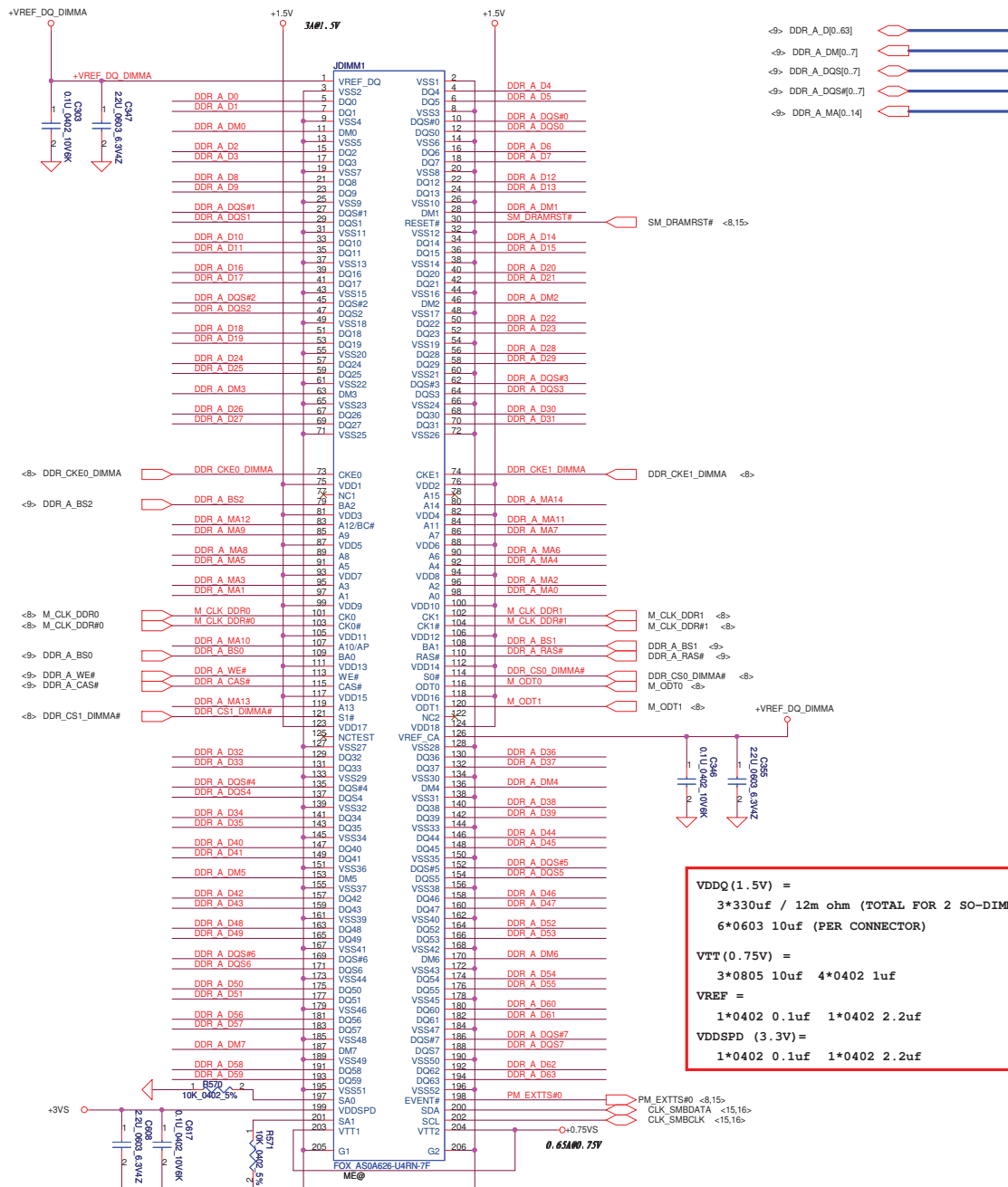
10/01 Danson
Change D38 from SC1H751H010 to SC500000Z00 .





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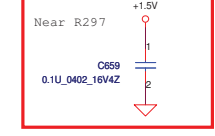




DDR3 SO-DIMM A H=4mm Reverse type

- <-> DDR_A_D[0..63]
- <-> DDR_A_DM[0..7]
- <-> DDR_A_DQS[0..7]
- <-> DDR_A_DQS#0..7]
- <-> DDR_A_MA[0..14]

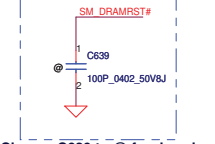
Pre MP ADD for ESD solution



For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.

07/17/2009

Place closely pin JDIMM1.30



1224 Change C639 to @ for download image fail issue

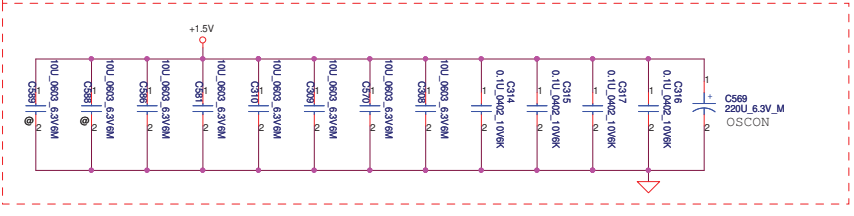
Layout Note:
Place near DIMM

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf





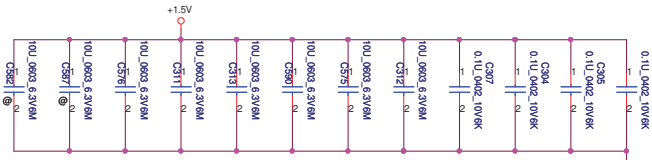
DDR3 SO-DIMM A H=8mm Reverse type

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

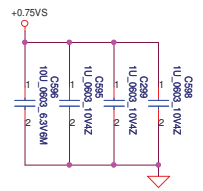
VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VDDSPD(3.3V) =
1*0402 0.1uf 1*0402 2.2uf
1*0402 0.1uf 1*0402 2.2uf

Layout Note:
Place near DIMM



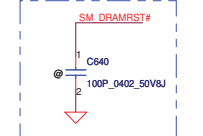
Layout Note:
Place near DIMM

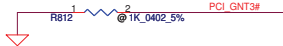
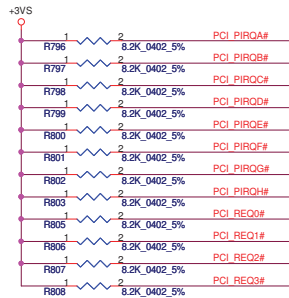
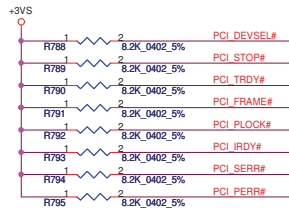


For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.

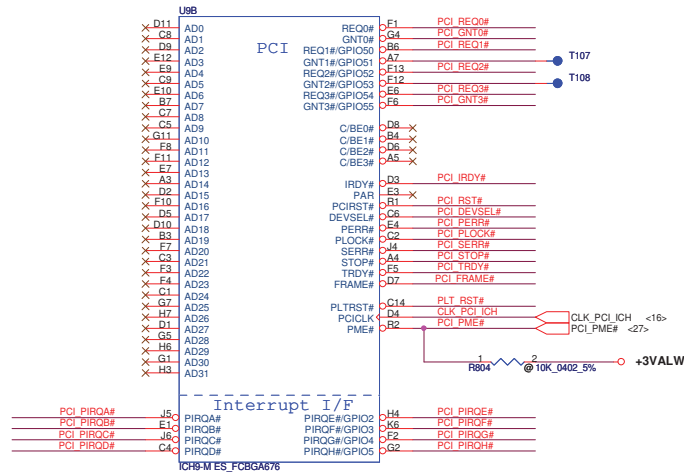
07/17/2009

Place closely pin JDIMM2.30





A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

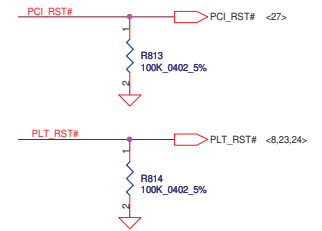
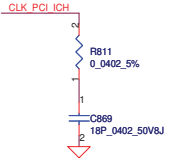


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

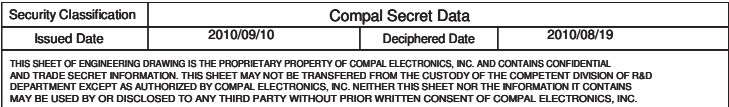
09/16 Add C858 For ESD
Place closely pin C14

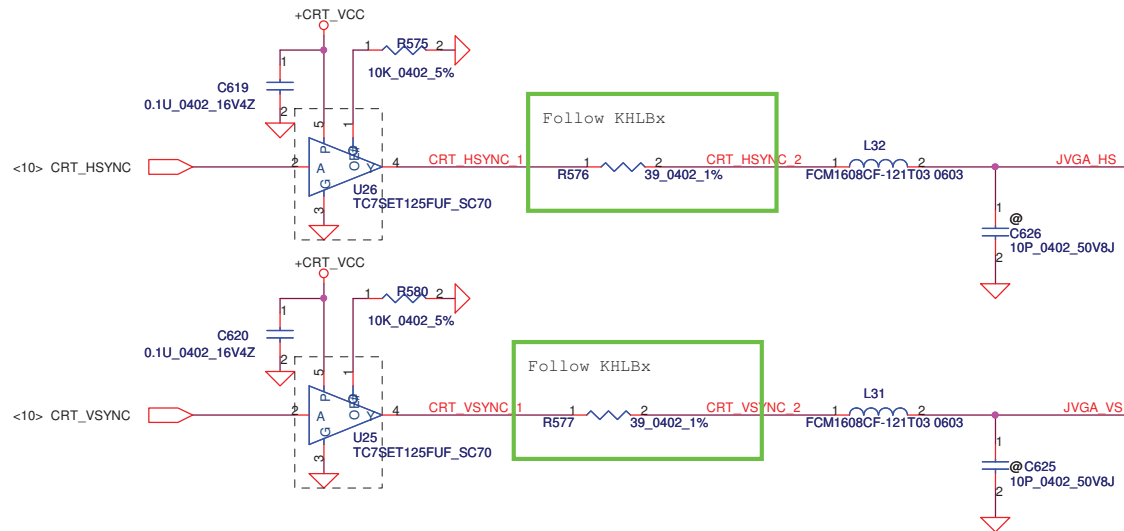
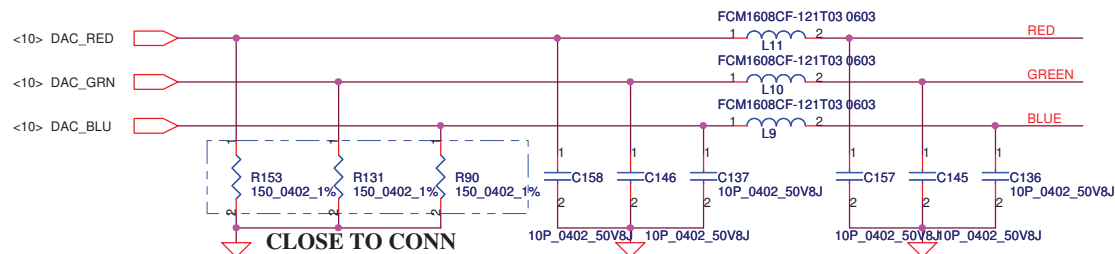
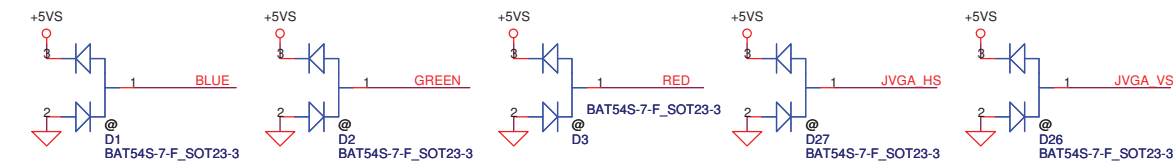


Place closely pin D4

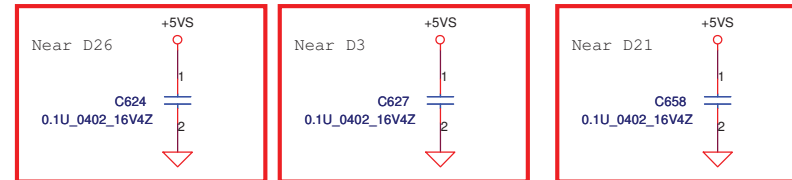


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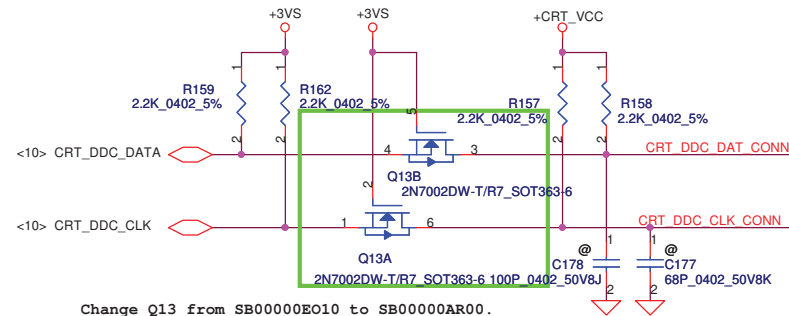
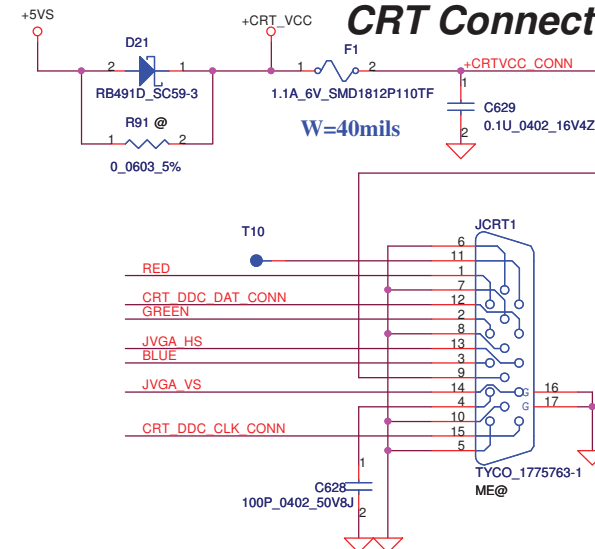




Pre MP ADD for ESD solution

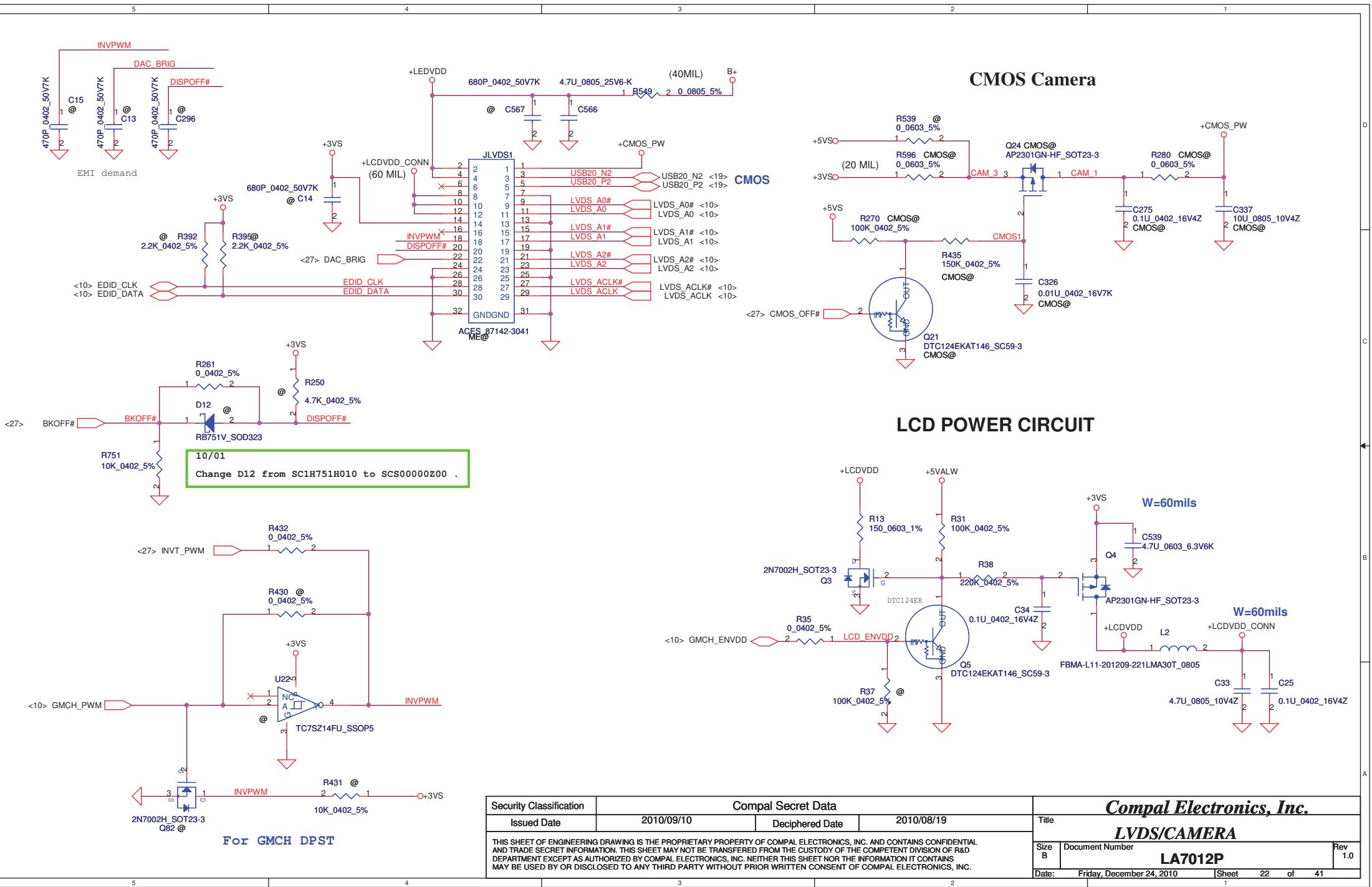


CRT Connector



Change Q13 from SB00000EO10 to SB00000AR00.

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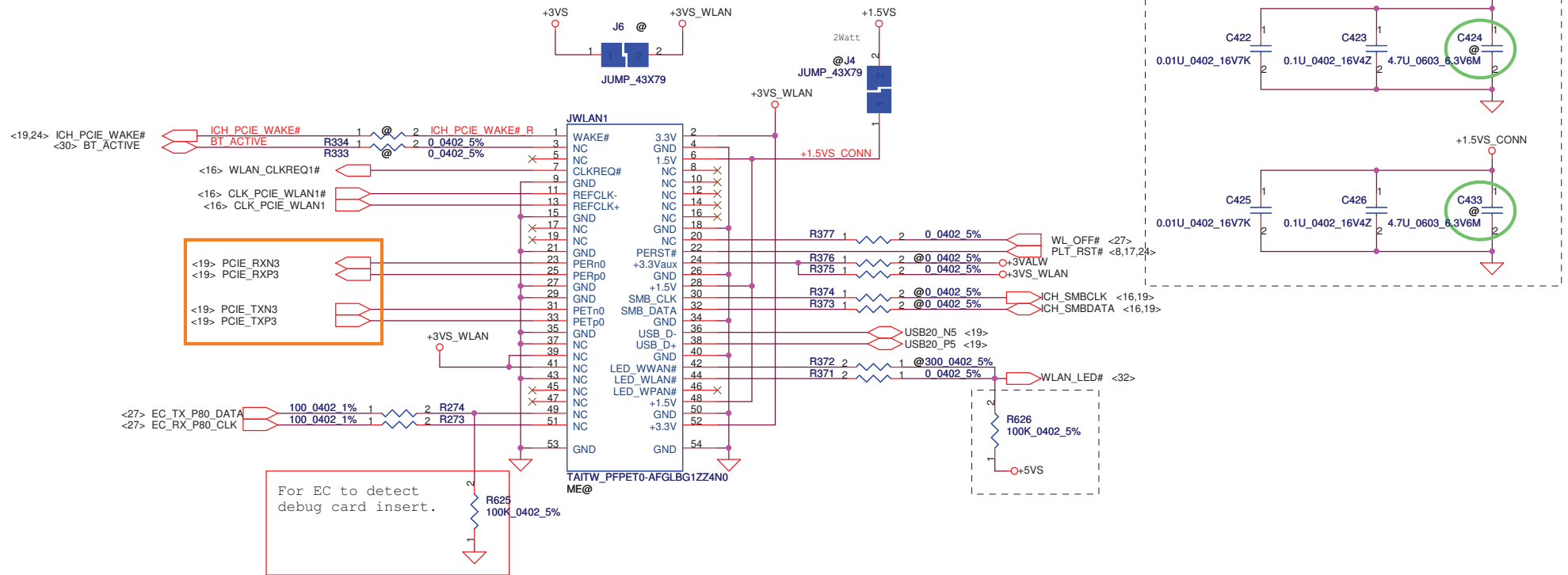
CMOS Camera

LCD POWER CIRCUIT

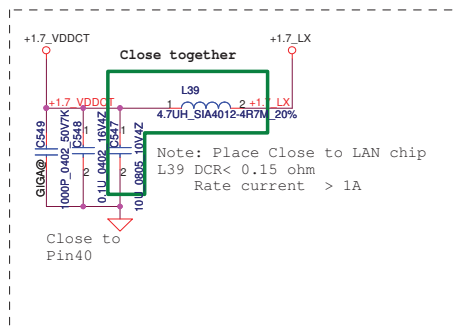
For GMCH DPST

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Mini-Express Card for WLAN(Half)

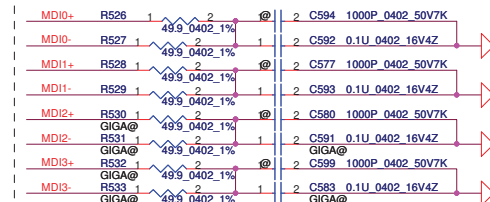
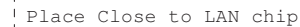


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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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				Document Number	1.0
				LA7012P	
				Date:	Friday, December 24, 2010
				Sheet	23 of 41



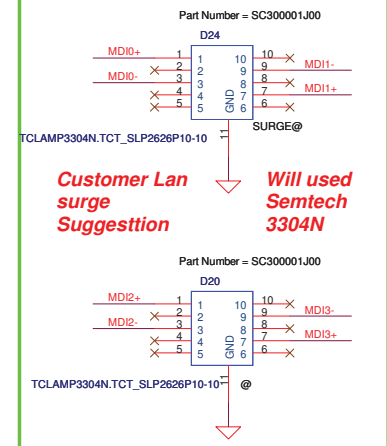
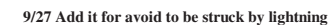
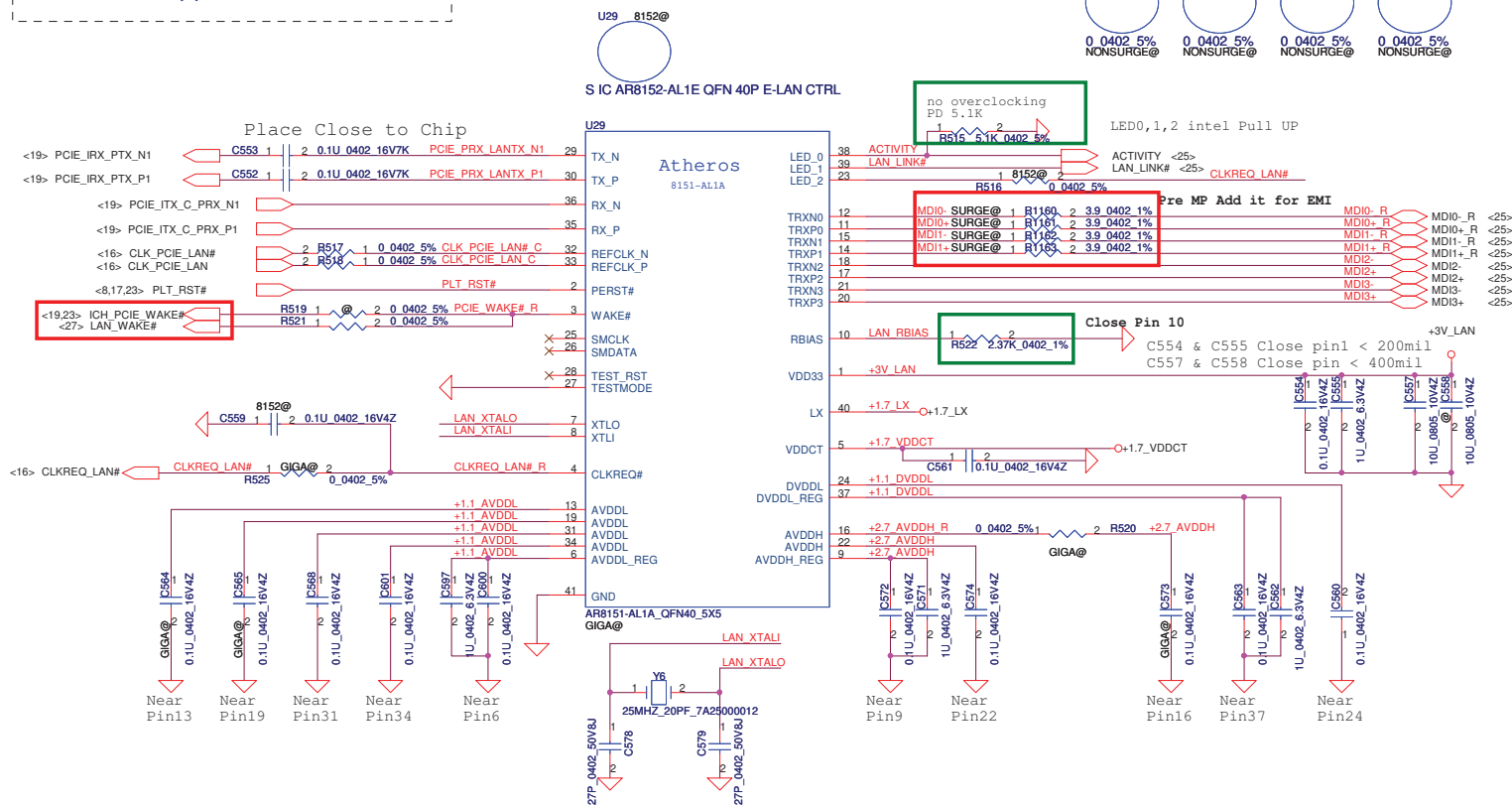
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED1	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--



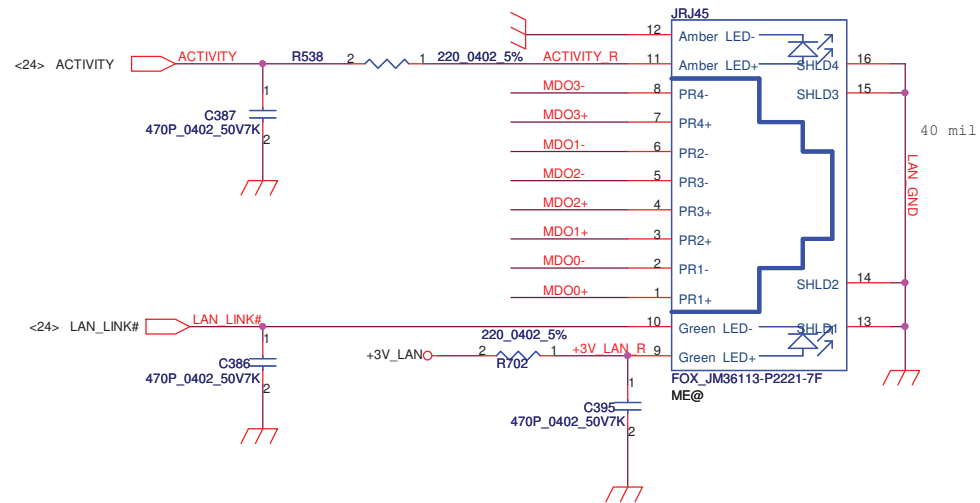
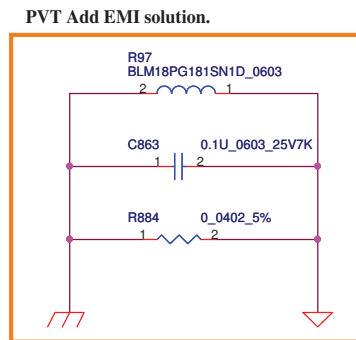
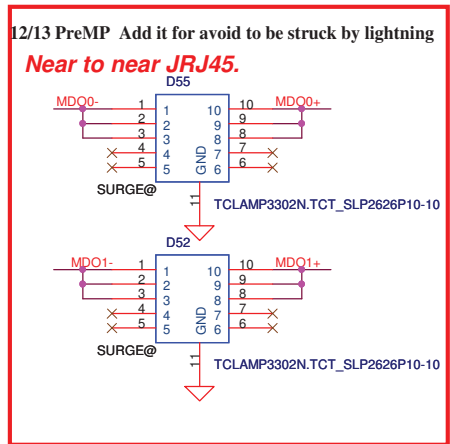
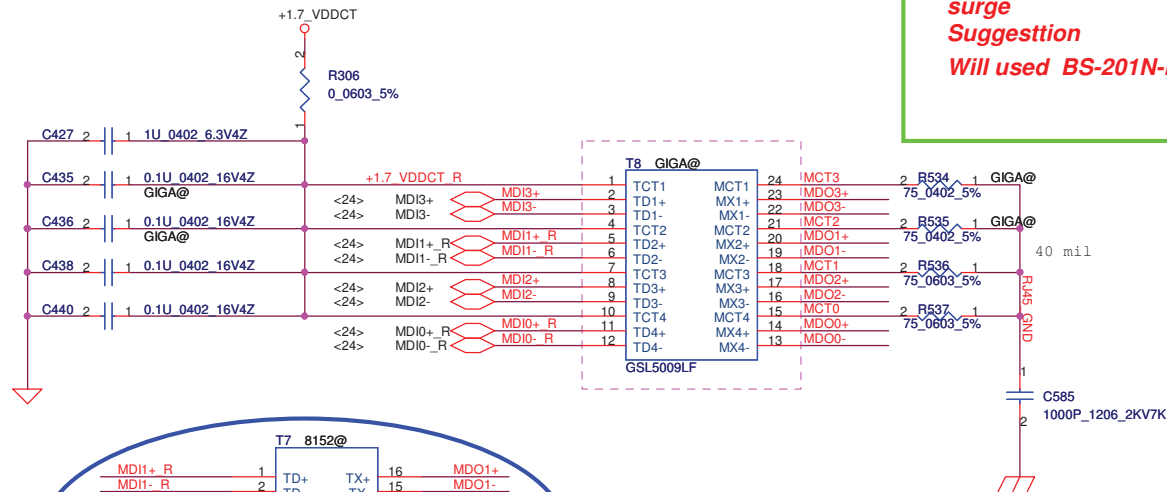
```
| Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+
| resister and cap
```

¹ Note 2 : C594, C577, C580, C599, reserved for EMI.



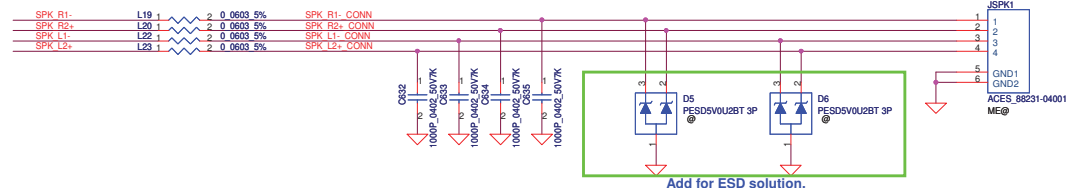
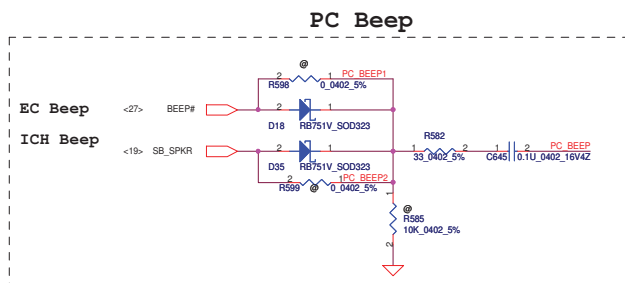
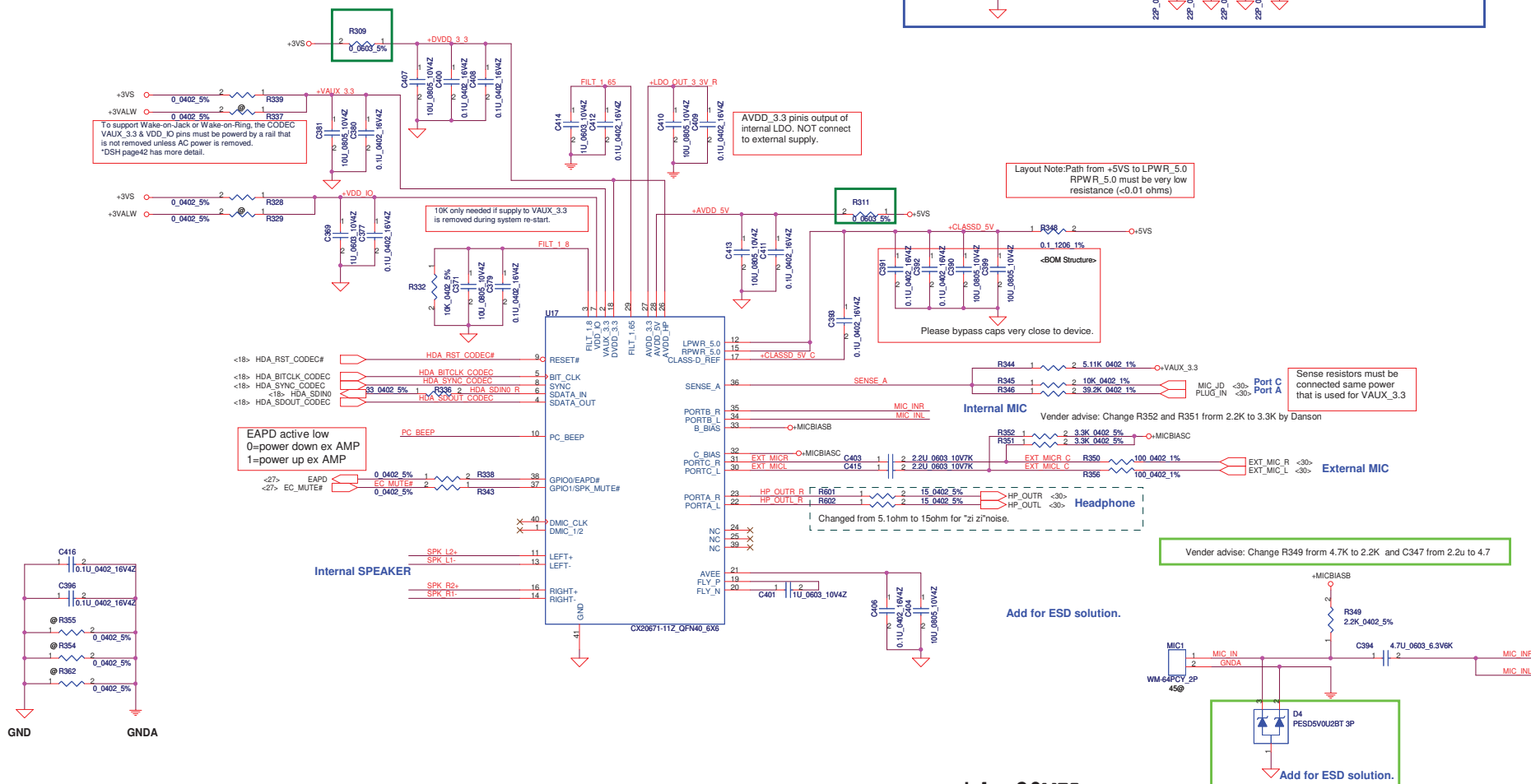
	Pin4	Configure			Pin23	Configure
		R525	C559			
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED [2]	

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					Size	Document Number		Rev	
					Custom	LA7012P		1.0	
					Date:	Friday, December 24, 2010	Sheet	24	of

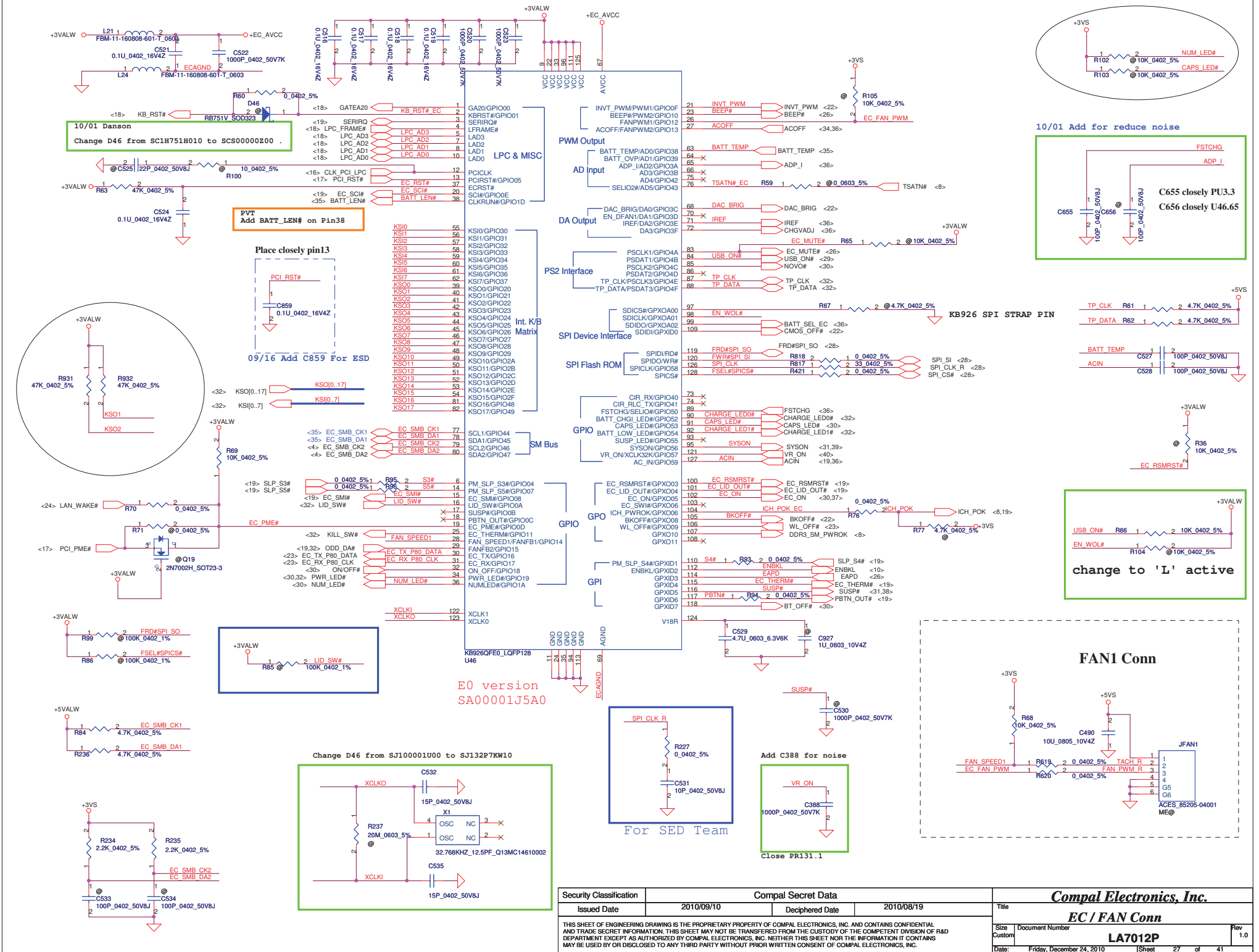


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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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				Size	Document Number
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

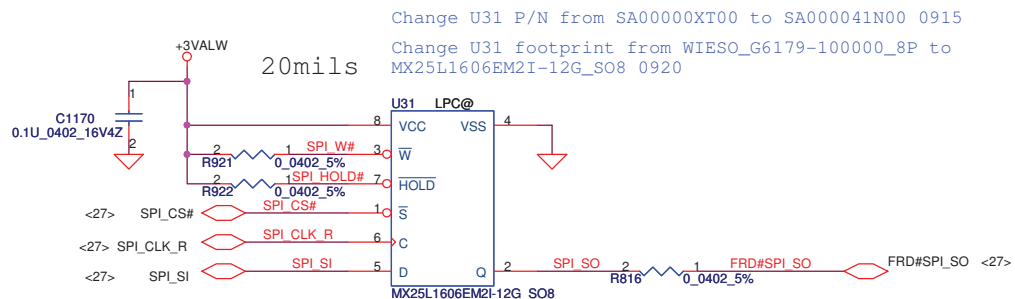


Security Classification		Compal Secret Data		Compal Electronics, Inc. Title CX20671 Codec	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Size	Document Number
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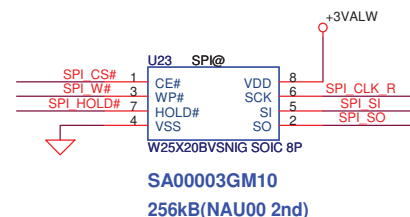
SPI Flash (16Mb*1)

FOR EC 16M SPI ROM



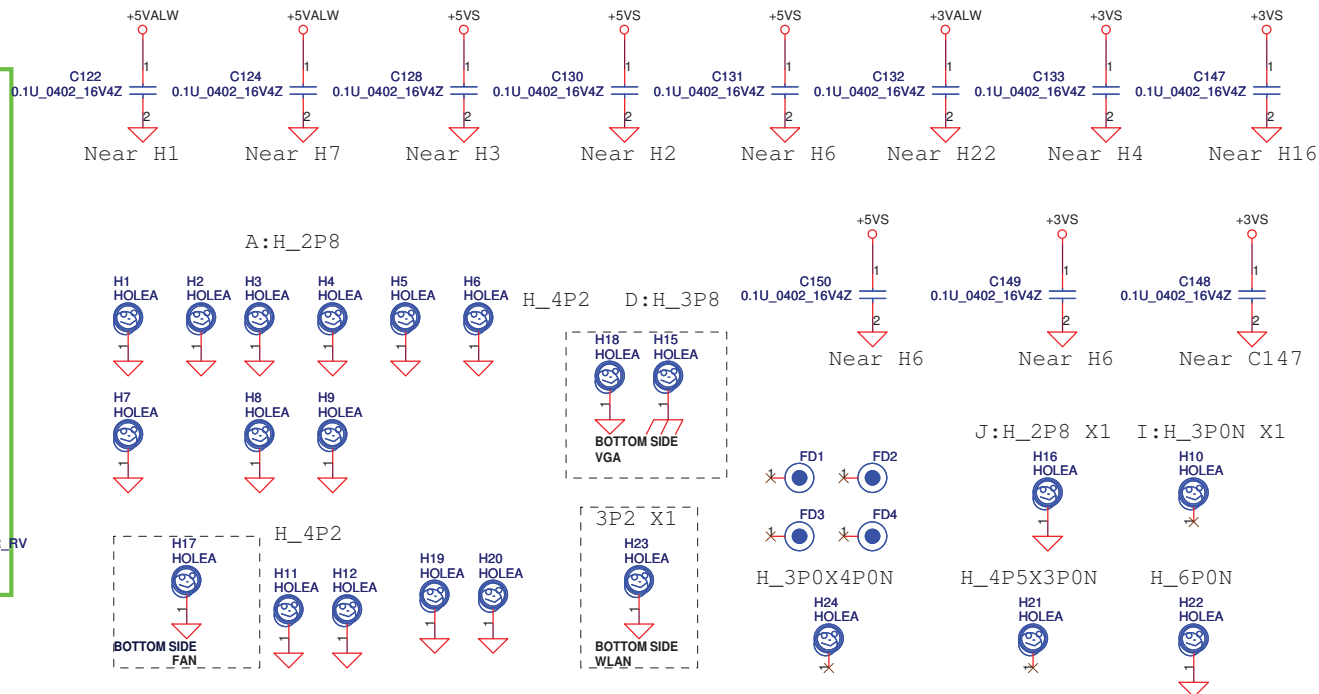
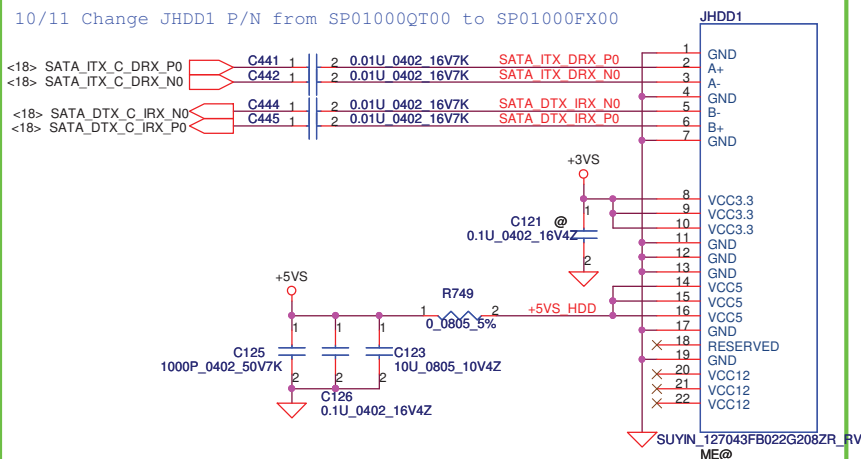
FOR EC 256K SPI ROM (NONShare ROM)

2010/09/24 Add U23 for NONShare SPI ROM.



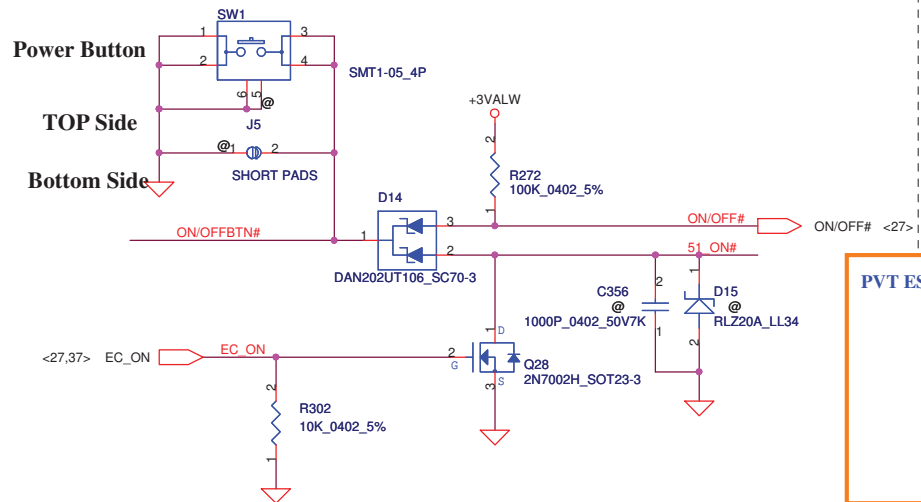
SATA HDD Conn.

10/11 Change JHDD1 P/N from SP01000QT00 to SP01000FX00

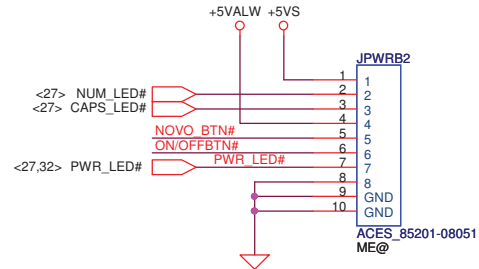


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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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				Size B	Document Number
				LA7012P	
				Date:	Friday, December 24, 2010
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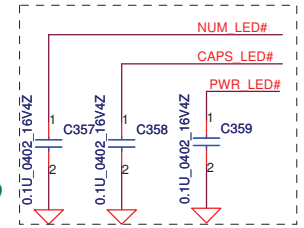
ON/OFF switch



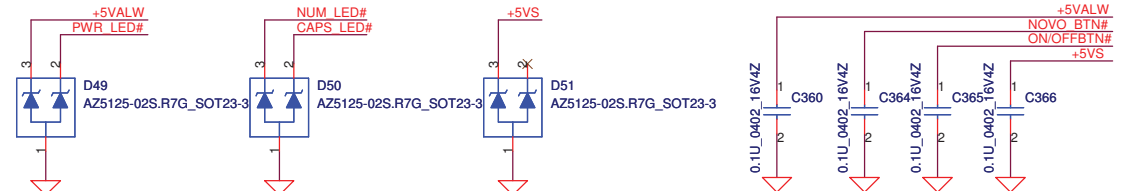
Power Bottom Board Conn. 8pin



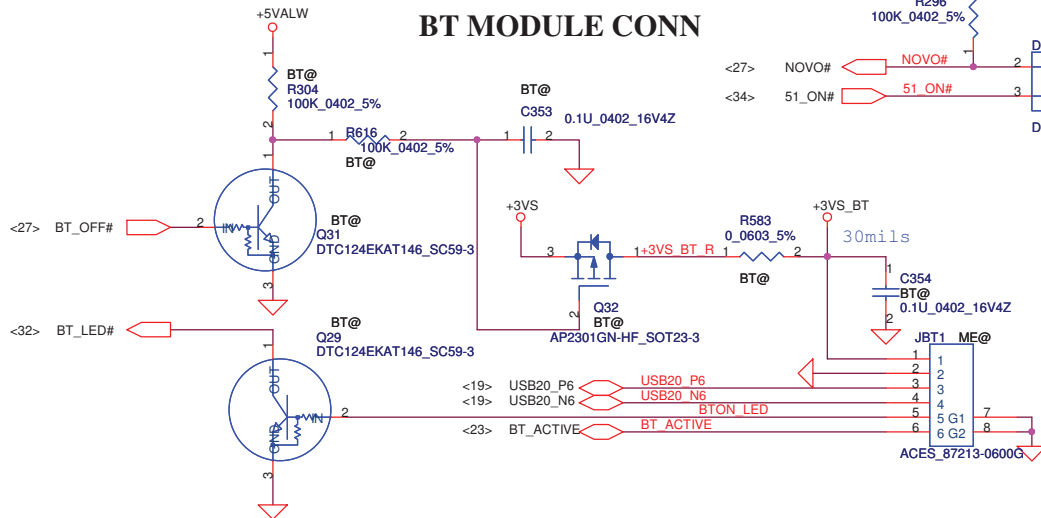
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00



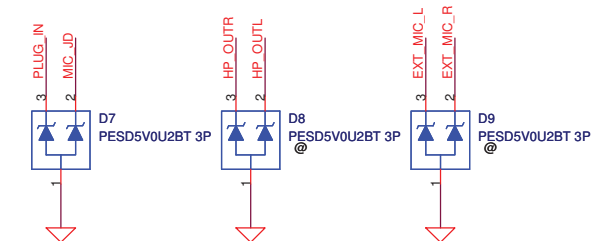
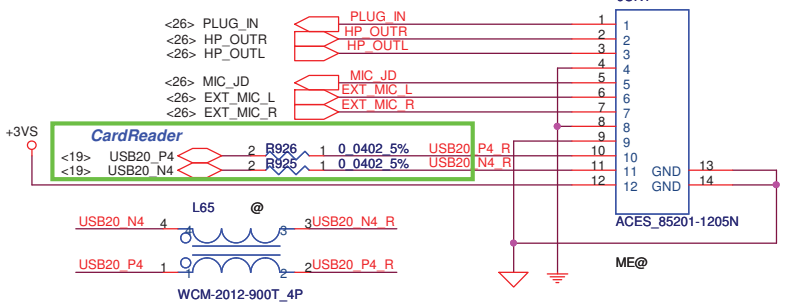
PVT ESD solution.



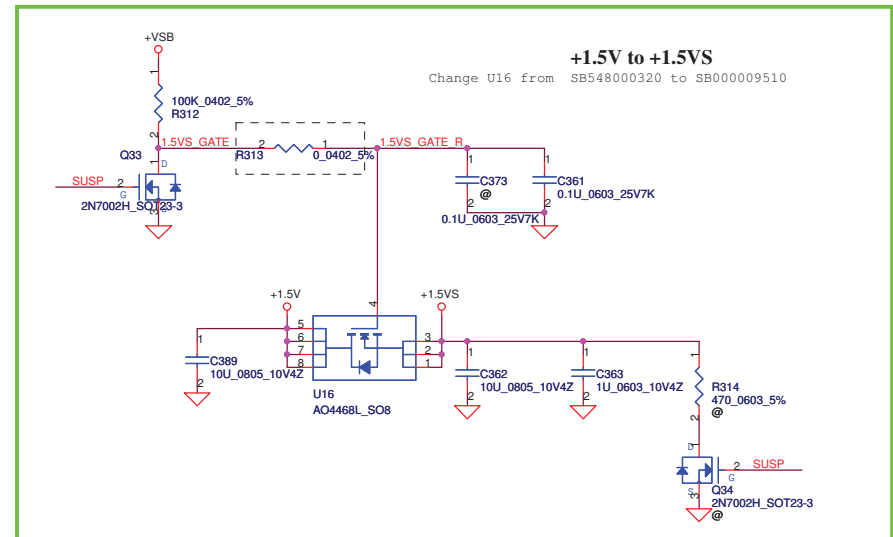
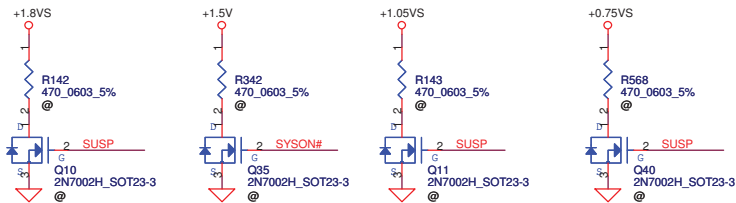
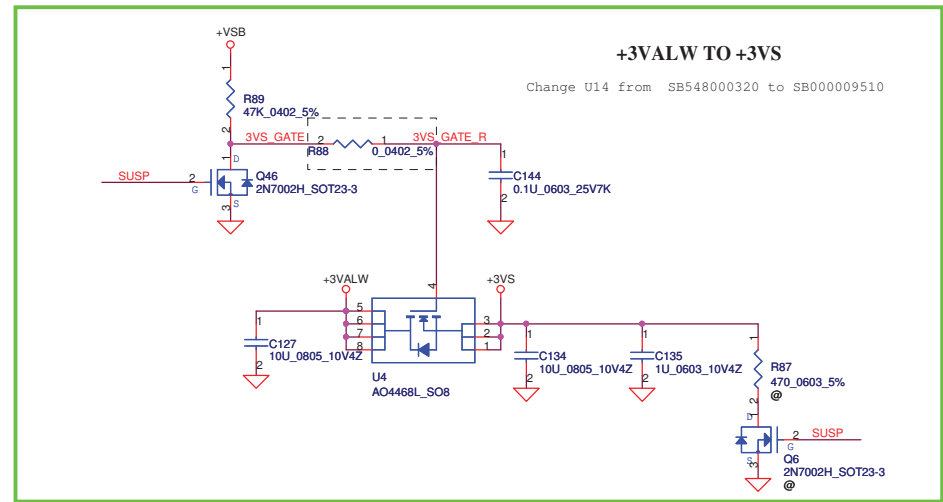
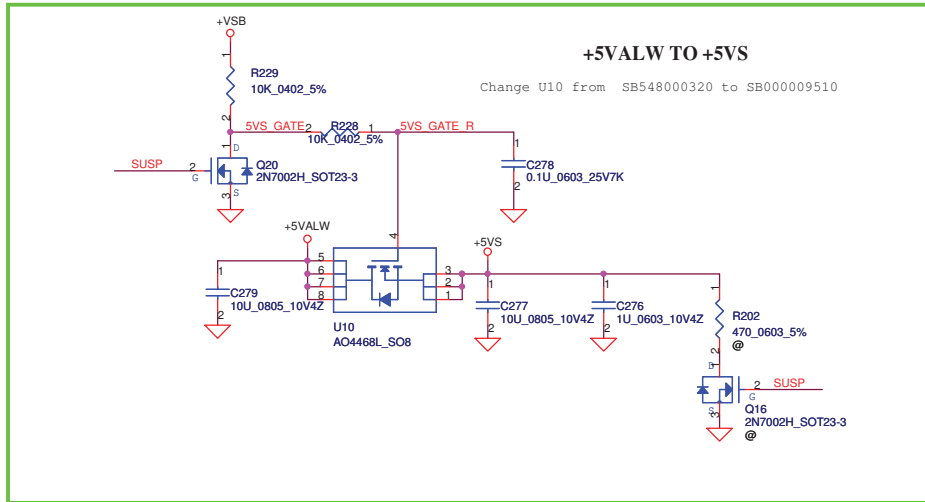
BT MODULE CONN



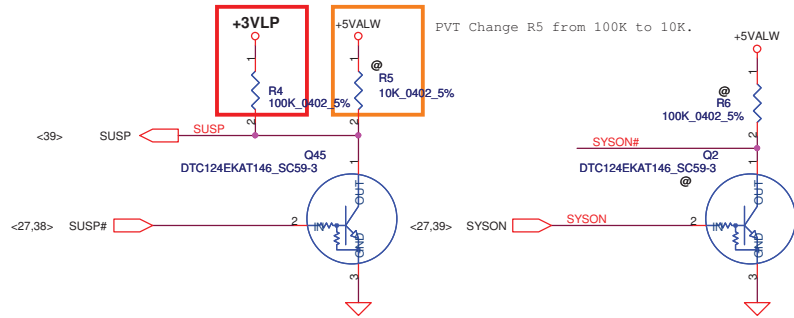
Card Reader/Audio Jack SB CONN



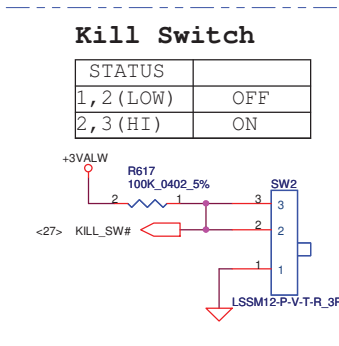
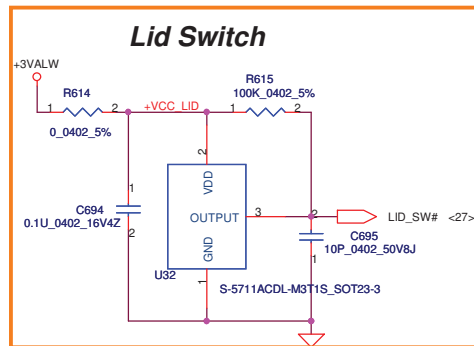
Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	Audio Jack & SW & BT Conn.
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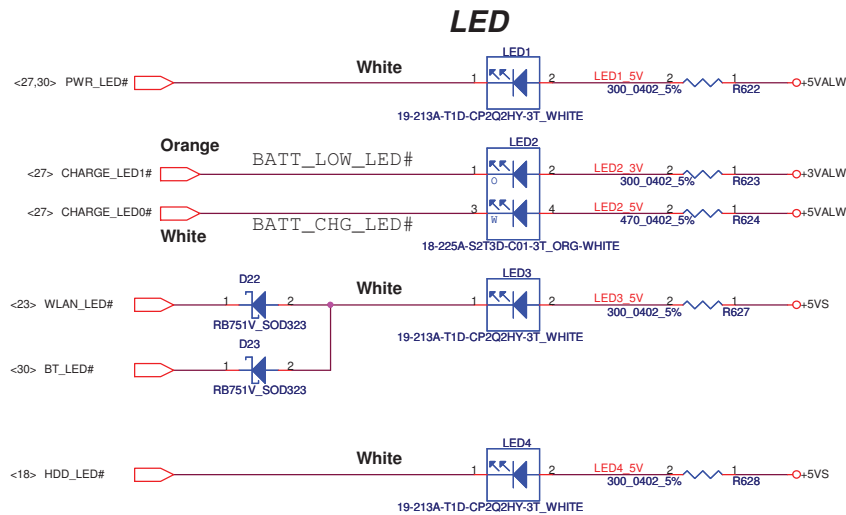
Pre MP Change SUSP pull high from +5VALW to +3VLP.



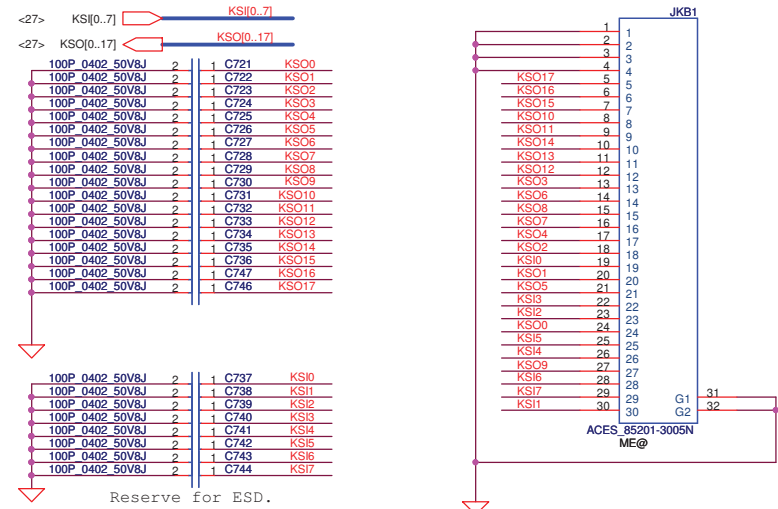
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	
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PVT Change U32 part number from SA032120010 to SA000031C00



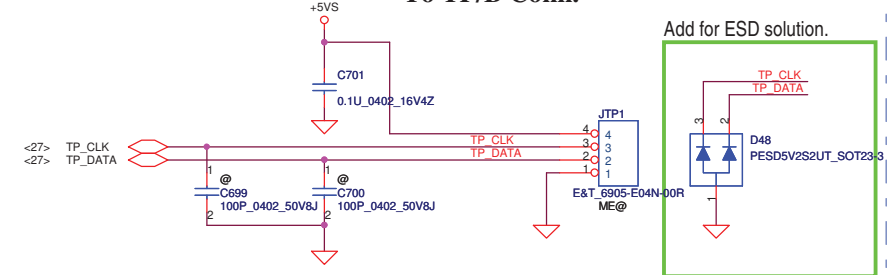
INT_KBD Conn.



check connector & pin define.

CONN PIN define need double check

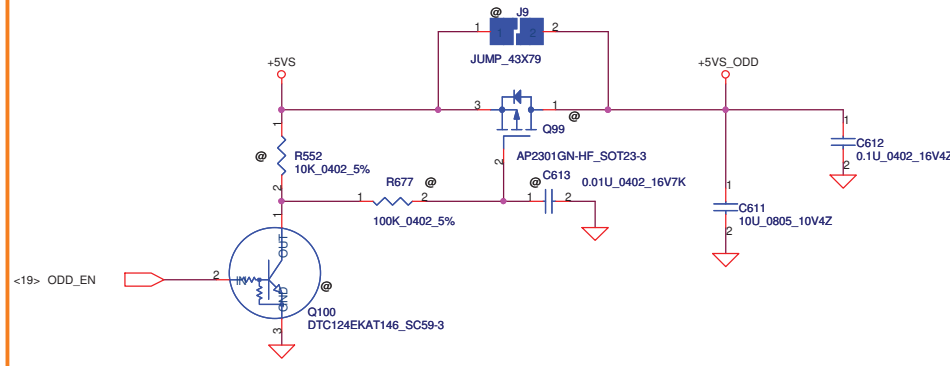
To TP/B Conn.



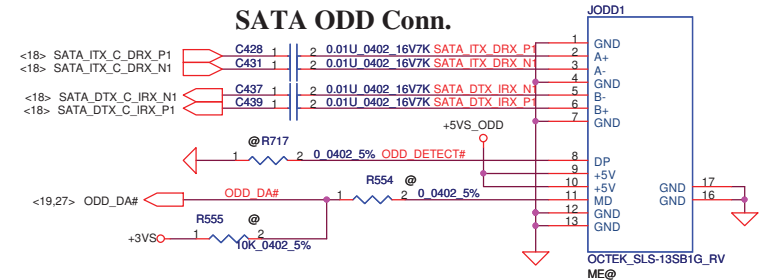
Add for ESD solution.

ODD Power Control

11/05 Add this function.



SATA ODD Conn.



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				Size	Rev
				Custom	1.0
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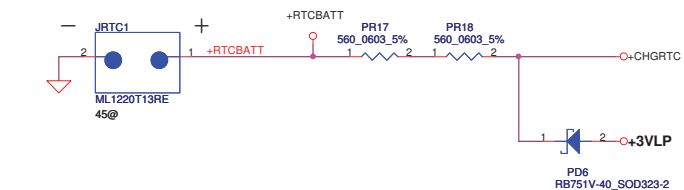
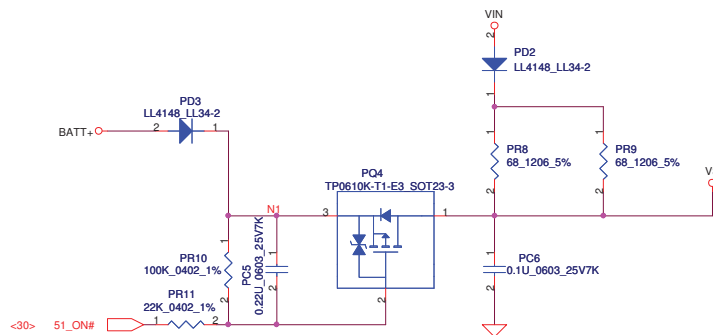
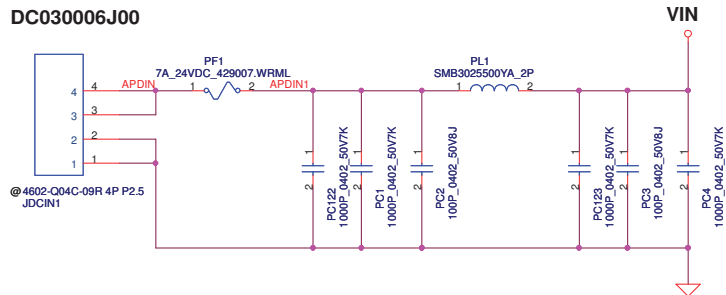
Version change list (P.I.R. List)

Page 1 of 1 for HW

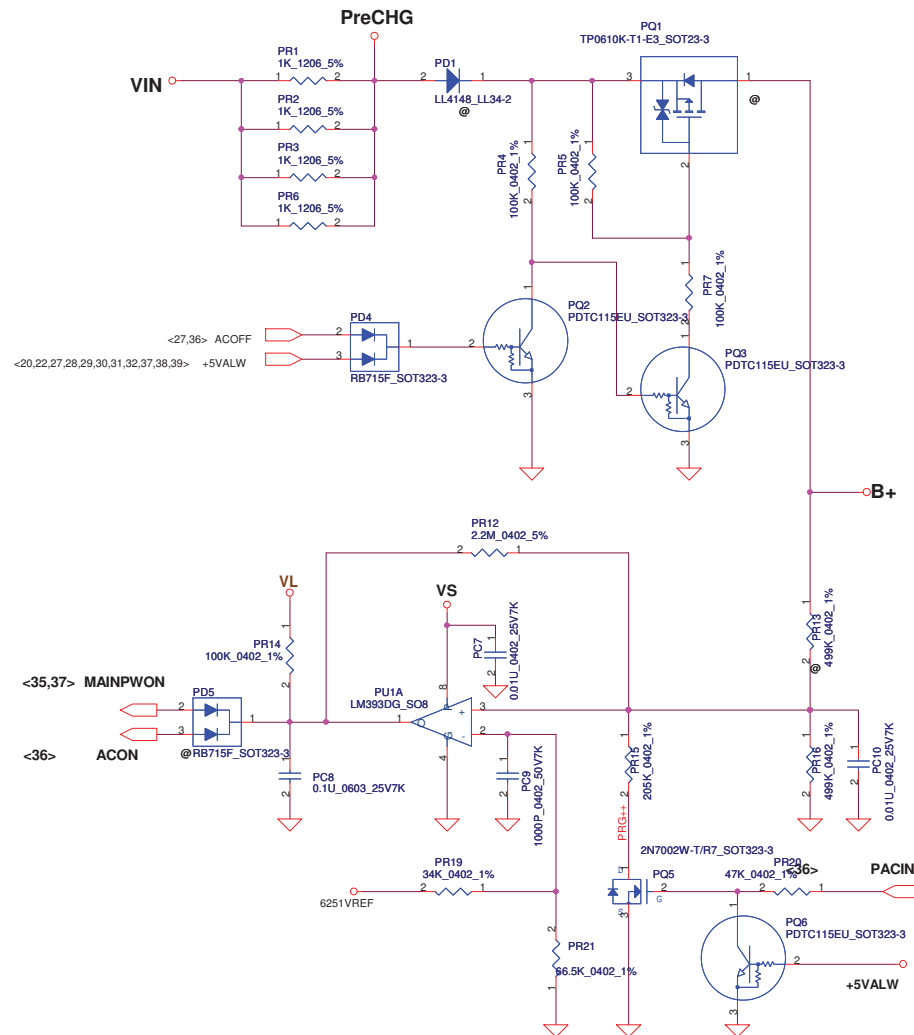
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
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31							

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DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

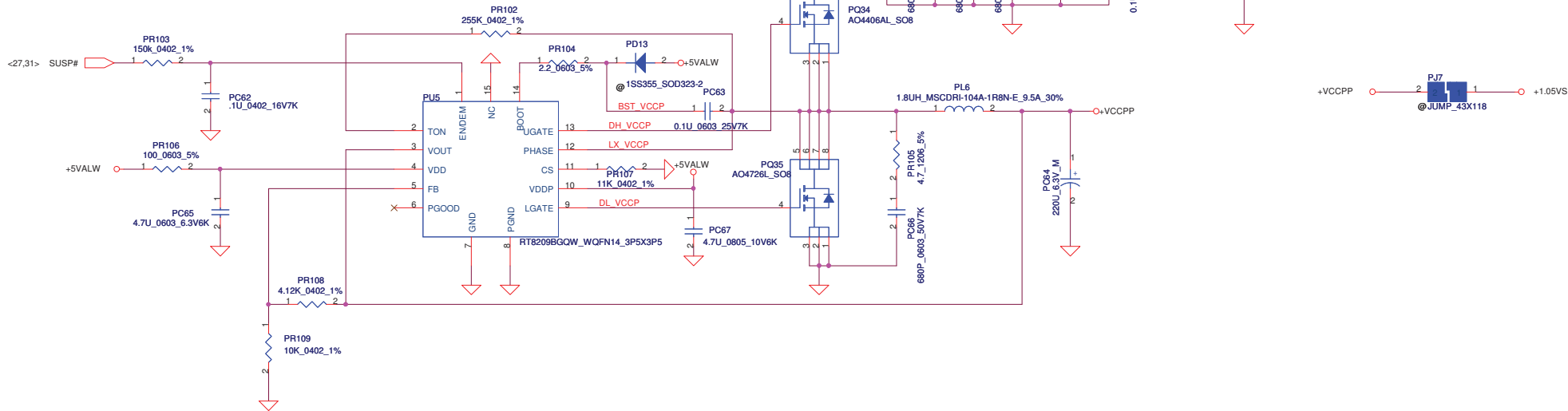
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

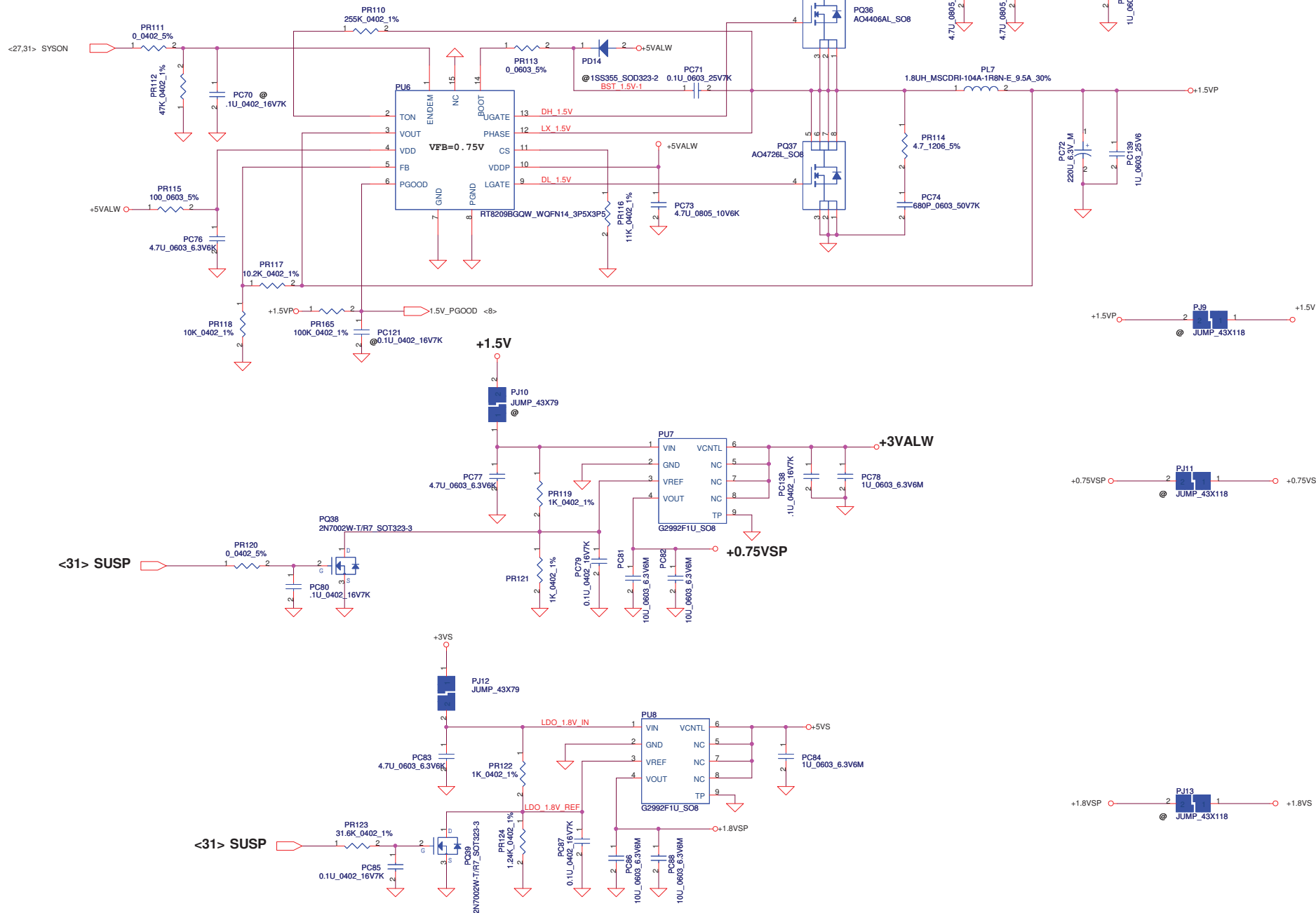
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

A vertical number line with four points labeled A, B, C, and D from bottom to top. An arrow points from point B to point C.

4



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								Size	Document Number						Rev
															1.0
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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damaged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transistor, the design margin of PQ11 is not enough.	Add PQ44
p39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Power PIR	
2010/09/10		2010/08/19		Rev 1.0	
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				Sheet 41 of 41	