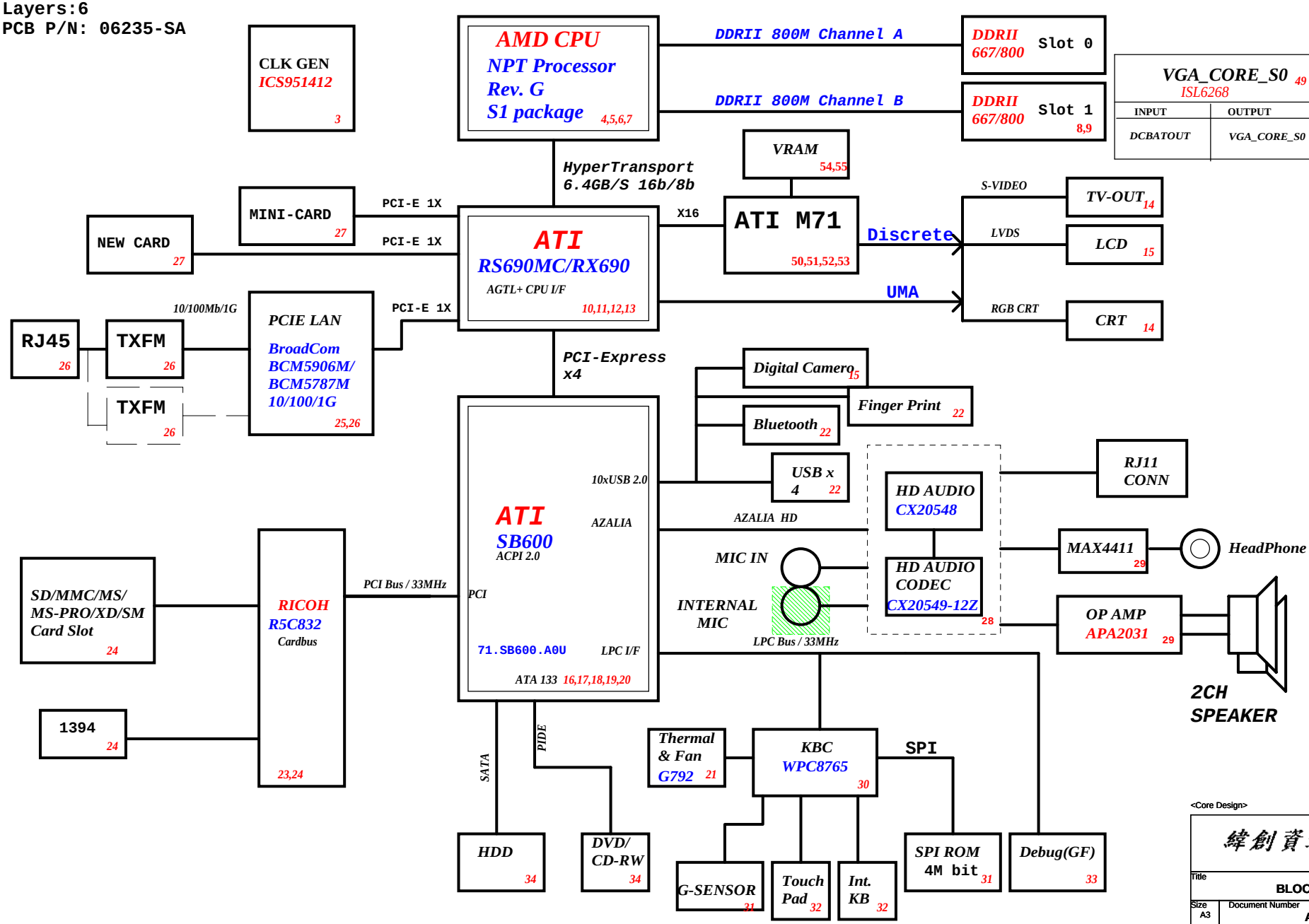
A-NOTE 2.0 Block Diagram

Project Code:91.4T001.001
Layers:6
PCB P/N: 06235-SA



PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

VGA_CORE_S0 49
ISL6268

INPUT	OUTPUT
DCBATOUT	VGA_CORE_S0

Battery Charger 44
ISL6255

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 41
TPS 51120

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC 18
APL5332KAC

INPUT	OUTPUT
3D3V_S5	1D2V_S5

SYSTEM POWER 42
TPS51116

INPUT	OUTPUT
DCBATOUT	1D8V_S3 0D9V_S3

1D2V_S0 43
ISL6268

INPUT	OUTPUT
DCBATOUT	1D2V_S0

CPU V_CORE 38,39
ISL6264

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 41
TPS 51120

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA
Date: Tuesday, September 26, 2006 | Sheet 1 of 55

SA: 07/31/06 Start

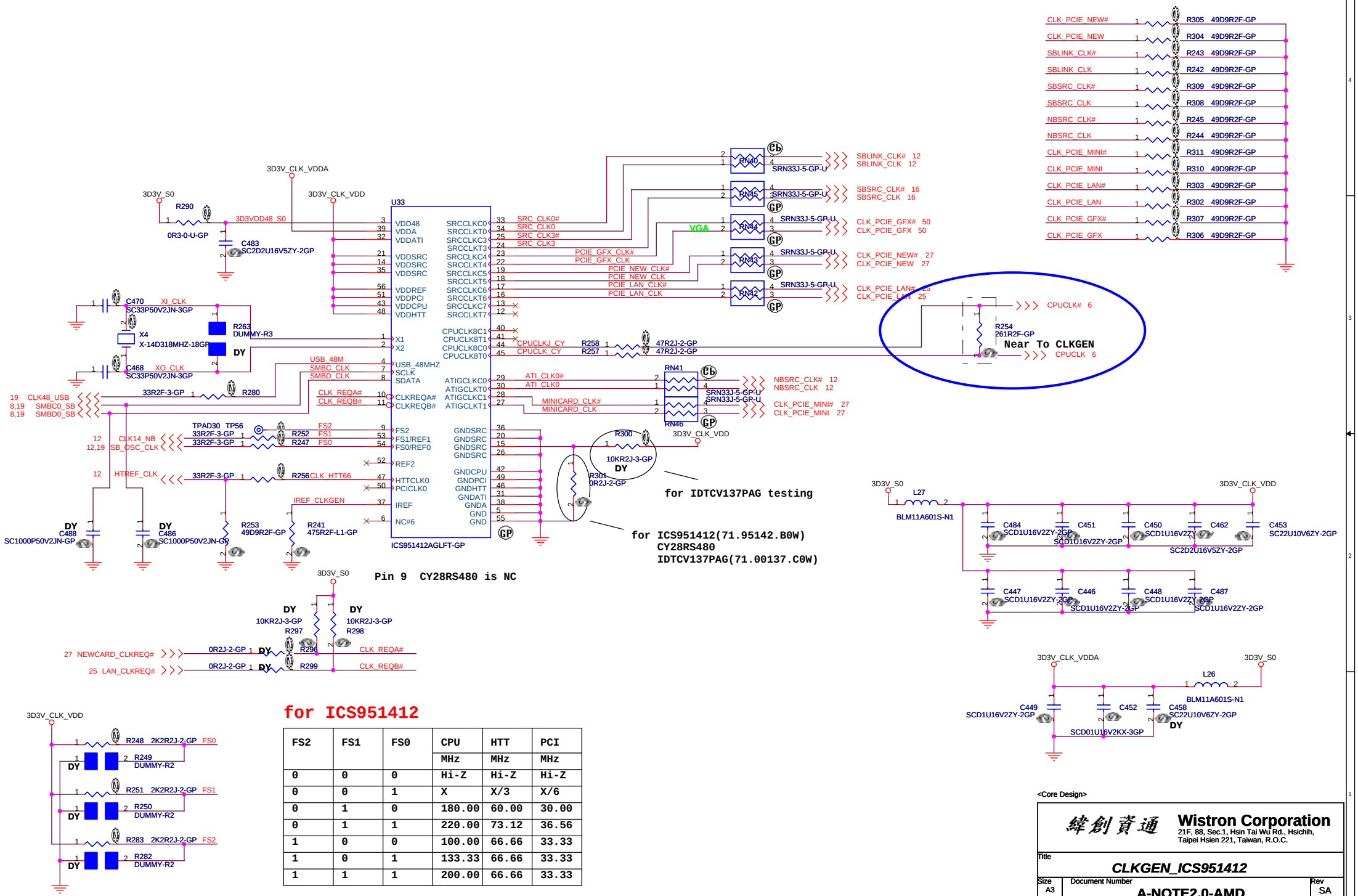
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHANGE HISTORY**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 2 of 55



for ICS951412

FS2	FS1	FS0	CPU	HTT	PCI
			MHz	MHz	MHz
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	73.12	36.56
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33

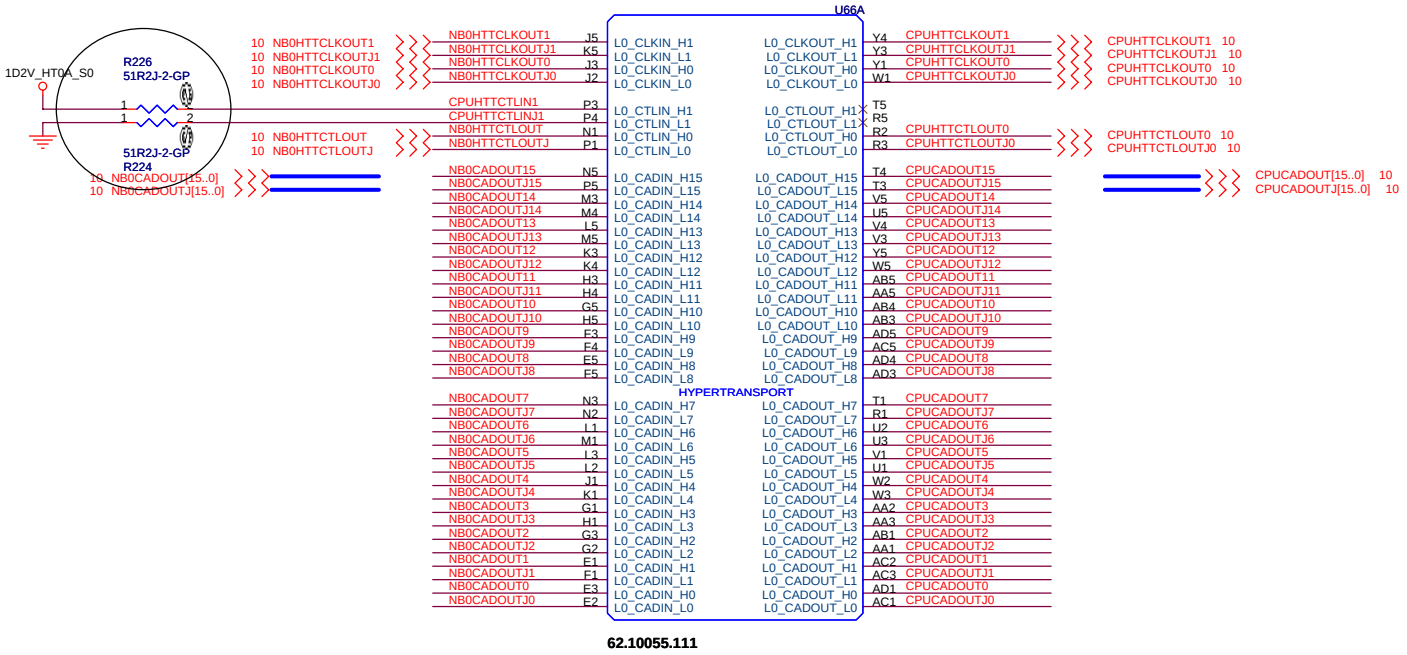
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN_ICS951412**

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 3 of 55



62.10055.111

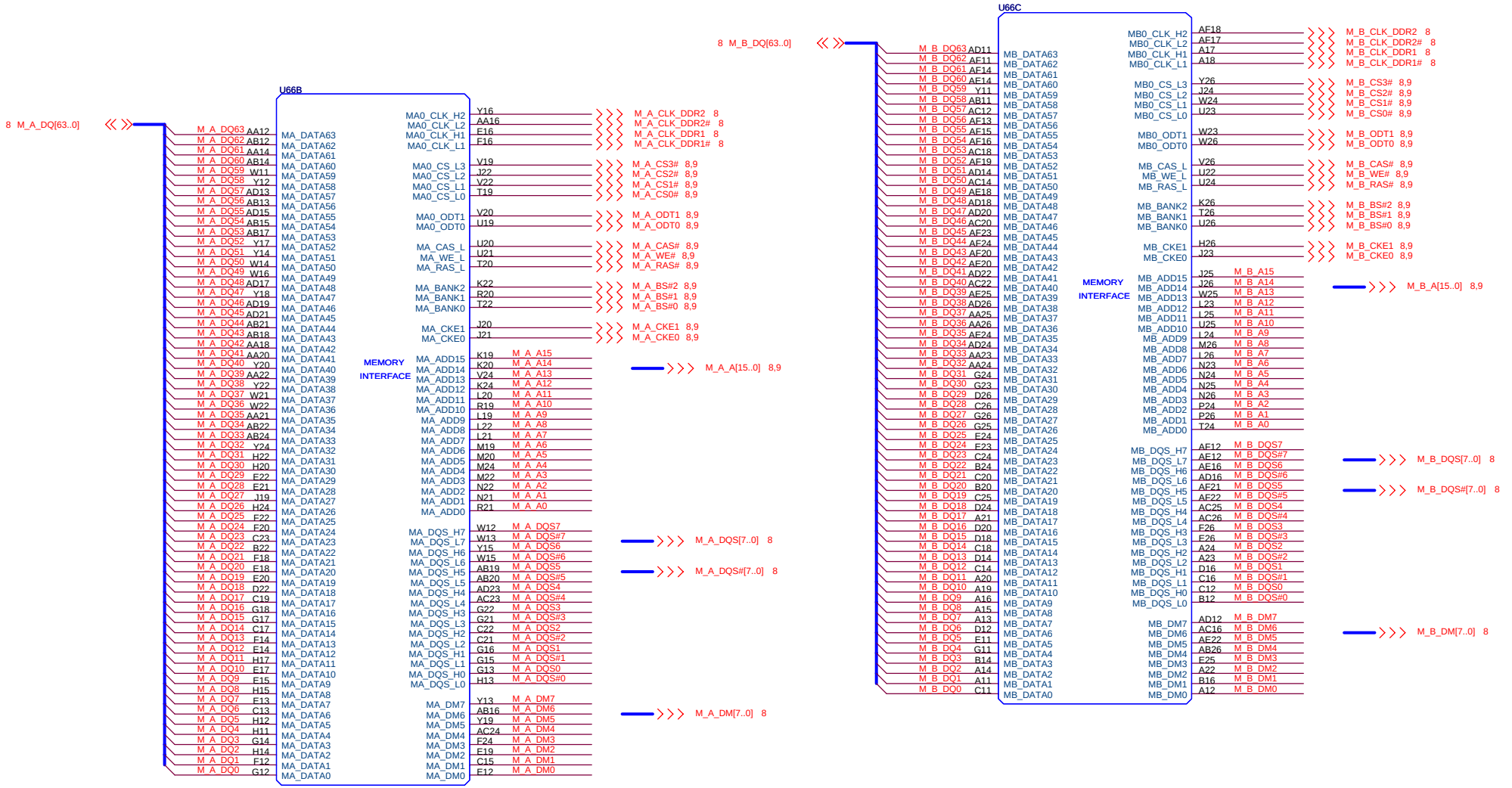
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(1/4)_HyperTransport I/F

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 4 of 55



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 5 of 55

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

Near To CPU

Remove these resistor when using EVT CPU

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

LAYOUT: Locate close to CPU

VREF_DDR_CLAW

SD

HDT Connectors

08/31

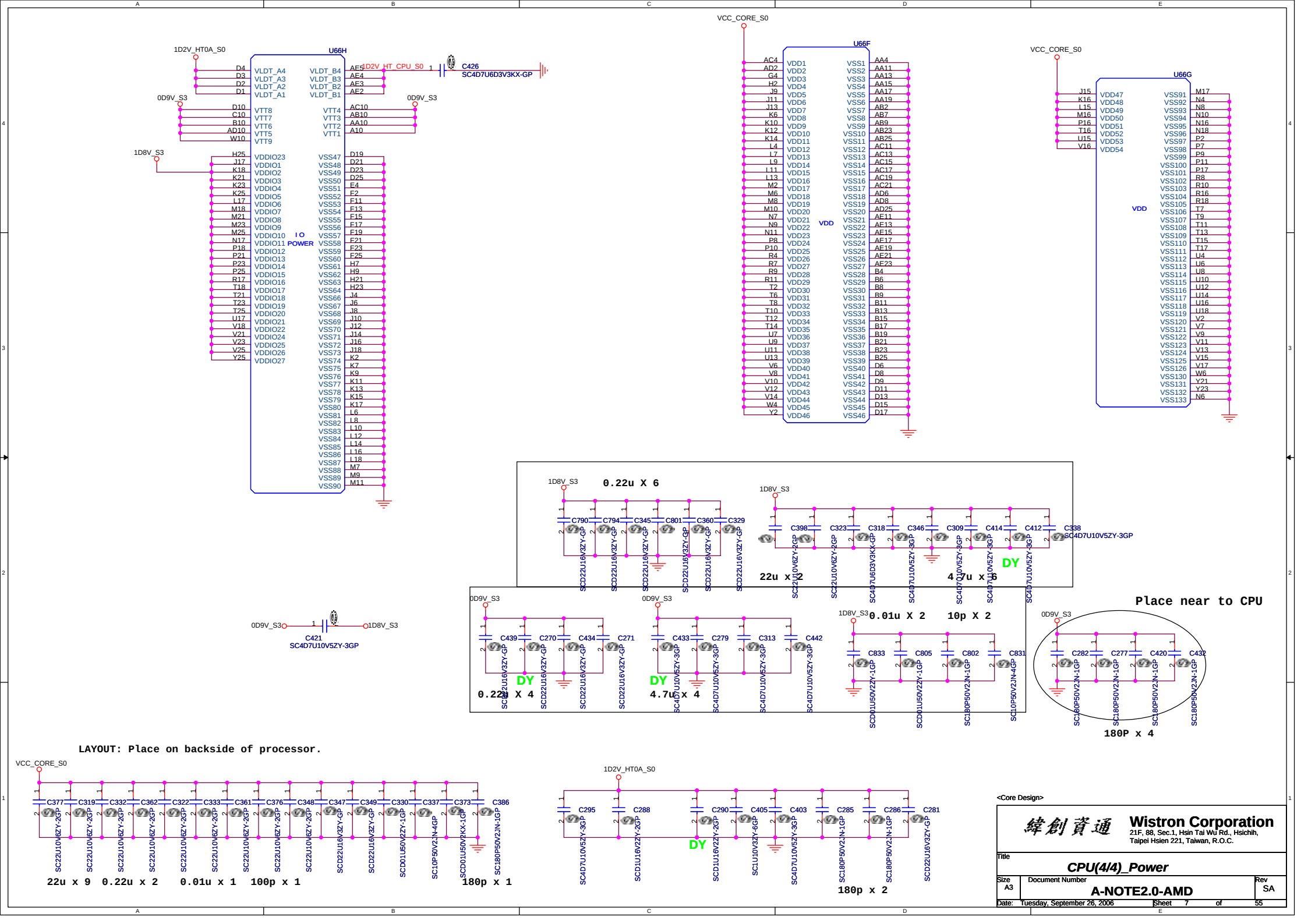
<Core Design>

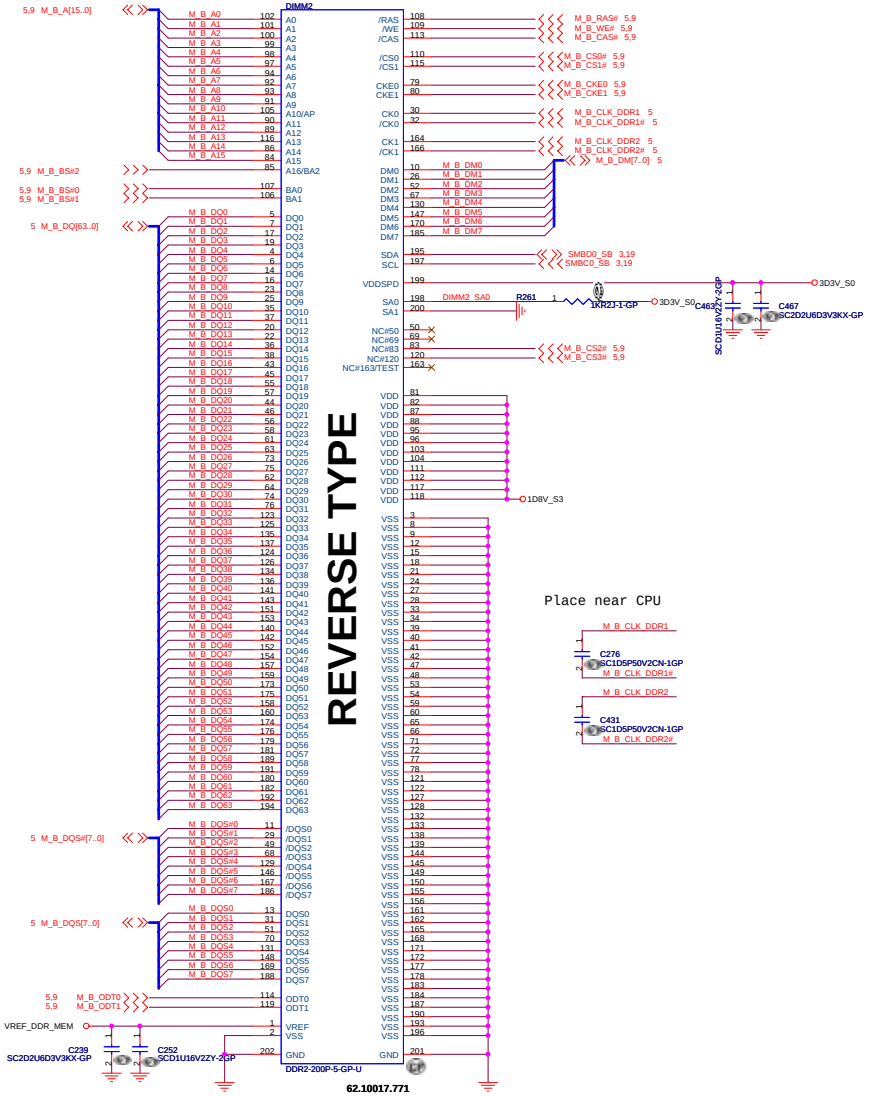
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

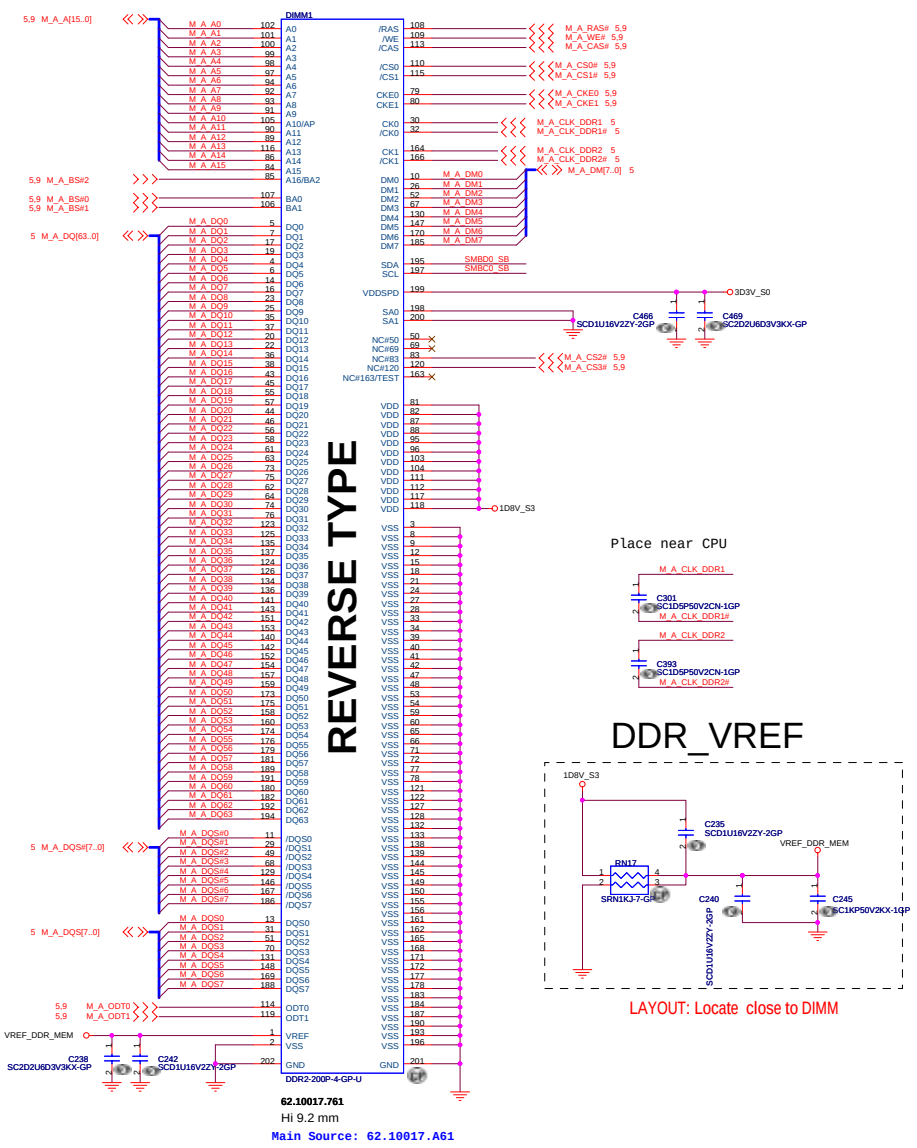
Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 6 of 55


U66H
1D2V_HT0A_S0
0D9V_S3
1D8V_S3
1D2V_HT_CPU_S0
C426
SC4D7U6D3V3KX-GP
VLDT_A4
VLDT_A3
VLDT_A2
VLDT_A1
VLDT_B4
VLDT_B3
VLDT_B2
VLDT_B1
VTT8
VTT7
VTT6
VTT5
VTT9
VTT4
VTT3
VTT2
VTT1
VDDIO23
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDIO6
VDDIO7
VDDIO8
VDDIO9
VDDIO10
VDDIO11
VDDIO12
VDDIO13
VDDIO14
VDDIO15
VDDIO16
VDDIO17
VDDIO18
VDDIO19
VDDIO20
VDDIO21
VDDIO22
VDDIO24
VDDIO25
VDDIO26
VDDIO27
I O
POWER
VCC_CORE_S0
U66F
VDD
U66G
VDD47
VDD48
VDD49
VDD50
VDD51
VDD52
VDD53
VDD54
0.22u X 6
22u x 2
4.7u x 6
DY
0.22u X 4
4.7u x 4
0.01u X 2
10p X 2
Place near to CPU
180P x 4
C421
SC4D7U10V5ZY-3GP
LAYOUT: Place on backside of processor.
22u x 9
0.22u x 2
0.01u x 1
100p x 1
180p x 1
180p x 2
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(4/4)_Power
Size
A3
Document Number
A-NOTE2.0-AMD
Rev
SA
Date: Tuesday, September 26, 2006
Sheet 7 of 55





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

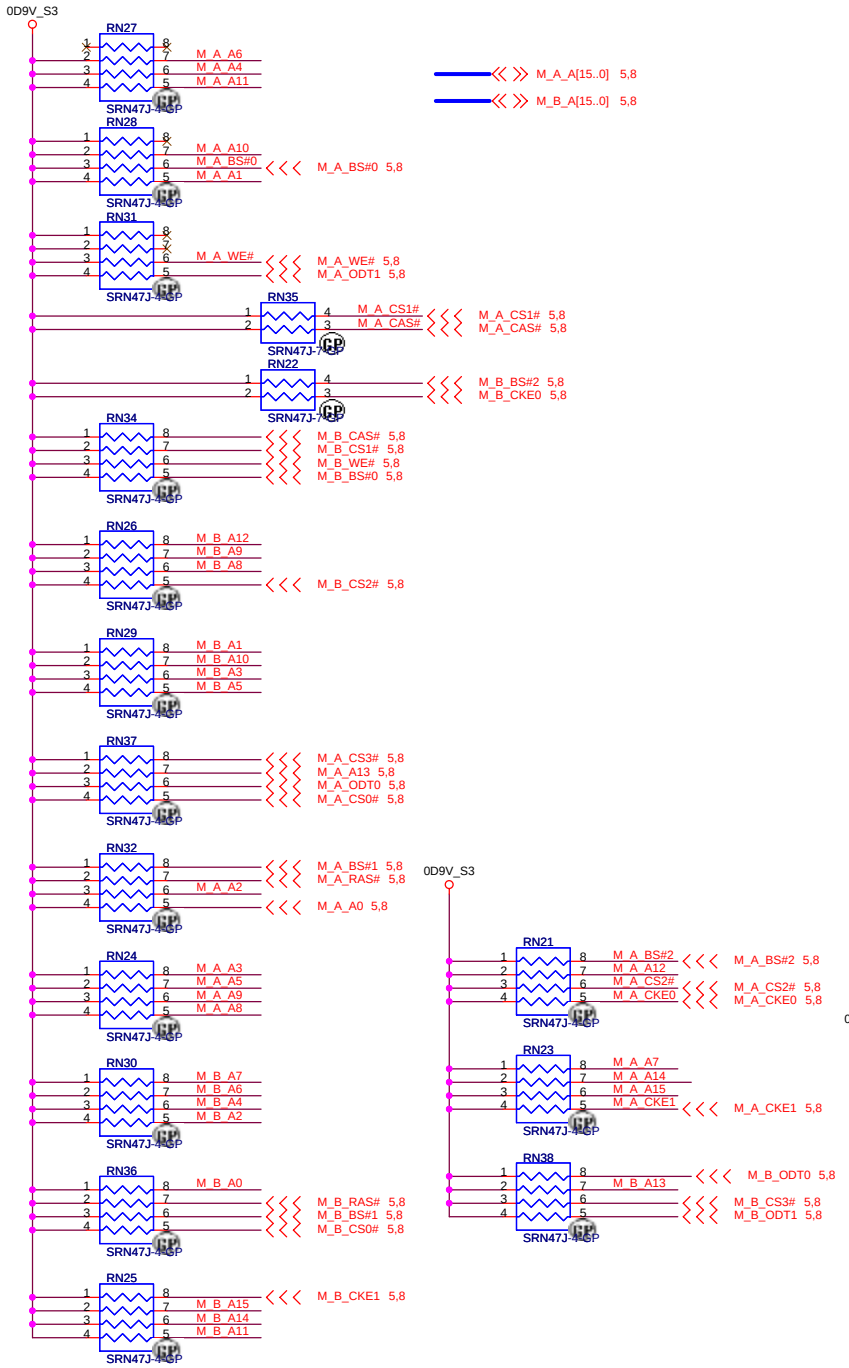
Title: DDR SO-DIMM SKT

Size	Document Number	Rev
A2	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 8 of 55

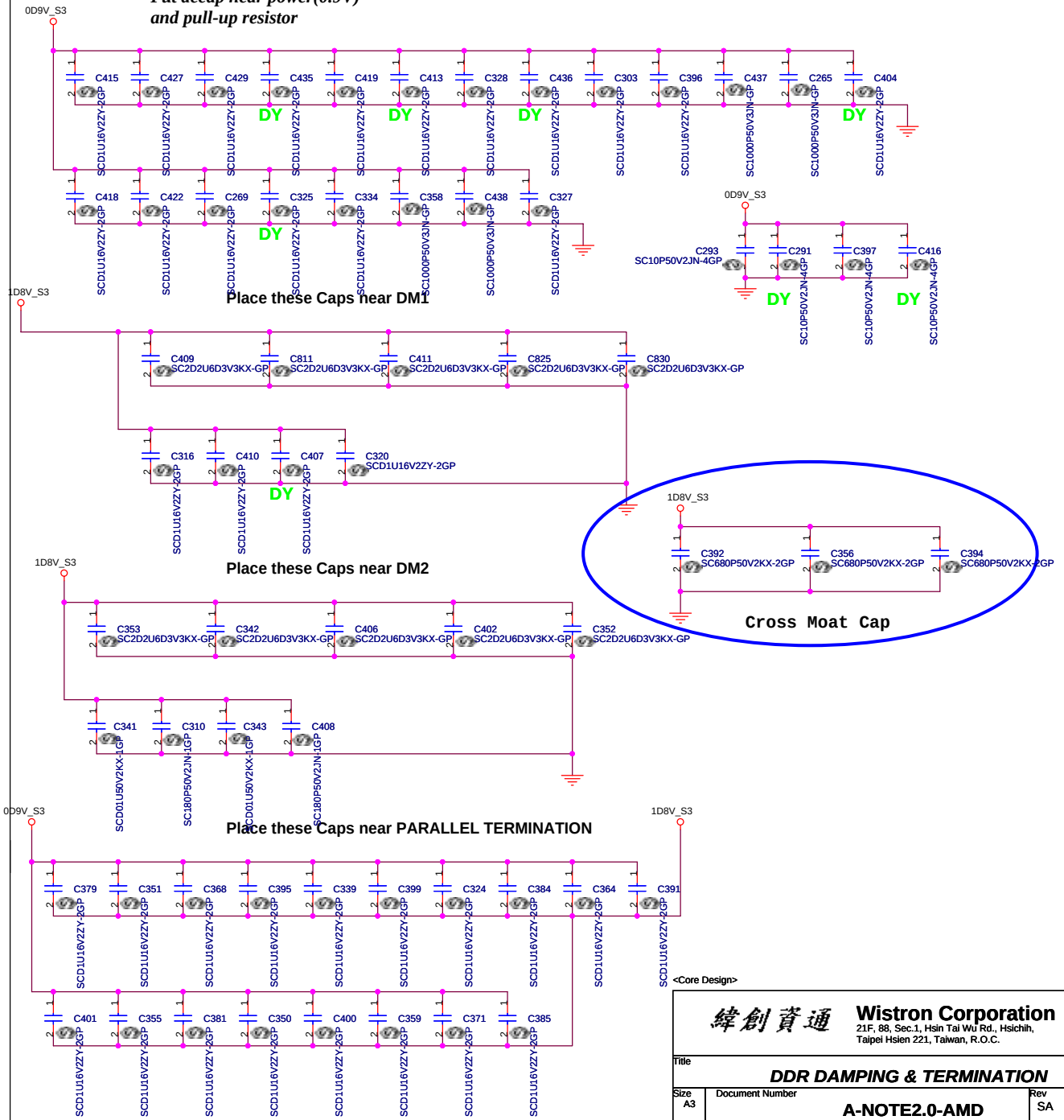
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

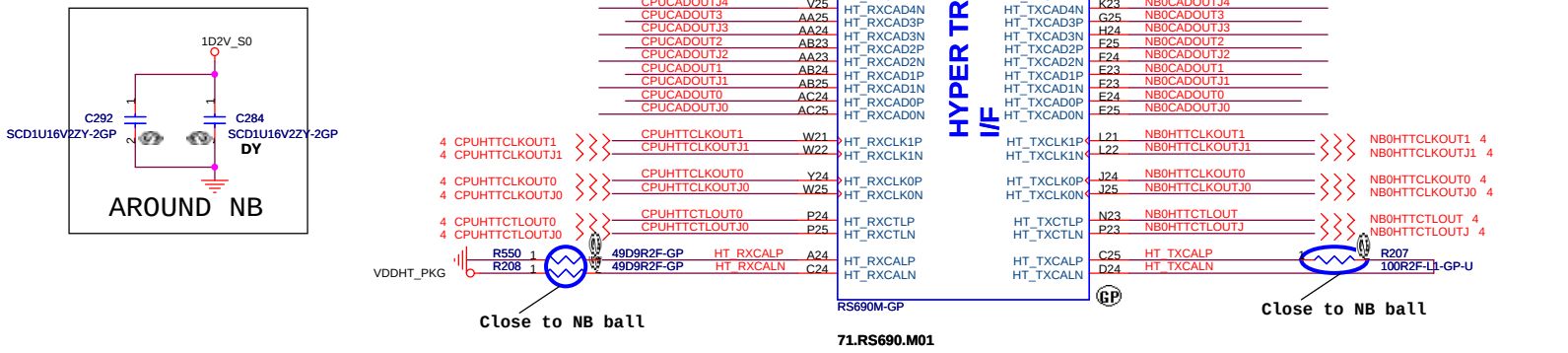
Title: **DDR DAMPING & TERMINATION**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 9 of 55

CLAW HAMMER TO NB

NB TO CLAW HAMMER



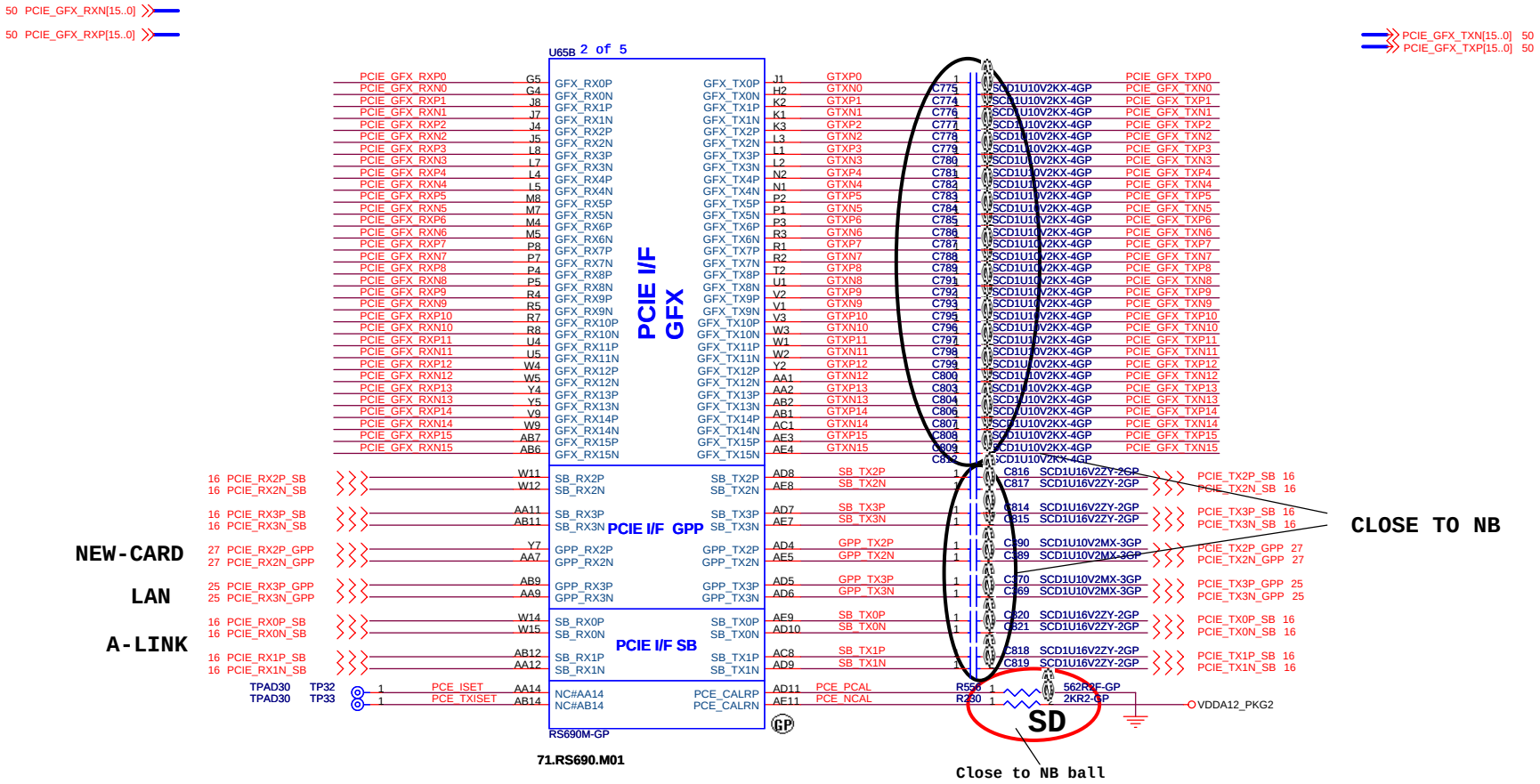
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_HT

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 10 of 55



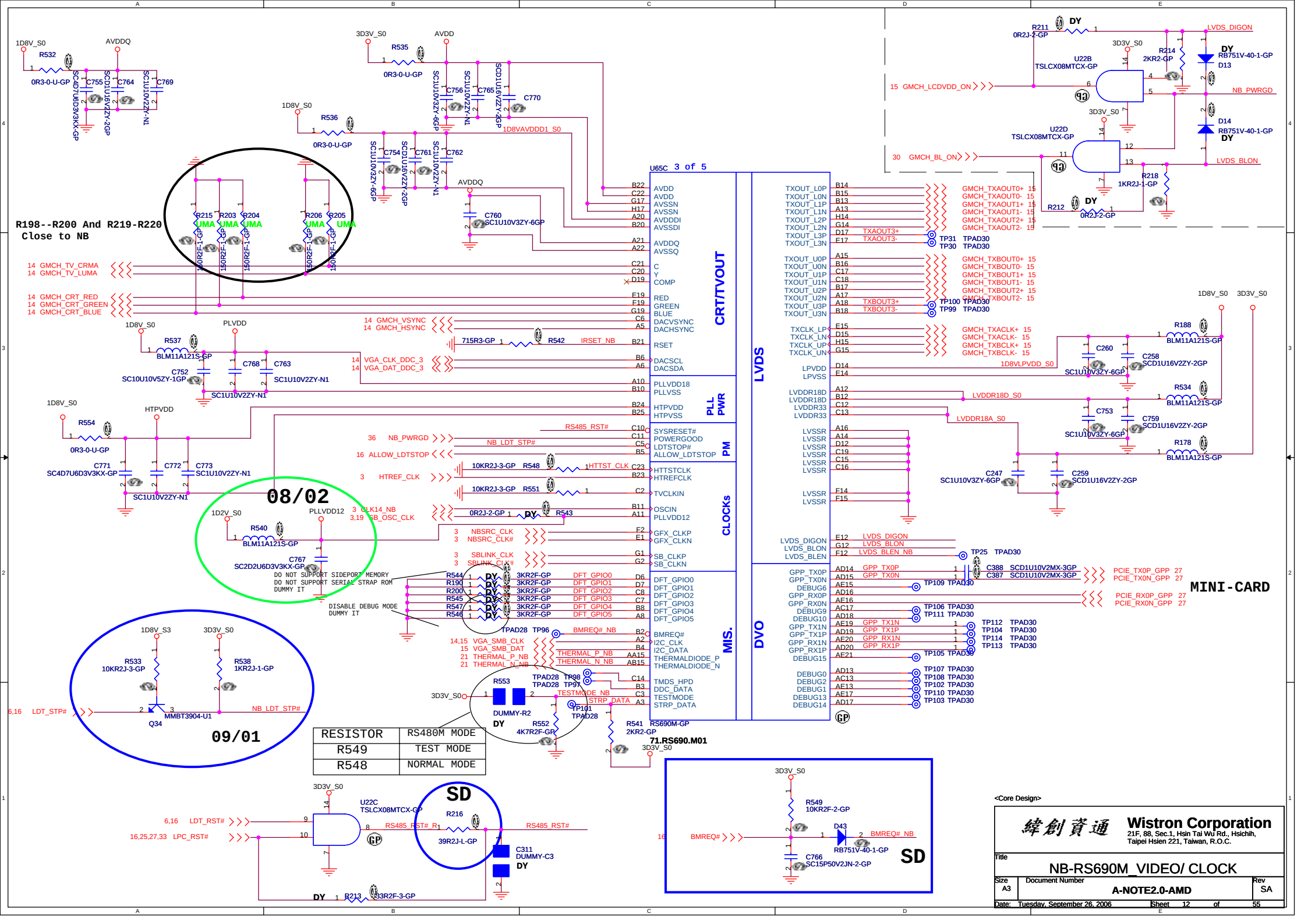
<Core Design>

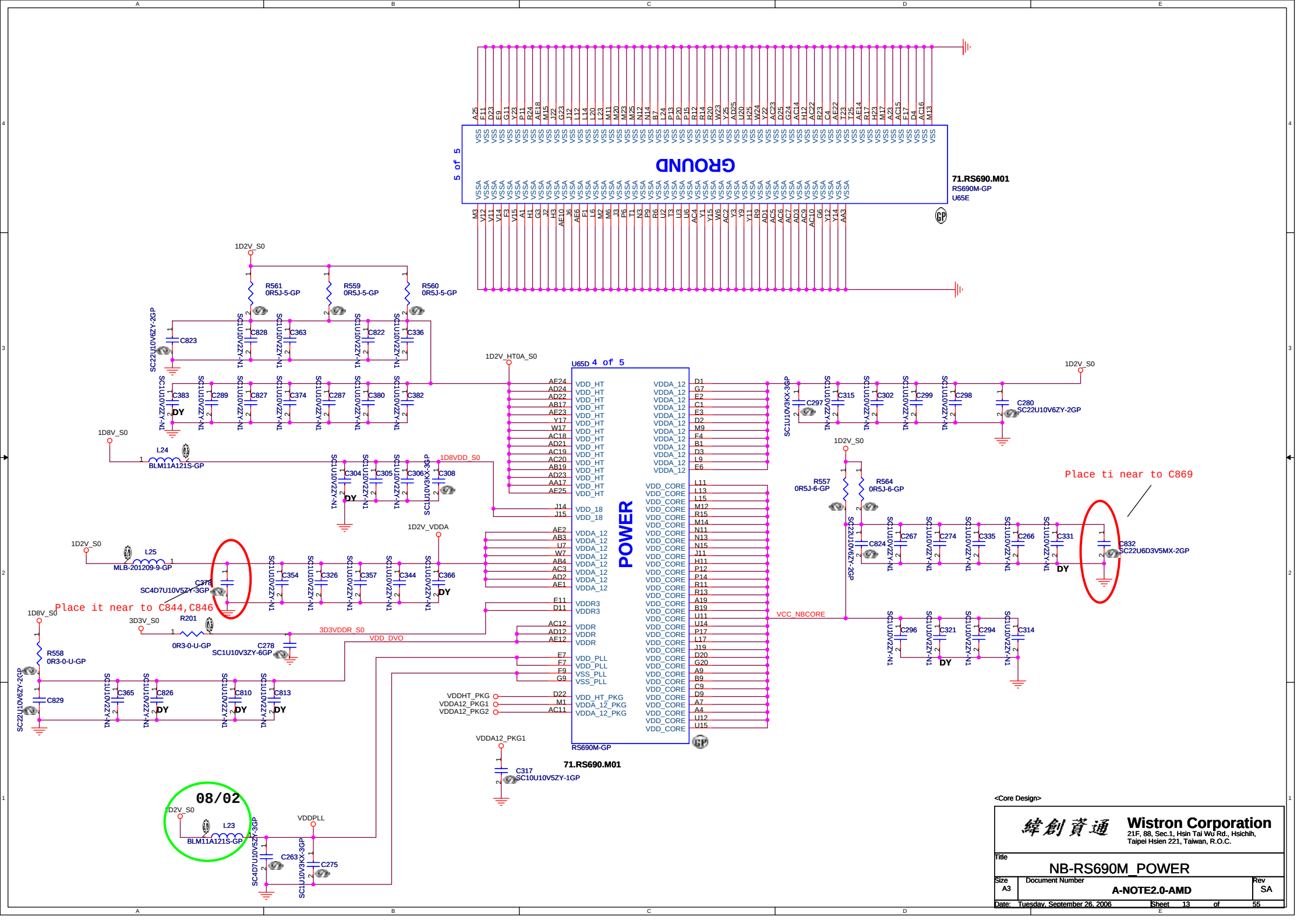
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_MEM/PCIE_LINK I/F

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 11 of 55

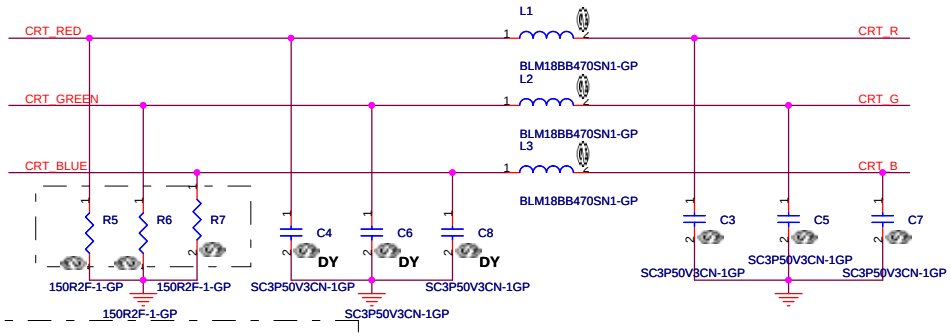

R198--R200 And R219-R220
Close to NB
U65C 3 of 5
CRT/TVOUT
PLL PWR
PM
CLOCKs
MIS.
LVDS
DVO
08/02
09/01
SD
MINI-CARD
71.RS690.M01
RESISTOR | RS480M MODE
R549 | TEST MODE
R548 | NORMAL MODE
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_VIDEO/ CLOCK
Size A3
Document Number A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 12 of 55



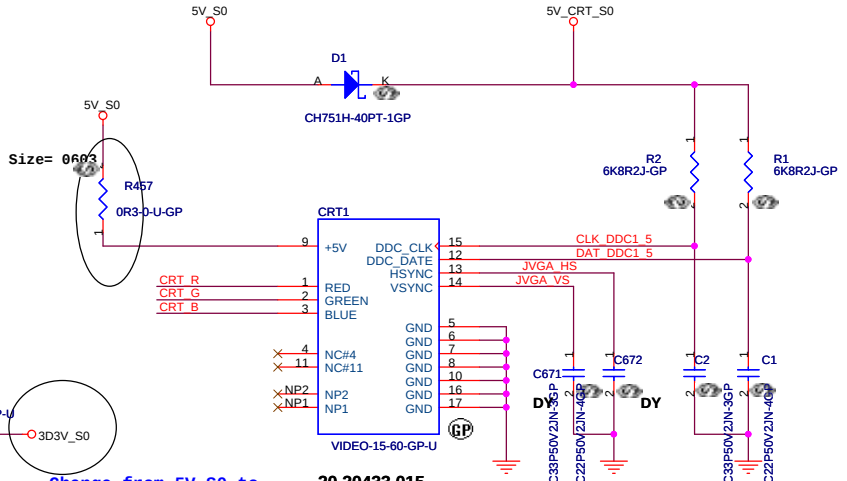
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	NB-RS690M_POWER
Size	A3
Document Number	A-NOTE2.0-AMD
Rev	SA
Date:	Tuesday, September 26, 2006
Sheet	13 of 55

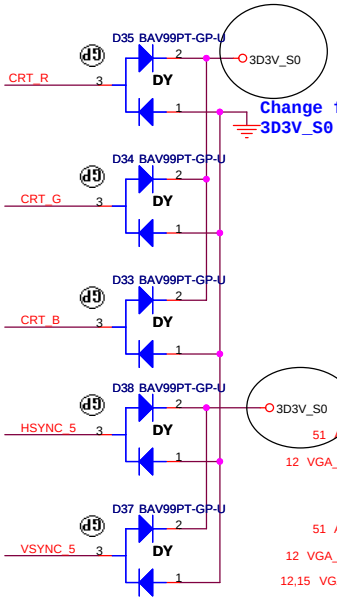
CRT I/F & CONNECTOR

Ferrite bead impedance: 47ohm@100MHz



Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
R857--R859 Close to CRT Conn,the trace impedance between NB and 150ohm resistor should be 50ohm+/-15%, the trace impedance between 150ohm resistor and conn shoulld be 75ohm+/-15%

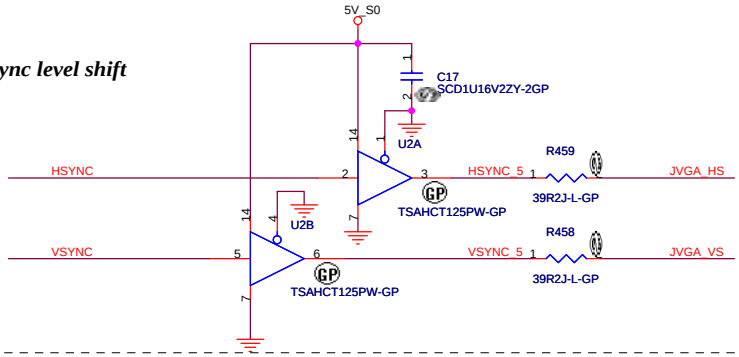




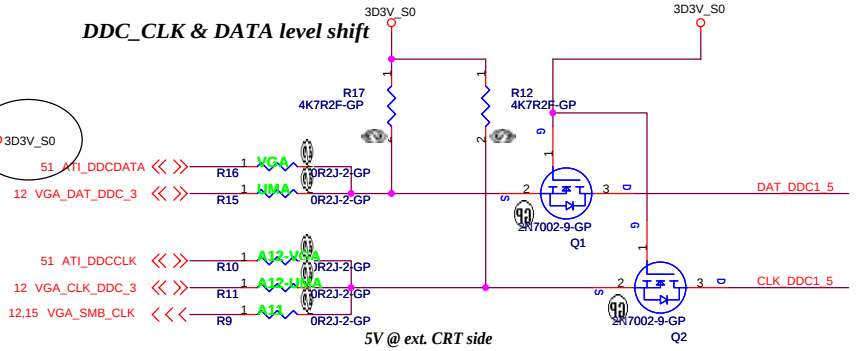
Change from 5V_S0 to 3D3V_S0 as ATI suggestion.

20.20433.015

Hsync & Vsync level shift



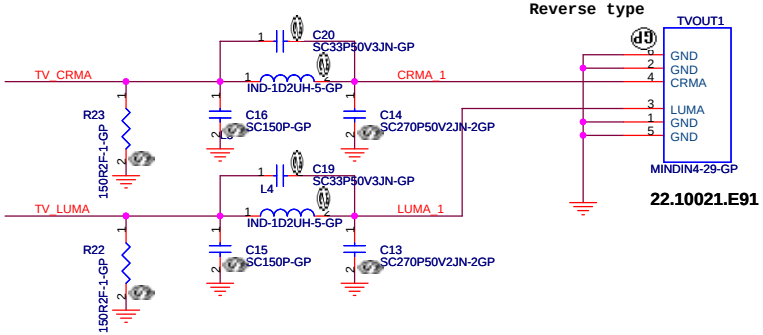
DDC_CLK & DATA level shift



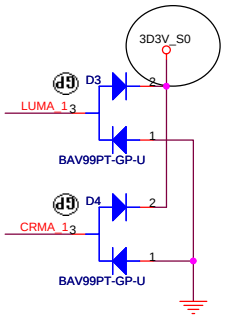
5V @ ext. CRT side

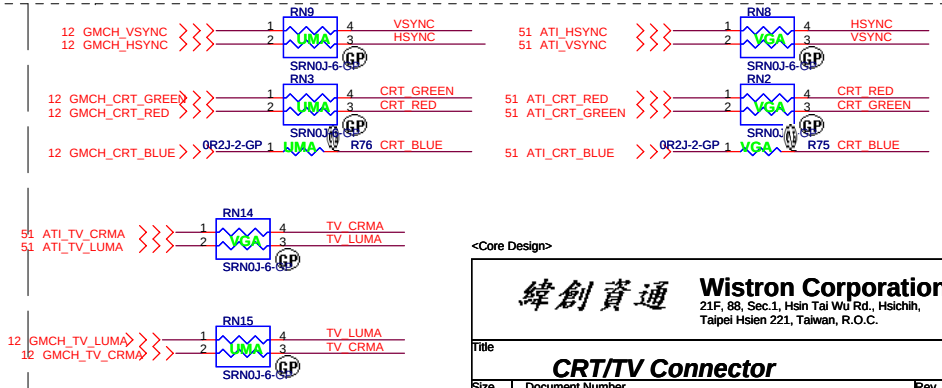
TV OUT CONN

Reverse type



22.10021.E91





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV Connector**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 14 of 55

LED / INVERTER INTERFACE

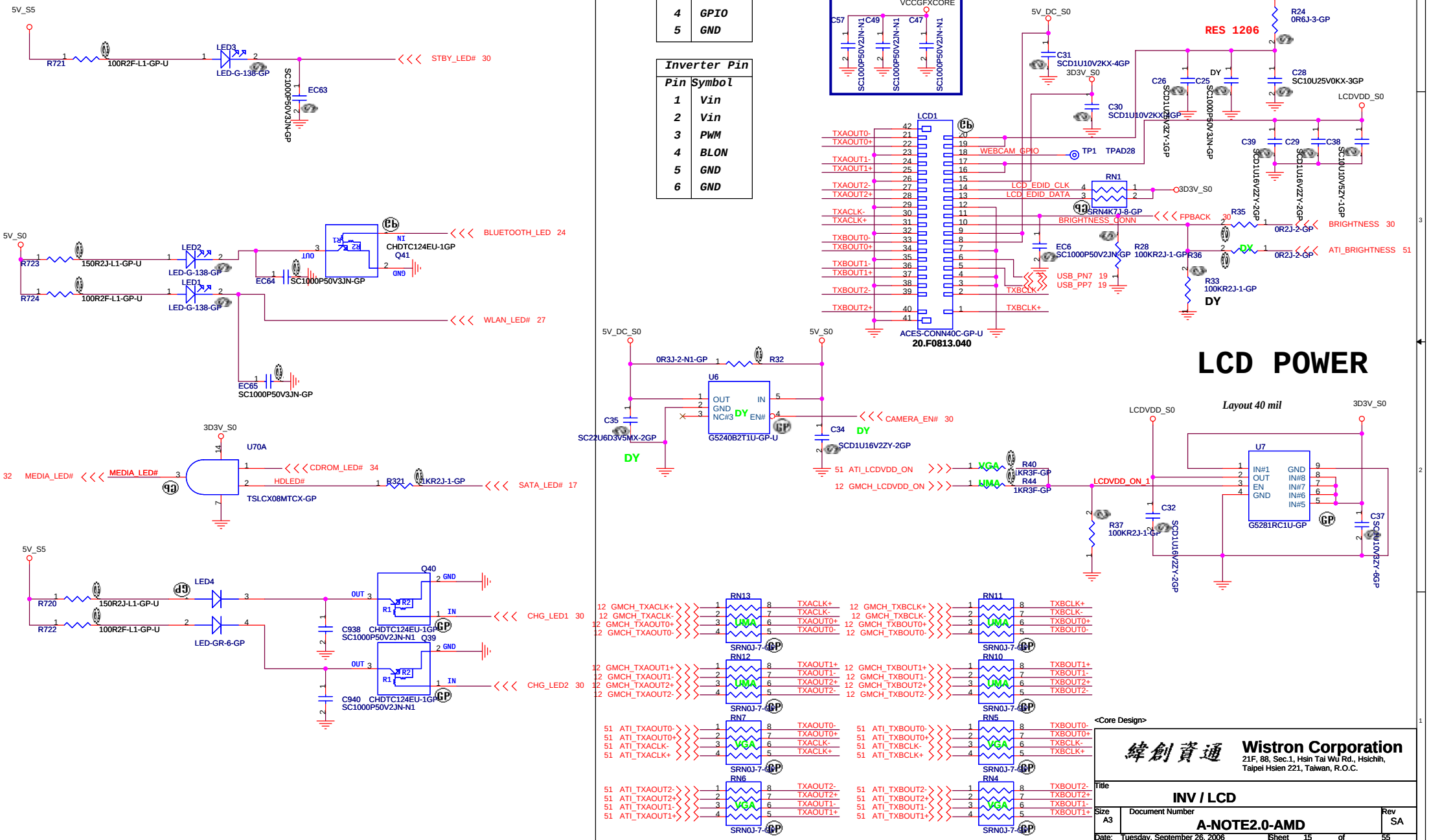
LCD/INVERTER/CCD CONN

TOP VIEW

40 LCD 1

CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GPIO
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INV / LCD

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 15 of 55

Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

32K suspend clock output

SB600 asserts PLTRST# to reset devices on the platform.

Secondary PCI Bus reset signal.

PCIRST# 3V to 5V level shift for HDD & CDROM

08/28

2nd source: 20.D0198.103

SB600-GP

71.SB600.00U

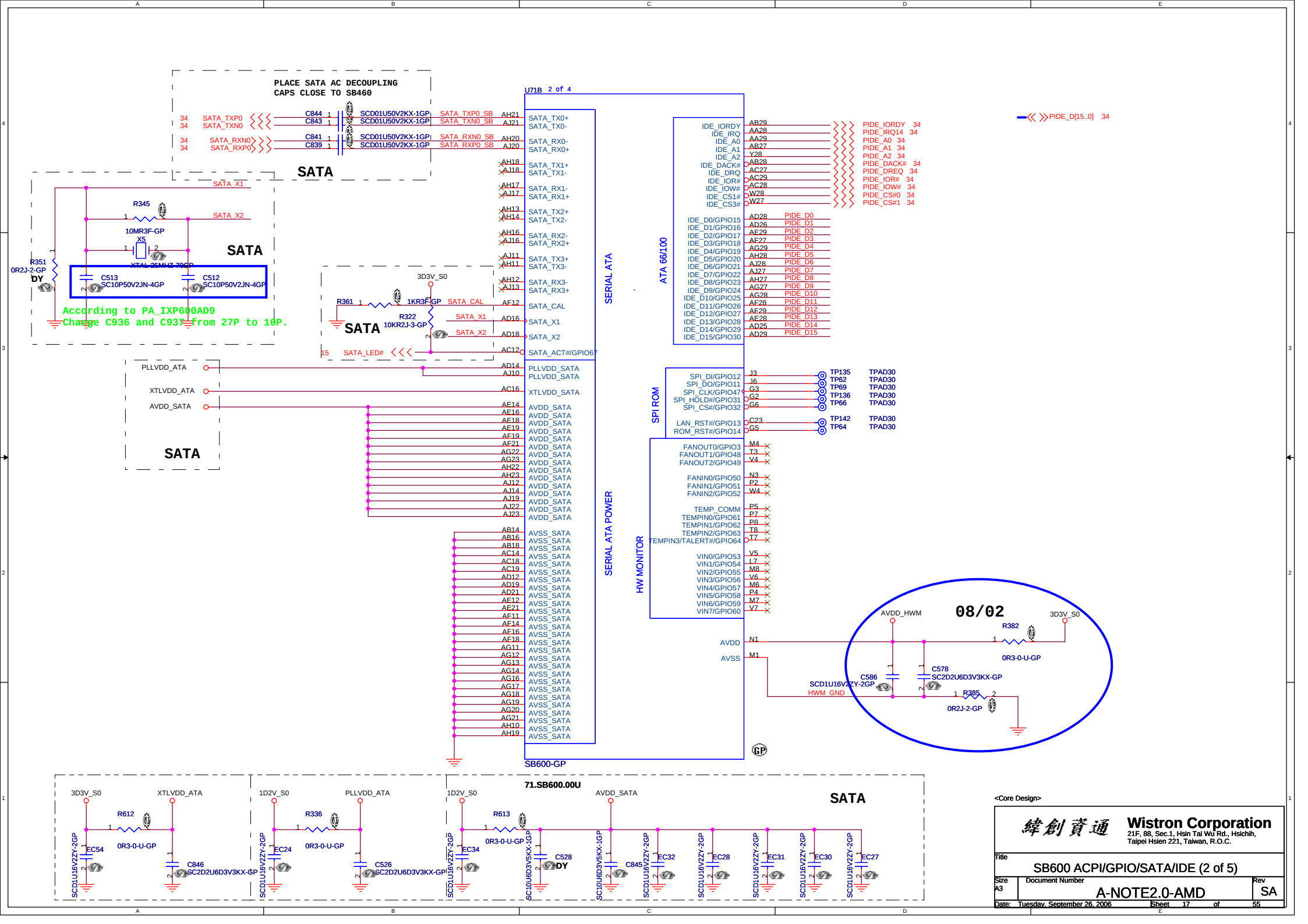
<Core Design>

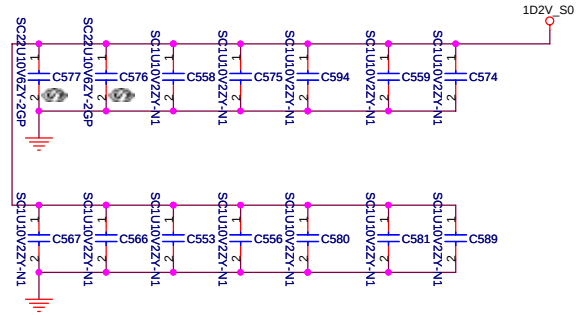
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

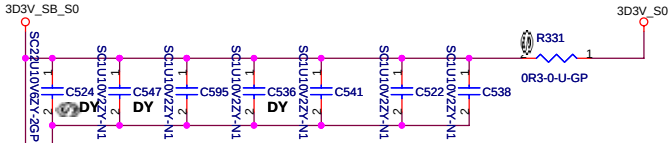
Title: SB600 PCI/CPU/LPC/RTC (1 of 5)

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

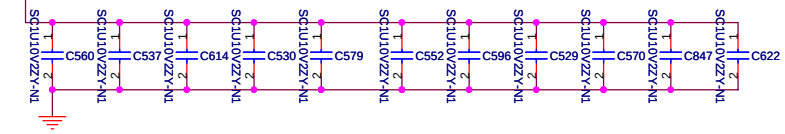
Date: Tuesday, September 26, 2006 | Sheet 16 of 55

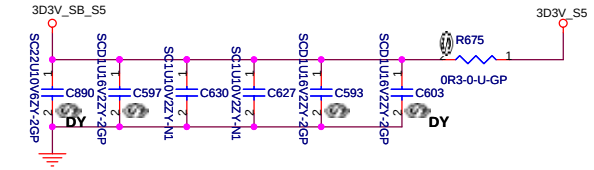

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460
SATA
SATA
SATA
SATA
According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.
U71B 2 of 4
SERIAL ATA
SERIAL ATA POWER
ATA 66/100
SPI ROM
HW MONITOR
SB600-GP
71.SB600.00U
08/02
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 ACPI/GPIO/SATA/IDE (2 of 5)
A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 17 of 55

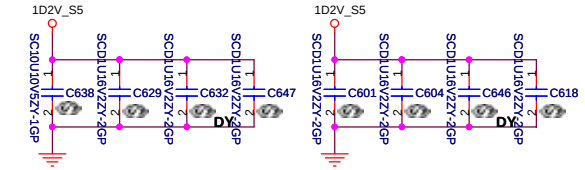


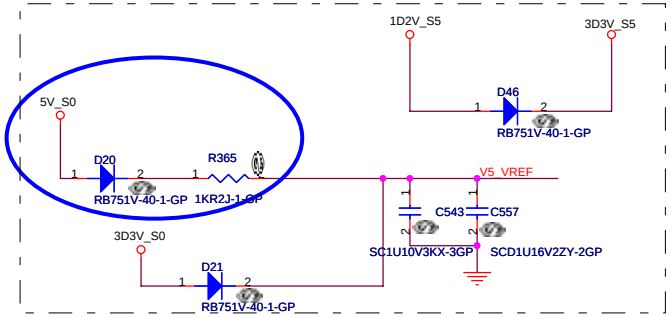


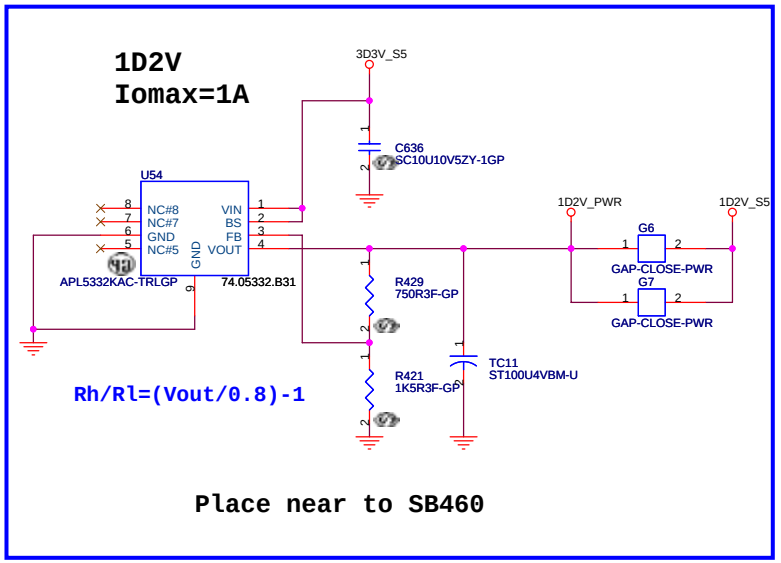
2Pin Use One Capcitance Uniformly.

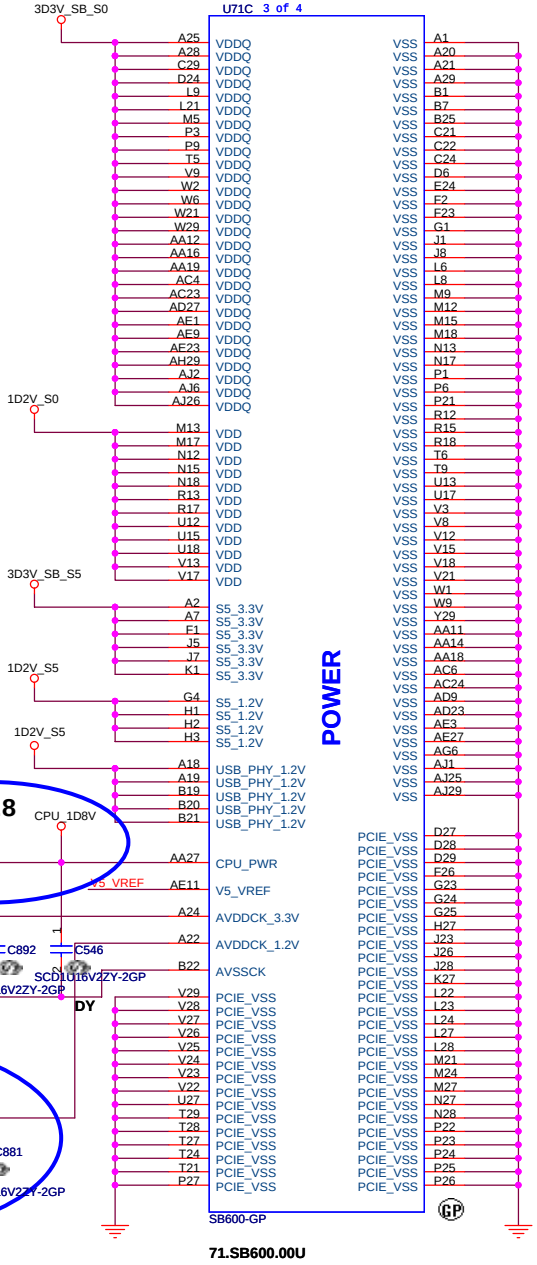












<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 POWER/DECOUPLING**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 18 of 55

DY-T 11/02,
DUMMY refer to
ATI reference circuit
ver1.1

GPIO1 Has Internal
Pull-Up To 3.3V_S0

Lynx Board Version Setting

Ver.	PCB_VER0	PCB_VER1
SA	0	0
SB	0	1
SC	1	0
SD	1	1

CHECK SB VERSION

SPEC change

USB	
Pair	Device
0	USB0
1	USB1
2	USB2
3	USB2
4	Mini-Card
5	Bluetooth
6	Reserved
7	CCD
8	Finger Print
9	New Card

New Card
Finger Print
CCD
Bluetooth
Mini-Card
USB2
USB2
USB1
USB0

U71D 4 of 4

ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR

SB600-GP

71.SB600.00U

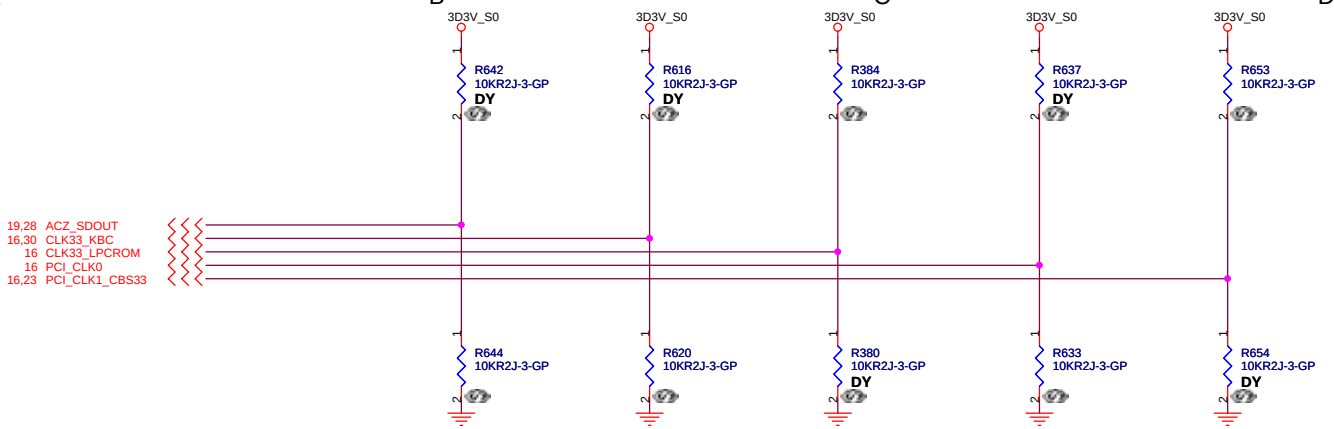
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 AC97/USB

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

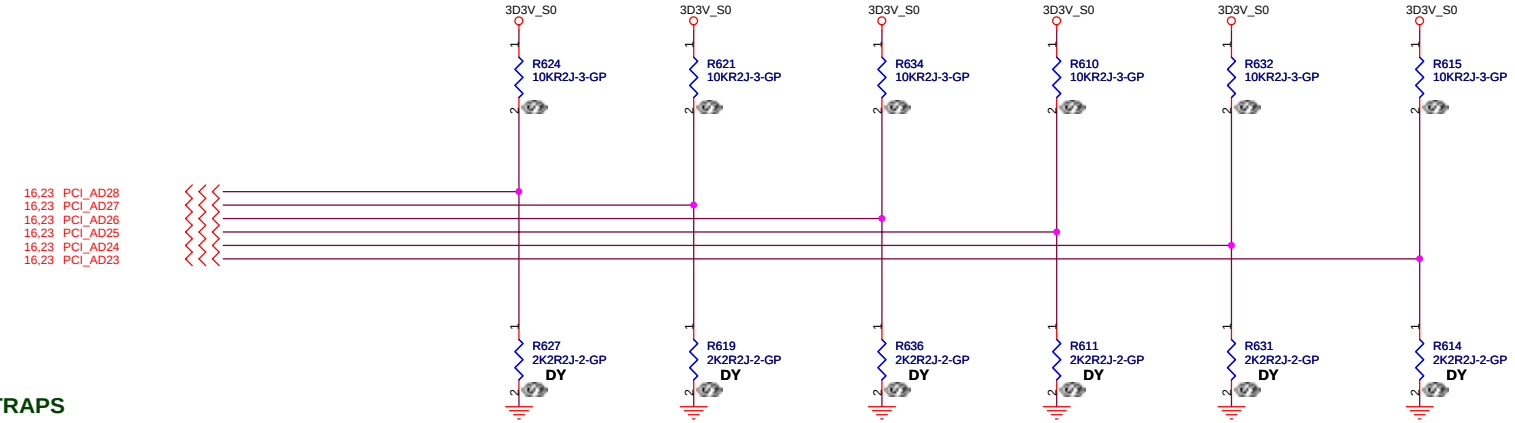
Date: Tuesday, September 26, 2006 | Sheet 19 of 55



REQUIRED SYSTEM STRAPS

		AC_SDOUT	PCI_CLK0,PCI_CLK1_CBS33	PCI_CLK4	PCI_CLK6
STRAP HIGH		USE DEBUG STRAPS	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	USB INT PLL48	CPU I/F=K8 DEFAULT
STRAP LOW		IGNORE DEBUG STRAPS DEFAULT	L,H=LPC ROM II L,L=Firmware Hub ROM	USB EXT. 48MHZ DEFAULT	CPU I/F=P4

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

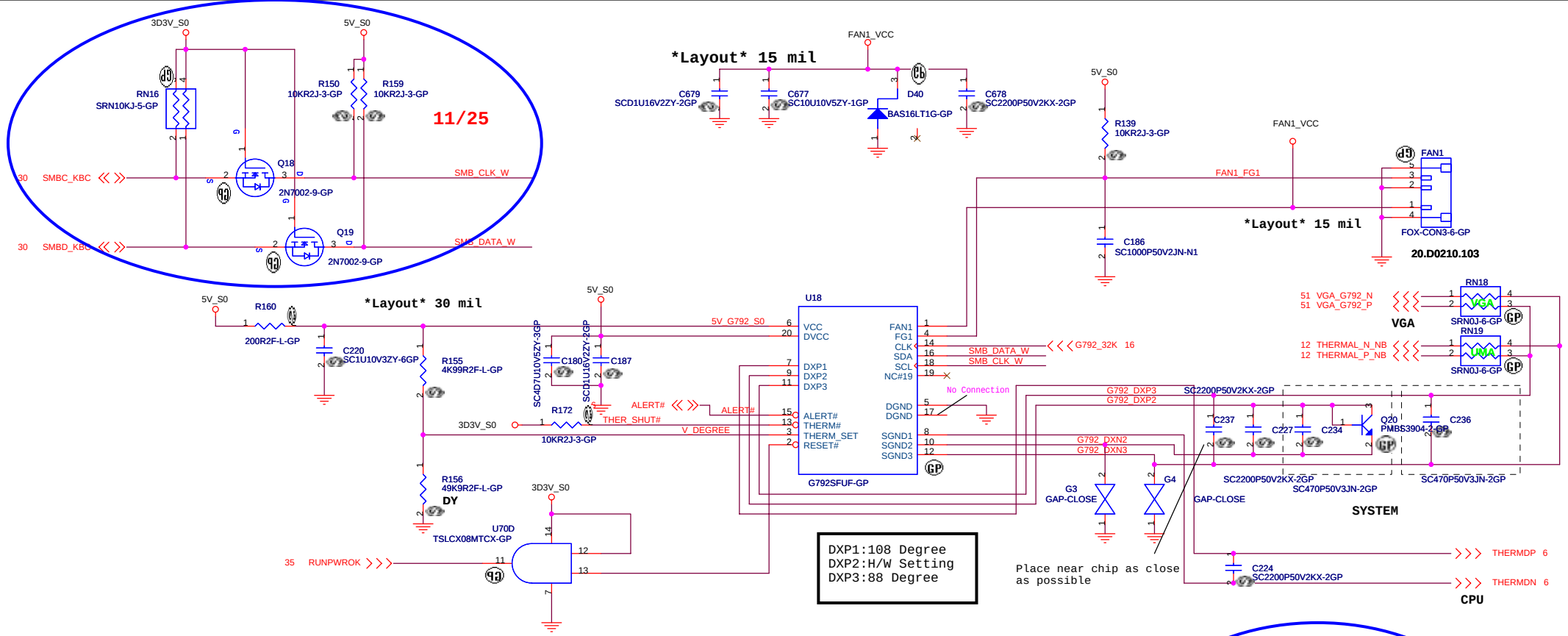
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

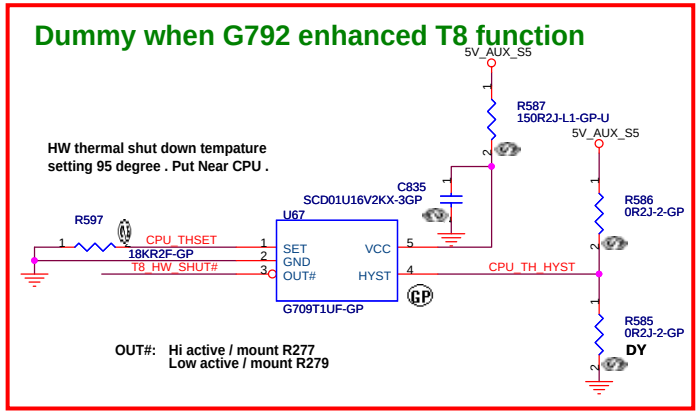
Title: SB600 STRAPPING PIN

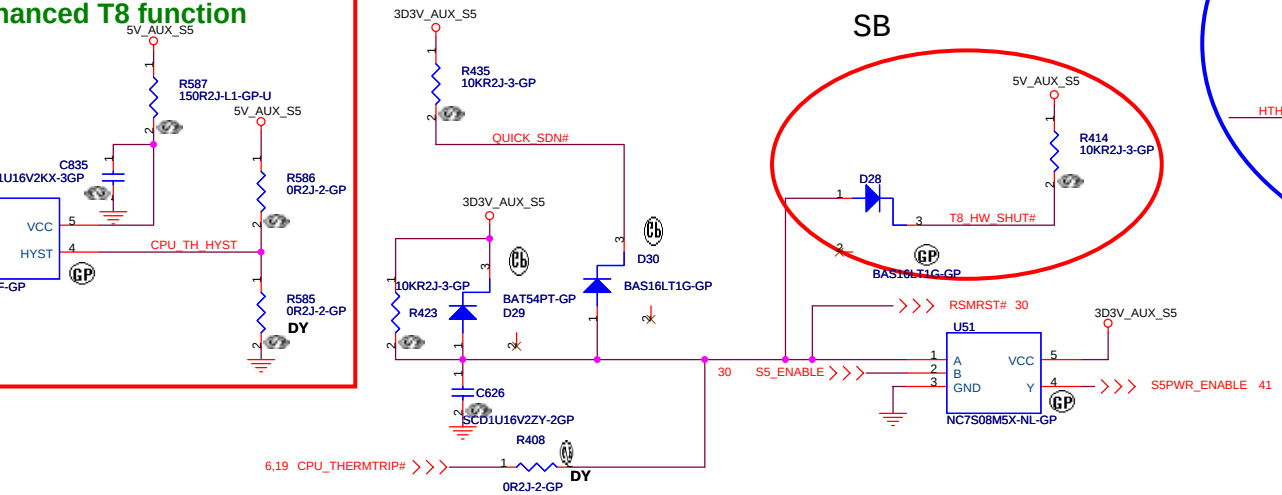
Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

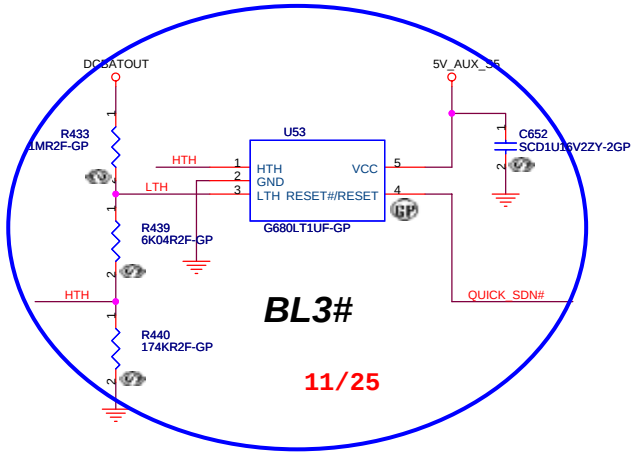
Date: Tuesday, September 26, 2006 | Sheet 20 of 55



HW Thermal Throttling







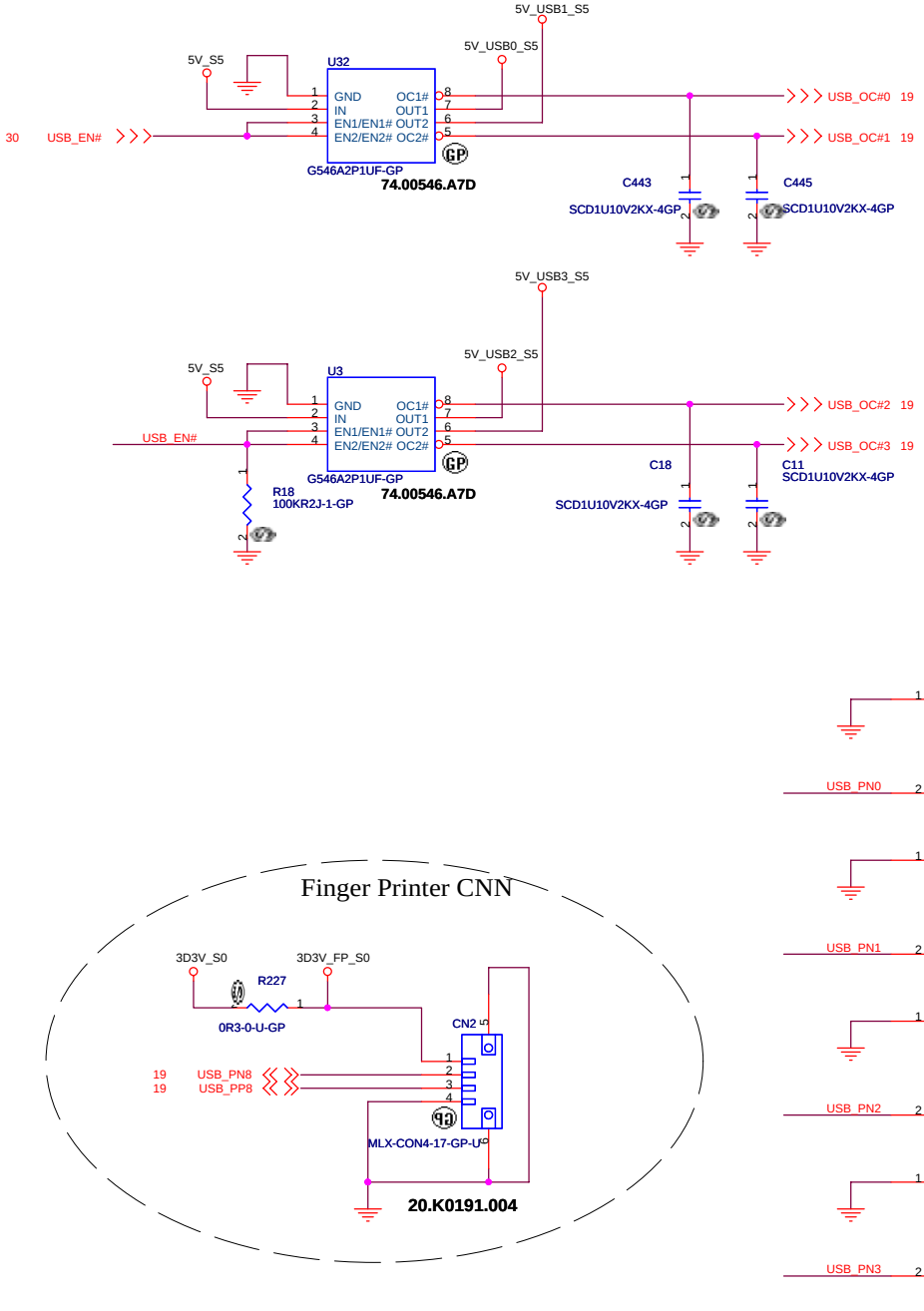
<Core Design>

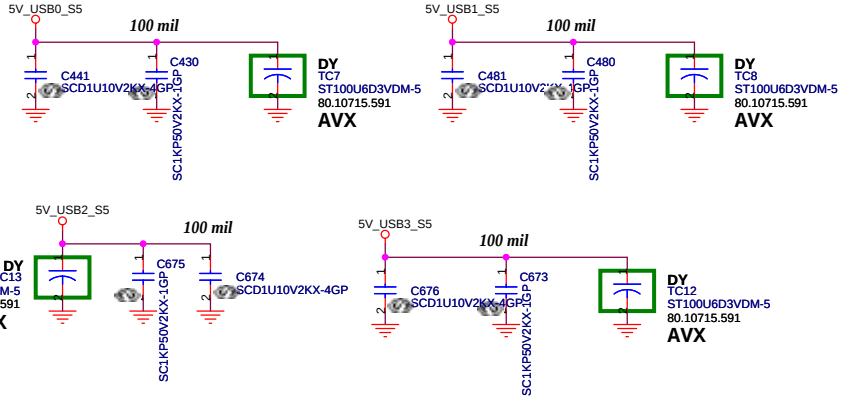
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

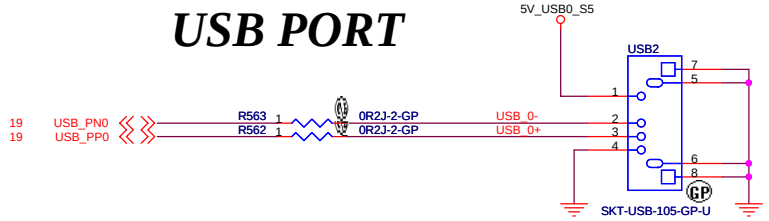
Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

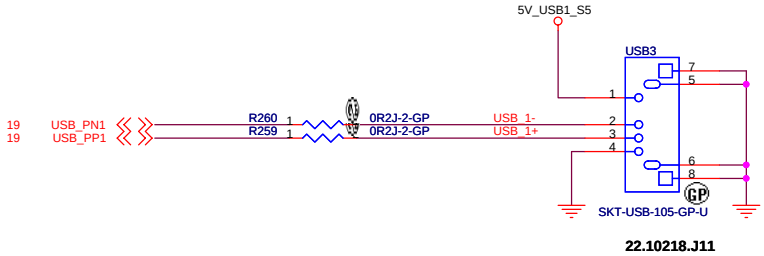
Date: Tuesday, September 26, 2006 Sheet 21 of 55





USB PORT





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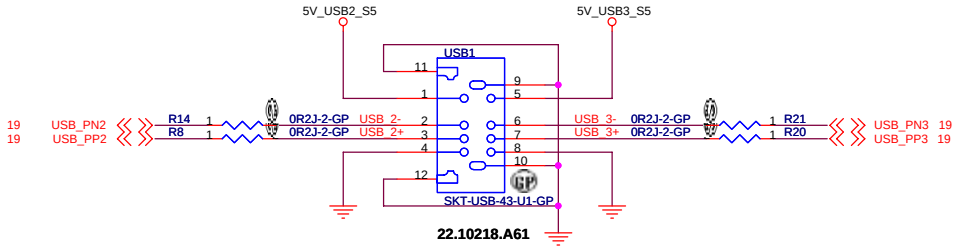
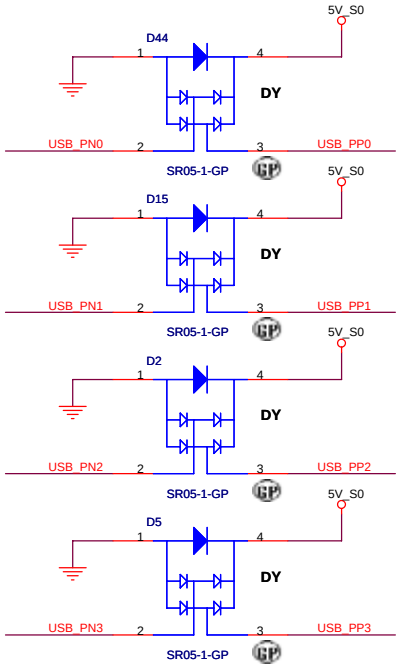
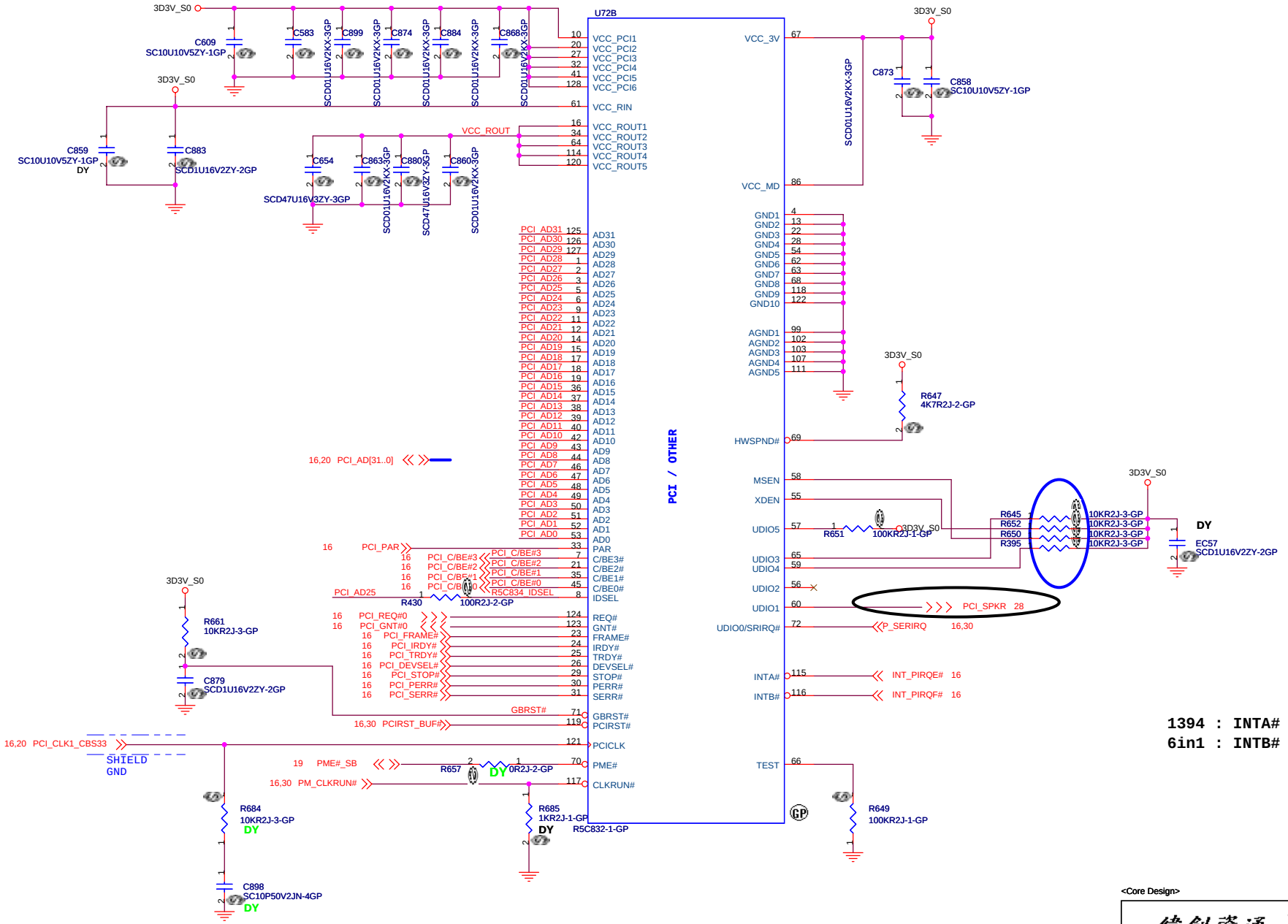


22.10218.A61



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB/MDC/BT and TV TURNER I/F		
Size: A3	Document Number: A-NOTE2.0-AMD	Rev: SA
Date: Tuesday, September 26, 2006	Sheet 22 of 55	



<Core Design>

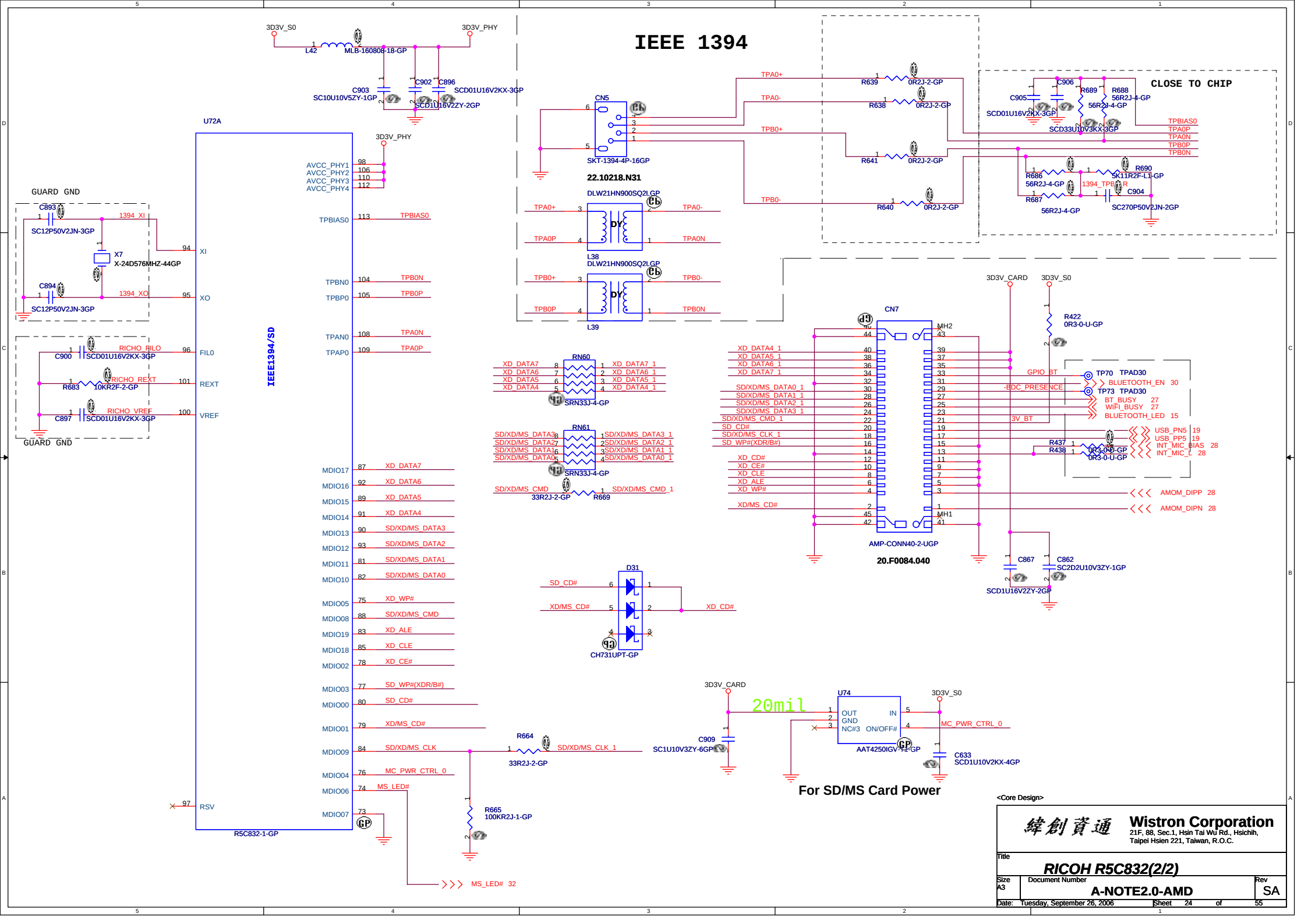
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RICOH R5C832(1/2)

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 23 of 55

IEEE 1394



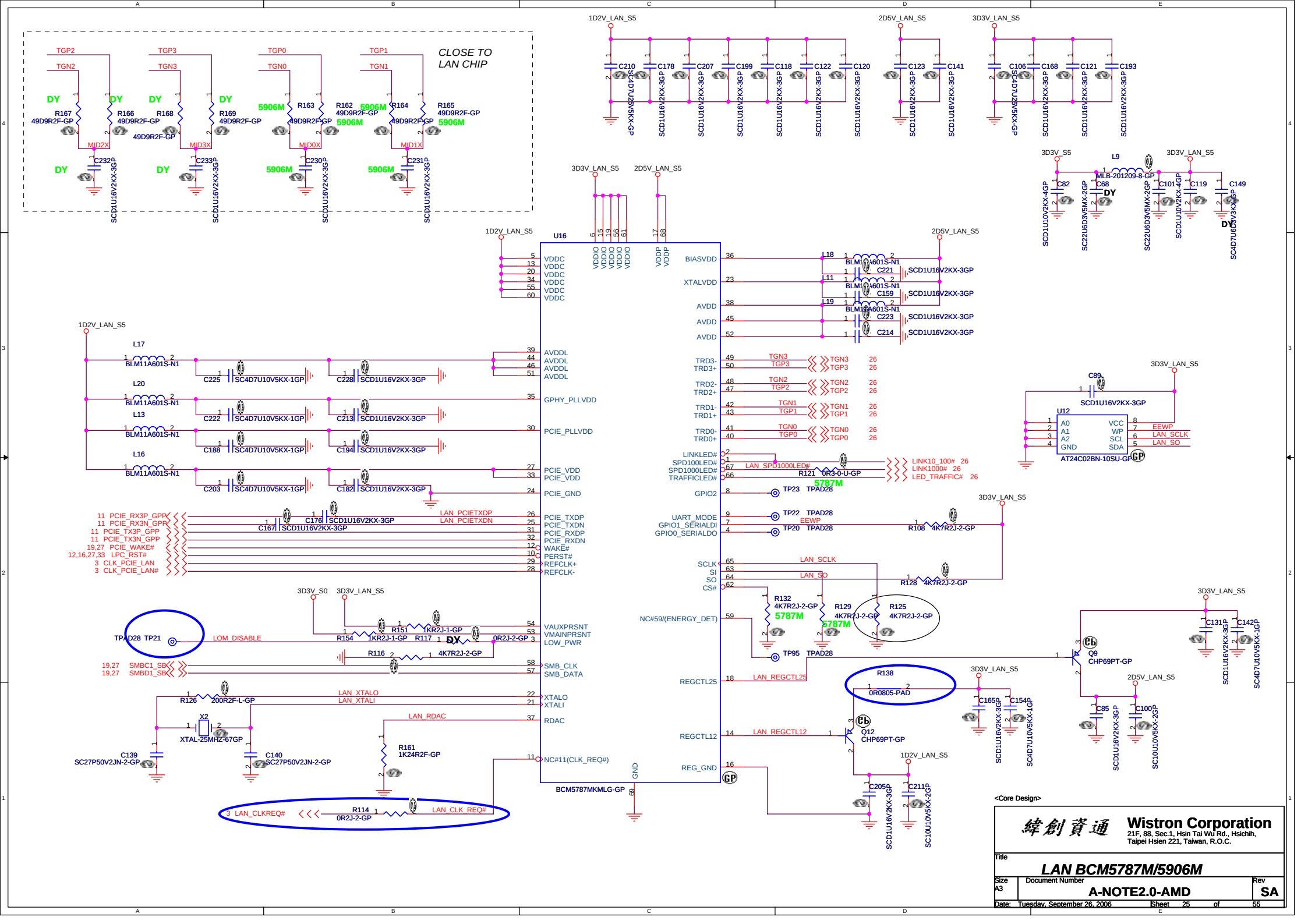
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RICOH R5C832(2/2)**

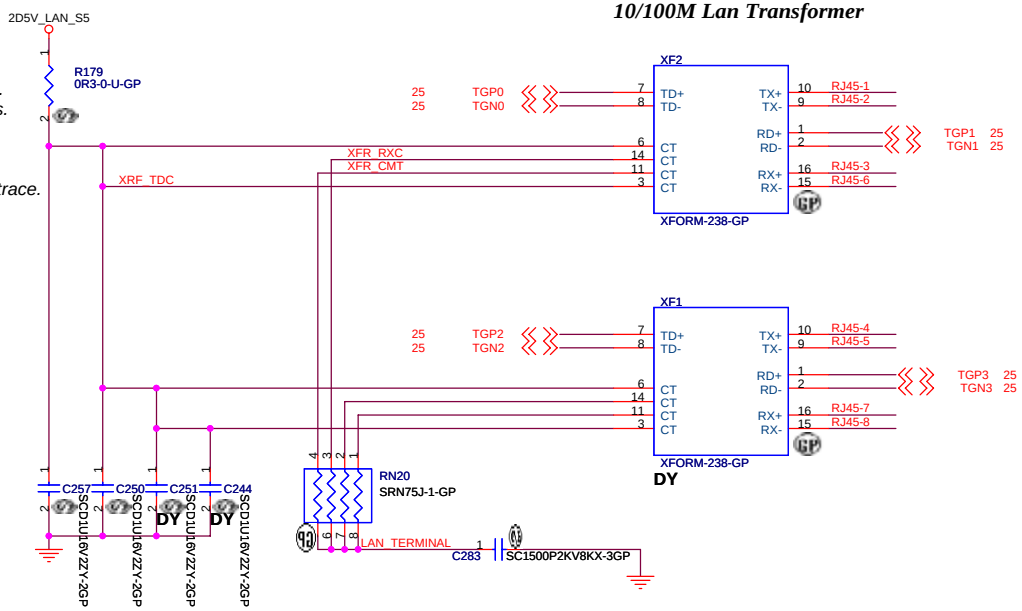
Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 24 of 55

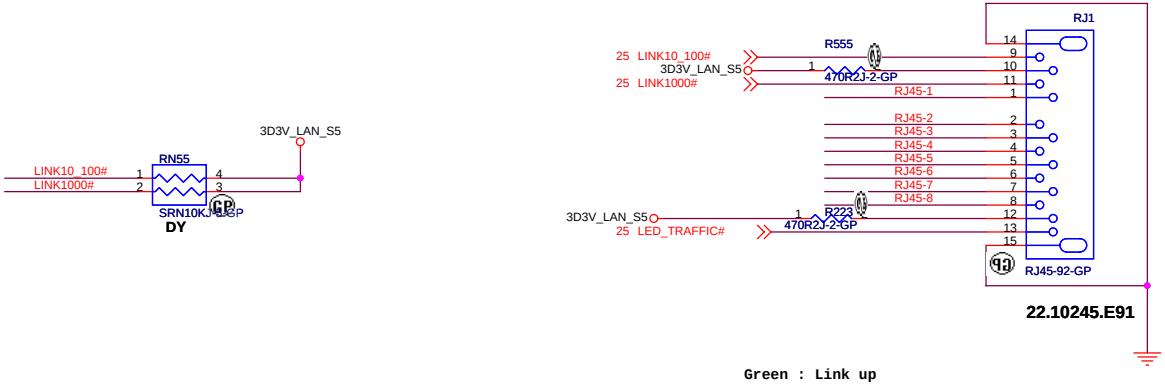

CLOSE TO LAN CHIP
TGP2
TGN2
TGP3
TGN3
TGP0
TGN0
TGP1
TGN1
DY
5906M
R167 49D9R2F-GP
R166 49D9R2F-GP
R168 49D9R2F-GP
R169 49D9R2F-GP
R163 49D9R2F-GP
R162 49D9R2F-GP
R164 49D9R2F-GP
R165 49D9R2F-GP
MID2X
MID3X
MID0X
MID1X
C232
C233
C230
C231
SCD1U16V2KX-3GP
1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
C210
C178
C207
C199
C118
C122
C120
C123
C141
C106
C168
C121
C193
SCD1U16V2KX-3GP
SCD1U16V2KX-3GP
L9
MLB-201209-8-GP
C82
C68
C101
C119
C149
SCD1U10V2KX-4GP
SC22U6D3V5MX-2GP
SC22U6D3V5MX-2GP
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
3D3V_S0
2D5V_S5
U16
VDDIO
VDDP
VDDC
BIASVDD
XTALVDD
AVDD
AVDDL
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_VDD
PCIE_GND
PCIE_TXDP
PCIE_TXDN
PCIE_RXDP
PCIE_RXDN
WAKE#
PERST#
REFCLK+
REFCLK-
TRD3-
TRD3+
TRD2-
TRD2+
TRD1-
TRD1+
TRD0-
TRD0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
GPIO2
UART_MODE
GPIO1_SERIALDI
GPIO0_SERIALDO
SCLK
SI
SO
CS#
NC#59/(ENERGY_DET)
REGCTL25
REGCTL12
REG_GND
VAUXPRSNT
VMAINPRSNT
LOW_PWR
SMB_CLK
SMB_DATA
XTALO
XTALI
RDAC
NC#11(CLK_REQ#)
GND
BCM5787MKMLG-GP
L17
L20
L13
L16
L18
L11
L19
BLM11A601S-N1
C225
C222
C188
C203
C228
C213
C194
C182
C221
C159
C223
C214
SC4D7U10V5KX-1GP
SCD1U16V2KX-3GP
TGN3
TGP3
TGN2
TGP2
TGN1
TGP1
TGN0
TGP0
26
LAN_SPD1000LED#
R121 0R3-0-U-GP
5787M
LINK10_100#
LINK1000#
LED_TRAFFIC#
TP23 TPAD28
TP22 TPAD28
EEWP
TP20 TPAD28
R108 4K7R2J-2-GP
R128 4K7R2J-2-GP
LAN_SCLK
LAN_SO
R132 4K7R2J-2-GP
R129 4K7R2J-2-GP
R125 4K7R2J-2-GP
TP95 TPAD28
R138 0R0805-PAD
LAN_REGCTL25
LAN_REGCTL12
Q12 CHP69PT-GP
Q9 CHP69PT-GP
C165
C154
C85
C100
C131
C142
SCD1U16V2KX-3GP
SC4D7U10V5KX-1GP
SCD1U16V2KX-3GP
SC10U10V5KX-2GP
SCD1U16V2KX-3GP
SC4D7U10V5KX-1GP
C89
U12
AT24C02BN-10SU-GP
A0
A1
A2
GND
VCC
WP
SCL
SDA
EEWP
LAN_SCLK
LAN_SO
C205
C211
SCD1U16V2KX-3GP
SC10U10V5KX-2GP
11 PCIE_RX3P_GPP
11 PCIE_RX3N_GPP
11 PCIE_TX3P_GPP
11 PCIE_TX3N_GPP
19,27 PCIE_WAKE#
12,16,27,33 LPC_RST#
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
C176
C167
LAN_PCIETXDP
LAN_PCIETXDN
TPAD28 TP21
LOM_DISABLE
R151 1KR2J-1-GP
R154 1KR2J-1-GP
R117 DX
0R2J-2-GP
R116 4K7R2J-2-GP
19,27 SMBC1_SB
19,27 SMBD1_SB
R126 200R2F-L-GP
X2
XTAL-25MHZ-67GP
C139 SC27P50V2JN-2-GP
C140 SC27P50V2JN-2-GP
LAN_XTALO
LAN_XTALI
LAN_RDAC
R161 1K24R2F-GP
3 LAN_CLKREQ#
R114 0R2J-2-GP
LAN_CLK_REQ#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN BCM5787M/5906M
Size A3
Document Number A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 25 of 55

10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



PIN09 : GREEN
PIN11 : ORANGE



Green : Link up
Blinking : TX/RX activity

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

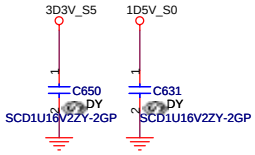
Title: **LAN Connector**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

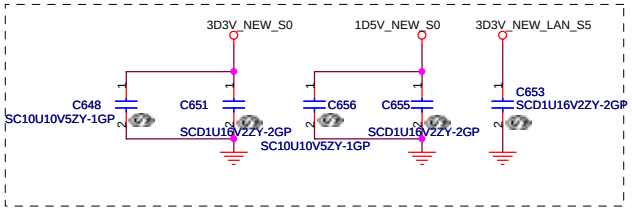
Date: Tuesday, September 26, 2006 Sheet 26 of 55

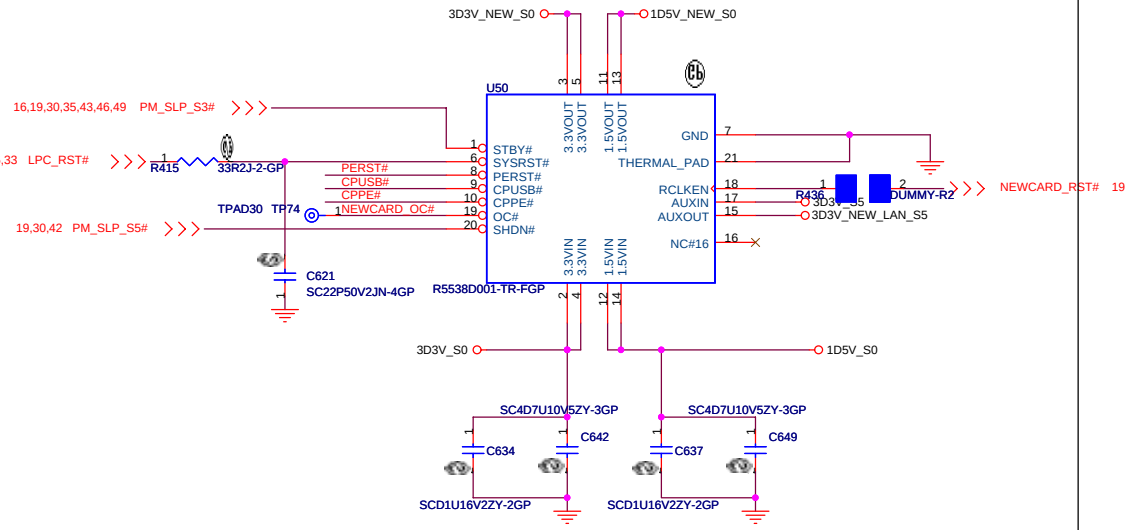
NEWCARD Connector

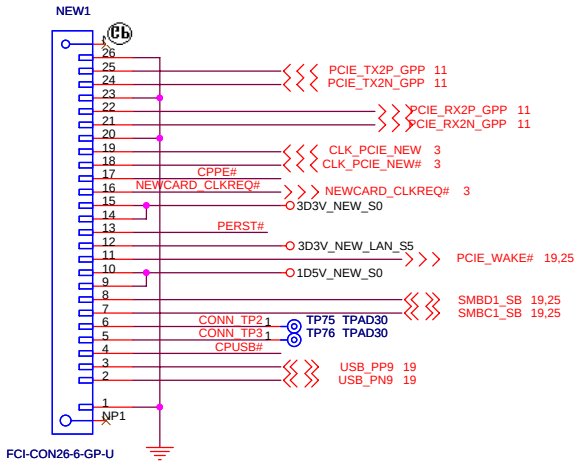
Place them Near to Chip



Place them Near to Connector







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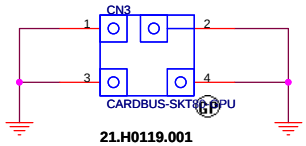
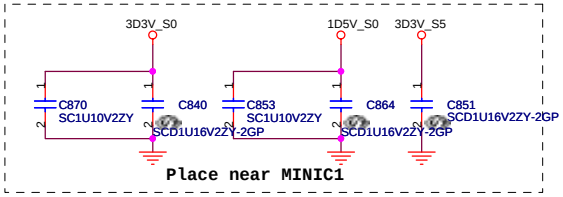


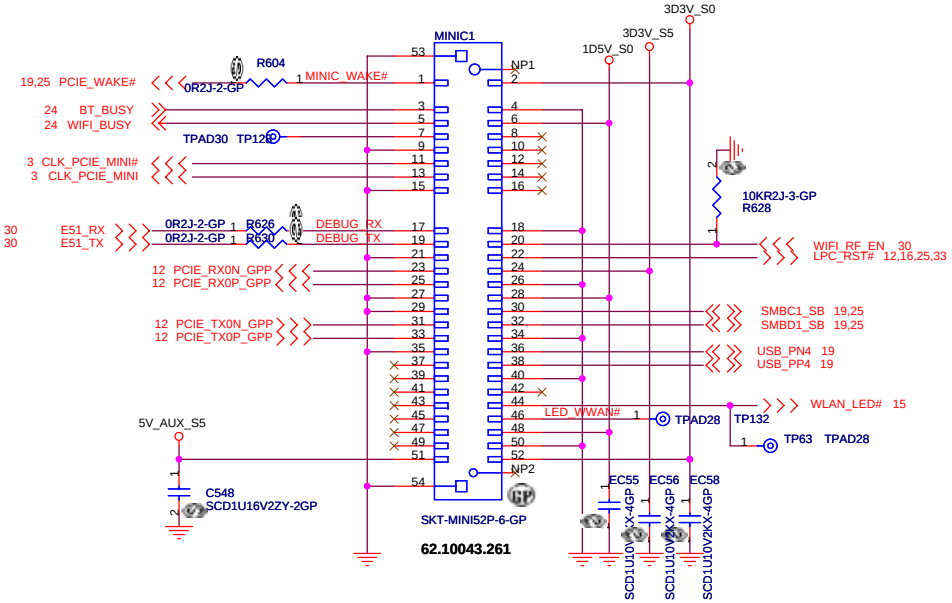
21.H0119.001

For Newcard socket

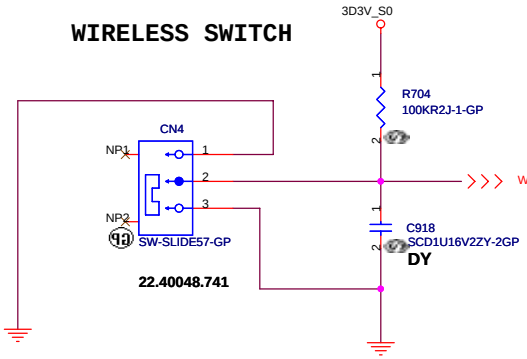


Place near MINIC1

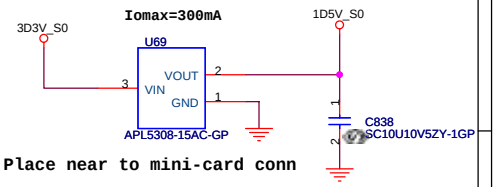
Mini Card Connector



WIRELESS SWITCH



22.40048.741

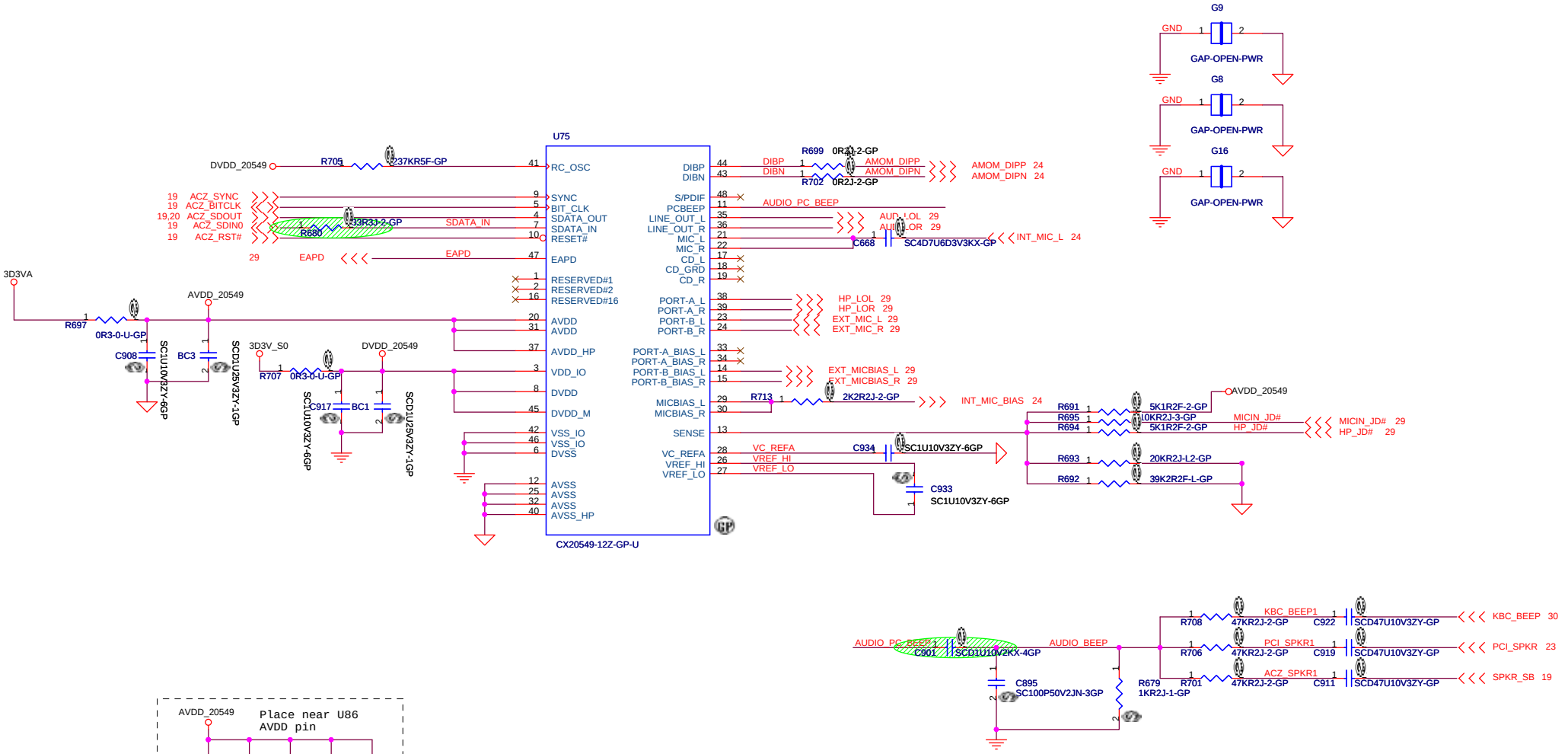


Place near to mini-card conn

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MINI-PCIE***	
Size A3	Document Number **A-NOTE2.0-AMD**	Rev SA
Date: Tuesday, September 26, 2006	Sheet 27 of 55	



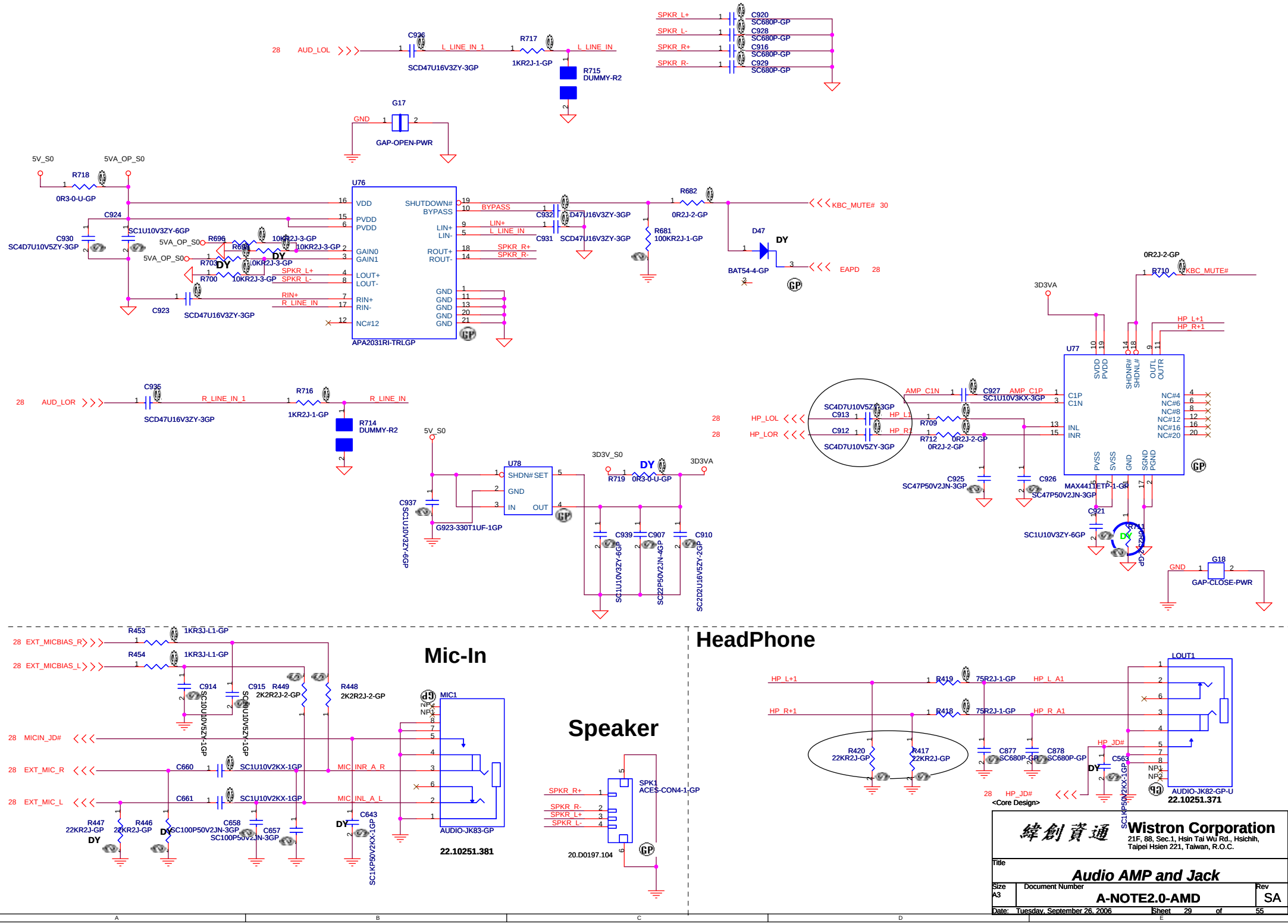
<Core Design>

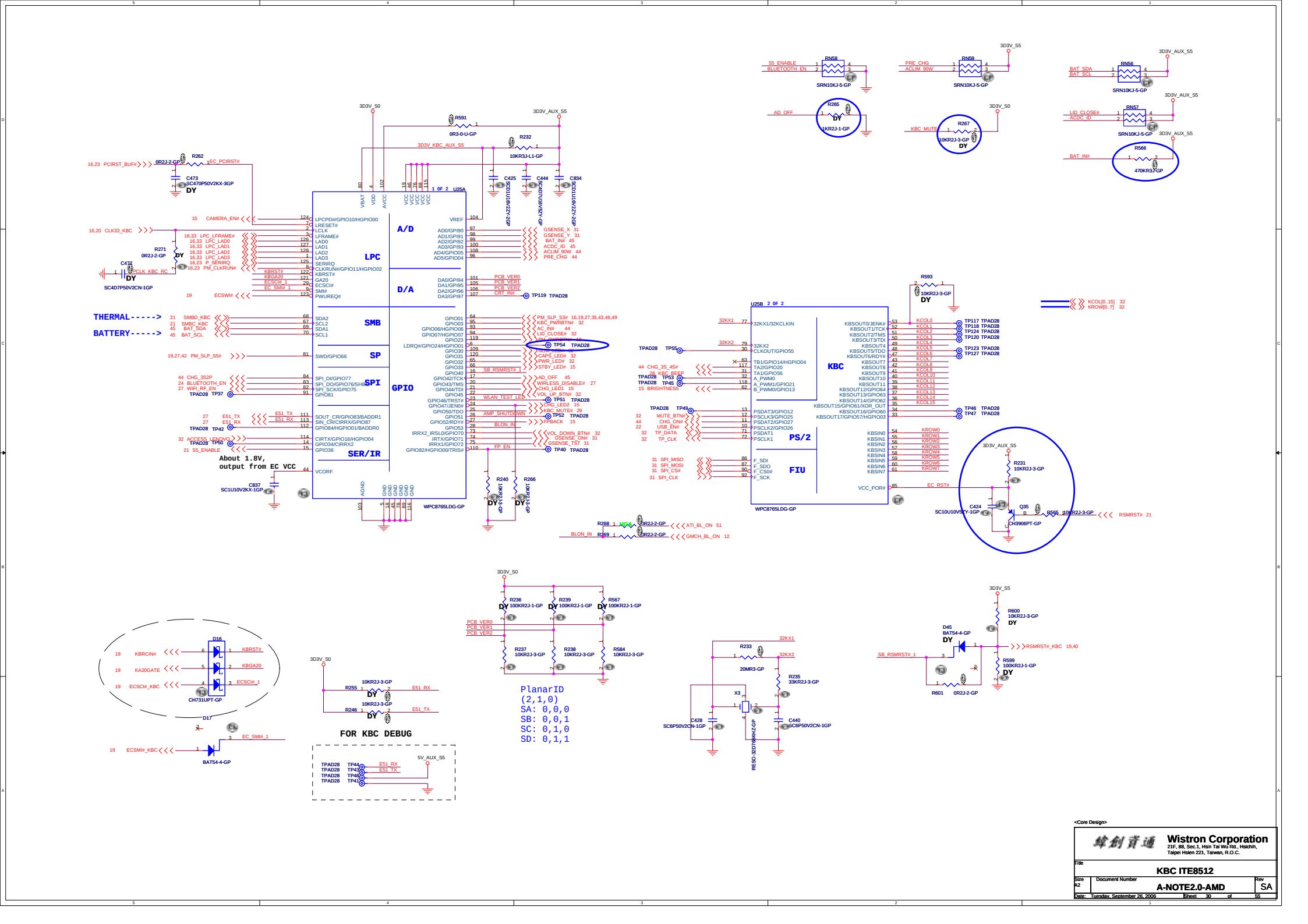
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

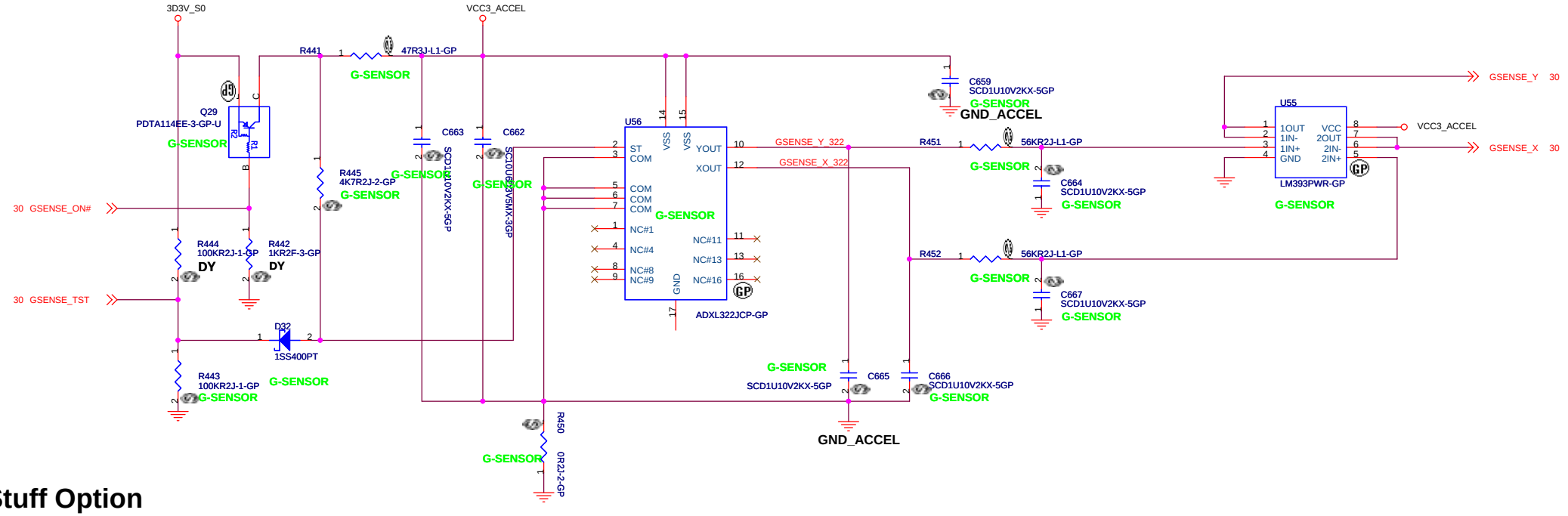
Title: AUDIO (1/2) -- CODEC CX20549

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 28 of 55


C926
SCD47U16V3ZY-3GP
R717
1KR2J-1-GP
R715
DUMMY-R2
G17
GAP-OPEN-PWR
C920
SC680P-GP
C928
SC680P-GP
C916
SC680P-GP
C929
SC680P-GP
U76
APA2031RI-TRLGP
R718
0R3-0-U-GP
C924
SC1U10V3ZY-6GP
C930
SC4D7U10V5ZY-3GP
C923
SCD47U16V3ZY-3GP
R696
R699
R703
R700
10KR2J-3-GP
C932
C931
R682
0R2J-2-GP
R681
100KR2J-1-GP
D47
BAT54-4-GP
C935
SCD47U16V3ZY-3GP
R716
1KR2J-1-GP
R714
DUMMY-R2
U78
G923-330T1UF-1GP
C937
SC1U10V3ZY-6GP
R719
0R3-0-U-GP
C939
C907
C910
SC1U10V3ZY-6GP
SC22P50V2JN-4GP
SC2D2U16V5ZY-2GP
U77
MAX4411ETP-1-GR
C927
SC1U10V3KX-3GP
C925
SC47P50V2JN-3GP
C926
SC47P50V2JN-3GP
C921
SC1U10V3ZY-6GP
R710
0R2J-2-GP
R709
R712
C912
C913
SC4D7U10V5ZY-3GP
G18
GAP-CLOSE-PWR
Mic-In
R453
R454
1KR3J-L1-GP
C914
C915
R449
2K2R2J-2-GP
R448
2K2R2J-2-GP
MIC1
AUDIO-JK83-GP
22.10251.381
C660
C661
SC1U10V2KX-1GP
C658
SC100P50V2JN-3GP
C657
SC100P50V2JN-3GP
C643
SC1K50V2KX-1GP
R447
R446
22KR2J-GP
Speaker
SPK1
ACES-CON4-1-GP
20.D0197.104
HeadPhone
R419
R418
75R2J-1-GP
R420
R417
22KR2J-GP
C877
C878
SC680P-GP
C563
SC1K50V2KX-1GP
LOUT1
AUDIO-JK82-GP-U
22.10251.371
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio AMP and Jack
Size
A3
Document Number
A-NOTE2.0-AMD
Rev
SA
Date: Tuesday, September 26, 2006
Sheet 29 of 55


THERMAL------>
BATTERY------>
About 1.8V, output from EC VCC
FOR KBC DEBUG
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
WPC8765LDG-GP
U25A 1 OF 2
U25B 2 OF 2
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ITE8512
A-NOTE2.0-AMD
Tuesday, September 26, 2006

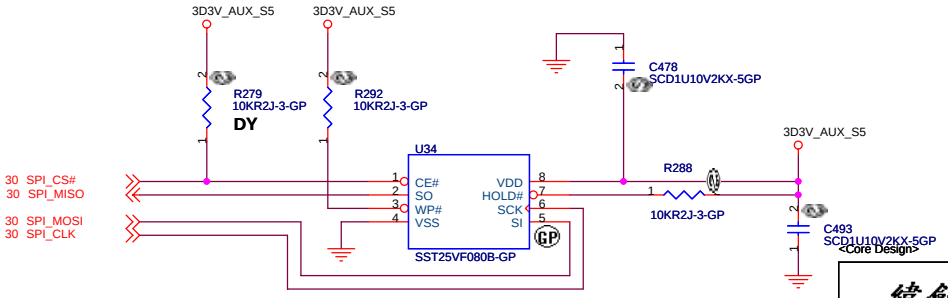


Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

SPI ROM for System & KBC



1. SST 25VF016B
2. Macronix MX25L1605A
3. SST 8Mbit 72.25080.G01

緯創資通 Wistron Corporation
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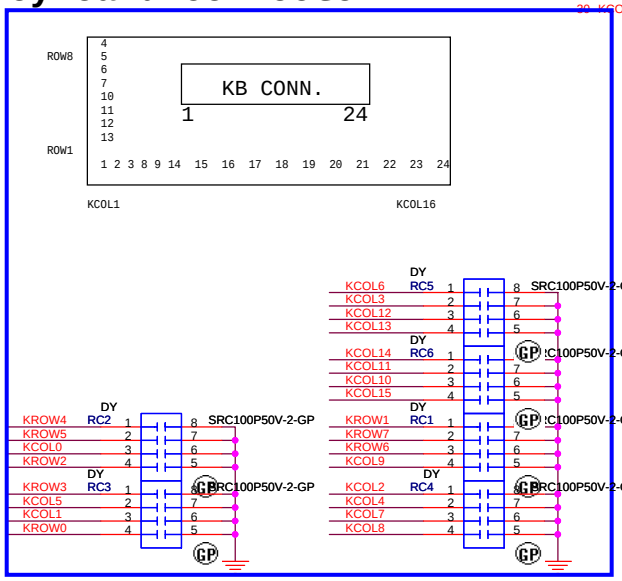
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS ROM/G-Sensor

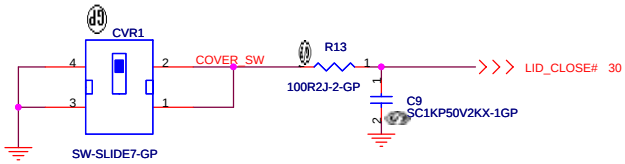
Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 31 of 55

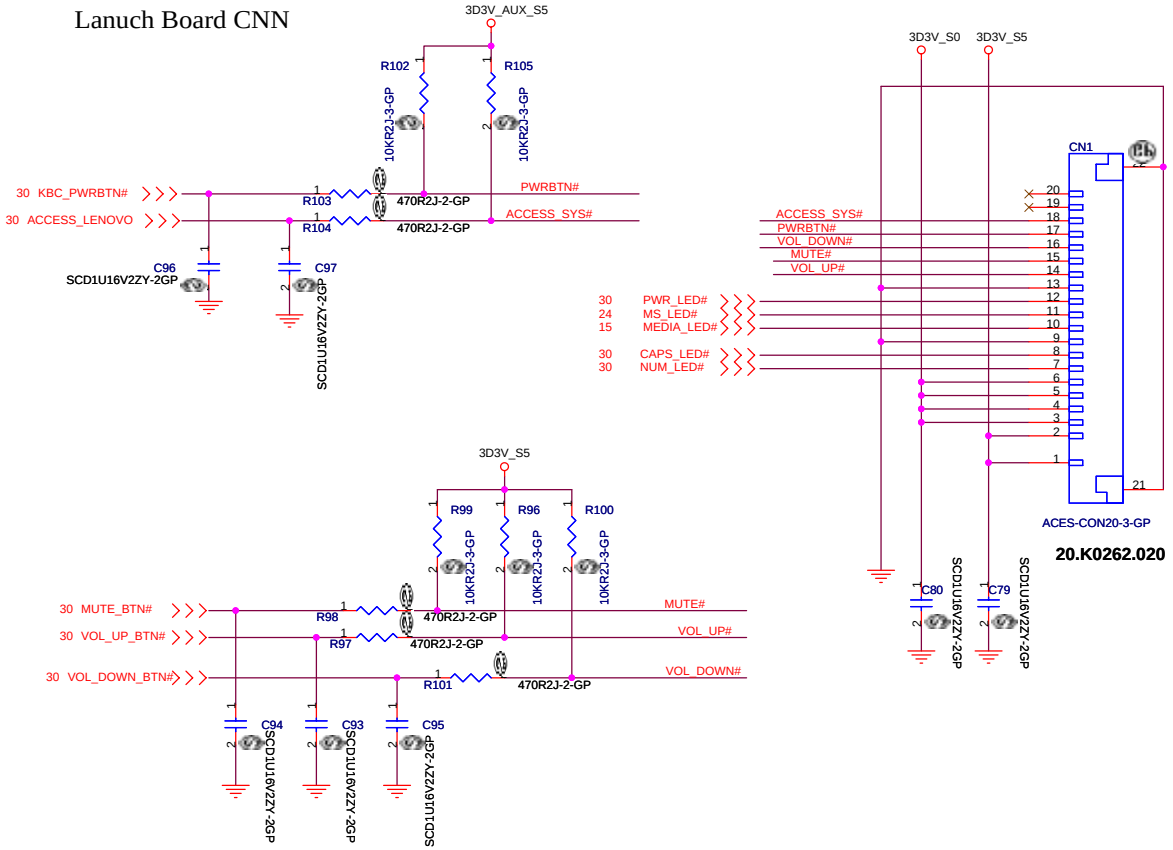
Internal KeyBoard Connector



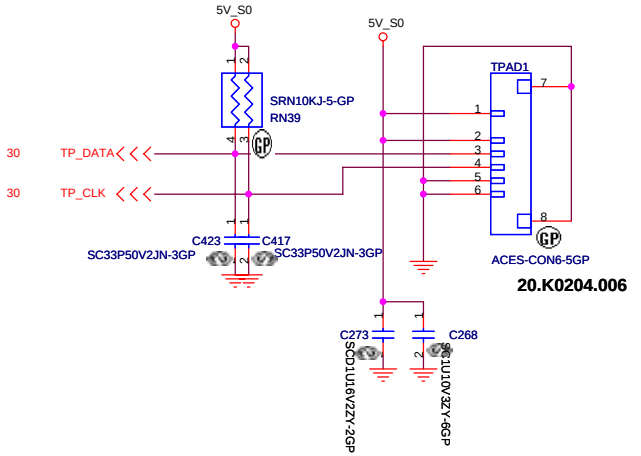
COVER SWITCH



Lanuch Board CNN



TOUCH PAD



<Core Design>

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Title: LAUNCH / TOUCHPAD / KB CONN

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 32 of 55

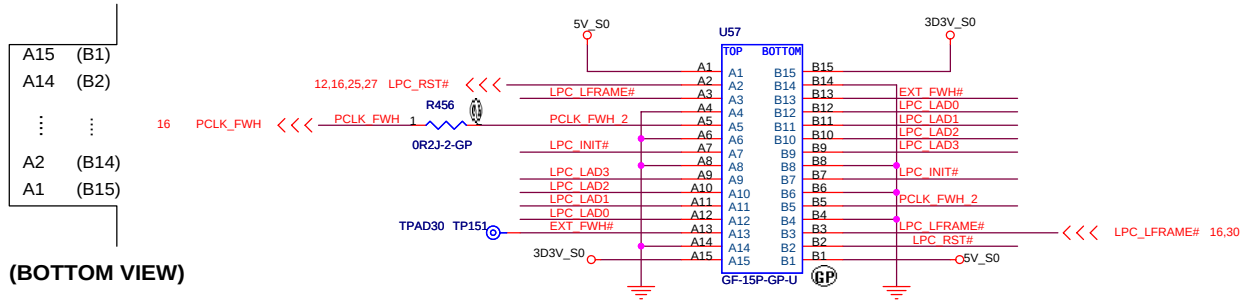
LPC_LAD[0..3] 16,30

GOLDEN FINGER FOR DEBUG BOARD

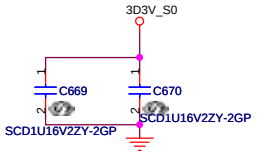
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



<Core Design>

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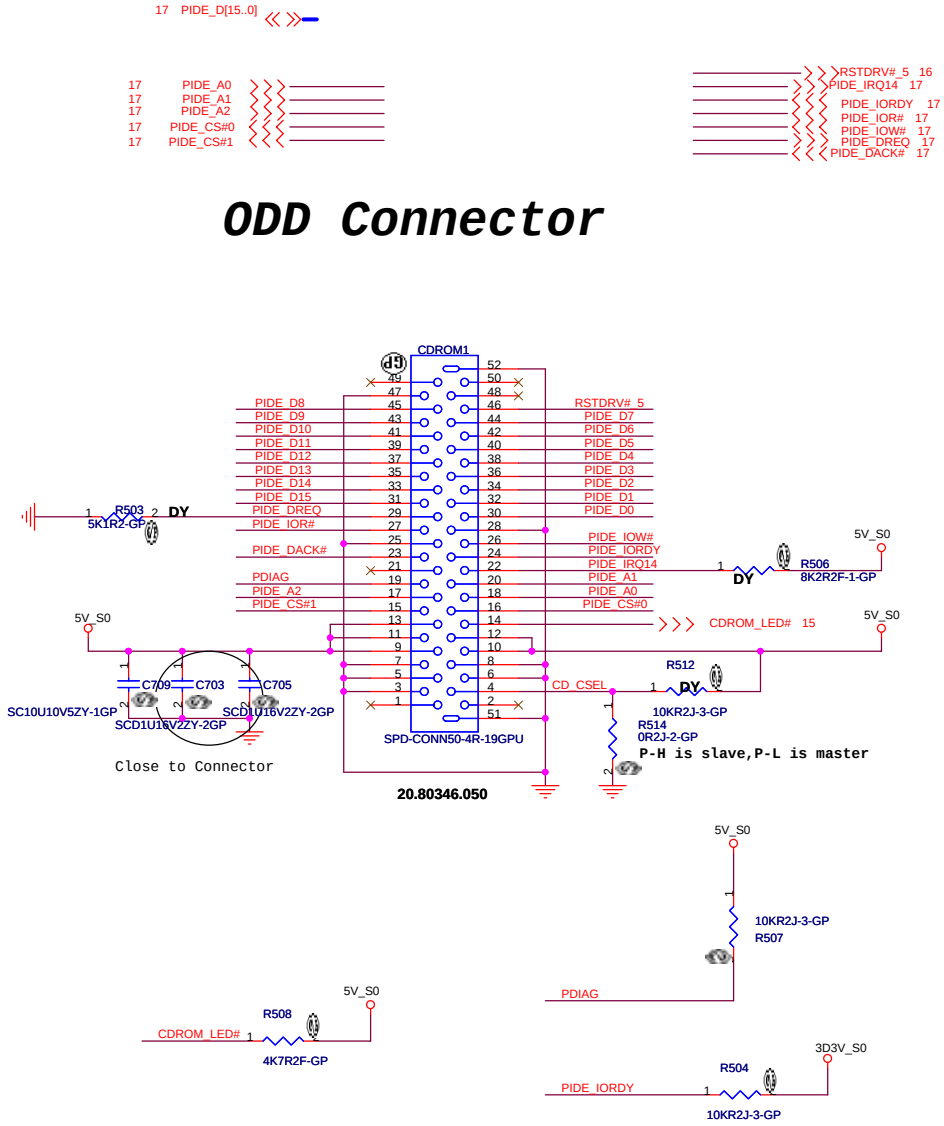
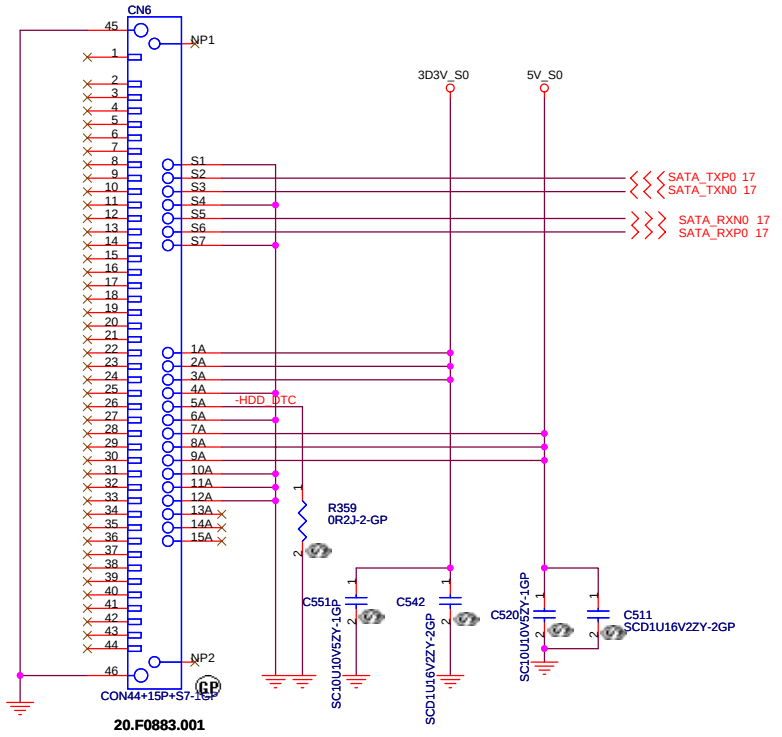
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Debug (Gold Finger)***	
Size A3	Document Number ***A-NOTE2.0-AMD***	Rev **SA**
Date: Tuesday, September 26, 2006	Sheet 33 of 55	

ODD Connector



SATA HD Connector



<Core Design>

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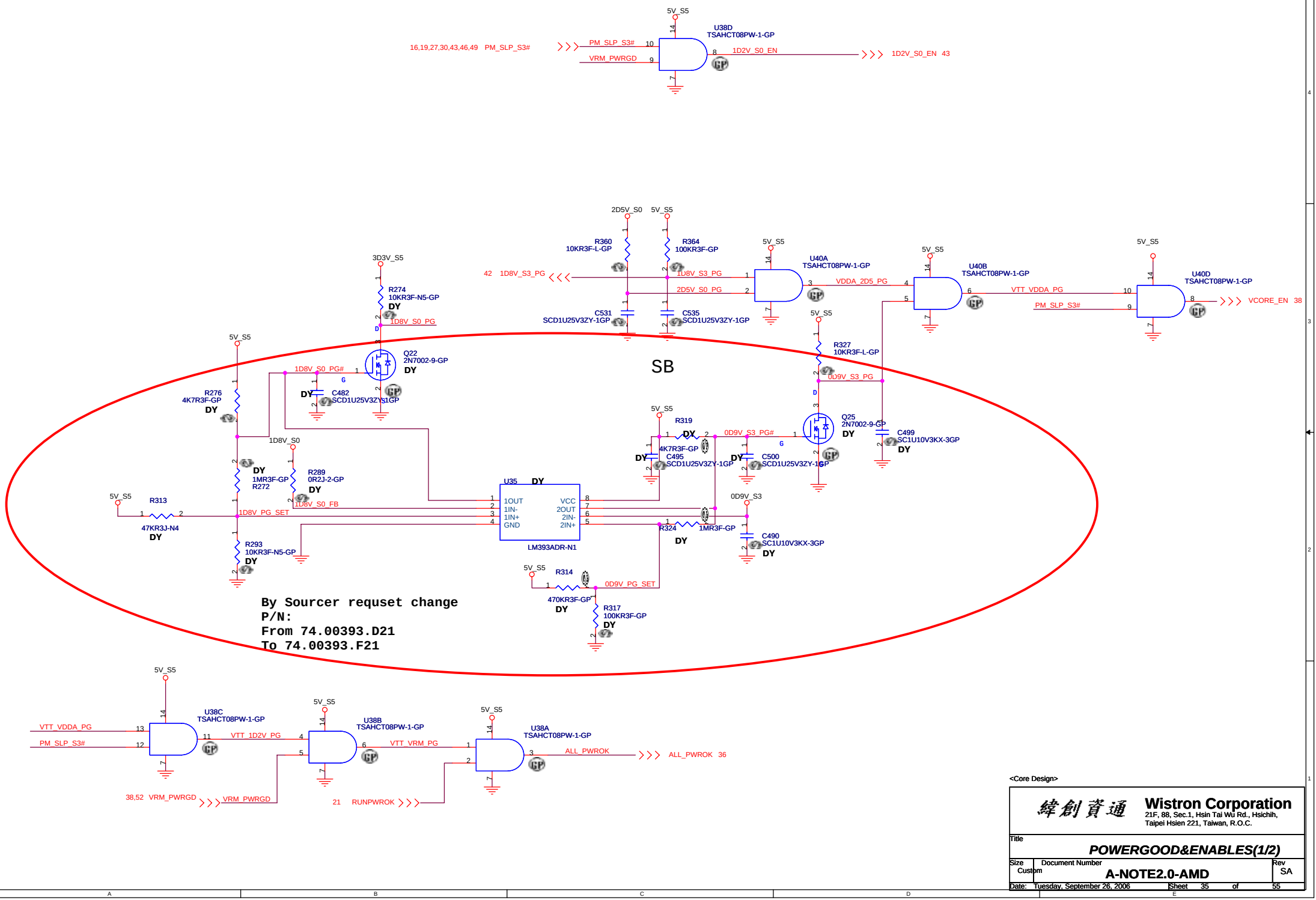
Title	HDD/CDROM CONN	
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 34 of 55	



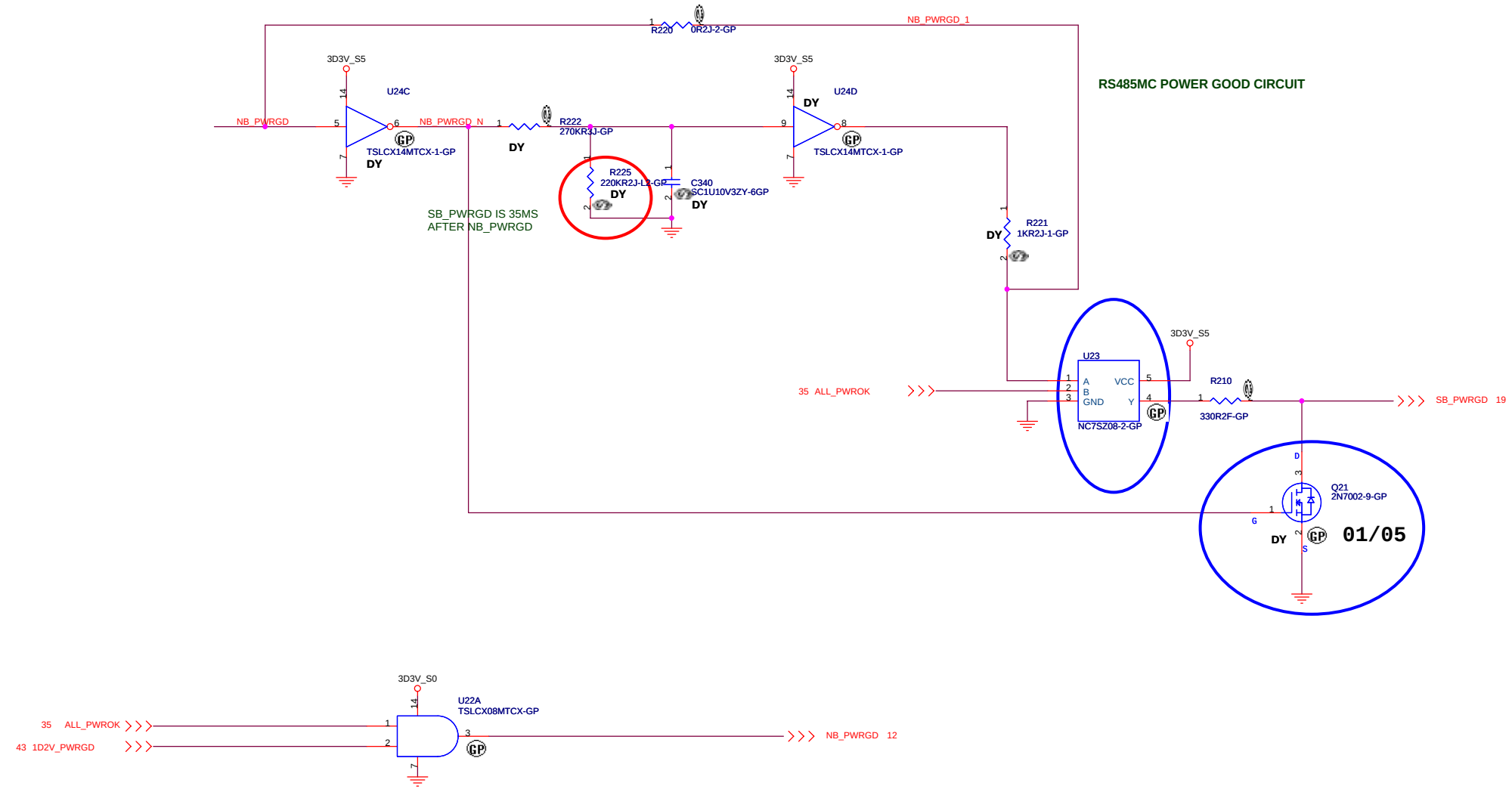
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWERGOOD&ENABLES(1/2)***

Size	Document Number	Rev
Custom	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 35 of 55



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 36 of 55

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal (I)
Input Power VCC(I) VCC(I)

Output Signal (O)
Output Power VCC(O)

AD_IN
AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Input Power
DCIN (I)

AD+

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

Output Power
VCC (O)
VCC (O)

AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
DCBATOUT
5V_S5
VCC(I)
VCC(I)

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

1D2V (6.5A)

ISL6268_VGA_CORE

VGA_CORE_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

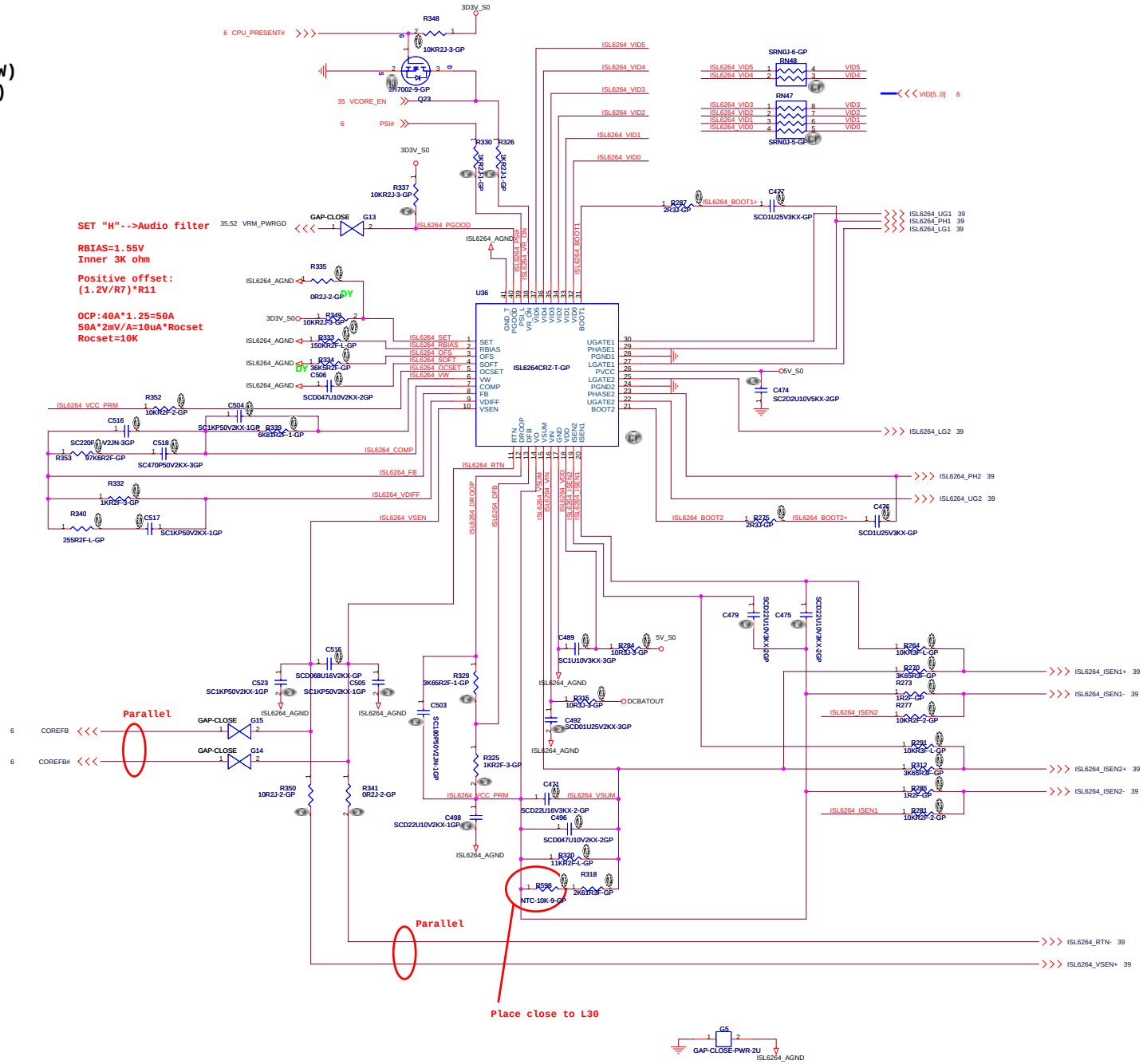
Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 37 of 55

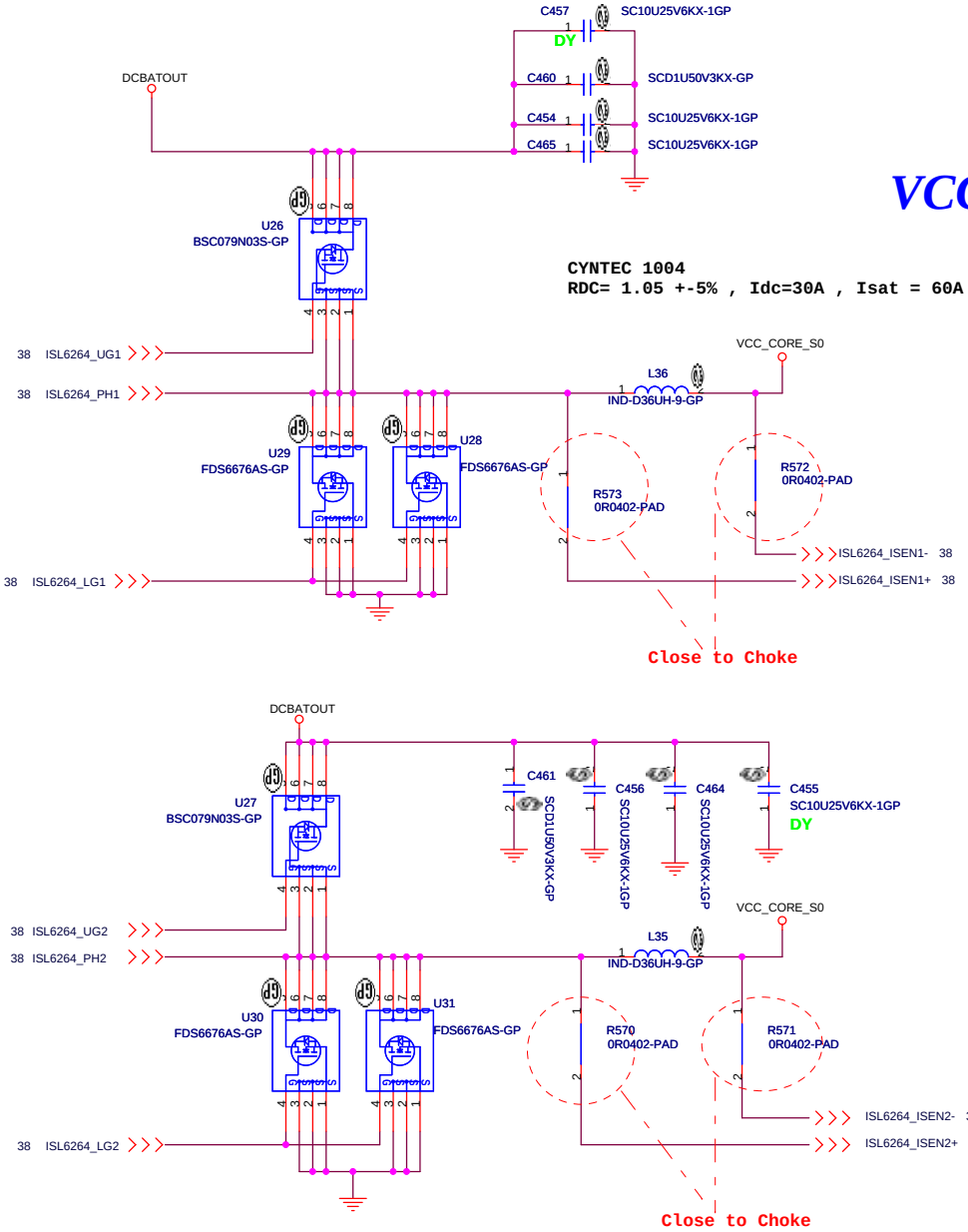
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

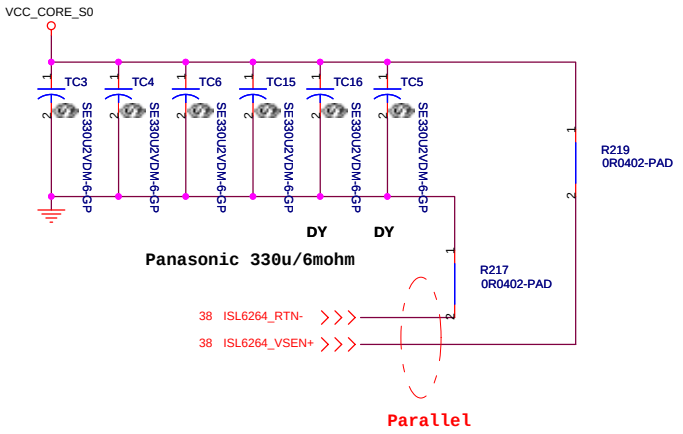
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



VCC_CORE_S0



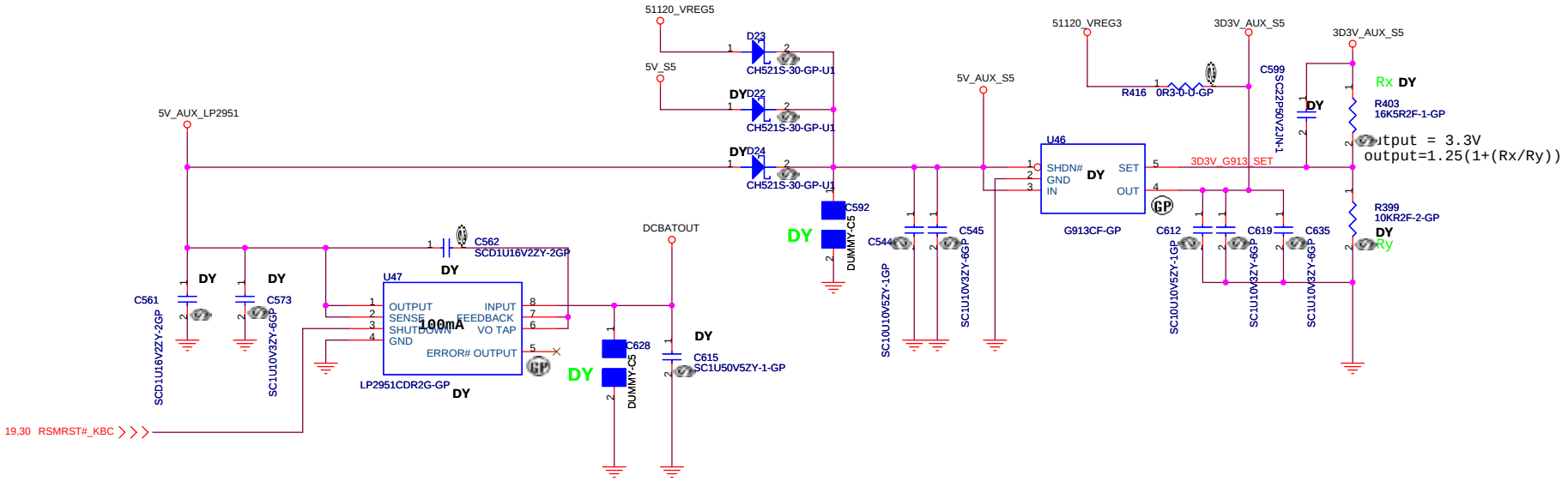


<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU Vcore Power_2		
Size: A3	Document Number: A-NOTE2.0-AMD	Rev: SA
Date: Tuesday, September 26, 2006	Sheet 39 of 55	

Aux Power

3D3V_AUX_S5



<Core Design>

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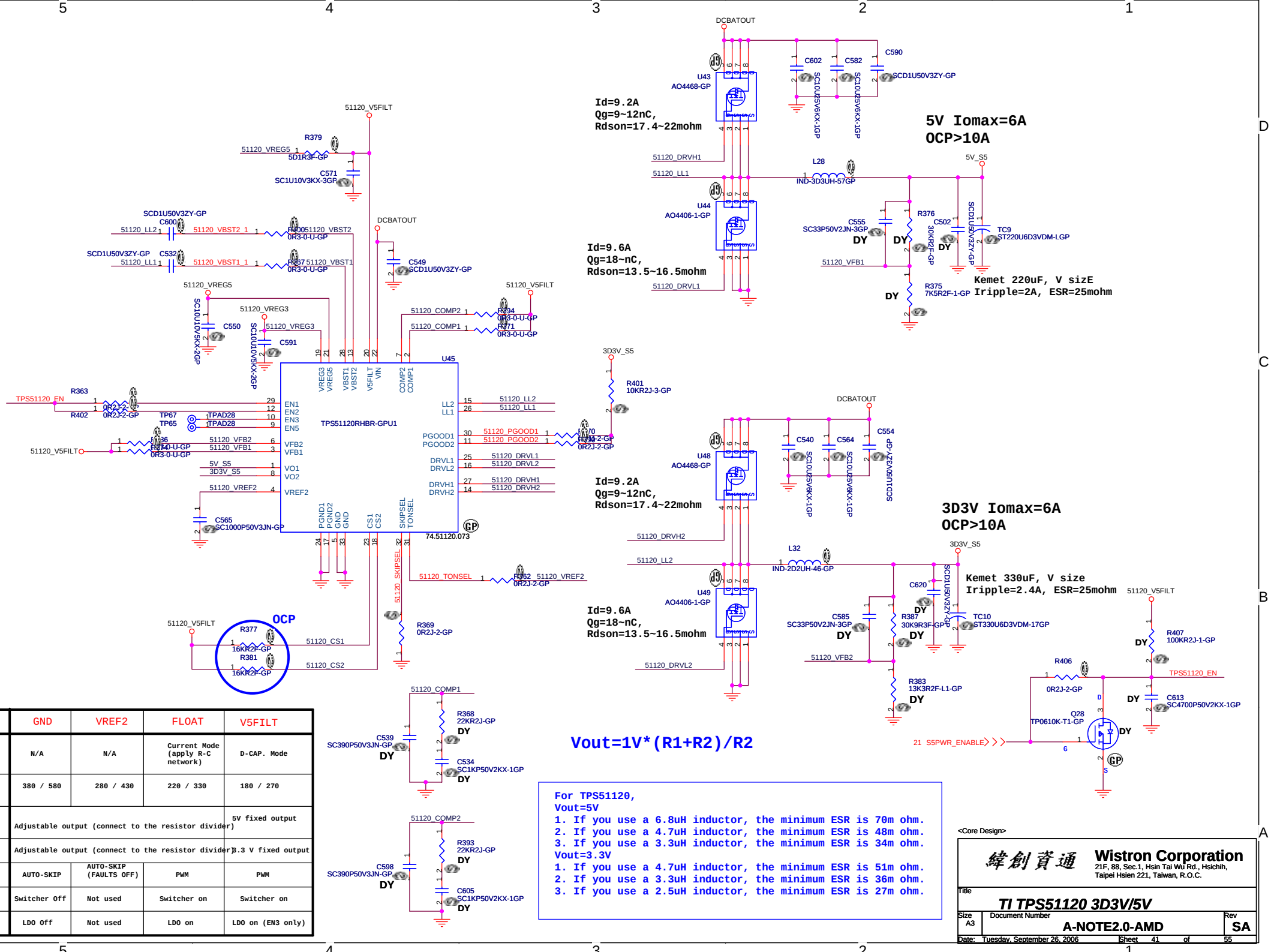
Title	3D3V/ 5V_AUX	
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 40 of 55	



Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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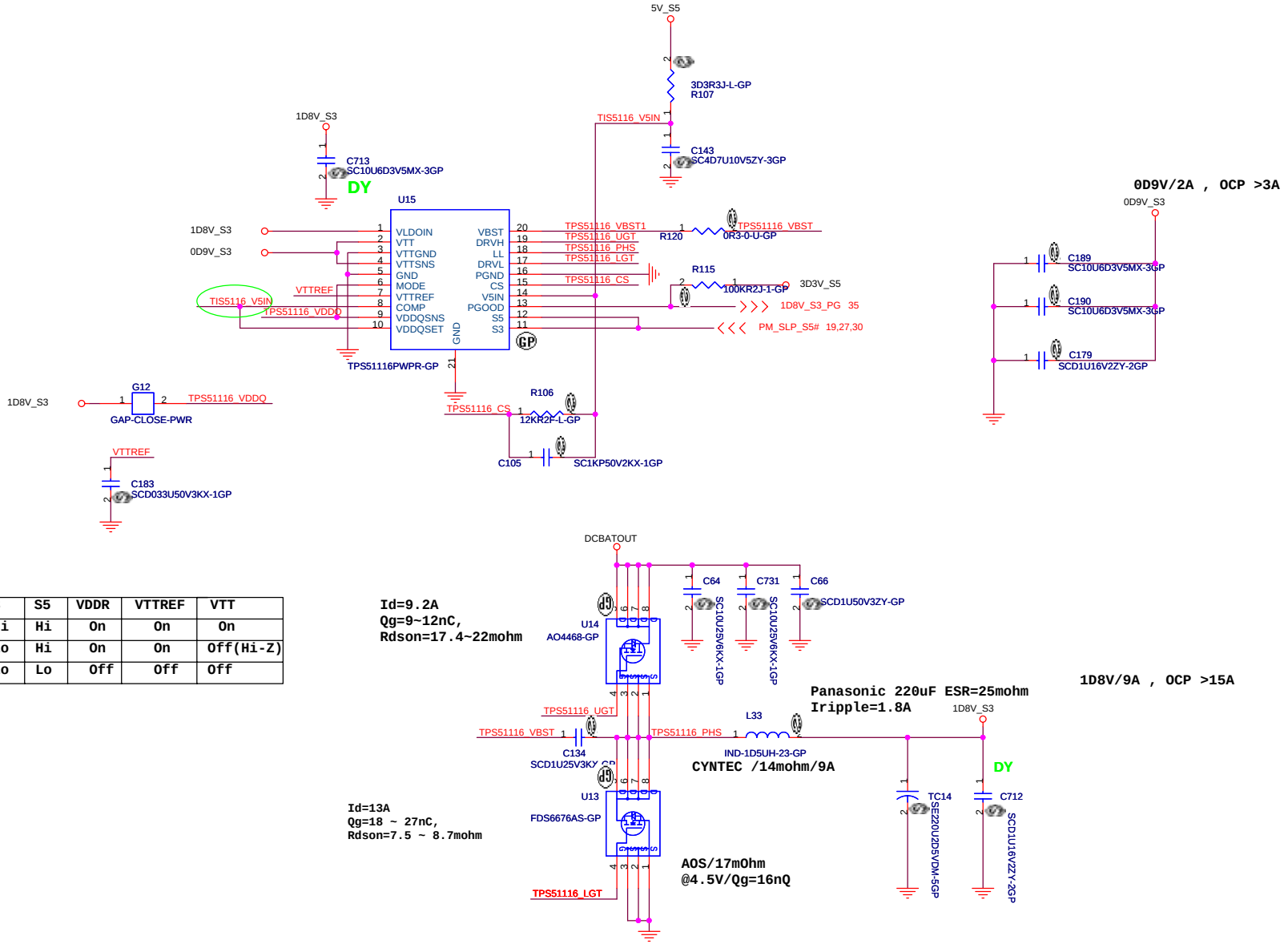
Title: TI TPS51120 3D3V/5V

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 41 of 55

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

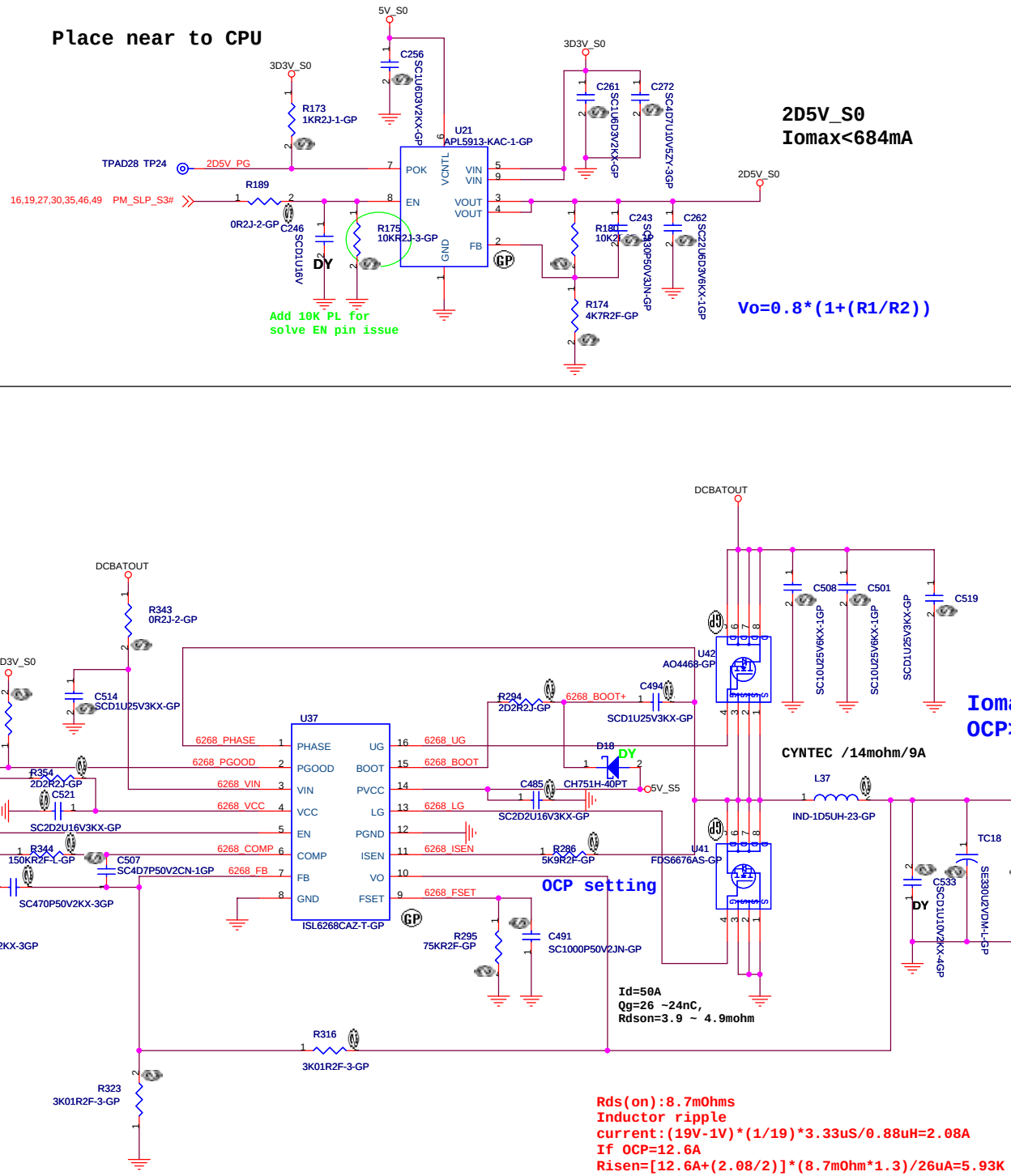
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI TPS51116 1D8V / 0D9V

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 42 of 55



<Core Design>

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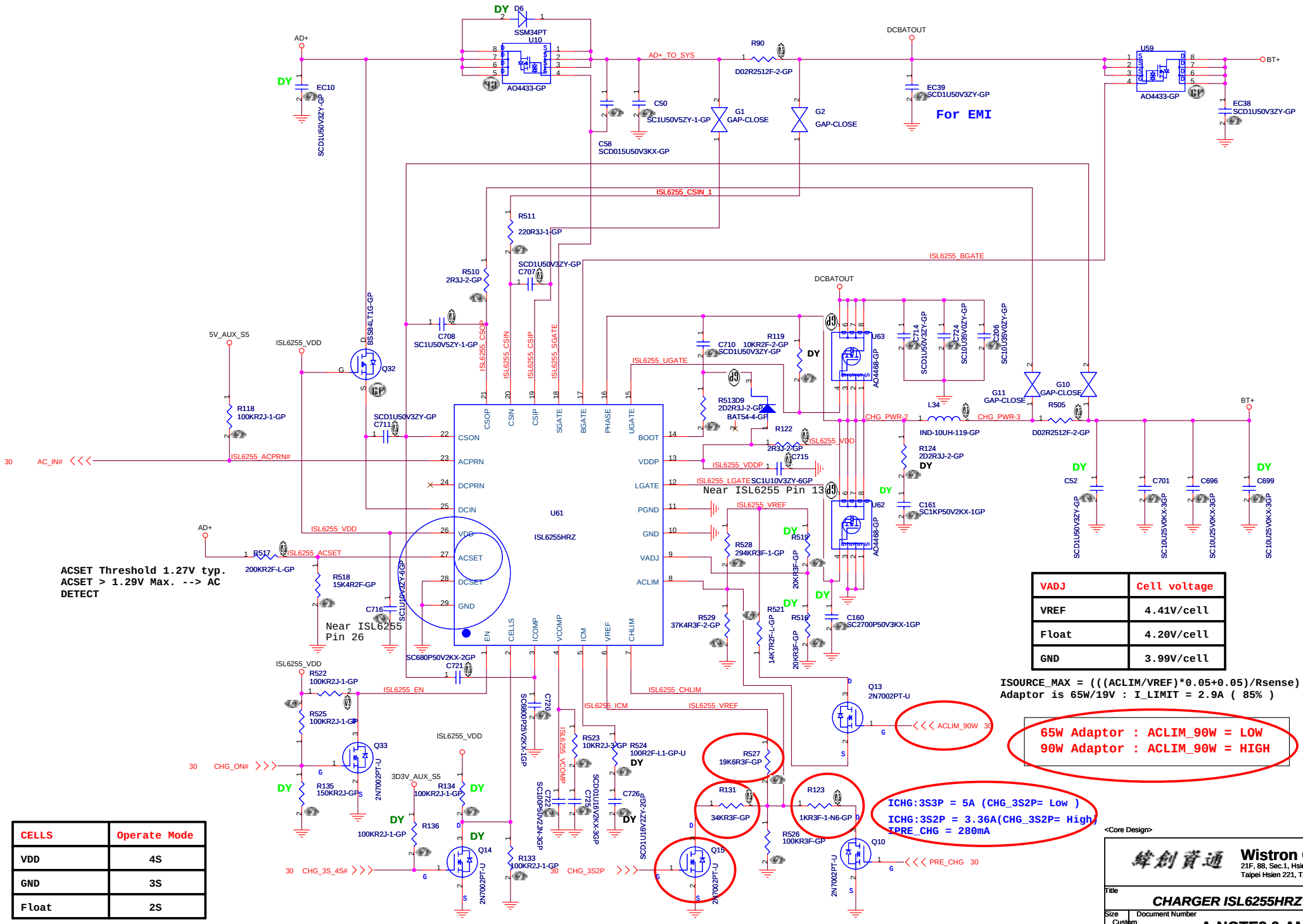
Title: ISL6268 1D2V

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 43 of 55



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

<Core Design>

Wistron Corporation
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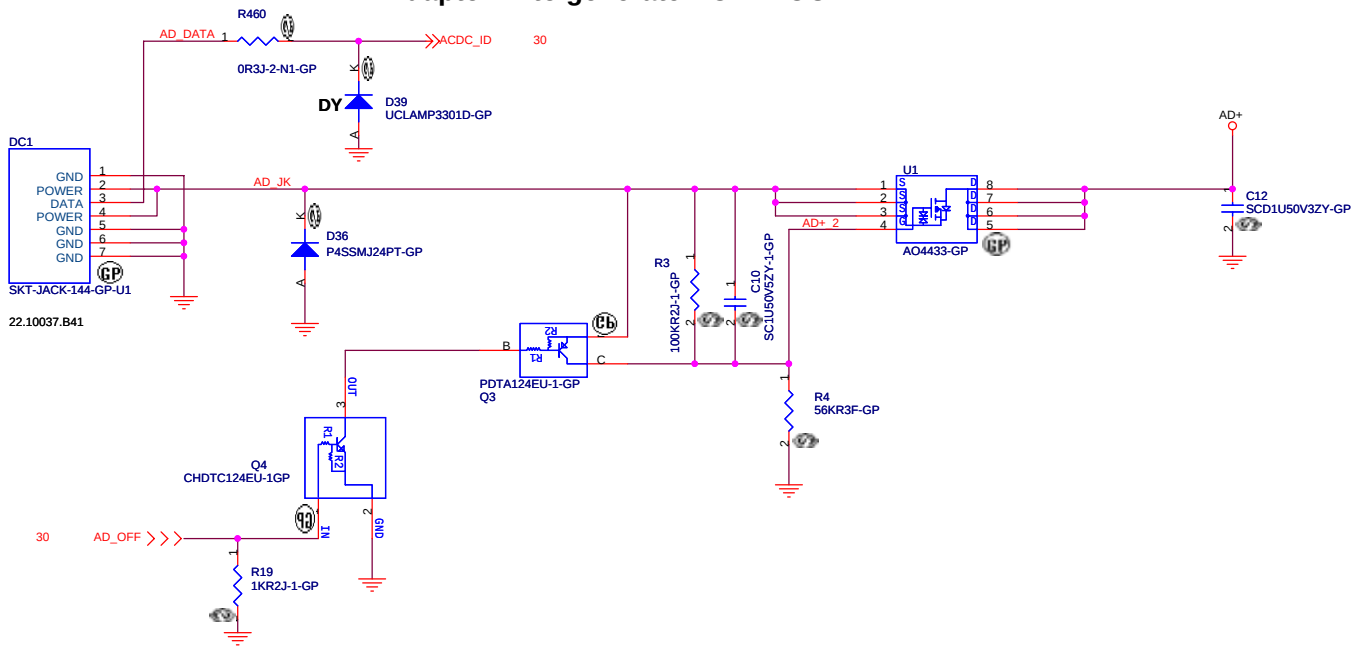
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6255HRZ

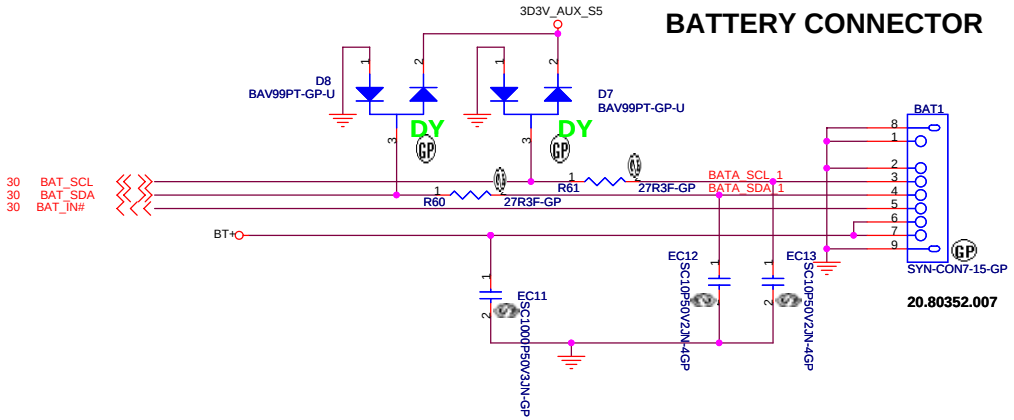
Size: Custom | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 44 of 55

Adaptor in to generate DCBATOUT



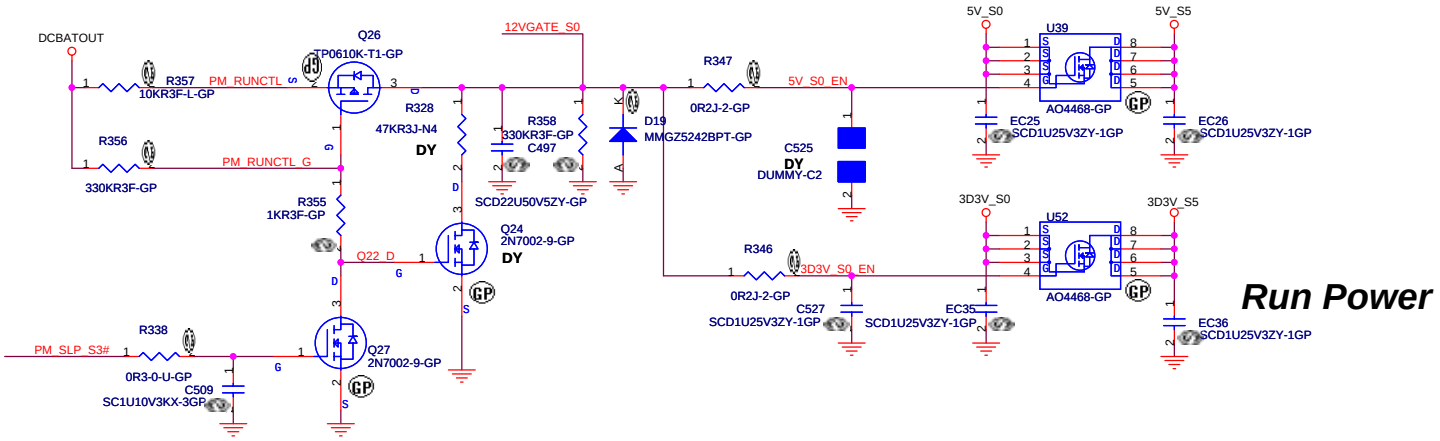
BATTERY CONNECTOR



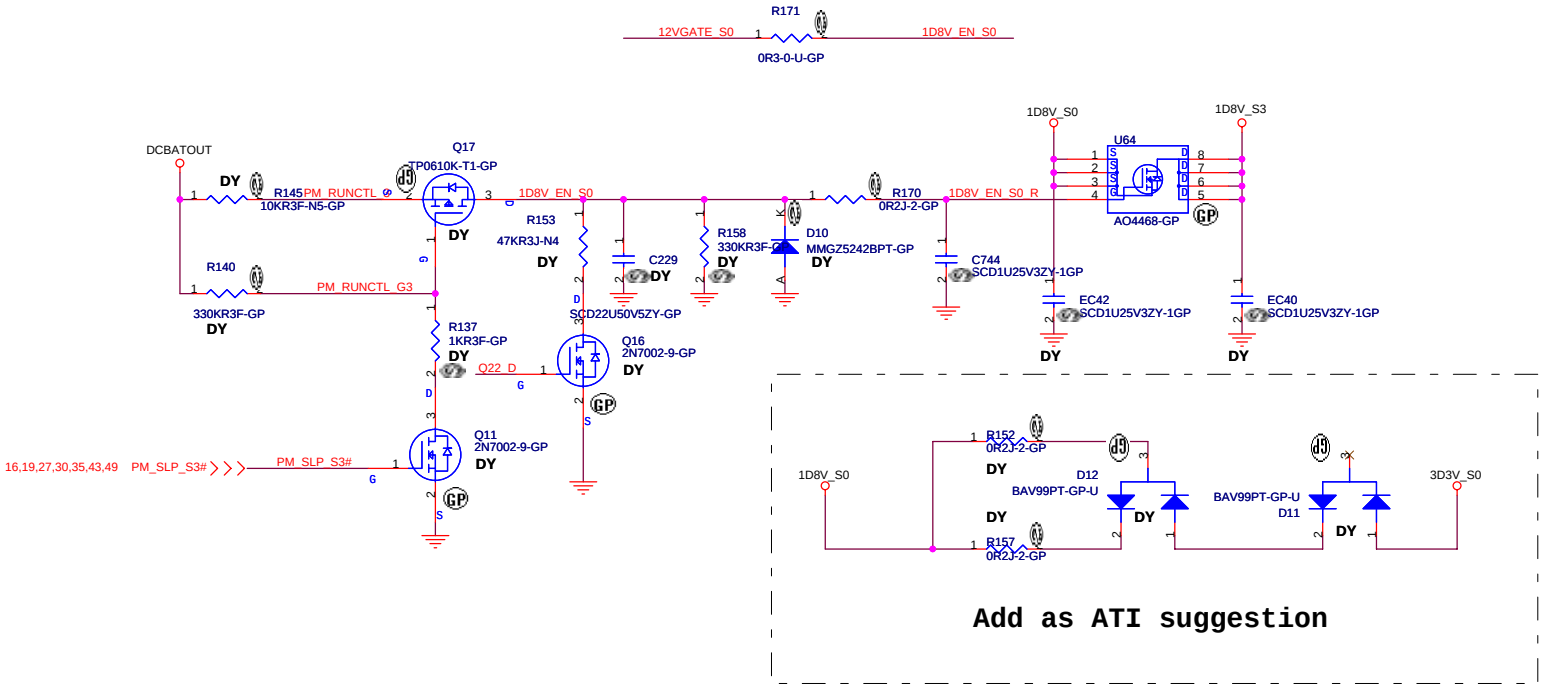
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BAT CONN***	
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 45 of 55	



Run Power



Add as ATI suggestion

Power On Logic

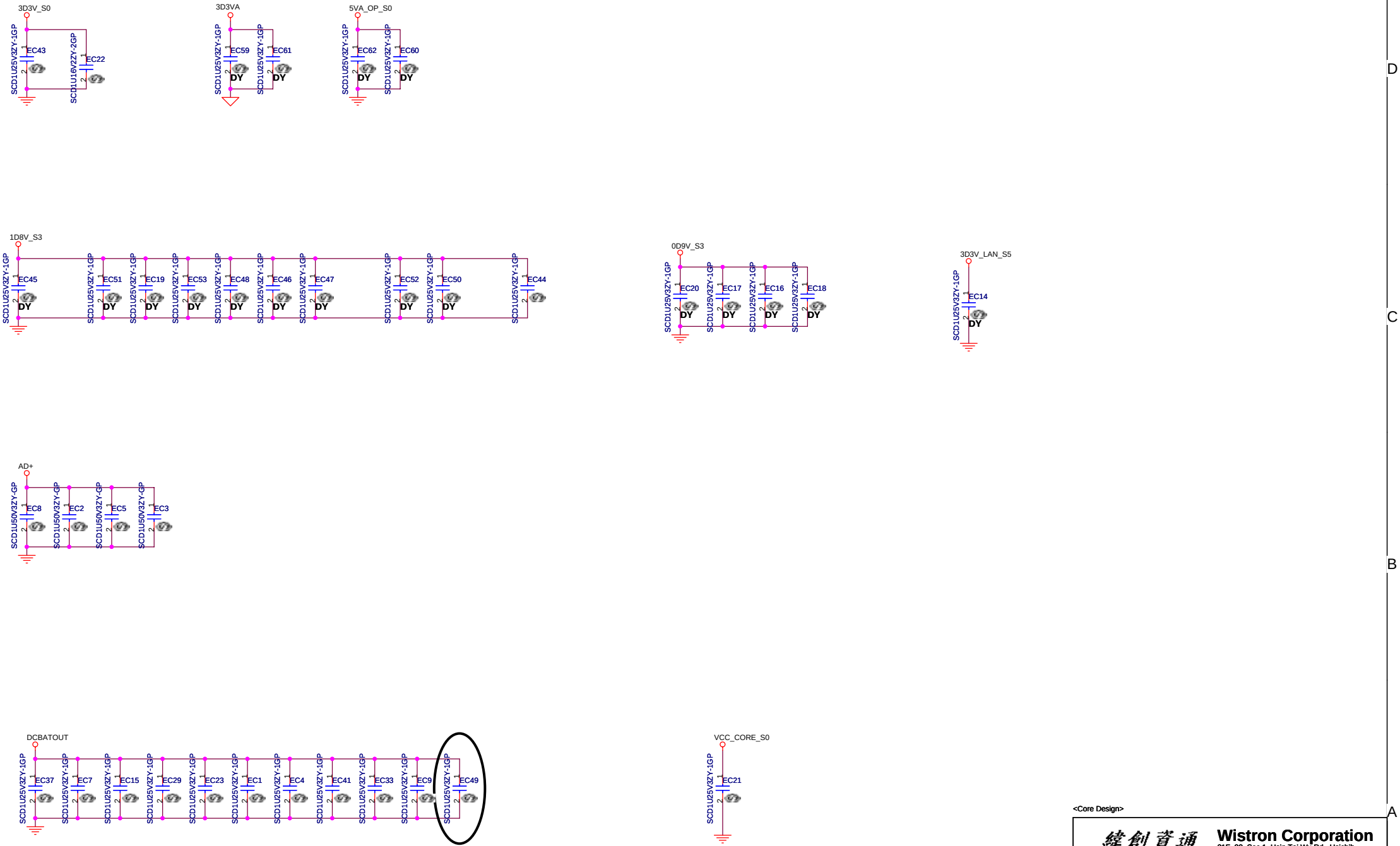
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWR CTL LOGIC / PWR PLANE

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 46 of 55



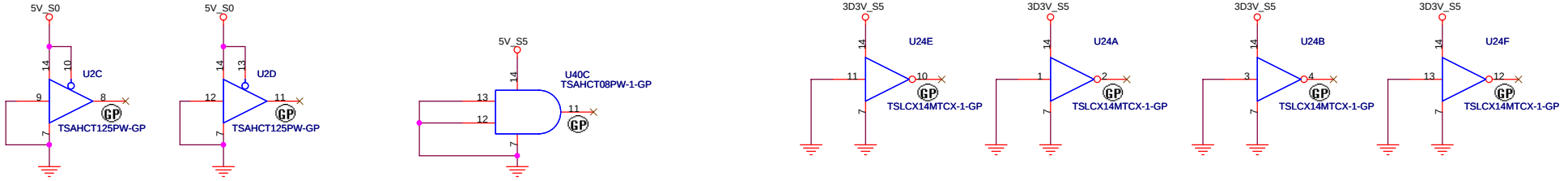
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai WU Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI COMPONENTS**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 47 of 55



34.4T003.001 x 2

HOLE1 HTE8BE8R28-D-4
HOLE2 HOLE295X354R110-S

34.4T002.001 x 1

HOLE19 HOLET217B79R71

34.41Q08.011 x 3

HOLE4 HTE7BE7R28-D-33
HOLE3 HOLE315R110
HOLE5 HTE8BE8R28-D-65
HOLE20 HOLET217B79R71
HOLE21 HOLE315R102
HOLE6 HOLE354X354R110-S1
HOLE23 HOLE315R102
HOLE24 HOLE315R102
HOLE16 HOLE354X315R110-S8
HOLE7 HOLE315R110
HOLE8 HTE8BE8R28-D-65
HOLE9 HTE8BE8R28-D-65
HOLE12 HT217X185B197R118-S
HOLE11 HTE6BE6R28-L-37
HOLE18 HOLE354X315R110-S9
HOLE14 HT205X217B197R118-S
HOLE22 HOLE
HOLE10 HTE8BE8R24-D-413
HOLE25 HOLE276R94
HOLE26 HOLE276R94
HOLE27 HOLE276R94
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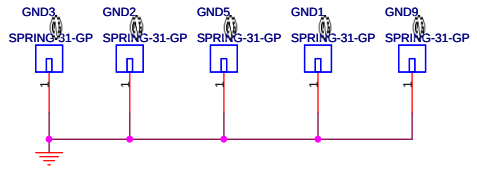
HOLE15 HT217X185B197R118-S
HOLE17 HOLE354X315R110-S10



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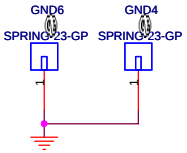

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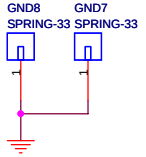

34.4B312.001 x 2

<Core Design>

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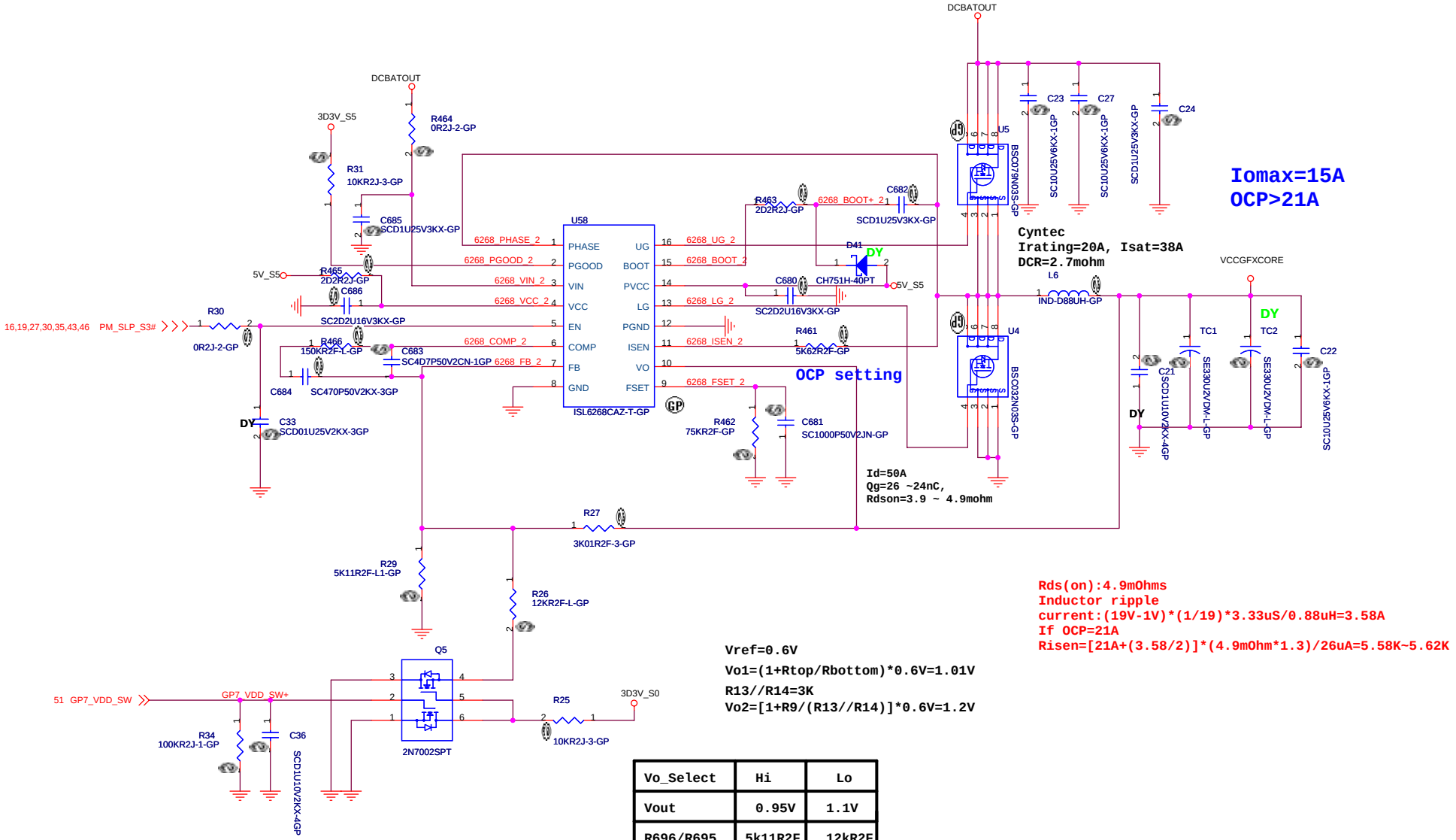
Title: ***MISC***

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 48 of 55



Vo_Select	Hi	Lo
Vout	0.95V	1.1V
R696/R695	5k11R2F	12kR2F

Vo_Select	Hi	Lo
Vout	0.95V	1.2V
R696/R695	5k11R2F	7k15R2F

<Core Design>

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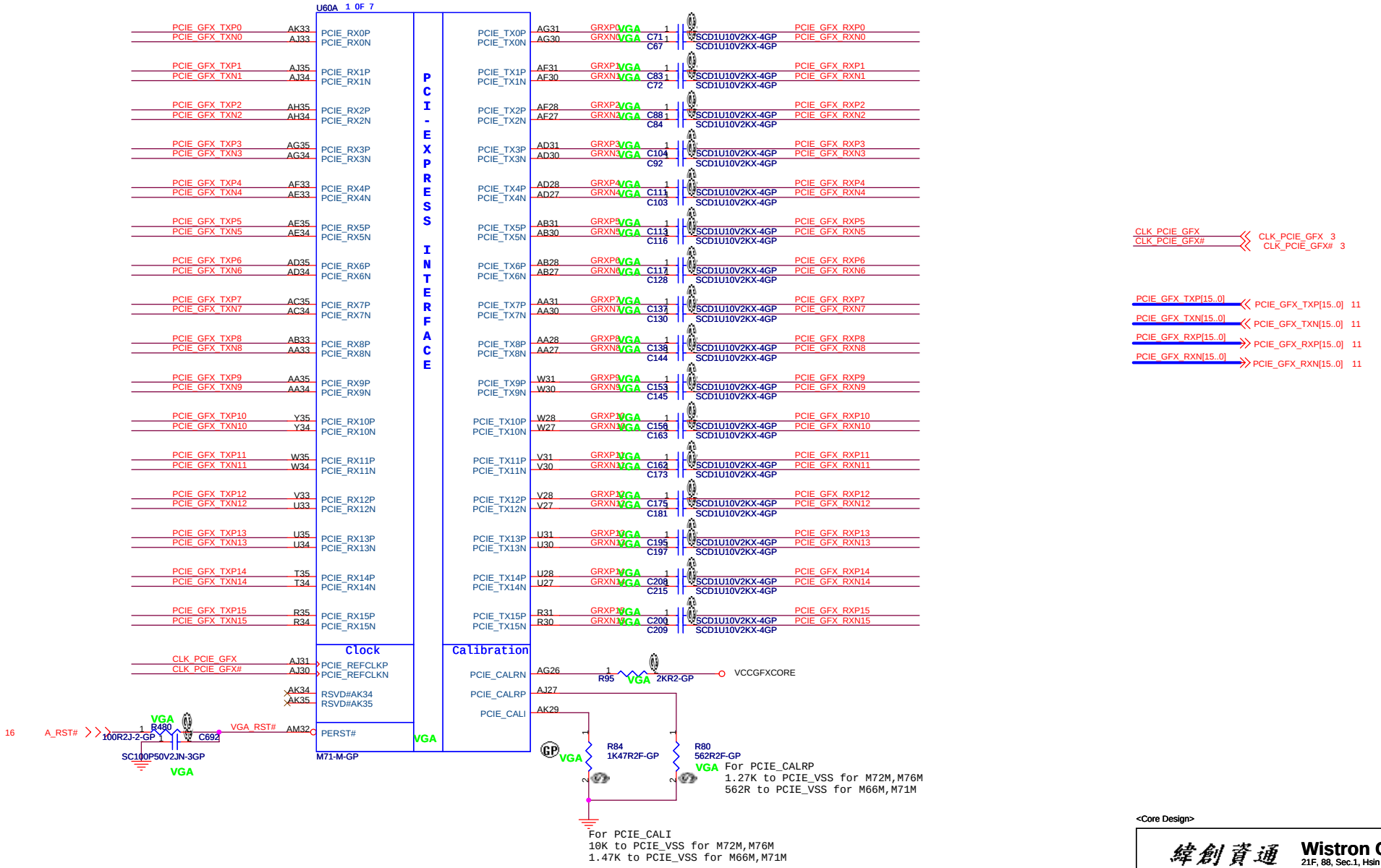
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 49 of 55



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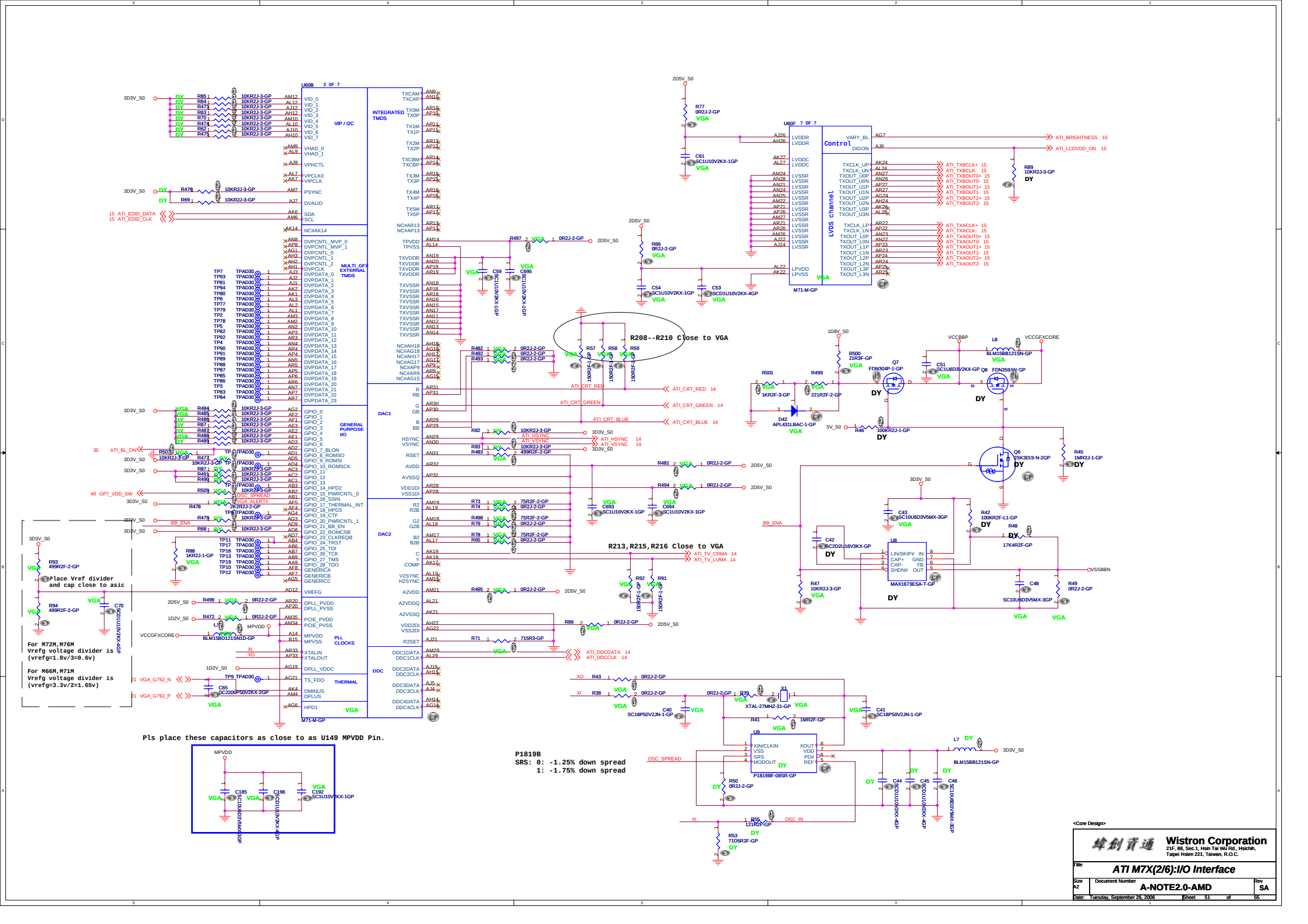
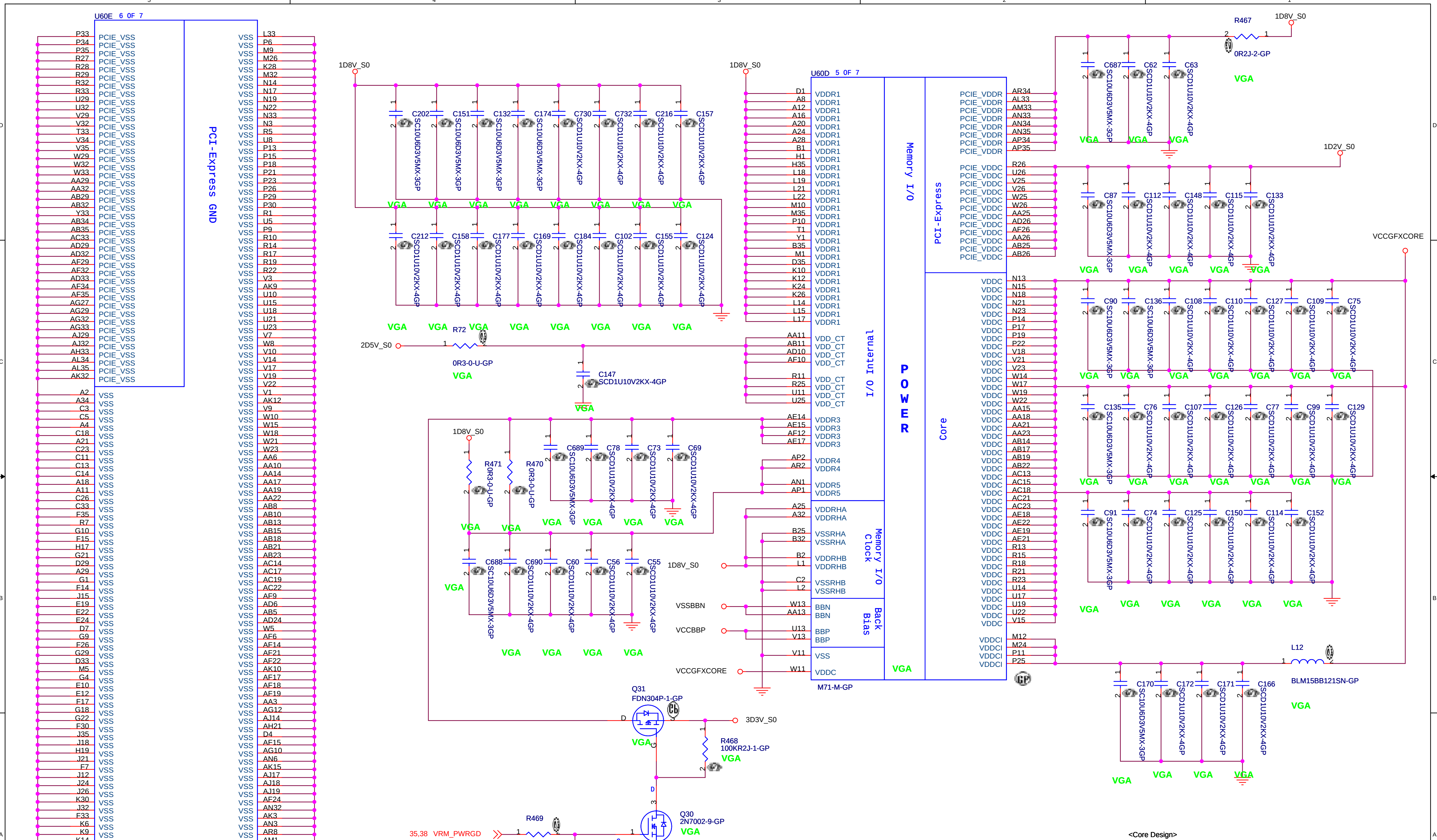
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M7X(1/6):PCIE Interface**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 50 of 55


U60B 2 0F 7
VIP / I2C
INTEGRATED TMDS
MULTI_GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
DAC1
DAC2
DDC
PLL CLOCKS
THERMAL
M71-M-GP
U60F 7 0F 7
Control
LVDS channel
M71-M-GP
R208--R210 Close to VGA
R213,R215,R216 Close to VGA
Place Vref divider and cap close to asic
For M72M,M76M
Vrefg voltage divider is
(vrefg=1.8v/3=0.6v)
For M66M,M71M
Vrefg voltage divider is
(vrefg=3.3v/2=1.65v)
Pls place these capacitors as close to as U149 MPVDD Pin.
P1819B
SRS: 0: -1.25% down spread
1: -1.75% down spread
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M7X(2/6):I/O Interface
Size A2
Document Number A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 51 of 55



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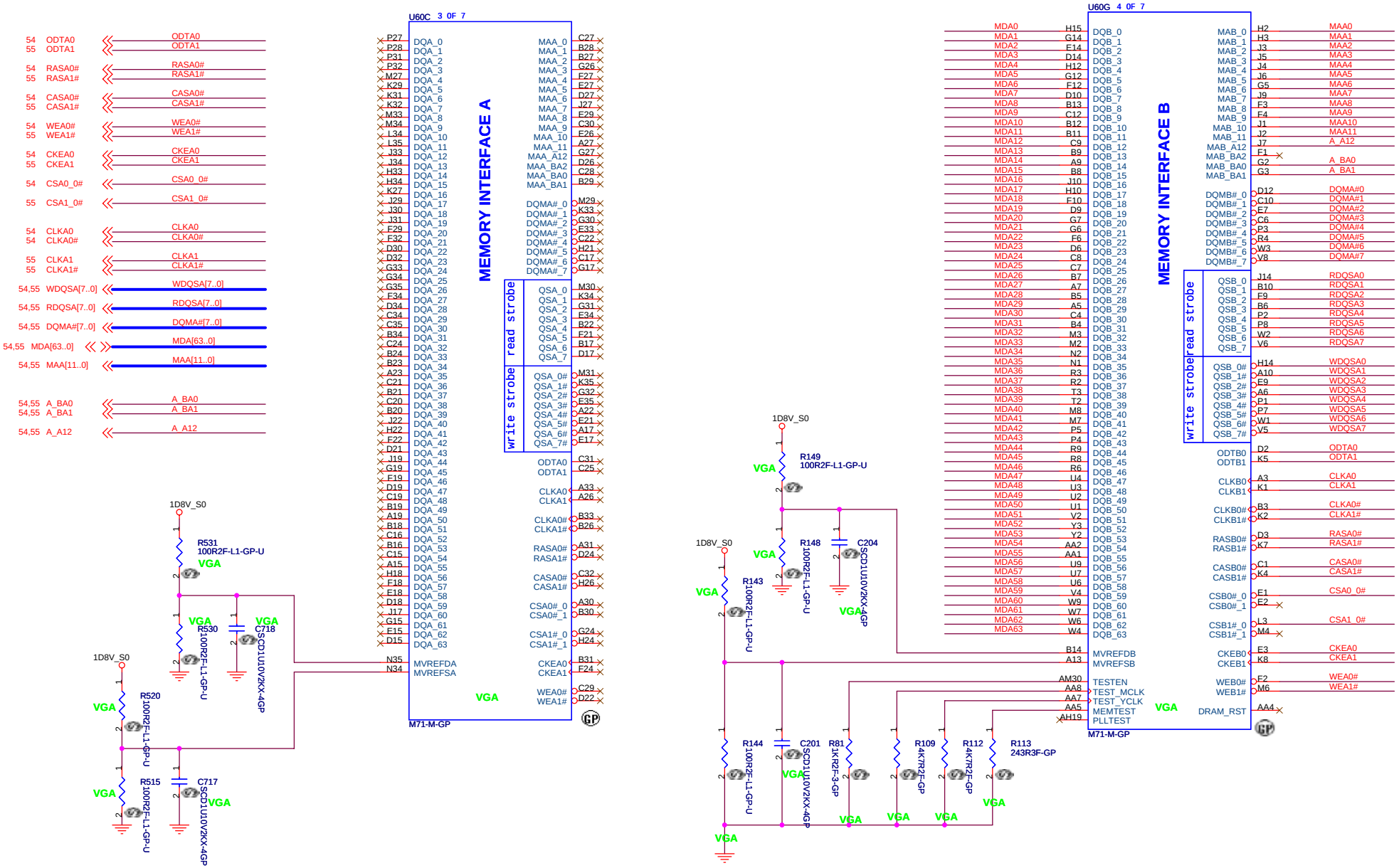
Title: ATI M7X(3/6):VCC/GND

Size	Document Number	Rev
Custom	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 52 of 55



<Core Design>

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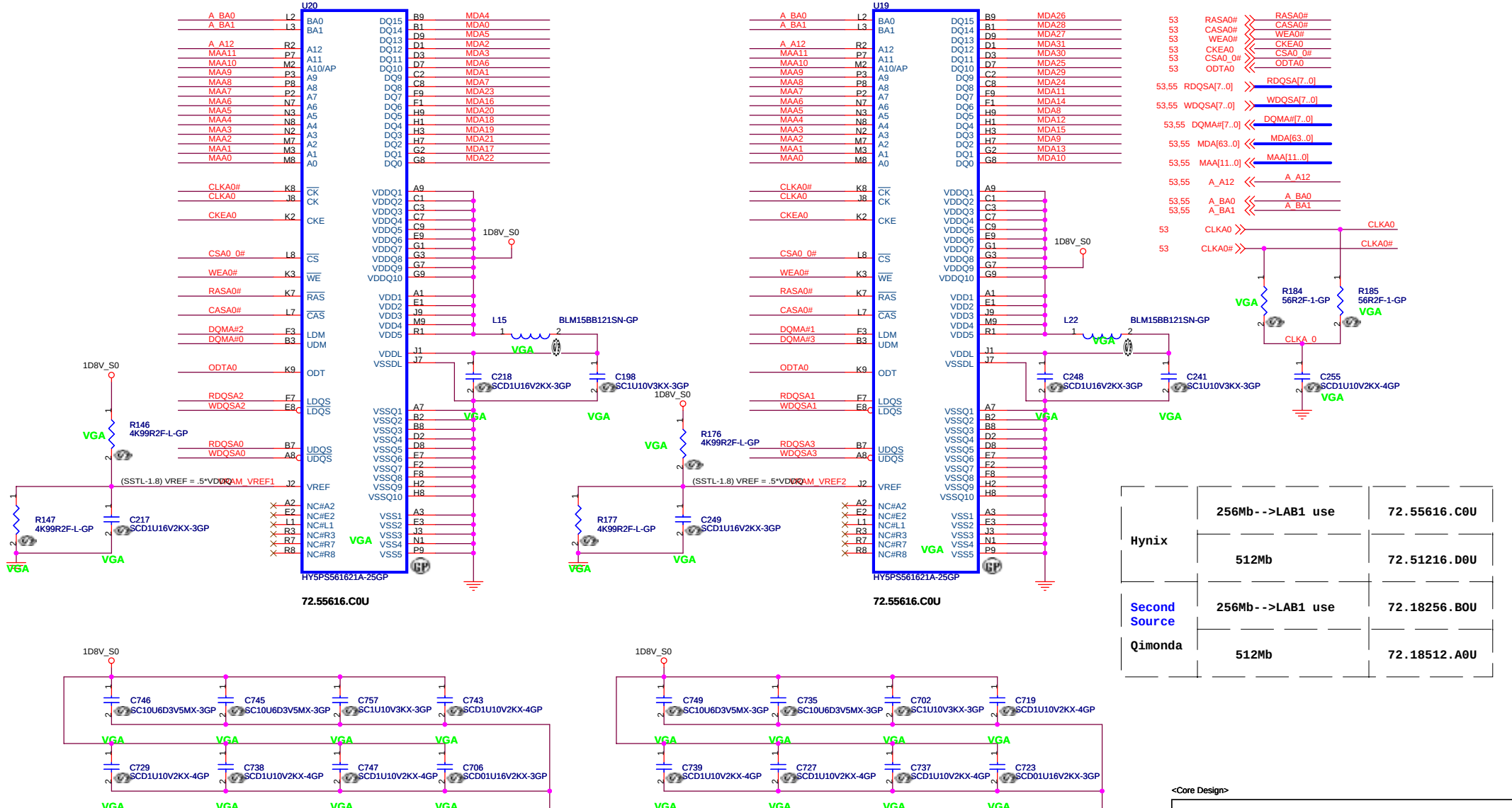
Title: **ATI M7X(4/6):Memory Interface**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 53 of 55

DDR2 BGA MEMORY



Hynix	256Mb-->LAB1 use	72.55616.C0U
	512Mb	72.51216.D0U
Second Source Qimonda	256Mb-->LAB1 use	72.18256.B0U
	512Mb	72.18512.A0U

<Core Design>

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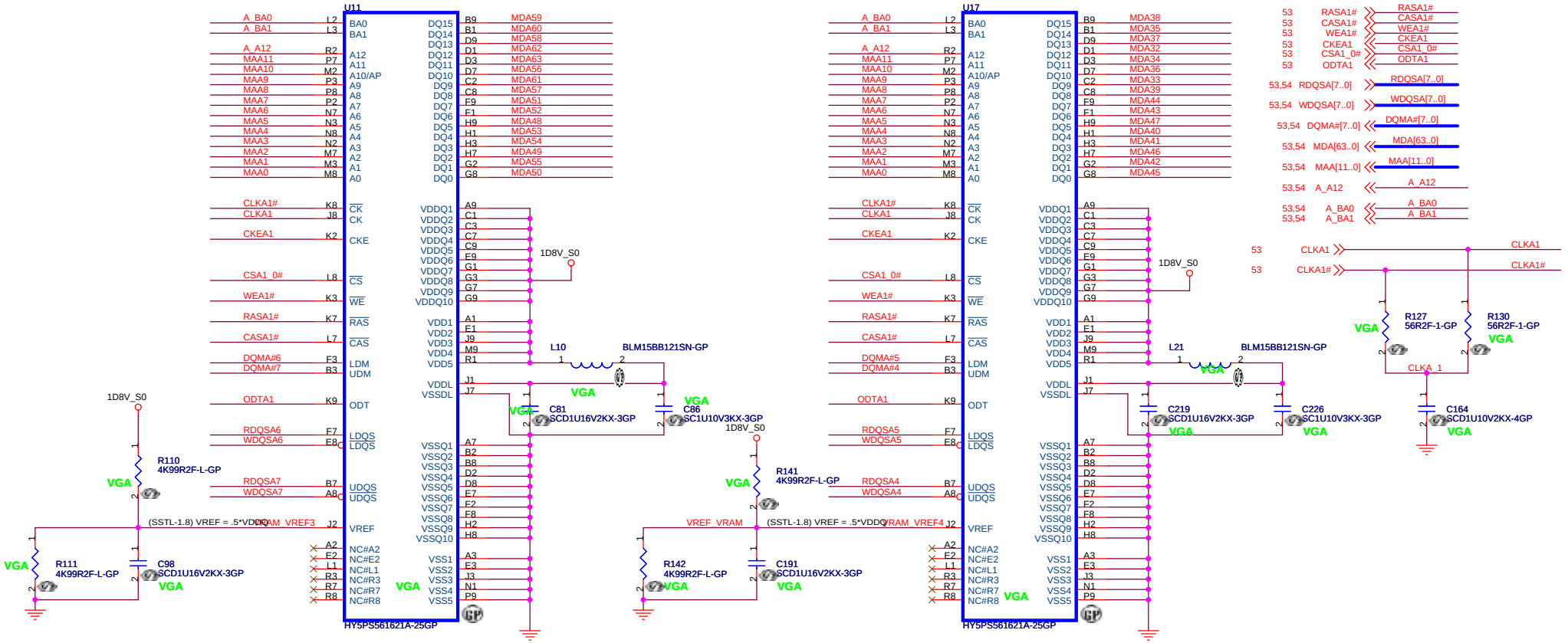
Title: ***VRAM***

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 54 of 55

DDR2 BGA MEMORY



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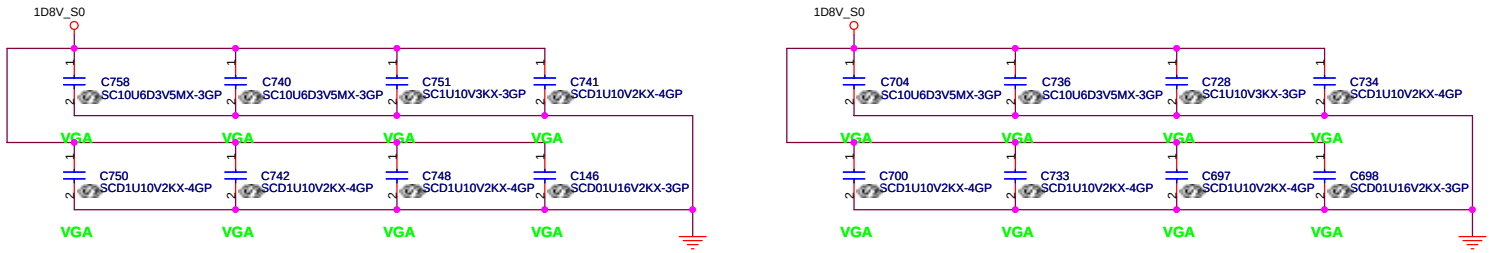

<Core Design>

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Title	***VRAM***	
Size A3	Document Number **A-NOTE2.0-AMD**	Rev **SA**
Date: Tuesday, September 26, 2006	Sheet 55 of 55	