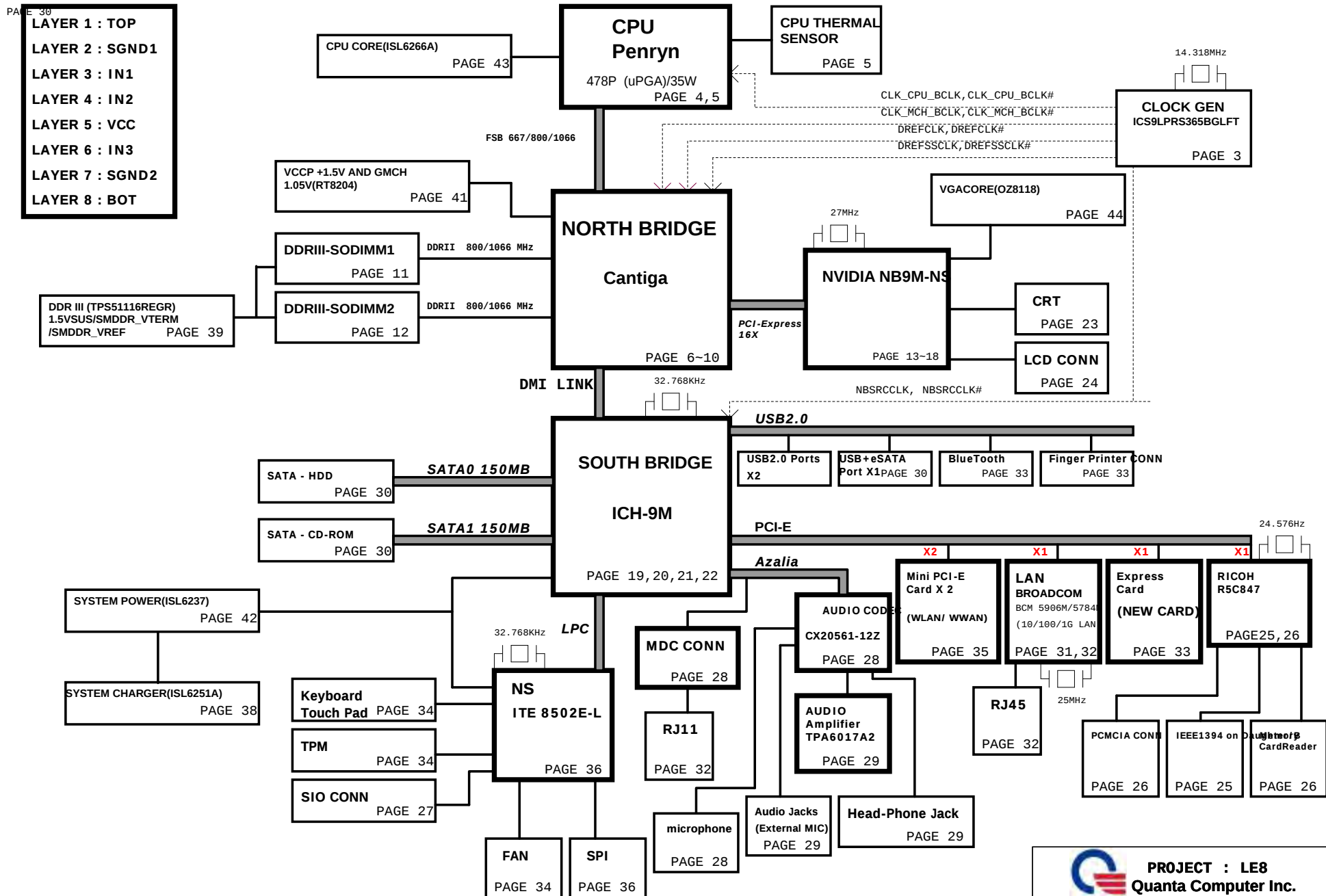


PCB STACK UP 8L

LE9E(LE8) BLOCK DIAGRAM

01

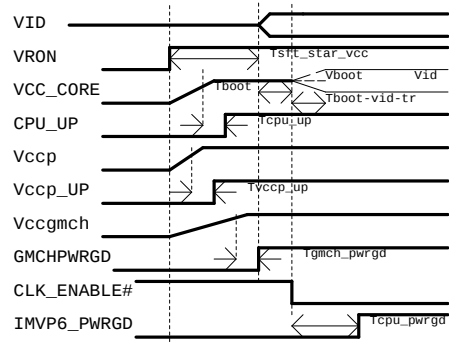


Board Stack up Description

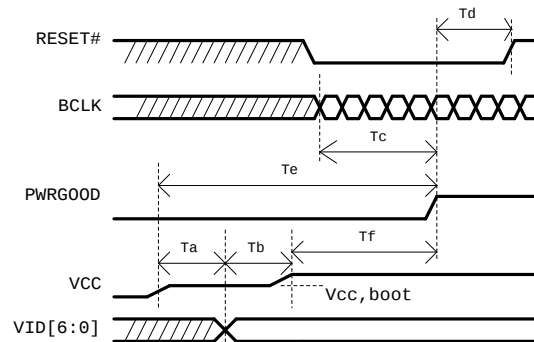
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



MEROM Power-up Timing Specifications



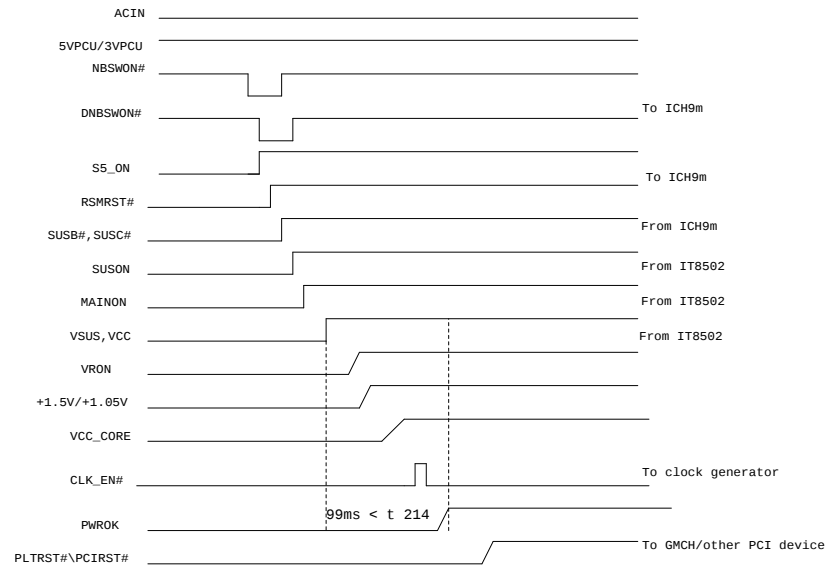
+1.05V

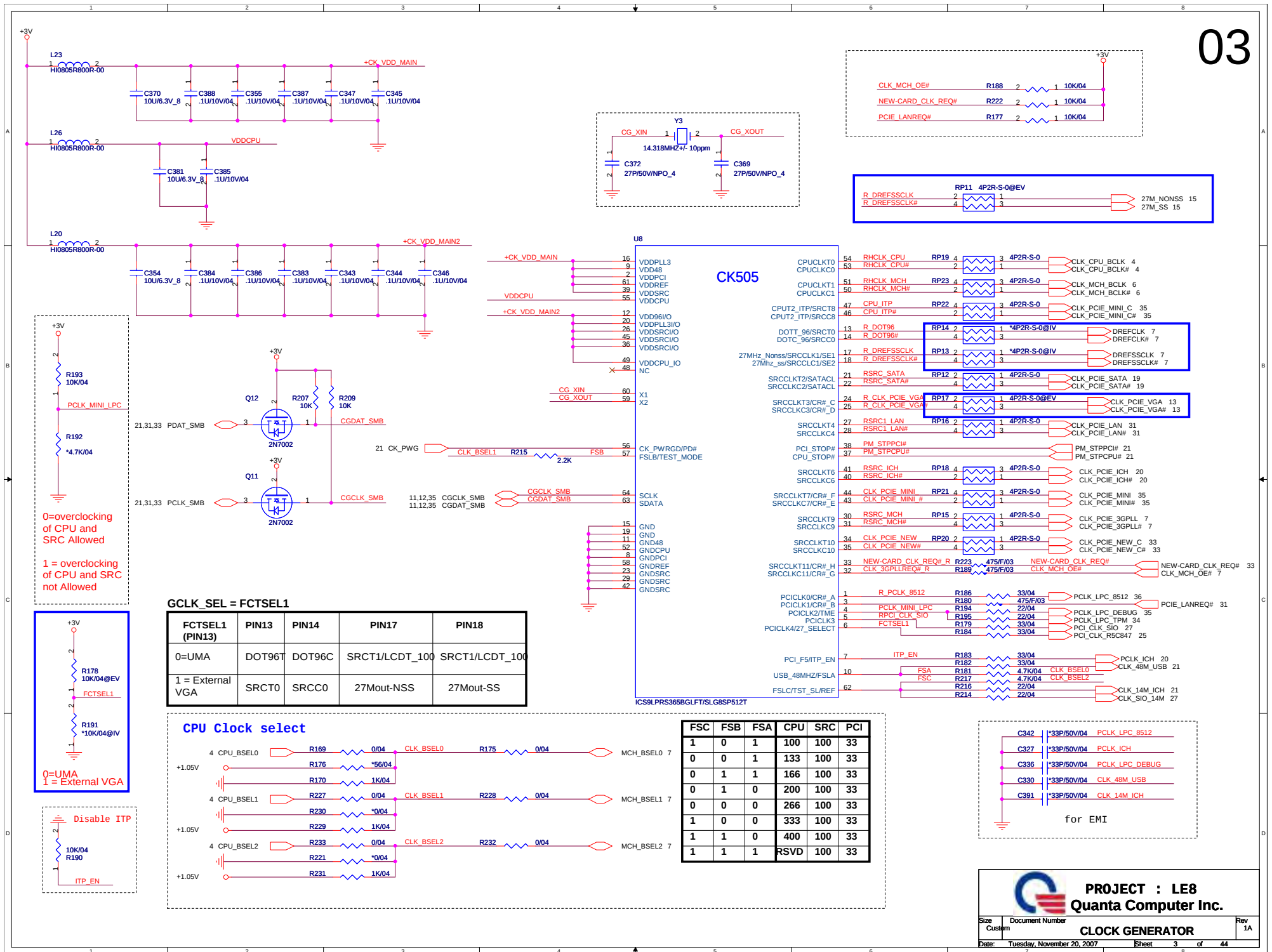
Ta=VCC and VCCP assertion to VID[6:0] valid
Tb=VID[6:0] stable to VCC valid
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot valid to PWRGOOD assertion time

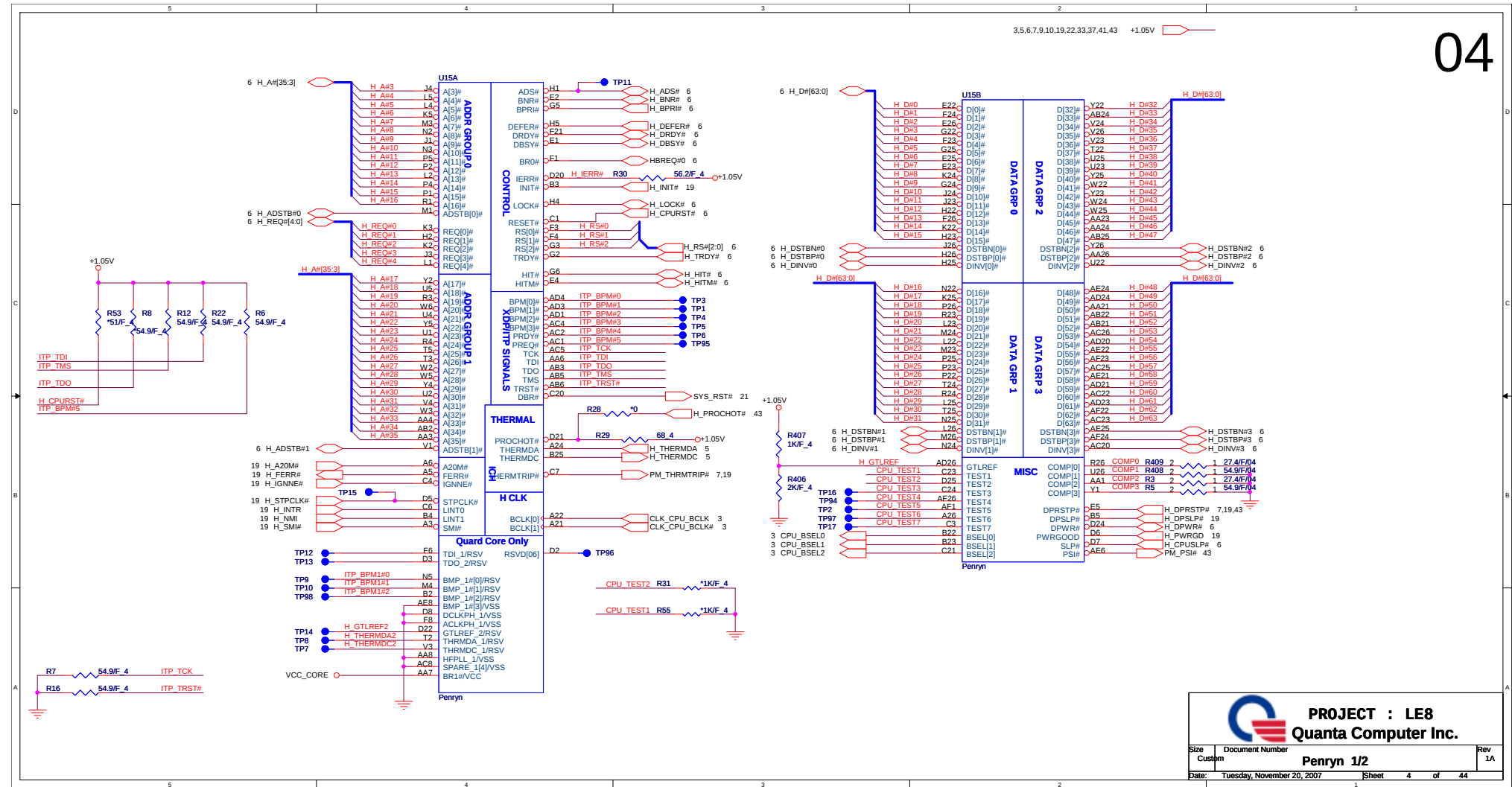
Voltage Rails

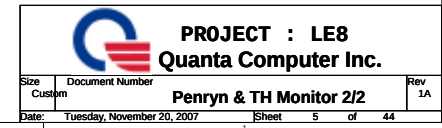
Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.5VSUS	X	X			SUSON
SMDRR_VTERM/+3V/+5V/+15V/+1.8V	X				MAINON
+VGACORE/+VGA1.1V	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING









3.5,10,11,12,13,15,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44
+3V
9.10,11,12,33,37,39,44 1.5VSUS
3.4,5,6,9,10,19,22,33,37,41,43 1.05V_PEG
10 +1.05V_PEG

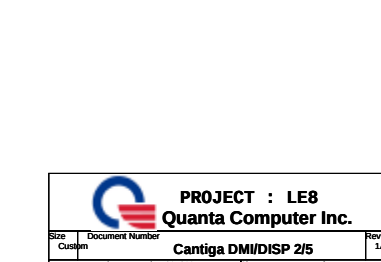
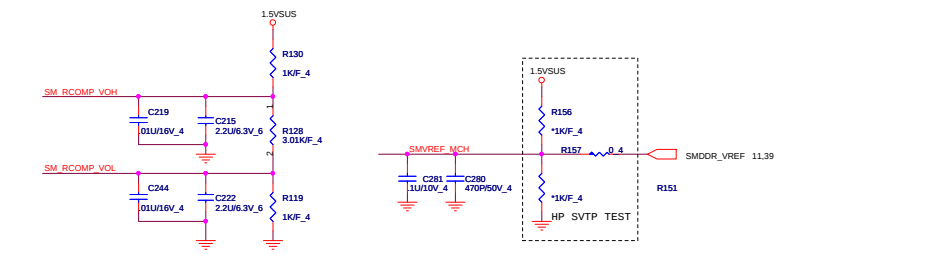
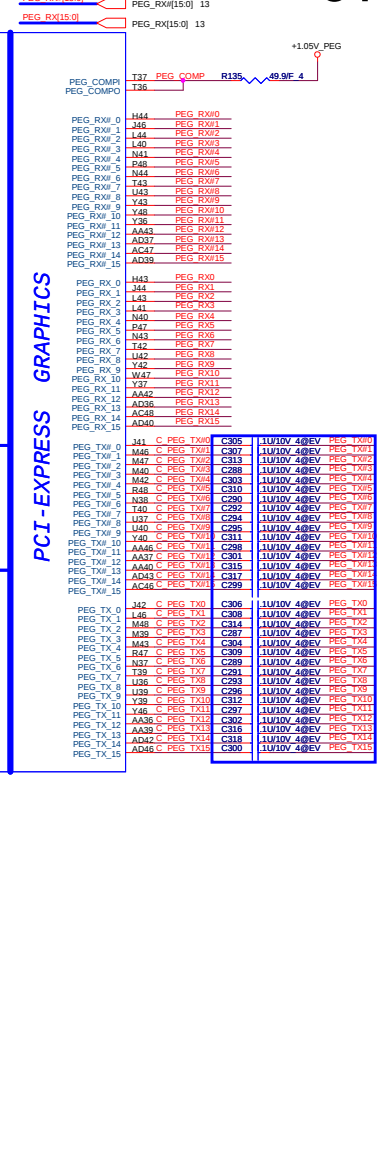
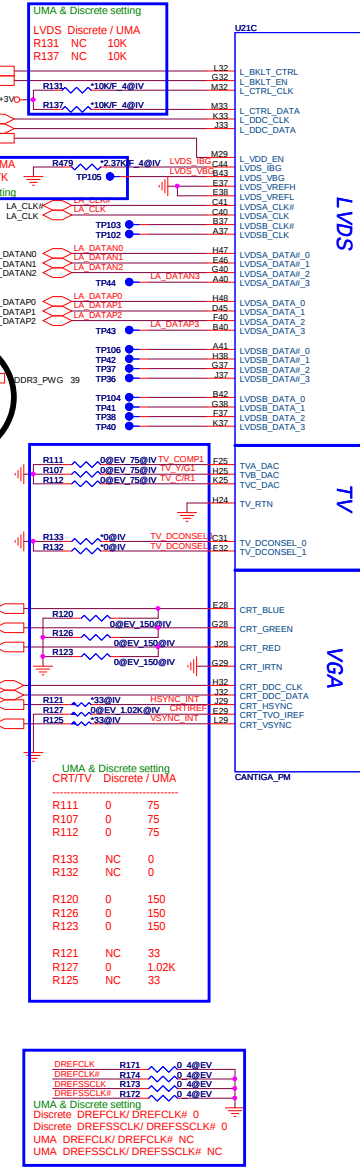
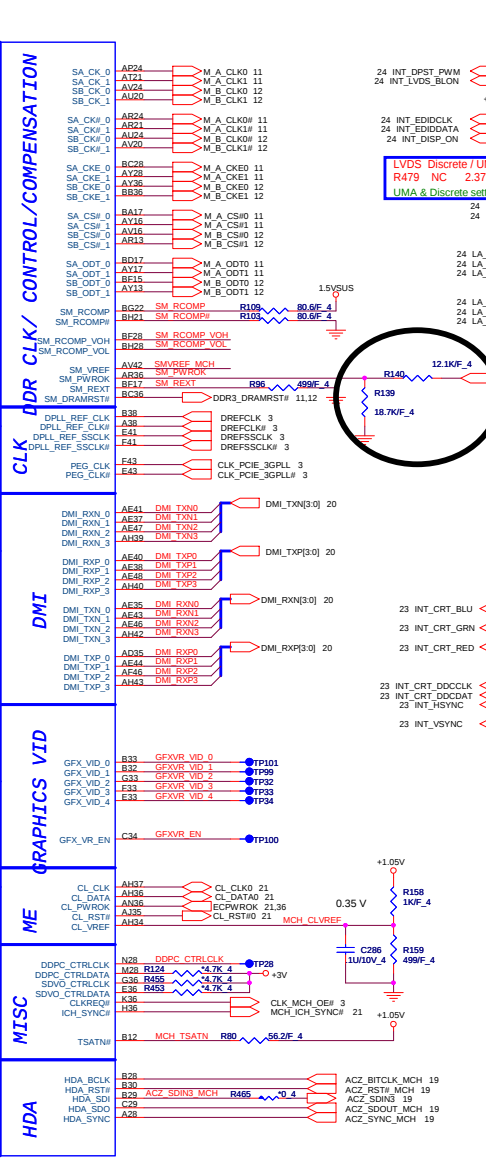
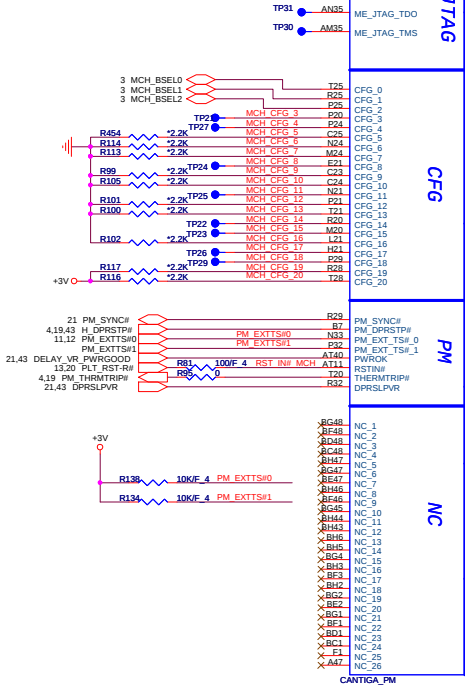


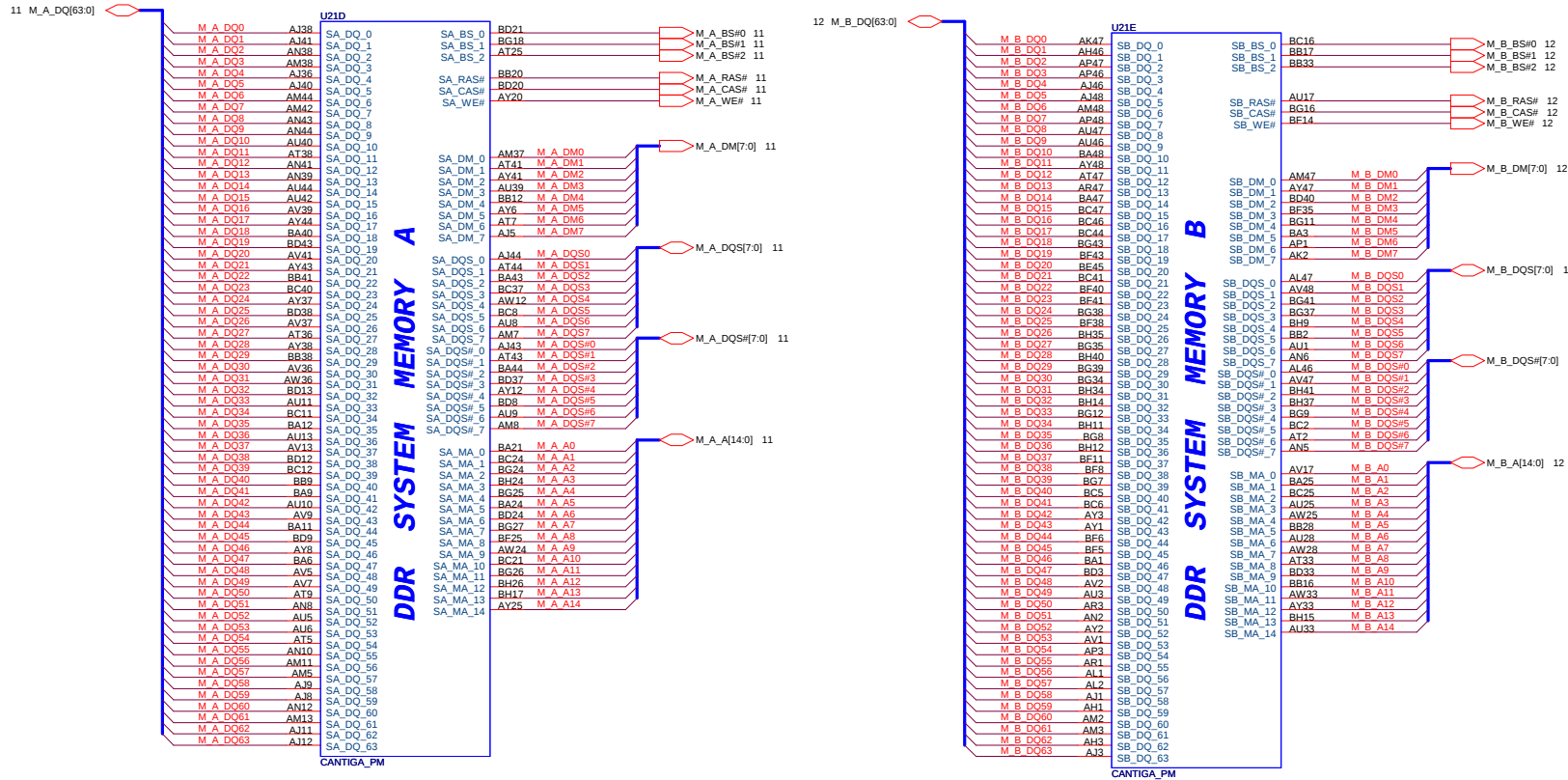
PEG_TX[15:0] PEG_TX[15:0] 13
PEG_TX[15:0] PEG_TX[15:0] 13
PEG_RX[15:0] PEG_RX[15:0] 13
PEG_RX[15:0] PEG_RX[15:0] 13

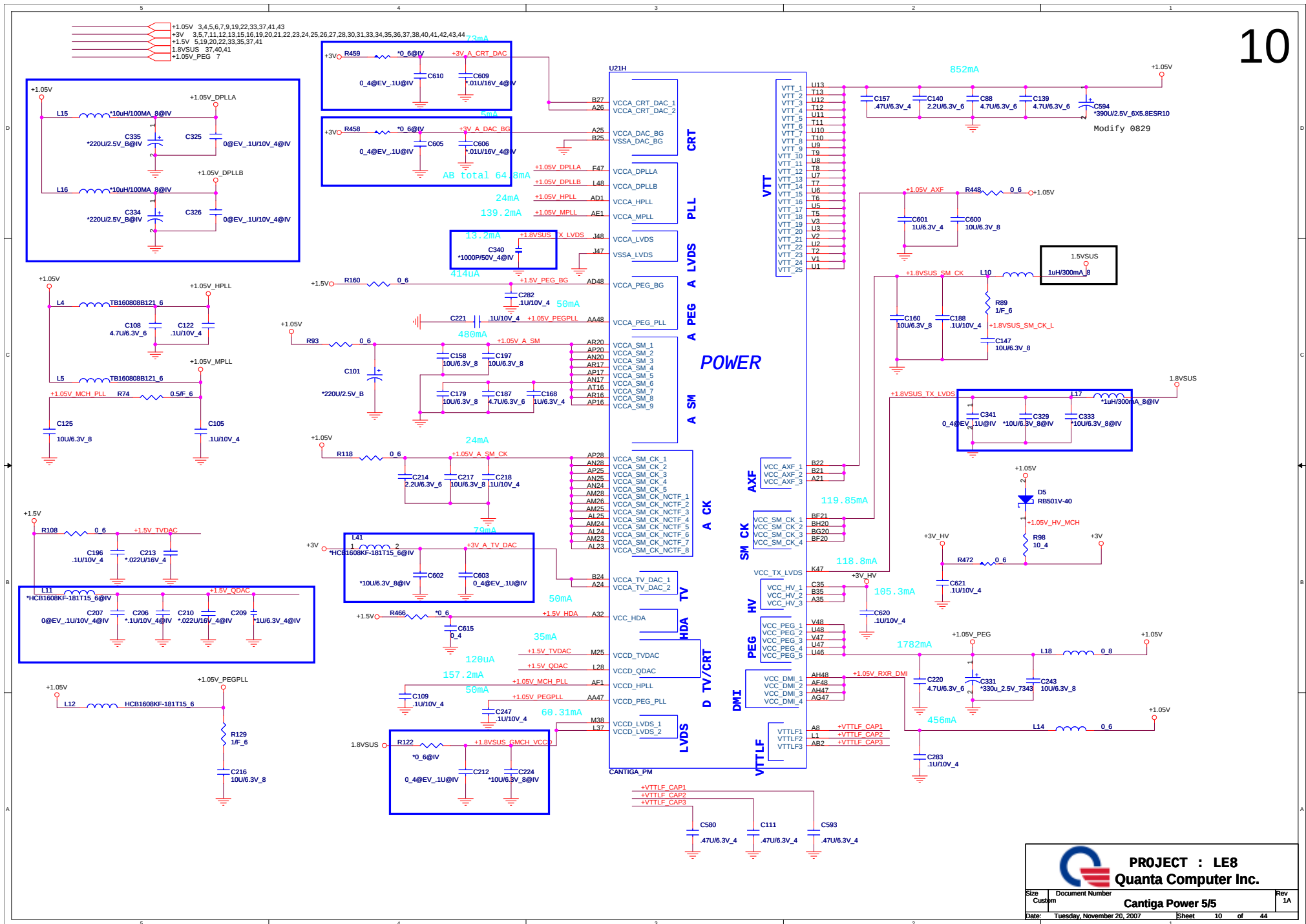
07

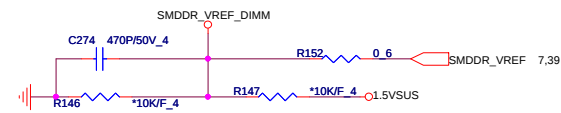
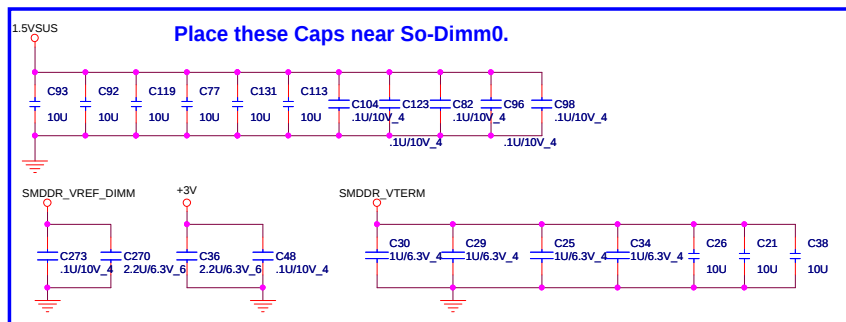
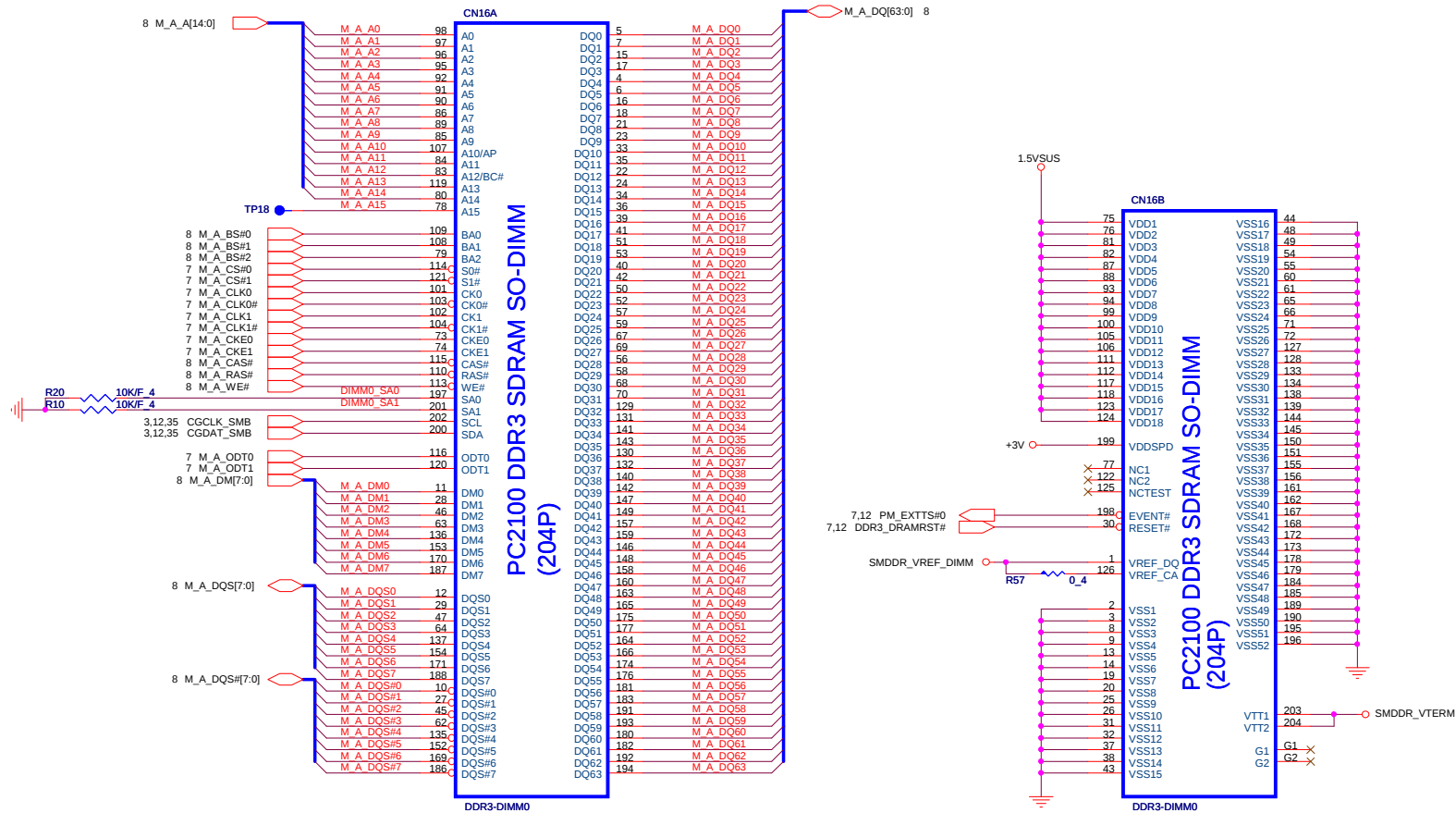
- MCH_CFG_5 DMiX2 selection
Low: DMiX2
High: DMiX4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)
MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low: Normal (Default)
High: Lane Reserved
MCH_CFG_6 ITPM Host Interface
Low: ITPM Host Interface enabled
High: ITPM Host Interface disabled (Default)
MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

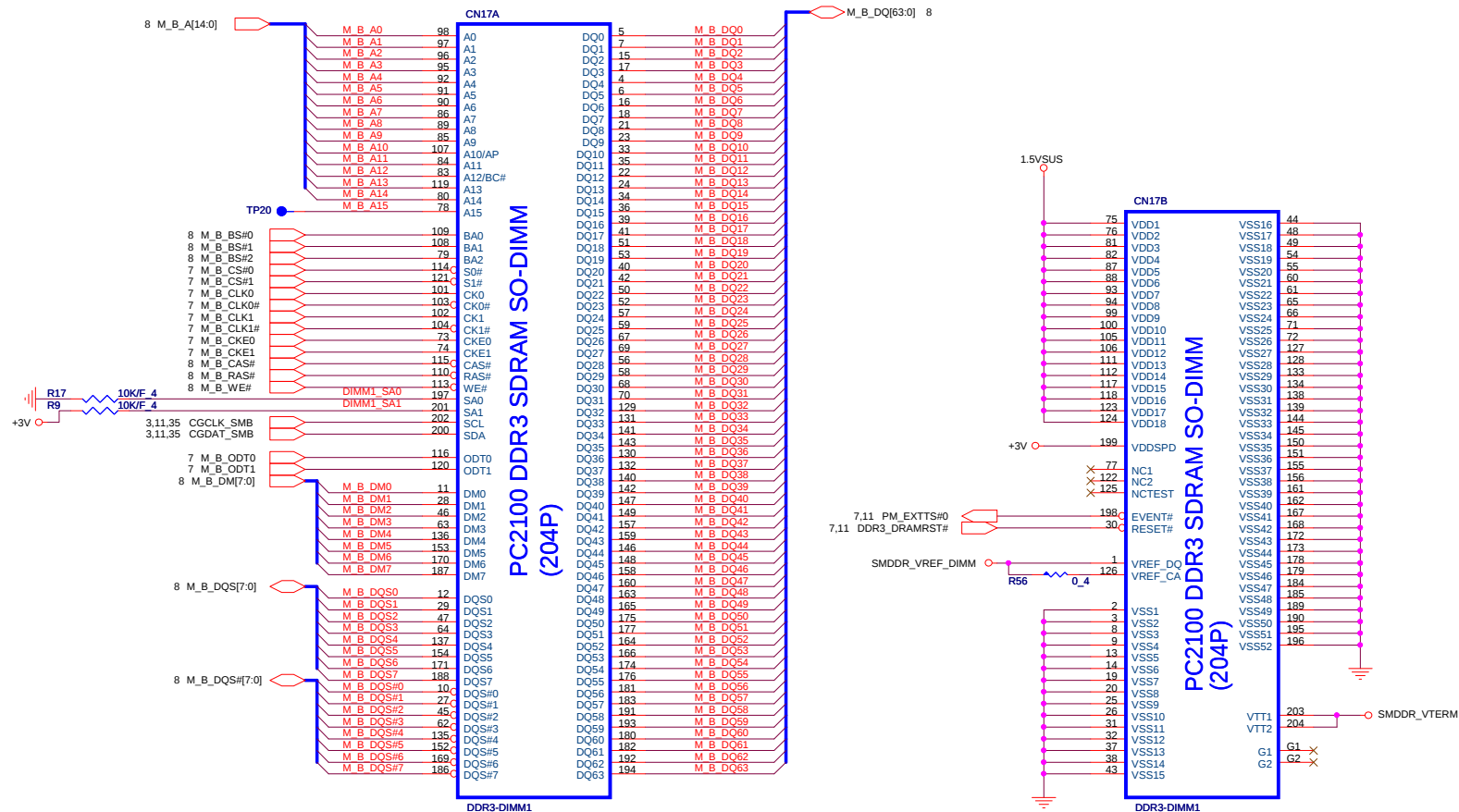
- MCH_CFG_10 PCIe Lookback Enable
Low: Enabled
High: Disabled (Default)
MCH_CFG_12/13 XOR/ALL2/CLOCK Un-gating
MCH_CFG_13 MCH_CFG_12 Configuration
0 0 Reserved
1 0 XOR Mode enabled
0 1 All-2 Mode enabled
1 1 Normal operation (Default)



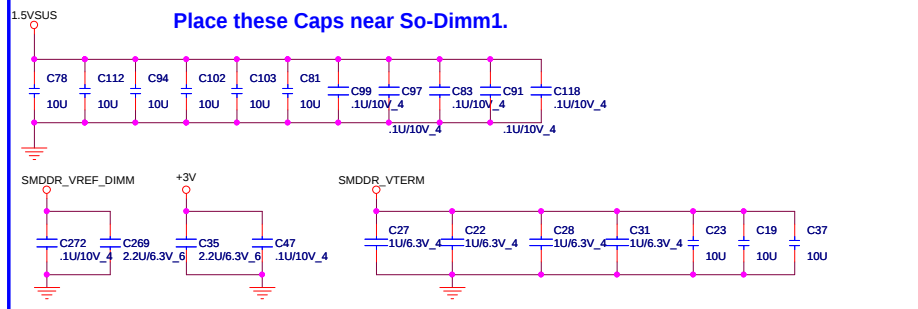






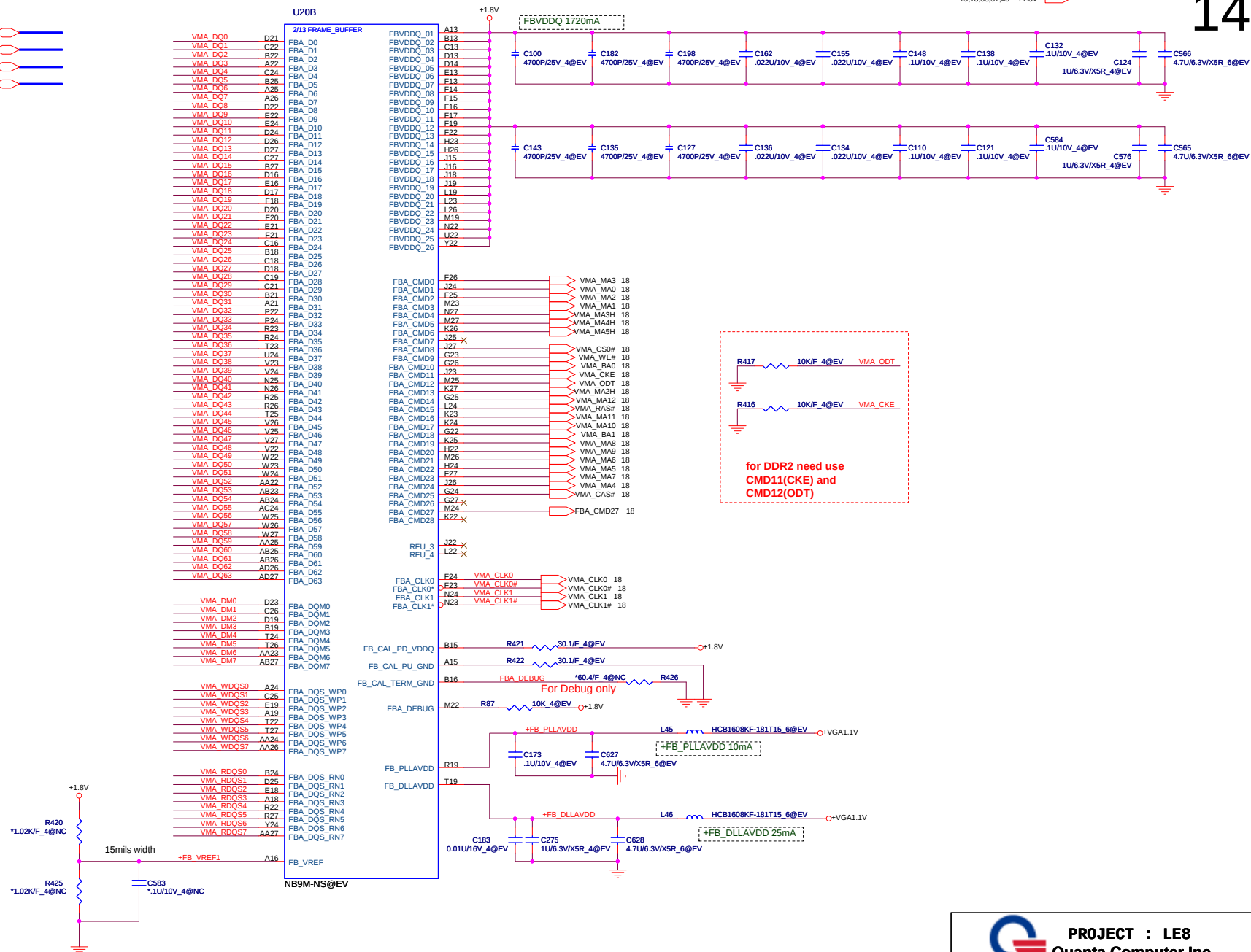


Place these Caps near So-Dimm1.



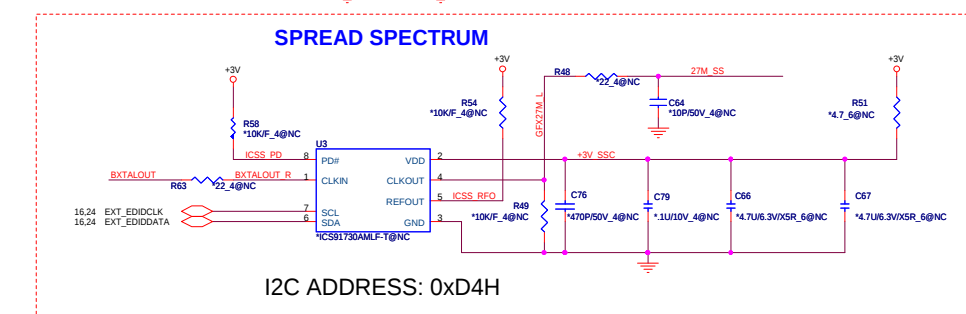
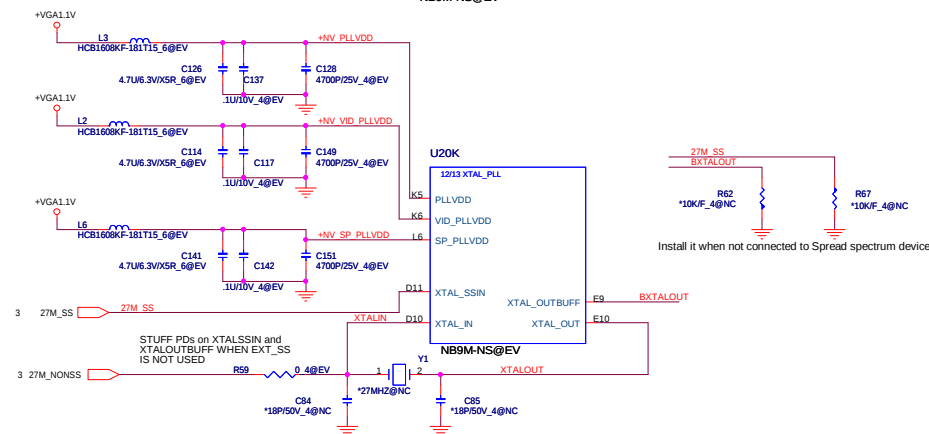
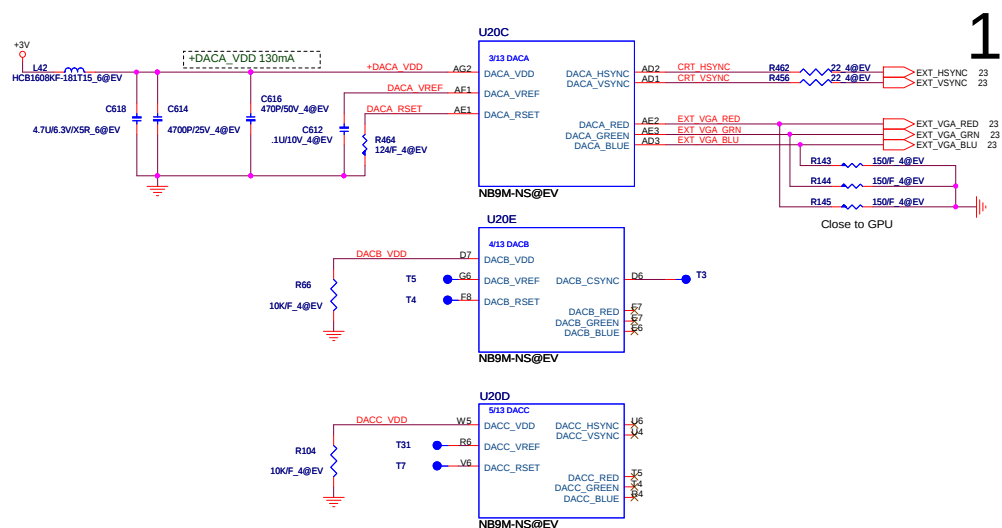
PROJECT : LE8
Quanta Computer Inc.

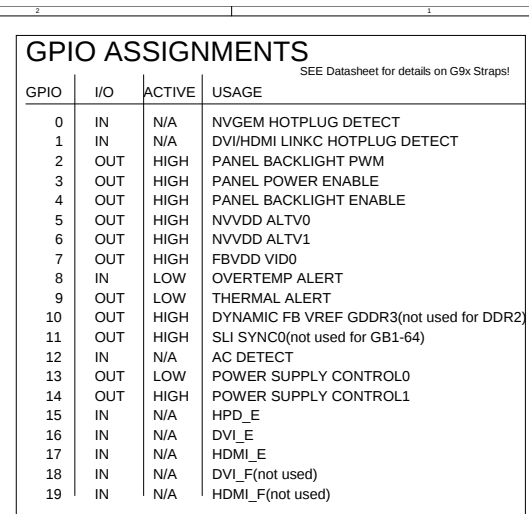
18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]



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Size Document Number
Custom NV9X (MEMORY I/F) 2/5
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3,5,7,10,11,12,13,15,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44

U20J

13/13 GND_NC

AC11	GND_01	NC_01	AA6
AC14	GND_02	NC_02	AC19
AC17	GND_03	NC_03	E15
AC2	GND_04	NC_04	T6
AC20	GND_05		
AC23	GND_06		
AC26	GND_07		
AC5	GND_08		
AC8	GND_09		
AF11	GND_10		
AF14	GND_11		
AF17	GND_12		
AF2	GND_13		
AF20	GND_14		
AF23	GND_15		
AF26	GND_16		
AF5	GND_17		
AF8	GND_18		
B11	GND_19		
B14	GND_20		
B17	GND_21		
B2	GND_22		
B20	GND_23		
B23	GND_24		
B26	GND_25		
B5	GND_26		
B8	GND_27		
E11	GND_28		
E14	GND_29		
E17	GND_30		
E2	GND_31		
E20	GND_32		
E23	GND_33		
E26	GND_34		
E5	GND_35		
E8	GND_36		
H2	GND_37		
H5	GND_38		
J11	GND_39		
J14	GND_40		
J17	GND_41		
K19	GND_42		
K9	GND_43		
L11	GND_44		
L12	GND_45		
L13	GND_46		
L14	GND_47		
L15	GND_48		
L16	GND_49		
L17	GND_50		
L2	GND_51		
L5	GND_52		
M12	GND_53		
M13	GND_54		
M14	GND_55		
M15	GND_56		
M16	GND_57		
P19	GND_58		
P2	GND_59		
P23	GND_60		
P26	GND_61		
P5	GND_62		
P9	GND_63		
T12	GND_64		
T13	GND_65		
T14	GND_66		
T15	GND_67		
T16	GND_68		
U11	GND_69		
U12	GND_70		
U13	GND_71		
U14	GND_72		
U15	GND_73		
U16	GND_74		
U17	GND_75		
U2	GND_76		
U23	GND_77		
U26	GND_78		
U5	GND_79		
V19	GND_80		
V9	GND_81		
W11	GND_82		
W14	GND_83		
W17	GND_84		
Y2	GND_85		
Y23	GND_86		
Y26	GND_87		
Y5	GND_88		

NB9M-NS@EV

NB9M: VGACORE +0.9V ~ +1.0V

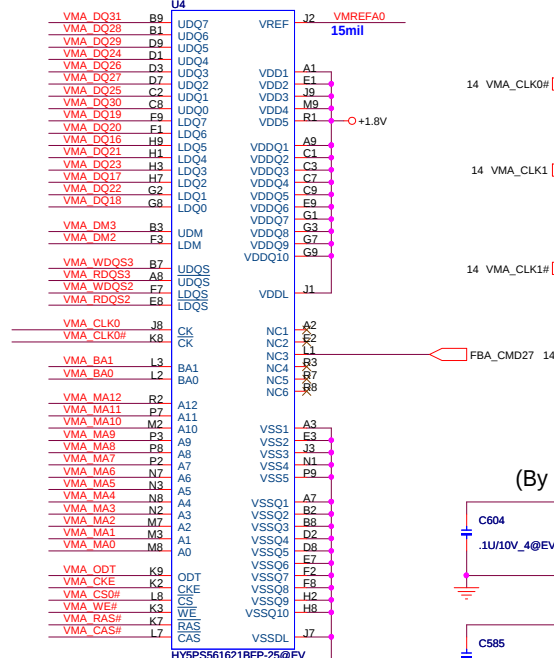
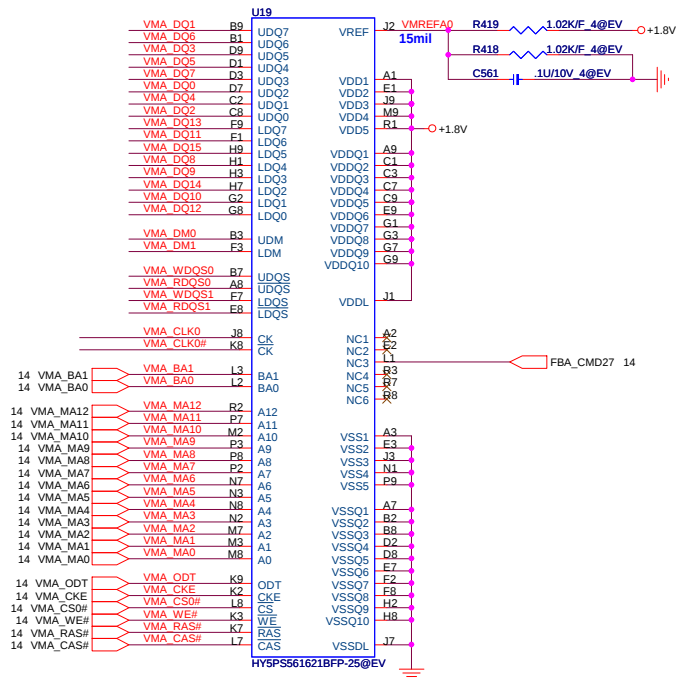
power up sequence

PXE 1.1VDD
I/O 3.3V
NVCORE
1.8VFBDDQ

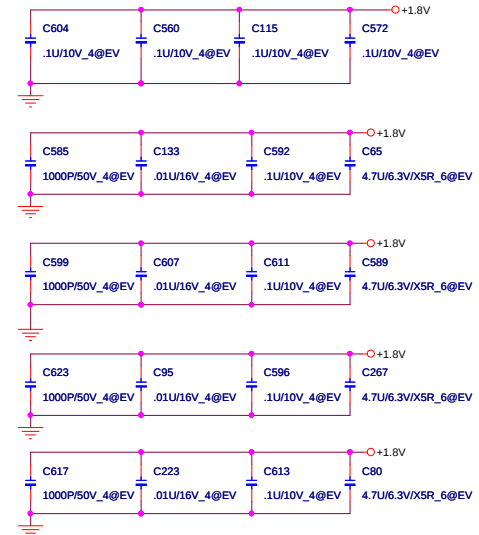


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Custom	NV9X GND 5/5	1A
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(By pass capacitor)



512Mb(32Mx16) : AKD5FG-TW31/Hynix(HY5PS121621CFP-25)
AKD5FG-T04/Quimonda(HYB18T512162B2F-20)

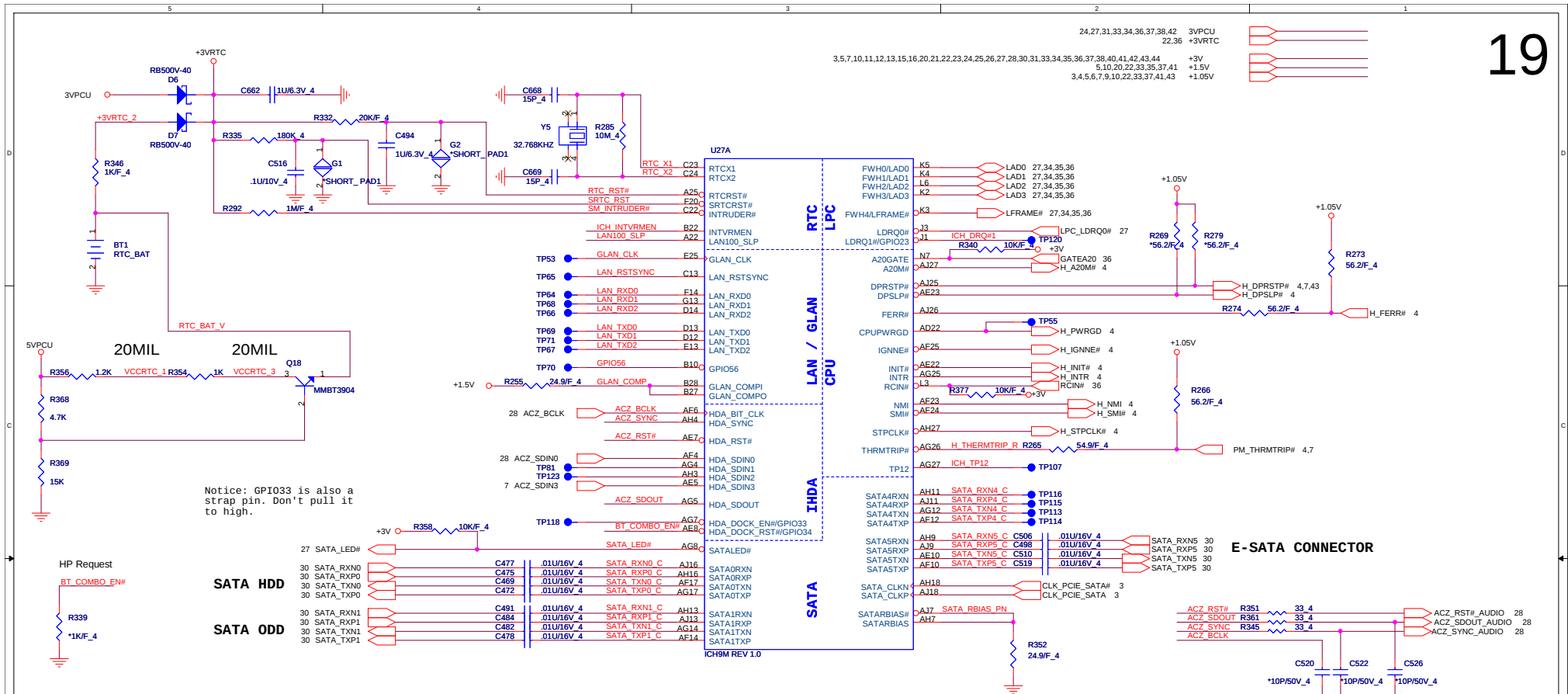
14 VMA_DQ[63..0]

14 VMA_DM[7..0]

14 VMA_WDQS[7..0]

14 VMA_RDQS[7..0]

14,15,33,37,40 +1.8V



SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

*1K/F_4	R349	GNT0# 20,25
*1K/F_4	R294	SPI_CS#1_R 20

A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---

*1K/F_4	R348	GNT3# 20
---------	------	----------

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

*1K/F_4	R342	ACZ_SPKR 21,28
---------	------	----------------

TPM physical presence	
ICH_GPIO57	Low: Default

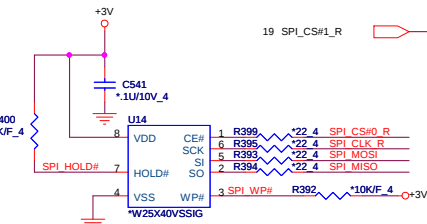
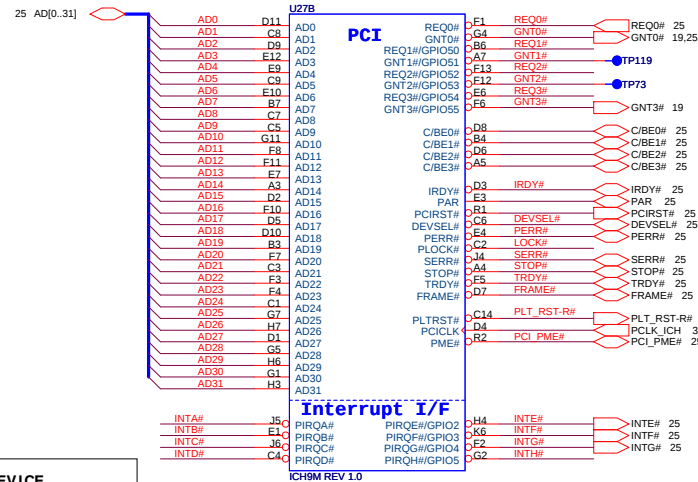
3V_55	R570	ICH_GPIO57 21
	R568	100K/F_4

MINI CARD PCI-E(WLAN)

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E(WWAN)

PCI-E-LAN

512K byte SPI ROM
For HDCP only

PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#, G#	RICOH R5C847

3,5,7,10,11,12,13,15,16,19,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44
5.10,19,22,33,35,37,41 +1.5V
21,25,26,28,33,34,35,37,39,43 +3V
3V3US



USB Connector

Finger Printer

BLUETOOTH

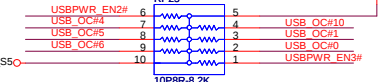
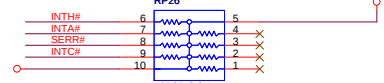
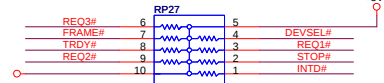
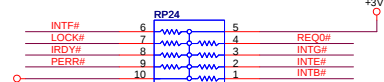
NEW CARD

USB Connector

USB Connector

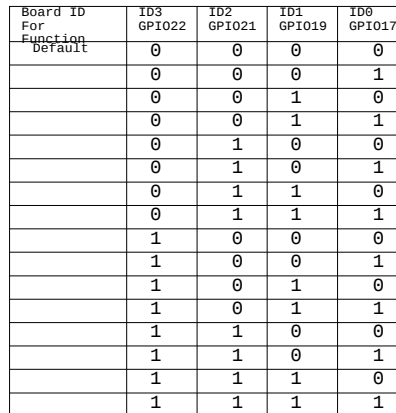
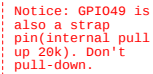
WWAN Min-Card

WLAN Min-Card

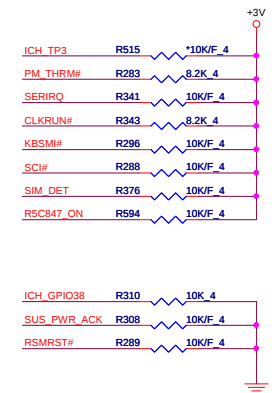


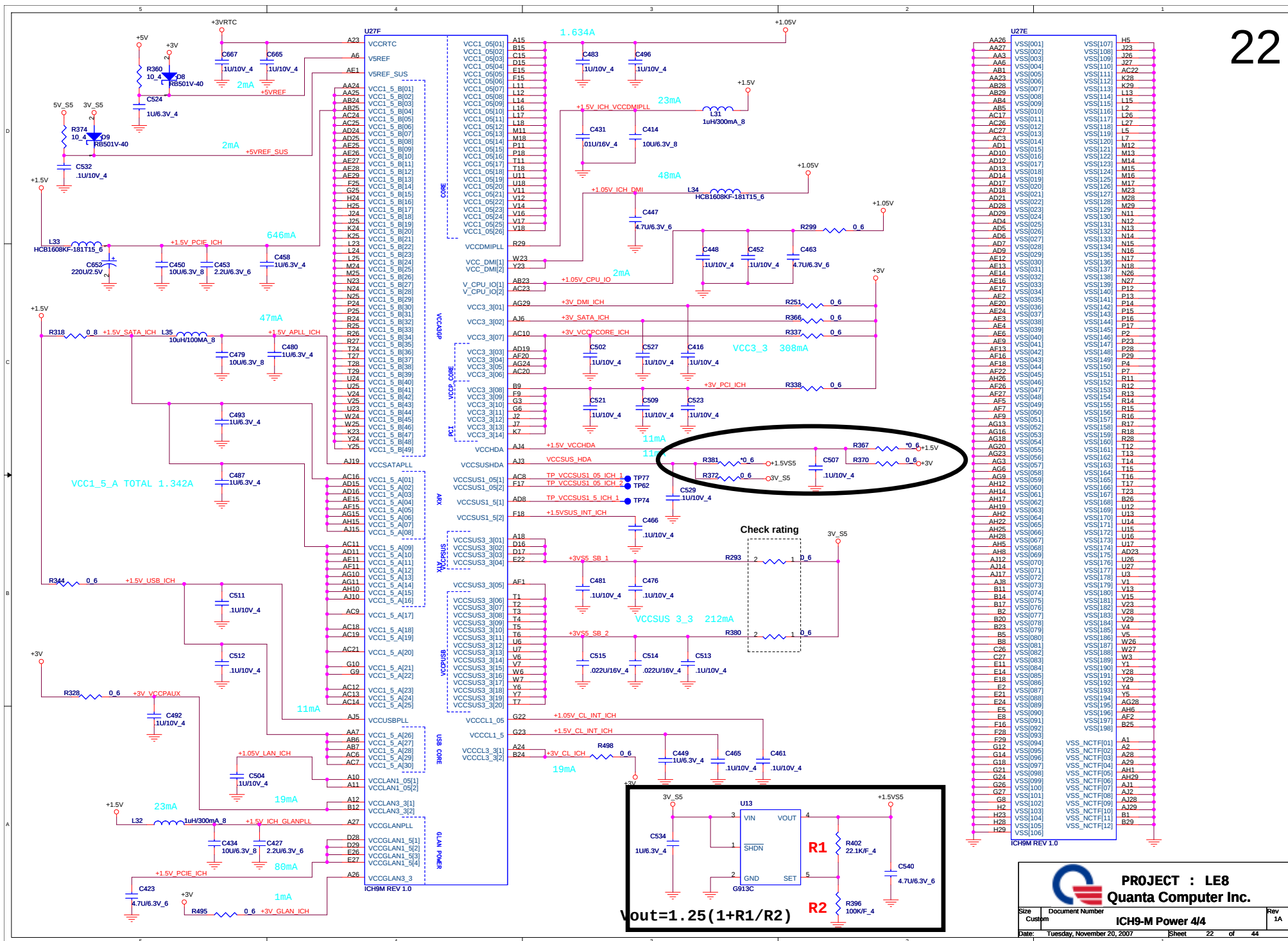
PROJECT : LE8
Quanta Computer Inc.

Size: Custom Document Number: ICH9-M PCIE 2/4
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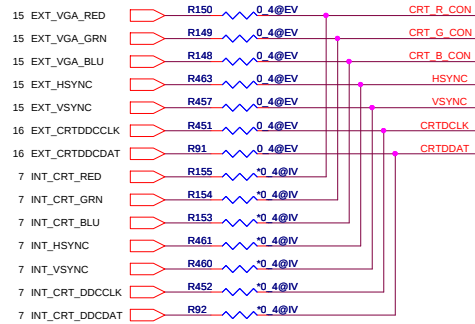


Board ID For Model	ID5 GPIO37	ID4 GPIO38
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1





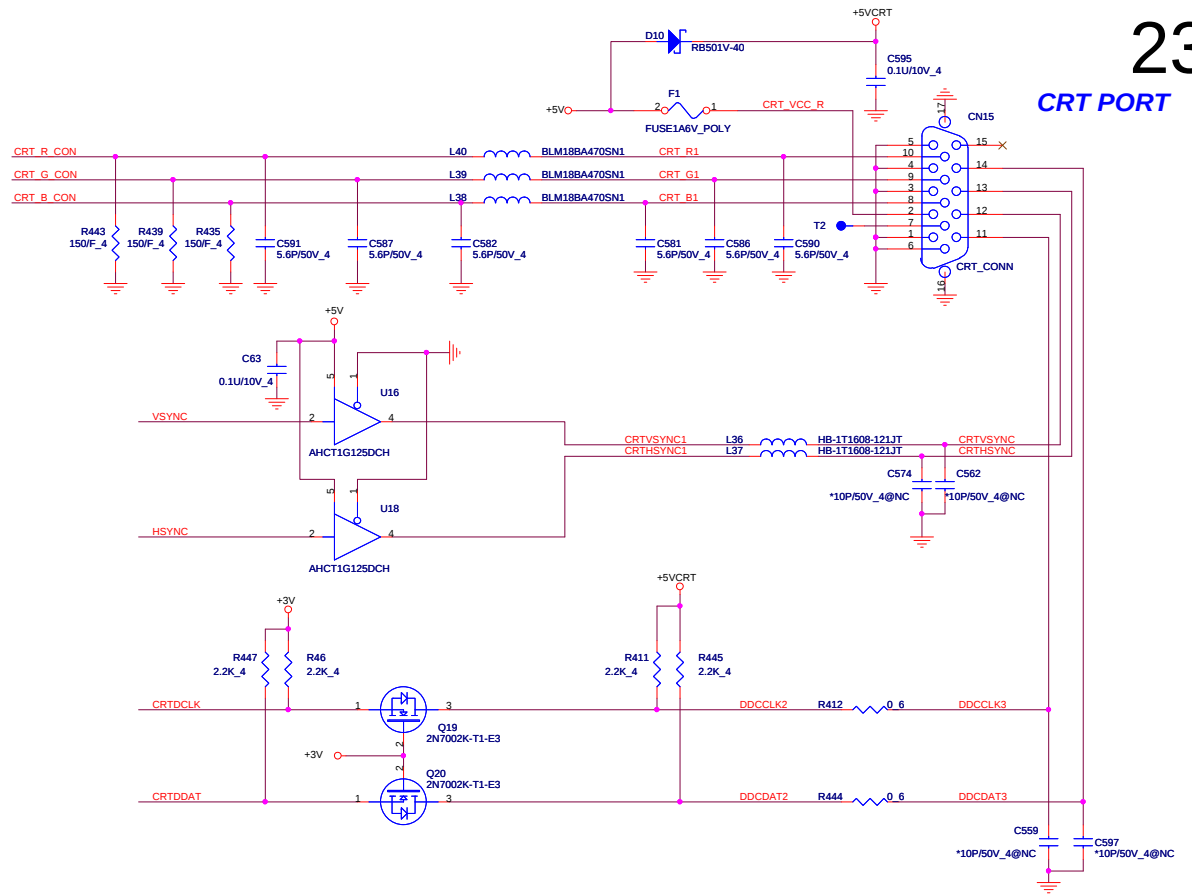
CRT SWITCH



UMA & Discrete setting

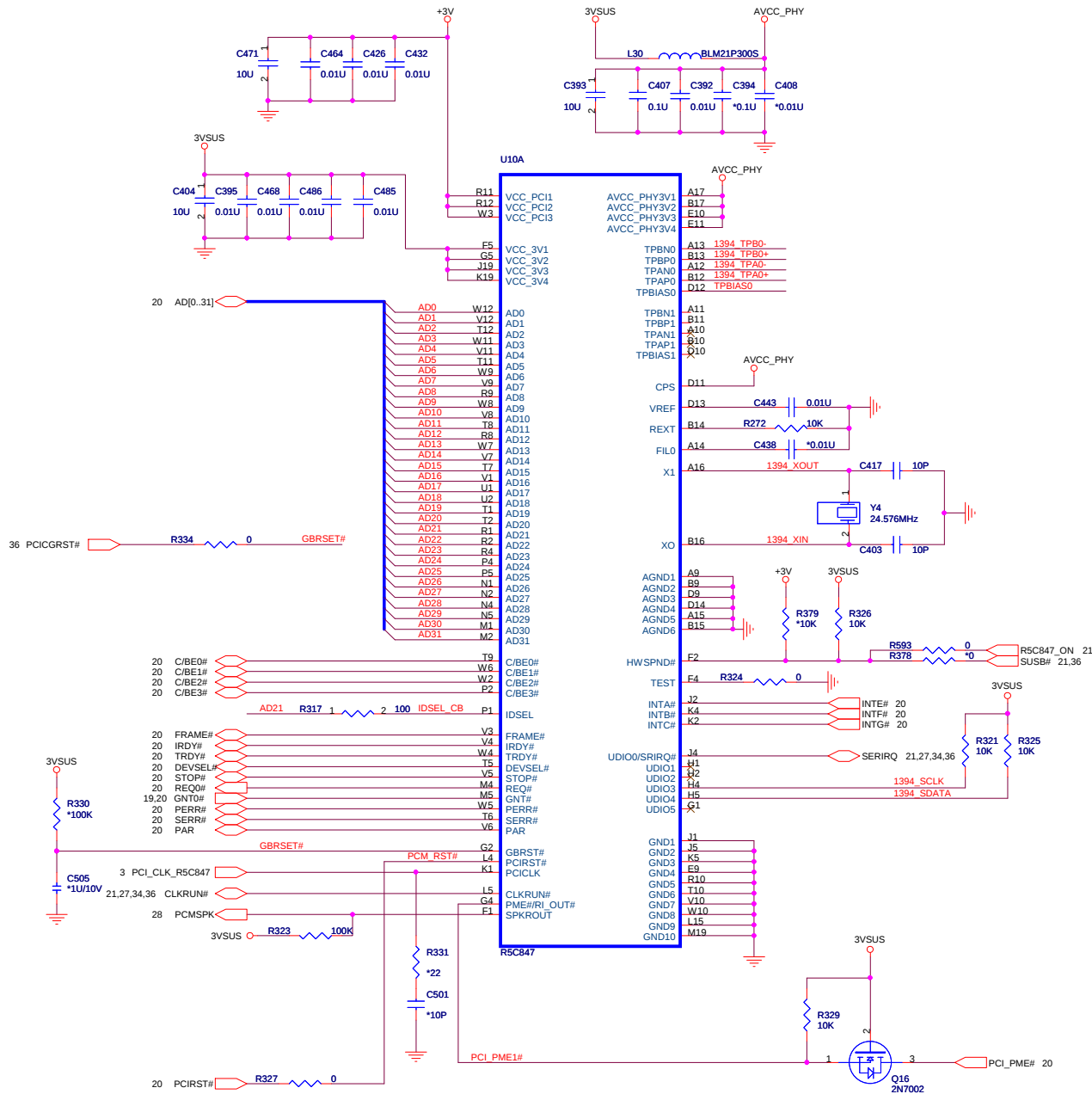
LVDS Discrete / UMA

R150	0	NC
R149	0	NC
R148	0	NC
R463	0	NC
R457	0	NC
R451	0	NC
R91	0	NC
R155	NC	0
R154	NC	0
R153	NC	0
R461	NC	0
R460	NC	0
R452	NC	0
R92	NC	0

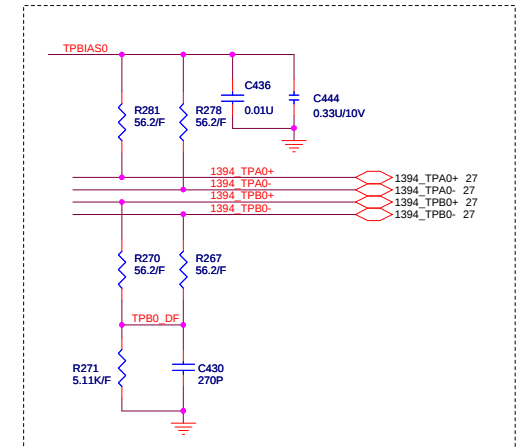


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CLOSED CHIP



R5C847 pin to pin compatible with R5C843/R5C841



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PCMCIA CONNECTOR

This schematic diagram illustrates the PCMCIA connector interface, showing the connection between the PCMCIA connector (CN9) and the internal circuitry. The diagram includes the following components and connections:

- PCMCIA Connector (CN9):** The connector is shown with pins 1 through 68. Pins 1-16 are for data (CDATA0-CDATA15), pins 17-32 are for address (CADDR0-CADDR15), pins 33-48 are for control (OE#, WE#, CE1#, CE2#, REG#, RESET, WAIT#, IOIS16#, IREQ#, SPKR#, CHST#, VS2, VS1, CD1#, INPACK#, IORD#, IOWR#, USBP, USBD, AVPPEN0, AVPPEN1, AVCC3EN#, AVCCSEN#), and pins 49-68 are for power (A_VCC, A_VPP, 3VSUS, 5VSUS, VCC, GND).
- Internal Circuitry:** The diagram shows the internal circuitry of the PCMCIA controller, including the R5C847 chip. The chip is connected to the PCMCIA connector pins and the internal power supply. The chip has pins for VCC, GND, A_VCC, A_VPP, 3VSUS, 5VSUS, VCC, GND, and various control signals.
- Power Supply:** The power supply is shown with pins for A_VCC, A_VPP, 3VSUS, 5VSUS, VCC, and GND. The power supply is connected to the PCMCIA connector pins and the internal circuitry.
- Control Signals:** The control signals are shown with pins for OE#, WE#, CE1#, CE2#, REG#, RESET, WAIT#, IOIS16#, IREQ#, SPKR#, CHST#, VS2, VS1, CD1#, INPACK#, IORD#, IOWR#, USBP, USBD, AVPPEN0, AVPPEN1, AVCC3EN#, and AVCCSEN#.

CARD-READER CONNECTOR (SD / MMC / MS)

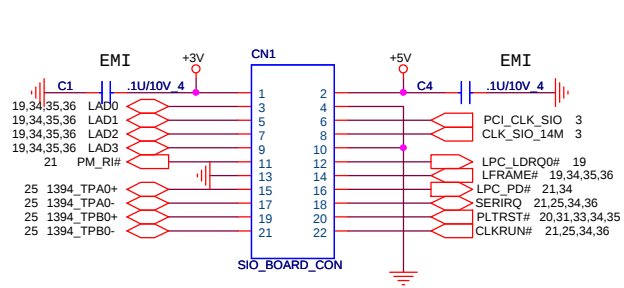
This schematic diagram illustrates the card-reader connector interface, showing the connection between the card-reader connector (CN12) and the internal circuitry. The diagram includes the following components and connections:

- Card-Reader Connector (CN12):** The connector is shown with pins 1 through 40. Pins 1-10 are for data (MS-DATA1, MS-DATA2, MS-DATA3, MS-DATA0, SD-CLK, SD-CMD, SD-D0, SD-D1, SD-D2, SD-D3, SD-D4, SD-D5, SD-D6, SD-D7, SD-D8, SD-D9, SD-D10, SD-D11, SD-D12, SD-D13, SD-D14, SD-D15, SD-D16, SD-D17, SD-D18, SD-D19, SD-D20, SD-D21, SD-D22, SD-D23, SD-D24, SD-D25, SD-D26, SD-D27, SD-D28, SD-D29, SD-D30, SD-D31, SD-D32, SD-D33, SD-D34, SD-D35, SD-D36, SD-D37, SD-D38, SD-D39, SD-D40), pins 11-20 are for address (MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS, MS-BS), and pins 21-40 are for power (VCC, GND, A_VCC, A_VPP, 3VSUS, 5VSUS, VCC, GND, and various control signals).
- Internal Circuitry:** The diagram shows the internal circuitry of the card-reader controller, including the U29 chip. The chip is connected to the card-reader connector pins and the internal power supply. The chip has pins for VCC, GND, A_VCC, A_VPP, 3VSUS, 5VSUS, VCC, GND, and various control signals.
- Power Supply:** The power supply is shown with pins for A_VCC, A_VPP, 3VSUS, 5VSUS, VCC, and GND. The power supply is connected to the card-reader connector pins and the internal circuitry.
- Control Signals:** The control signals are shown with pins for MS-DATA1, MS-DATA2, MS-DATA3, MS-DATA0, SD-CLK, SD-CMD, SD-D0, SD-D1, SD-D2, SD-D3, SD-D4, SD-D5, SD-D6, SD-D7, SD-D8, SD-D9, SD-D10, SD-D11, SD-D12, SD-D13, SD-D14, SD-D15, SD-D16, SD-D17, SD-D18, SD-D19, SD-D20, SD-D21, SD-D22, SD-D23, SD-D24, SD-D25, SD-D26, SD-D27, SD-D28, SD-D29, SD-D30, SD-D31, SD-D32, SD-D33, SD-D34, SD-D35, SD-D36, SD-D37, SD-D38, SD-D39, and SD-D40.

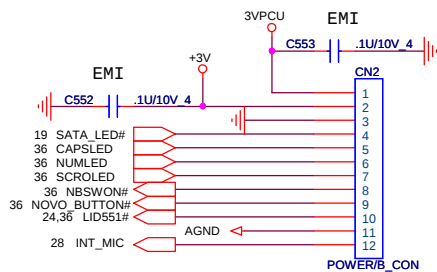
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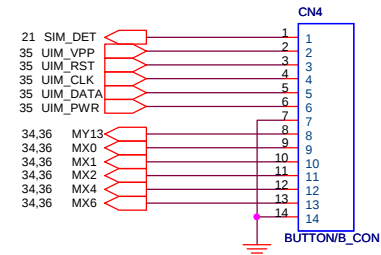
SIO BOARD



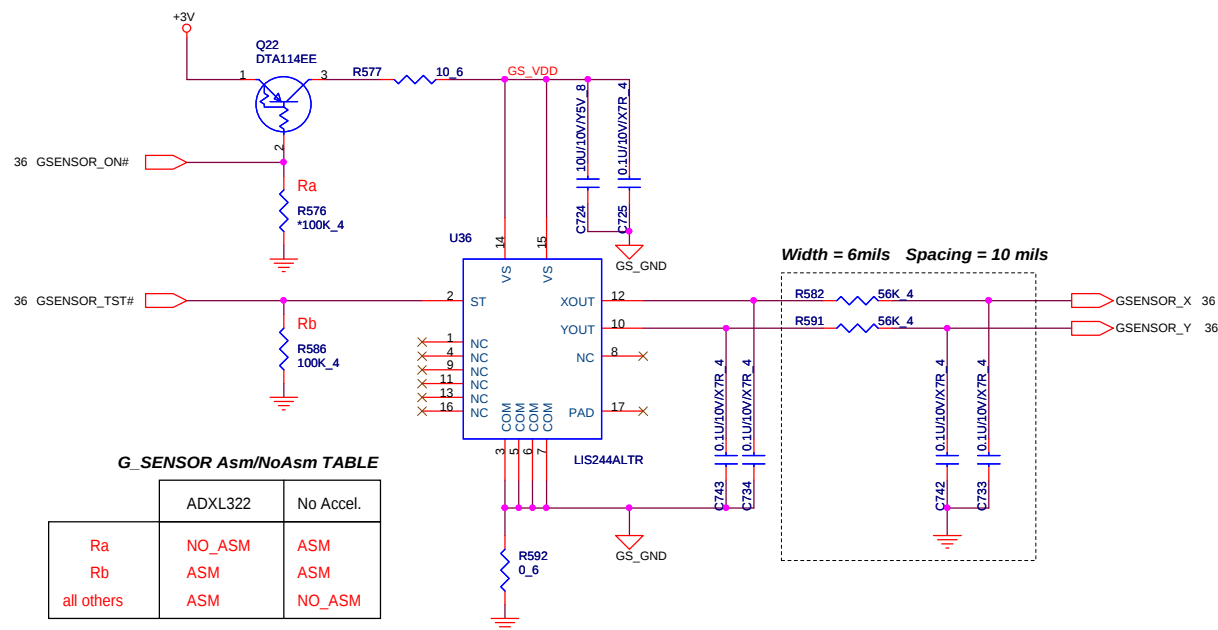
POWER BOARD

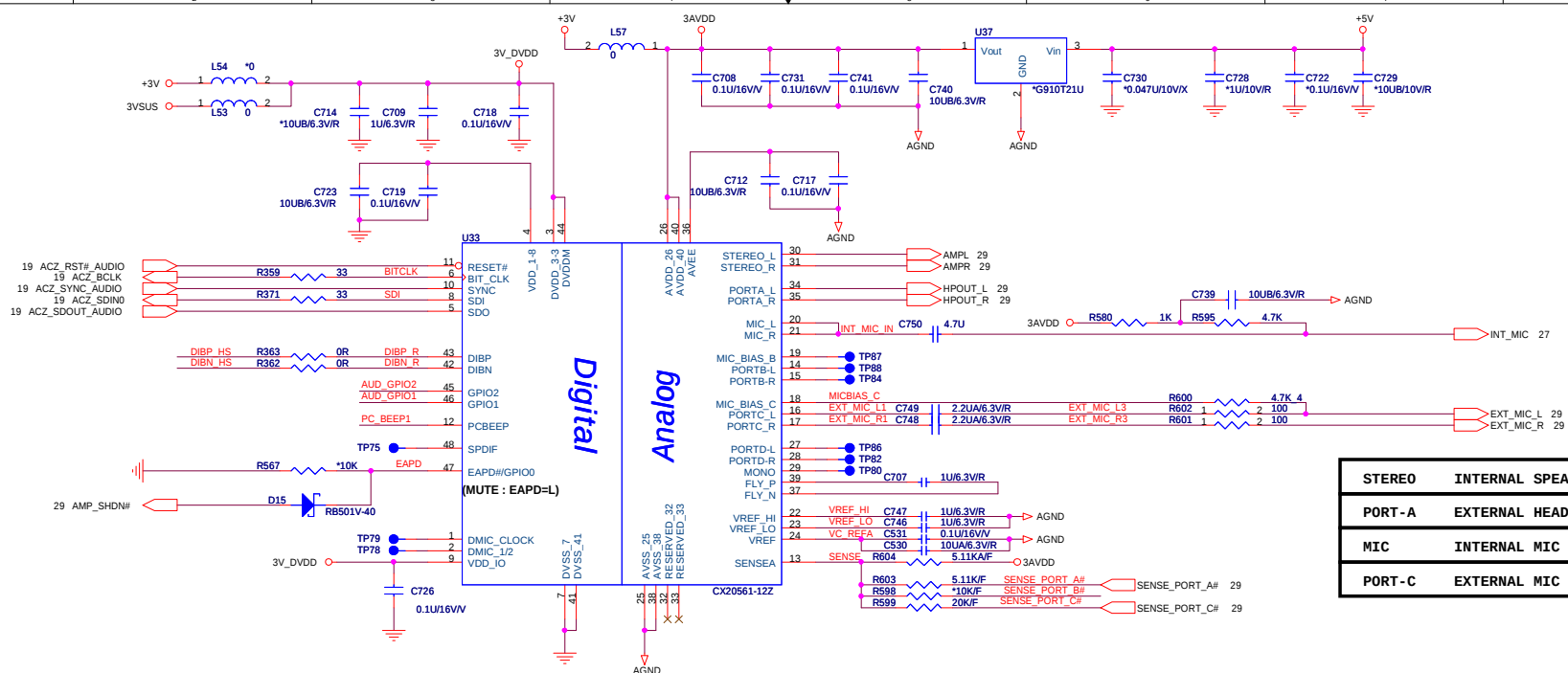


BUTTON BOARD



G-SENSOR





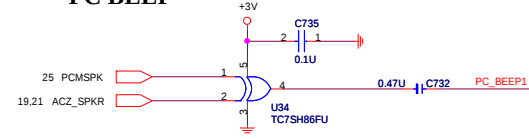
STEREO	INTERNAL SPEAKERS
PORT - A	EXTERNAL HEAD - PHONE
MIC	INTERNAL MIC
PORT - C	EXTERNAL MIC

GAIN	10K GPIO RESISTORS	
	GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

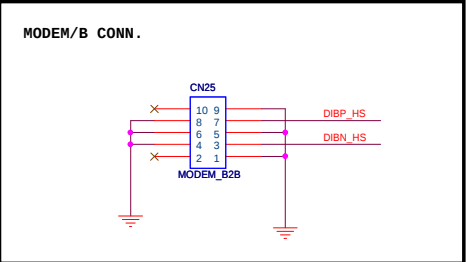
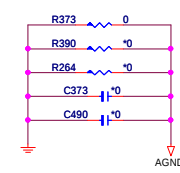
Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2



PC BEEP



FOR EMI SOLUTION



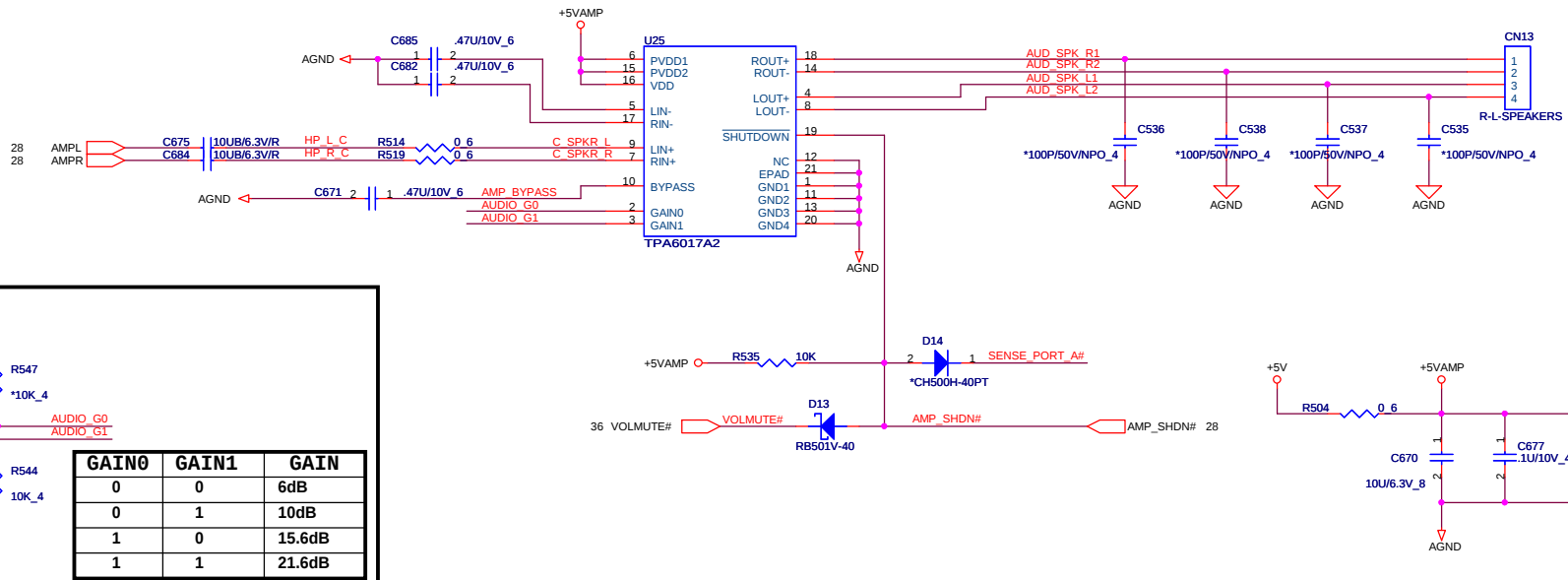


PROJECT : LE8
Quanta Computer Inc.

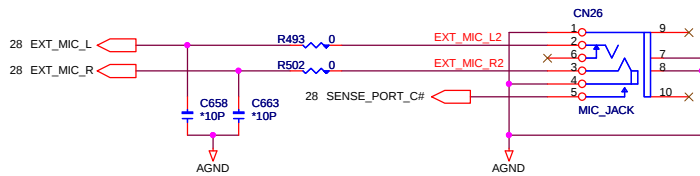
Size	Document Number	Rev
Custom		1A
AUDIO CODEC+MODEM		
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INTERNAL SPEAKER AMPLIFIER

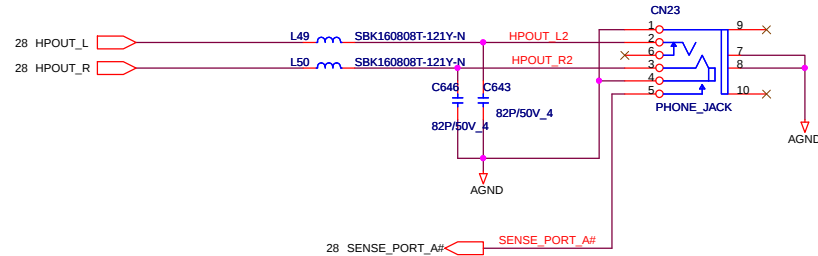
29



MIC-IN JACK

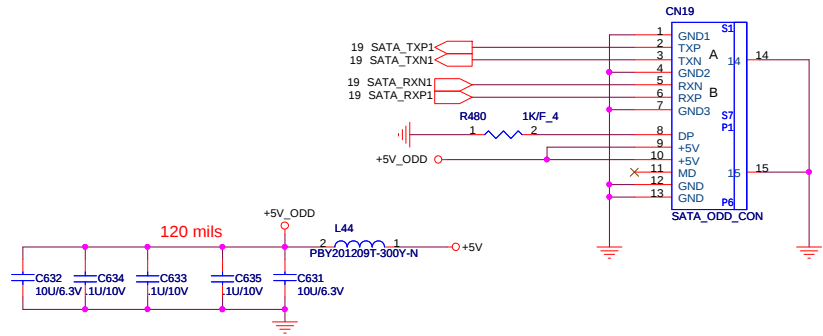


HEADPHONE

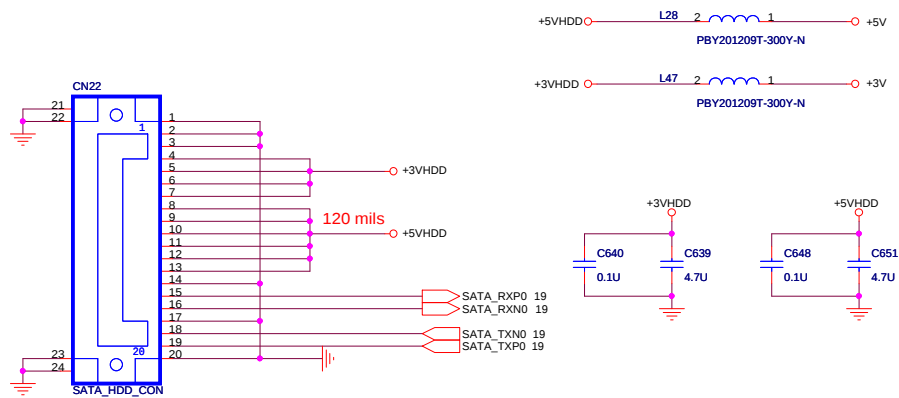


PROJECT : LE8
Quanta Computer Inc.

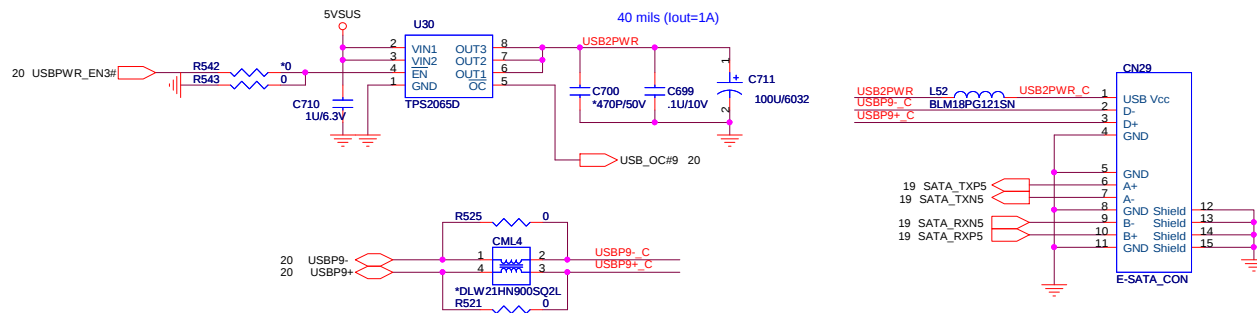
Size Custom	Document Number AMP_TPA6017 & JACKS	Rev 1A
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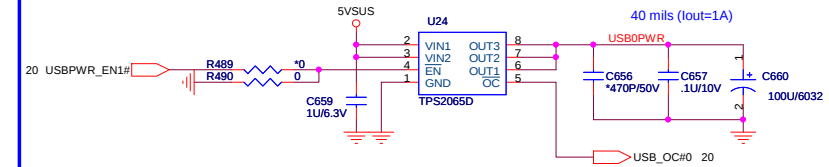
SATA-HDD CONNECTOR



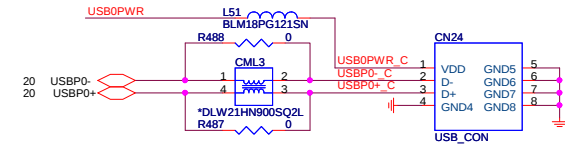
USB + eSATA CONNECTOR



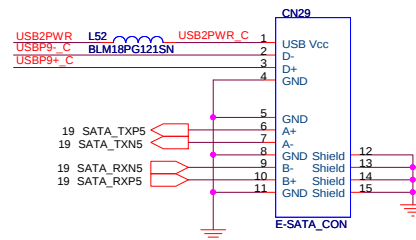
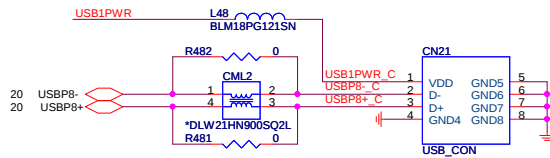
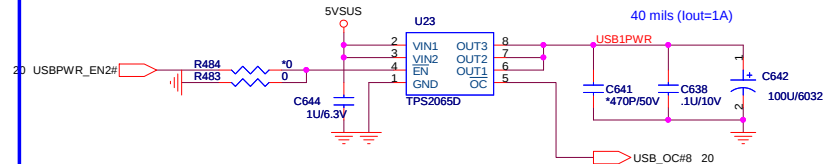
USBX2

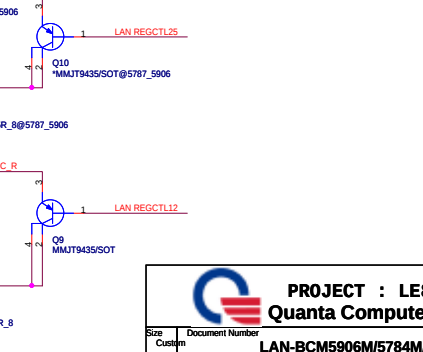


USB 0



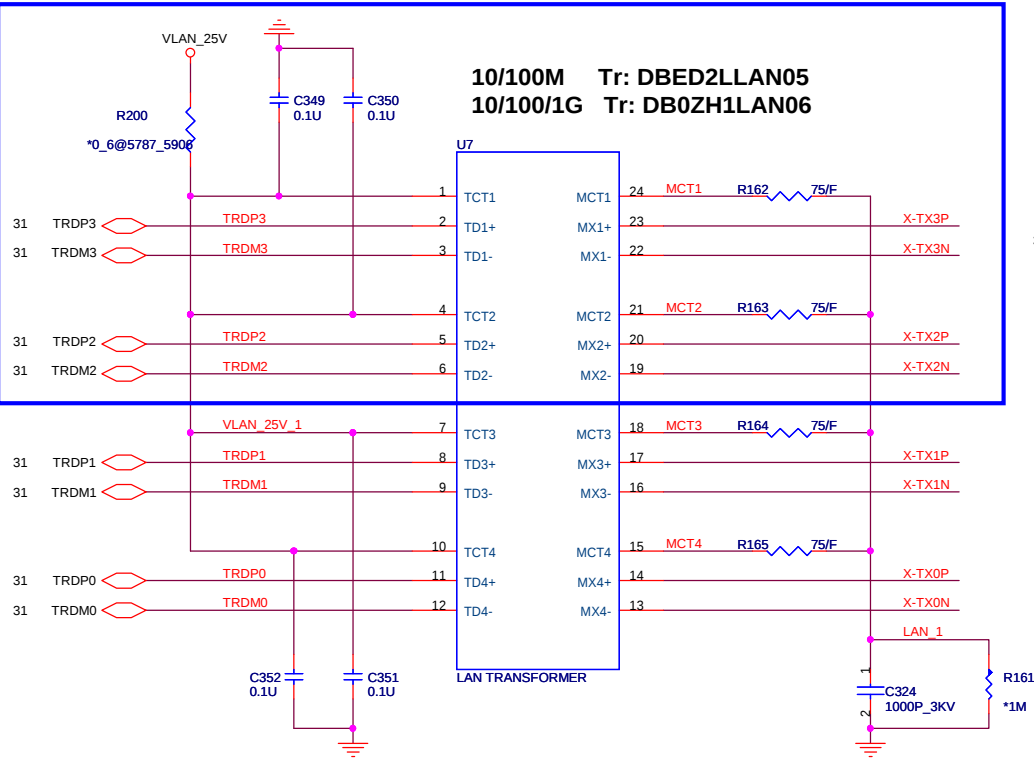
USB 1



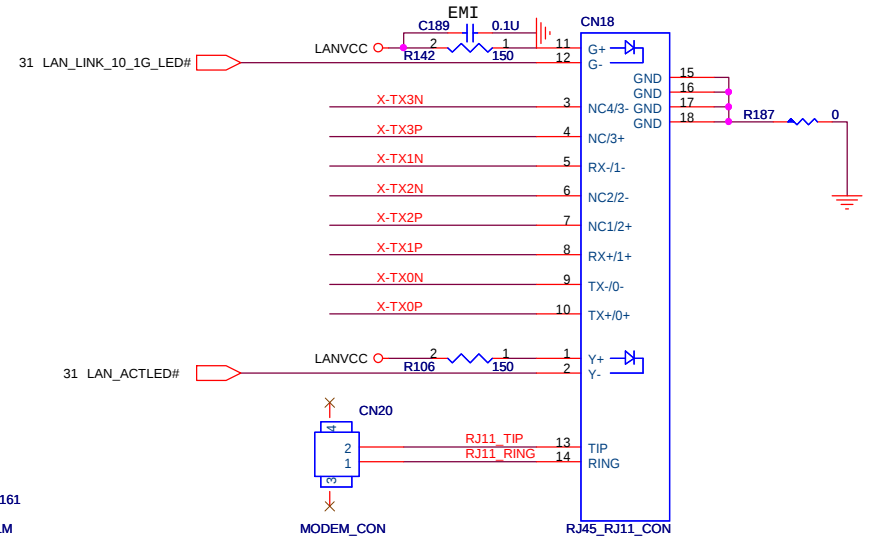


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Size	Document Number		
Custom			
LAN-BCM5906M/5784M/5787M			
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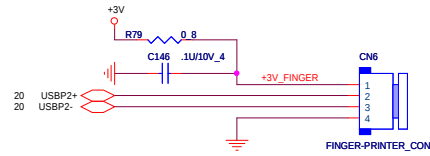
10/100M Tr: DBED2LLAN05
10/100/1G Tr: DB0ZH1LAN06



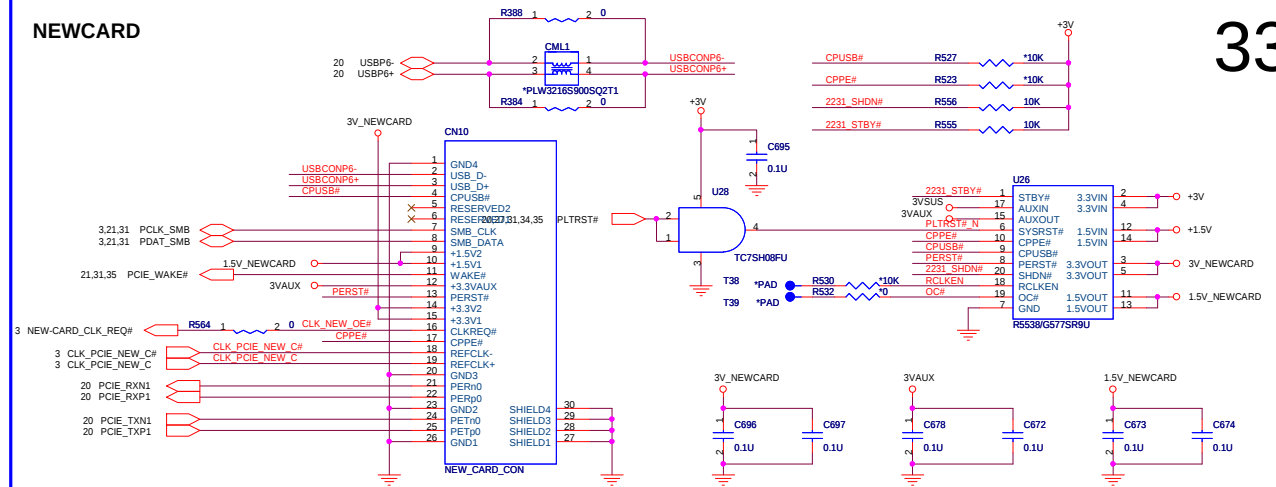
RJ45/RJ11 Connector



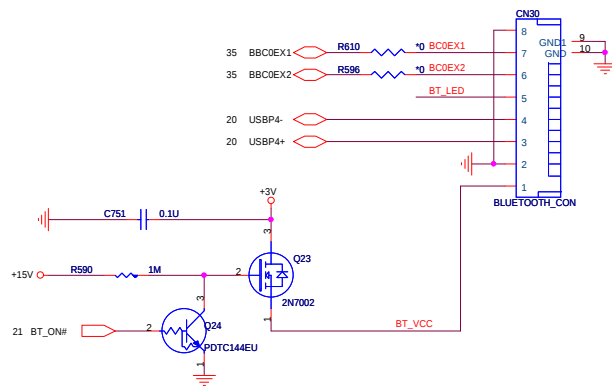
FINGER PRINTER



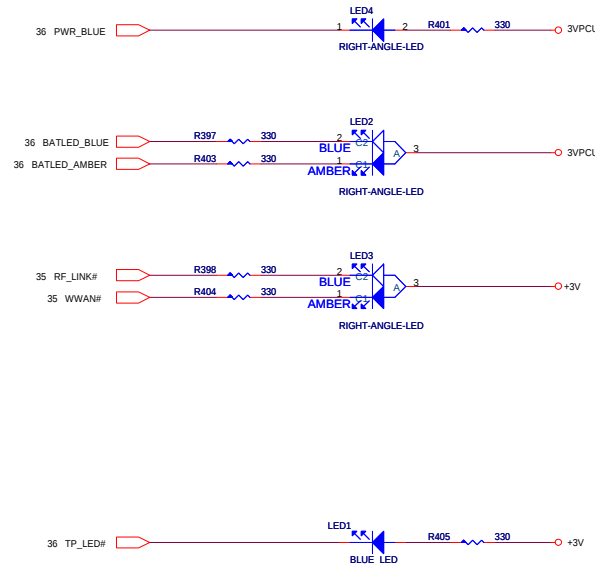
NEWCARD



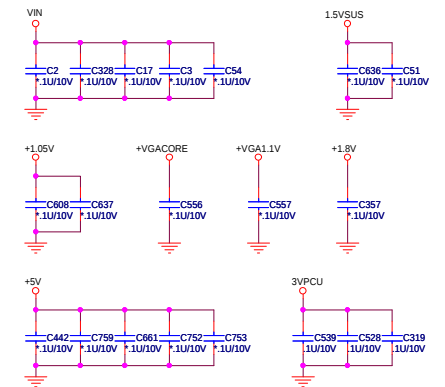
BLUETOOTH



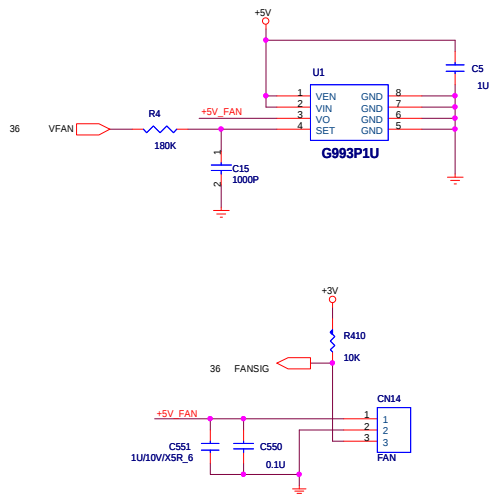
LED



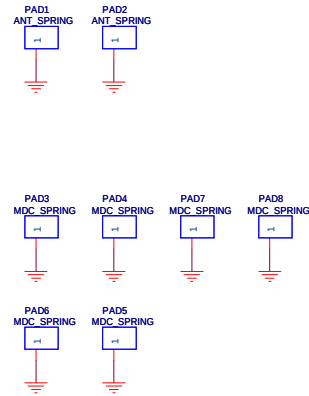
EMI CAPACITORS



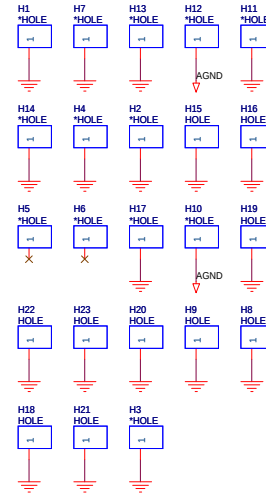
FAN CONTROL



EMI PAD

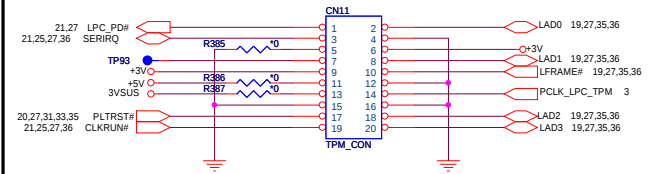


HOLES

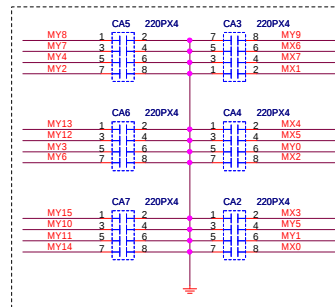
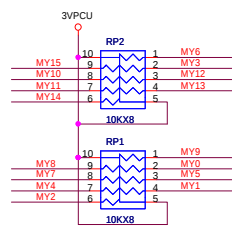
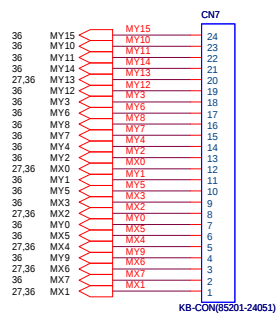


Board TO Board TPM MODULE

34

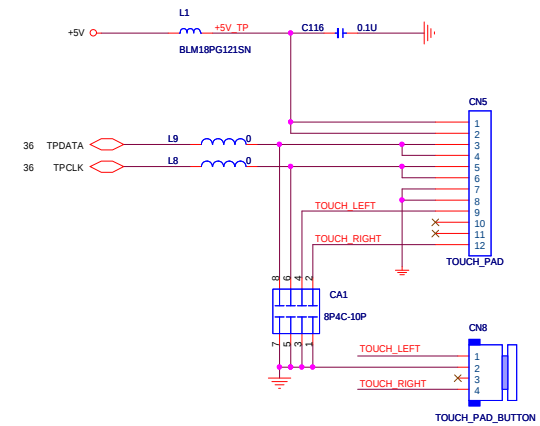


KEYBOARD



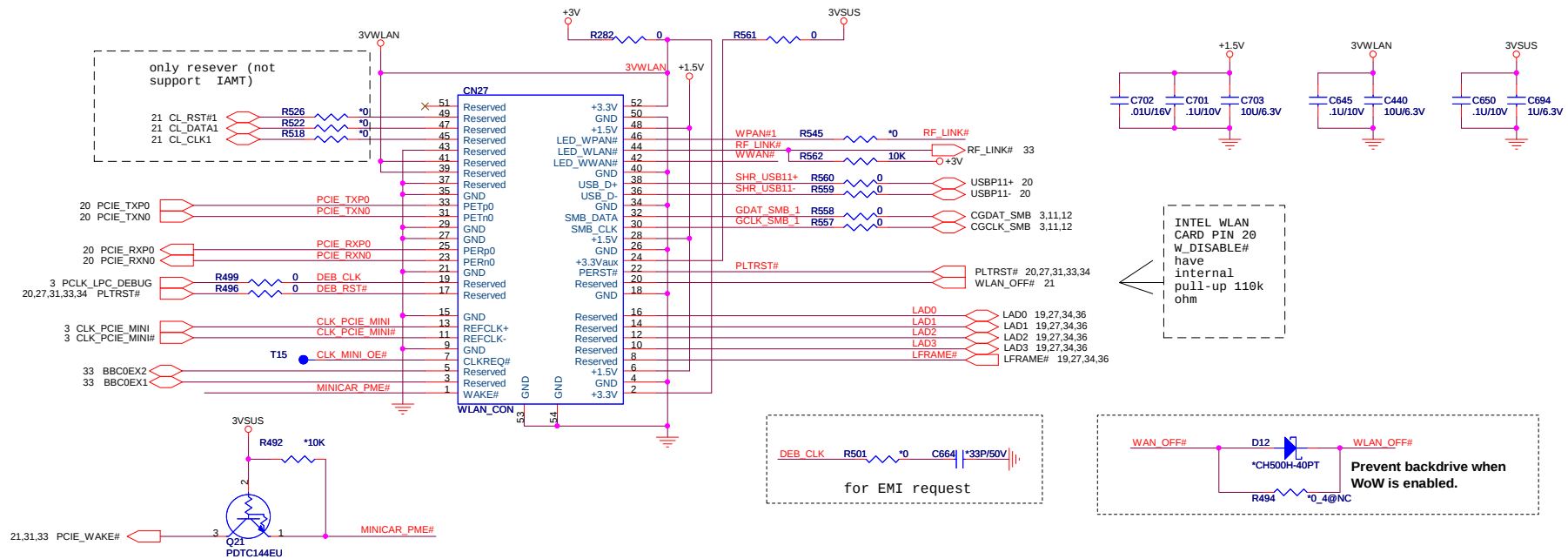
For EMI request

TOUCH PAD

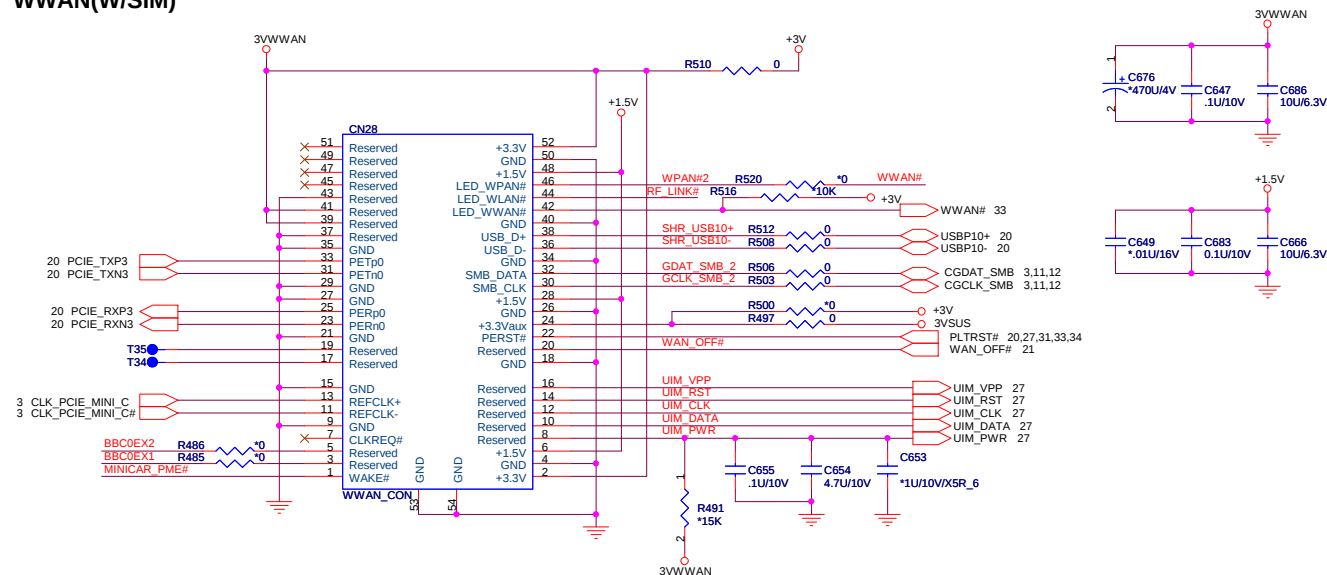


Mini PCI-E Card 1 WLAN

35

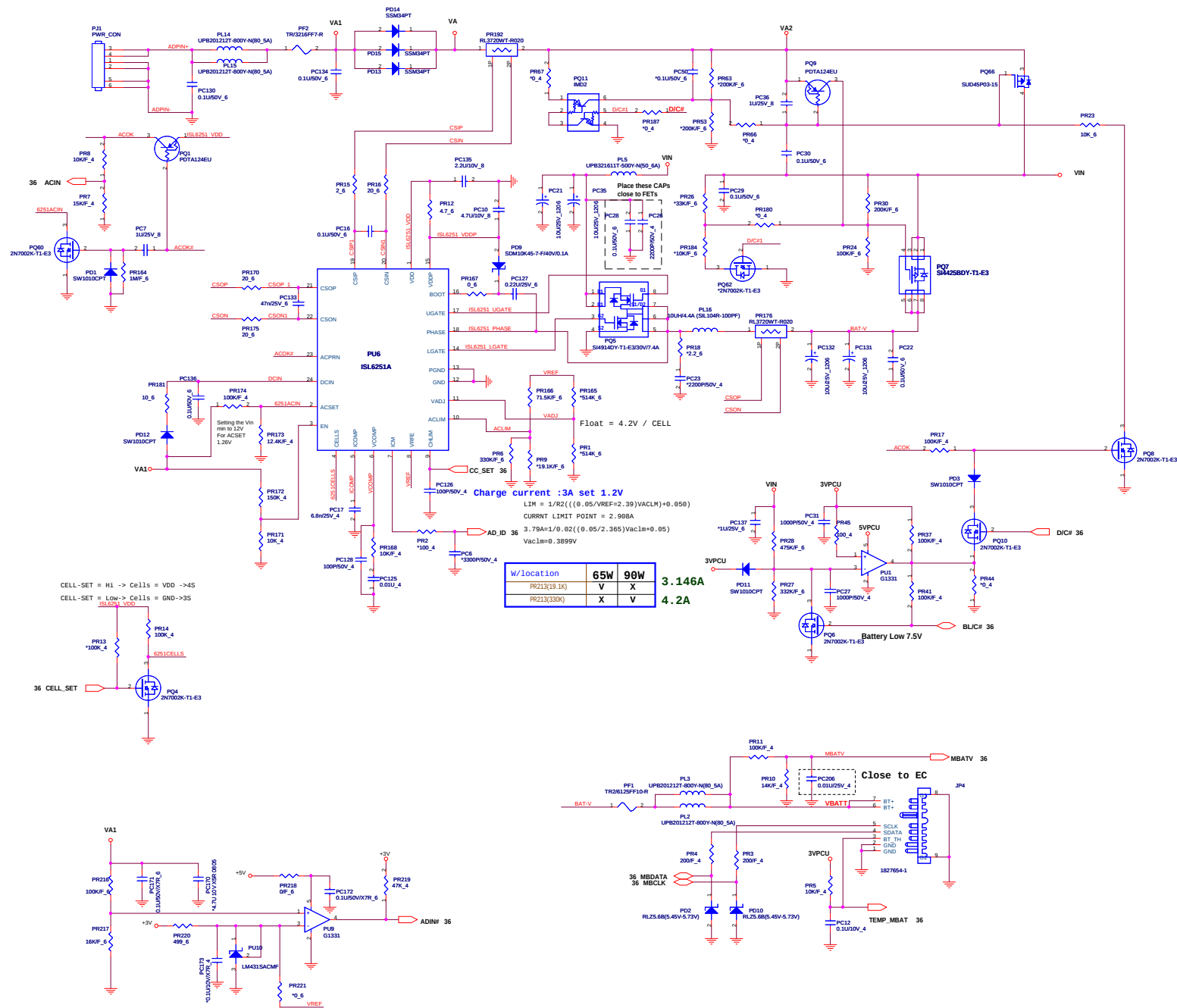


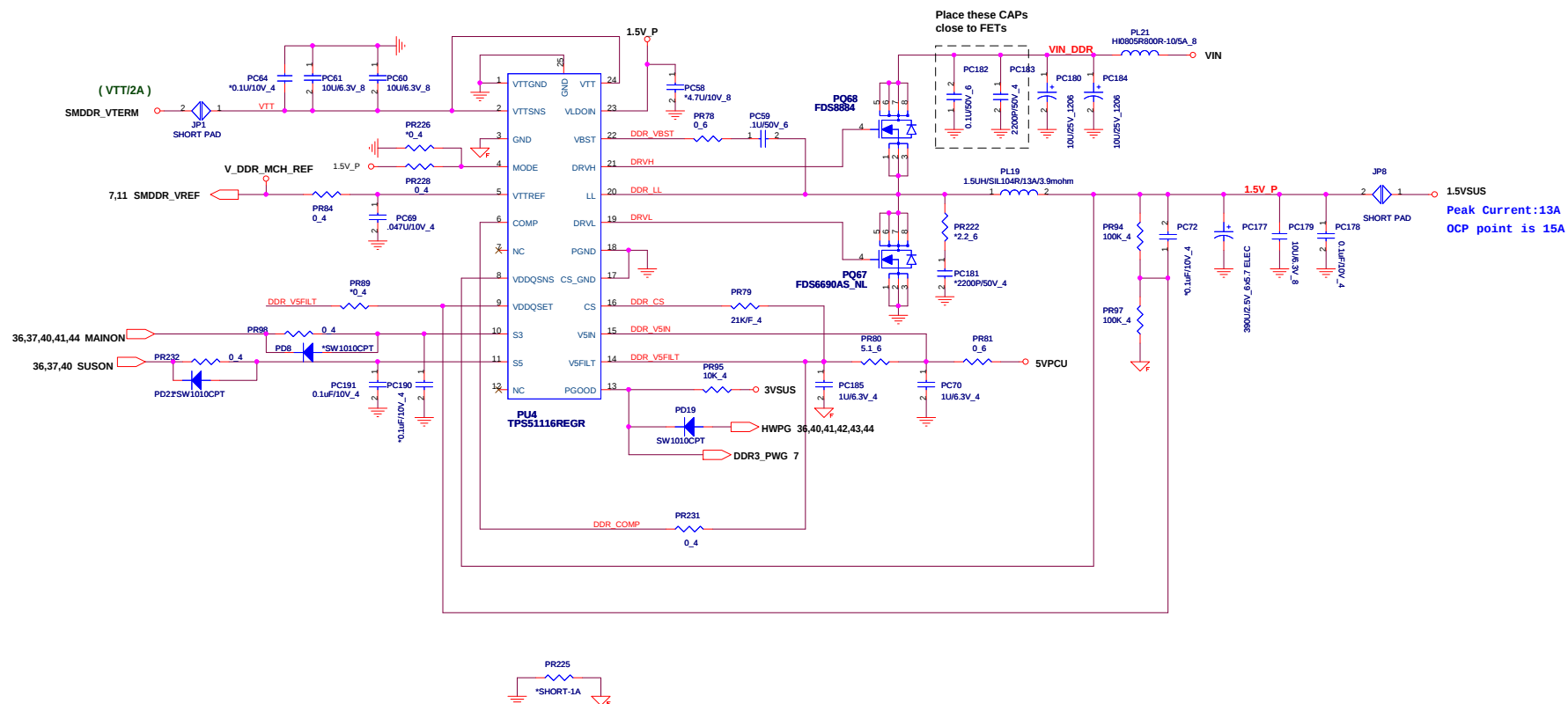
Mini PCI-E Card 2 WWAN(W/SIM)



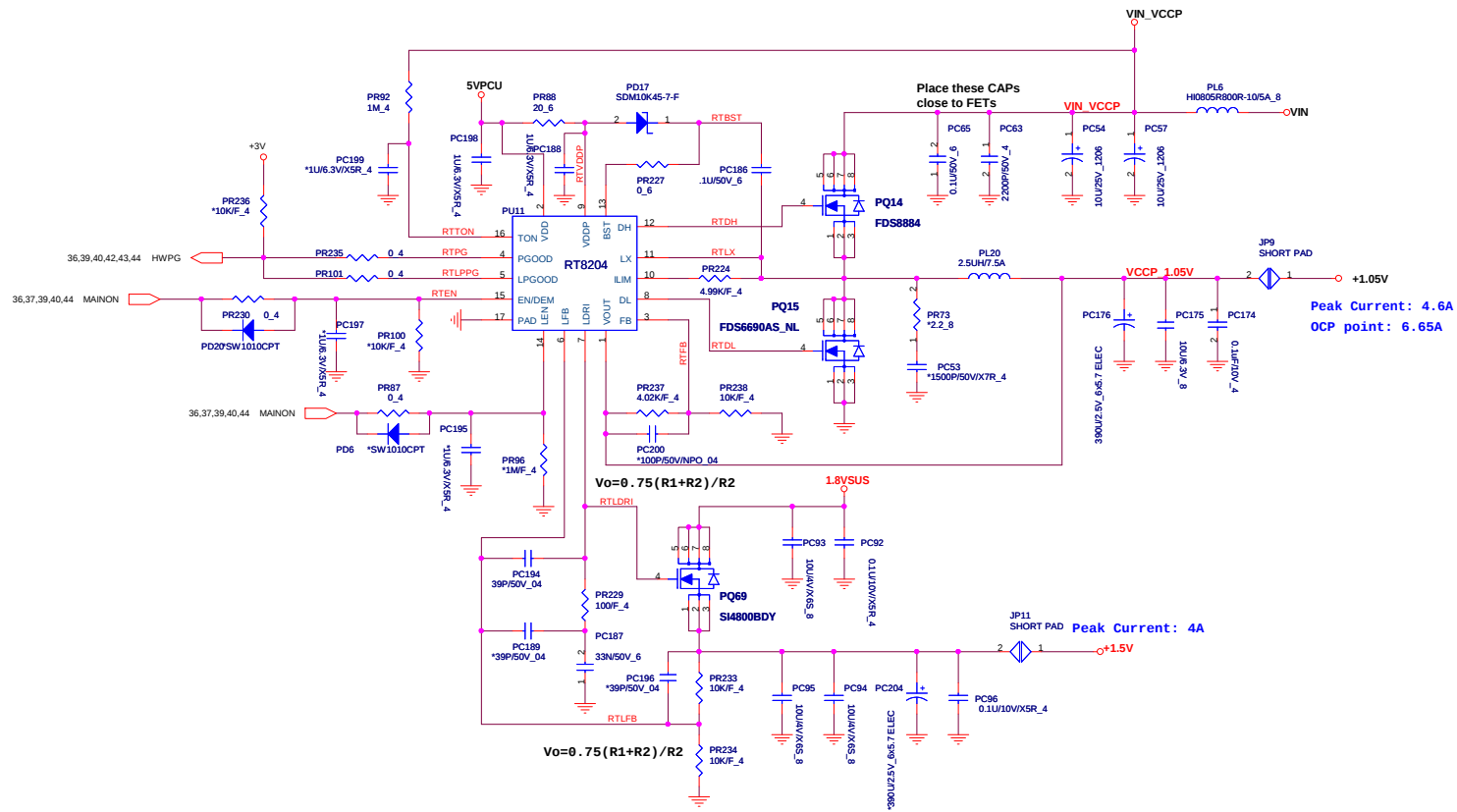


[illegible]





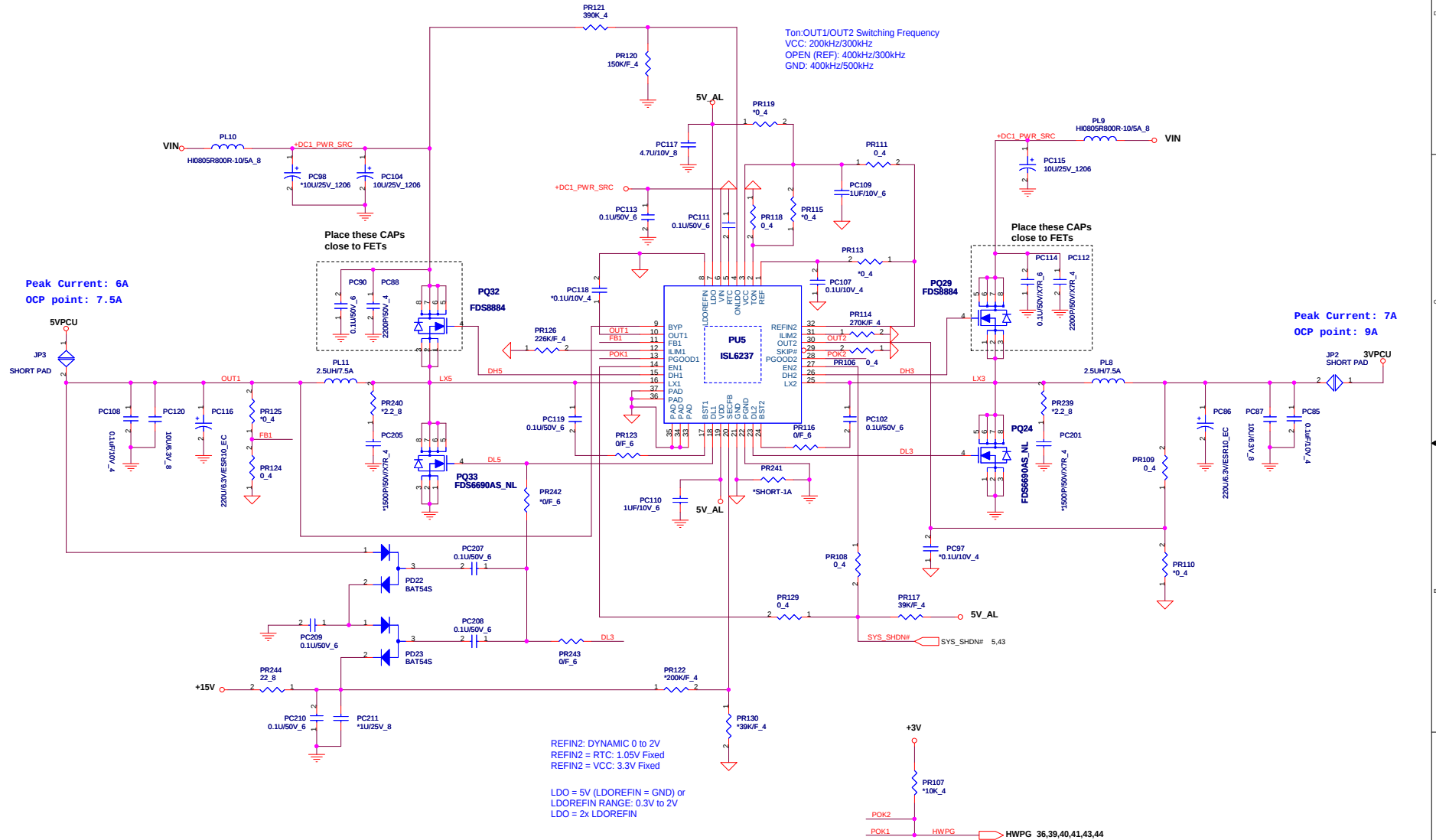




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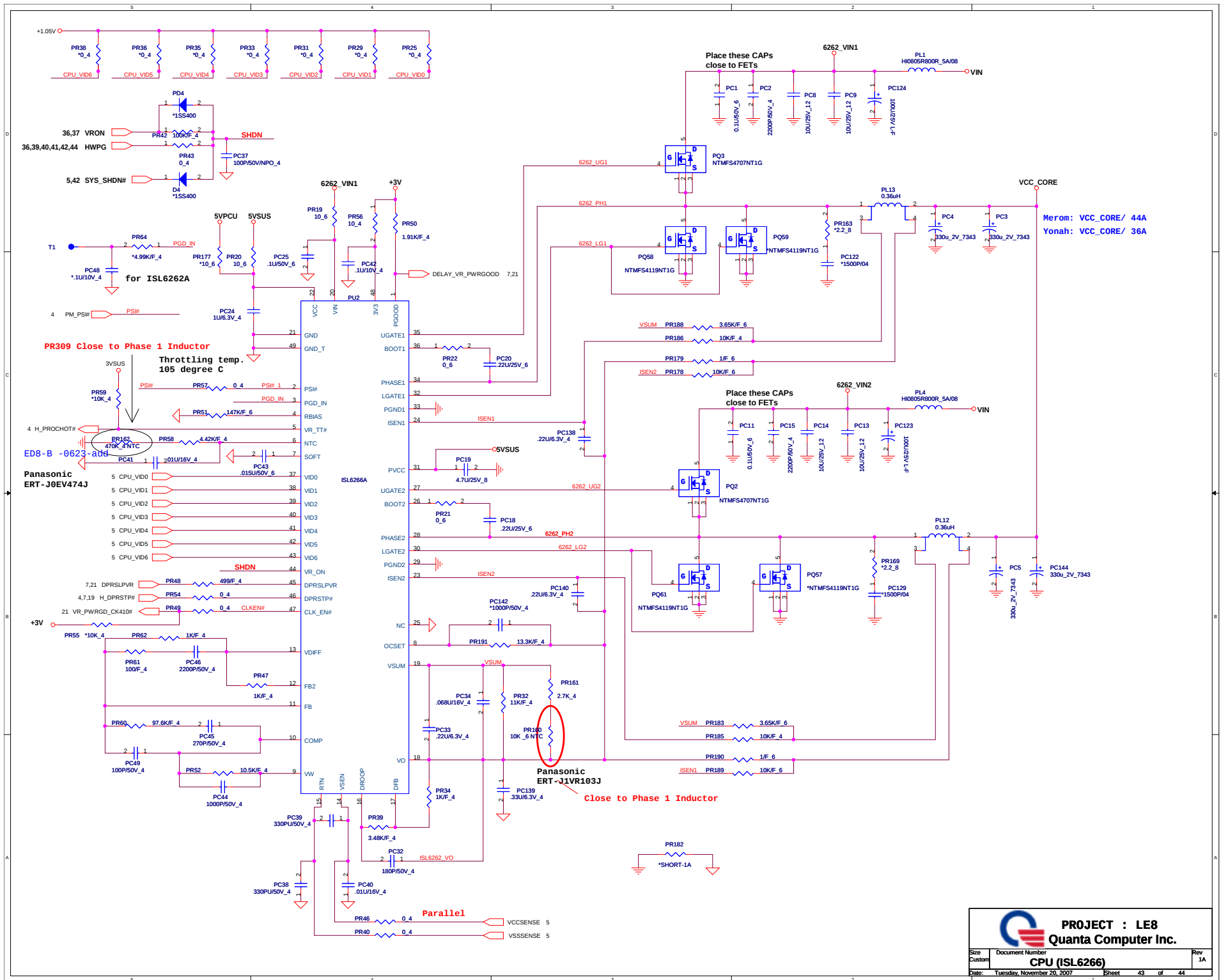
Size	Document Number	Rev
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DC/DC 3VPCU/5VPCU/+15V



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LE8 SYSTEM POWER BLOCK DIAGRAM

