

IGT30

Schematics Document

Mobile Merom uFCPGA with Intel Crestline_GM/PM+ICH8-M core logic

Monday, December 25, 2006

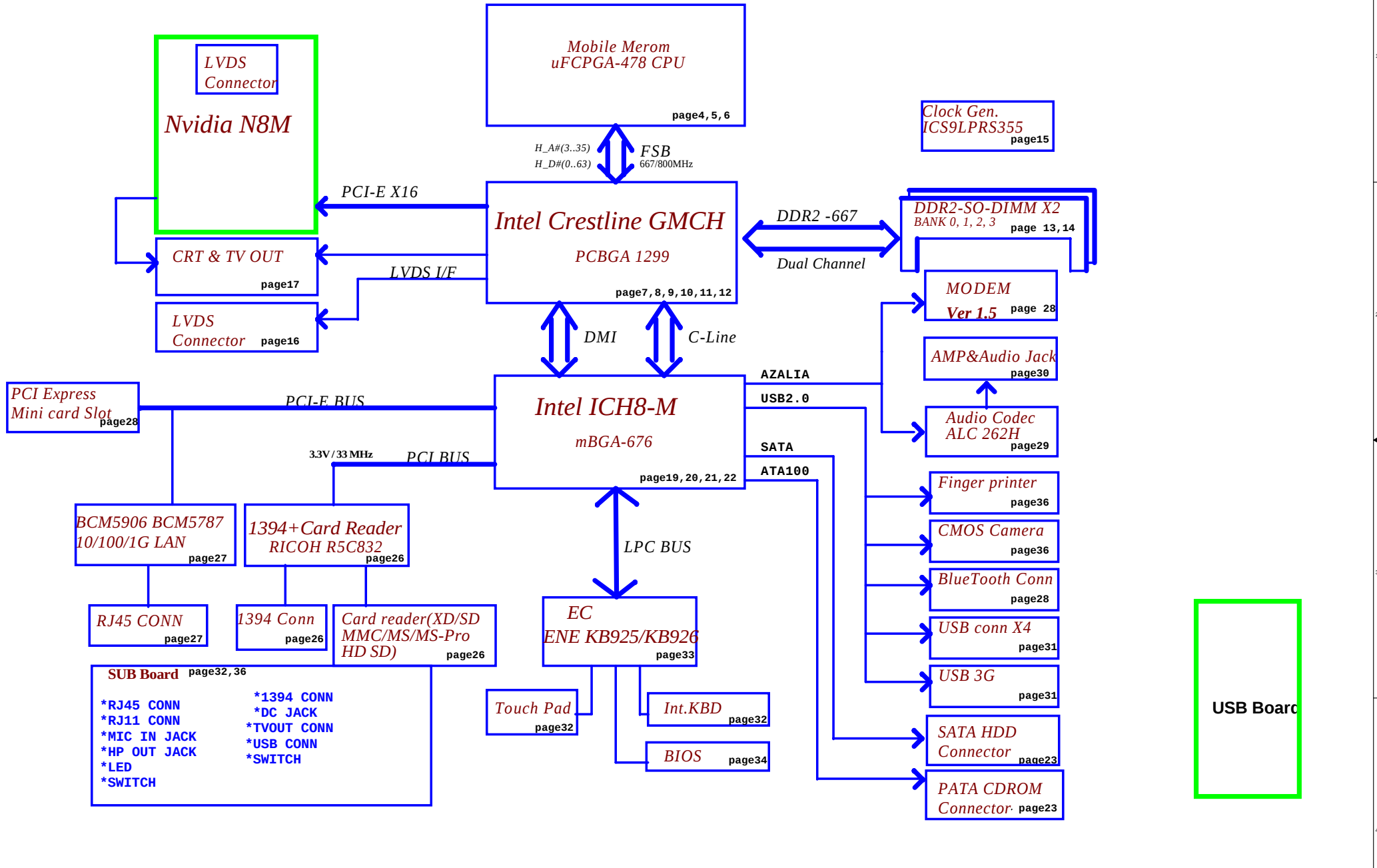
REV:0.1

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				Cover Sheet		
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LEFT SWITCH Board

LEDs Board



USB Board

TP Board

Voltage Rails

0 MEANS ON X MEANS OFF

power plane State	+B LD03 LD05	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	CLOCK
S0	0	0	0	0	0
S3	0	0	0	X	0
S5 S4/AC	0	0	X	X	0
S5 S4/ Battery only	0	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

0 MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

ICH8 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Structure

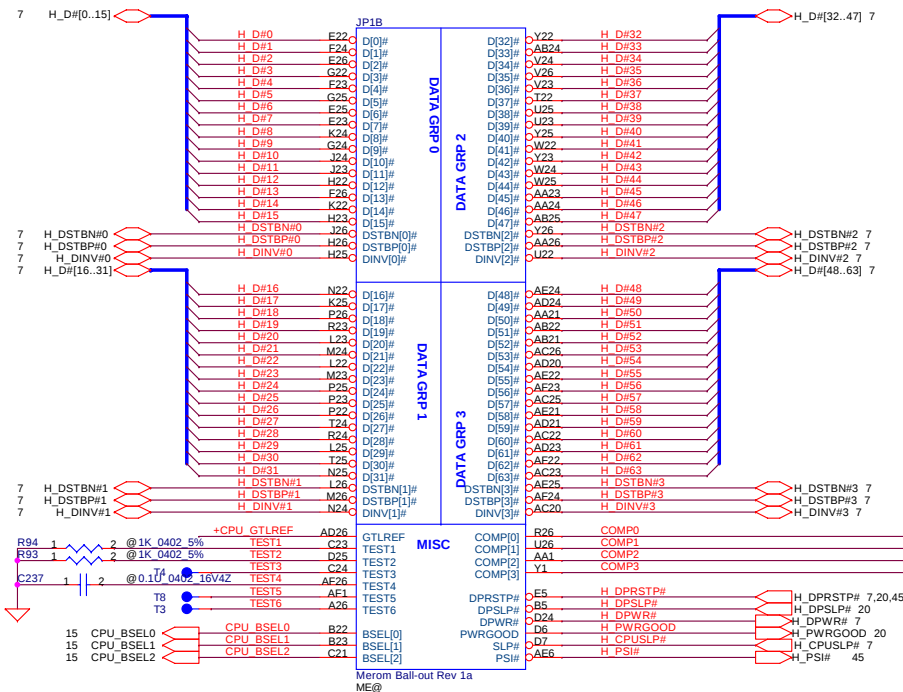
MARK	FUNCTION
@	NC FOR ALL
GIGA@	BCM5787
100@	BCM5906
UMA@	Internal 965GM
VGA@	965PM + Ext VGA

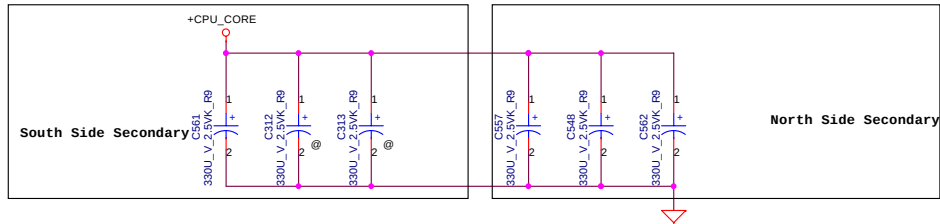
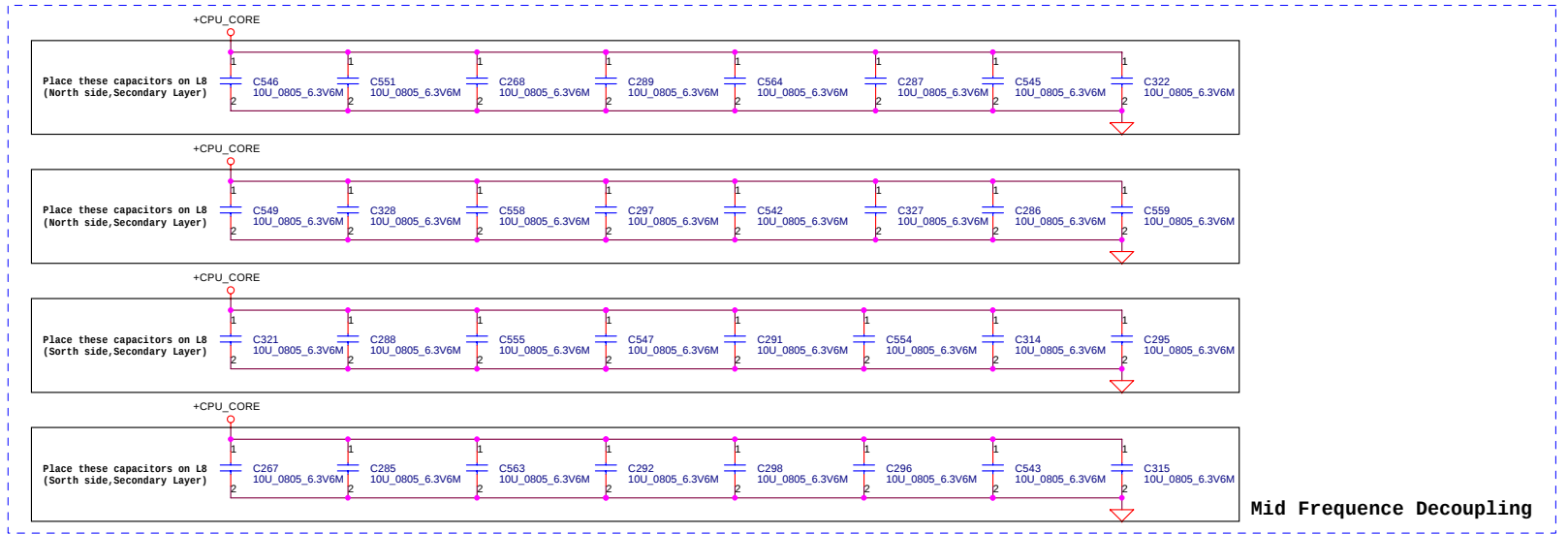
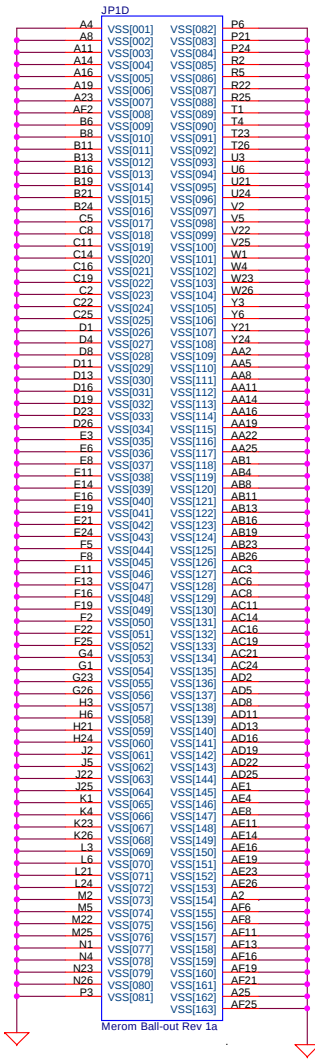
Address

USB PORT LIST

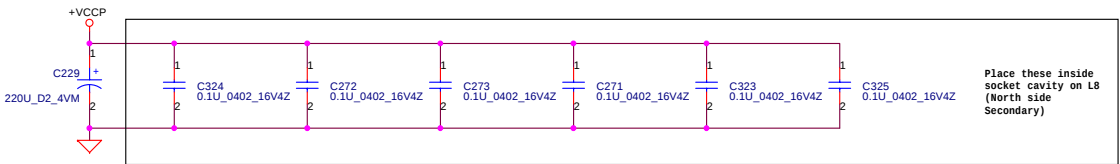
PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	
7	BT(HDL20)
8	
9	3G

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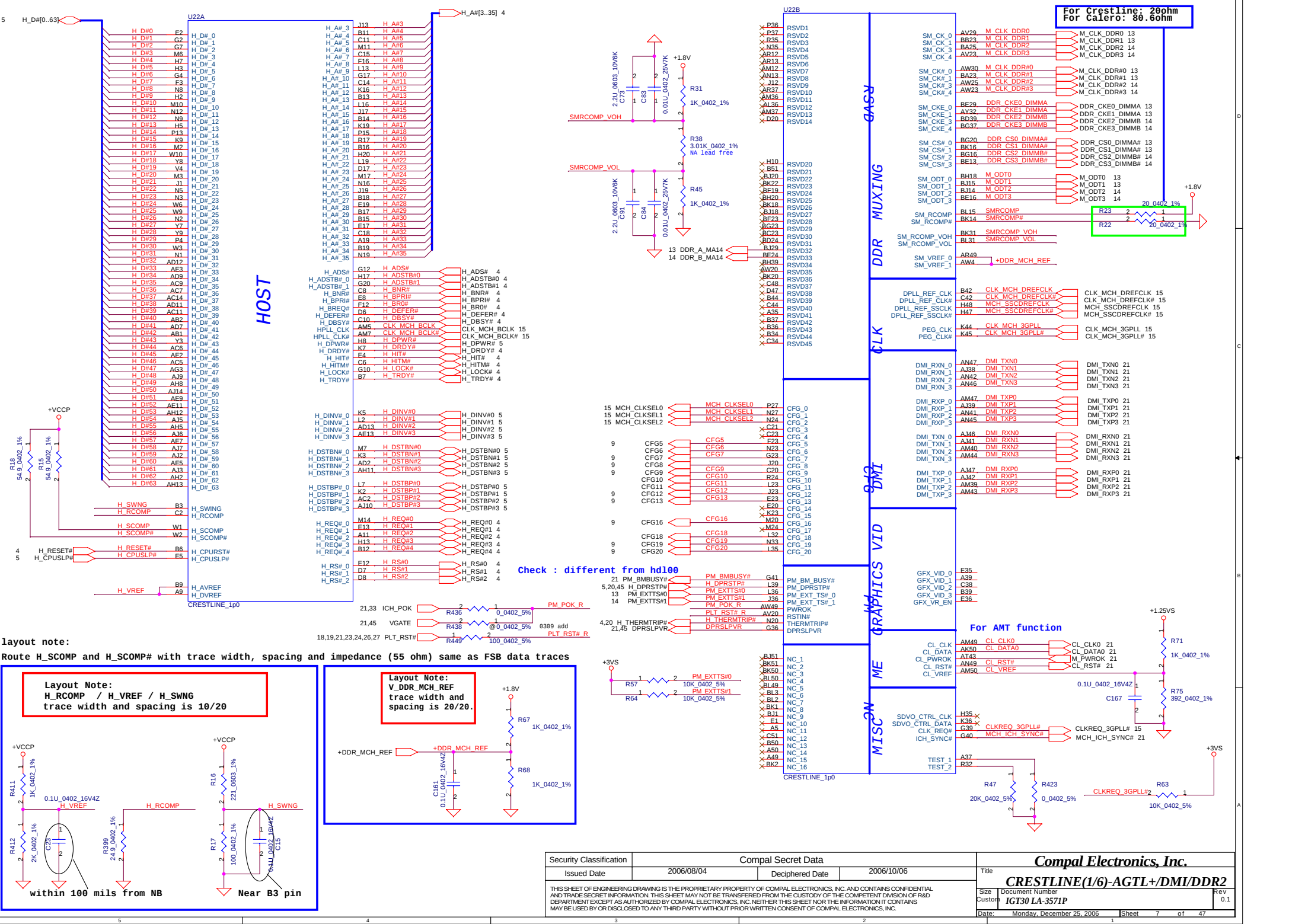




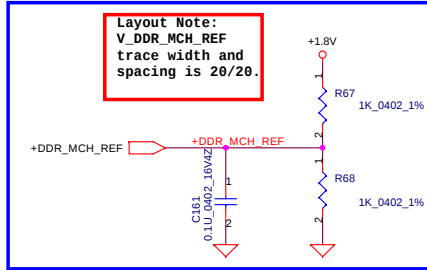
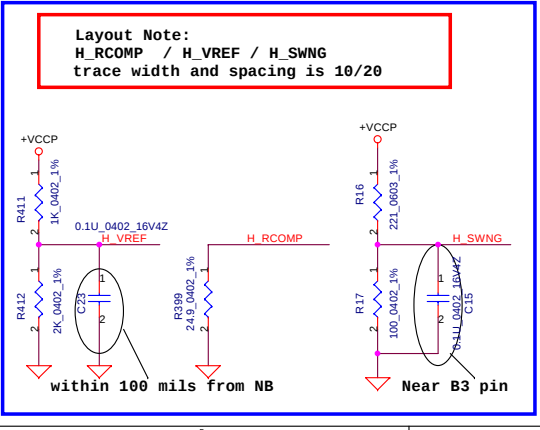
ESR <= 1.5m ohm
Capacitor > 1980uF



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layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



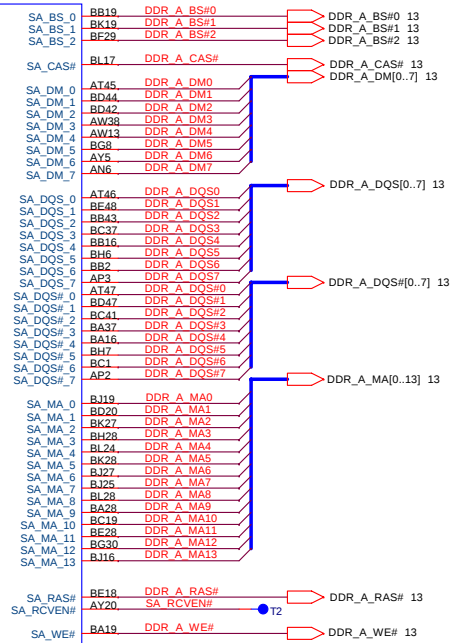
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Title		Compal Electronics, Inc.	
CRESTLINE(1/6)-AGTL+/DMI/DDR2		Rev 0.1	
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13 DDR_A_D[0..63]



DDR SYSTEM MEMORY A

CRESTLINE_1p0

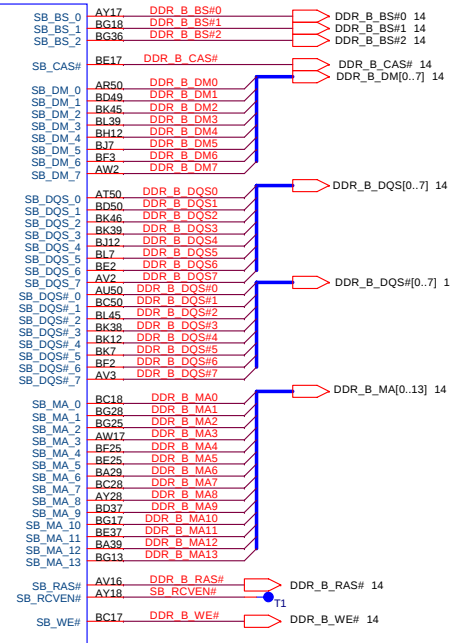


14 DDR_B_D[0..63]



DDR SYSTEM MEMORY B

CRESTLINE_1p0

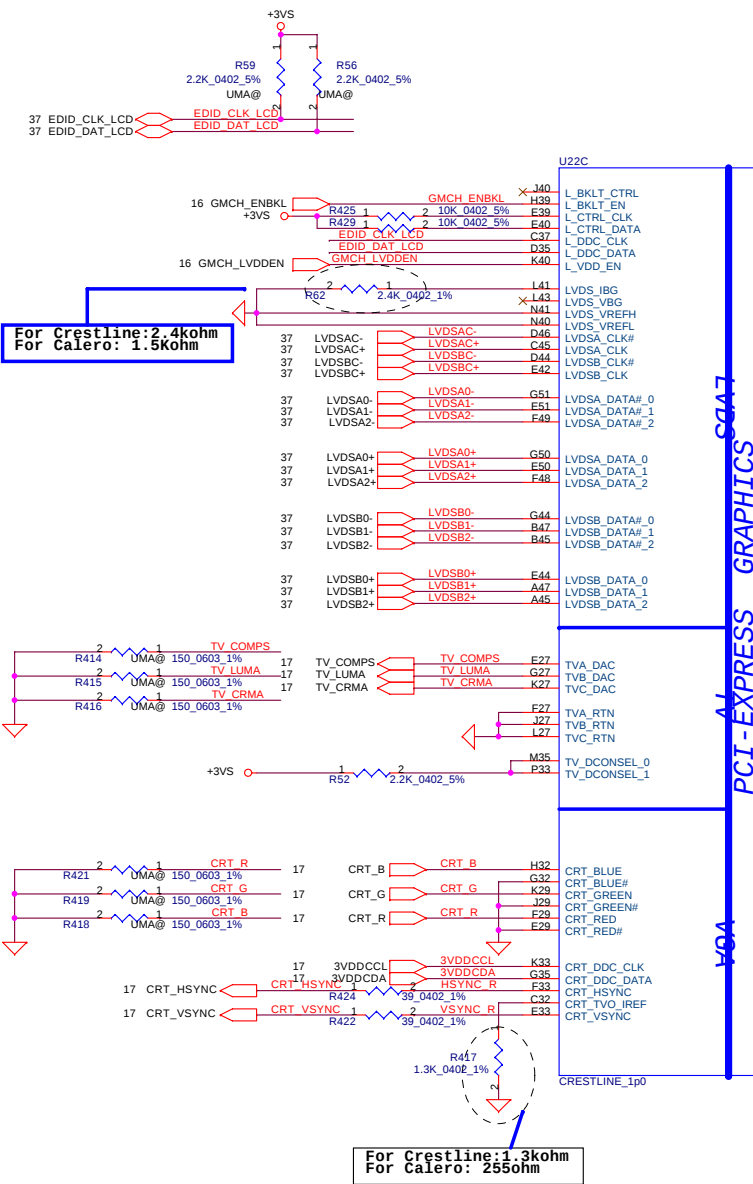


Compal Electronics, Inc.

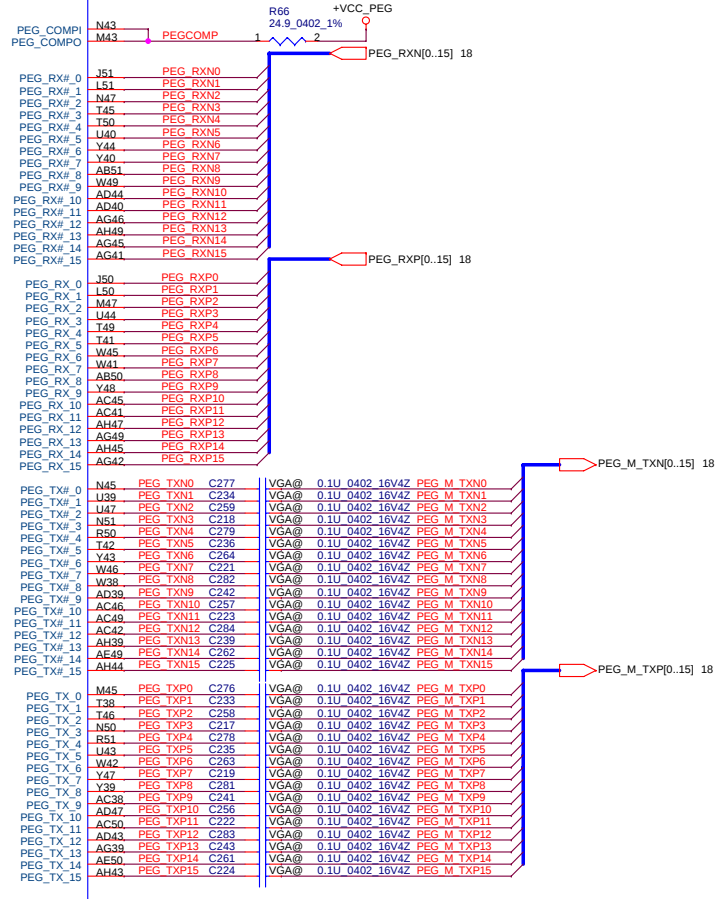
CRESTLINE((2/6)-DDR2 A/B CH

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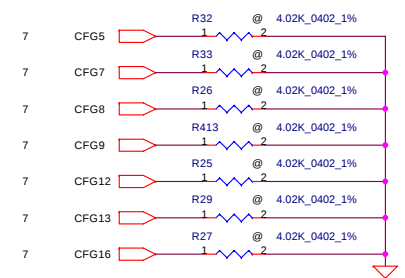


PEGCOMP trace width and spacing is 20/25 mils.

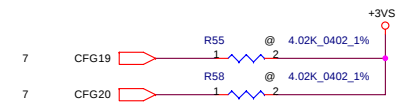


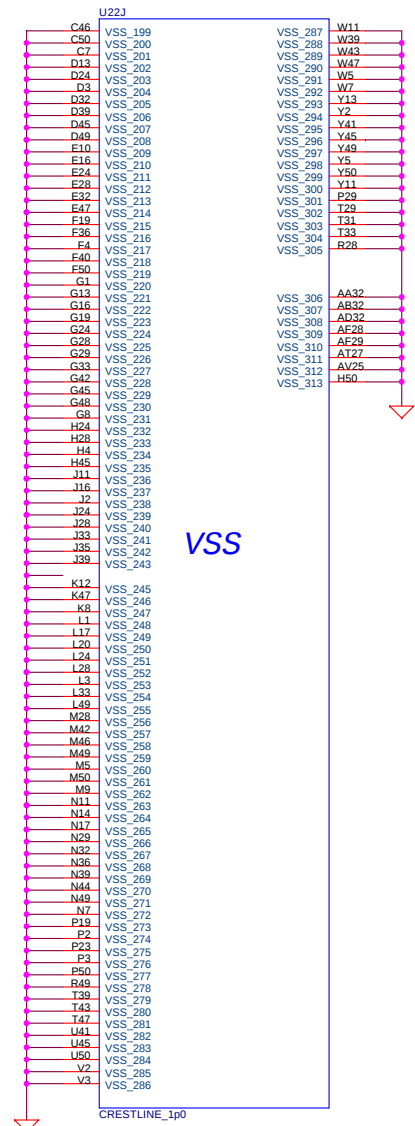
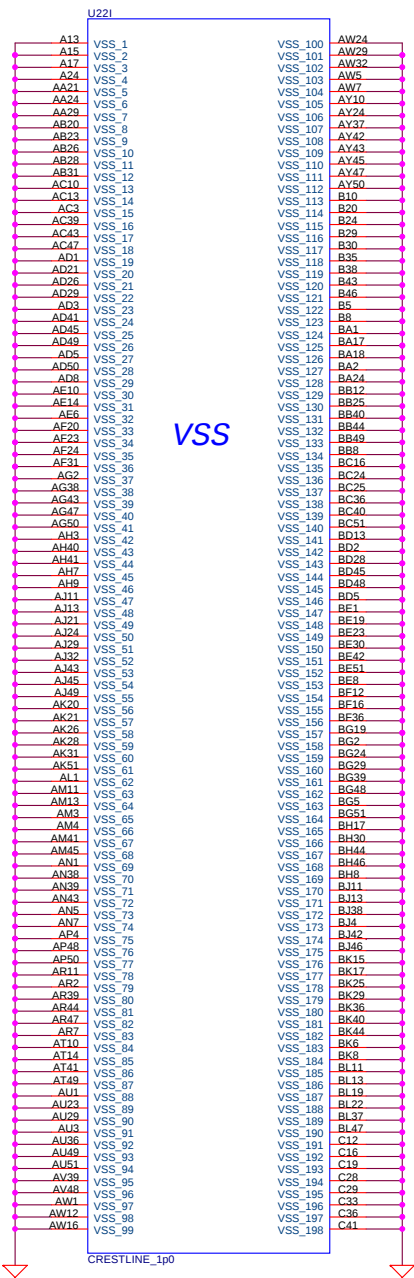
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = XOR 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

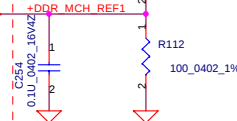
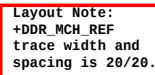


CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

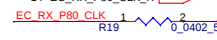




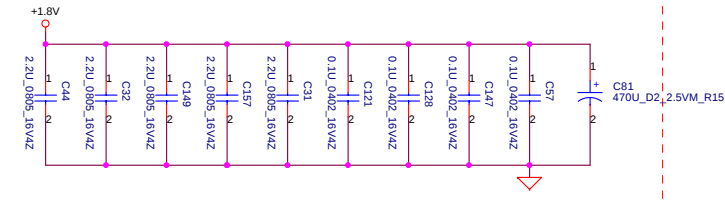
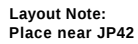
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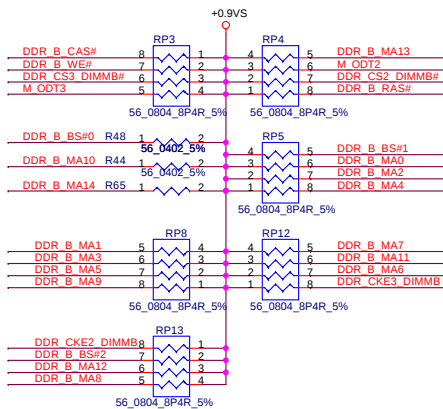
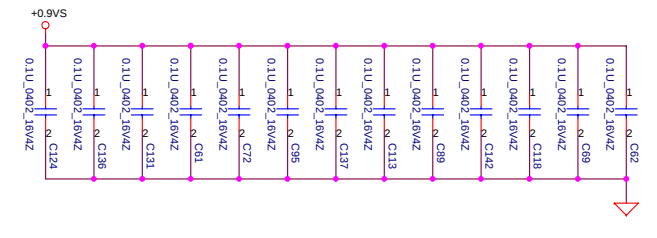
Layout Note:
Place these resistor
closely JP41,all
trace length Max=1.5"



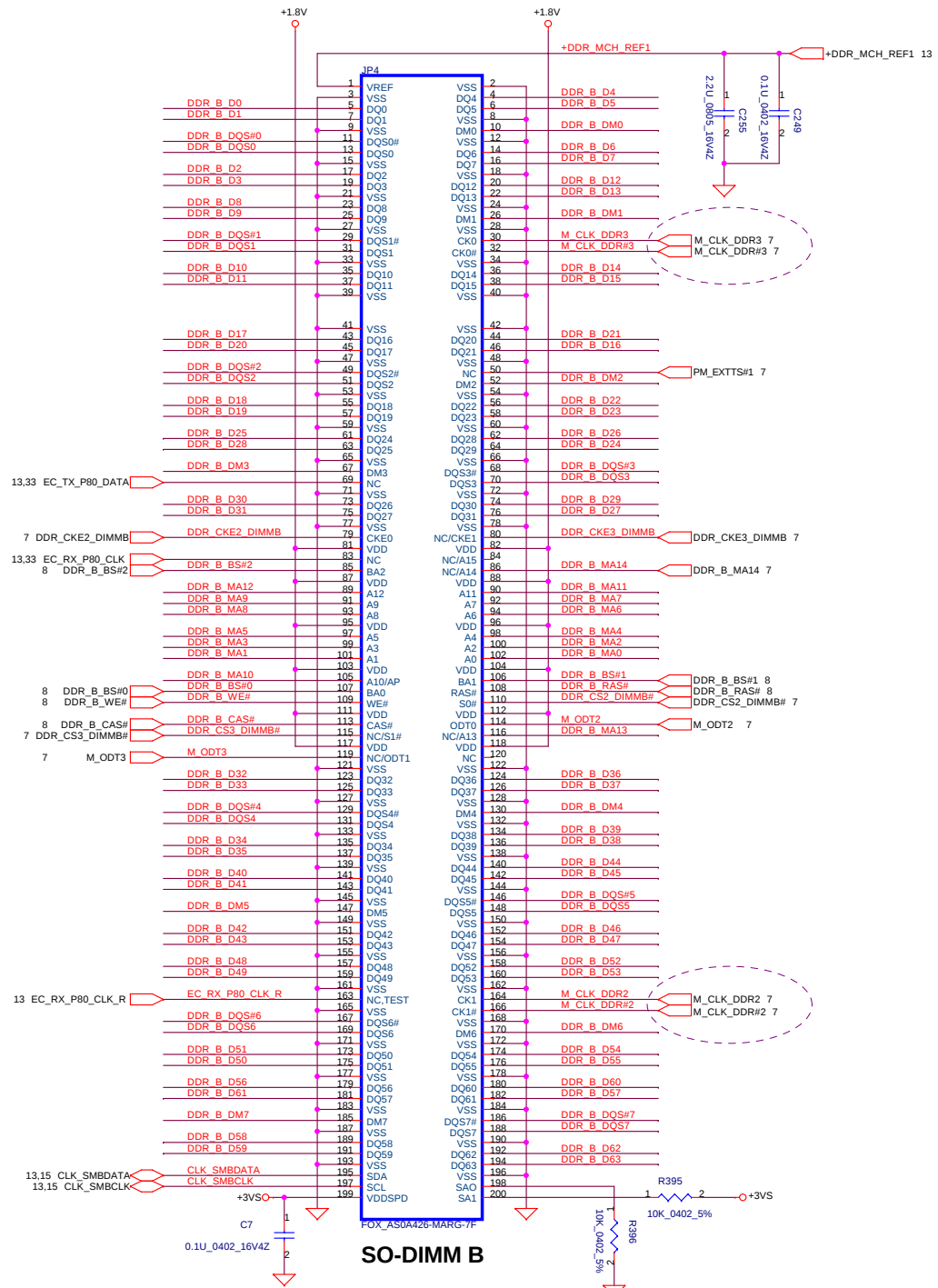
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Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"

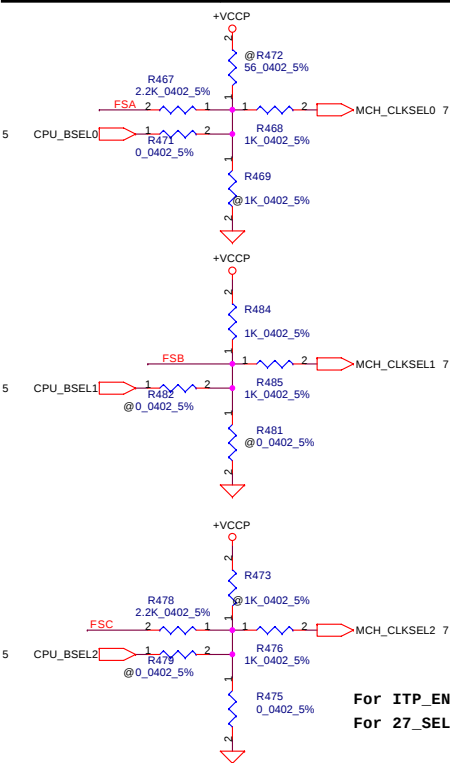


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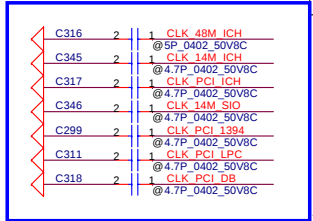
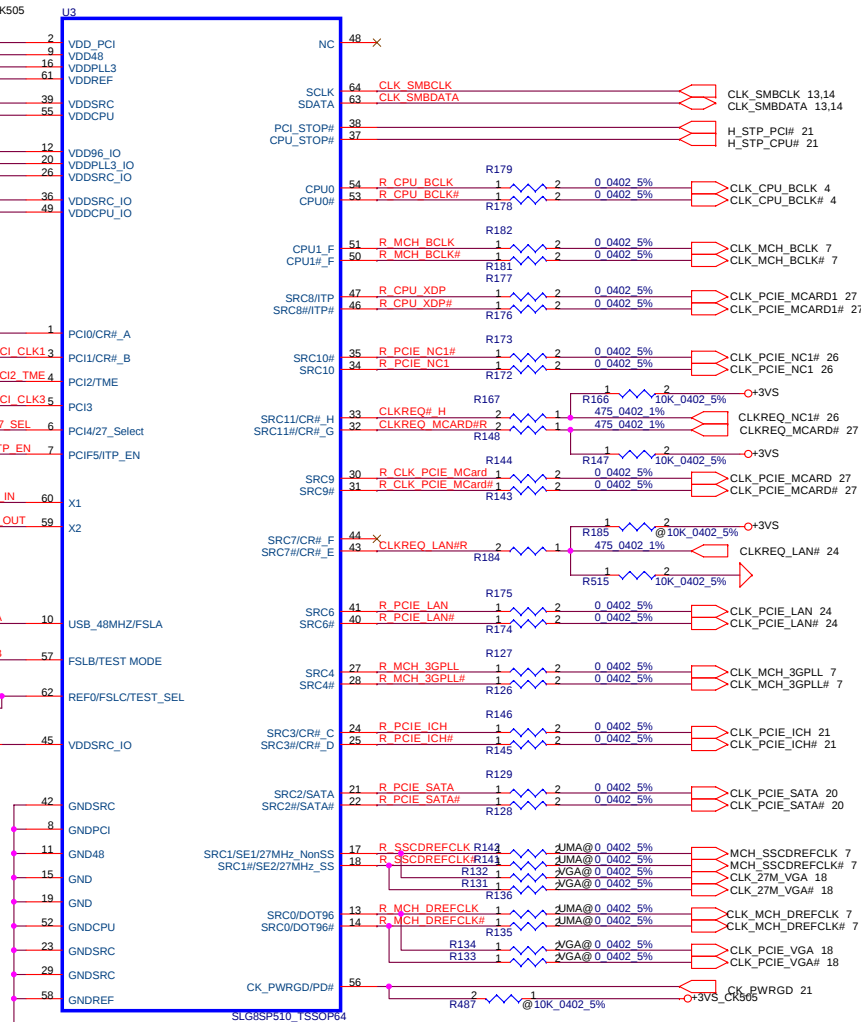
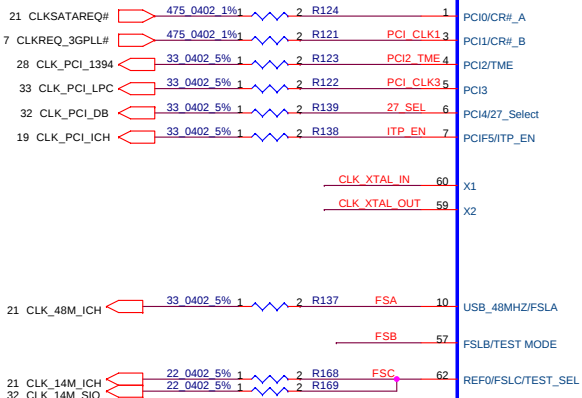
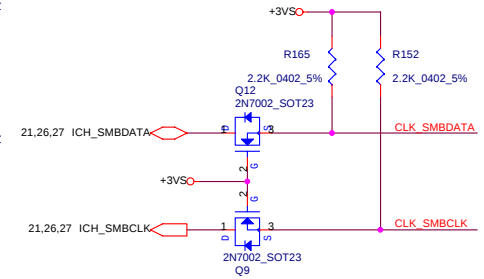
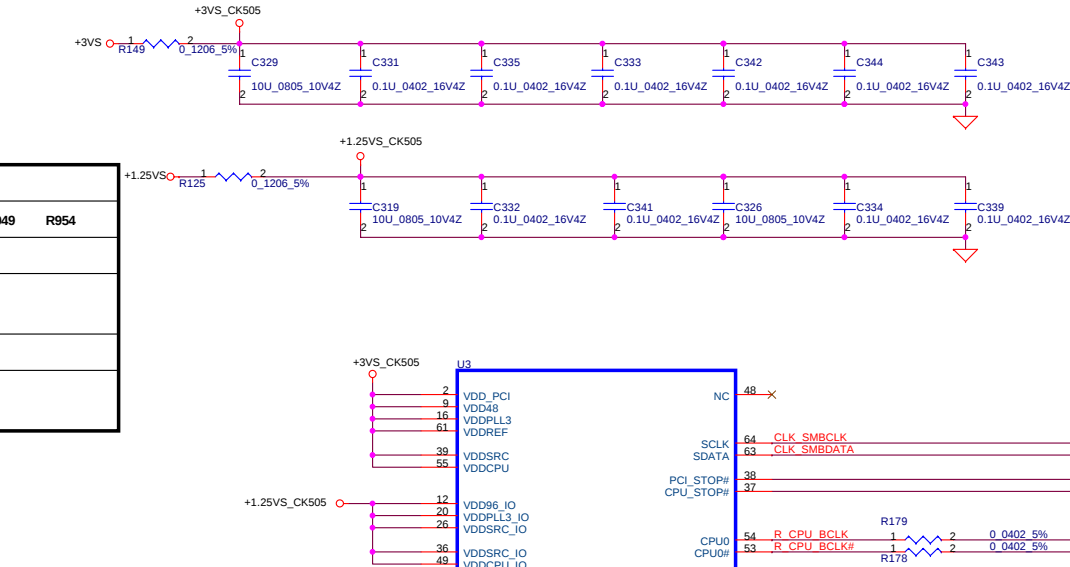
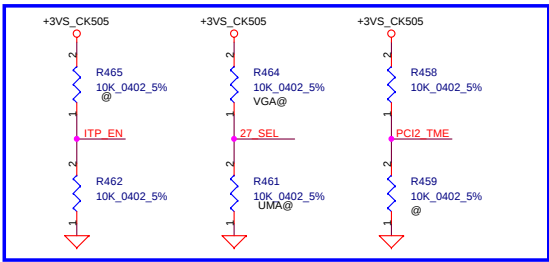
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R919	R940	R956
*(Default)	No Stuff	R914	R921	R930
		R943	R949	R954
667MHZ	Stuff	R959	R930	R914
	No Stuff	R919	R940	R956
		R949	R943	R921
800MHZ	Stuff	R959	R930	R921
	No Stuff	R919	R940	R956
		R949	R943	R914

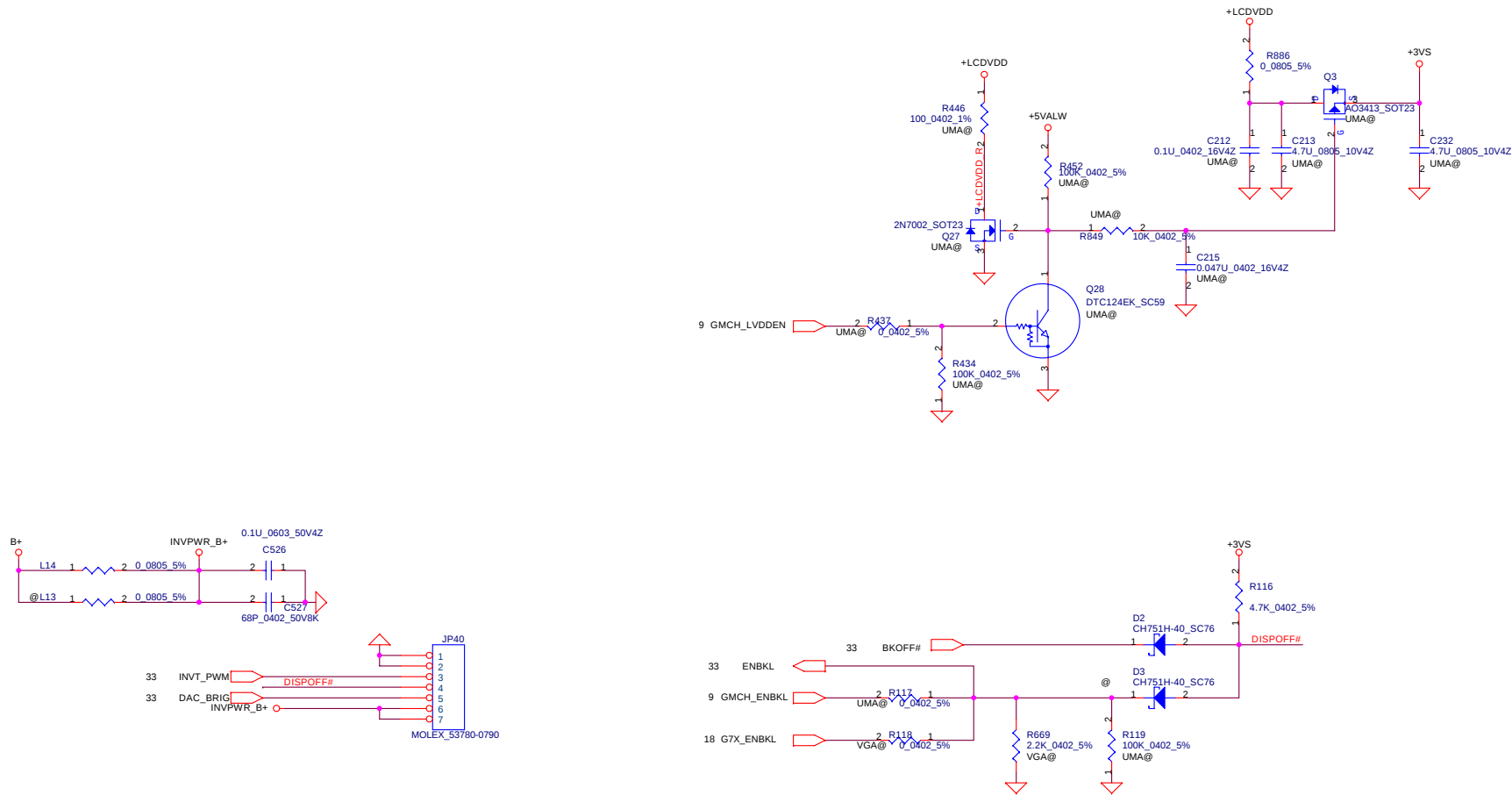


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

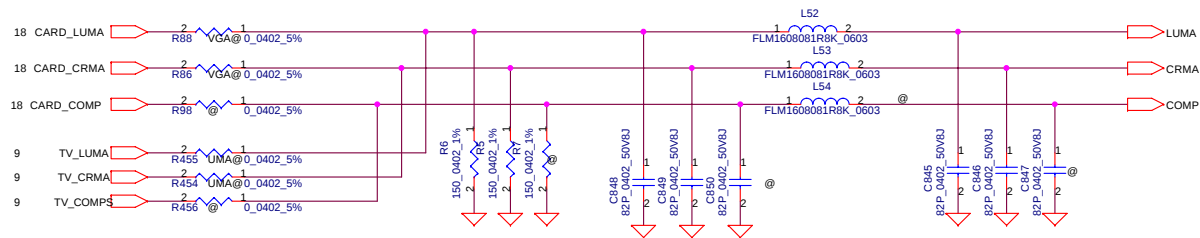


Place close to U41

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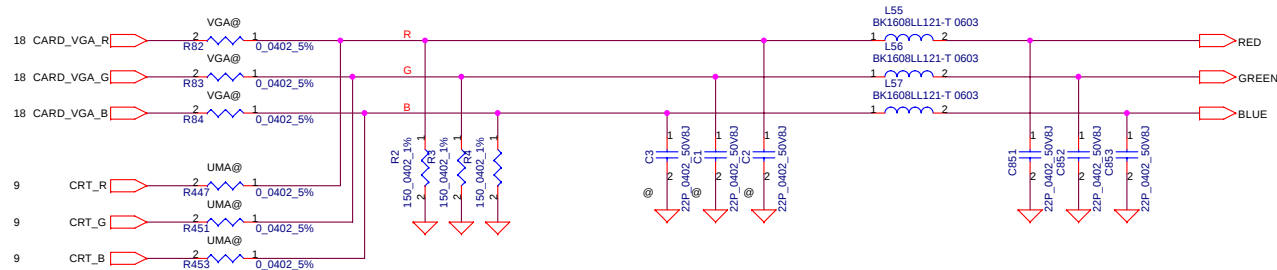


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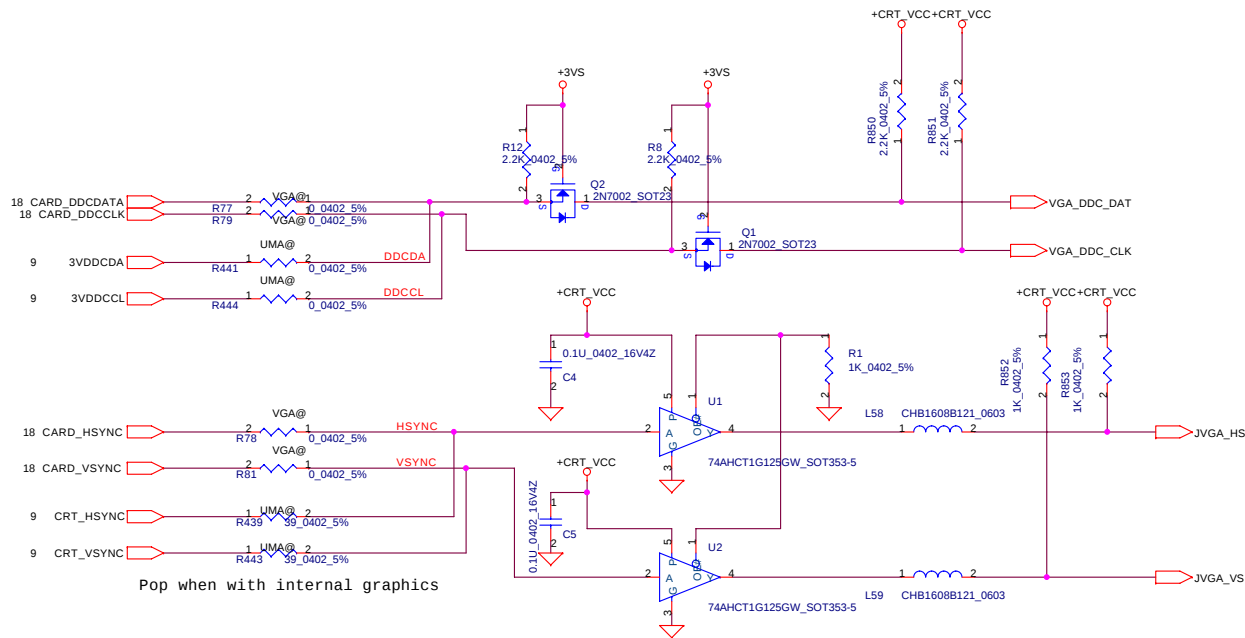


Pop when with internal graphics

CRT Conn.



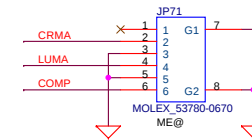
Pop when with internal graphics



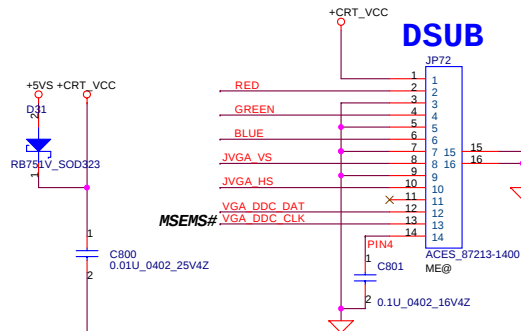
Pop when with internal graphics

VGA I/O PORT Connector

S-VIDEO

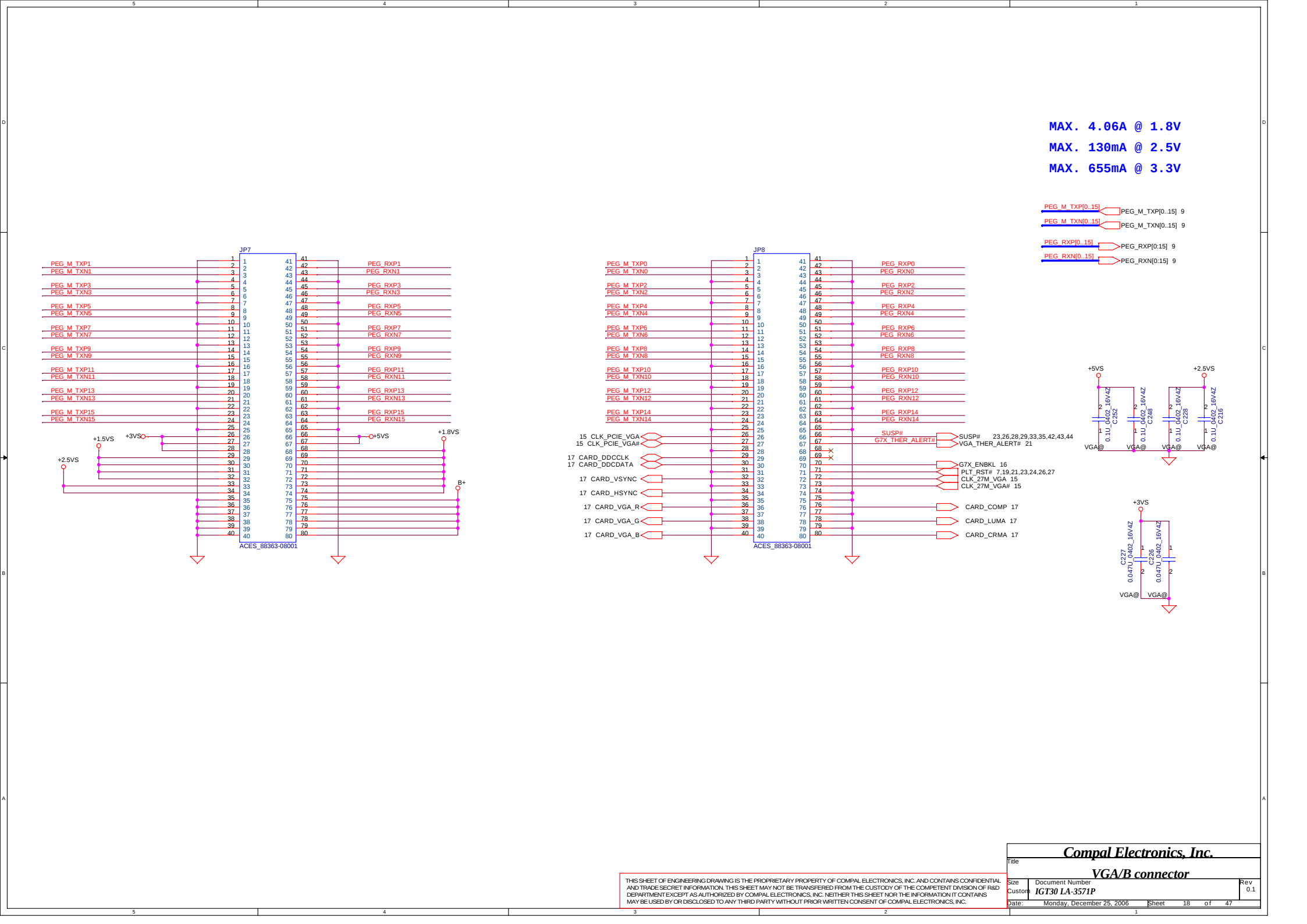


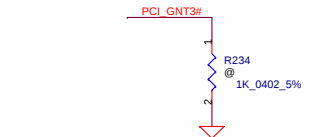
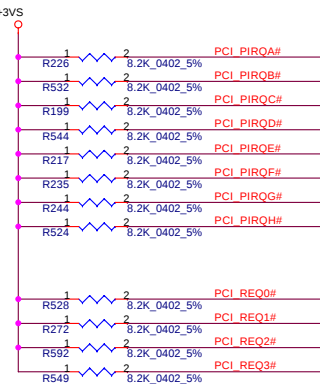
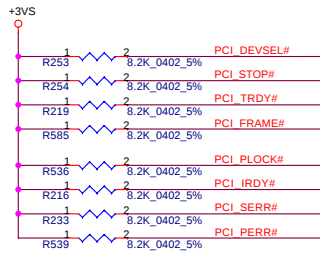
DSUB



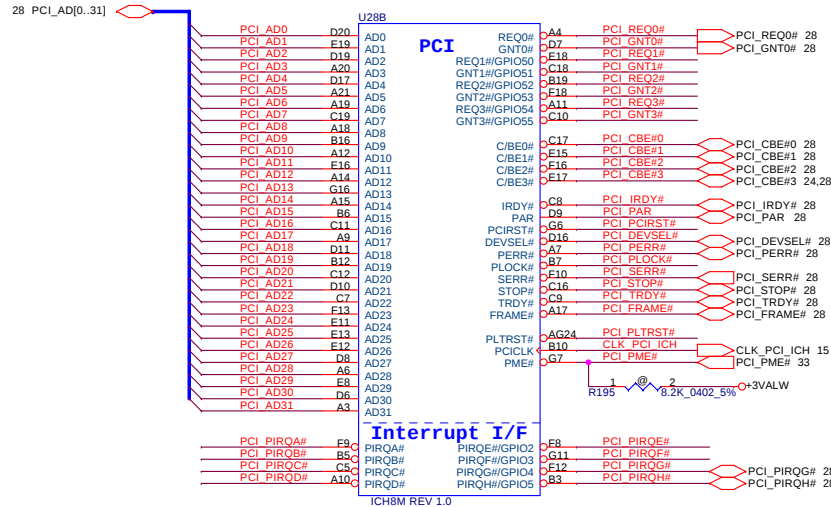
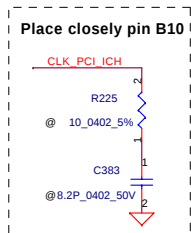
PIN ASSIGMENT

PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYS			
9	10	GND			
10	13	HSYS			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

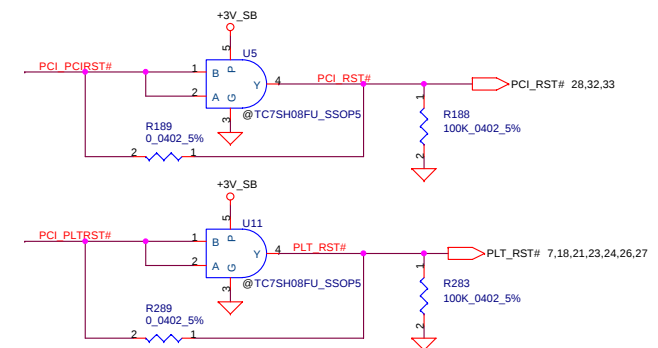
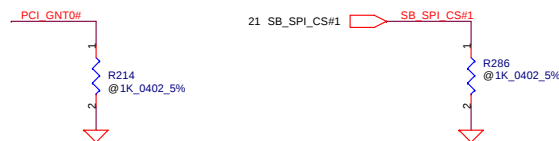




A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

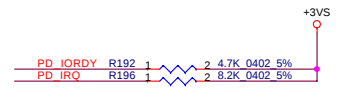
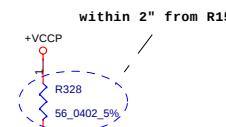
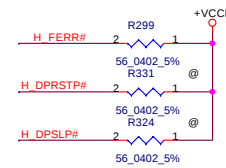
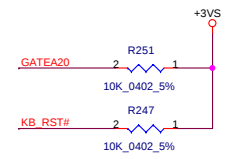


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

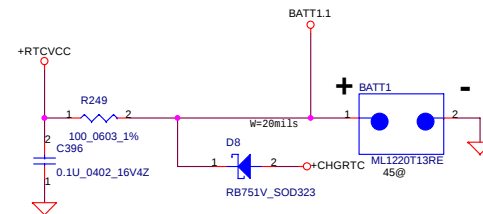
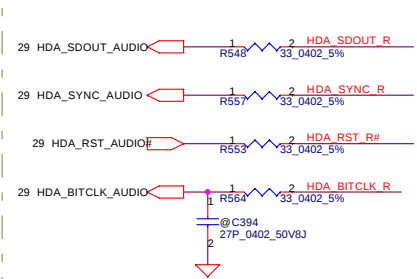


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				19	IGT30 LA-3571P
				Date	Monday, December 25, 2006
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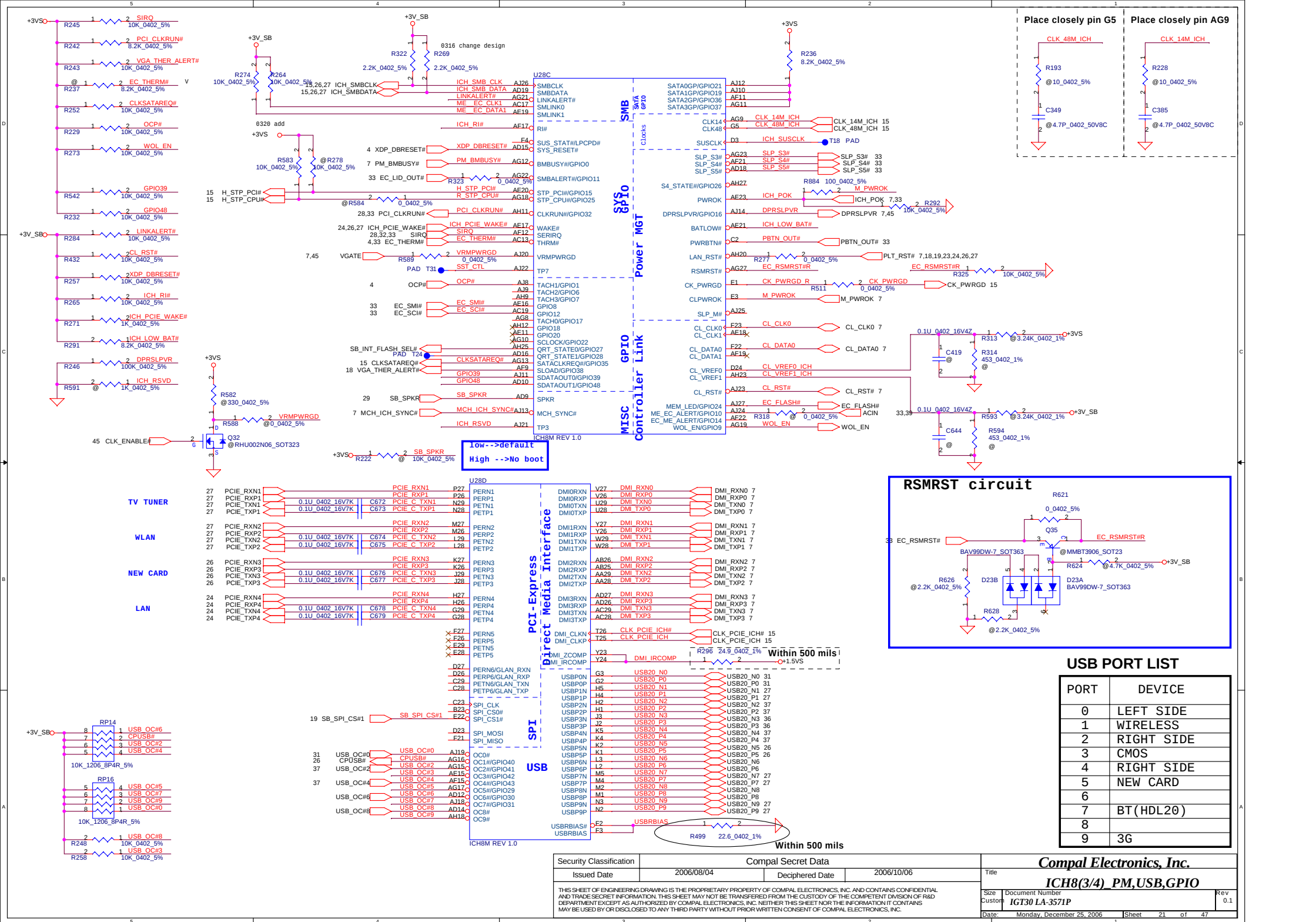
LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_INTVRMEN	

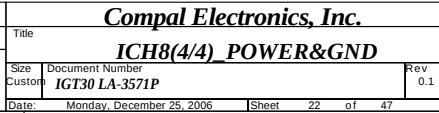


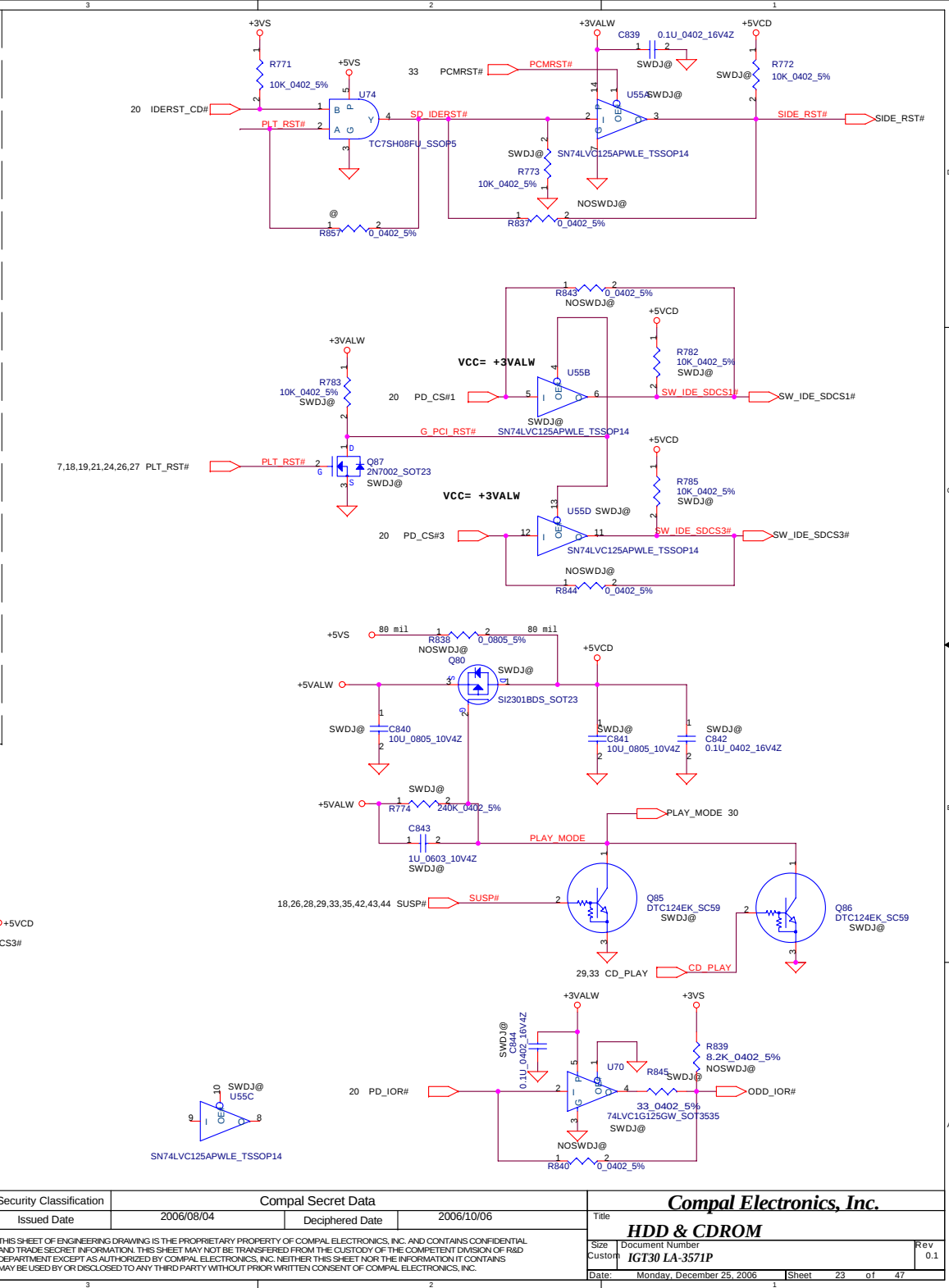
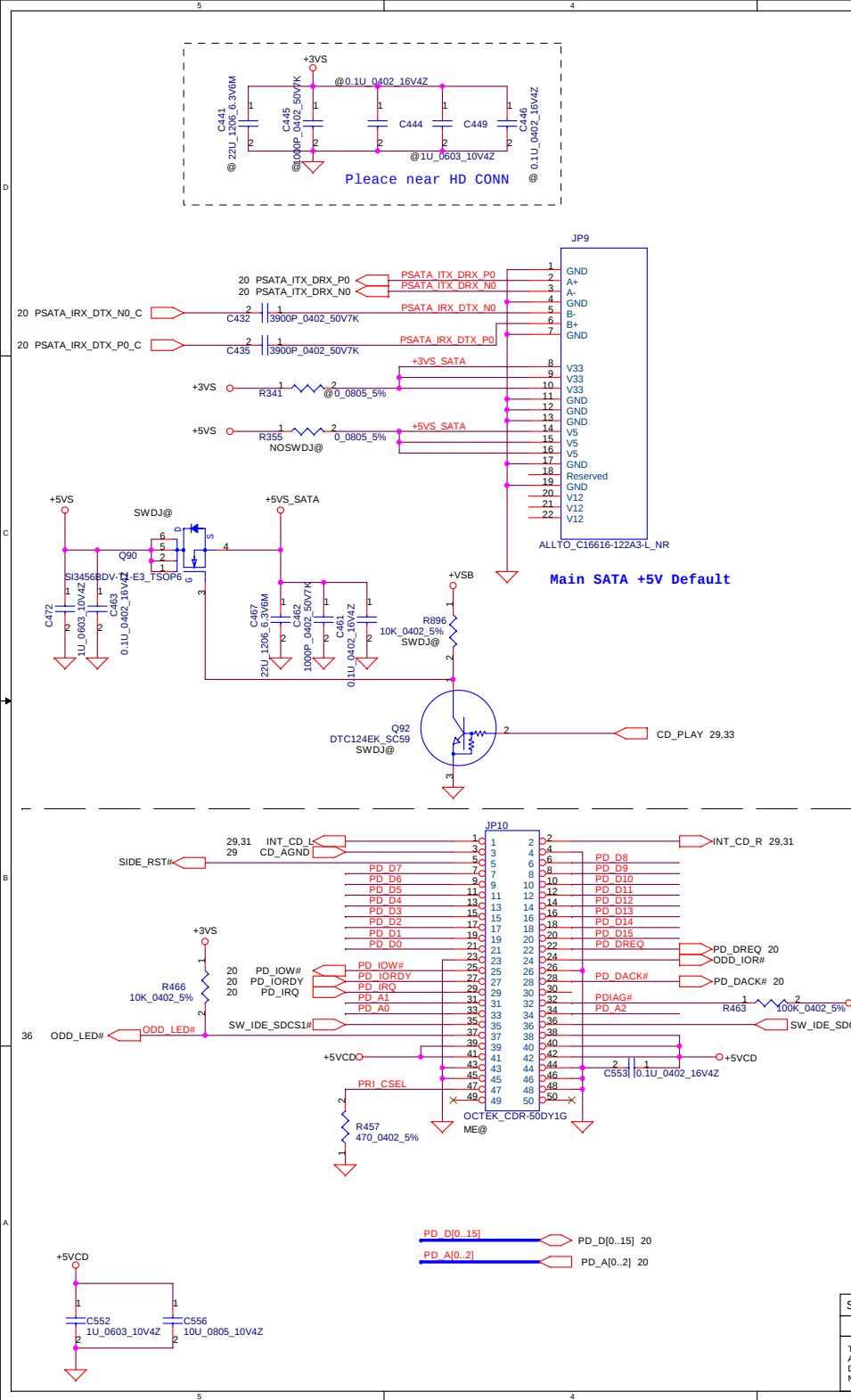
Close to ICH



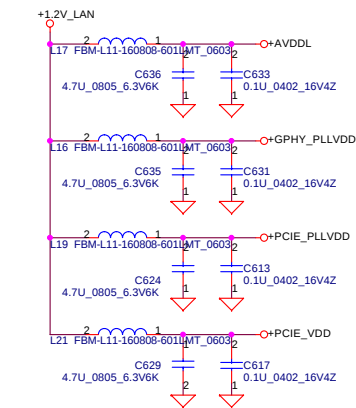
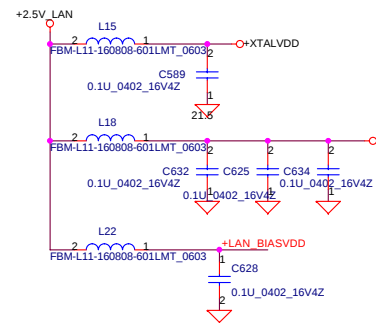
Security Classification		Compal Secret Data		Compal Electronics, Inc. ICH8(2/4)_LAN,HD,IDE,LPC	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	
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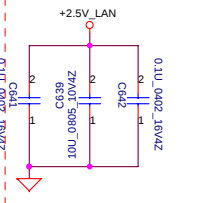




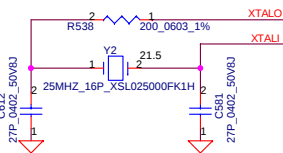
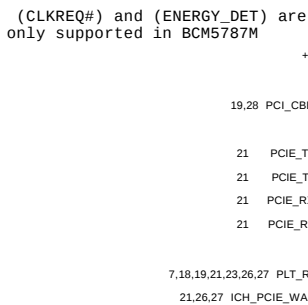
Layout Notice : Filter place as close chip as possible.



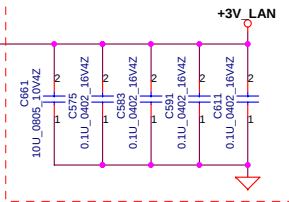
Layout Notice : Place as close chip as possible.



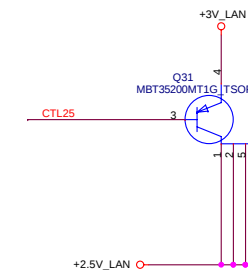
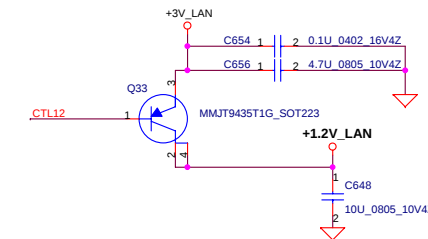
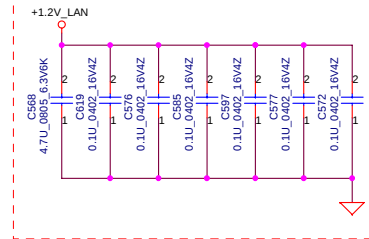
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



Layout Notice : Place as close chip as possible.

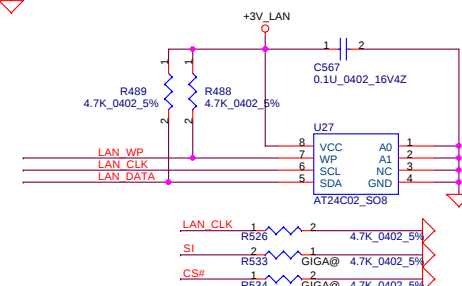


Layout Notice : 1.2V filter. Place as close chip as possible.

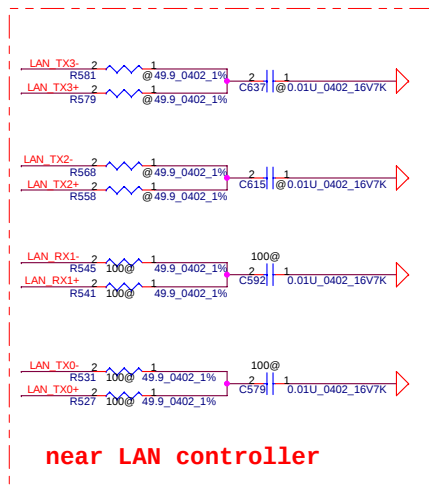
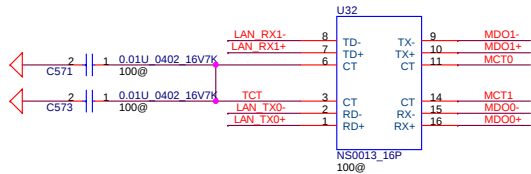
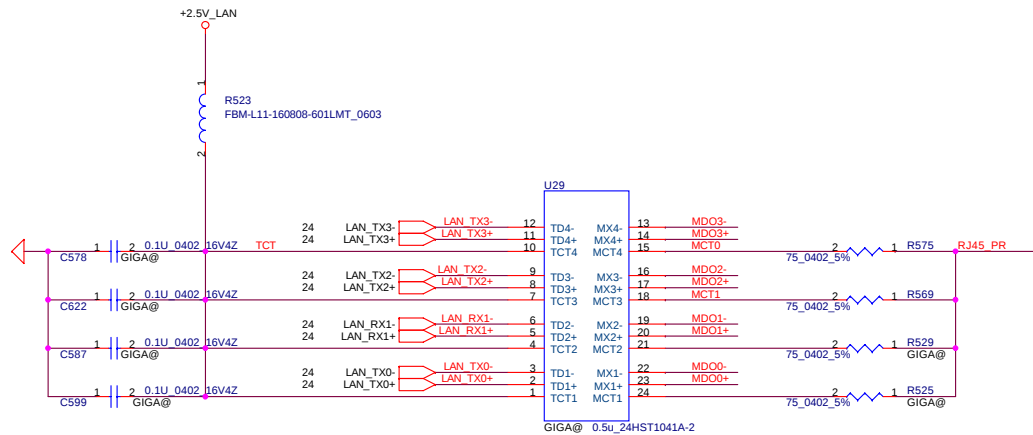


Notice : 4.7u 6.3V capacitor Thickness 1.25mm

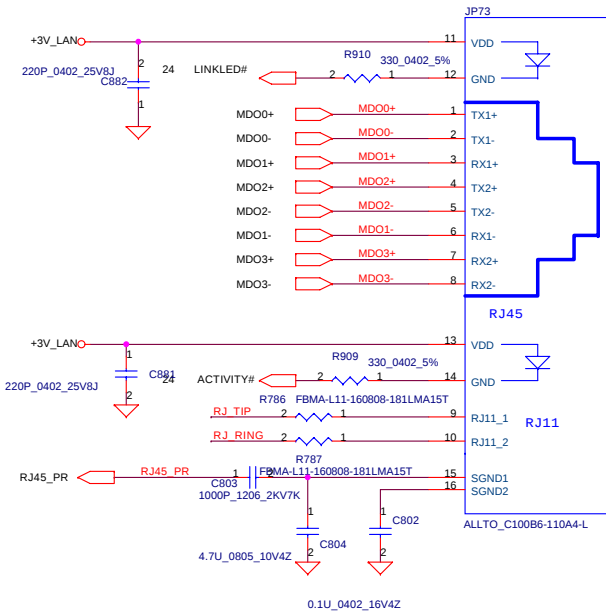
Layout Notice : Filter place as close chip as possible.



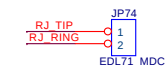
Security Classification	Compal Secret Data			Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	BCM5787MKML	
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RJ11+RJ45 CONN

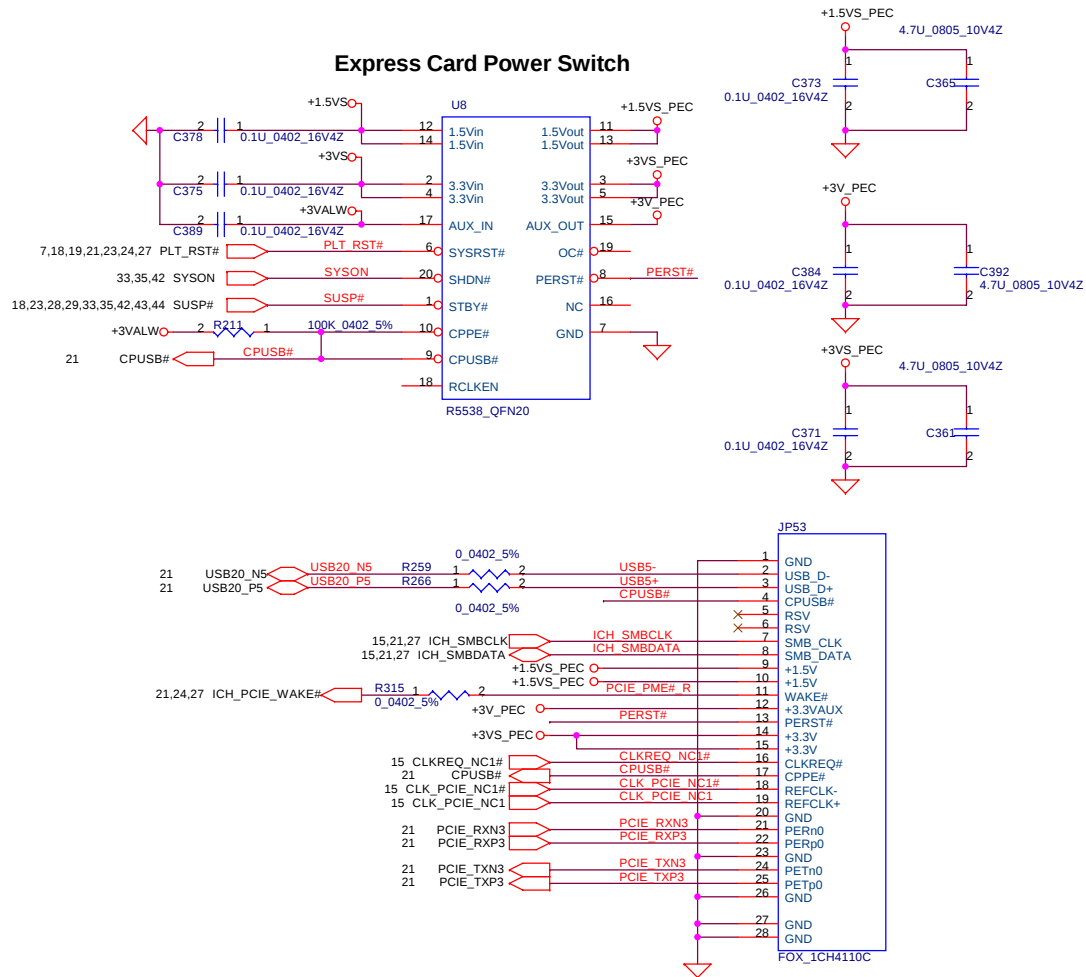


MDC CONN



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				Size	Document Number
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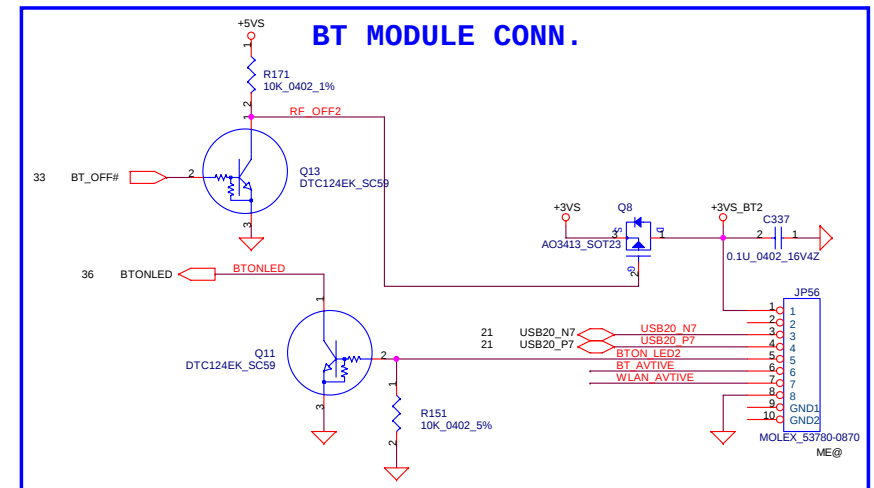
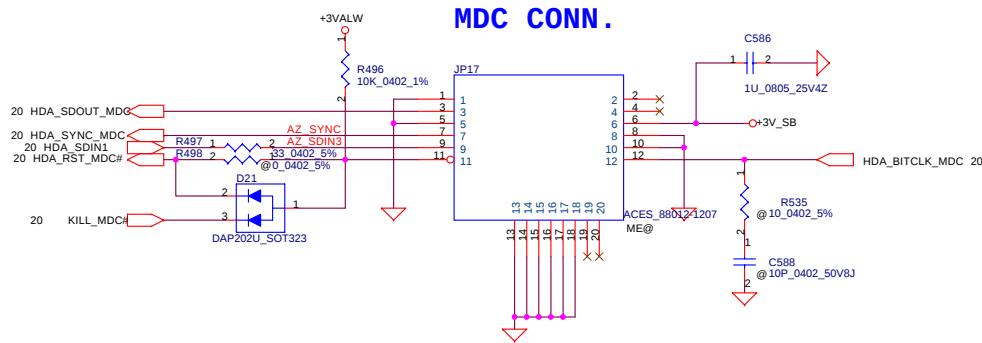
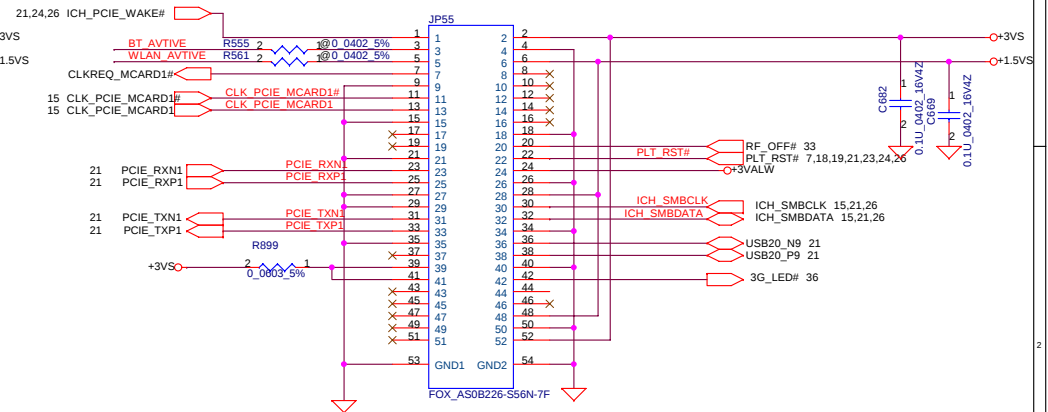
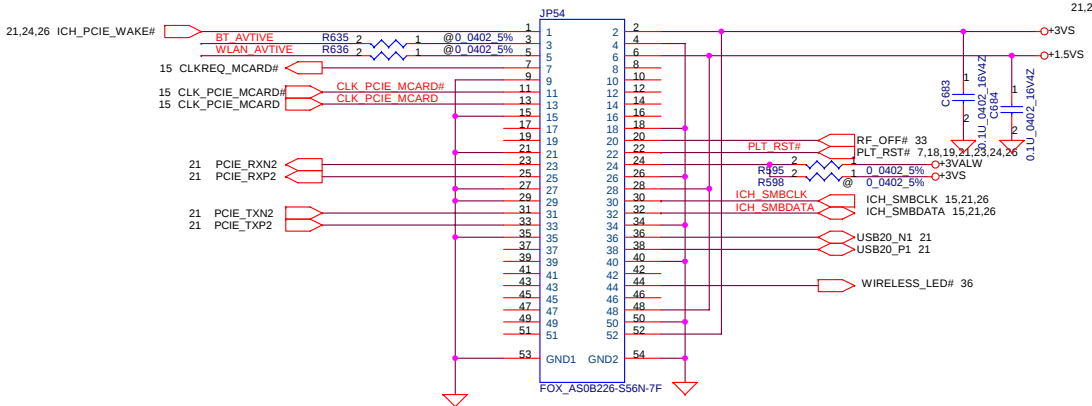
Express Card Power Switch



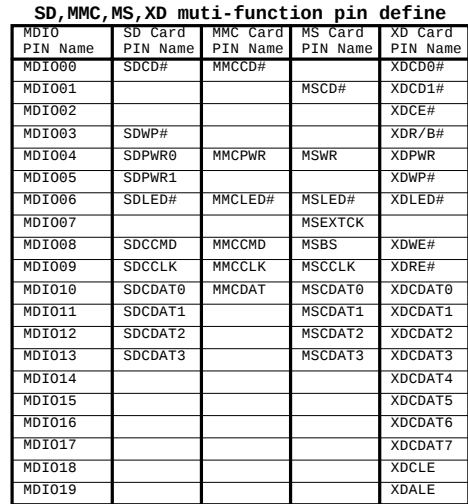
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	
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Size	Custom	Document Number	IGT30 LA-3571P	Rev	0.1
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Mini-Express Card(Slot 1-WLAN)

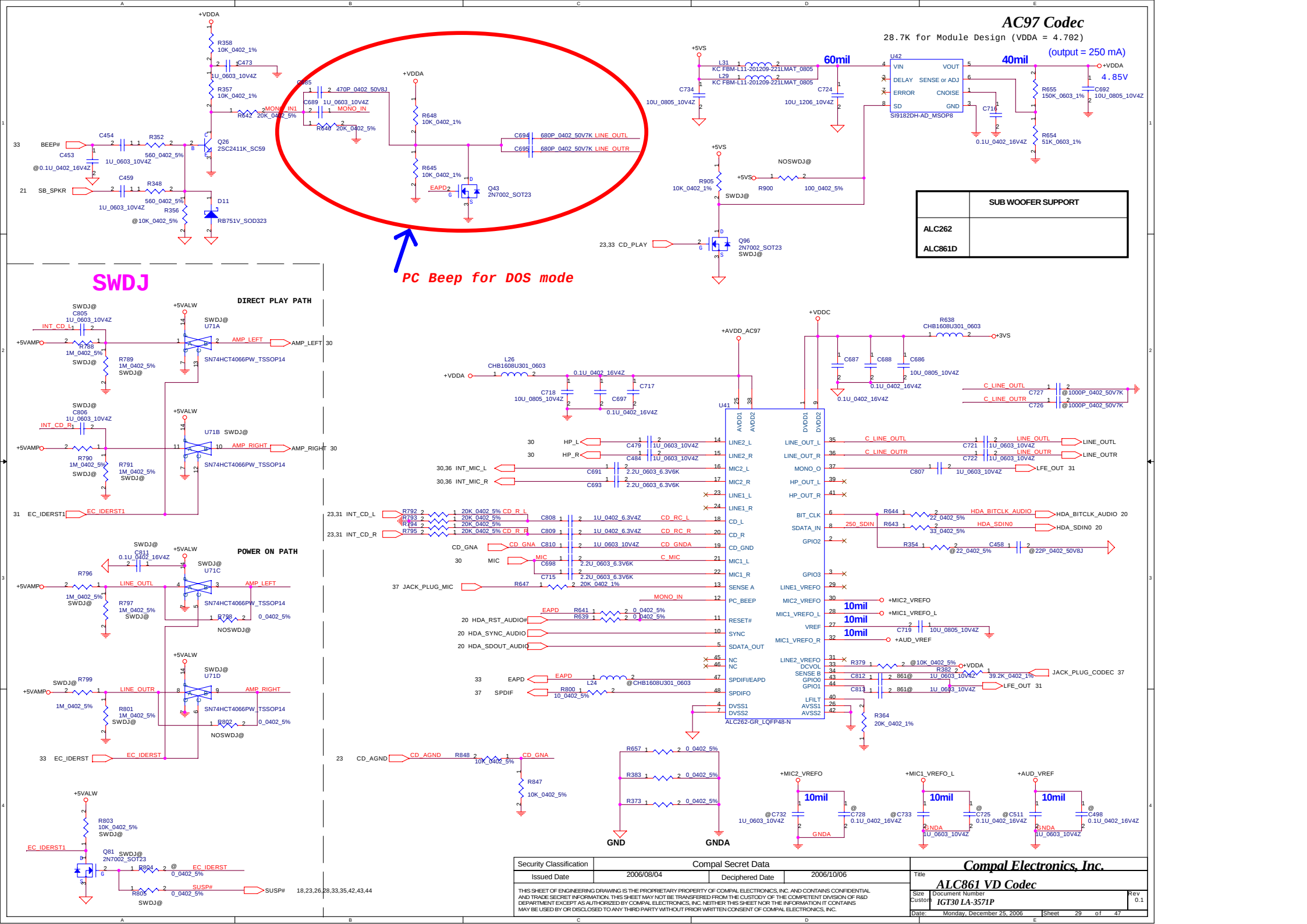
Mini-Express Card(Slot 2-3G)



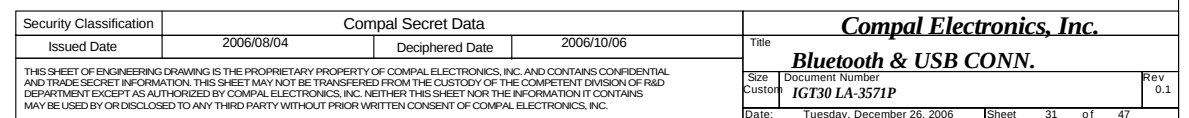
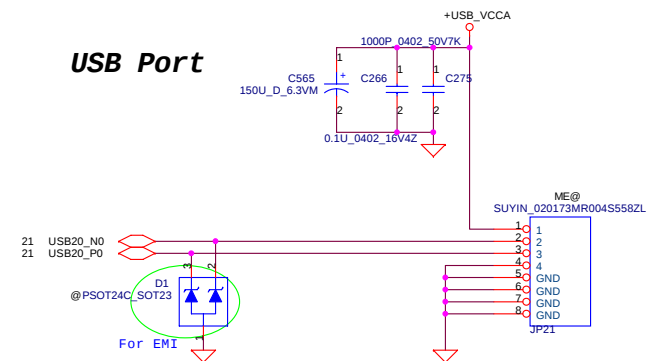
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Compal Electronics, Inc.	
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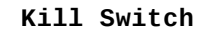
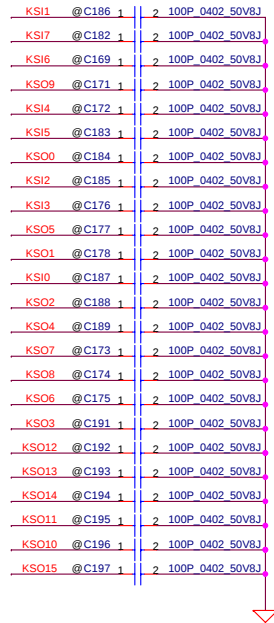


Function set pin define				
UDI03	UDI04	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

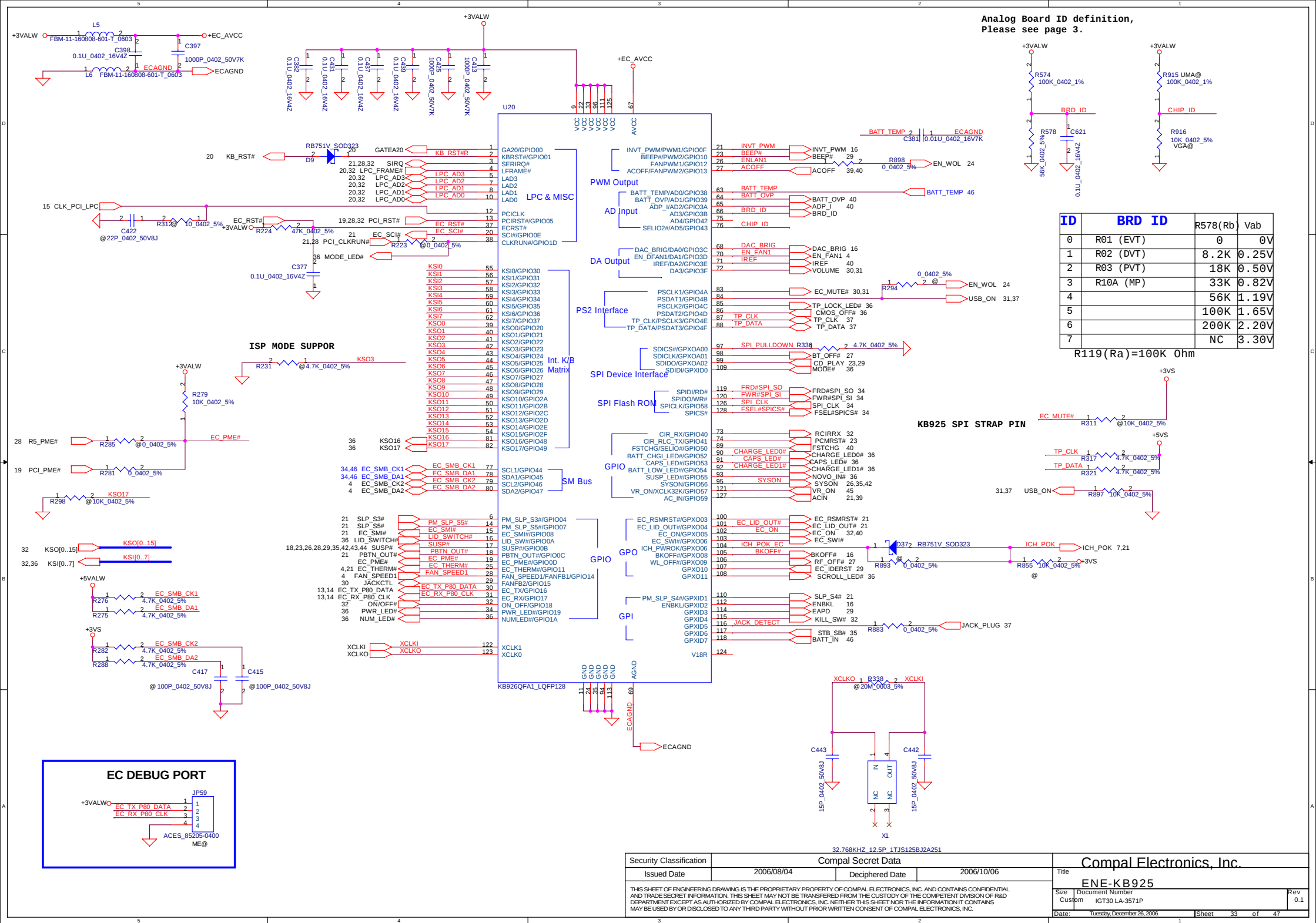


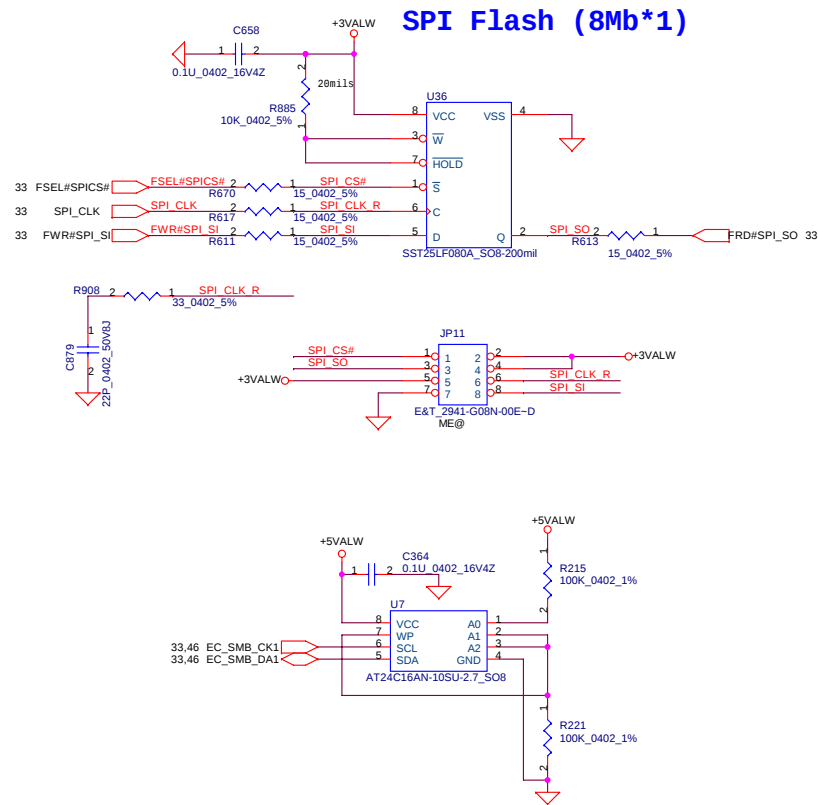
WOOFER@



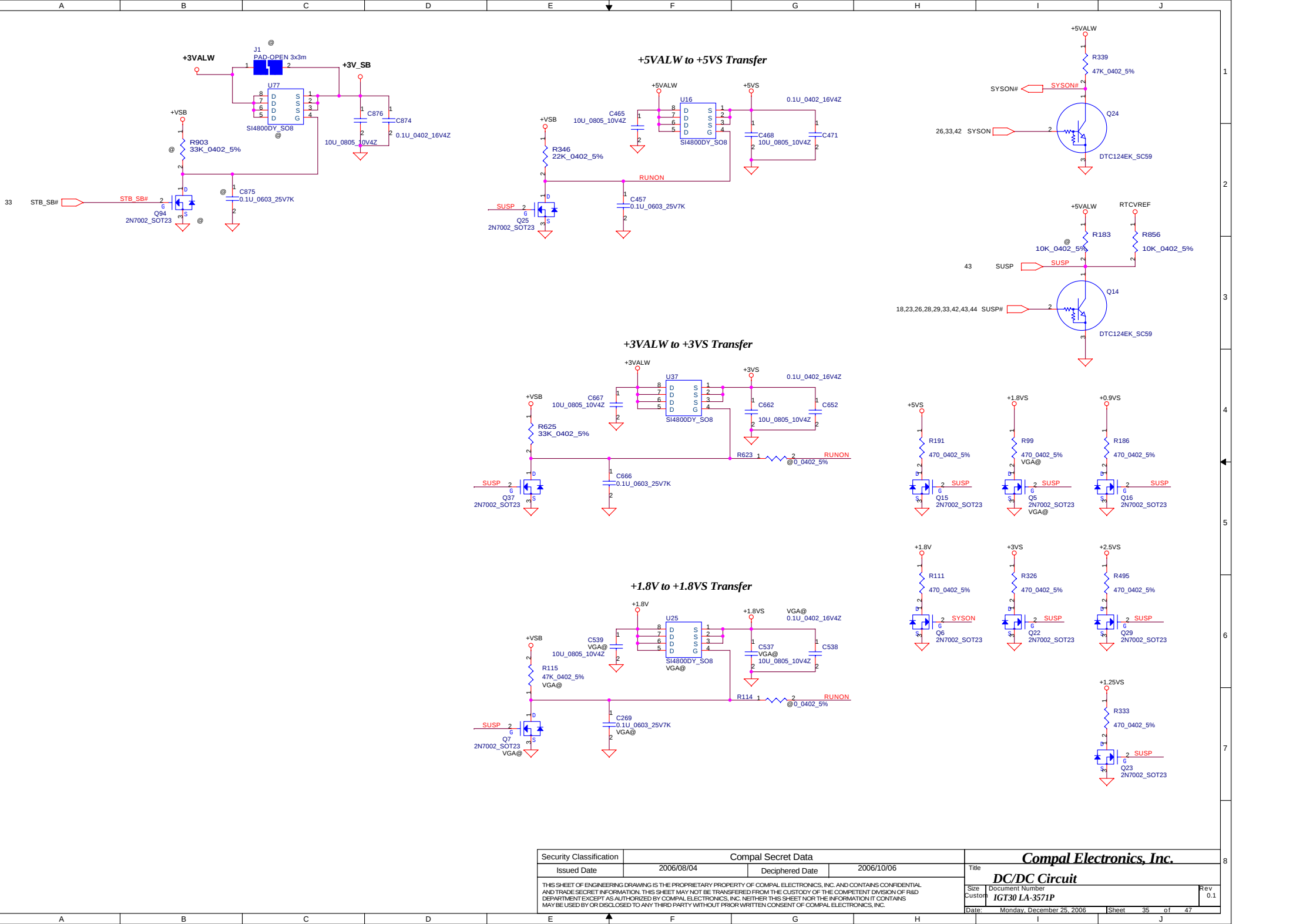


Security Classification		Compal Secret Data		Compal Electronics, Inc. KBD,ON/OFF,T/P,LED/B,DEBUG	
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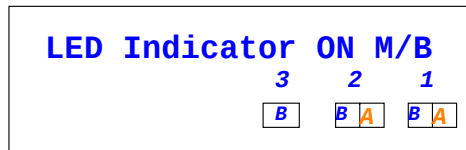




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	DC/DC Circuit
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Wireless / Bluetooth LED

Blue

Amber

STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

(1)

(2)

(3)

BATT_CHG_LED#

Blue

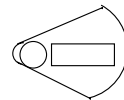
BATT_LOW_LED#

Amber

Blue : Power On,
Blinking Blue : Suspend

STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

Dial Wheel



Function

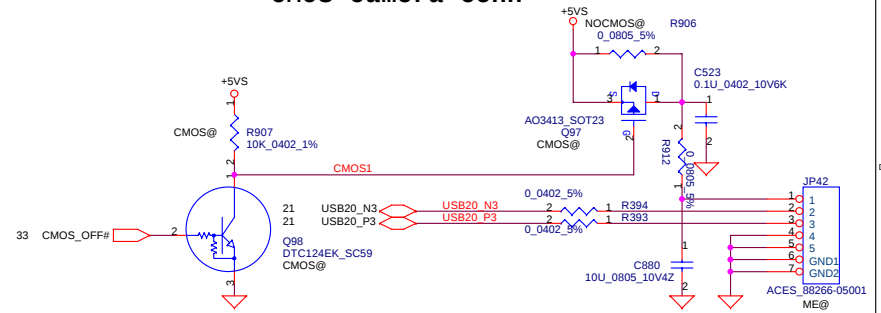
KEY Matrix	K016	K017
KSI0	DW-UP	DW-DOWN
KSI1	DW-ENTER	MUTE

NOVA_BTN#

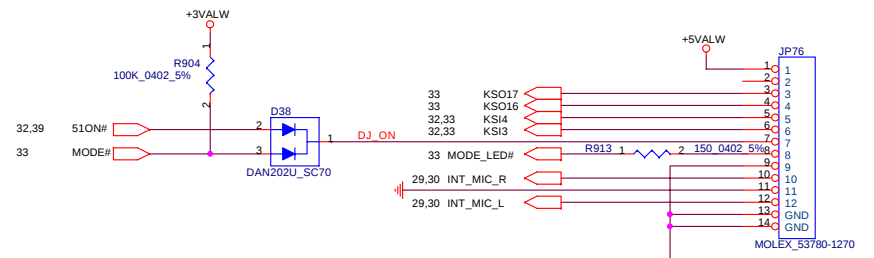
NOVO BTN

C839, C841, C842 For EMI Solution

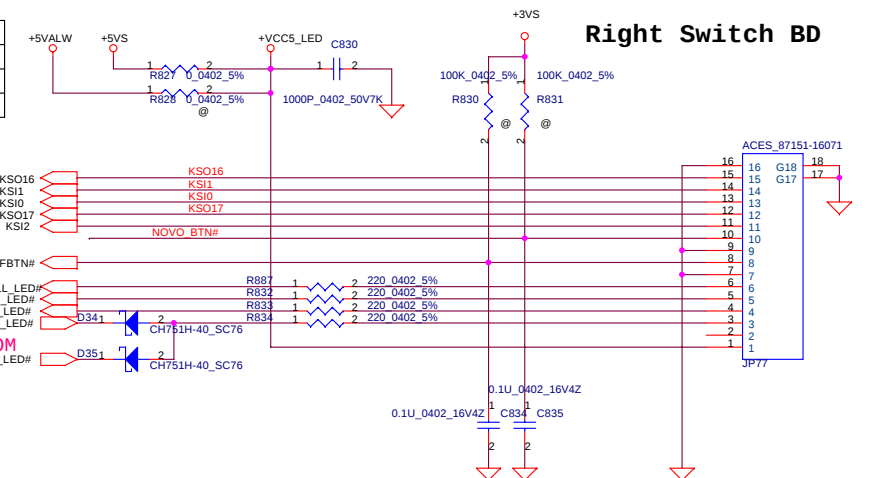
CMOS Camera Conn



Left Switch BD(AUDIO DJ)

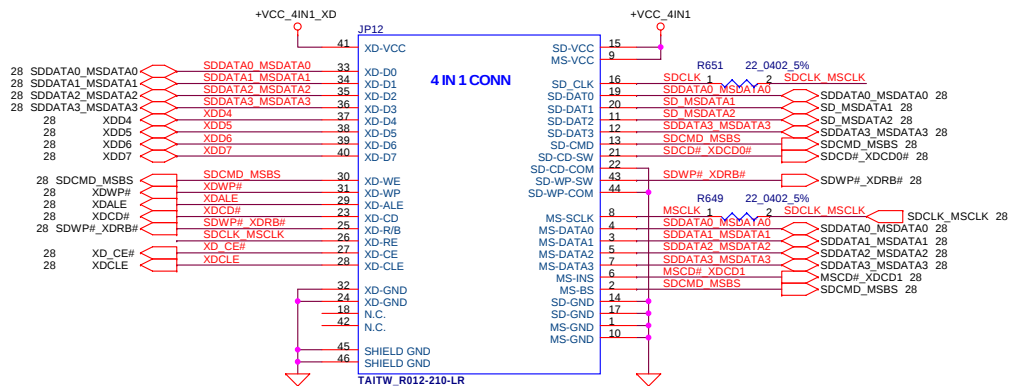


Right Switch BD

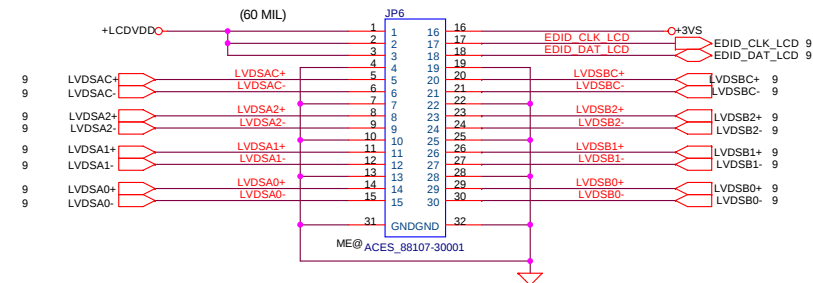


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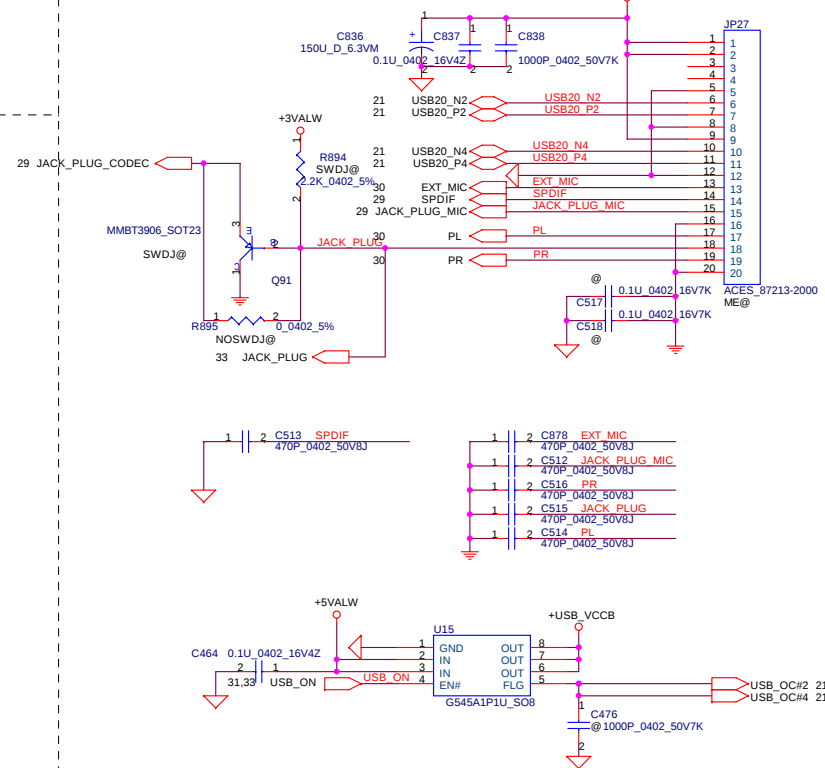
4 in 1 Card Reader



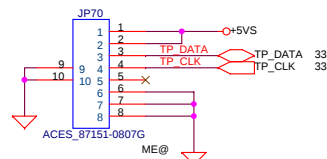
UMA LCD/PANEL Conn.



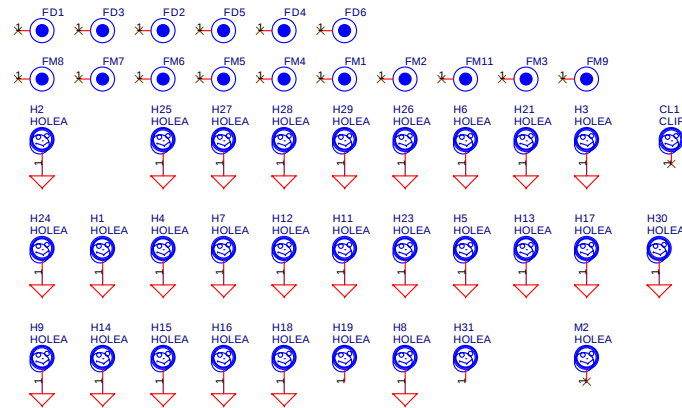
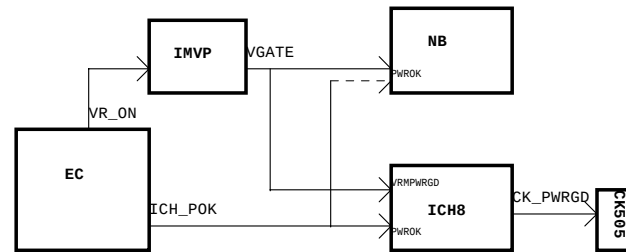
Audio Jack/USB Conn.



T/P Board



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	Hole
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ACIN

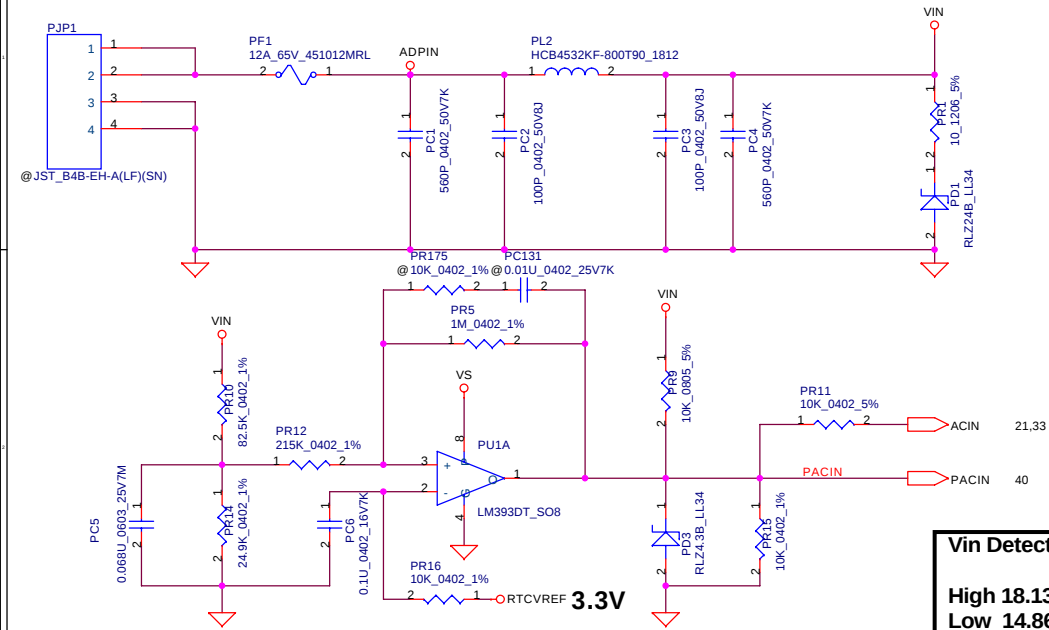
Precharge detector

	Min.	typ.	Max.
H-->L	13.843V	14.247V	14.636V
L-->H	14.936V	15.381V	15.814V

BATT ONLY

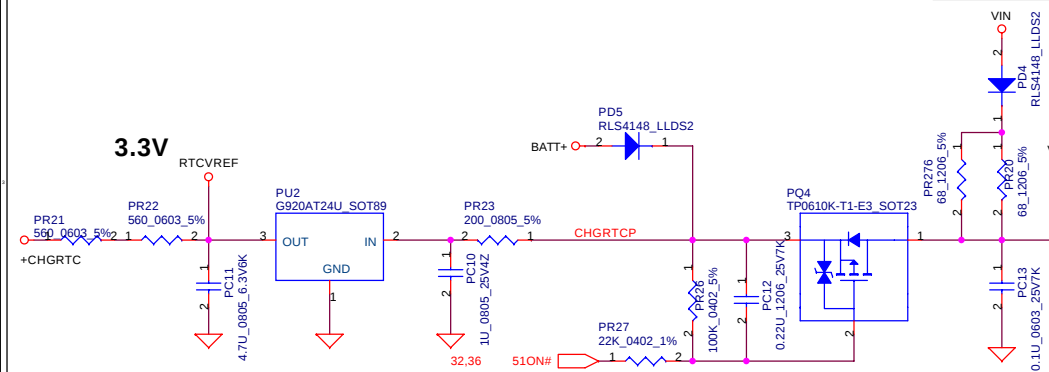
Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



Vin Detector

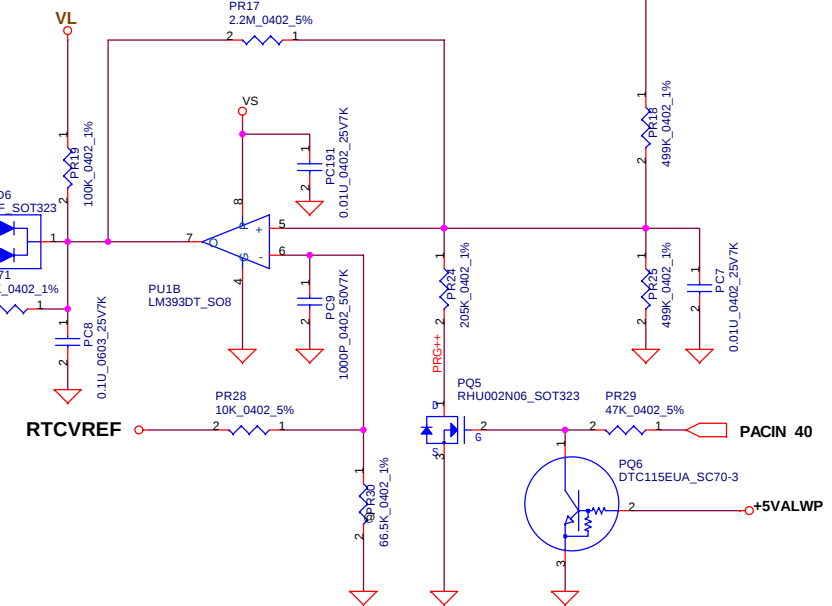
	High	18.135	17.566	17.011
	Low	14.866	14.355	14.063



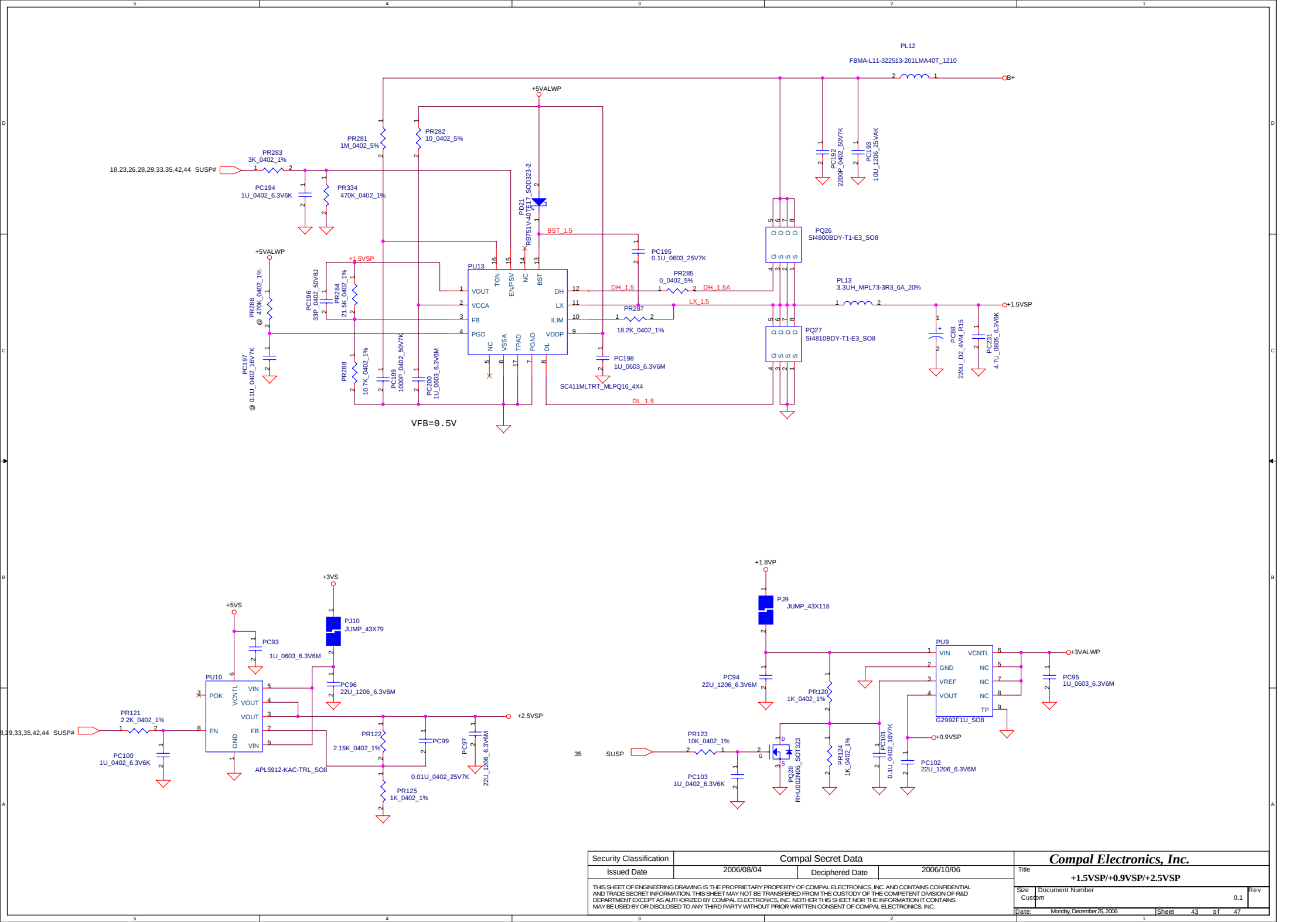
41,46 MAINPWON

40 ACON

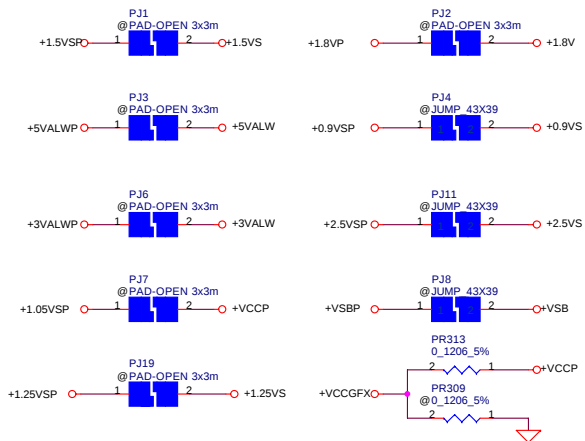
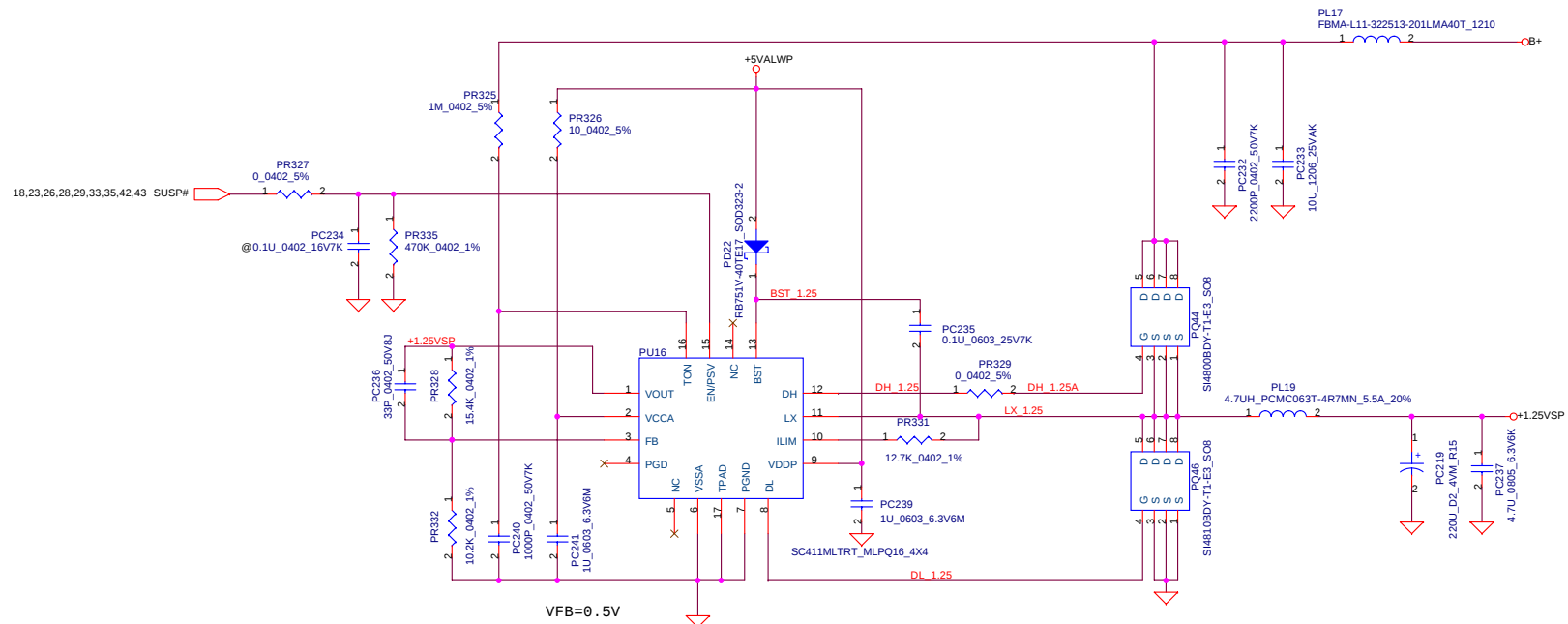
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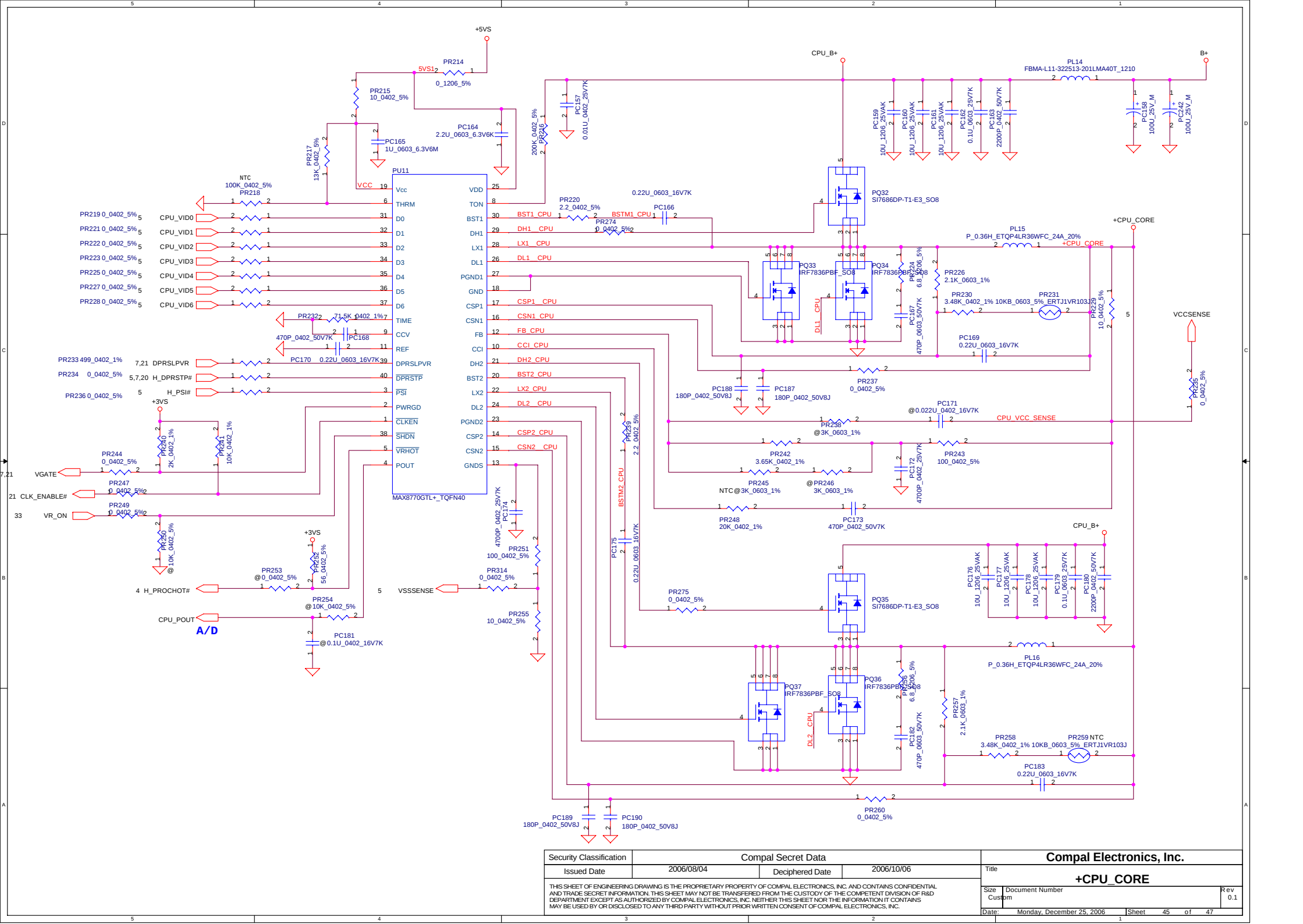
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