Compal Confidential

G470/G570 DIS+UMA+Muxless M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Robson/PX3.0,PX4.0

2010-10-22

LA-6751P / LA-6753P

REV:0.3

Security Classification	Compal Secret Data		
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Title: Cover Page

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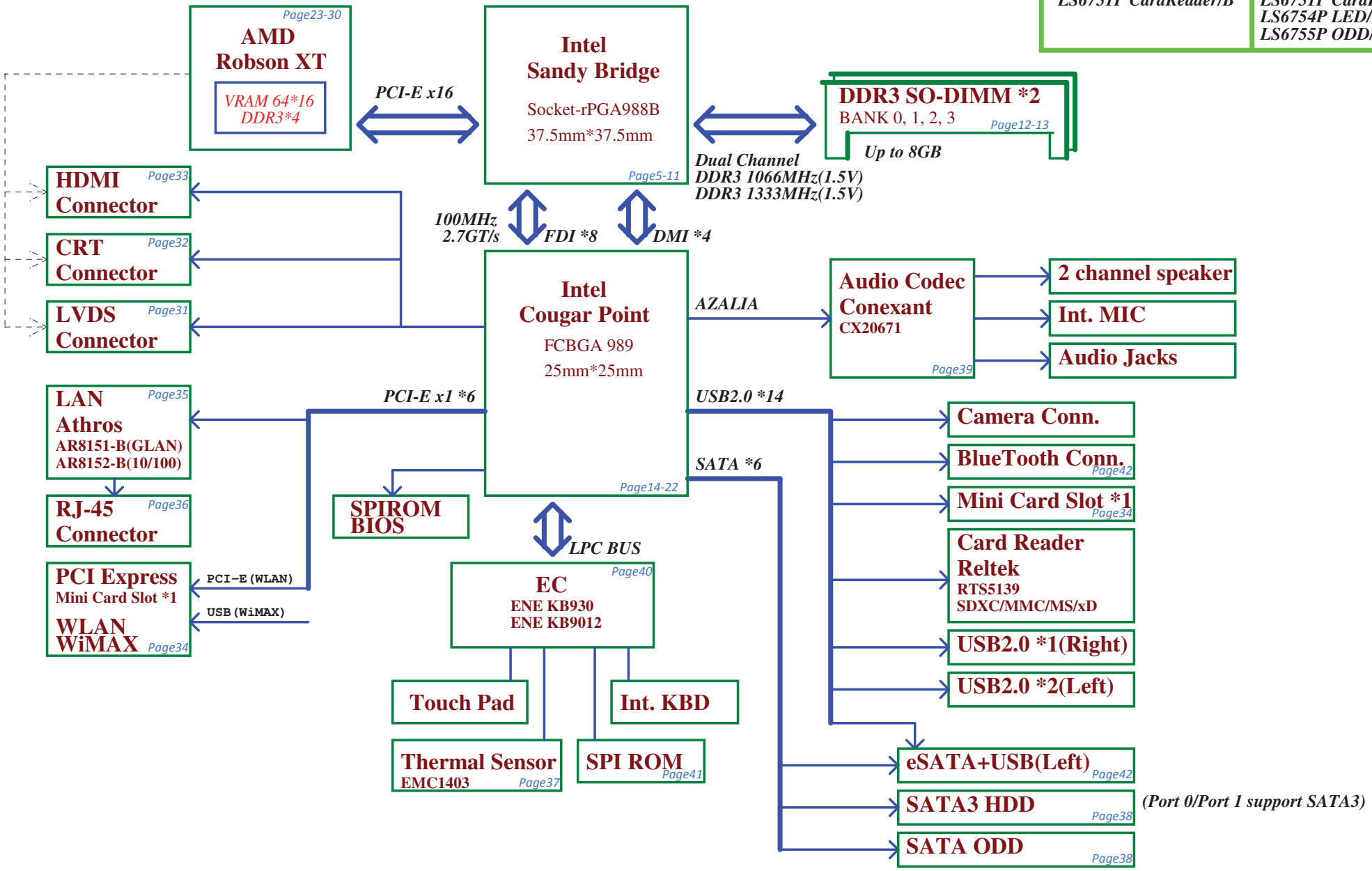
File Name : G470/G570

For 14"(Page 4x)	For 15"(Page 4x+1)
LS6753P PWR/B LS6751P CardReader/B	LS6753P PWR/B LS6751P CardReader/B LS6754P LED/B LS6755P ODD/B



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Title: Block Diagram

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Thermal Sensor EMC1402-1	100_1100 b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
UMA and PX bus	PX@
Discrete Only	DIS@
PX3.0 only, not for BACO	PX3@
BACO	BACO@
COMMON HDMI	HDMI@
UMA HDMI	UMA_HDMI@
Discrete HDMI	VGA_HDMI@
eSATA	ESATA@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Cameara	CMOS@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

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Power-Up/Down Sequence

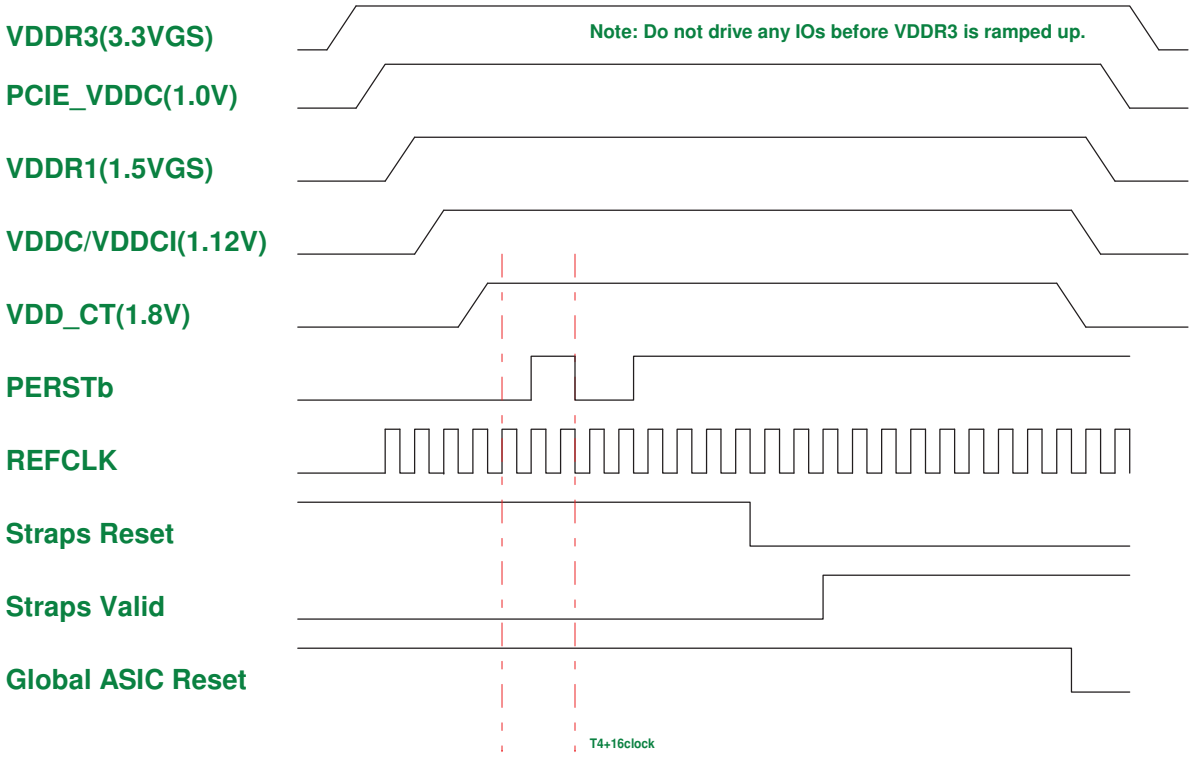
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



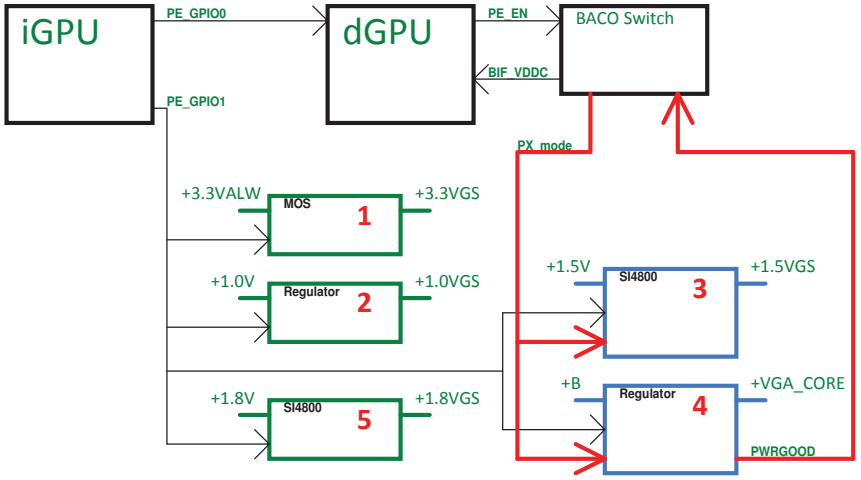
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

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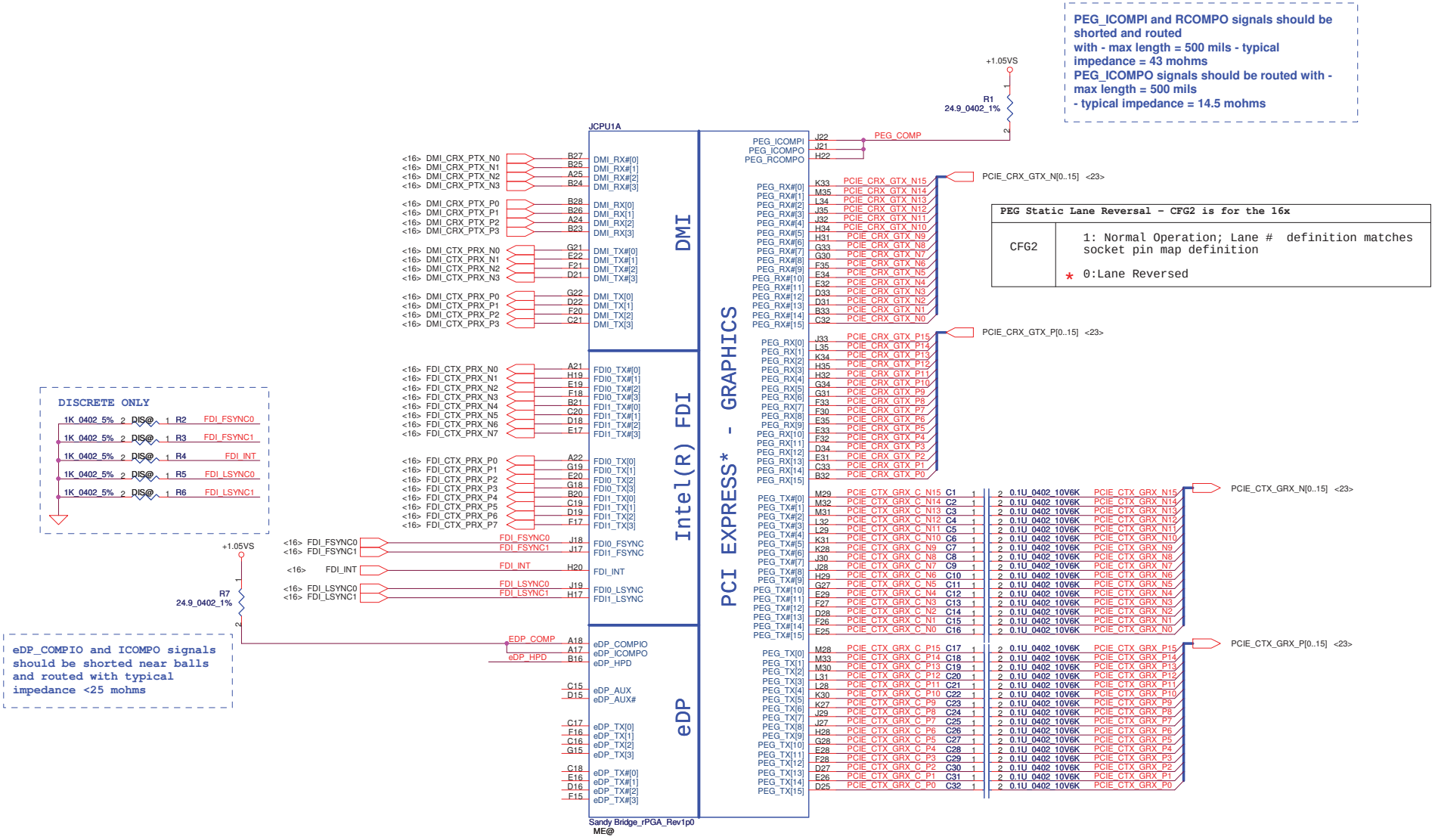

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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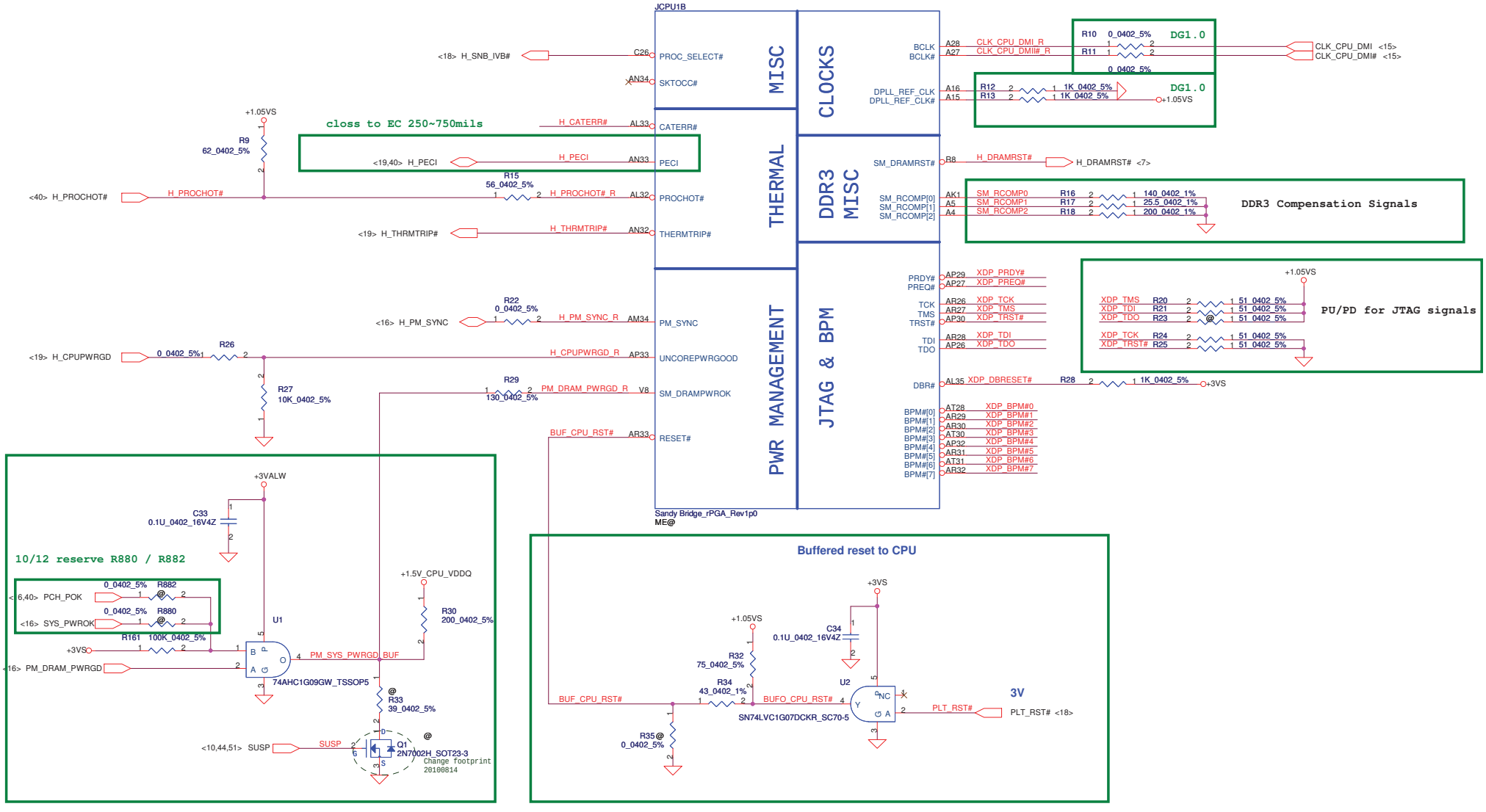

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Title: PROCESSOR(2/7) PM,XDP,CLK

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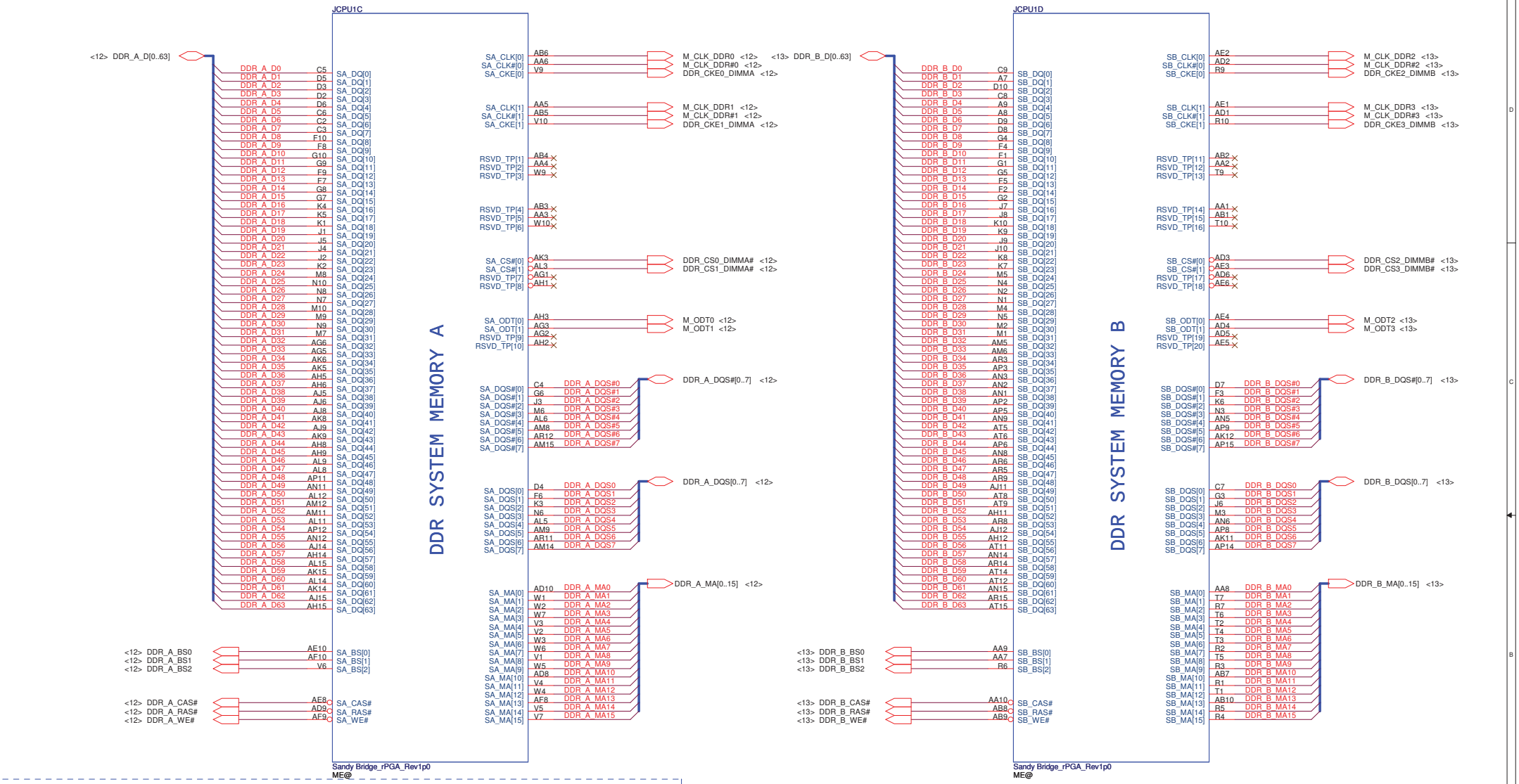

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Title: **PROCESSOR(3/7) DDRIII**

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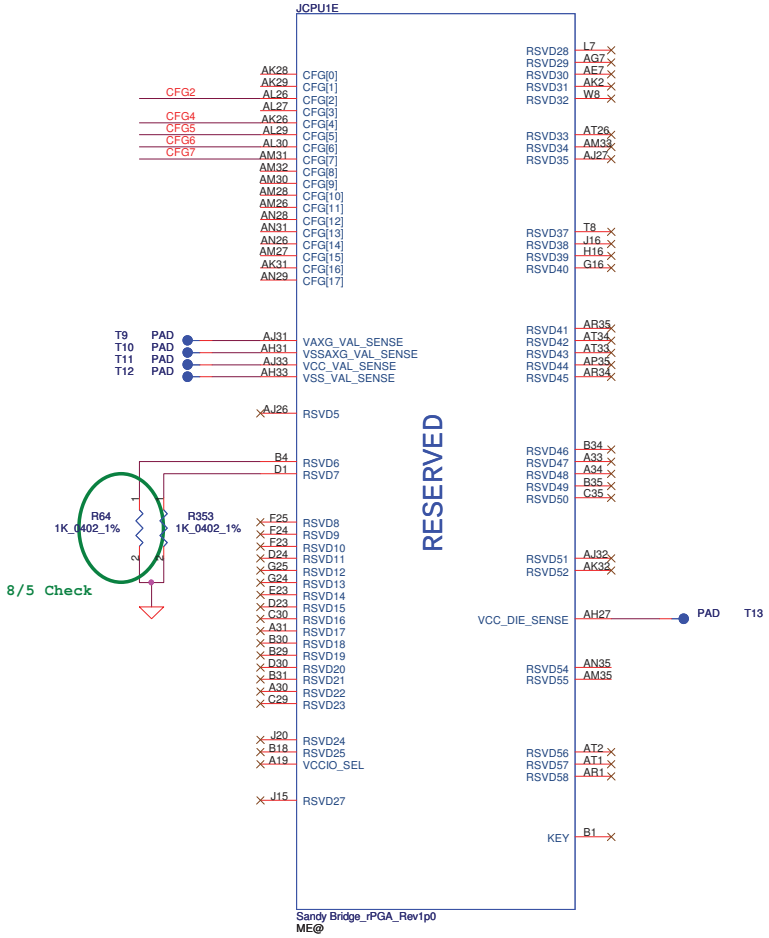
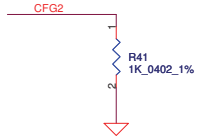
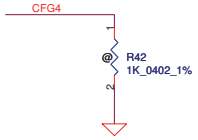
CFG Straps for Processor

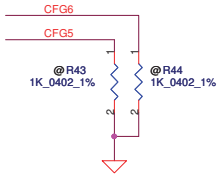




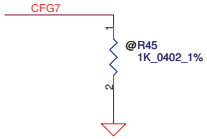
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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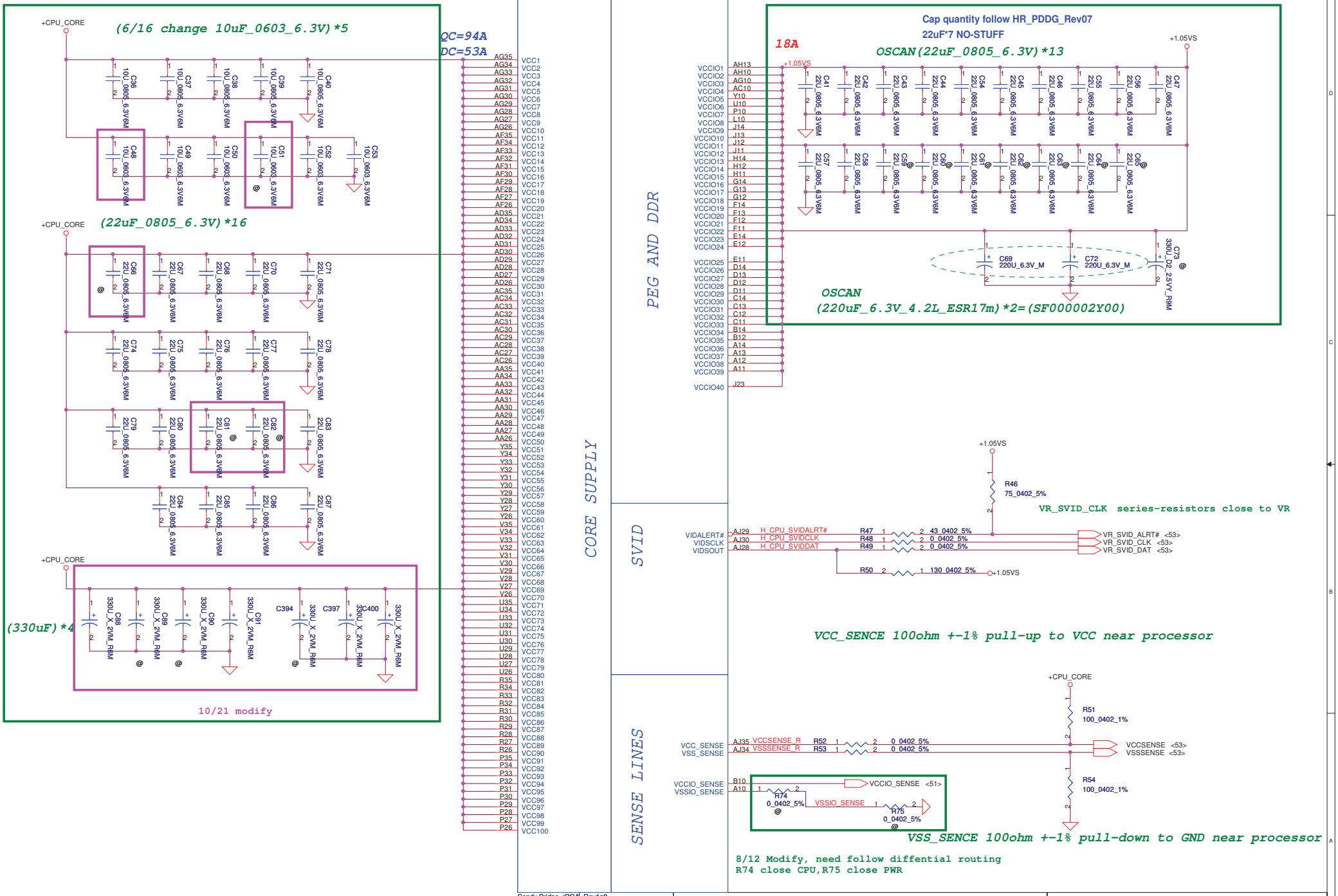
POWER



Sandy Bridge_rPGA_Rev1.0
ME@

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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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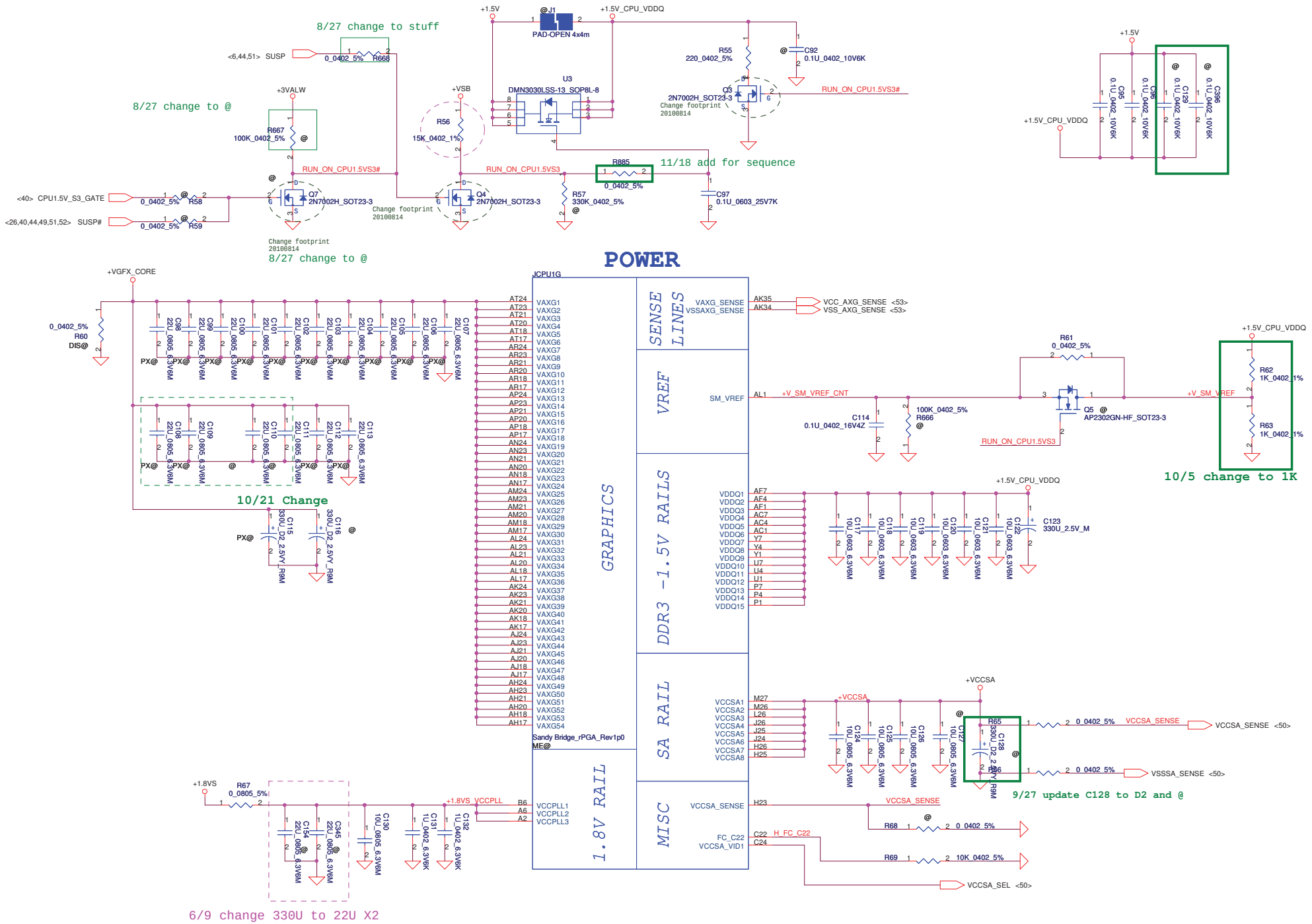

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Title: **PROCESSOR(6/7) PWR**

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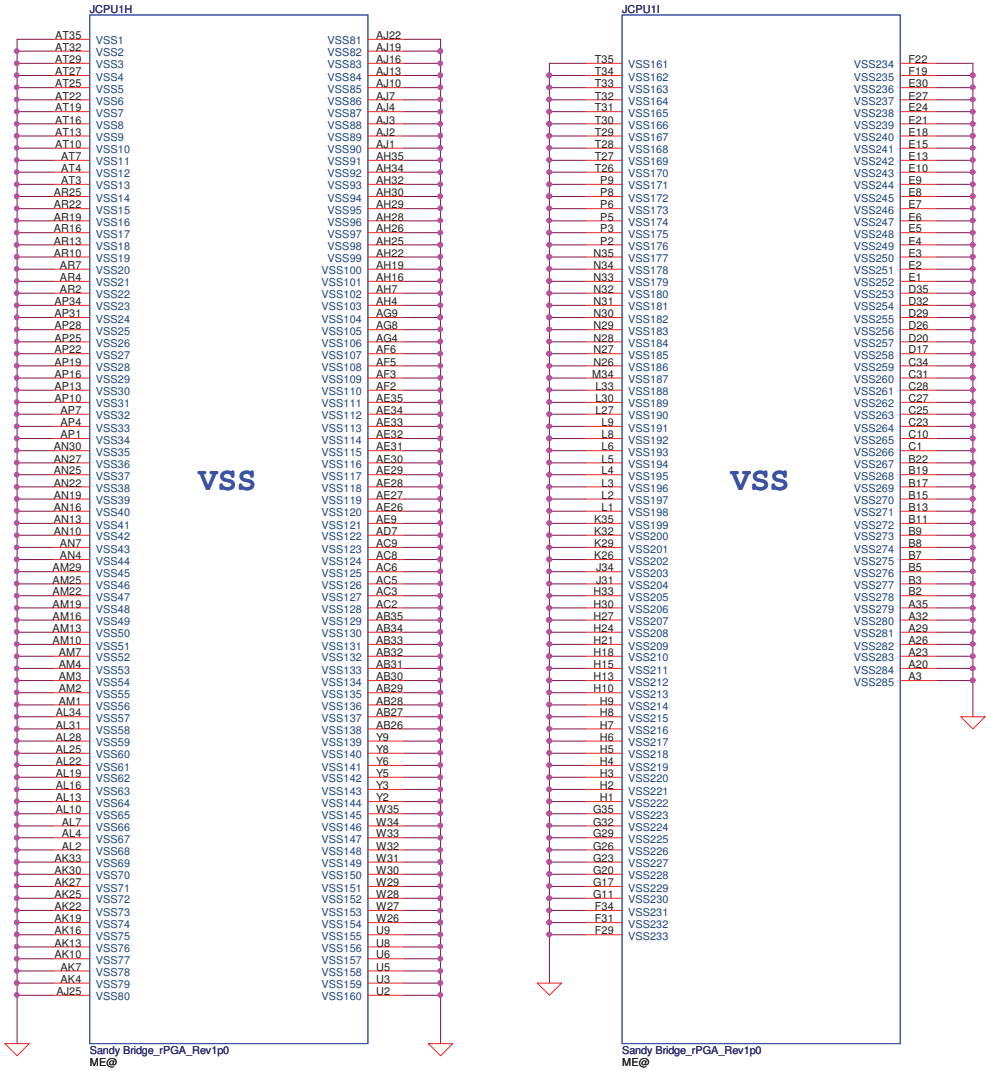

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Title: **PROCESSOR(7/7) VSS**

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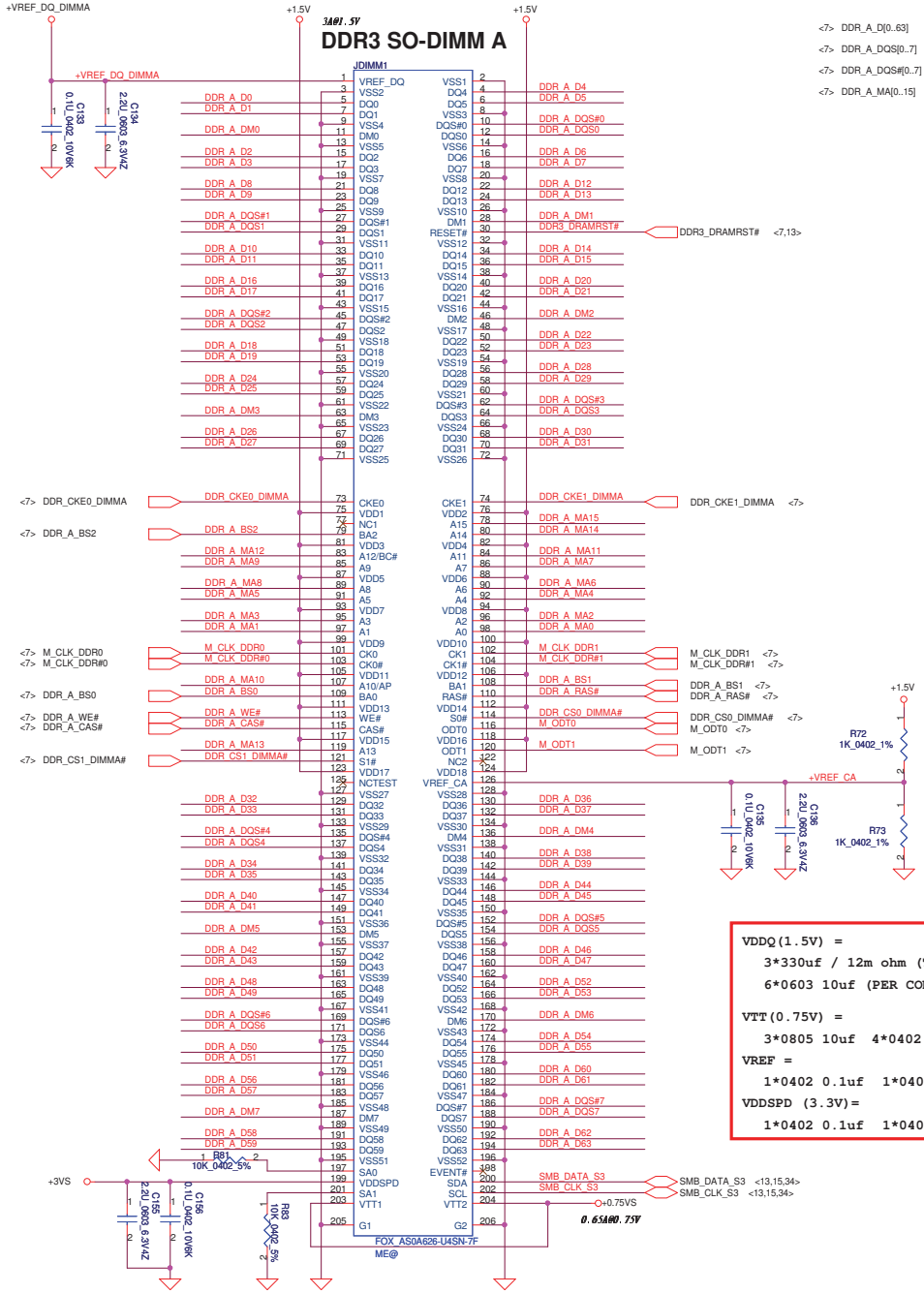
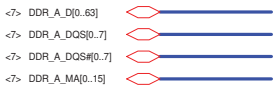
DDR3 SO-DIMM A

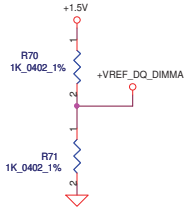
JDIMM1

FOX_AS0A626-U4SN-7F

ME@







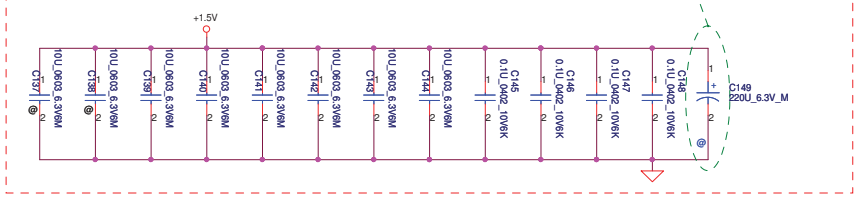

```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf
VREF =
  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

Layout Note:
Place near DIMM



Layout Note:
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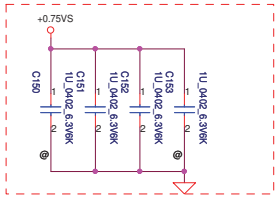
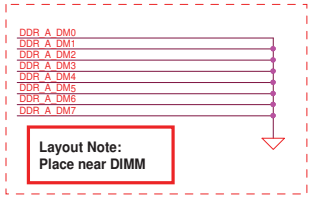


7/28 Update connect GND directly



Layout Note:
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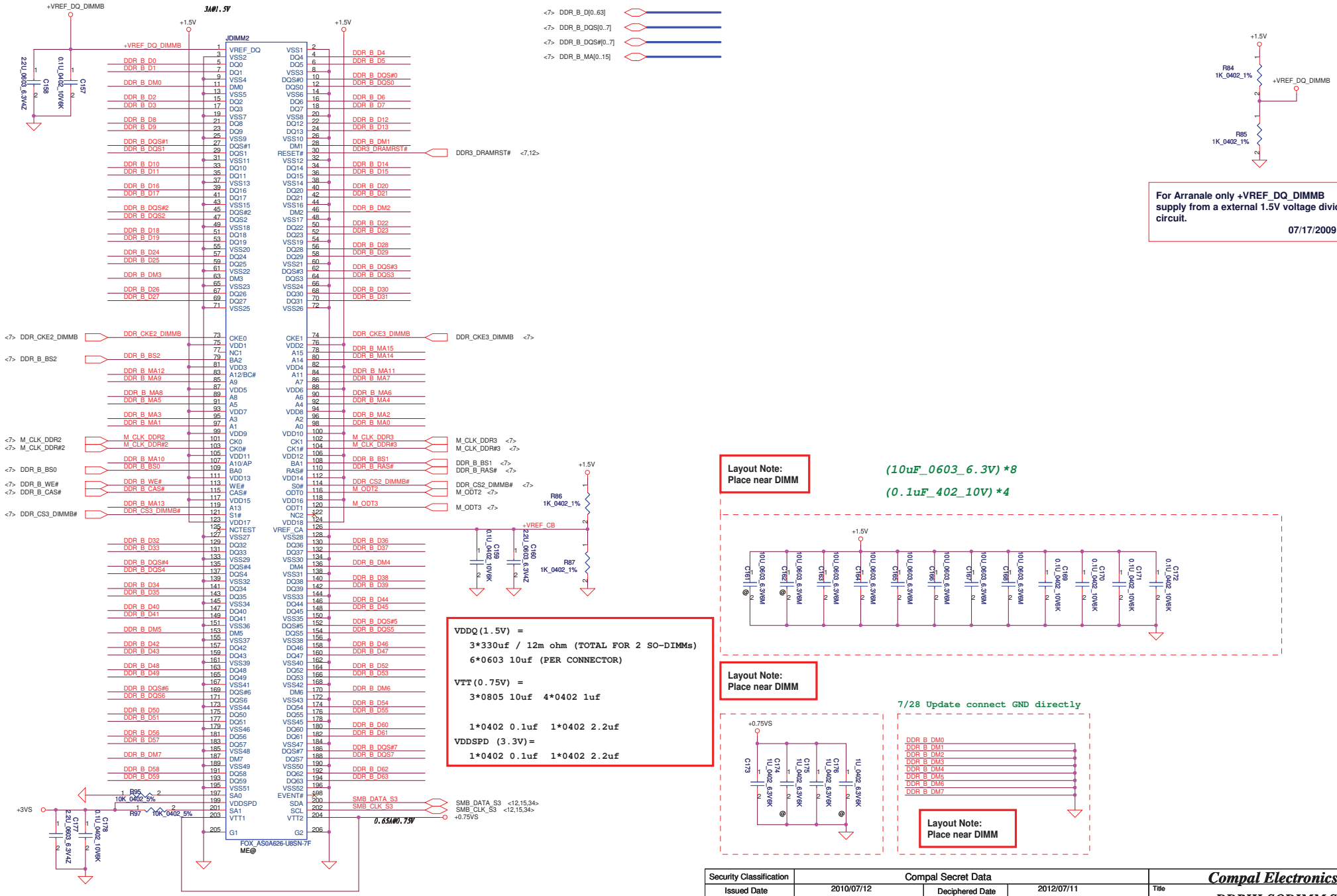
Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 12 of 59



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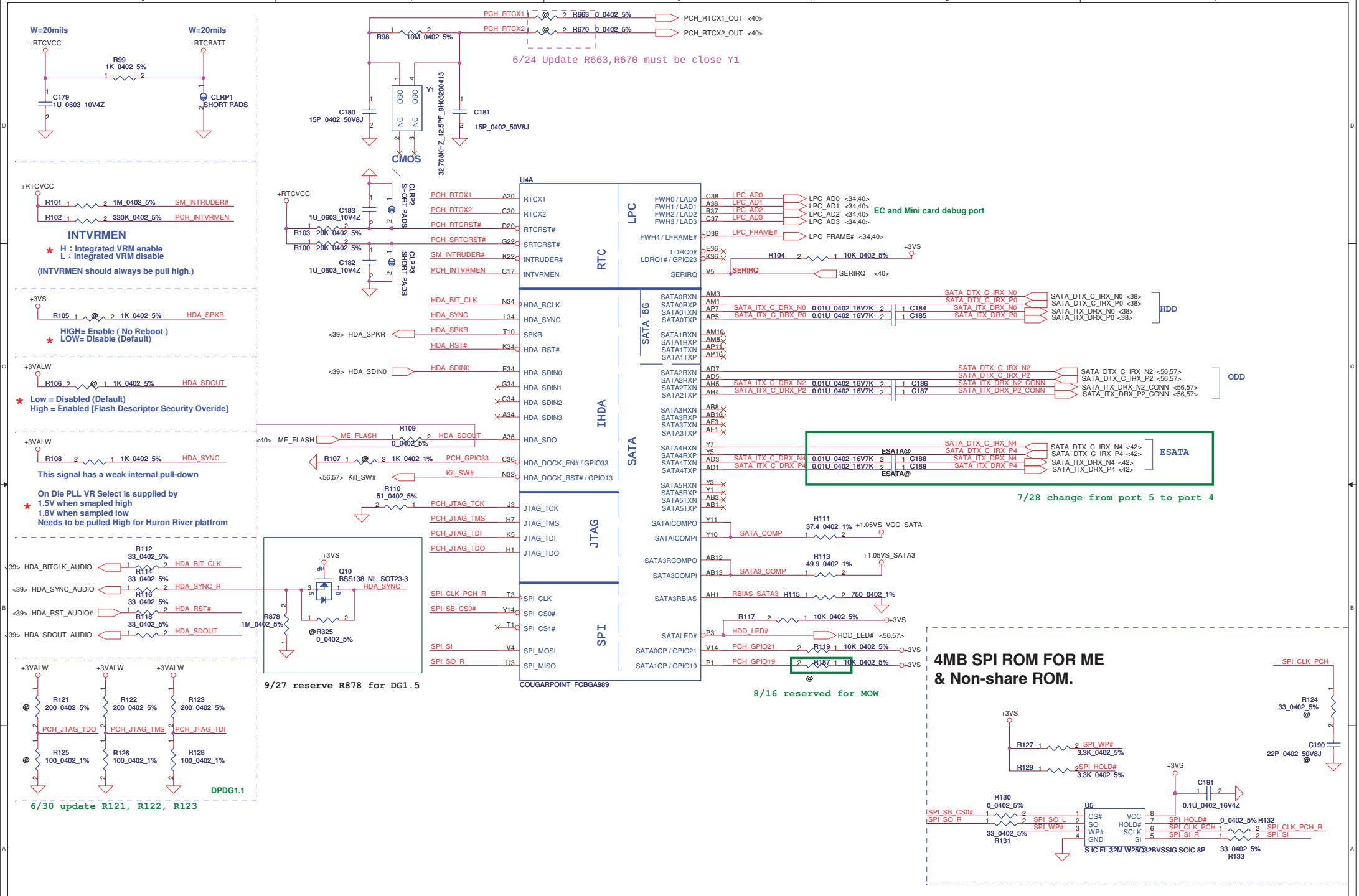
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size: | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 13 of 59



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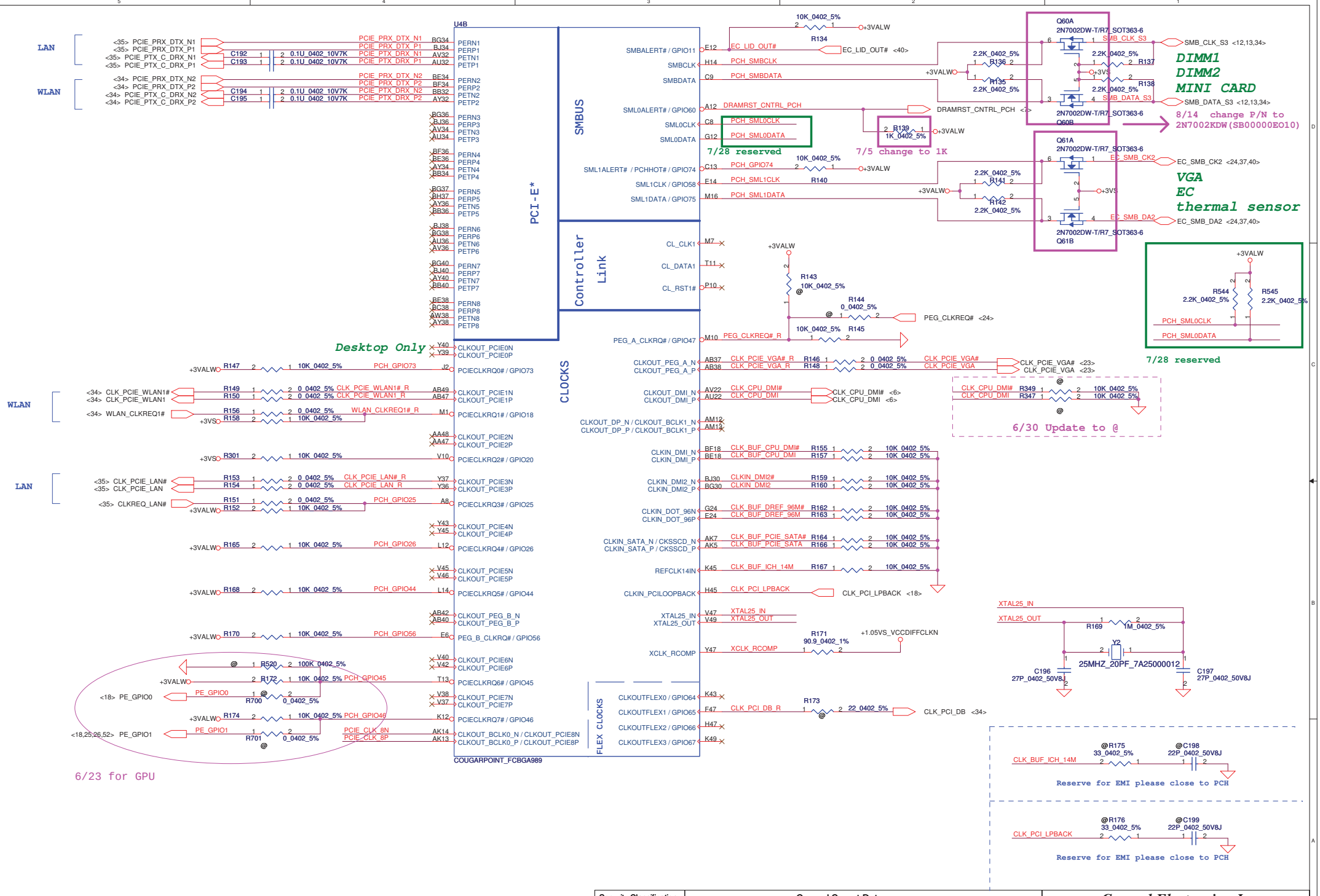
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 14 of 59



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Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

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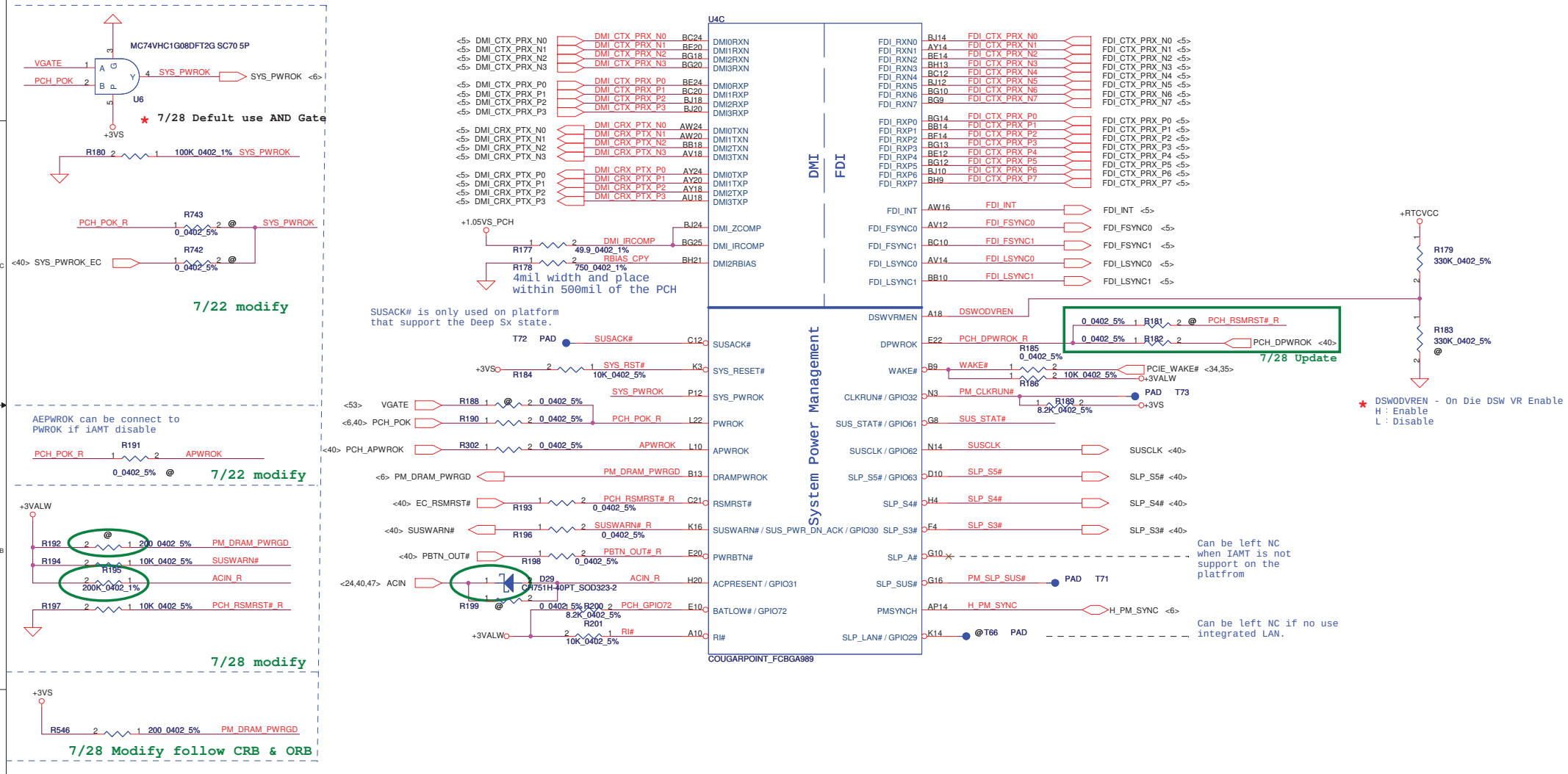
Date: Friday, November 26, 2010 | Sheet 15 of 59



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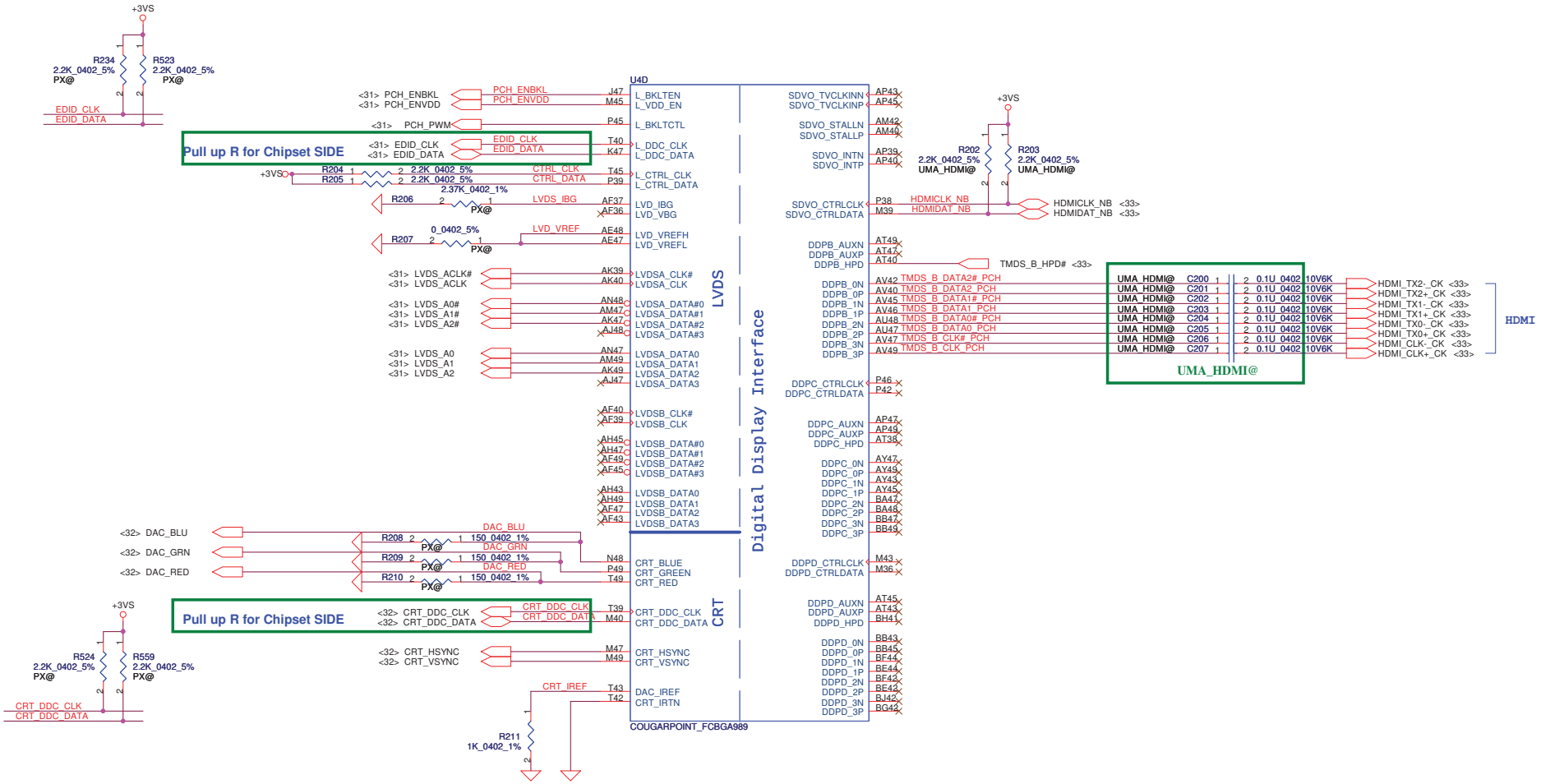
Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size: Custom | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 16 of 59



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Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

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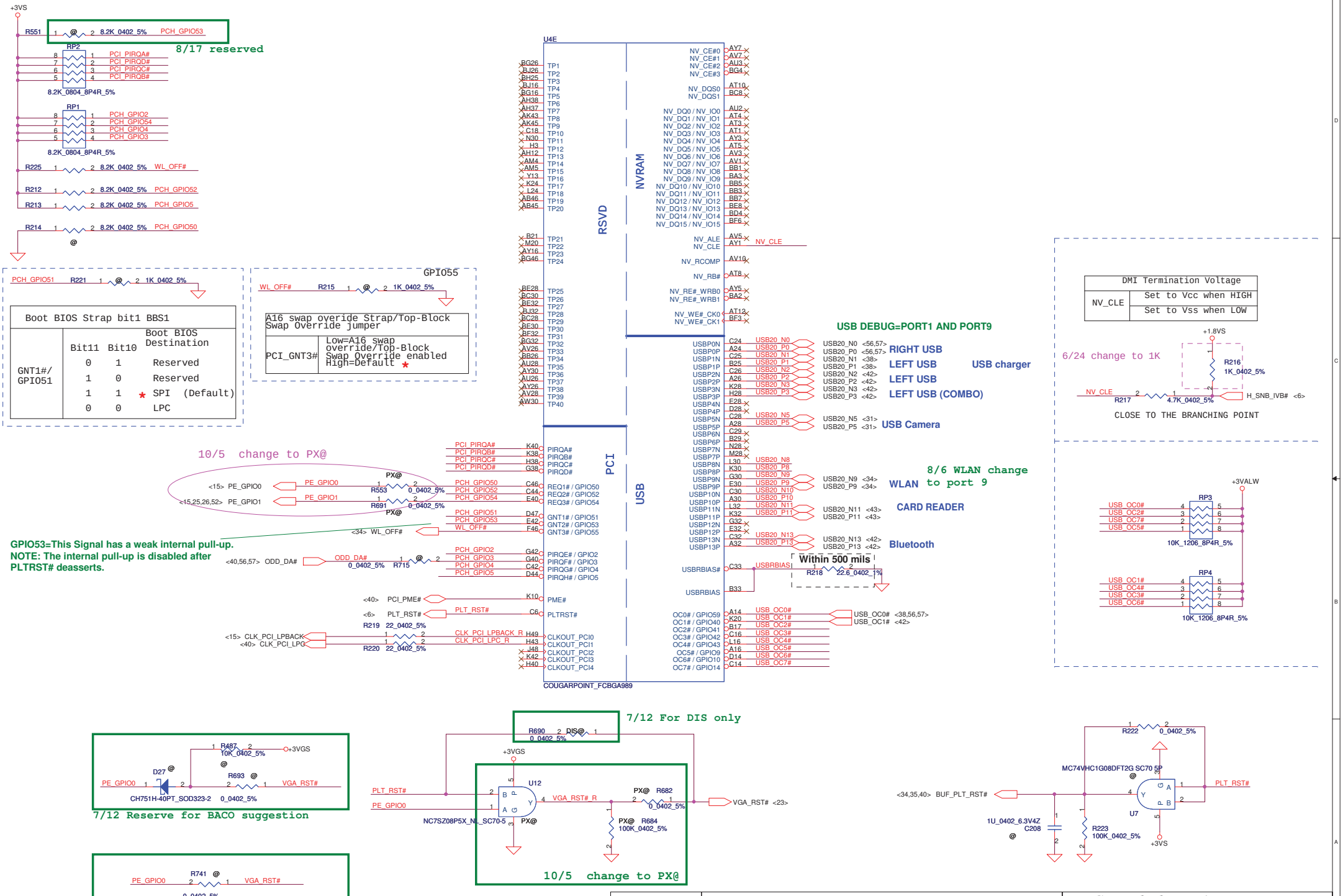
Date: Friday, November 26, 2010 | Sheet 17 of 59



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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: LA-6751P | Rev: 0.1

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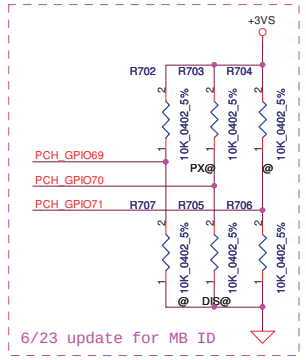
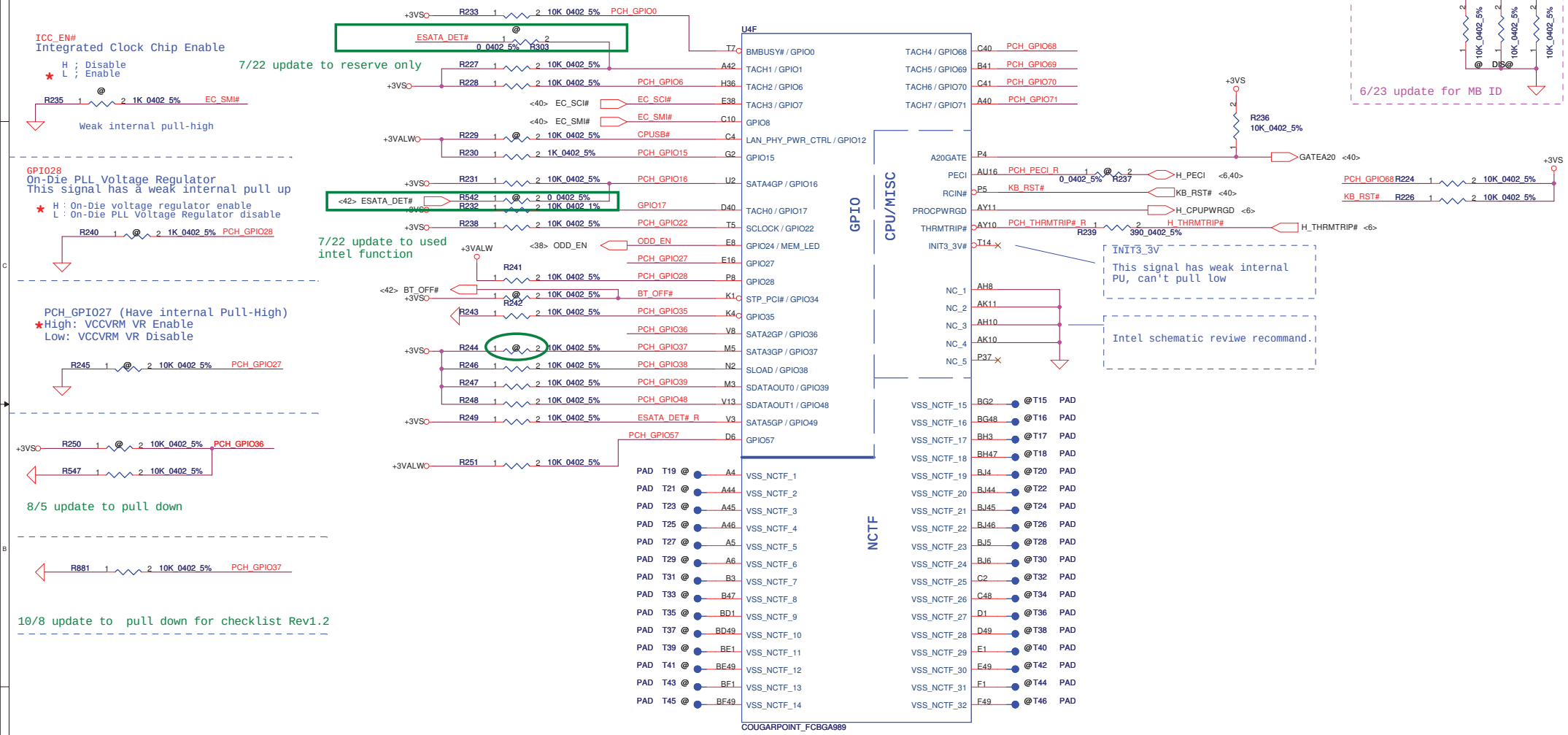
PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA
1	0	0	DIS
0	1	0	PX3.0
1	1	0	PX4.0 *





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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-6751P | Rev: 0.2

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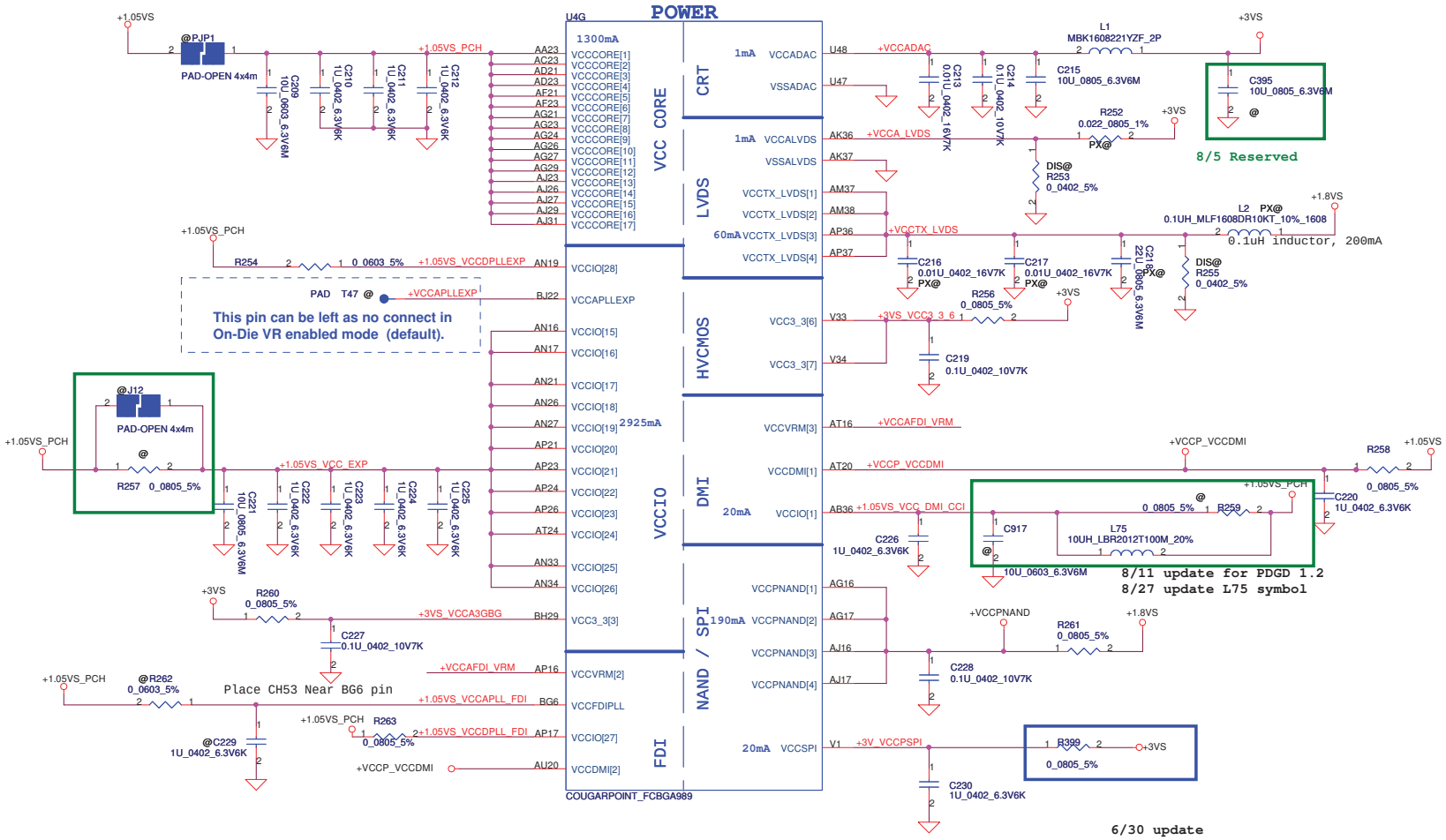

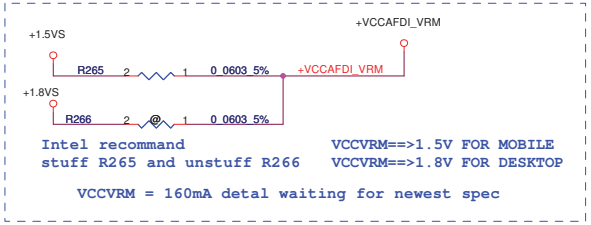

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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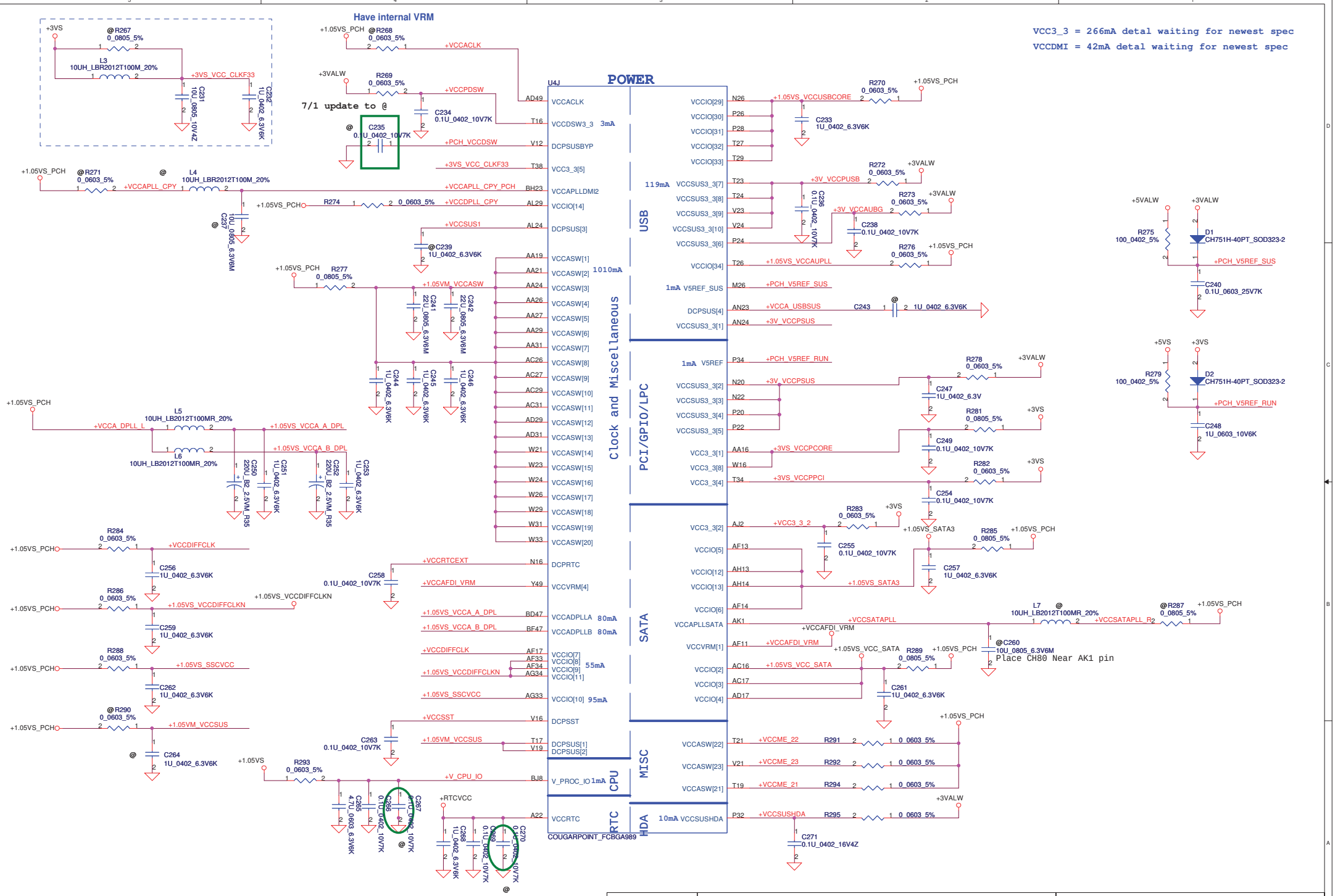
Have internal VRM
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec
7/1 update to @
POWER
U4J
COUGARPOINT_FCBGA989
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
VCCACLK
VCCDSW3_3 3mA
DCPSUSBYP
VCC3_3[5]
VCCAPLLDMI2
VCCIO[14]
DCPSUS[3]
VCCASW[1]
VCCASW[2] 1010mA
VCCASW[3]
VCCASW[4]
VCCASW[5]
VCCASW[6]
VCCASW[7]
VCCASW[8]
VCCASW[9]
VCCASW[10]
VCCASW[11]
VCCASW[12]
VCCASW[13]
VCCASW[14]
VCCASW[15]
VCCASW[16]
VCCASW[17]
VCCASW[18]
VCCASW[19]
VCCASW[20]
DCPRTC
VCCVRM[4]
VCCADPLLA 80mA
VCCADPLLB 80mA
VCCIO[7]
VCCIO[8]
VCCIO[9] 55mA
VCCIO[11]
VCCIO[10] 95mA
DCPSST
DCPSUS[1]
DCPSUS[2]
V_PROC_IO 1mA
VCCRTC
VCCIO[29]
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
119mA VCCSUS3_3[7]
VCCSUS3_3[8]
VCCSUS3_3[9]
VCCSUS3_3[10]
VCCSUS3_3[6]
VCCIO[34]
1mA V5REF_SUS
DCPSUS[4]
VCCSUS3_3[1]
1mA V5REF
VCCSUS3_3[2]
VCCSUS3_3[3]
VCCSUS3_3[4]
VCCSUS3_3[5]
VCC3_3[1]
VCC3_3[8]
VCC3_3[4]
VCC3_3[2]
VCCIO[5]
VCCIO[12]
VCCIO[13]
VCCIO[6]
VCCAPLLSATA
VCCVRM[1]
VCCIO[2]
VCCIO[3]
VCCIO[4]
VCCASW[22]
VCCASW[23]
VCCASW[21]
10mA VCCSUSHDA
+3VS_VCC_CLKF33
+VCCACLK
+VCCPDSW
+PCH_VCCDSW
+VCCAPLL_CPY_PH
+VCCDPLL_CPY
+VCCSUS1
+VCCASW
+VCCA_DPLL_L
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCDIFFCLK
+1.05VS_VCCDIFFCLKN
+1.05VS_SSCVCC
+1.05VM_VCCSUS
+VCCRTCEXT
+VCCAFDI_VRM
+V_CPU_IO
+RTCVCC
+1.05VS_VCCUSBCORE
+3V_VCCPUSB
+3V_VCCAUBG
+1.05VS_VCCAUPLL
+PCH_V5REF_SUS
+VCCA_USBSUS
+3V_VCCPSUS
+PCH_V5REF_RUN
+3VS_VCCPCORE
+3VS_VCCPPCI
+VCC3_3_2
+1.05VS_SATA3
+VCCSATAPLL
+VCCSATAPLL_R
+1.05VS_VCC_SATA
+VCCME_22
+VCCME_23
+VCCME_21
+VCCSUSHDA
Place CH80 Near AK1 pin
Security Classification
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Title
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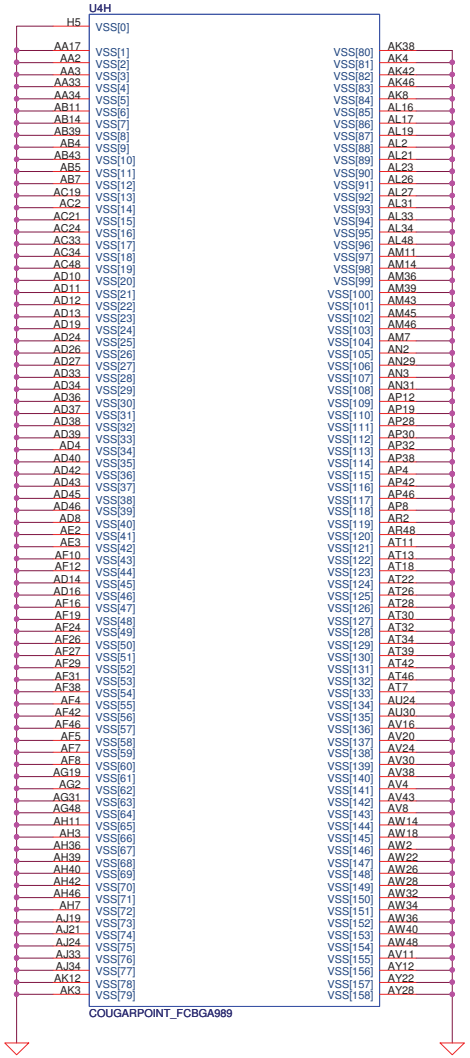

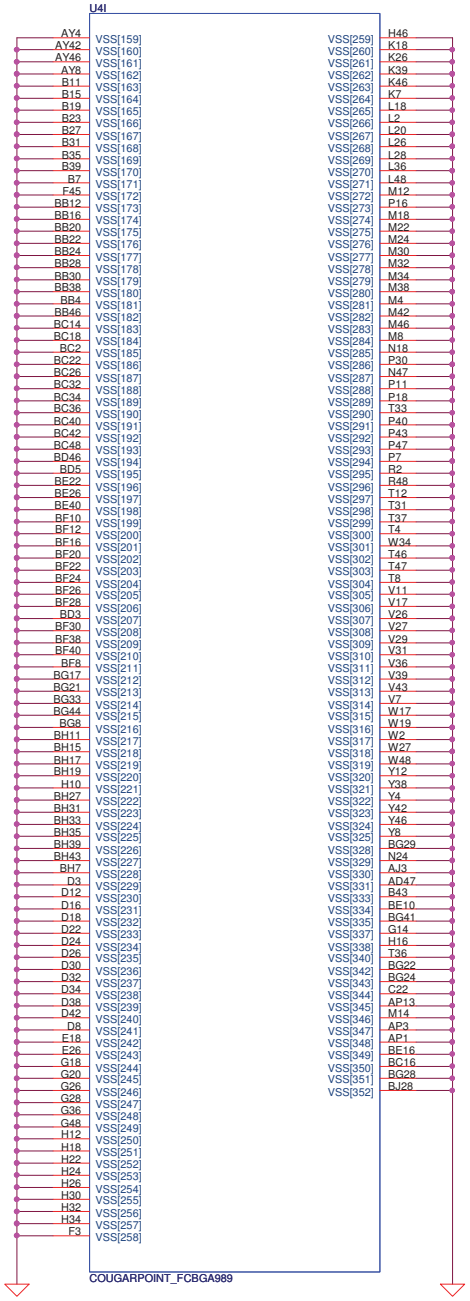

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Compal Electronics, Inc.

Title: PCH (9/9) VSS

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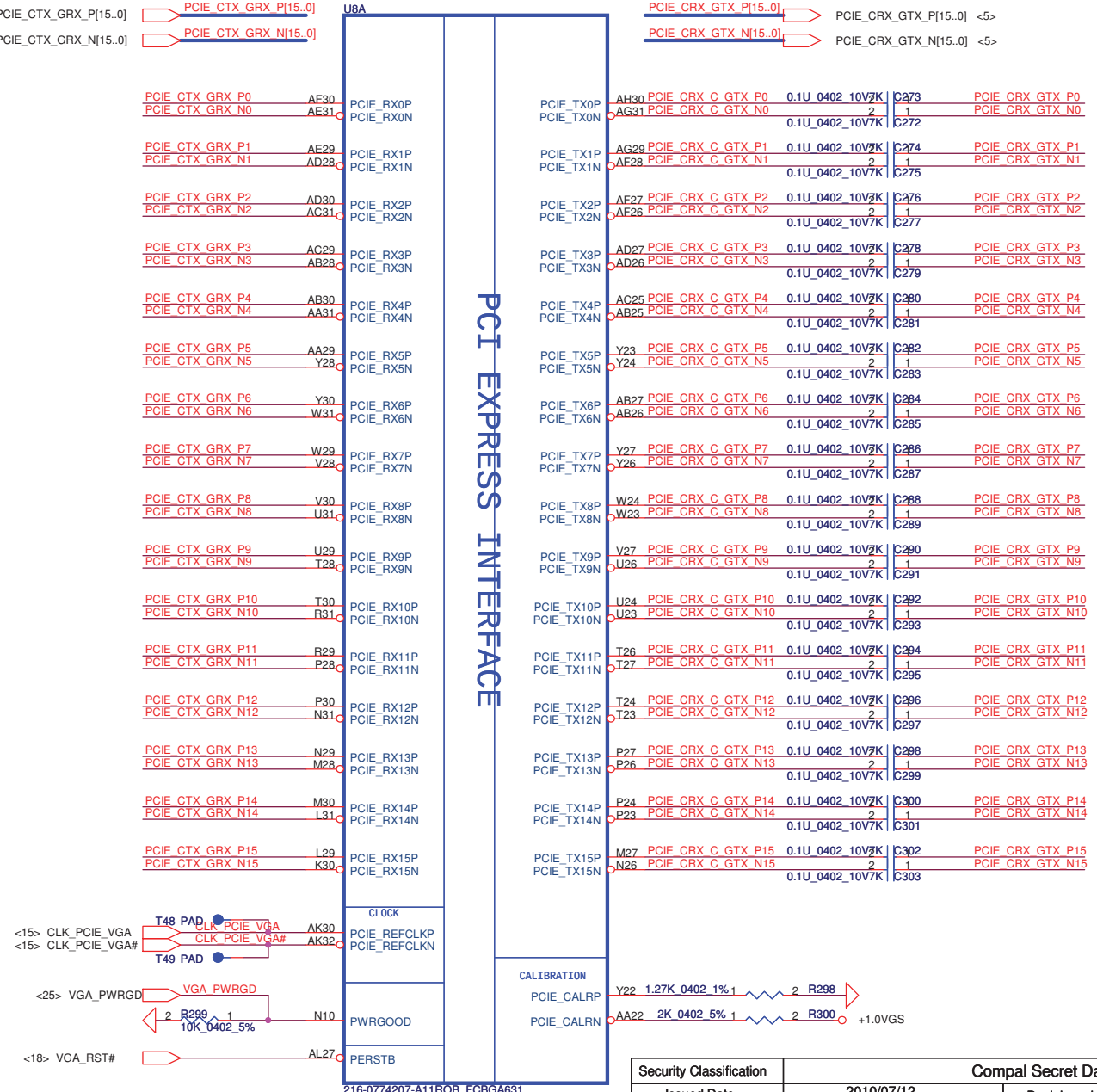
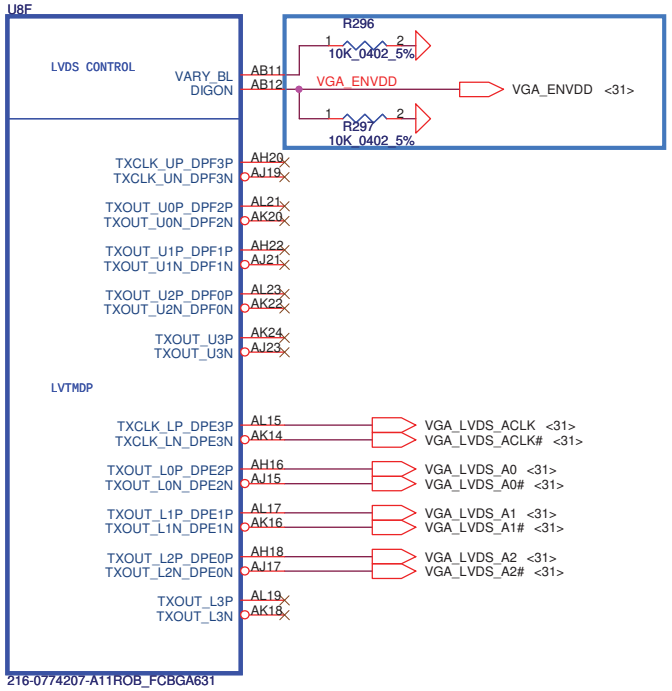


PCIE LANE



LVDS

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Compal Electronics, Inc.

Title: RobsonXT-S3 PCIE/LVDS

Size: B | Document Number | Rev: 0.1

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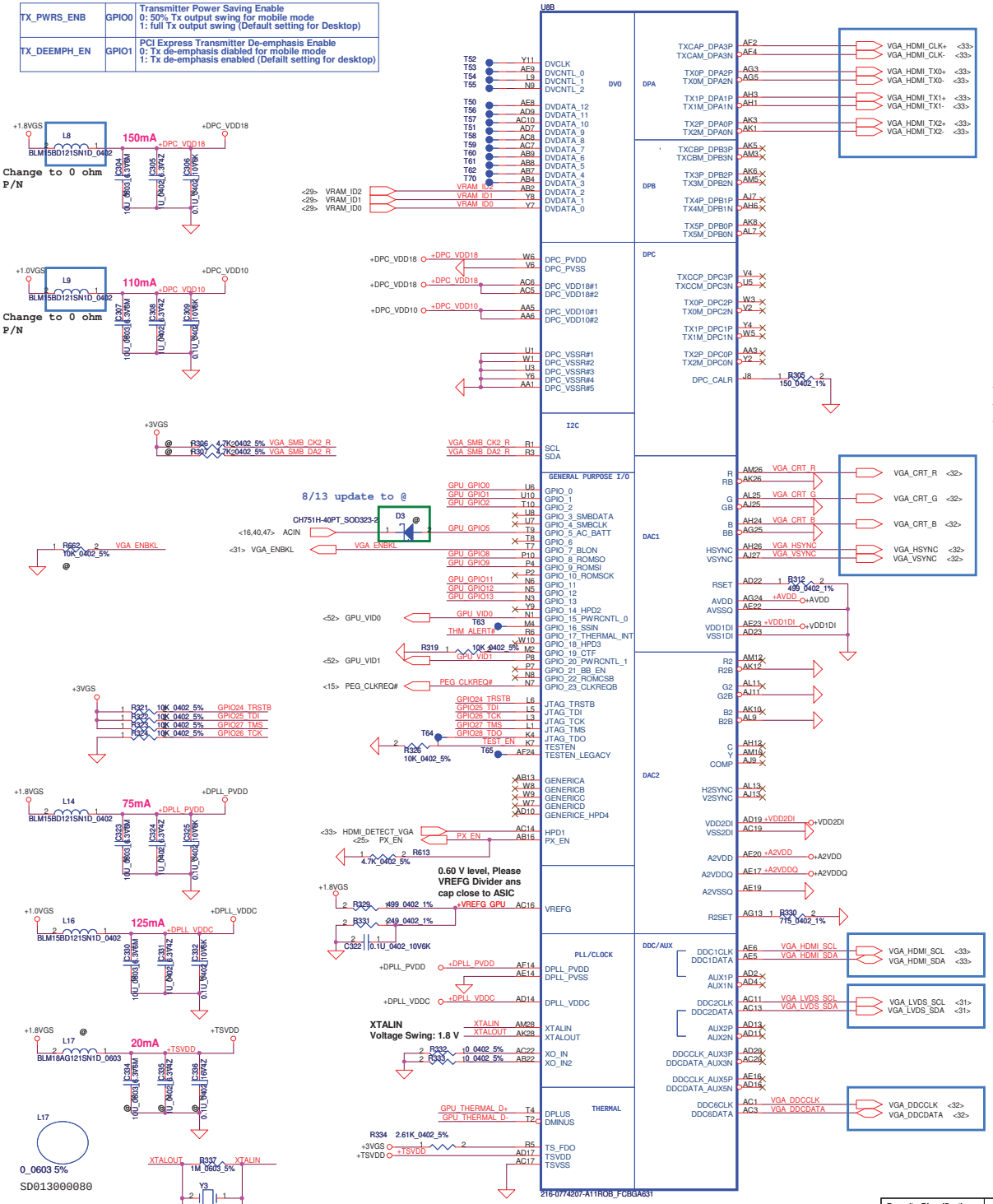
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

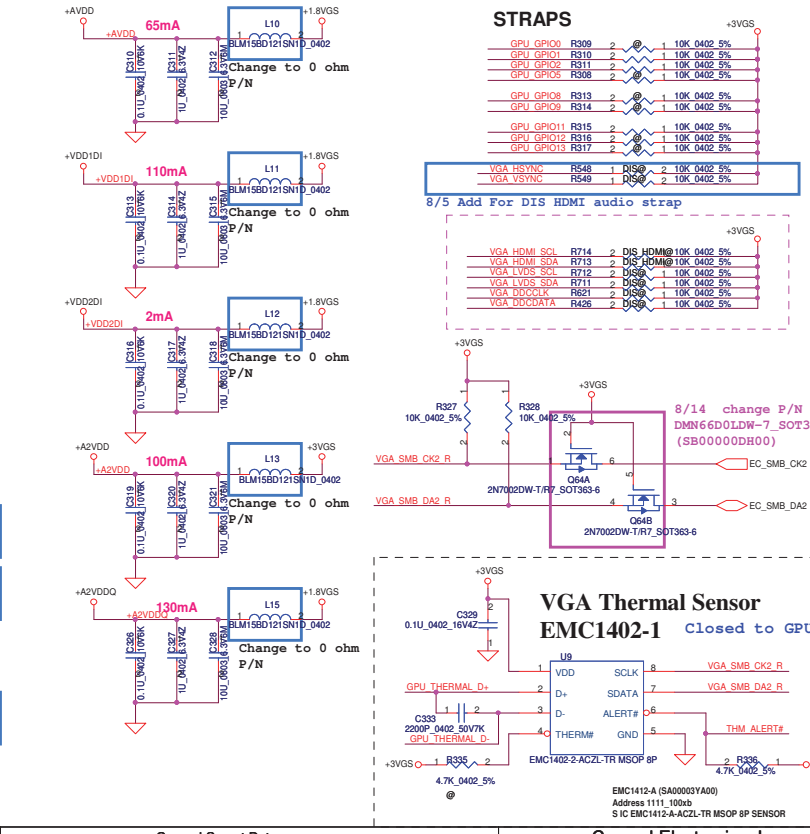
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8



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Compal Electronics, Inc.

Title: RobsonXT-S3 Main Generic/MSIC

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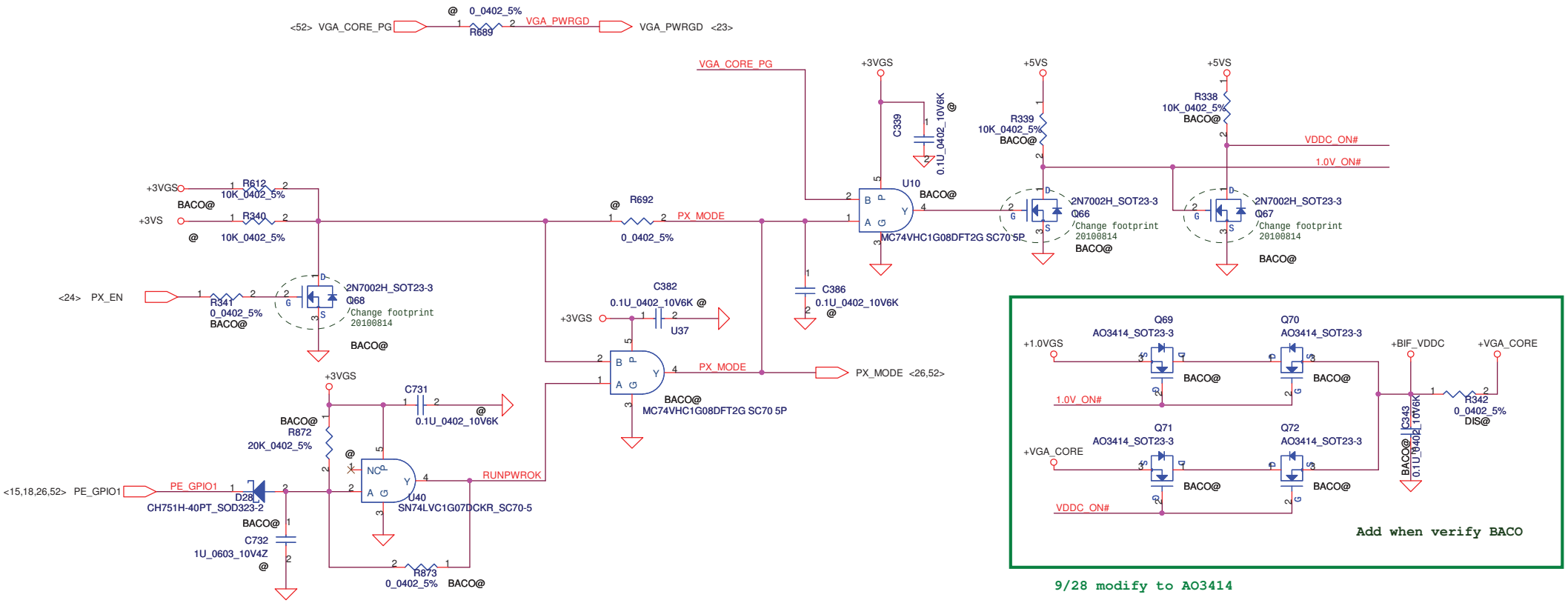

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Compal Electronics, Inc.

Title: PARK-S3 Main Generic/MSIC

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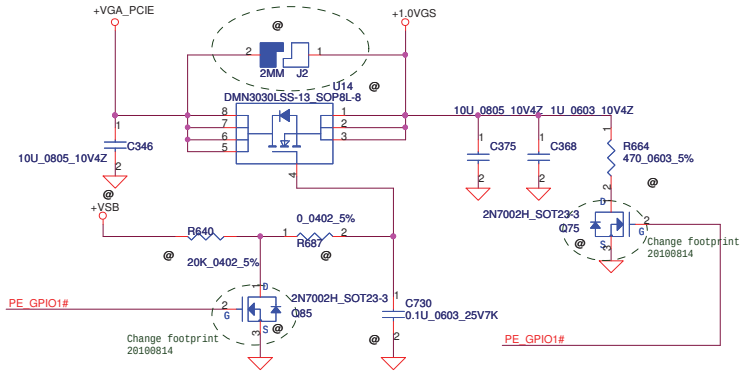
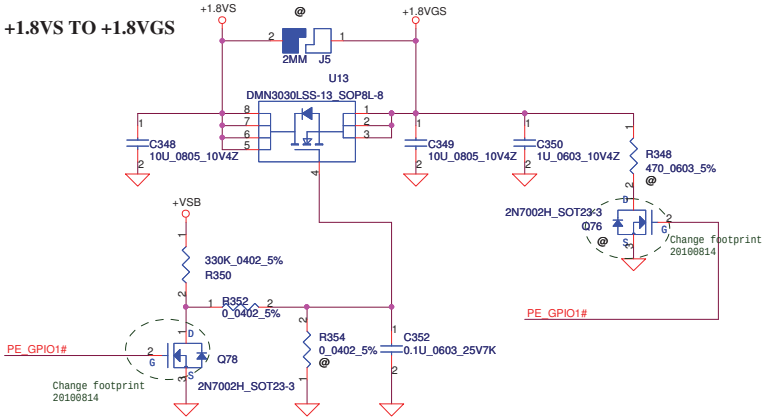
Short J2 for control sequence at PWM

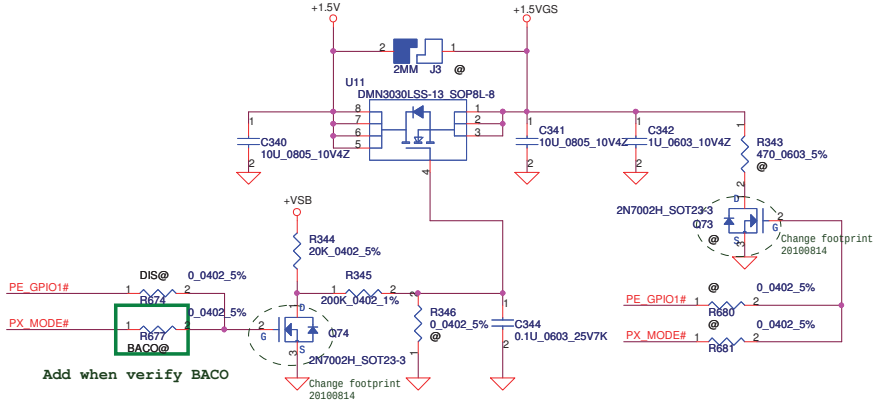
+VGA_PCIE TO +1.0VGS



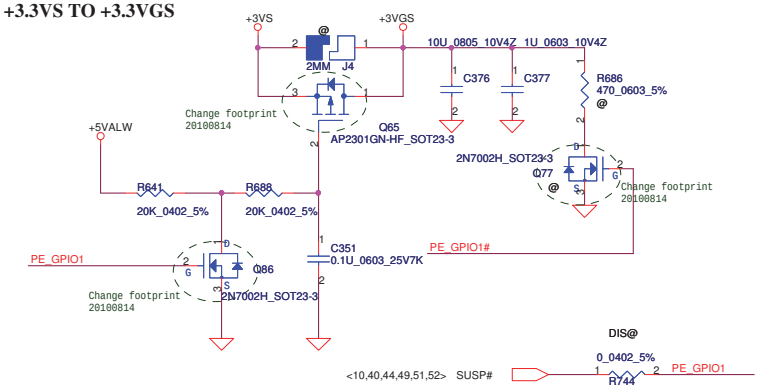
+1.8VS TO +1.8VGS

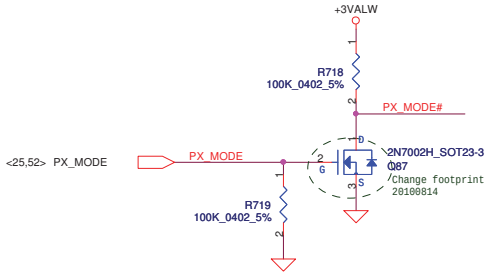


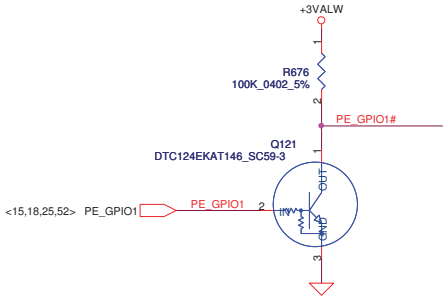
+1.5VS TO +1.5VGS



+3.3VS TO +3.3VGS







Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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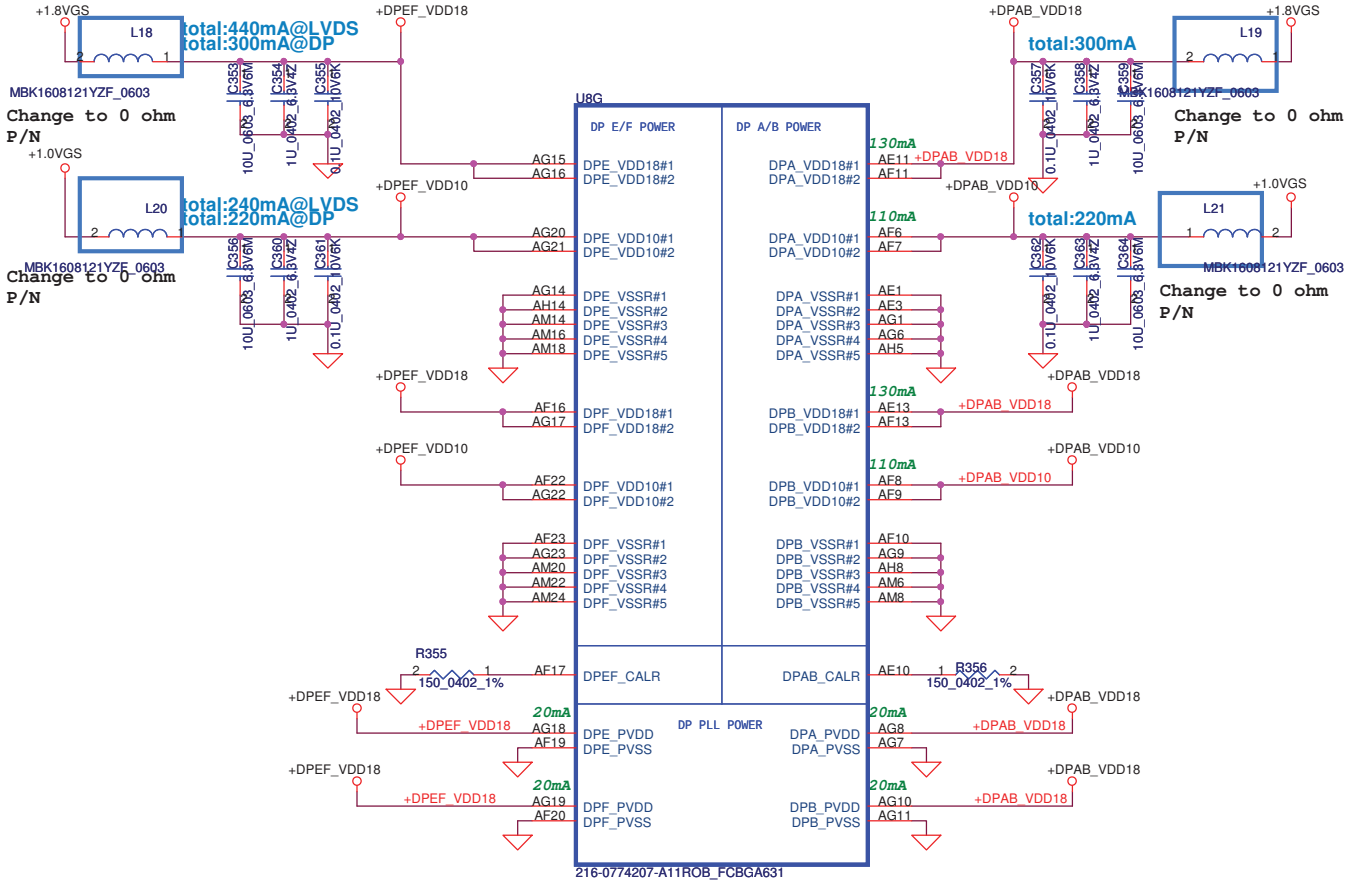
Compal Electronics, Inc.

Title: PARK-S3 Main Generic/MSIC

Size: Custom | Document Number: LA-6751P | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 26 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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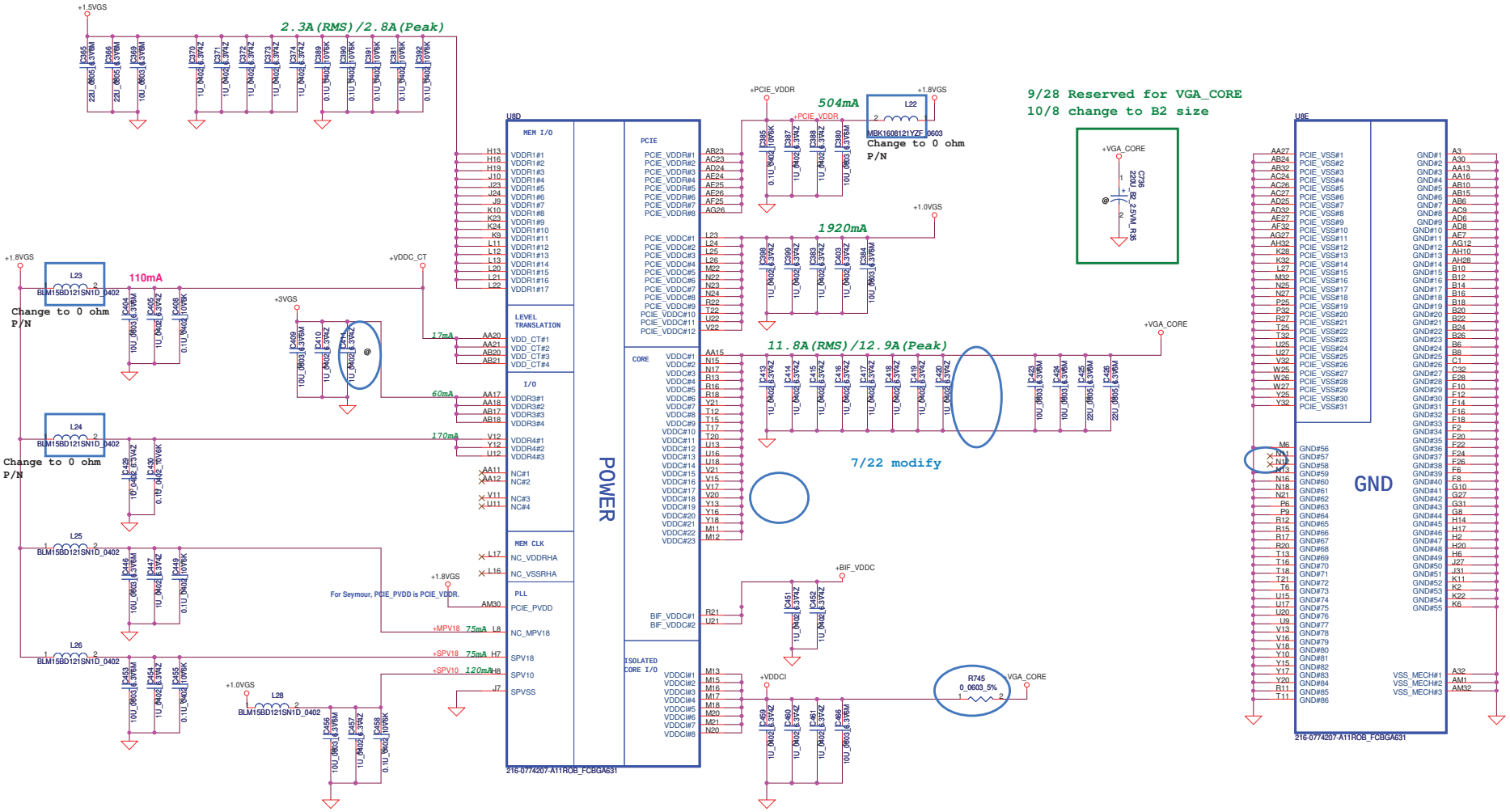
Compal Electronics, Inc.

Title: RobsonXT-S3 DP PWR

Size: B | Document Number | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 27 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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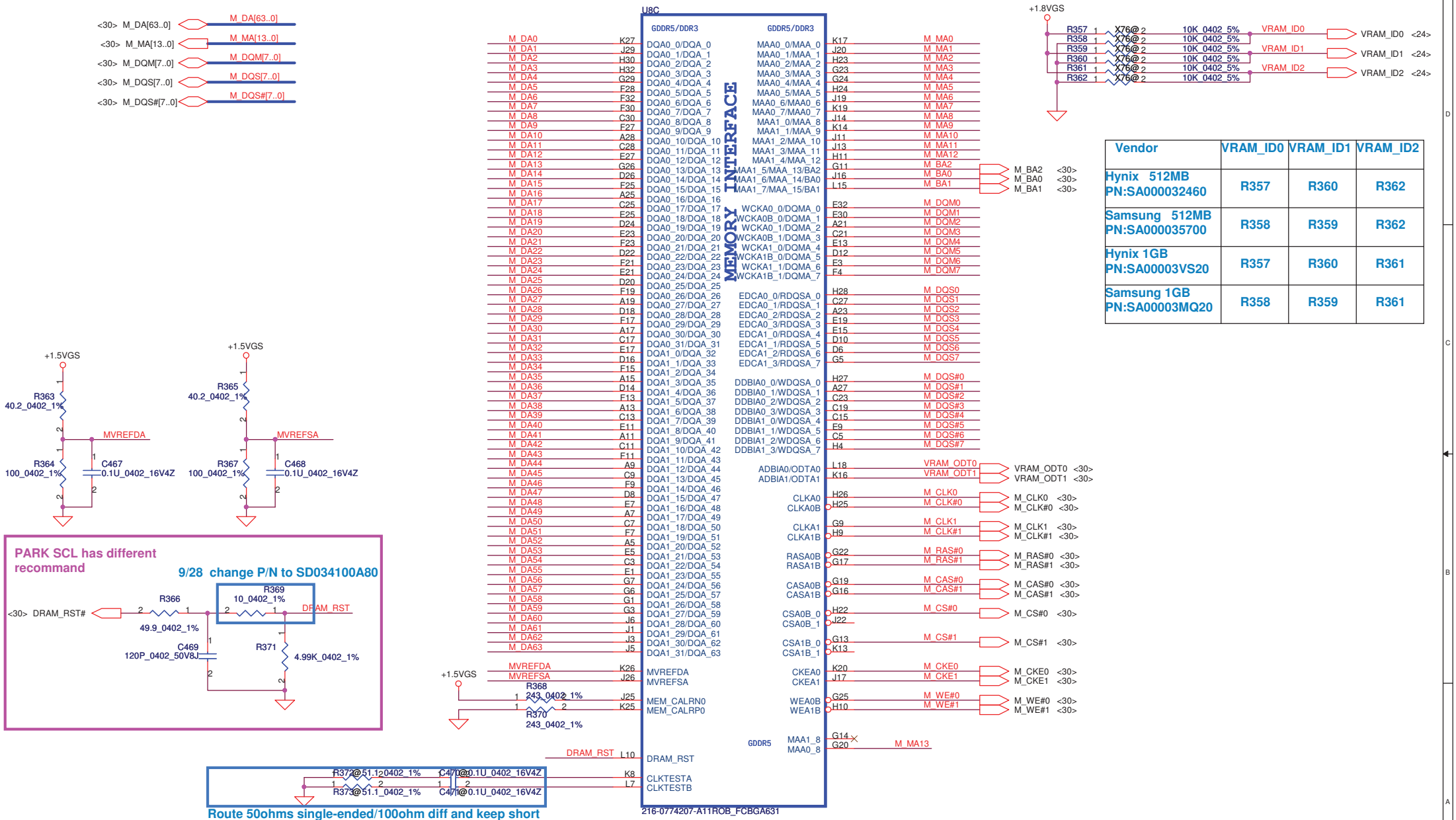
Compal Electronics, Inc.

Title: RobsonXT-S3 PWR/GND

Size	Document Number	Rev
C		0.2

Date: Friday, November 26, 2010 | Sheet 28 of 59



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 512MB PN:SA000032460	R357	R360	R362
Samsung 512MB PN:SA000035700	R358	R359	R362
Hynix 1GB PN:SA00003VS20	R357	R360	R361
Samsung 1GB PN:SA00003MQ20	R358	R359	R361

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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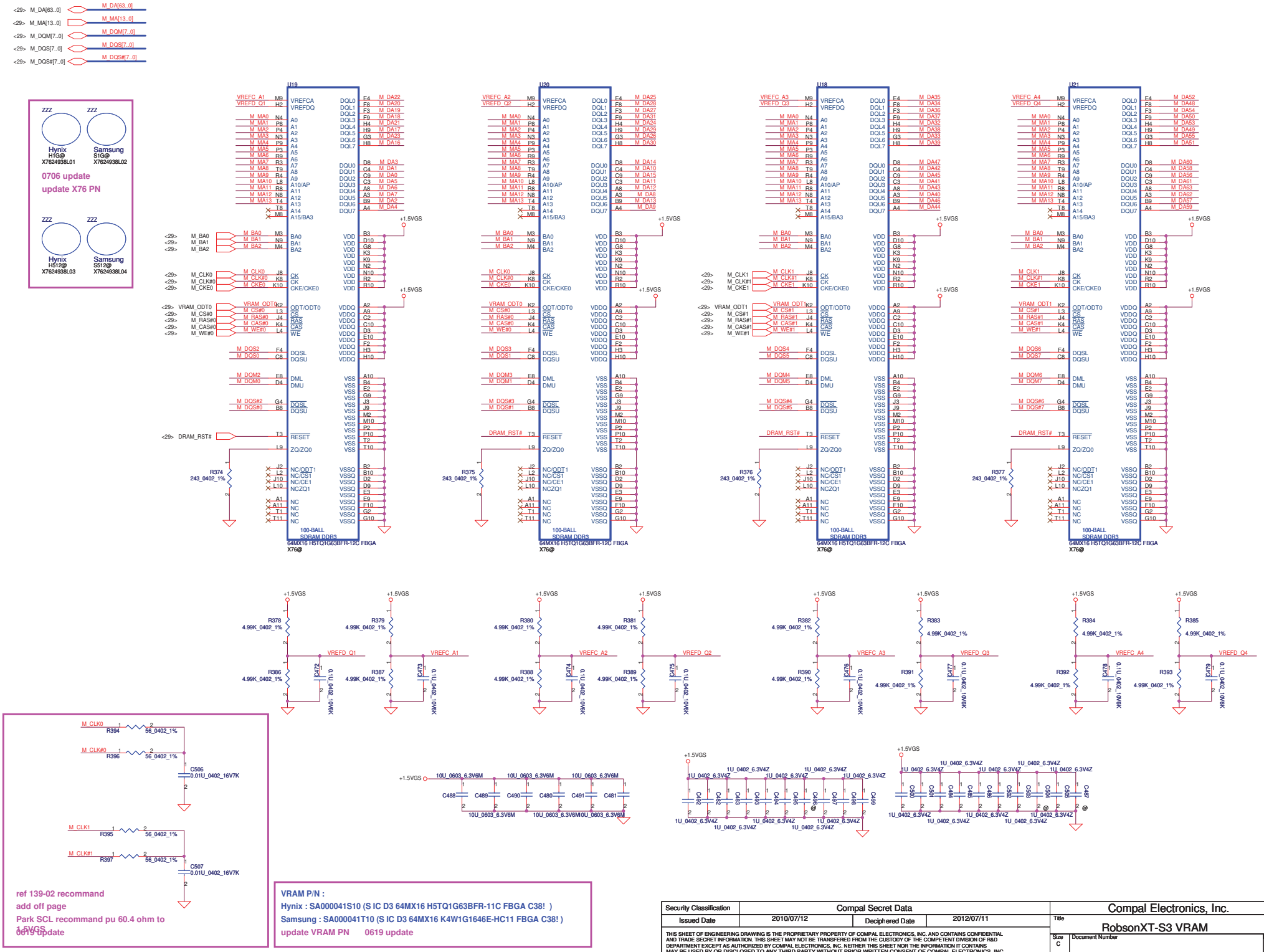
Compal Electronics, Inc.

Title: RobsonXT-S3 MEM Interface

Size: B | Document Number | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 29 of 59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Hynix H1G@ X7624938L01
Samsung S1G@ X7624938L02
Hynix H512@ X7624938L03
Samsung S512@ X7624938L04
0706 update
update X76 PN
U19
U20
U18
U21
100-BALL SDRAM DDR3
64MX16 H5TQ1G63BFR-12C FBGA
X76@
+1.5VGS
DRAM_RST#
R374 243_0402_1%
R375 243_0402_1%
R376 243_0402_1%
R377 243_0402_1%
R378 4.99K_0402_1%
R379 4.99K_0402_1%
R380 4.99K_0402_1%
R381 4.99K_0402_1%
R382 4.99K_0402_1%
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R393 4.99K_0402_1%
VREFD_Q1
VREFC_A1
VREFC_A2
VREFD_Q2
VREFC_A3
VREFD_Q3
VREFC_A4
VREFD_Q4
C472 0.1U_0402_10V6K
C473 0.1U_0402_10V6K
C474 0.1U_0402_10V6K
C475 0.1U_0402_10V6K
C476 0.1U_0402_10V6K
C477 0.1U_0402_10V6K
C478 0.1U_0402_10V6K
C479 0.1U_0402_10V6K
R394 56_0402_1%
R396 56_0402_1%
C506 0.01U_0402_16V7K
R395 56_0402_1%
R397 56_0402_1%
C507 0.01U_0402_16V7K
10U_0603_6.3V6M
C488
C489
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C480
C491
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1U_0402_6.3V4Z
C482
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C496
C497
C498
C499
C500
C501
C504
C505
C502
C503
C506
C507
ref 139-02 recommand
add off page
Park SCL recommand pu 60.4 ohm to 1.5VGS
0619 update
VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update
Security Classification
Compal Secret Data
Issued Date
2010/07/12
Deciphered Date
2012/07/11
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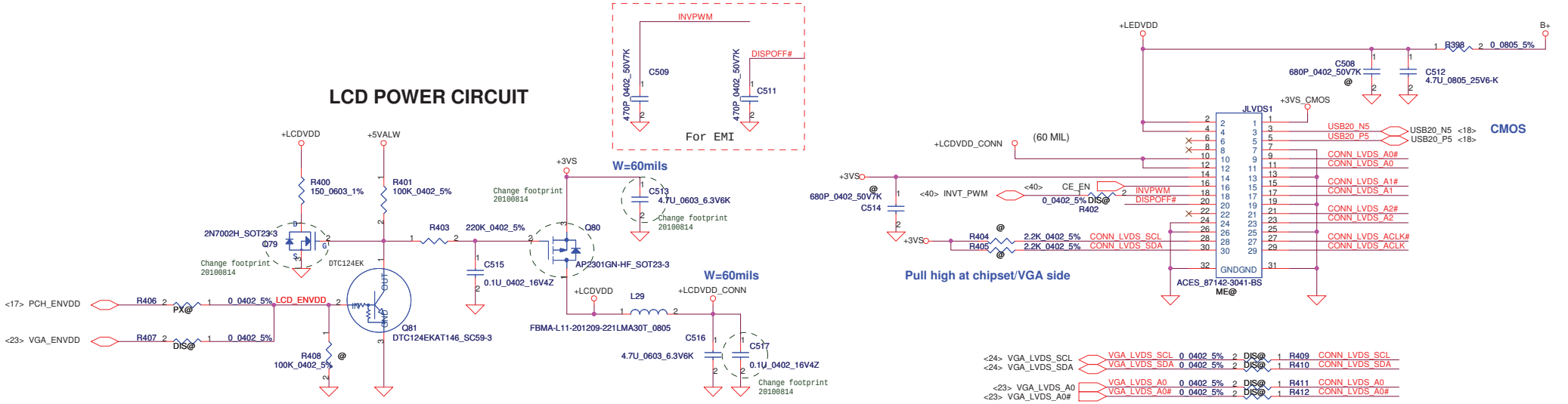
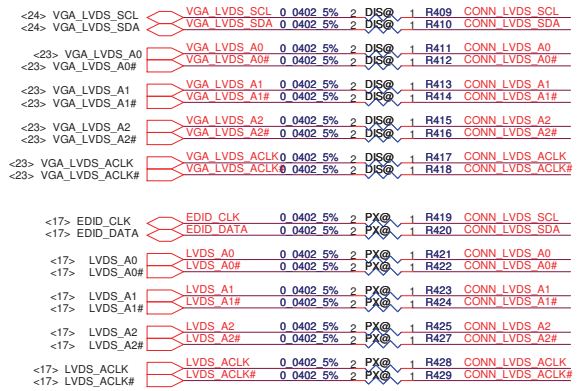
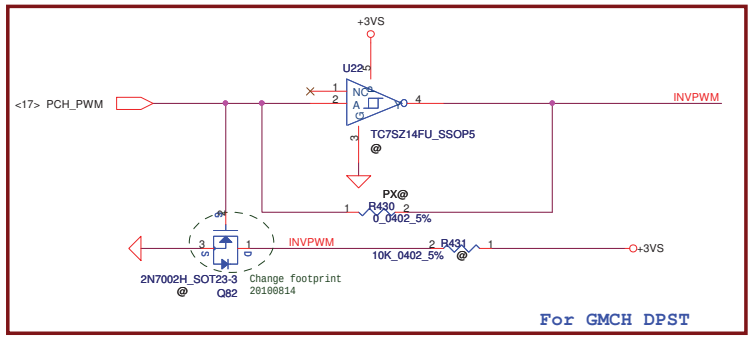
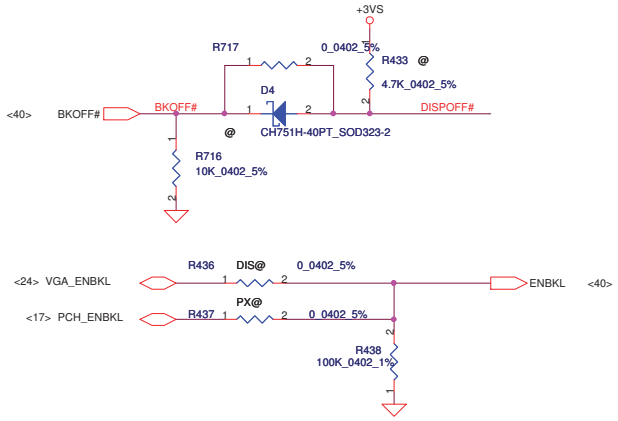
Compal Electronics, Inc.
Title
RobsonXT-S3 VRAM
Size C
Document Number
Rev 0.2
Date: Friday, November 26, 2010
Sheet 30 of 59

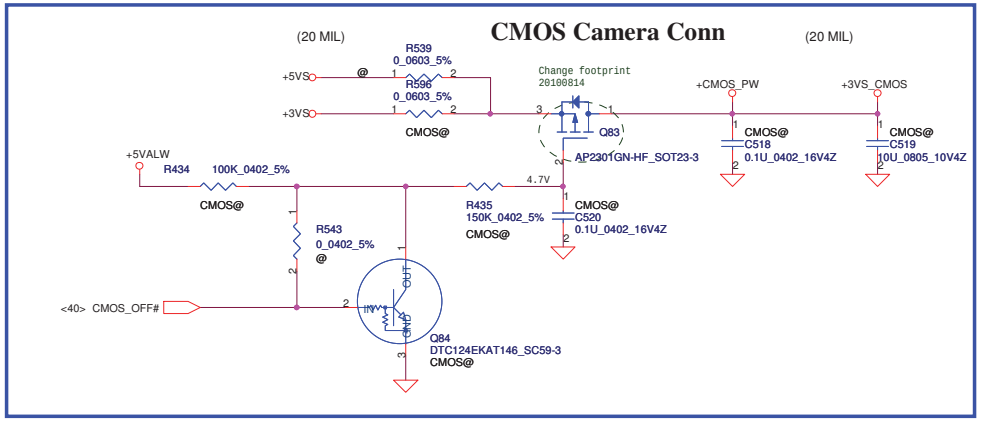
LCD POWER CIRCUIT











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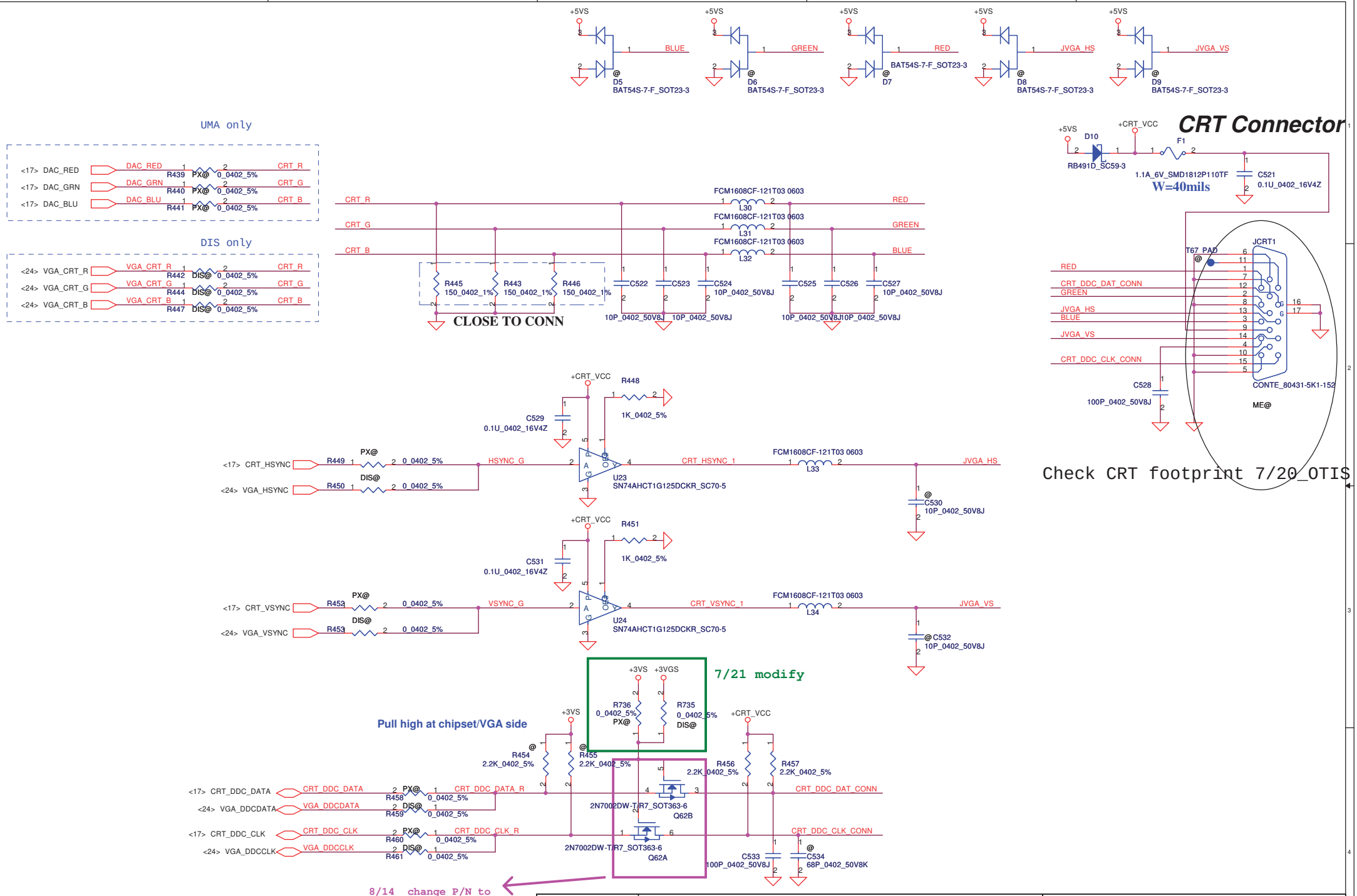
Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size: B | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 31 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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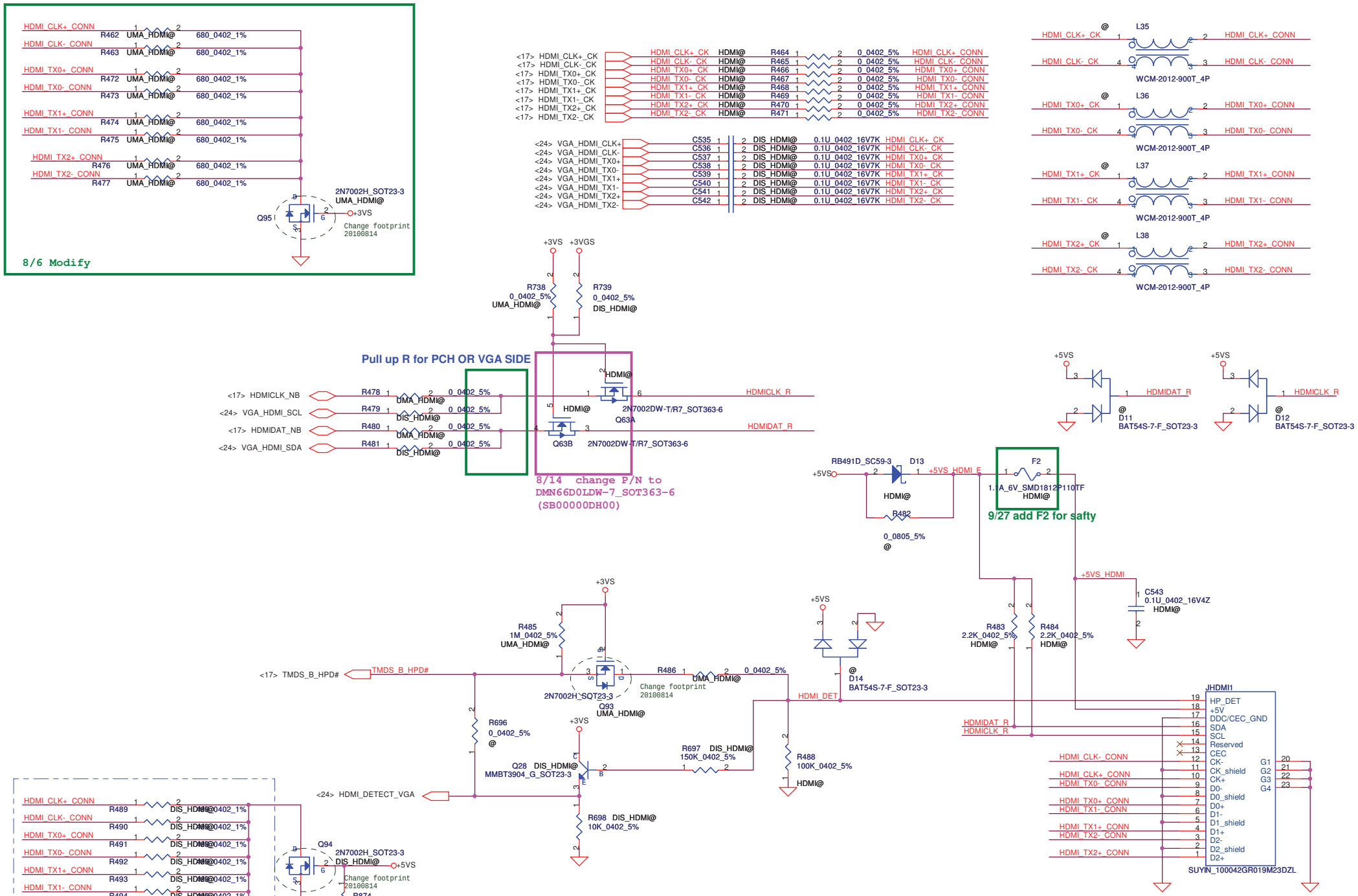
Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 32 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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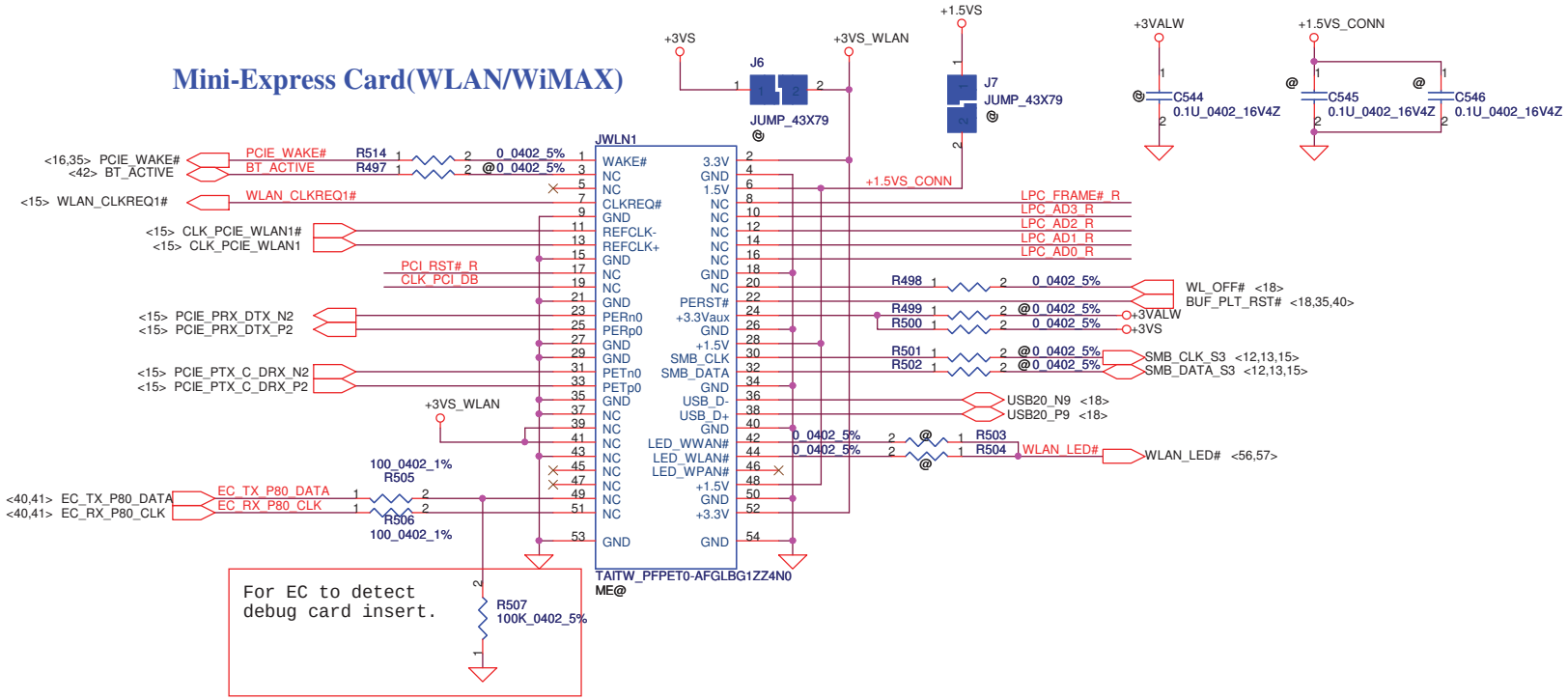
Compal Electronics, Ltd.

Title: **HDMI CONN**

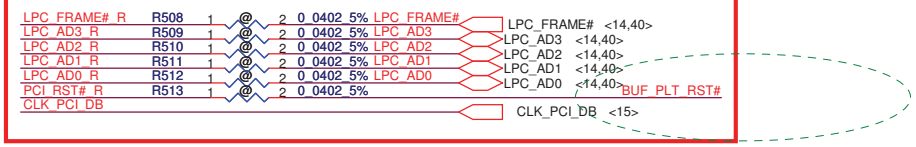
Size: Custom | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 33 of 59

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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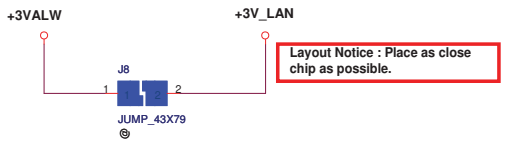
Compal Electronics, Inc.

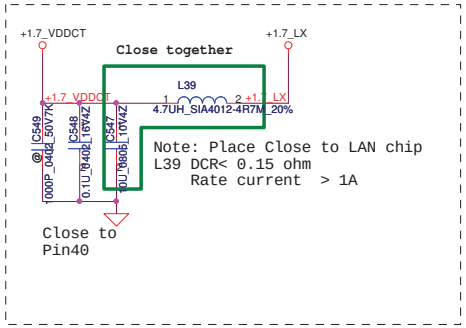
Title: **Mini-Card/NEW Card/SIM**

Size | Document Number: **LA-6751P** | Rev 0.2

Date: Friday, November 26, 2010 | Sheet 34 of 59

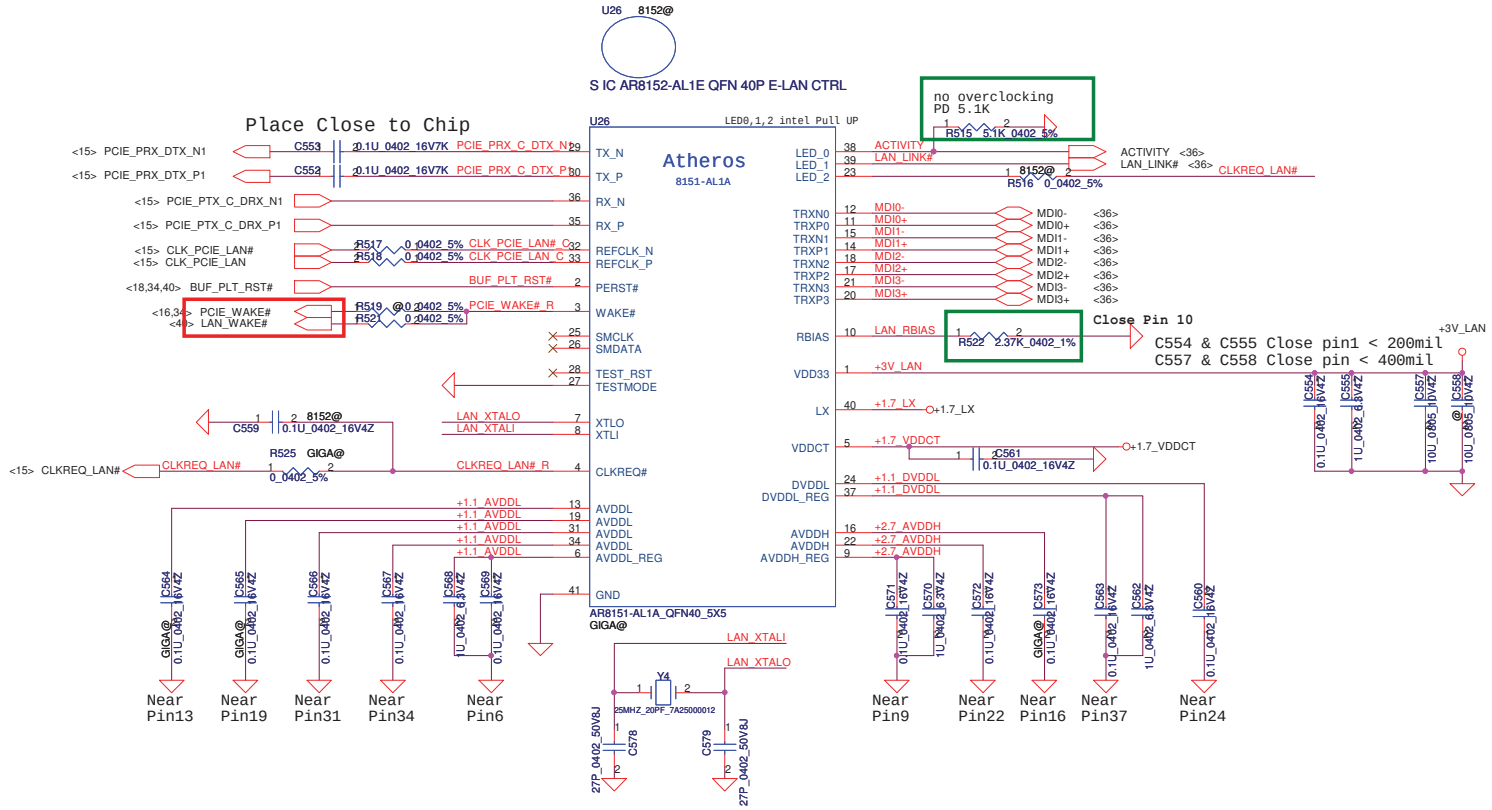


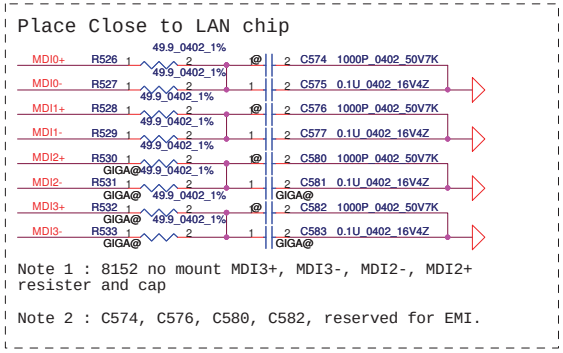
Atheros request can't disable LAN power



Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--





	Pin4	Configure R525	Configure C559		Pin23	Configure R516
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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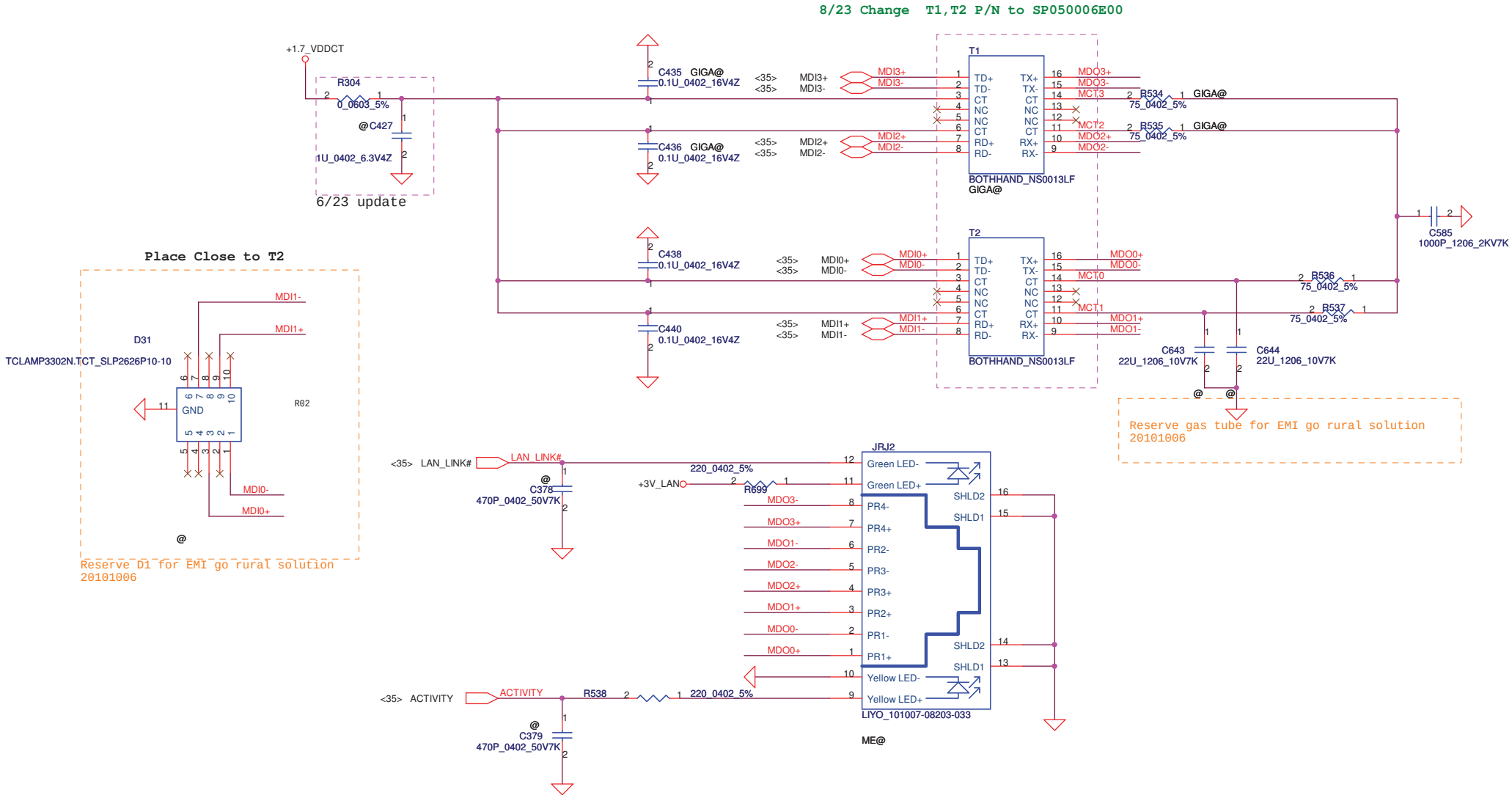
Compal Electronics, Inc.

Title: LAN-AR8151/8152

Size: Custom | Document Number: LA-6751P | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 35 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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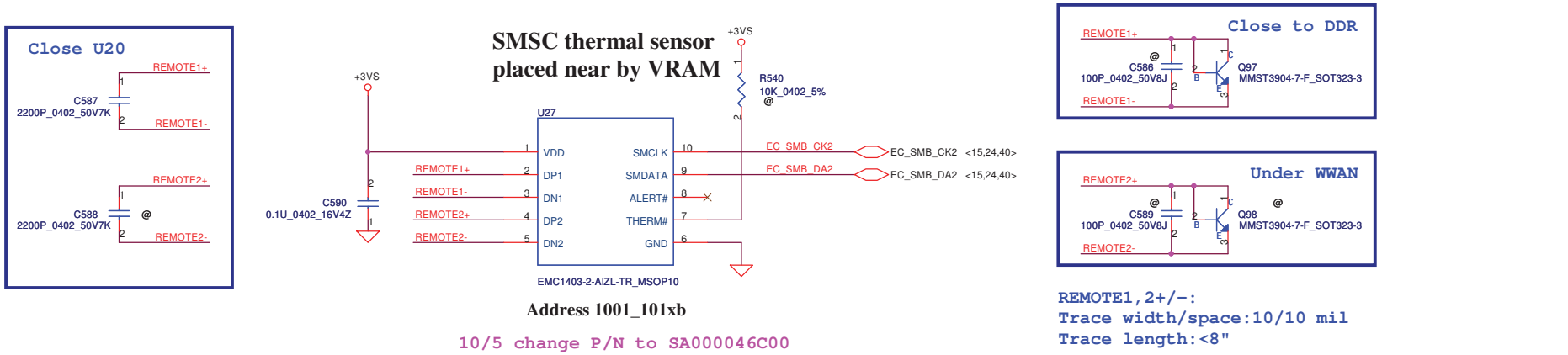
Compal Electronics, Inc.

Title: **LAN_Transformer**

Size: B | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 36 of 59

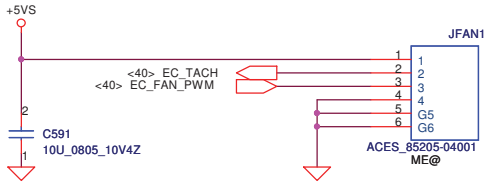


Address 1001_101xb

10/5 change P/N to SA000046C00

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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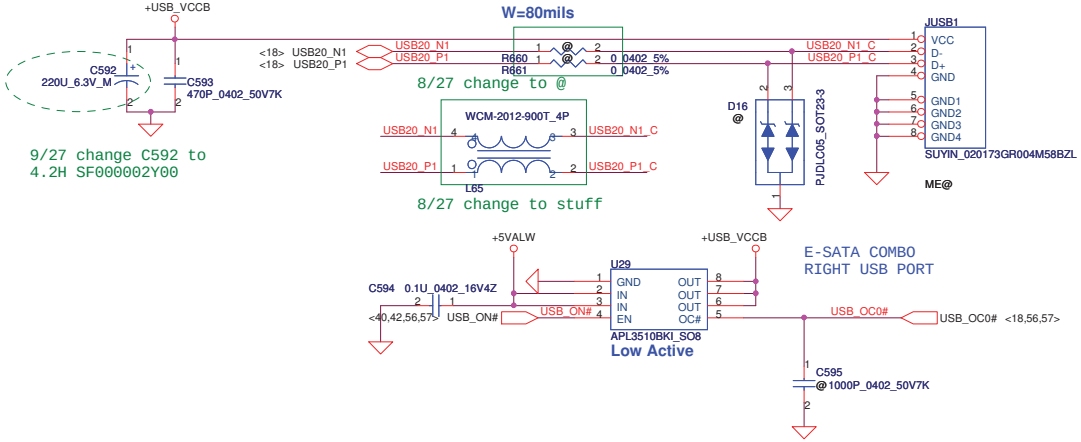
Compal Electronics,Ltd.

Title: EMC1403_Thermal sensor/FAN

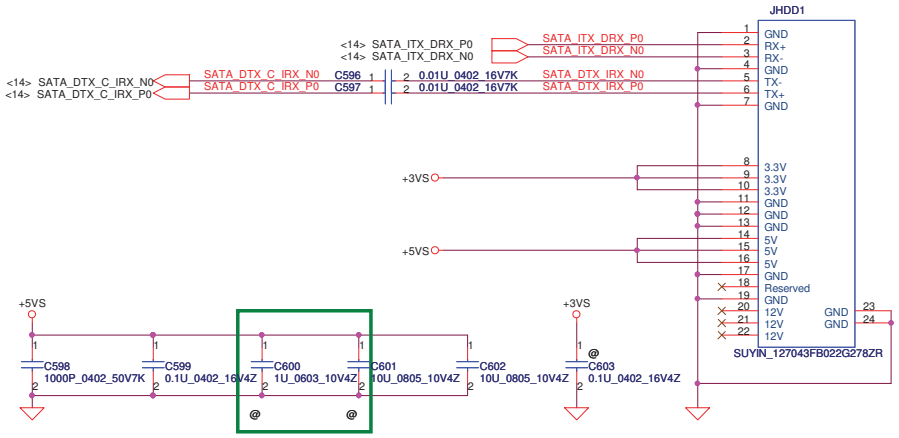
Size: Custom | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 37 of 59

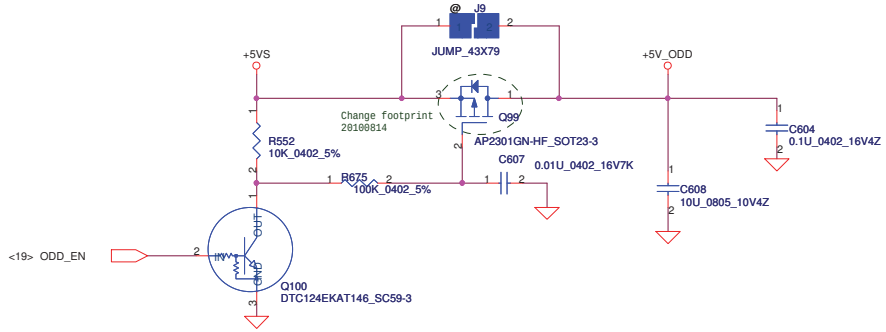
Left USB Conn.



SATA HDD Conn.



ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

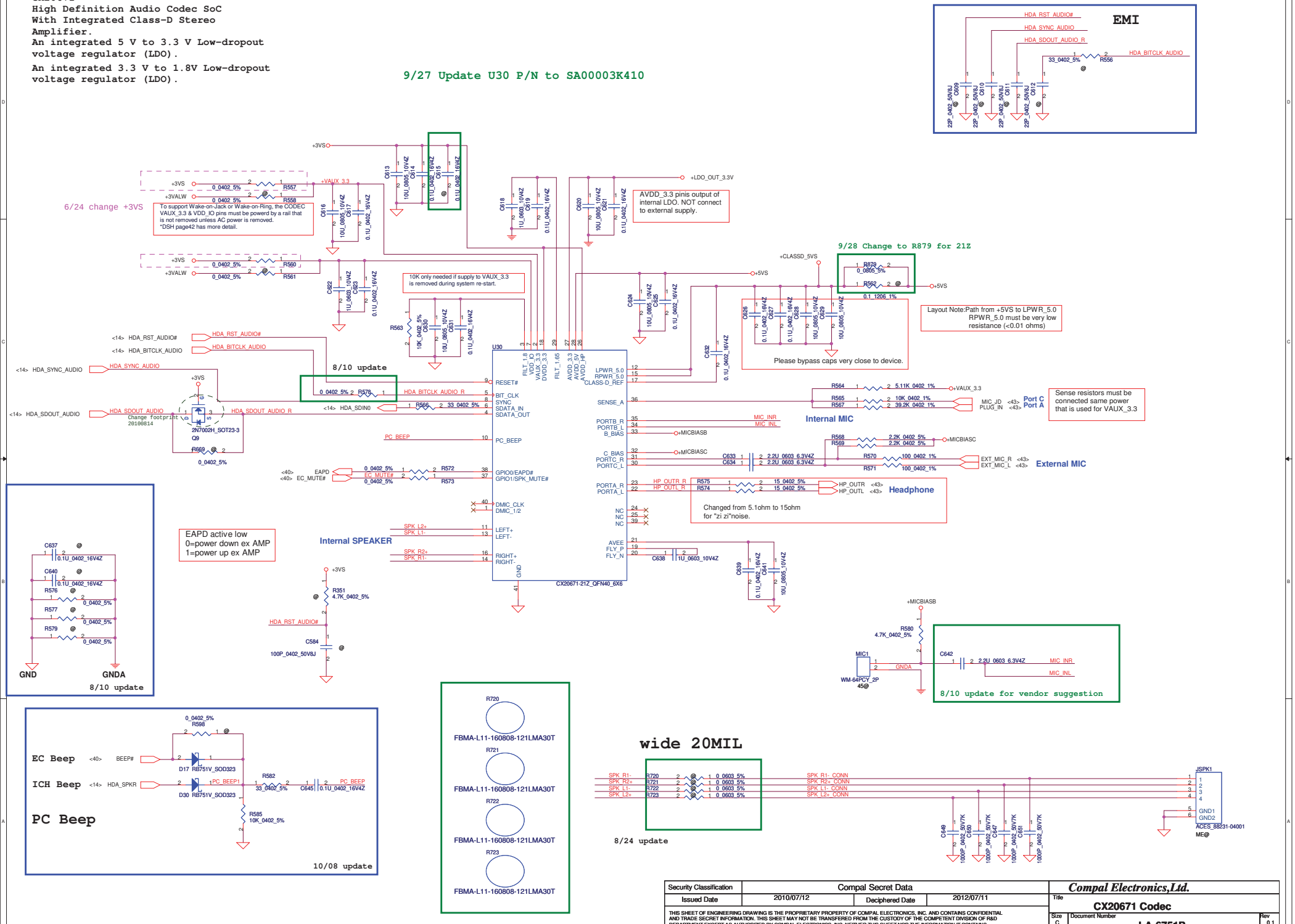
Title: HDD/ODD Connector

Size: B | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 38 of 59

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

9/27 Update U30 P/N to SA00003K410



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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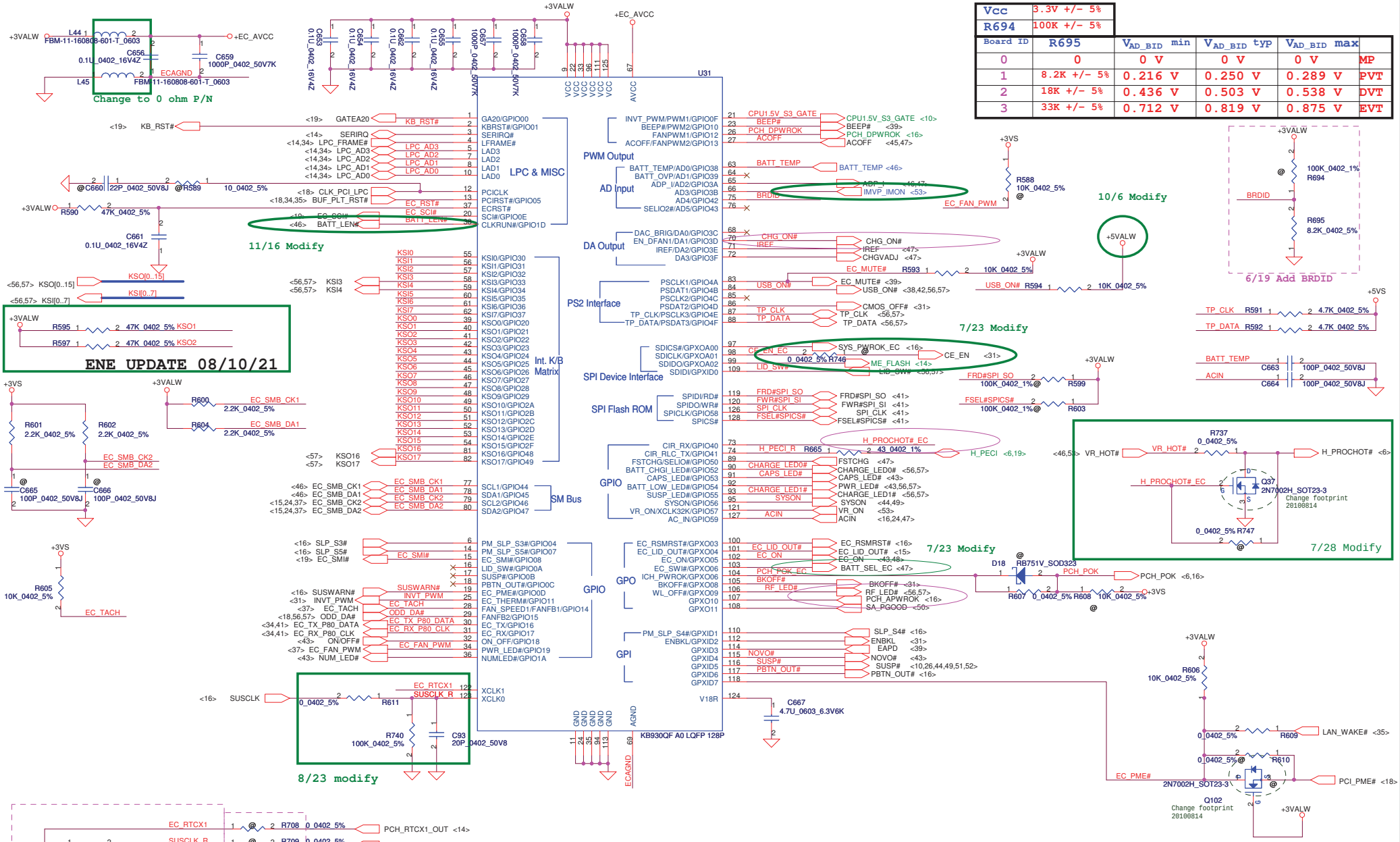
Compal Electronics,Ltd.

Title: CX20671 Codec

Size: C | Document Number: LA-6751P | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 39 of 59



Vcc	3.3V +/- 5%
R694	100K +/- 5%

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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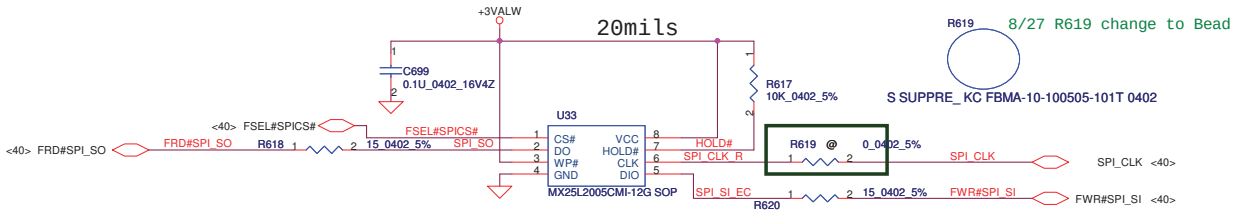
Compal Electronics, Inc.

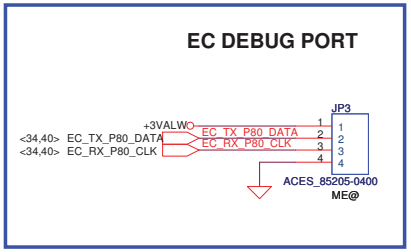
Title: **BIOS & EC I/O Port**

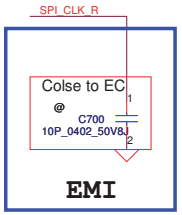
Size: Custom | Document Number: **LA-6751P** | Rev: 0.2

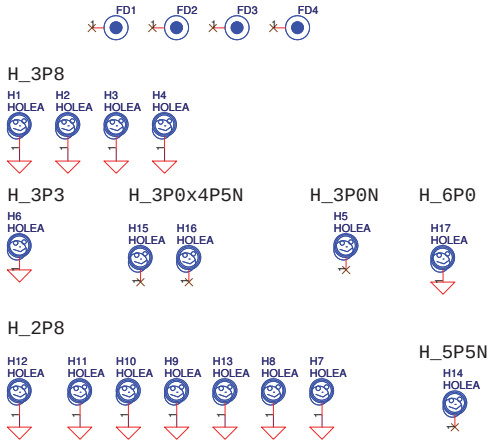
Date: Friday, November 26, 2010 | Sheet 40 of 59

FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00









Security Classification	Compal Secret Data		
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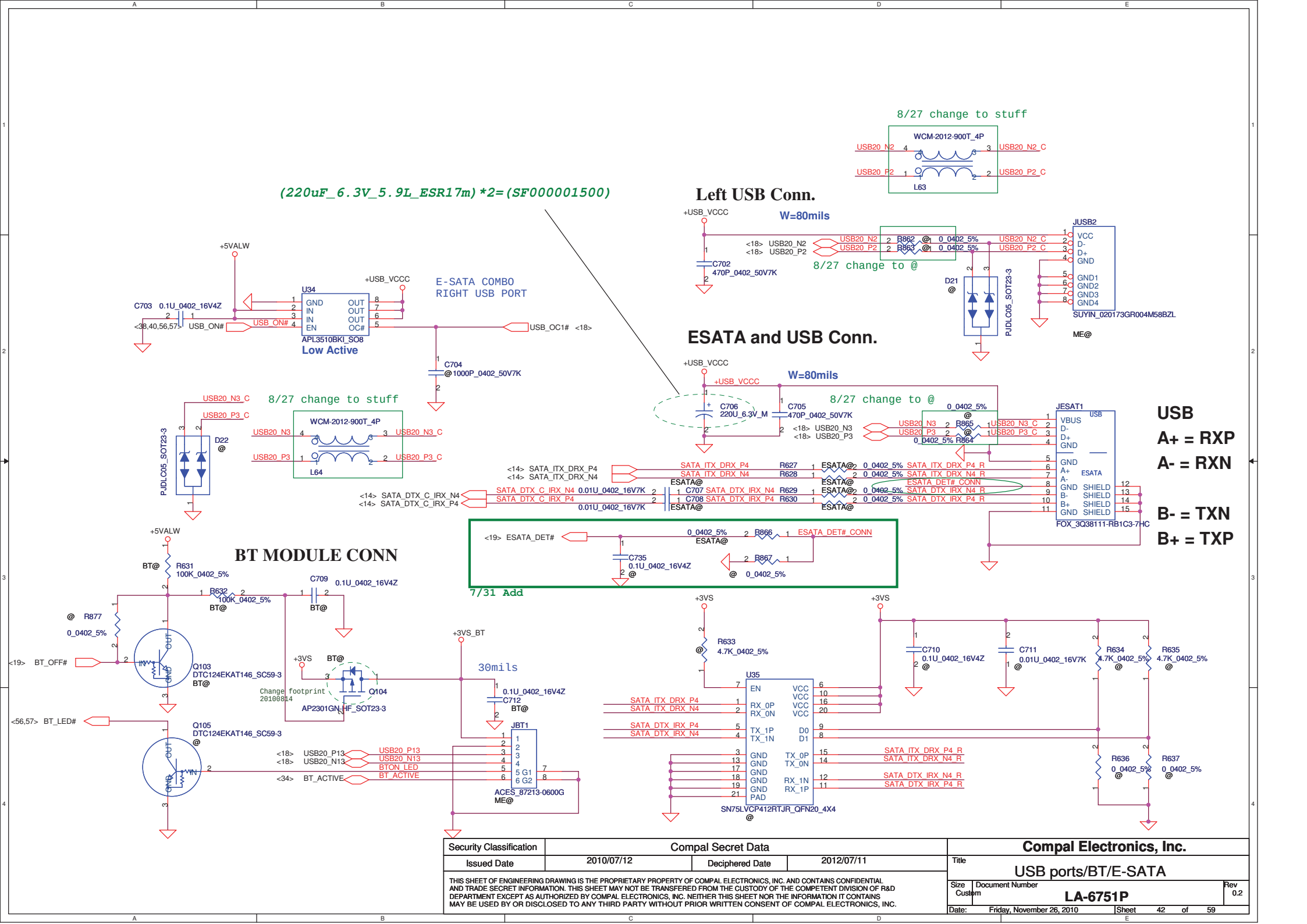
Compal Electronics, Inc.

Title: **LED/EC SPI ROM**

Size: B | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 41 of 59



Security Classification	Compal Secret Data		
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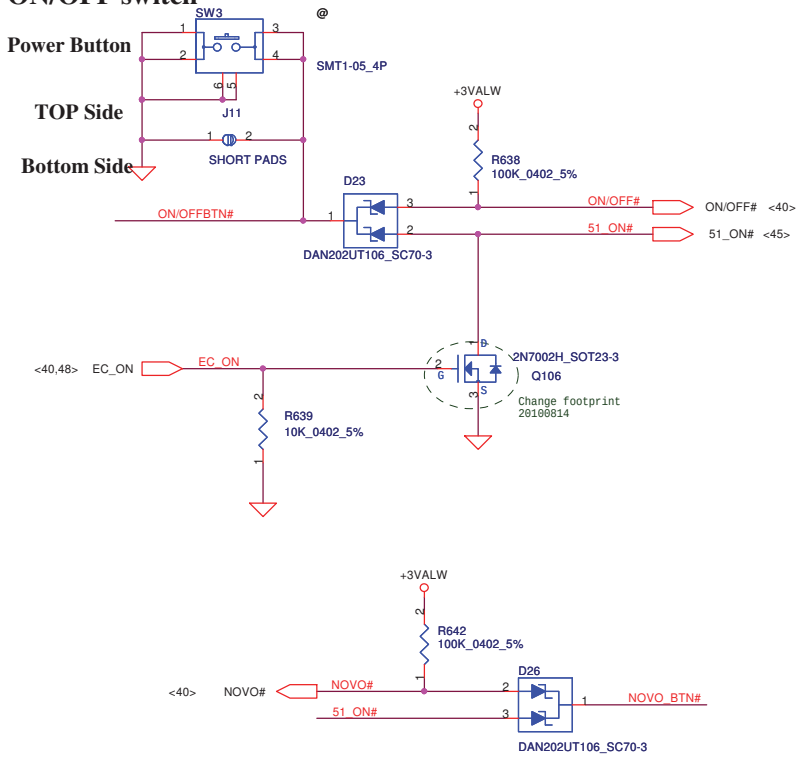
Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

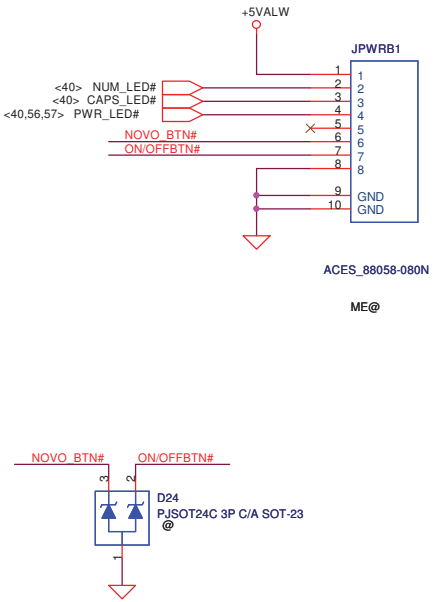
Size: Custom | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 42 of 59

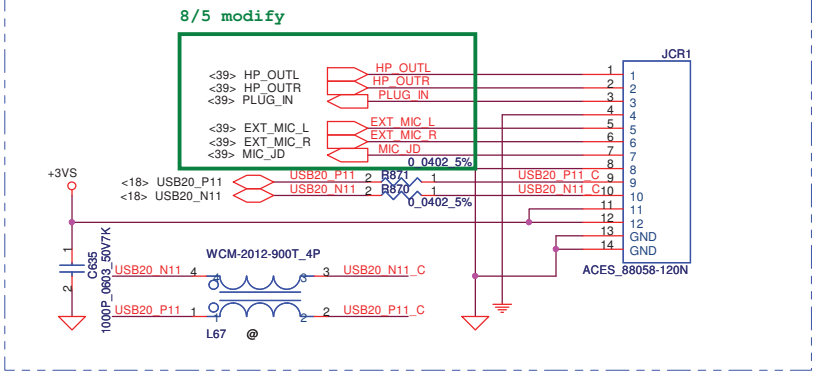
ON/OFF switch



Power Bottom Board Conn. 8pin



Card Reader/Audio Jack SB CONN



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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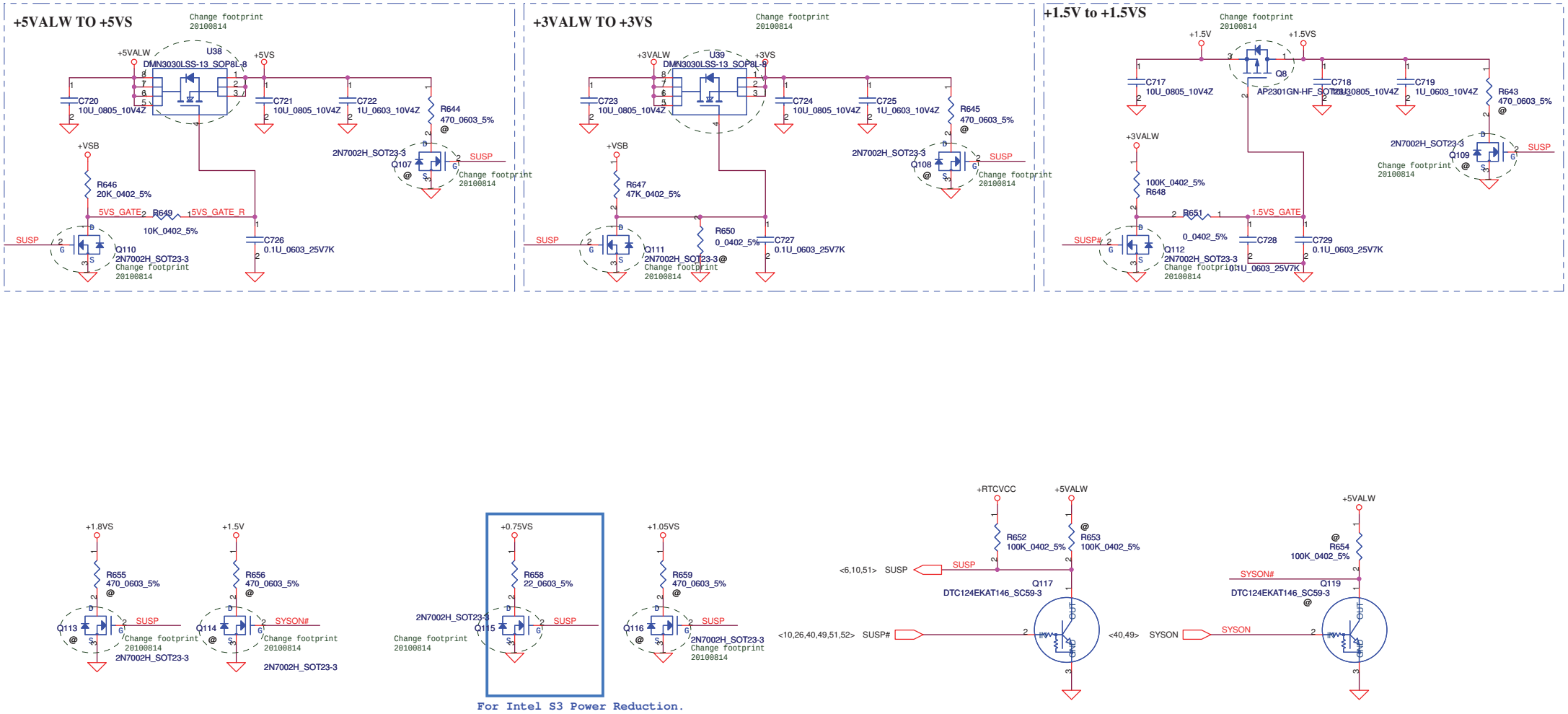
Compal Electronics,Ltd.

Title: **other IO connector**

Size: Custom | Document Number: **LA-6751P** | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 43 of 59



For Intel S3 Power Reduction.

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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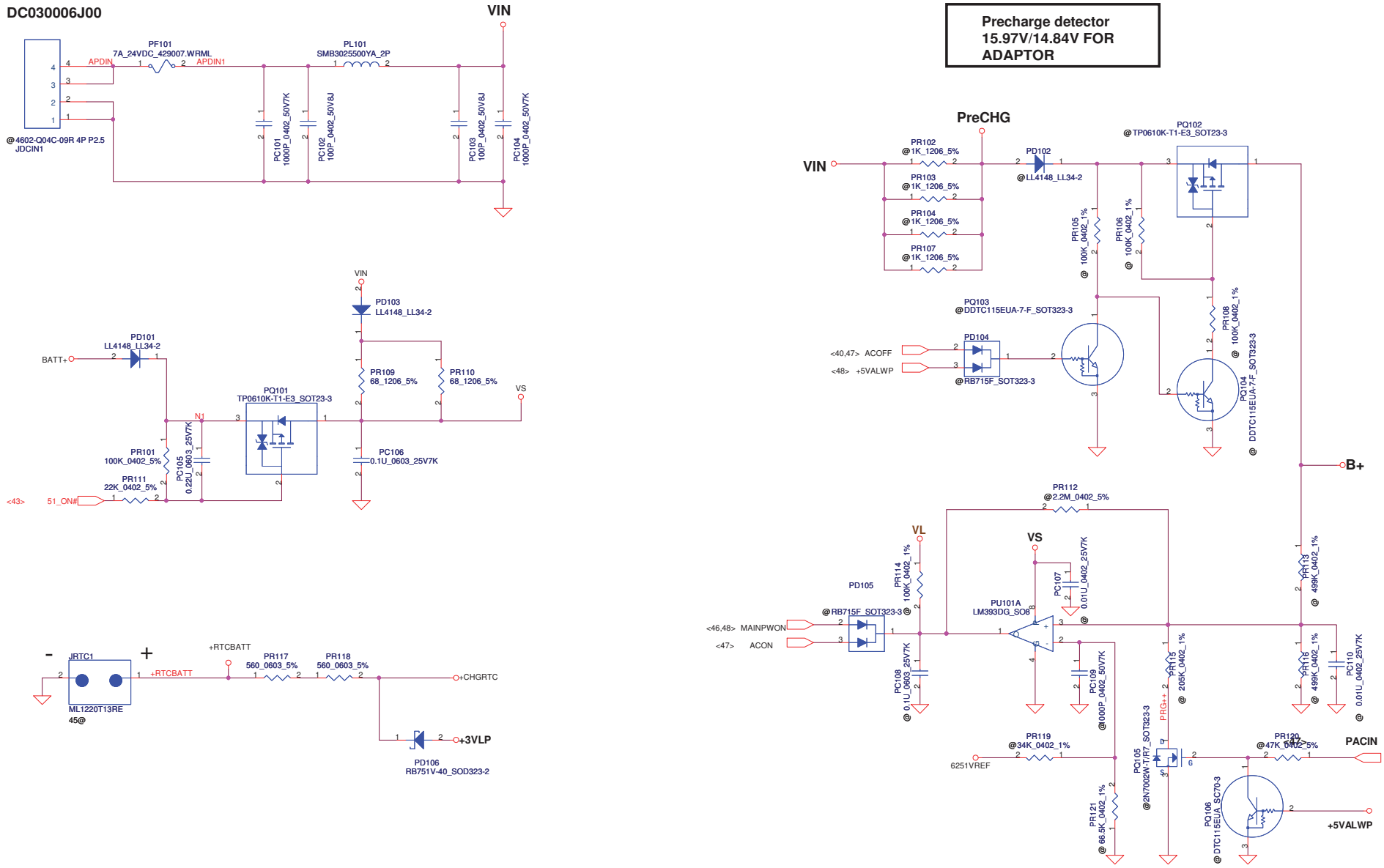
Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-6751P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 44 of 59



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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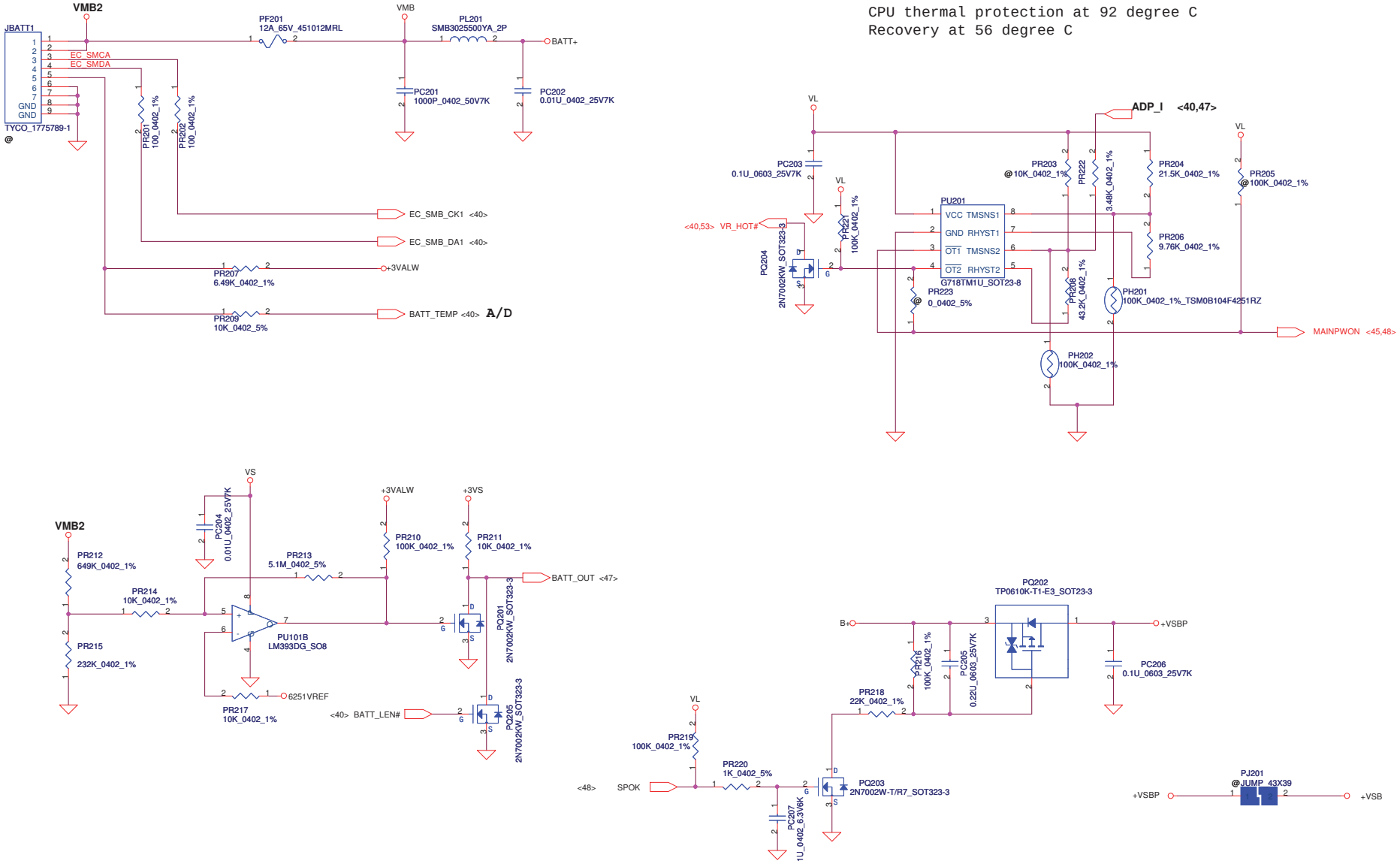
Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 45 of 54

PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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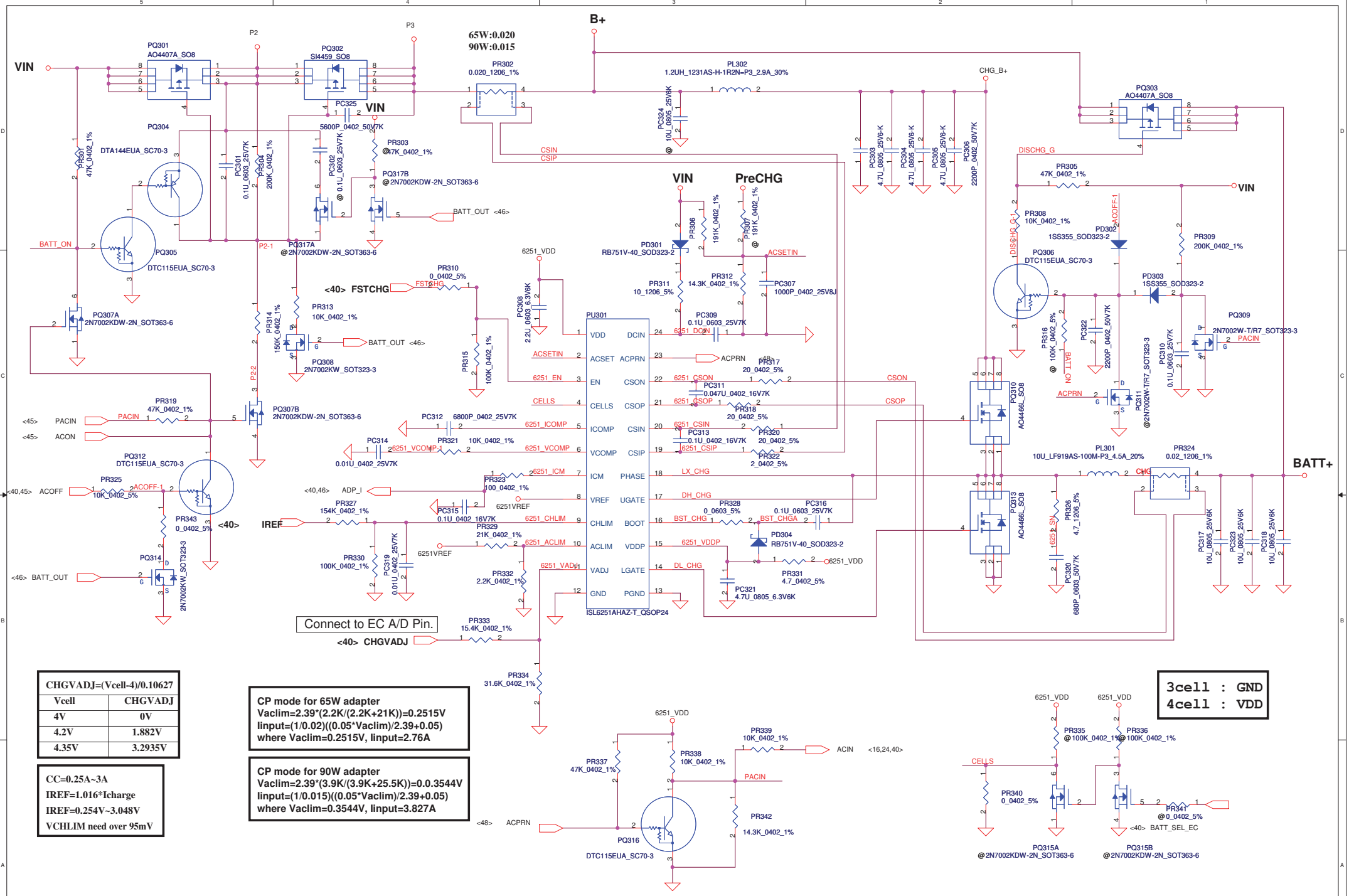
Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size: Custom | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 46 of 54



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CP mode for 65W adapter
Vaclim=2.39*(2.2K/(2.2K+21K))=0.2515V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2515V, Iinput=2.76A

CP mode for 90W adapter
Vaclim=2.39*(3.9K/(3.9K+25.5K))=0.0.3544V
Iinput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.3544V, Iinput=3.827A

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

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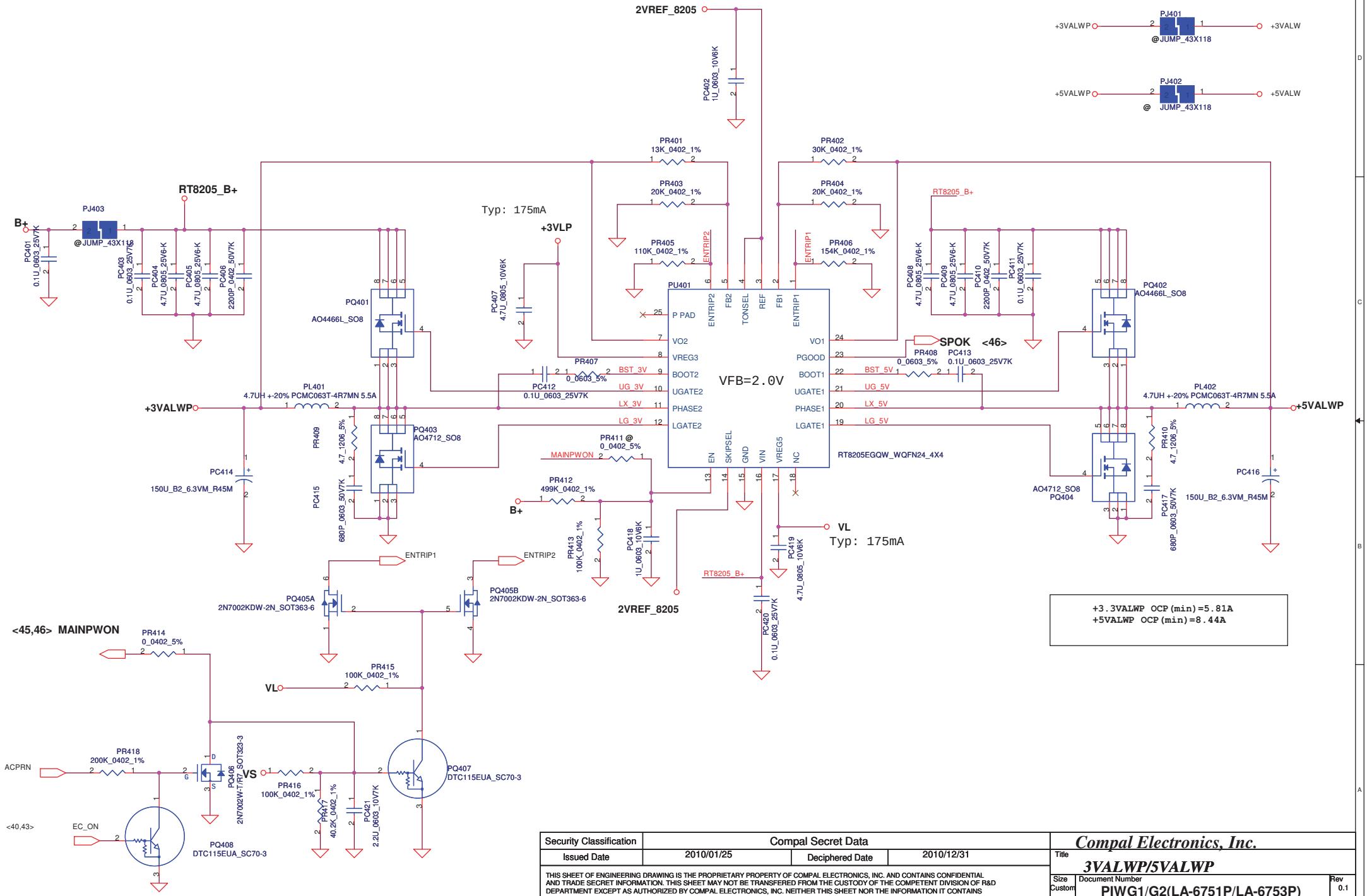
Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 47 of 54

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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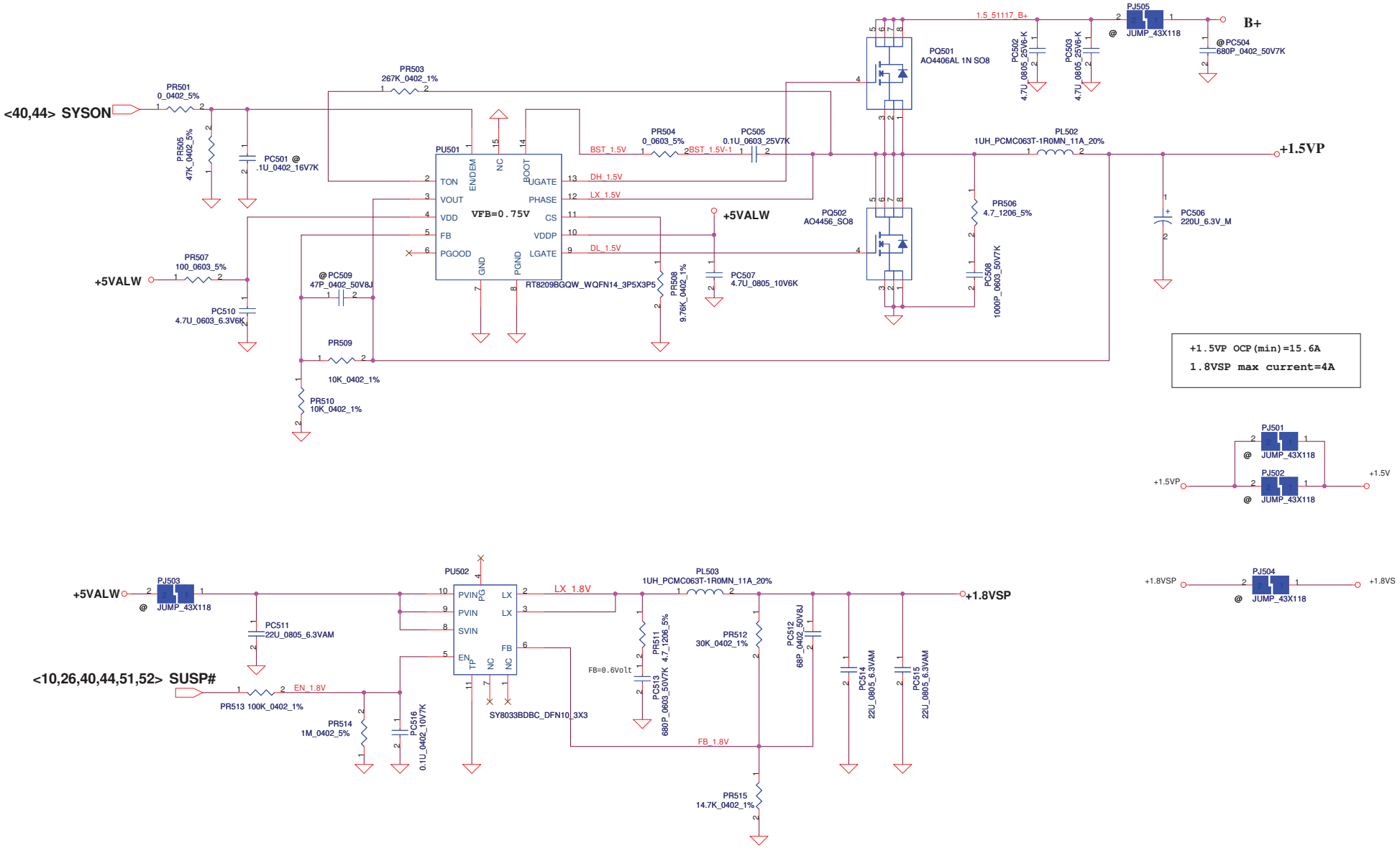
Compal Electronics, Inc.

Title: **3VALWP/5VALWP**

Size: Custom | Document Number: **PIWG1/G2(LA-6751P/LA-6753P)** | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 48 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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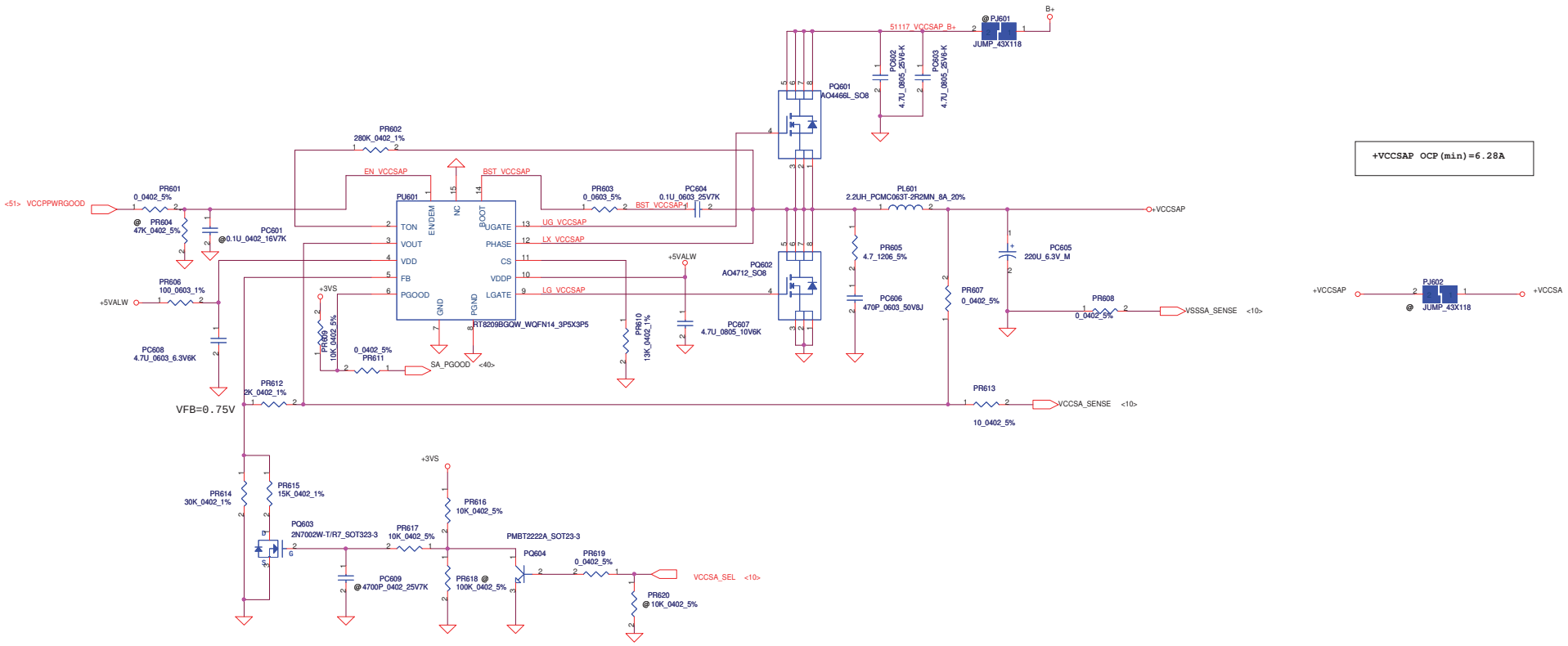
Compal Electronics, Inc.

Title: ***PWR-+1.5VP/+1.8VSP***

Size: Custom | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 49 of 54



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.725V	No/Yes
1	1	0.675V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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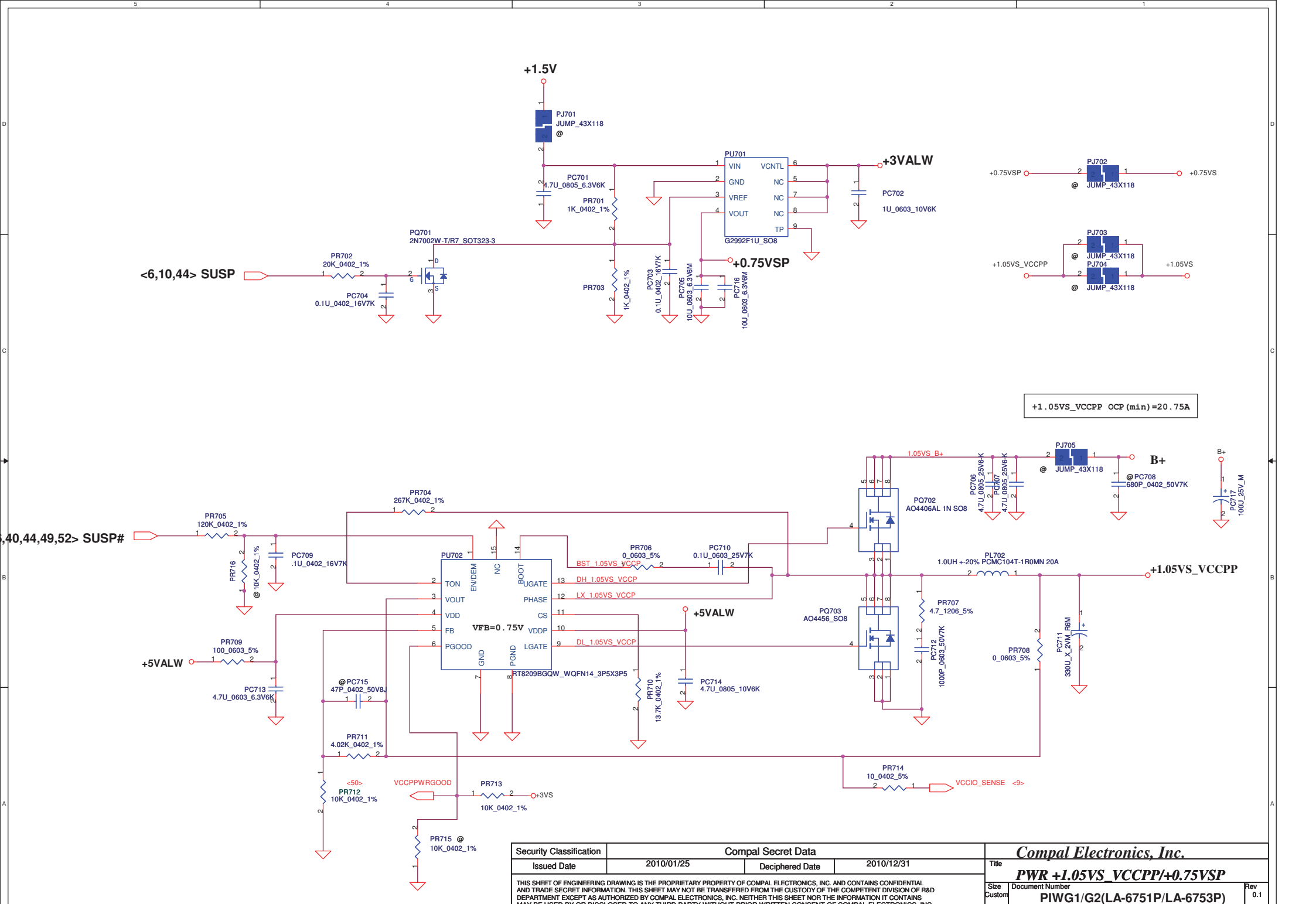
Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 50 of 54



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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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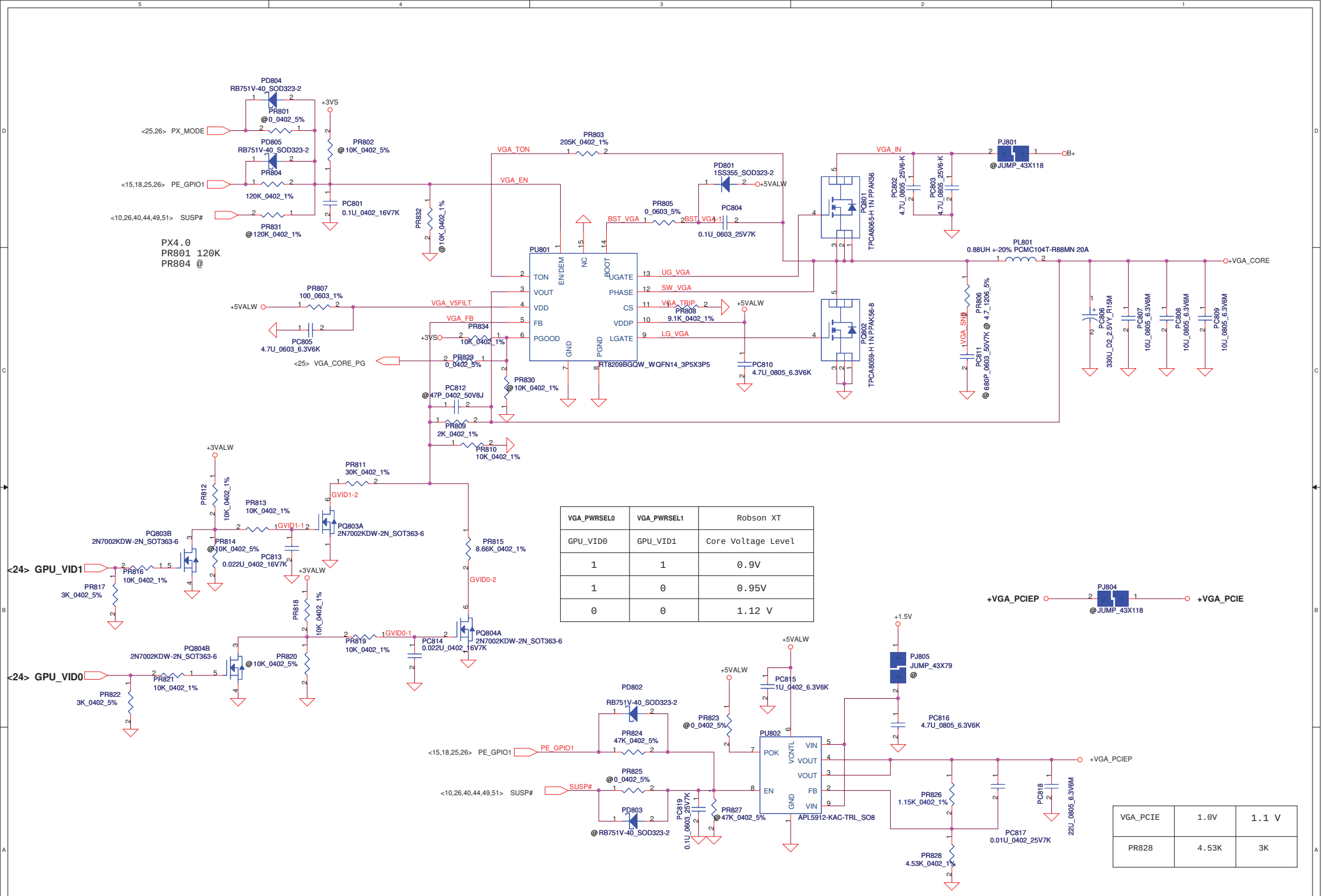
Compal Electronics, Inc.

Title: **PWR +1.05VS_VCCPP/+0.75VSP**

Size: Custom | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 51 of 54



VGA_PWRSEL0	VGA_PWRSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V

VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: PWR +VGA_CORE/PCIE

Size | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev 0.1

Date: Friday, November 26, 2010 | Sheet 52 of 54

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

ISL95831CRZ-T_TQFN48_6X6

PU901

(Ipeak=54A)

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: PIWG1/G2(LA-6751P/LA-6753P) | Rev: 0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	To reduce charger ripple	47	Add PC323	2010.08.15	DVT
2	HW request for power sequence	51	Change +VGA_PCIE enable signal from PX_MODE to PE_GPIO1 PR804:120K PR831,PR801,PR825 UN-POP PR824:47K PC819:0.2uF	2010.08.15	DVT
3	Change Vboot setting	52	Change PR942 as 4.32K	2010.08.15	DVT
4	Change OCP setting	52	Change PR958 as 1.47K	2010.08.15	DVT
5	Add PC955 for loadline adjust	52	Add PC955	2010.08.15	DVT
6	Reserve pull low resistor	51	Add PR718,PR832	2010.09.29	PVT
7	Remove jump	51	Remove PJ802,PJ803	2010.09.29	PVT
8	Adapter protect circuit	46	Pop PR222,PR208,PH202,PR221,PQ204 Un-Pop PR223,PR203	2010.09.29	PVT
9	EMI Request	47	Remove PJ301 Add PL302 and reserve PC324	2010.09.29	PVT
10					
11					
12					
13					
14					
15					
16					
17					

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Issued Date	2009/01/06	Deciphered Date	2009/01/06

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Title: PIR (PWR)

Size: Custom | Document Number: PIWG1/G2 | Rev: 0.1

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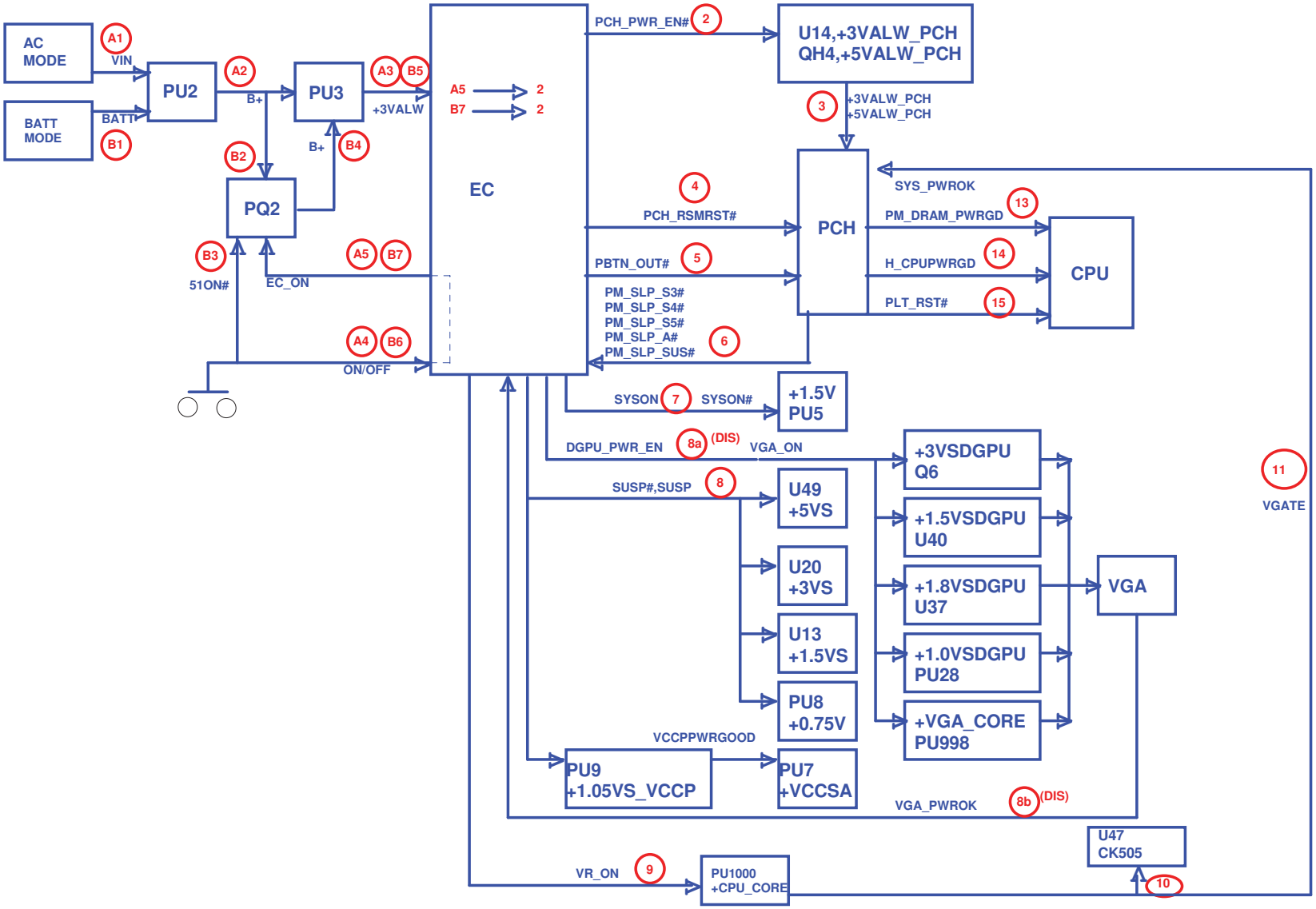

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Title: Power sequence

Size: Custom | Document Number: LA-6751P | Rev: 0.2

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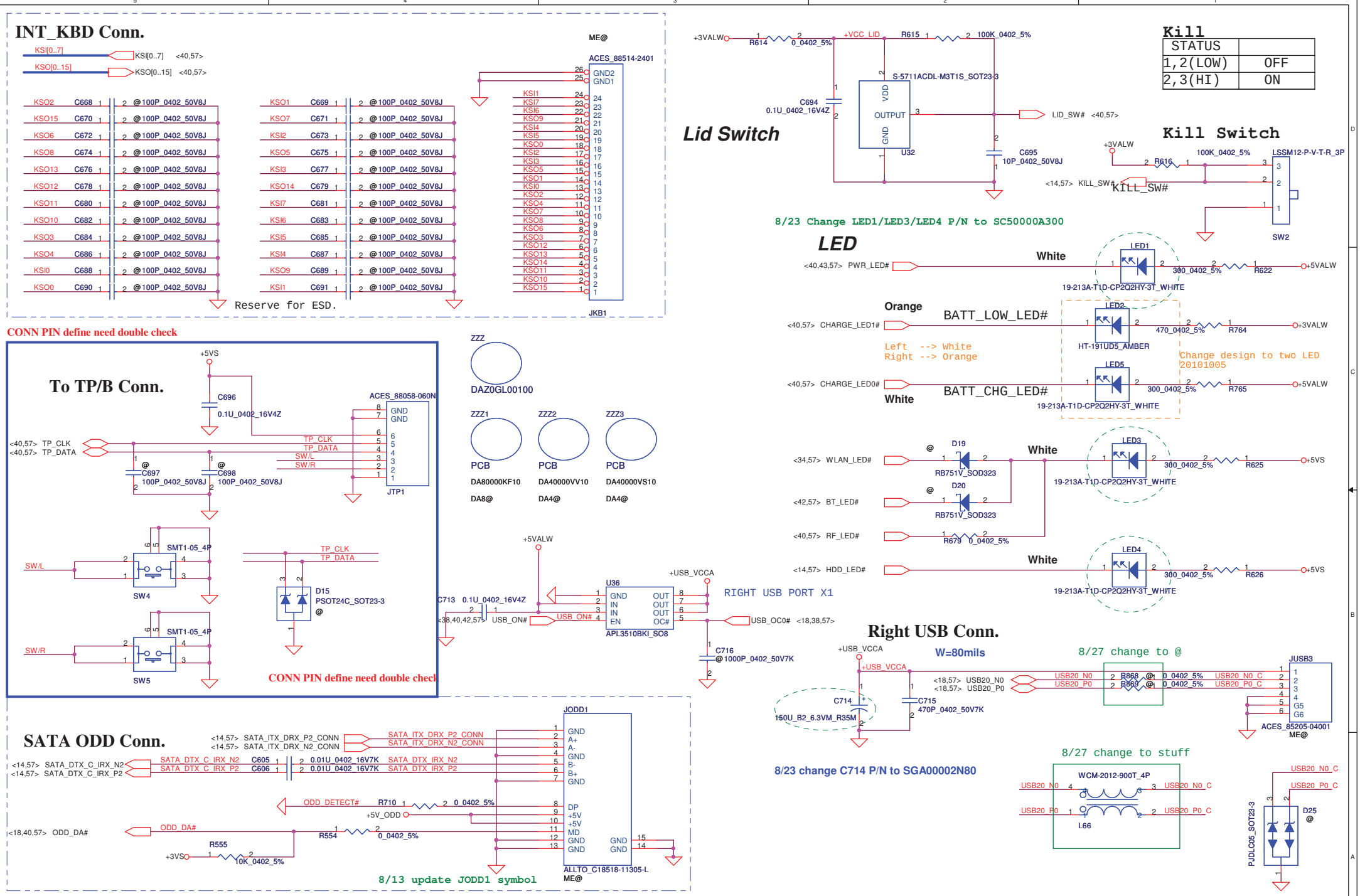

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Title: **KB /SW /LPC Debug Conn.**

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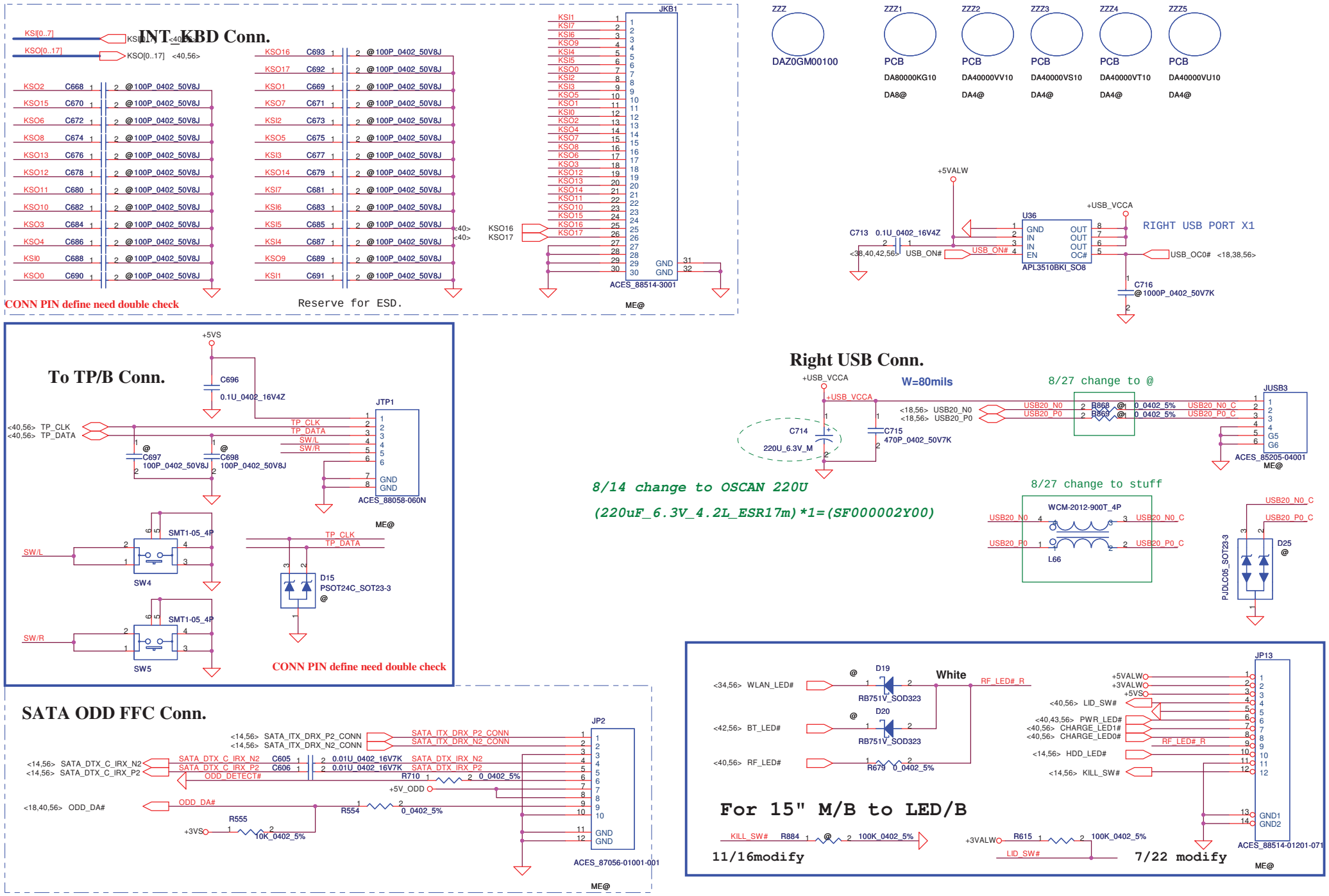

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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PHASE	PAGE	Modification list	PURPOSE
0.2	P31	Change CRT Symbol	For CRT footprint issue
0.2	P31	Del C510	For Non-used part
0.2	P39	change C610 pin 1 net name	change C610 pin 1 net name to correct
0.2	P35	U25 change to U26	For co-lay 10/100 and GIGA
0.2	P32	Add R735,R736	For DIS only SMBus pull high
0.2	P33	Add R738,R739	For DIS only SMBus pull high
0.2	P33	Change Q63 BOM structure to HDMI@	For DIS HDMI function
0.2	P40	Add R740, C93	For EC request
0.2	P18	Change R215 pin1 net name	Change R215 pin1 net name to correct
0.2	P18	Add R741	Add R741 for Reserved PE_GPIO0
0.2	P16	Add R742, R743	For PCH power sequence
0.2	P38	Del U28, R542~R551 , J12	Del USB charger circuit
0.2	P40	Add EC pin 97,98,103	Add EC pin 97 for SYS_PWROK_EC , pin 98 for CE_EN , pin 103 for BATT_SEL_EC
0.2	P24	Change R662 pin 2 net name	Change R662 pin 2 net name to correct
0.2	P28	Del C421,C422,C431,C432,C433, L27, Add R745, U8 pin N11,N12 change to NC	For AMD new document suggestion
0.2	P26	Add R744	Add R744 for control PE_GPIO1 from SUSP#
0.2	P39	Change J10 footprint and Add J13	Change J10 footprint by DFx request and Add J13 by vendor suggestion
0.2	P39	Change PC_Beep circuit	Change PC_Beep circuit
0.2	P6	Add R161, R182, R192 BOM structure hange to @	Follow ORB circuit
0.2	P58/59	Add R615 in 15" and 17" page	Pull high LID_SW# at M/B side
0.2	P31	Add Q83 pin 1 power net name +CMOS_PW	For power trace net
0.2	P56/57/58	Change JP21 to JKB1	Change connector to standard name
0.2	P56/57/58	Change JP4 to JTP1	Change connector to standard name
0.2	P43/60	Change JP6 to JPWRB1	Change connector to standard name
0.2	P34	Change JP1 to JWLN1	Change connector to standard name
0.2	P42	Change JP5 to JBT1	Change connector to standard name
0.2	P43/60	Change JP7 to JCR1	Change connector to standard name
0.2	P19	Add R542	For ESATA detect function
0.2	P42	Add R886, R887 , C735	For ESATA detect function
0.2	P31	Add R543	For reserve EC control directly
0.2	P39	Change J10 footprint, Del C635, C636	Change J10 for DFx and Del component for layout
0.2	P42	Add R877	For reserve EC control directly
0.2	P42	SW3 BOM structure change to @	For ME ASSY concern
0.2	P24	R324 BOM structure change, del @	For AMD update
0.2	P25	Change Q69,Q70,Q71,Q72 to BSS138, change Q66,Q67 pin 1 net name, D28 change to @	For Change BACO part follow AMD reference DATA ,D28 change to @ for leakage
0.2	P42	Change ESATA from port 5 to port 4	For intel risk
0.2	P15	Add R544,R545	For Pull high SMBus
0.2	P12/13	Del R74~R80,R82 R88~R94,R96	For DDR3 DM Bus to GND
0.2	P16	Add R182,R546	Add 186 for reserve sequence, Add R546 for follow CRB & ORB
0.2	P20	Del Add J12, R257 change to @	For voltage drop
0.2	P26	R161 Change Q6 to U14	Change SI2301 to SI4800 for loading current
0.2	P6	R161 change to 100K	Follow CRB
0.2	P19	Add R547 , R250 change to @	Follow Module and CRB
0.2	P18	WLAN USB port for port8 to port9	For debug port
0.2	P25	AND Gate power change to +3VGS	For VGA circuit
0.2	P24	Add R548, R549	For DIS HDMI audio strap
0.2	P39	Del J13	For layout space
0.2	P20,39,42	Add C395 , R581 , R583 , R584 , R586 , R587	For customer request reserved
0.2	P20	Add C129, C396 , Del R264	For reserved
0.2	P40	Add PIN 66 , R740,C93 change to @	Add IMVP_IMON
0.2	P9	Add R74	For VCCIO_SENSE / VSSIO_SENSE differential routing

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Compal Electronics, Inc.

Title: **KB /SW /LPC Debug Conn.**

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PHASE	PAGE	Modification list	PURPOSE
0.2	P33	Del RQ51 ~ Q54 Add Q95	For DIS HDMI
0.2	P39	Del J10, C637,C640,R576,R577,R579 change to @ , L40~L43 change to R720~R723	For Vendor suggestion and EMI
		Del C643, R578 , MIC_INR connect MIC_INL , Add R578	Del C653, R578 connect MIC_INR/L for vendor suggestion , Add R578 for EMI
0.2	P20	Add L75 , R264 , C917, R259 C226 change to @	For intel PDDG update
0.2	P20	Change JCR1 pin define , MIC change with HP	For correct ID
0.2	P9	Add C394, C397 ,C400 ,Add R75	For CPU_CORE power reserved at Bottom side, Add R75 for reserved at cpu side and pwr side
0.2	P26	Add R688 change to 20k, R345 change to 200k , R350 change to 330k , Q65 stuff	For VGA power sequence
0.2	P42	Change C706 P/N to SF000001500	Change to H=6 OSCAN
0.2	P10	Change C128 to @	For Reserved
0.2	P26	Change D3 change to @	For VGA leakage
0.2	P25	Change BIF_VDDC control pin net name	For correct behavior
0.2	P56	Update JODD1 symbol	For ME update drawing
0.2	P16	D29 change to @	For AC detect issue
0.2	P24	R548,R549 change to DIS@	For AC detect issue
0.2	P10	C128 change to stuff	For test on DVT
0.2	P44	Del Q118, R657	For not need
0.2	P57	Change 15" C714 to OSCAN	For ME Space ok
0.2		Change R513, R516 ,R667 P/N and from 0805 to 0603	For common part
0.2		Change C633, C634 , C642	For common part
0.2		Change D3, D29 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change Q8,Q65,Q80,Q83,Q99,Q104 P/N and symbol	For common part
0.2		Change Q1,Q37,Q93 P/N and symbol	For common part
0.2		Change Q94, Q95 P/N and symbol	For common part
0.2		Change Q3,Q4,Q7,Q9,Q66,Q67,Q68,Q73,Q74,Q75,Q76,Q77,Q78,	For common part
		Q79,Q82,Q85,Q86,Q87,Q102,Q106,Q107,Q108,Q109,Q110,Q111,Q112,Q113,Q114,Q115,Q116 P/N and symbol	
0.2	P43	Change C635 part and change to @	For EMI
0.2	P18	Reserved R551	Reserved
0.2	P9	Change C53,C85,C86,C87 ,C394,C397,C400 to stuff and change C48,C80,C81,C82,C89,C90,C91 to @	For CPU_CORE
0.2	P10	Change C110,C111,C112,C113 to stuff	For VGFX_CORE
0.2	P56	Change LED1/LED3/LED4 P/N to SC50000A300	Change P/N
0.2	P36	Change T1,T2 P/N to SP050003N00	For test pass part
0.2	P40	Change R611,R740,C93 to stuff and change Y5,C347,C367 to @	For SUS_CLK
		Change R695 to 18K, Q37 change to @, R747 change to stuff,	R695 for Board ID, Q37, R747 for VR_HOT
0.2	P41	Change U33 P/N to SA00003FL10	For BIOS ROM
0.2		Change C509,C511,C635 to stuff	For EMI request
0.2	P56	Change 14" C714 P/N to SGA00002N80	For Sourcer request
0.2	P39	Change R720,R721,R722,R723 P/N to SM01000BZ00(Bead), and Change C647,C649,C650,C651 to Stuff	For EMI request
0.2	P19	Change R303 to Stuff, and change R542 to @	For BIOS ESATA detect function
0.2	P56	Change U32 P/N to SA000031C00	For common part
0.2	P36	Change T1,T2 P/N to SP050006E00	For correct part
0.2	P10	R688 change to stuff , R687 ,Q7 change to @	For S3 power reduction
0.2		Change R660,R661,R862,R863,R864,R865,R868,R869 to @ , change L63,L64,L65,L66 to stuff , change R619 to Bead (SM01000DI00)	For EMI
0.2	P20	Change L75 symbol	For common part

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Title: **HW-PIR**

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PHASE	PAGE	Modification list	PURPOSE
0.3	P10	Update Q5 symbol	For update symbol
0.3	P33	Add F2	For safty request
0.3	P39	Update U30 P/N to SA00003K410 and Add R879	For Audio update to 21Z
0.3	P10	Change C128 to D2 size and @	Change size for M/E issue
0.3	P14	Add reserve R878	For Intel DG 1.5
0.3	P37	C592 change P/N to SF000001500 (H=6)	For ME Z high ok
0.3	P25	Update Q69~Q72 to AO3414 ,D28 R873 change to BACO@ , U40 change to @	For PX4.0
0.3	P28	Add reserve C94	For reserve VGA_CORE
0.3	P29	R369 P/N change to SD034100A80	For GP part
0.3	P18	R553,R691,R684,R682,U12 change to PX@	For PX 4.0
0.3	P6	Reserved R880 to SYS_PWROK	Follow ORB
0.3	P10	R62,R63 change to 1K	Follow CRB
0.3	P19	R303 change to @, Change M/B ID to PX4.0	For ESATA and PX4.0
0.3	P25	Q69~Q72 change to BACO @	For PX4.0
0.3	P26	R719 change to stuff, R744 change to @ , R677 change to BACO@	For PX4.0
0.3	P33	R483,R484 change connect to +5V_HDMI_F	For Add F2
0.3	P37	Change U27 P/N to SA000046C00	For Fintek
0.3	P40	Change R594 pull high to +5VALW	For leakage issue
0.3	P19	R881 change to Dtuff, R244 change to @	For intel MRC Rev0.9
0.3	P14	R878 change to stuff	For intel DG 1.5
0.3	P31	Del R432	For non-used part
0.3	P36	Reserved D31 , C643 , C644	For reserved EMI parts
0.3	P37	Del R581	For non-used part
0.3	P38	Del R550	For non-used part
0.3	P38	Change C592 P/N to SF000002Y00	For M/E Z high limlt
0.3	P39	Del R584, R586 , R587	For non-used part
0.3	P40	Change R600, R604 to 2.2K Change R695 to 8.2k	Change R600, R604 for Battery SMBus, R695 for Board ID
0.3	P42	Del R583	For non-used part
0.3	P6	Reserved R882 connect to PCH_PWROK	Reserved for intel
0.3	P56	R765 change to 300 ohm	For LED
0.3	P25	R324, R744 , R674 change DIS@	For DIS only sku

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