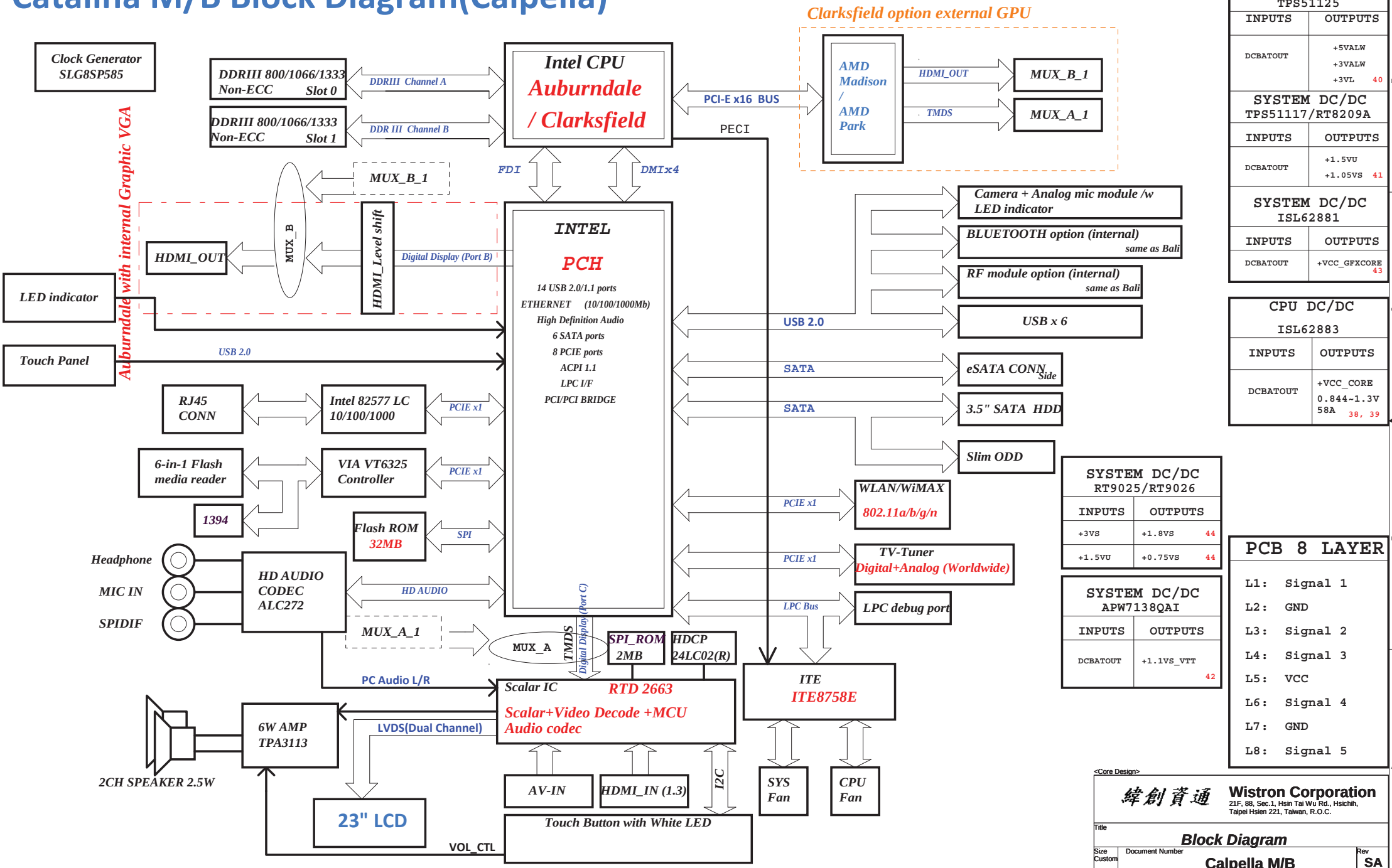
Catalina M/B Block Diagram(Calpella)



SYSTEM DC/DC
TPS51125

INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 40

SYSTEM DC/DC
TPS51117/RT8209A

INPUTS	OUTPUTS
DCBATOUT	+1.5VU +1.05VS 41

SYSTEM DC/DC
ISL62881

INPUTS	OUTPUTS
DCBATOUT	+VCC_GFXCORE 43

CPU DC/DC
ISL62883

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 58A 38, 39

SYSTEM DC/DC
RT9025/RT9026

INPUTS	OUTPUTS
+3VS	+1.8VS 44
+1.5VU	+0.75VS 44

SYSTEM DC/DC
APW7138QAI

INPUTS	OUTPUTS
DCBATOUT	+1.1VS_VTT 42

PCB 8 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4
L7: GND
L8: Signal 5

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Block Diagram**

Size: Custom | Document Number: Calpella M/B | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 1 of 59

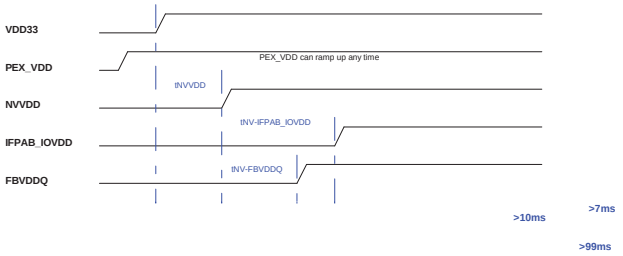
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

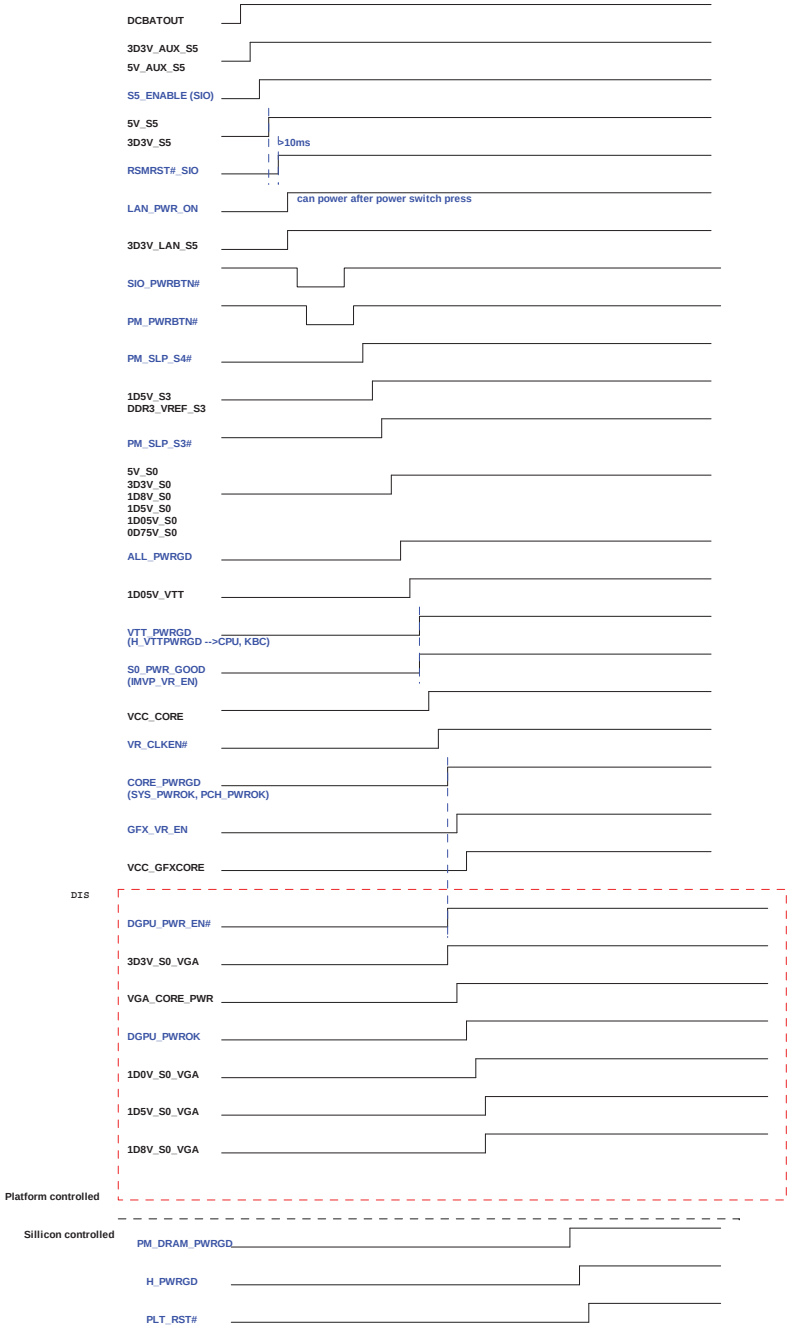
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence



Power Sequence



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緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

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Size A2	Document Number <Doc>	Rev <RevCode>
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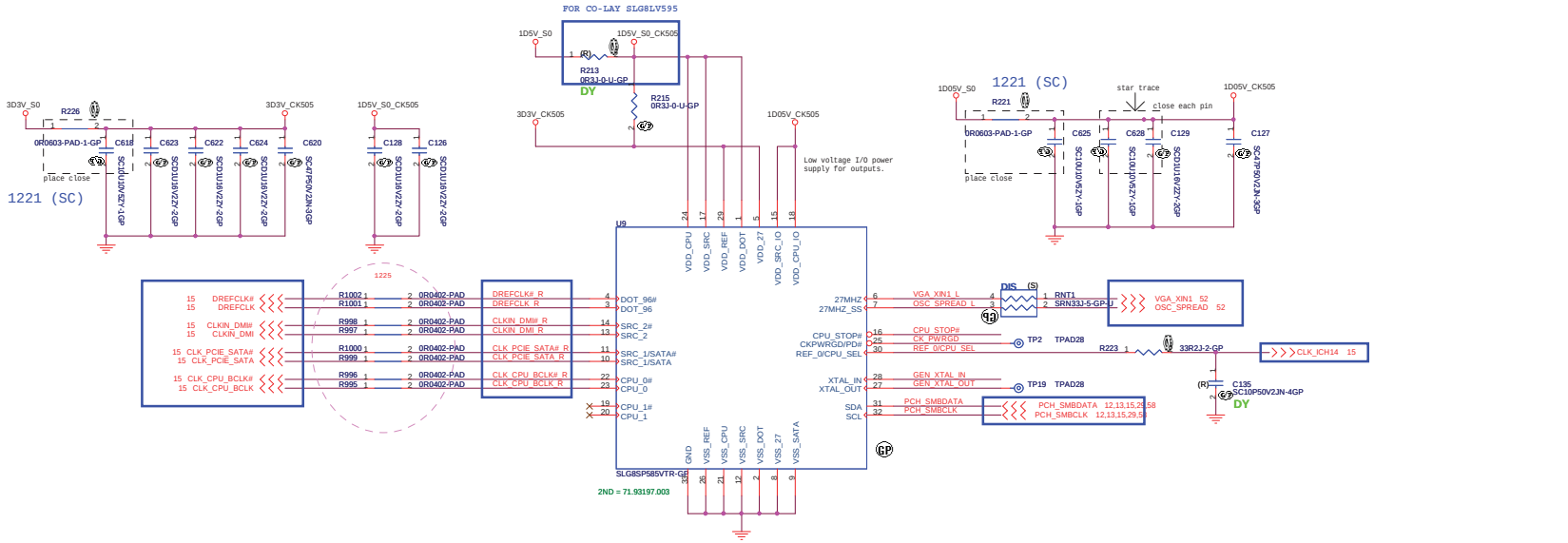

FSC	0	1
SPEED	133MHz (Default)	100MHz

Layout Notes:

Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.

<Variant Name>

Wistron Corporation
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Title: Ali Mountain

Size: A2 | Document Number: CK505_SLG8SP585 | Rev: <RevCode>

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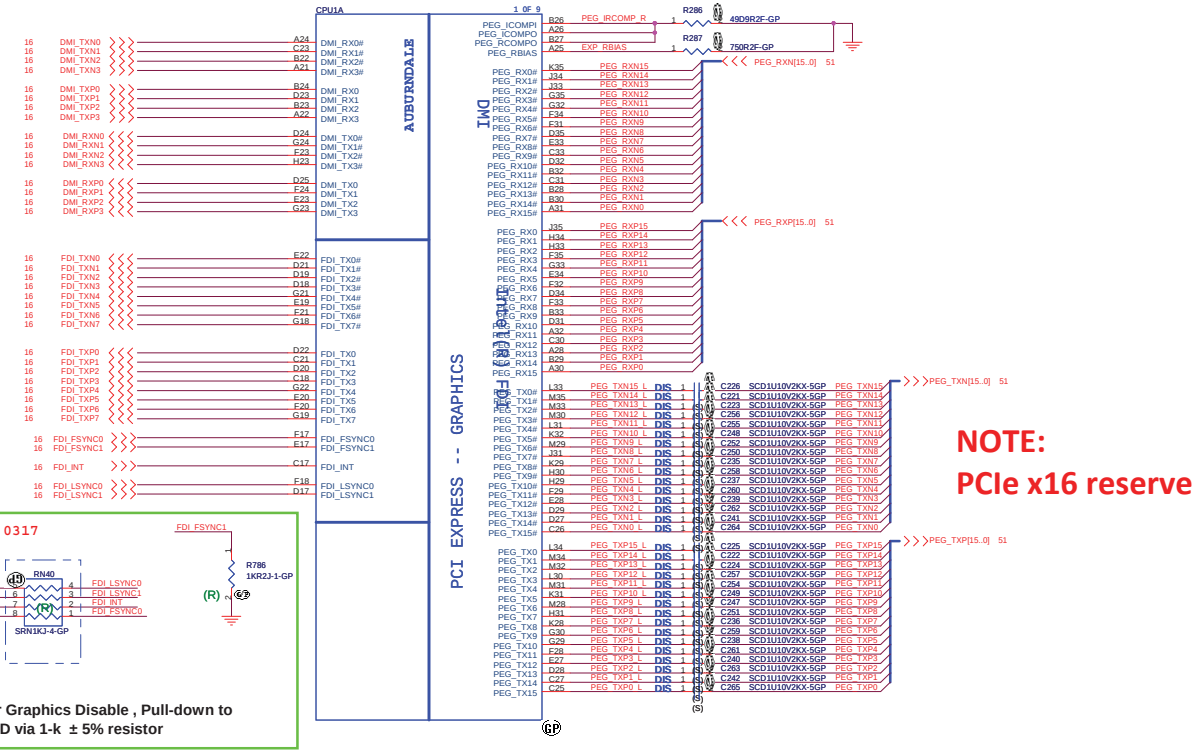
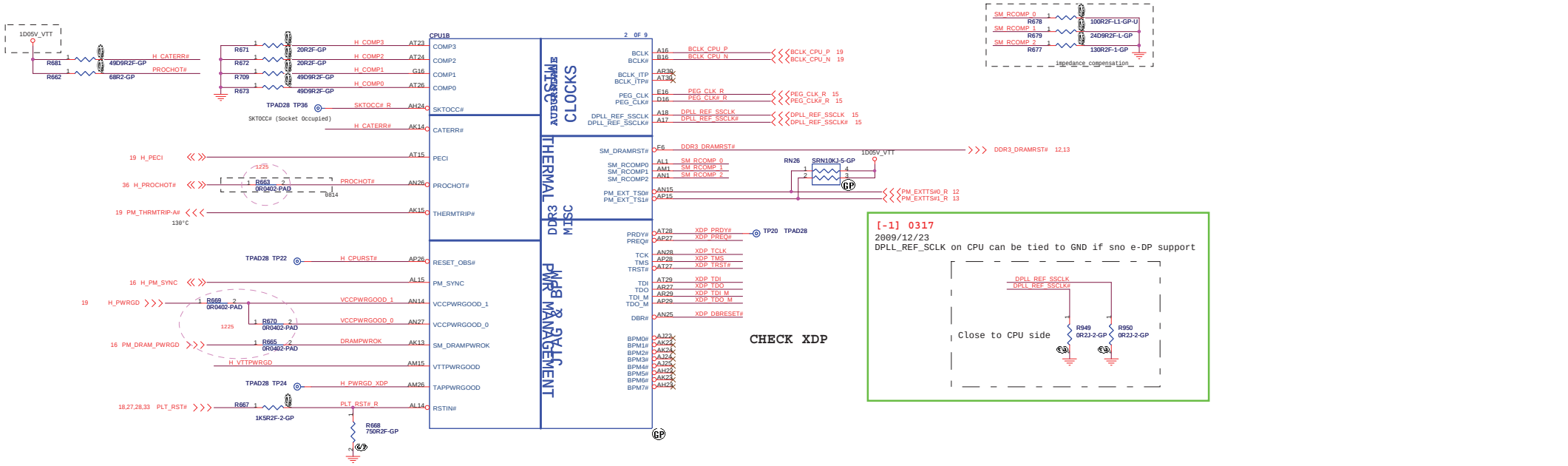


NOTE:
PCIe x16 reserve

62.10040.611
2nd = 62.10055.321

<Variant Name>

緯創資通	Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title: <Title>		
Size: A2	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, April 06, 2010	Sheet 4 of 59	



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (2/7)-HOST

Size	Document Number	Rev
A2	Catalina	SA

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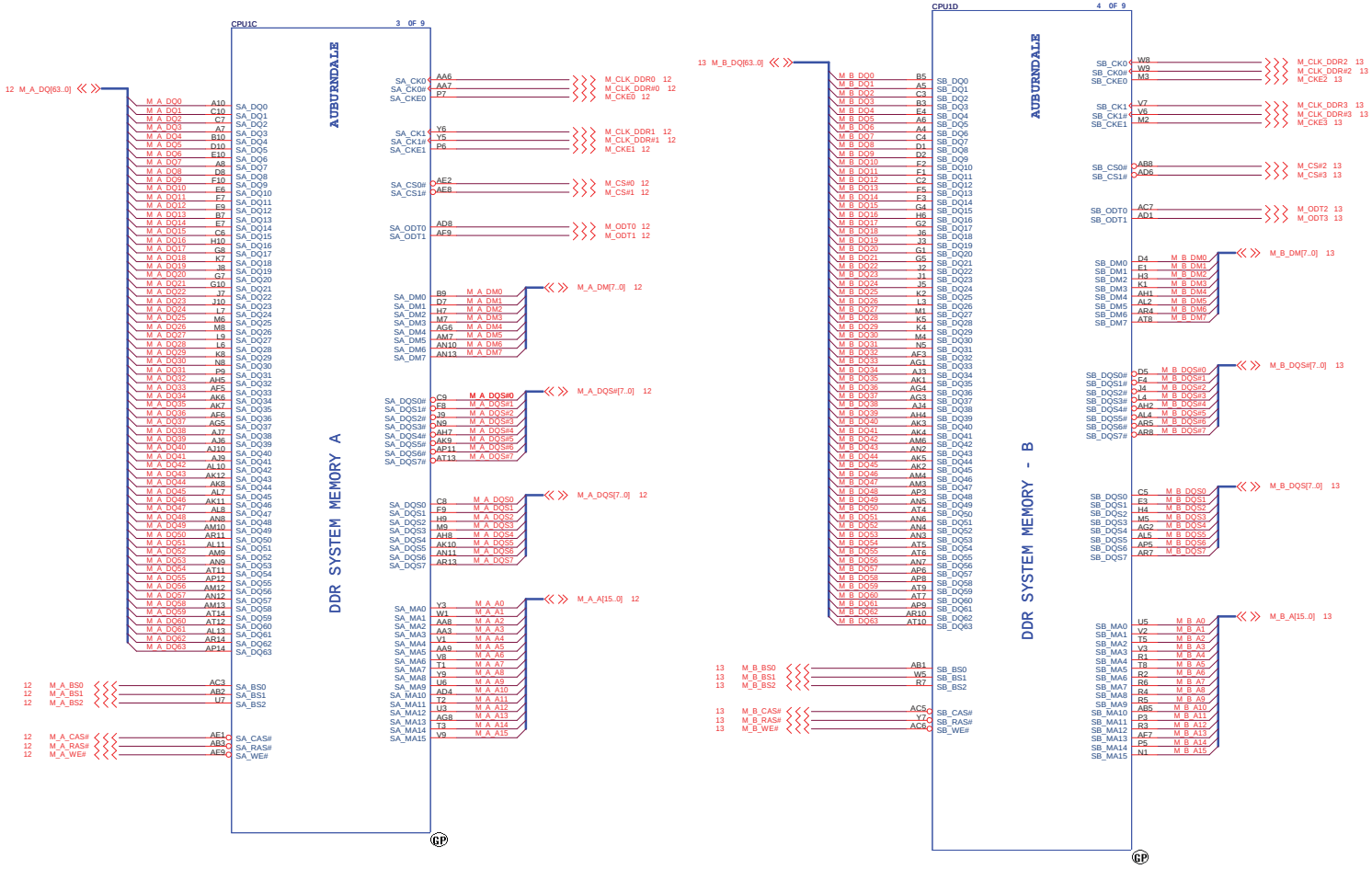

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/7)

Size: A2 | Document Number: Catalina | Rev: SA

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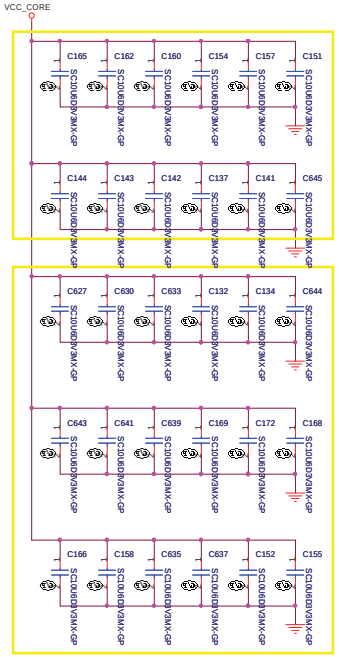
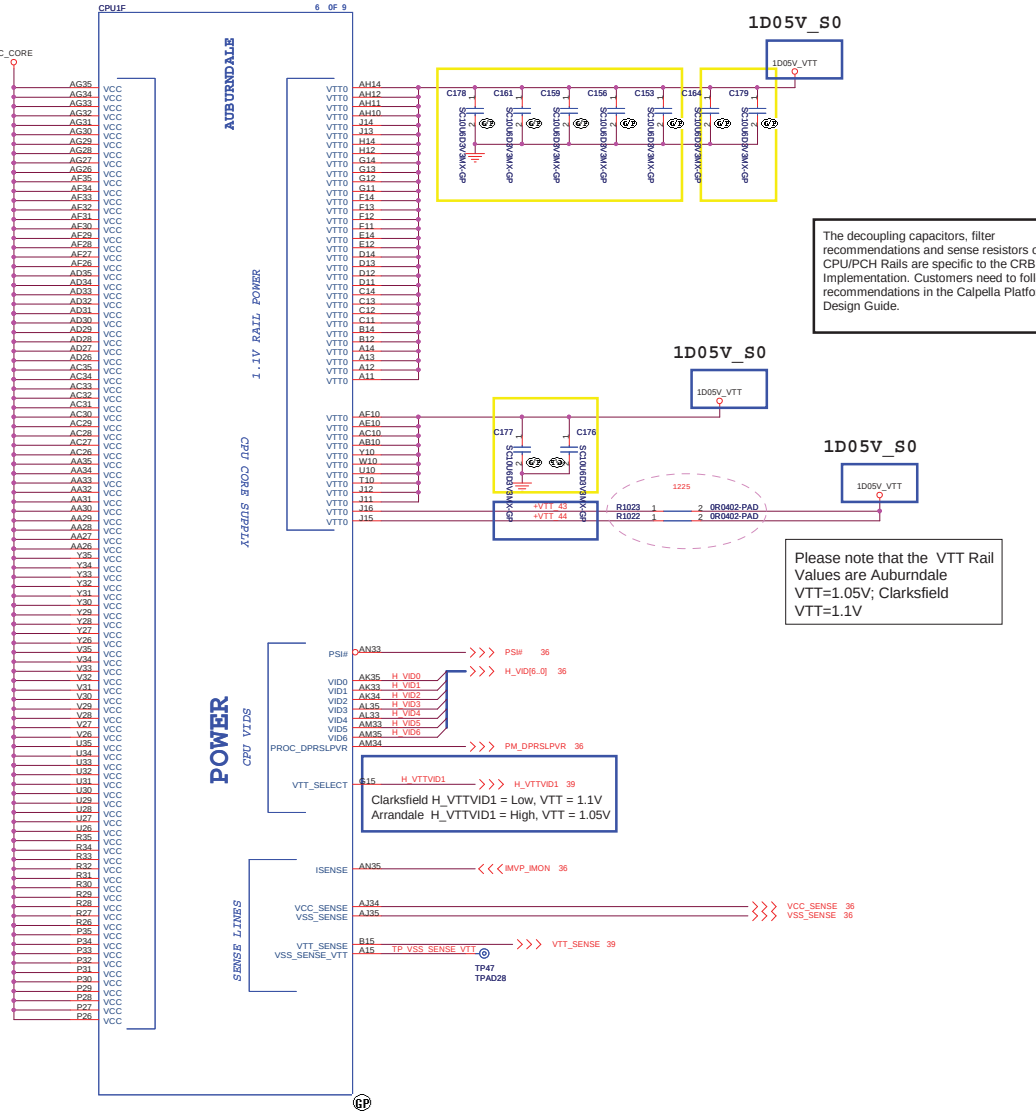
30pcs : 10uF 6.3V X5R

PROCESSOR CORE POWER

48A -->Arrandale





The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V

<Variant Name>

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Title <Title>

Size A2 | Document Number <Doc> | Rev <RevCode>

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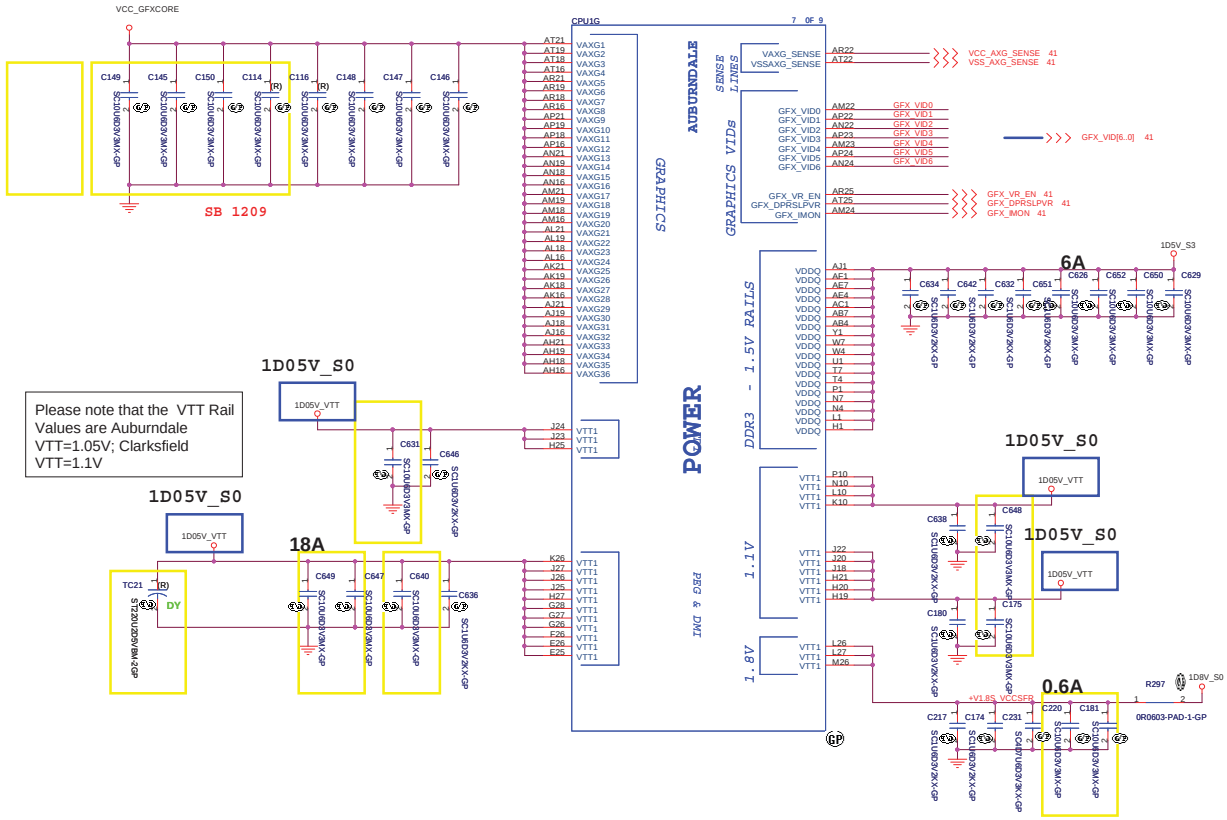

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Wistron Corporation
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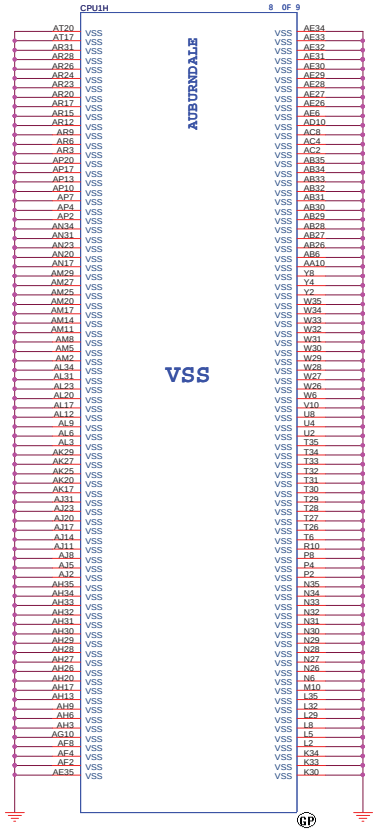

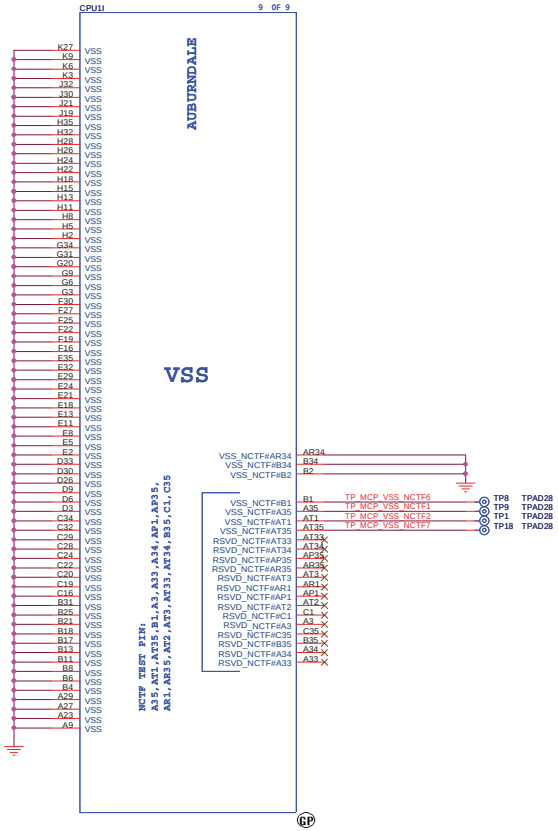

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Title: CPU(6/7)

Size	Document Number	Rev
A2	Catalina	SA

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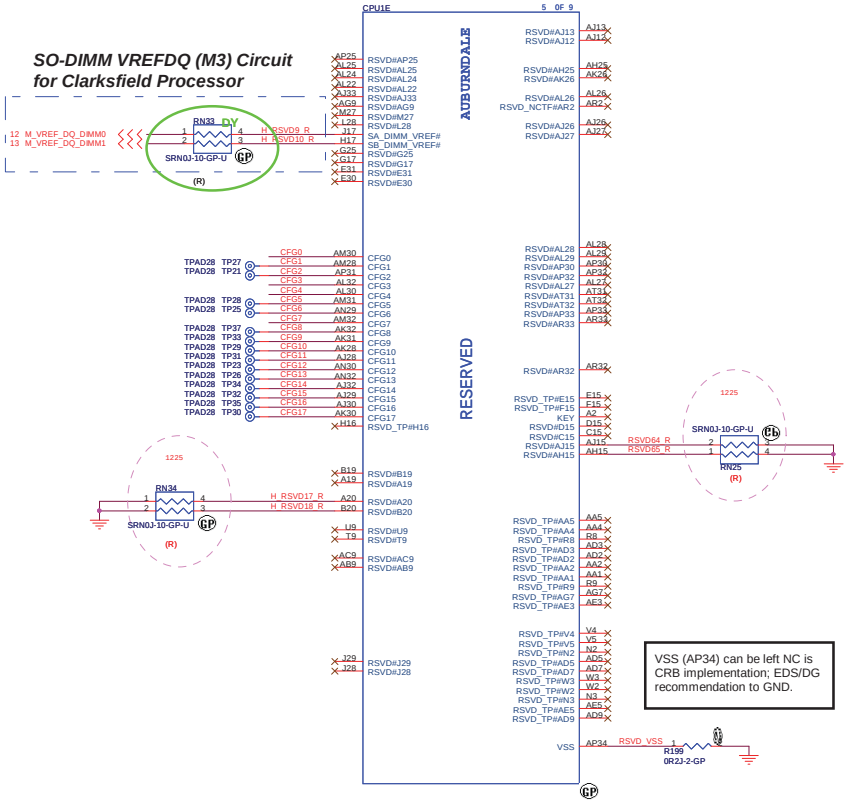

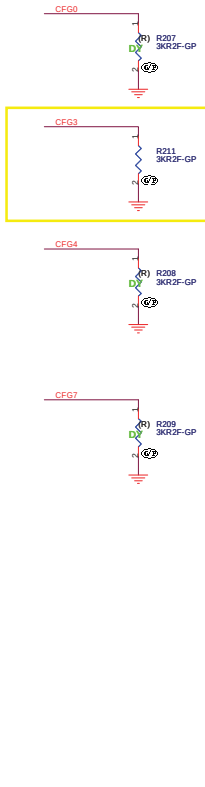

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shoubld be used. Does not impact AUB functionality.

<Core Design>

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Title: CPU(7/7)

Size	Document Number	Rev
A2	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 10 of 59

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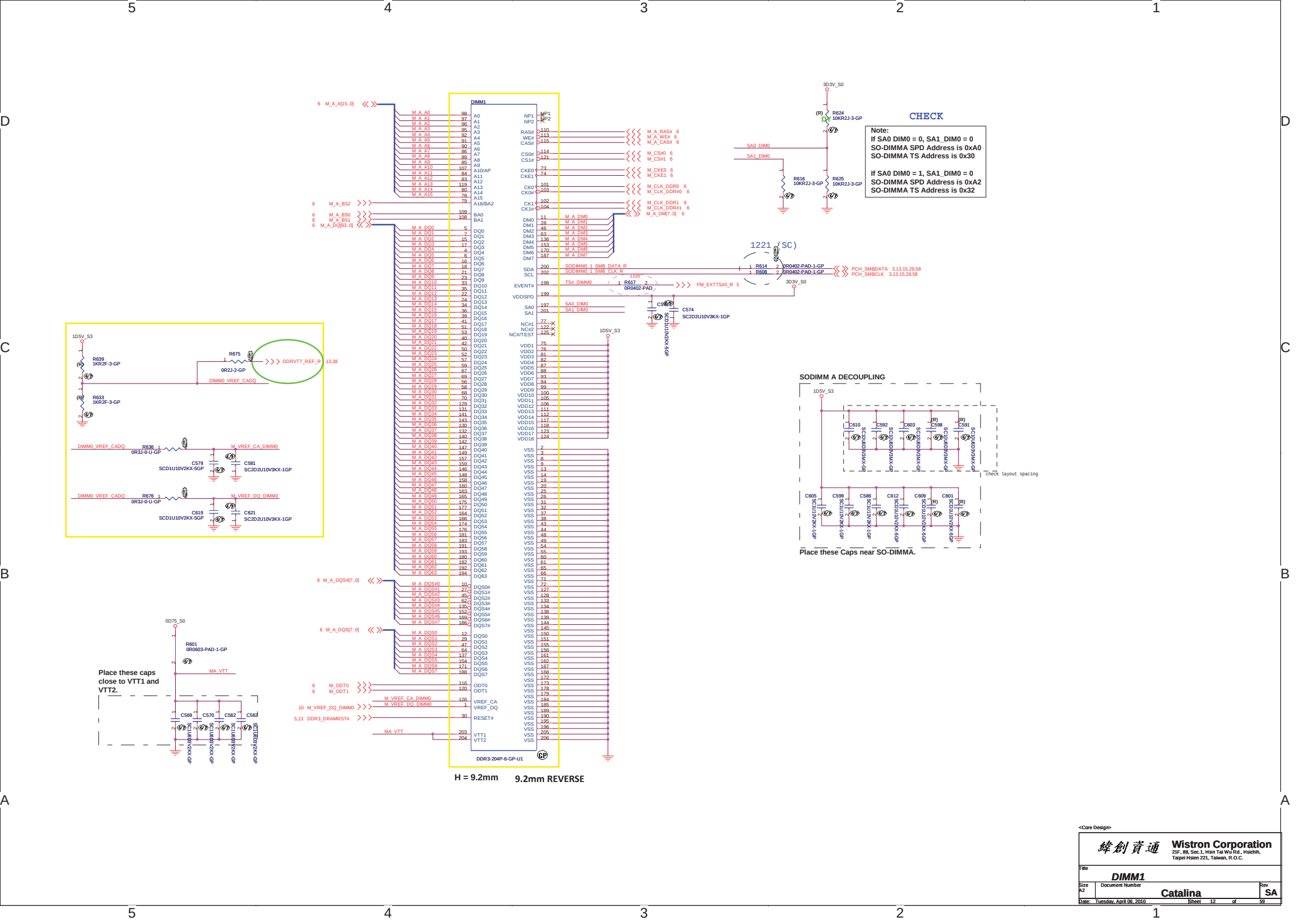
Size: A2	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, April 06, 2010	Sheet 11 of 59	



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Title	DIMM1
Size	A2
Document Number	Catalina
Rev	SA
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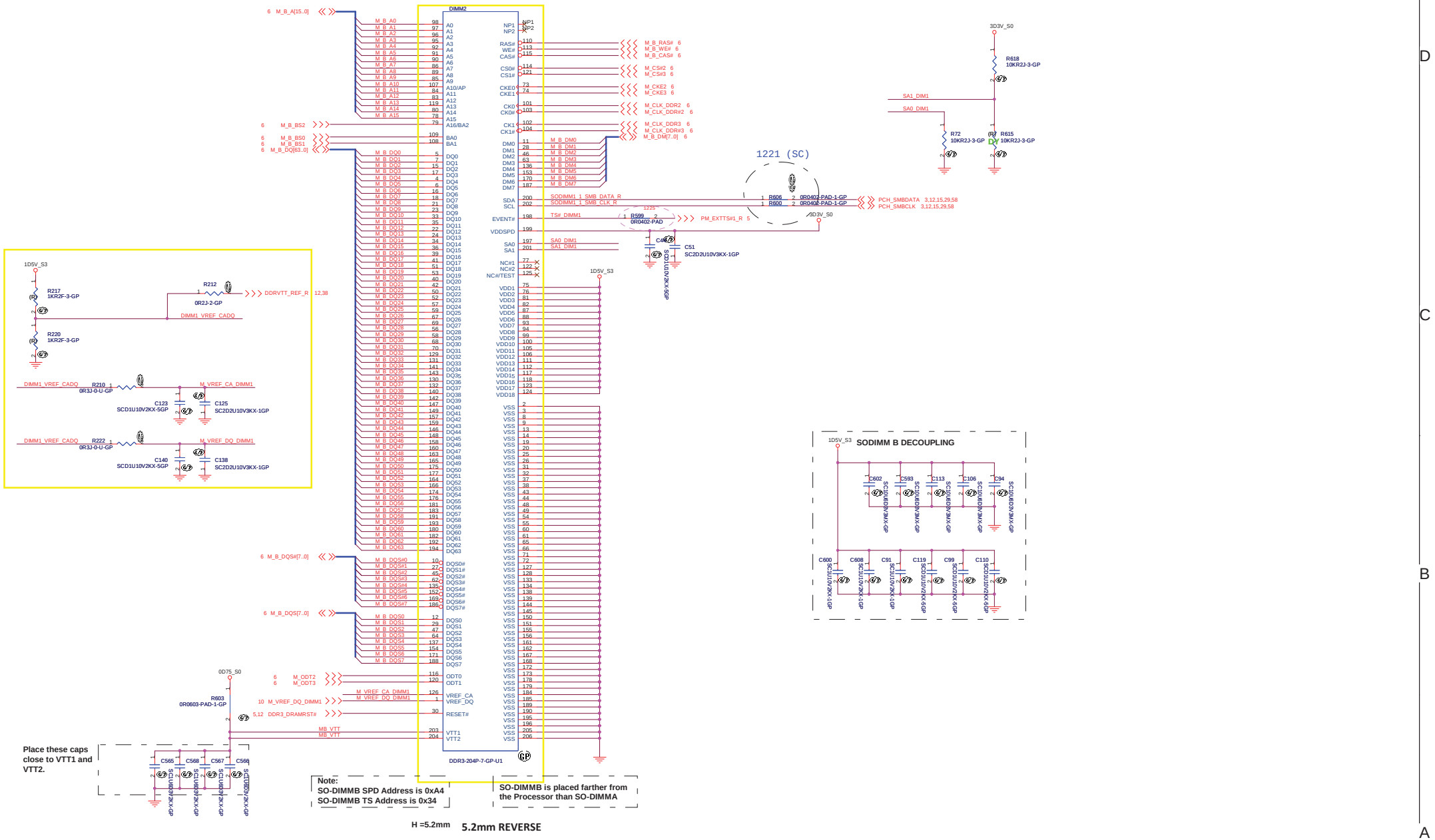

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DIMM2

Size	Document Number	Rev
A2	Catalina	SA

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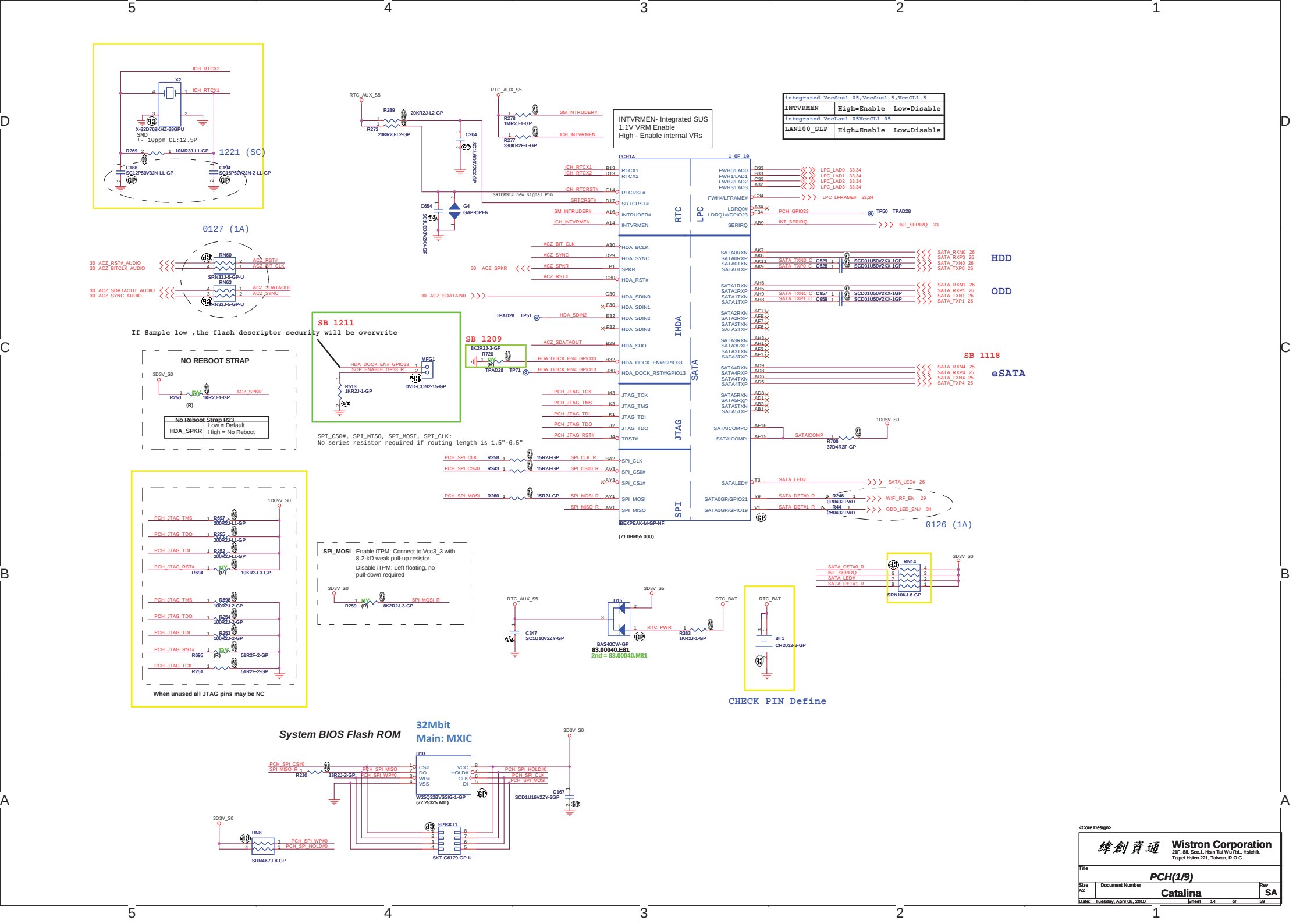
ICH_RTCX2
X2
ICH_RTCX1
X-32D768KHZ-38GPU
SMD
+- 10ppm CL:12.5P
R269 10MR3J-L1-GP
C188 SC12P50V3JN-LL-GP
C189 SC15P50V2JN-2-LL-GP
1221 (SC)
0127 (1A)
RN60
RN63
SRN33J-5-GP-U
30 ACZ_RST#_AUDIO
30 ACZ_BITCLK_AUDIO
30 ACZ_SDATAOUT_AUDIO
30 ACZ_SYNC_AUDIO
ACZ_RST#
ACZ_BIT_CLK
ACZ_SDATAOUT
ACZ_SYNC
If Sample low ,the flash descriptor security will be overwrite
NO REBOOT STRAP
3D3V_S0
R250 1KR2J-1-GP
ACZ_SPKR
No Reboot Strap R23
HDA_SPKR
Low = Default
High = No Reboot
SB 1211
HDA_DOCK_EN#_GPIO33
SOP_ENABLE_GP33_R
MFG1
DVD-CON2-15-GP
R513 1KR2J-1-GP
SB 1209
8K2R2J-3-GP
R720
TPAD28
TP71
HDA_DOCK_EN#_GPIO13
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
PCH_SPI_CLK R258 15R2J-GP SPI_CLK_R
PCH_SPI_CS#0 R243 15R2J-GP SPI_CS#0_R
PCH_SPI_MOSI R260 15R2J-GP SPI_MOSI_R
SPI_MISO_R
1D05V_S0
PCH_JTAG_TMS R697 200R2J-L1-GP
PCH_JTAG_TDO R255 200R2J-L1-GP
PCH_JTAG_TDI R252 200R2J-L1-GP
PCH_JTAG_RST# R694 10KR2J-3-GP
PCH_JTAG_TCK R251 51R2F-2-GP
When unused all JTAG pins may be NC
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
R259 8K2R2J-3-GP
RTC_AUX_S5
R289 20KR2J-L2-GP
R273 20KR2J-L2-GP
C204 SC1U6D3V2KX-GP
C654 SC1U6D3V2KX-GP
G4 GAP-OPEN
SRTCRST# new signal Pin
R278 1MR2J-1-GP
R277 330KR2F-L-GP
SM_INTRUDER#
ICH_INTVRMEN
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
ICH_RTCX1
ICH_RTCX2
ICH_RTCRST#
SRTCRST#
SM_INTRUDER#
ICH_INTVRMEN
ACZ_BIT_CLK
ACZ_SYNC
ACZ_SPKR
ACZ_RST#
ACZ_SDATAIN0
HDA_SDIN2
ACZ_SDATAOUT
HDA_DOCK_EN#_GPIO33
HDA_DOCK_RST#_GPIO13
PCH_JTAG_TCK
PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
SERIRQ
PCH_GPIO23
INT_SERIRQ
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_TXN0_C_C529
SATA_TXP0_C_C528
SATA_TXN1_C_C957
SATA_TXP1_C_C959
SCD01U50V2KX-1GP
SATA_RXN0 26
SATA_RXP0 26
SATA_TXN0 26
SATA_TXP0 26
SATA_RXN1 26
SATA_RXP1 26
SATA_TXN1 26
SATA_TXP1 26
HDD
ODD
SB 1118
eSATA
SATA_RXN4 25
SATA_RXP4 25
SATA_TXN4 25
SATA_TXP4 25
SATAICOMP
R708 37D4R2F-GP
SATA_LED# 26
SATA_DET#0_R
SATA_DET#1_R
WIFI_RF_EN 29
ODD_LED_EN# 34
R246 0R0402-PAD
R44 0R0402-PAD
IBEXPEAK-M-GP-NF
(71.0HM55.00U)
0126 (1A)
RN14
SRN10KJ-6-GP
INT_SERIRQ
SATA_LED#
RTC_AUX_S5
C347 SC1U10V2ZY-GP
D15 BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
RTC_PWR
R383 1KR2J-1-GP
RTC_BAT
BT1
CR2032-3-GP
CHECK PIN Define
System BIOS Flash ROM
32Mbit
Main: MXIC
U10
W25Q32BVSSIG-1-GP
(72.25325.A01)
PCH_SPI_CS#0
SPI_MISO_R
R230 33R2J-2-GP
PCH_SPI_MISO
PCH_SPI_WP#0
PCH_SPI_HOLD#0
PCH_SPI_CLK
PCH_SPI_MOSI
C167 SCD1U16V2ZY-2GP
SPISKT1
SKT-G6179-GP-U
RN8
SRN4K7J-8-GP
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH(1/9)
Size A2
Document Number
Catalina
Rev SA
Date: Tuesday, April 06, 2010
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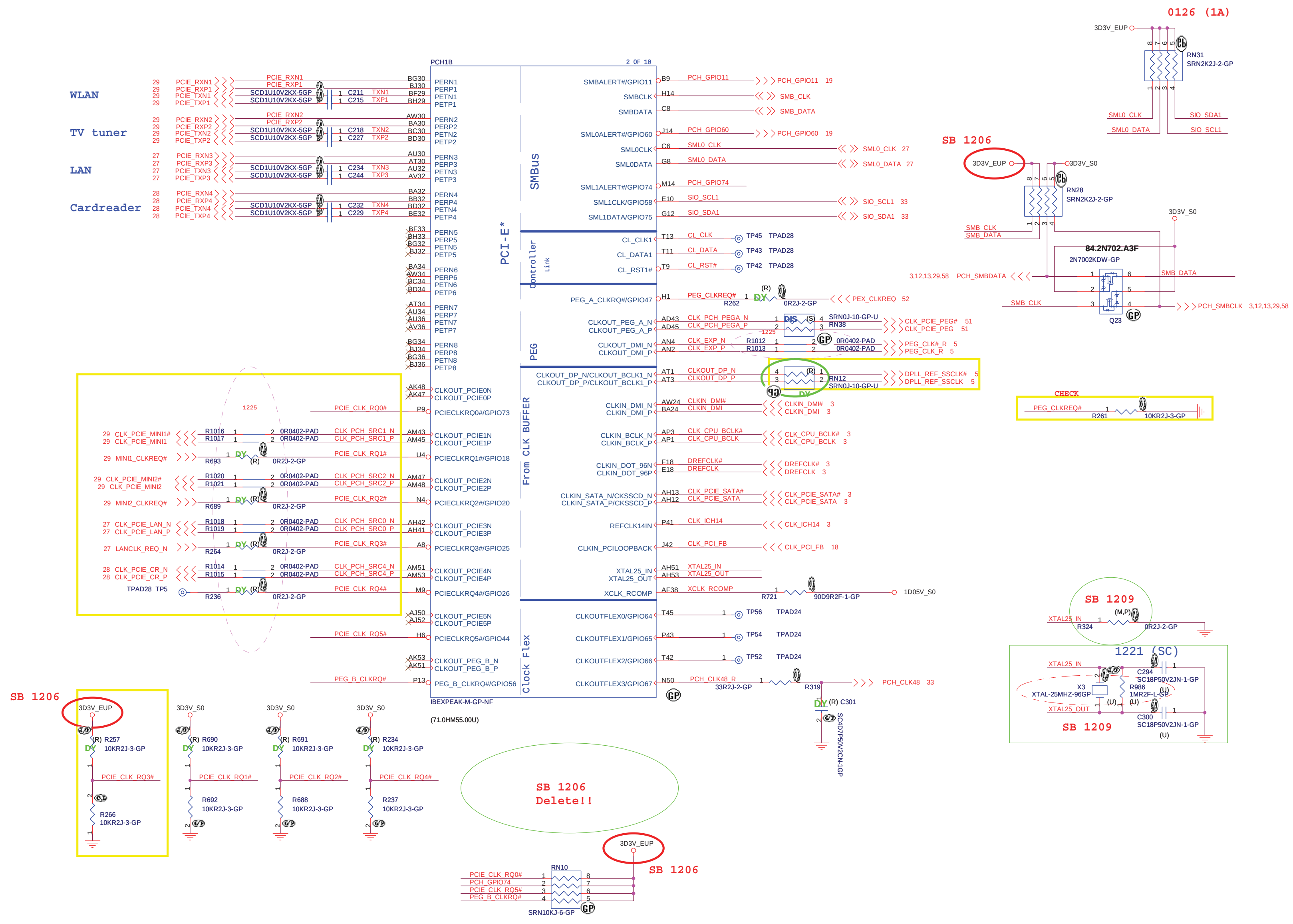

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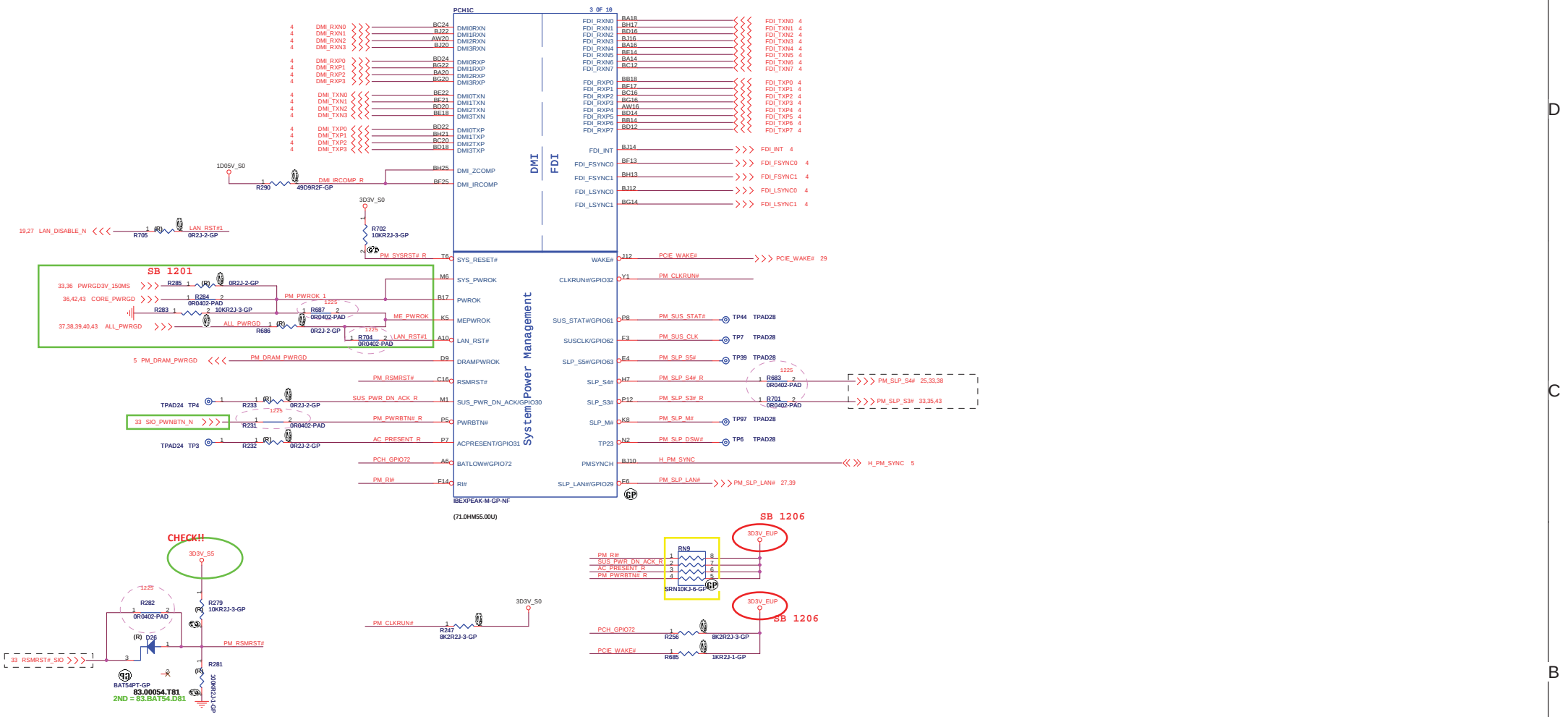
PCH1C
3 OF 10
DMI
FDI
System Power Management
SB 1201
SB 1206
CHECK!!
R705
R702
10KR2J-3-GP
R290
49D9R2F-GP
R285
R284
R283
R687
R686
R704
R233
R231
R232
R282
R279
10KR2J-3-GP
R281
R247
8K2R2J-3-GP
R256
R685
1KR2J-1-GP
RN9
SRN10KJ-6-GP
D26
BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.DB1
iBEXPEAK-M-GP-NF
(71.0HM55.00U)
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
<Variant Name>
<Title>
<Doc>
<RevCode>
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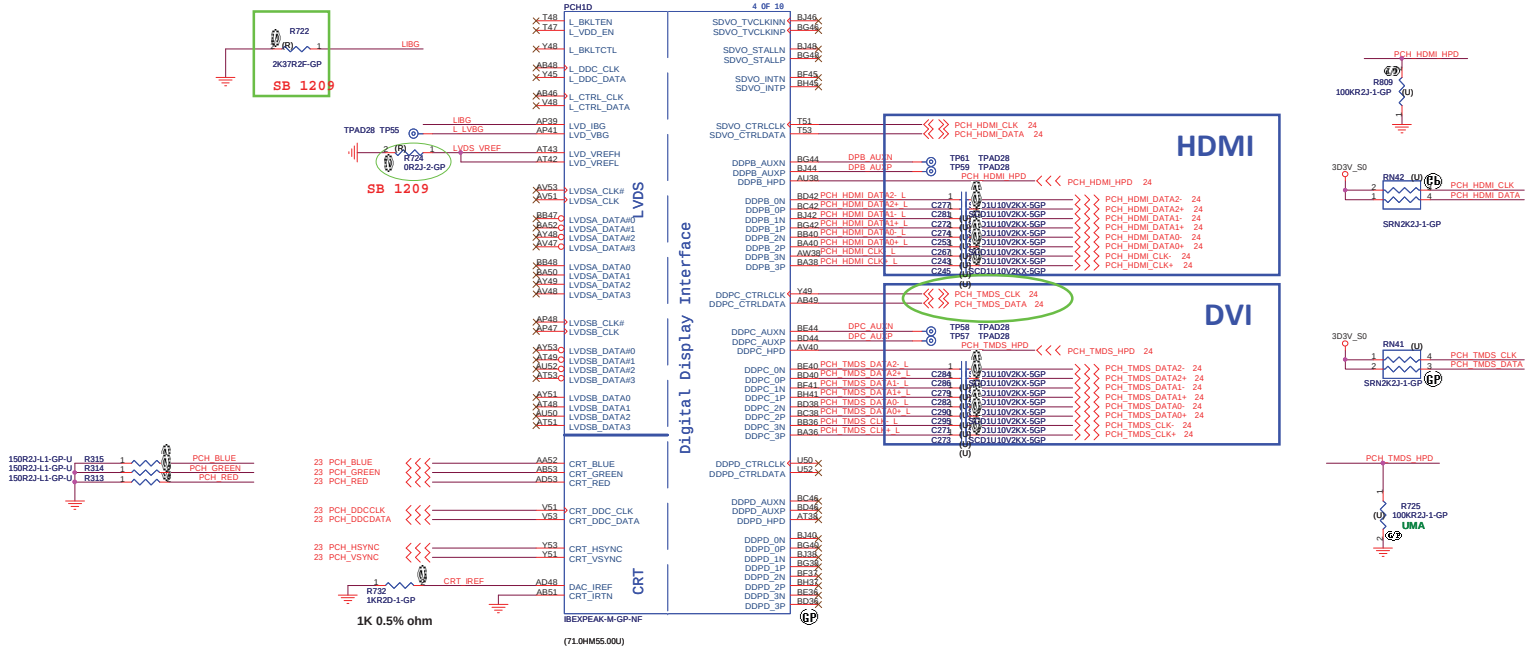

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Taipei Hsien 221, Taiwan, R.O.C

Title	<Title>	
Size A2	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, April 06, 2010	Sheet 17 of 59	

1226 (SC)

RN37 SRN8K2J-4-GP
INT_PIRQG#
PCI_TRDY#
PCI_DEVSEL#
PCI_PLOCK#

RN36 SRN8K2J-4-GP
PCI_STOP#
PCI_FRAME#
INT_PIRQD#
PCI_IRDY#

3D3V_S0

These pins are left as NC, because the function is disable.

R323 8K2R2J-3-GP INT_PIRQB# PCI_REQ3#
R321 8K2R2J-3-GP
R738 8K2R2J-3-GP PCI_PERR#
R322 8K2R2J-3-GP INT_PIRQF#

RN35 SRN8K2J-4-GP
INT_PIRQA# PCI_SERR# INT_PIRQC# INT_PIRQE#

RN39 SRN8K2J-4-GP
PCI_REQ0# INT_PIRQH# PCI_REQ1# PCI_REQ2#

0126 (1A)

PCI_GNT0# R736 1KR2J-1-GP
PCI_GNT1# R730 1KR2J-1-GP
USE SPI

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

PCH1E
5 OF 10
IBEXPEAK-M-GP-NF
(71.0HM55.00U)

PCI
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
C/BE0# C/BE1# C/BE2# C/BE3#
PIRQA# PIRQB# PIRQC# PIRQD#
REQ0# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54
GNT0# GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
PCIRST#
SERR# PERR#
IRDY# PAR DEVSEL# FRAME#
PLOCK#
STOP# TRDY#
PME#
PLTRST#
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4

NVRAM
NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0/NV_IO0 NV_DQ1/NV_IO1 NV_DQ2/NV_IO2 NV_DQ3/NV_IO3 NV_DQ4/NV_IO4 NV_DQ5/NV_IO5 NV_DQ6/NV_IO6 NV_DQ7/NV_IO7 NV_DQ8/NV_IO8 NV_DQ9/NV_IO9 NV_DQ10/NV_IO10 NV_DQ11/NV_IO11 NV_DQ12/NV_IO12 NV_DQ13/NV_IO13 NV_DQ14/NV_IO14 NV_DQ15/NV_IO15
NV_ALE NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE# NV_WR#1_RE#
NV_WE#_CK0 NV_WE#_CK1

R263 32D4R2F-GP DY

These pins are left as NC, because the function is disable.

DMI Termination Voltage

NV_CLE	Set to Vss when low. Set to Vcc when high.

+V_NVRAM_VCCQ
R249 1KR2J-1-GP DY NV_CLE
R248 1KR2J-1-GP DY NV_ALE

Danbury Technology:
Disabled when Low.
Enable when High.

USB
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
USBRBIAS USBRBIAS#
USB_RBIAS_PN R291 22D6R2F-L1-GP

USB0 MINI2 [-1] 0317
USB2
USB3
USB4
Touch panel
Reserve [-1] 0317
Reserve
USB8
USB9
Reserve USB
MINI2 [-1] 0317
Bluetooth (SB 1204)
Camera

Pair	Device
0	USB0
1	MINI1
2	USB2
3	USB3
4	USB4
5	Touch panel
6	Reserve
7	Reserve
8	USB8
9	USB9
10	Reserve USB
11	MINI2
12	Bluetooth
13	Camera

SB 1206
Check!!
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14
OC*08 OC*23 OC*49 OC*67
3D3V_EUP R707 10KR2J-3-GP

33 LPC_PME_N
5,27,28,33 PLT_RST#
33 CLK_PCI_SIO
15 CLK_PCI_FB
34 CLK_PCI_PORT80
R320 22R2J-2-GP CLK_PCI_SIO_R
R318 51R2J-2-GP CLK_PCI_FB_R
R731 47R2J-2-GP CLK_PCI_PORT80_R
CLK_PCI_3
CLK_PCI_4
TPAD28 TP11
TPAD28 TP60

34 PCI_RST#

PCI_GNT2# R718 4K7R2J-2-GP (R)
PCI_GNT3# R316 4K7R2J-2-GP (R)

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(5/9)
Size: A2
Document Number: Catalina
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

SB 1206

0126 (1A)

[-1] 0401

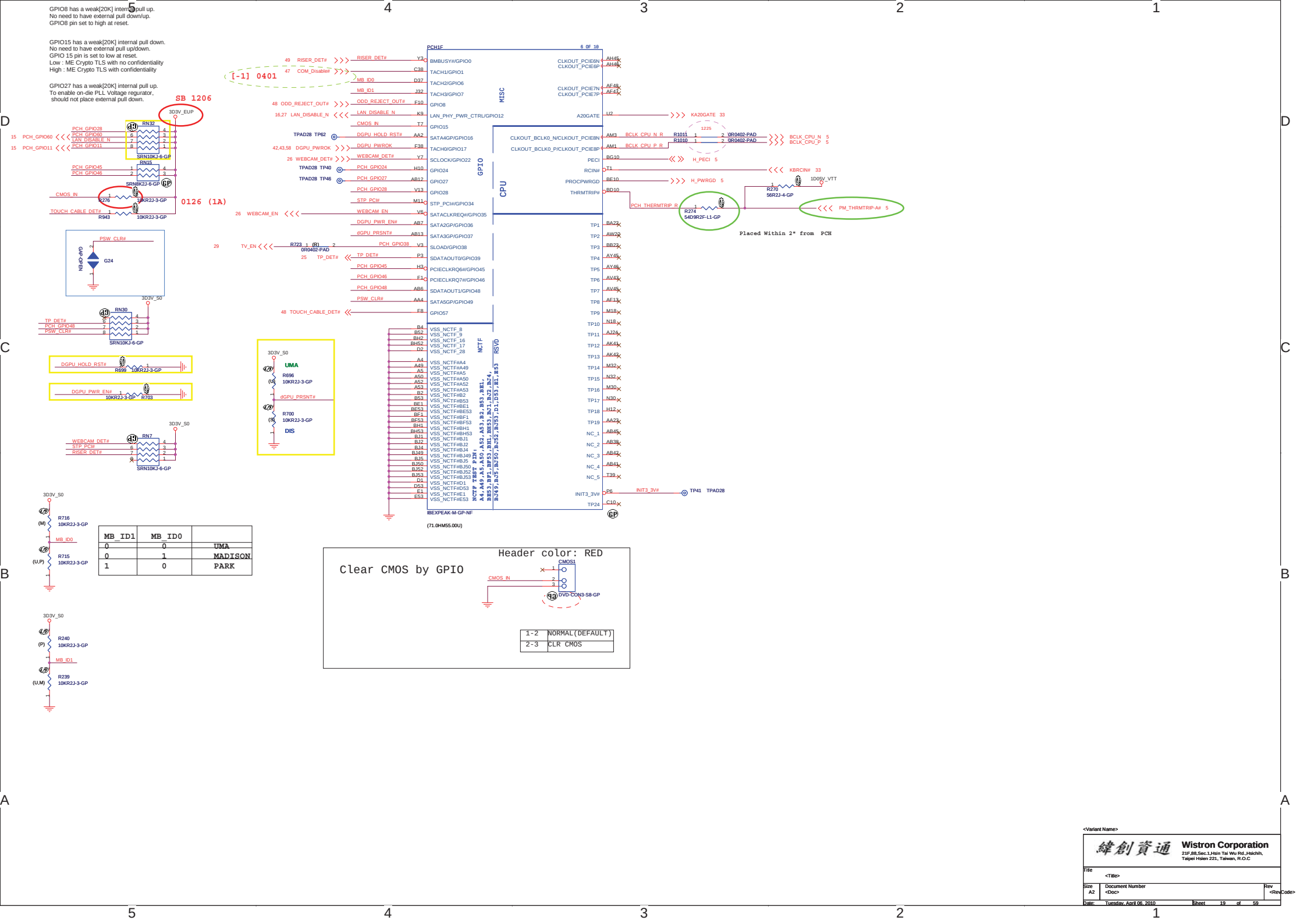
Placed Within 2" from PCH

Header color: RED

Clear CMOS by GPIO

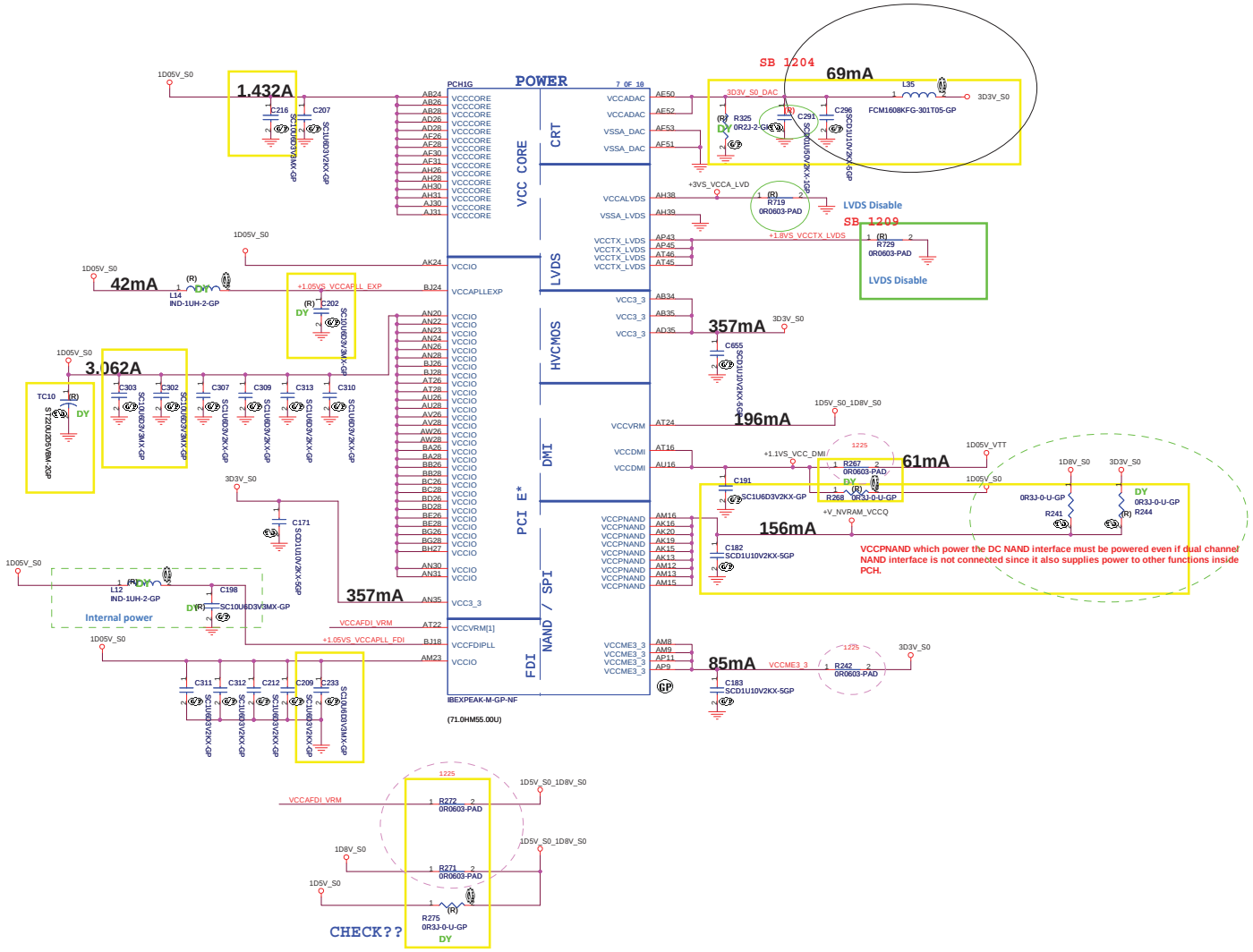
1-2	NORMAL(DEFAULT)
2-3	CLR CMOS

MB_ID1	MB_ID0	
0	0	UMA
0	1	MADISON
1	0	PARK



<Variant Name>
緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

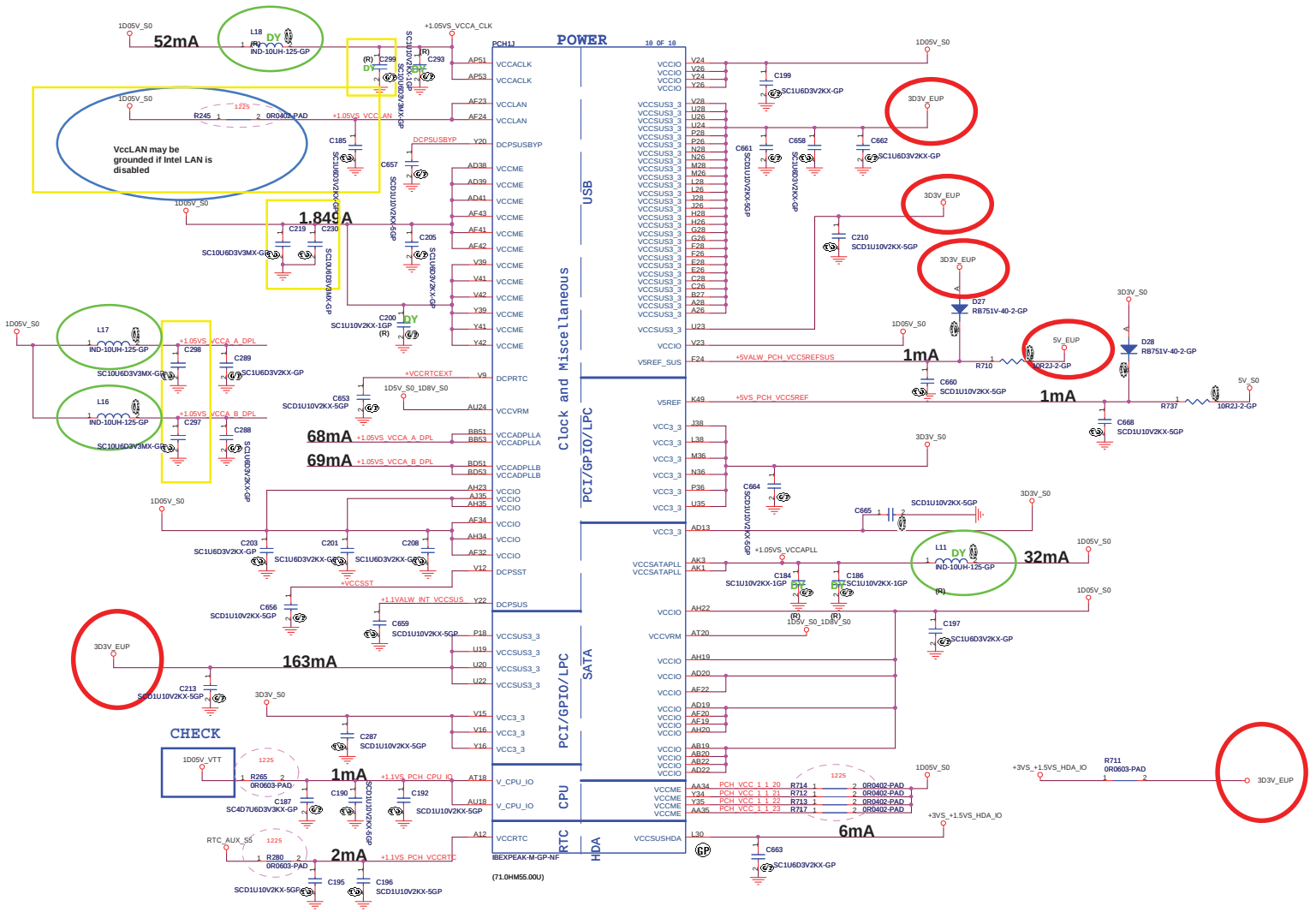
Title	<Title>		
Size A2	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, April 06, 2010	Sheet 19 of 59		



<Variant Name>

緯創資通 Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title <Title>
Size A2 | Document Number <Doc> | Rev <RevCode>
Date: Tuesday, April 06, 2010 | Sheet 20 of 59



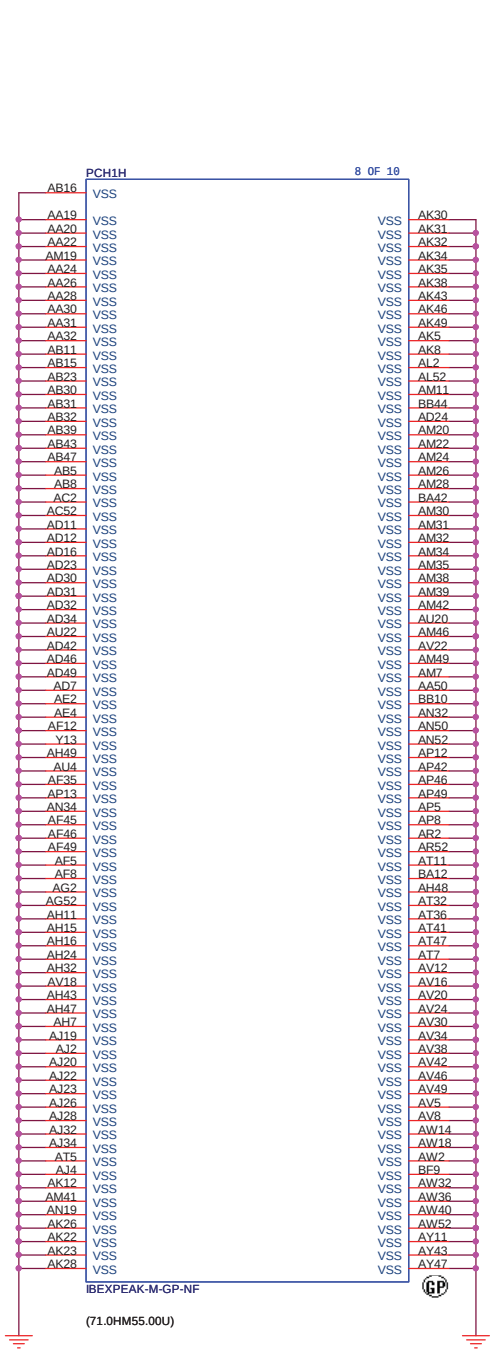
<Core Design>

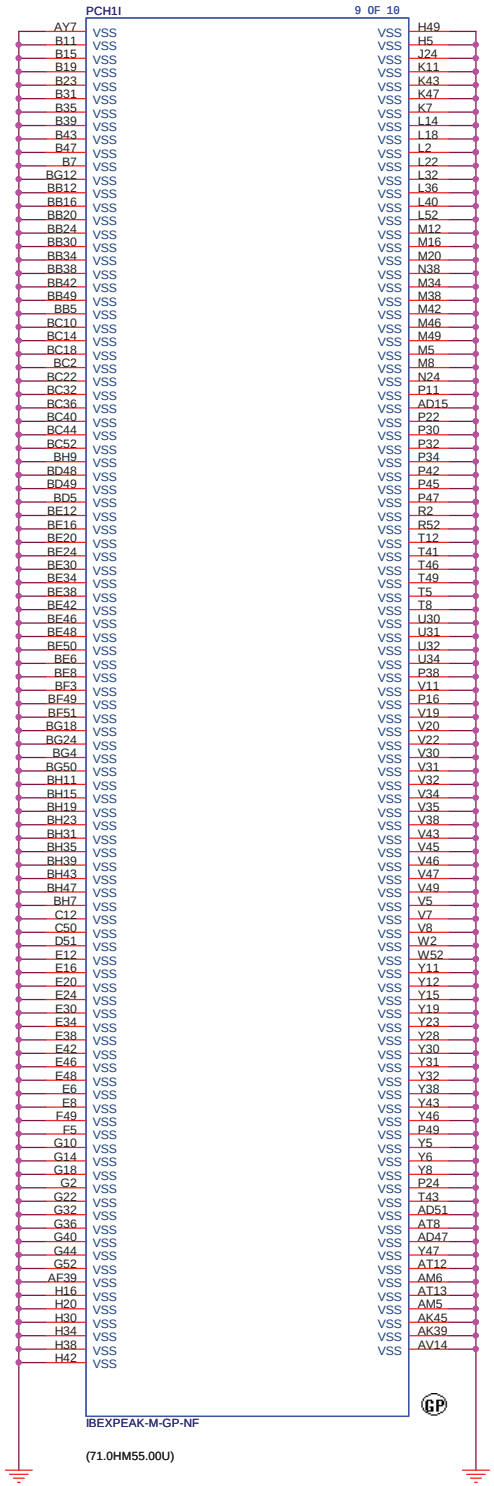
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(8/9)

Size: A2 | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 21 of 59





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH(9/9)***

Size	Document Number	Rev
A3	Catalina	SA

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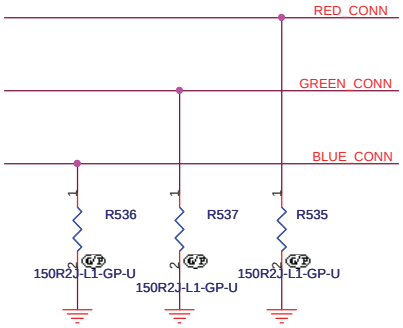
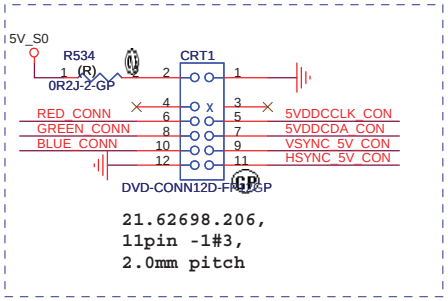
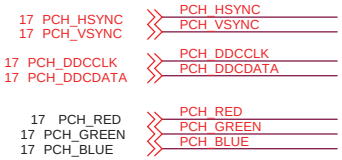
CRT header for debug

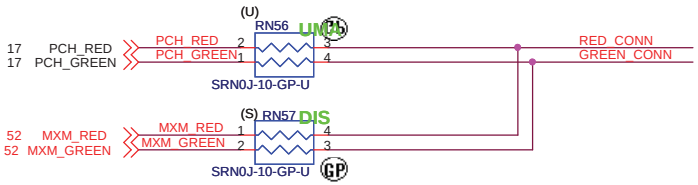


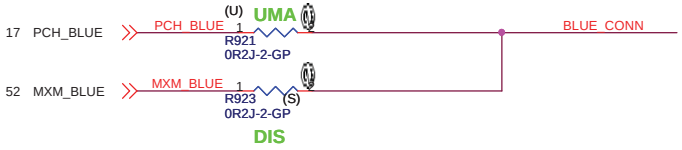


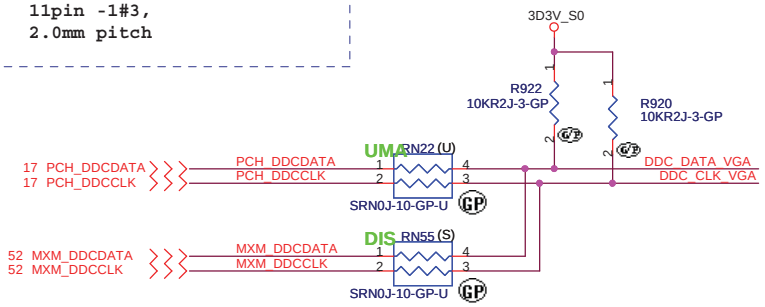
From PCH

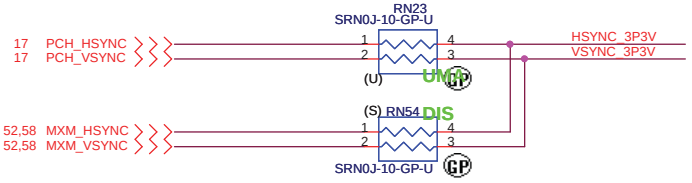


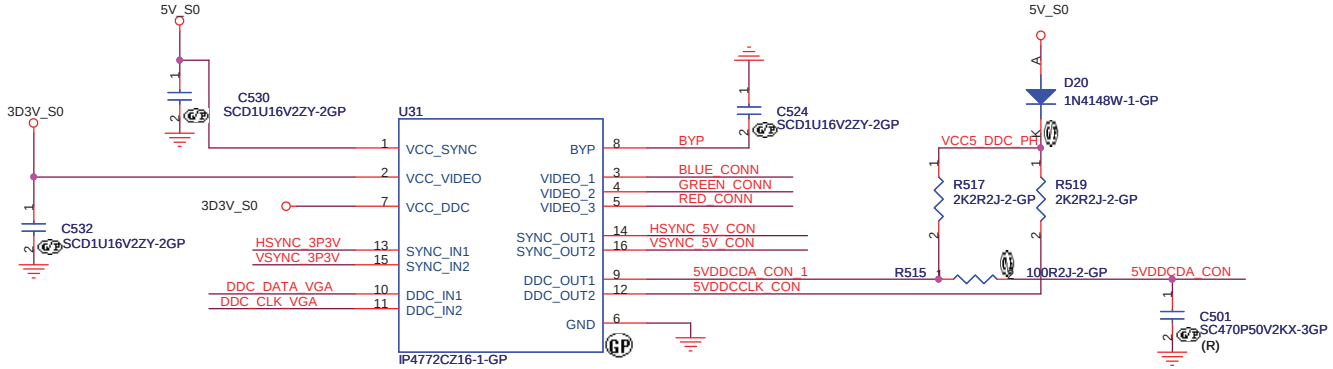
From MXM











<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA header**

Size	Document Number	Rev
B	Catalina	SA

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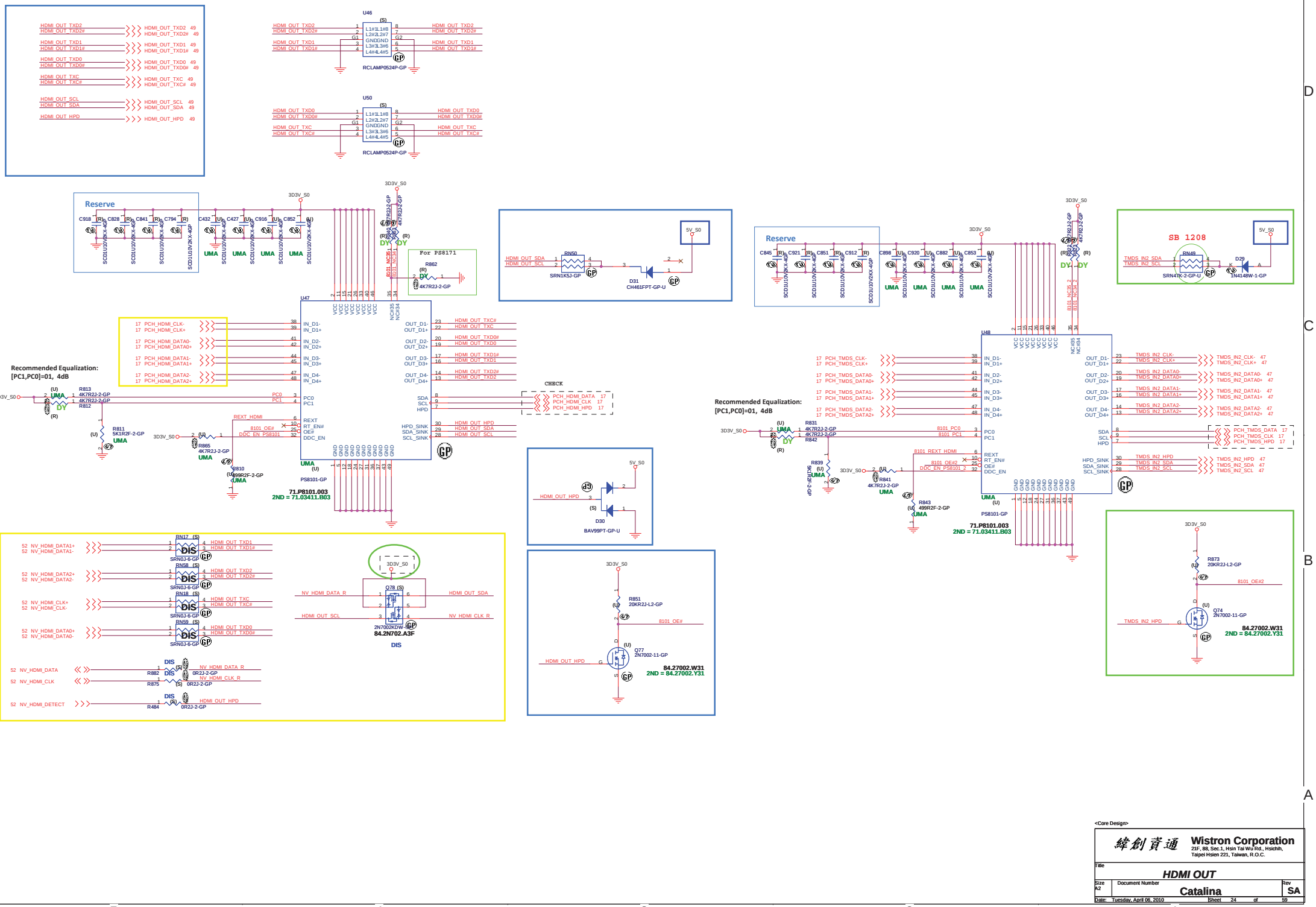
CHECK UMA AND DIS !!



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI OUT**

Size	Document Number	Rev
A2	Catalina	SA

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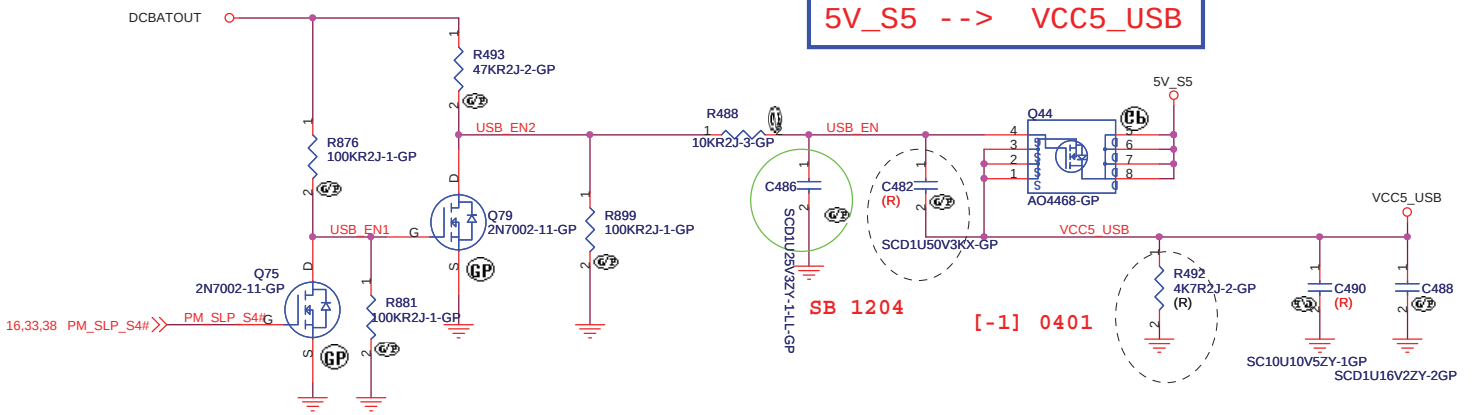
USB PORT

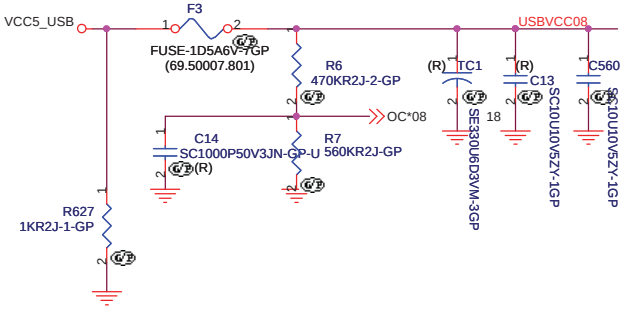
Side 2 USB PORT (0/1)

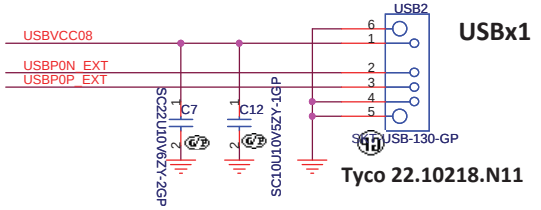
5V_S5 --> VCC5_USB

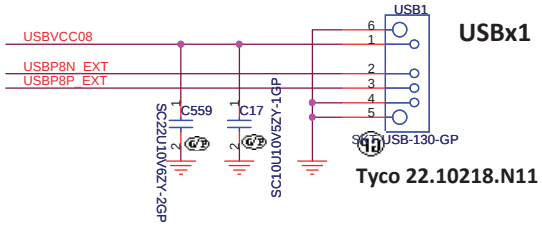


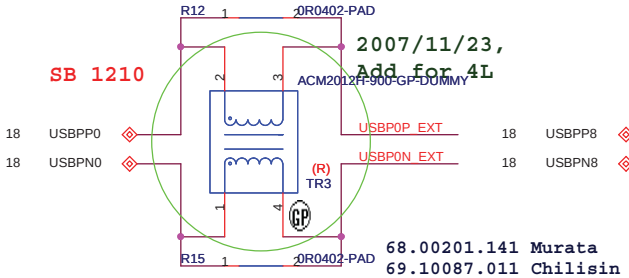
USB Power

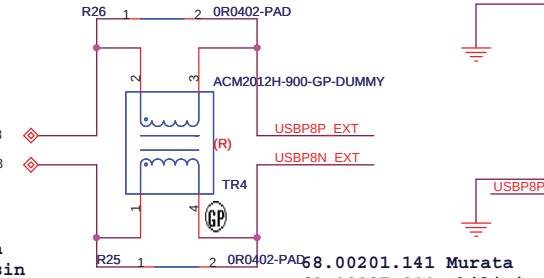
Use 69.50007.801 (Littelfuse)

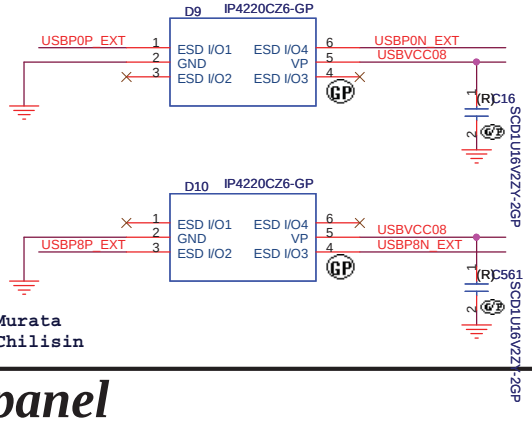




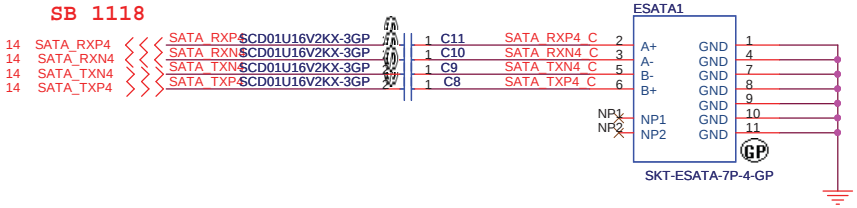




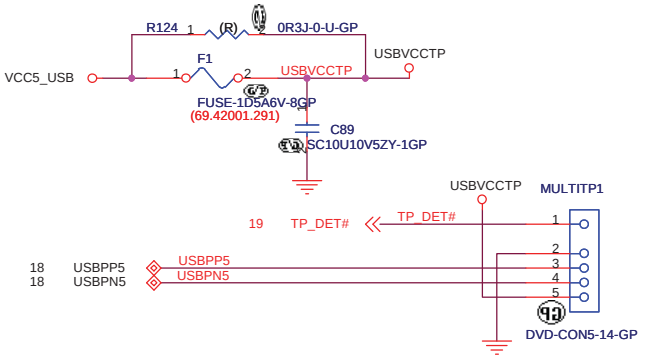




eSATA PORT



Touch panel



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB IO/eSATA/TP**

Size: B | Document Number: **Catalina** | Rev: SA

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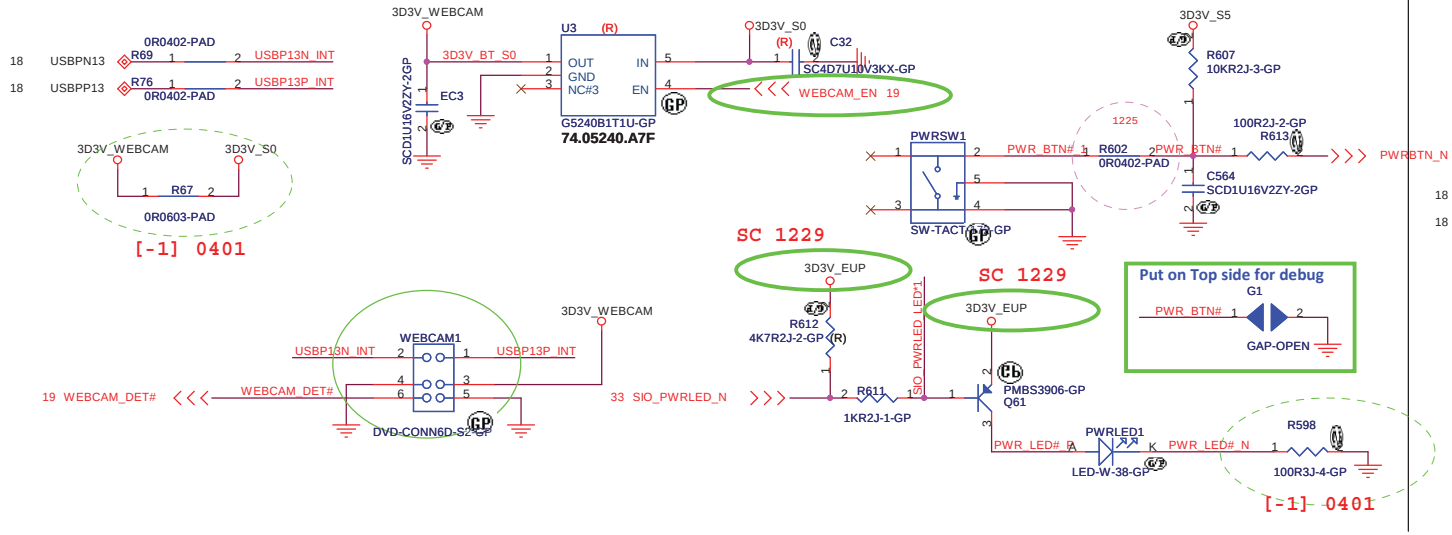
CAMERA

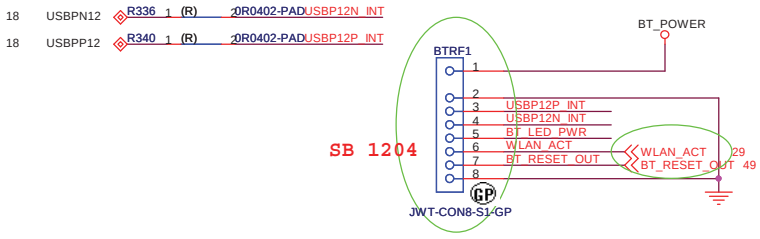


RF->Wireless KB/MS

REMOVE!!

SB 1204

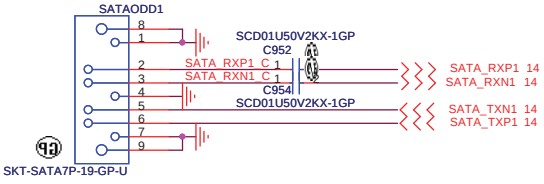
Blue tooth



CD-ROM CONNECTOR

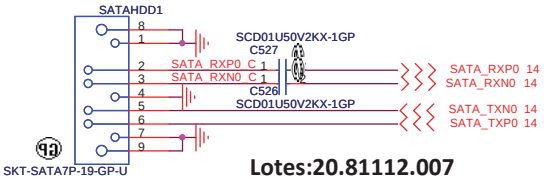
Check HD power(+12V) and connector type

Check connection!!



MAIN HDD Connector

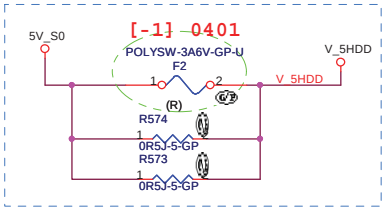
Check connection!!

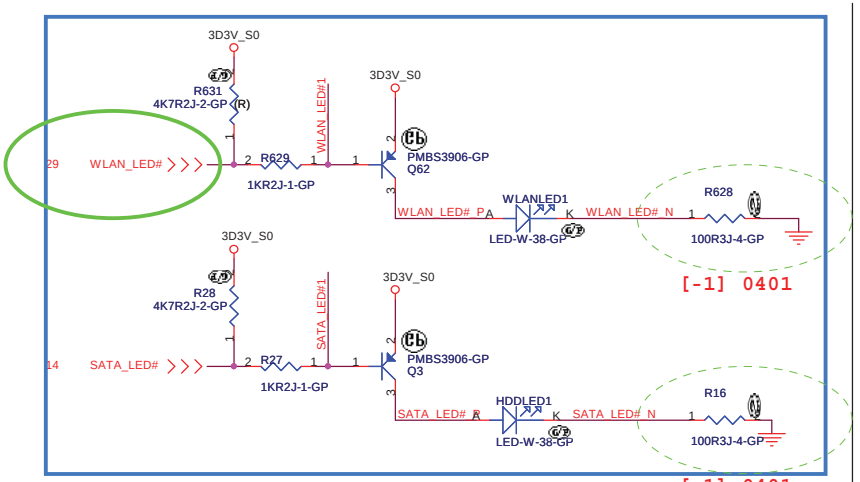


Black

Lotes:20.81112.007

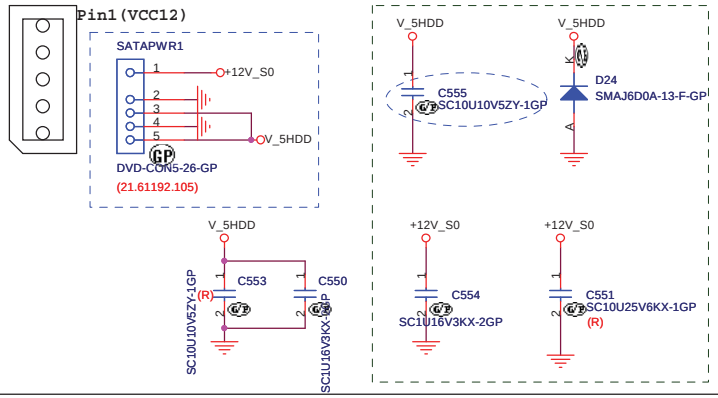
Molex: 20.80618.007



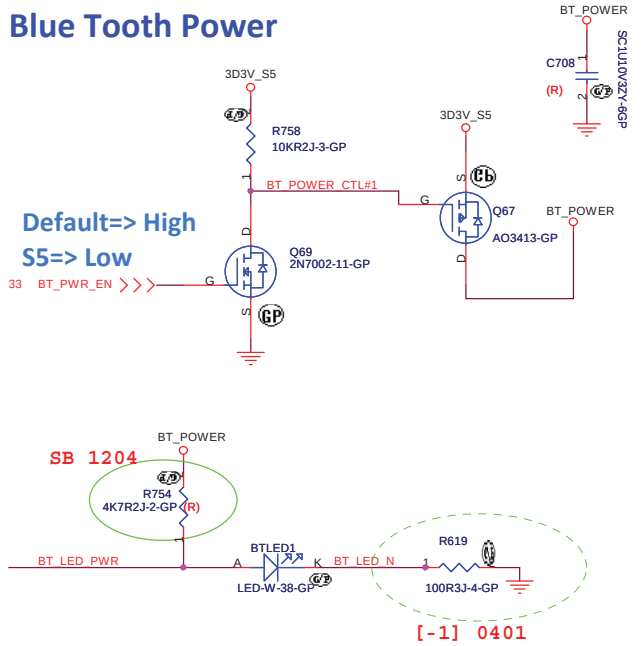


HDD Power Connector

Layout: Please put them together



Blue Tooth Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/ODD IF+USB device**

Size: A3 | Document Number: Catalina | Rev: SA

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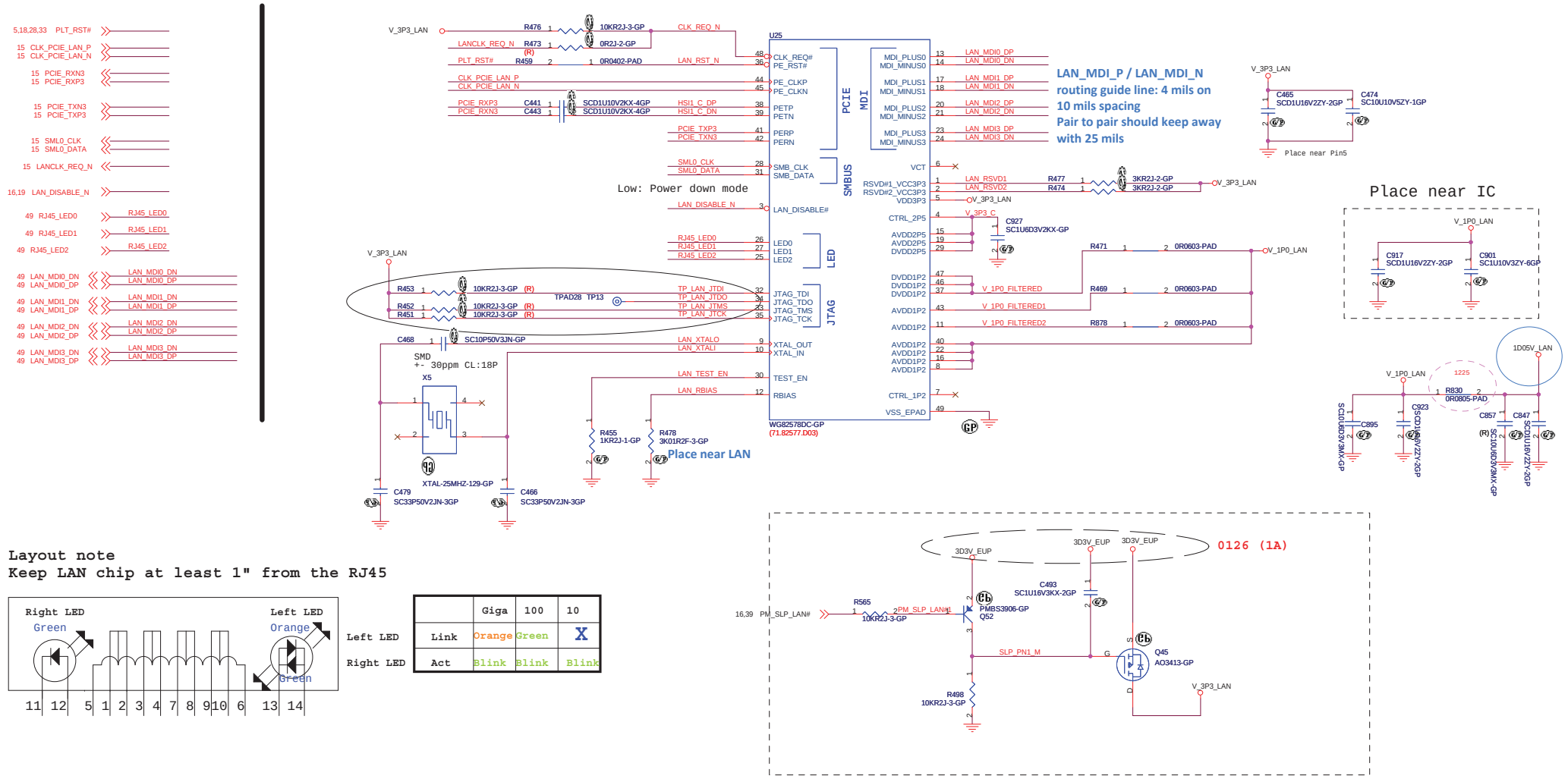

Layout note
Keep LAN chip at least 1" from the RJ45

	Giga	100	10
Left LED	Link	Orange	Green	X
Right LED	Act	Blink	Blink	Blink

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INTEL Gb LAN-WG82577LC

Size: Custom | Document Number: Catalina | Rev: SA

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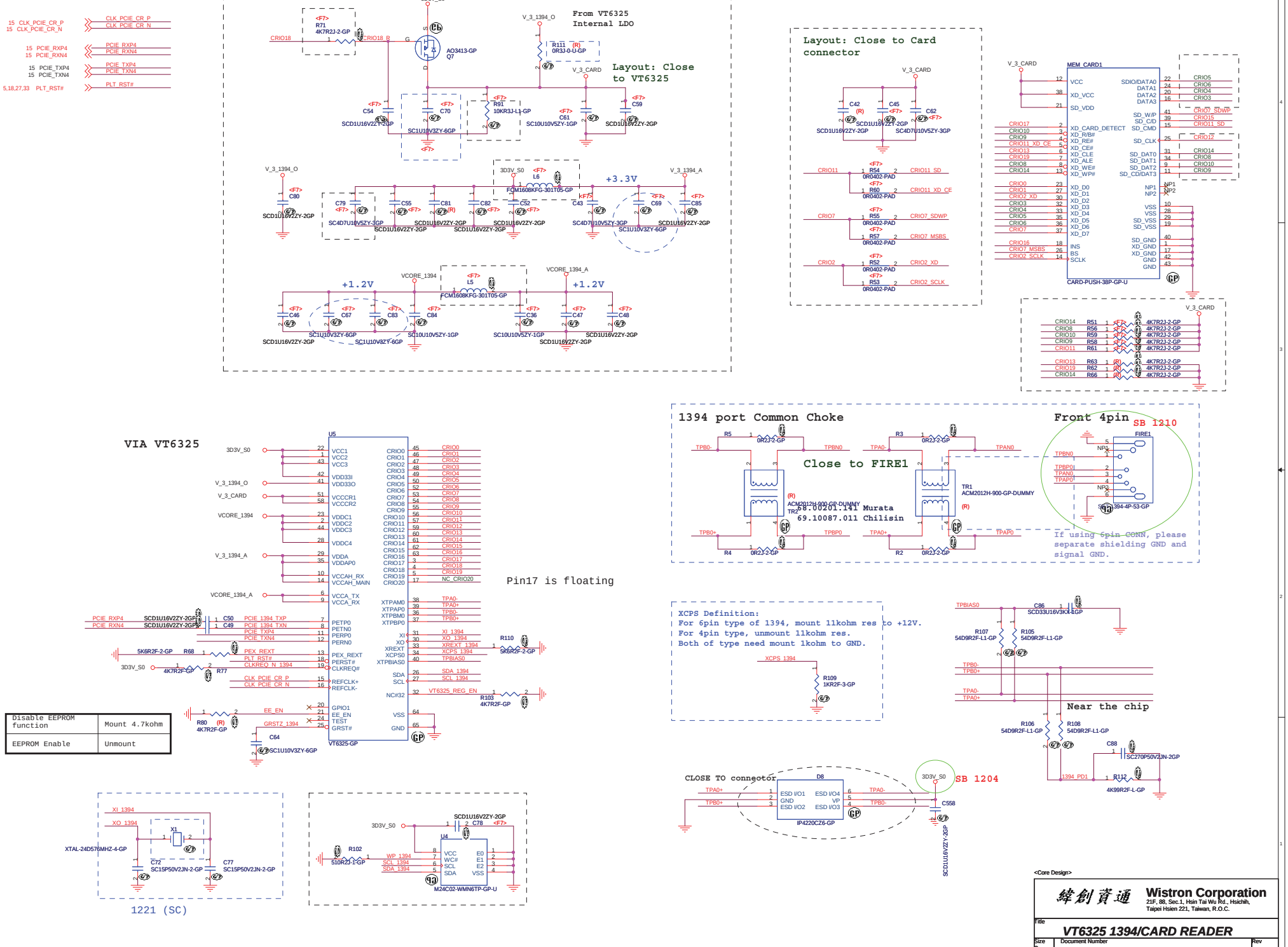
15 CLK_PCIE_CR_P
15 CLK_PCIE_CR_N
CLK_PCIE_CR_P
CLK_PCIE_CR_N
15 PCIE_RXP4
15 PCIE_RXN4
PCIE_RXP4
PCIE_RXN4
15 PCIE_TXP4
15 PCIE_TXN4
PCIE_TXP4
PCIE_TXN4
5,18,27,33 PLT_RST#
PLT_RST#
From VT6325 Internal LDO
Layout: Close to VT6325
Layout: Close to Card connector
VIA VT6325
U5
VT6325-GP
Pin17 is floating
1394 port Common Choke
Close to FIRE1
Front 4pin
SB 1210
FIRE1
TR1 ACM2012H-900-GP-DUMMY
TR2 ACM2012H-900-GP-DUMMY
If using 6pin CONN, please separate shielding GND and signal GND.
XCPS Definition:
For 6pin type of 1394, mount 11kohm res to +12V.
For 4pin type, unmount 11kohm res.
Both of type need mount 1kohm to GND.
Near the chip
CLOSE TO connector
SB 1204
IP4220CZ6-GP
MEM_CARD1
CARD-PUSH-38P-GP-U
M24C02-WMN6TP-GP-U
XTAL-24D576MHZ-4-GP
1221 (SC)
Disable EEPROM function
Mount 4.7kohm
EEPROM Enable
Unmount
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
VT6325 1394/CARD READER
Catalina
Size C
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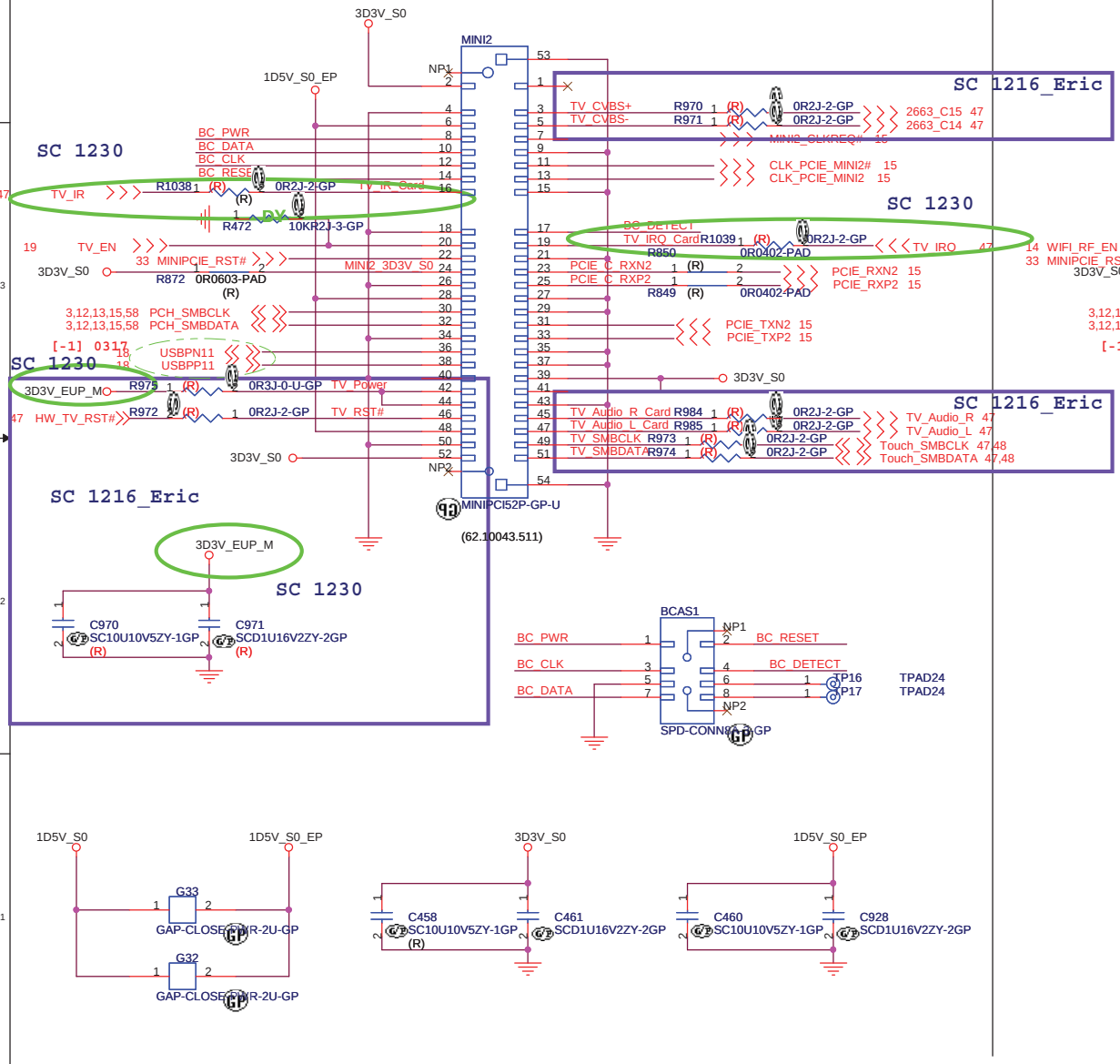
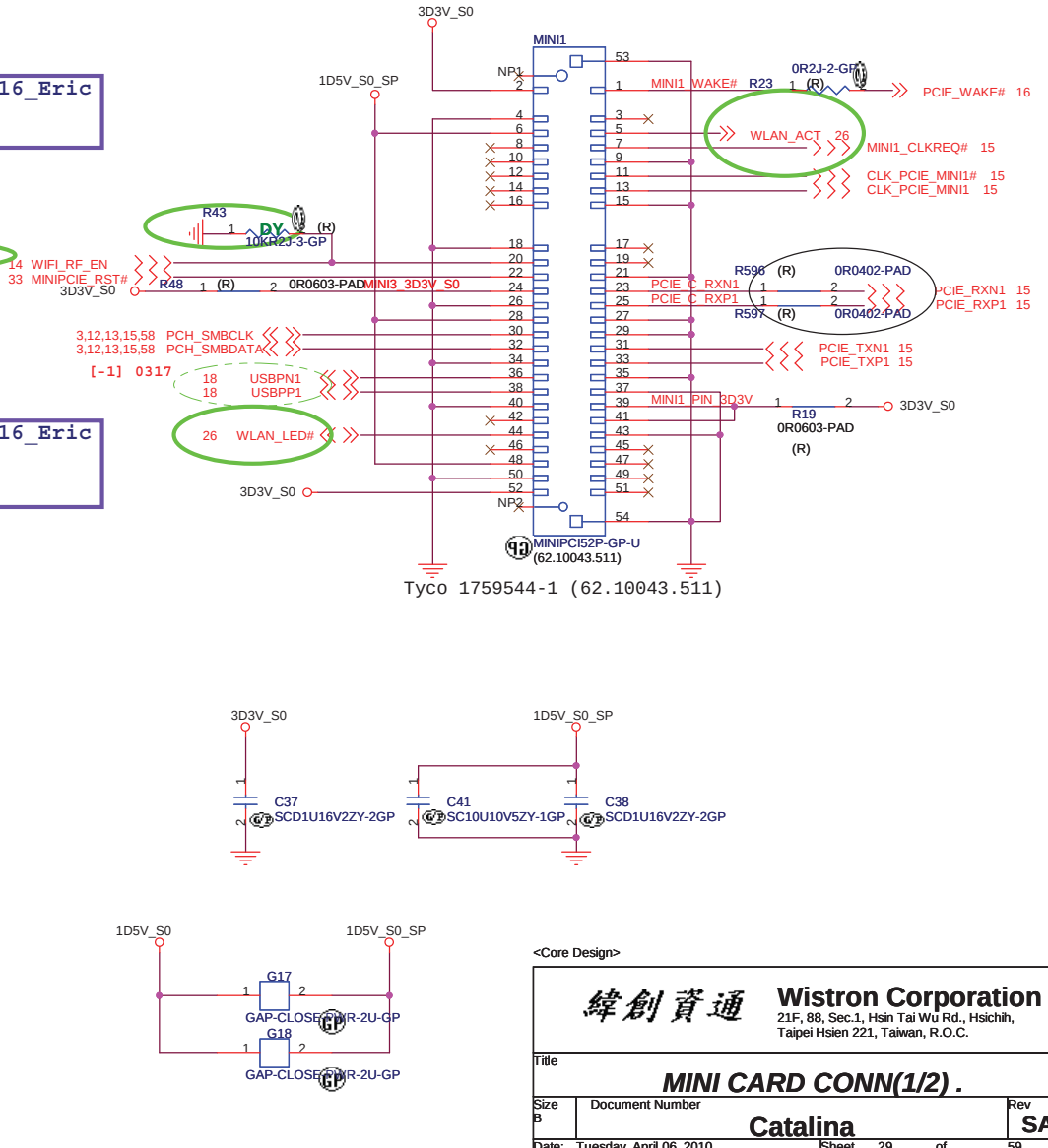
Mini PCI-E Connector

TV-TUNER Card



Wireless Card(Present support EP/SP)



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **MINI CARD CONN(1/2) .**		
Size: B	Document Number: **Catalina**	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 29 of 59	

To PCH

14 ACZ_RST#_AUDIO >> ACZ_RST#_AUDIO
14 ACZ_SYNC_AUDIO >> ACZ_SYNC_AUDIO
14 ACZ_SDATAIN0 >> ACZ_SDATAIN0
14 ACZ_BITCLK_AUDIO >> ACZ_BITCLK_AUDIO
14 ACZ_SDATAOUT_AUDIO >> ACZ_SDATAOUT_AUDIO
14 ACZ_SPKR >> ACZ_SPKR

MIC JK IN

32 MIC_R_JACK >> MIC_R_JACK
32 MIC_L_JACK >> MIC_L_JACK

SPDIF

49 SPDIF <<< SPDIF

Jack Detect

32 MIC_IN_JD >> MIC_IN_JD
32 HP_OUT_JD >> HP_OUT_JD

AMP mute logic use

32 EAPD# <<< EAPD#

Put near Pin38

near codec

SB 1209

AUDIO OUT TO SCALAR

32 PC_AUDIO_L <<< PC_AUDIO_L
32 PC_AUDIO_R <<< PC_AUDIO_R

U2

ALC272 (LQFP-48)

REALTEK

SB 1209 DELETE!!

SPDIF OUT

[-1] 0317

EXT_MIC

MIC_R_JACK 32
MIC_L_JACK 32
MIC_IN_JD 32

ACZ_RST#_AUDIO 14
ACZ_SYNC_AUDIO 14
ACZ_SDATAIN0 14
ACZ_BITCLK_AUDIO 14
ACZ_SDATAOUT_AUDIO 14

14 ACZ_SPKR >>

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC-ALC272

Size: Custom | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 30 of 59

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserve

Size	Document Number	Rev
B	**Catalina**	SA

Date: Tuesday, April 06, 2010 Sheet 31 of 59

MIC IN

30 MIC_L_JACK
30 MIC_R_JACK

HP OUT

30 ALC272_HP_OUT_L → ALC272_HP_OUT_L
30 ALC272_HP_OUT_R → ALC272_HP_OUT_R

JACK DETECT

30 MIC_IN_JD → MIC_IN_JD
30 HP_OUT_JD → HP_OUT_JD

30 EAPD# → EAPD#

47,48 TPA3113_SD# → TPA3113_SD#

LINE OUT to Scalar

30 PC_AUDIO_R → PC_AUDIO_R
30 PC_AUDIO_L → PC_AUDIO_L

47 PC_AUDIO_R_C → PC_AUDIO_R_C
47 PC_AUDIO_L_C → PC_AUDIO_L_C

HP JACK (14/15)

Cehck Jack Spec

HP OUT

SB 1209
DELETE!!

SB 1209
DELETE!!

5V_EUP
AUD_AGND
MUTE_LO#
MUTE_LO*
ALC272_HP_OUT_L
ALC272_HP_OUT_R
ALC272_MUTE
R65 10KR2J-3-GP
R70 4K7R2J-2-GP
Q8 PMBS3906-GP
R10 1KR2J-1-GP
R11 1KR2J-1-GP
R8 100R2J-2-GP
R9 100R2J-2-GP
L3 FCM1608KF-1-GP
L4 FCM1608KF-1-GP
Impedance=60 ohm
R22 4K7R2J-2-GP
R21 4K7R2J-2-GP
Q2 PMBS3904-1-GP
Q1 PMBS3904-1-GP
R64 100KR2J-1-GP
D25 1N4148W-1-GP
R46 10KR2J-3-GP
Q6 PMBS3904-1-GP
EAPD#
TPA3113_SD#
R84 10KR2J-3-GP
Q9 MMBT3904-7-F-GP (R)
(R)

HP_OUT_L_C
HP_OUT_R_C
HP_OUT_JD
C1 SC100P50V2JN-3GP (R)
C5 SC100P50V2JN-3GP
C6 SC100P50V2JN-3GP
D1 (R)
D2 (R)
MLVG0402SR005BP-GP
MLVG0402SR005BP-GP
HPOUT1
SHIELDING
GND_1
GND_2
NP1
NP2
AUDIO-JK132-GP
D6
AZ2025-02S-GP

If use: 83.02025.0A1

FRONT MIC JACK (21/22)

MIC IN

MIC_L_JACK
MIC_R_JACK
MIC_IN_L_JK
MIC_IN_R_JK
MIC_IN_JD
L1 FCM1608KF-1-GP
L2 FCM1608KF-1-GP
Impedance=60 ohm
C2 SC100P50V2JN-3GP
C3 SC100P50V2JN-3GP
C4 SC100P50V2JN-3GP (R)
D4 (R)
D3 (R)
MLVG0402SR005BP-GP
MLVG0402SR005BP-GP
MICJK1
SHIELDING
GND_1
GND_2
NP1
NP2
AUDIO-JK132-GP
D5
AZ2025-02S-GP

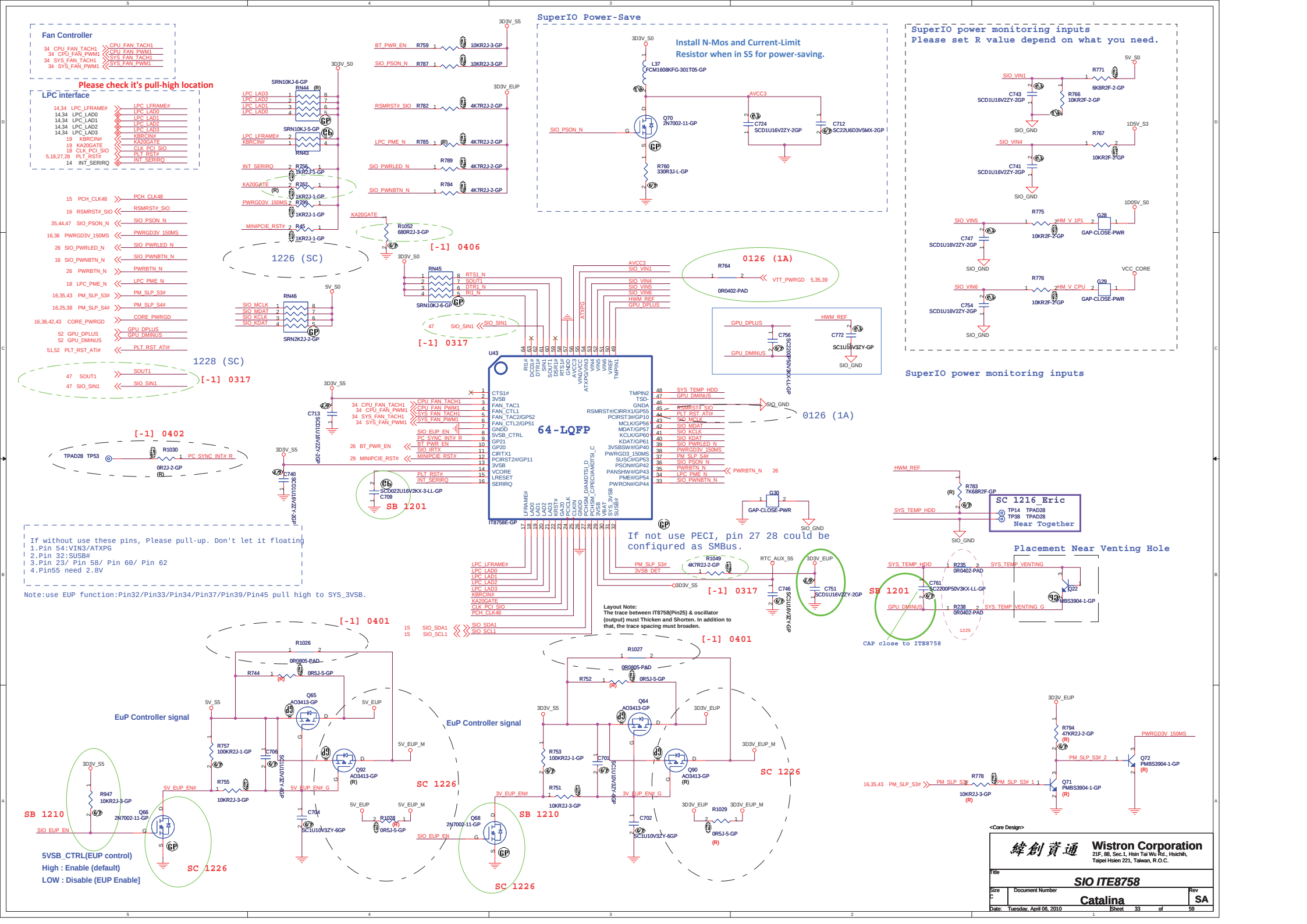
If use: 83.02025.0A1

Speaker Out (35/36) Placement Near Scalar

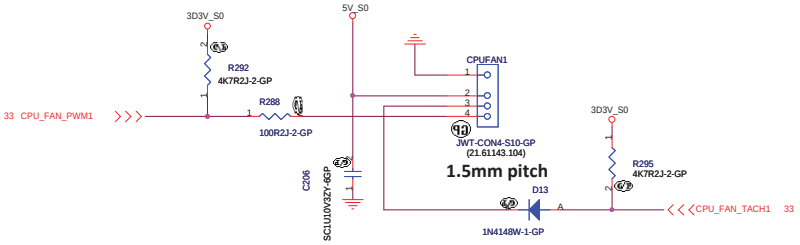
PC_AUDIO_R
PC_AUDIO_L
PC_AUDIO_R_1
PC_AUDIO_L_1
PC_AUDIO_R_C
PC_AUDIO_L_C
R605 0R0402-PAD
R604 0R0402-PAD
C572 SC22U6D3V5MX-2GP
C571 SC22U6D3V5MX-2GP
near codec
near codec
SB 1209
SB 1209
SC 1226
1225
1223
1225
1223

<Core Design>

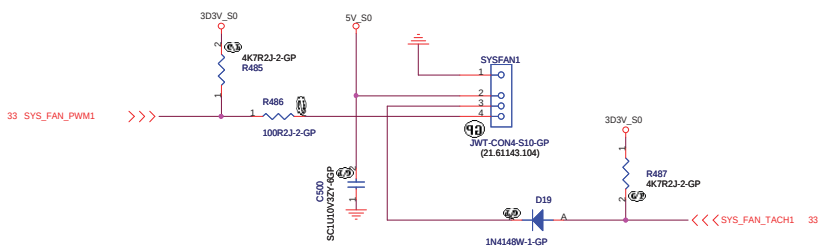
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO HP_JK/ MIC_JK		
Size: A3	Document Number: Catalina	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 32 of 59	


Fan Controller
Please check it's pull-high location
LPC interface
SuperIO Power-Save
Install N-Mos and Current-Limit
Resistor when in S5 for power-saving.
SuperIO power monitoring inputs
Please set R value depend on what you need.
SuperIO power monitoring inputs
1226 (SC)
1228 (SC)
[-1] 0317
[-1] 0406
[-1] 0402
[-1] 0401
0126 (1A)
64-LQFP
IT8758E-GP
SB 1201
SB 1210
SC 1226
Near Together
Placement Near Venting Hole
CAP close to ITE8758
If not use PECI, pin 27 28 could be
configured as SMBus.
If without use these pins, Please pull-up. Don't let it floating
1.Pin 54:VIN3/ATXPG
2.Pin 32:SUSB#
3.Pin 23/ Pin 58/ Pin 60/ Pin 62
4.Pin55 need 2.8V
Note:use EUP function:Pin32/Pin33/Pin34/Pin37/Pin39/Pin45 pull high to SYS_3VSB.
Layout Note:
The trace between IT8758(Pin25) & oscillator
(output) must Thicken and Shorten. In addition to
that, the trace spacing must broaden.
EuP Controller signal
5VSB_CTRL(EUP control)
High : Enable (default)
LOW : Disable (EUP Enable)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SIO ITE8758
Catalina
Tuesday, April 06, 2010
Sheet 33 of 59

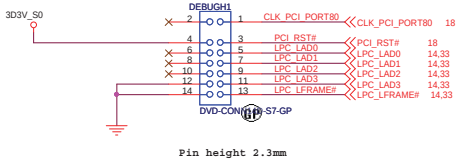
CPU FAN



MXM_SYS FAN

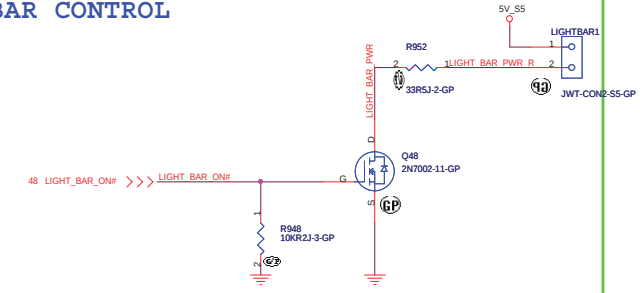


LPC DEBUG PORT

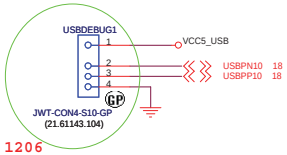


Pin height 2.3mm

LIGHT BAR CONTROL



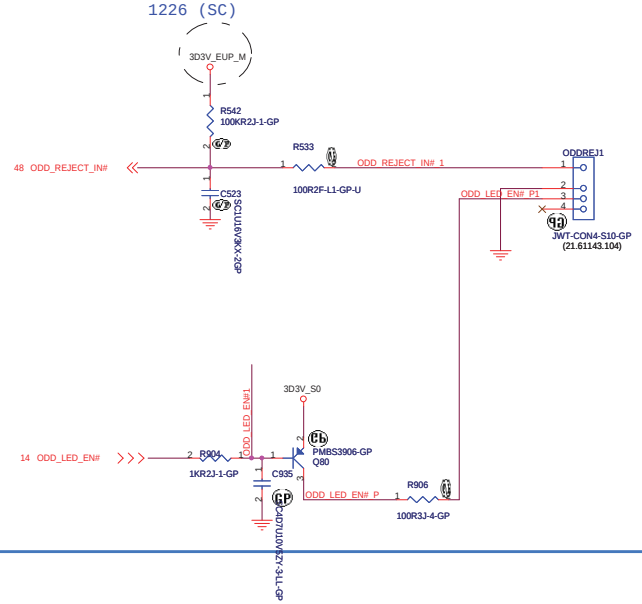
USB RESERVE



SB 1206

ODD REJECTION

1226 (SC)



<Core Design>

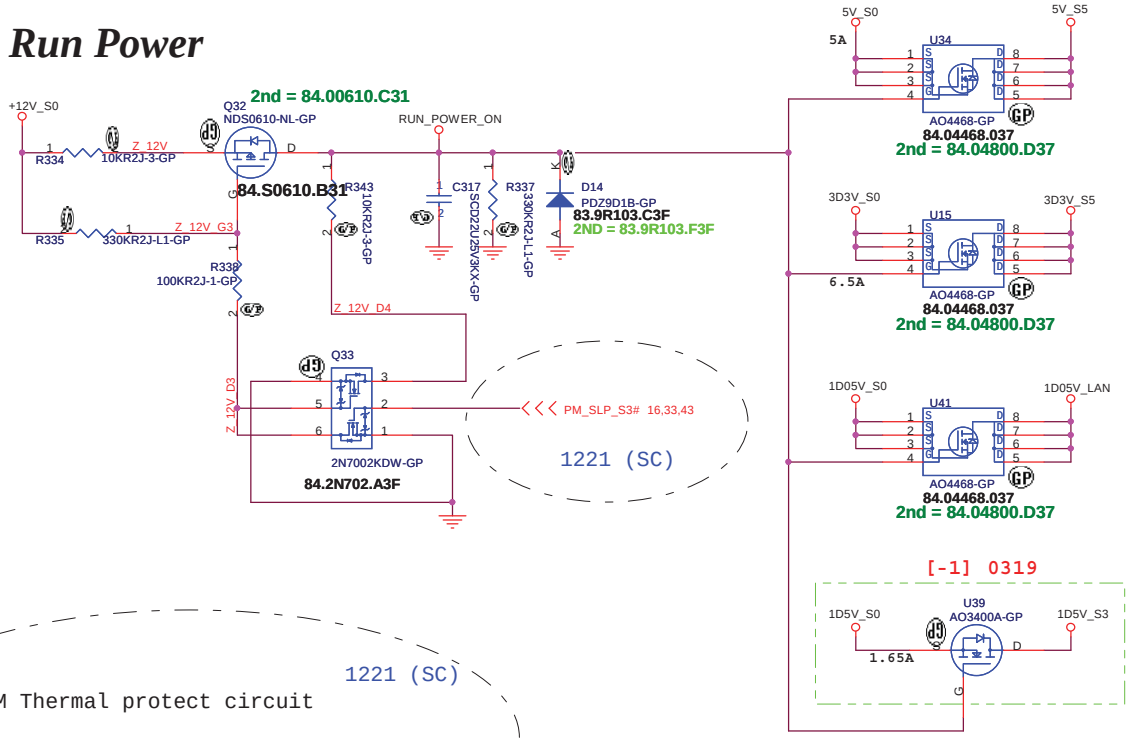
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

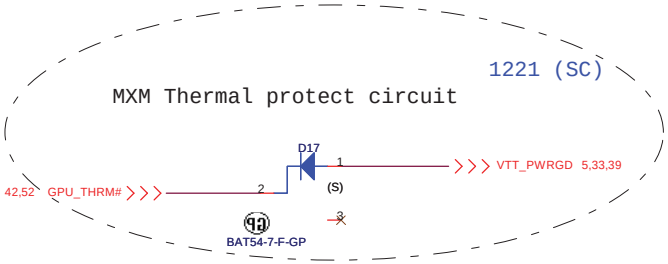
Title: Fan control

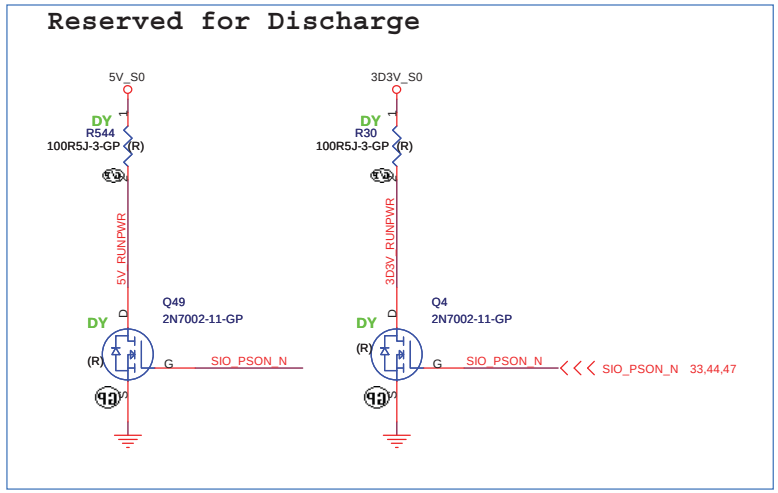
Size	Document Number	Rev
C	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 34 of 59

Run Power







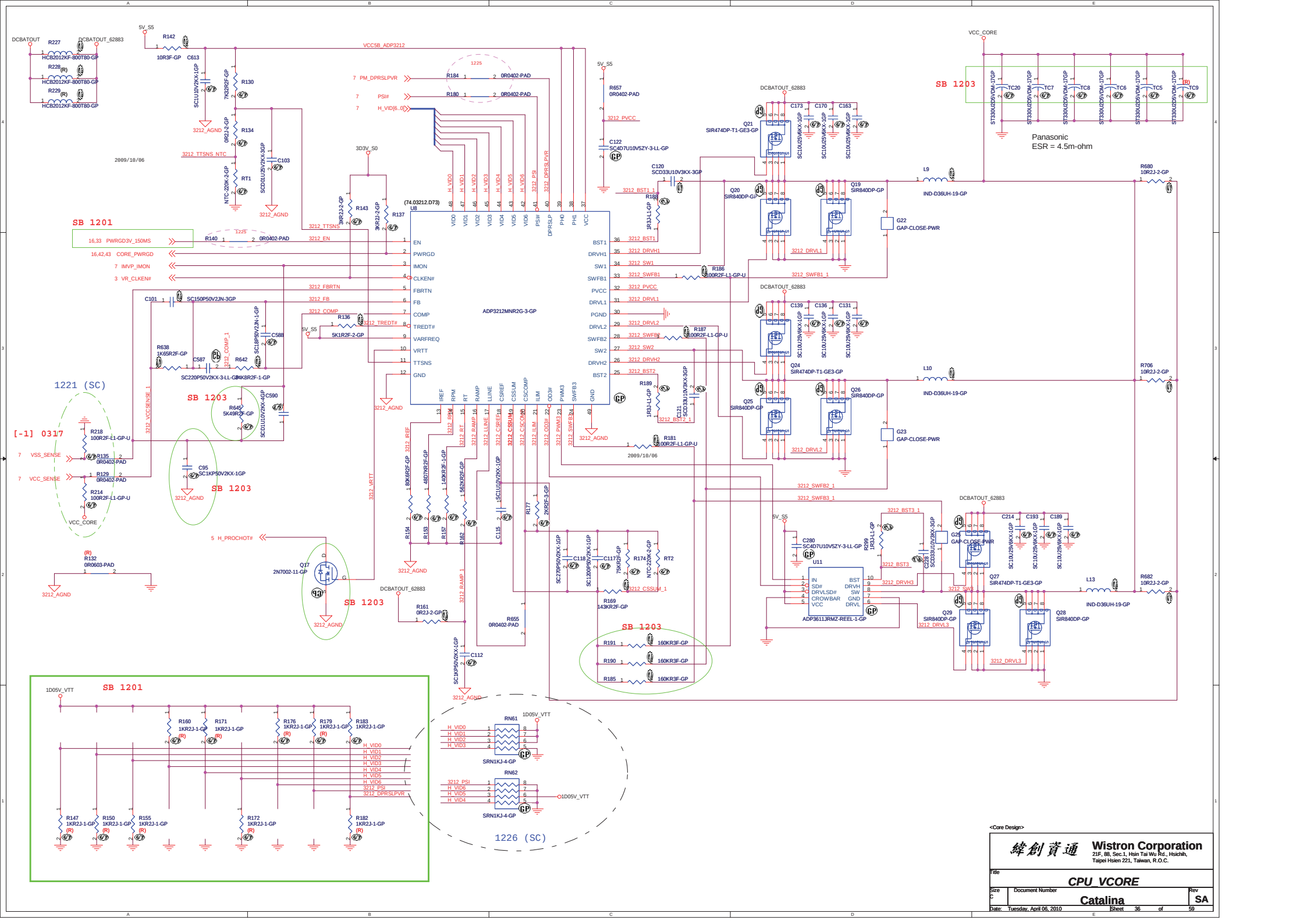
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Run Power

Size: A3 | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 35 of 59


ADP3212MNR2G-3-GP
(74.03212.D73)
U8
SB 1201
SB 1203
1221 (SC)
1226 (SC)
Panasonic
ESR = 4.5m-ohm
2009/10/06
[-1] 0317
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_VCORE
Size C
Document Number
Catalina
Rev SA
Date: Tuesday, April 06, 2010
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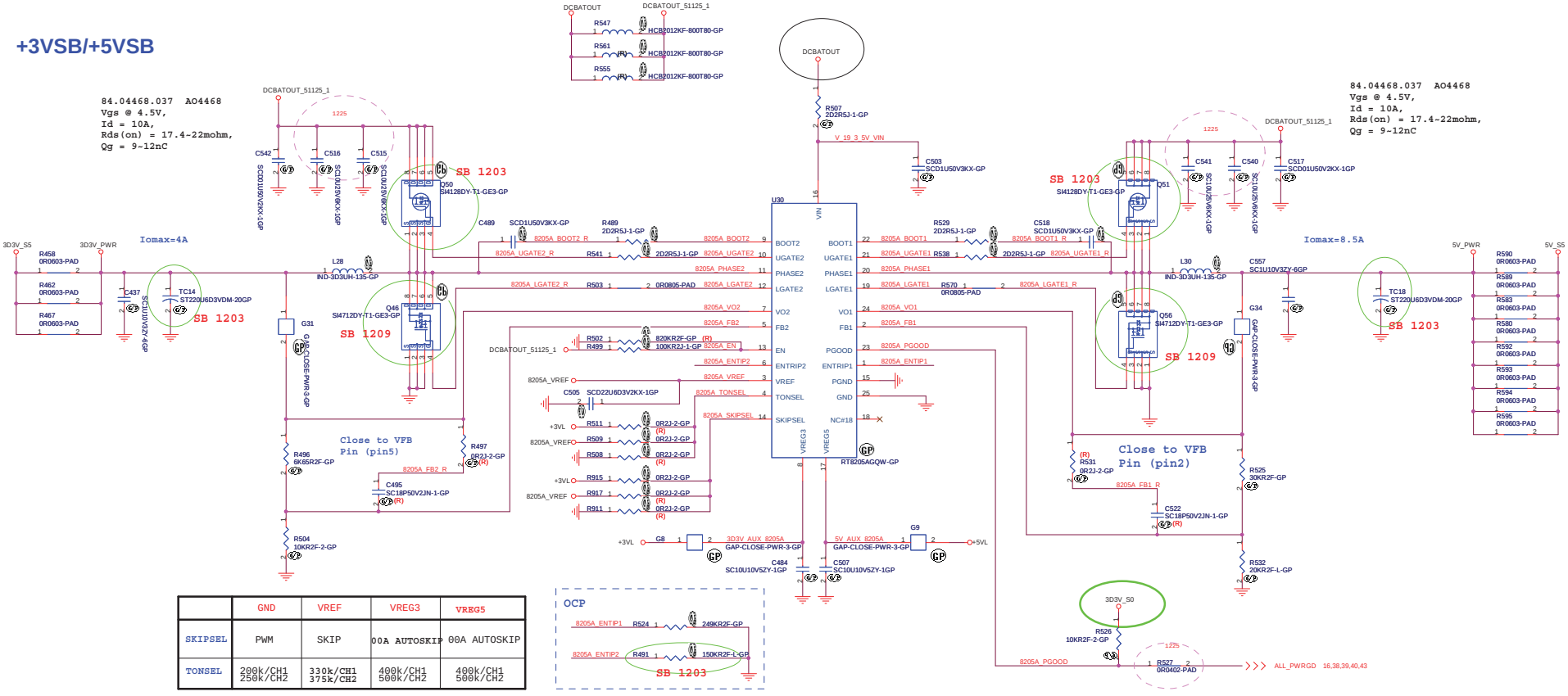
+3VSB/+5VSB



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	330k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2

<Core Design>

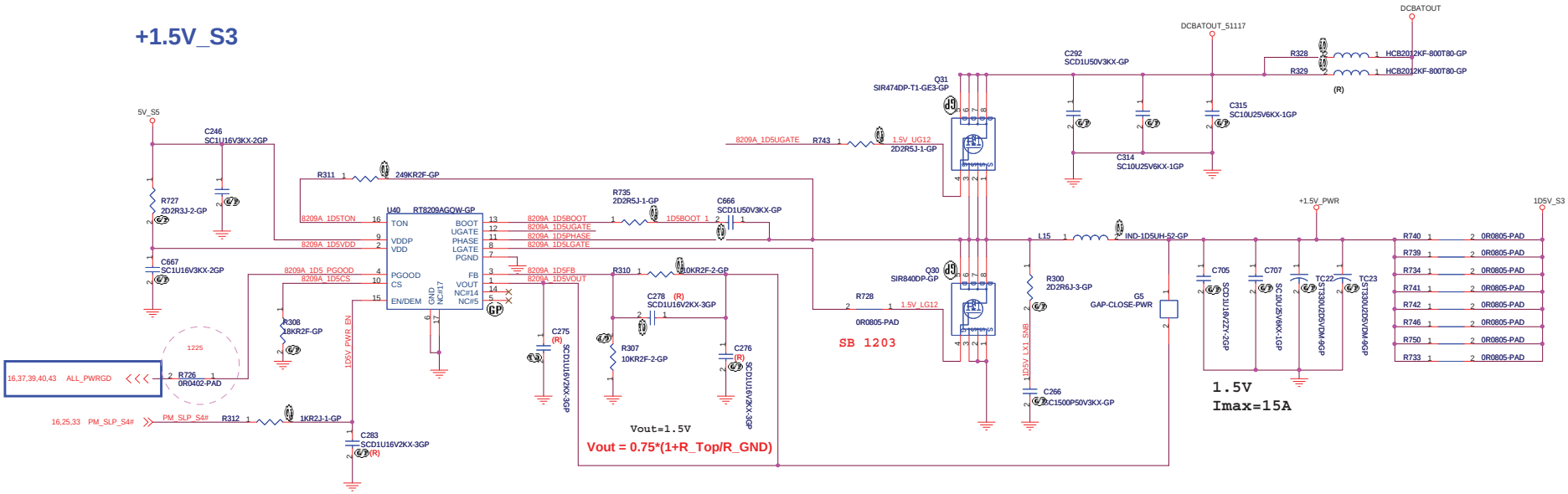
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205A 3V&5V

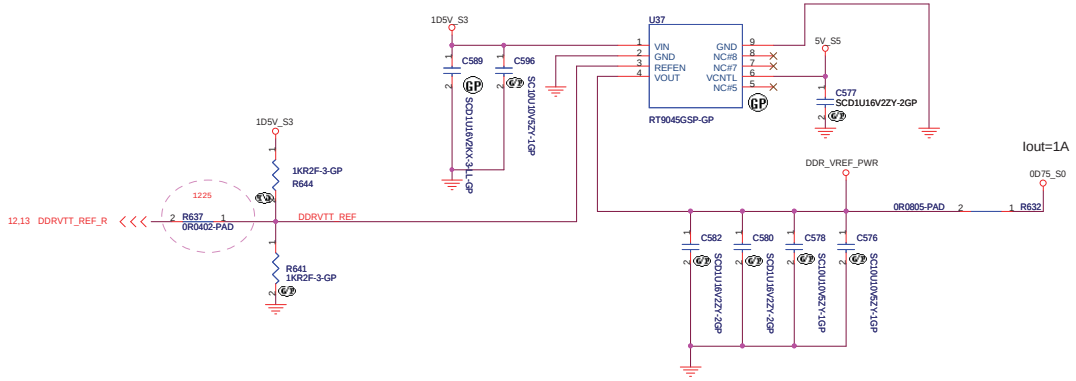
Size: A2 | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 37 of 59

+1.5V_S3



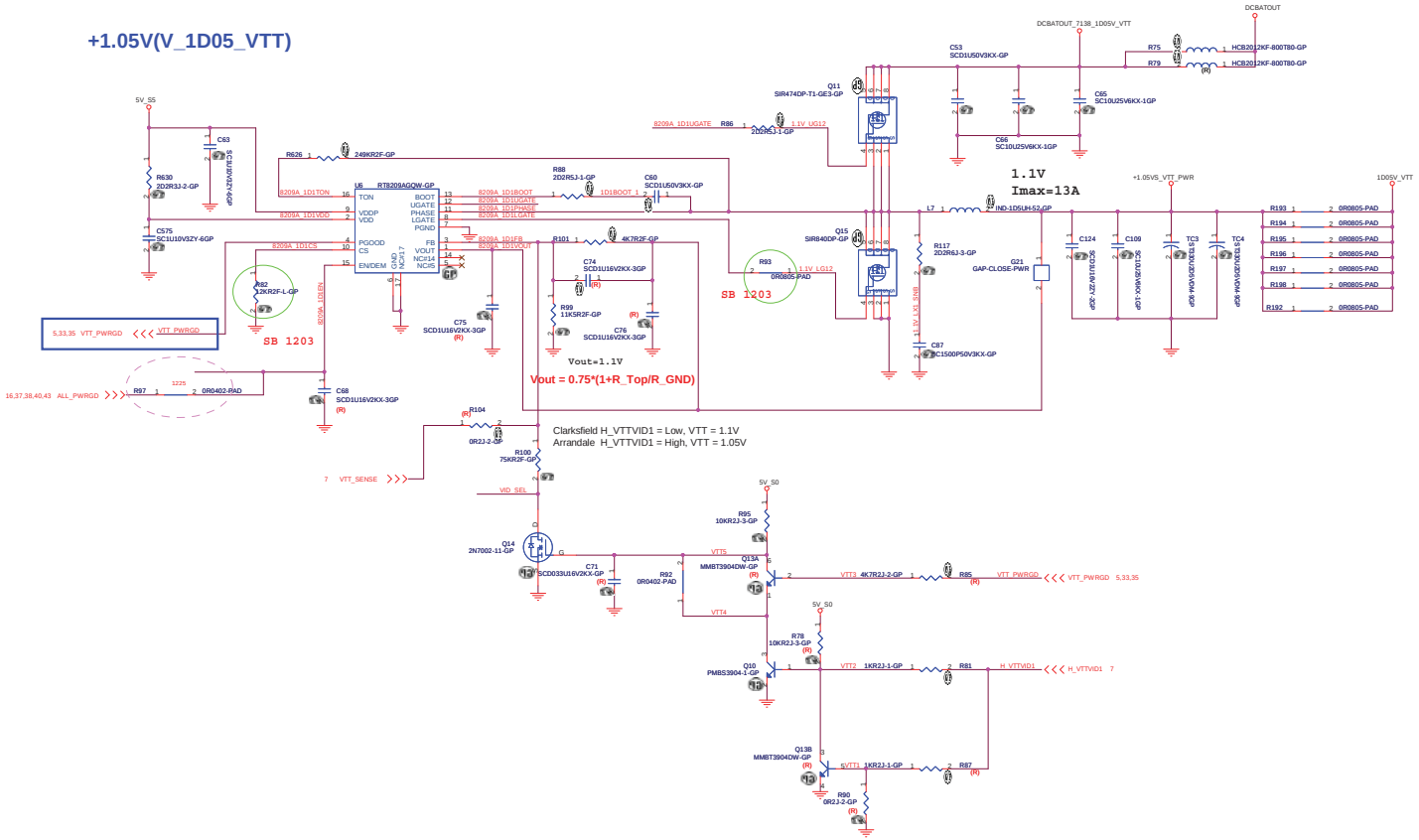
+0.75V_MEM_VTT



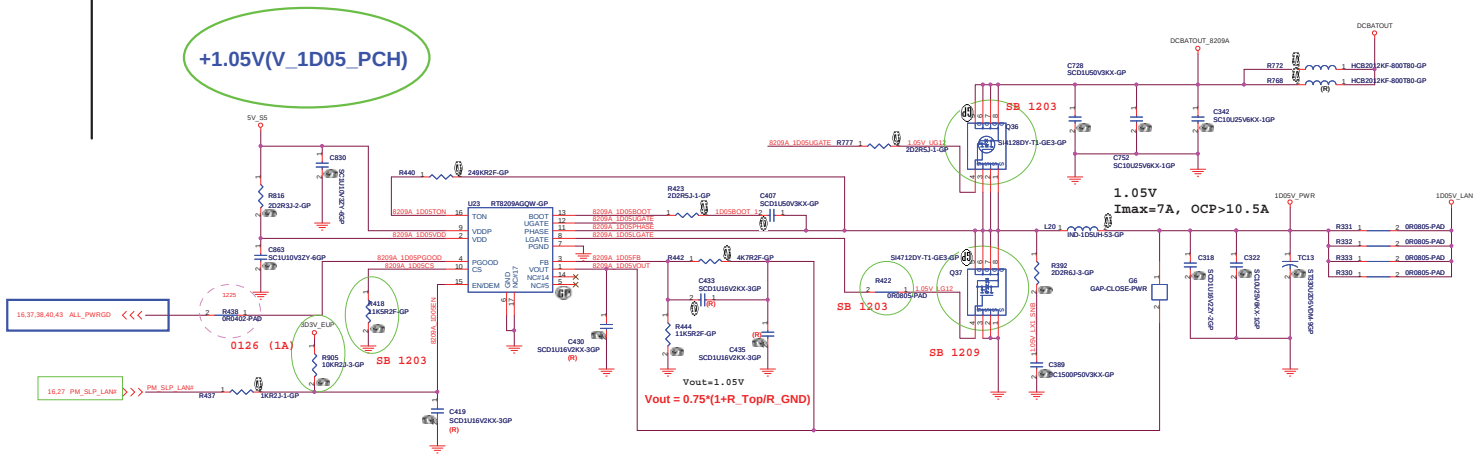
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***+1.5V/+0.75V***	
Size: C	Document Number: **Catalina**	Rev: **SA**
Date: Tuesday, April 06, 2010	Sheet 38 of 59	

+1.05V(V_1D05_VTT)



+1.05V(V_1D05_PCH)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: V_1P1_VTT/ V_1P05_PCH

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Custom	Catalina	SA

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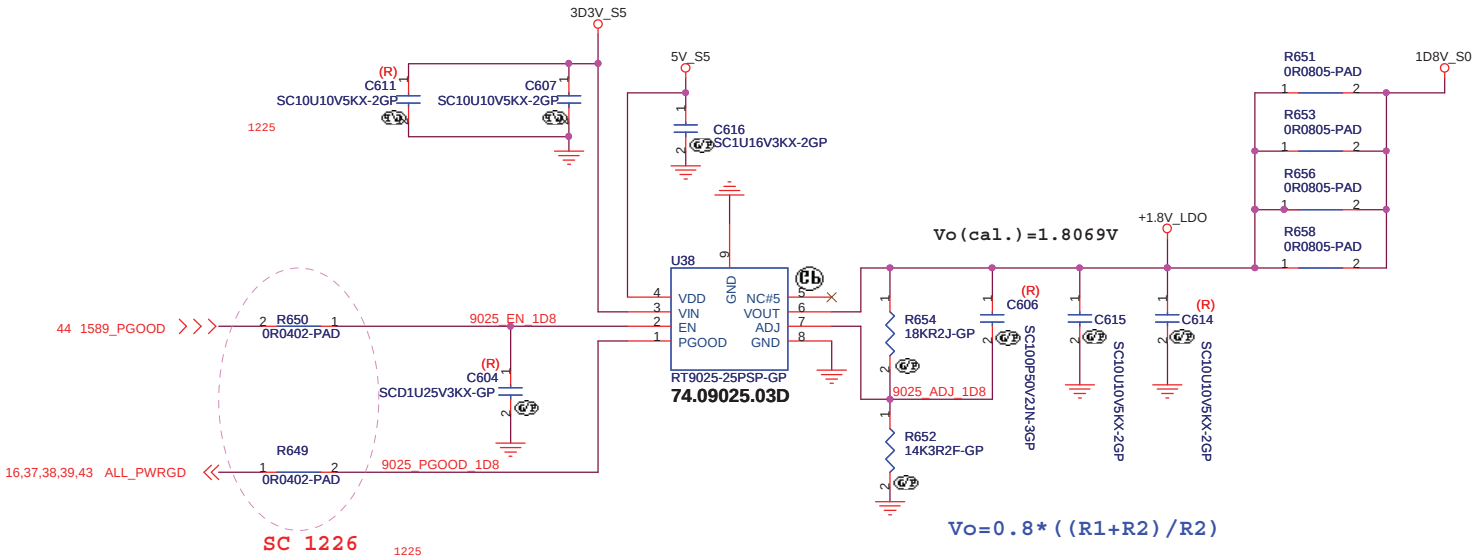
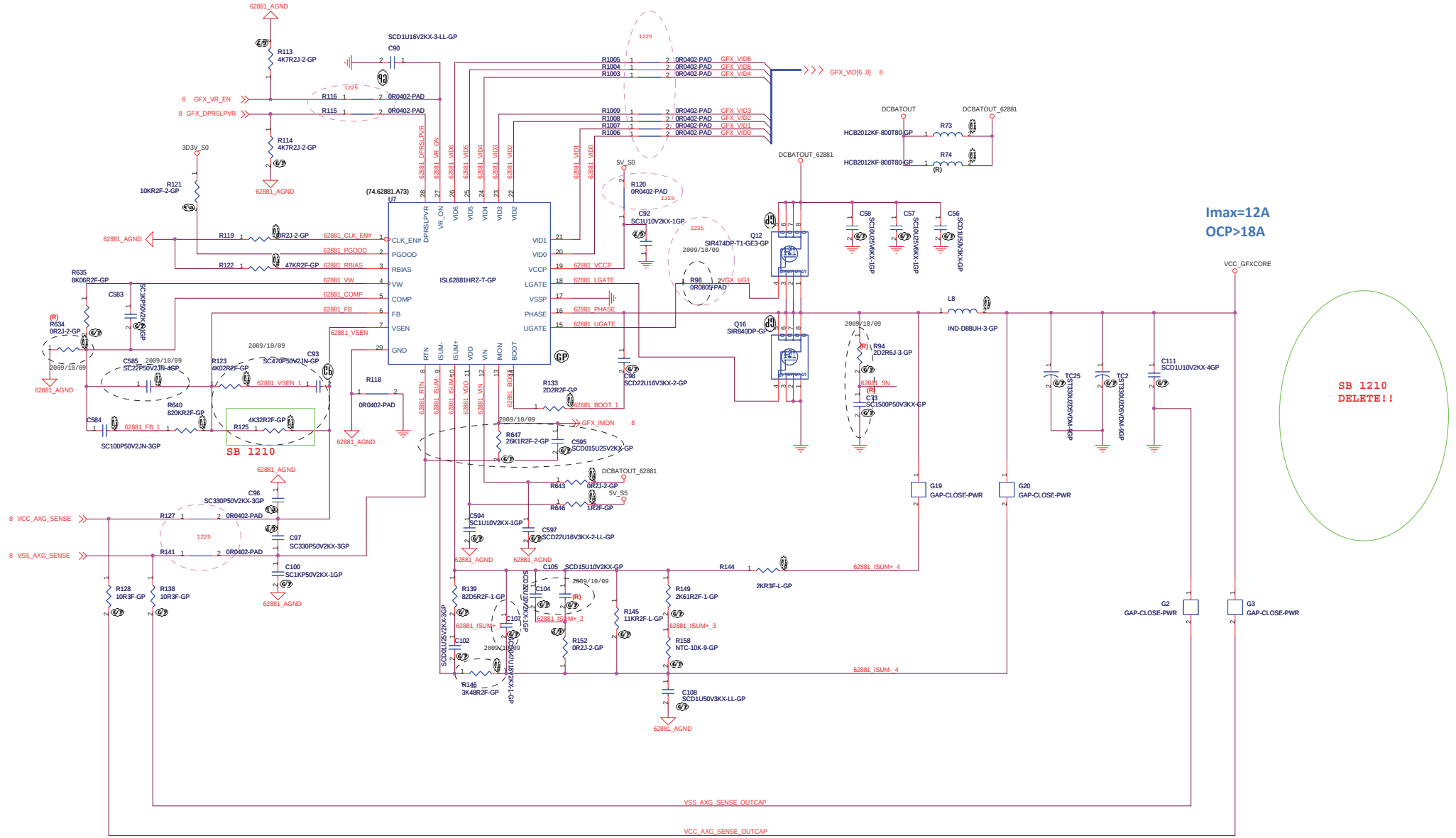
1D8V_S0 (RT9025)



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D8V POWER		
Size: B	Document Number: Catalina	Rev: SA
Date: Tuesday, April 06, 2010	Sheet 40 of 59	



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*GFX_Vcore*
Size: C	Document Number: Catalina
Rev	SA
Date: Tuesday, April 06, 2010	Sheet 41 of 59

For GPU Core and GPIO15/20 relationship as below:

VID1(GPIO20)	VID0(GPIO15)	Core
0	0	1.22V
0	1	1.02V
1	0	1.12V
1	1	0.92V

0.9V~1.2V@20A
OCP>30A

VGA power sequence modify!!

SB 1209

SB 1209

SB 1201

SB 1201

SB 1201

[Park]R412=30.9k
[Madison]R412=28k

[-1] 0317

<Core Design>

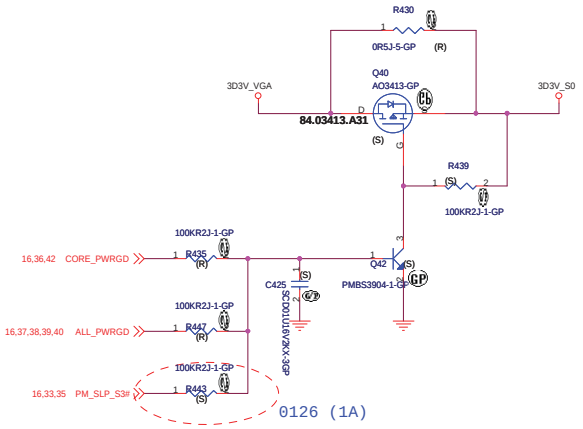
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MXM_GFX_Vcore

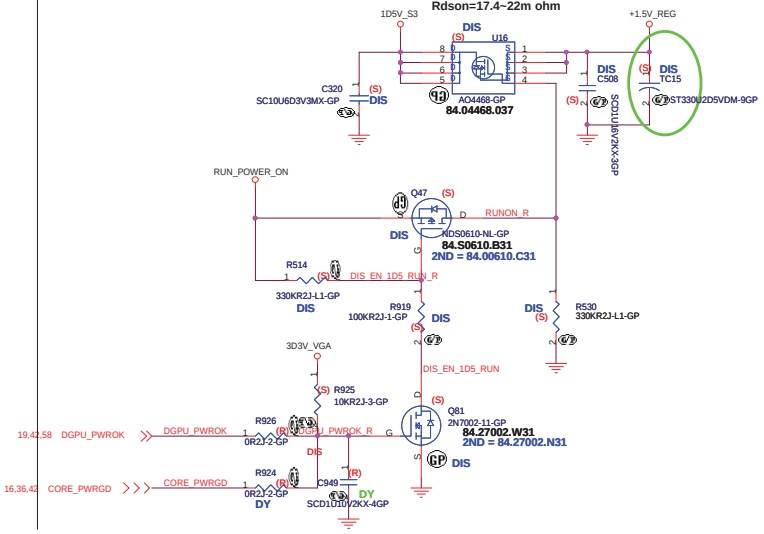
Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 42 of 59

3D3V_S0 to 3D3V_DELAY Transfer

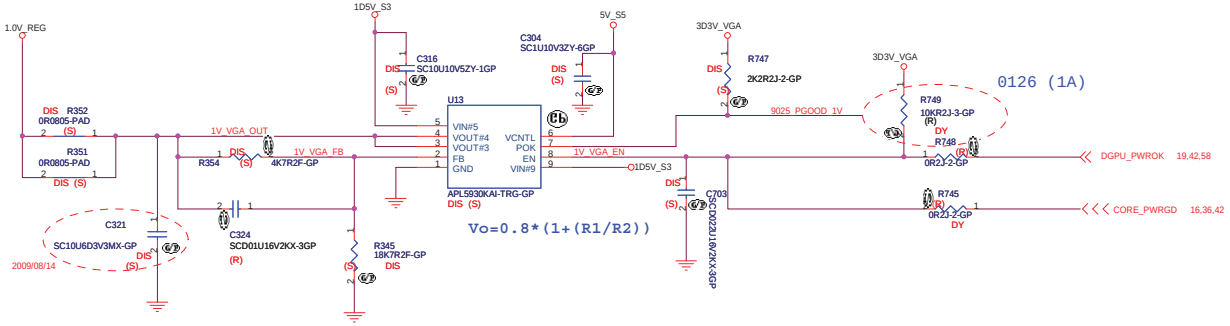


AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



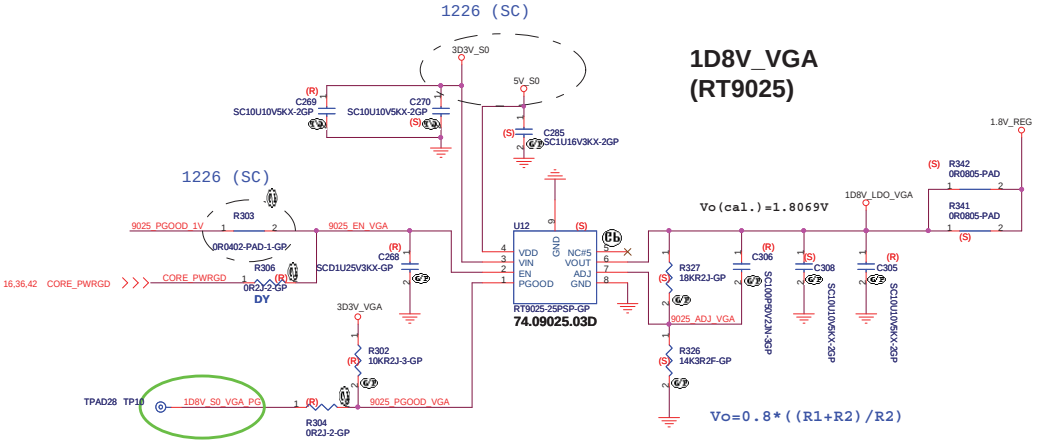
Iout=1.5A

Vout= 1V_VGA



1226 (SC)

1D8V_VGA (RT9025)



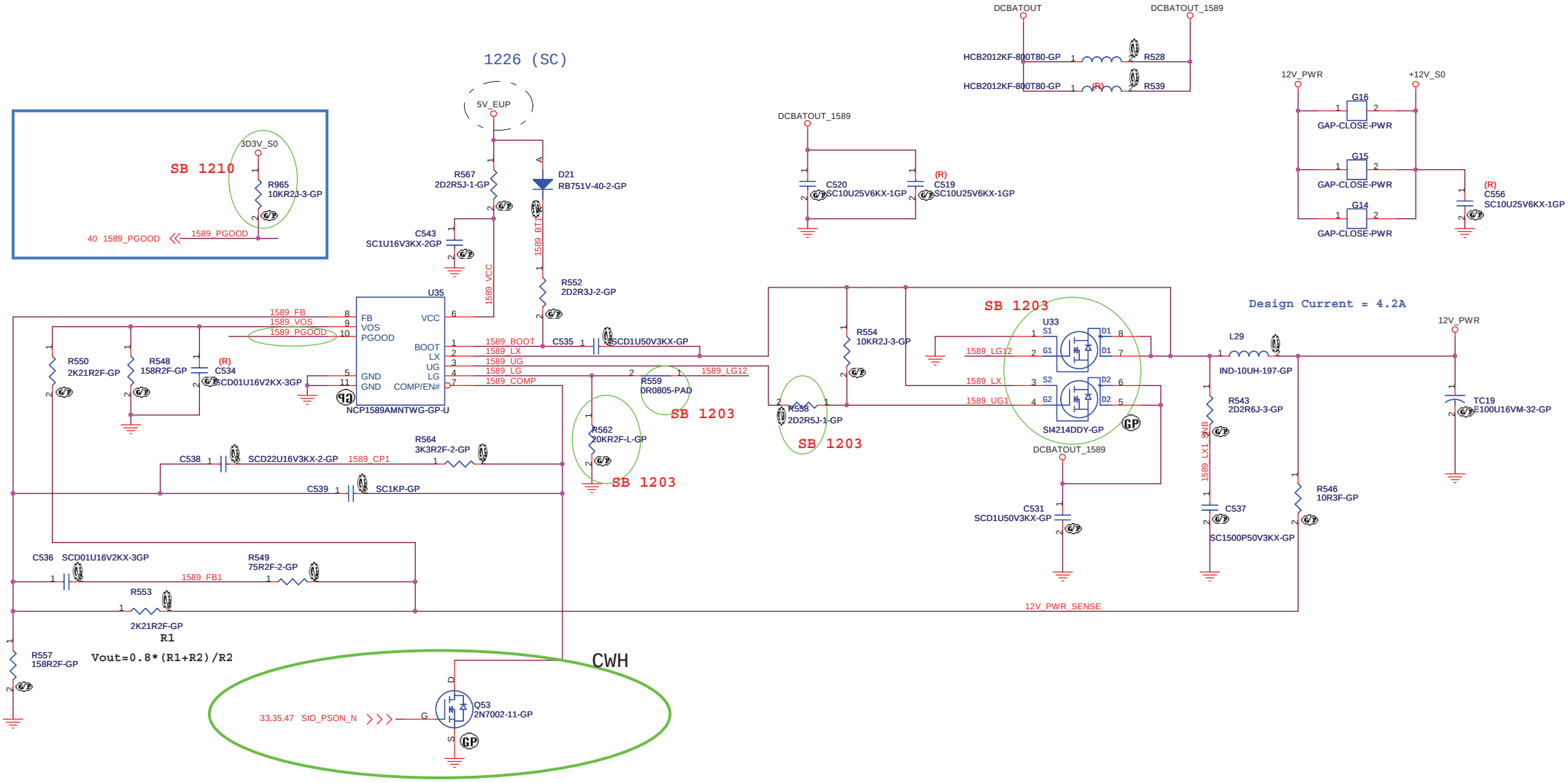
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1.8V_REG/1V_PCIE

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 43 of 59



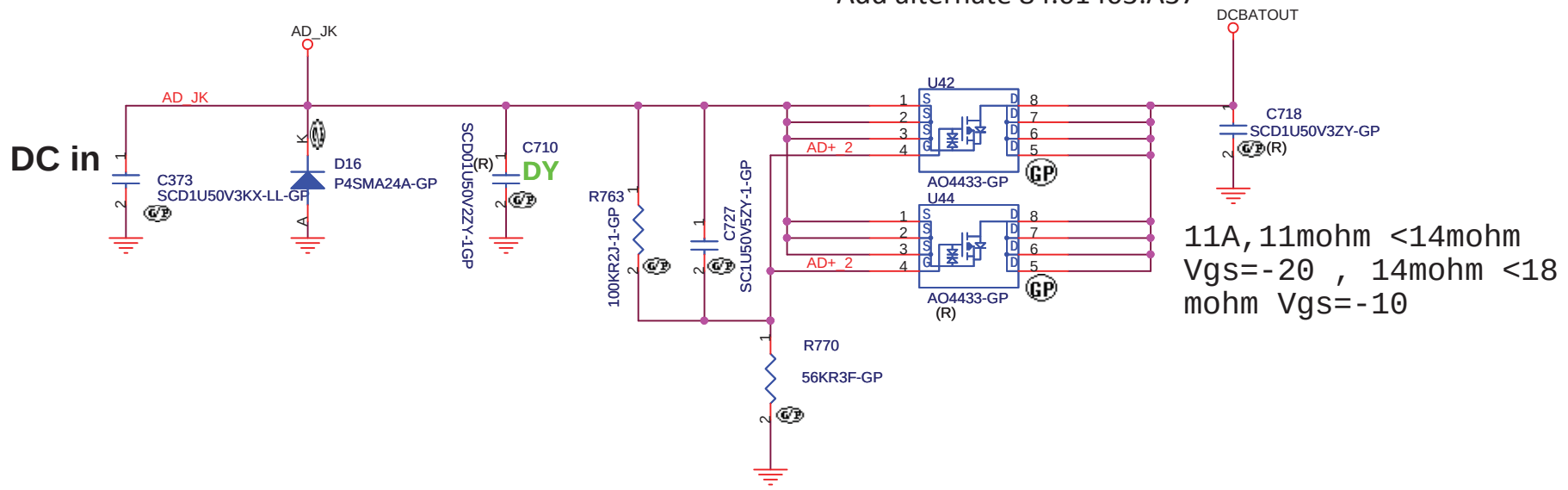
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**+12V**	
Size: Custom	Document Number: **Catalina**	Rev: **SA**
Date: Tuesday, April 06, 2010	Sheet 44 of 59	

Adaptor in to generate DCBATOUT

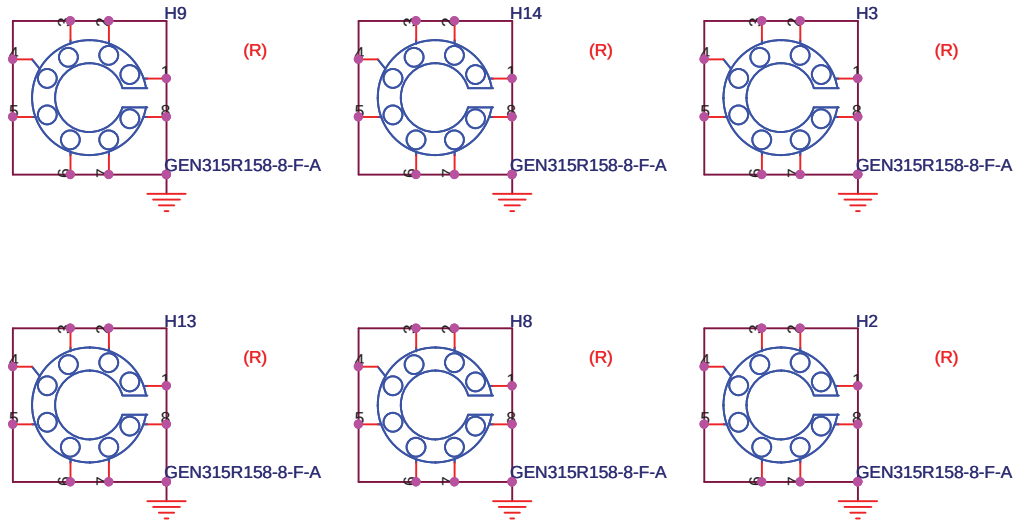
Add alternate 84.01403.A37

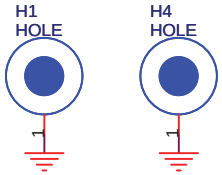


<Core Design>

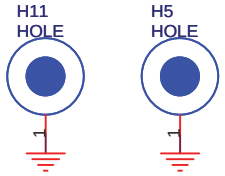
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC IN	
Size A4	Document Number: Catalina	Rev SA
Date: Tuesday, April 06, 2010	Sheet 45 of 59	

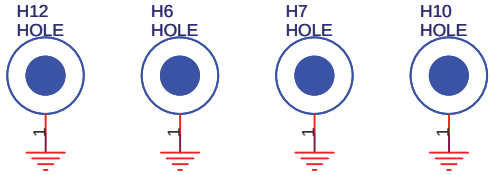




Mini PCIE holder



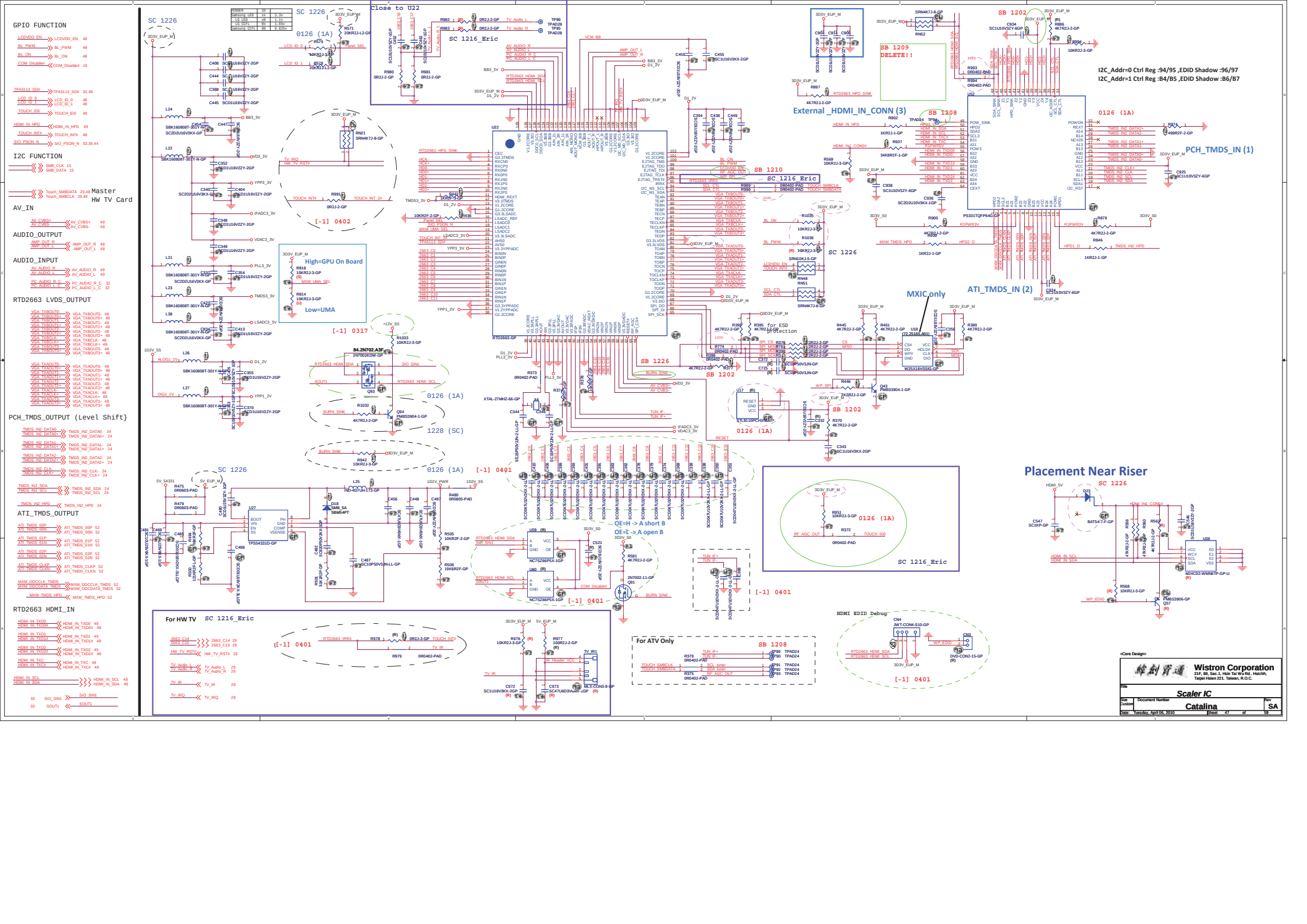
FAN holder



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Screw hole***		
Size: A4	Document Number: **Catalina**	Rev: **SA**
Date: Tuesday, April 06, 2010	Sheet 46 of 59	


GPIO FUNCTION
I2C FUNCTION
Master
HW TV Card
AV_IN
AUDIO_OUTPUT
AUDIO_INPUT
RTD2663 LVDS_OUTPUT
PCH_TMDS_OUTPUT (Level Shift)
ATI_TMDS_OUTPUT
RTD2663 HDMI_IN
SC 1226
SC 1216_Eric
Close to U22
0126 (1A)
[-1] 0402
[-1] 0317
[-1] 0401
1228 (SC)
High=GPU On Board
Low=UMA
SB 1202
SB 1209
DELETE!!
SB 1208
SB 1210
SB 1226
External _HDMI_IN_CONN (3)
PCH_TMDS_IN (1)
ATI_TMDS_IN (2)
MXIC only
Placement Near Riser
I2C_Addr=0 Ctrl Reg :94/95 ,EDID Shadow :96/97
I2C_Addr=1 Ctrl Reg :B4/B5 ,EDID Shadow :B6/B7
For HW TV
For ATV Only
HDMI EDID Debug
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Scaler IC
Catalina
Tuesday, April 06, 2010
47
59

Touch Key

TOUCH_INT#
L: Touch any key
H: Normal

BT_RESET_IN# (Mechical Key)
L: RESET_BT
H: Normal

BT_RESET_OUT
L: BT_RESET_IN#
H: BT_RESET

BL_CTL_OFF
Power ON: High (Default]
Touch: Low/High/Low...

LIGH_BAR_ON
LIGH Bar Off : High (Default]
Touch: Low/High/Low...

0126 (1A)

H: Enable
L: Disable

High: Enable
Low: Disable

[-1] 0401

Low: Enable
High: Disable

High: Enable
Low: Disable

Odd: channel A
Even: channel B

+19V_S5_INV Power

INVERTER BOARD CONNECTOR

Internal Speaker x 2

[-1] 0319

SB 1204
SB 1208

LPF for fc(-3dB)=500Hz

SB 1202

SB 1210

SC 1226

SHUTDOWN	TPA3111D2
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE

GAIN1	GAIN0	GAIN (dB)
0	0	20
1	0	26
~~0~~	~~1~~	~~32~~
~~1~~	~~1~~	~~36~~

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cy to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the sup connected to PVCC. This "virtual" rail is 4 times the voltage at the PLIMIT pin. This output voltage can be usec calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\frac{R_L}{R_L + 2 \times R_S} \times V_P\right)^2}{2 \times R_L}$$ for unclipped power

Where:
R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.
R_L is the load resistance.
V_P is the peak amplitude of the output possible within the supply rail.
$V_P = 4 \times$ PLIMIT voltage if PLIMIT < $4 \times V_P$
P_{OUT} (10%THD) = $1.25 \times P_{OUT}$ (unclipped)

Table 2. PLIMIT Typical Operation

TEST CONDITIONS ()	PLIMIT VOLTAGE	OUTPUT POWER (W)	OUTPUT VOLTAGE AMPLITUDE (V_{P-P})
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=26dB	1.62	5	14
PVCC=24V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.86	5	14.8
PVCC=12V, Vin=1Vrms, RL=8Ω, Gain=20dB	1.76	5	15

HCB2012KF-600T30-GP
Z=60 ohm,Rdc=0.04 ohm
I=3A ,0805

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PANEL OUTPUT & AMP

Size: Custom | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 48 of 59

REAR USB

18 USBPN2
18 USBPP2
18 USBPN3
18 USBPP3
18 USBPN4
18 USBPP4
18 USBPN9
18 USBPP9

LAN

27 RJ45_LED0 → RJ45_LED0
27 RJ45_LED1 → RJ45_LED1
27 RJ45_LED2 → RJ45_LED2

27 LAN_MDI0_DN → LAN_MDI0_DN
27 LAN_MDI0_DP → LAN_MDI0_DP
27 LAN_MDI1_DN → LAN_MDI1_DN
27 LAN_MDI1_DP → LAN_MDI1_DP
27 LAN_MDI2_DN → LAN_MDI2_DN
27 LAN_MDI2_DP → LAN_MDI2_DP
27 LAN_MDI3_DN → LAN_MDI3_DN
27 LAN_MDI3_DP → LAN_MDI3_DP

HDMI OUT

HDMI_OUT_TXD2 → HDMI_OUT_TXD2 24
HDMI_OUT_TXD2# → HDMI_OUT_TXD2# 24
HDMI_OUT_TXD1 → HDMI_OUT_TXD1 24
HDMI_OUT_TXD1# → HDMI_OUT_TXD1# 24
HDMI_OUT_TXD0 → HDMI_OUT_TXD0 24
HDMI_OUT_TXD0# → HDMI_OUT_TXD0# 24
HDMI_OUT_TXC → HDMI_OUT_TXC 24
HDMI_OUT_TXC# → HDMI_OUT_TXC# 24
HDMI_OUT_SCL → HDMI_OUT_SCL 24
HDMI_OUT_SDA → HDMI_OUT_SDA 24
HDMI_OUT_HPD → HDMI_OUT_HPD 24

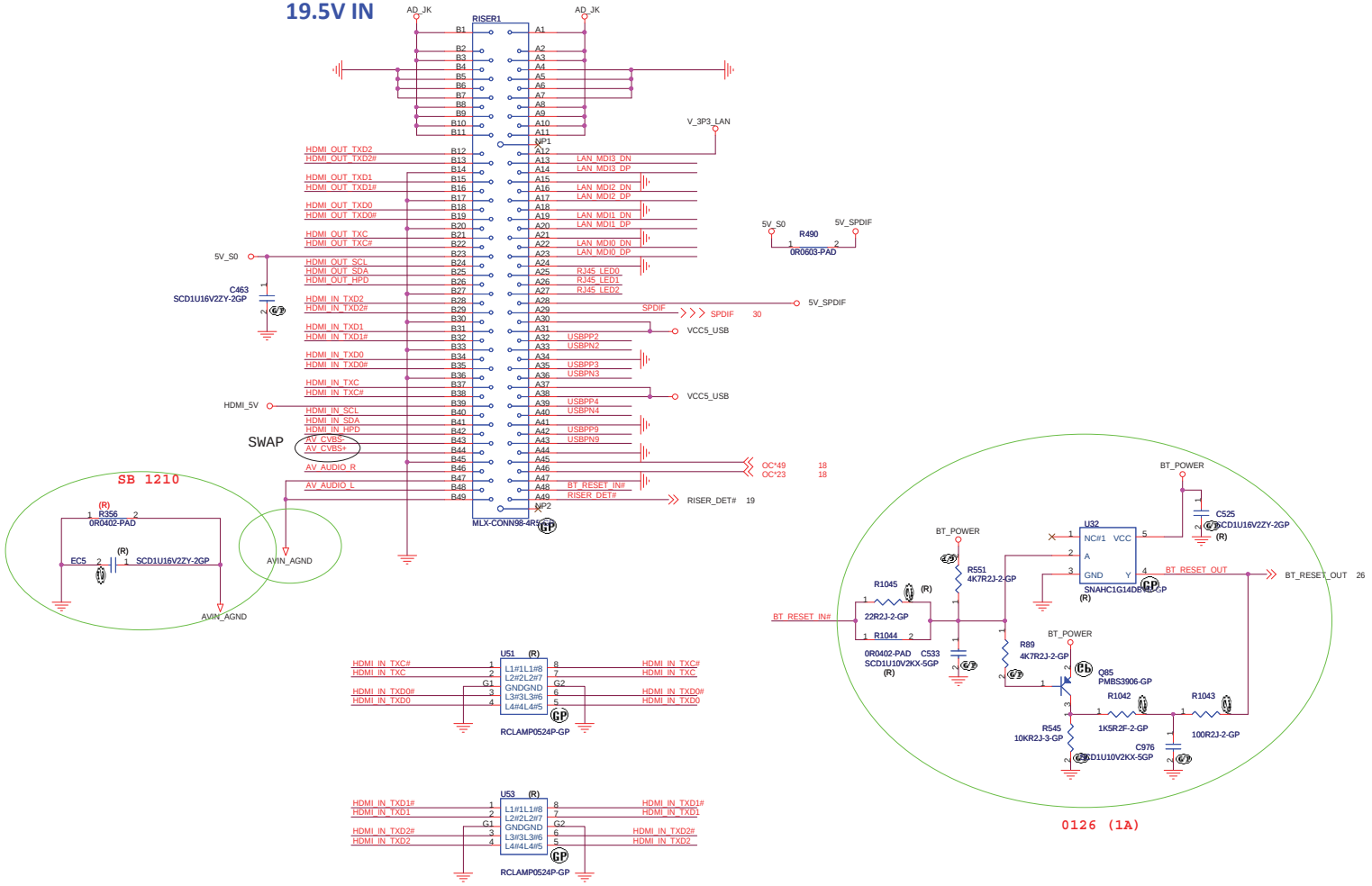
HDMI IN

HDMI_IN_TXD2 → HDMI_IN_TXD2 47
HDMI_IN_TXD2# → HDMI_IN_TXD2# 47
HDMI_IN_TXD1 → HDMI_IN_TXD1 47
HDMI_IN_TXD1# → HDMI_IN_TXD1# 47
HDMI_IN_TXD0 → HDMI_IN_TXD0 47
HDMI_IN_TXD0# → HDMI_IN_TXD0# 47
HDMI_IN_TXC → HDMI_IN_TXC 47
HDMI_IN_TXC# → HDMI_IN_TXC# 47
HDMI_IN_SCL → HDMI_IN_SCL 47
HDMI_IN_SDA → HDMI_IN_SDA 47
HDMI_IN_HPD → HDMI_IN_HPD 47

AV IN

47 AV_CVBS+ → AV_CVBS+
47 AV_CVBS- → AV_CVBS-
47 AV_AUDIO_R → AV_AUDIO_R
47 AV_AUDIO_L → AV_AUDIO_L

19.5V IN



0126 (1A)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Riser slot

Size	Document Number	Rev
C	Catalina	SA

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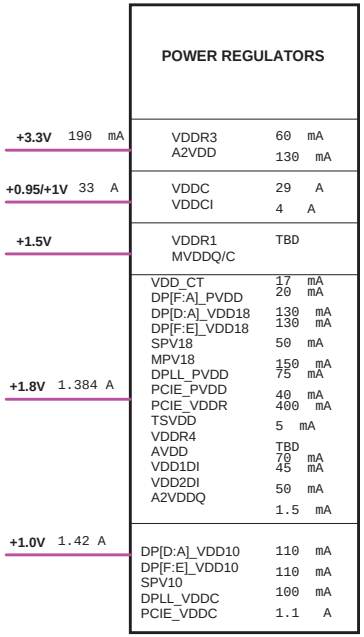

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_Power rail

Size	Document Number	Rev
C	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 50 of 59

PCI_E x16

4 PEG_TXP[15..0]
PEG_TXP0 PEG_TXP1 PEG_TXP2 PEG_TXP3 PEG_TXP4 PEG_TXP5 PEG_TXP6 PEG_TXP7 PEG_TXP8 PEG_TXP9 PEG_TXP10 PEG_TXP11 PEG_TXP12 PEG_TXP13 PEG_TXP14 PEG_TXP15

4 PEG_TXN[15..0]
PEG_TXN0 PEG_TXN1 PEG_TXN2 PEG_TXN3 PEG_TXN4 PEG_TXN5 PEG_TXN6 PEG_TXN7 PEG_TXN8 PEG_TXN9 PEG_TXN10 PEG_TXN11 PEG_TXN12 PEG_TXN13 PEG_TXN14 PEG_TXN15

4 PEG_RXP[15..0]
PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 PEG_RXP8 PEG_RXP9 PEG_RXP10 PEG_RXP11 PEG_RXP12 PEG_RXP13 PEG_RXP14 PEG_RXP15

4 PEG_RXN[15..0]
PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 PEG_RXN8 PEG_RXN9 PEG_RXN10 PEG_RXN11 PEG_RXN12 PEG_RXN13 PEG_RXN14 PEG_RXN15

15 CLK_PCIE_PEG#
15 CLK_PCIE_PEG
CLK_PCIE_PEG#
CLK_PCIE_PEG

52 ATI_RST#
ATI_RST#

U21A 1 OF 8

PCI EXPRESS INTERFACE

PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_T_TXP0	DIS	C699	SCD1U10V2KX-4GP	PEG_RXP0
PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_T_TXN0	DIS	C700	SCD1U10V2KX-4GP	PEG_RXN0
PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_T_TXP1	DIS	C673	SCD1U10V2KX-4GP	PEG_RXP1
PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_T_TXN1	DIS	C674	SCD1U10V2KX-4GP	PEG_RXN1
PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_T_TXP2	DIS	C687	SCD1U10V2KX-4GP	PEG_RXP2
PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_T_TXN2	DIS	C688	SCD1U10V2KX-4GP	PEG_RXN2
PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_T_TXP3	DIS	C675	SCD1U10V2KX-4GP	PEG_RXP3
PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_T_TXN3	DIS	C676	SCD1U10V2KX-4GP	PEG_RXN3
PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_T_TXP4	DIS	C689	SCD1U10V2KX-4GP	PEG_RXP4
PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_T_TXN4	DIS	C690	SCD1U10V2KX-4GP	PEG_RXN4
PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_T_TXP5	DIS	C677	SCD1U10V2KX-4GP	PEG_RXP5
PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_T_TXN5	DIS	C678	SCD1U10V2KX-4GP	PEG_RXN5
PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_T_TXP6	DIS	C691	SCD1U10V2KX-4GP	PEG_RXP6
PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_T_TXN6	DIS	C694	SCD1U10V2KX-4GP	PEG_RXN6
PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_T_TXP7	DIS	C679	SCD1U10V2KX-4GP	PEG_RXP7
PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_T_TXN7	DIS	C680	SCD1U10V2KX-4GP	PEG_RXN7
PEG_TXP8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_T_TXP8	DIS	C695	SCD1U10V2KX-4GP	PEG_RXP8
PEG_TXN8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_T_TXN8	DIS	C692	SCD1U10V2KX-4GP	PEG_RXN8
PEG_TXP9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_T_TXP9	DIS	C681	SCD1U10V2KX-4GP	PEG_RXP9
PEG_TXN9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_T_TXN9	DIS	C682	SCD1U10V2KX-4GP	PEG_RXN9
PEG_TXP10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_T_TXP10	DIS	C693	SCD1U10V2KX-4GP	PEG_RXP10
PEG_TXN10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_T_TXN10	DIS	C696	SCD1U10V2KX-4GP	PEG_RXN10
PEG_TXP11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_T_TXP11	DIS	C683	SCD1U10V2KX-4GP	PEG_RXP11
PEG_TXN11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_T_TXN11	DIS	C684	SCD1U10V2KX-4GP	PEG_RXN11
PEG_TXP12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_T_TXP12	DIS	C697	SCD1U10V2KX-4GP	PEG_RXP12
PEG_TXN12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_T_TXN12	DIS	C698	SCD1U10V2KX-4GP	PEG_RXN12
PEG_TXP13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_T_TXP13	DIS	C669	SCD1U10V2KX-4GP	PEG_RXP13
PEG_TXN13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_T_TXN13	DIS	C670	SCD1U10V2KX-4GP	PEG_RXN13
PEG_TXP14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_T_TXP14	DIS	C685	SCD1U10V2KX-4GP	PEG_RXP14
PEG_TXN14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_T_TXN14	DIS	C686	SCD1U10V2KX-4GP	PEG_RXN14
PEG_TXP15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_T_TXP15	DIS	C672	SCD1U10V2KX-4GP	PEG_RXP15
PEG_TXN15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_T_TXN15	DIS	C671	SCD1U10V2KX-4GP	PEG_RXN15

CLOCK
CALIBRATION

SB 1202

15 CLK_PCIE_PEG → CLK_PCIE_PEG → AB35 PCIE_REFCLKP
15 CLK_PCIE_PEG# → CLK_PCIE_PEG# → AA36 PCIE_REFCLKN

R821 1 (S) PWRGOOD_ATI 2 10KR2J-3-GP
AJ21 NC#AJ21
AK21 NC#AK21
AH16 PWRGOOD

ATI_RST# 1 R353 2 0R0402-PAD PLT_RST1# M92 1 AA30 PERST#

C325 (R) SC47P50V2JN-3GP

PCIE_CALRP Y30 1 R790 (S) 1K27R2F-L-GP 1.0V_REG
PCIE_CALRN Y29 1 R792 (S) 2K2R2F-3-GP

MADISON-PRO-GP
(M71.MDSON.M03, P71.0PARK.M05)

33,52 PLT_RST_ATI# → PLT_RST_ATI# 1 R344 2 0R0402-PAD ATI_RST#

[-1] 0401

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ATI_Mad_PCIE
Size: C | Document Number: Catalina | Rev: SA
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HSYNC/VSYNC are transmitted on TX0P/M_DP[A, C]2P/N,
TX3P/M_DP[B, D]2P/N, TXOUT_L0P/N_DPE2P/N,
or TXOUT_U0P/N_DPF2P/N (Blue) channel during blank

Layout notice:
It should be place near HDMI connector

DVPDATA [3:0]
Hynix-H5TQ1G63BFR-12C (800MHz)
Samsung-K4W1G1646E-HC12 (800MHz)

09/09/28
Must be tied high if not used.

09/09/28
delete
do not need LVDS

SB 1202
09/09/28
A 3-K external pull-up (3.3 V) is required
if an external BIOS ROM chip is used.

SERIAL EEPROM 512K/1M
A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE
ROM OR STRAPPING

0126 (1A)

MxM HDMI OUT

NV_HDMI_CLK+ 24
NV_HDMI_CLK- 24
NV_HDMI_DATA0+ 24
NV_HDMI_DATA0- 24
NV_HDMI_DATA1+ 24
NV_HDMI_DATA1- 24
NV_HDMI_DATA2+ 24
NV_HDMI_DATA2- 24
NV_HDMI_CLK 24
NV_HDMI_DATA 24
NV_HDMI_DETECT 24

MxM VGA OUT

MXM_RED 23
MXM_GREEN 23
MXM_BLUE 23
MXM_DDCCLK 23
MXM_DDCDATA 23
MXM_HSYNC 23,58
MXM_VSYNC 23,58

GPIOS

58 GPIO6
58 GPIO1
58 GPIO2
58 GPU_SMBDAT
58 GPU_SMBCLK
58 GPIO5
58 GPIO8
58 GPIO9
58 GPIO11
58 GPIO12
58 GPIO13
58 GPIO22
58 GENERICC
42 AMD_GPIO15
42 AMD_GPIO20
15 PEX_CLKREQ

OTHERS

H2SYNC 58
V2SYNC 58

HDMI

NV_HDMI_CLK+ 24
NV_HDMI_CLK- 24
NV_HDMI_DATA0+ 24
NV_HDMI_DATA0- 24
NV_HDMI_DATA1+ 24
NV_HDMI_DATA1- 24
NV_HDMI_DATA2+ 24
NV_HDMI_DATA2- 24

TMDS to Scalar

ATI_TMDS_CLKP 47
ATI_TMDS_CLKN 47
ATI_TMDS_D0P 47
ATI_TMDS_D0N 47
ATI_TMDS_D1P 47
ATI_TMDS_D1N 47
ATI_TMDS_D2P 47
ATI_TMDS_D2N 47

VGA

MXM_DDCCLK 23
MXM_DDCDATA 23

TMDS to Scalar

MXM_DDCCLK_TMDS 47
MXM_DDCDATA_TMDS 47

HDMI

NV_HDMI_CLK 24
NV_HDMI_DATA 24

SB 1202

SB 1202

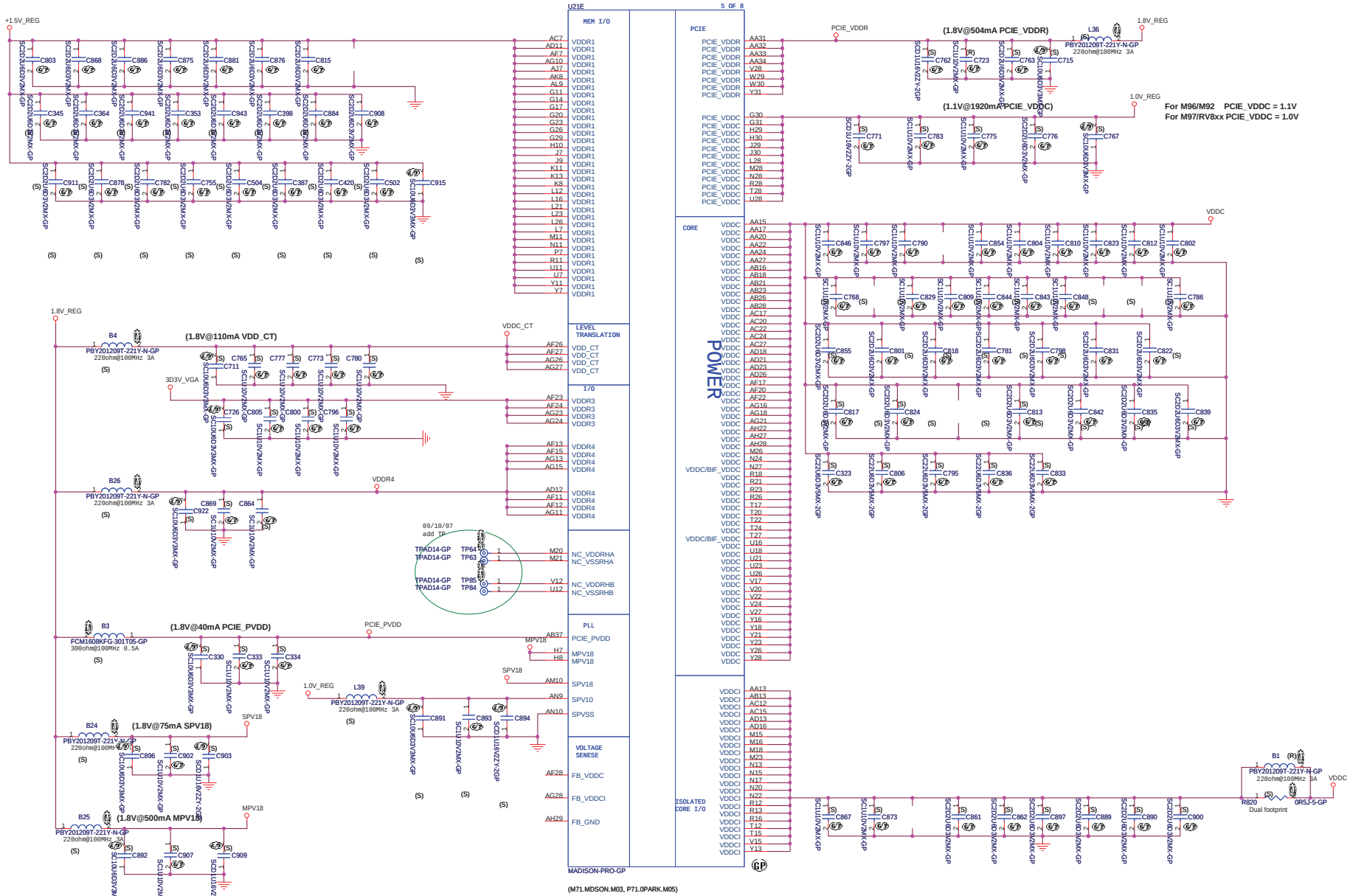
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI Mad IO

Size: D | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 52 of 59



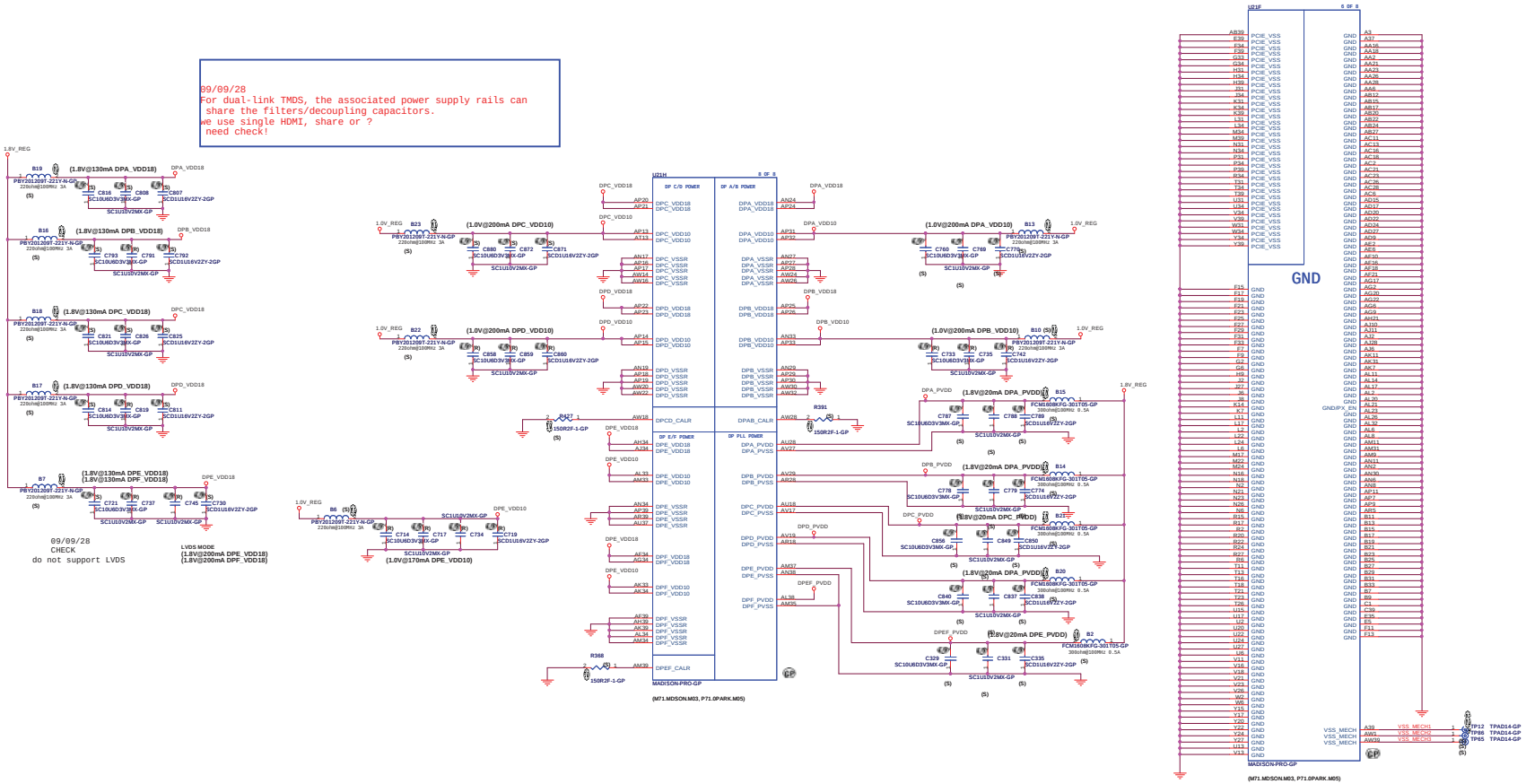
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_Mad_POWER

Size	Document Number	Rev
C	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 53 of 59

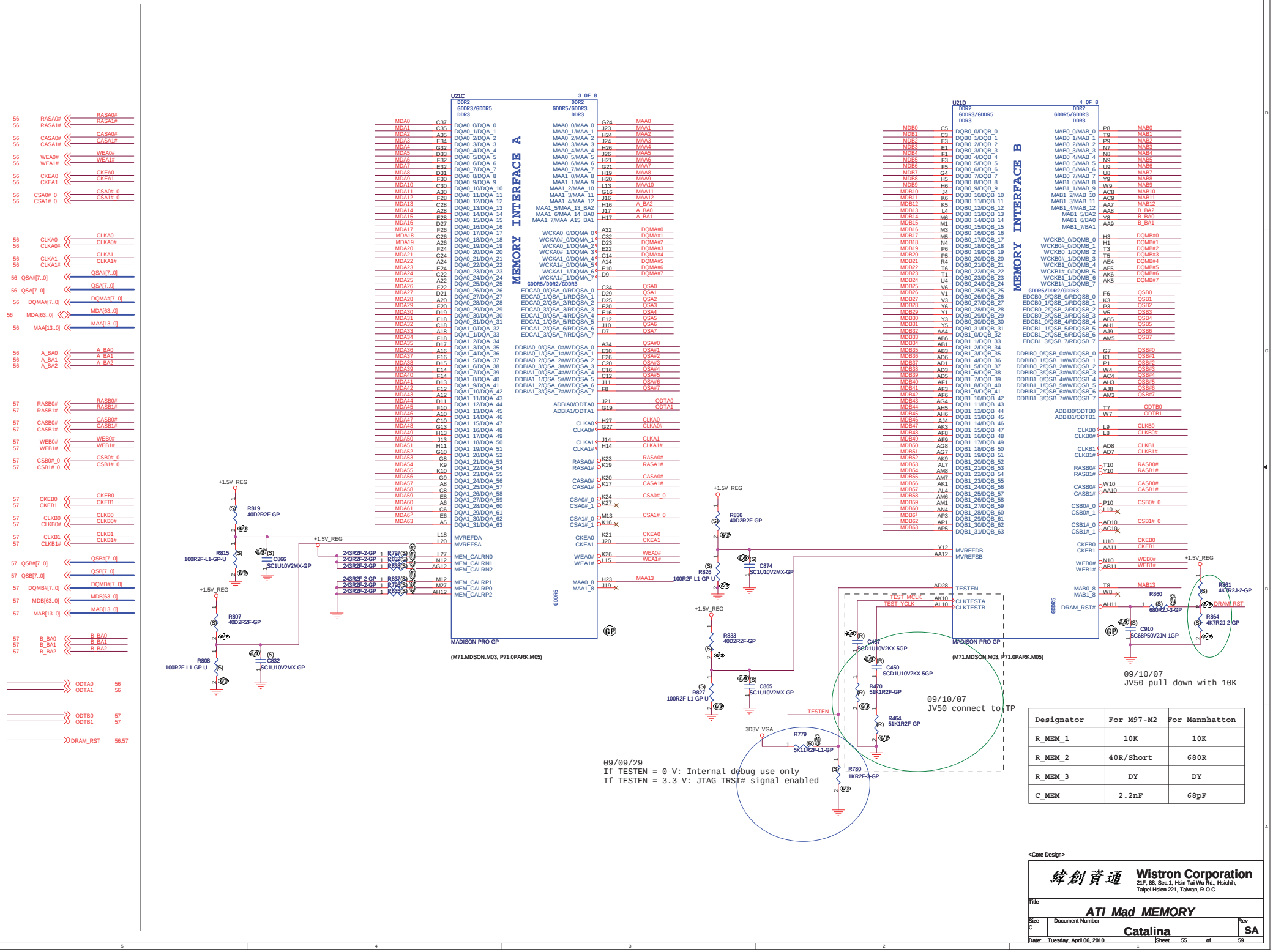


<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI DP POWER

Size	Document Number	Rev
D	Catalina	SA

Date: Tuesday, April 06, 2010 Sheet 54 of 59



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI_Mad_MEMORY**

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 55 of 59

CHANNEL A: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12

09/10/07
JV50 use 243

09/10/07
JV50 use 1K05 and D01U

Should be 240 Ohms +-1%

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_DDR3 64MX16 A

Size: C | Document Number: Catalina | Rev: SA

Date: Tuesday, April 06, 2010 | Sheet 56 of 59

CHANNEL B: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12

55 MDB[63..0]
MDB0 MDB1 MDB2 MDB3 MDB4 MDB5 MDB6 MDB7 MDB8 MDB9 MDB10 MDB11 MDB12 MDB13 MDB14 MDB15 MDB16 MDB17 MDB18 MDB19 MDB20 MDB21 MDB22 MDB23 MDB24 MDB25 MDB26 MDB27 MDB28 MDB29 MDB30 MDB31 MDB32 MDB33 MDB34 MDB35 MDB36 MDB37 MDB38 MDB39 MDB40 MDB41 MDB42 MDB43 MDB44 MDB45 MDB46 MDB47 MDB48 MDB49 MDB50 MDB51 MDB52 MDB53 MDB54 MDB55 MDB56 MDB57 MDB58 MDB59 MDB60 MDB61 MDB62 MDB63

55 MAB[13..0]
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13

55 DQMB#[7..0]
DQMB#0 DQMB#1 DQMB#2 DQMB#3 DQMB#4 DQMB#5 DQMB#6 DQMB#7

55 QSB[7..0]
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7

55 QSB#[7..0]
QSB#0 QSB#1 QSB#2 QSB#3 QSB#4 QSB#5 QSB#6 QSB#7

55 B_BA0 B_BA1 B_BA2
55 CLKB0 CLKB0# CKEB0
55 ODTB0 CSB0#_0 RASB0# CASB0# WEB0#
55 CLKB1 CLKB1# CKEB1
55 ODTB1 CSB1#_0 RASB1# CASB1# WEB1#

U28 / U55 / U54 / U29
VREFCA VREFDQ
DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7 DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15
B_BA0 B_BA1 B_BA2
CLKB0 CLKB0# CKEB0
ODTB0 CSB0#_0 RASB0# CASB0# WEB0#
QSB0 QSB1 DQSL DQSU
DQMB#3 DQMB#1 DML DMU
QSB#3 QSB#1 DQSL DQSU
55,56 DRAM_RST
VDD#B2 VDD#D9 VDD#G7 VDD#K2 VDD#K8 VDD#N1 VDD#N9 VDD#R1 VDD#R9
VDDQ#A1 VDDQ#A8 VDDQ#C1 VDDQ#C9 VDDQ#D2 VDDQ#E9 VDDQ#F1 VDDQ#H2 VDDQ#H9
VSS#A9 VSS#B3 VSS#E1 VSS#G8 VSS#J2 VSS#J8 VSS#M1 VSS#M9 VSS#P1 VSS#P9 VSS#T1 VSS#T9
VSSQ#B1 VSSQ#B9 VSSQ#D1 VSSQ#D8 VSSQ#E2 VSSQ#E8 VSSQ#F9 VSSQ#G1 VSSQ#G9
NC#J1 NC#L1 NC#J9 NC#L9
100-BALL SDRAM DDR3
H5TQ1G63BFR-12C-GP (S)

Should be 240 Ohms +-1%
R481 240R2F-1-GP
R912 240R2F-1-GP
R889 240R2F-1-GP
R520 240R2F-1-GP

09/10/07
JV50 use 1K05 and D01U

+1.5V_REG
R483 4K99R2F-L-GP
R482 4K99R2F-L-GP
VREFC_U24
C477 SCD1U10V2KX-5GP
R918 4K99R2F-L-GP
R916 4K99R2F-L-GP
VREFC_U25
C939 SCD1U10V2KX-5GP
R891 4K99R2F-L-GP
R890 4K99R2F-L-GP
VREFC_U26
C932 SCD1U10V2KX-5GP
R521 4K99R2F-L-GP
R522 4K99R2F-L-GP
VREFC_U27
C511 SCD1U10V2KX-5GP
R913 4K99R2F-L-GP
R908 4K99R2F-L-GP
VREFD_U24
C937 SCD1U10V2KX-5GP
R884 4K99R2F-L-GP
R885 4K99R2F-L-GP
VREFD_U25
C929 SCD1U10V2KX-5GP
R518 4K99R2F-L-GP
R523 4K99R2F-L-GP
VREFD_U26
C510 SCD1U10V2KX-5GP
R887 4K99R2F-L-GP
R888 4K99R2F-L-GP
VREFD_U27
C931 SCD1U10V2KX-5GP

CLKB0 CLKB1
R516 56R2J-4-GP
R515 56R2J-4-GP
R910 56R2J-4-GP
R914 56R2J-4-GP
C506 SCD01U50V2KX-1GP
C942 SCD01U50V2KX-1GP
C930 C476 C766 C494 C509
C945 C899 C514
C940 C491 C416 C475 C498
C944 C933 C473 C483 C948
C470 C471 C947 C499 C472
SCD1U10V2MX-GP
402

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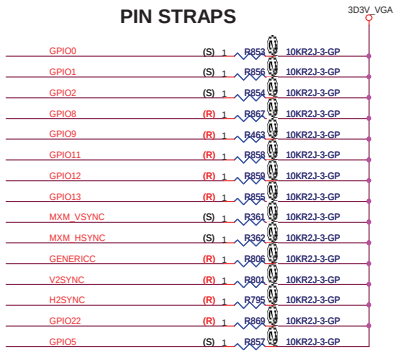
52 GPIO0
52 GPIO1
52 GPIO2
52 GPIO8
52 GPIO9
52 GPIO11
52 GPIO12
52 GPIO13
23,52 MXM_VSYNC
23,52 MXM_HSYNC
52 GENERICC
52 V2SYNC
52 H2SYNC
52 GPIO22
52 GPIO5

13,15,29 PCH_SMBCLK
13,15,29 PCH_SMBDATA

19,42,43 DGPU_PWROK

52 GPU_SMBCLK
52 GPU_SMBDAT

PIN STRAPS



	Manufacturer	Part Number	Size	CONFIG[2:0]
STRAP	ST Microelectronics	M25P05A	512 kbit	100

		HSYNC VSYNC
STRAP	Audio for both DisplayPort and HDMI.	11
	Audio for DisplayPort and HDMI if dongle is detected	10

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	1 0 0
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1

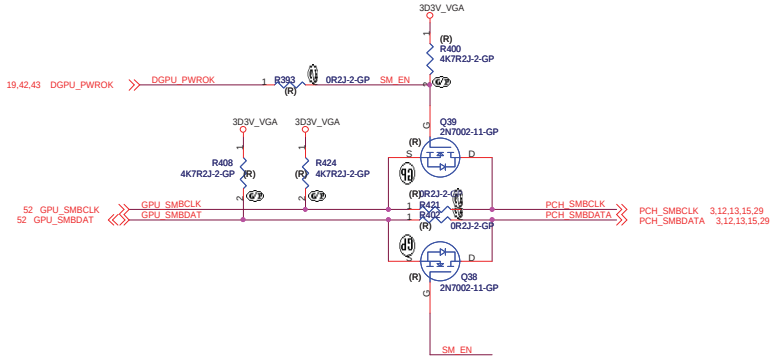
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN



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