Compal Confidential

C560 LA-A061P Schematics Document

INTEL Haswell CPU with DDRIII + PCH Lynx-Point

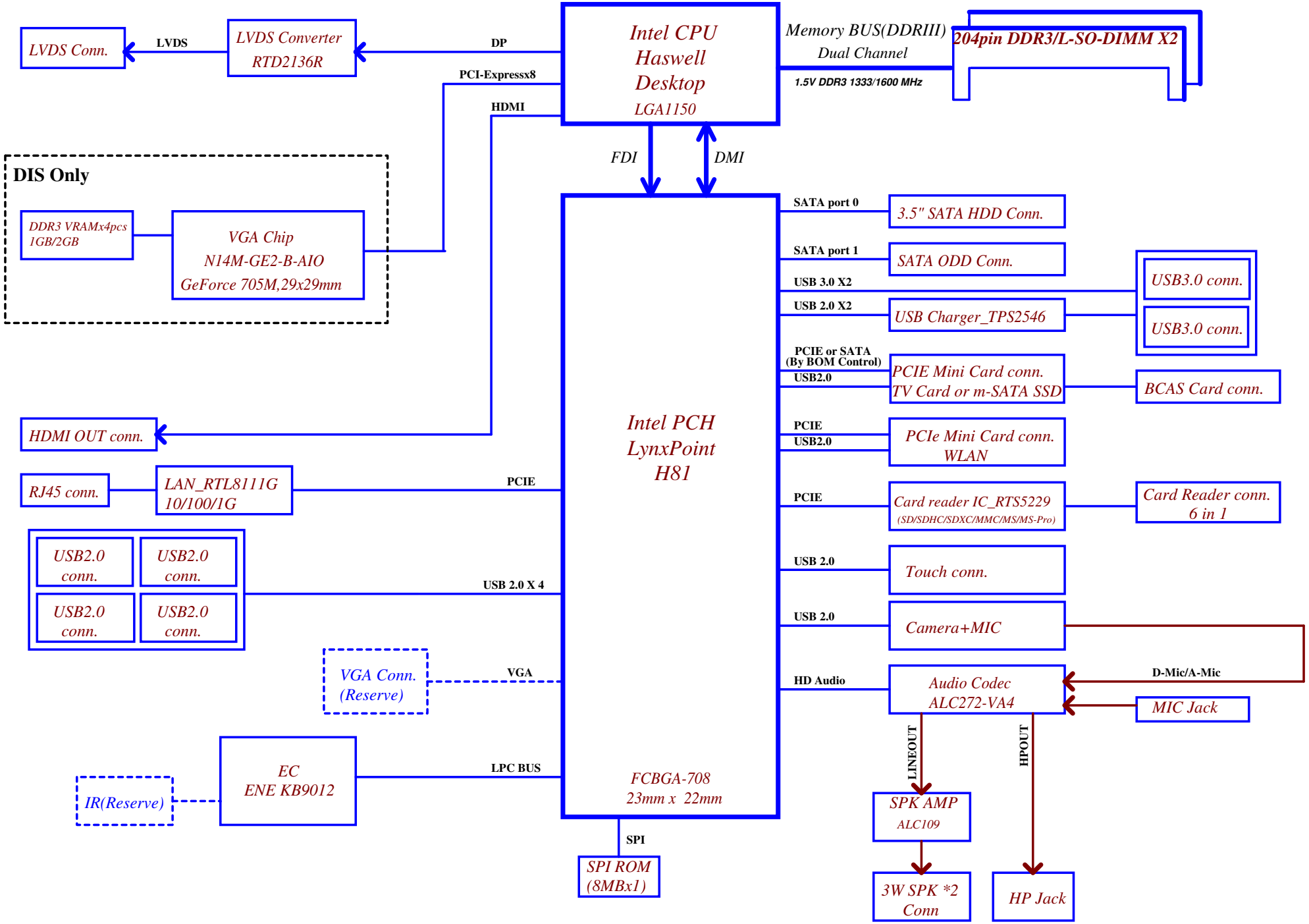
AIO M/B

September 24, 2013

REV:1.0

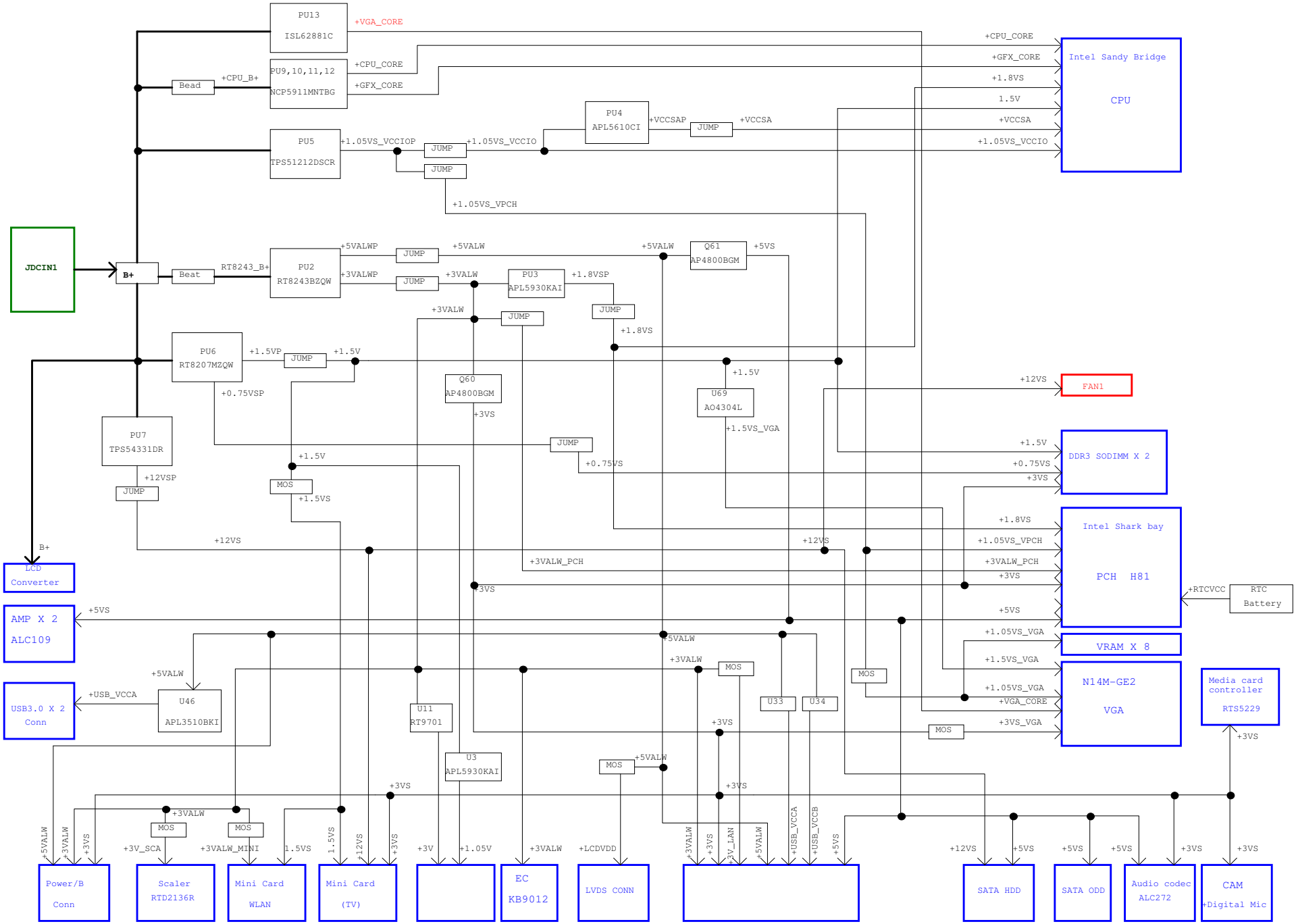
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title: *Cover Page*			
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 1 of 59		



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.	
Title	Block Diagram
Size: Custom	Document Number: ZEA00 LA-A061P M/B
Rev: 0.3	
Date: Tuesday, September 24, 2013	Sheet 2 of 59



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **Power Tree**

Size	Document Number	Rev
	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 | Sheet 3 of 59

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW *1	+VS *2	+1.5V	+0.75VS	+RTCVCC
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	OFF	ON	OFF	ON
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF	ON
S5(Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF	ON

Note:

*1:+VALW power reail include +3VALW,+5VALW,B+,+VSB,+3VALW_PCH

*2:+VS power reail include +3VS,+5VS,+12VS,+1.05VS_VPCH,+1.5VS_VGA,+VGA_CORE,+CPU_CORE

USB Port Table

USB 2.0	USB 1.1	Port	Device
RMH1	UHCI0	0	Co-lay w/USB30 PORT0
		1	Co-lay w/USB30 PORT1(Debug)
	EHCI1	2	Rear IO USB20 Conn
		3	Rear IO USB20 Conn
	UHCI2	4	WLAN
		5	Touch
	UHCI3	6	Disabled on H81
		7	Disabled on H81
RMH2	UHCI4	8	Rear IO USB20 Conn
		9	Rear IO USB20 Conn(Debug)
	UHCI5	10	TV
		11	Camera
	UHCI6	12	Disabled on H81
		13	Disabled on H81

BOM Structure Table

BTO Item	BOM Structure
ME components	CONN@
UMA Only	UMA@
DISCRETE Only	DIS@
EMI Pop components	EMI@
ESD Pop components	ESD@
EMI Unpop components	@EMI@
ESD Unpop components	@ESD@
HDMI OUT	HDMIO@
TV	TV@
SSD	SSD@
CRT	CRT@(EVTonly)
Unpop	@
VRAM select	X76@
EVT for Reserve components	EVT@
PCB	PCB@
SKU IO Select	GPIO68_H@
	GPIO68_L@
	GPIO69_H@
	GPIO69_L@
	GPIO70_H@
	GPIO70_L@
Touch	TOUCH@
Non Charger	NCHG@
Charger	CHG@

SATA Port Table

Port		Device
6G	0	HDD
	1	m-SATA
3G	2	Disabled on H81
	3	Disabled on H81
	4	ODD
	5	NC

PCIE Port Table

Port	Device
1	LAN
2	Card Reader
3	WLAN
4	TV
5	NC
6	NC
7	Disabled on H81
8	Disabled on H81

BOARD ID Table

Board ID	PCB Revision
0	0.1
3	0.2
4	0.3
5	

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR(JDDRL2)		1010 000X b
+3VS	DDR(JDDRH1)		1010 010X b

EC SM Bus1 Address

Power	Device	HEX	Address
	ALC106	48H	0100_100xb

PCH SML1 Bus Address

Power	Device	HEX	Address
	VGA Ext. thermal sensor		
	VGA Int. thermal sensor (default)		0x9b

Board ID	Rb	V_{SB} min	V_{SB} typ	V_{SB} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00 - 0x0C
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31 - 0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A - 0x59
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A - 0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F - 0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC - 0xFF

SKU ID(Project) Table

Project_ID2 (GPIO68)	Project_ID1 (GPIO69)	Project_ID0 (GPIO70)	SKU	
0	0	0	UMA 4519QH38L04	TV@ NLDO@ EMI@ 8111G@ ESD@ CHG@ GPIO68_L@ GPIO69_L@ GPIO70_L@ PCB@
0	0	1	UMA_W/HDMI 4519QH38L05	HDMIO@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_L@ GPIO69_L@ TOUCH@ GPIO70_H@ PCB@
0	1	0	DIS-MIC1G 4519QH38L06	DIS@ NLDO@ EMI@ 8111G@ ESD@ TOUCH@ GPIO68_L@ GPIO69_H@ GPIO70_L@ PCB@
0	1	1	DIS-SAM1G_W/HDMI 4519QH38L07	DIS@ HDMIO@ TV@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_L@ GPIO69_H@ GPIO70_H@ PCB@
1	0	0	DIS-MIC2G_W/HDMI 4519QH38L08	DIS@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_H@ GPIO69_L@ TOUCH@ GPIO70_L@ PCB@
1	0	1	DIS-MIC2G_W/HDMI 4519QH38L09	DIS@ HDMIO@ TV@ NLDO@ EMI@ 8111G@ ESD@ NCHG@ GPIO68_H@ GPIO69_L@ TOUCH@ GPIO70_L@ PCB@
1	1	0		
1	1	1		

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 4 of 59

ESD request Close to CPU as possible

PECI 10mil spacing and Max Length < 15"

R11 follow CDB R42PR add 0ohm serial resistor

R12 follow CDB R34PR add 0ohm serial resistor

Trace width=12mil, spacing 20mil, max L=500mil

v1.0 update

100 MHz

Place C6 close to CPU pin J40 as close as possible. No stub

For BDW new CPU

v0.2 update

FOX_3H993827-4M41-01H_HASWELL

HDMI OUT (To Conn.)

DP_RCOMP trace width=20mil spacing 25mil length<200mil

FDI For VGA

eDP brightness

eDP (To LVDS Converter)

ESD request Close to JCPU1 G40

PU/PD for JTAG signals

v0.2 update

ESD request Close to JCPU1

Table 8-1. Configuration-wise Mapping of HDMI signals for Processor on DDI ports

Port	Digital Display Interface Differential Pairs	HDMI Signals	Processor Digital Display Interface Pins
Port B	DDIB_TXBP0	HDMIB_TX2_DP	DDIB_TXB[0]
	DDIB_TXBN0	HDMIB_TX2_DN	DDIB_TXB#[0]
	DDIB_TXBP1	HDMIB_TX1_DP	DDIB_TXB[1]
	DDIB_TXBN1	HDMIB_TX1_DN	DDIB_TXB#[1]
	DDIB_TXBP2	HDMIB_TX0_DP	DDIB_TXB[2]
	DDIB_TXBN2	HDMIB_TX0_DN	DDIB_TXB#[2]
	DDIB_TXBP3	HDMIB_CLK_DP	DDIB_TXB[3]
	DDIB_TXBN3	HDMIB_CLK_DN	DDIB_TXB#[3]
	DDPB_HPD	DDSP_1_HPD0	Hot plug detect used by HDMI Port B
	DDPB_CTRLCLK	DDPB_CTRL_CLK	HDMI DDC lines for Port B
	DDPB_CTRLDATA	DDPB_CTRL_CLK	
Port C	DDIC_TXBP0	HDMIC_TX2_DP	DDIC_TXB[0]
	DDIC_TXBN0	HDMIC_TX2_DN	DDIC_TXB#[0]
	DDIC_TXBP1	HDMIC_TX1_DP	DDIC_TXB[1]
	DDIC_TXBN1	HDMIC_TX1_DN	DDIC_TXB#[1]
	DDIC_TXBP2	HDMIC_TX0_DP	DDIC_TXB[2]
	DDIC_TXBN2	HDMIC_TX0_DN	DDIC_TXB#[2]
	DDIC_TXBP3	HDMIC_CLK_DP	DDIC_TXB[3]
	DDIC_TXBN3	HDMIC_CLK_DN	DDIC_TXB#[3]
	DDIPC_HPD	DDSP_2_HPD1	Hot plug detect used by HDMI Port C
	DDIPC_CTRLCLK	DDIPC_CTRL_CLK	HDMI DDC lines for Port C
	DDIPC_CTRLDATA	DDIPC_CTRL_CLK	
Port D	DDID_TXBP0	HDMID_TX2_DP	DDID_TXB[0]
	DDID_TXBN0	HDMID_TX2_DN	DDID_TXB#[0]
	DDID_TXBP1	HDMID_TX1_DP	DDID_TXB[1]
	DDID_TXBN1	HDMID_TX1_DN	DDID_TXB#[1]
	DDID_TXBP2	HDMID_TX0_DP	DDID_TXB[2]
	DDID_TXBN2	HDMID_TX0_DN	DDID_TXB#[2]
	DDID_TXBP3	HDMID_CLK_DP	DDID_TXB[3]
	DDID_TXBN3	HDMID_CLK_DN	DDID_TXB#[3]
	DDIPD_HPD	DDSP_3_HPD2	Hot plug detect used by HDMI Port D
	DDIPD_CTRLCLK	DDIPD_CTRL_CLK	HDMI DDC lines for Port D
	DDIPD_CTRLDATA	DDIPD_CTRL_CLK	

PDG P132

HSW A0+LPT A0 change R21 to 4.7K, R19 to 3.3K

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	Haswell_JTAG/XDP/DDI		
Size	Document Number		Rev
Custom	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	5 of 59

PCIE_GTX_C_CRX_N[0..15] → PCIE_GTX_C_CRX_N[0..15] [21]

PCIE_GTX_C_CRX_P[0..15] → PCIE_GTX_C_CRX_P[0..15] [21]

PCIE_CTX_C_GRX_N[0..15] → PCIE_CTX_C_GRX_N[0..15] [21]

PCIE_CTX_C_GRX_P[0..15] → PCIE_CTX_C_GRX_P[0..15] [21]

+VCCIOA

R22 24.9_0402_1%

PEG_RCOMP trace width=12mil
spacing 15mil length<400mil

JCPU1A

[14]	DMI_PTX_CRX_N0	DMI_PTX_CRX_N0	T3	DMI_RXN0	DMI	PEG	P3 PEG_RCOMP
[14]	DMI_PTX_CRX_N1	DMI_PTX_CRX_N1	V1	DMI_RXN1			F15 PCIE_GTX_C_CRX_N15
[14]	DMI_PTX_CRX_N2	DMI_PTX_CRX_N2	V2	DMI_RXN2			E14 PCIE_GTX_C_CRX_N14
[14]	DMI_PTX_CRX_N3	DMI_PTX_CRX_N3	W3	DMI_RXN3			F13 PCIE_GTX_C_CRX_N13
							E12 PCIE_GTX_C_CRX_N12
[14]	DMI_PTX_CRX_P0	DMI_PTX_CRX_P0	U3	DMI_RXP0			F11 PCIE_GTX_C_CRX_N11
[14]	DMI_PTX_CRX_P1	DMI_PTX_CRX_P1	U1	DMI_RXP1			G10 PCIE_GTX_C_CRX_N10
[14]	DMI_PTX_CRX_P2	DMI_PTX_CRX_P2	W2	DMI_RXP2			F9 PCIE_GTX_C_CRX_N9
[14]	DMI_PTX_CRX_P3	DMI_PTX_CRX_P3	Y3	DMI_RXP3			G8 PCIE_GTX_C_CRX_N8
							D4 PCIE_GTX_C_CRX_N7
[14]	DMI_CTX_PRX_N0	DMI_CTX_PRX_N0	AA5	DMI_TXN0			E5 PCIE_GTX_C_CRX_N6
[14]	DMI_CTX_PRX_N1	DMI_CTX_PRX_N1	AB4	DMI_TXN1			F6 PCIE_GTX_C_CRX_N5
[14]	DMI_CTX_PRX_N2	DMI_CTX_PRX_N2	AC4	DMI_TXN2			G5 PCIE_GTX_C_CRX_N4
[14]	DMI_CTX_PRX_N3	DMI_CTX_PRX_N3	AC2	DMI_TXN3			H6 PCIE_GTX_C_CRX_N3
							J5 PCIE_GTX_C_CRX_N2
[14]	DMI_CTX_PRX_P0	DMI_CTX_PRX_P0	AA4	DMI_TXP0			K6 PCIE_GTX_C_CRX_N1
[14]	DMI_CTX_PRX_P1	DMI_CTX_PRX_P1	AB3	DMI_TXP1			L5 PCIE_GTX_C_CRX_N0
[14]	DMI_CTX_PRX_P2	DMI_CTX_PRX_P2	AC5	DMI_TXP2			E15 PCIE_GTX_C_CRX_P15
[14]	DMI_CTX_PRX_P3	DMI_CTX_PRX_P3	AC1	DMI_TXP3			D14 PCIE_GTX_C_CRX_P14
							E13 PCIE_GTX_C_CRX_P13
[14]	FDI_CSYNC	FDI_CSYNC	D16	FDI_CSYNC	FDI		D12 PCIE_GTX_C_CRX_P12
[14]	FDI_INT	FDI_INT	D18	DISP_INT			E11 PCIE_GTX_C_CRX_P11
							F10 PCIE_GTX_C_CRX_P10
							E9 PCIE_GTX_C_CRX_P9
							F8 PCIE_GTX_C_CRX_P8
							D3 PCIE_GTX_C_CRX_P7
							E4 PCIE_GTX_C_CRX_P6
							F5 PCIE_GTX_C_CRX_P5
							G4 PCIE_GTX_C_CRX_P4
							H5 PCIE_GTX_C_CRX_P3
							J4 PCIE_GTX_C_CRX_P2
							K5 PCIE_GTX_C_CRX_P1
							L4 PCIE_GTX_C_CRX_P0
							B12 PCIE_CTX_C_GRX_N15
							C11 PCIE_CTX_C_GRX_N14
							D10 PCIE_CTX_C_GRX_N13
							C9 PCIE_CTX_C_GRX_N12
							D8 PCIE_CTX_C_GRX_N11
							C7 PCIE_CTX_C_GRX_N10
							B6 PCIE_CTX_C_GRX_N9
							C5 PCIE_CTX_C_GRX_N8
							E2 PCIE_CTX_C_GRX_N7
							F3 PCIE_CTX_C_GRX_N6
							G2 PCIE_CTX_C_GRX_N5
							H3 PCIE_CTX_C_GRX_N4
							J2 PCIE_CTX_C_GRX_N3
							K3 PCIE_CTX_C_GRX_N2
							M3 PCIE_CTX_C_GRX_N1
							L2 PCIE_CTX_C_GRX_N0
							A12 PCIE_CTX_C_GRX_P15
							B11 PCIE_CTX_C_GRX_P14
							C10 PCIE_CTX_C_GRX_P13
							B9 PCIE_CTX_C_GRX_P12
							C8 PCIE_CTX_C_GRX_P11
							B7 PCIE_CTX_C_GRX_P10
							A6 PCIE_CTX_C_GRX_P9
							B5 PCIE_CTX_C_GRX_P8
							E1 PCIE_CTX_C_GRX_P7
							F2 PCIE_CTX_C_GRX_P6
							G1 PCIE_CTX_C_GRX_P5
							H2 PCIE_CTX_C_GRX_P4
							J1 PCIE_CTX_C_GRX_P3
							K2 PCIE_CTX_C_GRX_P2
							M2 PCIE_CTX_C_GRX_P1
							L1 PCIE_CTX_C_GRX_P0

FOX_3H993827-4M41-01H_HASWELL

Reserve for x16 GPU

Reserve for x16 GPU

C2080	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N15
C2081	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N14
C2082	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N13
C2083	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N12
C2084	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N11
C2085	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N10
C2086	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N9
C2087	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N8
C12	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N7
C13	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N6
C14	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N5
C15	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N4
C16	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N3
C17	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N2
C18	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N1
C19	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_N0
C2088	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P15
C2089	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P14
C2090	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P13
C2091	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P12
C2092	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P11
C2093	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P10
C2094	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P9
C2095	1	2	@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P8
C20	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P7
C21	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P6
C22	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P5
C23	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P4
C24	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P3
C25	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P2
C26	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P1
C27	1	2	DIS@	0.22U_0402_16V7K	PCIE_CTX_C_GRX_P0

Reserve for x16 GPU

Reserve for x16 GPU

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: *Haswell_DMI/PEG/FDI*

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 6 of 59

[10] DDR_A_D[0..63]

[11] DDR_B_D[0..63]

JCPU1C

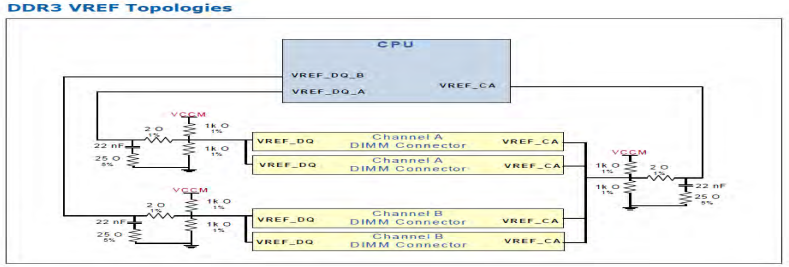
JCPU1D

FOX_3H993827-4M41-01H_HASWELL

FOX_3H993827-4M41-01H_HASWELL

+V_SM_VREF should have 20 mil trace width

DDR3 VREF Topologies



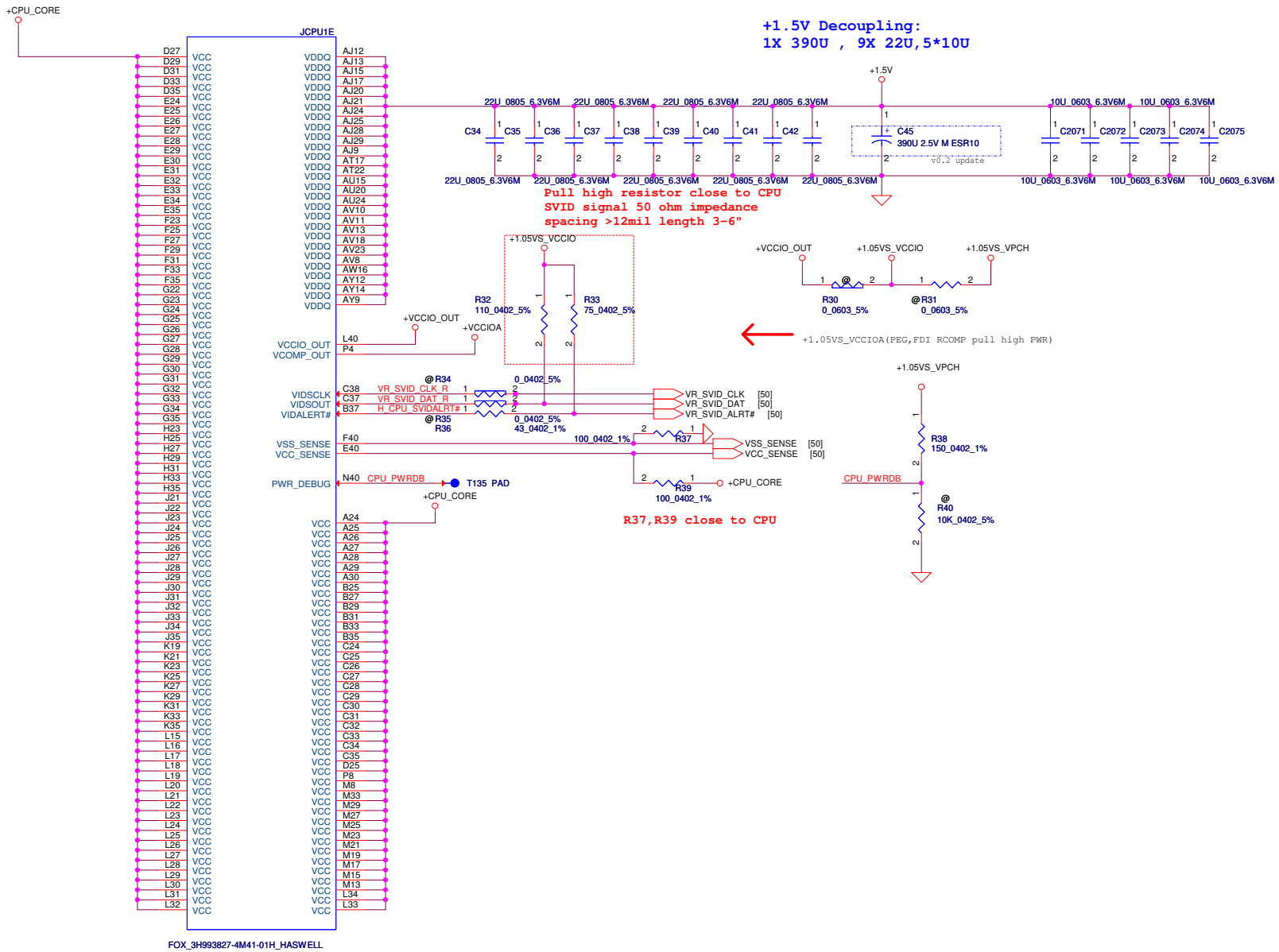
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: *Haswell_DDR3*

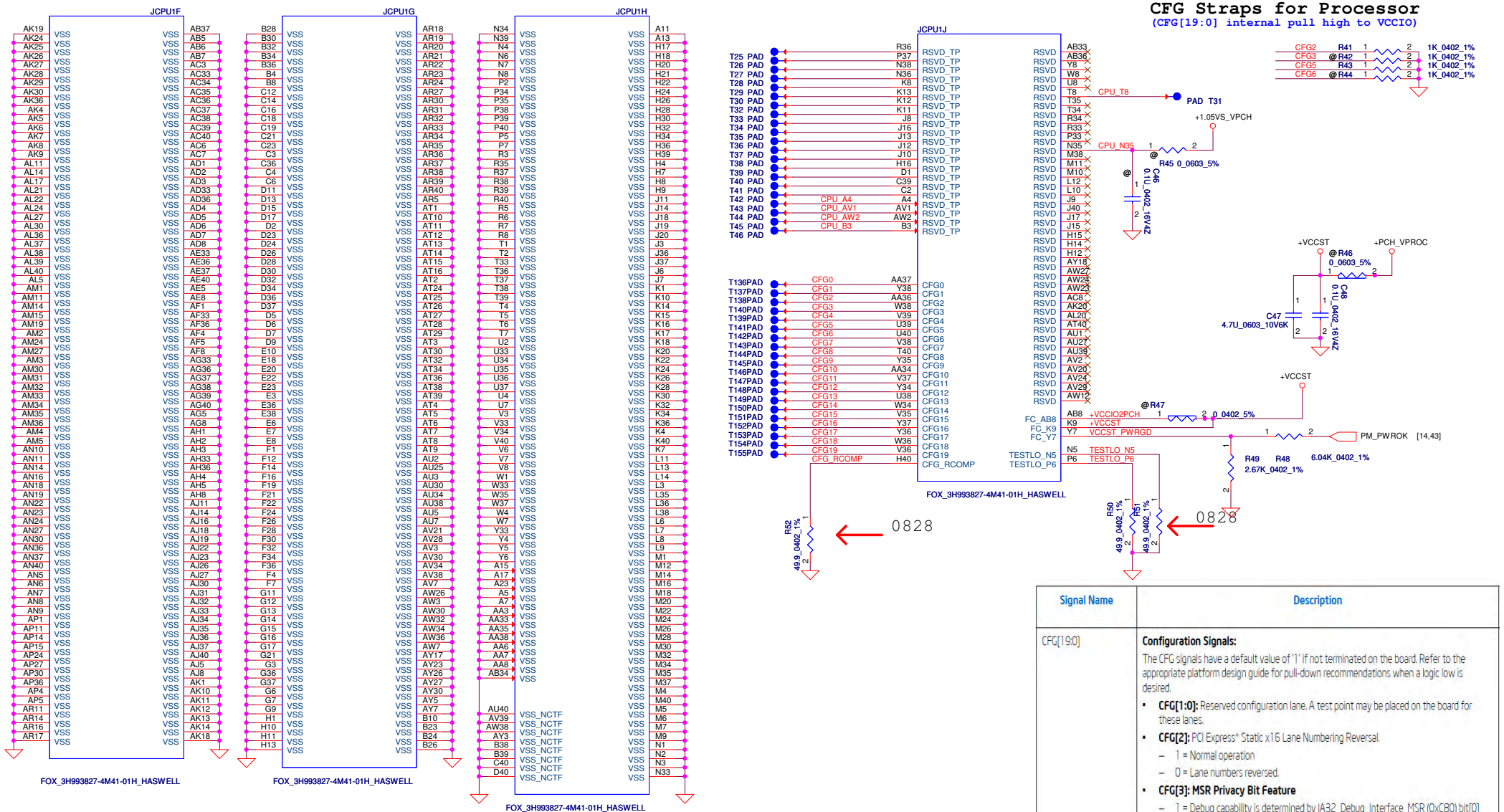
Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 7 of 59



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	Haswell_POWER		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 8 of 59		



Signal Name	Description
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]: MSR Privacy Bit Feature** – 1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting – 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ***Haswell_GND/CFG***

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 | Sheet 9 of 59

[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_D[0..63]
[7] DDR_A_MA[0..15]

CHA SO-DIMM 0(A0)

R626 1K_0402_1% — +VREF_DQA — +1.5V
R627 1K_0402_1%
C2030 0.1U_0402_16V4Z
C2031 2.2U_0603_6.3V6K
Close to JDIMM1

JDIMM1

1	VREF_DQ		2				
3	VSS2		4	VSS1			DDR_A_D4
5	DQ0	DDR_A_D0	6	DQ4	DDR_A_D5		
7	DQ1	DDR_A_D1	8	DQ5			
9	VSS3		10	DQS#0	DDR_A_DQS#0		
11	VSS4		12	DQS0	DDR_A_DQS0		
13	DM0		14	VSS6			
15	VSS5		16	DQ6	DDR_A_D6		
17	DQ2	DDR_A_D2	18	DQ7	DDR_A_D7		
19	DQ3	DDR_A_D3	20	VSS8			
21	VSS7		22	DQ12	DDR_A_D12		
23	DQ8	DDR_A_D8	24	DQ13	DDR_A_D13		
25	DQ9	DDR_A_D9	26	VSS10			
27	VSS9		28	DM1			
29	DQS#1	DDR_A_DQS#1	30	RESET#	SM_DRAMRST#	SM_DRAMRST#	[11,5]
31	DQS1	DDR_A_DQS1	32	VSS12			
33	VSS11		34	DQ14	DDR_A_D14		
35	DQ10	DDR_A_D10	36	DQ15	DDR_A_D15		
37	DQ11	DDR_A_D11	38	VSS14			
39	VSS13		40	DQ20	DDR_A_D20		
41	DQ16	DDR_A_D16	42	DQ21	DDR_A_D21		
43	DQ17	DDR_A_D17	44	VSS16			
45	VSS15		46	DM2			
47	DQS#2	DDR_A_DQS#2	48	VSS17			
49	DQS2	DDR_A_DQS2	50	DQ22	DDR_A_D22		
51	VSS18		52	DQ23	DDR_A_D23		
53	DQ18	DDR_A_D18	54	VSS19			
55	DQ19	DDR_A_D19	56	DQ28	DDR_A_D28		
57	VSS20		58	DQ29	DDR_A_D29		
59	DQ24	DDR_A_D24	60	VSS21			
61	DQ25	DDR_A_D25	62	DQS#3	DDR_A_DQS#3		
63	VSS22		64	DQS3	DDR_A_DQS3		
65	DM3		66	VSS24			
67	VSS23		68	DQ30	DDR_A_D30		
69	DQ26	DDR_A_D26	70	DQ31	DDR_A_D31		
71	DQ27	DDR_A_D27	72	VSS26			
73	VSS25		74	CKE1	DDRA_CKE1	DDRA_CKE1	[7]
75	CKE0	DDRA_CKE0	76	VDD2			
77	VDD1		78	A15	DDR_A_MA15		
79	NC1		80	A14	DDR_A_MA14		
81	BA2	DDR_A_BS2	82	VDD4			
83	VDD3		84	A11	DDR_A_MA11		
85	A12/BC#	DDR_A_MA12	86	A7	DDR_A_MA7		
87	A9	DDR_A_MA9	88	VDD6			
89	VDD5		90	A6	DDR_A_MA6		
91	A8	DDR_A_MA8	92	A4	DDR_A_MA4		
93	A5	DDR_A_MA5	94	VDD8			
95	VDD7		96	A2	DDR_A_MA2		
97	A3	DDR_A_MA3	98	A0	DDR_A_MA0		
99	A1	DDR_A_MA1	100	VDD10			
101	VDD9		102	CK1	DDRA_CLK1	DDRA_CLK1	[7]
103	CK0	DDRA_CLK0	104	CK1#	DDRA_CLK1#	DDRA_CLK1#	[7]
105	CK0#	DDRA_CLK0#	106	VDD12			
107	VDD11		108	BA1	DDR_A_BS1	DDR_A_BS1	[7]
109	A10/AP	DDR_A_MA10	110	RAS#	DDR_A_RAS#	DDR_A_RAS#	[7]
111	BA0	DDR_A_BS0	112	VDD14			
113	VDD13		114	S0#	DDRA_SCS0#	DDRA_SCS0#	[7]
115	WE#	DDR_A_WE#	116	ODT0	DDRA_ODT0	DDRA_ODT0	[7]
117	CAS#	DDR_A_CAS#	118	VDD16			
119	VDD15		120	ODT1	DDRA_ODT1	DDRA_ODT1	[7]
121	A13	DDR_A_MA13	122	NC2			
123	S1#	DDRA_SCS1#	124	VDD18			
125	VDD17		126	VREF_CA	+VREF_CAA		
127	NCTEST		128	VSS28			
129	VSS27		130	DQ36	DDR_A_D36		
131	DQ32	DDR_A_D32	132	DQ37	DDR_A_D37		
133	DQ33	DDR_A_D33	134	VSS30			
135	VSS29		136	DM4			
137	DQS#4	DDR_A_DQS#4	138	VSS31			
139	DQS4	DDR_A_DQS4	140	DQ38	DDR_A_D38		
141	VSS32		142	DQ39	DDR_A_D39		
143	DQ34	DDR_A_D34	144	VSS33			
145	DQ35	DDR_A_D35	146	DQ44	DDR_A_D44		
147	VSS34		148	DQ45	DDR_A_D45		
149	DQ40	DDR_A_D40	150	VSS35			
151	DQ41	DDR_A_D41	152	DQS#5	DDR_A_DQS#5		
153	VSS36		154	DQS5	DDR_A_DQS5		
155	DM5		156	VSS38			
157	VSS37		158	DQ46	DDR_A_D46		
159	DQ42	DDR_A_D42	160	DQ47	DDR_A_D47		
161	DQ43	DDR_A_D43	162	VSS40			
163	VSS39		164	DQ52	DDR_A_D52		
165	DQ48	DDR_A_D48	166	DQ53	DDR_A_D53		
167	DQ49	DDR_A_D49	168	VSS42			
169	VSS41		170	DM6			
171	DQS#6	DDR_A_DQS#6	172	VSS43			
173	DQS6	DDR_A_DQS6	174	DQ54	DDR_A_D54		
175	VSS44		176	DQ55	DDR_A_D55		
177	DQ50	DDR_A_D50	178	VSS45			
179	DQ51	DDR_A_D51	180	DQ60	DDR_A_D60		
181	VSS46		182	DQ61	DDR_A_D61		
183	DQ56	DDR_A_D56	184	VSS47			
185	DQ57	DDR_A_D57	186	DQS#7	DDR_A_DQS#7		
187	VSS48		188	DQS7	DDR_A_DQS7		
189	DM7		190	VSS50			
191	VSS49		192	DQ62	DDR_A_D62		
193	DQ58	DDR_A_D58	194	DQ63	DDR_A_D63		
195	DQ59	DDR_A_D59	196	VSS52			
197	VSS51		198	EVENT#			
199	SA0		200	SDA	PM_SMBDATA	PM_SMBDATA	[11,13,40,5]
201	VDDSPD		202	SCL	PM_SMBCLK	PM_SMBCLK	[11,13,40,5]
203	SA1		204	VTT2	+0.75VS		
205	VTT1	+0.75VS	206				
	G1			G2			

FOX_AS0A626-U2SN-7F
CONN@

+3VS — C2048 2.2U_0603_6.3V6K — C2049 0.1U_0402_16V4Z — R630 @ 0_0402_5%

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

Standard H:5.2mm

Layout Note: Place near JDIMM1

+1.5V
C2032 390U 2.5V M ESR10
C2033 10U_0805_6.3V6M
C2034 10U_0805_6.3V6M
C2035 10U_0805_6.3V6M
C2036 0.1U_0402_16V4Z
C2037 0.1U_0402_16V4Z
C2038 0.1U_0402_16V4Z
C2039 0.1U_0402_16V4Z
C2040 0.1U_0402_16V4Z
C2041 0.1U_0402_16V4Z
C2042 0.1U_0402_16V4Z
C2043 0.1U_0402_16V4Z

Layout Note: Place these Caps near +1.5V of JDIMM1

+1.5V — R628 1K_0402_1% — +VREF_CAA
R629 1K_0402_1%
C2044 2.2U_0603_6.3V6K
C2045 0.1U_0402_16V4Z
close to JDIMM1.126

Layout Note: Place near JDIMM1 Pin203 and 204

+0.75VS
C2046 4.7U_0603_6.3V6K
C2047 0.1U_0402_16V4Z

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: ***DDRIII-SODIMMA***

Size	Document Number	Rev
C	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 — Sheet 10 of 59

[7] DDR_B_DQS#[0..7]
[7] DDR_B_DQS[0..7]
[7] DDR_B_D[0..63]
[7] DDR_B_MA[0..15]

CHB SO-DIMM

JDIMM2

1	VREF_DQ	VSS1	2		3	VSS2	DQ4	4	DDR_B_D4
5	DDR_B_D0	DQ0	DQ5	6	DDR_B_D5				
7	DDR_B_D1	DQ1	VSS3	8		9	VSS4	DQS#0	10	DDR_B_DQS#0
11	DDR_B_DQS0	DM0	DQS0	12		13	VSS5	DQ2	14	
15	DDR_B_D2	DQ3	VSS6	16	DDR_B_D6					
17	DDR_B_D3	DQ7	DQ6	18	DDR_B_D7					
19	VSS7	DQ8	20		21	DDR_B_D8	DQ12	22	DDR_B_D12
23	DDR_B_D9	DQ13	DQ9	24	DDR_B_D13					
25	VSS9	DQS#1	VSS10	26		27	DDR_B_DQS#1	DM1	28	
29	DDR_B_DQS1	RESET#	VSS11	30	SM_DRAMRST#					
31	DQS1	VSS12	32		33	DDR_B_D10	DQ14	34	DDR_B_D14
35	DDR_B_D11	DQ10	DQ15	36	DDR_B_D15					
37	VSS13	DQ16	VSS14	38		39	DDR_B_D16	DQ20	40	DDR_B_D20
41	DDR_B_D17	DQ17	DQ21	42	DDR_B_D21					
43	VSS15	DQS#2	VSS16	44		45	DDR_B_DQS#2	DM2	46	
47	DDR_B_DQS2	DQS2	VSS17	48		49	DDR_B_D18	DQ22	50	DDR_B_D22
51	DDR_B_D19	DQ18	DQ23	52	DDR_B_D23					
53	DQ19	VSS18	54		55	DDR_B_D24	DQ28	56	DDR_B_D28
57	DDR_B_D25	DQ24	DQ29	58	DDR_B_D29					
59	DQ25	VSS20	60		61	DDR_B_DQS#3	DQS3	62	DDR_B_DQS3
63	DDR_B_DQS3	DM3	DQS3	64		65	DDR_B_D26	DQ26	66	DDR_B_D30
67	DDR_B_D27	DQ27	DQ31	68	DDR_B_D31					
69	VSS25	VSS26	70		71	DDRB_CKE0	CKE0	CKE1	72	DDRB_CKE1
73	VDD1	VDD2	74		75	NC1	A15	76	DDR_B_MA15
77	DDR_B_BS2	BA2	A14	78	DDR_B_MA14					
79	VDD3	VDD4	80		81	DDR_B_MA12	A12/BC#	A11	82	DDR_B_MA11
83	DDR_B_MA9	A9	A7	84	DDR_B_MA7					
85	VDD5	VDD6	86		87	DDR_B_MA8	A8	A6	88	DDR_B_MA6
89	DDR_B_MA5	A5	A4	90	DDR_B_MA4					
91	VDD7	VDD8	92		93	DDR_B_MA3	A3	A2	94	DDR_B_MA2
95	DDR_B_MA1	A1	A0	96	DDR_B_MA0					
97	VDD9	VDD10	98		99	DDRB_CLK0	CK0	CK1	100	DDRB_CLK1
101	DDRB_CLK0#	CK0#	CK1#	102	DDRB_CLK1#					
103	VDD11	VDD12	104		105	DDR_B_MA10	A10/AP	BA1	106	DDR_B_BS1
107	DDR_B_BS0	BA0	RAS#	108	DDR_B_RAS#					
109	VDD13	VDD14	110		111	DDR_B_WE#	WE#	S0#	112	DDRB_SCS0#
113	DDR_B_CAS#	CAS#	ODT0	114	DDRB_ODT0					
115	VDD15	VDD16	116		117	DDR_B_MA13	A13	ODT1	118	DDRB_ODT1
119	DDRB_SCS1#	S1#	NC2	120		121	VDD17	VDD18	122	
123	NCTEST	VREF_CA	124		125	DDR_B_D32	VSS27	VSS28	126	DDR_B_D36
127	DDR_B_D33	DQ32	DQ36	128	DDR_B_D37					
129	DQ33	VSS29	130		131	DDR_B_DQS#4	DQS#4	DM4	132	
133	DDR_B_DQS4	DQS4	VSS31	134		135	DDR_B_D34	DQ34	136	DDR_B_D38
137	DDR_B_D35	DQ35	DQ39	138	DDR_B_D39					
139	VSS32	DQ40	VSS33	140		141	DDR_B_D40	DQ41	142	DDR_B_D44
143	DDR_B_D41	DQ41	DQ45	144	DDR_B_D45					
145	VSS34	DQS#5	VSS35	146		147	DDR_B_D42	DM5	148	DDR_B_DQS#5
149	DDR_B_D43	DQS5	DQ47	150	DDR_B_D47					
151	VSS36	VSS37	152		153	DDR_B_D48	DQ42	VSS38	154	DDR_B_D46
155	DDR_B_D49	DQ43	DQ48	156	DDR_B_D52					
157	VSS39	DQ49	VSS40	158		159	DDR_B_DQS#6	DQ52	160	DDR_B_D53
161	DDR_B_DQS6	DQS6	DQ53	162		163	DDR_B_D50	VSS41	164	
165	DDR_B_D51	DQS#6	VSS42	166		167	DDR_B_D54	DQ50	168	DDR_B_D55
169	VSS43	DQ54	VSS44	170		171	DDR_B_D56	DQ51	172	DDR_B_D60
173	DDR_B_D57	DQ55	DQ56	174	DDR_B_D61					
175	VSS45	DQ60	VSS46	176		177	DDR_B_DQS#7	DQ57	178	DDR_B_DQS7
179	DDR_B_D58	DQS#7	VSS47	180		181	DDR_B_D62	DM7	182	DDR_B_D63
183	DDR_B_D59	DQS7	DQ62	184		185	VSS48	DQ58	186	
187	DQ63	VSS49	188		189	SA0	EVENT#	VSS50	190	
191	PM_SMBDATA	VDDSPD	SDA	192	PM_SMBDATA [10,13,40,5]					
193	PM_SMBCLK	SA1	SCL	194	PM_SMBCLK [10,13,40,5]					
195	VSS51	VTT1	VTT2	196	+0.75VS	197	VSS52	G1	G2	198

SUYIN_600023HB204G208ZL
CONN@

SM_DRAMRST# [10,5]

Close to JDIMM2

R631 1K_0402_1% — +1.5V — +VREF_DQB
R632 1K_0402_1%
C2050 2.2U_0603_6.3V6K
C2051 0.1U_0402_16V4Z

SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

+3VS — R635 10K_0402_5% — +0.75VS
@C2068 2.2U_0603_6.3V6K
C2069 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2

+1.5V
C2052 @ 390U 2.5V M ESR10
C2053 10U_0805_6.3V6M
C2054 10U_0805_6.3V6M
C2055 10U_0805_6.3V6M

+1.5V
C2056 0.1U_0402_16V4Z
C2057 0.1U_0402_16V4Z
C2058 0.1U_0402_16V4Z
C2059 0.1U_0402_16V4Z
C2060 0.1U_0402_16V4Z
C2061 0.1U_0402_16V4Z
C2062 0.1U_0402_16V4Z
C2063 0.1U_0402_16V4Z

Layout Note: Place these Caps near +1.5V of JDIMM2

+1.5V — R633 1K_0402_1% — +VREF_CAB
R634 1K_0402_1%
+VREF_CAB

C2064 2.2U_0603_6.3V6K
C2065 0.1U_0402_16V4Z
Close to JDIMM2

+0.75VS
C2066 4.7U_0603_6.3V6K
C2067 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM2 Pin203 and 204

Standard H:9.2mm

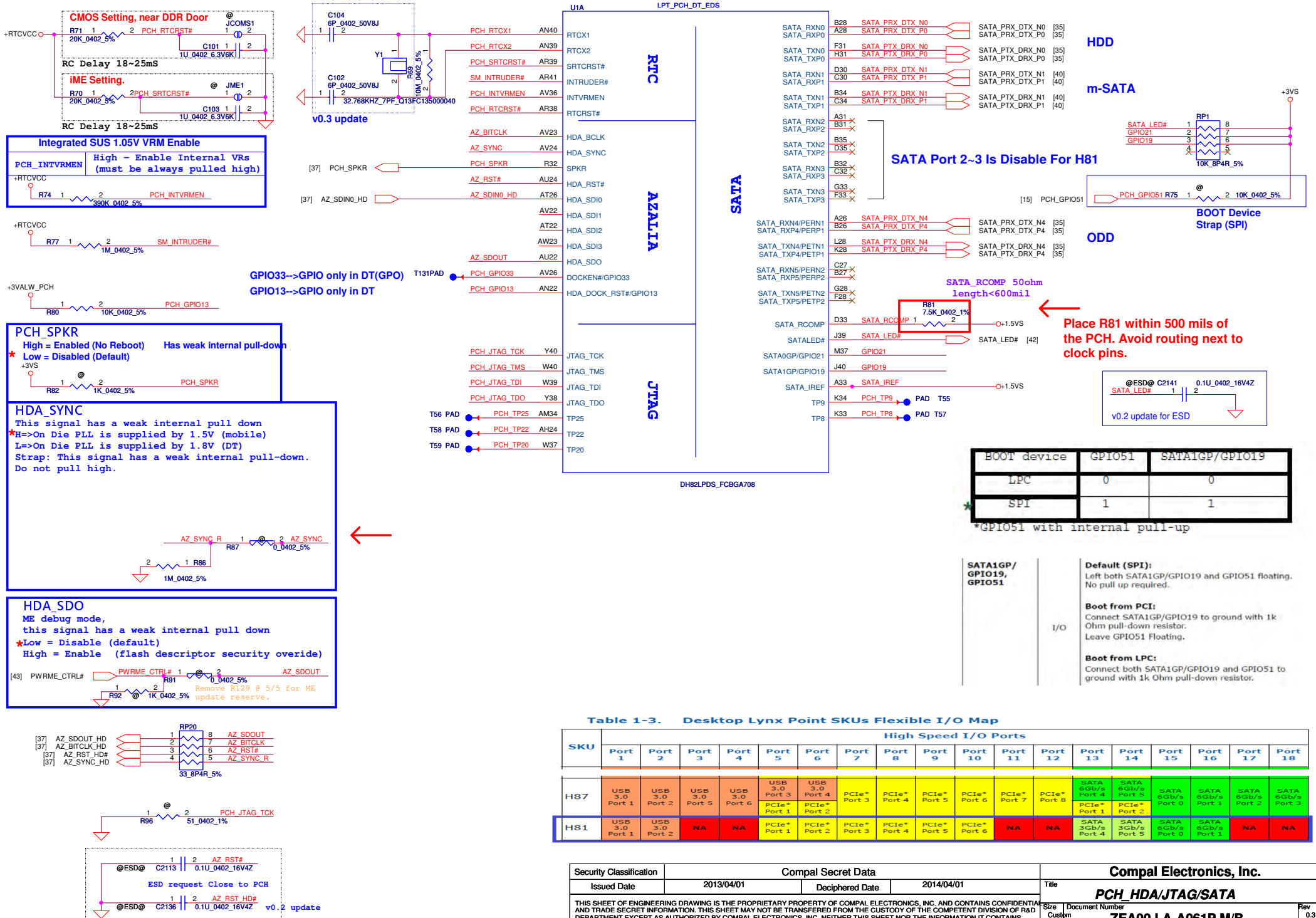
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ***DDRIII-SODIMM B***

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 | Sheet 11 of 59



BOOT device	GPIO51	SATA1GP/GPIO19
LPC	0	0
* SPI	1	1

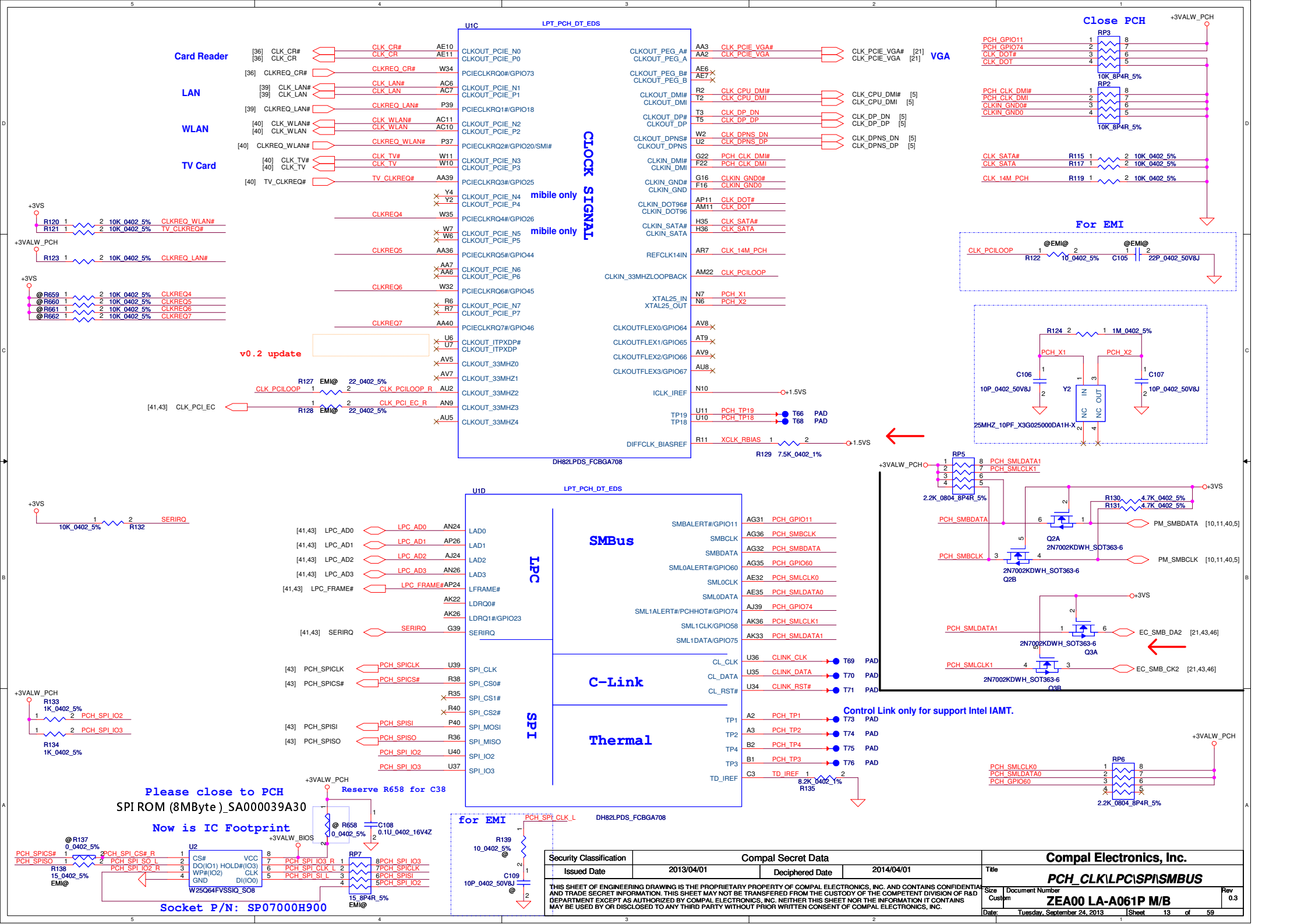
*GPIO51 with internal pull-up

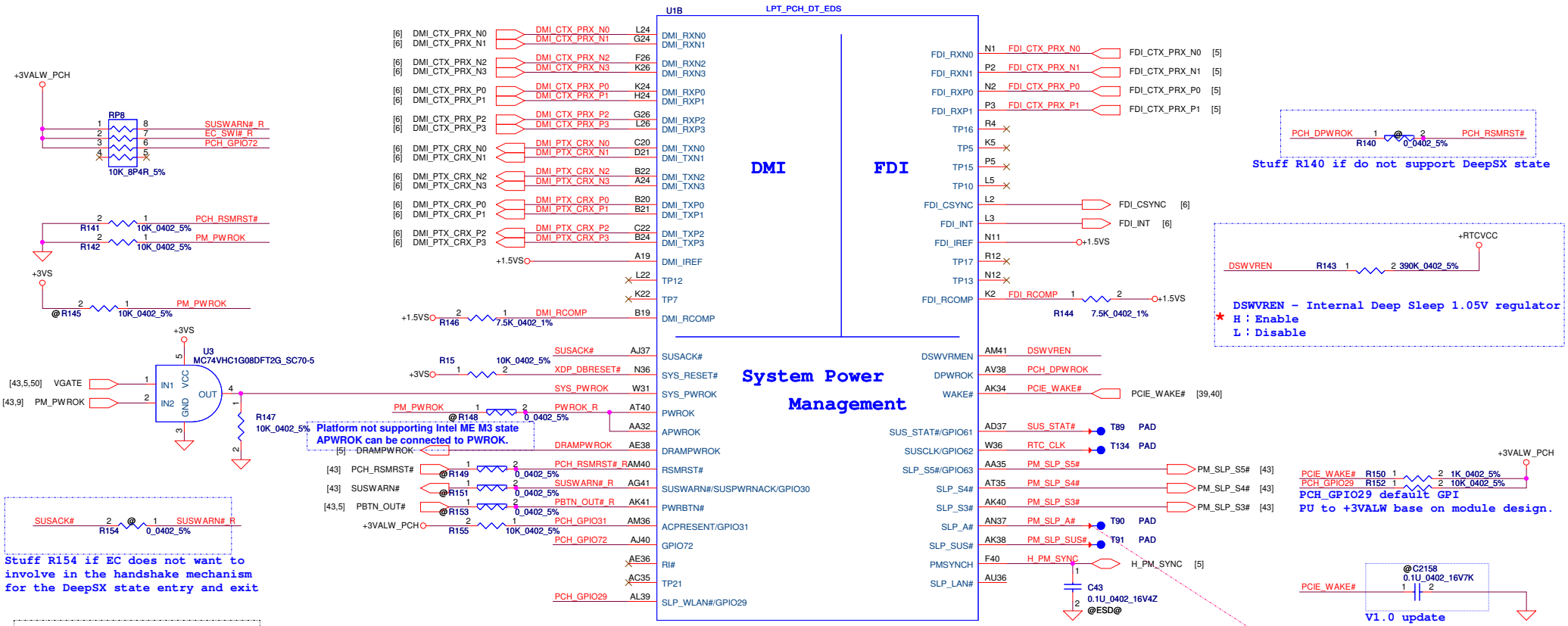
SATA1GP/ GPIO19, GPIO51	I/O	**Default (SPI):** Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required. **Boot from PCI:** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating. **Boot from LPC:** Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

Table 1-3. Desktop Lynx Point SKUs Flexible I/O Map

SKU	High Speed I/O Ports																	
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14	Port 15	Port 16	Port 17	Port 18
H87	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 5	USB 3.0 Port 6	USB 3.0 Port 3 / PCIe* Port 1	USB 3.0 Port 4 / PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	PCIe* Port 7	PCIe* Port 8	SATA 6Gb/s Port 4 / PCIe* Port 1	SATA 6Gb/s Port 5 / PCIe* Port 2	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	SATA 6Gb/s Port 2	SATA 6Gb/s Port 3
H81	USB 3.0 Port 1	USB 3.0 Port 2	NA	NA	PCIe* Port 1	PCIe* Port 2	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5	PCIe* Port 6	NA	NA	SATA 3Gb/s Port 4	SATA 3Gb/s Port 5	SATA 6Gb/s Port 0	SATA 6Gb/s Port 1	NA	NA

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/01	Deciphered Date 2014/04/01	Title: PCH_HDA/JTAG/SATA
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Custom; Document Number: ZEA00 LA-A061P M/B; Rev: 0.3
			Date: Tuesday, September 24, 2013; Sheet 12 of 59


Close PCH
For EMI
Card Reader
LAN
WLAN
TV Card
VGA
CLOCK SIGNAL
mibile only
v0.2 update
U1C
LPT_PCH_DT_EDS
DH82LPDS_FCBGA708
U1D
LPC
SPI
SMBus
C-Link
Thermal
Control Link only for support Intel IAMT.
Please close to PCH
SPI ROM (8MByte)_SA000039A30
Now is IC Footprint
Reserve R658 for C38
Socket P/N: SP07000H900
for EMI
Security Classification
Compal Secret Data
Issued Date
2013/04/01
Deciphered Date
2014/04/01
Compal Electronics, Inc.
PCH_CLK\LPC\SPI\SMBUS
ZEA00 LA-A061P M/B
Tuesday, September 24, 2013
Sheet 13 of 59



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	PCH_DMI/FDI/PM		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 14 of 59		

PCI PU resistor

RP9
1 8 PCI_PIRQD#
2 7 PCI_PIRQB#
3 6 PCH_GPIO5
4 5 PCI_PIRQC#
8.2K_8P4R_5%

R159 1 2 8.2K_0402_5% PCH_GPIO50
R160 1 2 8.2K_0402_5% PCH_GPIO52
R161 1 2 8.2K_0402_5% PCH_GPIO54

RP10
1 8 PCH_GPIO4
2 7 PCI_PIRQA#
3 6 PCH_GPIO3
4 5 PCH_GPIO2
8.2K_8P4R_5%

1 CRT@ 2 PCH_CRT_CLK
R162 2.2K_0402_5%
1 CRT@ 2 PCH_CRT_DATA
R163 2.2K_0402_5%

RP11
1 8 PCH_CRT_B
2 7 PCH_CRT_G
3 6 PCH_CRT_R
4 5
150_0804_8P4R_1%
CRT@

Close to PCH <250mils

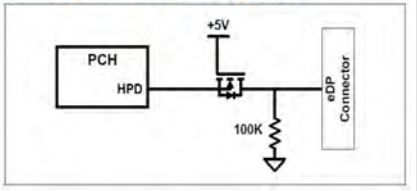
2 1 PCH_GPIO53
@R157 10K_0402_5%
2 1 PCH_GPIO55
@R158 10K_0402_5%

Internal pull high
Strap defalut high
GPIO53 DMI AC mode if Low
GPIO55 A16 SWAP OVERRIDE if Low

NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

RP17
PCH_DPD_CLK 1 8
PCH_DPD_DAT 2 7
PCH_HDMIOUT_CLK 3 6
PCH_HDMIOUT_DATA 4 5
2.2K_0804_8P4R_5%
+3VS

Figure 9-3. Processor Graphics eDP* HPD Signal off of Digital Port D



+5VS
Q57 BSS138LT1G_SOT23-3
DDPD_HPD 3 1 PCH_DDPD_HPD [29]
R605 @ 1 2 0_0402_5%
R606 100K_0402_5%

U1E LPT_PCH_DT_EDS

Data Need longer than CLK 1 inch

CRT
[41] PCH_CRT_B PCH_CRT_B AC3 VGA_BLUE
[41] PCH_CRT_G PCH_CRT_G AE2 VGA_GREEN
[41] PCH_CRT_R PCH_CRT_R AC2 VGA_RED
[41] PCH_CRT_CLK PCH_CRT_CLK AL2 VGA_DDC_CLK
[41] PCH_CRT_DATA PCH_CRT_DATA AL3 VGA_DDC_DATA
[41] PCH_CRT_HSYNC PCH_CRT_HSYNC AH3 VGA_HSYNC
[41] PCH_CRT_VSYNC PCH_CRT_VSYNC AH2 VGA_VSYNC
Disable use 1K on mobile
1 2 CRT_IREF AF5 DAC_IREF
R165 649_0402_1%
AG4 VGA_IRTN
CRT_IREF Close to PCH <500mils

LVDS
To Converter [29] PCH_EDP_PWM PCH_EDP_PWM AP2 EDP_BKLTCTL
[29] PCH_EDP_BLEN PCH_EDP_BLEN AT2 EDP_BKLTEN
v0.2 update
T133 PAD PCH_EDP_VDDEN AP1 EDP_VDDEN

PCI
PCI_PIRQA# AU29 PIRQA#
PCI_PIRQB# AU27 PIRQB#
PCI_PIRQC# AW28 PIRQC#
PCI_PIRQD# AV27 PIRQD#
[21,43] DGPU_HOLD_RST# 1 2 @R167 0_0402_5% PCH_GPIO50 AH26 GPIO50
PCH_GPIO52 AJ26 GPIO52
[23,43] DGPU_PWR_EN 1 2 @R170 0_0402_5% PCH_GPIO54 AW33 GPIO54
[12] PCH_GPIO51 PCH_GPIO51 AU31 GPIO51
PCH_GPIO53 AV31 GPIO53
PCH_GPIO55 R30 GPIO55

DISPLAY

DDPB_CTRLCLK AM1 PCH_HDMIOUT_CLK → PCH_HDMIOUT_CLK [30]
DDPB_CTRLDATA AJ5 PCH_HDMIOUT_DATA → PCH_HDMIOUT_DATA [30]
DDPC_CTRLCLK AN3 PCH_HDMI_CLK PAD T92
DDPC_CTRLDATA AM2 PCH_HDMI_DATA PAD T93
DDPD_CTRLCLK AN4 PCH_DPD_CLK
DDPD_CTRLDATA AN2 PCH_DPD_DAT

HDMI OUT
(To Conn.)

eDP
(LVDS Converter)

DDPB_AUXN AK6 DDPB_AUXN PAD T96
DDPC_AUXN AG7 DDPC_AUXN PAD T97
DDPD_AUXN AG11 PCH_DDPD_AUXN C112 1 2 0.1U_0402_16V4Z → PCH_DDPD_AUXN_C [29] LVDS Converter
DDPB_AUXP AK8 DDPB_AUXP PAD T98
DDPC_AUXP AG6 DDPC_AUXP PAD T99
DDPD_AUXP AG10 PCH_DDPD_AUXP C113 1 2 0.1U_0402_16V4Z → PCH_DDPD_AUXP_C [29] LVDS Converter
DDPB_HPD AJ2 PCH_HDMIOUT_HPD → PCH_HDMIOUT_HPD [30] HDMI OUT
DDPC_HPD AH5 DPD_HPD PAD T100
DDPD_HPD AJ4 DDPD_HPD LVDS Converter

PIRQE#/GPIO2 AR30 PCH_GPIO2
PIRQF#/GPIO3 AV29 PCH_GPIO3
PIRQG#/GPIO4 AV28 PCH_GPIO4
PIRQH#/GPIO5 AT27 PCH_GPIO5
PME# AA31 PCI_PME# PADT101
PLTRST# AA37 PCH_PLT_RST#
C2121 0.1U_0402_16V4Z @ESD@

DH82LPDS_FCBGA708

PCH_DDPD_AUXN_C R172 1 @ 2 100K_0402_5% +3VS
PCH_DDPD_AUXP_C R173 1 @ 2 100K_0402_5%
CRB Reserve PU/PL

Seperate U10, U57 location

@R164 0_0402_5%
+3VS
C111 0.1U_0402_16V4Z
U4 MC74VHC1G08DFT2G_SC70-5
PCH_PLT_RST# → IN1 IN2 VCC GND OUT → PLT_RST# [21,41,43]
For GPU/TPM/EC
R166 100K_0402_5%

R677 0_0402_5%
@R678 0_0402_5% +3VALW_PCH +3VS
v0.3 update
for wake from WLAN(BCM43142)
@ C2029 0.1U_0402_16V4Z
For Card reader/
LAN/WLAN/TV
U5 MC74VHC1G08DFT2G_SC70-5
IN1 IN2 VCC GND OUT → PLT_A_RST# [36,39,40]
R171 100K_0402_5%
C2135 ESD@ 0.1U_0402_16V4Z
v0.2 update

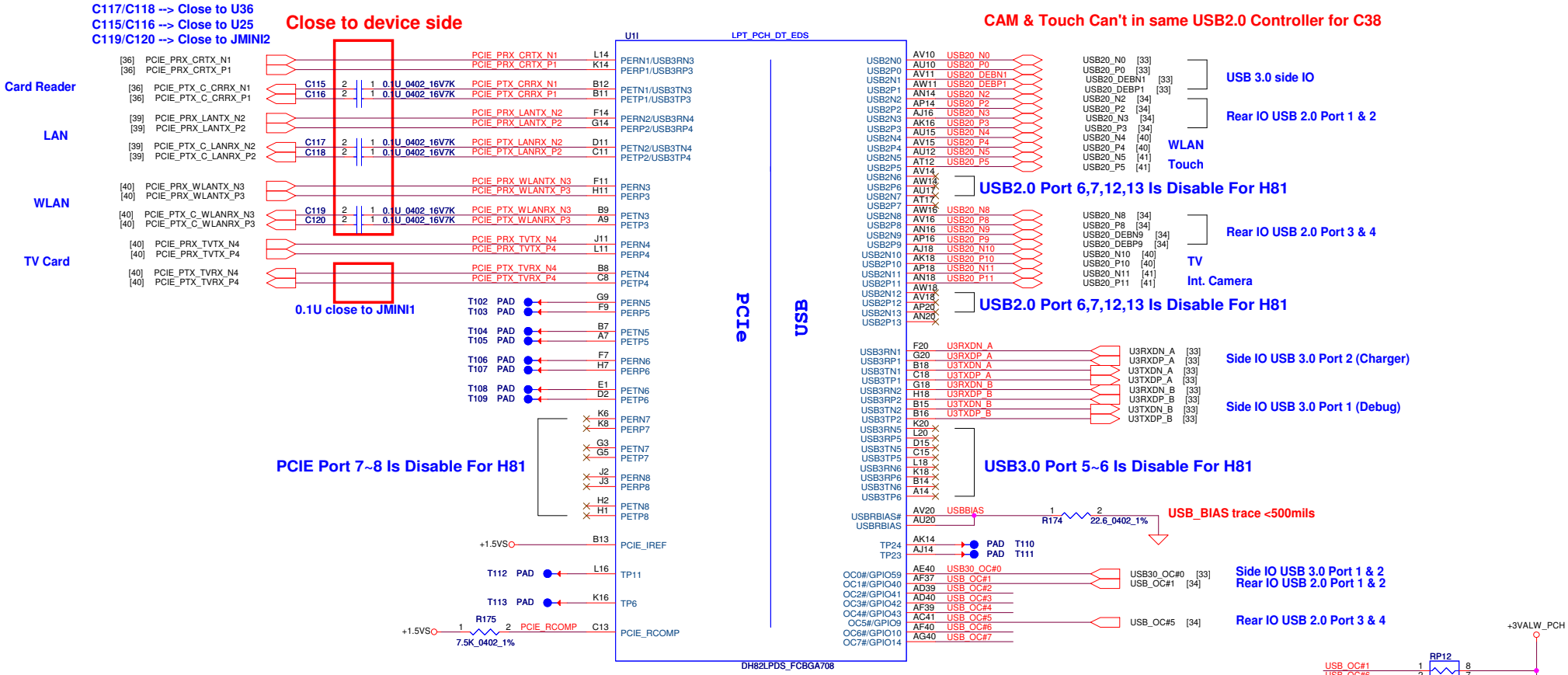
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

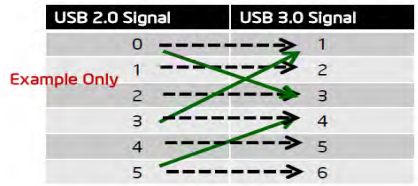
Title: PCH_CRT/DDC

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 Sheet 15 of 59



- Port mapping restrictions removed
  - USB 3.0 signals can now be paired with any of USB2.0 signal 0-13
  - Custom mapping through ACPI table/BIOS
  - Default mapping USB 3.0 1-6 to USB 2.0 0-5 ports



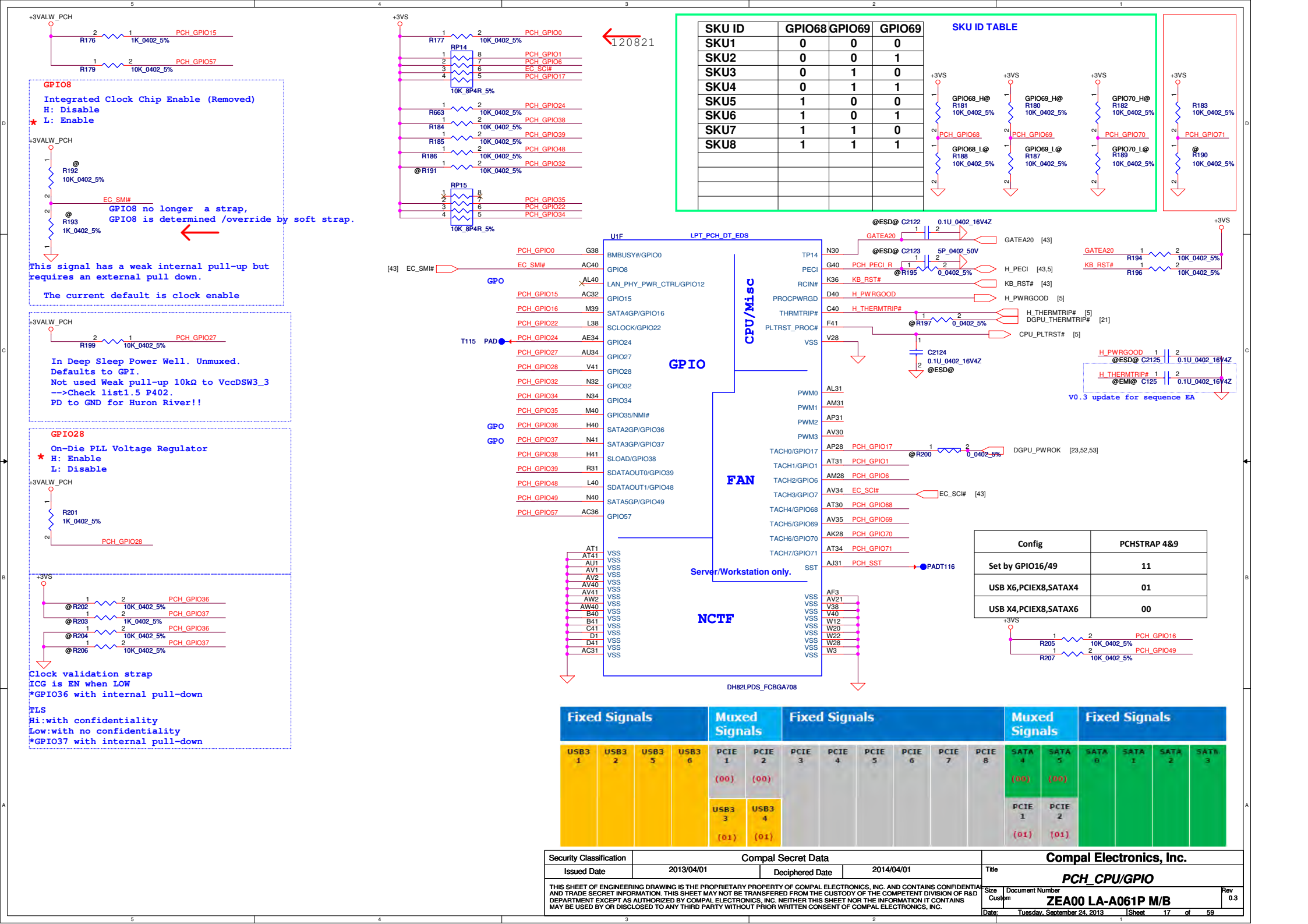
- Better USB 2.0 performance than EHCI
- Windows* 8 is expected to include a native inbox xHCI driver

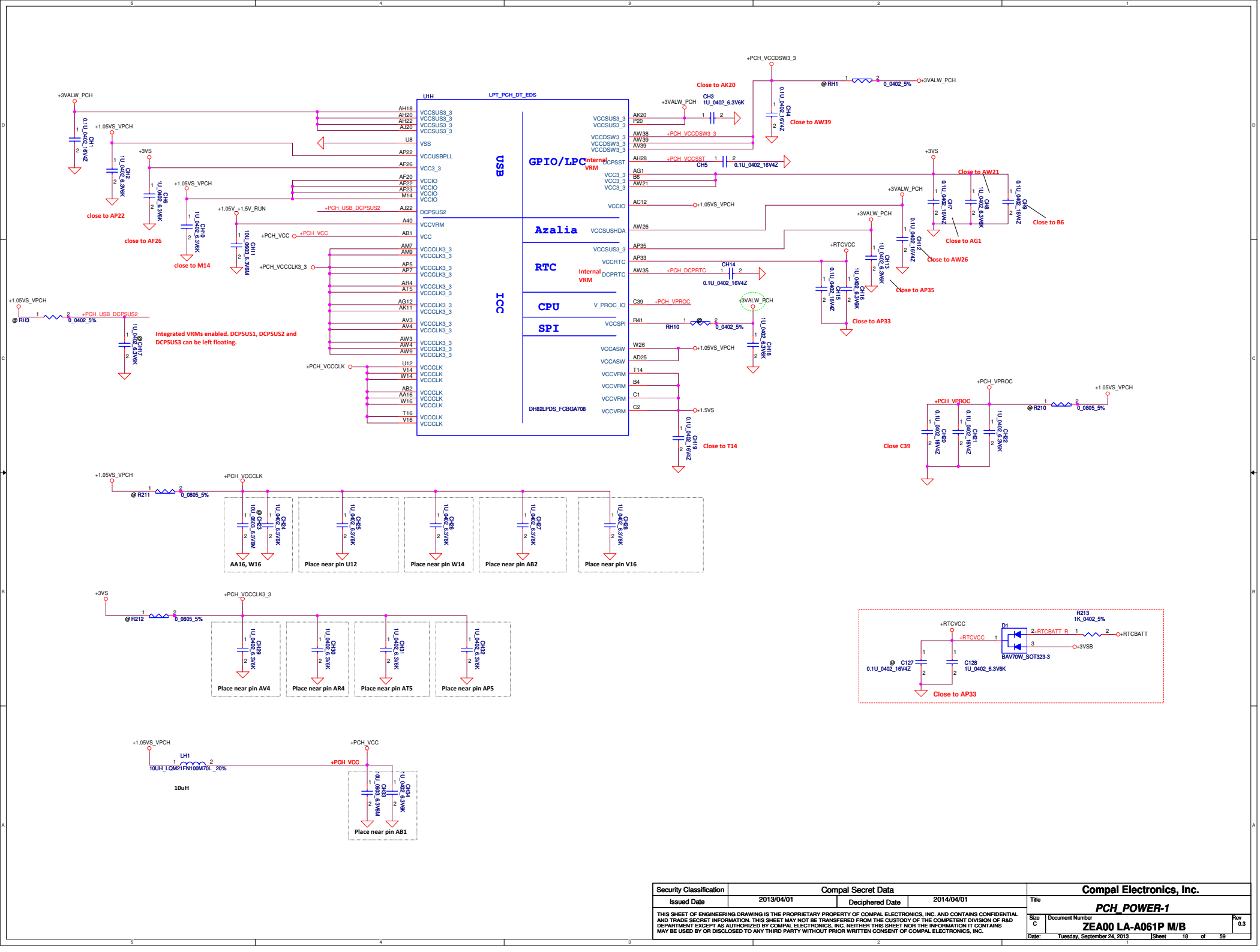
Table 14-4. Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	PCH_PCI-E/USB		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 16 of 59		


GPIO8
Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable
GPIO8 no longer a strap,
GPIO8 is determined /override by soft strap.
This signal has a weak internal pull-up but requires an external pull down.
The current default is clock enable
In Deep Sleep Power Well. Unmuxed.
Defaults to GPI.
Not used Weak pull-up 10kΩ to VccDSW3_3
-->Check list1.5 P402.
PD to GND for Huron River!!
GPIO28
On-Die PLL Voltage Regulator
* H: Enable
L: Disable
Clock validation strap
ICG is EN when LOW
*GPIO36 with internal pull-down
TLS
Hi:with confidentiality
Low:with no confidentiality
*GPIO37 with internal pull-down
120821
SKU ID TABLE
SKU ID | GPIO68 | GPIO69 | GPIO69
SKU1 | 0 | 0 | 0
SKU2 | 0 | 0 | 1
SKU3 | 0 | 1 | 0
SKU4 | 0 | 1 | 1
SKU5 | 1 | 0 | 0
SKU6 | 1 | 0 | 1
SKU7 | 1 | 1 | 0
SKU8 | 1 | 1 | 1
U1F
LPT_PCH_DT_EDS
GPIO
CPU/Misc
FAN
NCTF
Server/Workstation only.
DH82LPDS_FCBGA708
Config | PCHSTRAP 4&9
Set by GPIO16/49 | 11
USB X6,PCIEX8,SATAX4 | 01
USB X4,PCIEX8,SATAX6 | 00
V0.3 update for sequence EA
Fixed Signals
Muxed Signals
Fixed Signals
Muxed Signals
Fixed Signals
Security Classification
Compal Secret Data
Issued Date
2013/04/01
Deciphered Date
2014/04/01
Compal Electronics, Inc.
PCH_CPU/GPIO
ZEA00 LA-A061P M/B
Tuesday, September 24, 2013
Sheet 17 of 59

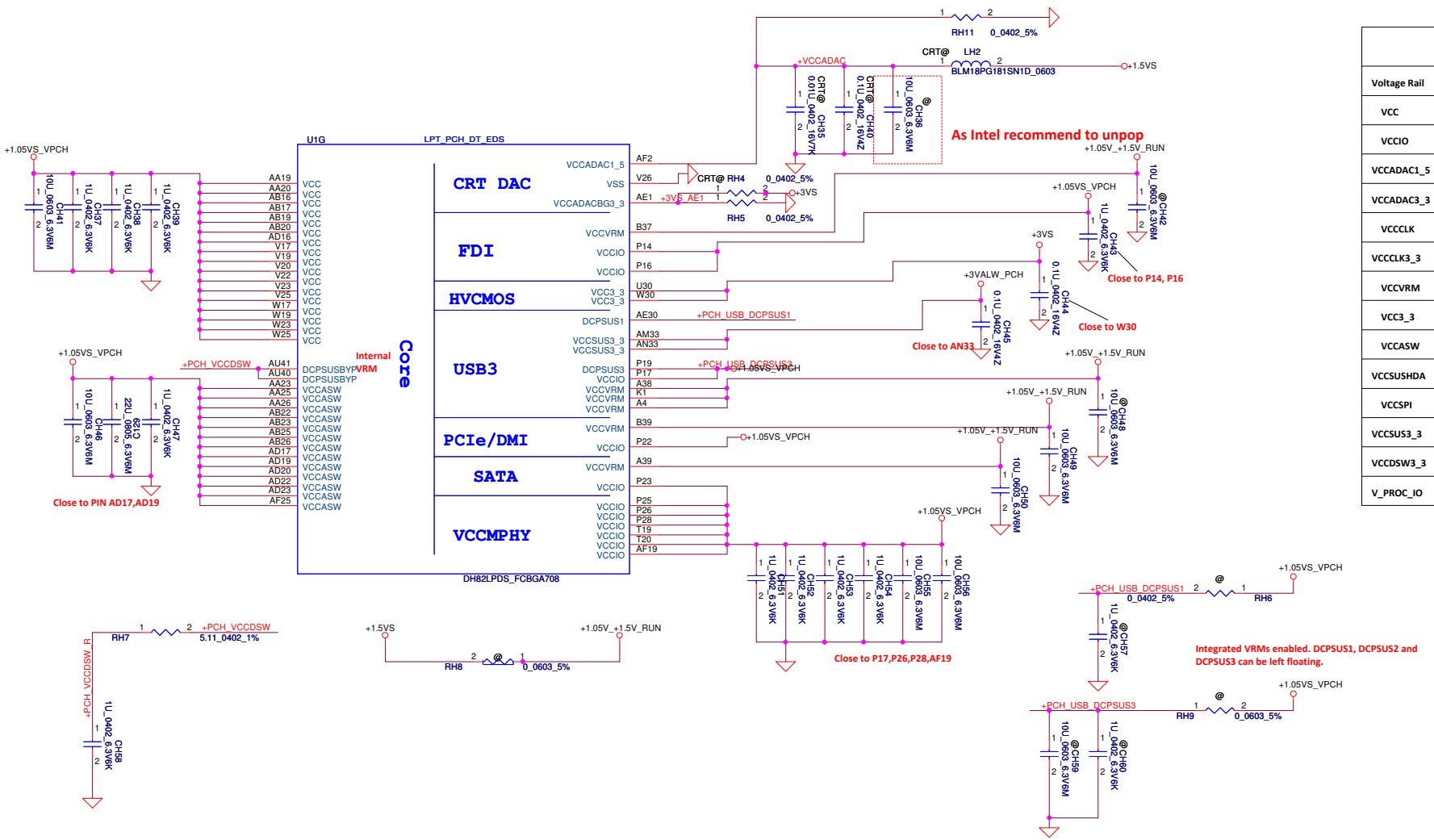


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/01	Deciphered Date	2014/04/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Title	PCH_POWER-1		
Size	Document Number		Rev
C	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	18 of 59

If CRT disable Pin AF2 & Pin AE1 can connect to GND



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

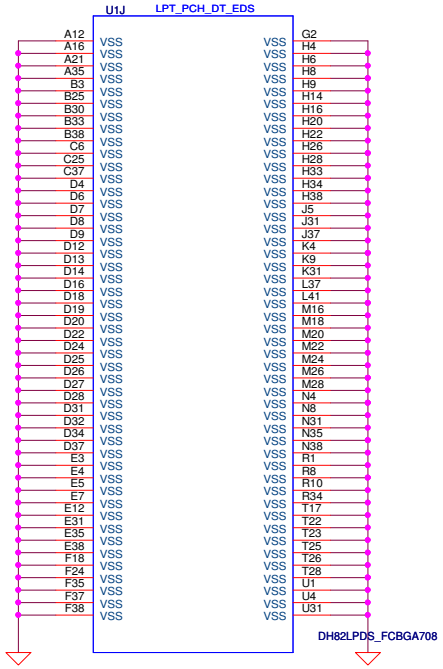
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

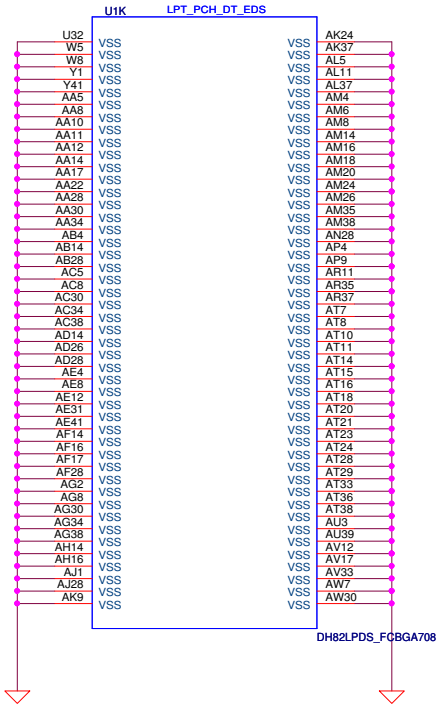
Compal Electronics, Inc.

Title: *PCH_POWER-2*

Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 19 of 59





Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ***PCH_GND***

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 | Sheet 20 of 59

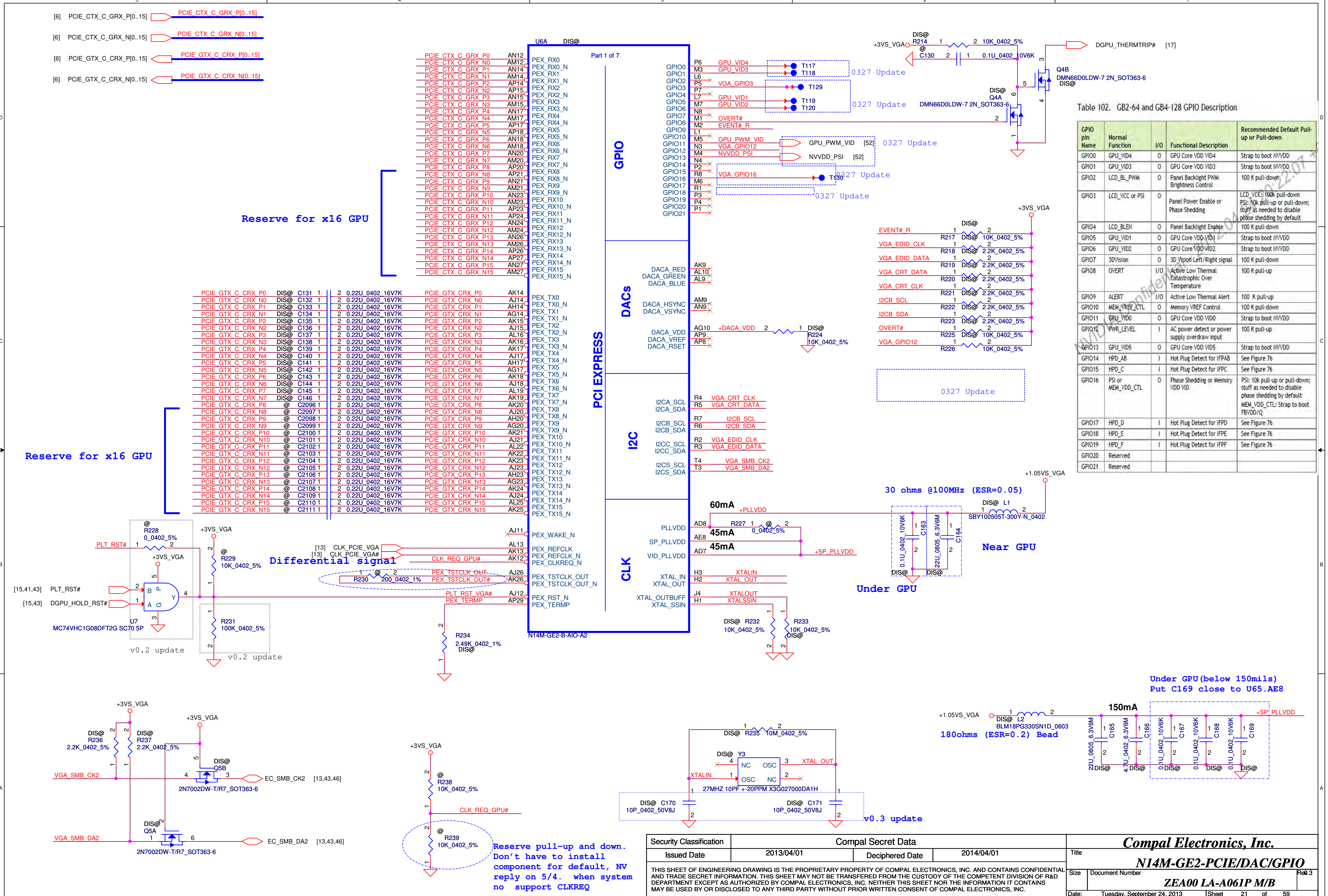


Table 102. GB2-64 and GB4-128 GPIO Description

GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100k pull-down PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVVDD
GPIO7	3DVision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **N14M-GE2-PCIE/DAC/GPIO**

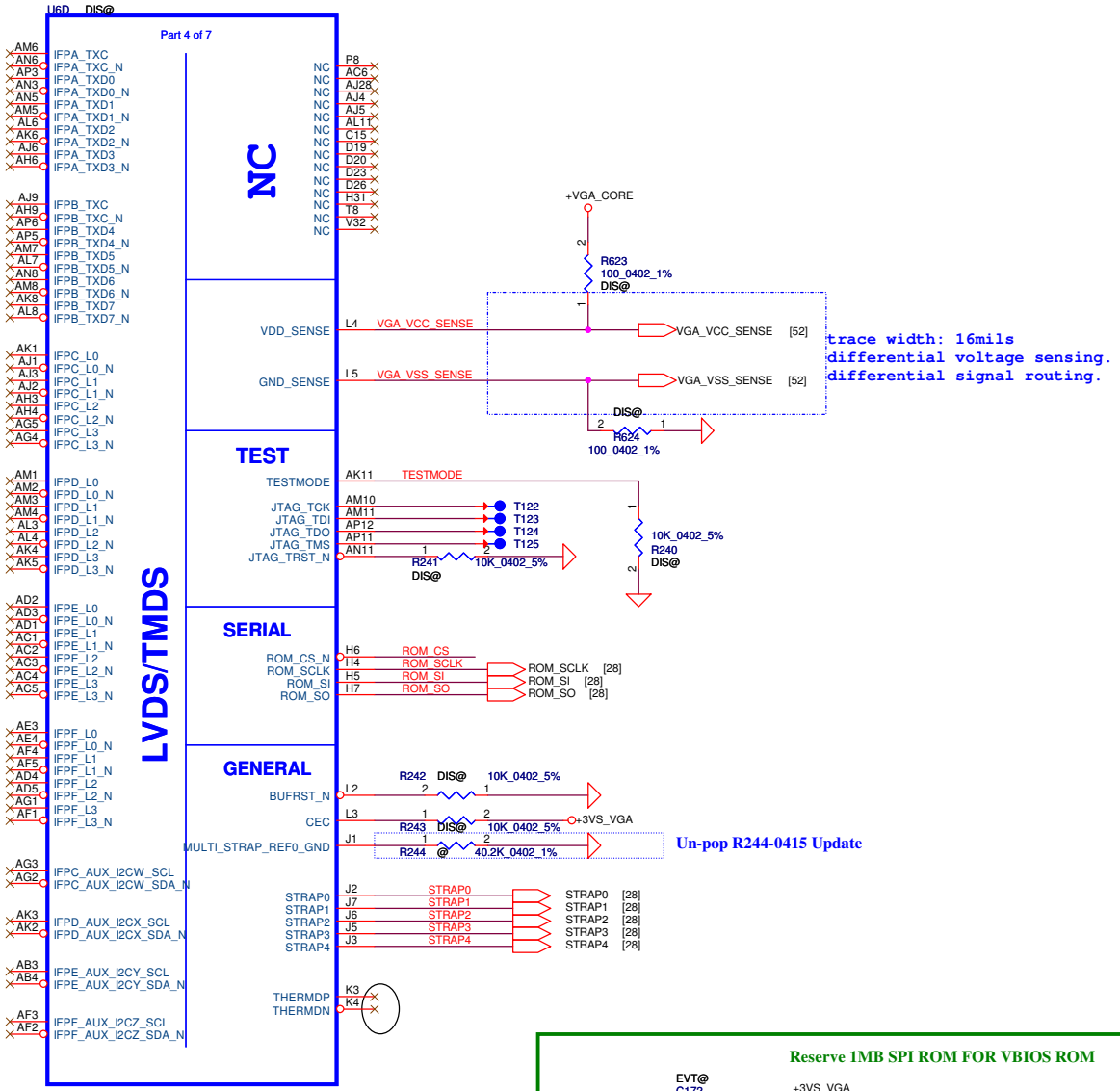
Size | Document Number: **ZEA00 LA-A061P M/B** | Rev 0.3

Date: Tuesday, September 24, 2013 | Sheet 21 of 59

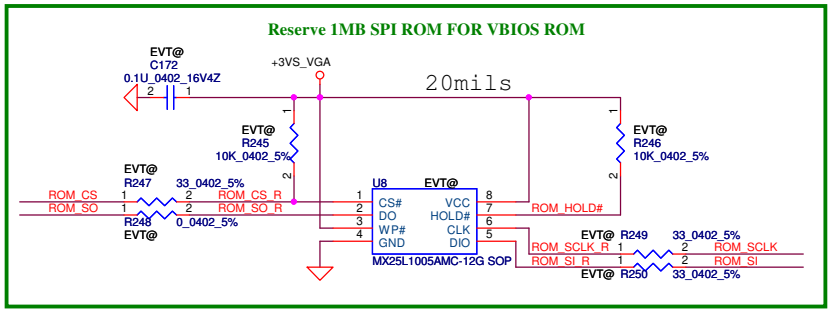
Table 66. N13x Family Display Link Summary

Link	Description
Link A	LVDS (Single Link or Dual Link with IFPB)
Link B	LVDS (Dual Link with IFPA)
Link C	DisplayPort, HDMI
Link D	DisplayPort, eDP
Link E	DisplayPort, DVI (Single Link or Dual Link with IFPF), HDMI
Link F	DisplayPort, DVI (Dual Link with IFPE), HDMI

- 2012.04.24 20:22



trace width: 16mils
differential voltage sensing.
differential signal routing.



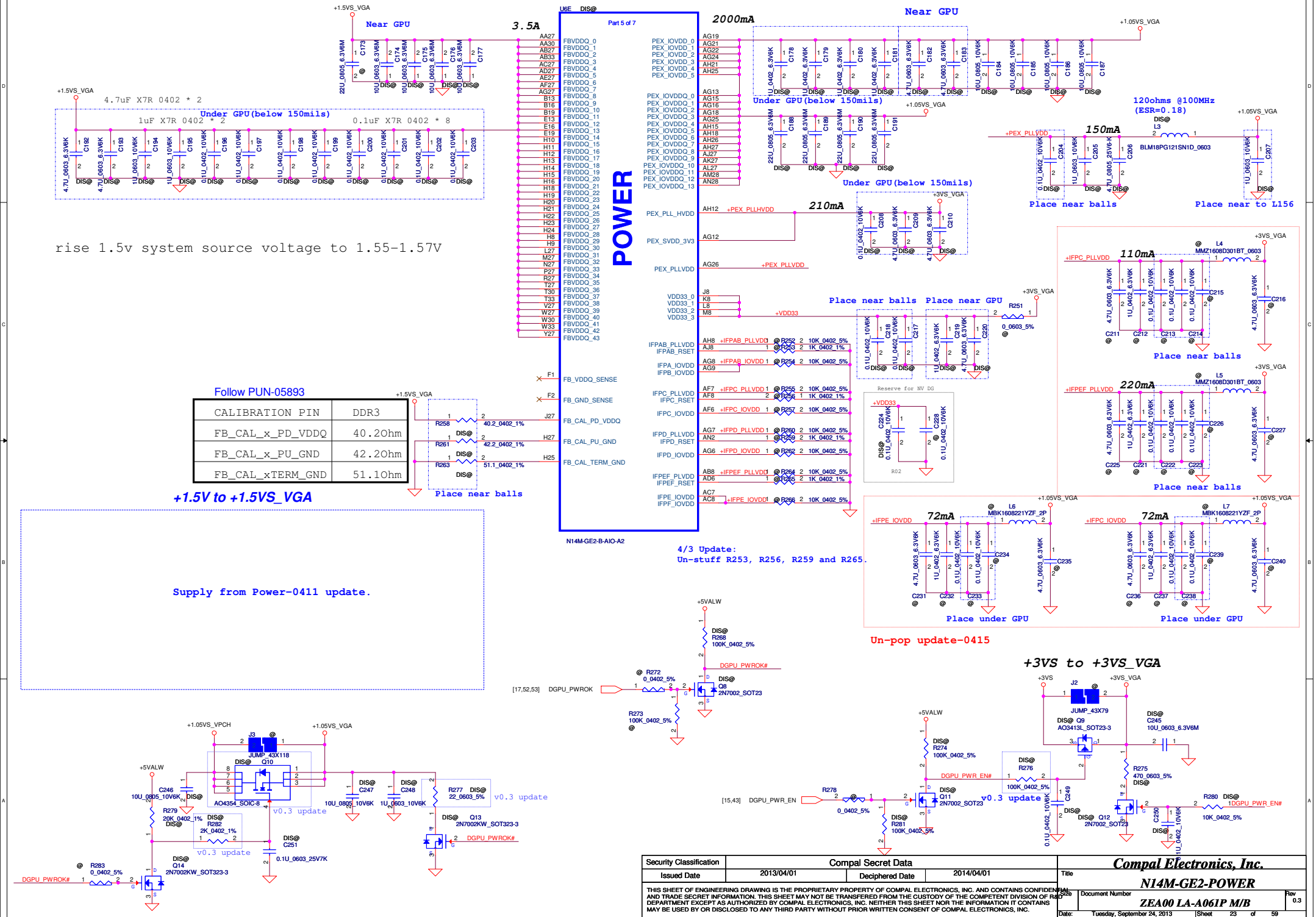
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-LVDS/HDMI/DP/THM

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 22 of 59



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

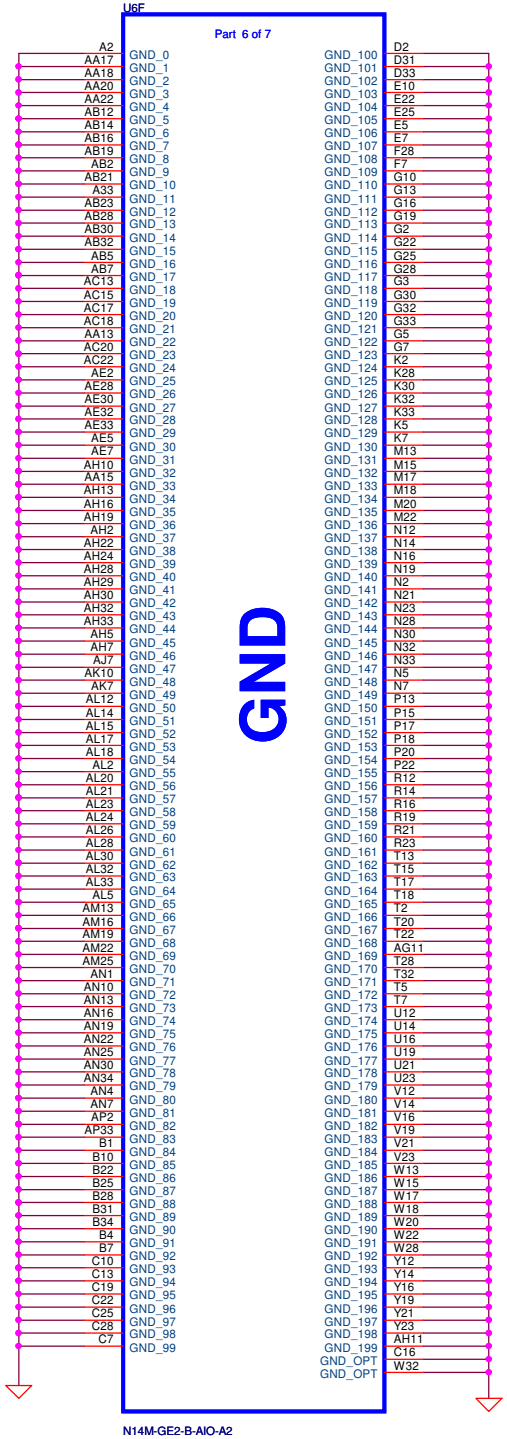
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

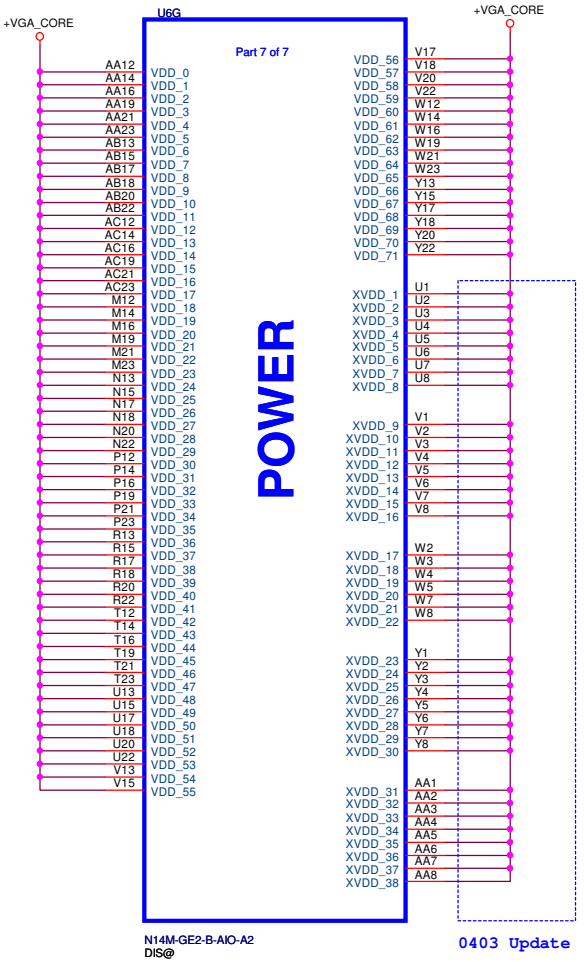
Compal Electronics, Inc.

Title: N14M-GE2-POWER

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 23 of 59





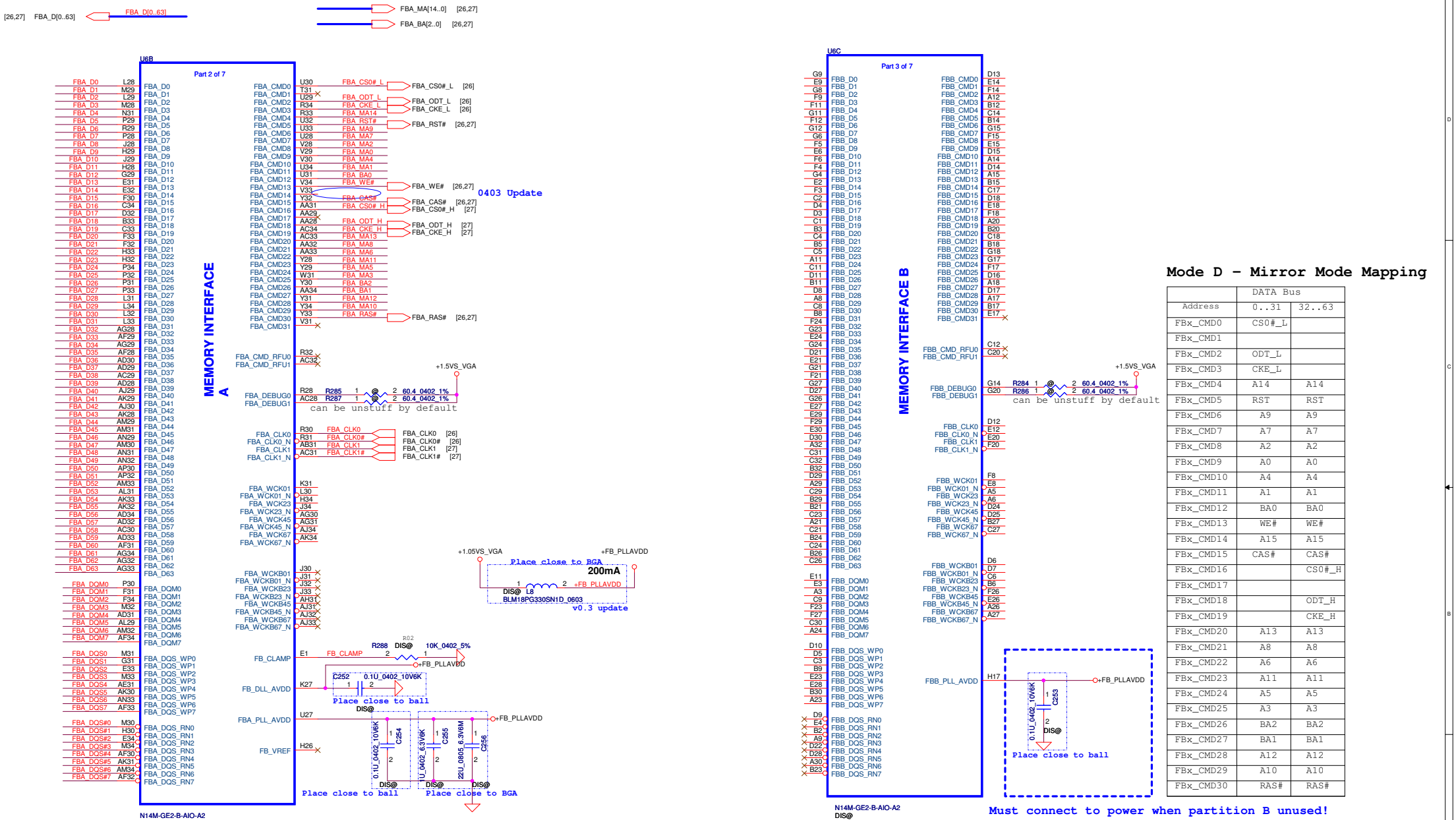
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: N14M-GE2-VGA CORE, GND

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 24 of 59



Mode D – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

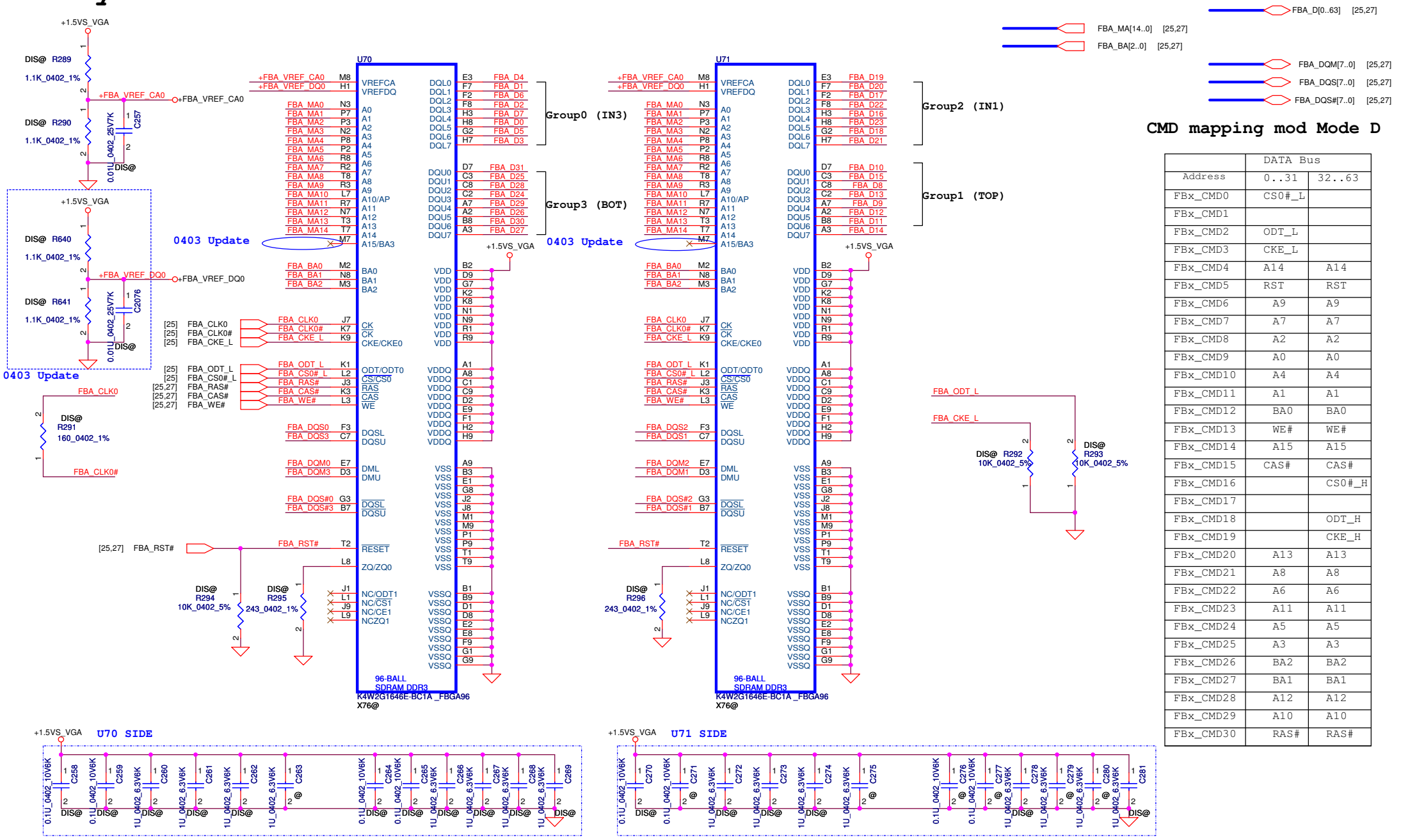
Compal Electronics, Inc.

Title: **N14M-GE2-MEM Interface**

Size	Document Number	Rev
	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 Sheet 25 of 59

Memory Partition A - Lower 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

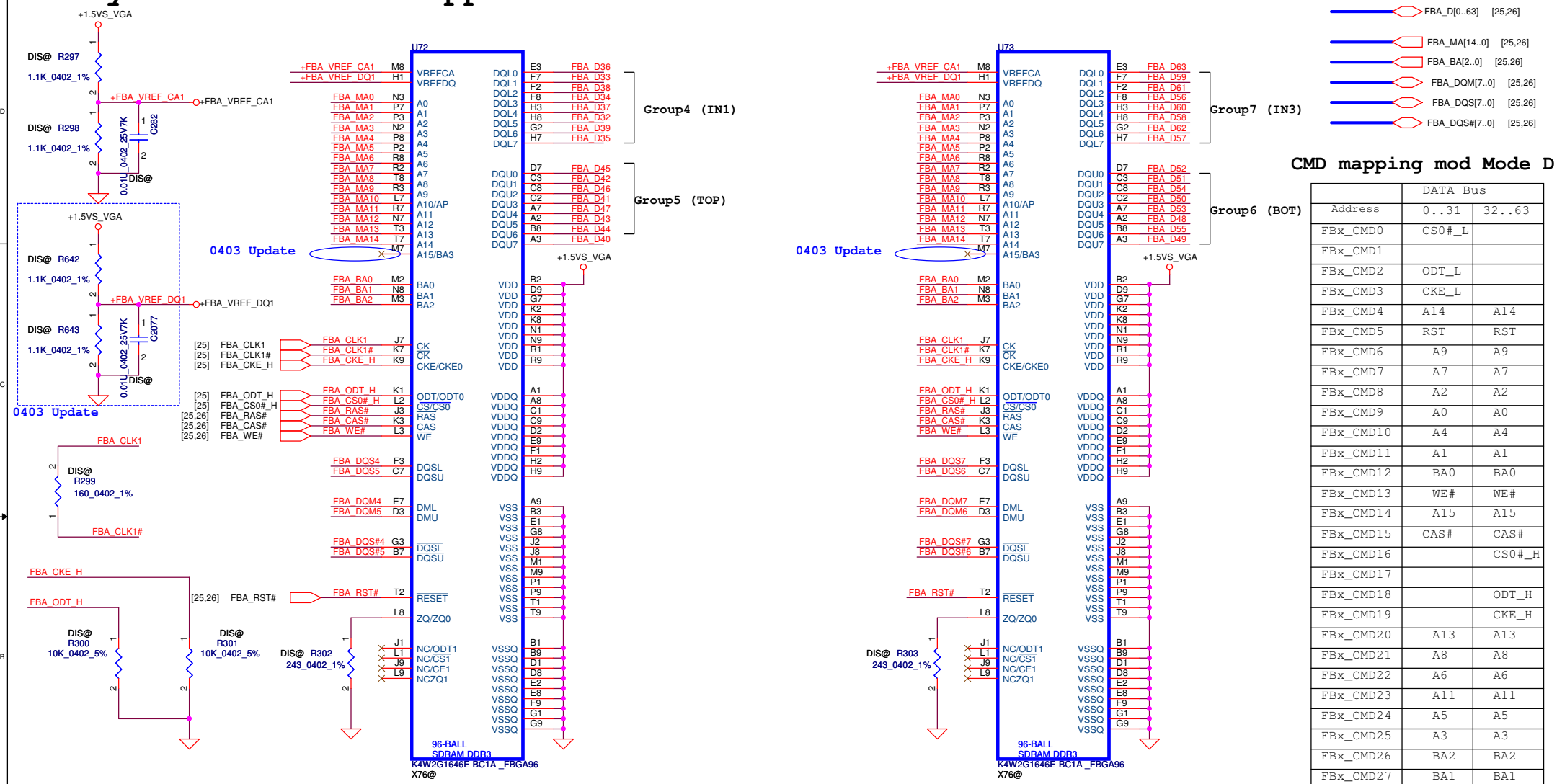
Compal Electronics, Inc.

Title: N14M-GE2-VRAM A Lower

Size | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

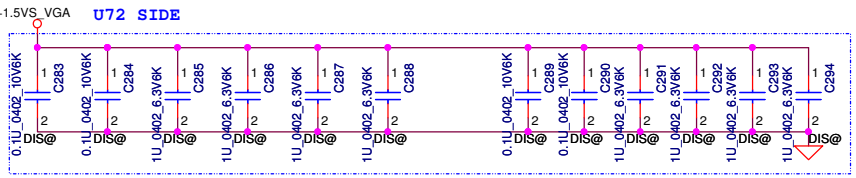
Date: Tuesday, September 24, 2013 | Sheet 26 of 59

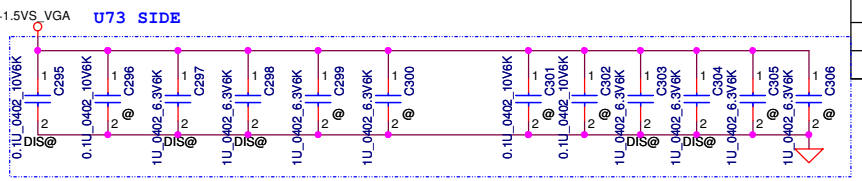
Memory Partition A – Upper 32 bits



CMD mapping mod Mode D

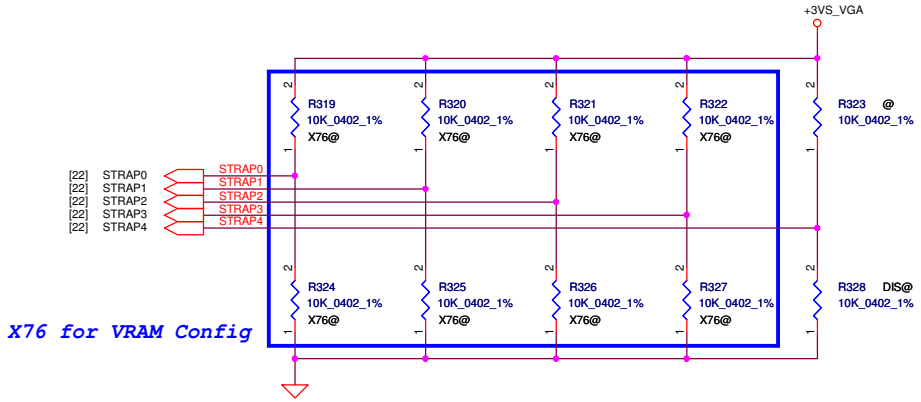
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



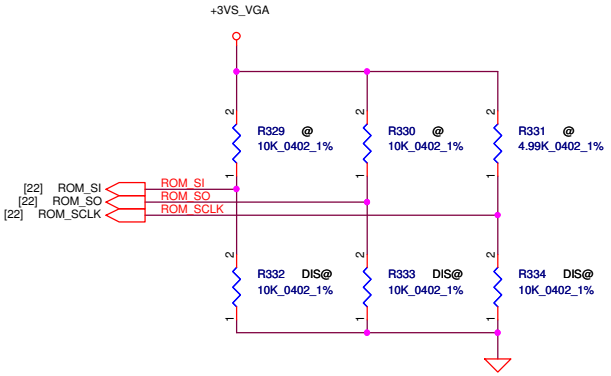


Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.	
Title	N14M-GE2-VRAM A Upper
Size	Document Number: ZEA00 LA-A061P M/B
Rev	0.3
Date: Tuesday, September 24, 2013	Sheet 27 of 59



X76 for VRAM Config



[PUN-06026-001]

Table 4. Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note
STRAP1	RAM_CFG[1]	10k Ω	See Note
STRAP2	RAM_CFG[2]	10k Ω	See Note
STRAP3	RAM_CFG[3]	10k Ω	See Note
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

[VRAM Config-RVL-06366-001]

GPU	Frenq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0
N14M-GE2	900 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BFR-11C SA00003YO10	0 R327 PD 10K	1 R321 PU 10K	1 R320 PU 10K	0 R324 PD 10K
			Samsung (0x5) K4W2G1646E-BC11 SA00005SH00	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Micron (0x1) MT41J128M16JT-107G:K SA00005SM30	0 R327 PD 10K	0 R326 PD 10K	0 R325 PD 10K	1 R319 PU 10K
N14M-GE2	900 MHz	256M* 16* 4 2GB	Micron (0xD) MT41K256M16HA-107G:E SA000065D20	1 R322 PU 10K	1 R321 PU 10K	0 R325 PD 10K	1 R319 PU 10K
			Samsung (0xB) K4W4G1646B-HC11 SA000068R10	1 R322 PU 10K	0 R326 PD 10K	1 R320 PU 10K	1 R319 PU 10K
			Hynix (0x4) H5TC4G63AFR-11C SA00006E800	0 R327 PD 10K	1 R321 PU 10K	0 R325 PD 10K	0 R324 PD 10K

Compal Electronics, Inc.			
Title: N14M-GE2_MISC			
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 28 of 59		

Power Consumption:

Pin 22 (PVCC) < 50 mA
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)

Pin5 (DPV33) < 20mA

Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)

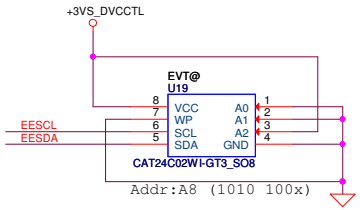
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 43 (VCCK) < 50mA
Pin 11 (DPV12) < 100mA

v0.2 update

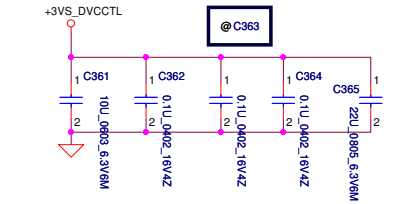
SE070104Z80
S CER CAP .1U 16V Z Y5V 0402
S CER CAP .1U 16V Z Y5V 0402

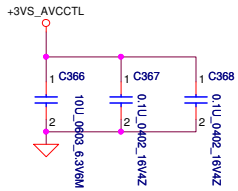
v0.2 update

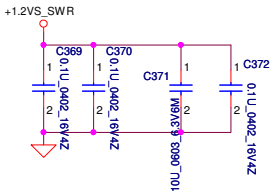
Vendor suggest to reserve for FW/EDID debug

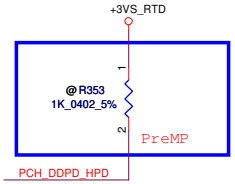


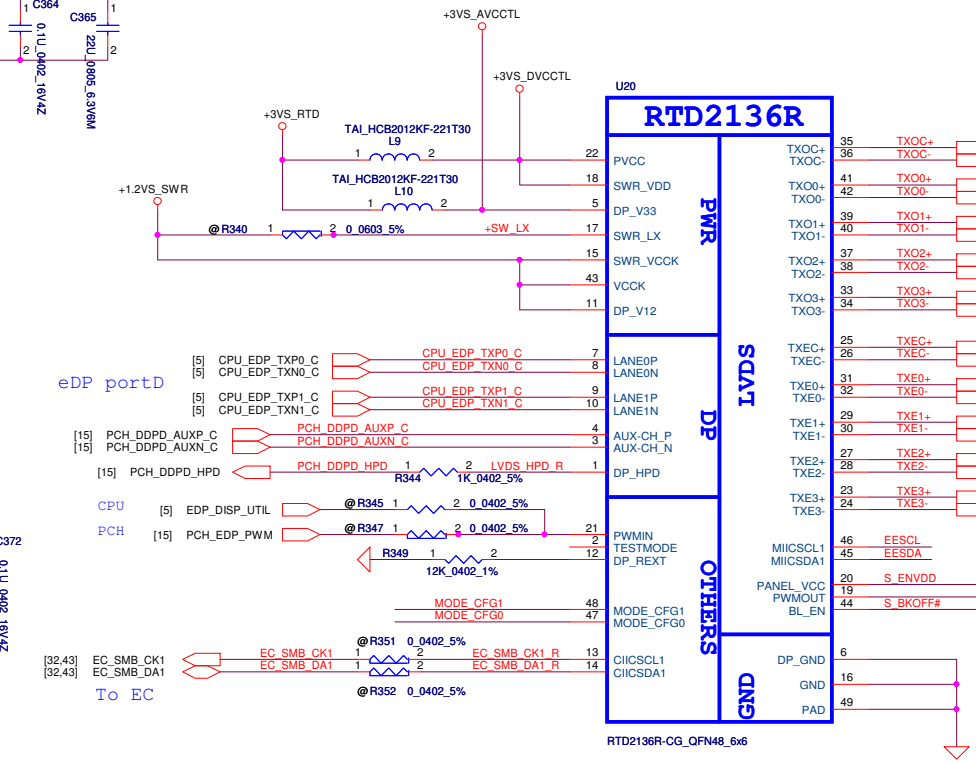
EVT Debug Only, un-pop for DVT











eDP portD

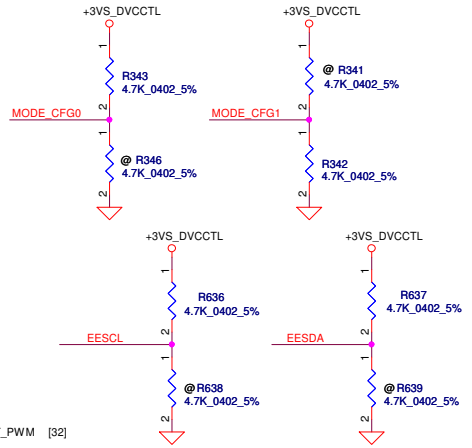
[5] CPU_EDP_TXP0_C
[5] CPU_EDP_TXN0_C
[5] CPU_EDP_TXP1_C
[5] CPU_EDP_TXN1_C
[15] PCH_DDPD_AUXP_C
[15] PCH_DDPD_AUXN_C
[15] PCH_DDPD_HPD
R344 1K_0402_5%
LVDS_HPD_R

CPU [5] EDP_DISP_UTIL
PCH [15] PCH_EDP_PWM
@R345 0_0402_5%
@R347 0_0402_5%
R349 12K_0402_1%

MODE_CFG1
MODE_CFG0

[32,43] EC_SMB_CK1
[32,43] EC_SMB_DA1
@R351 0_0402_5%
@R352 0_0402_5%
To EC

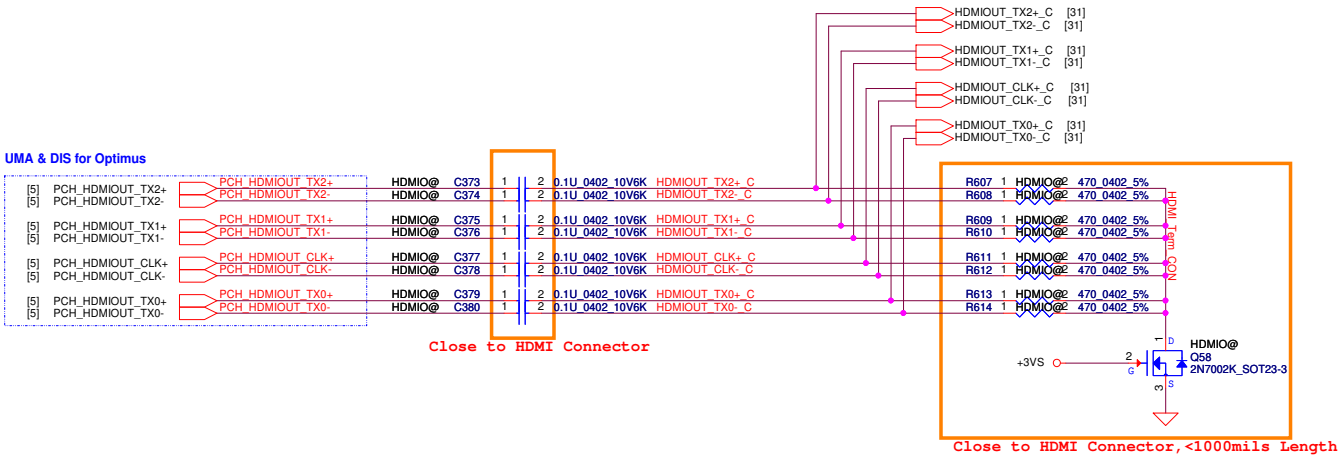
LVDS

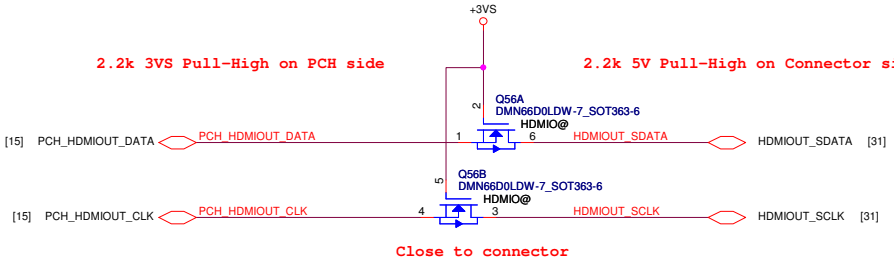


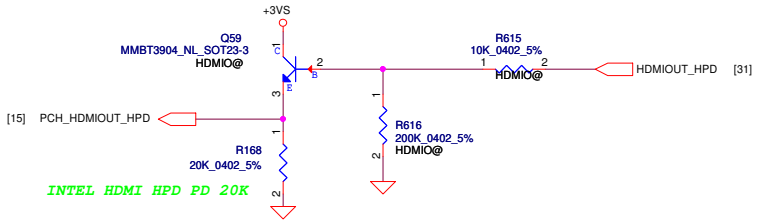
	Pin 47	
	0	1
Pin 48 0	X	EP Mode
Pin 48 1	ROM	EEPROM

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	LVDS Converter RTD2136S		
Size	Document Number	ZEA00 LA-A061P M/B	Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 29 of 59		







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

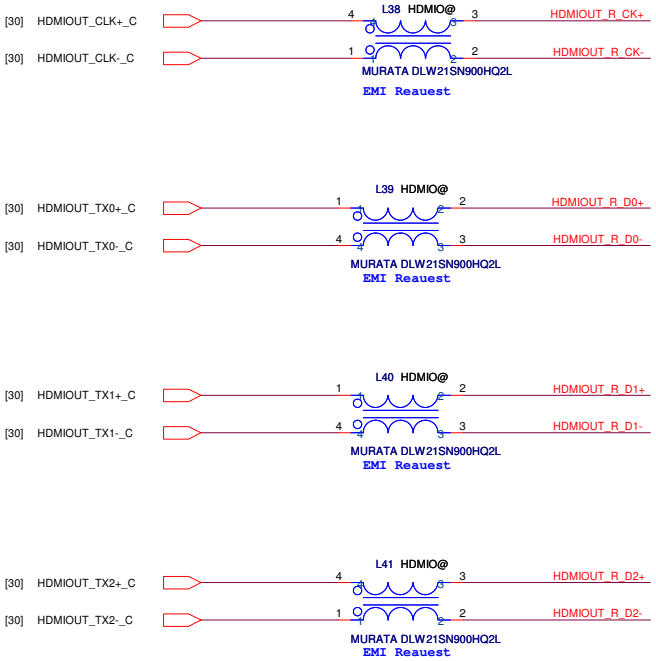
Compal Electronics, Inc.

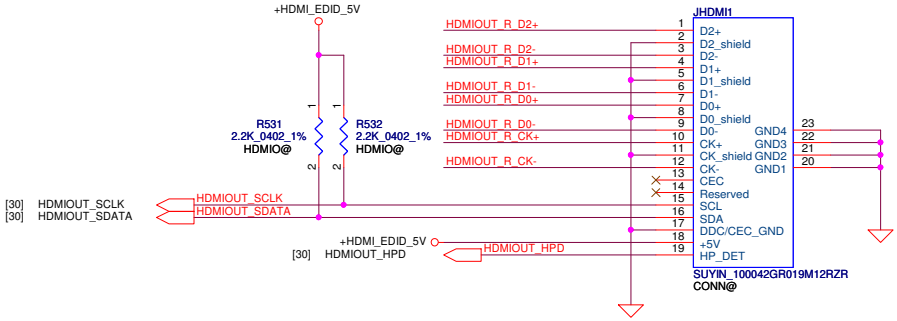
Title: ***HDMI-OUT Level Shift***

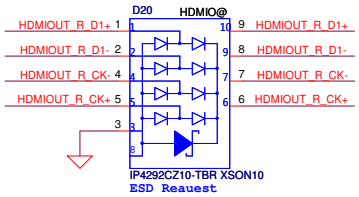
Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

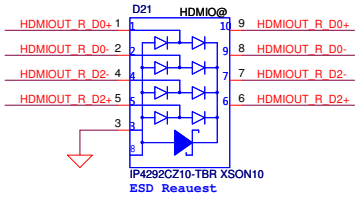
Date: Tuesday, September 24, 2013 | Sheet 30 of 59

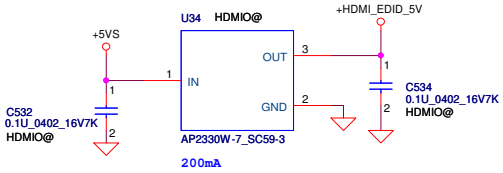
HDMI-OUT Connector

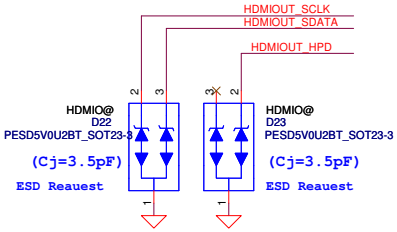












Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

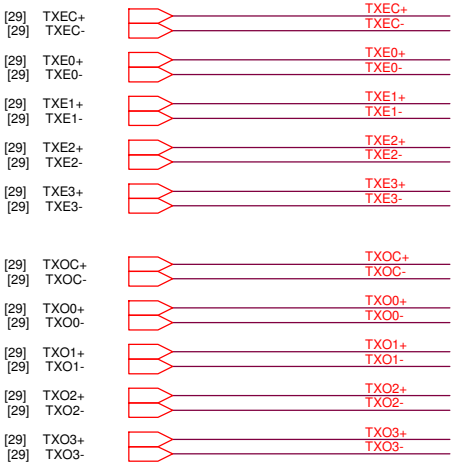
Compal Electronics, Inc.

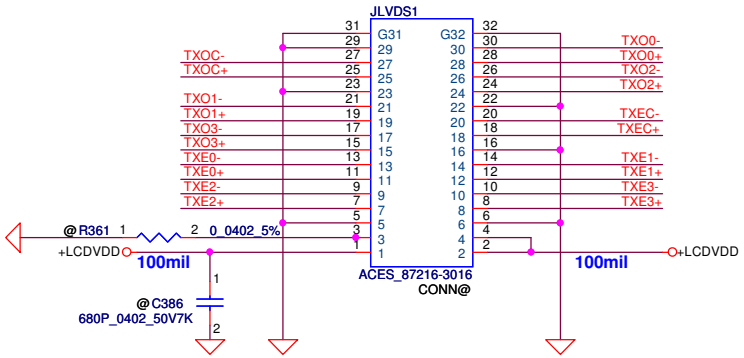
Title: HDMI-OUT

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

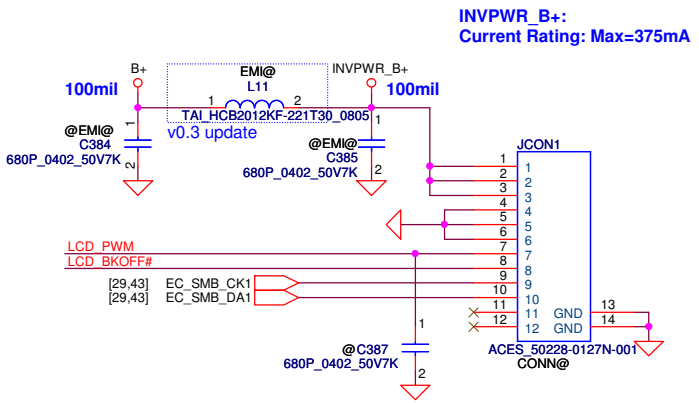
Date: Tuesday, September 24, 2013 | Sheet 31 of 59

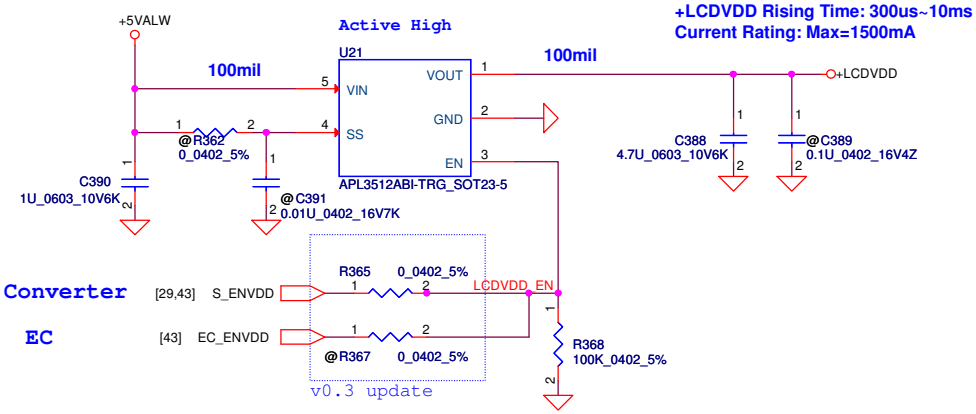
LVDS Conn.

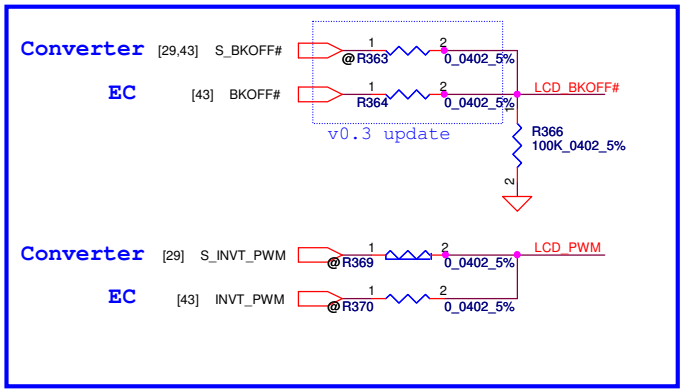




Converter

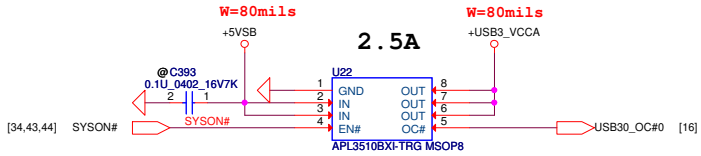


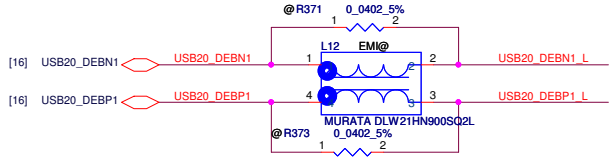


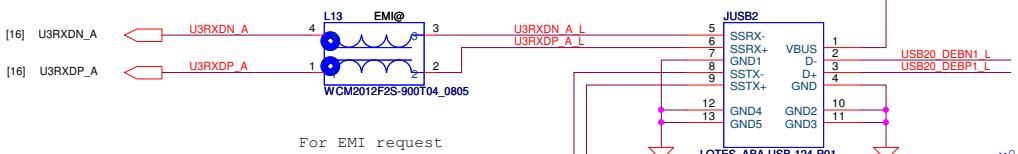


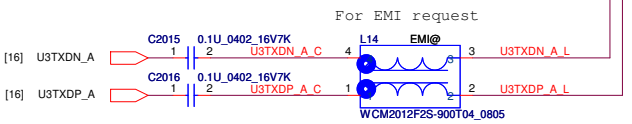
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

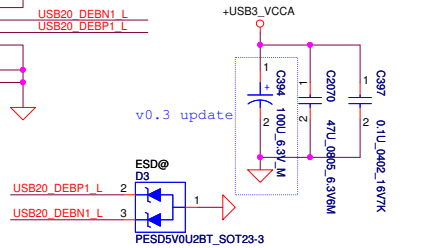
Compal Electronics, Inc.			
Title: LVDS			
Size: B	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 32 of 59		



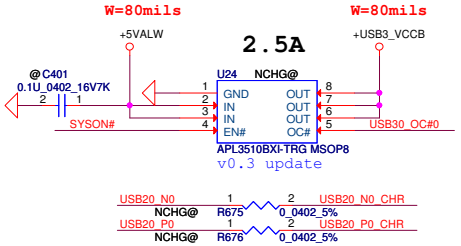




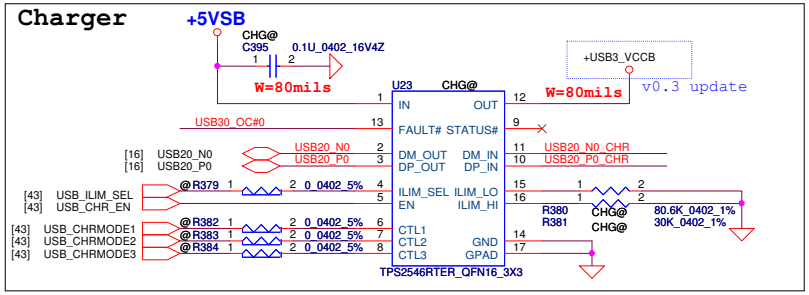


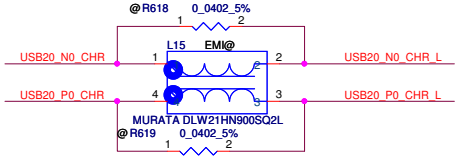


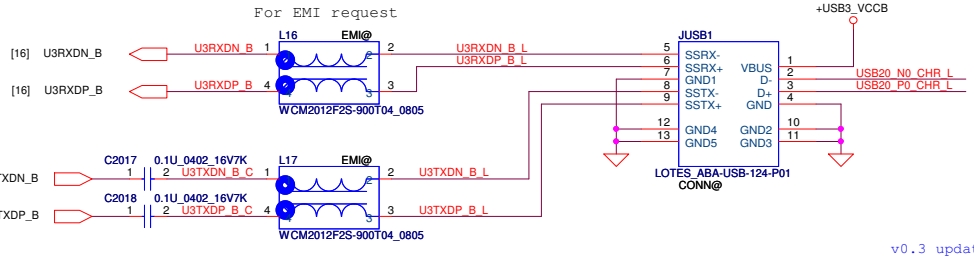
Non Changer



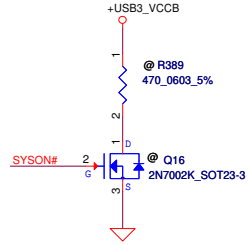
Charger

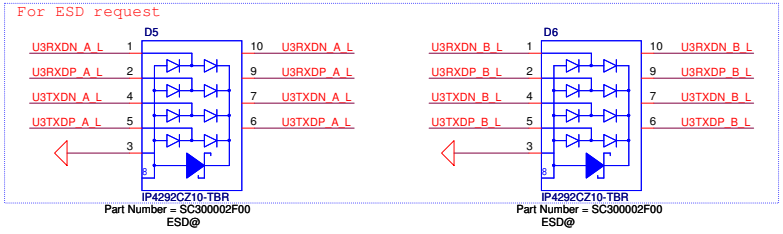






Charge USB Port





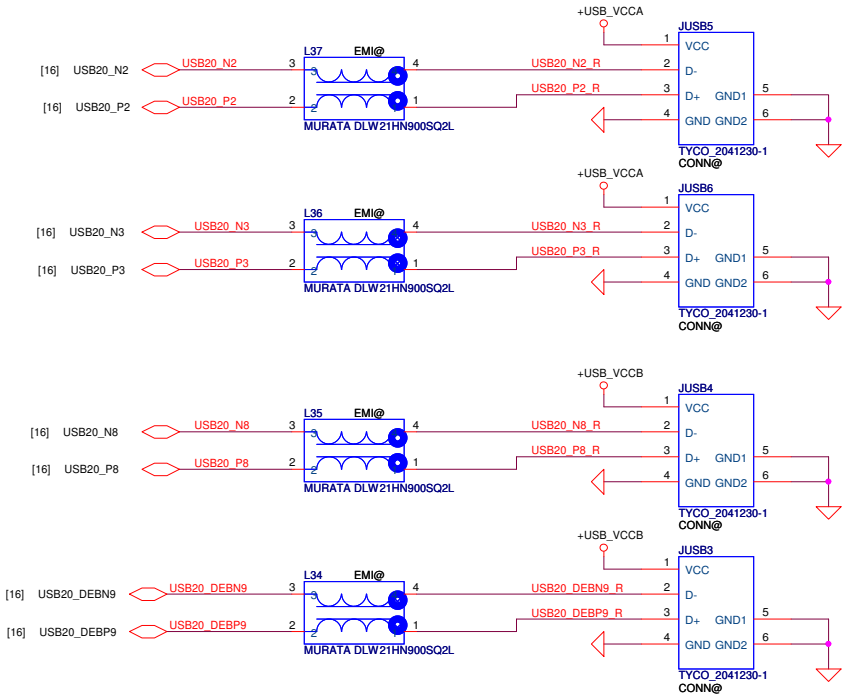
Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPXIOA07(pin104)	GPIO22(pin41)	GPXIOA11(pin108)	GPIO21(pin40)
S0(CDP)	1	1	1	1
S3(SDP)	1	1	1	0
S4/S5(DCP)	0	0	1	1

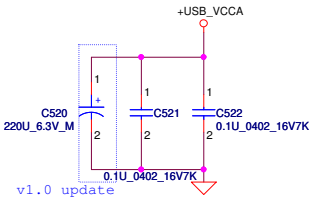
System Global Power State	TPS2546/TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S3	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake	0	0	1	1	ILIM_HI

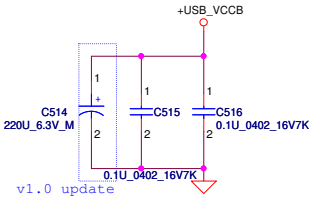
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: USB 3.0 CONN

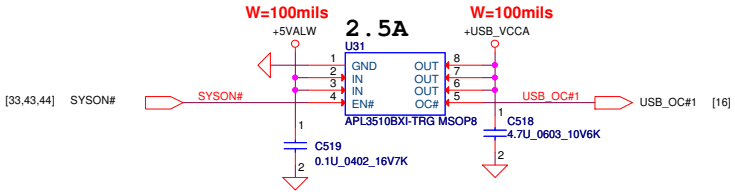
Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3
Date:	Sheet 33 of 59	

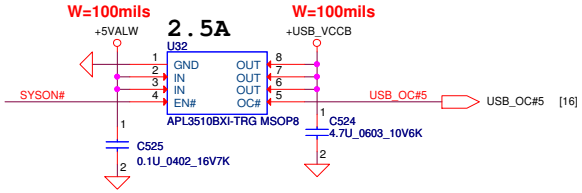
USB20



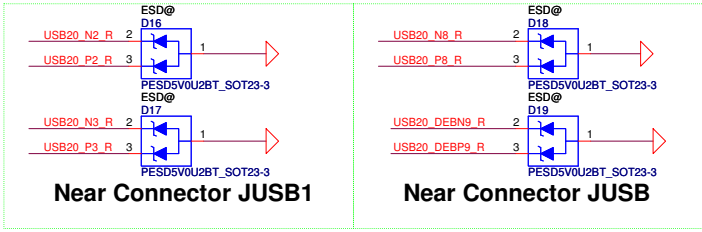


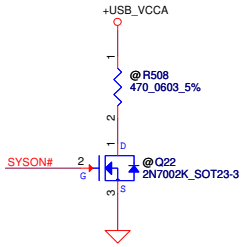


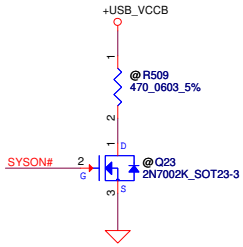




For USB2.0 ESD diode







Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

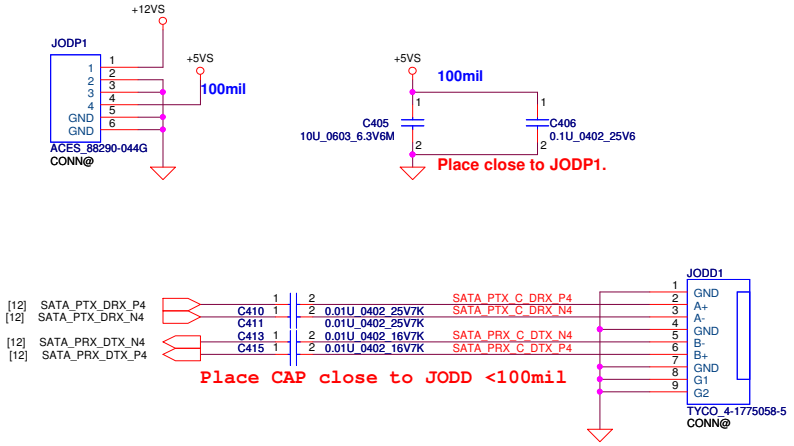
Compal Electronics, Inc.

Title: USB20

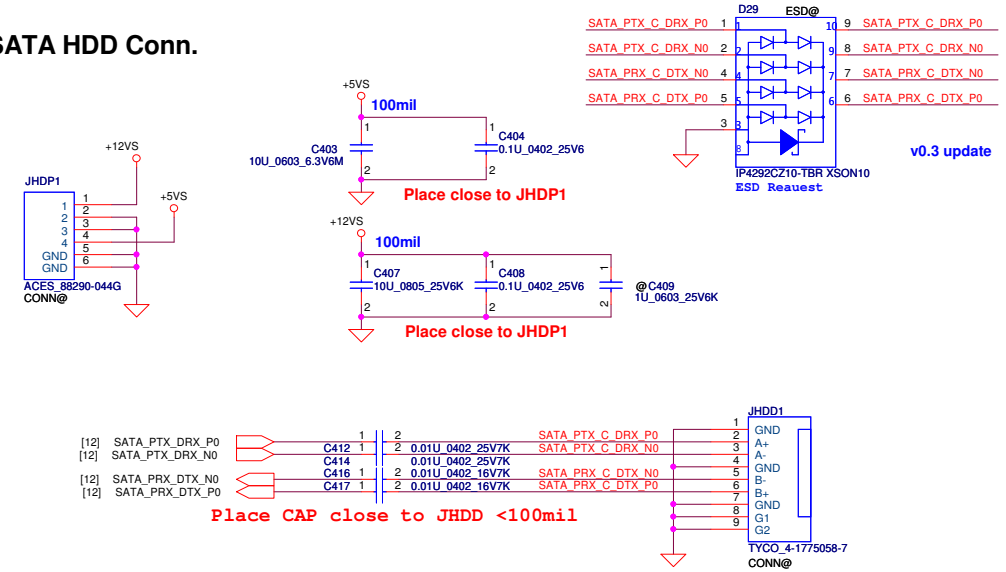
Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 | Sheet 34 of 59

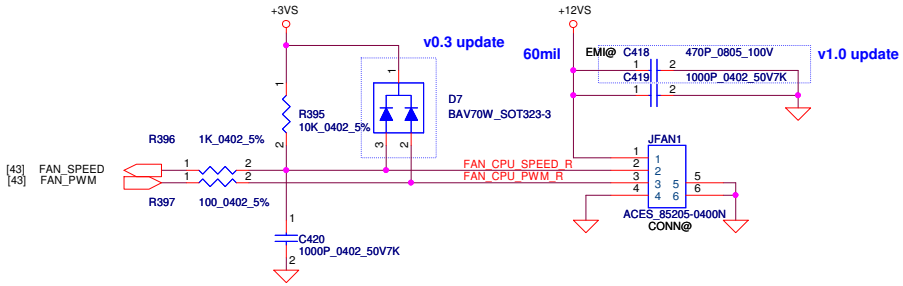
SATA ODD Conn



SATA HDD Conn.

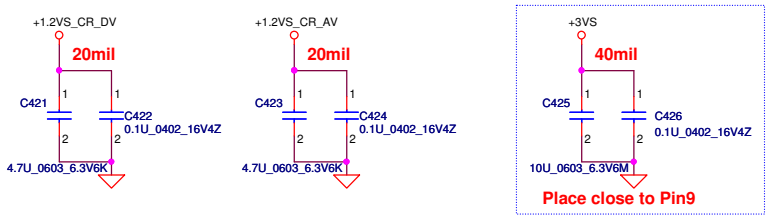


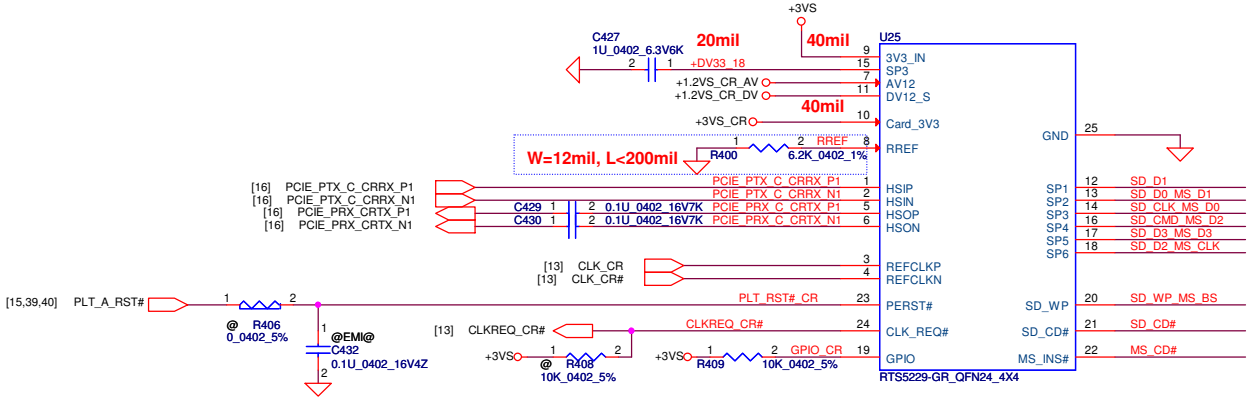
FAN Control Circuit



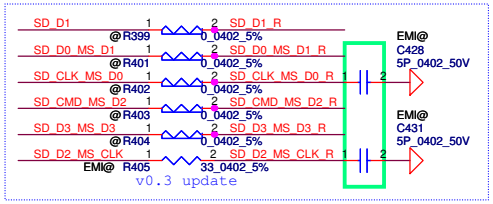
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	SATA-HDD/ODD/USB		
Size	Document Number		Rev
	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	35 of 59

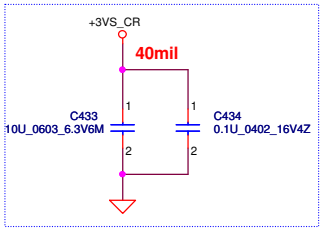


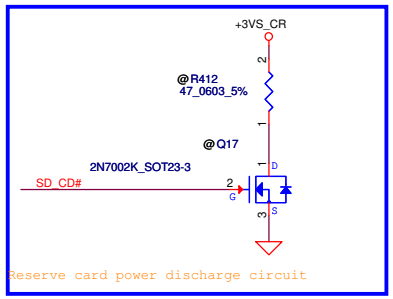


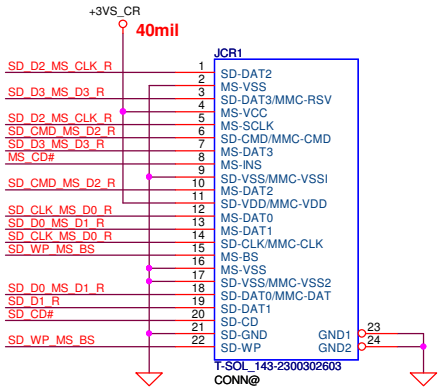
Length of per trace 2inch no more 2 via mismatch trace length <100mil 50ohm +-15% impedance.



Place close to JCR1 pin 12,21

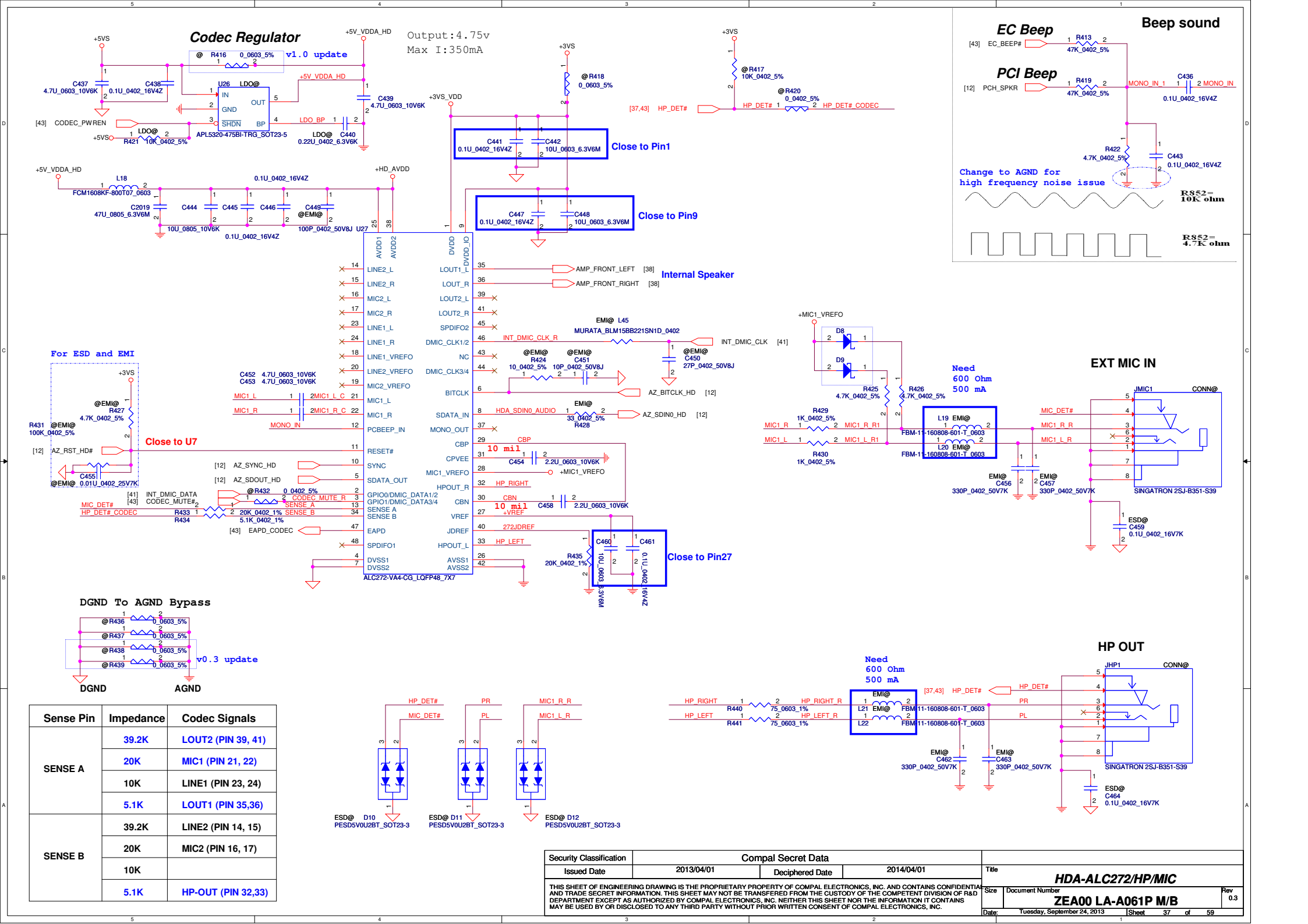






Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.		
Title: RTS5229 Media Card Controller		
Size: Custom	Document Number: ZEA00 LA-A061P M/B	Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 36 of 59	



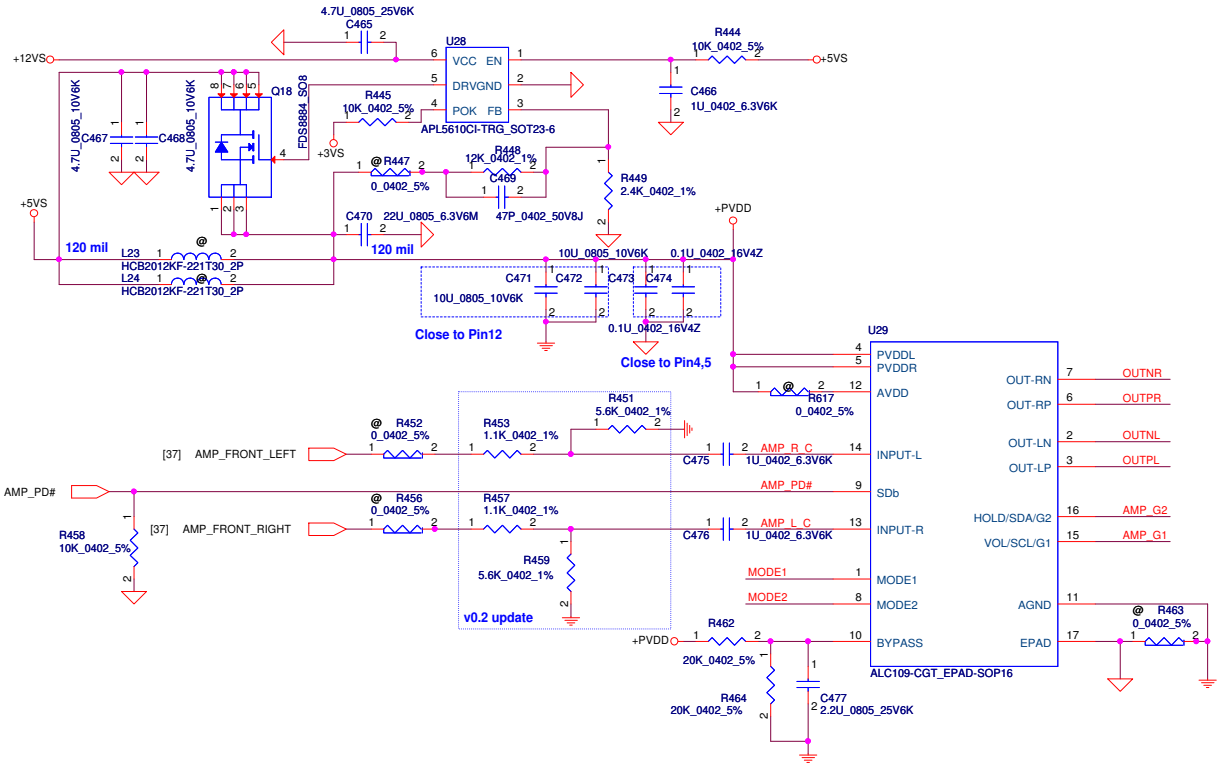
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	LOUT2 (PIN 39, 41)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	10K	
	5.1K	HP-OUT (PIN 32,33)

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

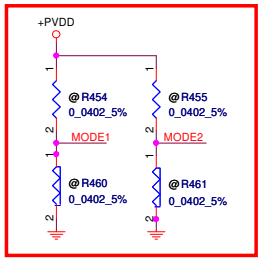
Title	HDA-ALC272/HP/MIC		
Size	Document Number		Rev
	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	37 of 59

@ESD@ C2154 1 2 0.1U_0402_16V4Z +5VS
@ESD@ C2155 1 2 0.1U_0402_16V4Z
v0.3 update

Vo=0.8(1+R606/R607)
Output:4.8V
Max I:7.5A

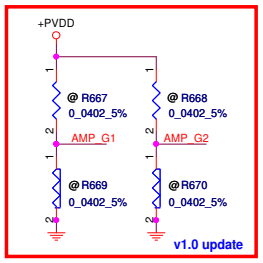


Mode selet: Fix Gain

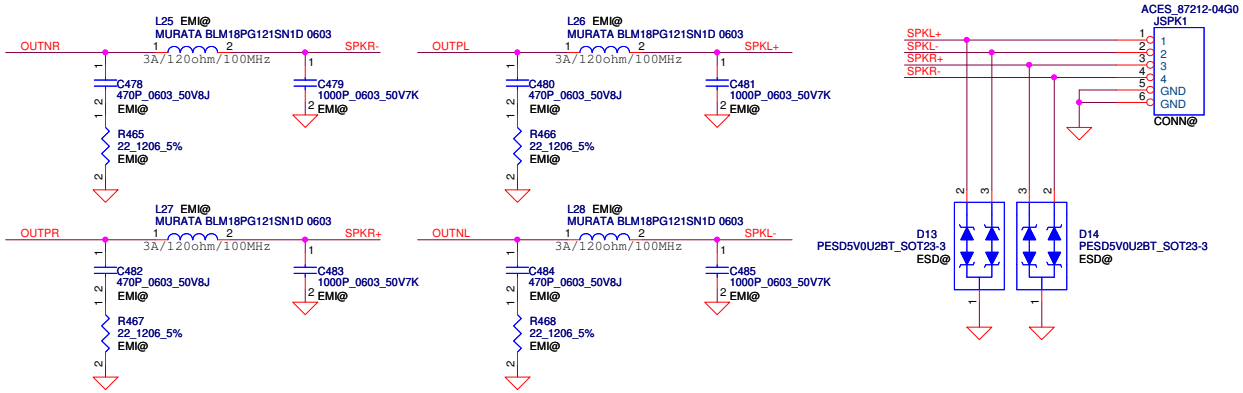


Mode1	Mode2	Option	Pin15	Pin16
0	0	Fixed Gain	G1	G2
0	1	I2C	SCL	SDA
1	0	PWM	PWM	Hold
1	1	DC	DC	Hold

Gain Select



AMP_G1	AMP_G2	Gain	
0	0	11dB	(Default)
0	1	14dB	
1	0	19dB	
1	1	25dB	



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: AMP

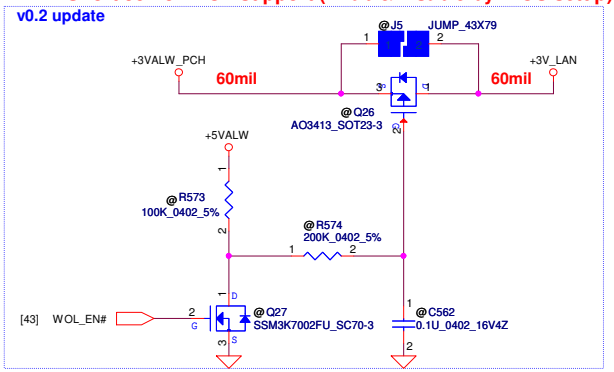
Size: Custom | Document Number: ZEA00 LA-A061P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 38 of 59

WOL circuit

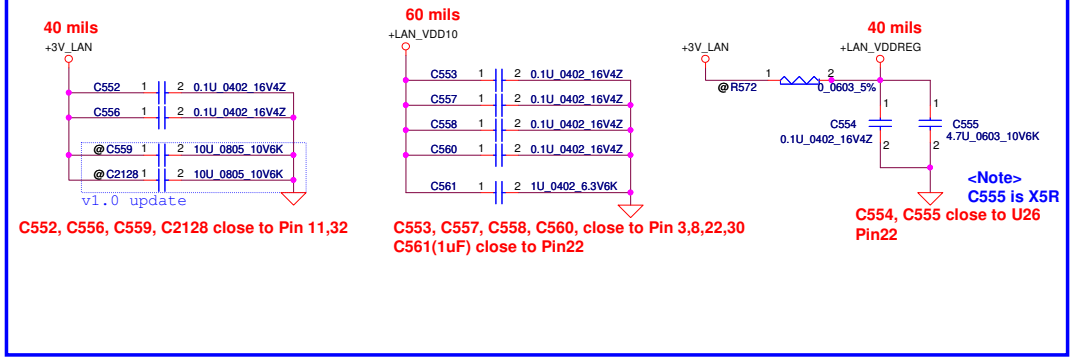
Short J5 for WOL support (Enable/Disable by BIOS setup)

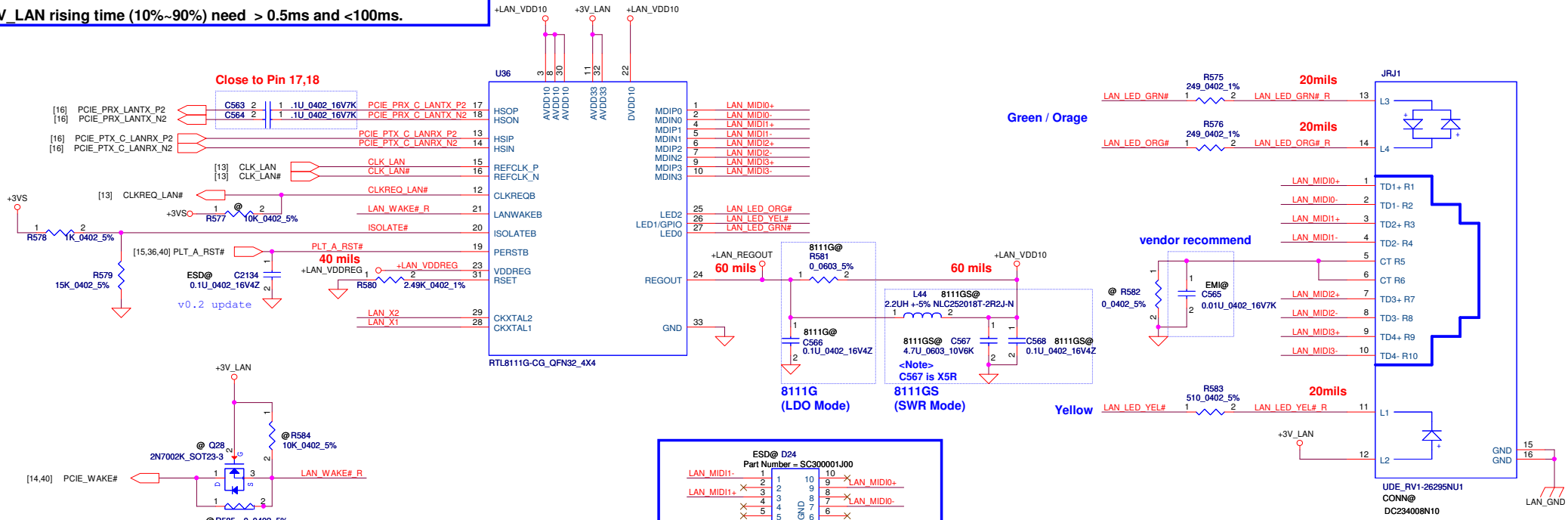
v0.2 update

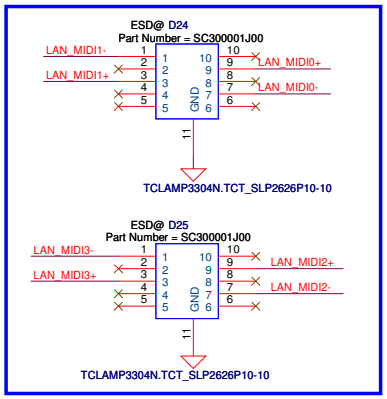


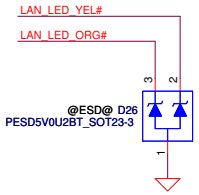
+3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

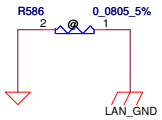
Power (Decoupling Cap.)



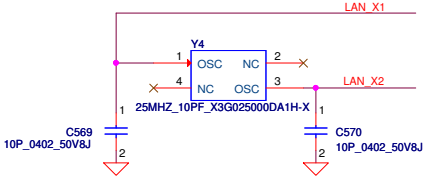








Crystal



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

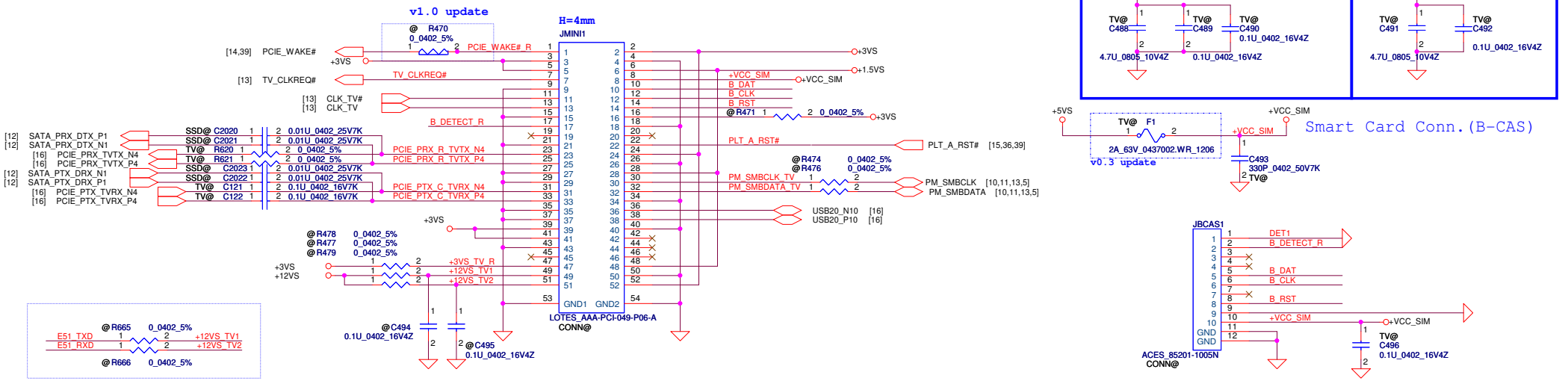
Title: LAN RTL8111G

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

Date: Tuesday, September 24, 2013 Sheet 39 of 59

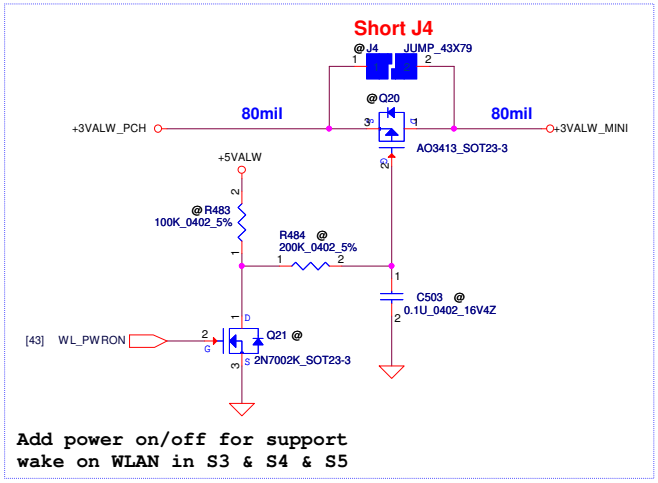
MINI (TV) /m-SATA SSD

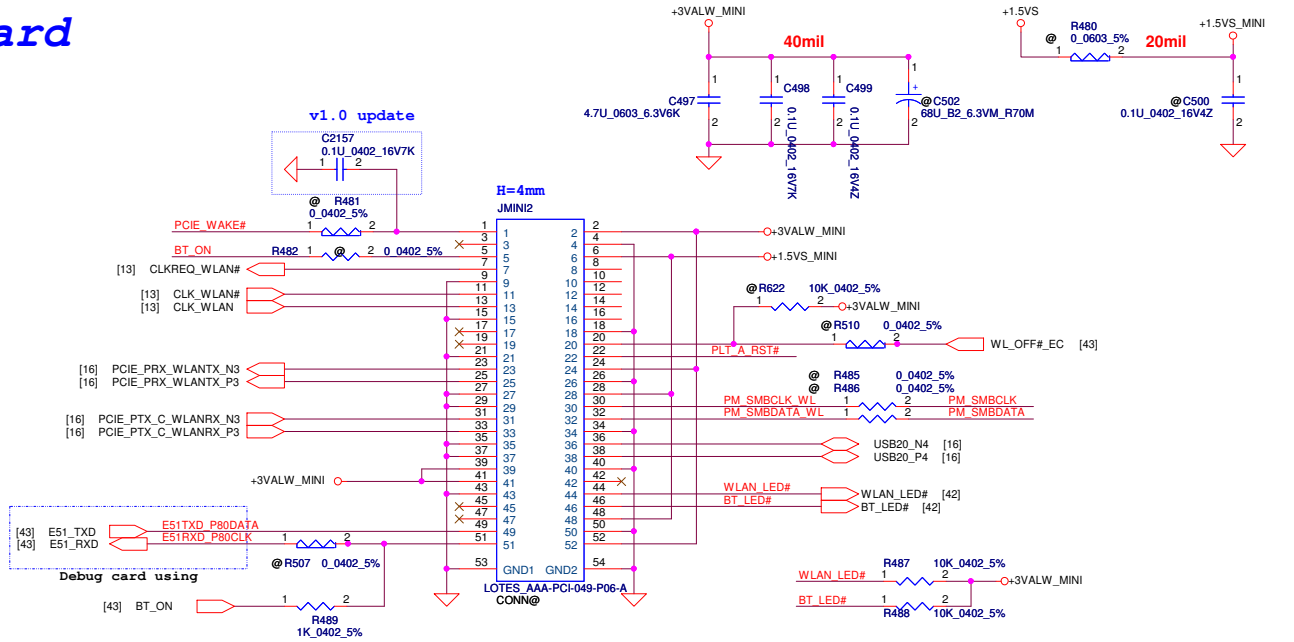
Mini Card Slot 1---TV tuner Current: +3VS : 2750mA, 1.5V: 500mA



WLAN & Bluetooth Combo Card

Mini Card Slot 2--- WLAN Current: 3.3 : 750mA,

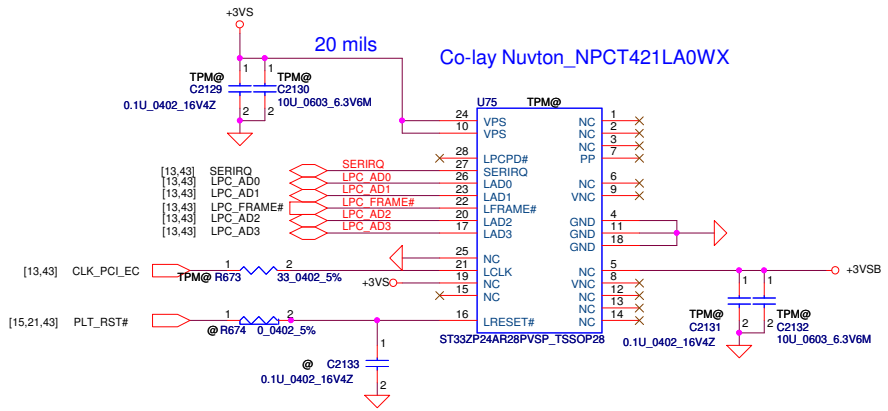




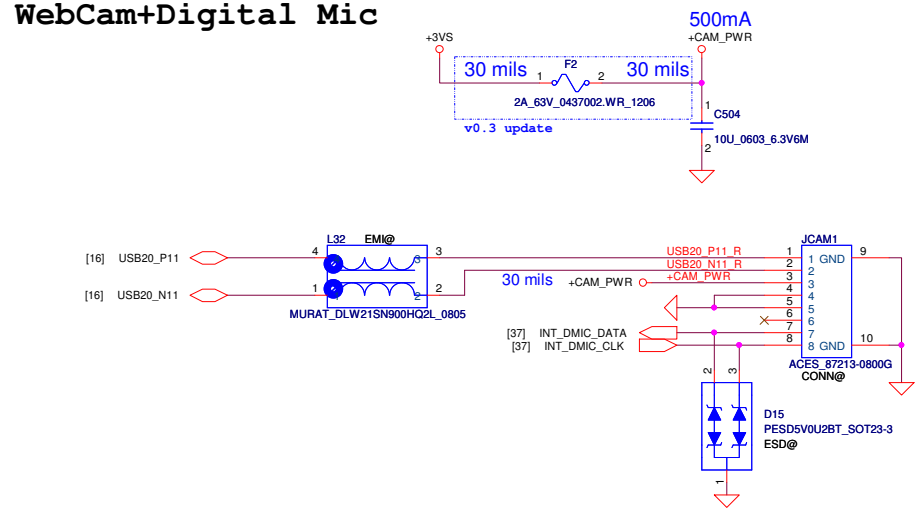
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Title	PCIe-WLAN/TV_B-CAS		
Size	Document Number		Rev
	ZEA00 LA-A061P M/B		0.3
Date:	Tuesday, September 24, 2013	Sheet	40 of 59

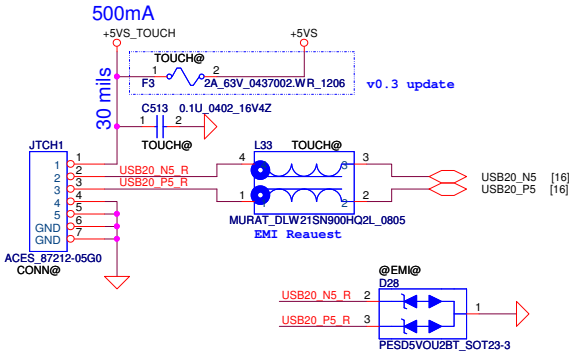
TPM(Reserve)



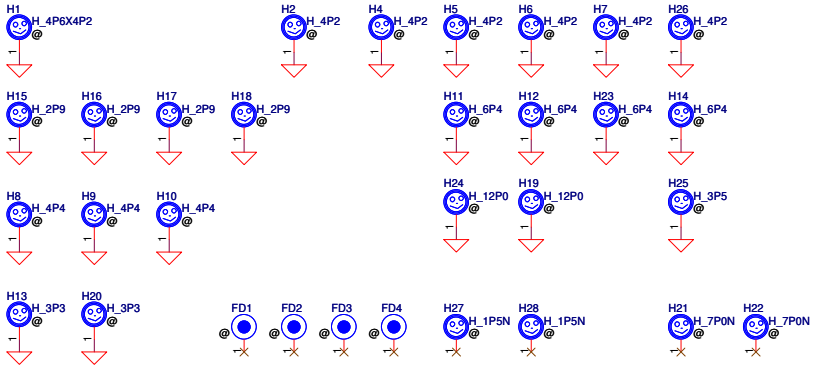
WebCam+Digital Mic



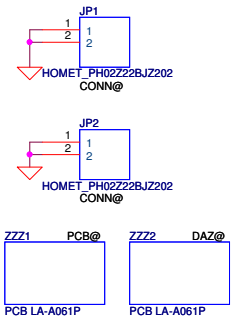
Touch



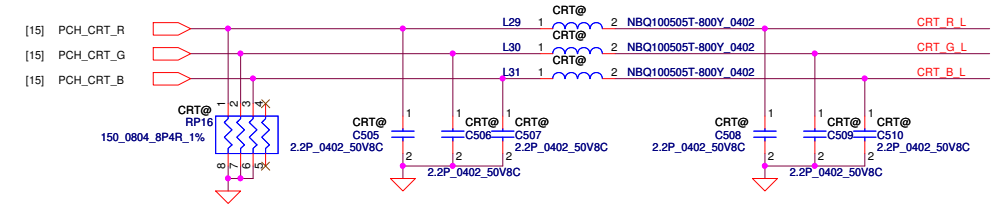
Screw Hole



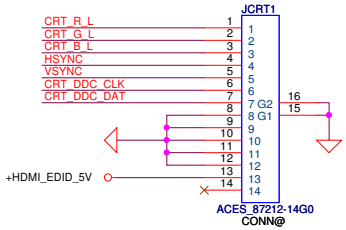
PCH heat sink

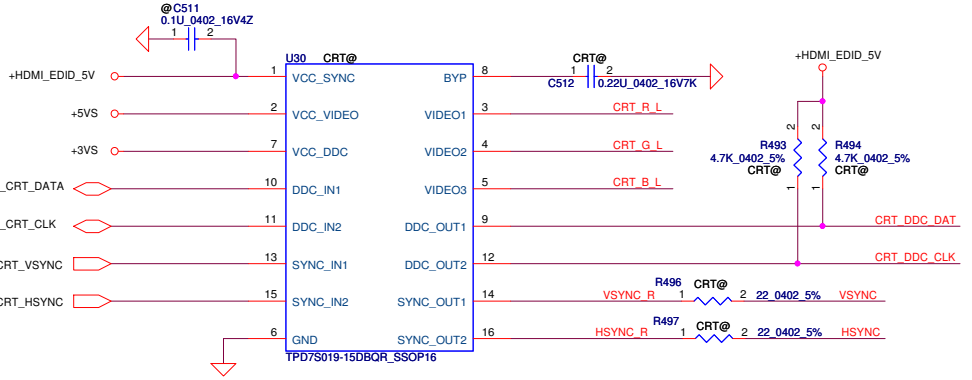


CRT Conn(Reserve 15pin)



Need PU/PL on PCH/FCH side
(2.2K*2pcs for DDC & 150_8P4R*1pcs for RGB)



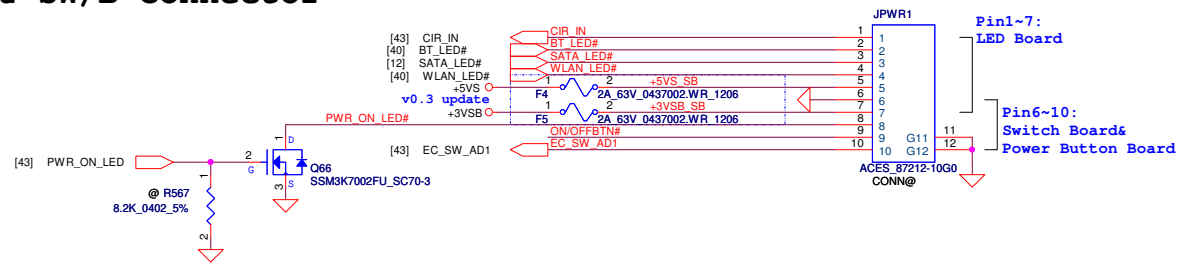


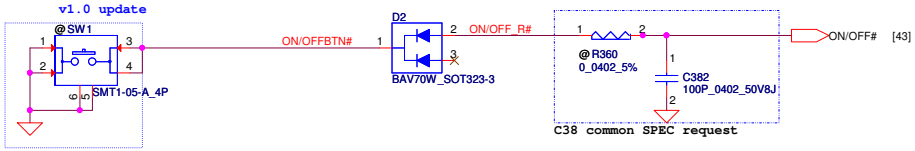
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

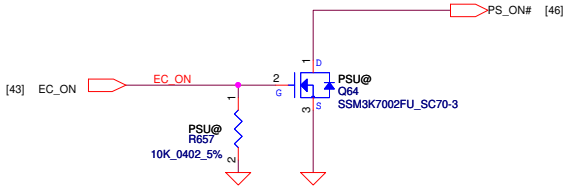
Title	PWR/Cap./TP/LED/LP/LS/Screw		
Size	Document Number	ZEA00 LA-A061P M/B	Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 41 of 59		

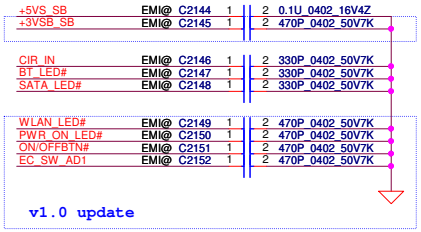
Power/B & SW/B Connector

8Pin sub-board Conncetor

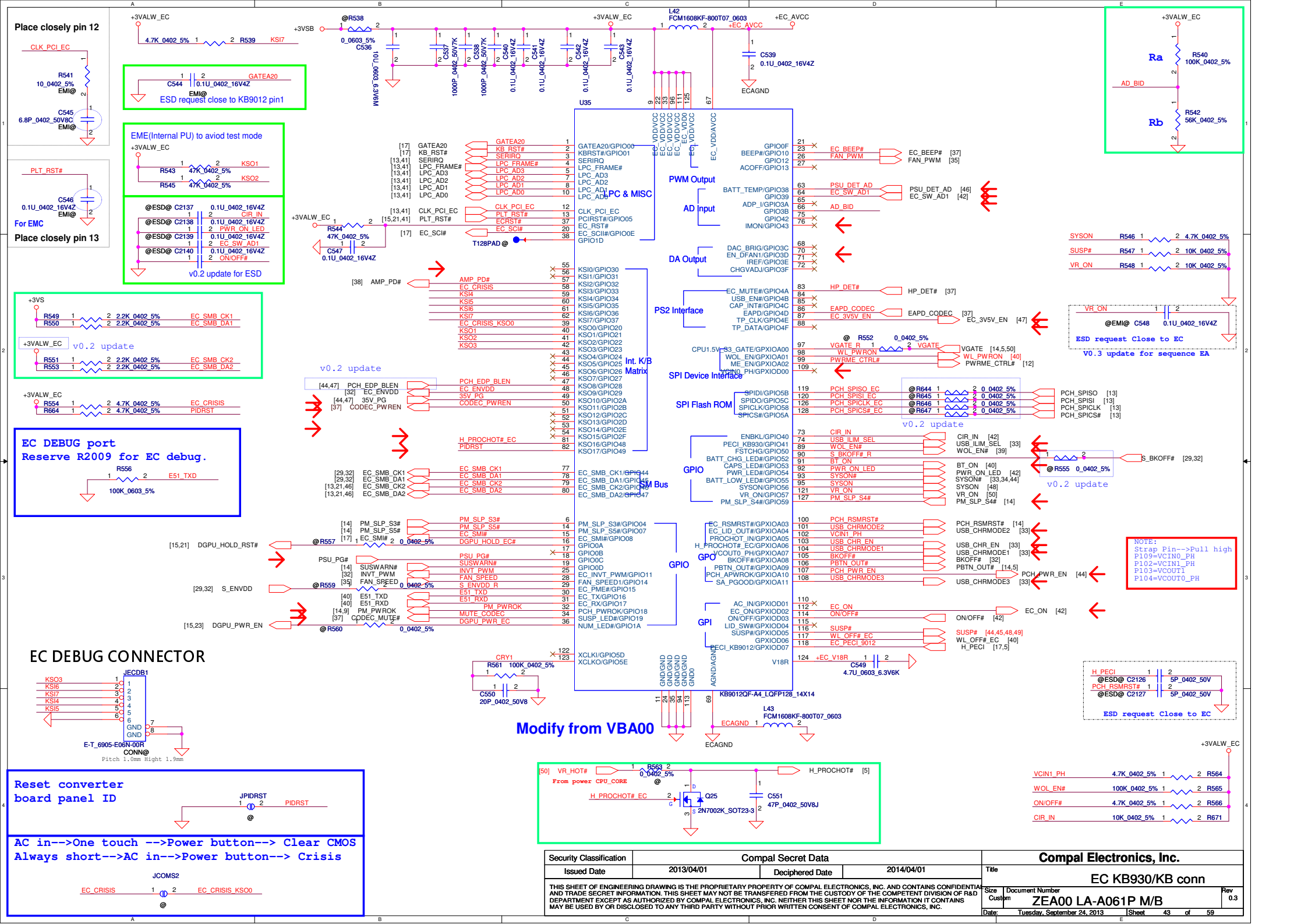








Compal Electronics, Inc.			
Title	Sub-board Connector		
Size: Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 42 of 59		



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

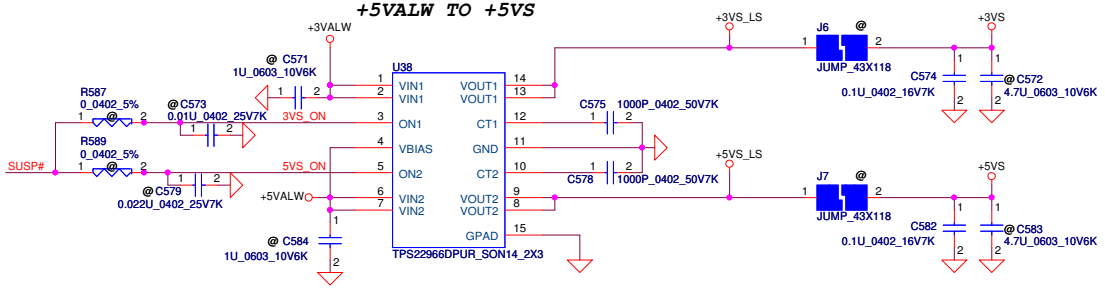
Title: EC KB930/KB conn

Size	Document Number	Rev
Custom	ZEA00 LA-A061P M/B	0.3

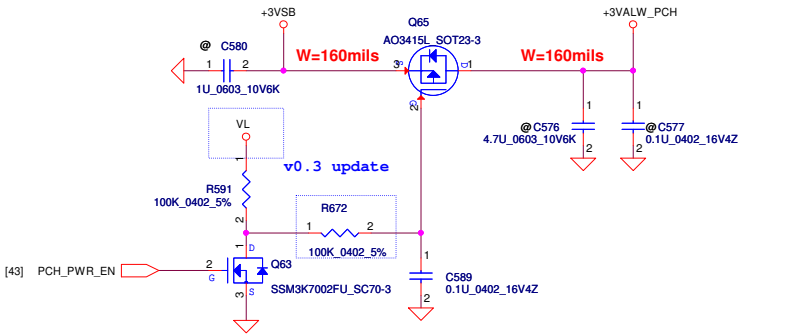
Date: Tuesday, September 24, 2013 | Sheet 43 of 59

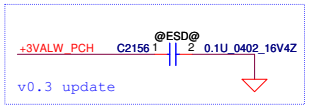
+3VALW TO +3VS
+5VALW TO +5VS

Vgs=10V, Id=9A, Rds=18.5mohm



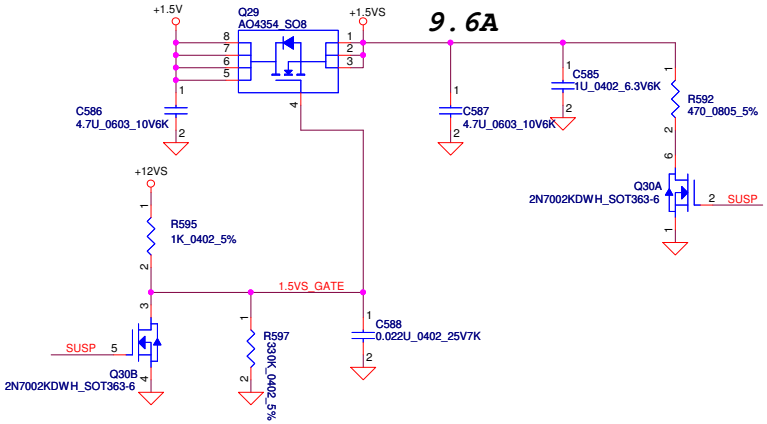
+3VALW TO +3VALW_PCH

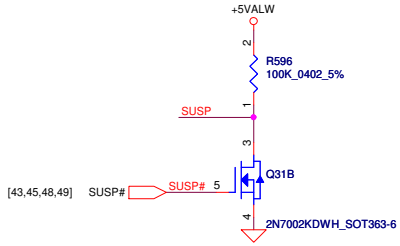




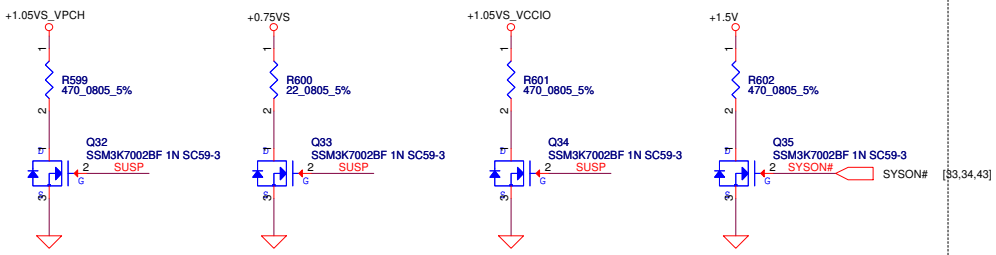
+1.5V to +1.5VS

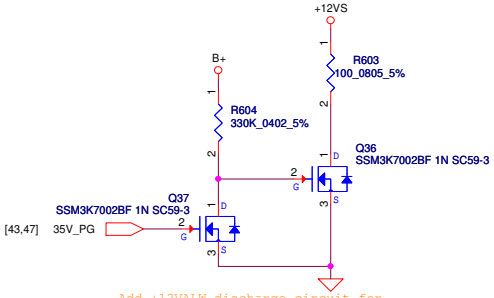
9.6A





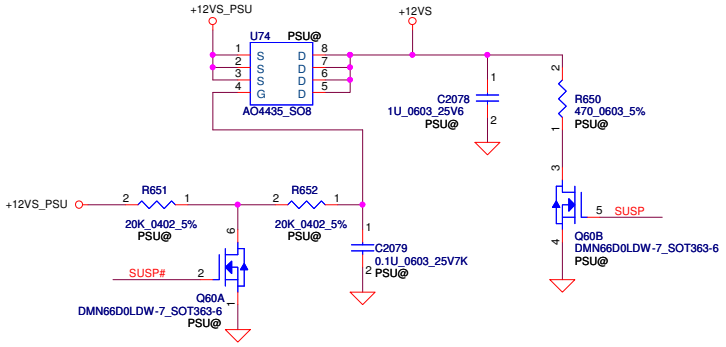
Discharge circuit





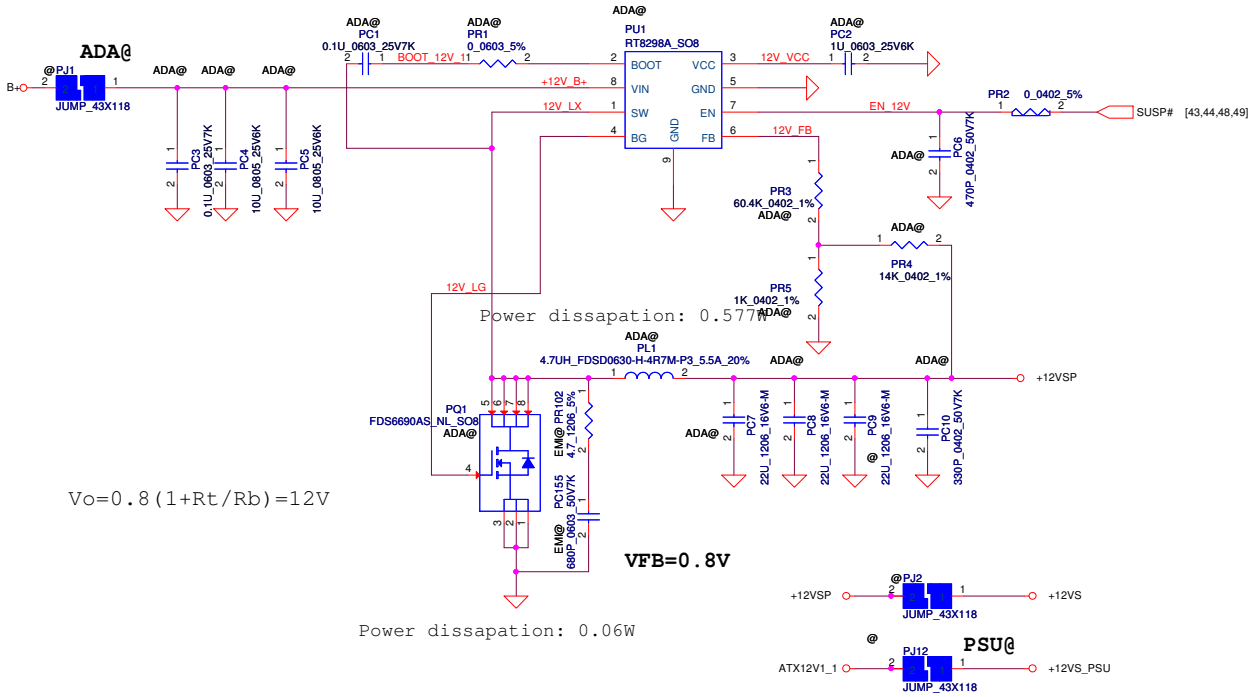
Add +12VALW discharge circuit for prevent DC plug in leakage 5/5.

+12V1 TO +12VS (Reserve for PSU)



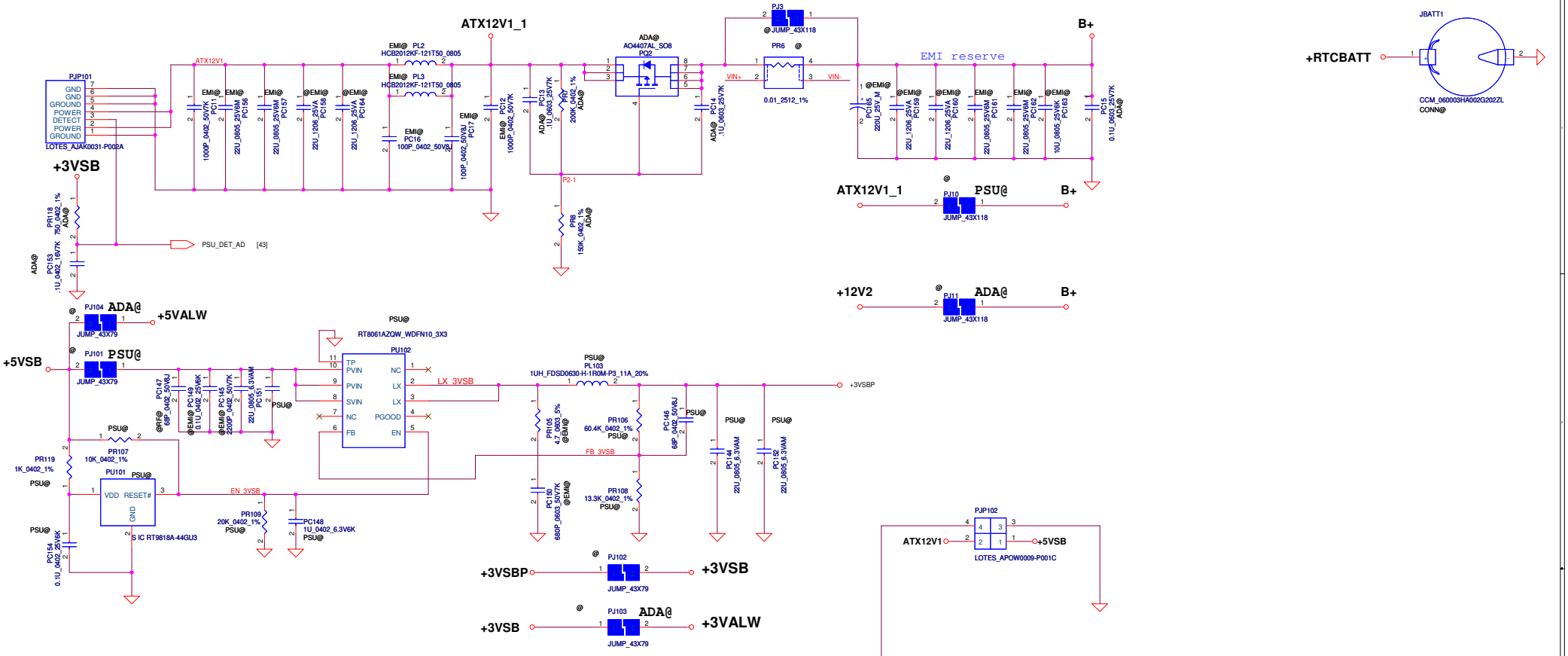
Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

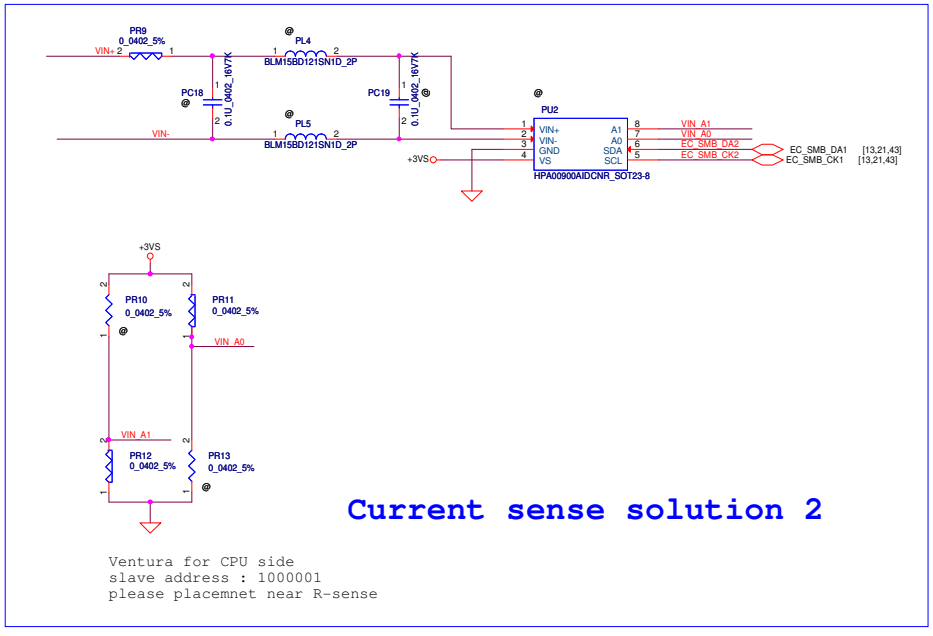
Compal Electronics, Inc.			
Title	DC-DC INTERFACE		
Size	Document Number ZEA00 LA-A061P M/B		Rev 0.3
Date: Tuesday, September 24, 2013	Sheet 44 of 59		



Security Classification	Compal Secret Data		
Issued Date	2012/04/27	Deciphered Date	2013/04/27

Compal Electronics, Inc.			
Title: PWR- 12VSP			
Size: Custom	Document Number: VBA11 LA-A111 M/B		Rev: 0.1
Date: Tuesday, September 24, 2013	Sheet 45 of 56		





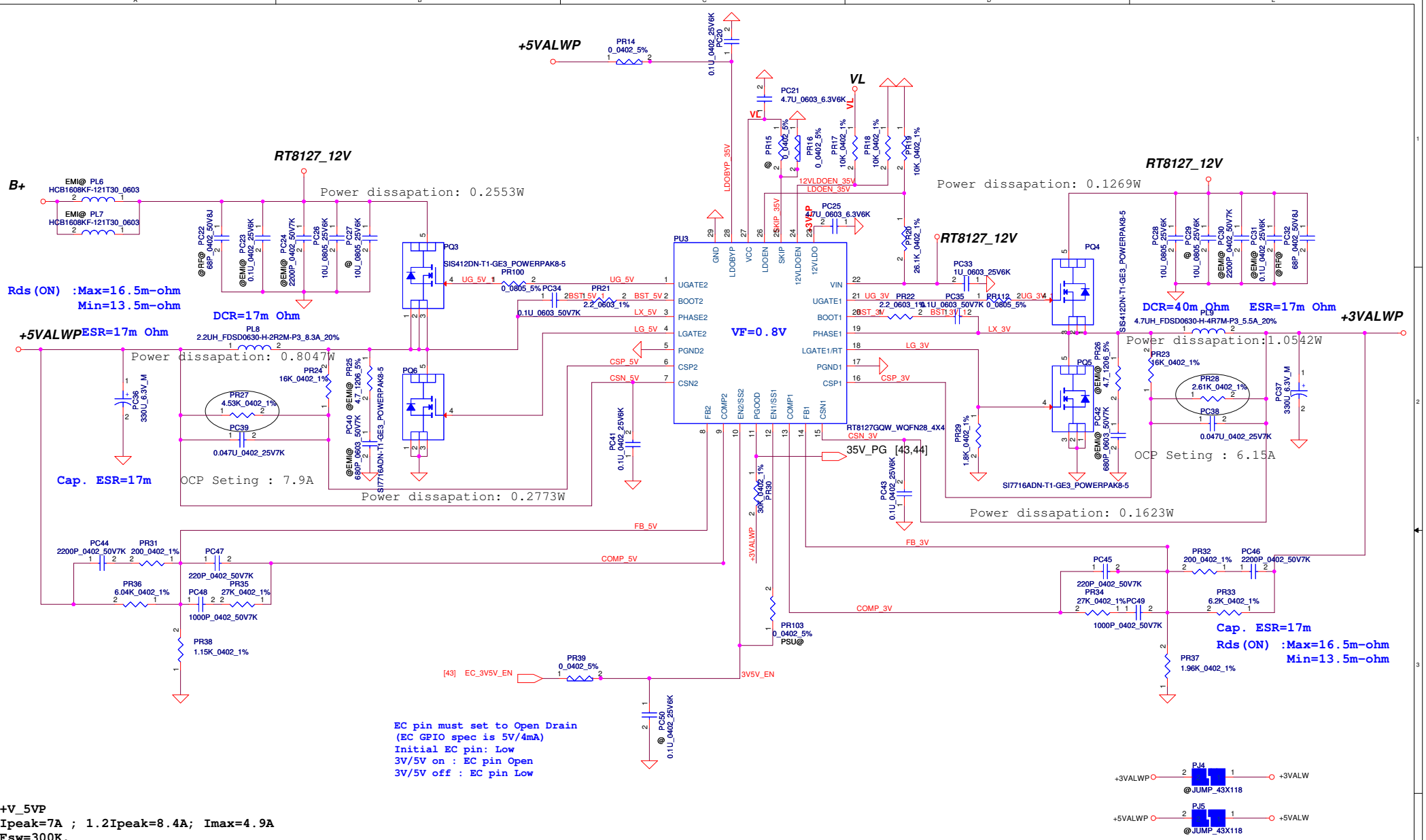
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2012/11/12

Compal Electronics, Inc.

Title: PSU IN

Size	Document Number	Rev
C		0.1

Date: Tuesday, September 24, 2013 | Sheet 46 of 56



+V_5VP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
Fsw=300K,
Iocp>=8.66A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

+V_3.3VP
Ipeak=4.437A ; 1.2Ipeak=5.325A; Imax=3.106A
Fsw=300K
Iocp>=5.33A
Rds H/S --> typ:24 mohm ; max: 30 mohm
L/S --> typ: 13.5 mohm ; max: 16.5 mohm

TON (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=300KHZ (+3VALWP)

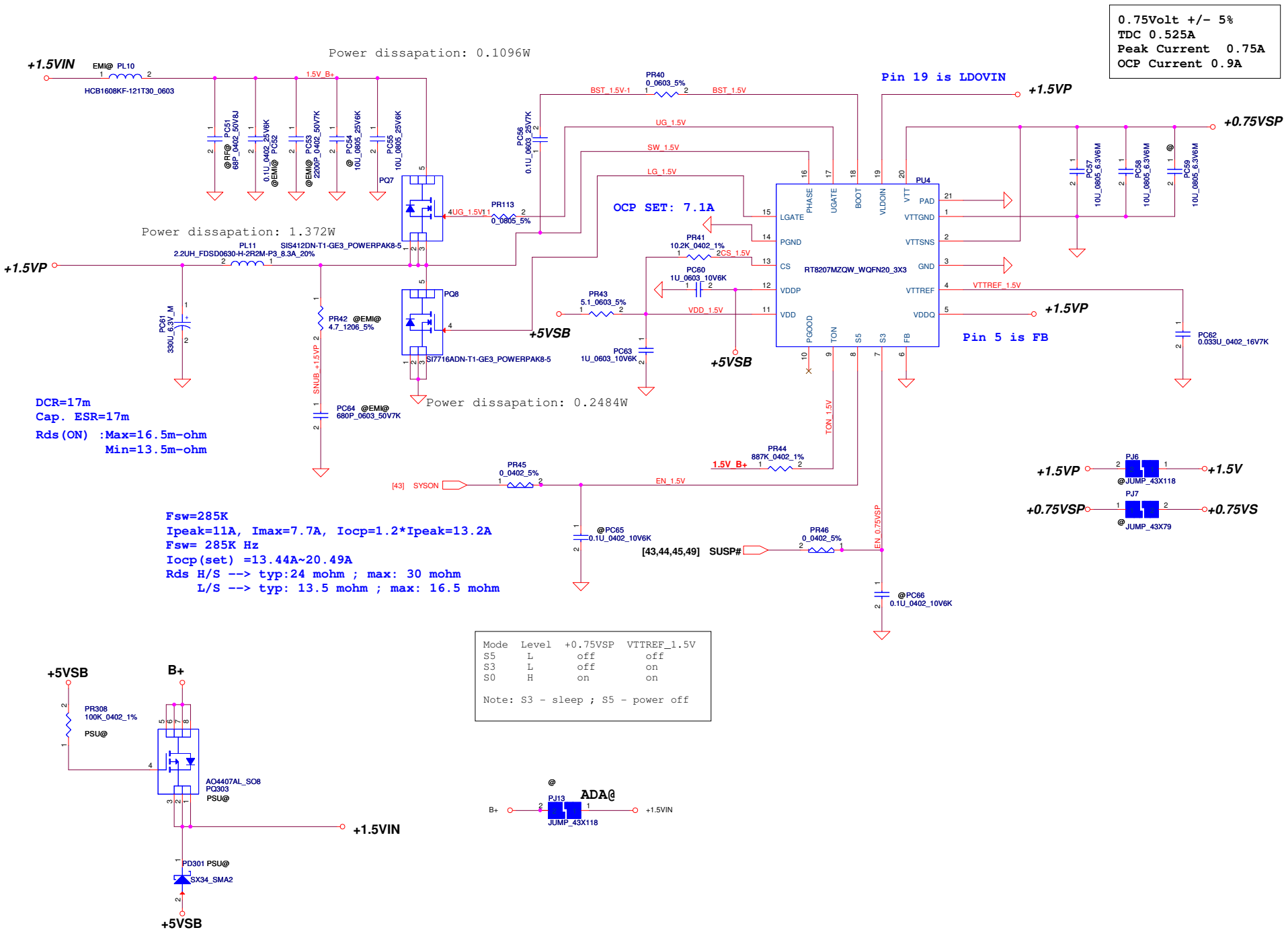
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR- 3VALWP/5VALWP

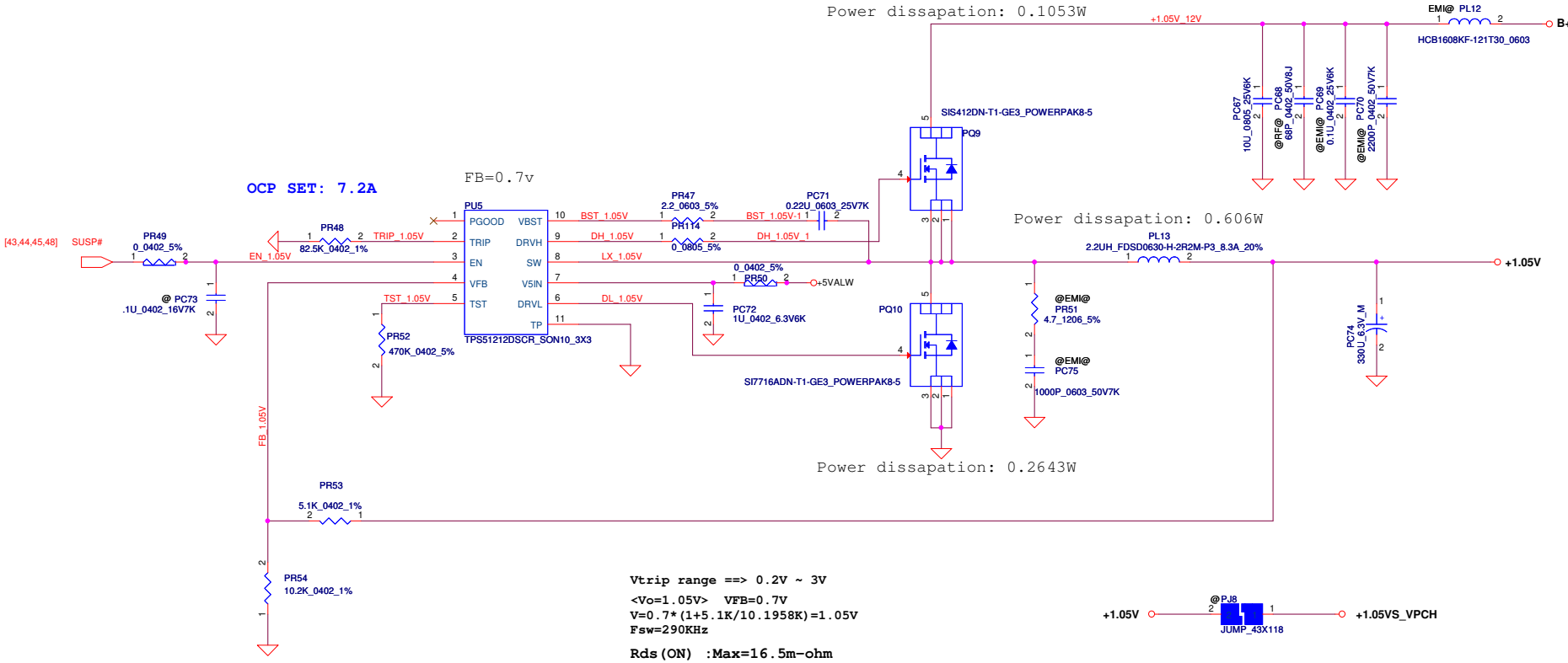
Size: Custom | Document Number: VCA00 LA-9792P M/B | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 47 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.			
Title: 1.5VP			
Size: B	Document Number		Rev: 0.1
Date: Tuesday, September 24, 2013	Sheet 48 of 56		



Vtrip range ==> 0.2V ~ 3V

<Vo=1.05V> VFB=0.7V

V=0.7*(1+5.1K/10.1958K)=1.05V

Fsw=290KHz

Rds(ON) :Max=16.5m-ohm

Typ=13.5m-ohm

Ipeak=6.526A, Imax=4.568A, 1.2*Ipeak=7.831A

Iocp(set)=7.851A~11.555A

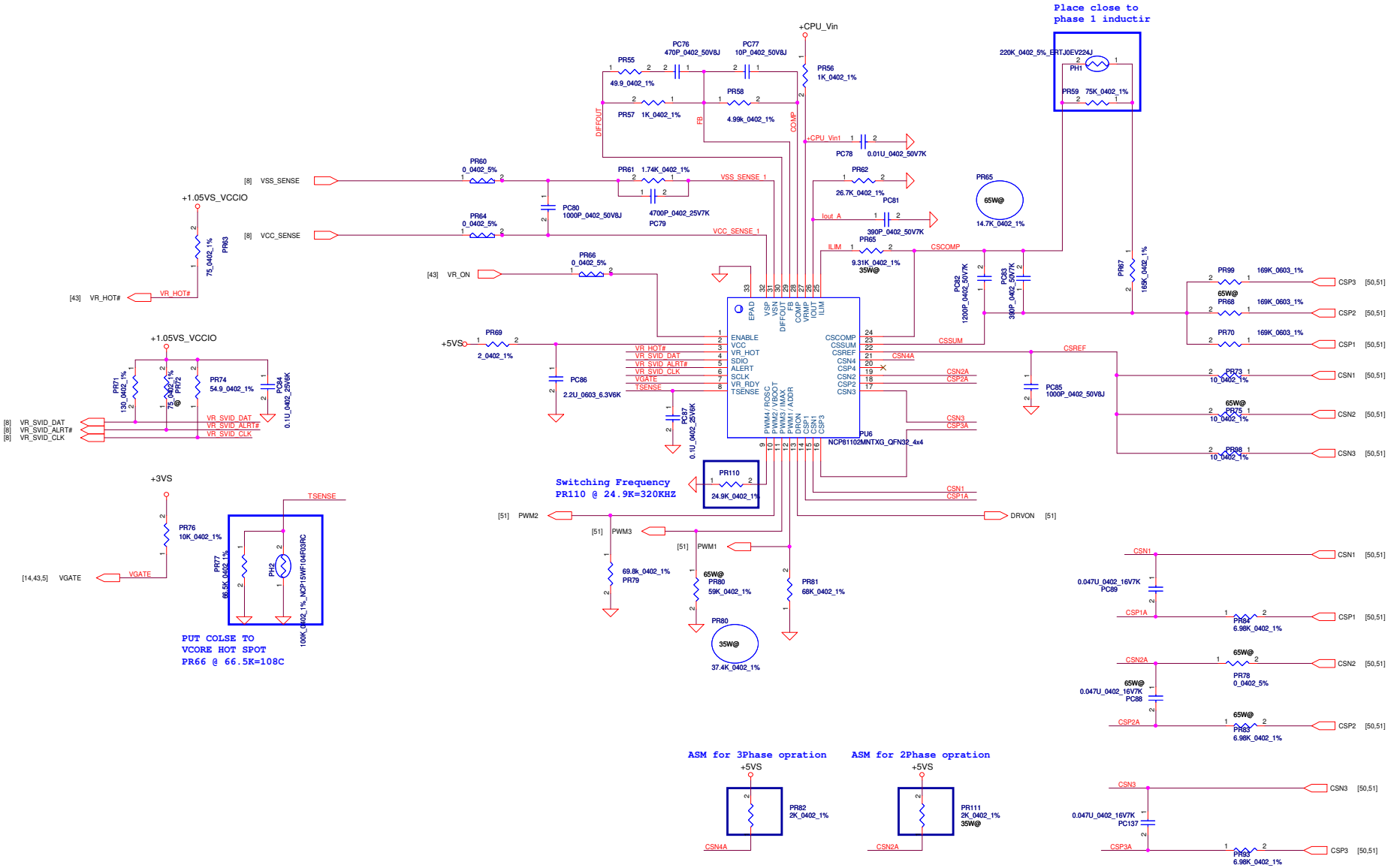
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

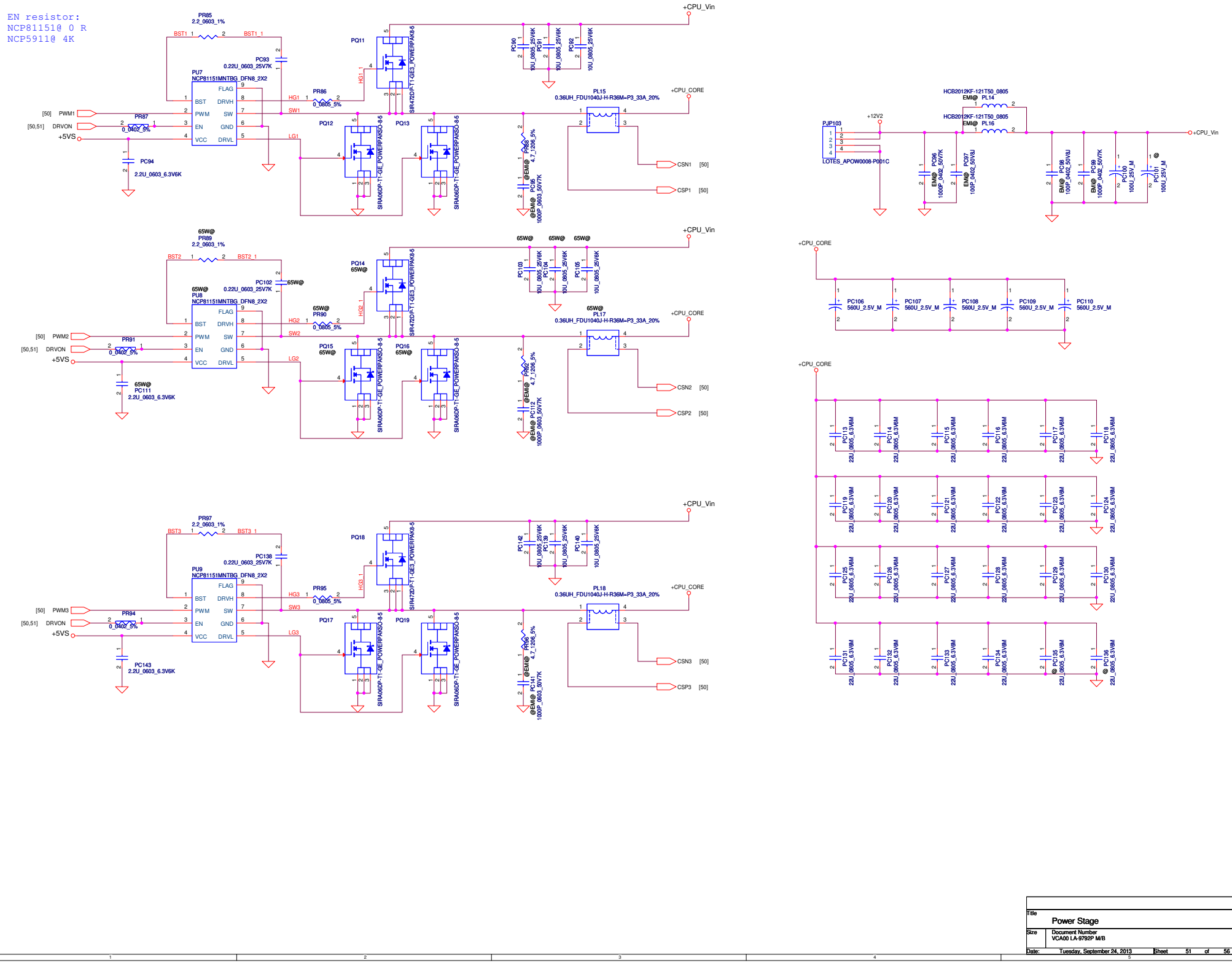
Title: +1.05VSP

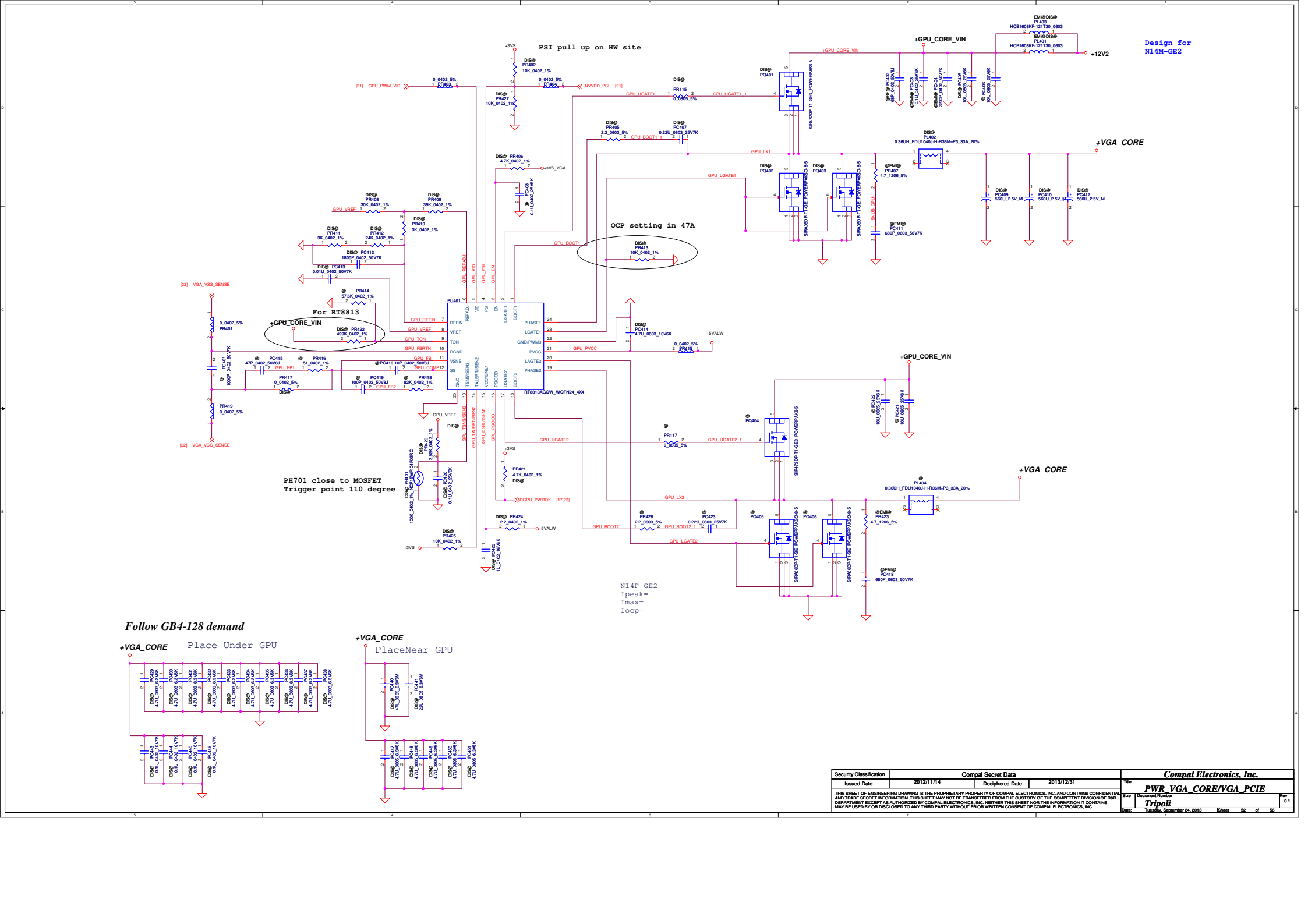
Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 49 of 56



Title	NCP81102	
Size	Document Number VCA00 LA-9792P M/B	Rev 0.1
Date: Tuesday, September 24, 2013	Sheet 50 of 56	


EN resistor:
NCP81151@ 0 R
NCP5911@ 4K
PU7
NCP81151MNTBG_DFN8_2X2
PU8
NCP81151MNTBG_DFN8_2X2
PU9
NCP81151MNTBG_DFN8_2X2
FLAG
BST
PWM
EN
VCC
DRVH
SW
GND
DRVL
+CPU_Vin
+CPU_CORE
+5VS
+12V2
[50] PWM1
[50,51] DRVON
[50] PWM2
[50] PWM3
CSN1 [50]
CSP1 [50]
CSN2 [50]
CSP2 [50]
CSN3 [50]
CSP3 [50]
PR85 2.2_0603_1%
PR86 0_0805_5%
PR87 0_0402_5%
PR89 2.2_0603_1%
PR90 0_0805_5%
PR91 0_0402_5%
PR95 0_0805_5%
PR94 0_0402_5%
PC93 0.22U_0603_25V7K
PC102 0.22U_0603_25V7K
PC138 0.22U_0603_25V7K
PC94 2.2U_0603_6.3V6K
PC111 2.2U_0603_6.3V6K
PC143 2.2U_0603_6.3V6K
PQ11
PQ12
PQ13
PQ14
PQ15
PQ16
PQ17
PQ18
PQ19
SIR472DP-T1-GE3_POWERPAK8-5
SIRA06DP-T1-GE_POWERPAK8-5
PL15 0.36UH_FDU1040J-H-R36M=P3_33A_20%
PL17 0.36UH_FDU1040J-H-R36M=P3_33A_20%
PL18 0.36UH_FDU1040J-H-R36M=P3_33A_20%
PC90 10U_0805_25V6K
PC91 10U_0805_25V6K
PC92 10U_0805_25V6K
PC103 10U_0805_25V6K
PC104 10U_0805_25V6K
PC105 10U_0805_25V6K
PC139 10U_0805_25V6K
PC140 10U_0805_25V6K
PC142 10U_0805_25V6K
PC95 @EMI@ 4.7_1206_5%
PC96 @EMI@ 4.7_1206_5%
PC97 @EMI@ 4.7_1206_5%
PC112 @EMI@ 1000P_0603_50V7K
PC113 @EMI@ 1000P_0603_50V7K
PC114 @EMI@ 1000P_0603_50V7K
PJP103
LOTES_APOW0008-P001C
HCB2012KF-121T50_0805 EMI@ PL14
HCB2012KF-121T50_0805 EMI@ PL16
PC96 EMI@ 1000P_0402_50V7K
PC97 EMI@ 100P_0402_50V8J
PC98 EMI@ 100P_0402_50V8J
PC99 EMI@ 1000P_0402_50V7K
PC100 100U_25V_M
PC101 100U_25V_M
PC106 560U_2.5V_M
PC107 560U_2.5V_M
PC108 560U_2.5V_M
PC109 560U_2.5V_M
PC110 560U_2.5V_M
PC115 22U_0805_6.3V6M
PC116 22U_0805_6.3V6M
PC117 22U_0805_6.3V6M
PC118 @ 22U_0805_6.3V6M
PC119 22U_0805_6.3V6M
PC120 22U_0805_6.3V6M
PC121 22U_0805_6.3V6M
PC122 22U_0805_6.3V6M
PC123 22U_0805_6.3V6M
PC124 22U_0805_6.3V6M
PC125 22U_0805_6.3V6M
PC126 22U_0805_6.3V6M
PC127 22U_0805_6.3V6M
PC128 22U_0805_6.3V6M
PC129 22U_0805_6.3V6M
PC130 @ 22U_0805_6.3V6M
PC131 22U_0805_6.3V6M
PC132 22U_0805_6.3V6M
PC133 22U_0805_6.3V6M
PC134 22U_0805_6.3V6M
PC135 @ 22U_0805_6.3V6M
PC136 @ 22U_0805_6.3V6M
65W@
Title
Power Stage
Size
Document Number
VCA00 LA-9792P M/B
Rev
0.1
Date: Tuesday, September 24, 2013
Sheet 51 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/11/14	Deciphered Date	2013/12/31

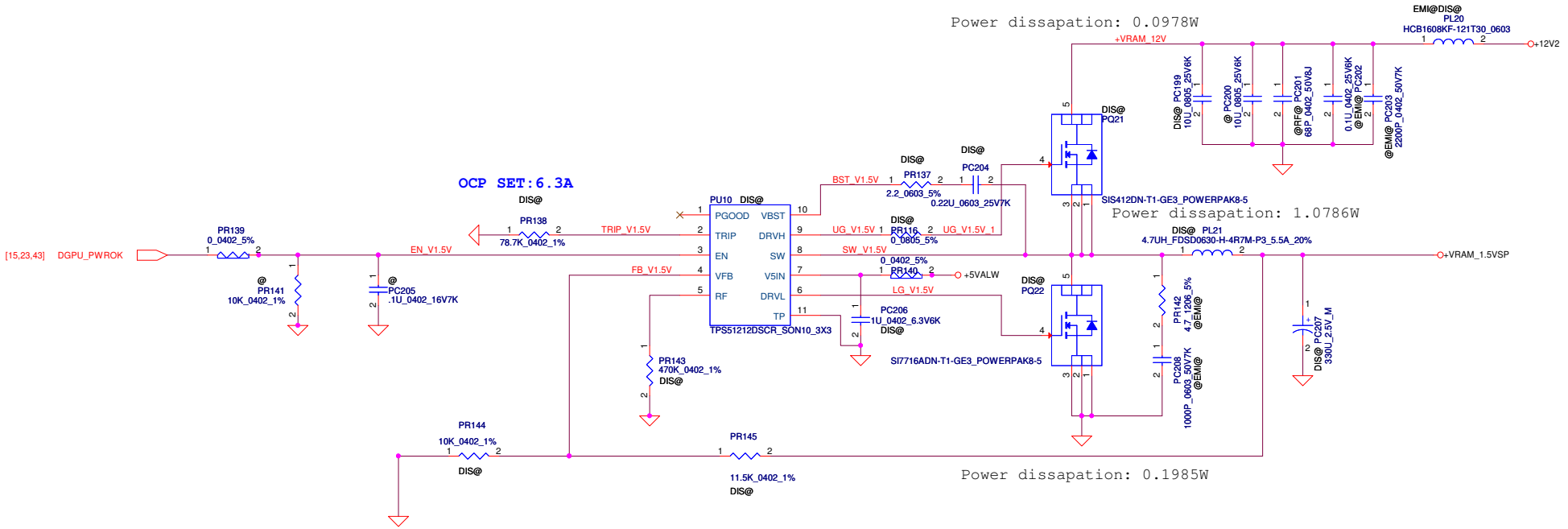
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **PWR_VGA_CORE/VGA_PCIE**

Size | Document Number: **Tripoli** | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 52 of 56



Cap. ESR=17m
Rds(ON) :Max=15m-ohm
Typ=12m-ohm
Vtrip range ==> 0.2V ~ 3V
<Vo=1.5V> VFB=0.7V
V=0.7*(1+11.5K/10K)=1.505V
Fsw=290KHz

Ipeak=4.7A, Imax=3.29A, Iocp=1.2*Ipeak=5.64A

Iocp(set)=5.718A~8.304A

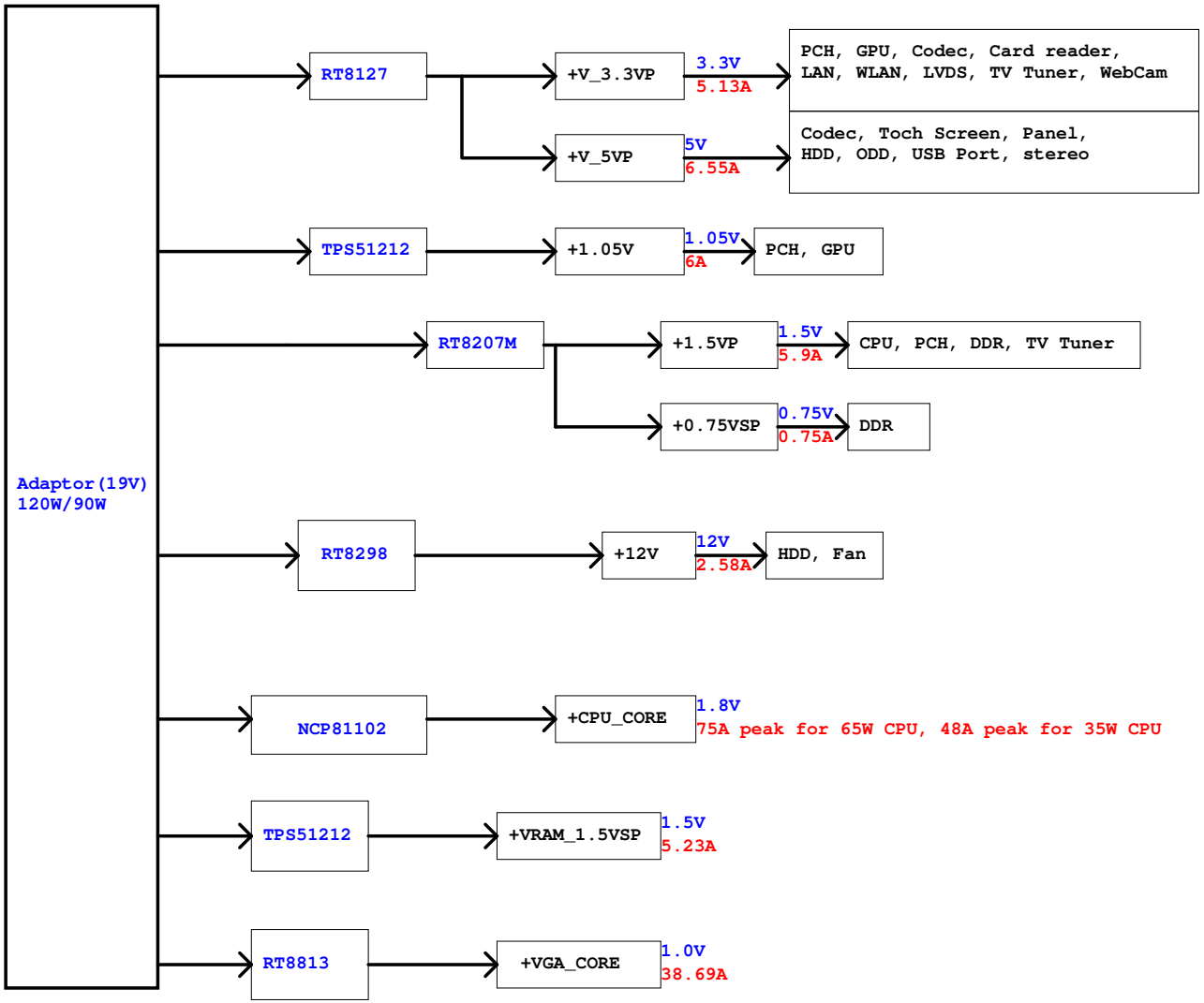
Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: PWR-VRAM_1.5VSP

Size: Custom | Document Number: VCA00 LA-9792P M/B | Rev: 0.1

Date: Tuesday, September 24, 2013 | Sheet 53 of 56



Security Classification	Compal Secret Data		
Issued Date	2011/09/12	Deciphered Date	2012/09/12

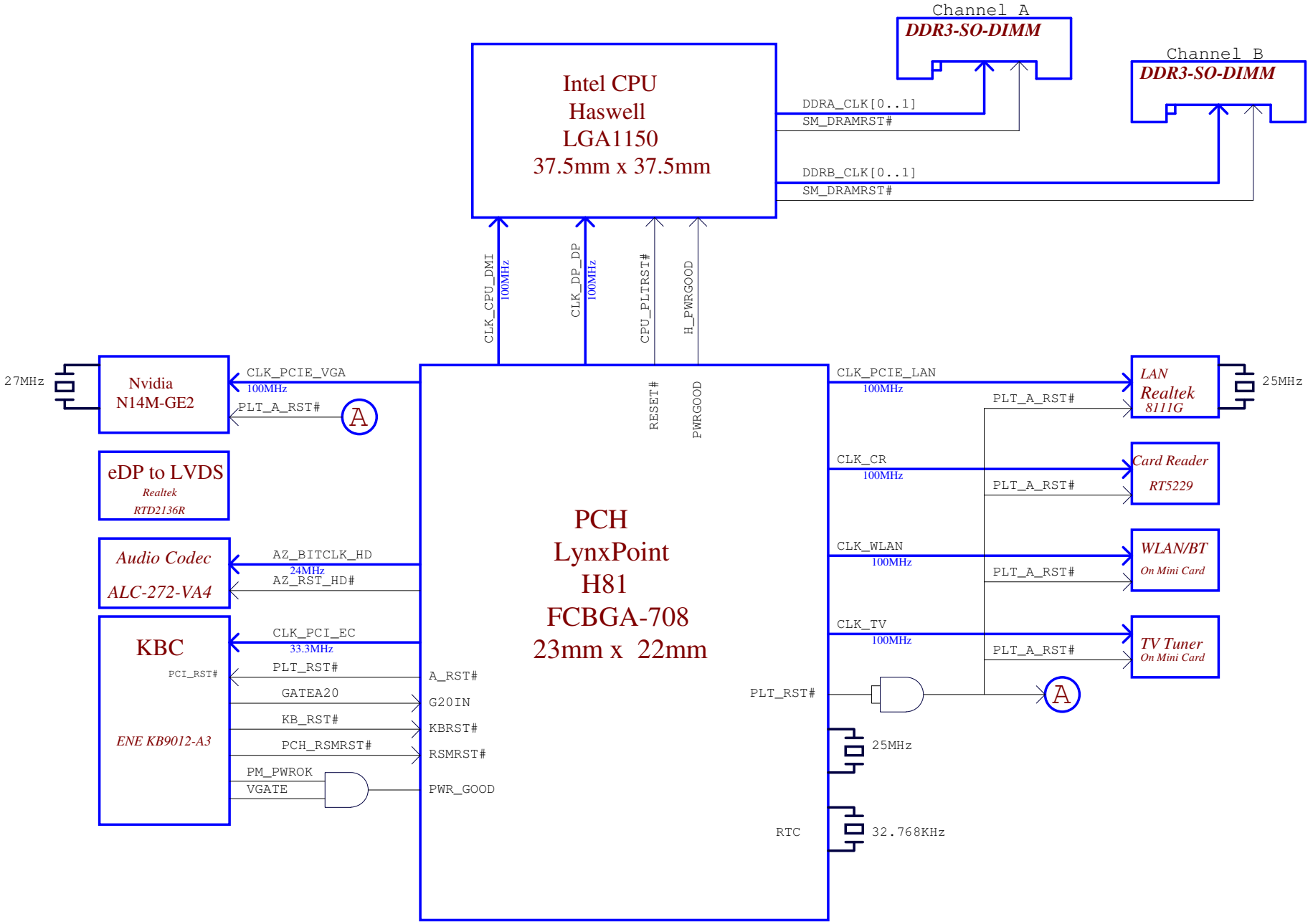
Compal Electronics, Inc.

Title: Power Rail

Size	Document Number	Rev
Custom	QLA13/15 LA-8501P M/B	0.4

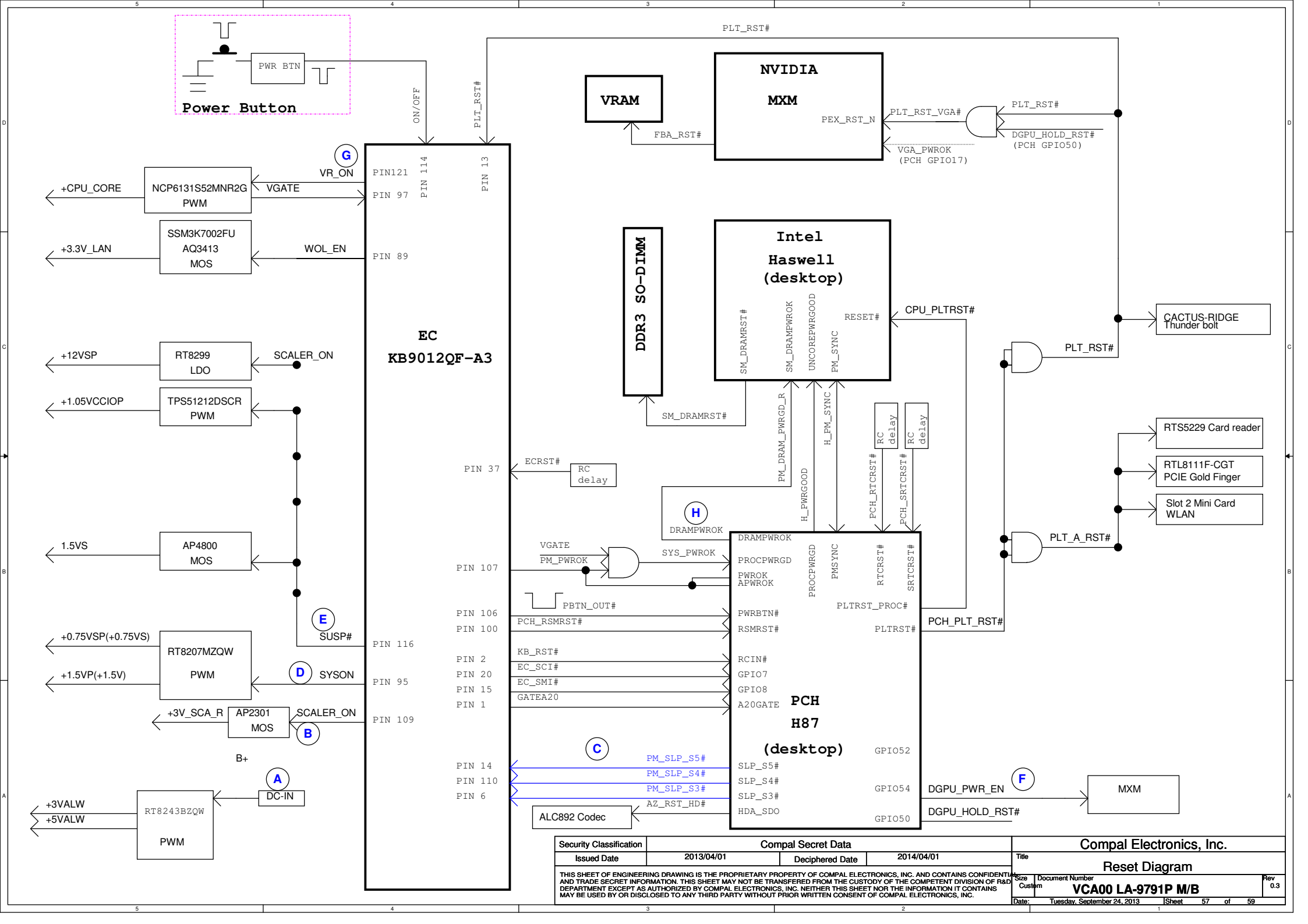
Date: Tuesday, September 24, 2013 | Sheet 55 of 59

Clock and Reset Diagram



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title: Clock/Reset Diagram			
Size: Custom	Document Number: VIA15 LA-A071P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 56 of 59		



Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Reset Diagram

Size	Document Number	Rev
Custom	VCA00 LA-9791P M/B	0.3

Date: Tuesday, September 24, 2013 Sheet 57 of 59

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	20130604	P47	Add PC154 and Change the pu101 to SA00005A600	For Pericom issue
2.	20130729	P45	Add PR105 ,PC155 Snaber	For EMI Request
3.	20130729	P45	Add PR1	For EMI Request
3.	20130729	P45	Add PR39	For S5 power loss issue

Security Classification	Compal Secret Data		
Issued Date	2011/09/12	Deciphered Date	2012/09/12

Compal Electronics, Inc.

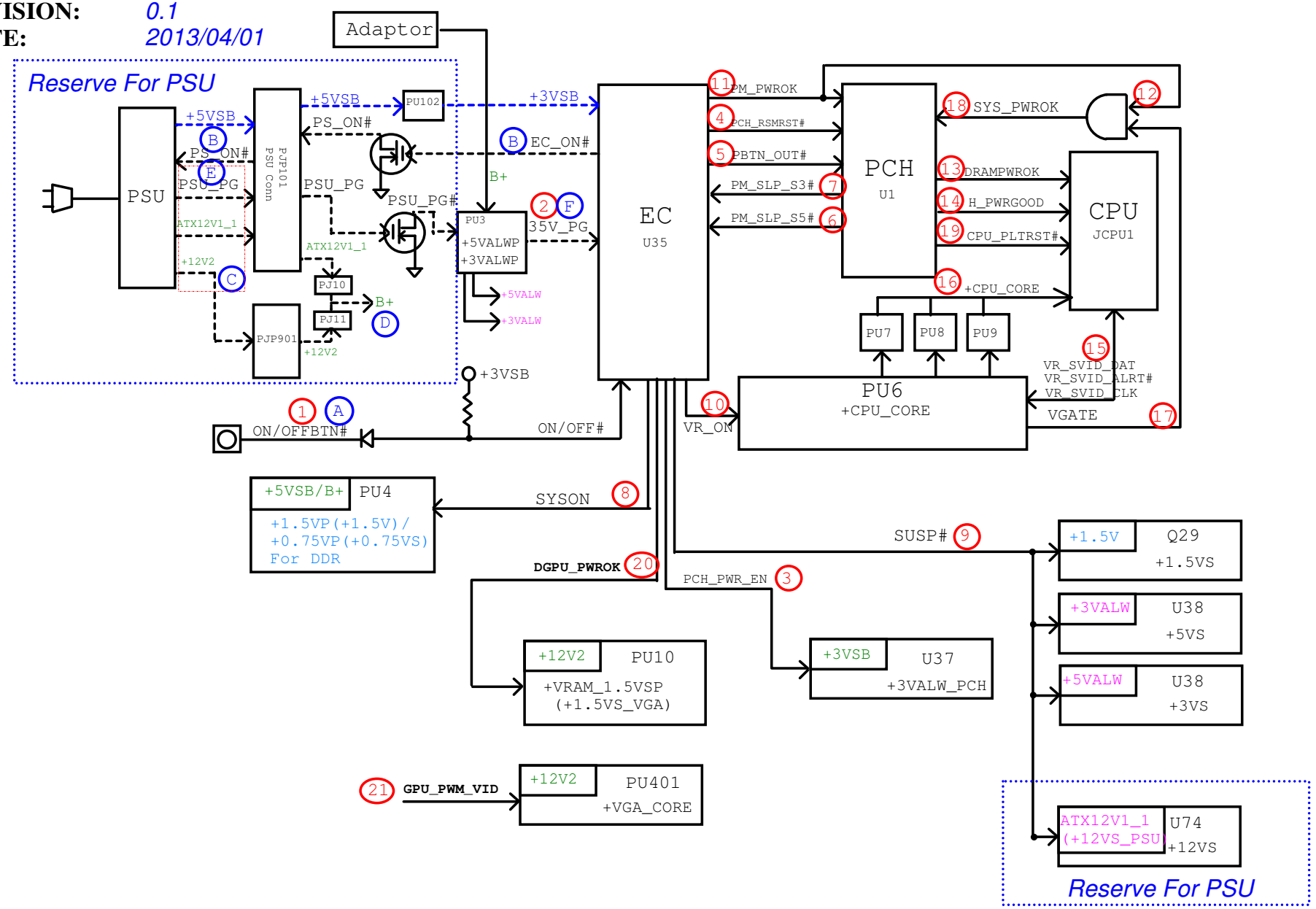
Title: PWR_PIR

Size	Document Number	Rev
Custom	B555 VA15 LA-A072P MB	0.5

Date: Tuesday, September 24, 2013 Sheet 57 of 60

COMPAL CONFIDENTIAL

MODEL NAME: *ZEA00 Power Sequence Block Diagram (Discrete)*
PCB NAME: *LA-A061P*
REVISION: *0.1*
DATE: *2013/04/01*



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/04/01	Deciphered Date	2014/04/01
Title	Power Sequence Diagram		
Size: B/26 Custom	Document Number: ZEA00 LA-A061P M/B		Rev: 0.3
Date: Tuesday, September 24, 2013	Sheet 58 of 59		

HW PIR (Product Improve Record)

ZEA00 LA-A061P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 --> 0.2
GERBER-OUT DATE: 2013/06/20

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

1. Change C45 from SF000002V00 to SF000003X00
2. Change +LCDVDD enable control from EC to LVDS convertor,un-pop R367 and R365 change short pad.
3. ~~Change LCD_BKOFF# control from EC to LVDS convertor,un-pop R364 and R363 change 0 ohm.~~
4. Remove un-used components(U18,R335,R336,C357,C359,C360,R338,R339) for eDP to LVDS convertor.
5. Pop R428 for AZ_SDIN0_HD.
6. U2 footprint change from socket to IC.
7. Add RH11
8. Change Y2 from SJ10000CU00 to SJ10000DE00,change C106 & C107 from 27pF to 4.7pF
9. Change R423 location to L45
10. Change D7 from SC2N202U010 to SC600000B00 for 替代料
11. Change Q29 from SB548000210 to SB00000ZN00.
12. Change D8&D9 from SCS00002G00 to SCS00000Z00
13. X1 code change:1.Change Q2,Q3,Q4,Q5,Q30,Q31 from SB01000JE00 to SB00000EO00. 2.Change Q9 from SB934130020 to SB934130000.
    3.Change Q10 from SB00000FC00 to SB00000F400. 4.Change L1 from SM01000JE00 to SB01000JN00.
14. Change R551 & R553 pull-high from +3VS to +3VALW_PCH for leakage.
15. Add R677 & R678 & R679 for PTC request, Change R473,R490,R679,R677,R678 from 0ohm to PTC(SP040005X00).
16. Change Q10 from SB00000FC00 to SB00000L800 for 替代料
17. Remove R469 0ohm for TV.
18. Add C2134 ,C2135,C2136,C2137,C2138,C2139,C2140,C2141,C2143 for ESD.
19. Remove JXDP1,OC1,OC2,RC3,RC4,R125,R126.
20. Pop U7&R231, un-pop R228 for PLT_RST_VGA#.
21. Swap SATA_PRX_DTX_N1 & SATA_PRX_DTX_P1 for m-SATA pin define.
22. Un-pop LAN power components Q26,Q27,R573,R574,C562.
23.0 ohm change to short pad: R347,R585,R507,R674,R644,R645,R646,R647
24.Change R453&R457 from 0ohm to 1.1K, R451&R459 from 300ohm to 5.6Kohm.
25.Pop R438,R439 for ESD request.

PVT change list:
1. Change Q10 from SB00000FC00(EOL soon) to SB00000ZN00(同Q29),SB00000FC00 as 2nd source.Schematic,需驗證
2. Change U23 pin12_+USB3_VCCA to +USB3_VCCB, pop U22, un-pop U24 for USB charger
3. R365 change from short pad to 0ohm.
4. U5 pin5 change from +3VSto +3VALW_PCH for BCM43142 wake from WLAN issue.
5. Change R473,R490,R677,R678,R679 from SP040005X00_0603 size to F1,F2,F4,F5,F3 SP040003S00_1206 size.
6. Change L11 from SM010014520 to SM01000EJ00 for ACL request
7. Change L8 from SM010007W00 to SM010019400 for ACL request
8. Change D7 from SC2N202U010 to SC600000B00(same as D1/D2), SC2N202U010 as 2nd source..
9. Change RP19 from SD309510A80(T88 P/N) to SD309510A10.
11. Change R276 from 10k to 100k for +3VS_VGA rise time.
12. Change R672 from 10k to 100k for +3VALW_PCH rise time.
14. Change R438 & R439 from 0_0603 to short pad.
15. Un-pop C125 & C548 for sequence EA.
16. Change C394, C398,C520 & C514 from 220uF(LELON_SF000001F00) to 100uF (Panasonic_SF000005100) to meet Inrush EA & ACL request.
17. Change C170 & C171 from 12pF to 10pF for EA.
20. Change C106 & C107 from 4.7pF to 10pF for 25MHz crystal.
21. Add R677 & reserve R678 on U5 AND gate for PLT_A_RST#
13. Change JUSB1 & JUSB2 from DC23300AE00 to DC233008R00(VBA11)
24. Change R591 pull-high from +5VSB to VL for power S5 Erp request.
22. Change D20 & D21 from SC300001Y00 to SC300002F00 for ESD request
23. Change D22 & D23 from SCA00001100 to SCA00000T00 for ESD ACL request
10. Add C2144~C2152 for EMI request.
18. Change R402 from short pad to 22ohm for EMI, R399,R401,R403 & R404 change from short pad to 0 ohm for EMI request.
19. Reserve C2153,C2154,C2155,C2156, add D29 for ESD.
20. Change R282 from 100k to 2k, R277 from 470 to 22 ohm for GPU power sequence.
21. Change Y1 from SJ100001K00 to SJ10000FA00 ,C102 & C107 to 6pF.

pre-MP change list:
1. Change R399,R401,R402,R403,R404 from 0ohm to short pad.
2. Add C2157 and reserve C2158.
3. Change R8,R470,R669,R670,R416 from 0ohm to short pad.
4. Un-pop JECDB1 & SW1.
5. For R3 P/N, change PCH P/N from SA00006RF00 to SA00006RF20, PCB P/N from DA60011S000 to DA60011S010 and GPU P/N from SA00006ZF00 to SA00006ZF10.
6. Change C520 & C514 from 100uF to 220uF.
7. Pop C2149~C2152 for ESD request.
8. Change C559 & C2128 from 0603 to 0805.
9. Change C2145 from 0.1uF to 470pF, change C2149~C2152 from 330pF to 470pF for EMI.
10. Add C418 for EMI.

Security Classification	Compal Secret Data		
Issued Date	2013/04/01	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: *HW-PIR*

Size | Document Number: VCA00 LA-9791P M/B | Rev: 0.3

Date: Tuesday, September 24, 2013 | Sheet 59 of 59