

Compal Confidential

NAWE6 Schematics Document

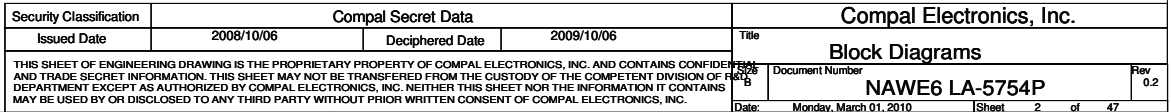
AMD Danube

Champlain Processor with RS880M/SB820/Park VGA

2010-02-24

LA5754 REV: 0.2

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Model Name : AMD Danube + Park

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.75VS	+0.75VS LDO power rail for DDR3 VTT	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	EMC1402-1 (CPU)	100_1100b	4CH
			EMC1412-A (GPU)	111_1100b	7CH
			EMC1403-2 (DDR,WWAN)	100_1101b	4DH

EC SM Bus2 address

SB820
SM Bus 0 address

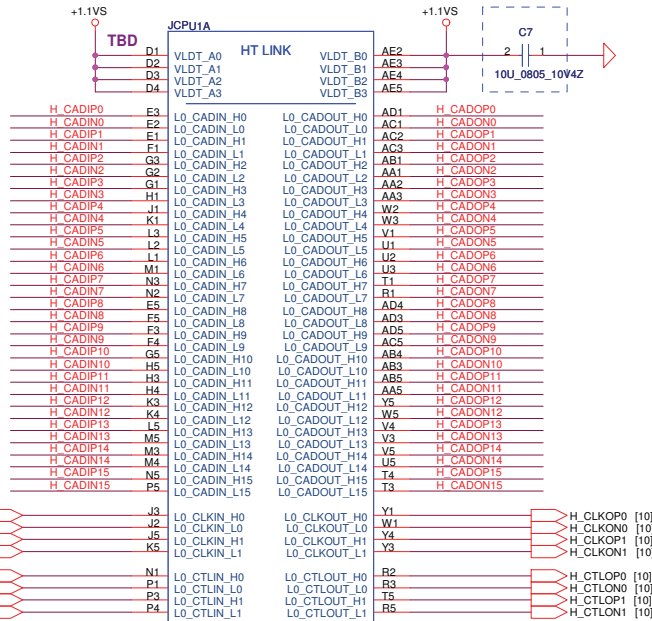
Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2		
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		

SB820
SM Bus 1 address

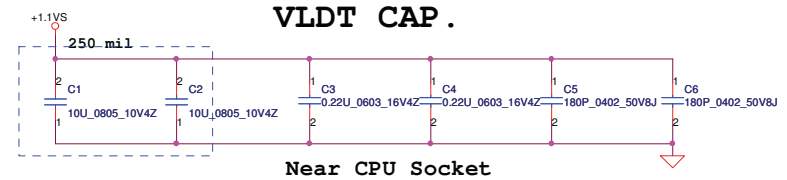
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Config
UMA only SKU: UMA@
DIS ONLY (Park S3): DIS@
EXT CLK Mode:EXT@
INT CLK mode:INT@
LAN GIGA: 8151@
LAN 100: 8152@
CMOS@
BT@
3G@
S@
H@

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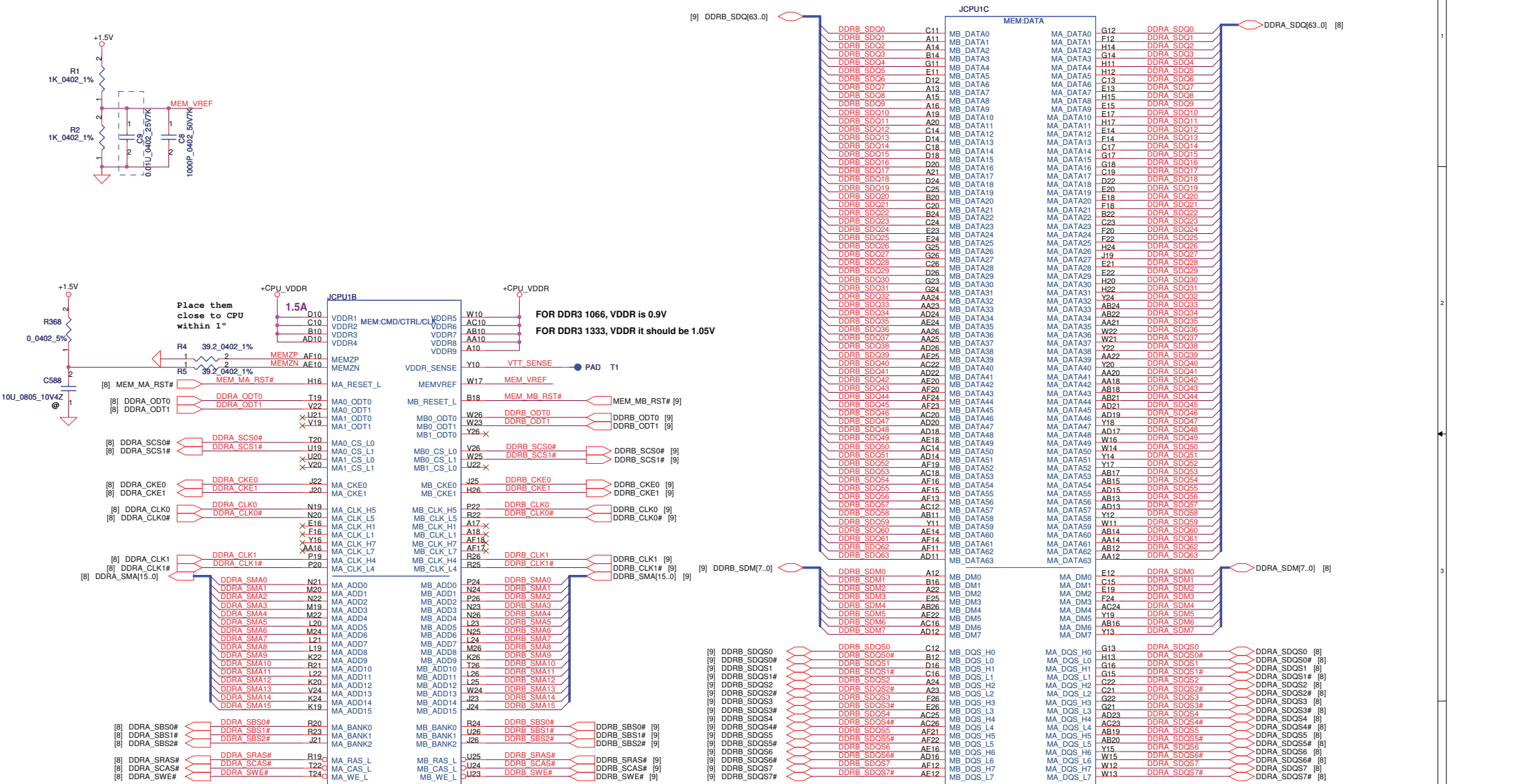


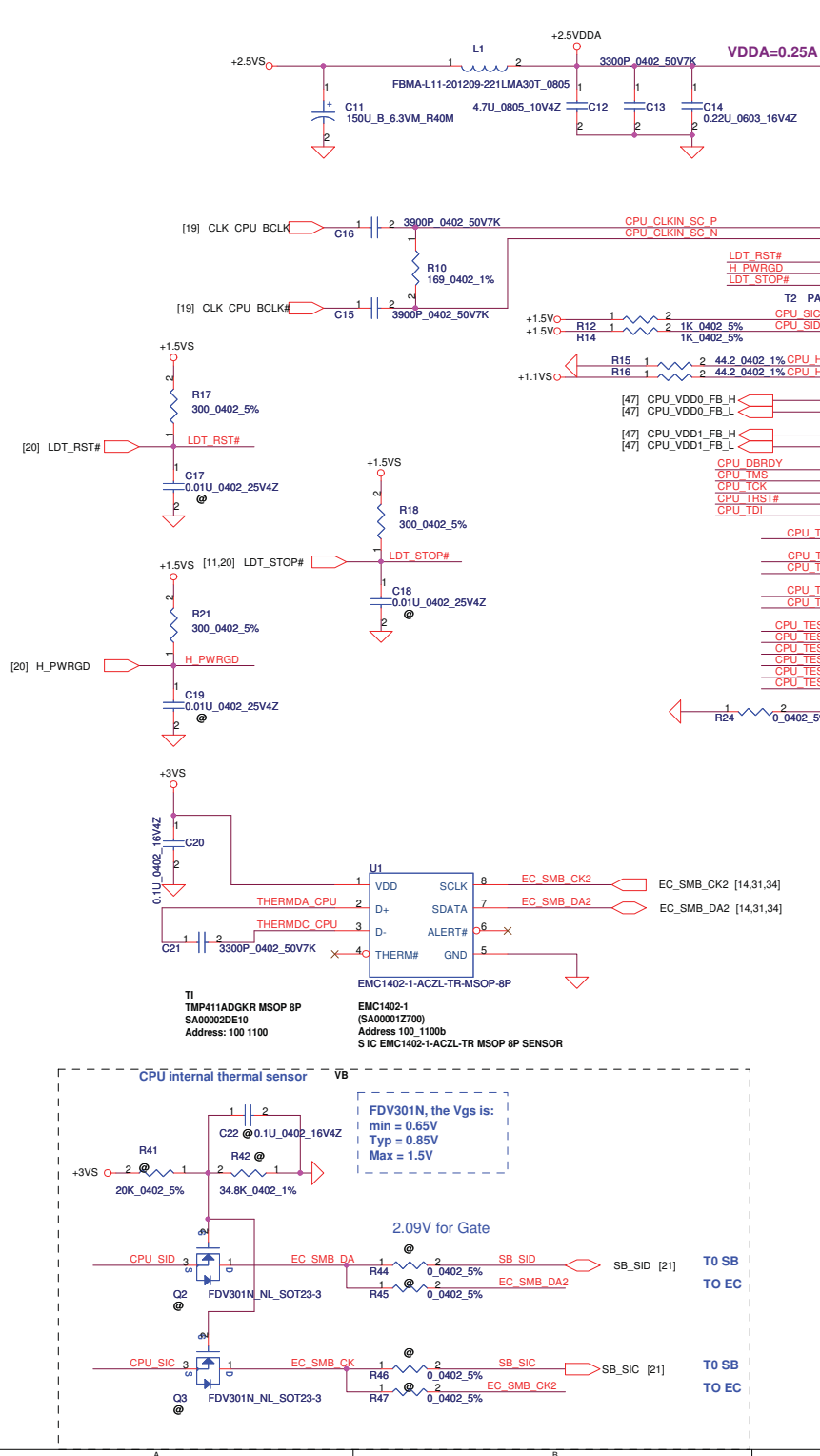
FOX_P26382A-284S-41F_Champian
ME@



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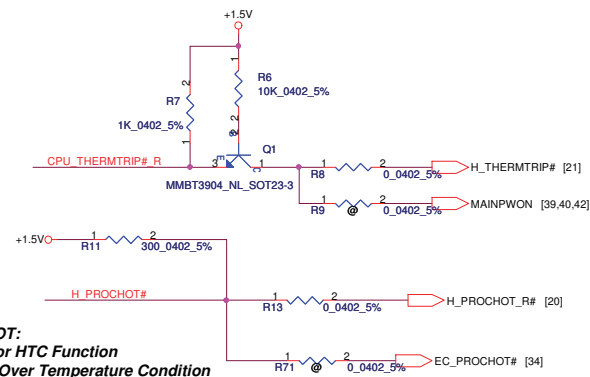
Processor DDR3 Memory Interface



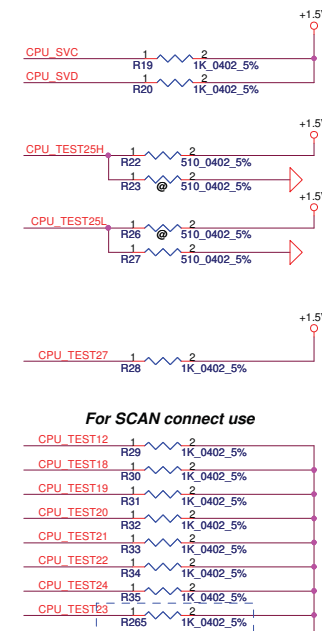


Champlain: C1E
C1E: LDT_REQ# no connect
CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
no support in S1g4

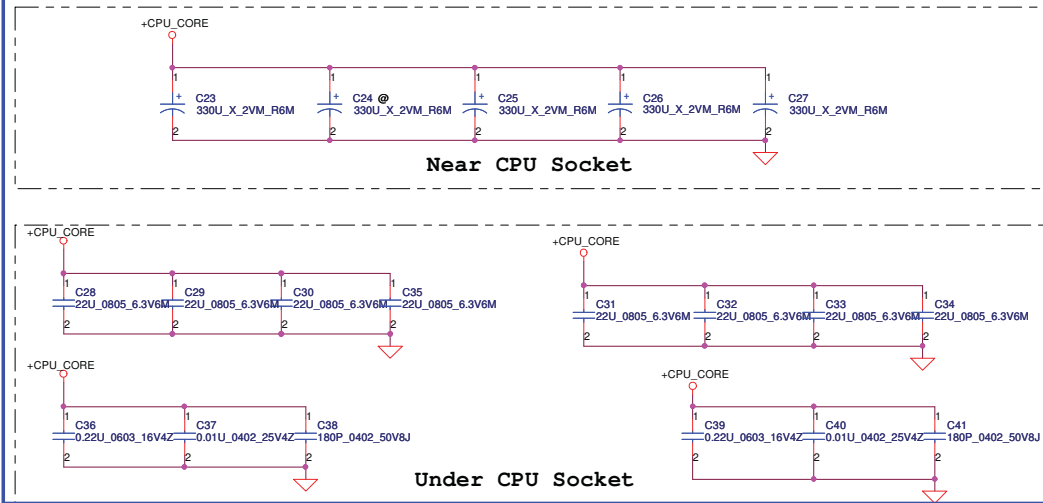


PROCHOT:
Input: For HTC Function
Output: Over Temperature Condition

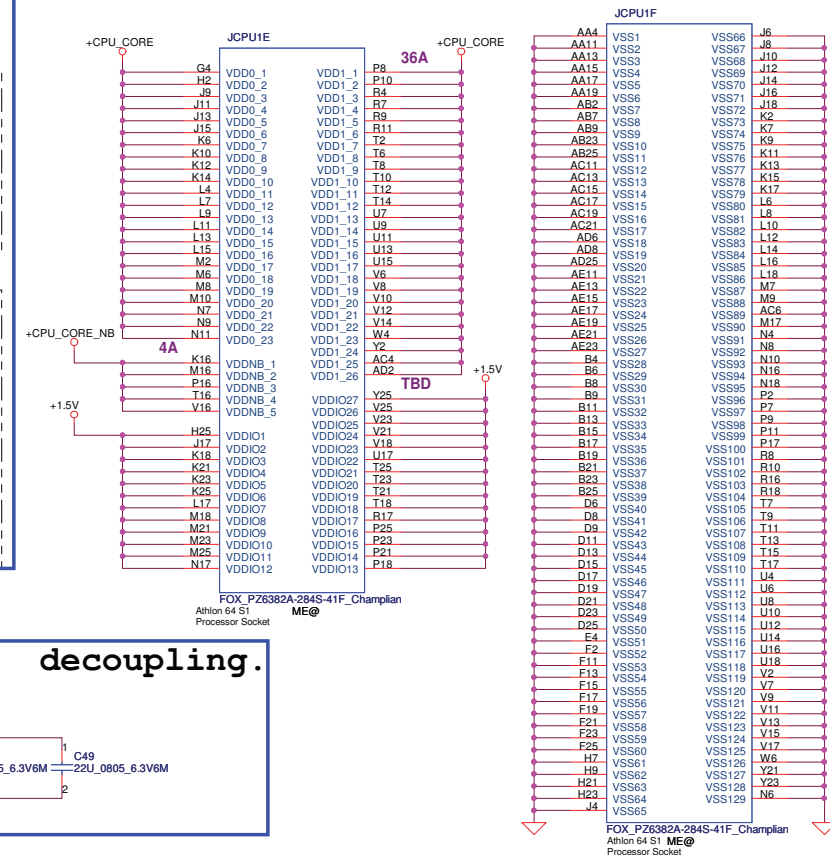
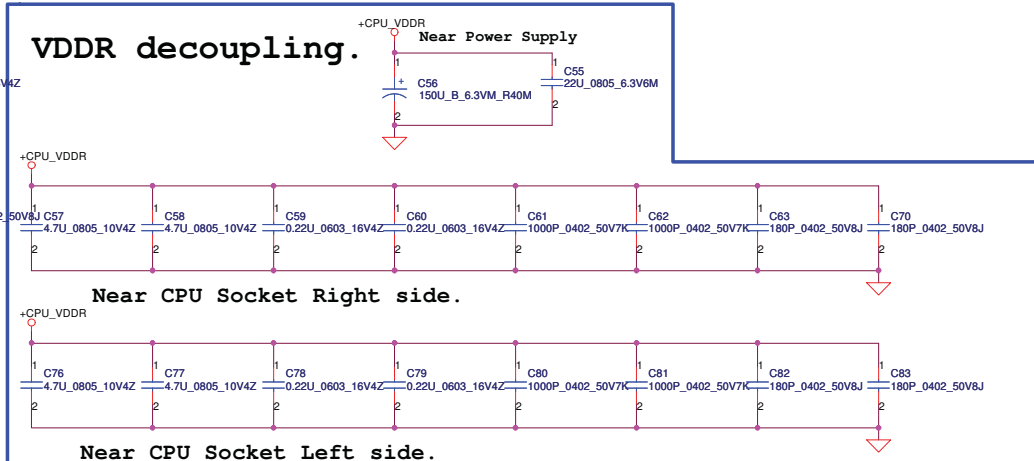
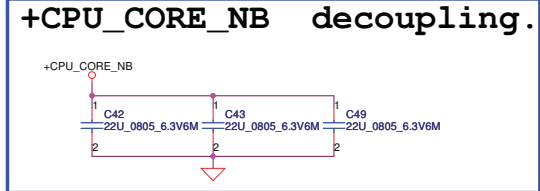
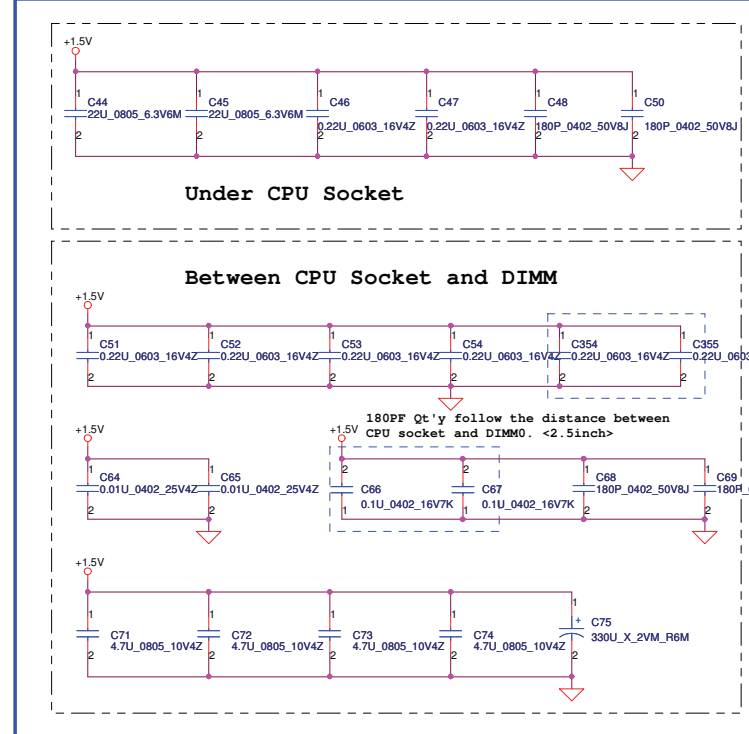


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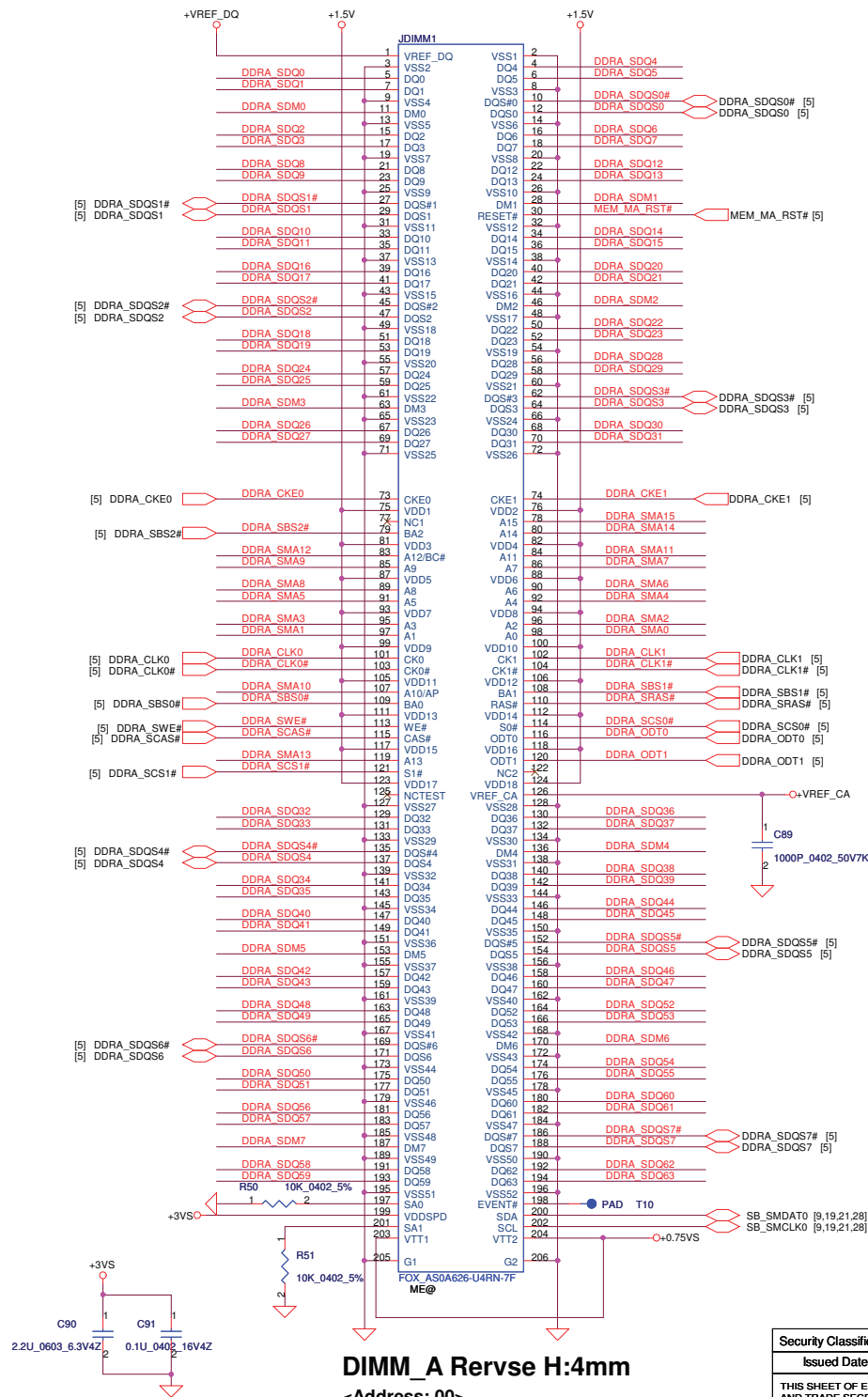
VDD (+CPU_CORE) decoupling.



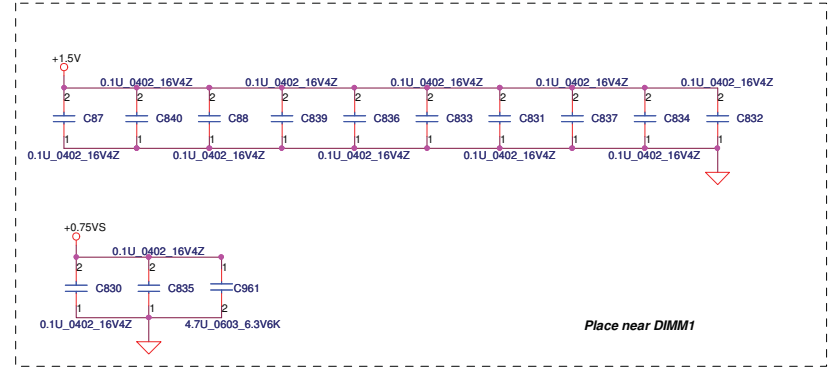
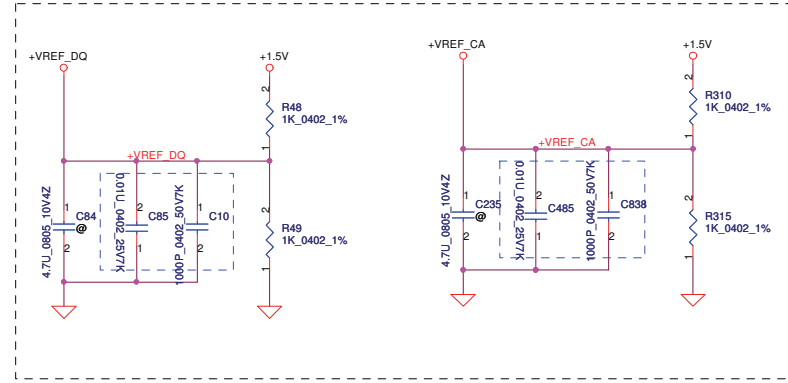
VDDIO decoupling.



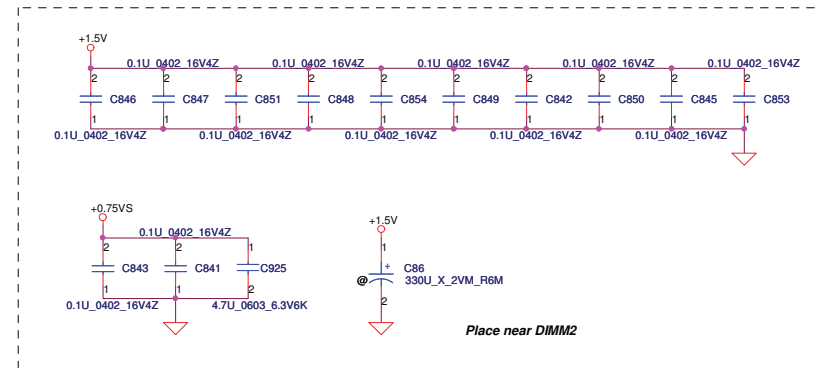
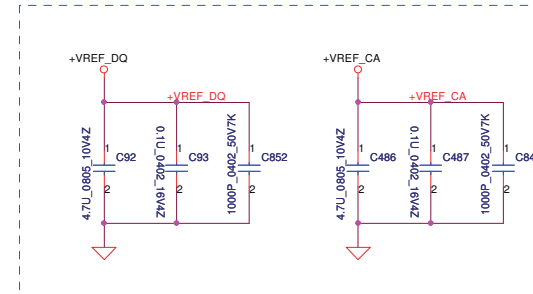
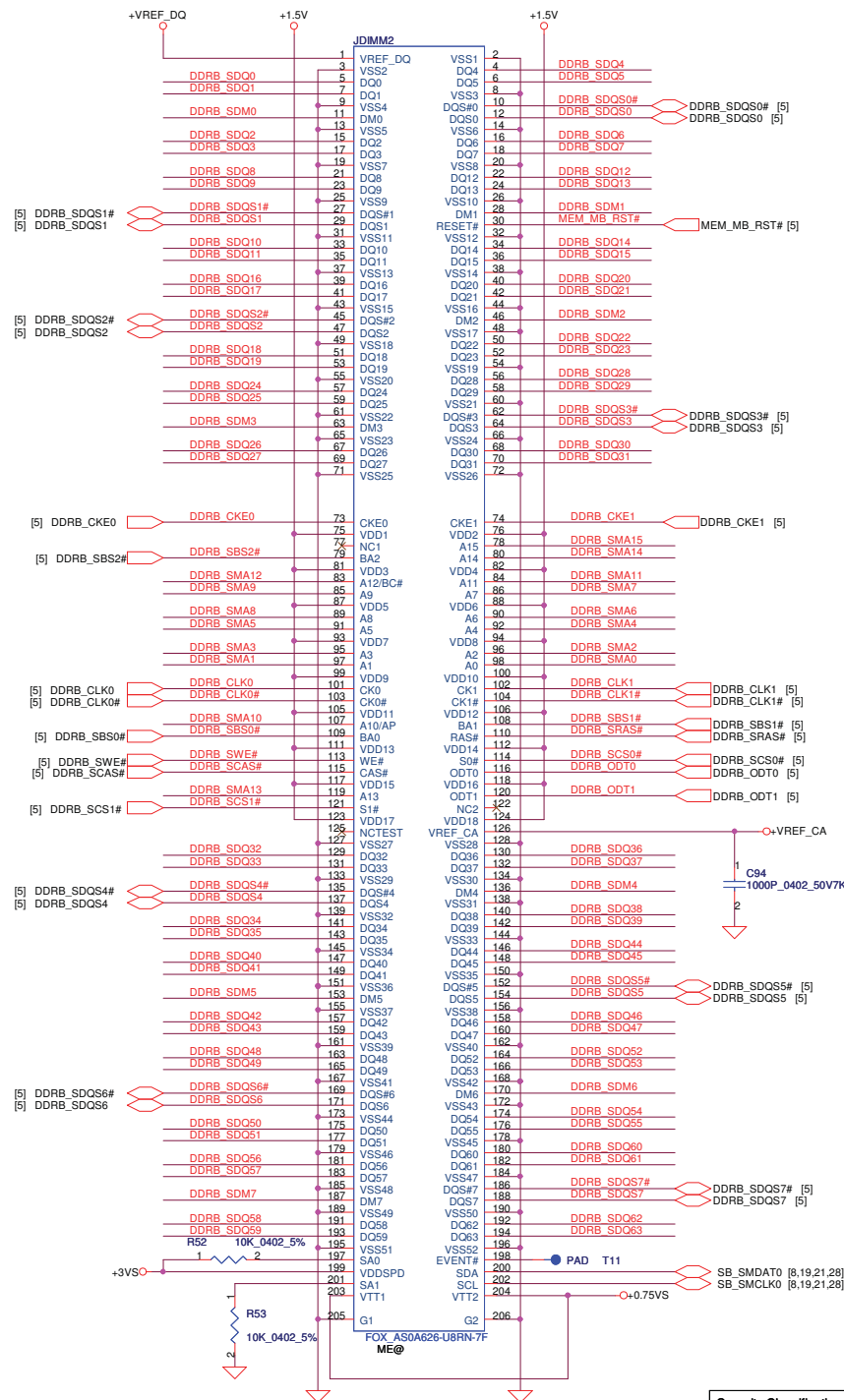
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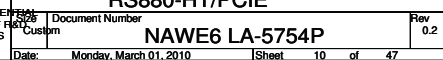
DDR_A SDQ[0..63] → DDR_A_SDQ[0..63] [5]
 DDR_A SDM[0..71] → DDR_A_SDM[0..71] [5]
 DDR_A SMA[0..15] → DDR_A_SMA[0..15] [5]

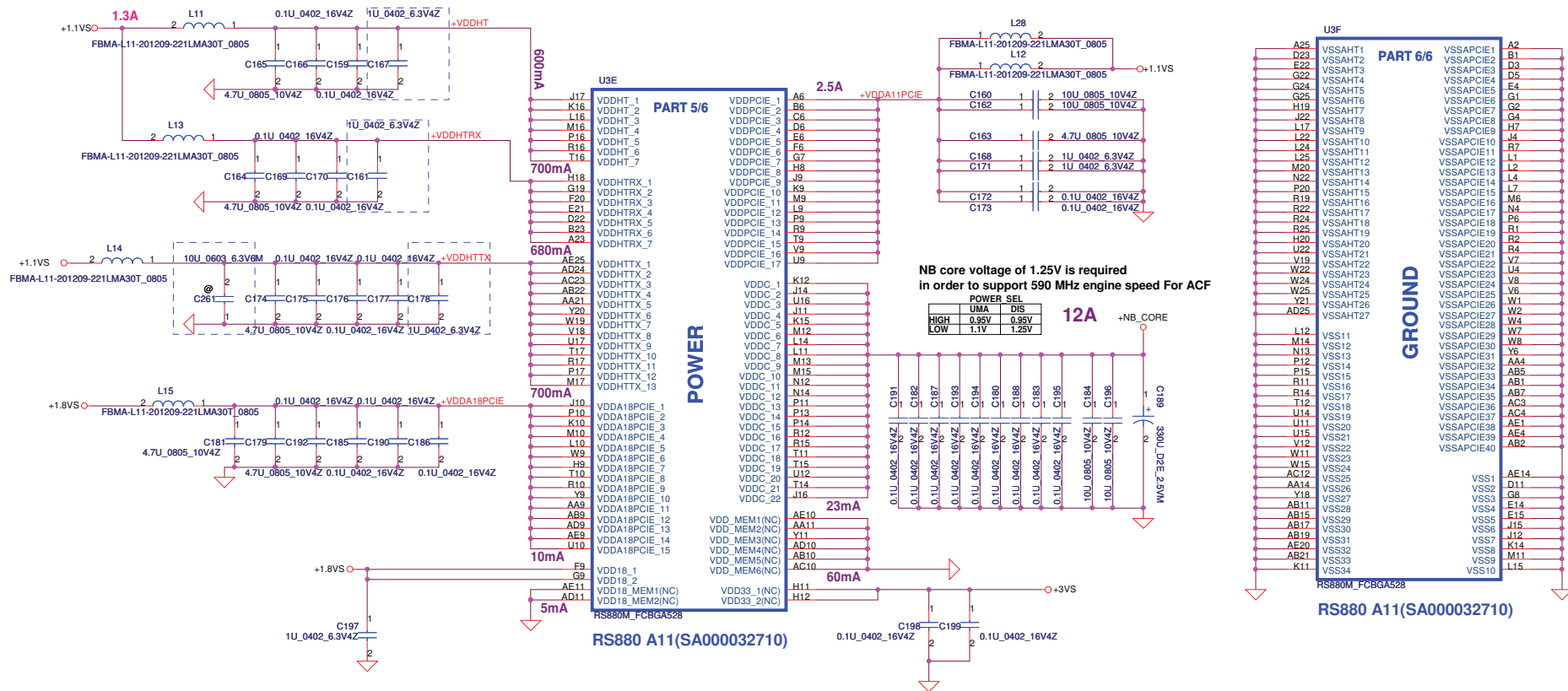


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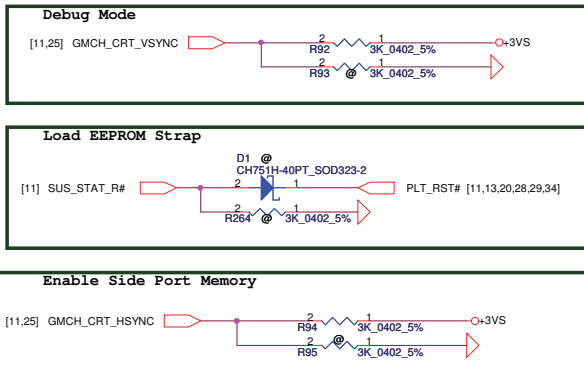


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Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable
 0 : Enable

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

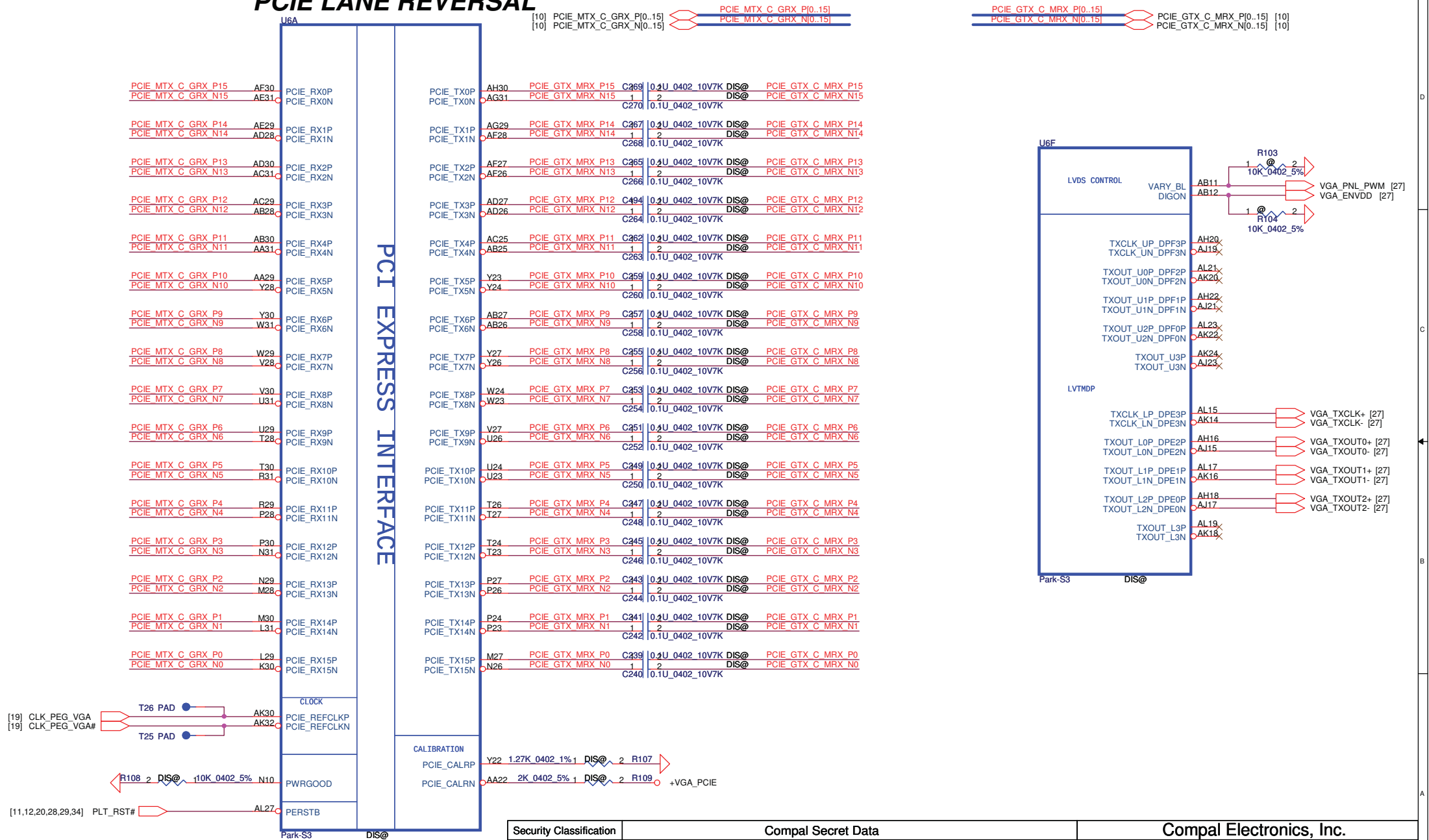
Enable Side Port Memory

RS880: HSYNC#
 0: Enable
 1 : Disable
 Register Readback of strap:
 NB_CLKCFG:CLK_TOP_SPARE_D[1]

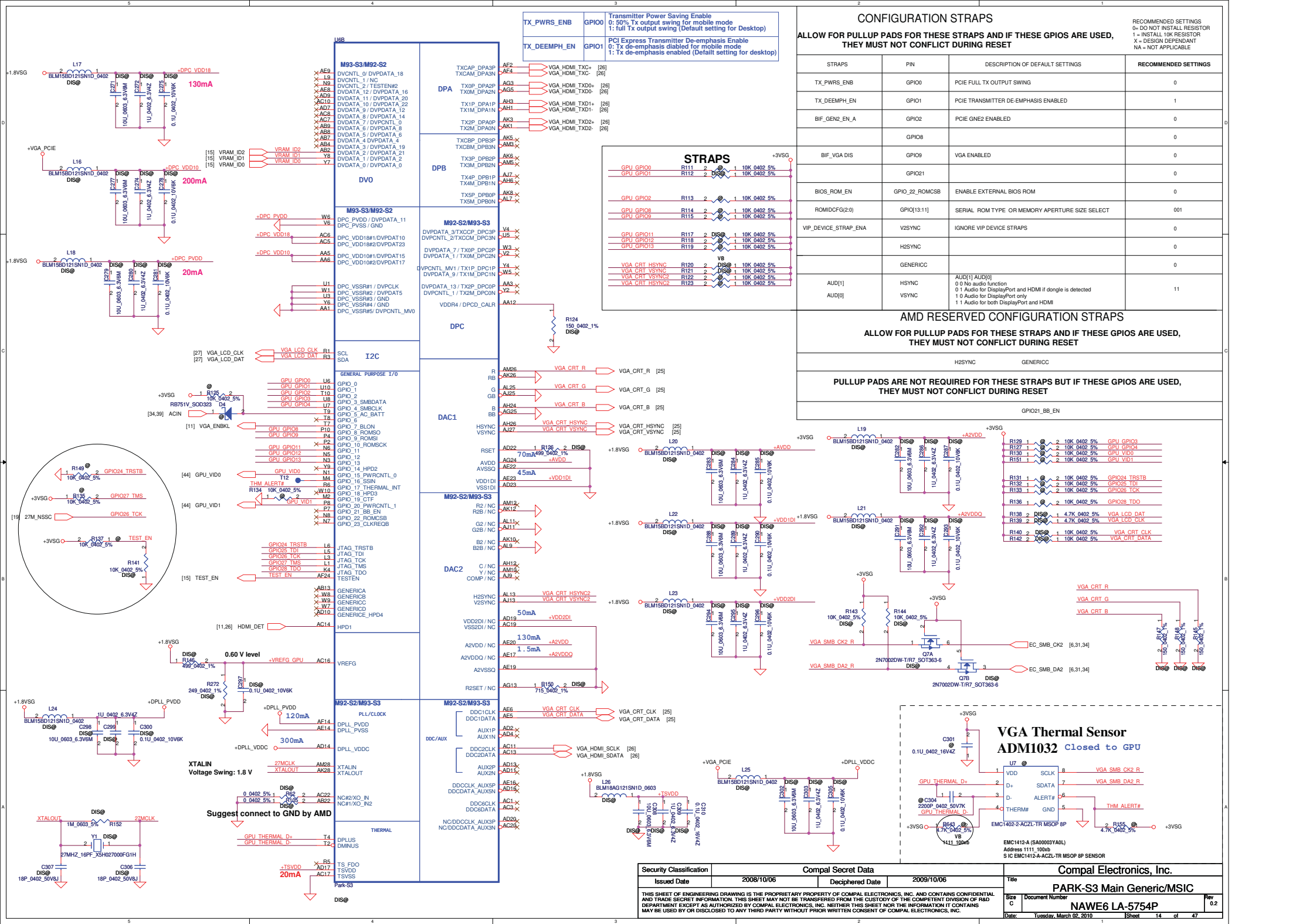


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PCIE LANE REVERSAL



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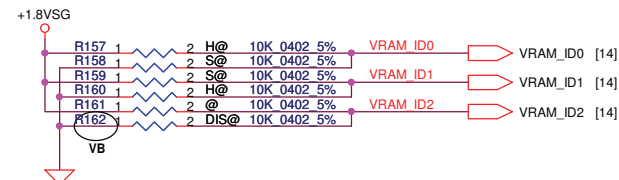


[18] M_DA[63..0] M_DA[63..0]
[18] M_MA[13..0] M_MA[13..0]
[18] M_DQM[7..0] M_DQM[7..0]
[18] M_DQS[7..0] M_DQS[7..0]
[18] M_DQS#[7..0] M_DQS#[7..0]

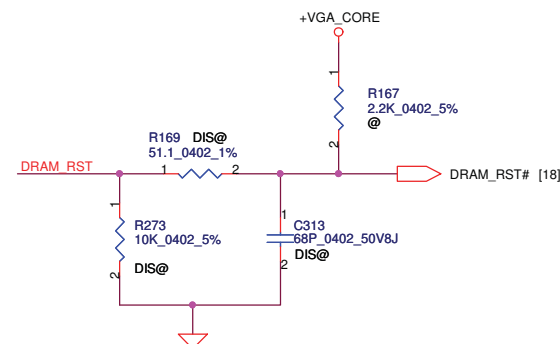
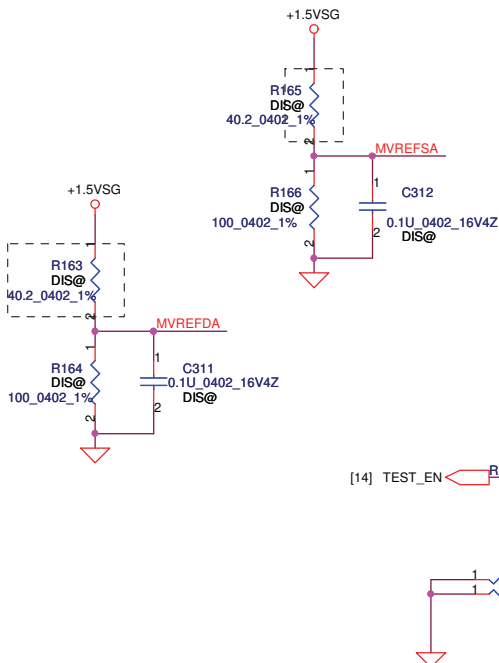
M_DA0 K27 DQA_0
M_DA1 J29 DQA_1
M_DA2 H30 DQA_2
M_DA3 H32 DQA_3
M_DA4 G29 DQA_4
M_DA5 F28 DQA_5
M_DA6 F32 DQA_6
M_DA7 F30 DQA_7
M_DA8 C30 DQA_8
M_DA9 F27 DQA_9
M_DA10 A28 DQA_10
M_DA11 C28 DQA_11
M_DA12 E27 DQA_12
M_DA13 G26 DQA_13
M_DA14 D26 DQA_14
M_DA15 F25 DQA_15
M_DA16 A25 DQA_16
M_DA17 C25 DQA_17
M_DA18 E25 DQA_18
M_DA19 D24 DQA_19
M_DA20 E23 DQA_20
M_DA21 F23 DQA_21
M_DA22 D22 DQA_22
M_DA23 F21 DQA_23
M_DA24 E21 DQA_24
M_DA25 D20 DQA_25
M_DA26 F19 DQA_26
M_DA27 D18 DQA_27
M_DA28 F17 DQA_28
M_DA29 C17 DQA_29
M_DA30 A17 DQA_30
M_DA31 C17 DQA_31
M_DA32 E17 DQA_32
M_DA33 D16 DQA_33
M_DA34 F15 DQA_34
M_DA35 A15 DQA_35
M_DA36 D14 DQA_36
M_DA37 F13 DQA_37
M_DA38 A13 DQA_38
M_DA39 C13 DQA_39
M_DA40 E13 DQA_40
M_DA41 A11 DQA_41
M_DA42 C11 DQA_42
M_DA43 F11 DQA_43
M_DA44 A9 DQA_44
M_DA45 C9 DQA_45
M_DA46 F9 DQA_46
M_DA47 D8 DQA_47
M_DA48 E7 DQA_48
M_DA49 A7 DQA_49
M_DA50 G7 DQA_50
M_DA51 F7 DQA_51
M_DA52 A5 DQA_52
M_DA53 E5 DQA_53
M_DA54 C3 DQA_54
M_DA55 F1 DQA_55
M_DA56 G7 DQA_56
M_DA57 G6 DQA_57
M_DA58 G1 DQA_58
M_DA59 G3 DQA_59
M_DA60 J6 DQA_60
M_DA61 J1 DQA_61
M_DA62 J3 DQA_62
M_DA63 J5 DQA_63

MEMORY INTERFACE

MAA_0 K17 M_MA0
MAA_1 J20 M_MA1
MAA_2 H23 M_MA2
MAA_3 G23 M_MA3
MAA_4 G24 M_MA4
MAA_5 H24 M_MA5
MAA_6 J19 M_MA6
MAA_7 K19 M_MA7
MAA_8 J14 M_MA8
MAA_9 K14 M_MA9
MAA_10 J11 M_MA10
MAA_11 J13 M_MA11
MAA_12 H11 M_MA12
MAA_13/BA2 G11 M_BA2 [18]
MAA_14/BA0 J16 M_BA0 [18]
MAA_15/BA1 L15 M_BA1 [18]
DQMA_0 E32 M_DQM0
DQMA_1 E30 M_DQM1
DQMA_2 A21 M_DQM2
DQMA_3 C21 M_DQM3
DQMA_4 E13 M_DQM4
DQMA_5 D12 M_DQM5
DQMA_6 E3 M_DQM6
DQMA_7 F4 M_DQM7
RDQSA_0 H28 M_DQS0
RDQSA_1 C27 M_DQS1
RDQSA_2 A23 M_DQS2
RDQSA_3 E19 M_DQS3
RDQSA_4 E15 M_DQS4
RDQSA_5 D10 M_DQS5
RDQSA_6 D6 M_DQS6
RDQSA_7 G5 M_DQS7
WDQSA_0 H27 M_DQS#0
WDQSA_1 A27 M_DQS#1
WDQSA_2 C23 M_DQS#2
WDQSA_3 C19 M_DQS#3
WDQSA_4 C15 M_DQS#4
WDQSA_5 E9 M_DQS#5
WDQSA_6 C5 M_DQS#6
WDQSA_7 H4 M_DQS#7
ODTA0 L18 M_ODT0
ODTA1 K16 M_ODT1
CLKA0 H26 M_CLK0
CLKA0B H25 M_CLK#0
CLKA1 G9 M_CLK1
CLKA1B H9 M_CLK#1
RASA0B G22 M_RAS#0
RASA1B G17 M_RAS#1
CASA0B G19 M_CAS#0
CASA1B G16 M_CAS#1
CSA0B_0 H22 M_CS#0
CSA0B_1 J22 M_CS#1
CSA1B_0 G13 M_CS#1
CSA1B_1 K13 M_CS#1
CKEA0 K20 M_CKE0
CKEA1 J17 M_CKE1
WEA0B G25 M_WE#0
WEA1B H10 M_WE#1
PX_EN AB16
RSVD#2 G14
RSVD#3 G20 M_MA13



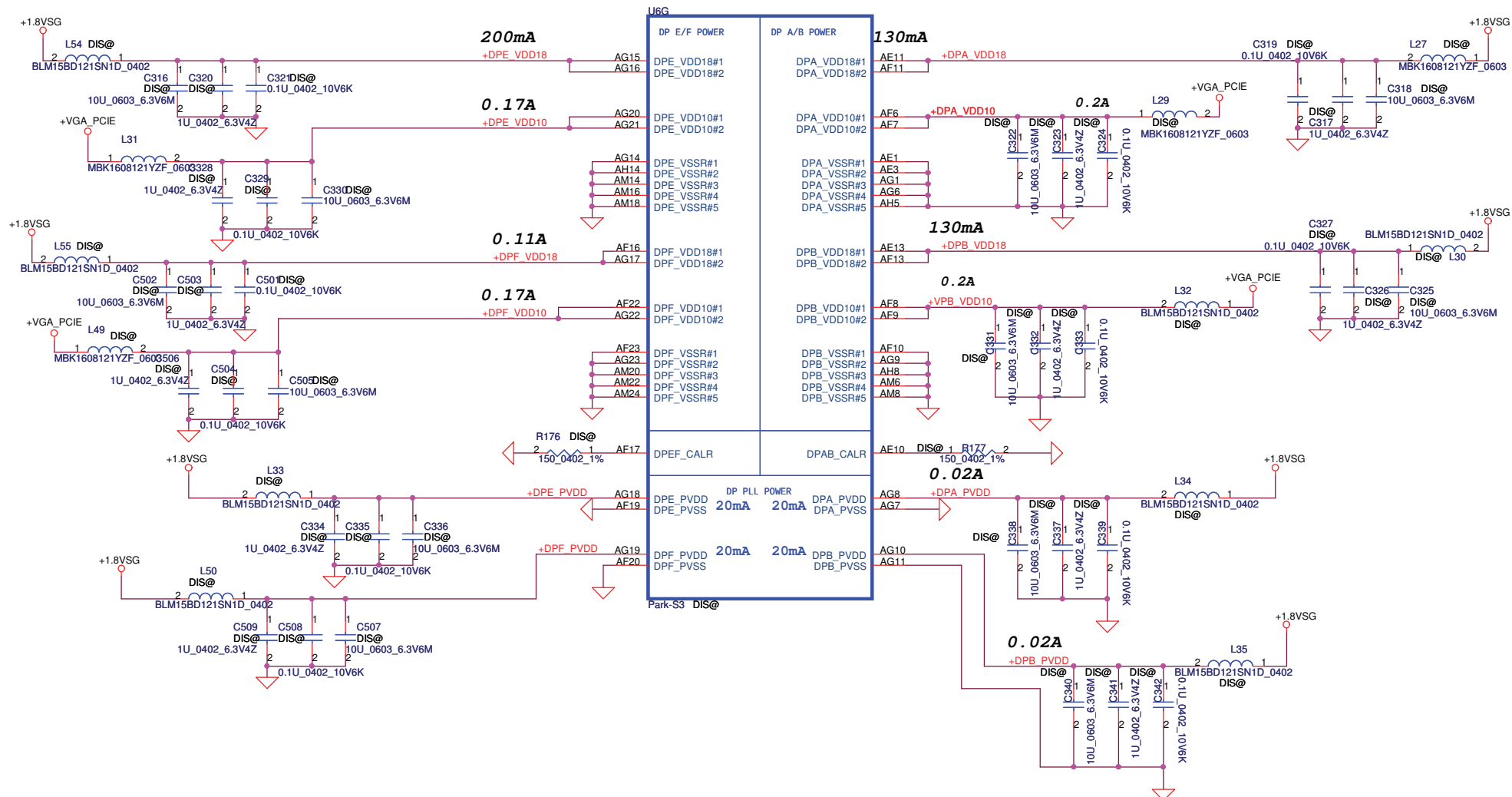
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix H5TQ1G63BFR-12C	1	0	0
Samsung K4W1G1646E-HC12	0	1	0



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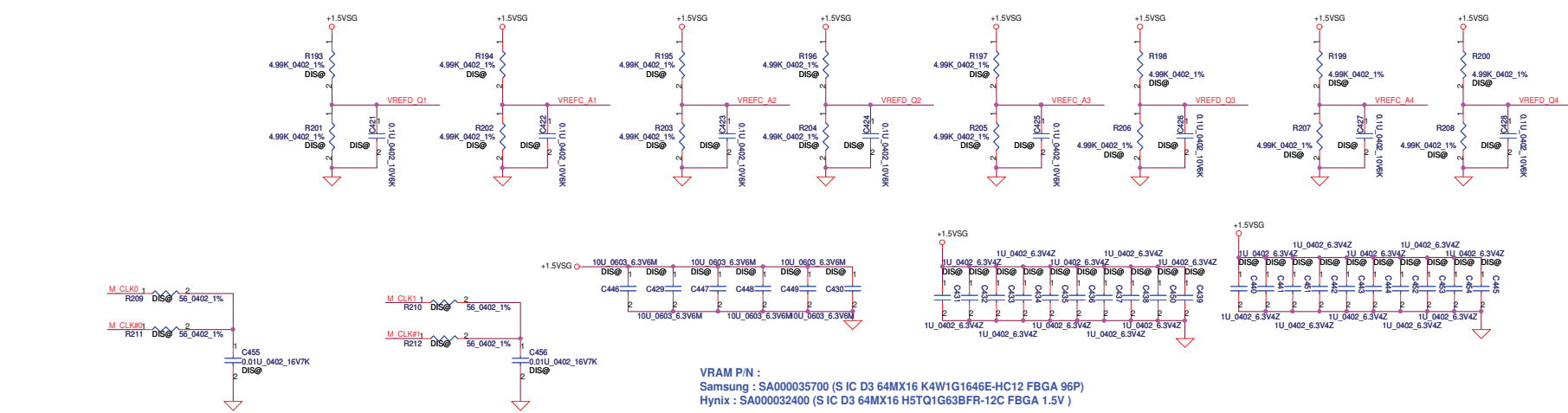
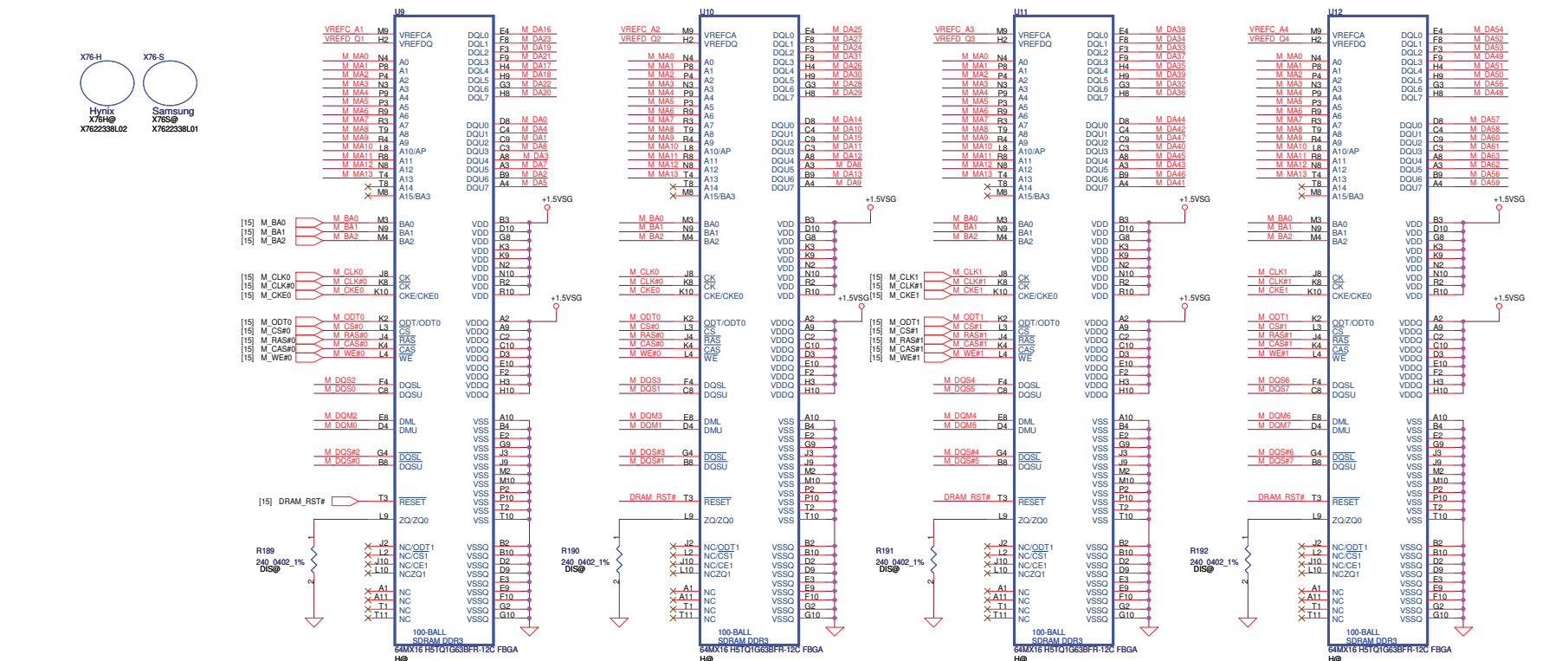
DPE_VDD10
DPF_VDD10

Park-S3: TMD5/DP=110mA@1.0V : LVDS=120mA@1.0V



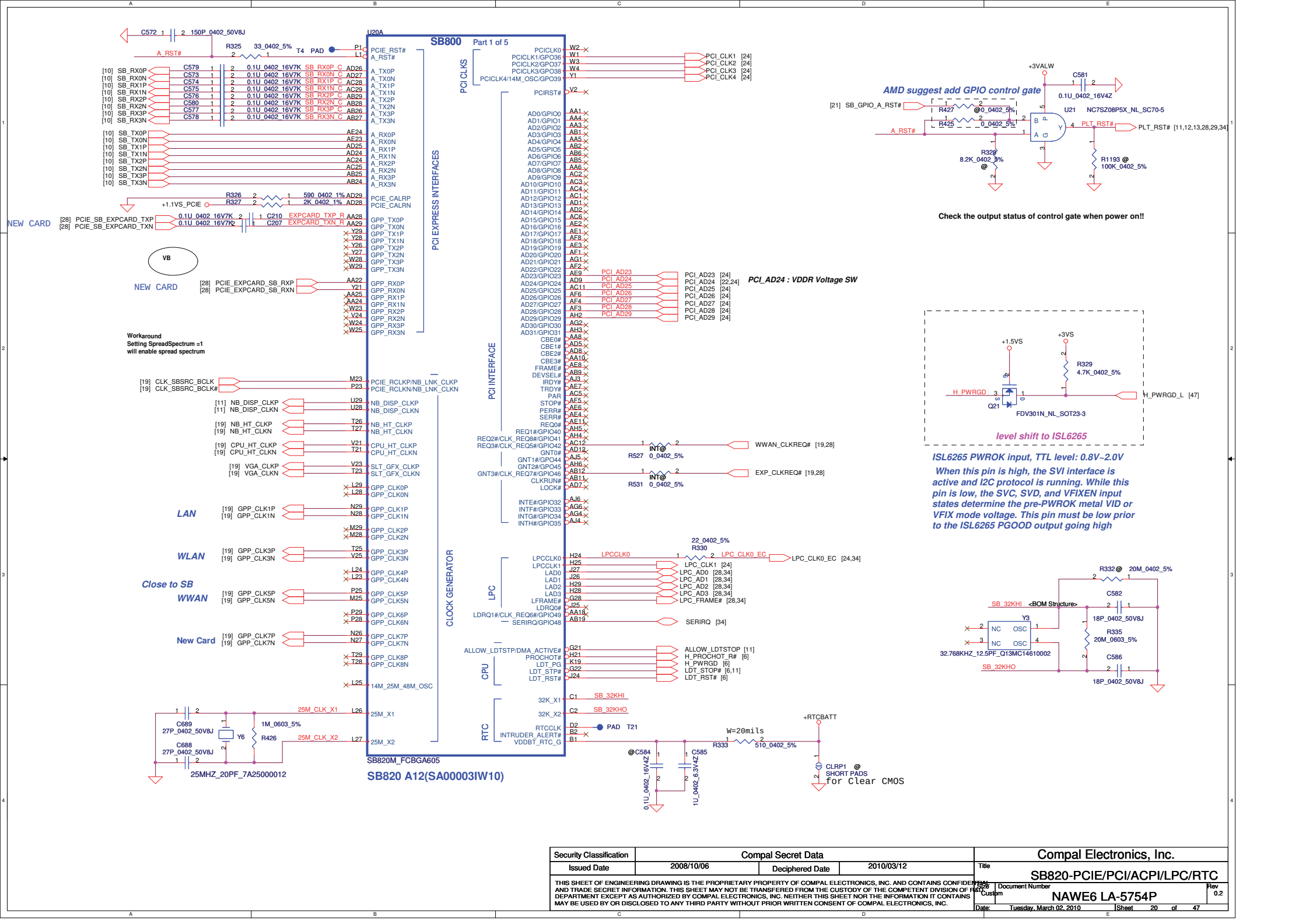
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	PARK-S3 DPX Power
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				Date:	Monday, March 01, 2010
				Sheet	16 of 47

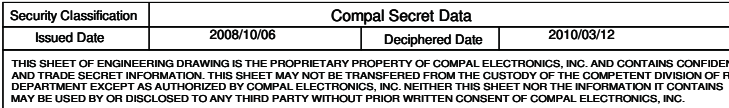
[15] M_DA[63..0] M_DA[63..0]
 [15] M_MA[13..0] M_MA[13..0]
 [15] M_DQM[7..0] M_DQM[7..0]
 [15] M_DQS[7..0] M_DQS[7..0]
 [15] M_DQS# [7..0] M_DQS# [7..0]



VRAM P/N :
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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Size	C	Document Number	NAWE6 LA-5754P	
Date	Monday, March 01, 2010	Sheet	18	of 47

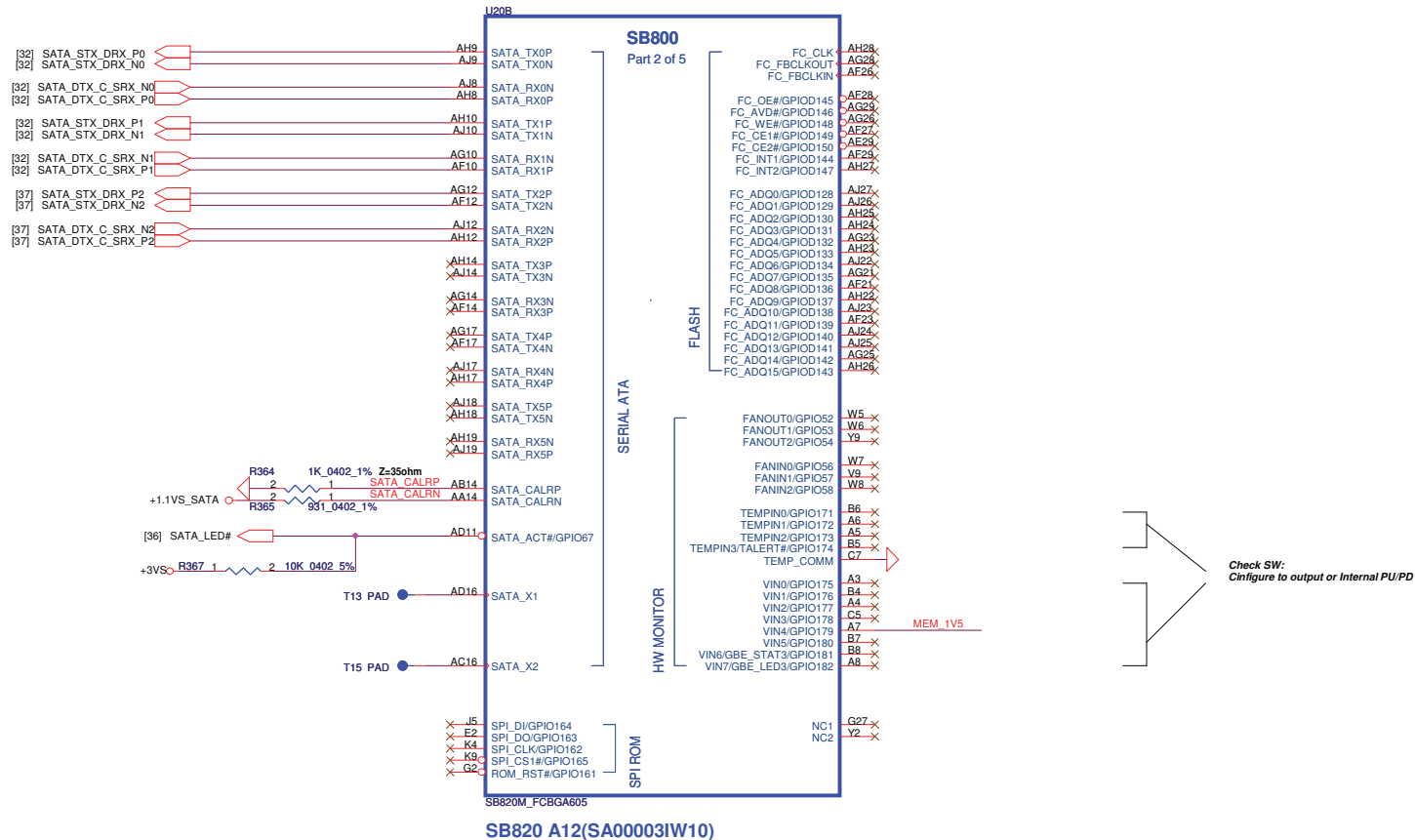




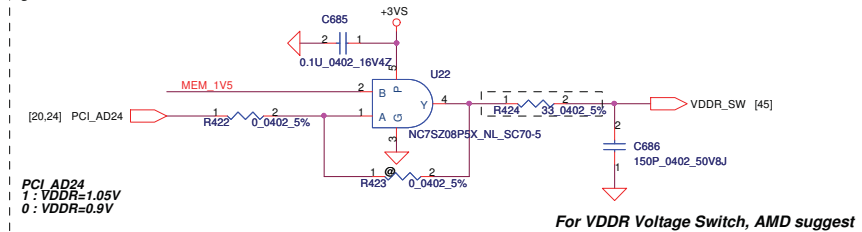
HDD

ODD

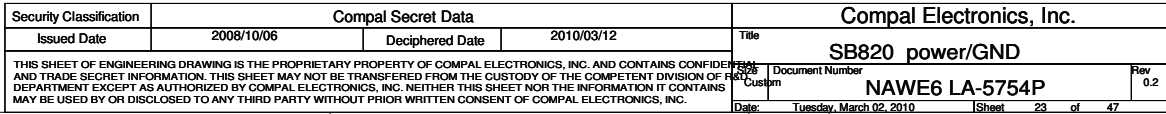
e-SATA



MEM_1V5 is for gating the
glitch on PCL_AD24



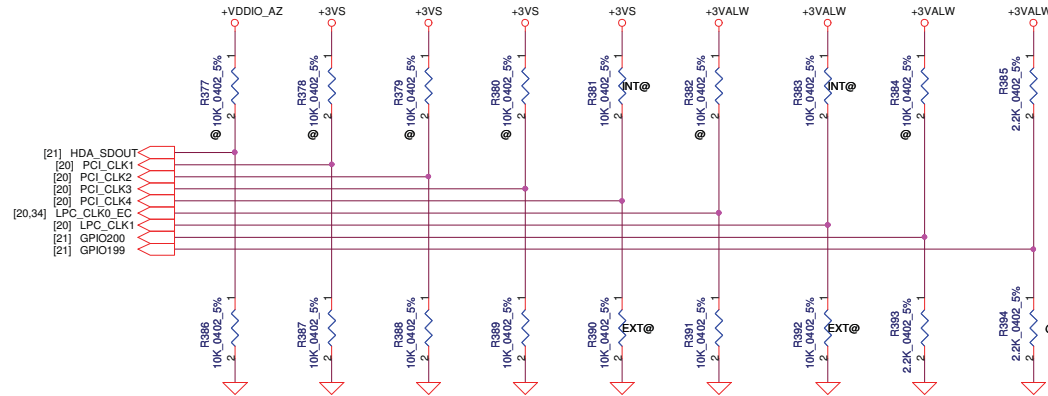
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Issued Date		2008/10/06		Deciphered Date		2010/03/12		Title					
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								Document Number				Rev	
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REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	CPU/HT CLK SEL Disable	EC DISABLE	CLOCKGEN DISABLE		
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		



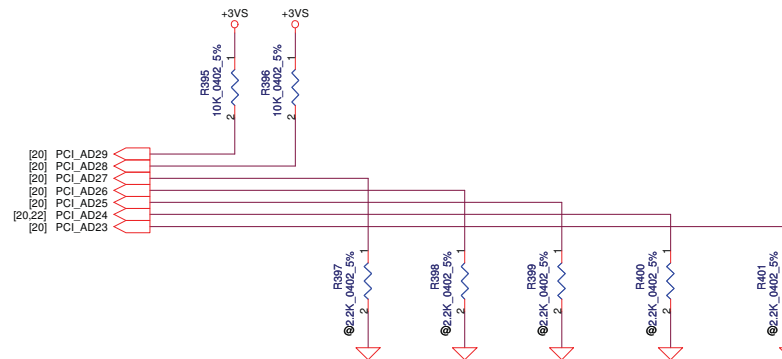
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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				SB820 STRAPS	0.2
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CRT Connector

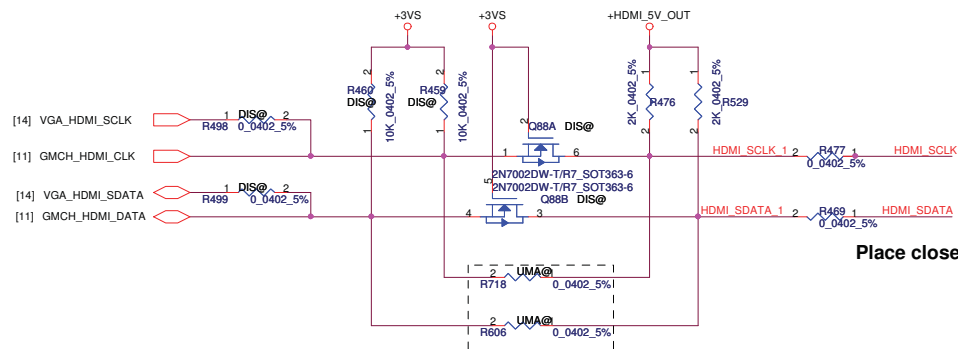
The schematic diagram illustrates the digital logic circuit for the CRT control system. It features two 74VHC00 inverters (Q87A, Q87B) and two 74VHC04 inverters (Q87C, Q87D). The inputs are DSUB_12 and DSUB_15. The outputs are CRT_DATA and CRT_CLK. The circuit is powered by +CRT_VCC and +3VS. The components are labeled with their part numbers and values: R457 (4.7K_0402_5%), R553 (4.7K_0402_5%), R676 (4.7K_0402_5%), and R544 (4.7K_0402_5%).

[1]	GMCH_CRT_R		GMCH CRT R	R677	2	UMA@	1	0	0.402	5%	CRT R
[1]	GMCH_CRT_G		GMCH CRT G	R542	2	UMA@	1	0	0.402	5%	CRT G
[1]	GMCH_CRT_B		GMCH CRT B	R679	2	UMA@	1	0	0.402	5%	CRT B
[11,12]	GMCH_CRT_HSYNC		GMCH CRT HSYNC	R547	2	UMA@	1	0	0.402	5%	CRT HSYNC
[11,12]	GMCH_CRT_VSYNC		GMCH CRT VSYNC	R543	2	UMA@	1	0	0.402	5%	CRT VSYNC
[1]	GMCH_CRT_DATA		GMCH CRT DATA	R546	2	UMA@	1	0	0.402	5%	CRT DATA
[1]	GMCH_CRT_CLK		GMCH CRT CLK	R678	2	UMA@	1	0	0.402	5%	CRT CLK

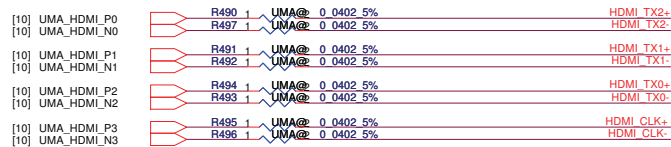
[14]	VGA_CRT_R		VGA CRT R	R539	2 DISE	1	0	0.402	5%	CRT R
[14]	VGA_CRT_G		VGA CRT G	R562	2 DISE	1	0	0.402	5%	CRT G
[14]	VGA_CRT_B		VGA CRT B	R554	2 DISE	1	0	0.402	5%	CRT B
[14]	VGA_CRT_HSYNC		VGA CRT HSYNC	R535	2 DISE	1	0	0.402	5%	CRT HSYNC
[14]	VGA_CRT_VSYNC		VGA CRT VSYNC	R557	2 DISE	1	0	0.402	5%	CRT VSYNC
[14]	VGA_DATA_DATA		VGA CRT DATA	R538	2 DISE	1	0	0.402	5%	CRT DATA
[14]	VGA_CRT_CLK		VGA CRT CLK	R556	2 DISE	1	0	0.402	5%	CRT CLK

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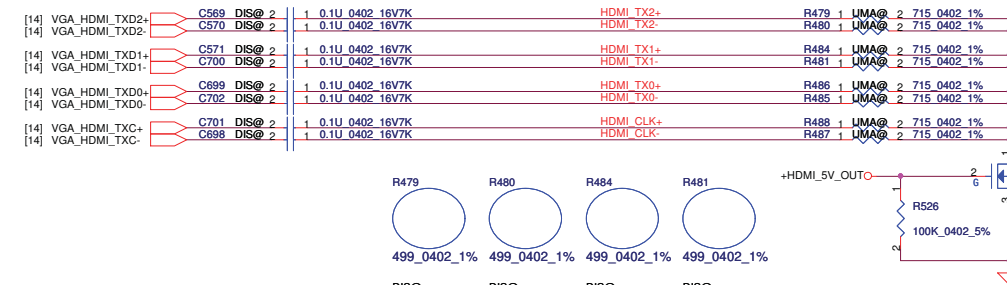
Compal Electronics, Inc.			
Title			
CRT Connector			
IDENTIFICATION OF REVISIONS	Document Number	NAWE6 LA-5754P	Rev 0.2
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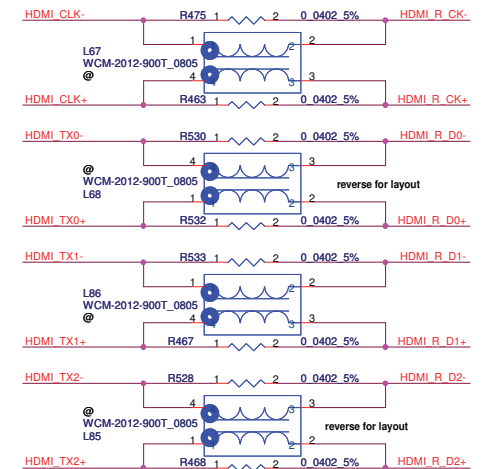
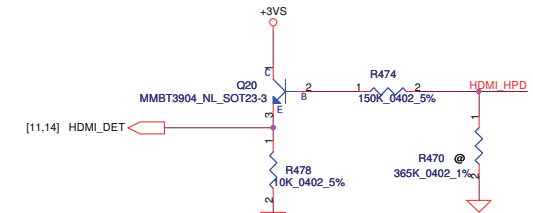
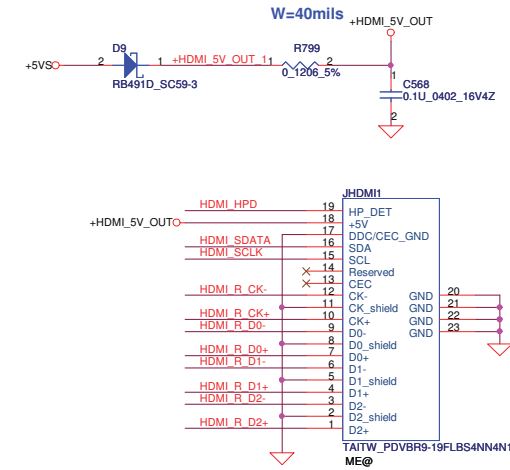
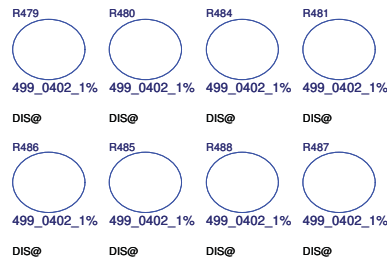
Place closed to JHDMI1



Place closed to JHDMI1

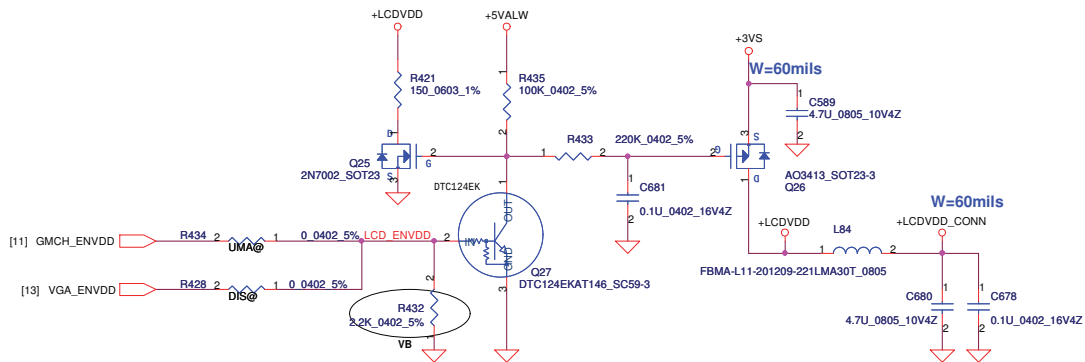


UMA use 715 ohm
VGA use 499 ohm

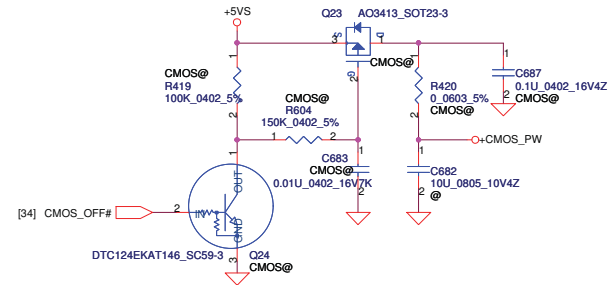


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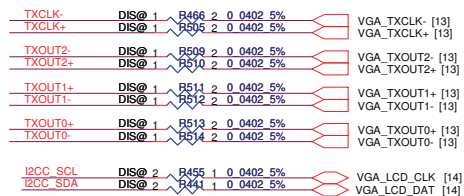
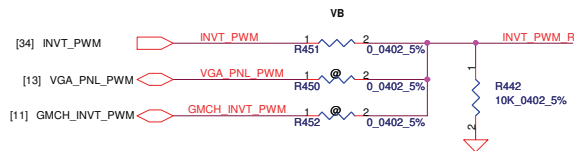
LCD POWER CIRCUIT



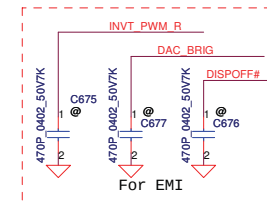
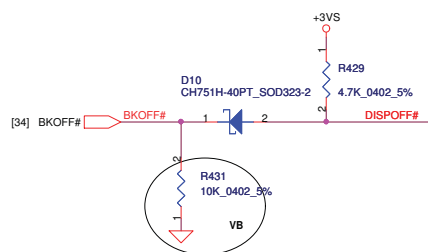
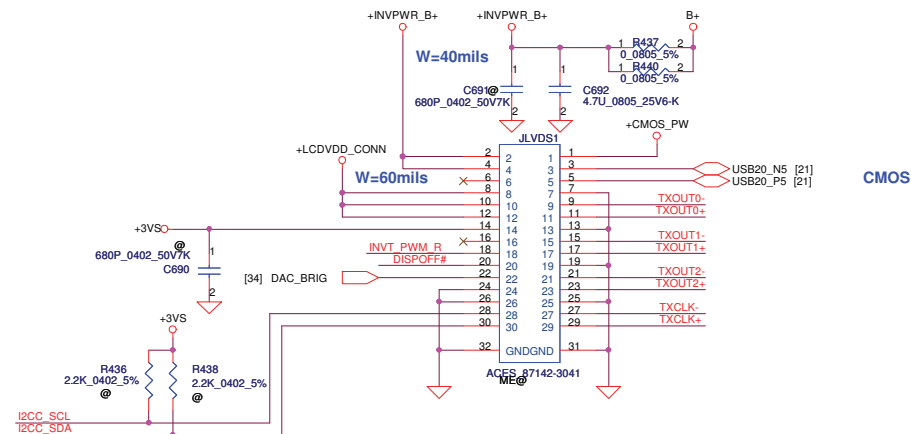
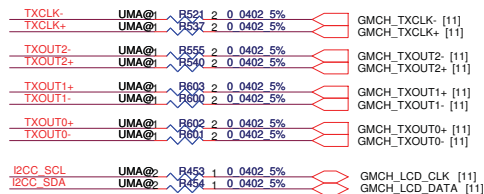
CMOS Camera



VGA ONLY

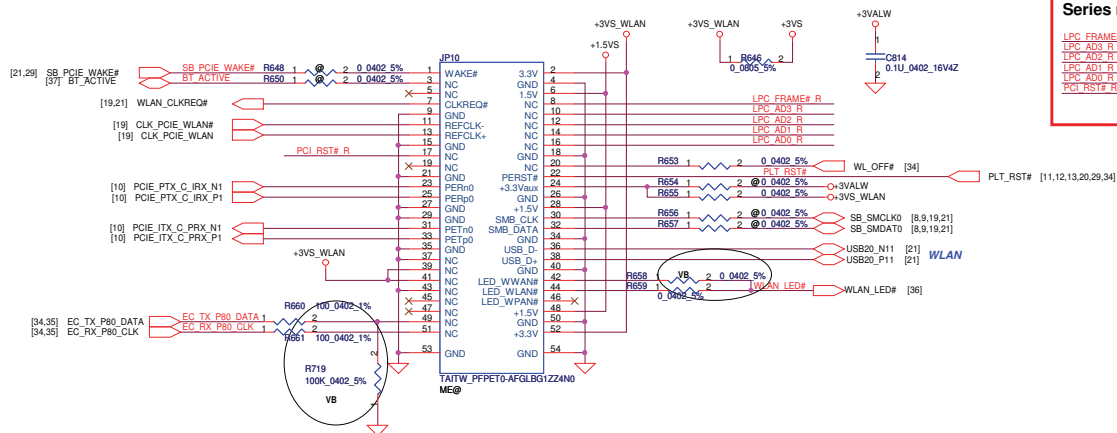


UMA ONLY



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Mini-Express Card for WLAN/WiMAX(Half)

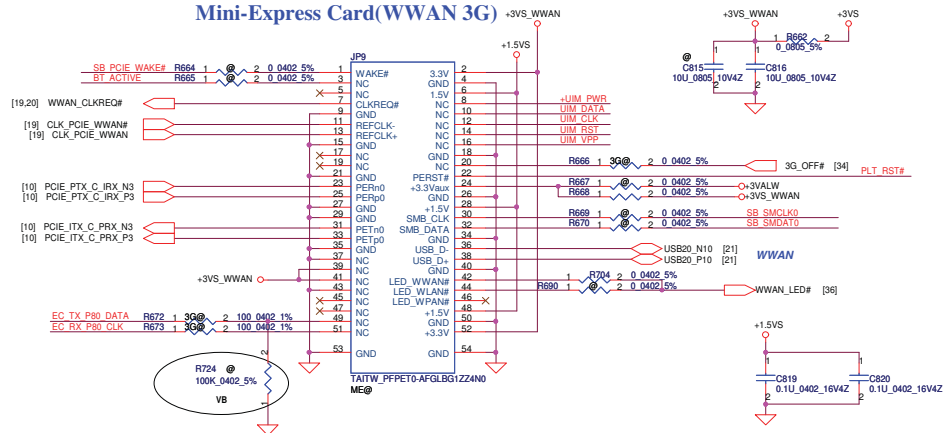


**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

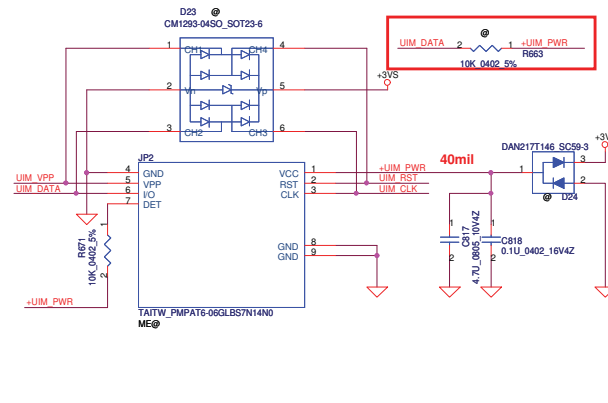
Source	Destination	Count	Rate	Destination	Count	Rate
LPC_FRAME# R	R644	1	2 0 0402 5%	LPC_FRAME#	1	20.34
LPC_AD3 R	R645	1	2 0 0402 5%	LPC_AD3	1	20.34
LPC_AD2 R	R647	1	2 0 0402 5%	LPC_AD2	1	20.34
LPC_AD1 R	R649	1	2 0 0402 5%	LPC_AD1	1	20.34
LPC_AD0 R	R651	1	2 0 0402 5%	LPC_AD0	1	20.34
PLT_RST# R	R652	1	2 0 0402 5%	PLT_RST#	1	11.12.13.20.29.34

Mini-Express Card for WWAN(Full)

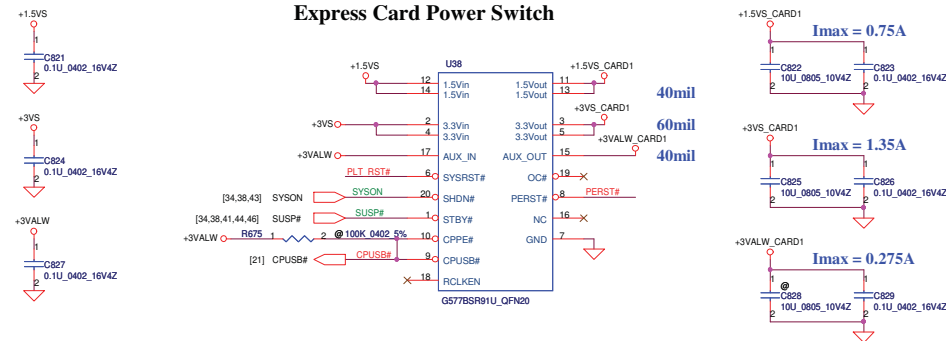
Mini-Express Card(WWAN 3G) +3VS_WWAN 8



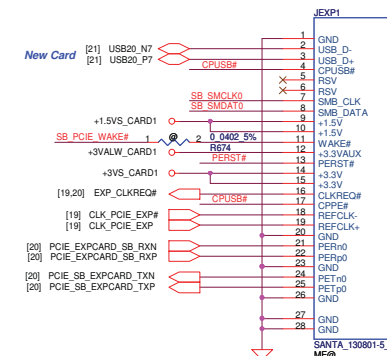
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



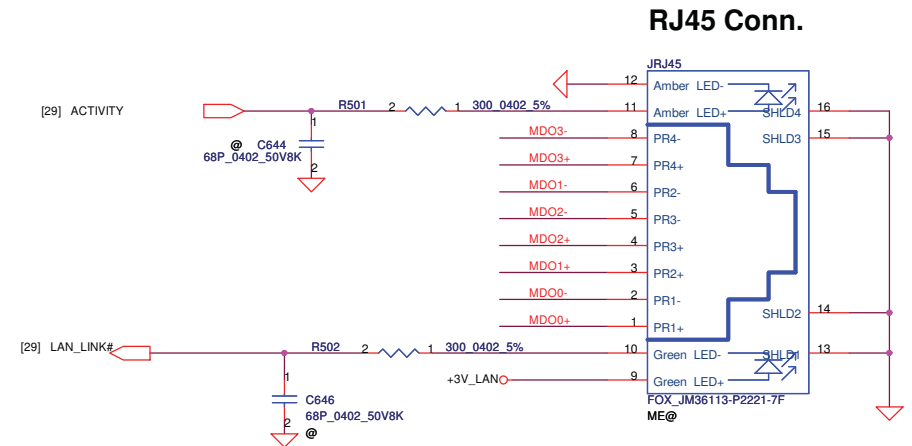
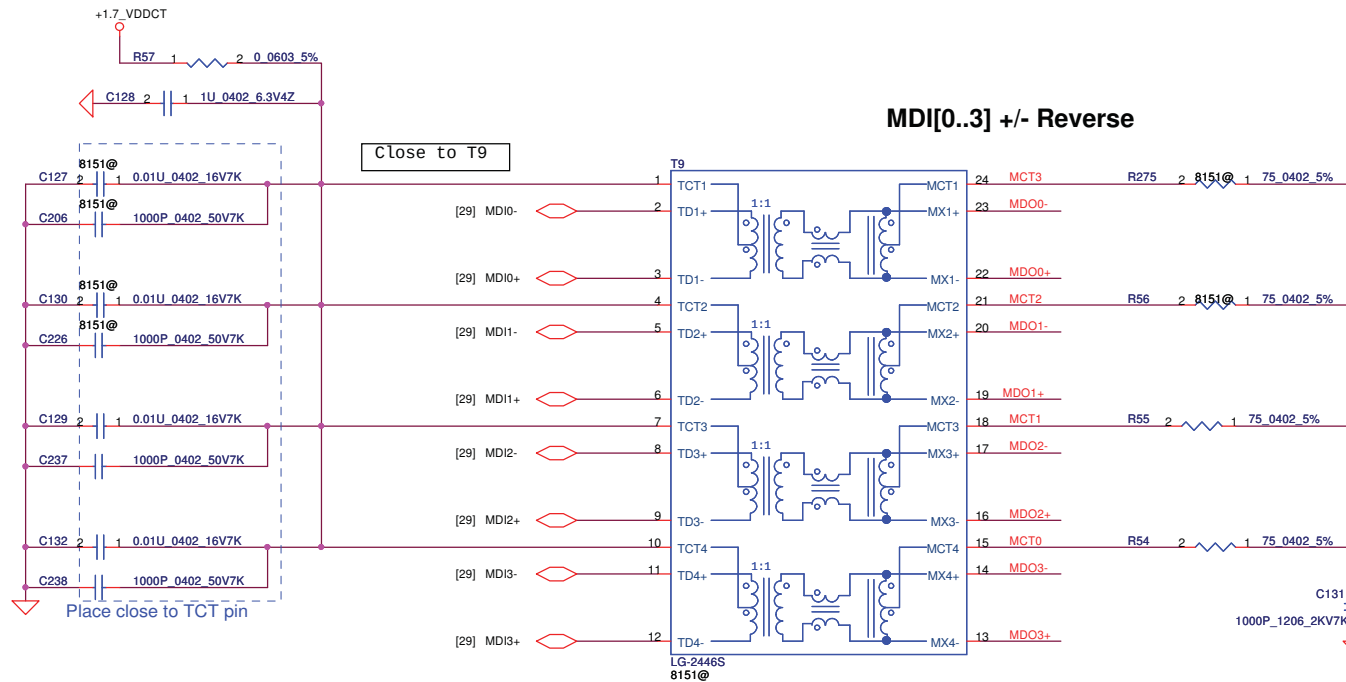
Express Card Power Switch



New Card 34mm Socket (Left/TOP)

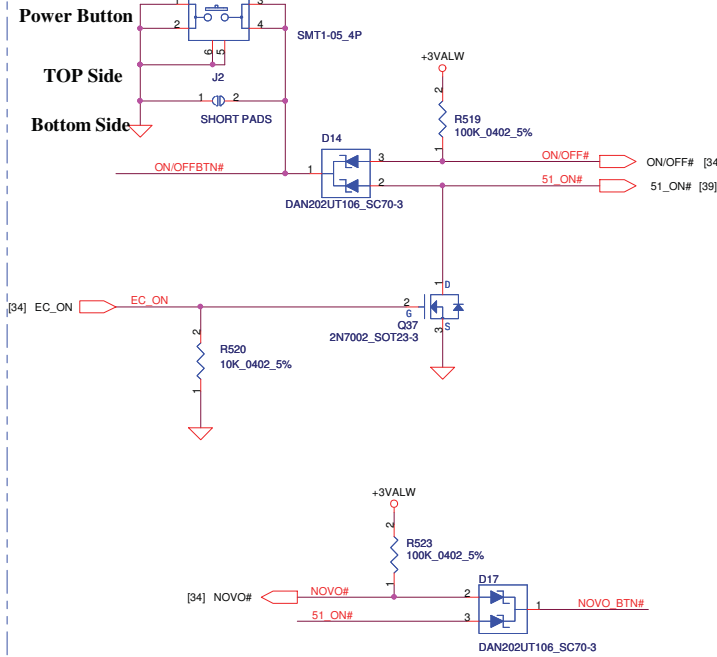


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						<i>Mini-Card/Nwe Card/SIM</i>		
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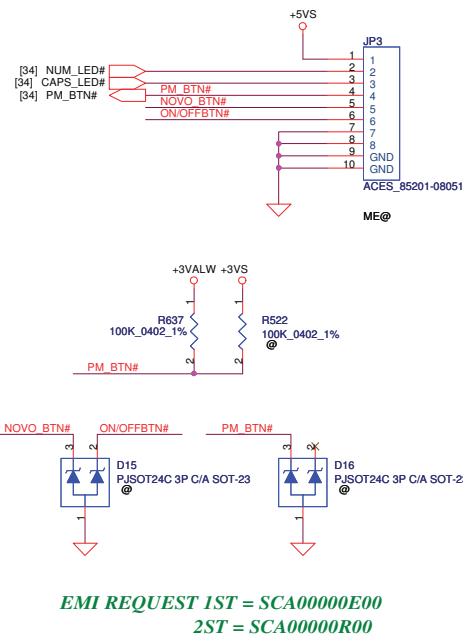


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Size	Custom	Document Number	NAWE6 LA-5754P		Rev 0.2
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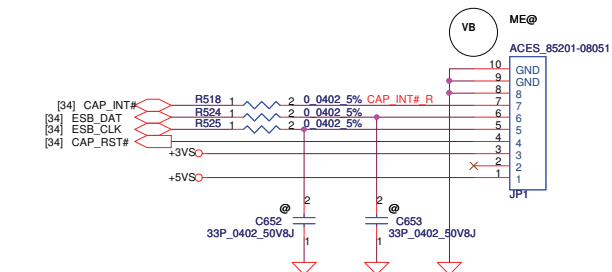
ON/OFF switch



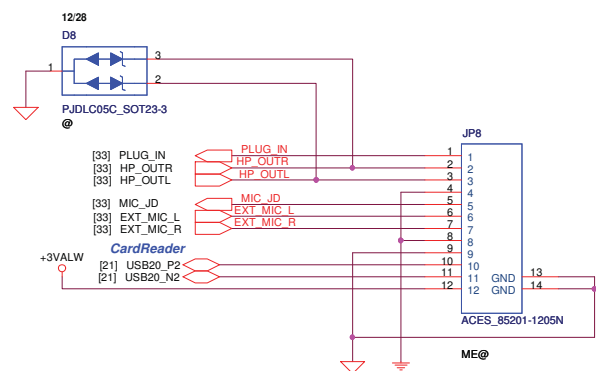
Power Bottom Board Conn. 8pin



Cap Sensor Board Conn. 8pin

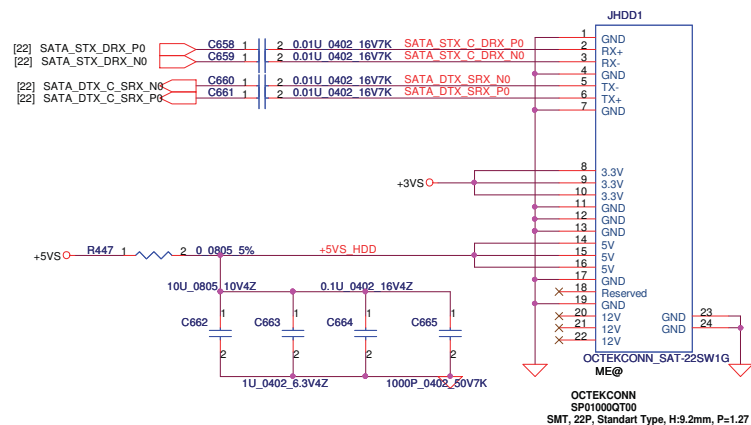
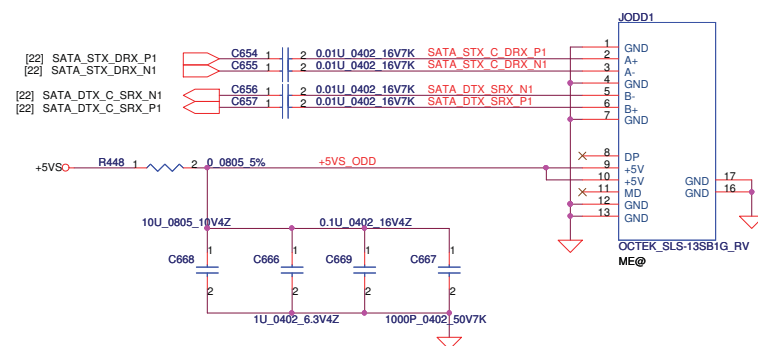


Card Reader/Audio Jack SB CONN



SATA HDD Conn.

SATA ODD Conn.

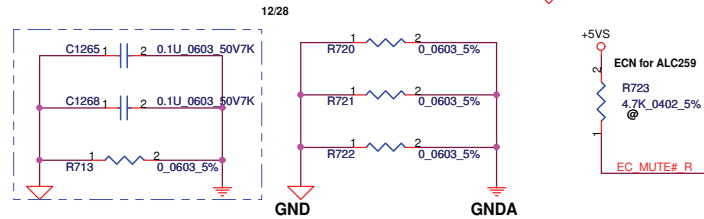
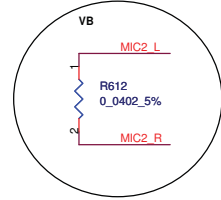
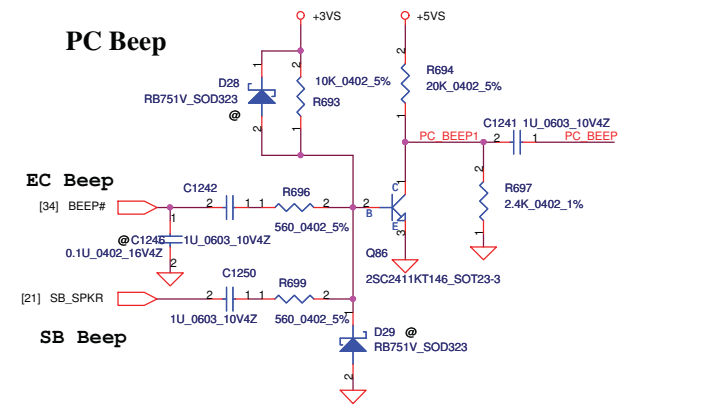


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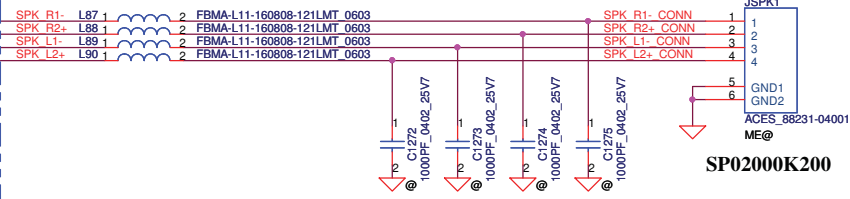
PC BEEP

EC BEEP

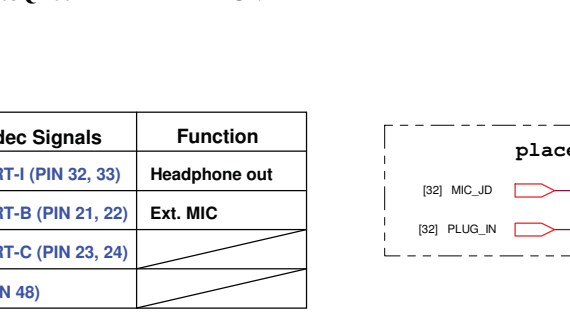
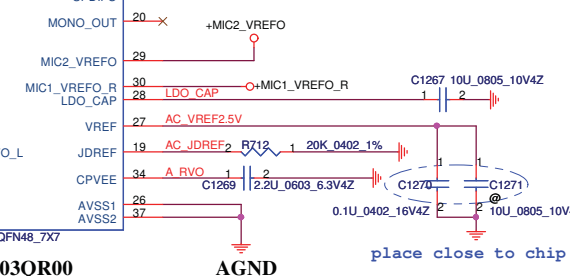
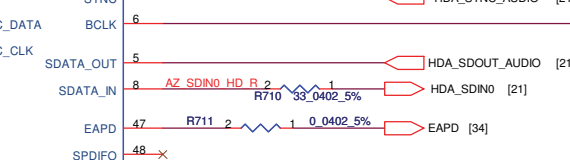
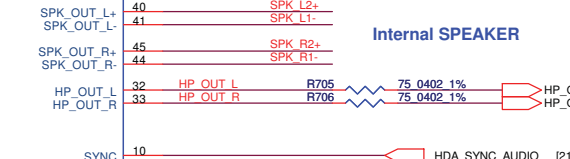
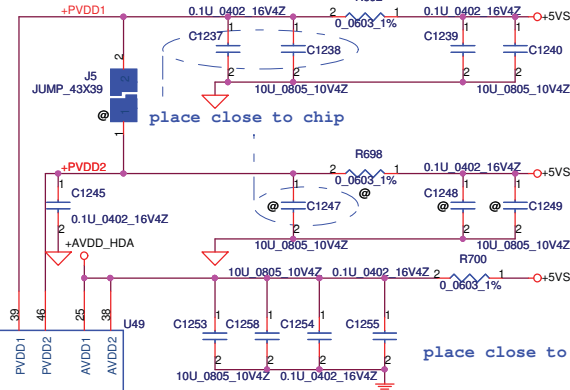
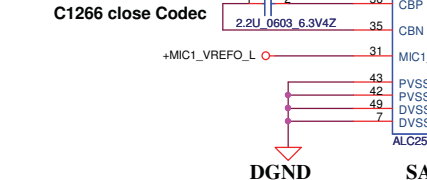
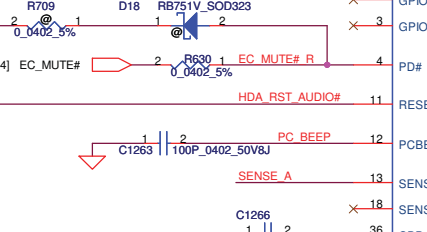
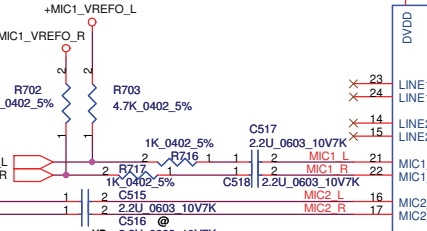
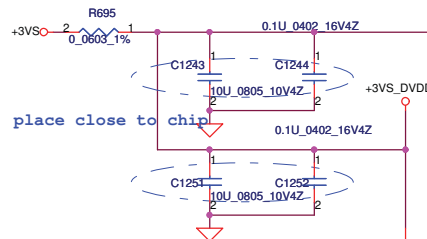
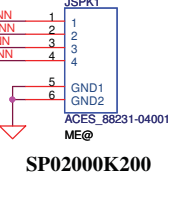
SB BEEP



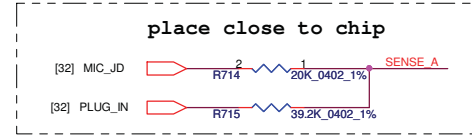
wide 20MIL



External MIC



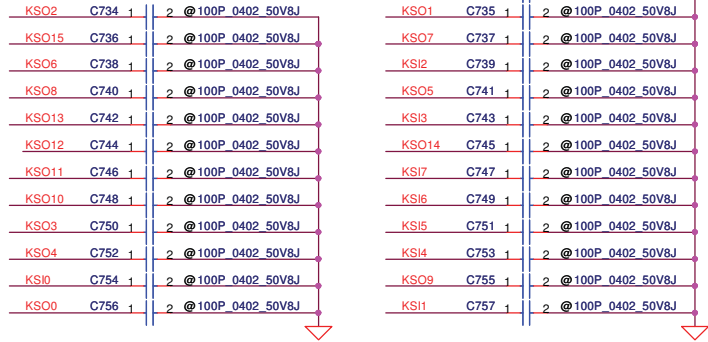
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	



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Size Custom				Document Number				NAWE6 LA-5754P			
Date: tuesday, March 02, 2010				Sheet 33 of 47				Rev 0.2			

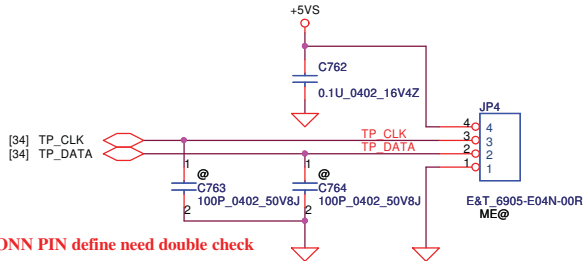
INT_KBD Conn.

KSI[0..7] [34]
KSO[0..17] [34]

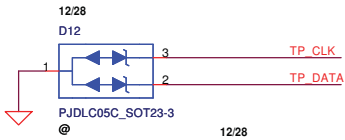


CONN PIN define need double check

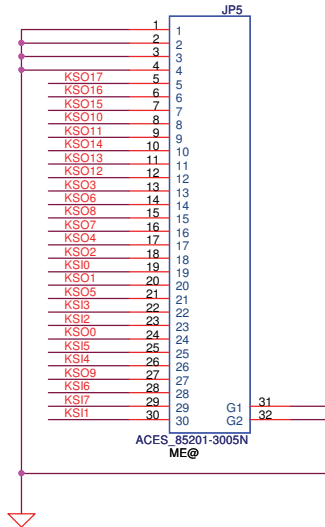
To TP/B Conn.



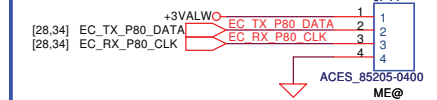
CONN PIN define need double check



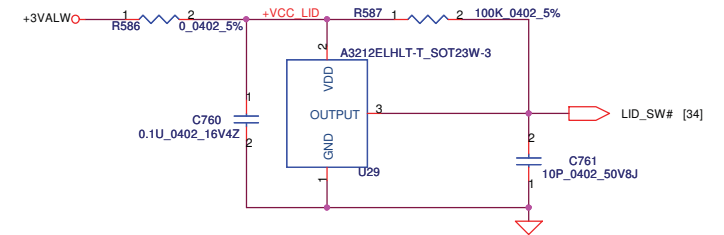
reversal of NIWE1



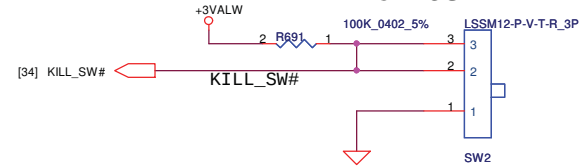
EC DEBUG PORT



Lid Switch



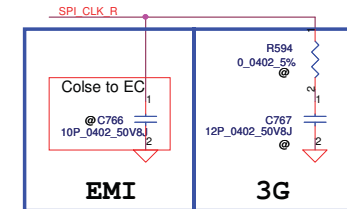
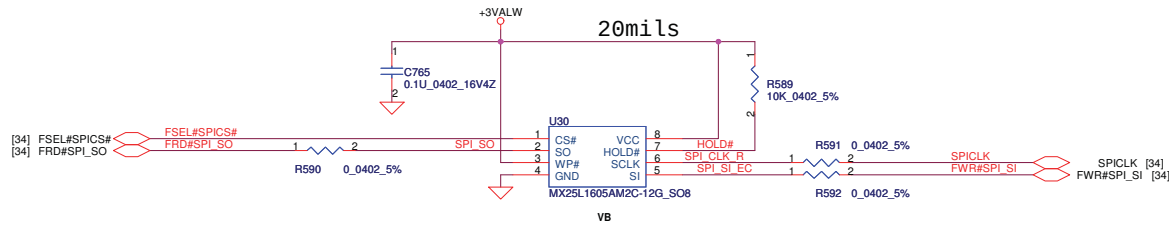
Kill Switch



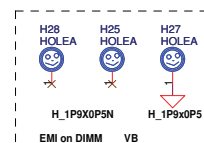
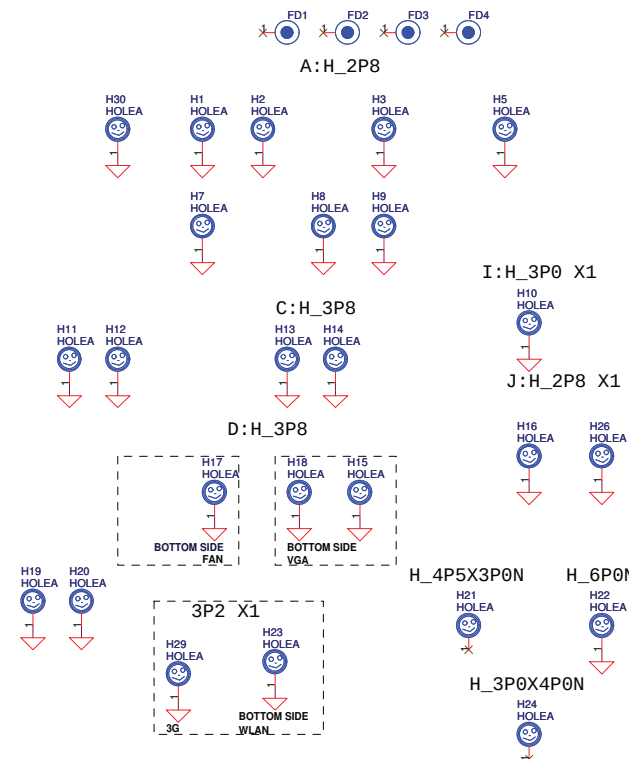
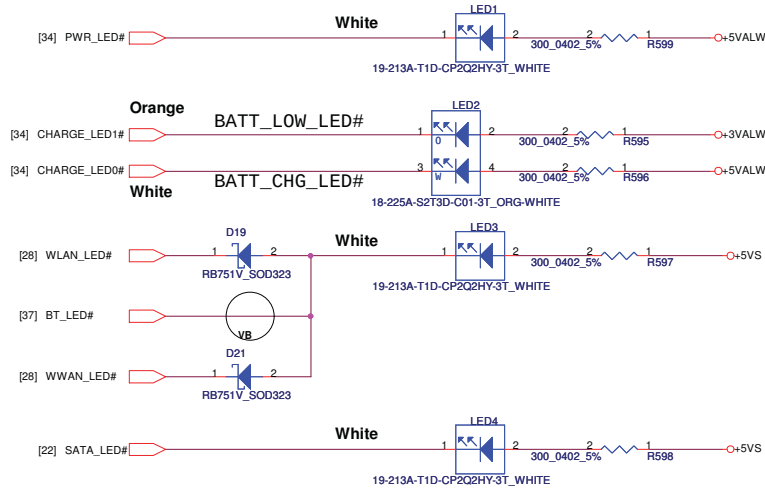
Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

SA00002TO00 package 200mil
S IC FL 16MBIT MX25L1605AM2C-12G SO8 ROM

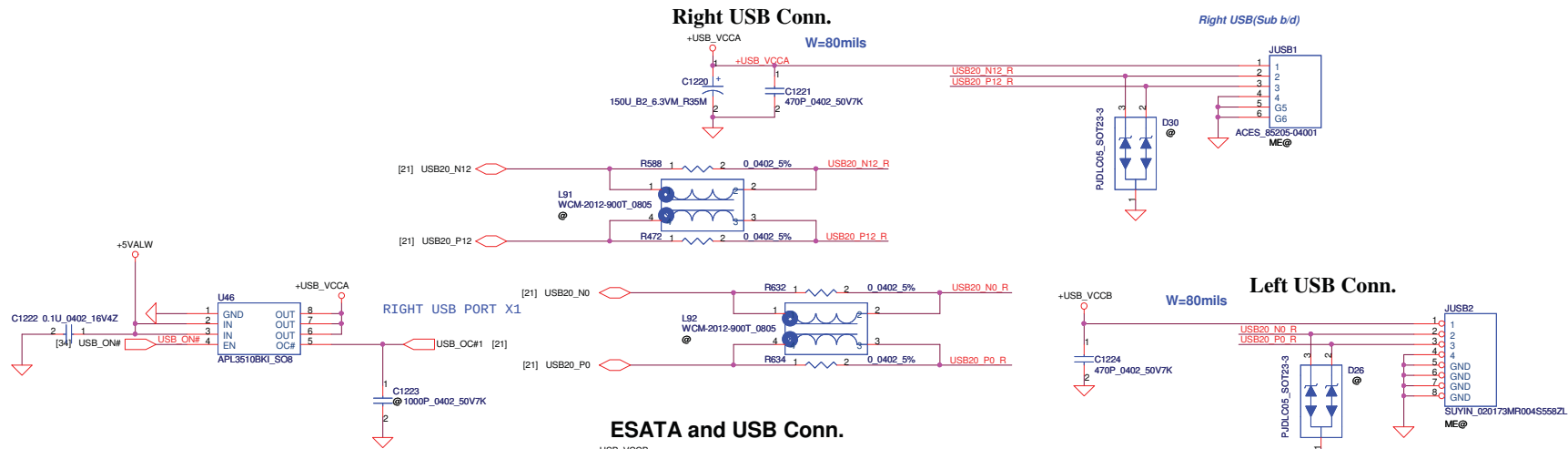


LED

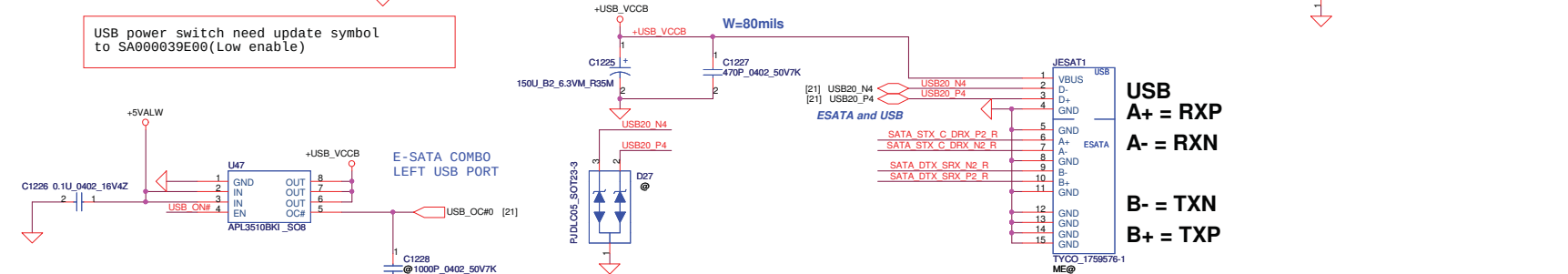


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Document Number				Rev
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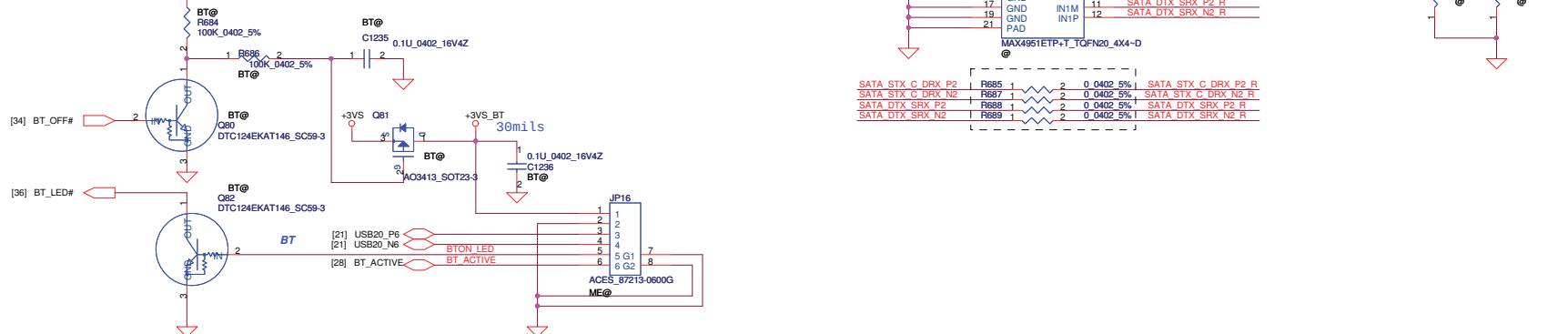
Right USB Conn.



ESATA and USB Conn.

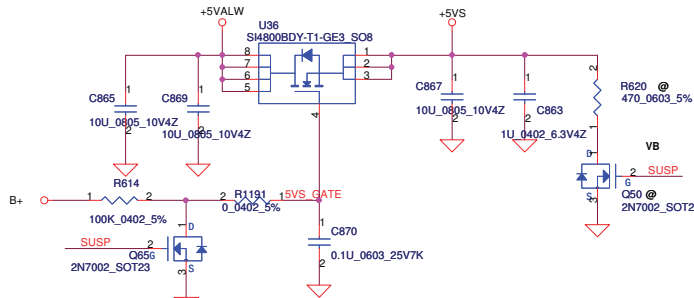


BT MODULE CONN

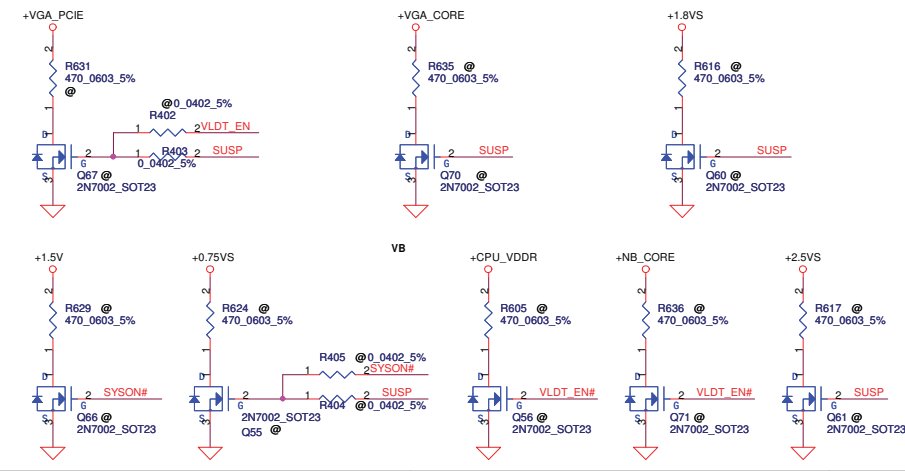
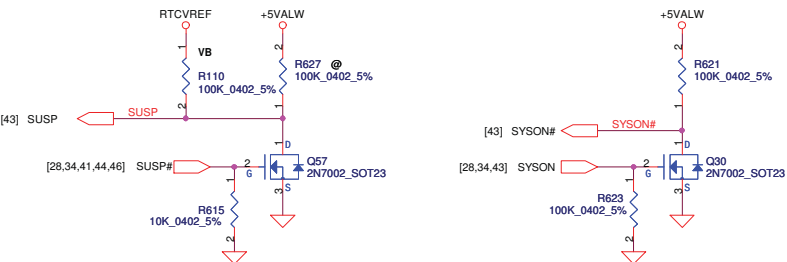
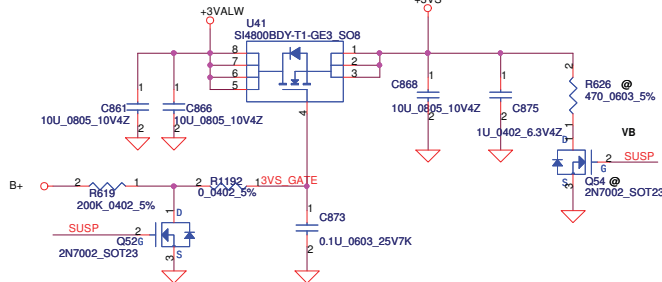


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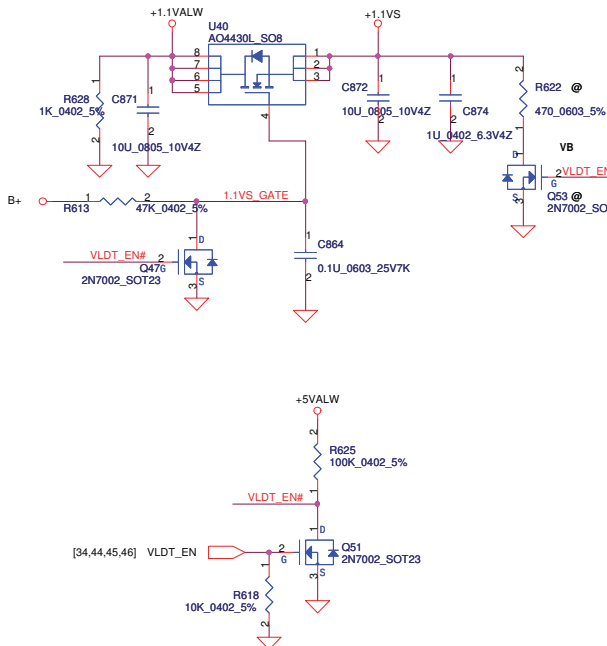
+5VALW TO +5VS



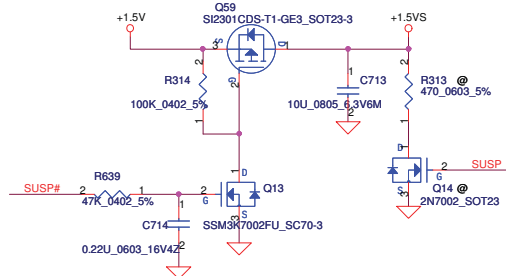
+3VALW TO +3VS



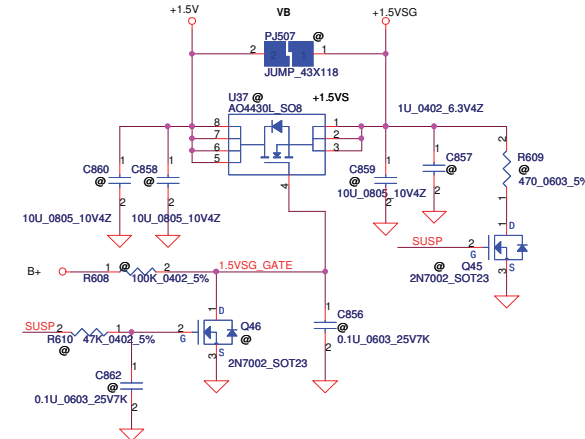
+1.1VALW TO +1.1VS (NB HT)



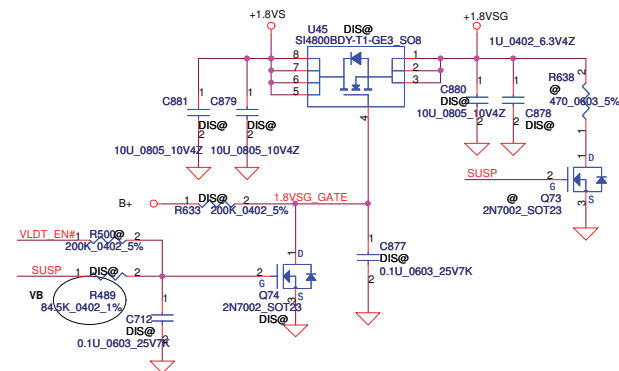
+1.5VS



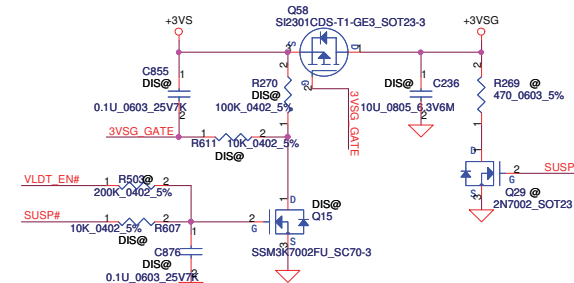
+1.5V to +1.5VSG



+1.8VS to +1.8VSG

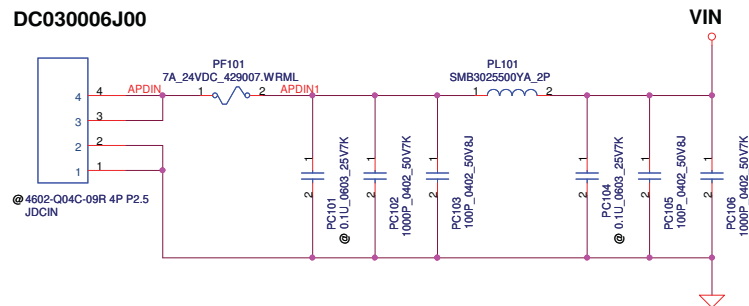


+3VSG



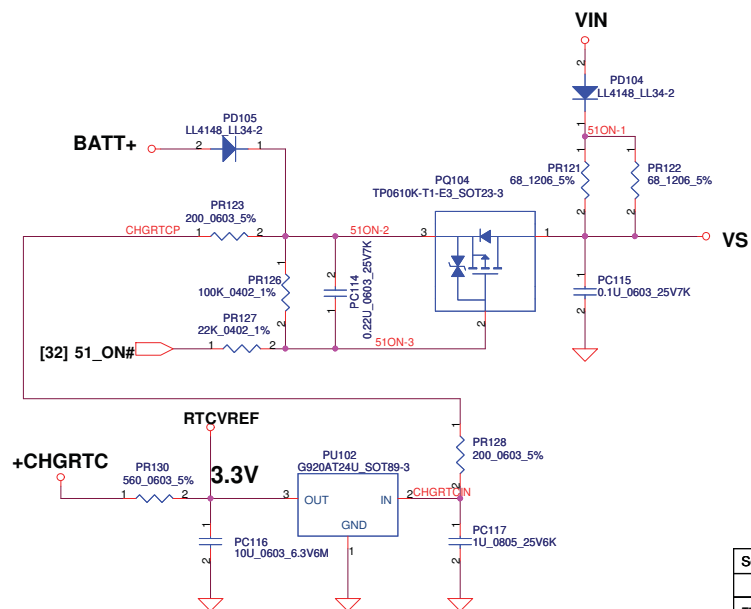
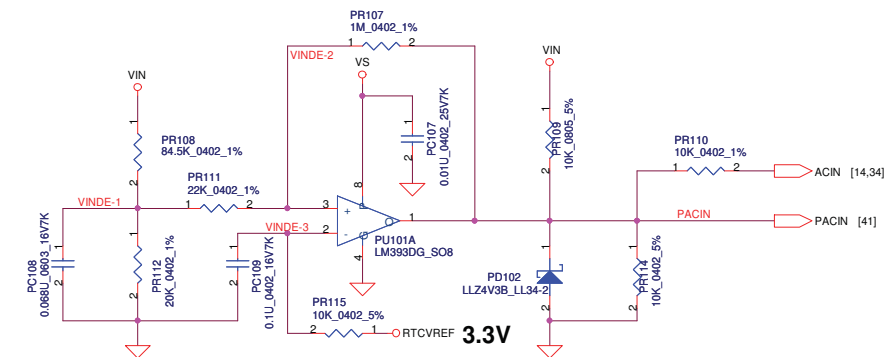
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Issued Date	2008/10/06	Deciphered Date	2010/03/12	DC Interface	
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DC030006J00



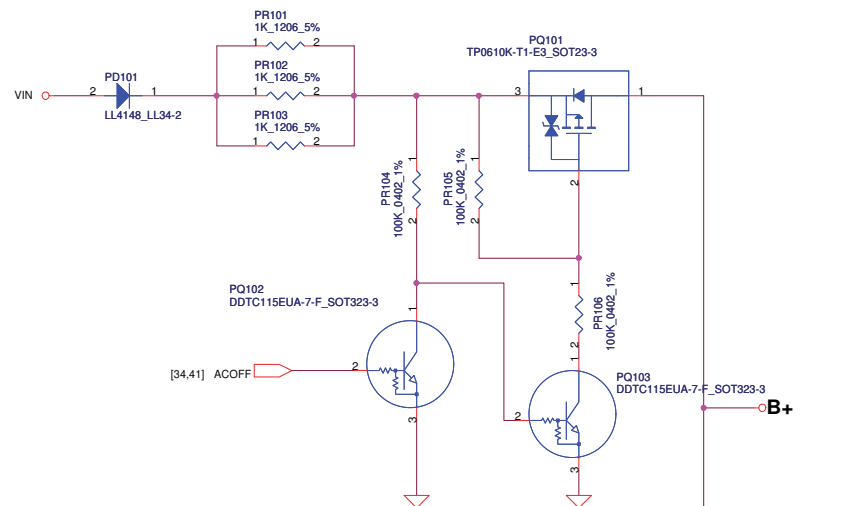
Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



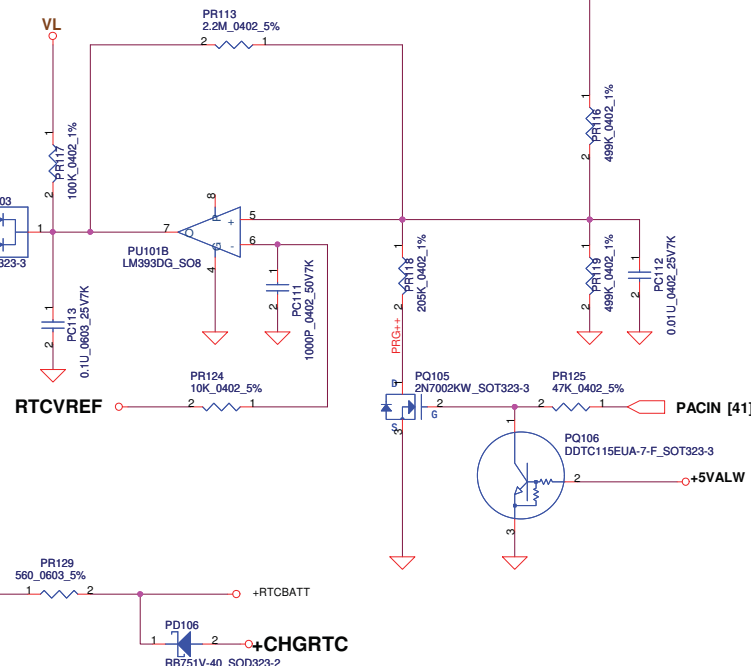
ACIN

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V



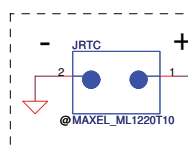
BATT ONLY

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



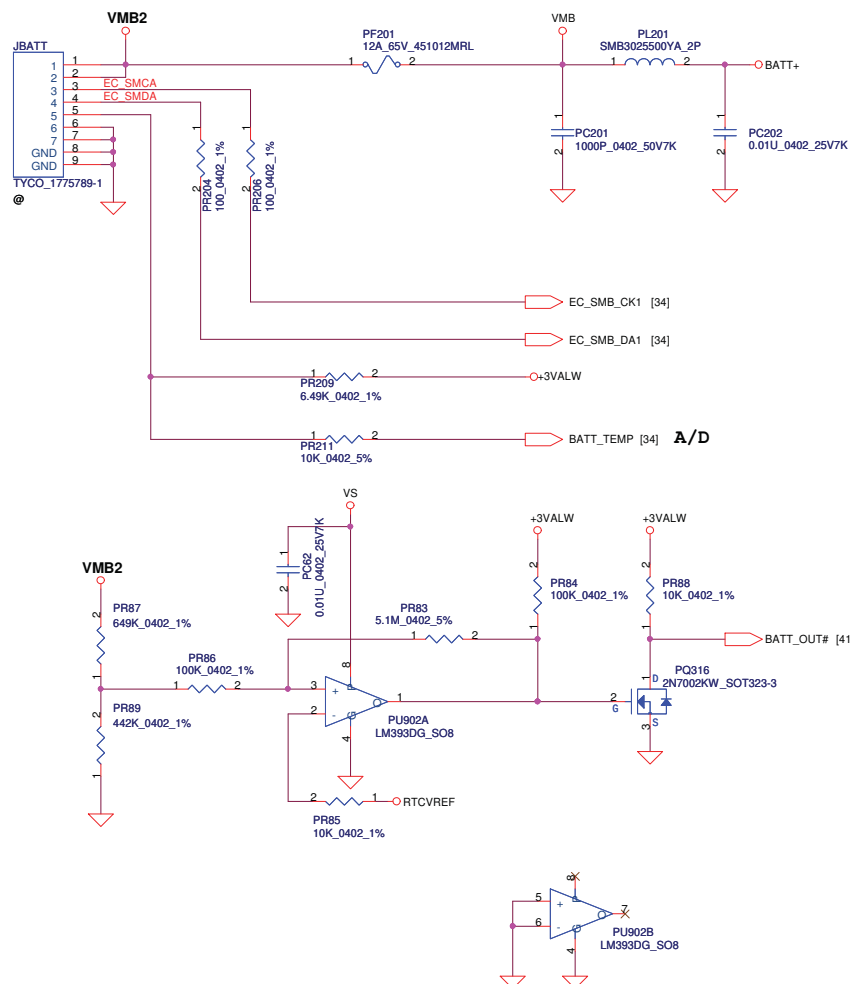
[6,40,42] MAINPWON

[41] ACIN

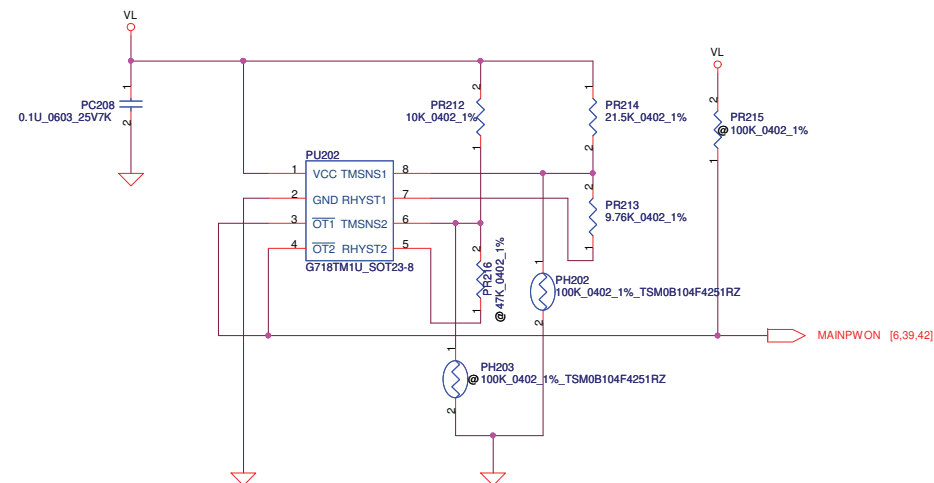


RTC Battery

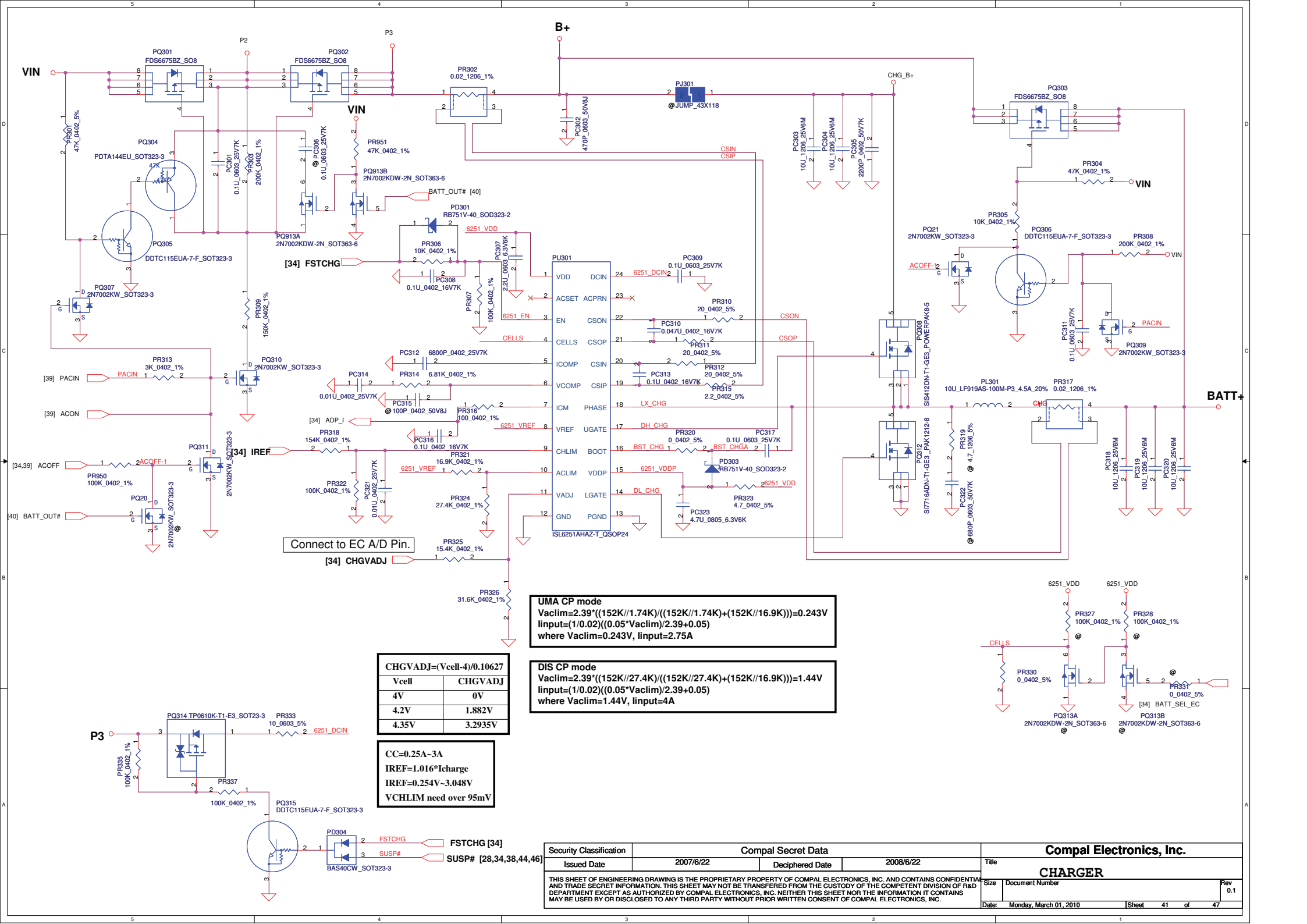
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Deciphered Date				2010/01/06				DCIN & DETECTOR			
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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Connect to EC A/D Pin.

[34] CHGVADJ

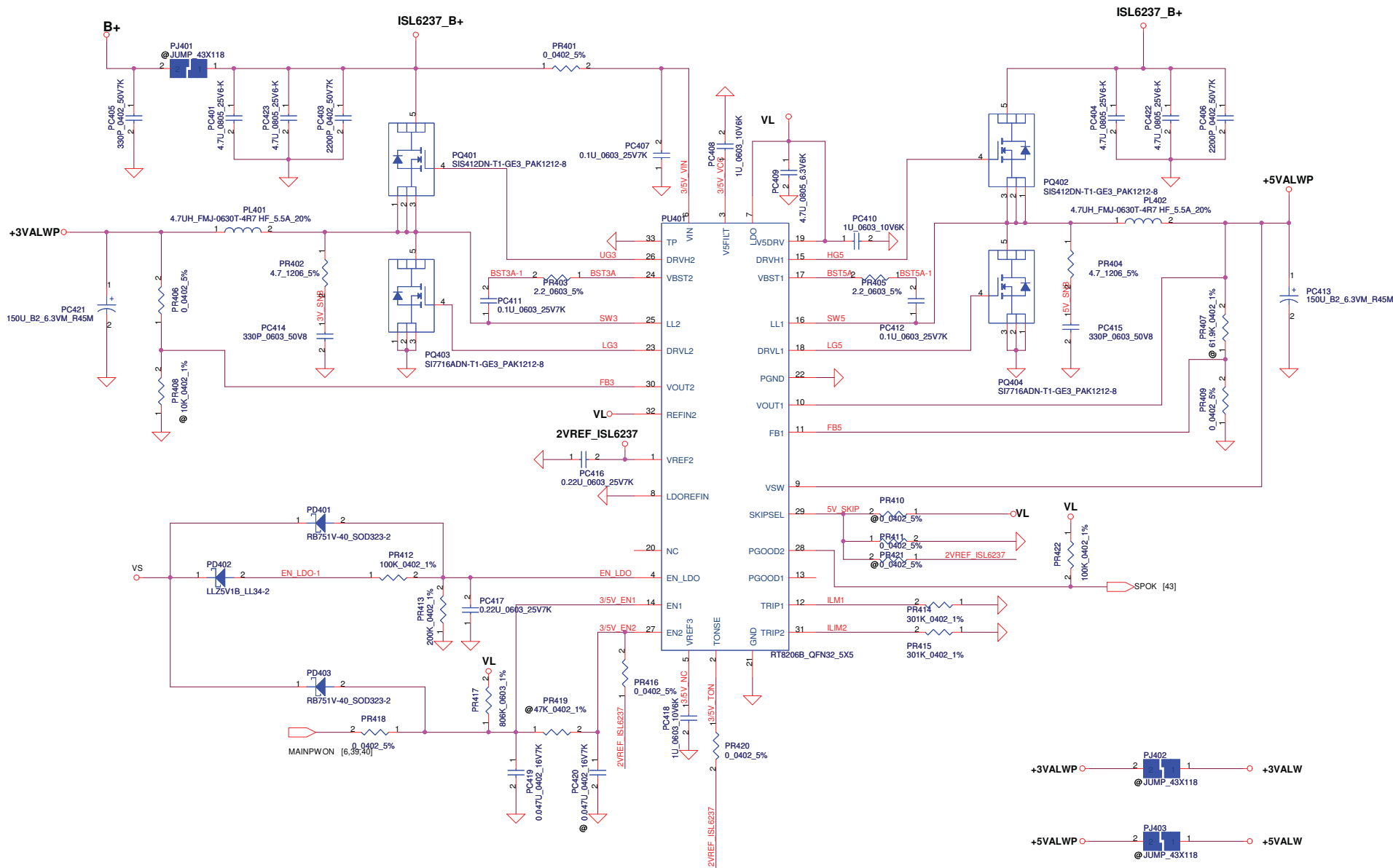
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

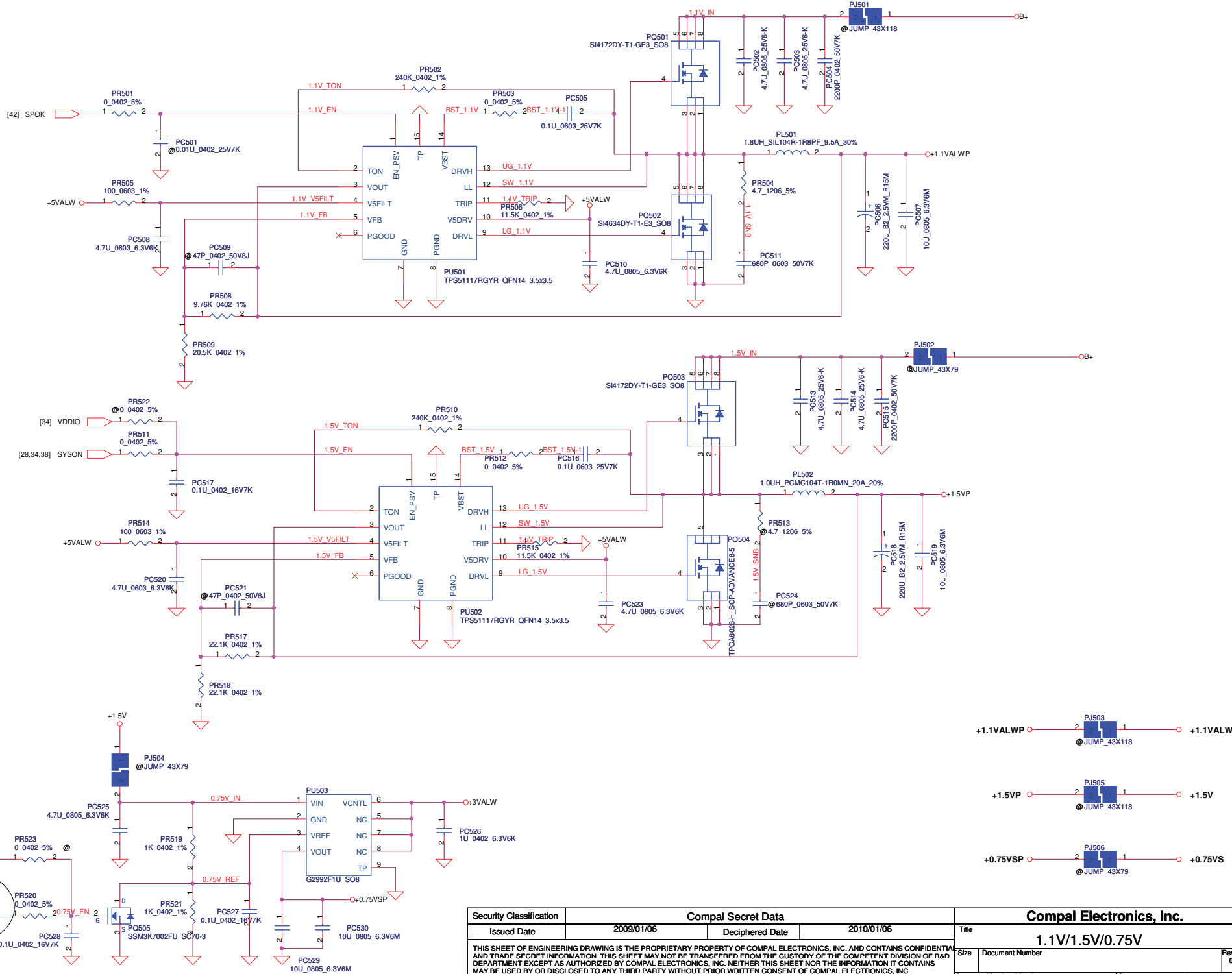
UMA CP mode
 $V_{acli} = 2.39 * ((152K / 1.74K) / ((152K / 1.74K) + (152K / 16.9K))) = 0.243V$
 $I_{in} = (1 / 0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
where $V_{acli} = 0.243V$, $I_{in} = 2.75A$

DIS CP mode
 $V_{acli} = 2.39 * ((152K / 27.4K) / ((152K / 27.4K) + (152K / 16.9K))) = 1.44V$
 $I_{in} = (1 / 0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
where $V_{acli} = 1.44V$, $I_{in} = 4A$

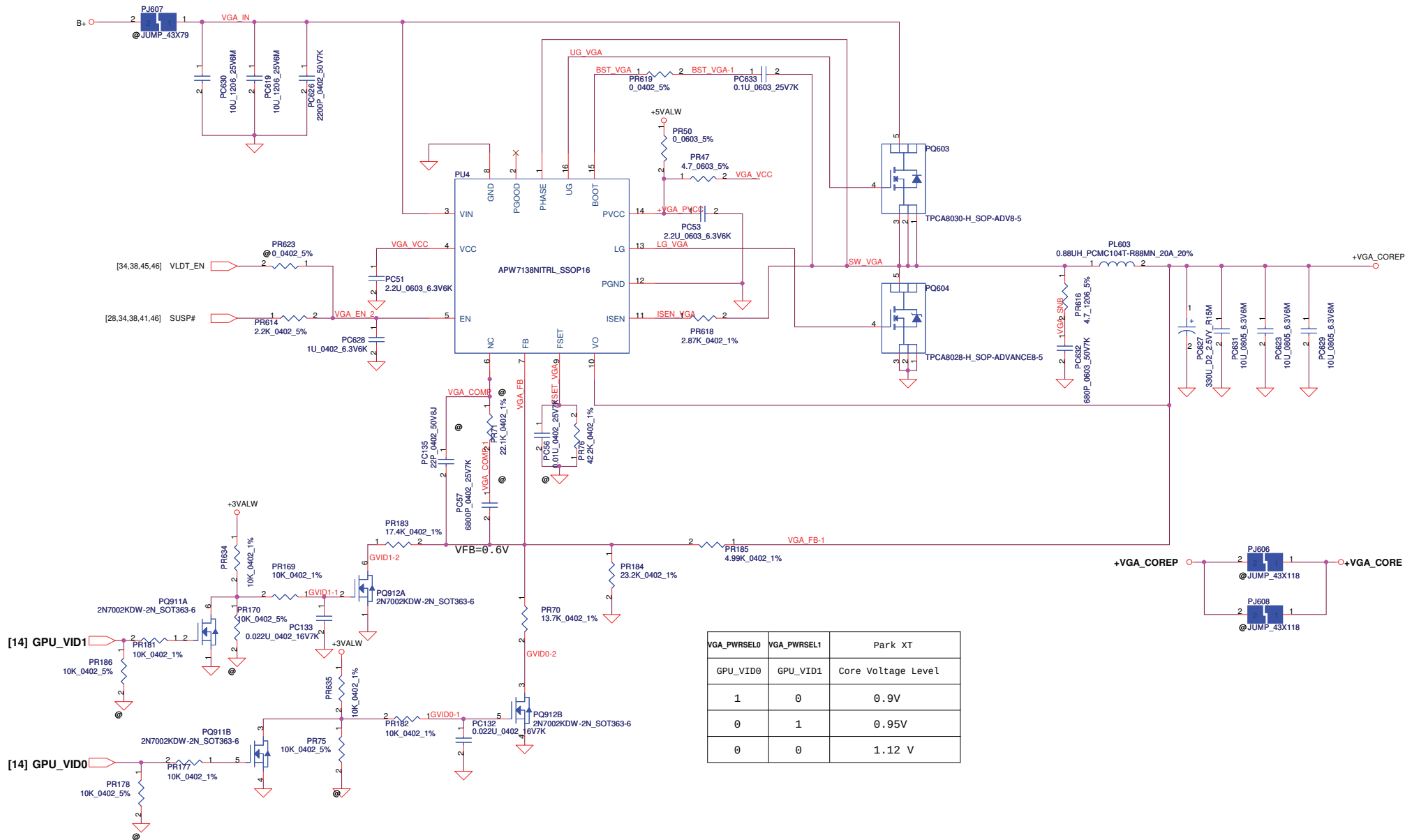
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								Size	
								0.1	
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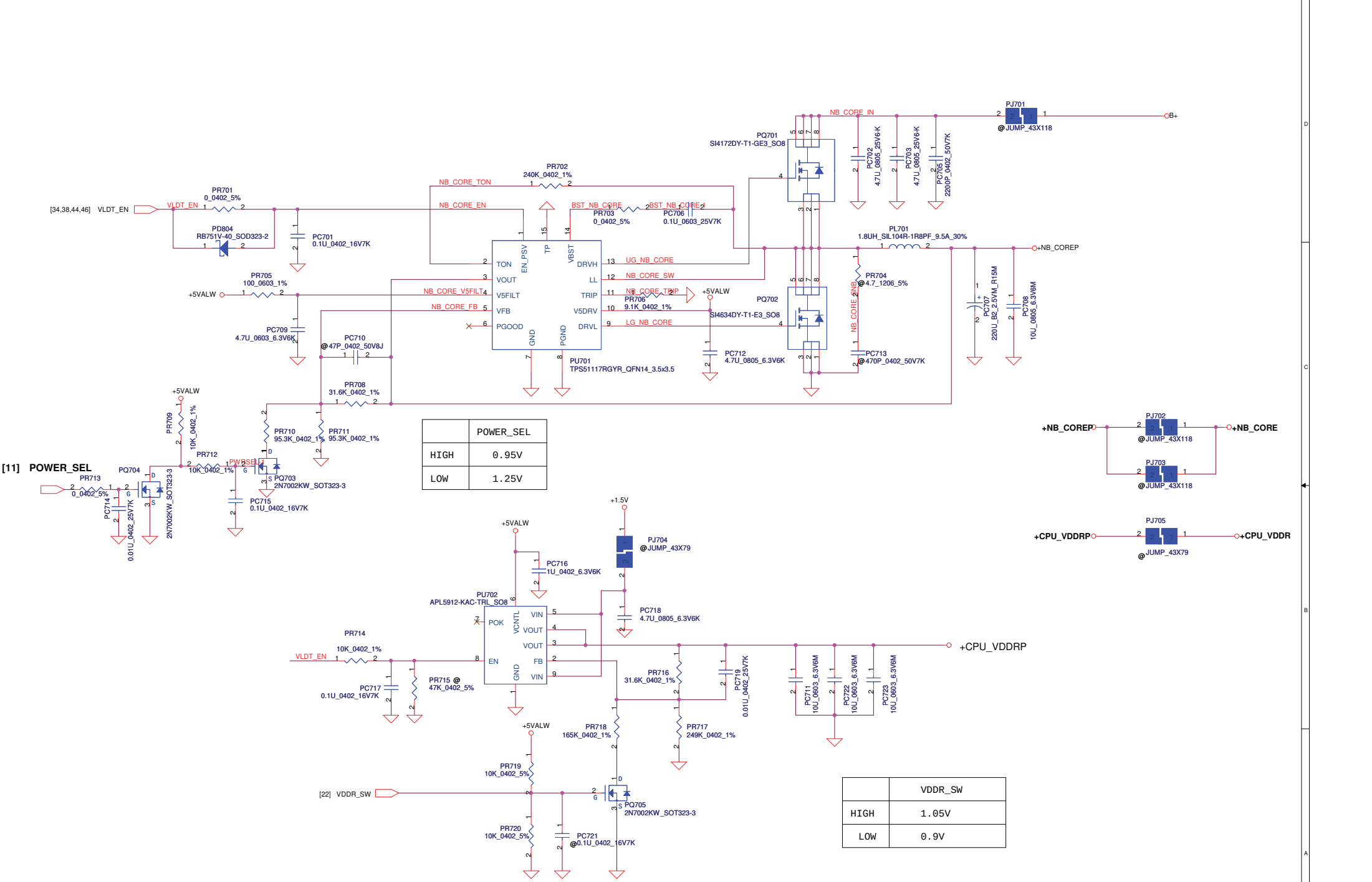


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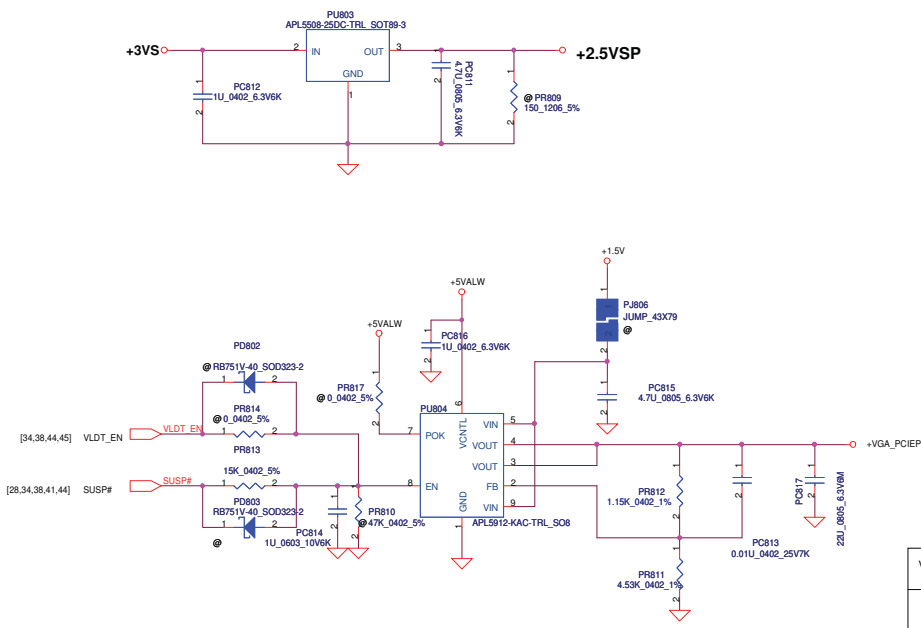
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								1.1V/1.5V/0.75V	
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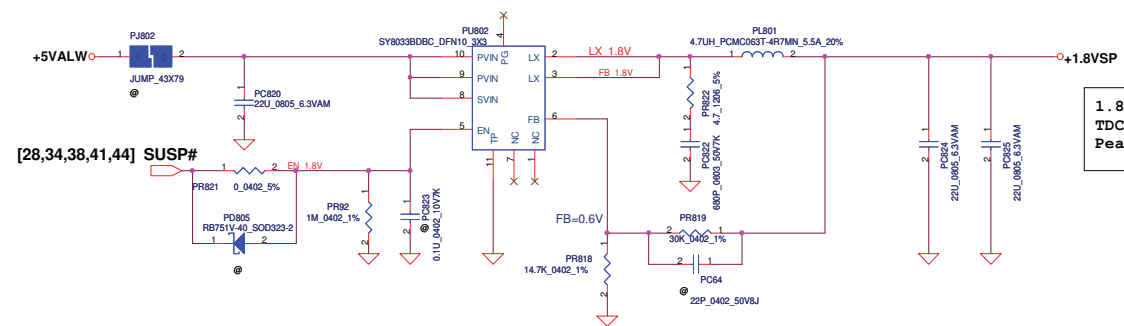
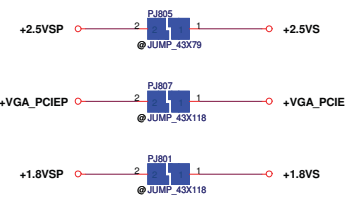


	POWER_SEL
HIGH	0.95V
LOW	1.25V

	VDDR_SW
HIGH	1.05V
LOW	0.9V



VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K



1.8VSP
TDC 2 A
Peak Current 3 A

