

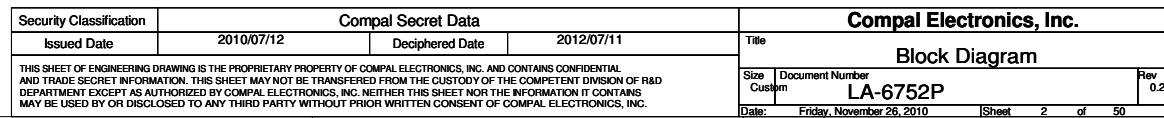
Compal Confidential

G470/G570 UMA M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

2010-10-22
LA-6752P / LA-6754P
REV: 0.2

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power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus2 address

Device	Device	Address
Smart Battery	0001 011X b	
	Thermal Sensor EMC1403-2	1001_101xb

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

[illegible]

Power-Up/Down Sequence

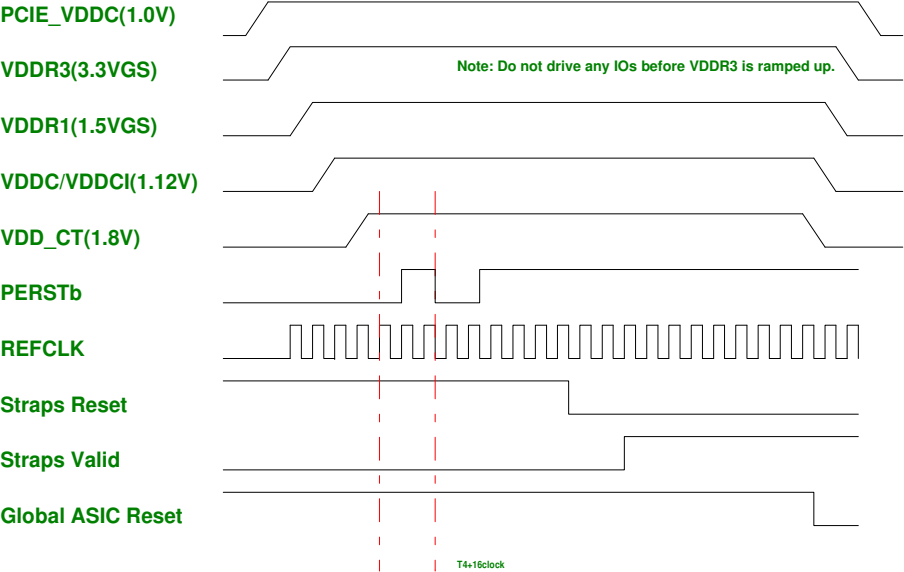
All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

VDDR3 should ramp-up before or simultaneously with VDDC.

For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation

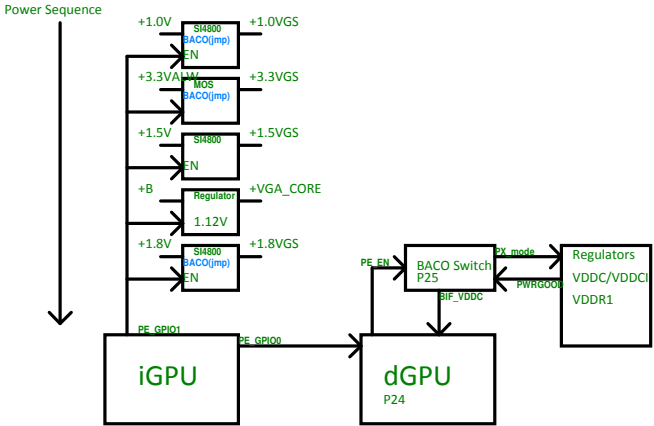
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)

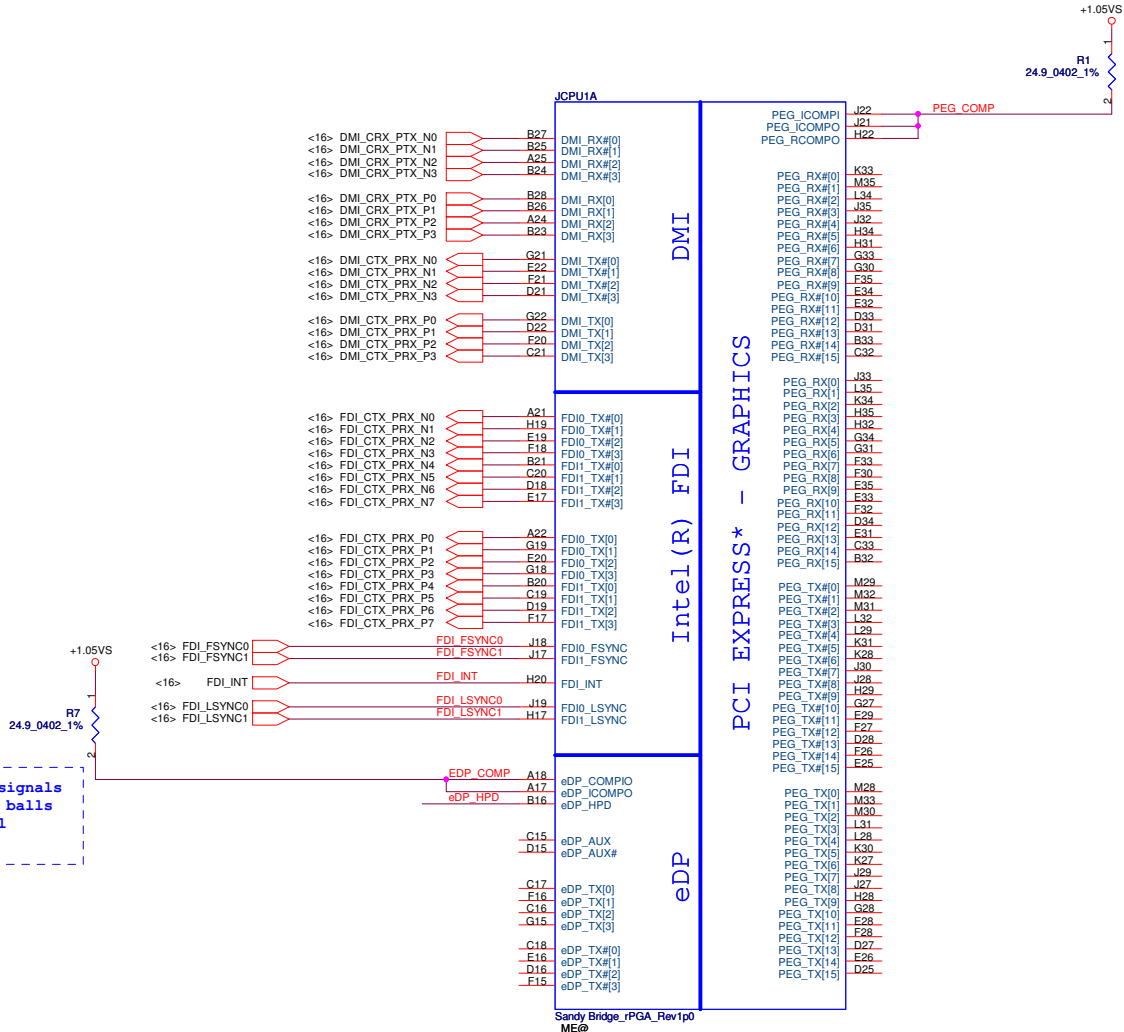
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

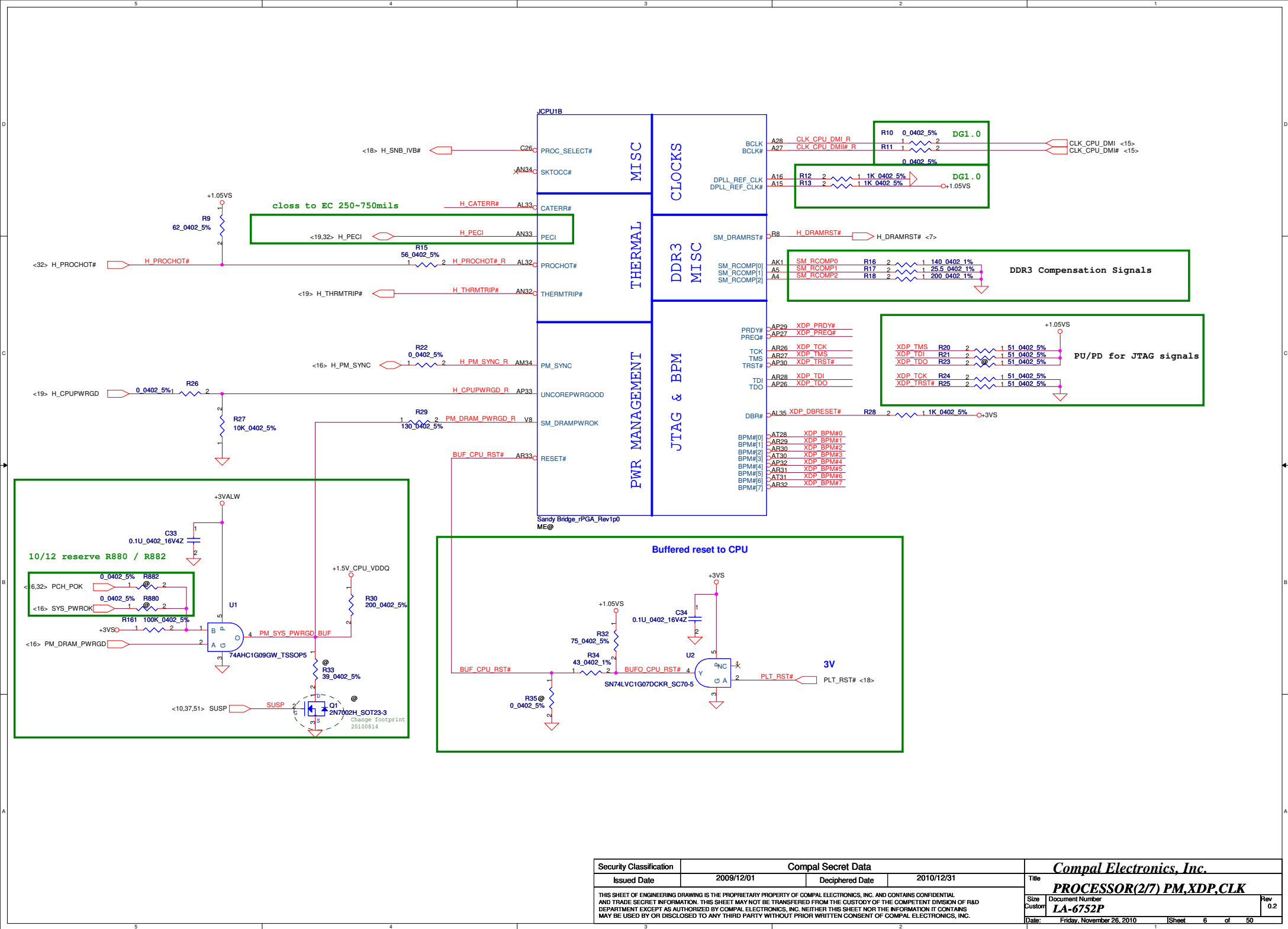
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIe_PVDD, PCIe_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIe_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIe_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

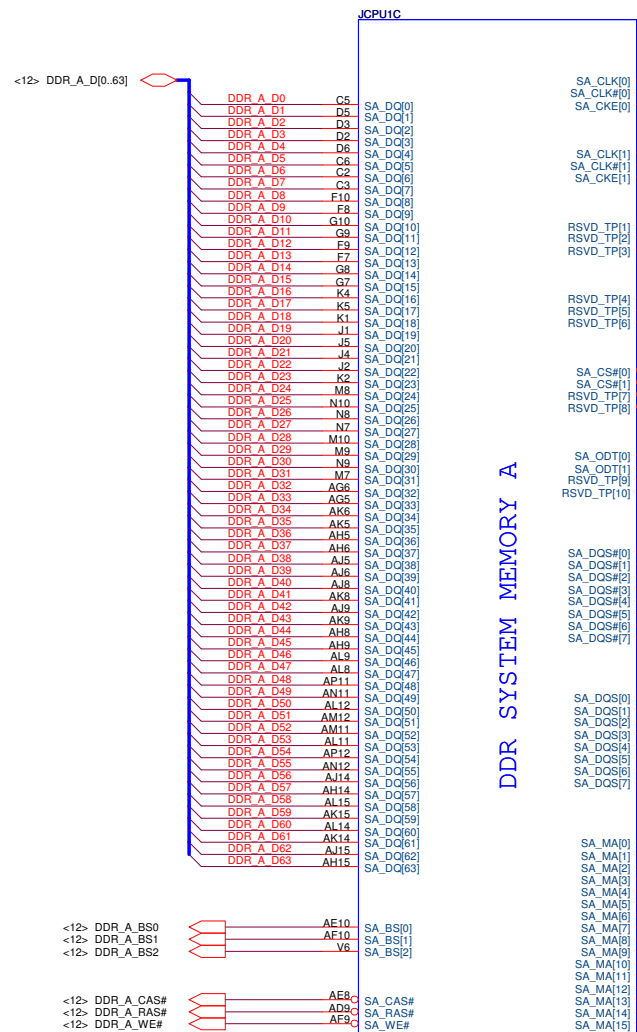


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

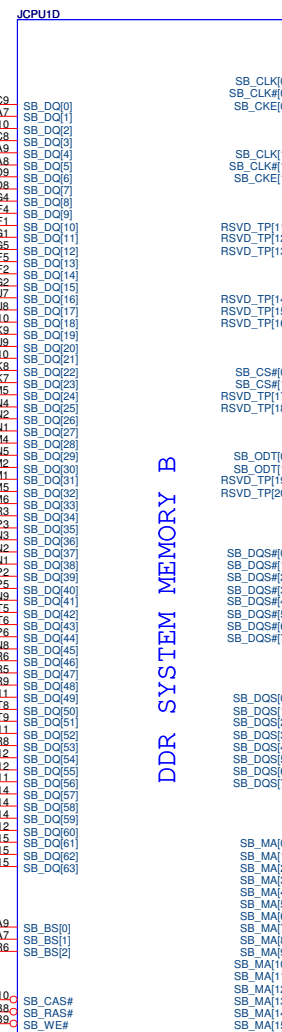
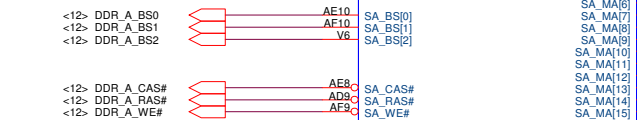
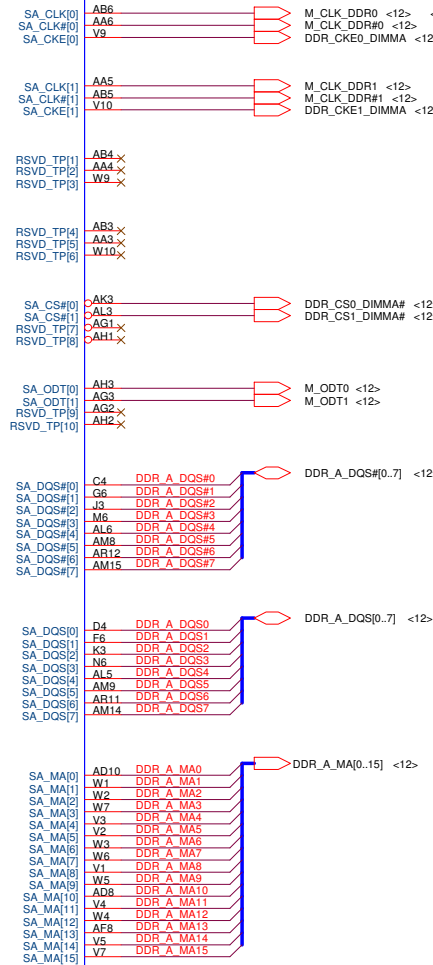
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



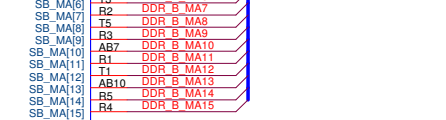
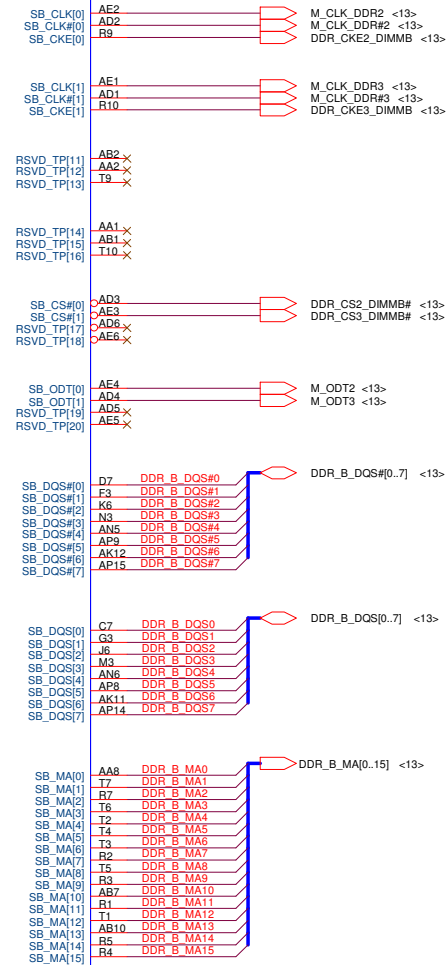




DDR SYSTEM MEMORY A

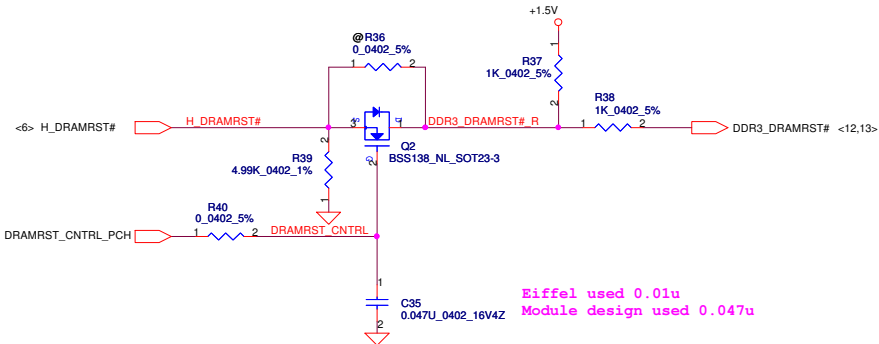


DDR SYSTEM MEMORY B



Sandy Bridge_rPGA_Rev1p0
ME@

Sandy Bridge_rPGA_Rev1p0
ME@



Eiffel used 0.01u
Module design used 0.047u

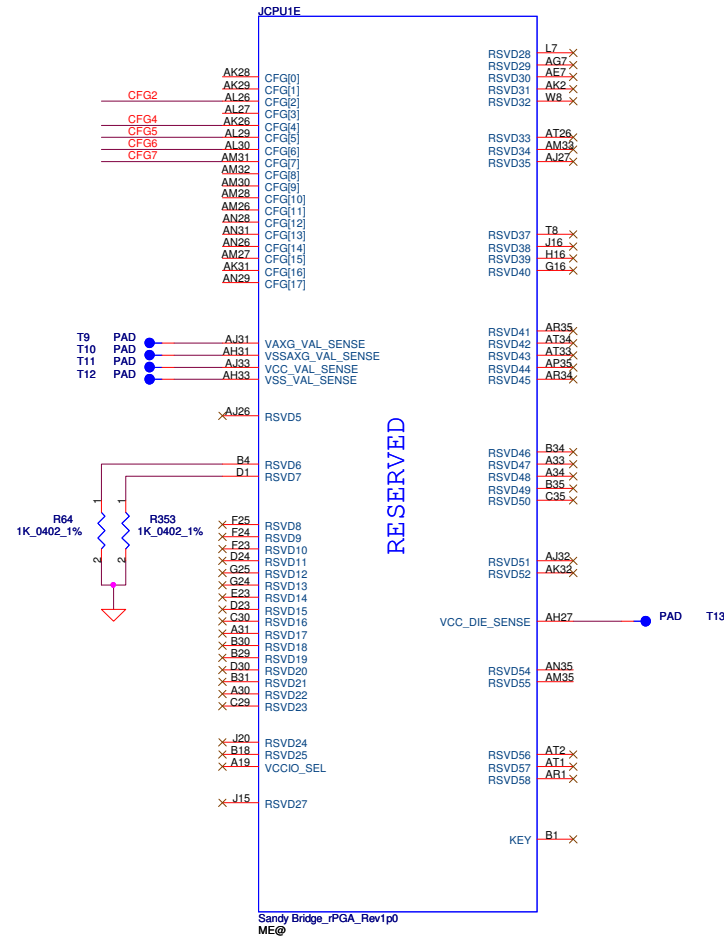
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						Size		Document Number		Rev	
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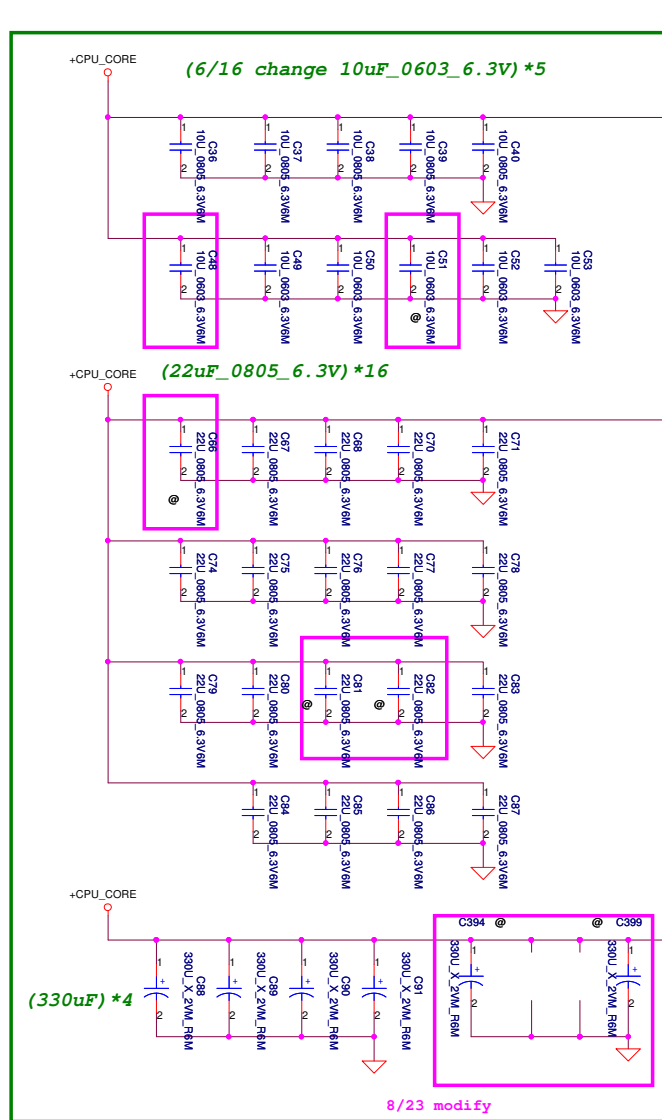
A schematic diagram showing a 1k resistor labeled R41 with a value of 1K_0402_1%. The resistor is connected between a pin labeled CFG2 and a ground symbol.

A circuit diagram showing a 1k resistor labeled R42. The resistor is connected to a signal source labeled CFG4 at its top terminal (pin 1) and to a ground symbol at its bottom terminal (pin 2).

A schematic diagram showing a 1k resistor connected to the CFG7 pin. The resistor is labeled "@ R45 1K_0402_1%". The CFG7 pin is shown as a horizontal line on the left, and the resistor is connected to it and to a ground symbol on the right.

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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	PROCESSOR(47) RSVD.CFG				
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QC=94A
DC=53A

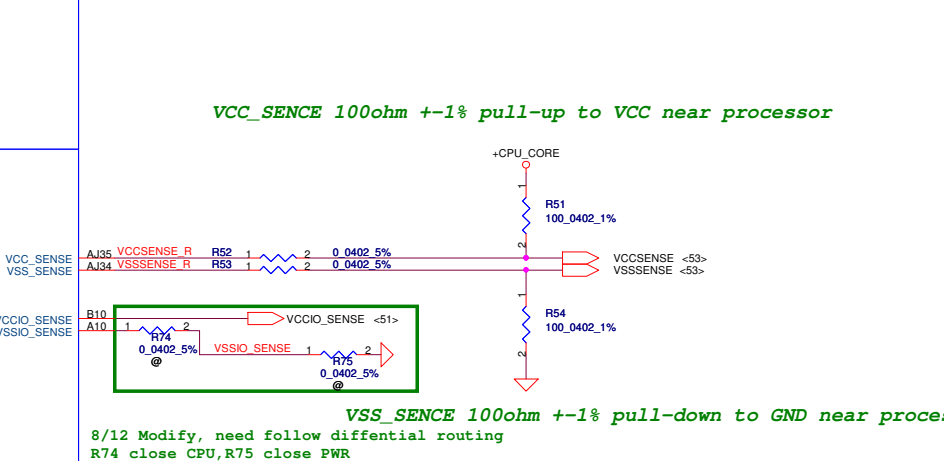
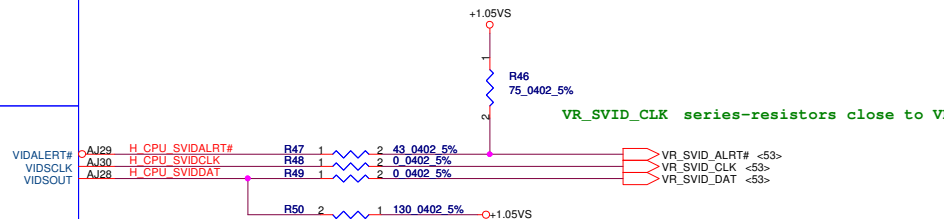
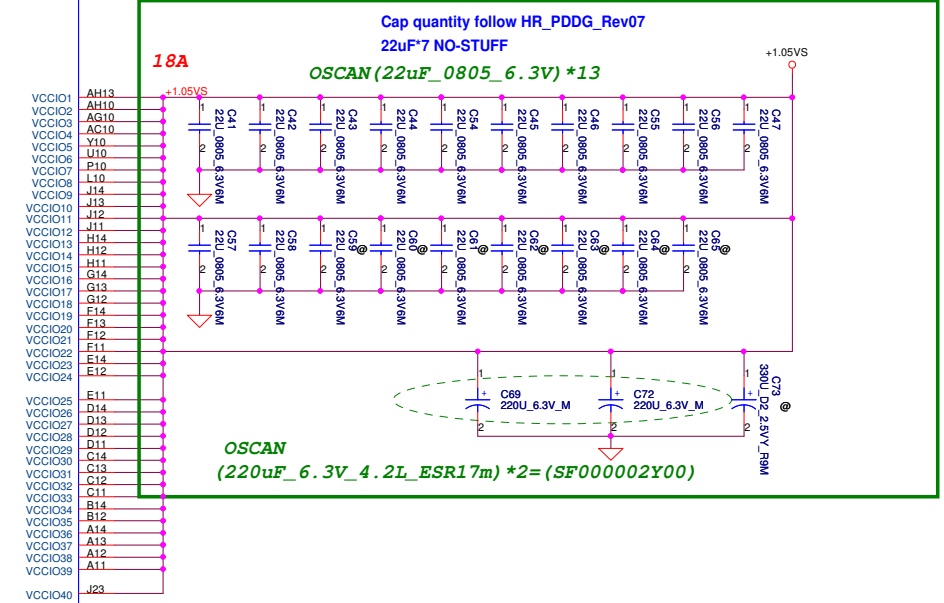
Pin	Signal
AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
Y35	VCC50
Y34	VCC51
Y33	VCC52
Y32	VCC53
Y31	VCC54
Y30	VCC55
Y29	VCC56
Y28	VCC57
Y27	VCC58
Y26	VCC59
Y25	VCC60
Y24	VCC61
Y23	VCC62
Y22	VCC63
Y21	VCC64
Y20	VCC65
Y19	VCC66
Y18	VCC67
Y17	VCC68
Y16	VCC69
Y15	VCC70
Y14	VCC71
Y13	VCC72
Y12	VCC73
Y11	VCC74
Y10	VCC75
Y09	VCC76
Y08	VCC77
Y07	VCC78
Y06	VCC79
Y05	VCC80
Y04	VCC81
Y03	VCC82
Y02	VCC83
Y01	VCC84
Y00	VCC85
Y99	VCC86
Y98	VCC87
Y97	VCC88
Y96	VCC89
Y95	VCC90
Y94	VCC91
Y93	VCC92
Y92	VCC93
Y91	VCC94
Y90	VCC95
Y89	VCC96
Y88	VCC97
Y87	VCC98
Y86	VCC99
Y85	VCC100

POWER

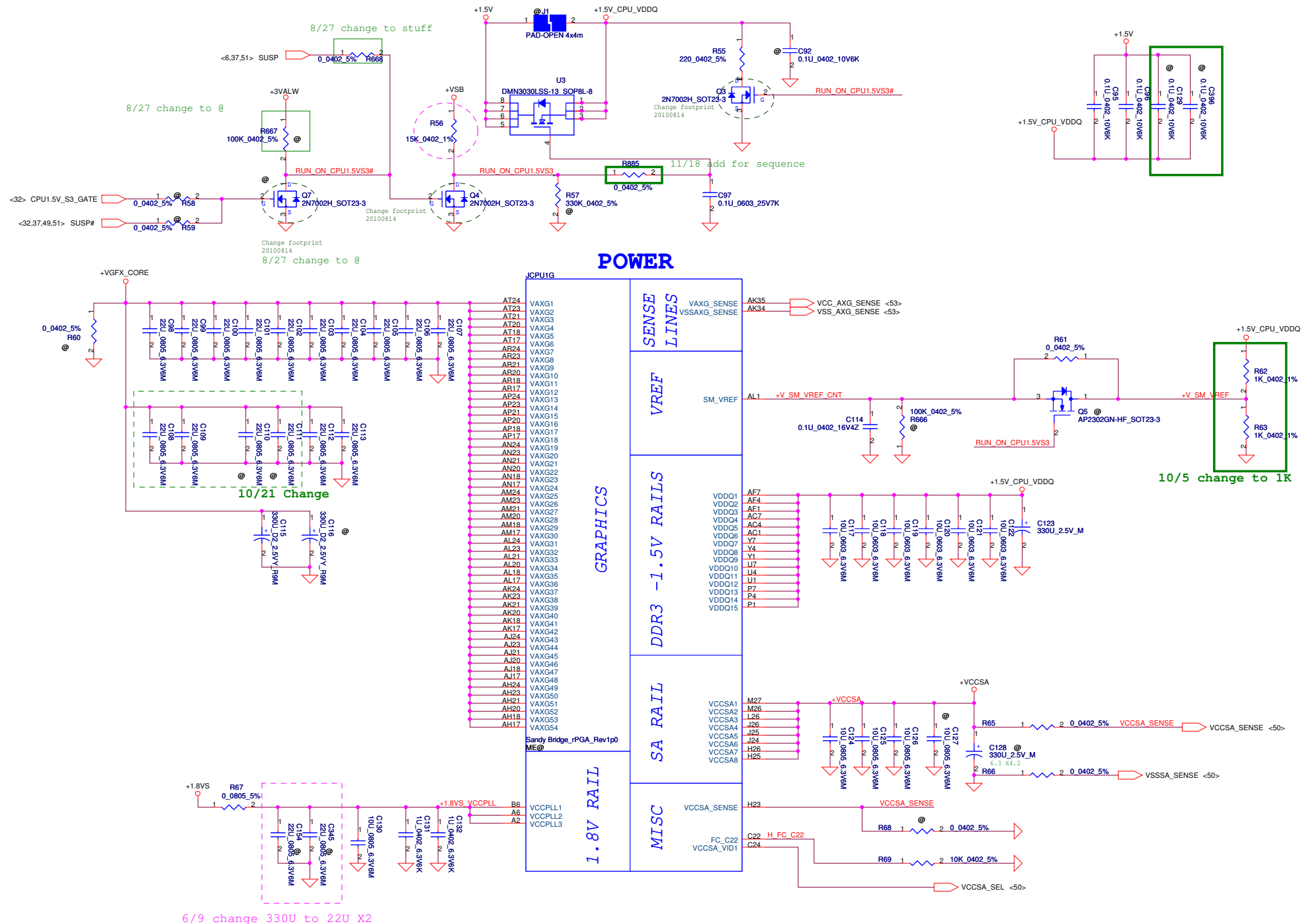
CORE SUPPLY

SVID

SENSE LINES



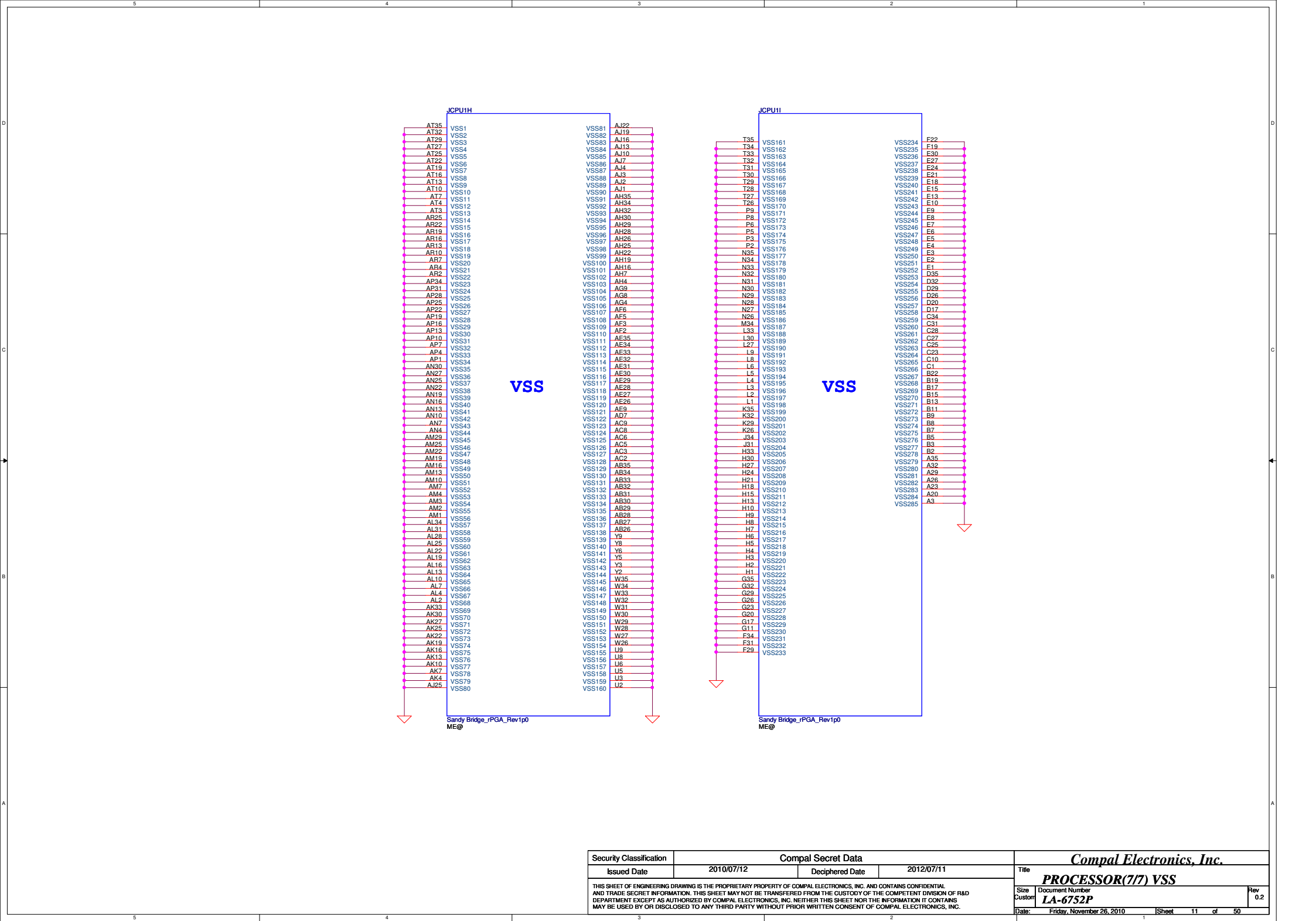
Sandy Bridge_rPGA Rev10A ME@		Security Classification		Compal Secret Data		Title	
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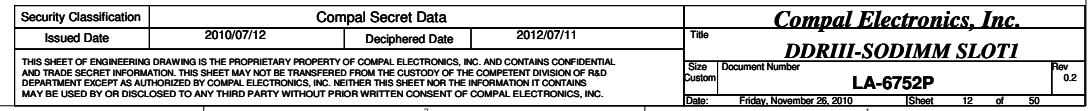


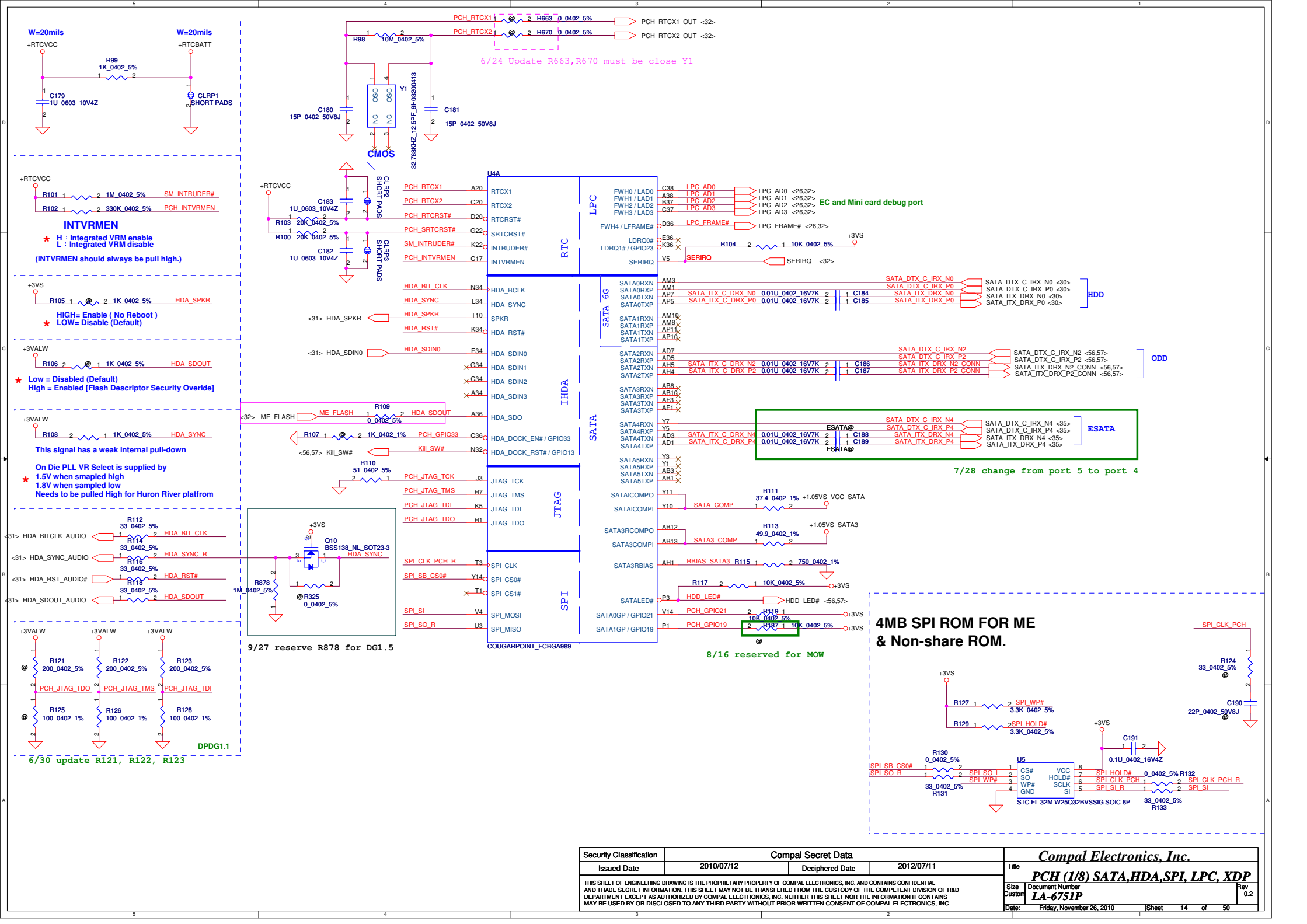
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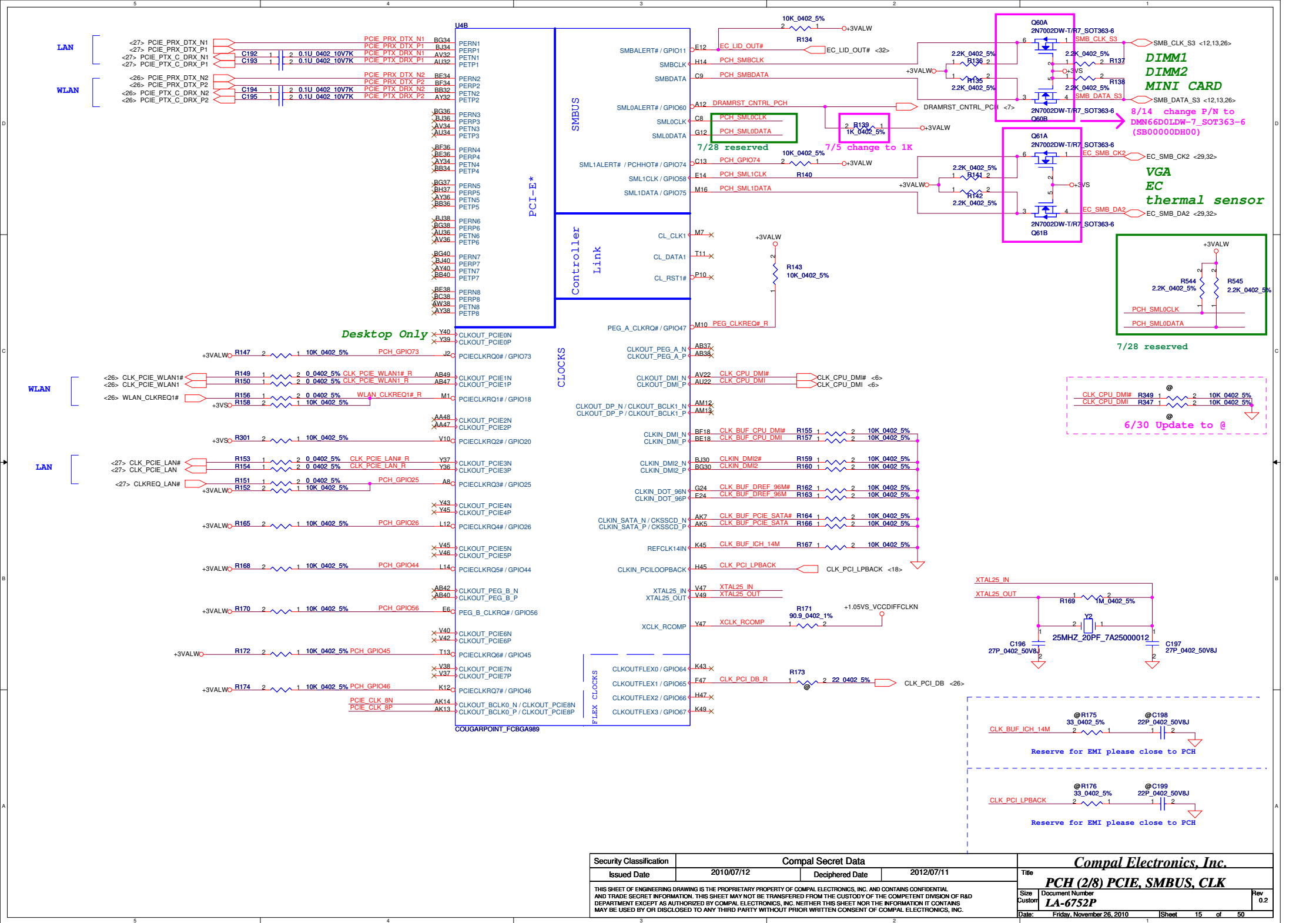
PROCESSOR(6/7) PWR

LA-6752P

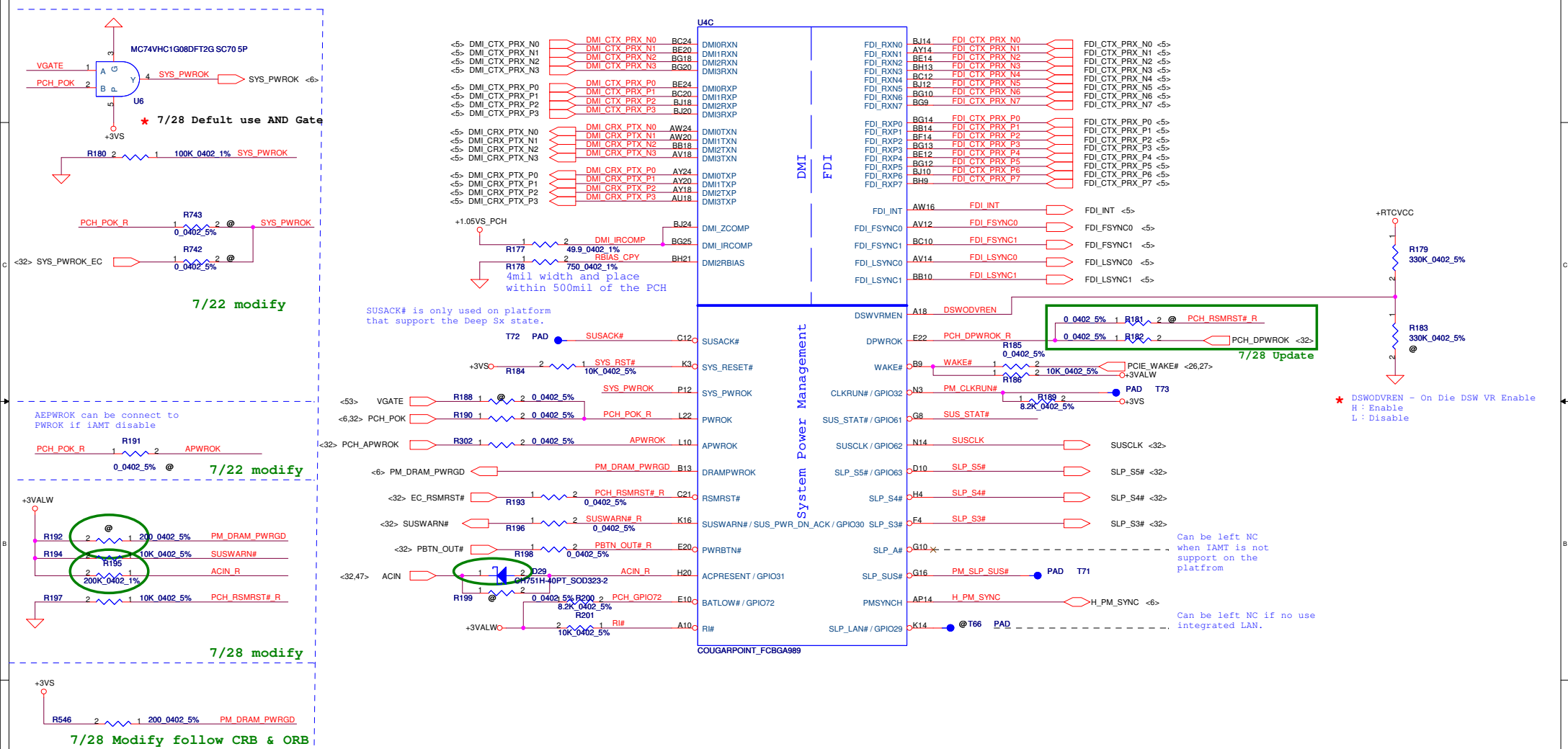


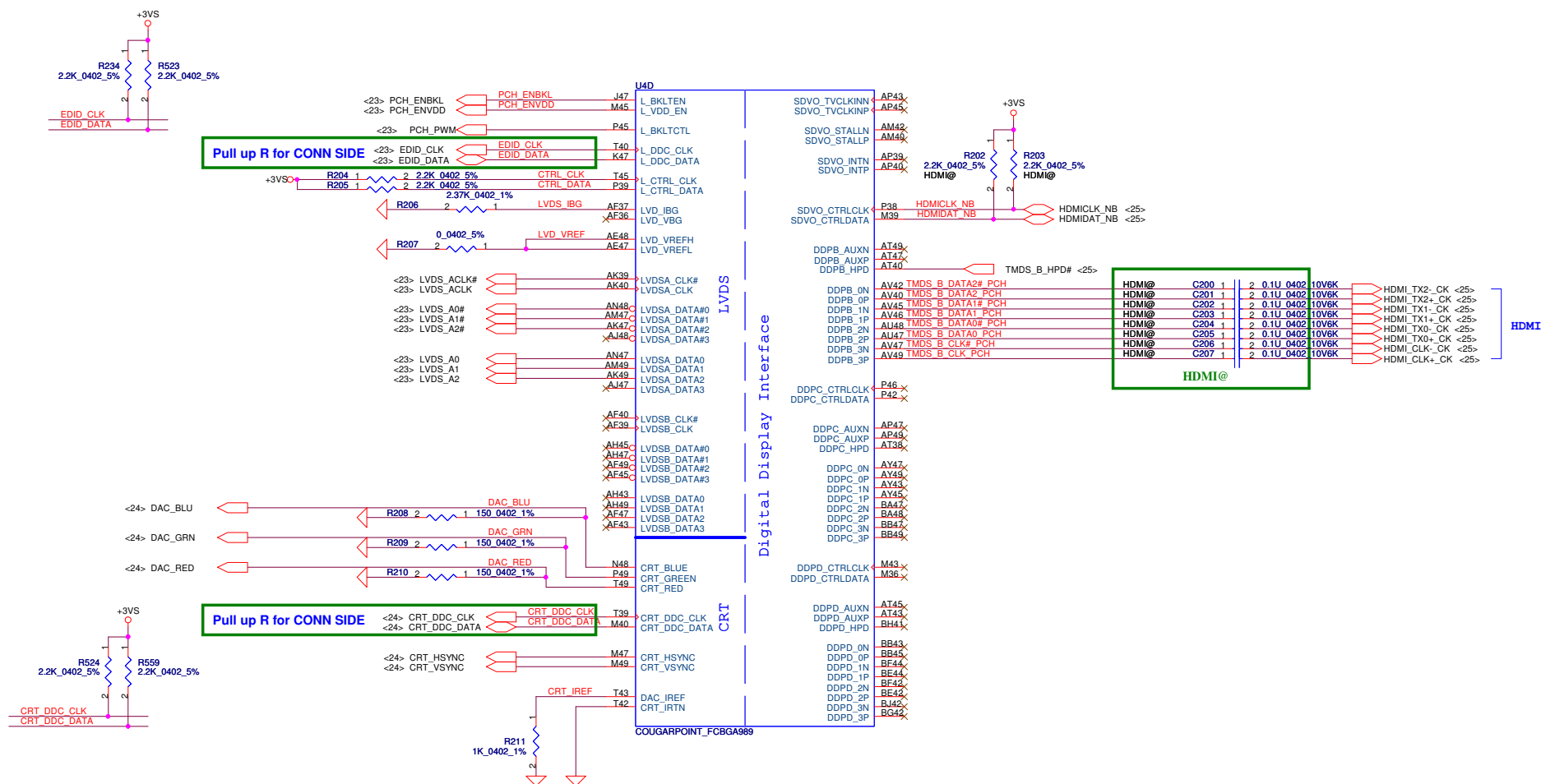






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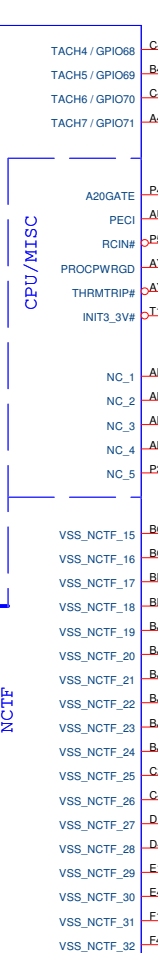
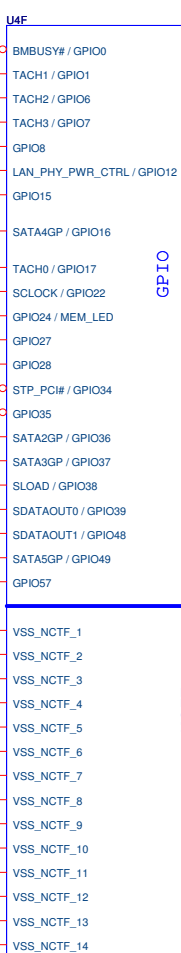
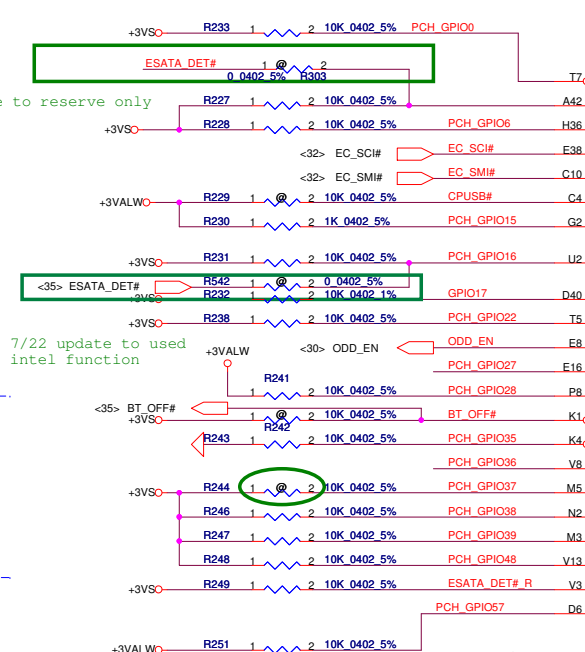
ICC_EN#
Integrated Clock Chip Enable
H ; Disable
★ L ; Enable
7/22 update to reserve only
R235 1 2 1K 0402 5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1 2 1K 0402 5% PCH_GPIO28

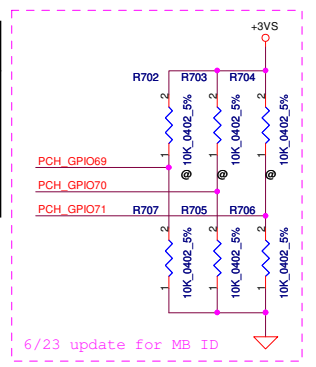
PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 1 2 1K 0402 5% PCH_GPIO27

R250 1 2 1K 0402 5% PCH_GPIO36
R547 1 2 10K 0402 5%
8/5 update to pull down

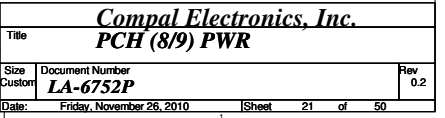
R881 1 2 10K 0402 5% PCH_GPIO37
10/8 update to pull down for checklist Rev1.2

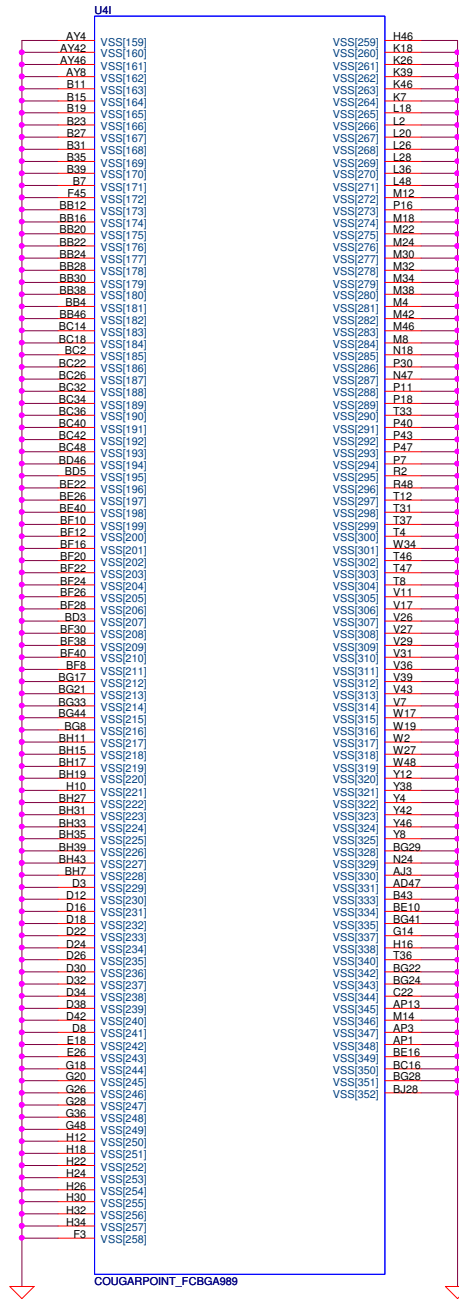
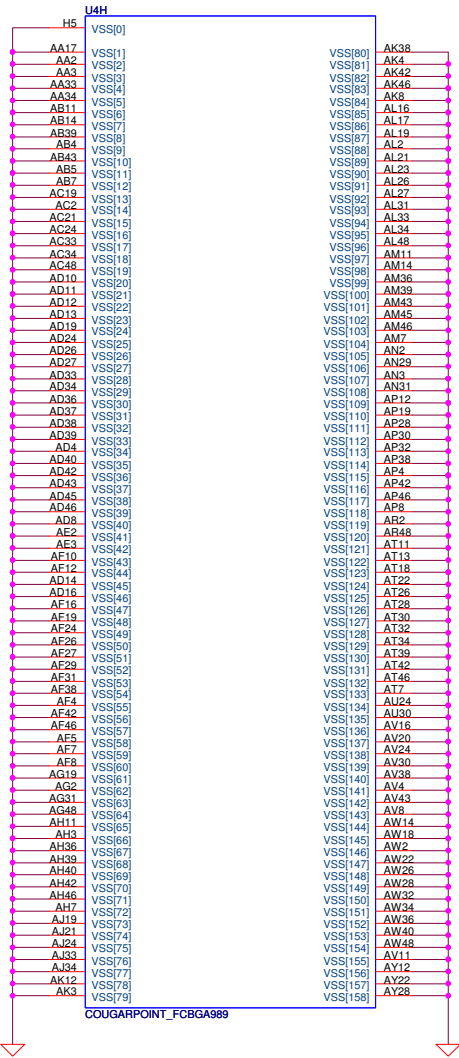


PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA ★
1	0	0	DIS
0	1	0	PX3.0
1	1	0	PX4.0



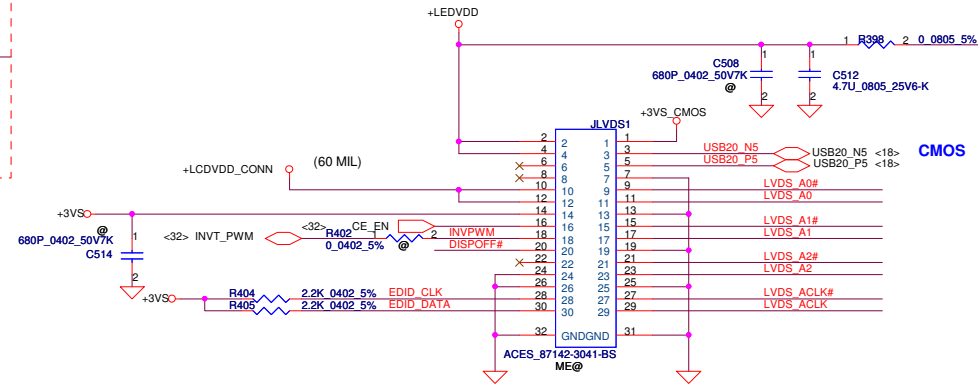
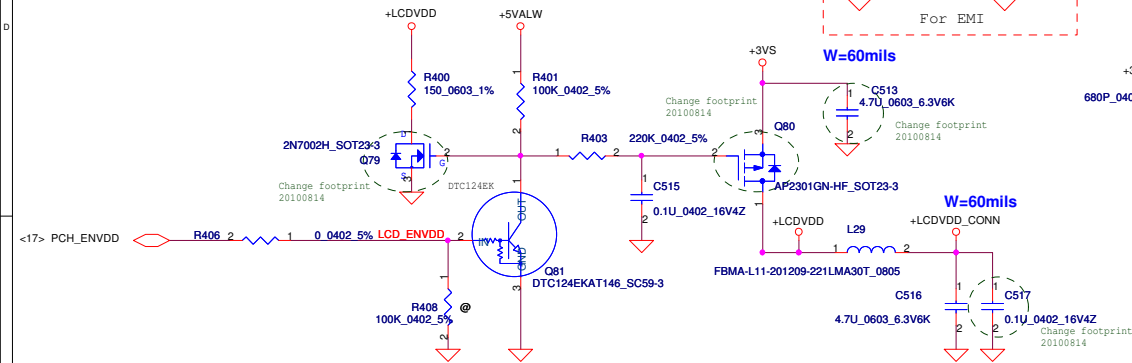
INIT3_3V
This signal has weak internal PU, can't pull low
Intel schematic review recommend.



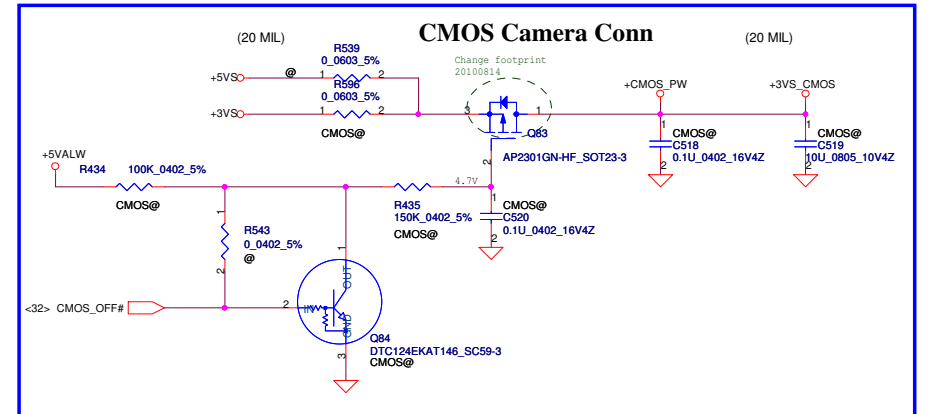
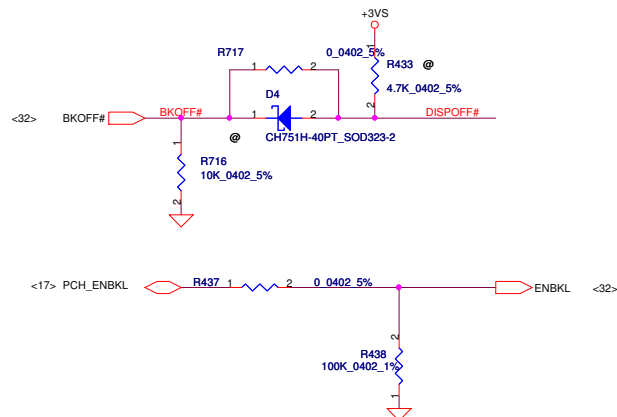
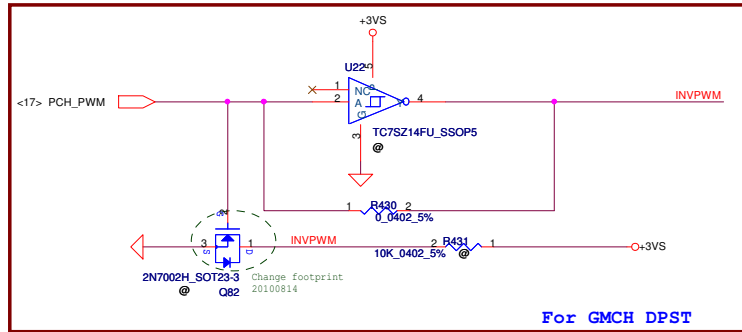


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								PCH (9/9) VSS			
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Custom		LA-6752P						0.2			
Date:		Friday, November 26, 2010		Sheet		22		of 50			

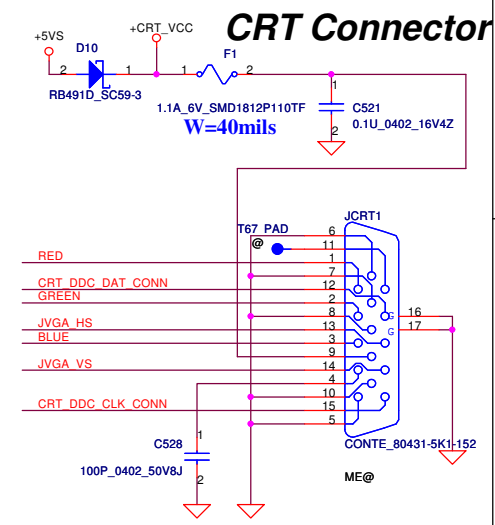
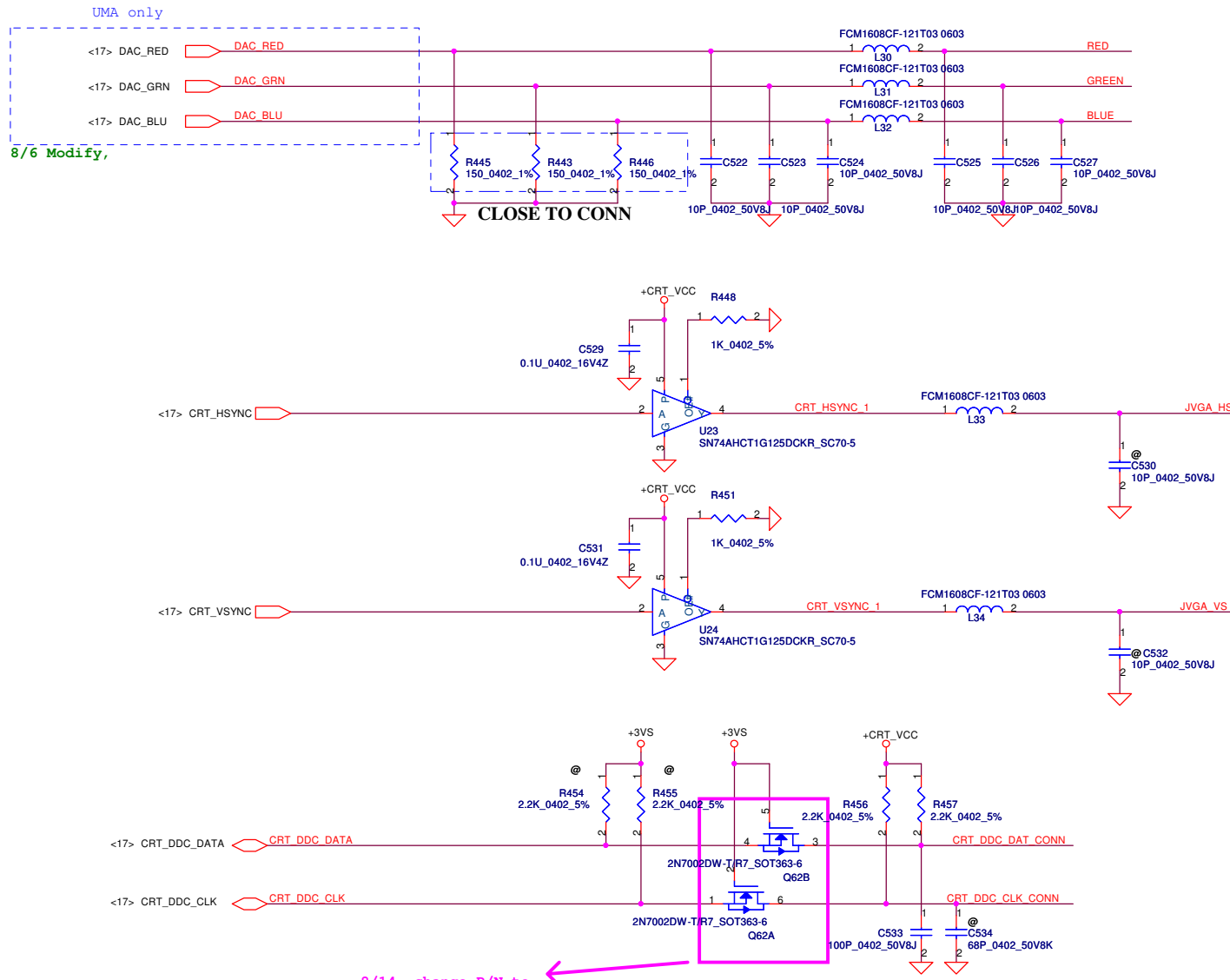
LCD POWER CIRCUIT



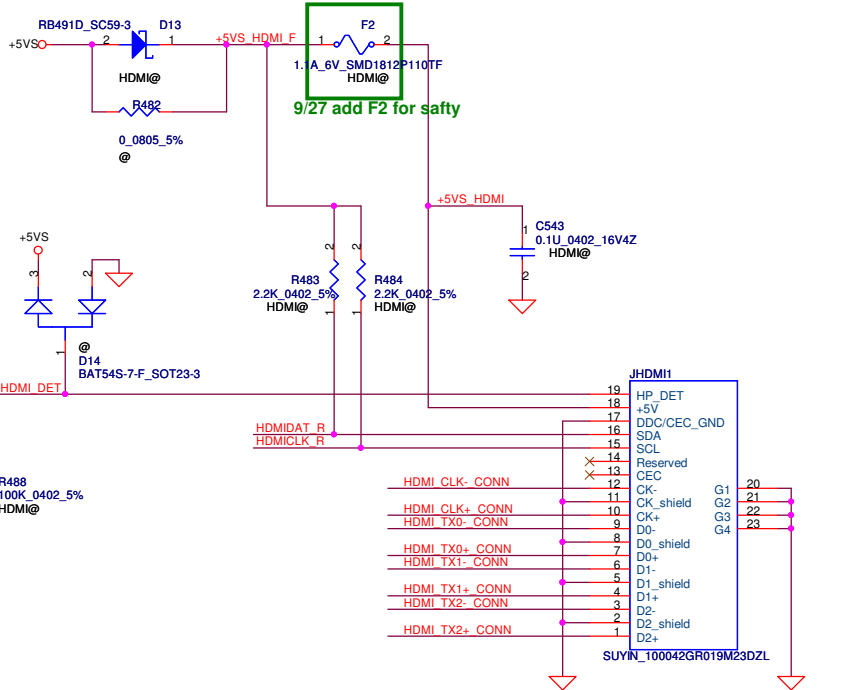
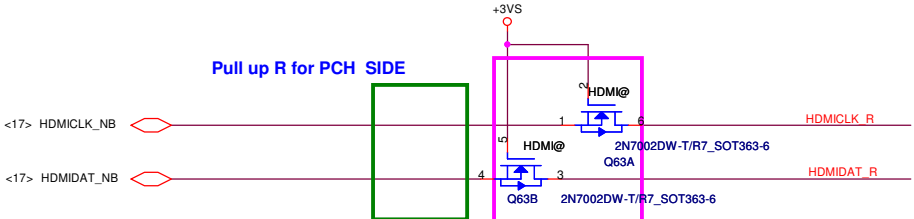
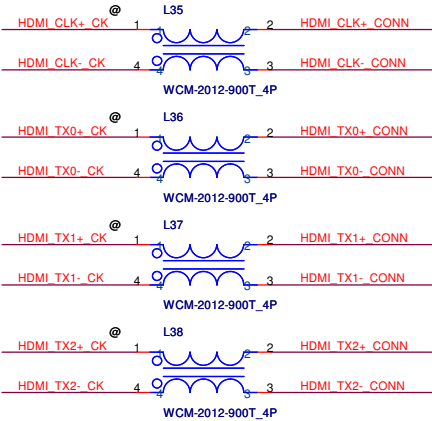
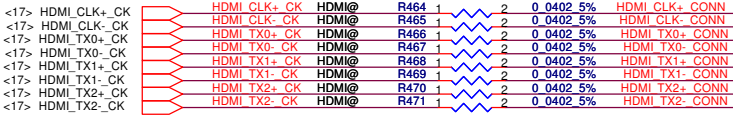
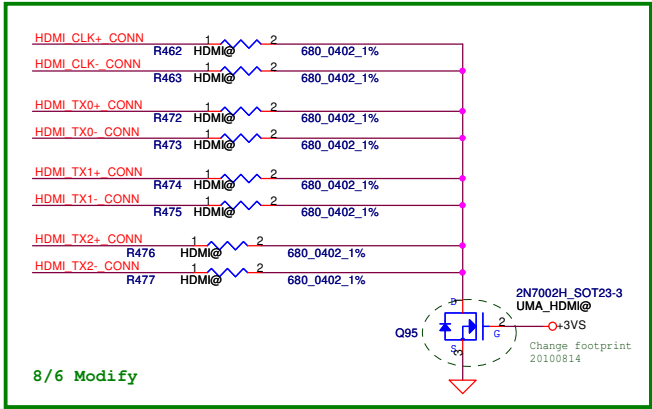
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Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/07/12				Title			
Deciphered Date				2012/07/11				LVDS/CAMERA			
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								LA-6752P			
								Rev 0.2			
								Date: Friday, November 26, 2010			
								Sheet 23 of 50			

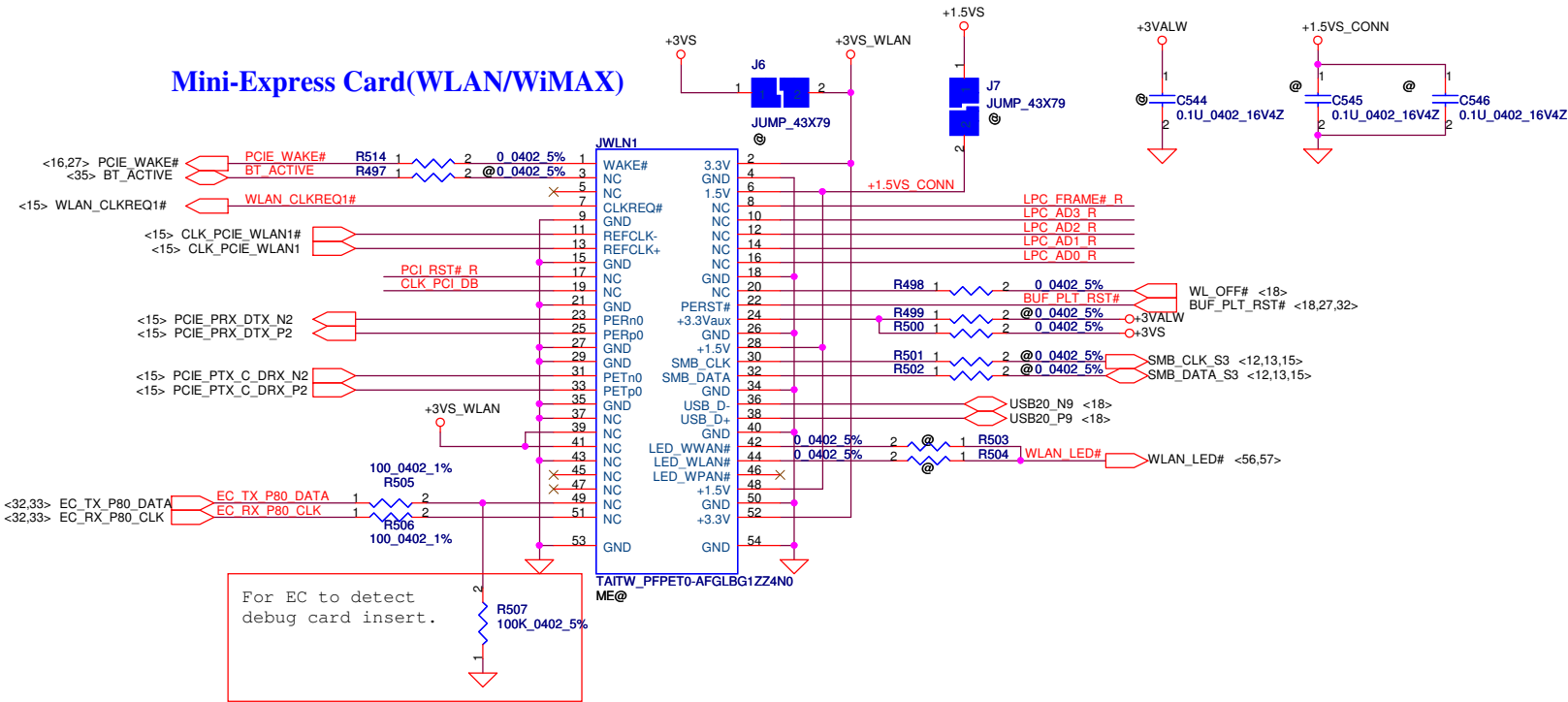


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2010/07/12		Deciphered Date		2012/07/11		Title			
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						Size		Document Number		Rev	
						Custom		LA-6752P		0.2	
						Date:		Friday, November 26, 2010		Sheet 24 of 50	



Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	HDMI CONN
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				Date: Friday, November 26, 2010	Rev 0.2
				Sheet 25	of 50

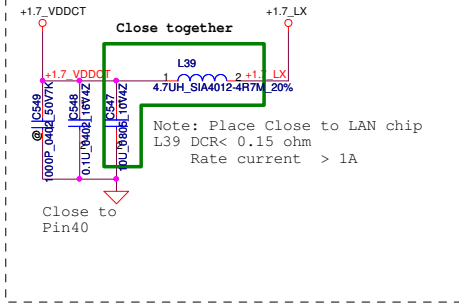
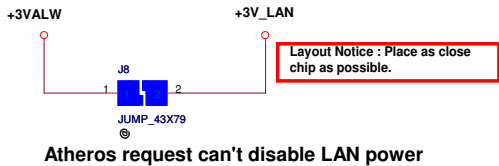
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R508	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,32>
LPC_AD3 R	R509	1	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,32>
LPC_AD2 R	R510	1	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,32>
LPC_AD1 R	R511	1	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,32>
LPC_AD0 R	R512	1	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,32>
PCI_RST# R	R513	1	2	0.0402 5%	PCI_RST#	PCI_RST# <14,32>
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB <15>

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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				Size	Document Number
				LA-6752P	
				Date:	Friday, November 26, 2010
				Sheet	26 of 50
				Rev	0.2

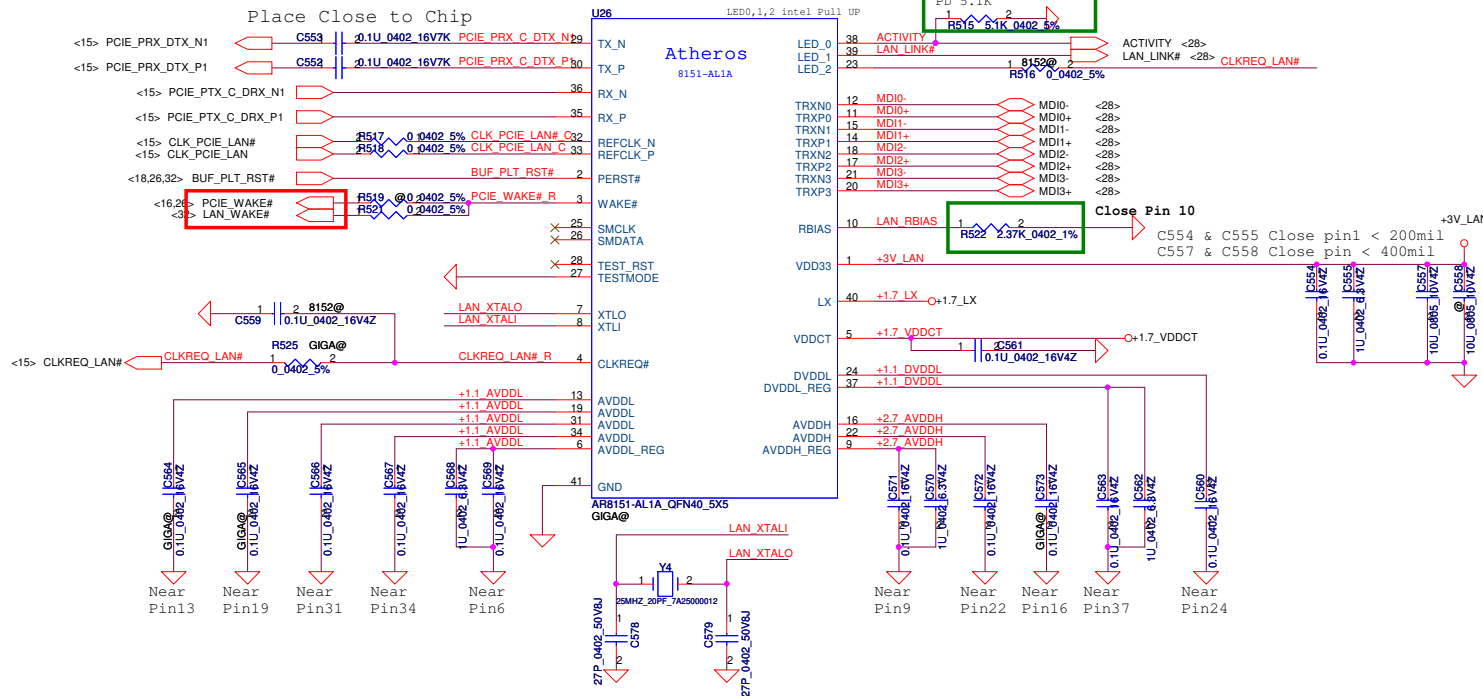


Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

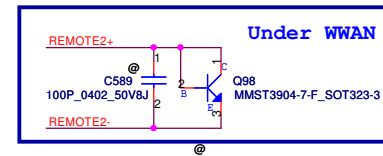
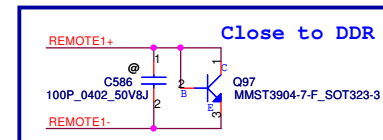
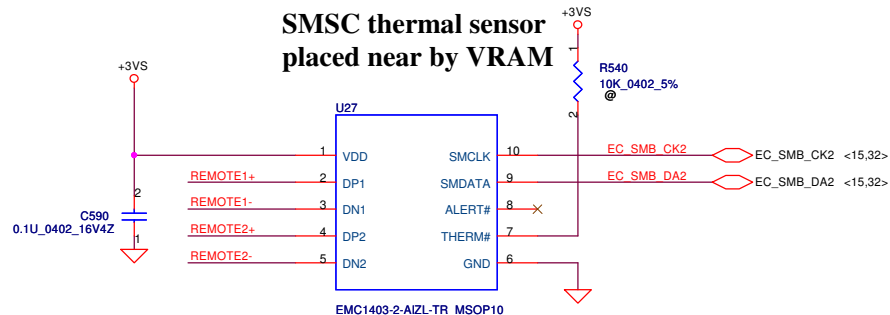
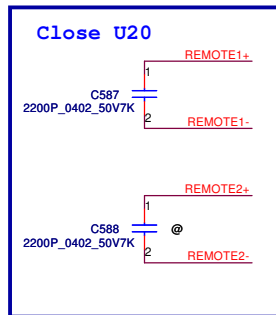


S IC AR8152-AL1E QFN 40P E-LAN CTRL

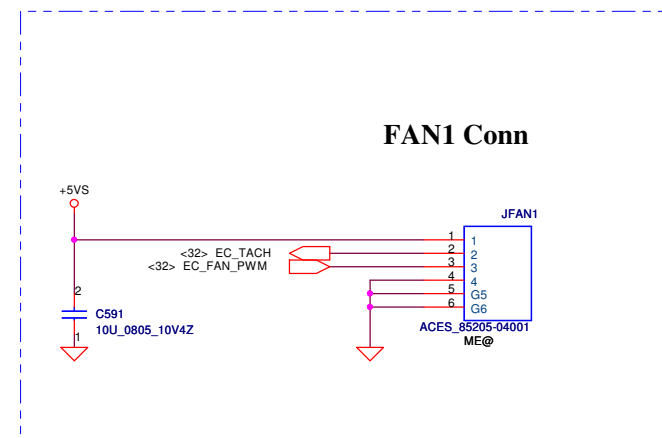


	Pin4	Configure		Pin23	Configure
		R525	C559		R516
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED[2]	

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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	LAN-AR8151/8152
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				Document Number	LA-6752P
				Date: Friday, November 26, 2010	Sheet 27 of 50

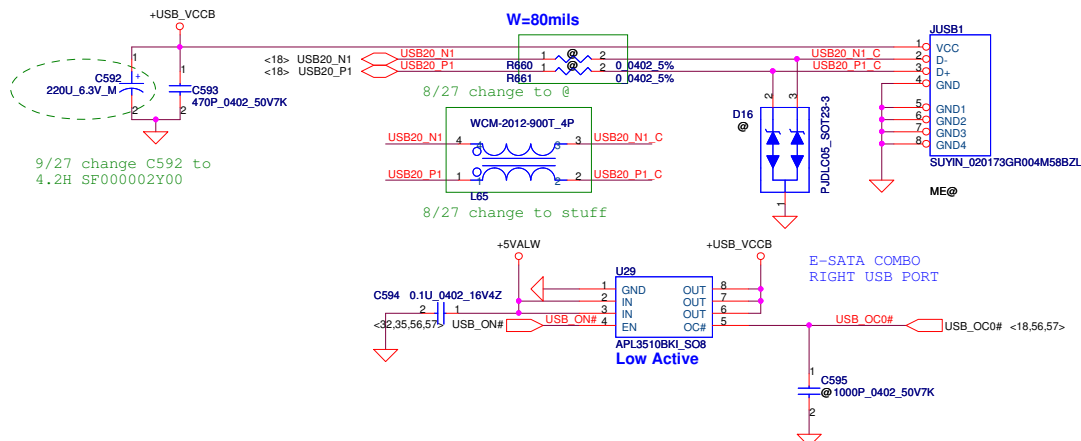


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

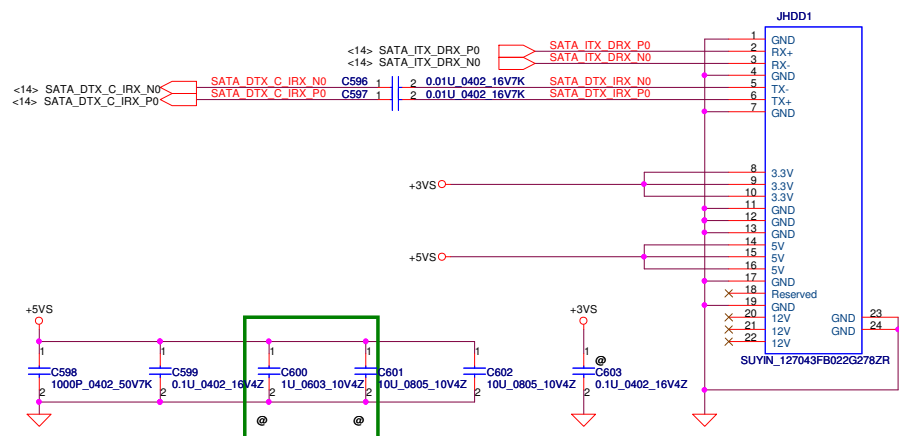


Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	EMC1403 Thermal sensor/FAN
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				Date: Friday, November 26, 2010	Sheet 29 of 50

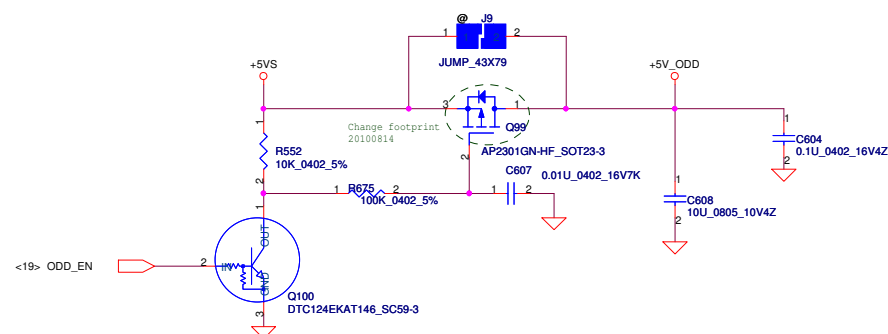
Left USB Conn.



SATA HDD Conn.



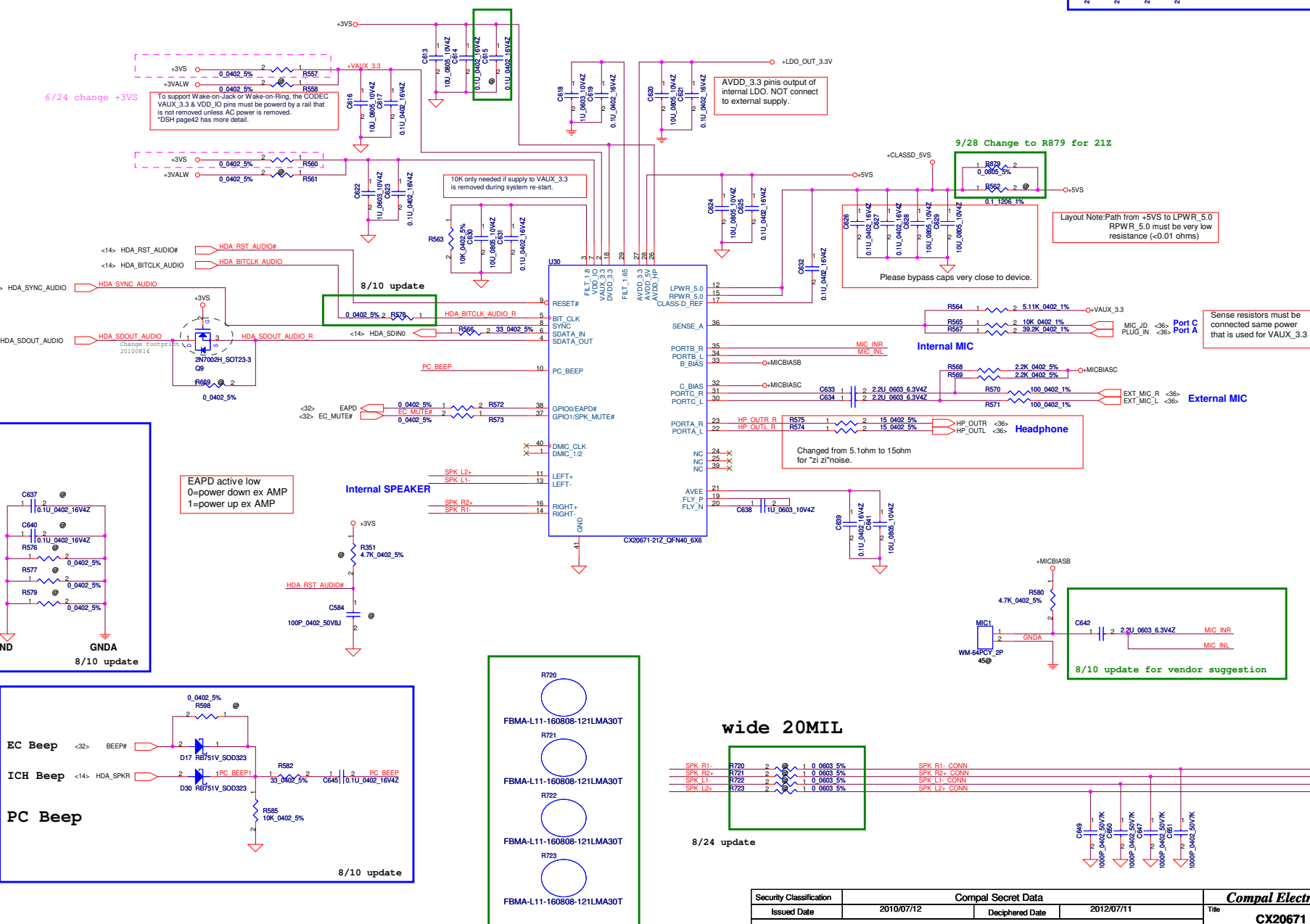
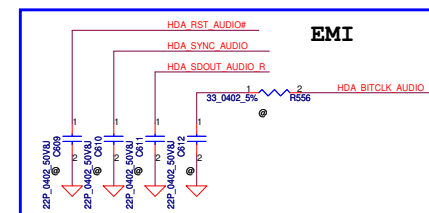
ODD Power Control



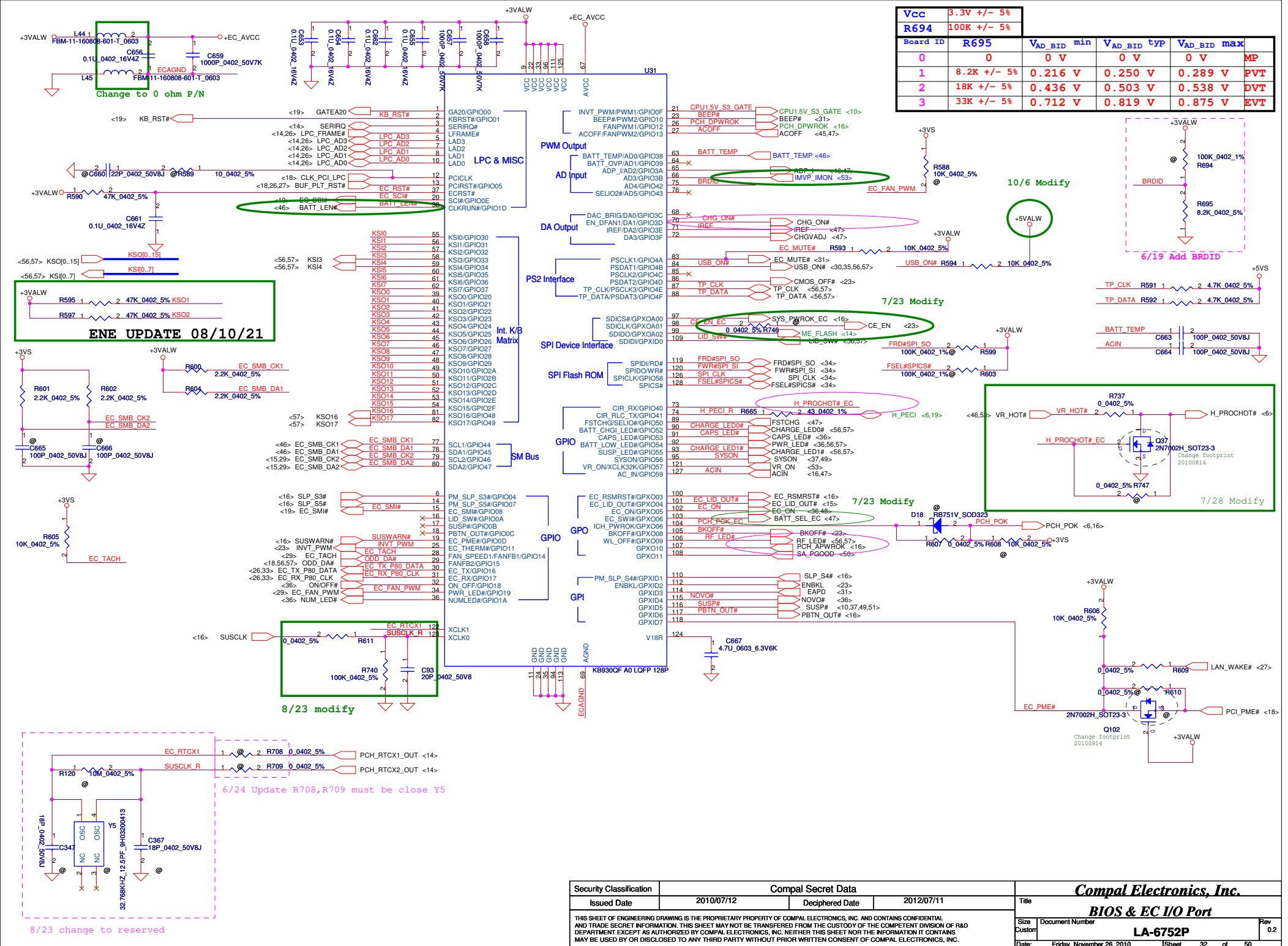
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Compal Electronics, Inc.	
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				Size B	Document Number
				LA-6752P	
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CK20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

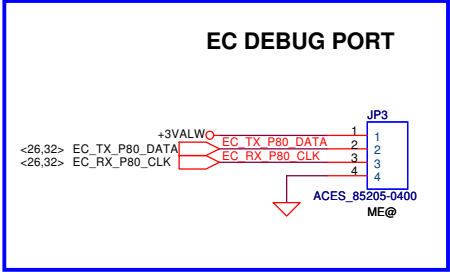
9/27 Update U30 P/N to SA00003K410



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		CX20671 Codec	
2010/07/12		2012/07/11		Size C Document Number	
				LA-6752P	
				Date: Friday, November 26, 2010	
				Sheet 31 of 50	

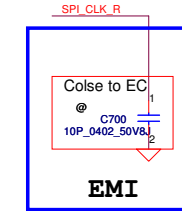
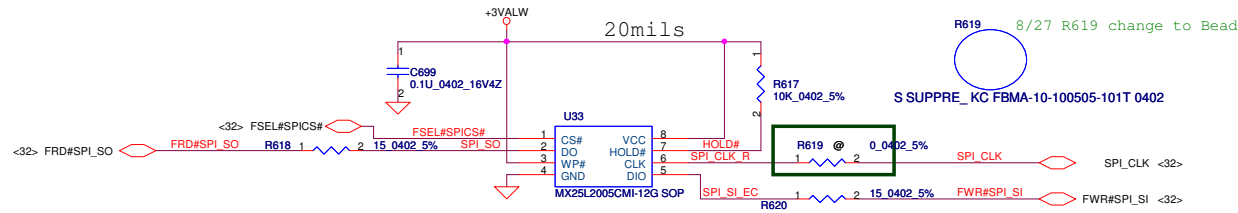


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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				Document Number	0.2
				LA-6752P	
Date:	Friday, November 26, 2010	ISheet	32	of	50

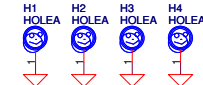


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	
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				Size B	Document Number
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FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00



H_3P8



H_3P3



H_3P0x4P5N



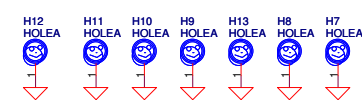
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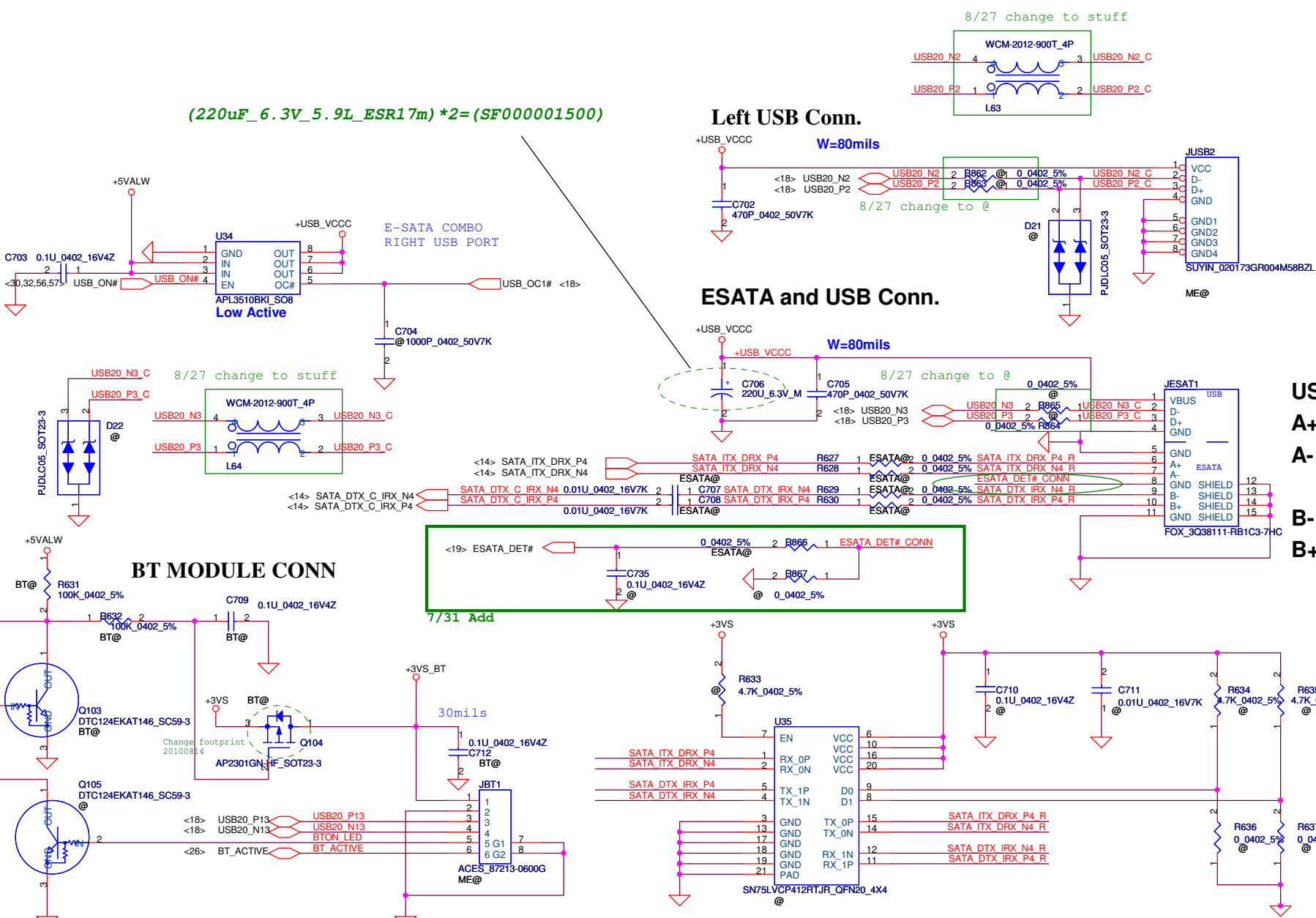
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H_2P8

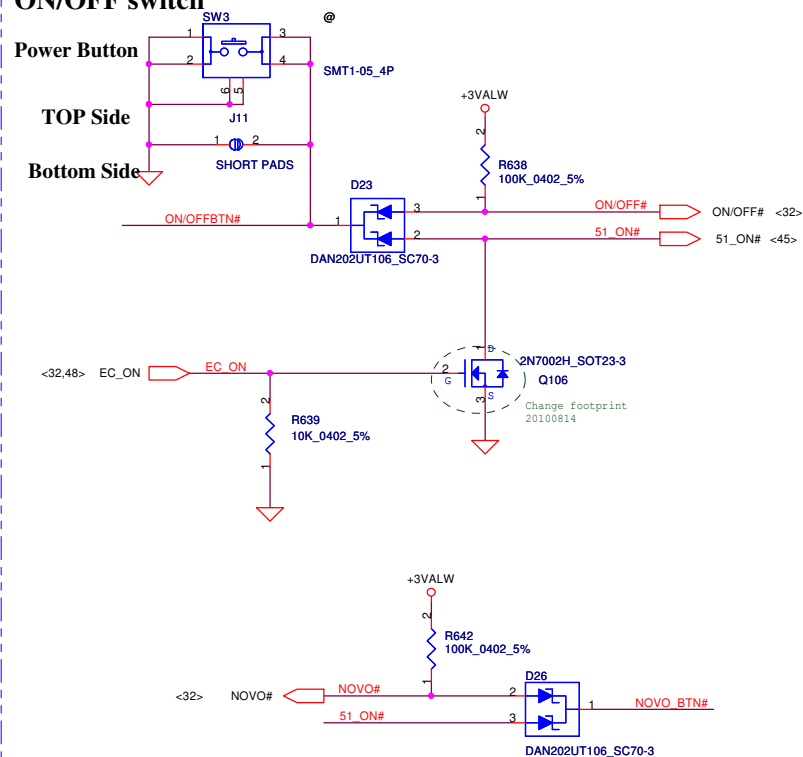


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Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title	LED/EC SPI ROM
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				Date:	Friday, November 26, 2010
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				LA-6752P	

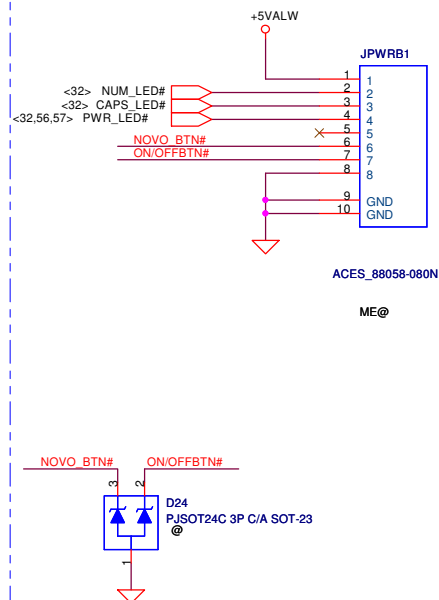


Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2010/07/12		Deciphered Date		2012/07/11		Title		
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		Size	Document Number						Rev	
		Custom	LA-6752P						0.2	
		Date:	Friday, November 26, 2010				Sheet	35	of	50

Bottom Side

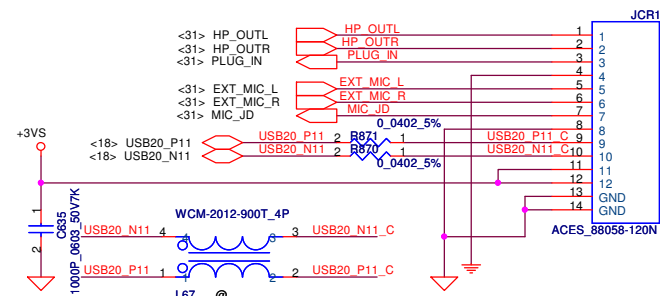


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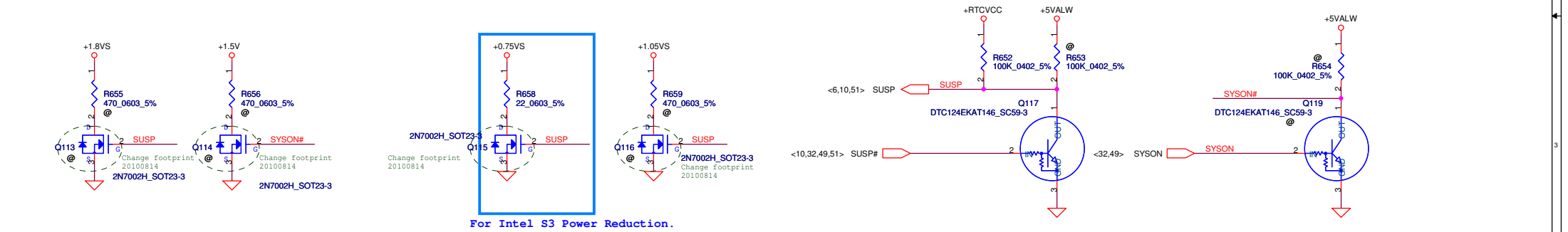
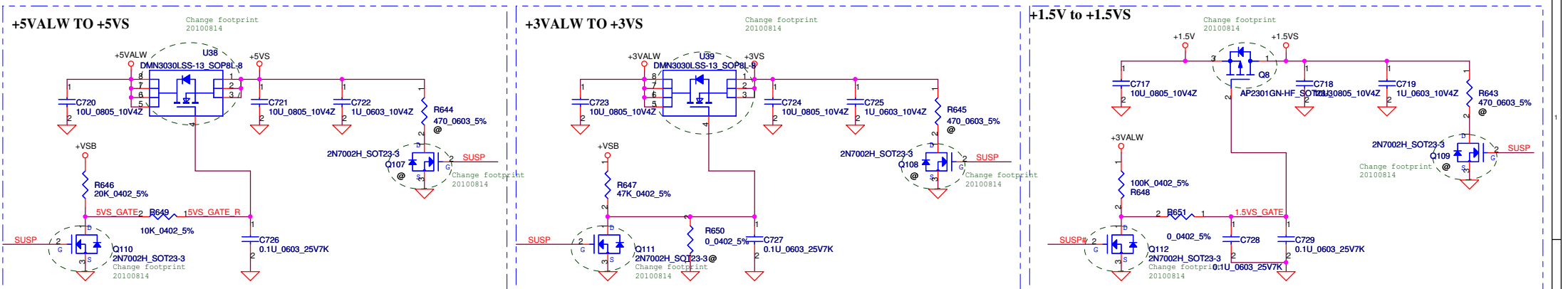


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

HP OUTL



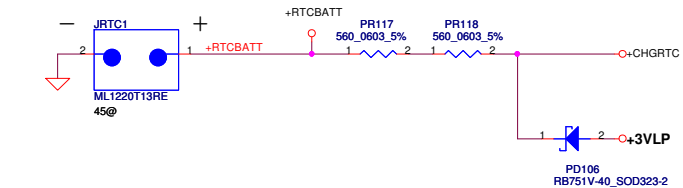
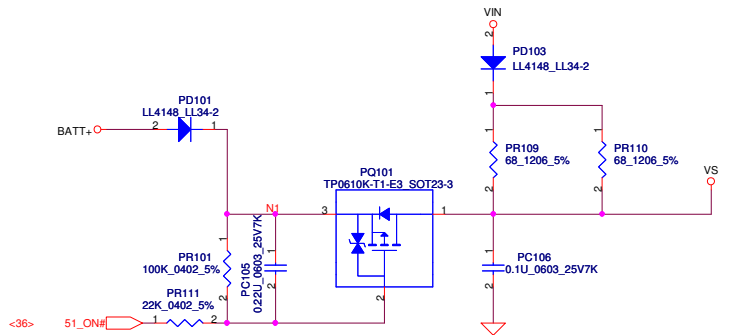
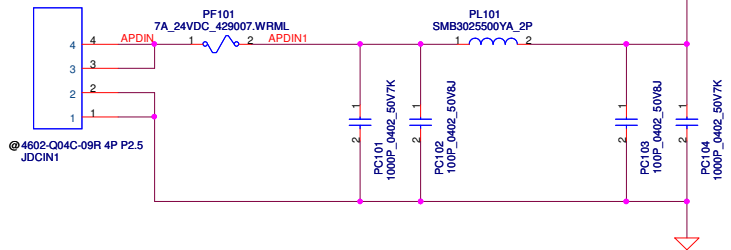
Security Classification		Compal Secret Data		Compal Electronics, Ltd.		
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title other IO connector		
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				Custom	LA-6751P	0.1
				Date:	Friday, November 26, 2010	Sheet: 36 of 50



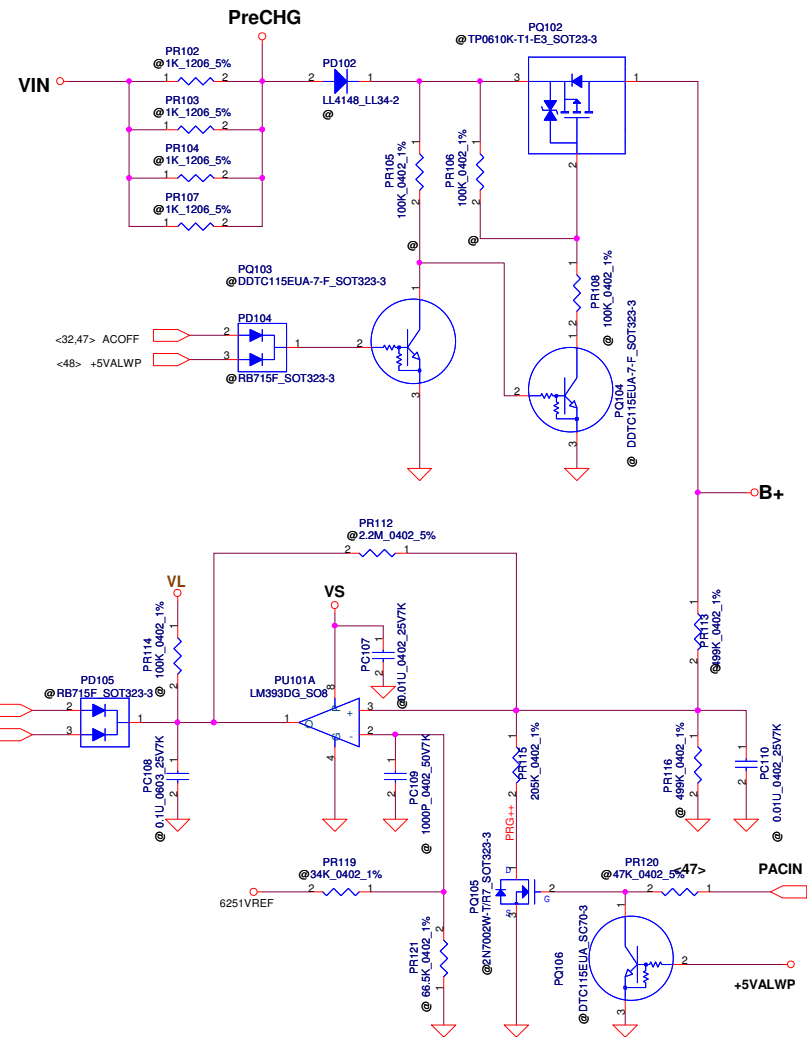
For Intel S3 Power Reduction.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2010/07/12	Deciphered Date	2012/07/11	Title
					DC Interface
					Size
					Document Number
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					Rev
					0.2

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



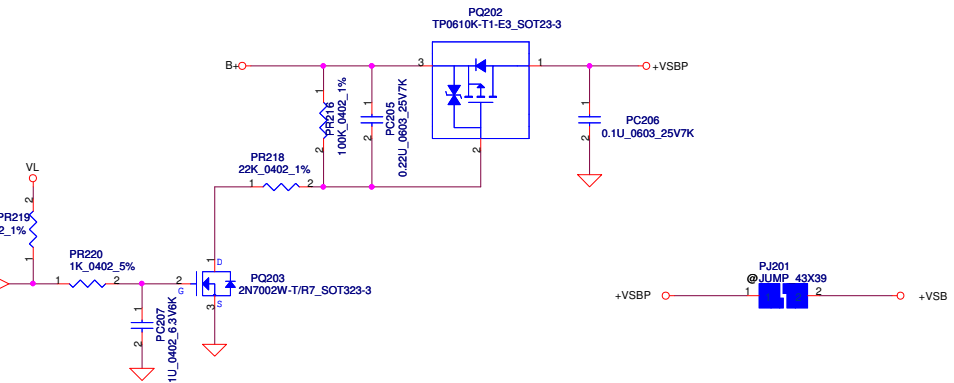
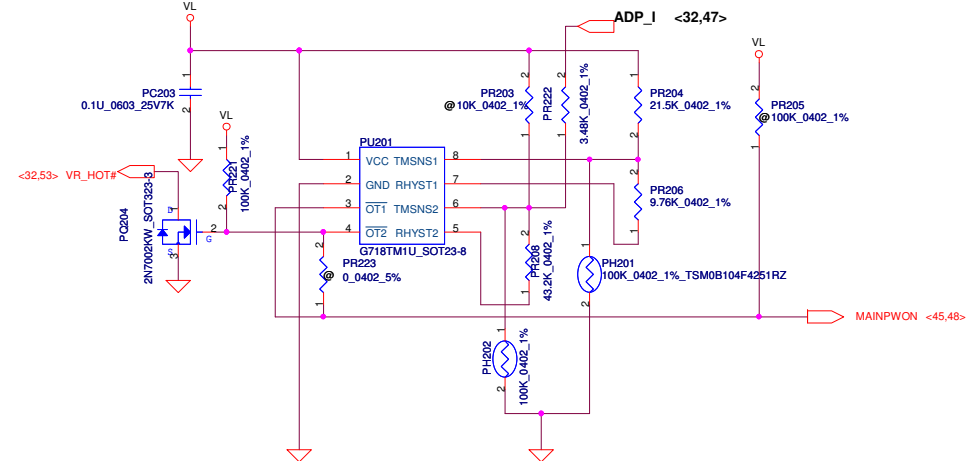
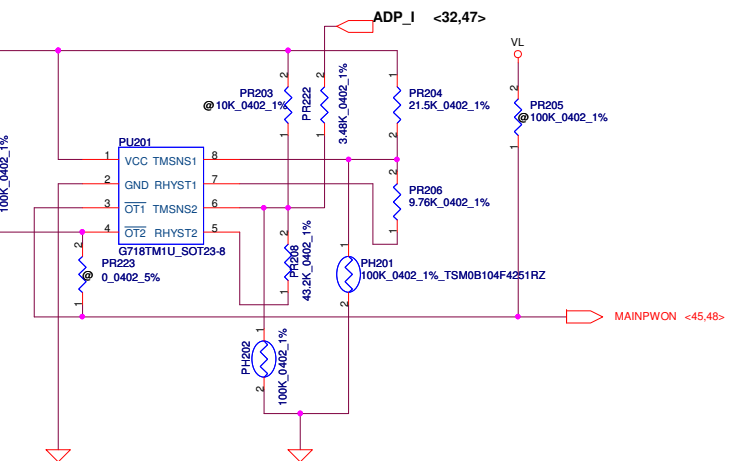
ACIN

Precharge detector			
Min.	typ.	Max.	
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

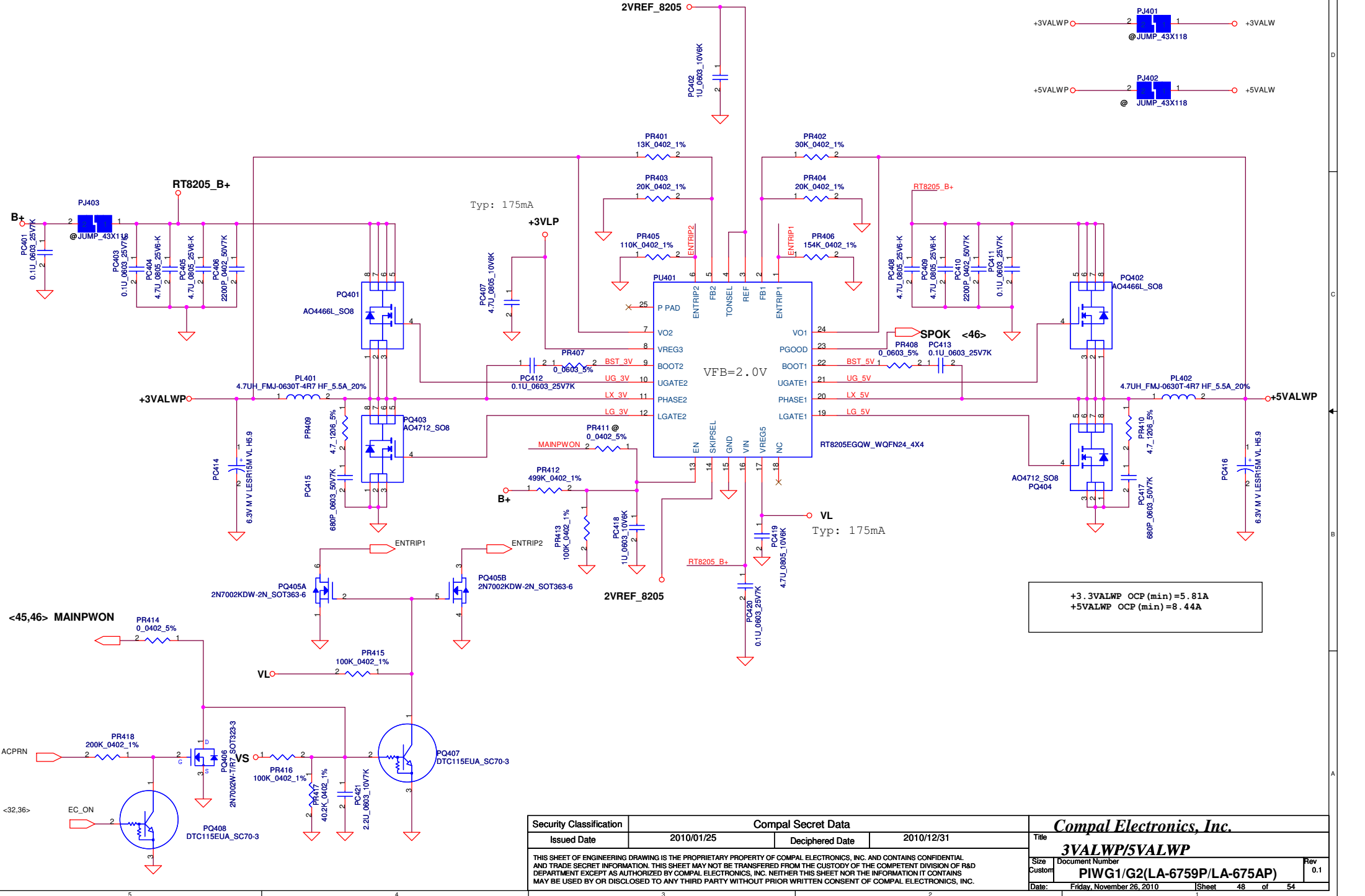
Precharge detector			
Min.	typ.	Max.	
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title PWR DCIN / Vin Detector /Pre-charge		
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				Date: Friday, November 26, 2010	Sheet 45 of 54	

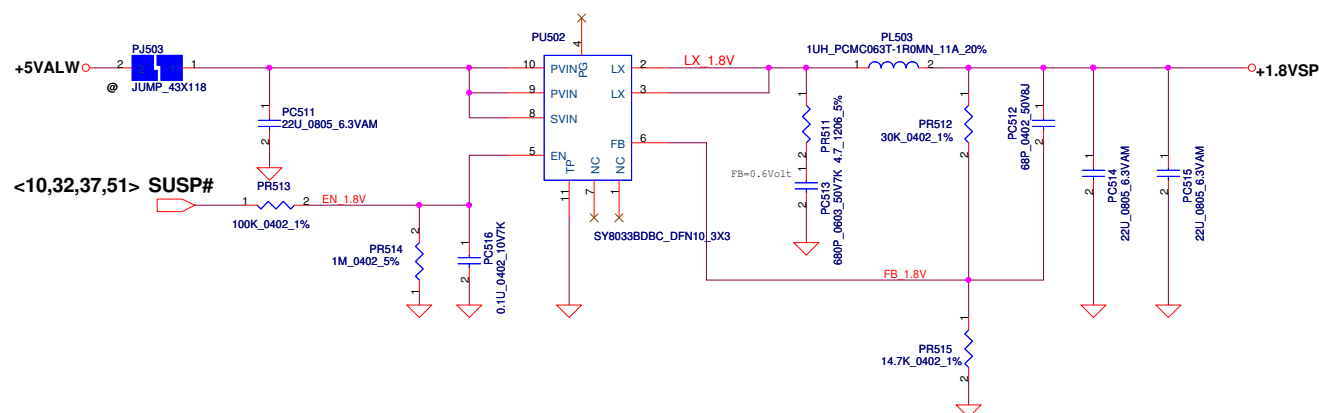
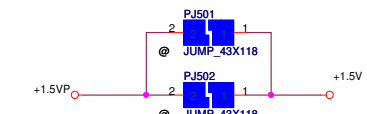
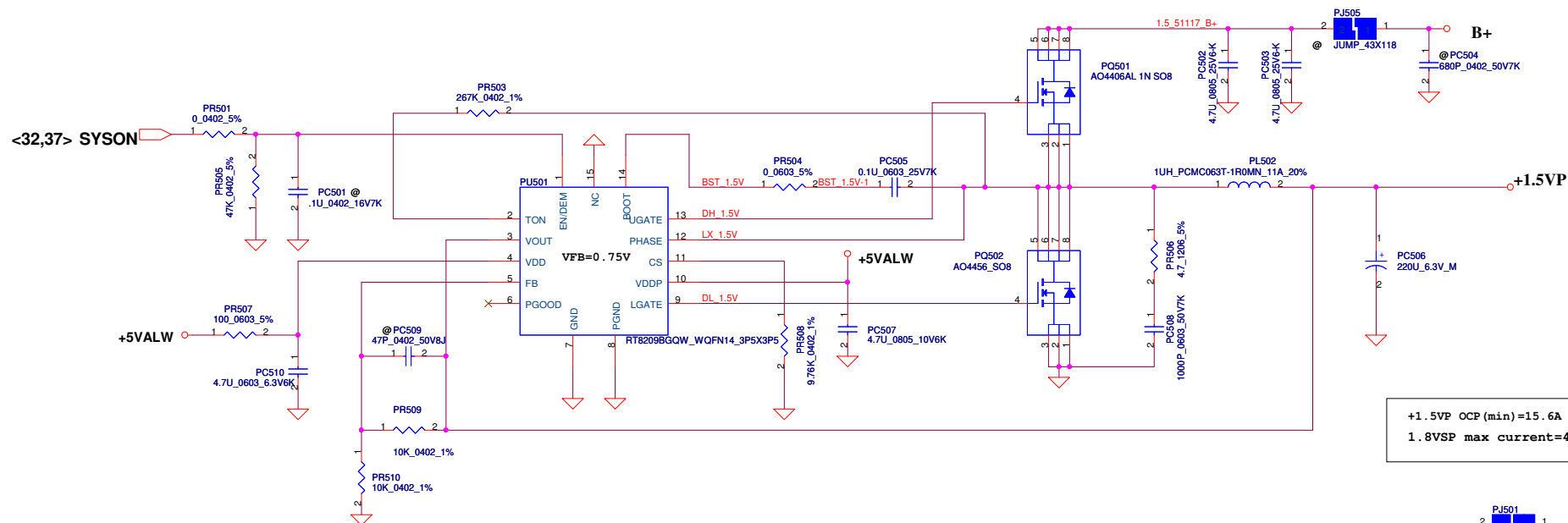


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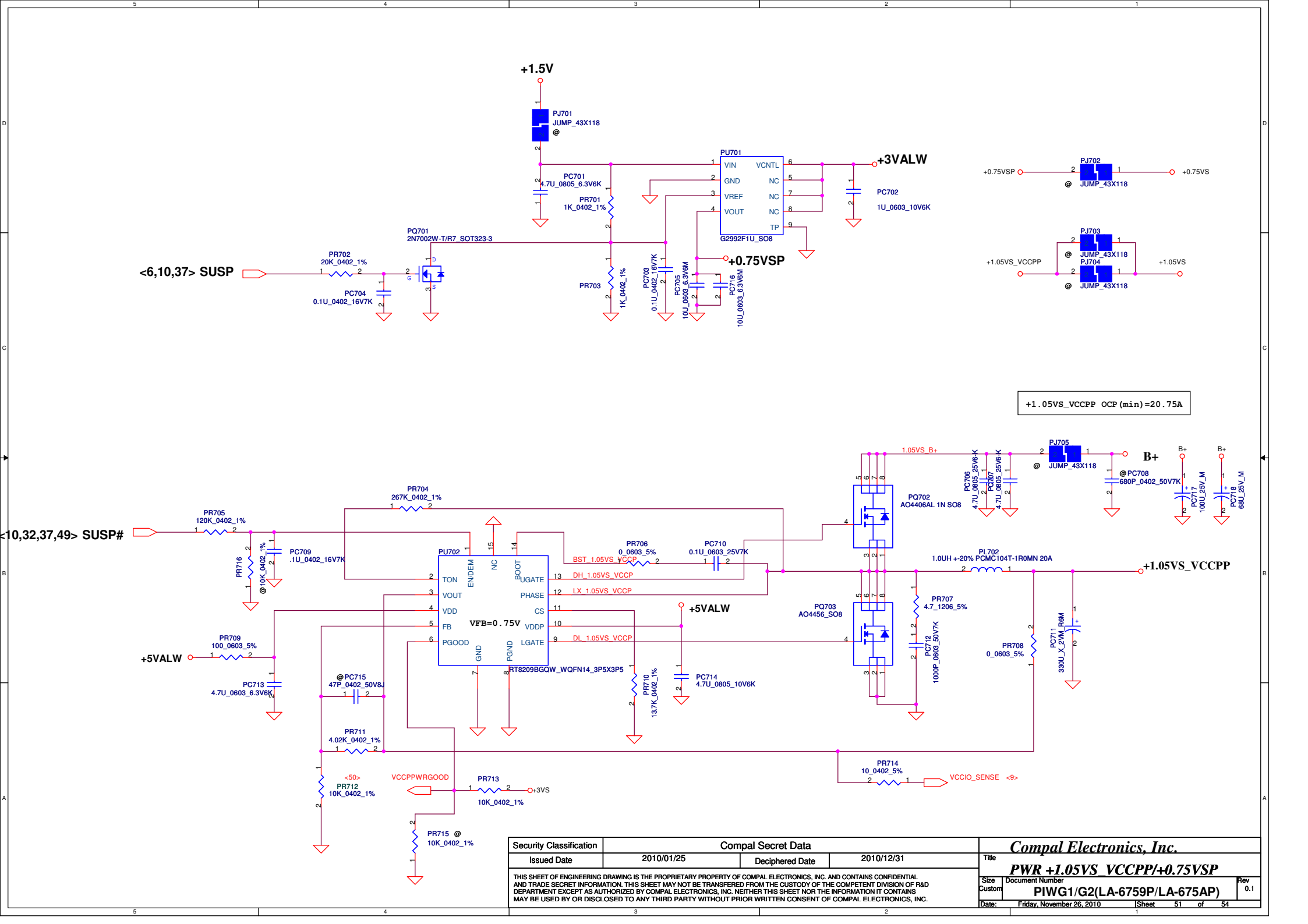
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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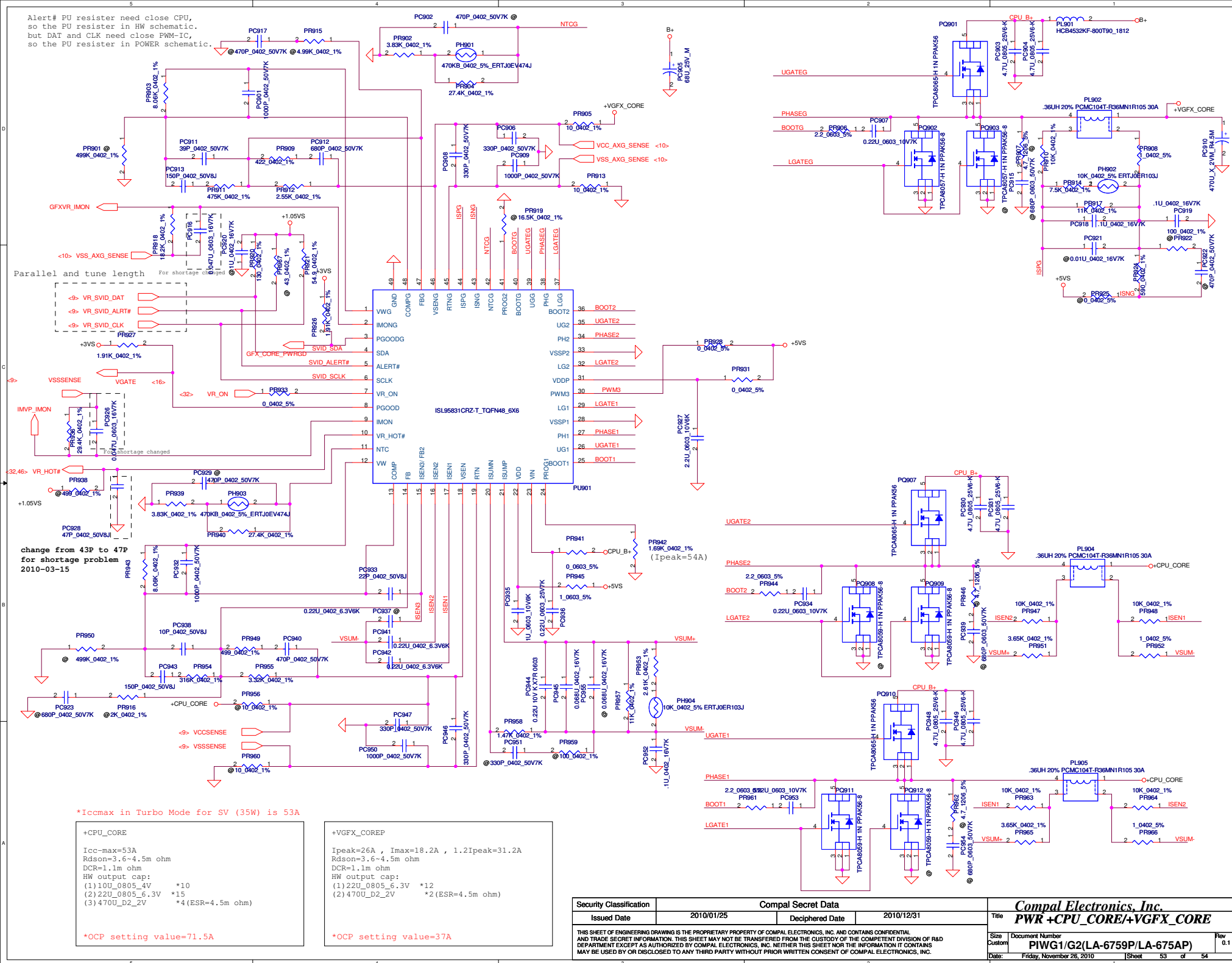


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				Rev	0.1

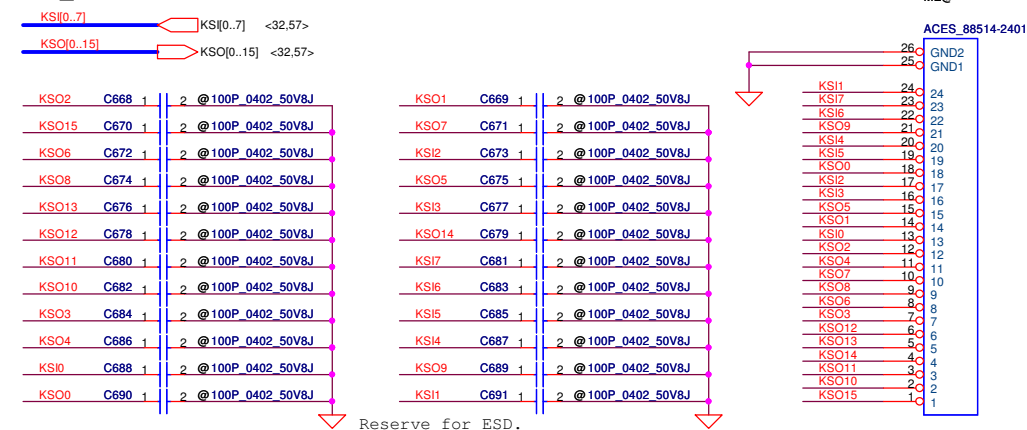
Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



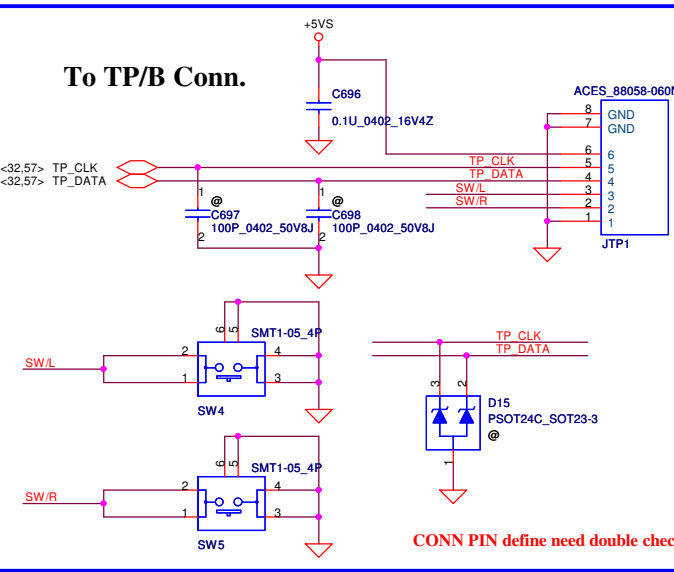
Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
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7					
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17					

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				PIWG1/G2(LA-6759P/LA-675AP)	
				Rev 0.1	
Date: Friday, November 26, 2010				Sheet 54 of 54	

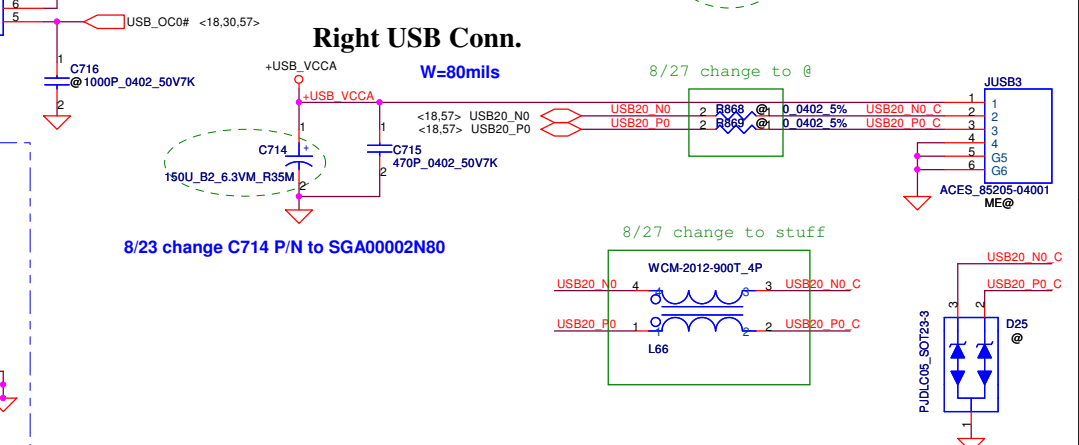
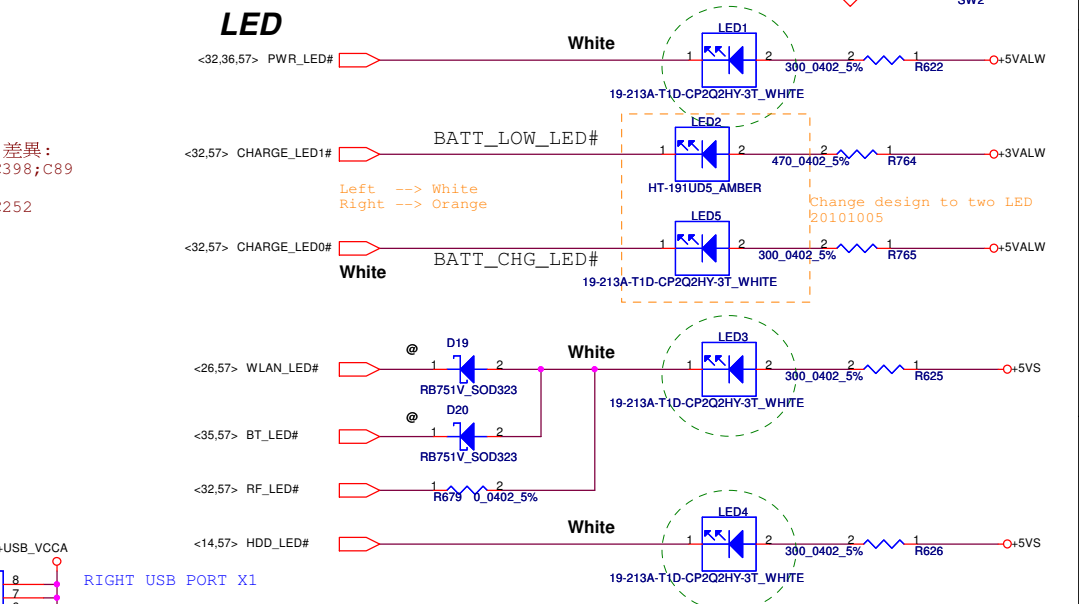
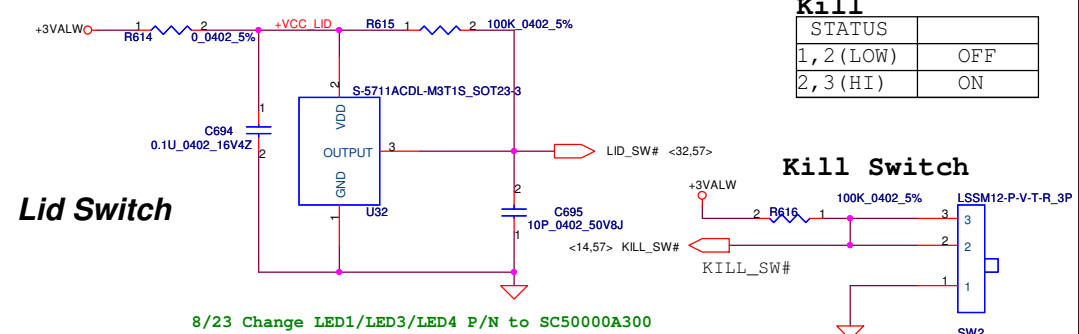
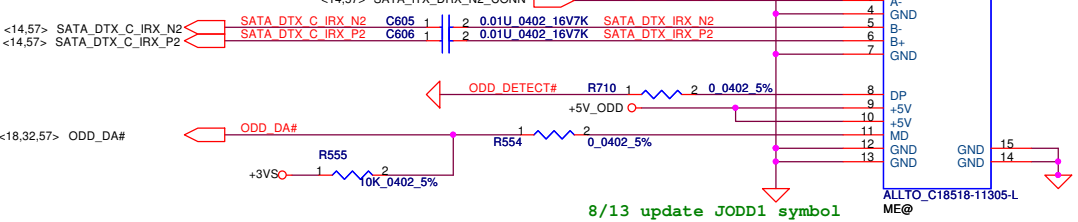
INT_KBD Conn.



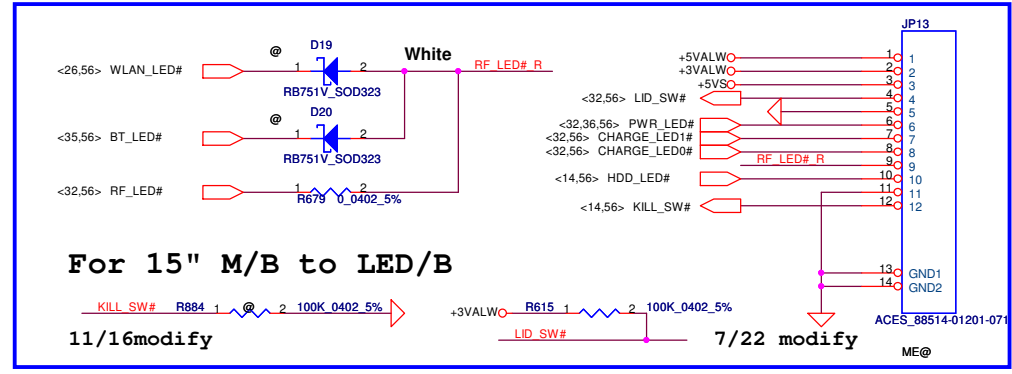
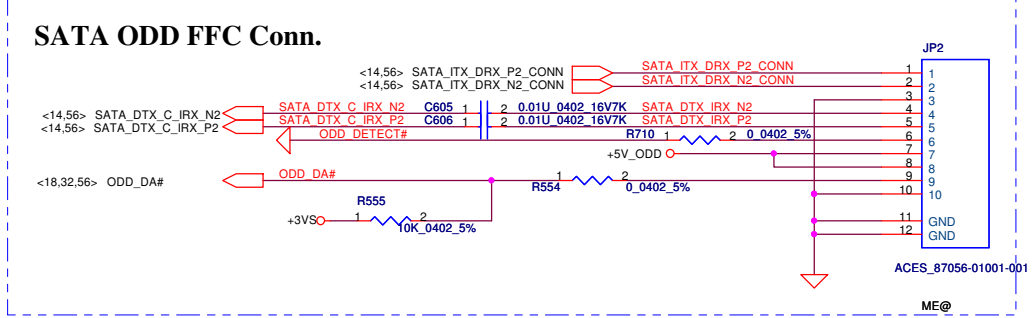
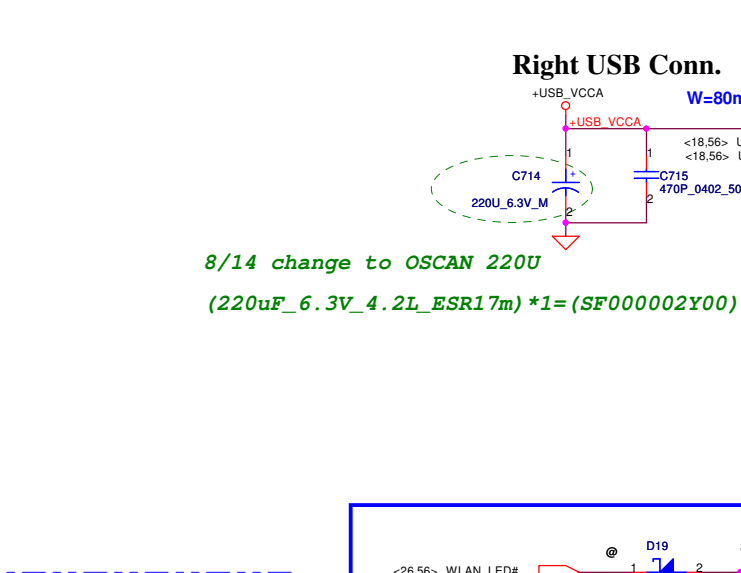
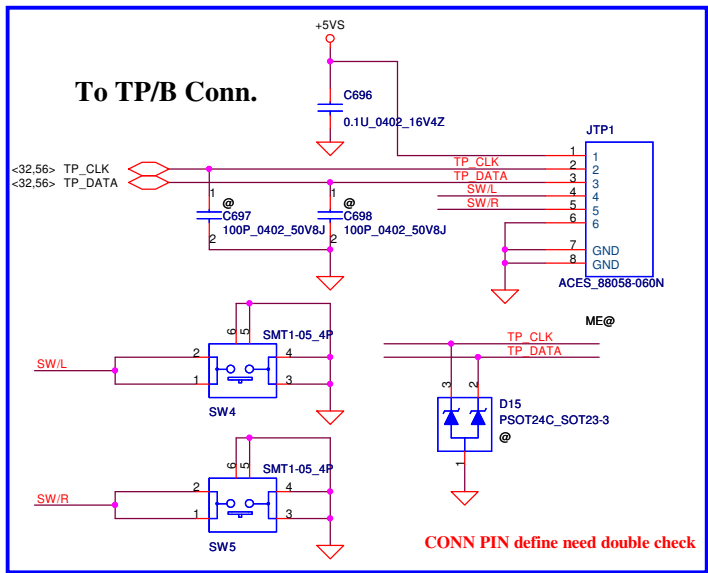
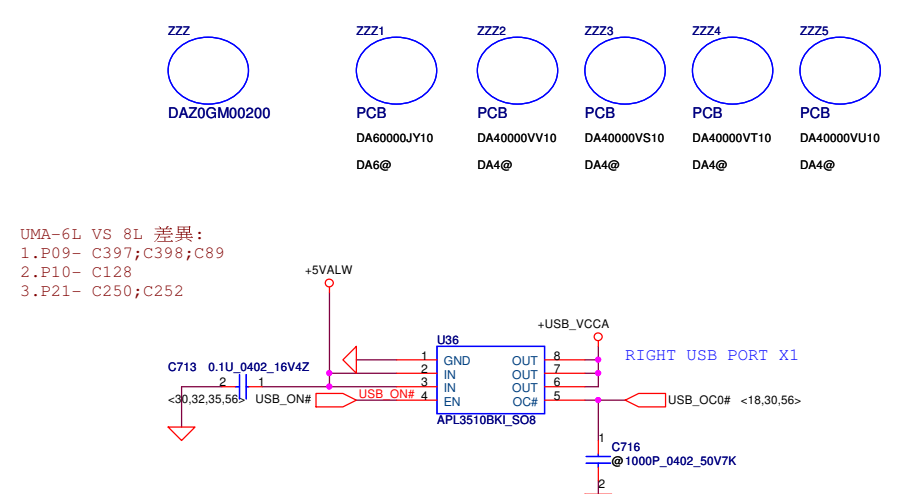
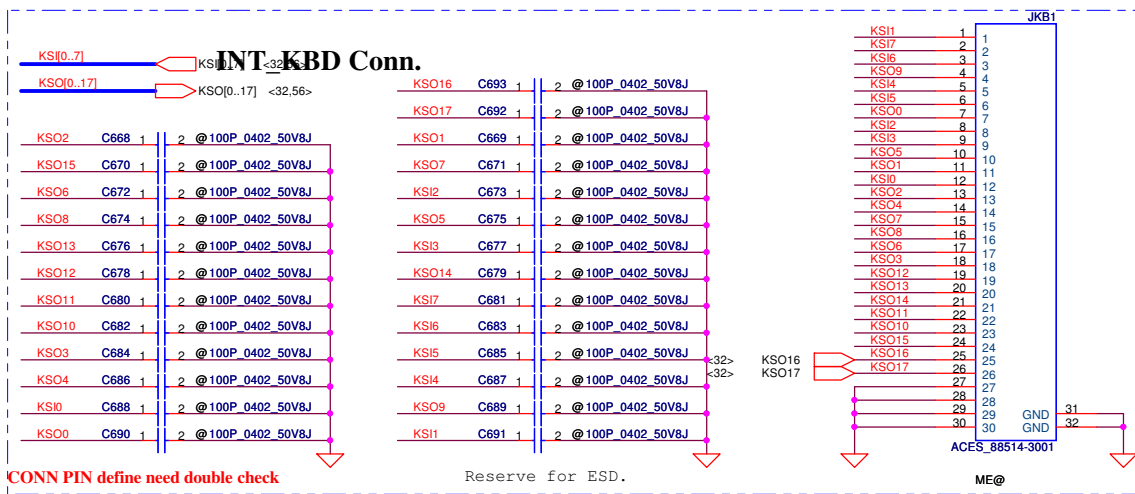
CONN PIN define need double check



SATA ODD Conn.



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	5		3		2		1
	PHASE	PAGE	Modification list		PURPOSE		
	0.2	P16	D29 change to @		For AC detect issue		
	0.2	P24	R548,R549 change to DIS@		For AC detect issue		
	0.2	P10	C128 change to stuff		For test on DVI		
	0.2	P44	Del Q118, R657		For not need		
	0.2		Change R513, R516 ,R667 P/N and from 0805 to 0603		For common part		
	0.2		Change C633, C634 , C642		For common part		
	0.2		Change D3, D29 P/N and symbol		For common part		
	0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol		For common part		
	0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol		For common part		
	0.2		Change Q8,Q65,Q80,Q83,Q99,Q104 P/N and symbol		For common part		
	0.2		Change Q1,Q37,Q93 P/N and symbol		For common part		
	0.2		Change Q94, Q95 P/N and symbol		For common part		
	0.2		Change Q3,Q4,Q7,Q9,Q66,Q67,Q68,Q73,Q74,Q75,Q76,Q77,Q78, Q79,Q82,Q85,Q86,Q87,Q102,Q106,Q107,Q108,Q109,Q110,Q111,Q112,Q113,Q114,Q115,Q116 P/N and symbol		For common part		
	0.2		Change C635 part and change to @		For EMI		
	0.2	P18	Reserved R297		Reserved		
	0.2	P9	Change C53,C85,C86,C87 ,C397,C398,C399 to stuff and change ,C48,C80,C81,C82, C90,C91 to @ Del C89		For CPU_CORE		
	0.2	P10	Change C110,C111,C112,C113 to stuff		For VGFX_CORE		
	0.2	P56	Change LED1/LED3/LED4 P/N to SC50000A300		Change P/N		
	0.2	P36	Change T1,T2 P/N to SP050003N00		For test pass part		
	0.2	P40	Change R611,R740,C93 to stuff and change Y5,C347,C367 to @ Change R695 to 18K, Q37 change to @, R747 change to stuff,		For SUS_CLK R695 for Board ID, Q37, R747 for VR_HOT		
	0.2	P40	Change U33 P/N to SA00003FL10		For BIOS ROM		
	0.2		Change C509,C511,C635 to stuff		For EMI		
	0.2	P56	Change I4" C714 P/N to SGA00002N80		For Sourcer request		
	0.2	P39	Change R720,R721,R722,R723 P/N to SM01000BZ00 (Bead), and Change C647,C649,C650,C651 to Stuff		For EMI request		
	0.2	P19	Change R303 to Stuff, and change R542 to @		For BIOS ESATA detect function		
	0.2	P56	Change U32 P/N to SA000031C00		For common part		
	0.2	P36	Change T1,T2 P/N to SP050006E00		For correct part		
	0.2	P10	R688 change to stuff , R687 ,Q7 change to @ Change R660,R661,R862,R863,R864,R865,R868,R869 to @ , change L63,L64,L65,L66 to stuff , change R619 to Bead (SM01000DI00)		For S3 power reduction For EMI		
	0.2	P20	Change L75 symbol		For common part		
	0.2	P30	Change R402 to @		For DPST		
	0.3	P10	Update Q5 symbol		For update symbol		
	0.3	P33	Add F2		For safty request		
	0.3	P39	Update U30 P/N to SA00003K410 and Add R879		For Audio update to 21Z		
	0.3	P10	Change CI28 to D2 size and @		Change size for M/E issue		
	0.3	P14	Add reserve R878		For Intel DG 1.5		
	0.3	P37	C592 change P/N to SF000001500 (H=6)		For ME Z high ok		
	0.3	P29	R369 P/N change to SD034100A80		For GP part		
	0.3	P6	Reserved R880 to SYS_PWROR		Follow ORB		
	0.3	P10	R62,R63 change to 1K		Follow CRB		
	0.3	P33	R483,R484 change connect to +5V_HDMI_F		For Add F2		
	0.3	P37	Change U27 P/N to SA000046C00		For Fintek		
	0.3	P40	Change R594 pull high to +5VALW		For leakage issue		

PHASE	PAGE	Modification list	PURPOSE
0.3	P19	R881 change to Dtuff, R244 change to @	For intel MRC Rev0.9
0.3	P14	R878 change to stuff	For intel DG 1.5
0.3	P31	Del R432	For non-used part
0.3	P36	Reserved D31 , C643 , C644	For reserved EMI parts
0.3	P37	Del R581	For non-used part
0.3	P38	Del R550	For non-used part
0.3	P38	Change C592 P/N to SF0000002Y00	For M/E Z high limlt
0.3	P39	Del R584, R586 , R587	For non-used part
0.3	P40	Change R600, R604 to 2.2K Change R695 to 8.2k	Change R600, R604 for Battery SMBus, R695 for Board ID
0.3	P42	Del R583	For non-used part
0.3	P31	Del R449, R452, R458, R460 (UMA change only)	For non-used part
0.3	P32	Del R478, R480, R486 (UMA change only)	For non-used part
0.3	P6	Reserved R882 connect to PCH_PWR0K	Reserved for intel
0.3	P56	R765 change to 300 ohm	For LED

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