LCFC Confidential

AILZA/B/C (ZX10)

MB MA181 Schematics

Intel Haswell Processor with DDRIIIL + Lynx Point HM86
nVIDIA N14P-GV2

2012-12-27

REV:1.1

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Title: Cover Page		
Size: Custom	Document Number: 401025	Rev: 1.1
Date: Friday, July 12, 2013	Sheet 1 of 61	

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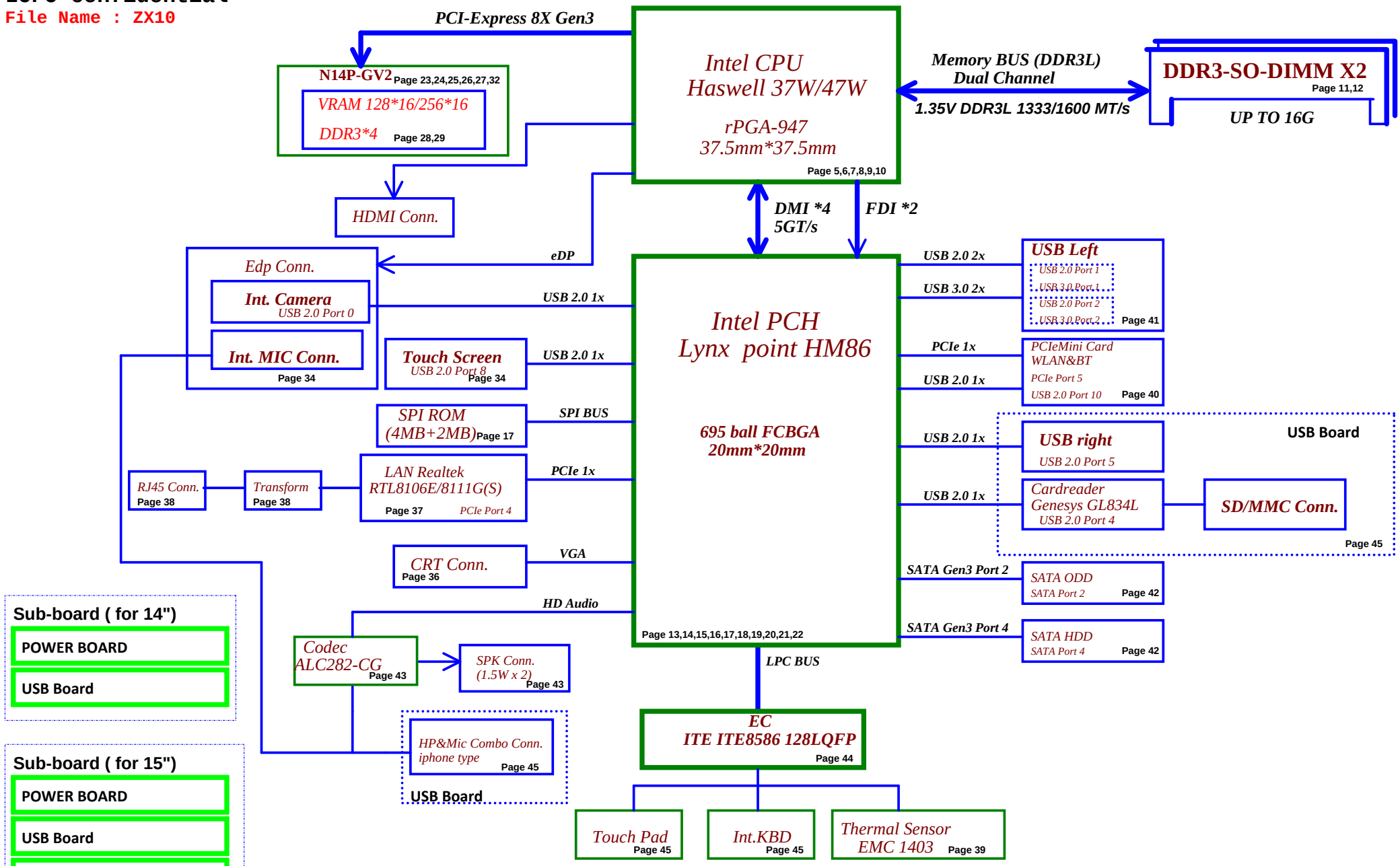
File Name : ZX10



Sub-board (for 14")

- POWER BOARD
- USB Board

Sub-board (for 15")

- POWER BOARD
- USB Board
- LED Board
- ODD Board

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Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **Block Diagram**

Size: Custom	Document Number: 401025	Rev: 1.1
Date: Friday, July 12, 2013	Sheet 2 of 61	

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW / +5VALW	+3V_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.675VS +CPU_CORE +VGA_CORE +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	X	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
EHCI1	XHCI 1	0	Camera
		1	USB Port (Left Side)
		2	USB Port (Left Side)
		3	
	2	4	Cardreader
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	TOUCH PANEL
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	

BOM Structure Table

BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	External GPU SKU ID part
UMA@	UMA SKU ID part
14@	For Z410 part
15@	For Z510 part
8106@	8106E LAN part
8111G@	8111G LAN Part
8111GS@	8111GS LAN Part
N14PGV2@	N14P GV2 stuff
GIGA@	GIGA LAN Part
Gastube@	Gastube Part
NOTS@	No Touch screen part
GC6@	GPU GC6 function part
TS@	Touch screen part
@	Not stuff
ME@	Connector
XDP@	XDP part
37@	37W CPU part
47@	47W CPU part
H2@	Hynix 2Gb Vram part
M2@	Micron 2Gb Vram part
M4@	Micron 4Gb Vram part
S2@	Samsung 2Gb Vram part
S4@	Samsung 4Gb Vram part
M1GB@	Micron 1GB Vram BOM
M2GB@	Micron 2GB Vram BOM
S1GB@	samsung 1GB Vram BOM
S2GB@	samsung 2GB Vram BOM
H1GB@	hynix 1GB Vram BOM

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	XDP
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VS_VGA	X	V +3VS	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3V_PCH	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS	X	V +3VS

PCIE PORT LIST

Port	Device
1	
2	
3	
4	LAN
5	WLAN
6	
7	
8	

	Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
HM86	USB3 1	USB3 2	NA	NA	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 6Gb/s 4 (1b)	SATA 6Gb/s 5 (1b)	SATA 3Gb/s 0	NA	SATA 3Gb/s 2	NA
					USB3 3 (01)	USB3 4 (01)							PCIE 1 (0b)	PCIE 2 (0b)				
HM87 QM87	USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 6Gb/s 4	SATA 6Gb/s 5	SATA 6Gb/s 0	SATA 6Gb/s 1	SATA 3Gb/s 2	SATA 3Gb/s 3
					USB3 4	USB3 5							PCIE 2	PCIE 3				

Soft Strap: (USB3P4_PCIEP2_MODE)
00: PCIe Lane 2 is statically assigned to PCIE Express (or GbE)
01: PCIe Lane 2 is statically assigned to USB3 Port 4

Soft Strap: (USB3P3_PCIEP1_MODE)
00: PCIe Lane 1 is statically assigned to PCIE Express (or GbE)
01: PCIe Lane 1 is statically assigned to USB3 Port 3

*

Config	GPIO16,49
SATA4,SATA5	11
PCIE1,PECI2	00

EC SM Bus1 address

Device	
Smart Battery	0001 011X b
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
VGA	0x9E
PCH	0x96

PCH SM Bus address

Device	Address
DDR DIMMA	0xA0
DDR DIMMB	0xA2
Wlan	Rsvd
TP	0x2C for Synaptics 0x15 for ELAN vendor

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Issued Date	2012/12/14	Deciphered Date	2012/12/21

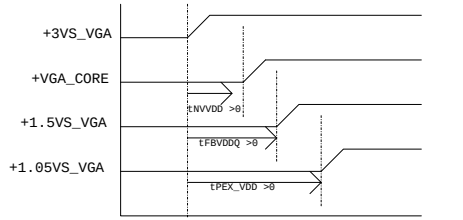
Title: Notes List

Size: Custom | Document Number: 401025 | Rev: 1.1

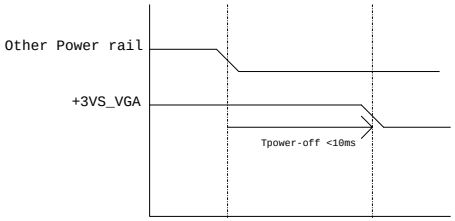
Date: Friday, July 12, 2013 | Sheet 3 of 61

VGA and GDDR3 Voltage Rails (N14P GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	IN	-	FB Clamp monitor
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5		N/A	
GPIO6	OUT	-	Active low FB Clamp toggle request
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (A)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N14P 64bit 1GB/2GB DDR3	25W	TBD	1000MHz	TBD	32	TBD	1.7	2.55	TBD	TBD	1.98	2.1	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

GPU	Device ID
N14P-GV2	0x1292

SMB_ALT_ADDR (ROM_SO Bit 1)	setting	I2C Slave addrees ID
	0	0x9E (Default)
	1	0x9C

GPU	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P-GV2	TBD	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PD 15K	PD 4.99K	PU 45.3K

GPU		N14P_GV2		
FB Memory (DDR3)		ROM_SI		
Samsung 1GHz	K4W2G1646E-BC1A 128M x 16	0x7 PD 45.3K		
Micron 1GMHz	MT41J128M16JT-093G:K 128M x 16	0x5 PD 30.1K		
Hynix 1GMHz	H5TC2G63FFR-11C 128M x 16	0x4 PD 24.9K		
Samsung 900MHz	K4W4G1646B-HC11 256M x 16	0x3 PD 20K		
Micron 900MHz	MT41K256M16HA-107G:E 256M x 16	0x1 PD 10K		

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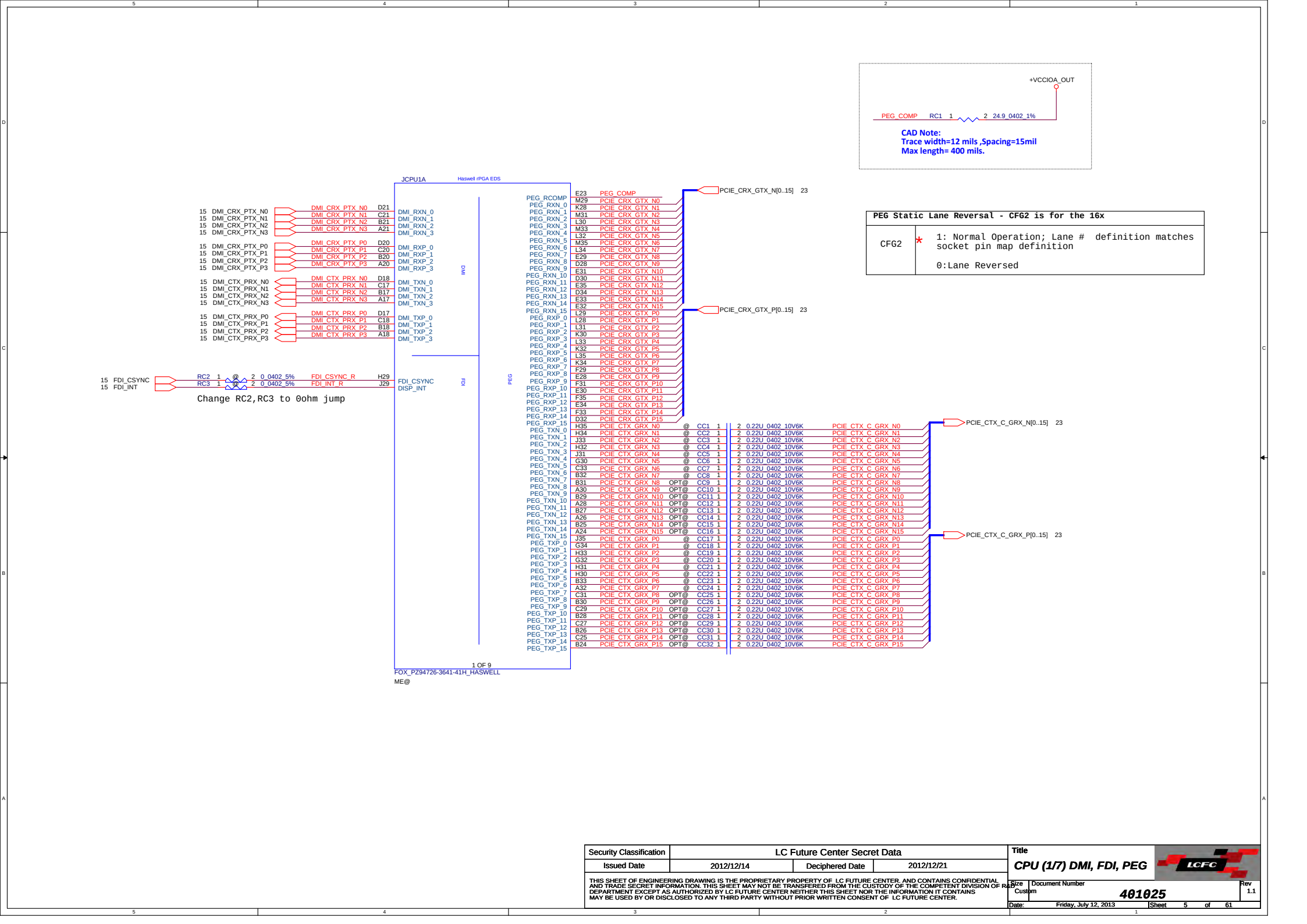
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: VGA Notes List

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 4 of 61



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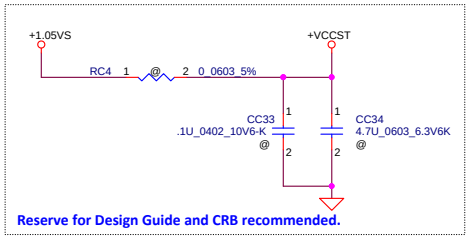
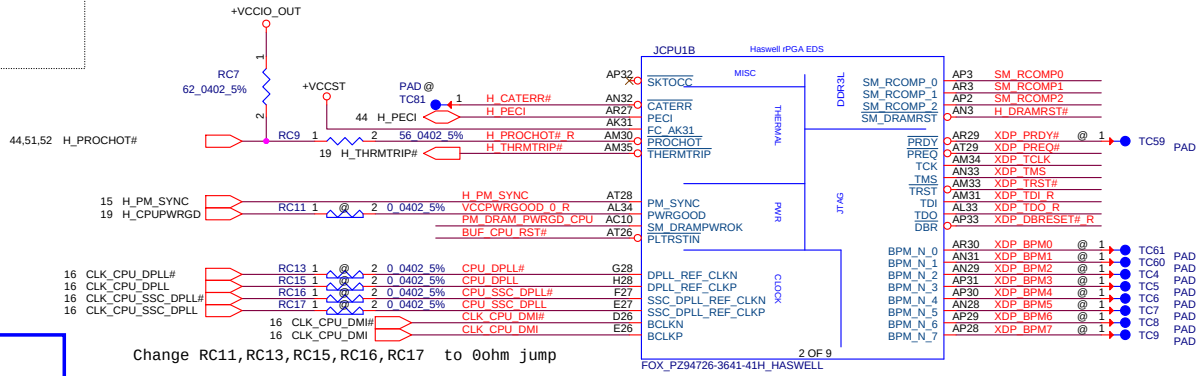
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: CPU (1/7) DMI, FDI, PEG

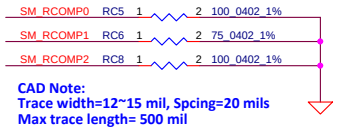
Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 5 of 61

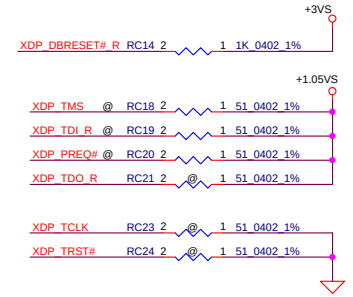




DDR3 COMPENSATION SIGNALS

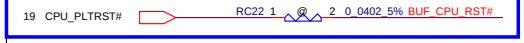


PU/PD for JTAG signals



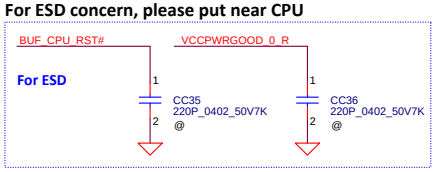
Buffered Reset to CPU

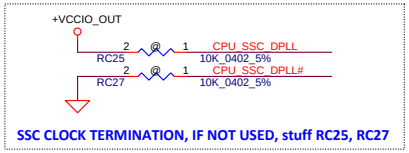
1.05V

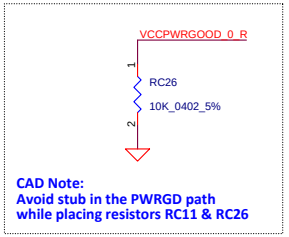


Change RC22 to 0ohm jump

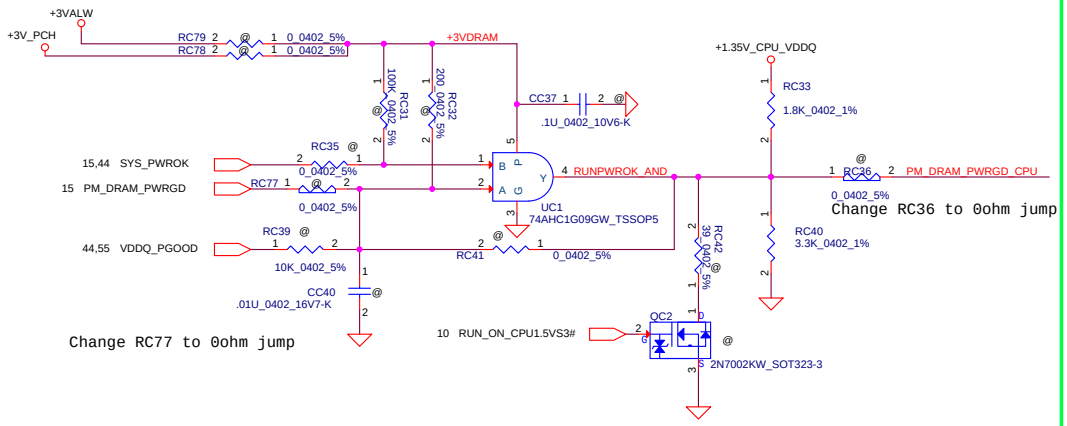
For ESD concern, please put near CPU



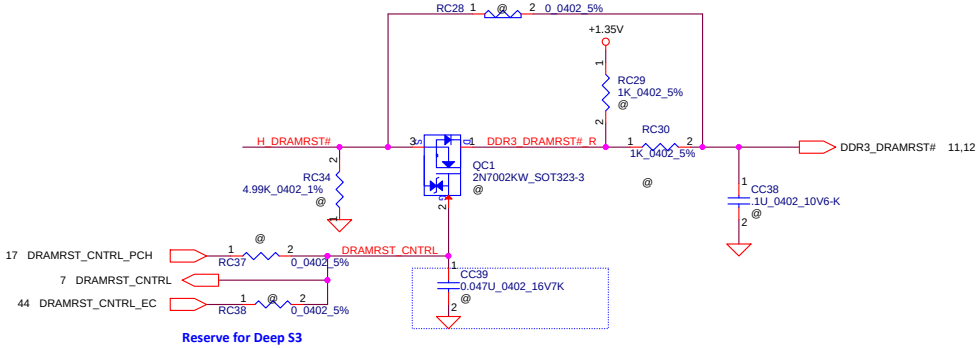




SM_DRAMPWROK with DDR Power Gating Topology



Change RC28 to 0ohm jump



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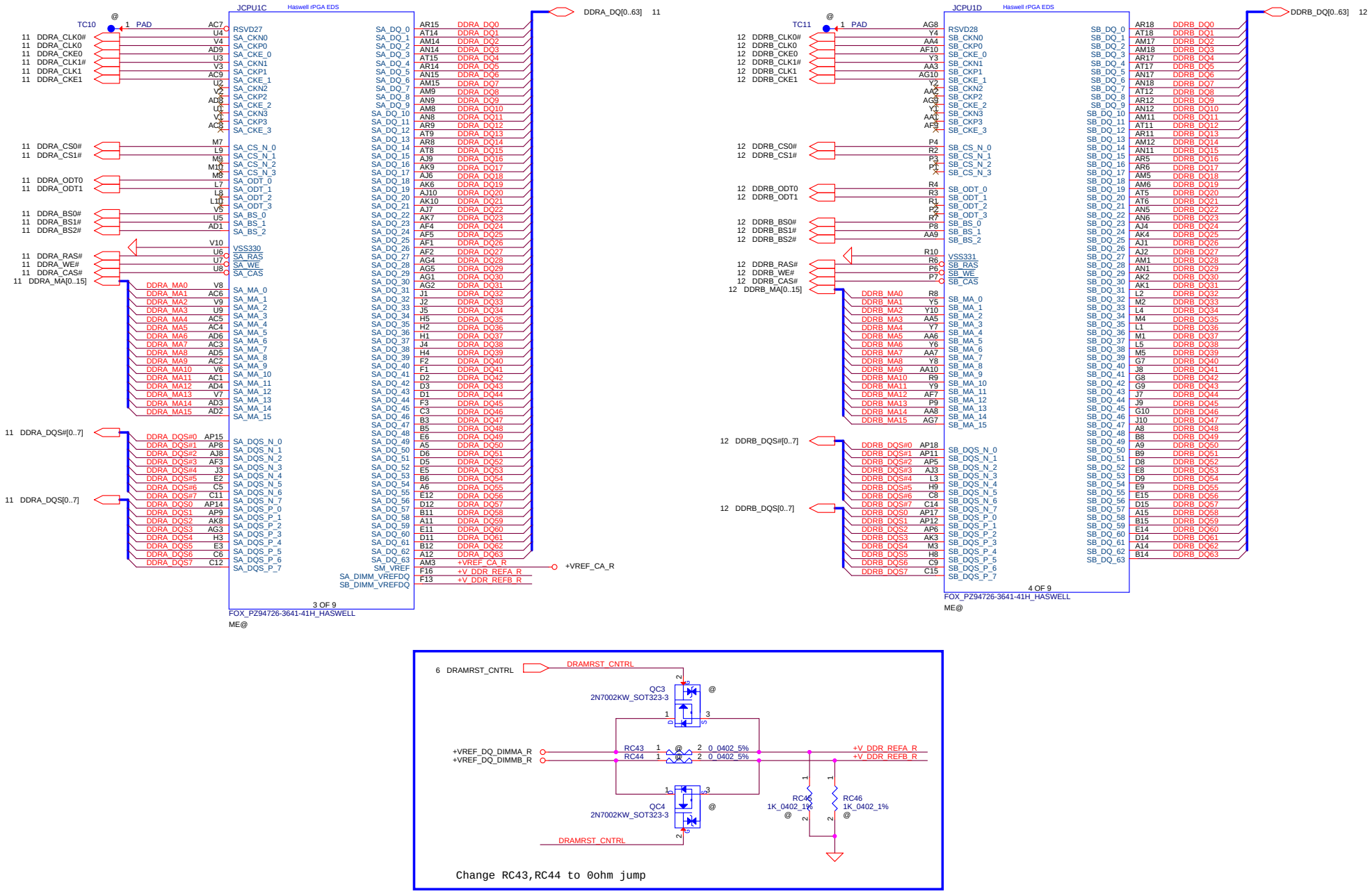
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: CPU (2/7) PM, XDP, CLK

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 6 of 61

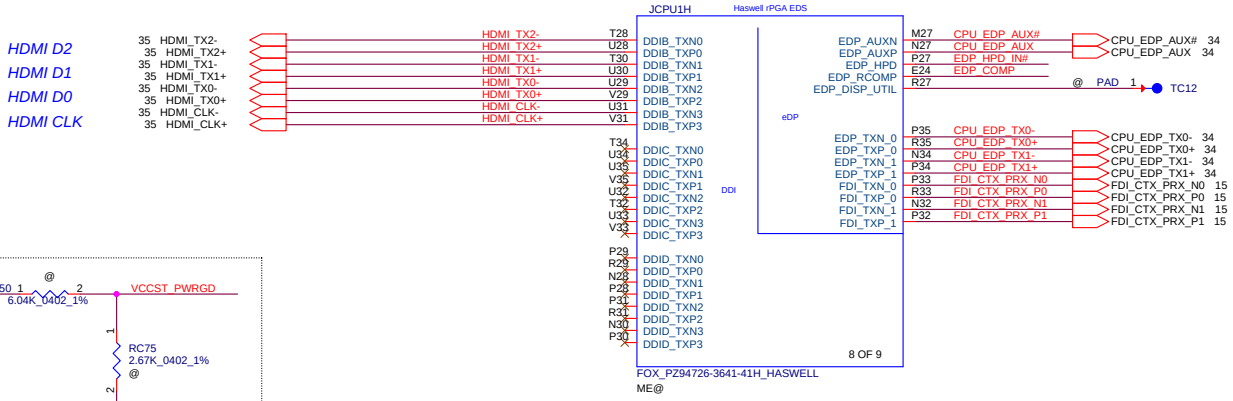


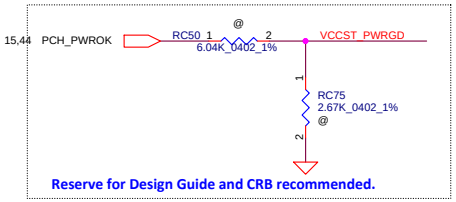
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

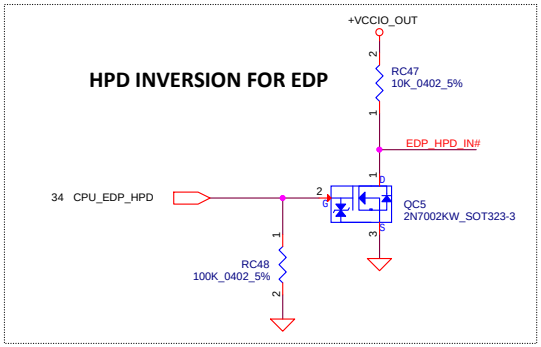
Title: **CPU (3/7) DDRIII**

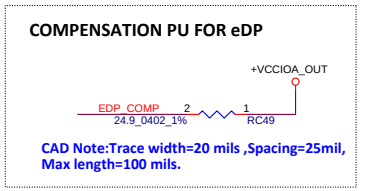
Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 7 of 61

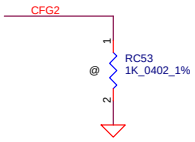




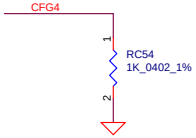




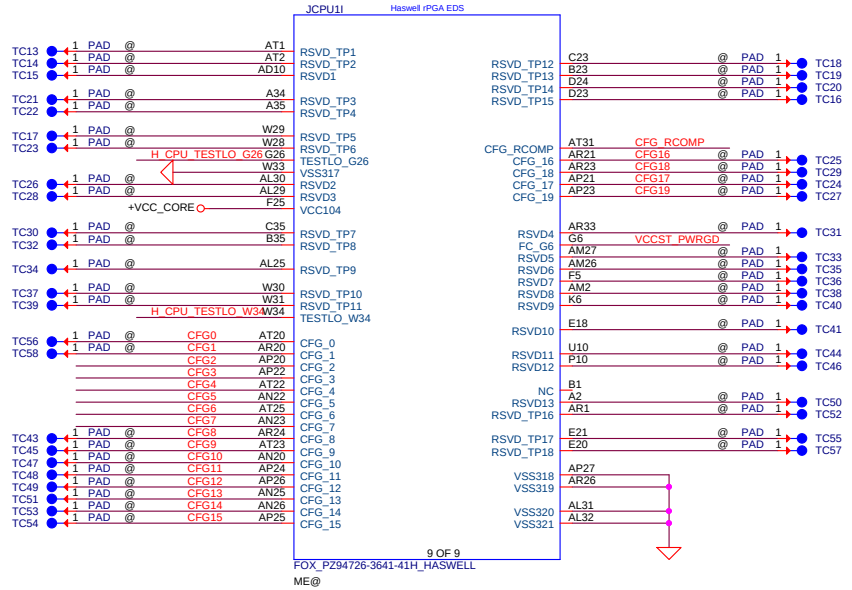
CFG STRAPS for CPU

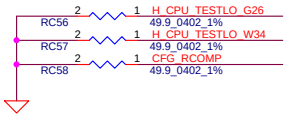


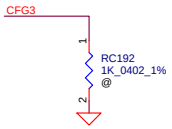
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



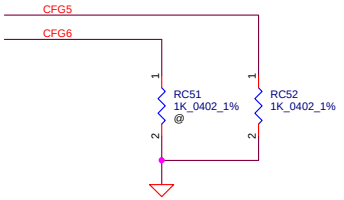
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



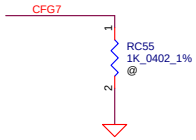




PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG3	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR * 1 : DISABLED



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Need confirm with Intel if this reserved circuit can be deleted.

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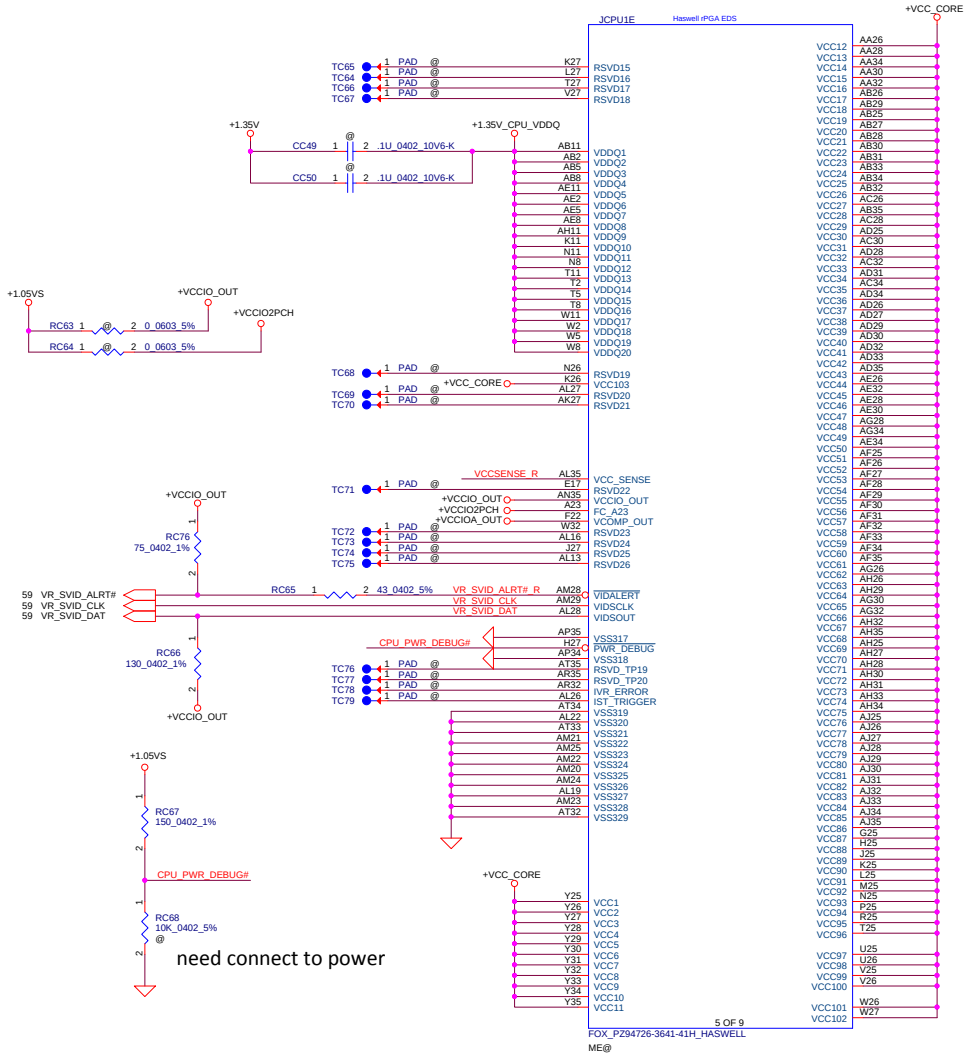
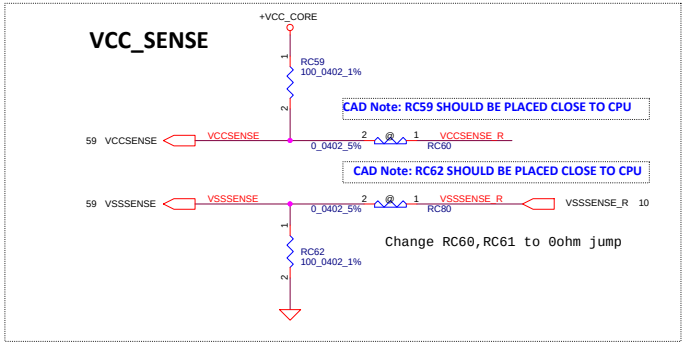
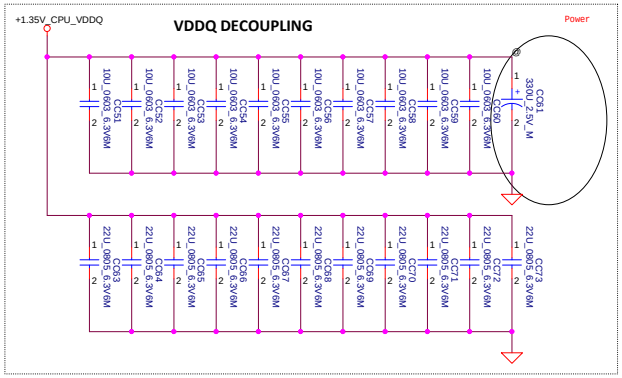
Title: CPU (4/7) RSVD,CFG

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 8 of 61







Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

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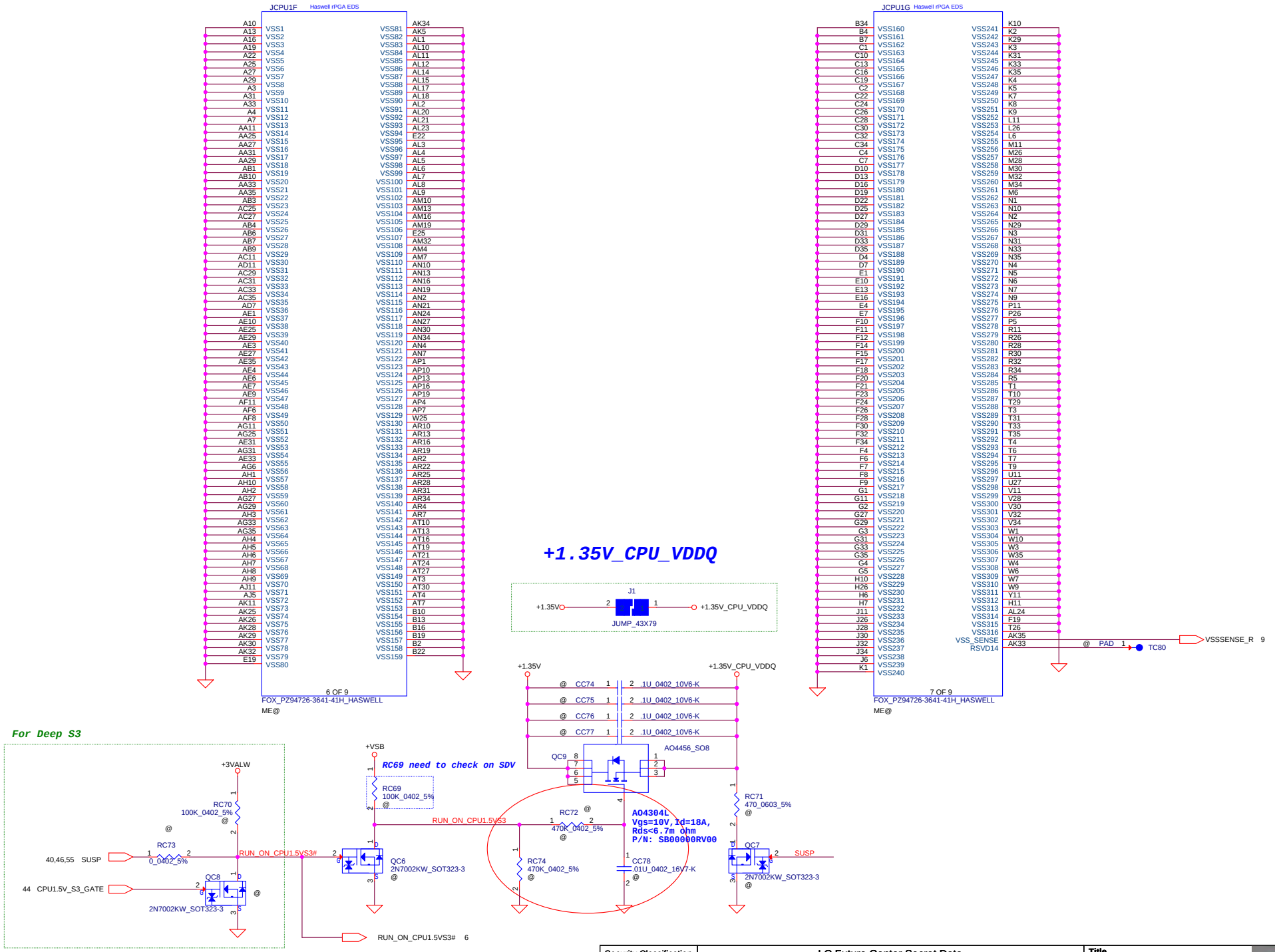
Title: **CPU (5/7) PWR, BYPASS**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 9 of 61



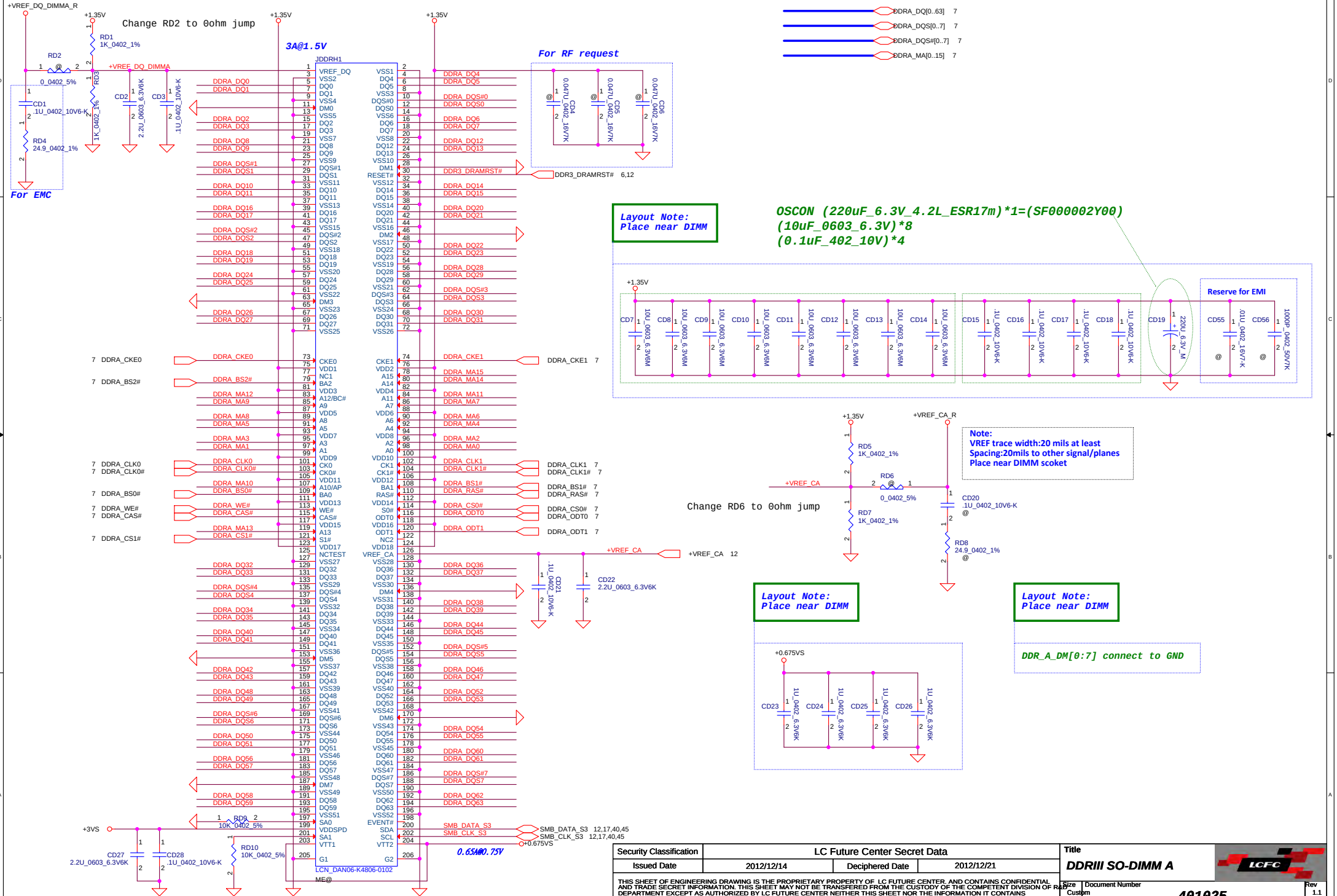
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **CPU (6/7) PWR**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 10 of 61

DDR3 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **DDRIII SO-DIMM A**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 11 of 61

DDR3 SO-DIMM B

Change RD12 to 0ohm jump

3A@1.5V

For RF request

For EMC

Layout Note: Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Change RD15 to 0ohm jump

Layout Note: Place near DIMM

Layout Note: Place near DIMM

DDR_B_DM[0:7] connect to GND

0.675A@0.75V

JDDRL1

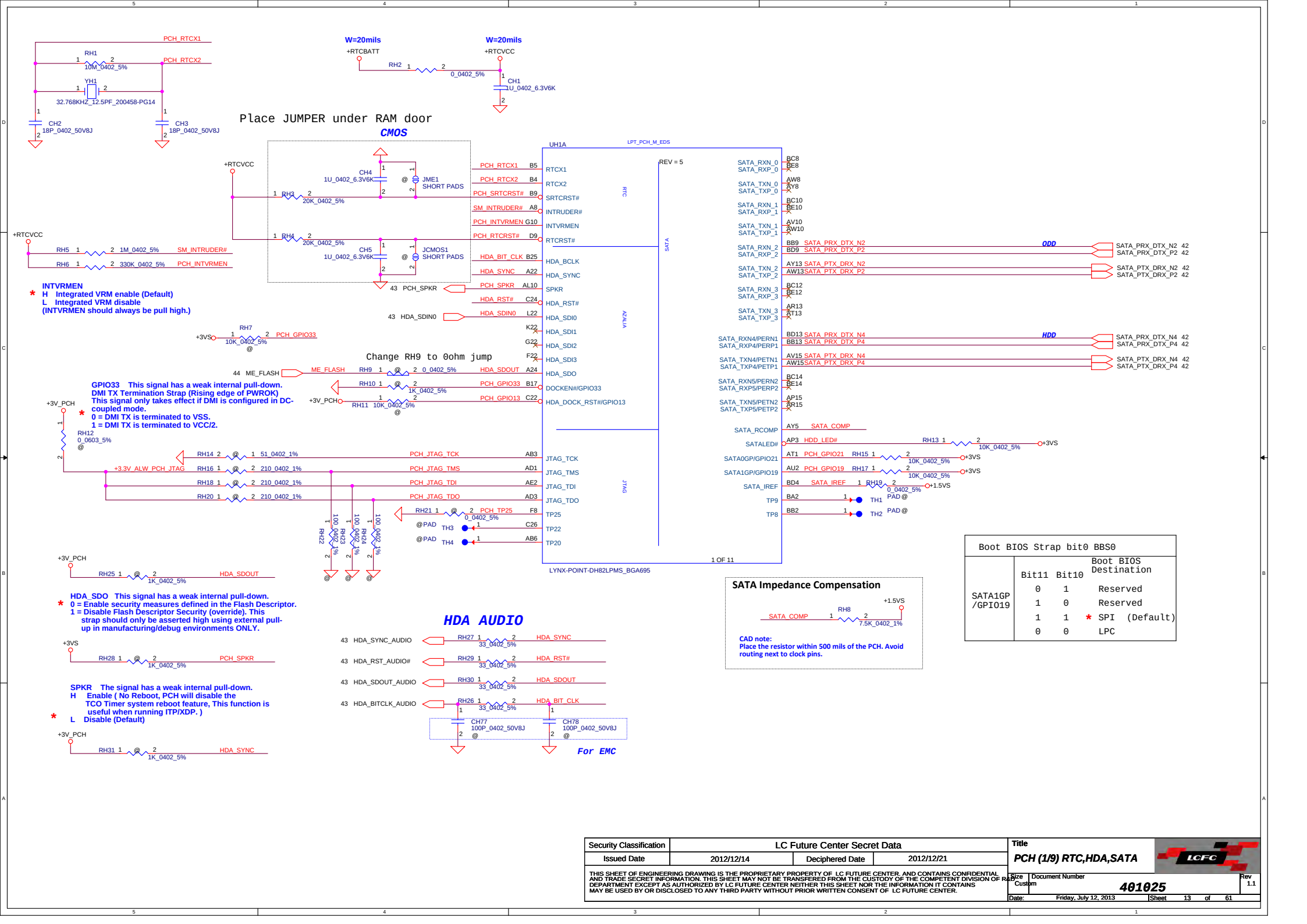
LCN_DAN06-K4406-0102
ME@

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: DDRIII SO-DIMM B

Size: Custom | Document Number: 401025 | Rev: 1.1

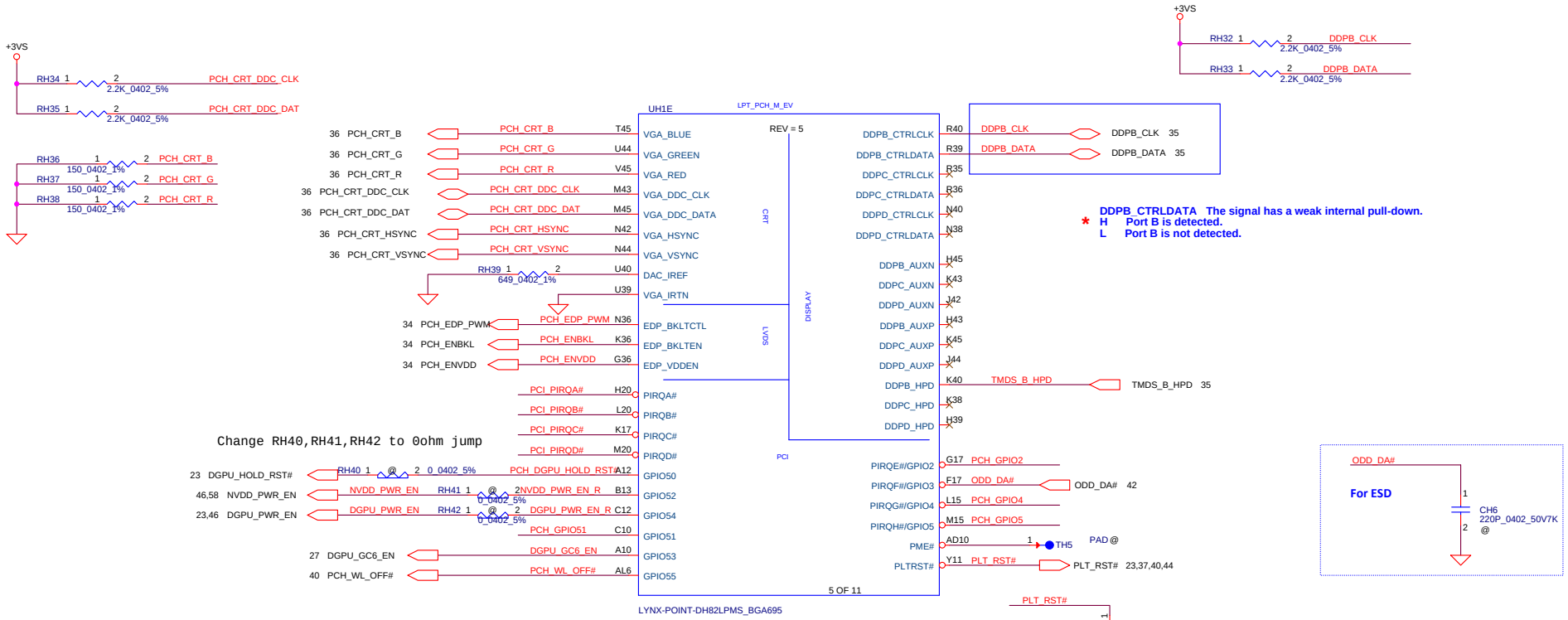
Date: Friday, July 12, 2013 | Sheet 12 of 61



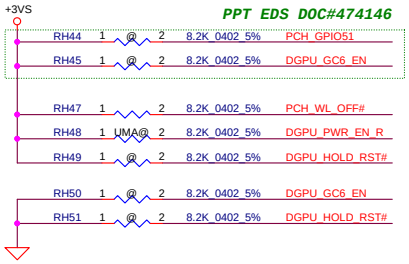
Title: PCH (1/9) RTC,HDA,SATA

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 13 of 61



PPT EDS DOC#474146



GPIO53 The signal has a weak internal pull-up.
* H DMI is in DC-coupling mode (desktop, mobile or server/workstation).
L DMI is in AC-coupling mode (server/workstation only, not meant for desktop/mobile).

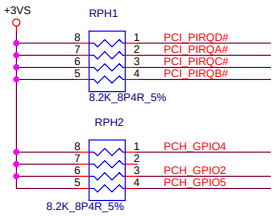
RH52 1 @ 2 1K_0402_5% PCH_WL_OFF#

GPIO55 The signal has a weak internal pull-up.
* H Disable ' Top-Block Swap ' mode.
L Enable ' Top-Block Swap ' mode.

PCH_GPIO51 RH46 1 @ 2 1K_0402_5%

Boot BIOS Strap

BBS_BIT1 (GPIO51)	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

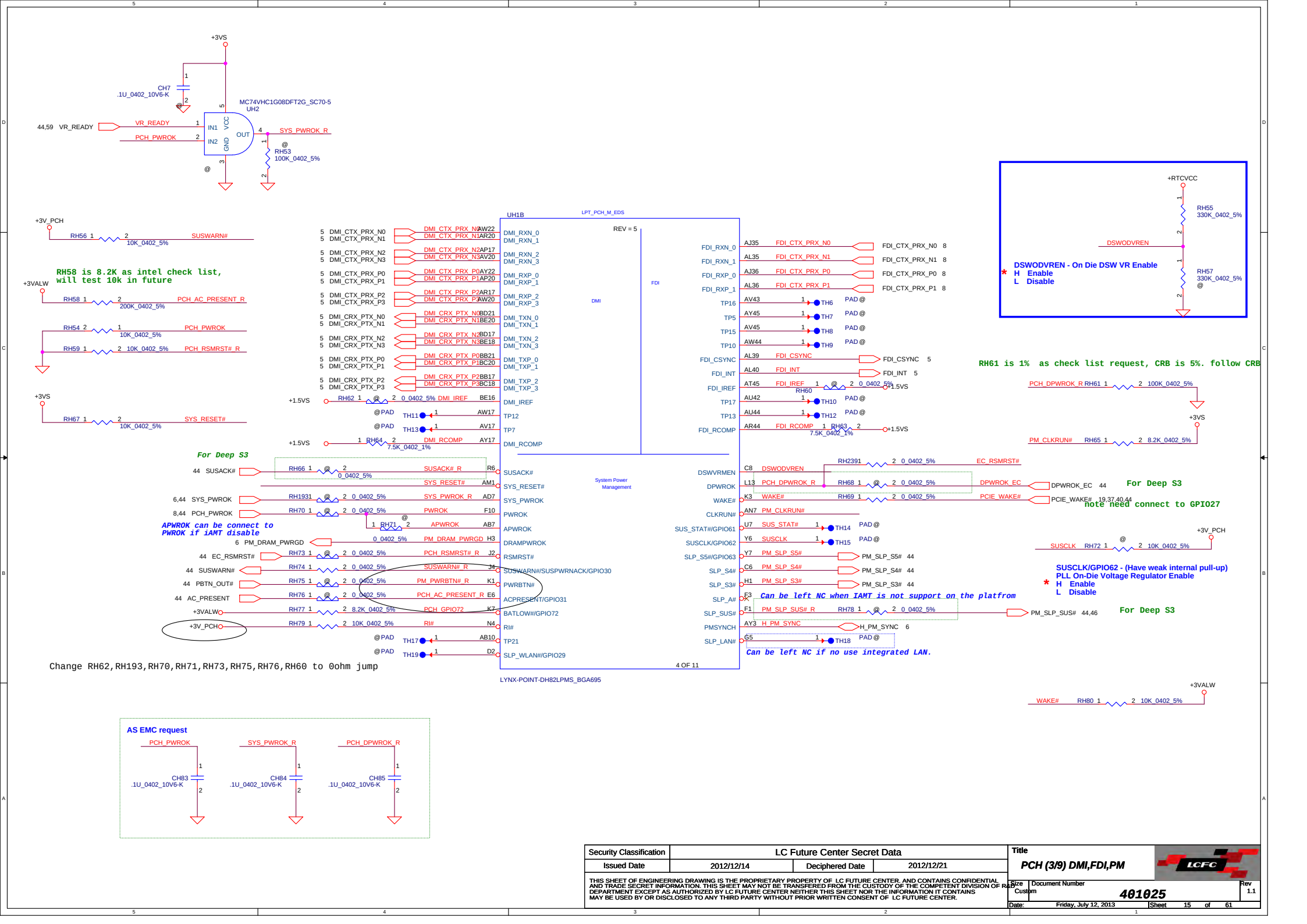


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: PCH (2/9) CRT,DP,PCI

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 14 of 61

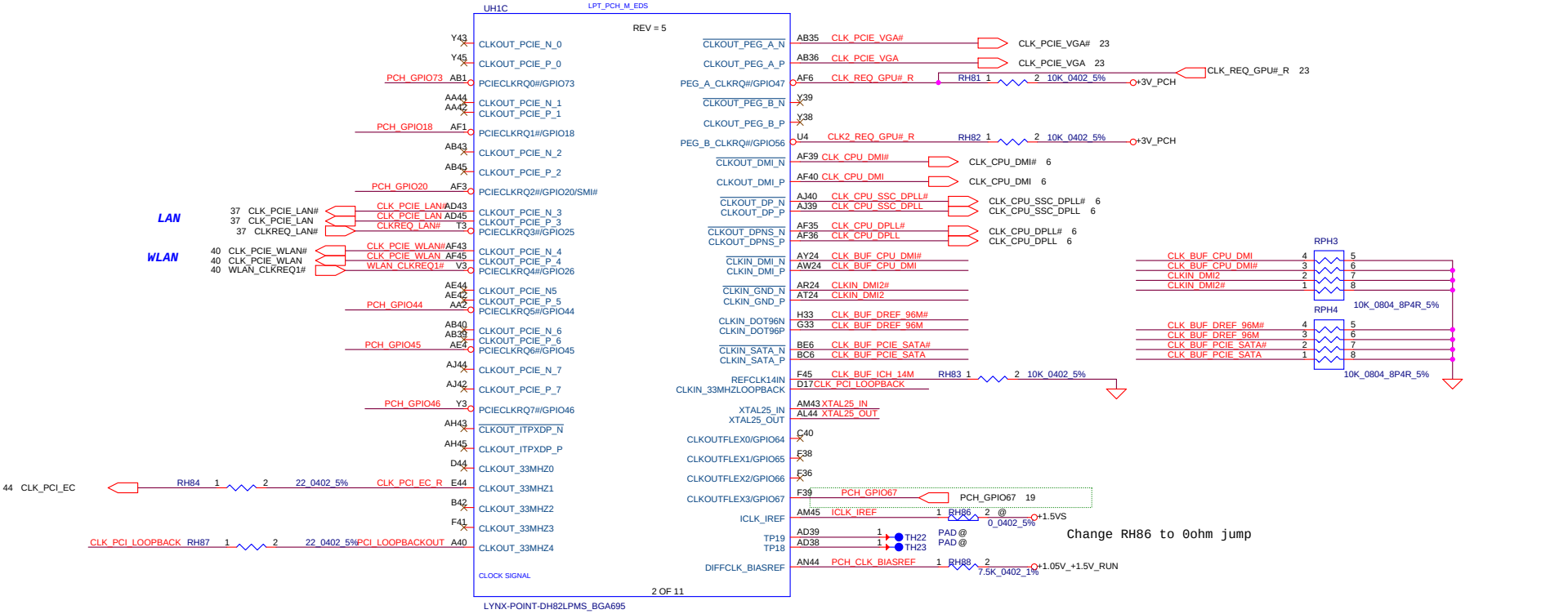


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: PCH (3/9) DMI,FDI,PM

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 15 of 61

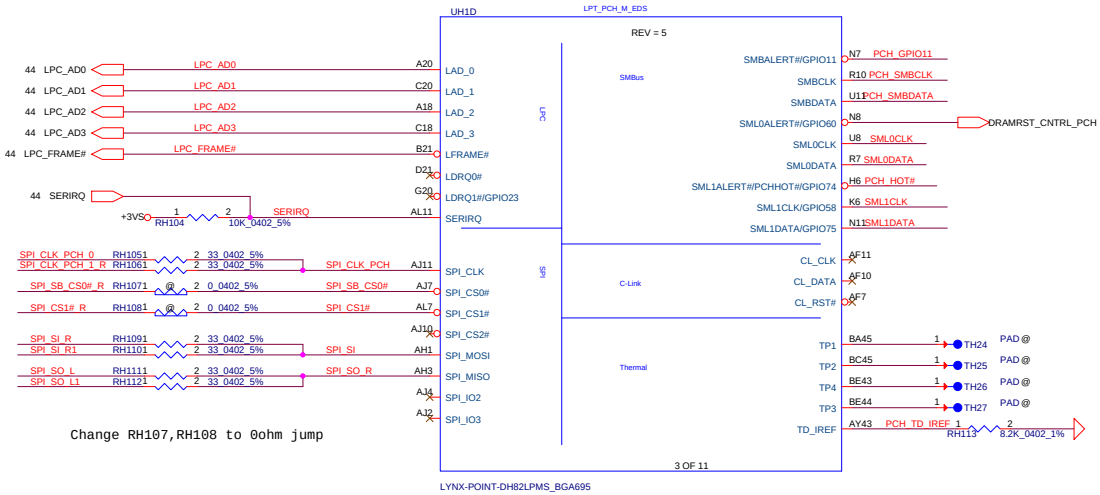


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

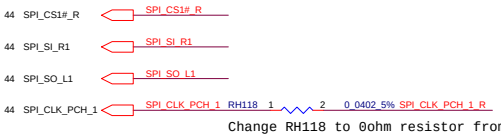
Title: PCH (3/9) CLOCK

Size	Document Number	Rev
Custom	401025	1.1

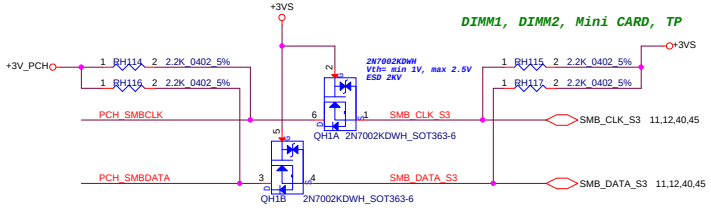
Date: Friday, July 12, 2013 Sheet 16 of 61

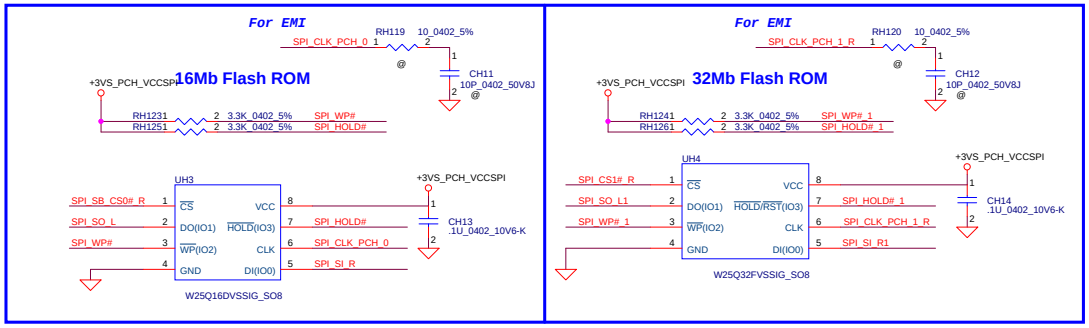


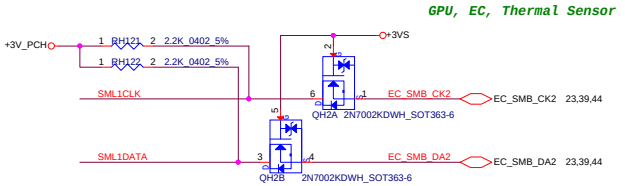
Change RH107,RH108 to 0ohm jump

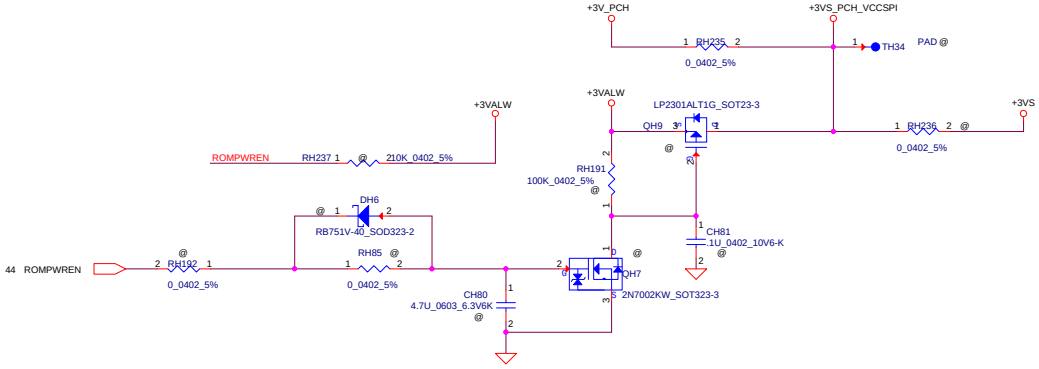


Change RH118 to 0ohm resistor from 0ohm jump







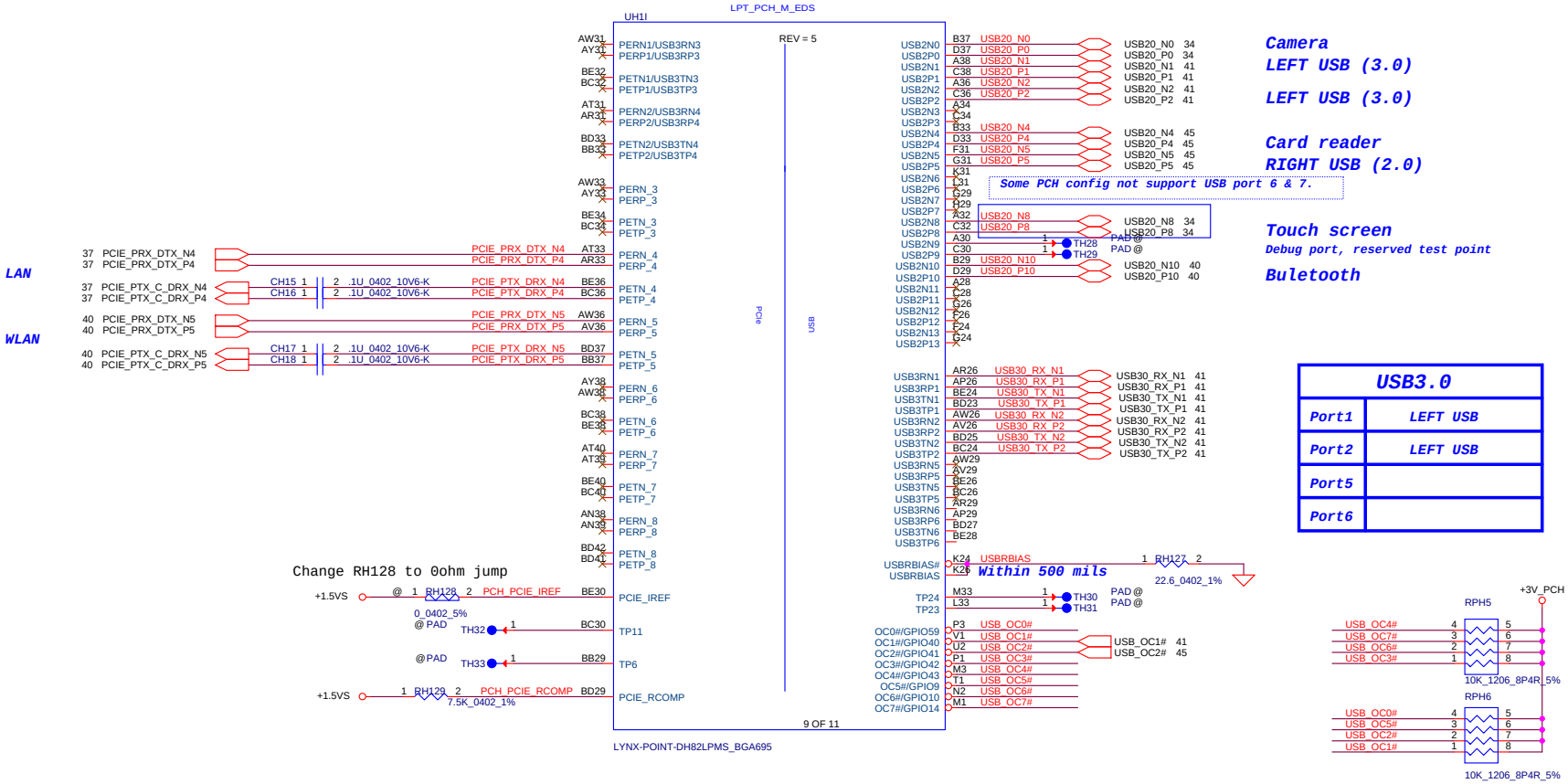


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: PCH (5/9) LPC,SPI,SMBUS

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 17 of 61

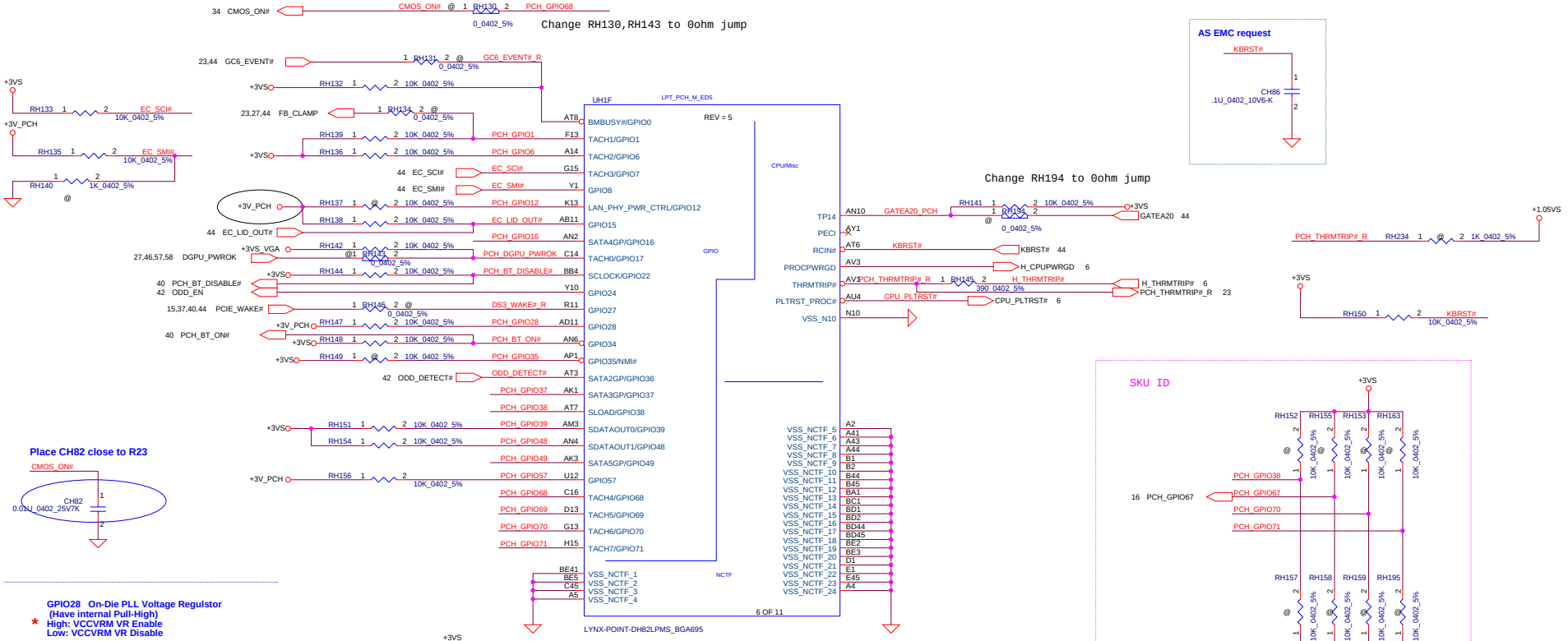


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: PCH (5/9) PCI, USB

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 18 of 61



Config	GPIO16,49
SATA4,SATA5	11
PCIE1,PECI2	00

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (1b)	SATA 5 (1b)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (0b)	PCIE 2 (0b)				

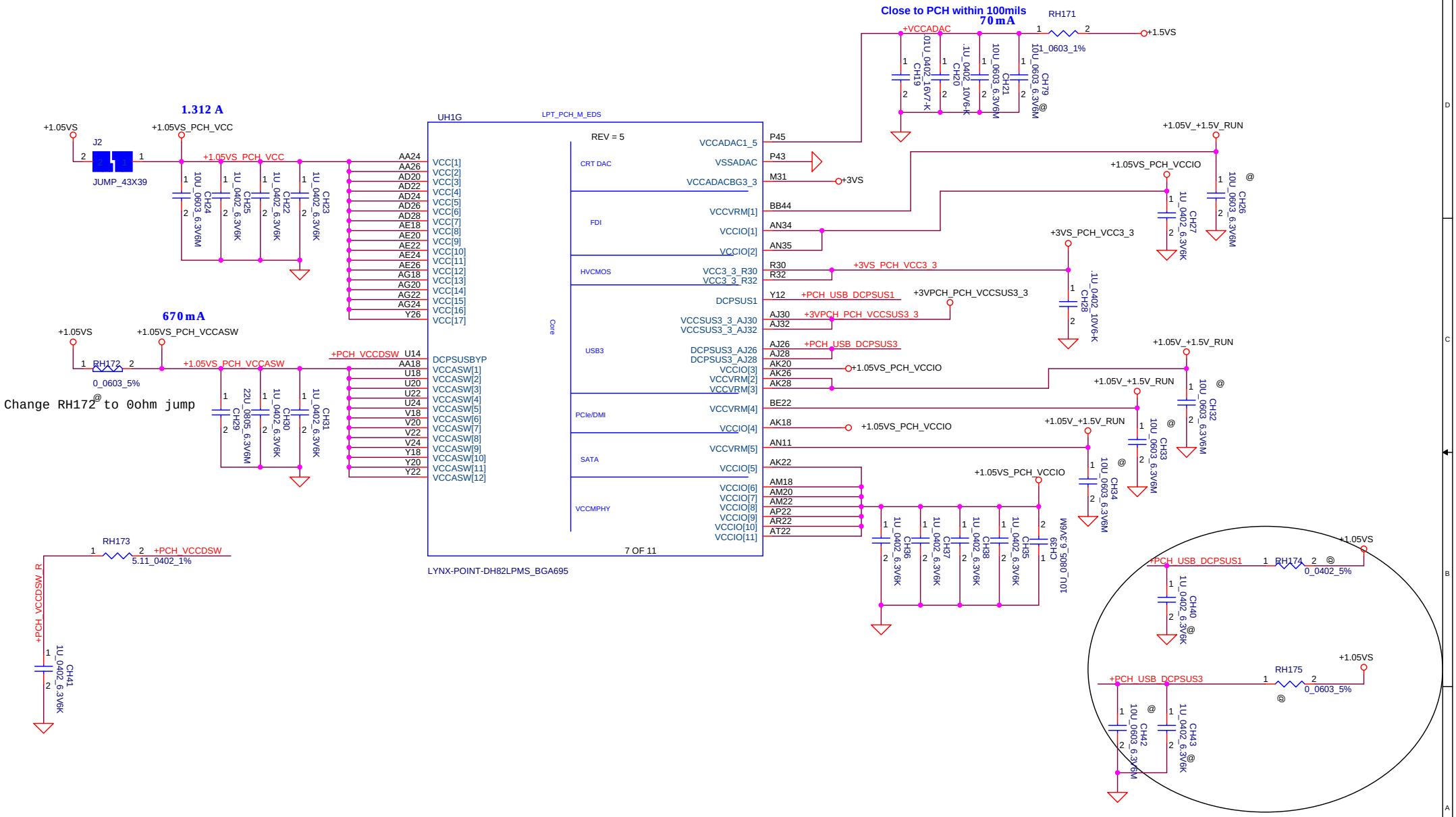
Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70	PCH_GPIO71
UMA 14"	0	0	0	0
UMA 15"	0	1	0	0
14" VRAM 900MHz	1	0	0	0
14" VRAM 1GHz	1	0	1	0
15" VRAM 900MHz	1	1	0	0
15" VRAM 1GHz	1	1	1	0
UMA 15" Touch	0	1	0	1
15" VRAM 900MHz Touch	1	1	0	1
15" VRAM 1GHz Touch	1	1	1	1

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
C	401025	1.1

Date: Friday, July 12, 2013 | Sheet 19 of 61

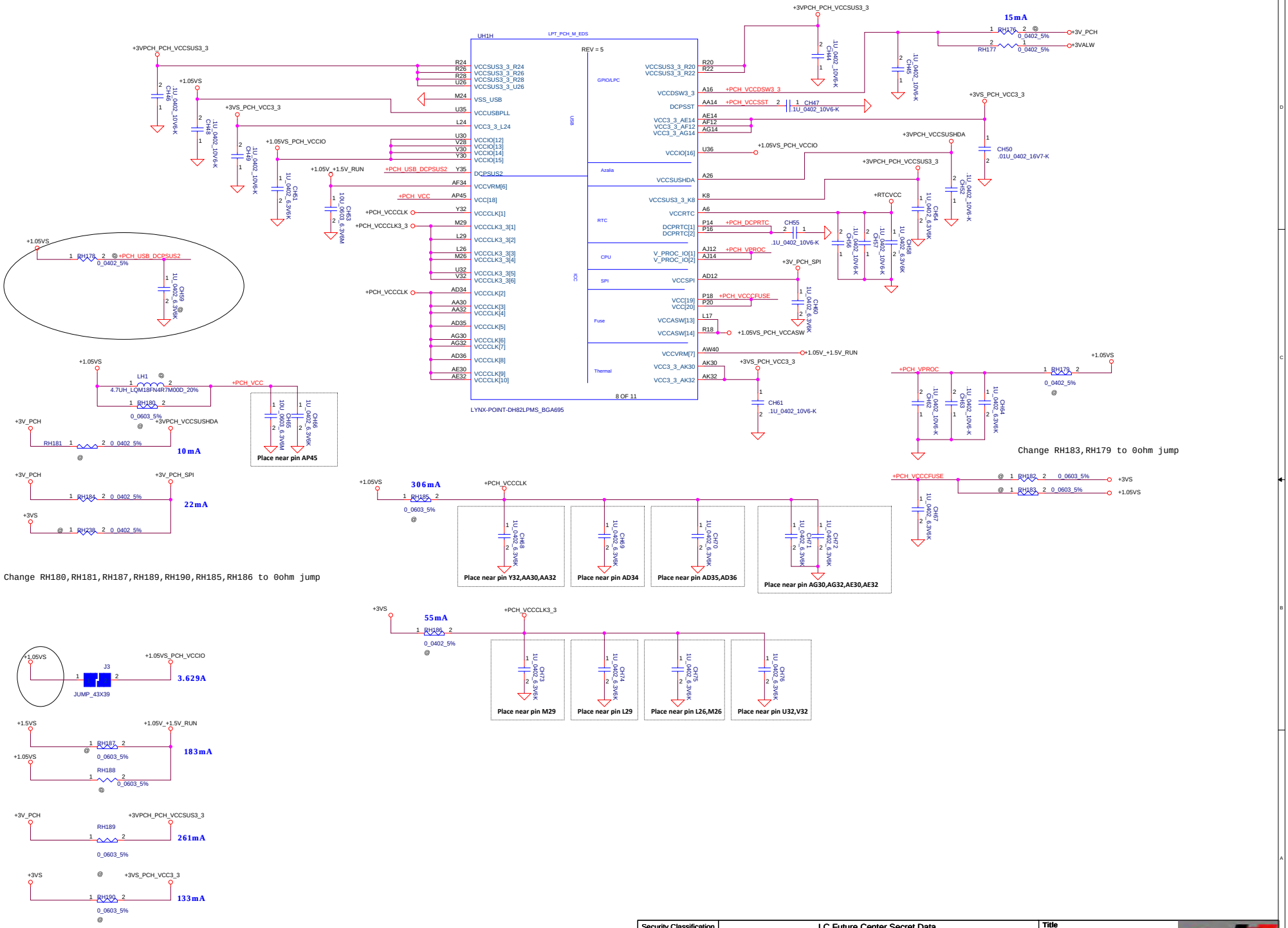


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **PCH (7/9) PWR**

Size	Document Number	Rev
B	401025	1.1

Date: Friday, July 12, 2013 Sheet 20 of 61

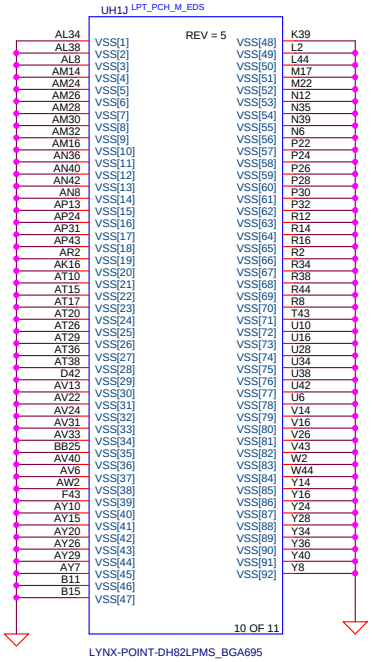


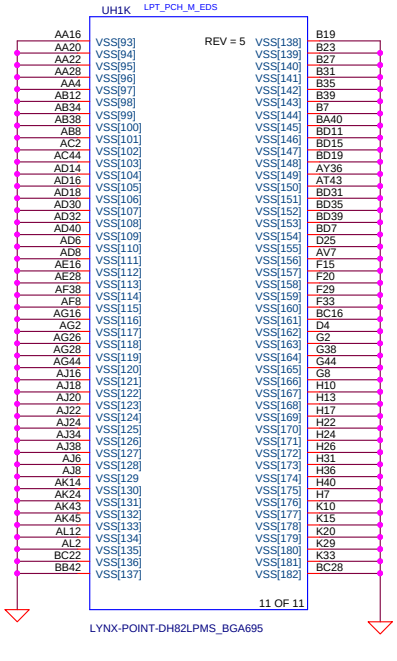
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: PCH (8/9) PWR

Size	Document Number	Rev
C	401025	1.1

Date: Friday, July 12, 2013 | Sheet 21 of 61



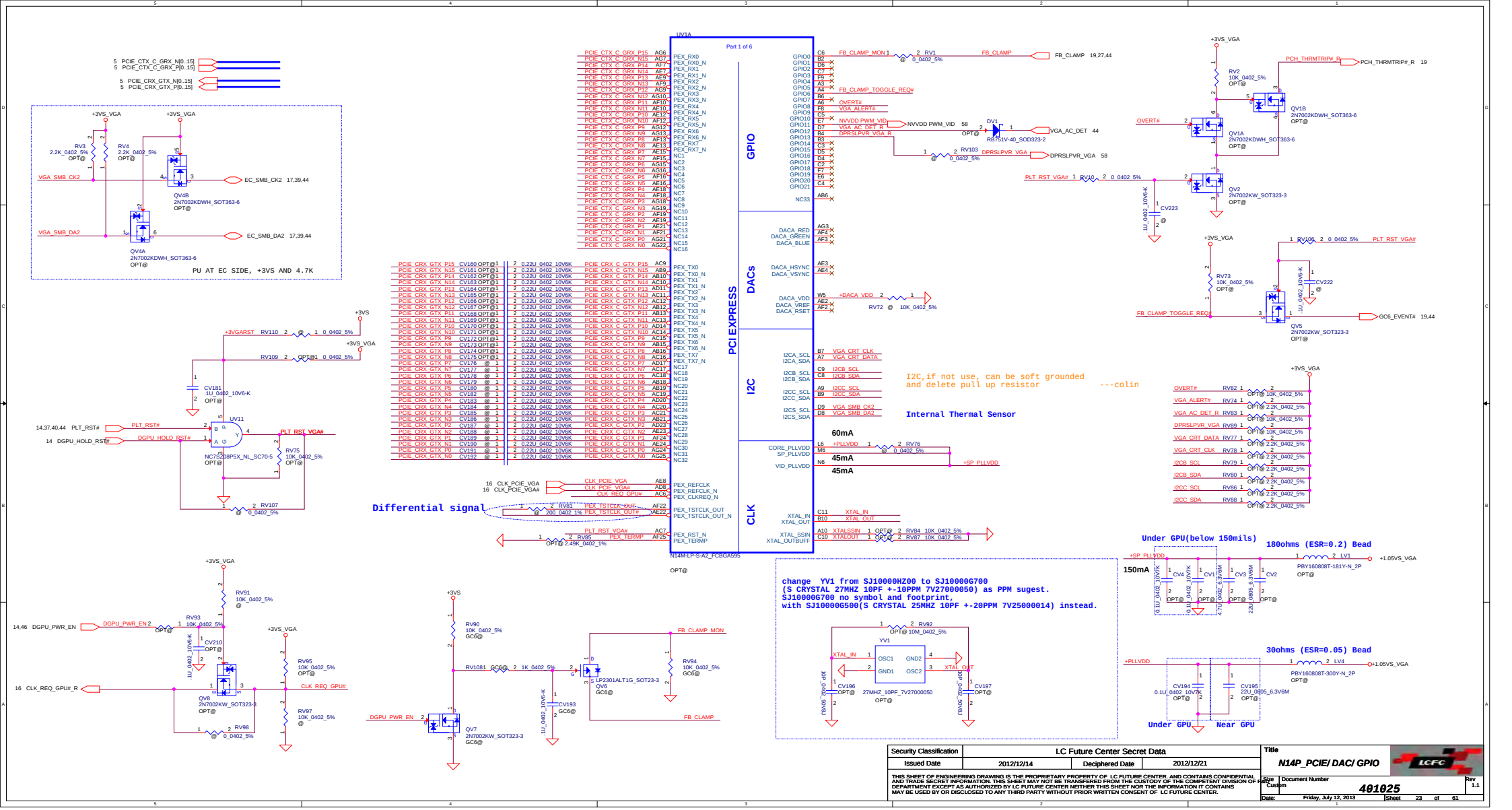


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 22 of 61



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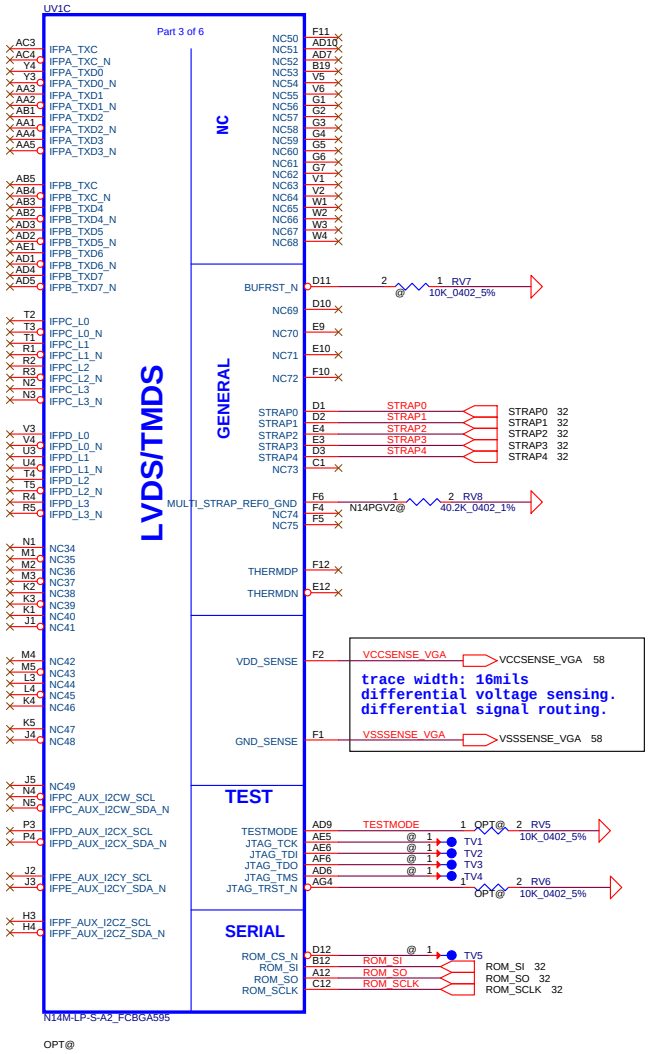
Title: N14P_PCIE/ DAC/ GPIO

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 23 of 61

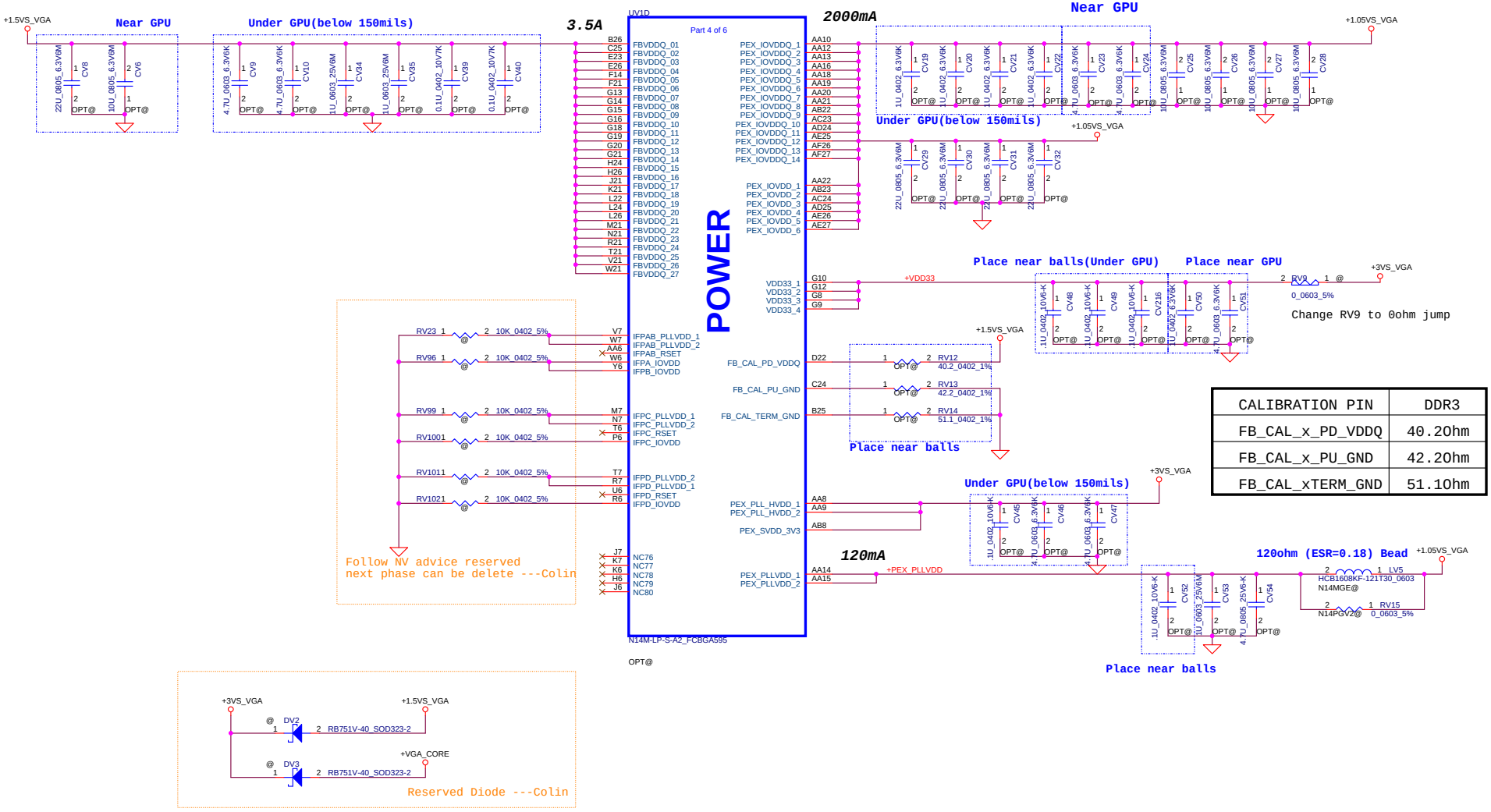


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: *N14P_LVDS/ HDMI/ THERM*

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 24 of 61



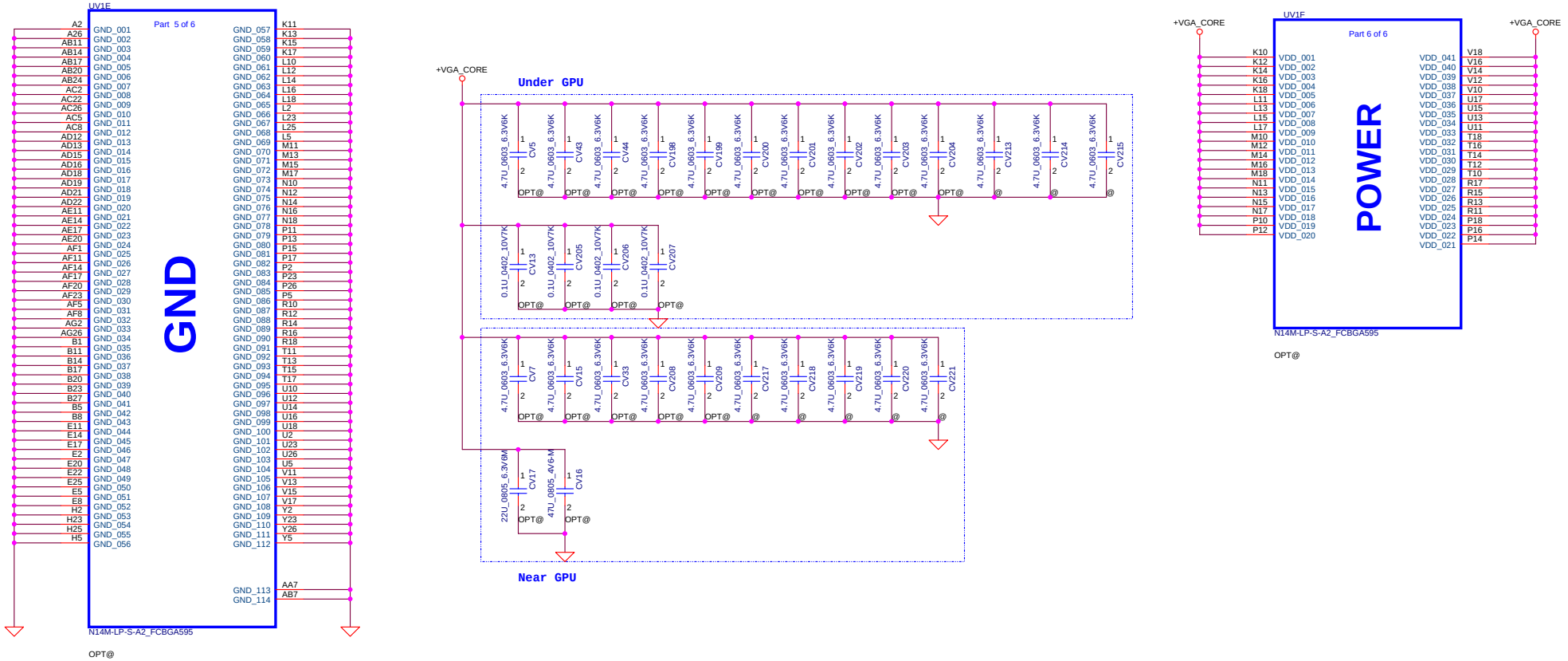
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	42.20hm
FB_CAL_xTERM_GND	51.10hm

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: *N14P_Power*

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 25 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

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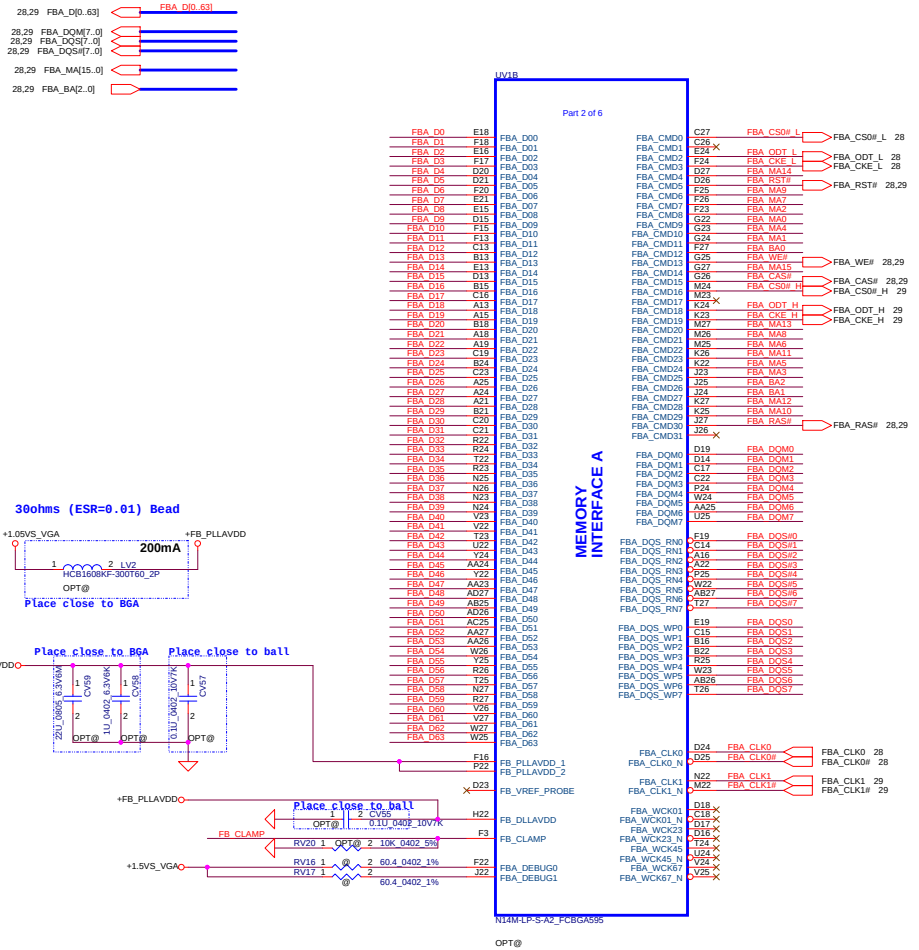
Title: *N14P_+VGA CORE, GND*

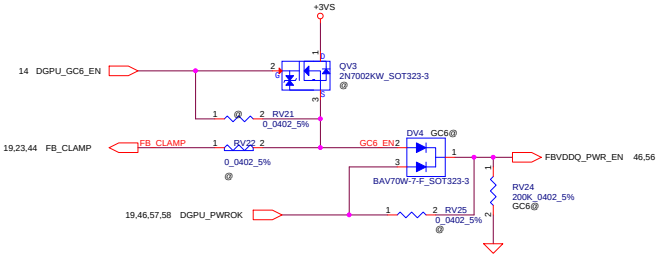
Size	Document Number	Rev
Custom	*401025*	1.1

Date: Friday, July 12, 2013 Sheet 26 of 61

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

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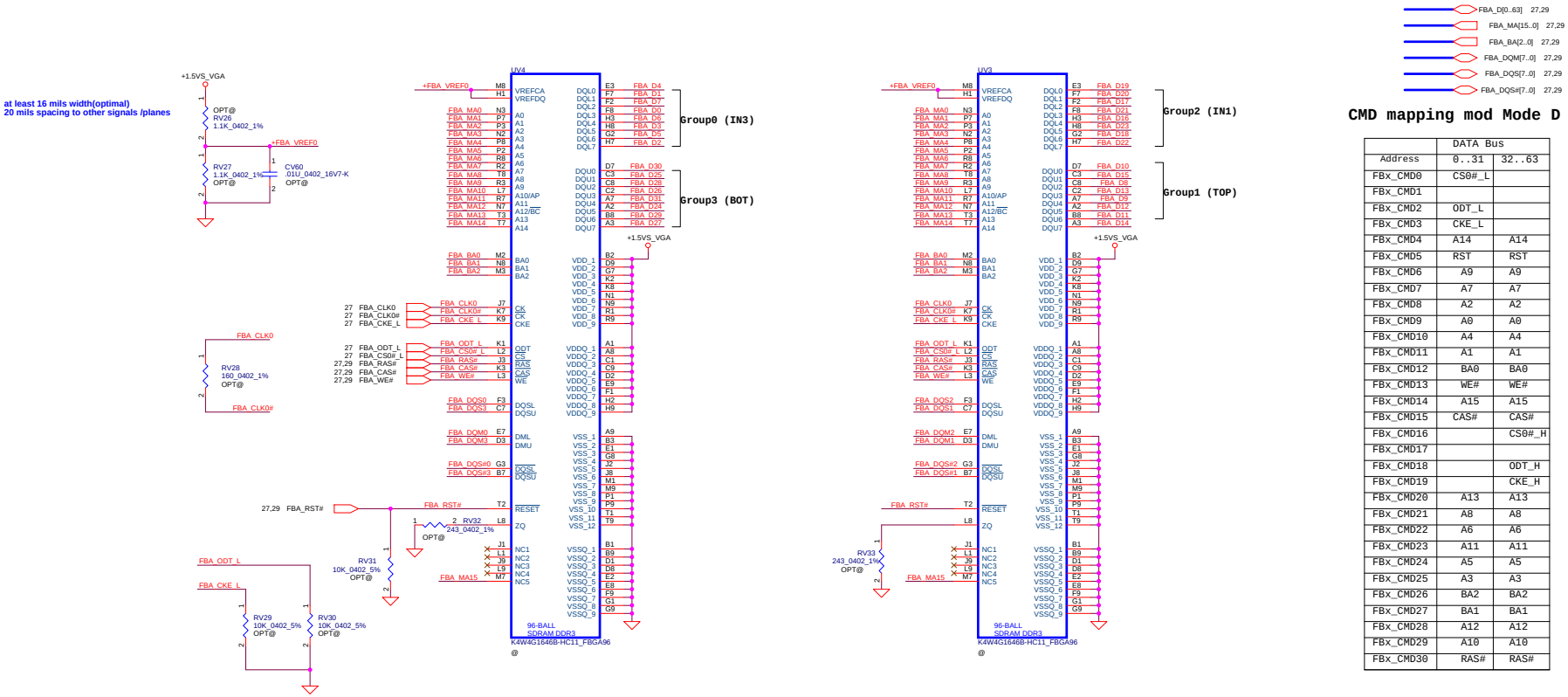
Title: N14P_MEM Interface

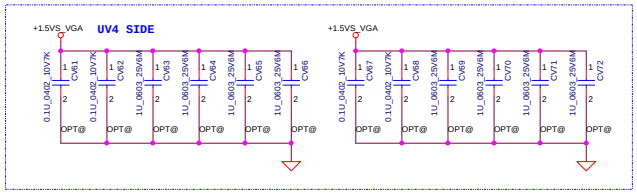
Size: Custom | Document Number: 401025 | Rev: 1.1

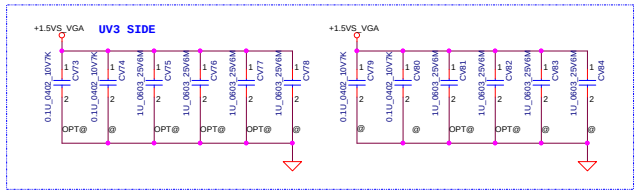
Date: Friday, July 12, 2013 | Sheet 27 of 61



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





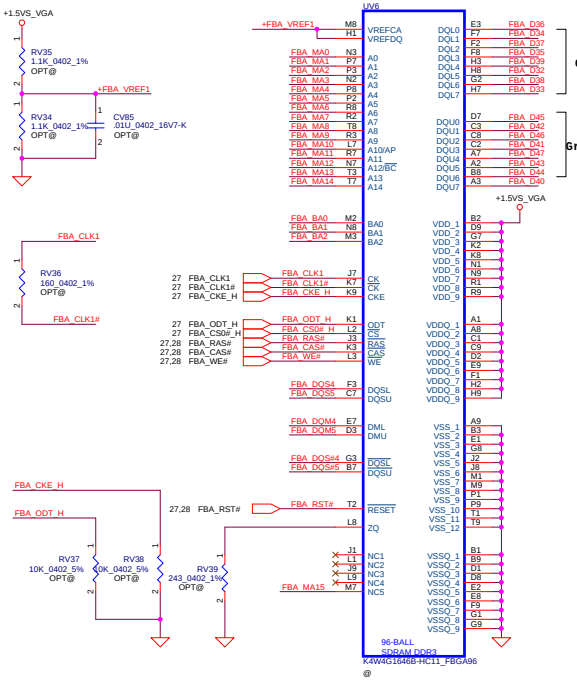
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

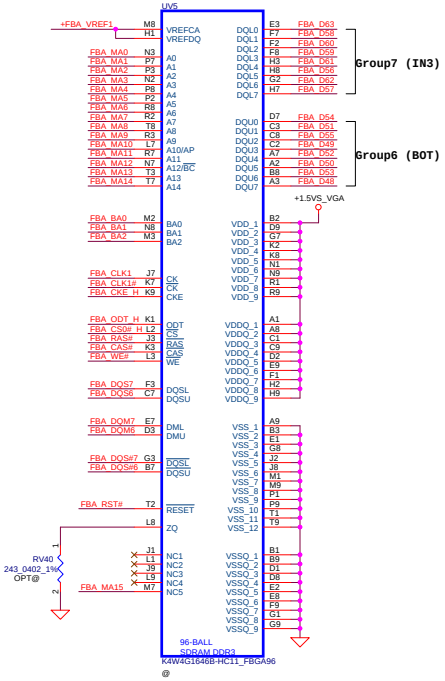
Title: *N14P_DDR3_A Lower*

Size: Custom | Document Number: *401025* | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 28 of 61

at least 16 mils width(optimal)
20 mils spacing to other signals /planes

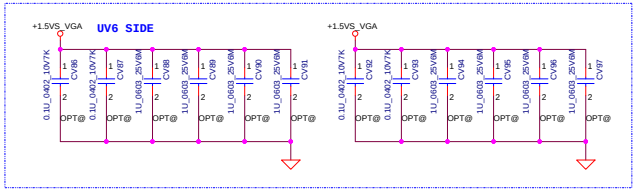


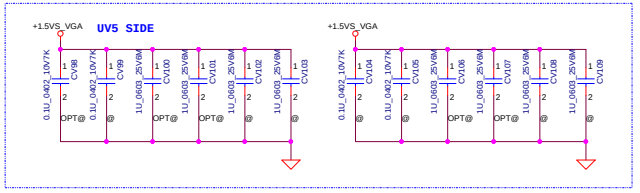


FBA_D[0..63] 27,28
FBA_MA[15..0] 27,28
FBA_BA[2..0] 27,28
FBA_DQM[7..0] 27,28
FBA_DQS[7..0] 27,28
FBA_DQS#[7..0] 27,28

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: N14P_DDR3_A Upper

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 29 of 61

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: ***Blank4***

Size	Document Number	Rev
Custom	***401025***	1.1

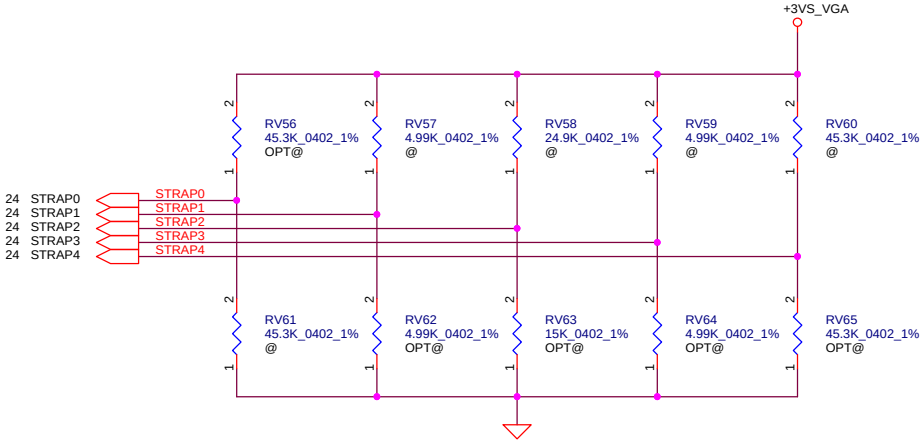
Date: Friday, July 12, 2013 | Sheet 30 of 61

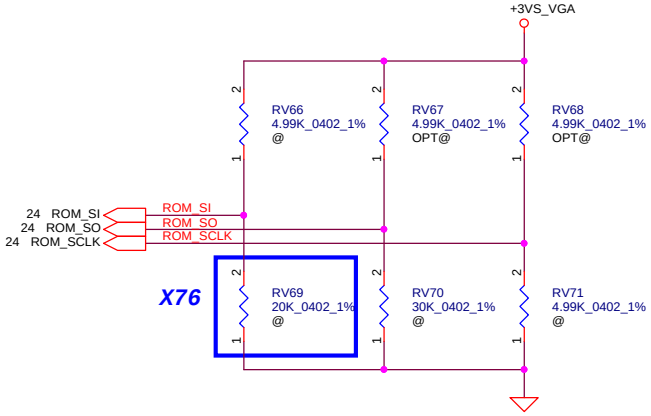
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: ***Blank5***

Size	Document Number	Rev
Custom	***401025***	1.1

Date: Friday, July 12, 2013 | Sheet 31 of 61





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PCIE_MAX_SPEED	
0	Limit booting to PCIE Gen1
1	Allow booting to PCIE Gen 2/3

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIE Gen3 operation
1	Enable PCIE Gen3 operation

USER Straps	
User[3:0]	
1000-1100	Customer defined

DP_PLL_VDD33V	
0	Reserved
1	Default

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

X76

GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV2	Samsung 1GHz	K4W2G1646E-BC1A 128M x 16	0x7 PD 45.3K	PU 4.99K	PU 4.99K	PU 45.3K	PD 4.99K	PD 15K	PD 4.99K	PU 45.3K
	Micron 1GMHz	MT41J128M16JT-093G:K 128M x 16	0x5 PD 30.1K							
	Hynix 1GMHz	H5TC2G63FFR-11C 128M x 16	0x4 PD 24.9K							
	Samsung 900MHz	K4W4G1646B-HC11 256M x 16	0x3 PD 20K							
	Micron 900MHz	MT41K256M16HA-107G:E 256M x 16	0x1 PD 10K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: *N14P_MISC*

Size	Document Number	Rev
Custom	*401025*	1.1

Date: Friday, July 12, 2013 Sheet 32 of 61

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

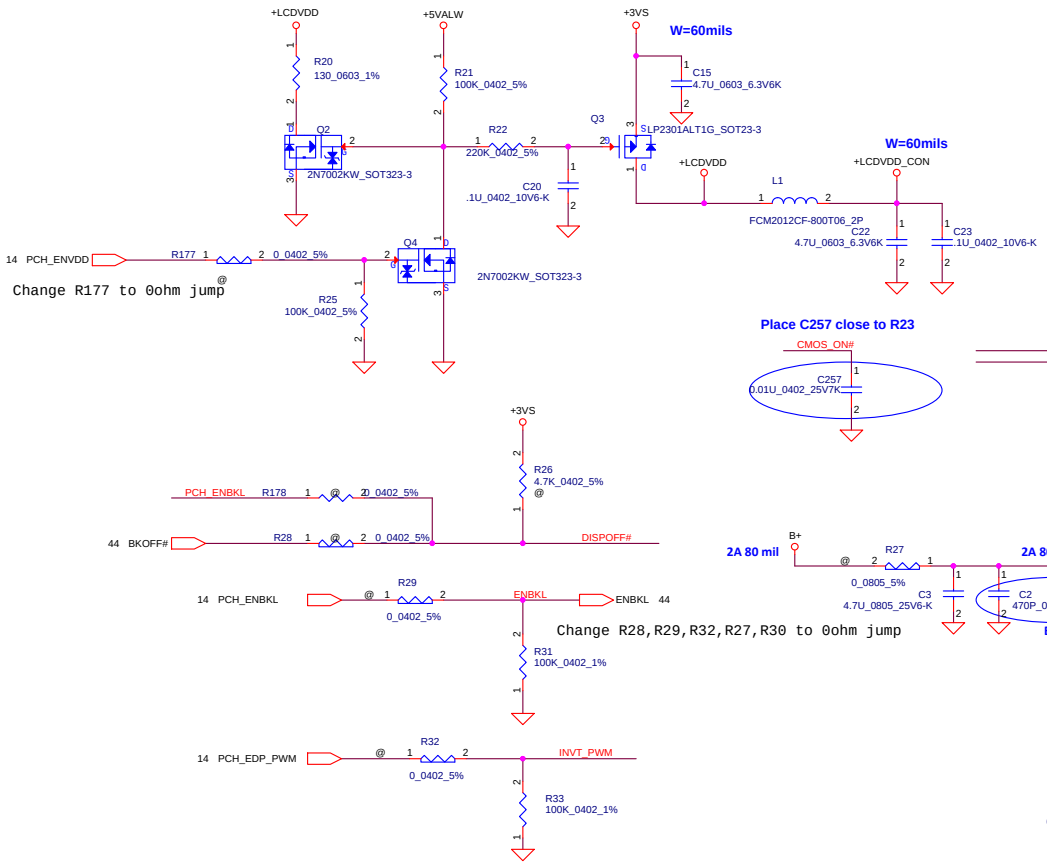
Title

XDP_CONN

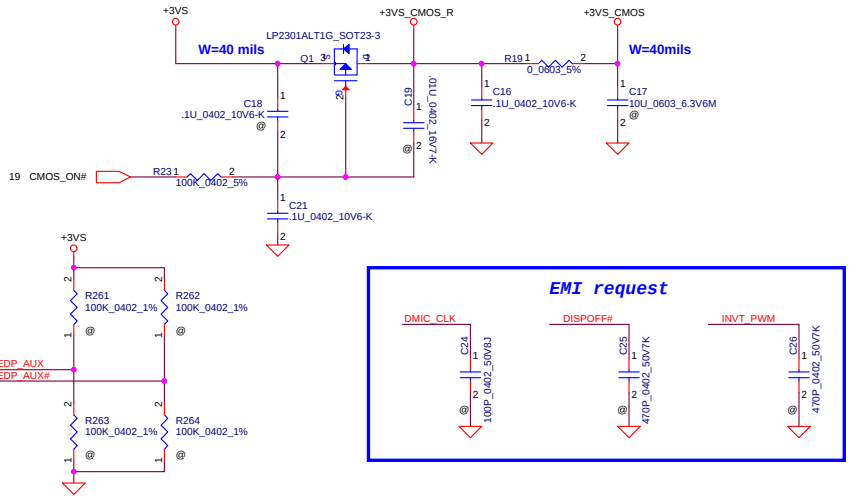
Size	Document Number	Rev
Custom	***401025***	1.1

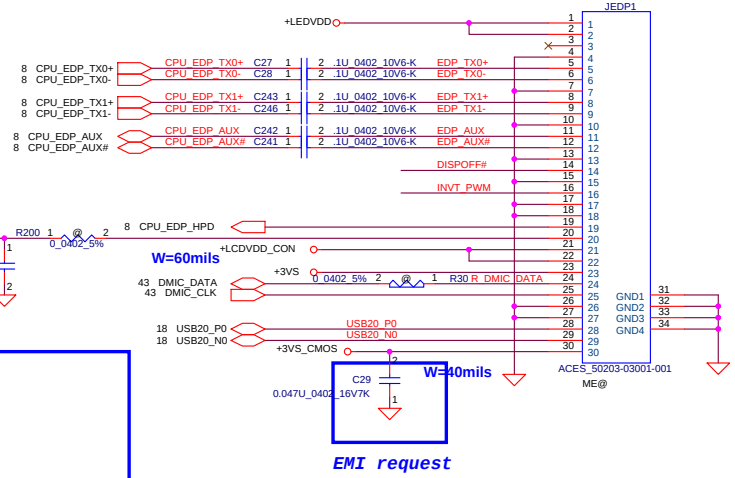
Date: Friday, July 12, 2013 Sheet 33 of 61

LCD POWER CIRCUIT

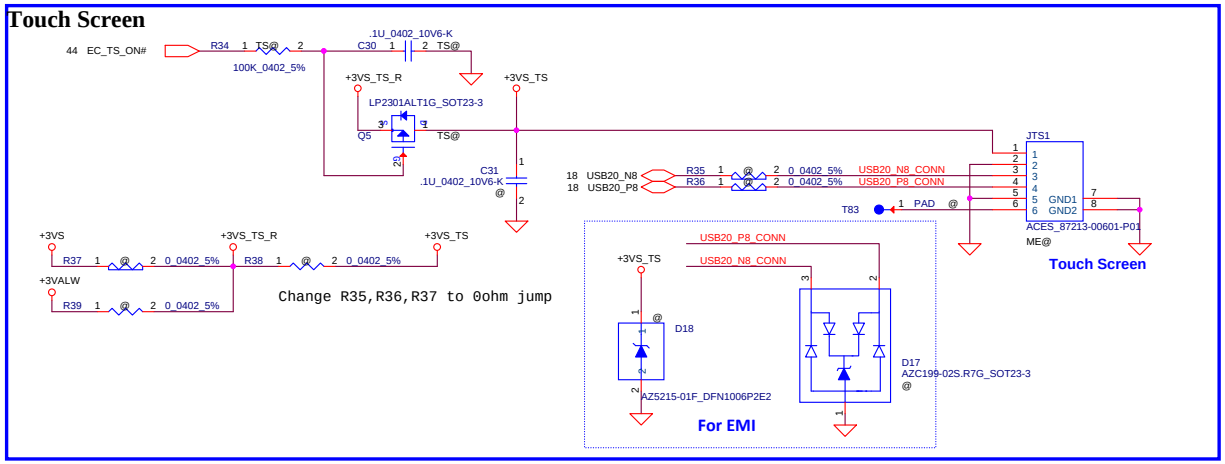


CMOS Camera





Touch Screen

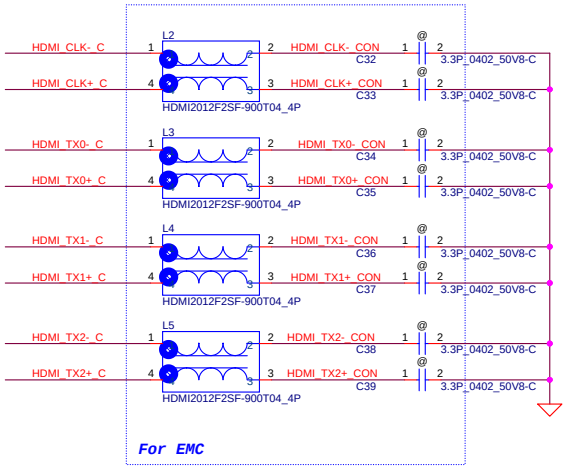


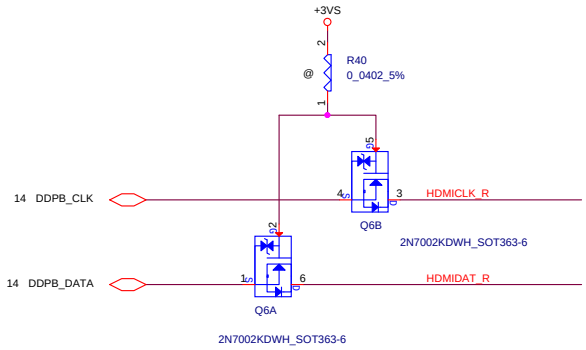
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

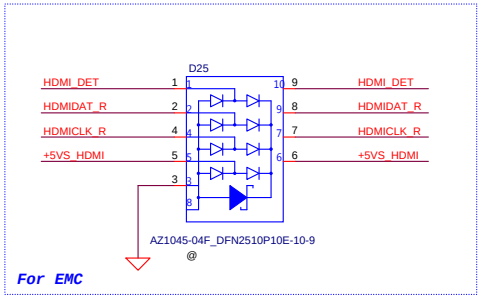
Title: *eDP/ CMOS/Touch screen*

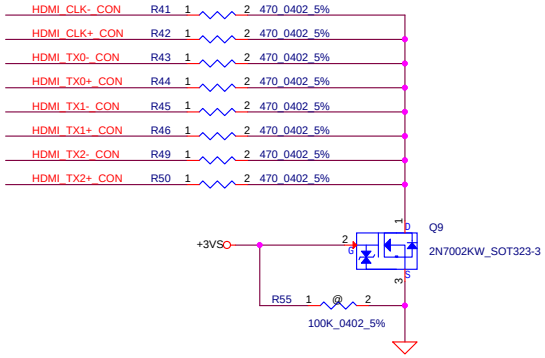
Size: Custom | Document Number: 401025 | Rev: 1.1

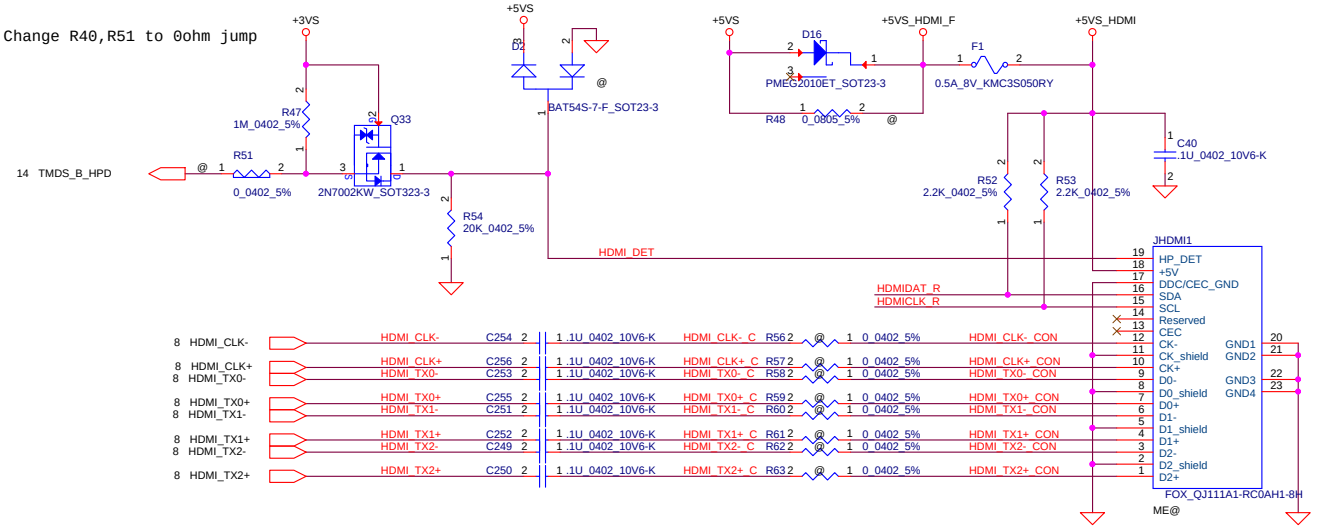
Date: Friday, July 12, 2013 | Sheet 34 of 61

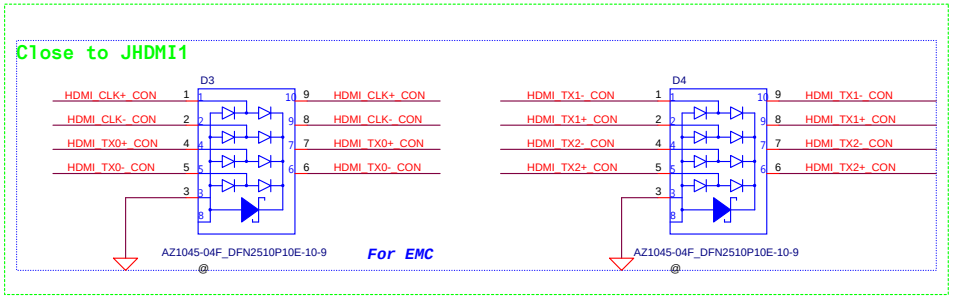












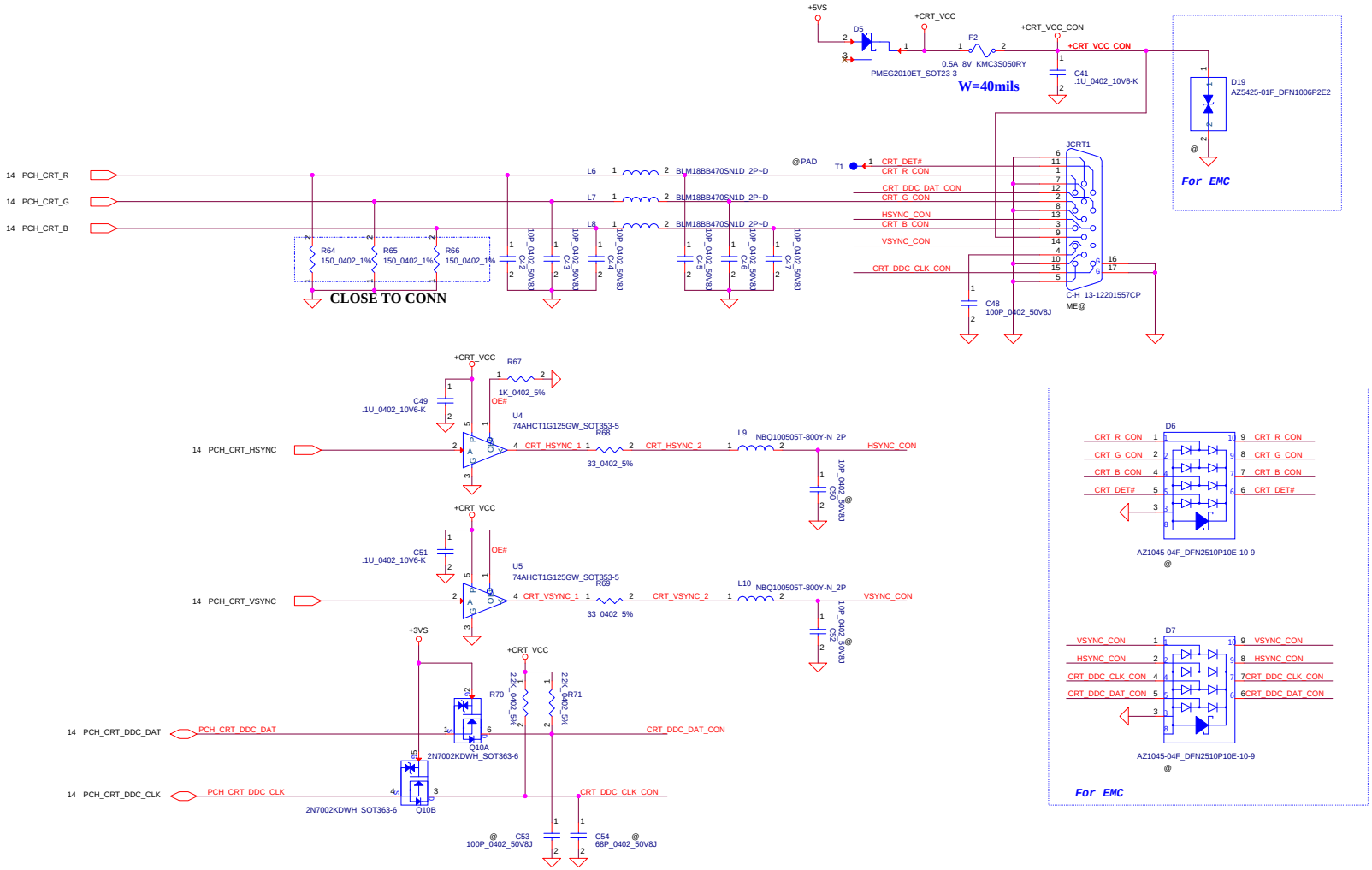
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **HDMI_CONN**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 35 of 61

CRT Connector



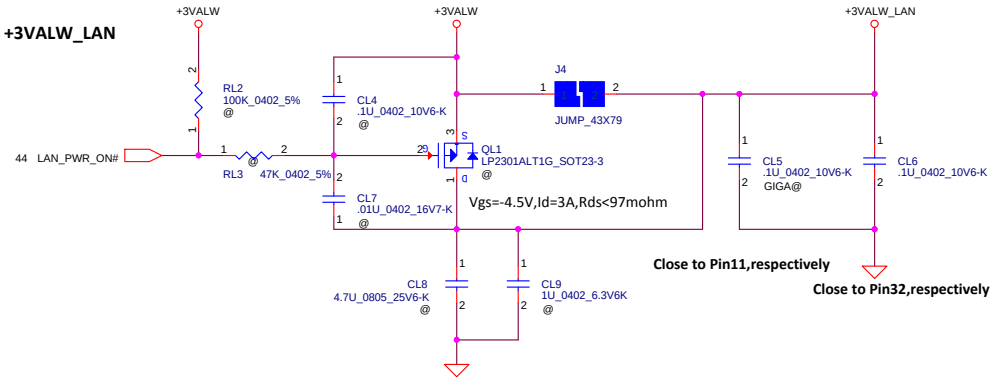
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

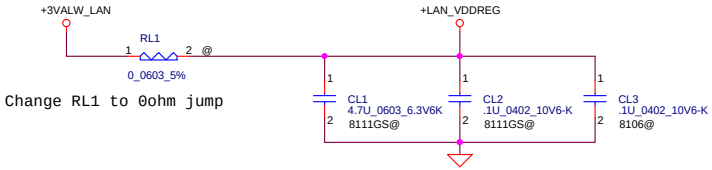
Title	CRT		
Size C	Document Number 401025		Rev 1.1
Date: Friday, July 12, 2013	Sheet 36 of 61		

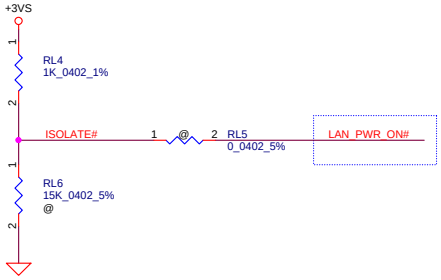
+3VALW_LAN rising time (10%~90%): 0.5ms＜spec＜100ms

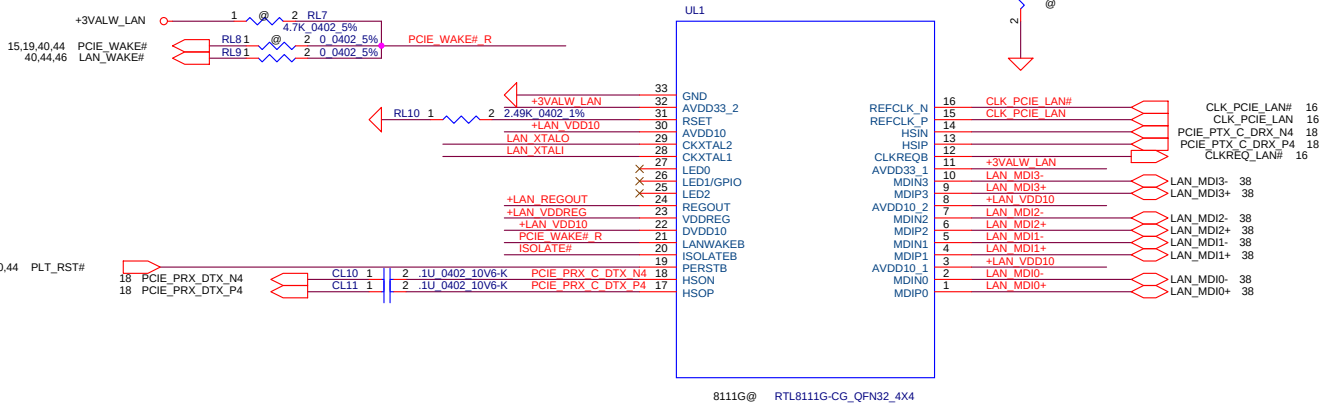
+3VALW_LAN width : 40 mils

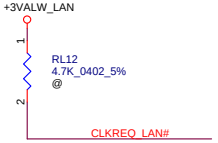
+3VALW TO +3VALW_LAN



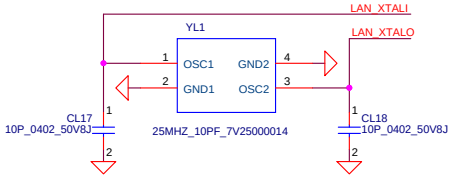


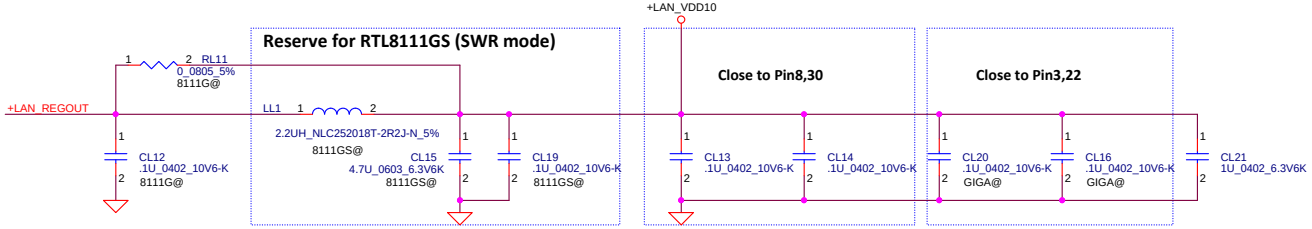






Vendor recommand reseve the PU resistor close LAN chip





Layout Note: LL1 must be within 200mil to Pin36, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

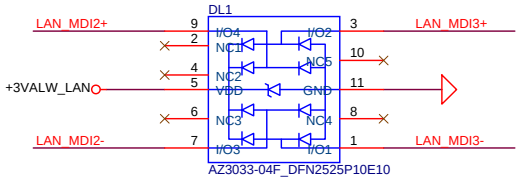
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: LAN_RTL8106E

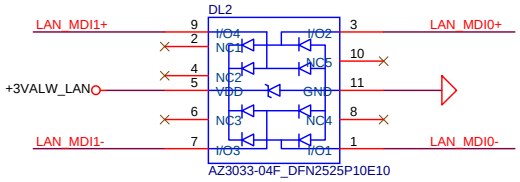
Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 37 of 61

DL1/DL2
1'S PN:SC300003M00

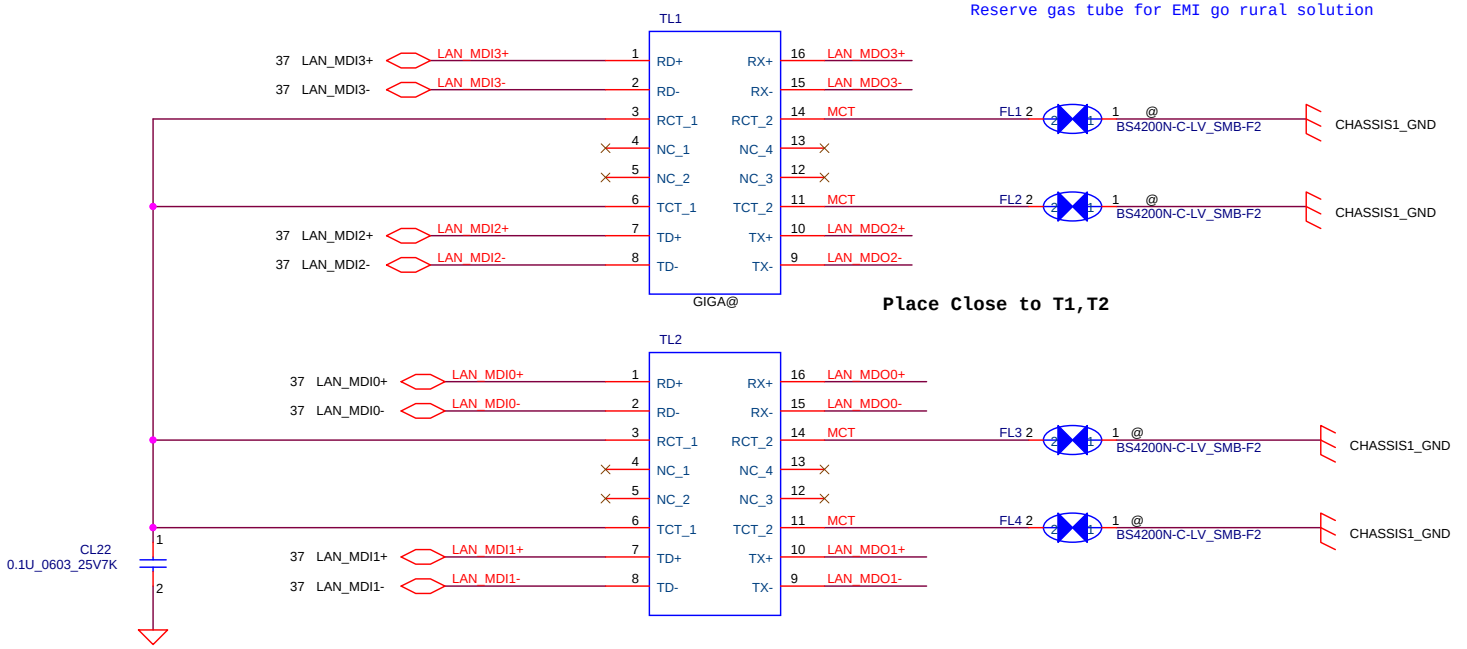


Place Close to TL1

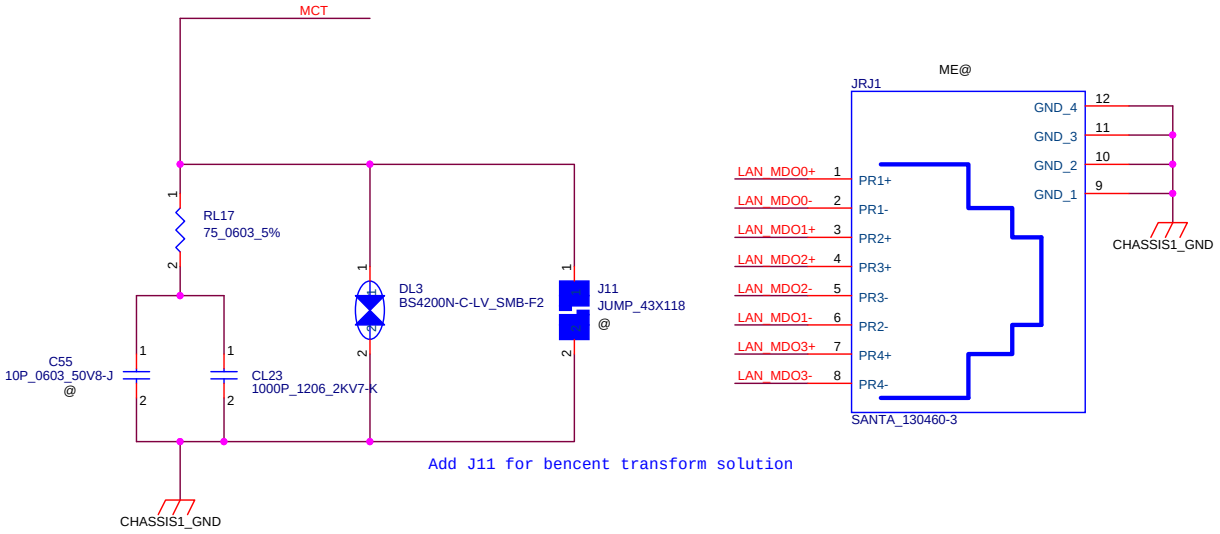


Place Close to TL2

Reserve gas tube for EMI go rural solution



Place Close to T1,T2



Add J11 for bencent transform solution

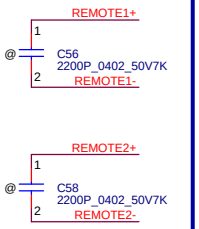
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: LAN_Transformer

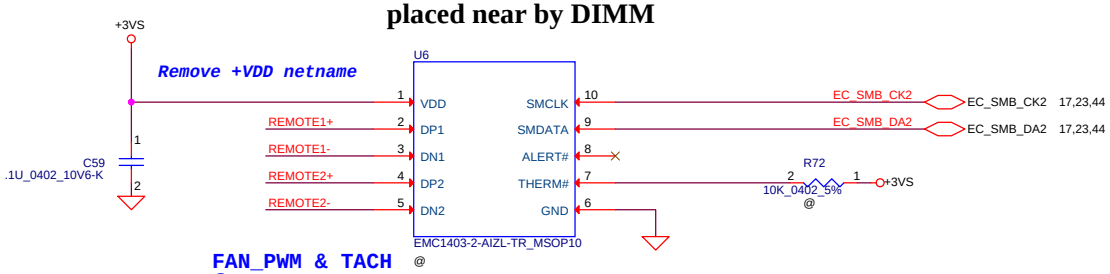
Size	Document Number	Rev
B	401025	1.1

Date: Friday, July 12, 2013 Sheet 38 of 61

Close U4



SMSC thermal sensor placed near by DIMM

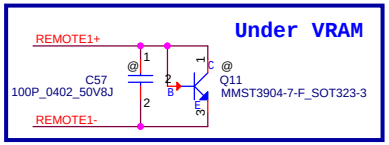


FAN_PWM & TACH for PWM FAN

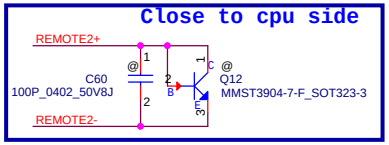
Address 1001_101xb

internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

Under VRAM

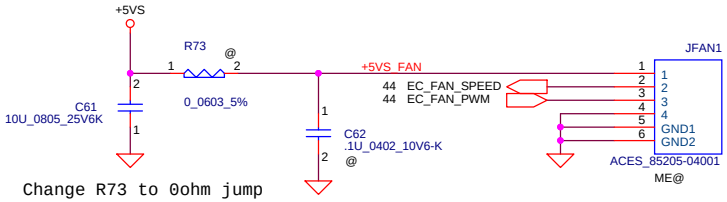


Close to cpu side



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn



Change R73 to 0ohm jump

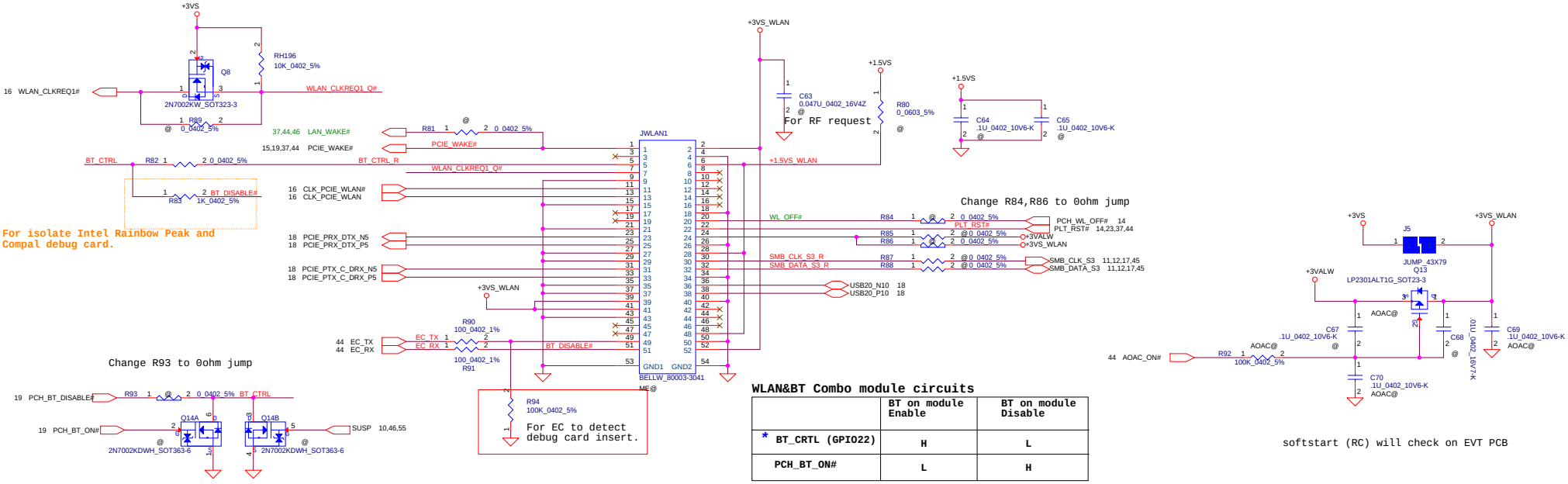
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: VGA Thermal sensor/FAN CONN

Size: Custom | Document Number: 401025 | Rev: 1.1

Date: Friday, July 12, 2013 | Sheet 39 of 61

Mini-Express Card(WLAN/WiMAX)

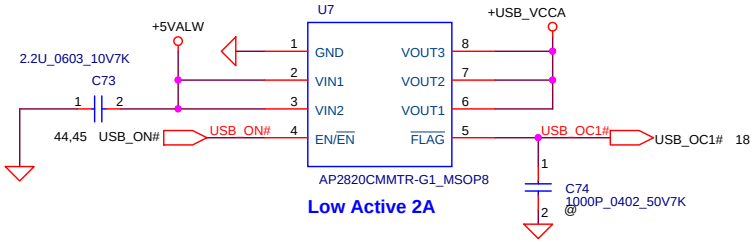


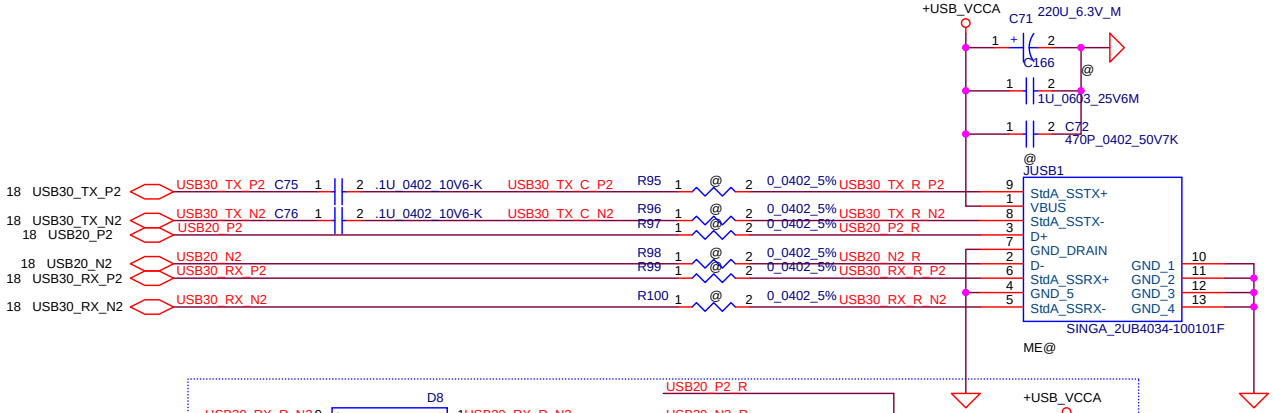
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
* BT_CRTL (GPIO22)	H	L
PCH_BT_ON#	L	H

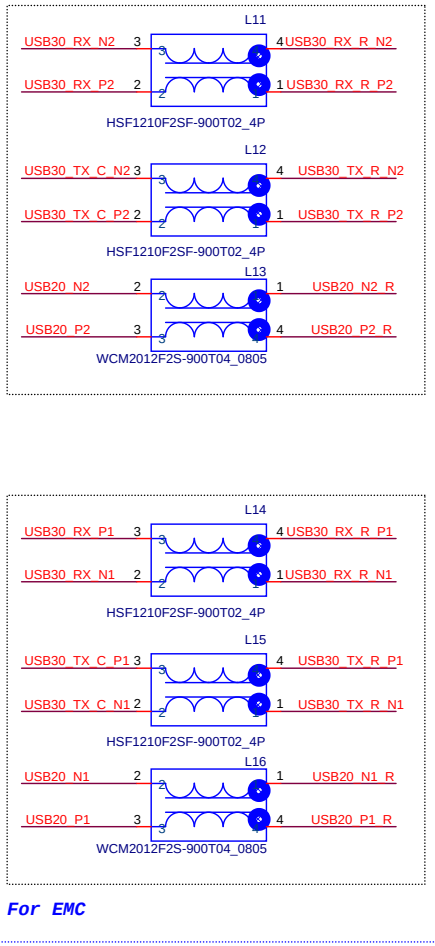
Title	Mini-Card		
Size C	Document Number	401025	Rev 1.1
Date:	Friday, July 12, 2013	Sheet 40 of 61	

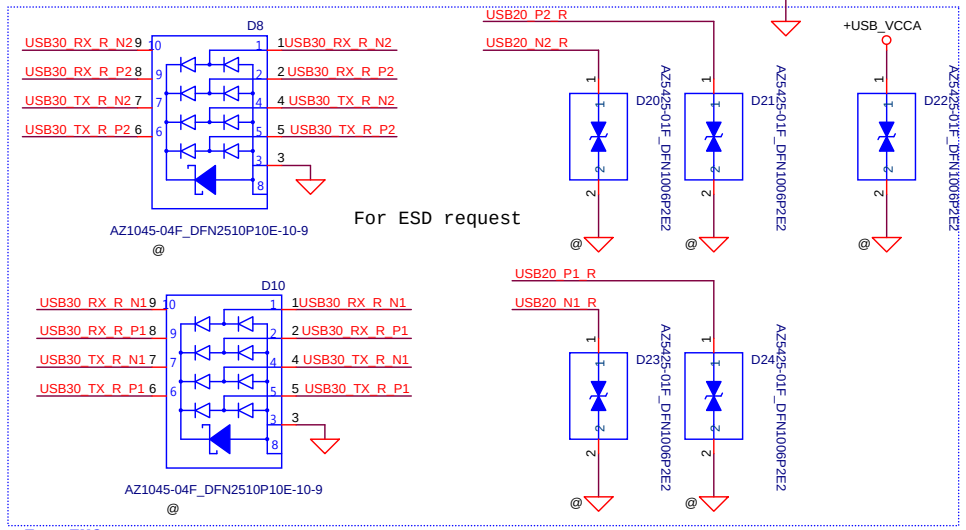
LEFT SIDE USB3.0 PORT X2

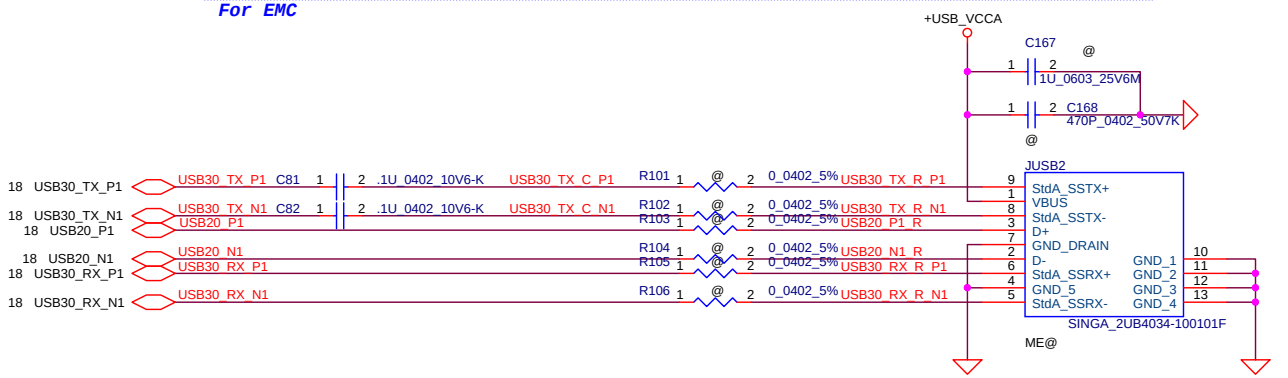




For EMI request
USB2.0 choke --> SM070001S0J
USB3.0 Choke --> SM070001S0J







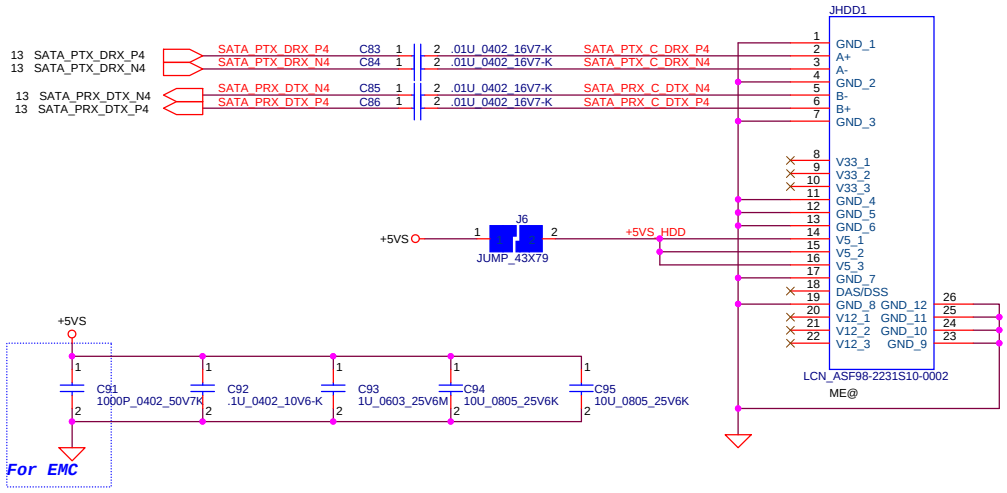
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **USB 3.0 PORT (LEFT)**

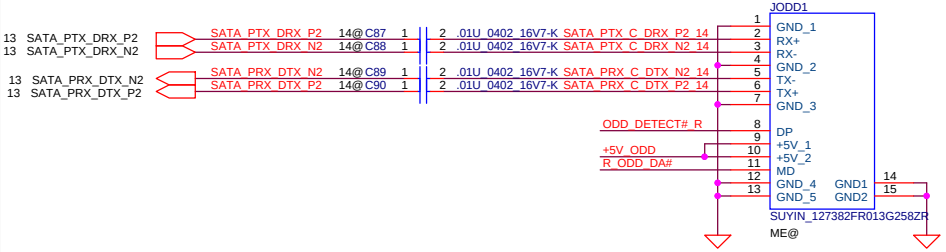
Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 | Sheet 41 of 61

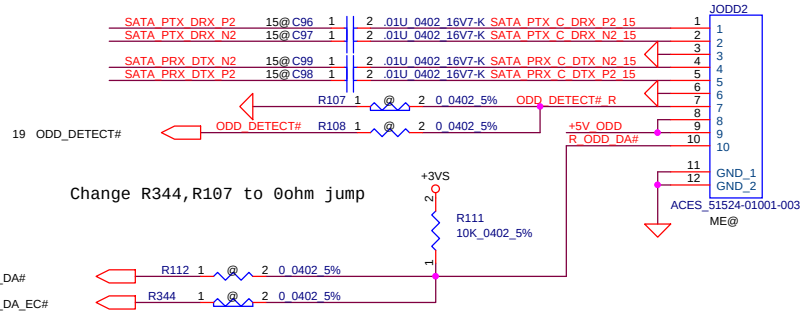
SATA HDD Conn.

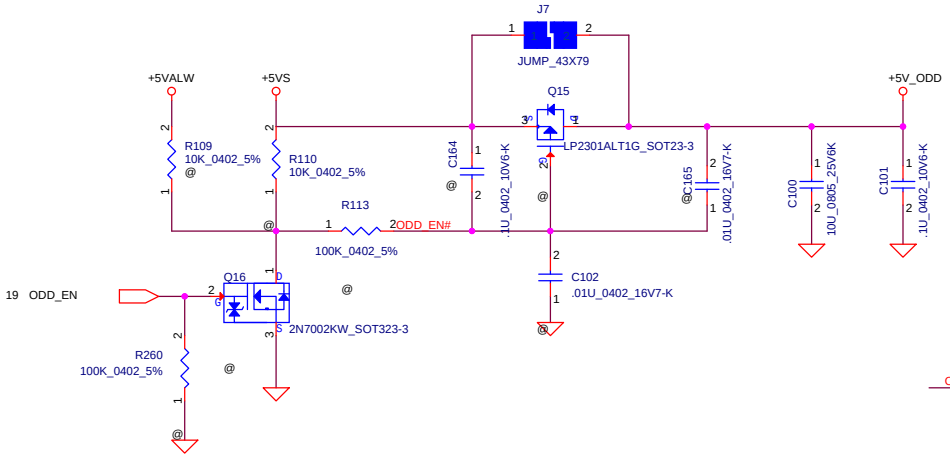


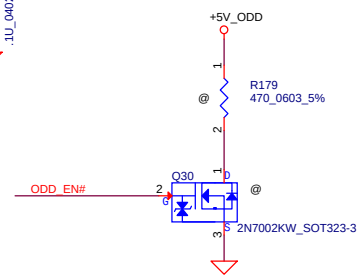
FOR 14"
SATA ODD Conn.

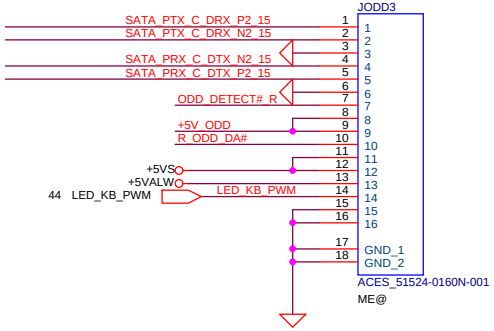


FOR 15"
Co-lay SATA ODD FFC Conn JODD2& JODD3.



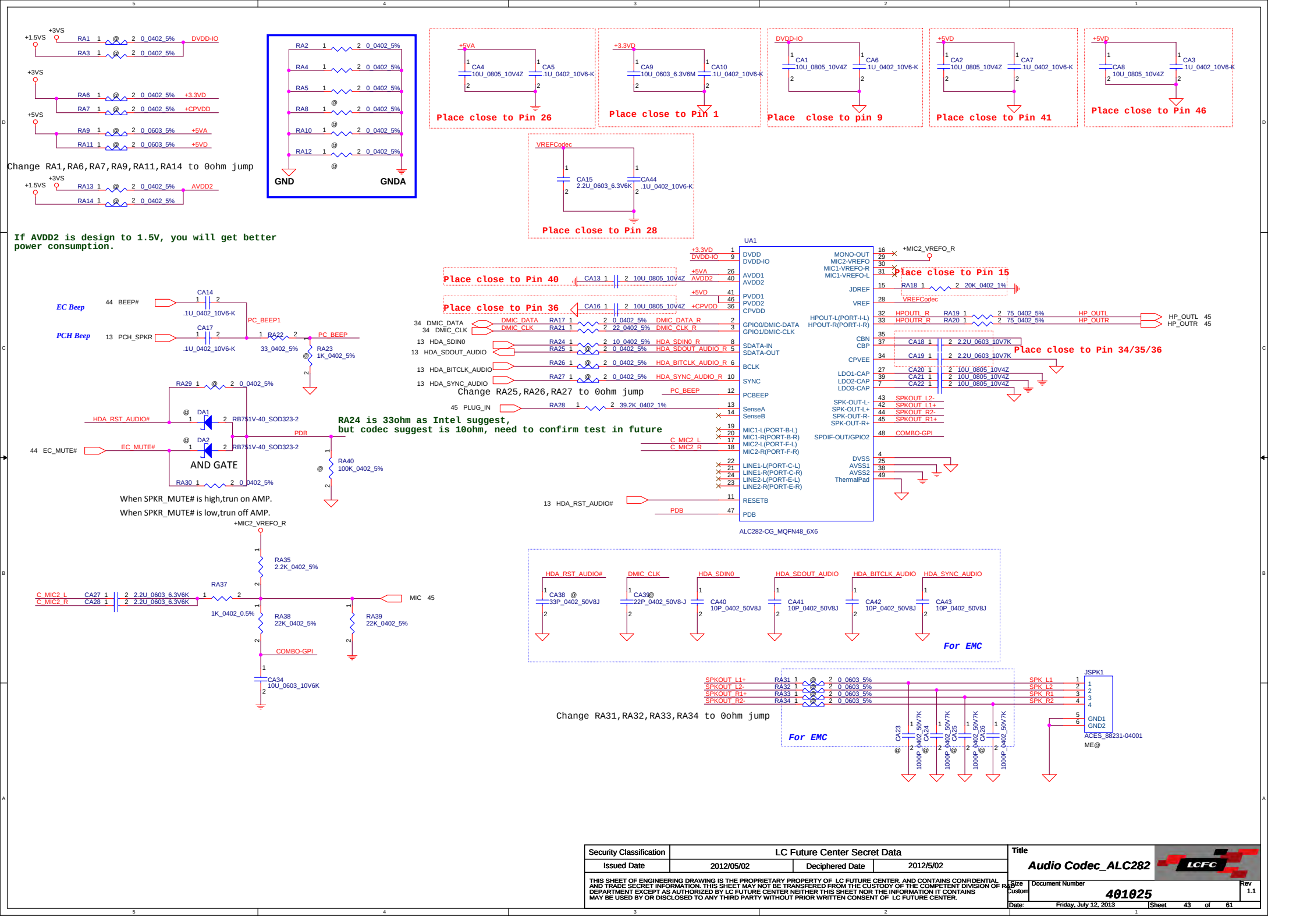






Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title	HDD/ODD CONN		
Size	Document Number		Rev
Custom	401025		1.1
Date:	Friday, July 12, 2013	Sheet	42 of 61

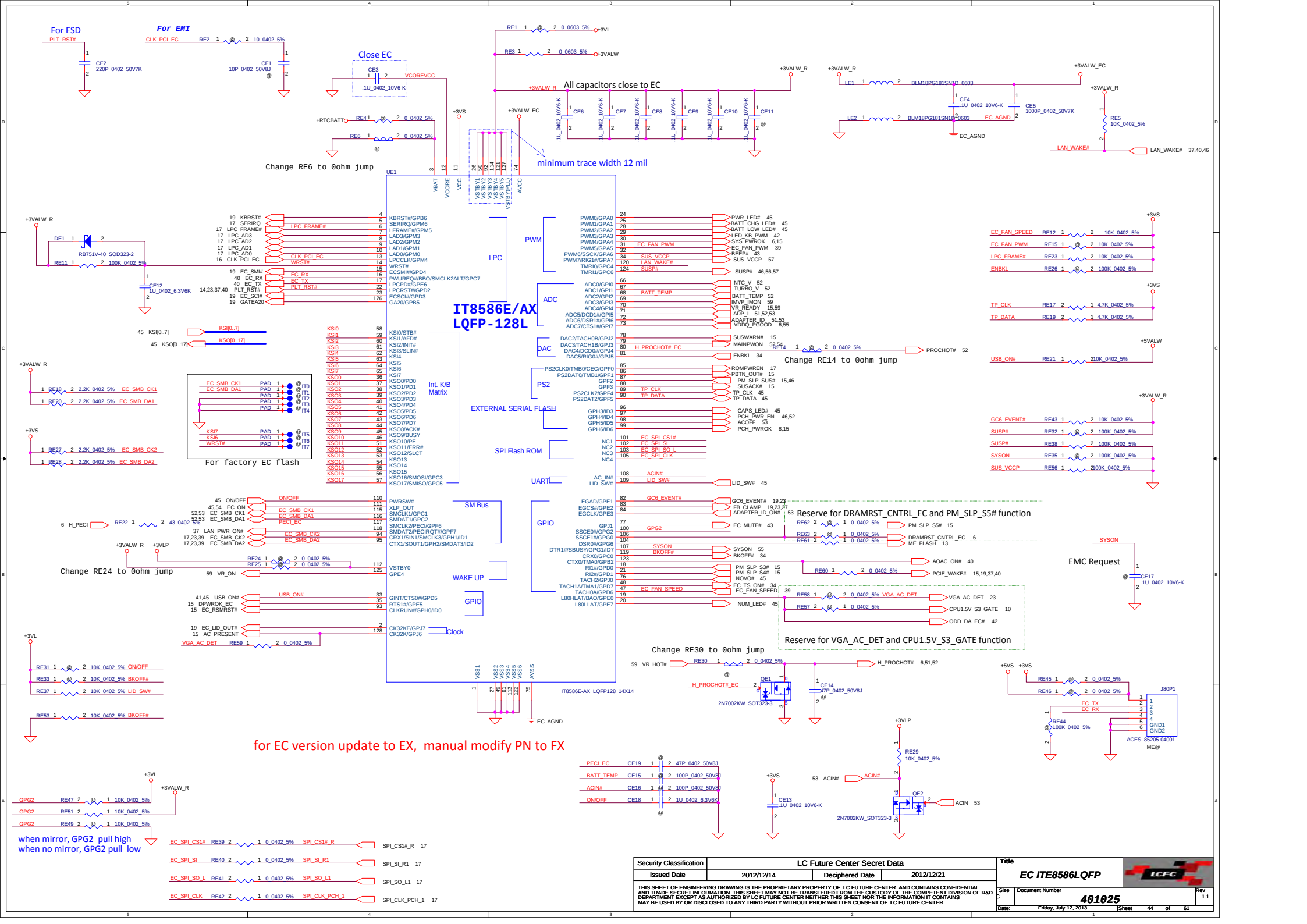


Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **Audio Codec_ALC282**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 43 of 61


For ESD
For EMI
Close EC
All capacitors close to EC
minimum trace width 12 mil
Change RE6 to 0ohm jump
IT8586E/AX
LQFP-128L
UE1
PWM
LPC
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
WAKE UP
GPIO
Clock
Int. K/B Matrix
For factory EC flash
Change RE14 to 0ohm jump
Reserve for DRAMRST_CNTRL_EC and PM_SLP_S5# function
Reserve for VGA_AC_DET and CPU1.5V_S3_GATE function
Change RE30 to 0ohm jump
Change RE24 to 0ohm jump
EMC Request
for EC version update to EX, manual modify PN to FX
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Security Classification
LC Future Center Secret Data
Issued Date
2012/12/14
Deciphered Date
2012/12/21
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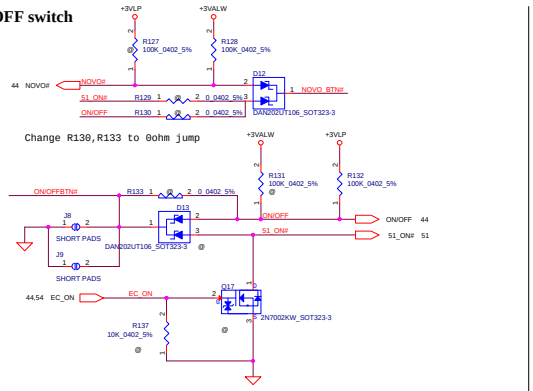
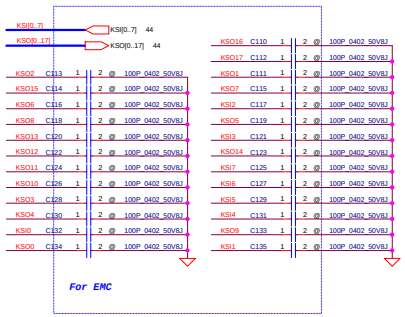
Title
EC ITE8586LQFP
Size
C
Document Number
401025
Rev
1.1
Date:
Friday, July 12, 2013
Sheet
44
of
61

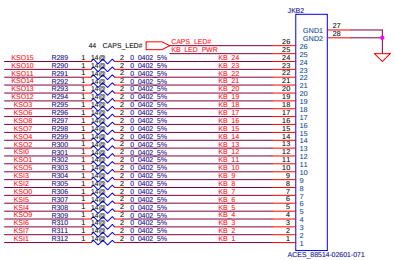
ON/OFF switch



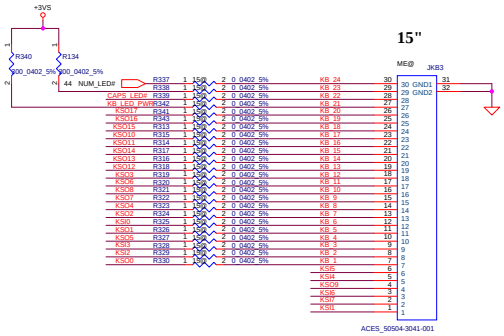
K/B Connector



14"

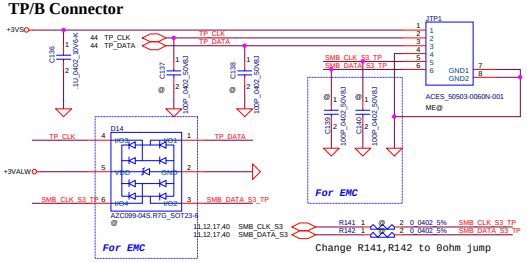


15"

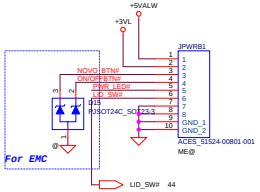


	14"	15"
KB_1	KSI1_14	KSO8_15
KB_2	KSI7_14	KSI2_15
KB_3	KSI6_14	KSI3_15
KB_4	KSO9_14	KSO5_15
KB_5	KSI4_14	KSO1_15
KB_6	KSI5_14	KSI0_15
KB_7	KSO8_14	KSO2_15
KB_8	KSI2_14	KSO4_15
KB_9	KSI3_14	KSO7_15
KB_10	KSO5_14	KSO8_15
KB_11	KSO1_14	KSO6_15
KB_12	KSI0_14	KSO3_15
KB_13	KSO2_14	KSO12_15
KB_14	KSO4_14	KSO13_15
KB_15	KSO7_14	KSO14_15
KB_16	KSO8_14	KSO11_14
KB_17	KSO6_14	KSO10_15
KB_18	KSO3_14	KSO15_15
KB_19	KSO12_14	KSO16_15
KB_20	KSO13_14	KSO17_15
KB_21	KSO14_14	KB_LED_PWR_15
KB_22	KSO11_14	CAPS_LED#_15
KB_23	KSO10_14	VDD_15
KB_24	KSO15_14	NUM_LED#_15

TP/B Connector

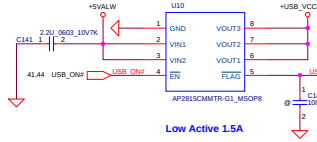


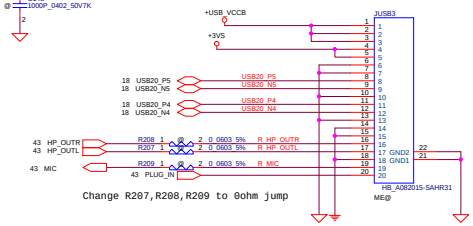
PWR/B Connector



USB I/O Connector

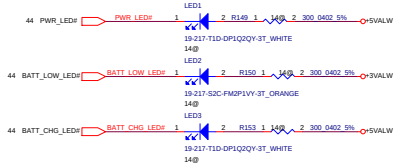
Right Side USB2.0 Port X 1 (USB/B)



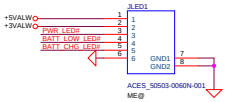


R345 place between JUSB3.13 and JUSB3.14

LED (For 14")



LED (For 15")

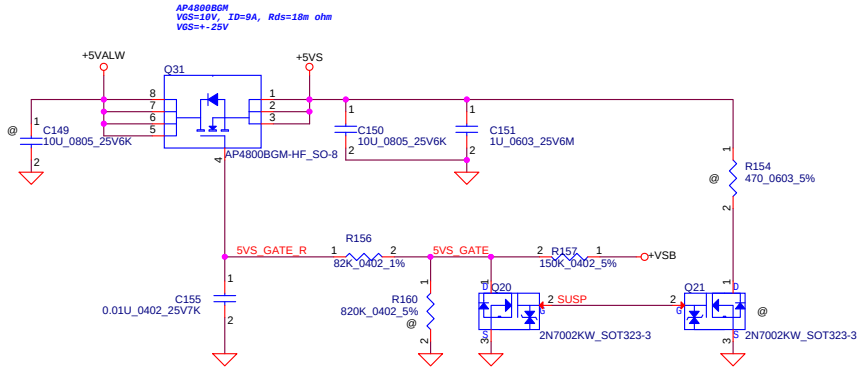


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

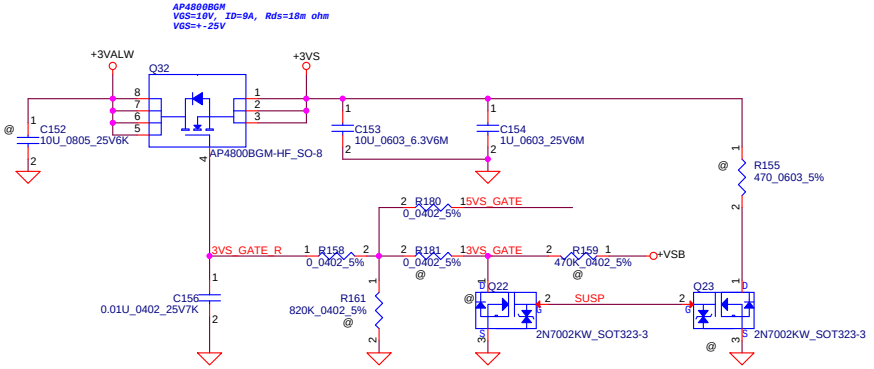
Title: **KBD/PWR/IO/LED/TP Conn.**

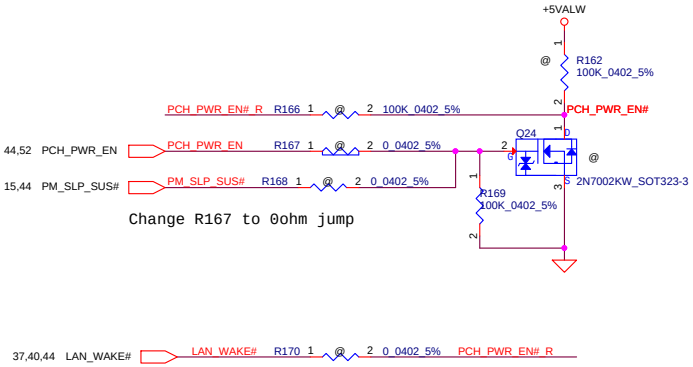
Size: Custom	Document Number: 401025		Rev: 1.1
Date: Friday, July 12, 2013		Sheet 45 of 61	

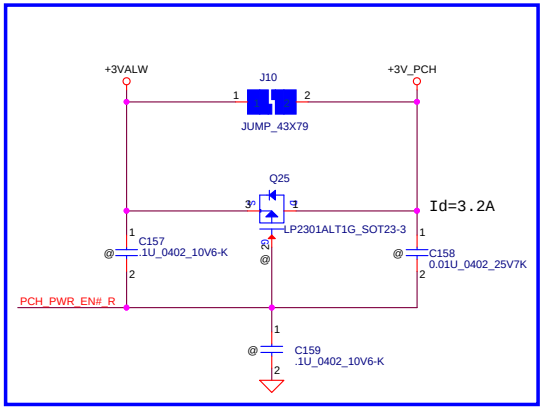
+5VALW to +5VS

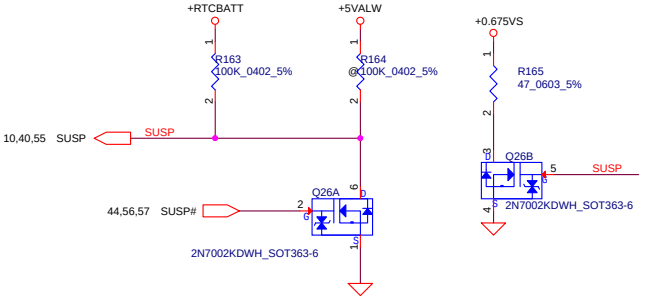


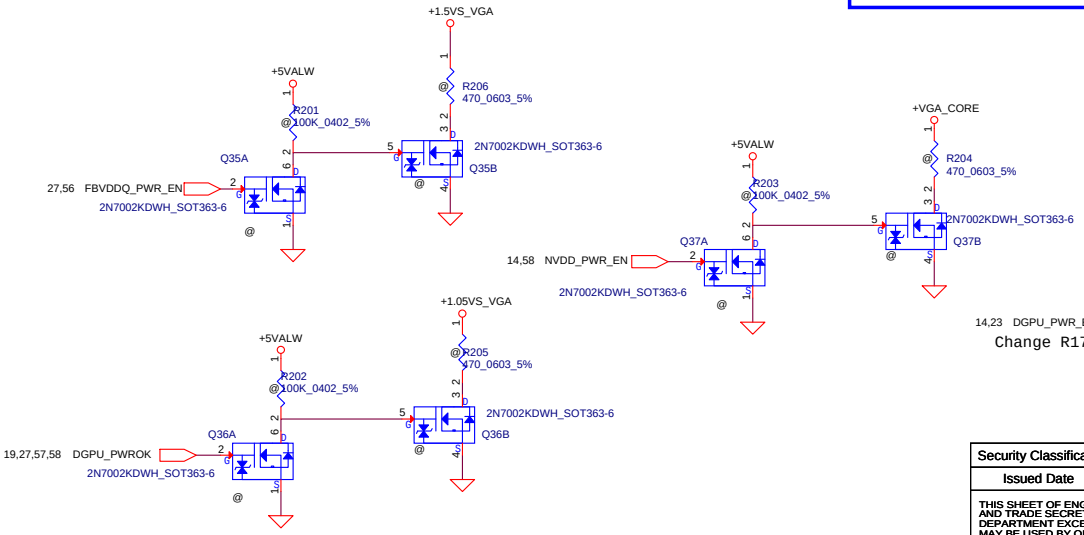
+3VALW to +3VS



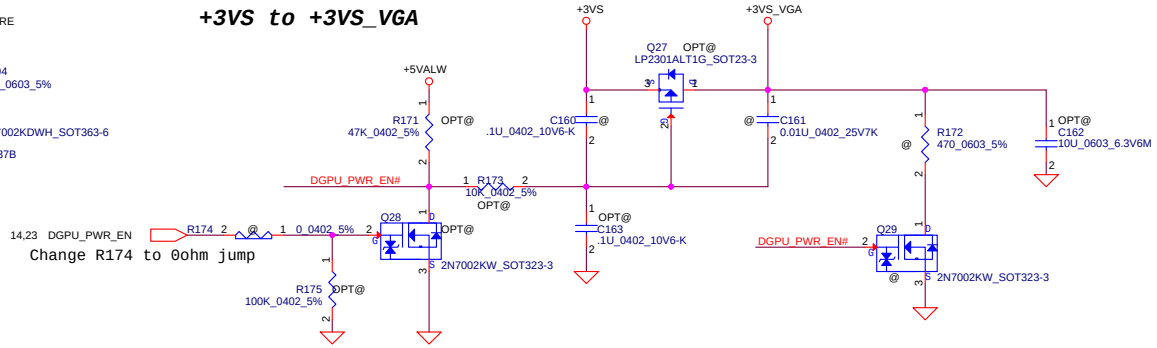








+3VS to +3VS_VGA



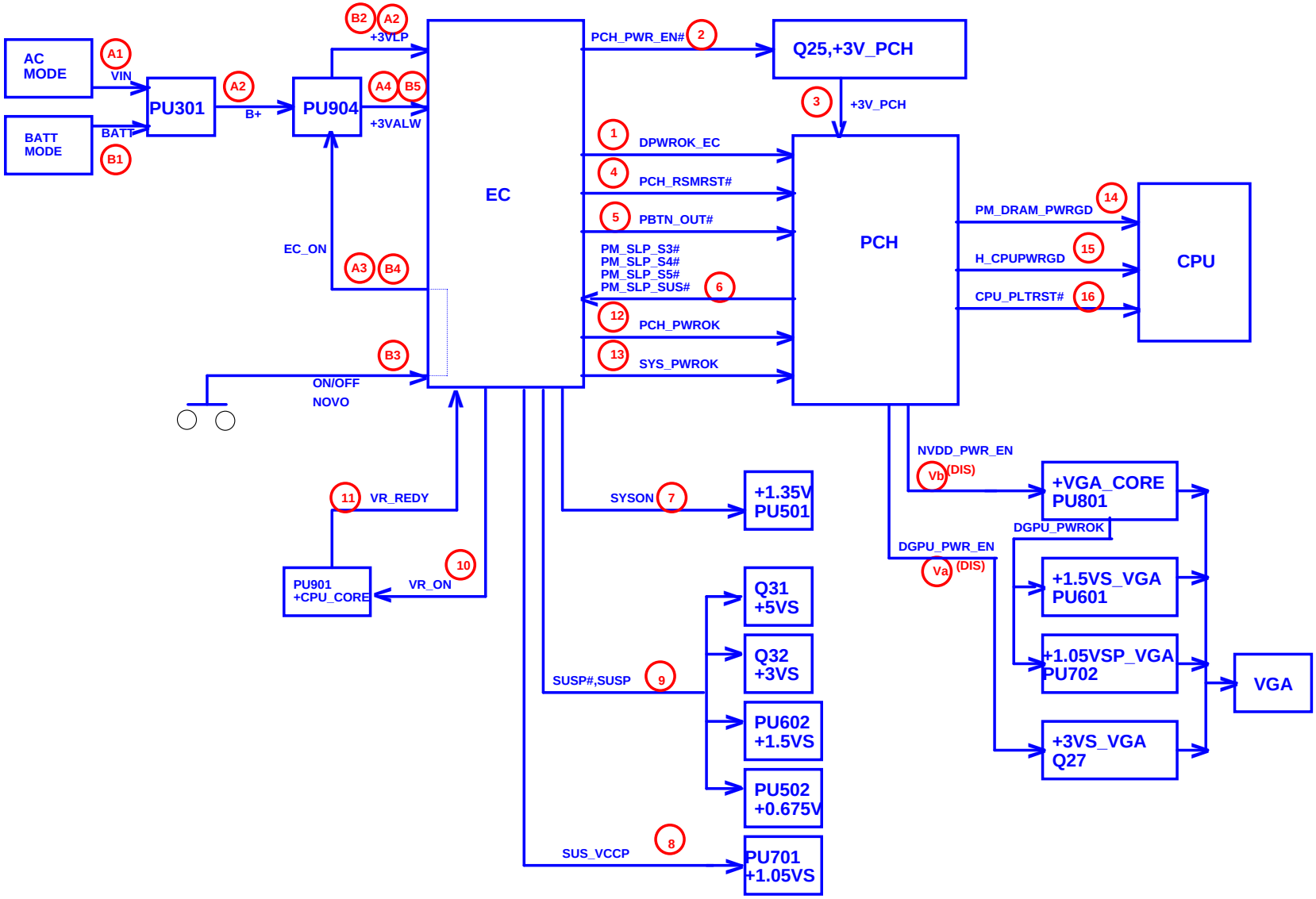
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: **DC V TO VS INTERFACE**

LCFC

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 | Sheet 46 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: *Power sequence Block*

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 47 of 61

UL1 8106@
RTL8106E-CG
SA00005MA00

UL1 8111GS@
RTL8111GS-CG
SA00005O70J

UV3 Samsung S2@ SA00005SH10
UV4 Samsung S2@ SA00005SH10
UV5 Samsung S2@ SA00005SH10
UV6 Samsung S2@ SA00005SH10

UV3 Micron M2@ SA00005M100
UV4 Micron M2@ SA00005M100
UV5 Micron M2@ SA00005M100
UV6 Micron M2@ SA00005M100

UV3 Hynix H2@ SA00005VS00
UV4 Hynix H2@ SA00005VS00
UV5 Hynix H2@ SA00005VS00
UV6 Hynix H2@ SA00005VS00

RV69 S2@ 45.3K_0402_1% SD03445328J
RH153 S2@ 10K_0402_5% SD02B10028J

RV69 M2@ 30.1K_0402_1% SD03430128J
RH153 M2@ 10K_0402_5% SD02B10028J

RV69 H2@ 24.9K_0402_1% SD03424928J
RH153 H2@ 10K_0402_5% SD02B10028J

ZZZ6 PCB PN DAZ0T100100 14@

ZZZ8 PCB PN DAZ0T200100 15@

UV3 K4W4G1646B-HC11_FBGA96 S4@ SA00005OM20
UV4 K4W4G1646B-HC11_FBGA96 S4@ SA00005OM20
UV5 K4W4G1646B-HC11_FBGA96 S4@ SA00005OM20
UV6 K4W4G1646B-HC11_FBGA96 S4@ SA00005OM20

UV3 Micron M4@ SA00005ON10
UV4 Micron M4@ SA00005ON10
UV5 Micron M4@ SA00005ON10
UV6 Micron M4@ SA00005ON10

RV69 S4@ 20K_0402_1% SD03420028J
RH159 S4@ 10K_0402_5% SD02B10028J

RV69 M4@ 10K_0402_1% SD03410028J
RH159 M4@ 10K_0402_5% SD02B10028J

UV3 hynix H4@ SA00005YL00
UV4 hynix H4@ SA00005YL00
UV5 hynix H4@ SA00005YL00
UV6 hynix H4@ SA00005YL00

RV69 H4@ 15K_0402_1% SD03415028J
RH159 H4@ 10K_0402_5% SD02B10028J

ZZZ4 Samsung S2GB@ X7602212001
ZZZ5 Micron M2GB@ X7602212002
ZZZ7 Hynix H2GB@ X7602212003
ZZZ1 Samsung S1GB@ X7602212004
ZZZ2 Micron M1GB@ X7602212005
ZZZ3 Hynix H1GB@ X7602212006

PR812 39K_0402_1% N14MGE@
PR811 30K_0402_1% N14MGE@
PR840 3K_0402_1% N14MGE@
PR815 24K_0402_1% N14MGE@
PR814 3K_0402_1% N14MGE@
PC812 1800P_0402_50V7-K N14MGE@

U6 EMC1403-2-AIZL-TR_MSOP10 OPT@ SA00002921J
Q12 MMST3904-7-F_SOT323-3 OPT@ SB000002R0J
C58 2200P_0402_50V7K OPT@ SE074222K8J
Q11 MMST3904-7-F_SOT323-3 OPT@ SB000002R0J
C56 2200P_0402_50V7K OPT@ SE074222K8J

U6 EMC1403-2-AIZL-TR_MSOP10 47W@ SA00002921J
Q12 MMST3904-7-F_SOT323-3 47W@ SB000002R0J
C58 2200P_0402_50V7K 47W@ SE074222K8J

PR917 7.5K_0402_1% 47W@
PR912 15.4K_0402_1% 47W@
PR910 66.5K_0402_1% 47W@

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/14	Deciphered Date	2012/12/21

Title: *Virtual symbol*

LCFC

Size: Custom | Document Number: 401025 | Rev: 0.3

Date: Friday, July 12, 2013 | Sheet 48 of 61

H15
HOLEA
PAD_C7P0D3P8
@

H2
HOLEA
PAD_C7P0D4P0
@

H3
HOLEA
PAD_C7P0D4P0
@

CPU scoket

H4
HOLEA
PAD_CT3P7B6P0D3P3

H5
HOLEA
PAD_CT3P7B6P0D3P3

GPU

H9
HOLEA
PAD_C6P0D3P3

WLAN

H1
HOLEA
CHASSIS1_GND
PAD_CT6P0B5P0D3P3

H24
HOLEA
CHASSIS1_GND
PAD_CT8P0B5P0D4P6
@

RJ45

PCB Fedical Mark PAD

FD1 @
FD2 @
FD3 @
FD4

H20
HOLEA
H_3P0N
@

H19
HOLEA
H_3P9N
@

H21
HOLEA
H_3P0X4P0N
@

H22
HOLEA
H_4P0X3P0N
@

NPTH

H8
HOLEA
PAD_CT9P0B7P0D2P8
@

H13
HOLEA
PAD_CT9P0B7P0D2P8
@

H10
HOLEA
PAD_CT9P0B7P0D2P8
@

H23
HOLEA
PAD_CT7P5B7P0D2P8
@

H12
HOLEA
PAD_CT7P5B7P0D2P8
@

H6
HOLEA
PAD_CT7P5B7P0D2P8
@

H11
HOLEA
PAD_CT9P0B7P0D2P3
@

H14
HOLEA
PAD_CT9P0B7P0D3P0
@

H16
HOLEA
PAD_CT7P5B7P0D2P8
@

H17
HOLEA
PAD_CT7P0B9P0D2P5
@

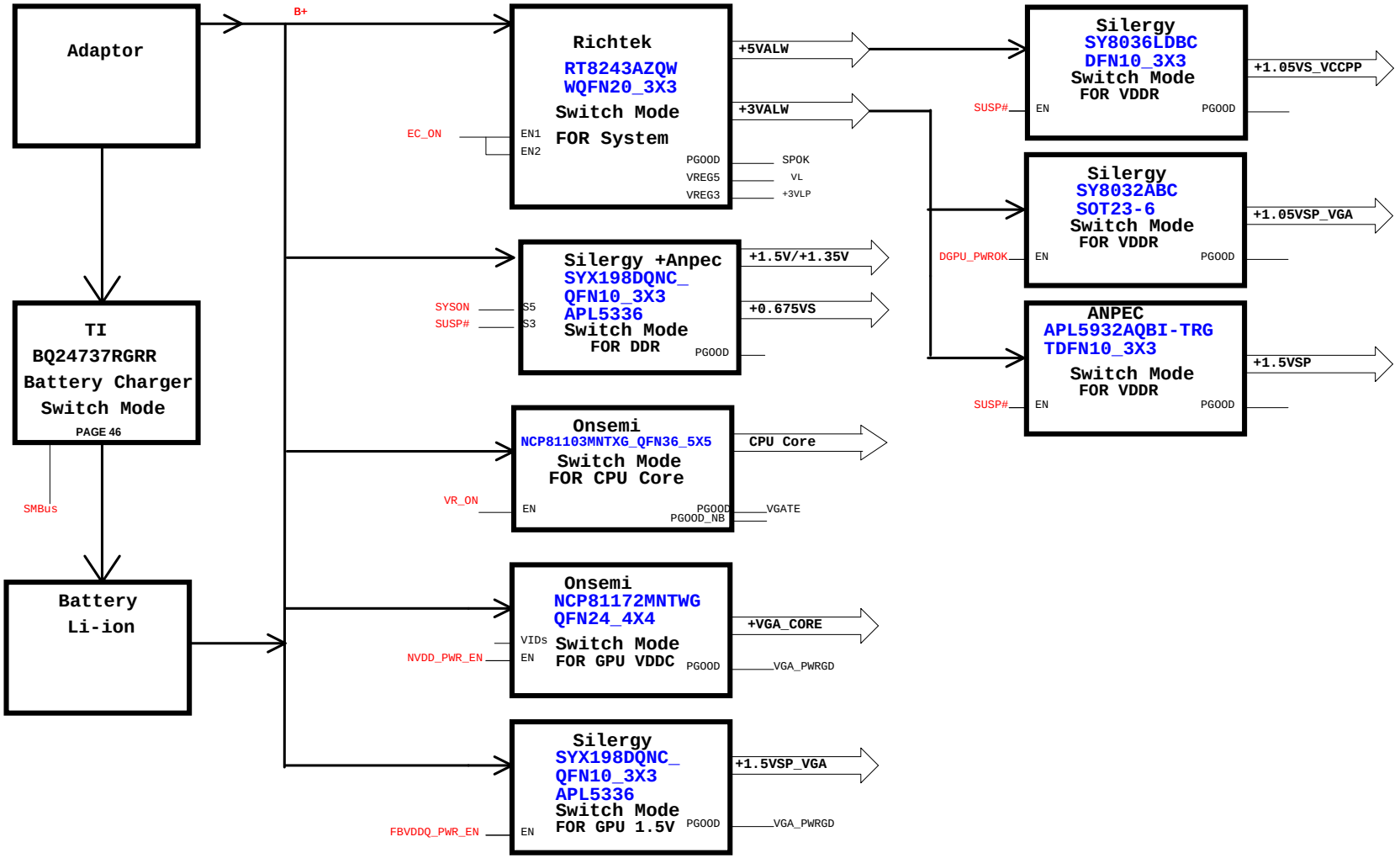
H18
HOLEA
PAD_CT7P5B9P0D2P8
@

H7
HOLEA
PAD_C10P0D7P0
@

H25
HOLEA
PAD_CT7P0B6P5D2P8
@

Title: Hole

Size: B	Document Number: 401025	Rev: 1.1
Date: Friday, July 12, 2013	Sheet 49 of 61	

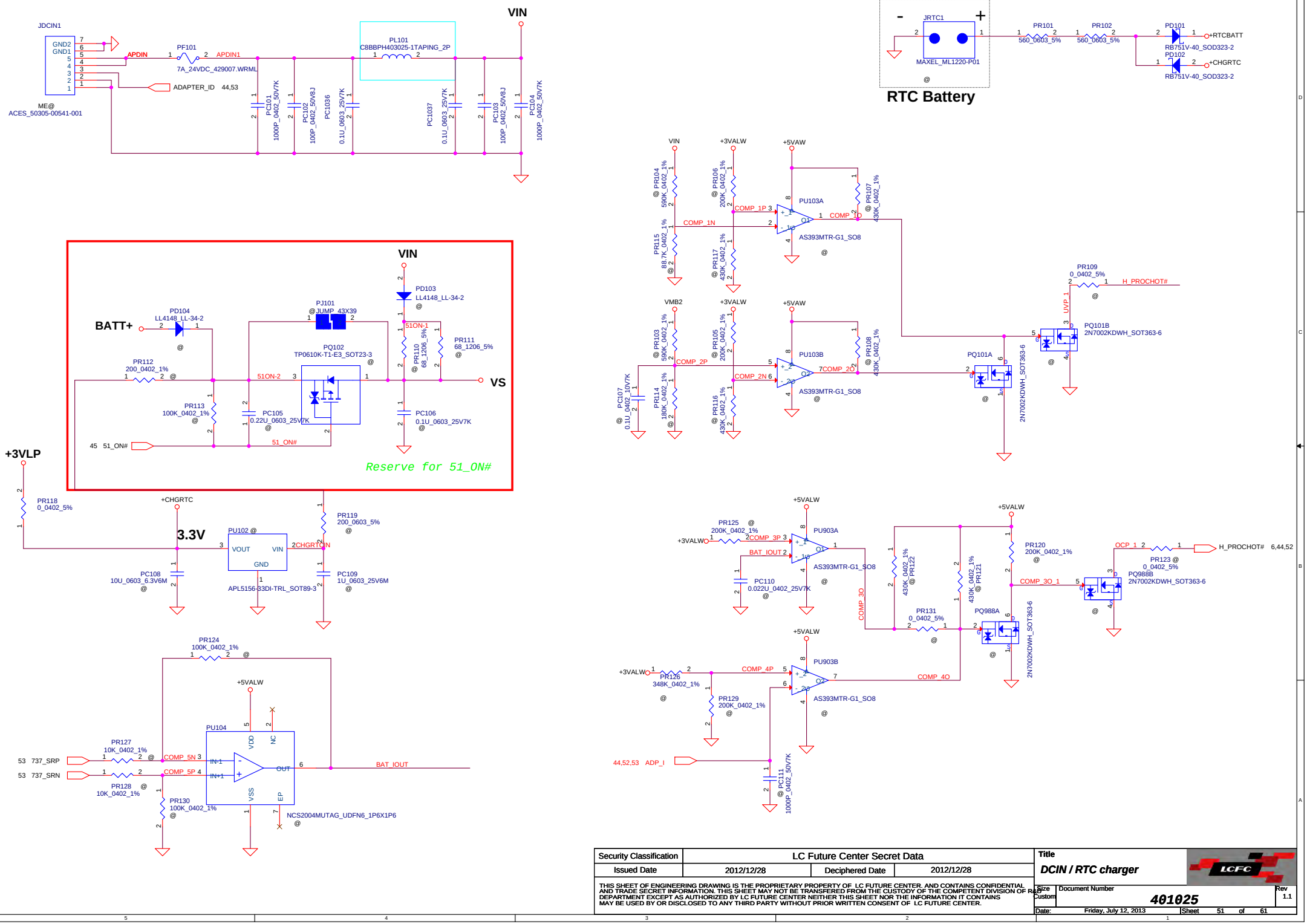


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title: **Power Diagram**

Size	Document Number	Rev
C	401025	1.1

Date: Friday, July 12, 2013 | Sheet 50 of 61

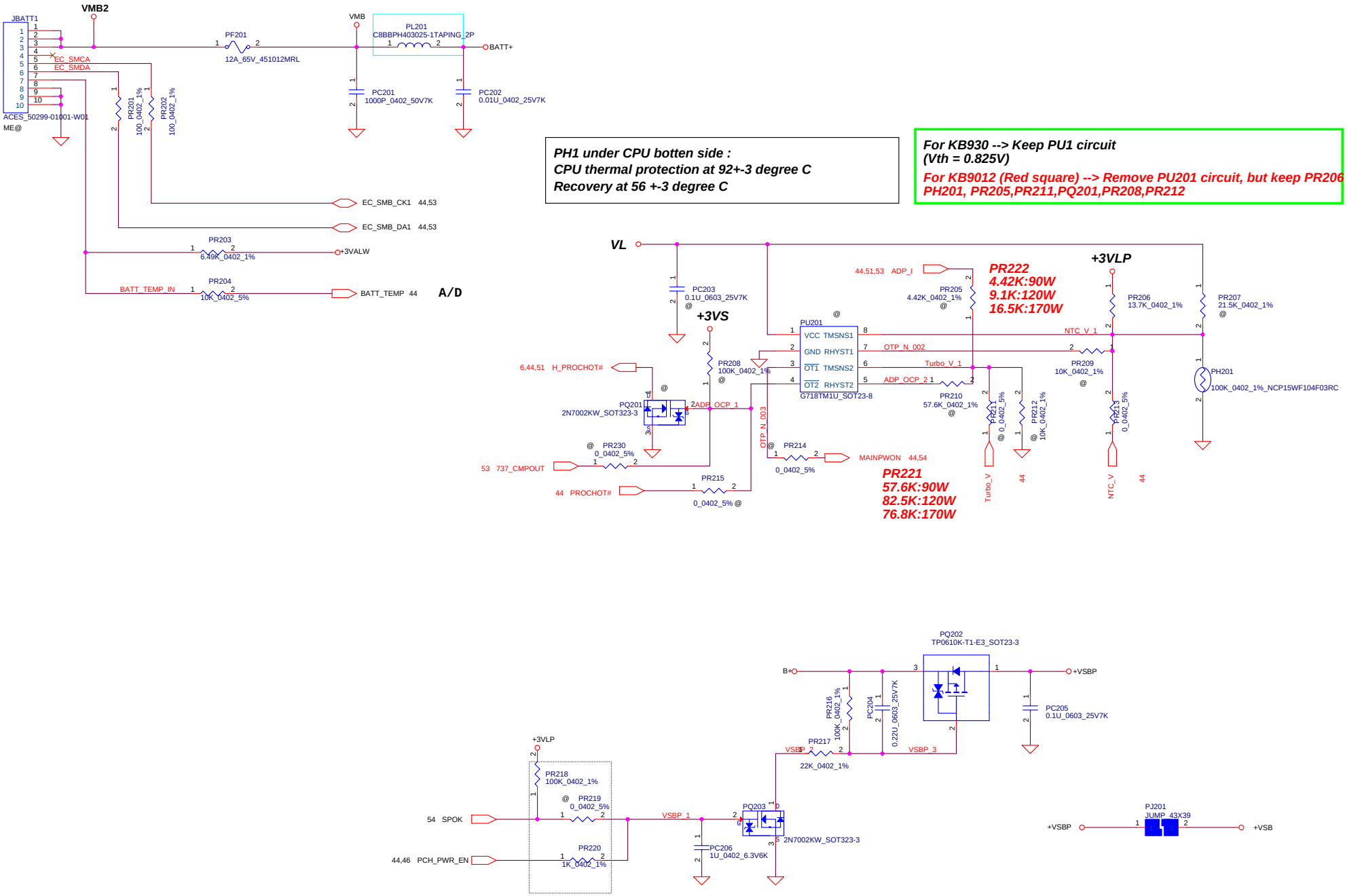


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title: **DCIN / RTC charger**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 51 of 61

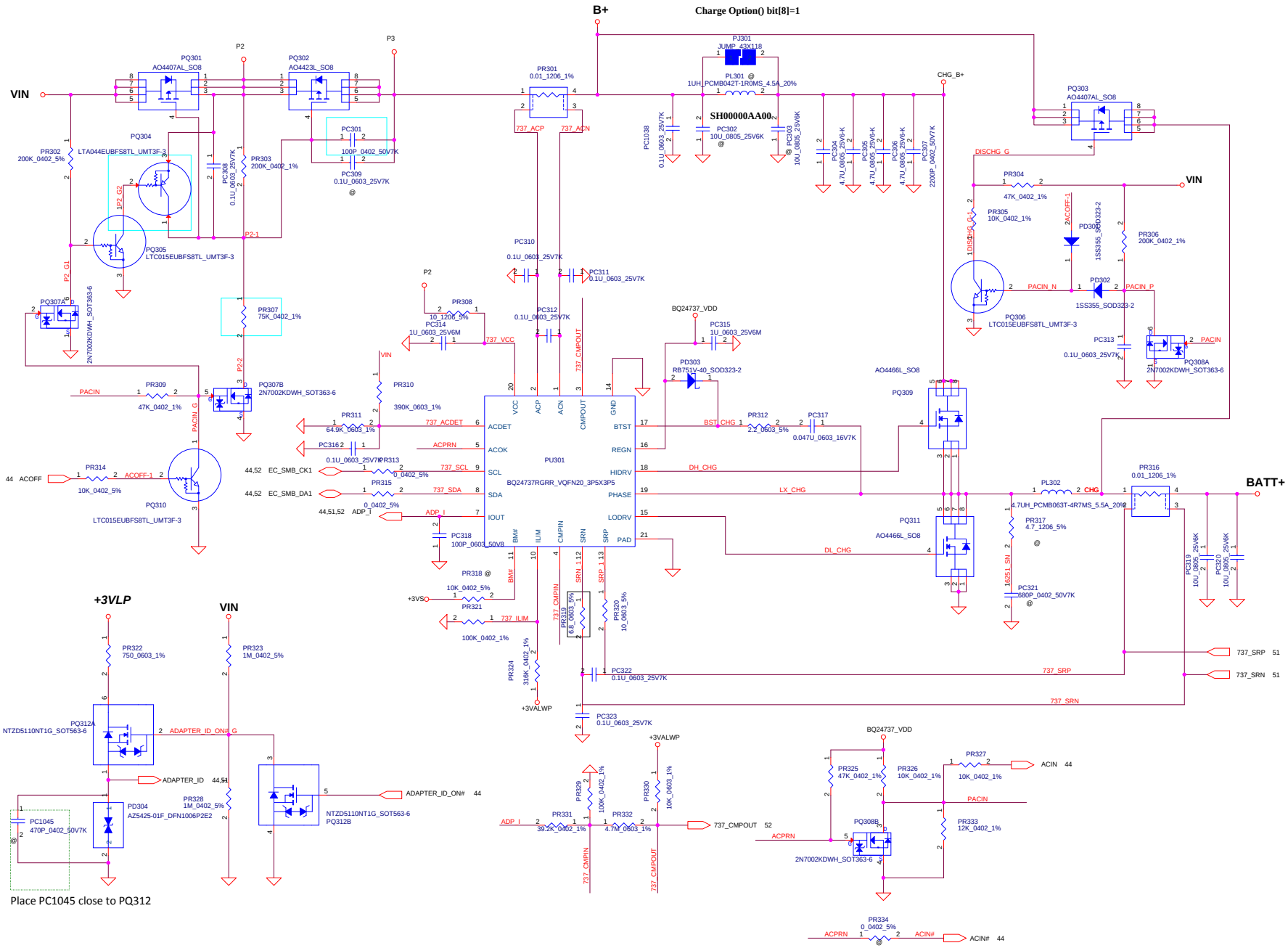


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 52 of 61


B+
Charge Option() bit[8]=1
VIN
CHG_B+
BATT+
+3VLP
+3VALWP
+3VS
PJ301
JUMP_43X118
PL301 @
1UH_PCMB042T-1R0MS_4.5A_20%
SH00000AA00
PQ301
AO4407AL_SO8
PQ302
AO4423L_SO8
PQ303
AO4407AL_SO8
PQ304
LTA044EUBFS8TL_UMT3F-3
PQ305
LTC015EUBFS8TL_UMT3F-3
PQ306
LTC015EUBFS8TL_UMT3F-3
PQ307A
2N7002KDWH_SOT363-6
PQ307B
2N7002KDWH_SOT363-6
PQ308A
2N7002KDWH_SOT363-6
PQ308B
2N7002KDWH_SOT363-6
PQ309
AO4466L_SO8
PQ310
LTC015EUBFS8TL_UMT3F-3
PQ311
AO4466L_SO8
PQ312A
NTZD5110NT1G_SOT563-6
PQ312B
NTZD5110NT1G_SOT563-6
PD302
1SS355_SOD323-2
PD303
RB751V-40_SOD323-2
PD304
AZ5425-01F_DFN1006P2E2
PU301
BQ24737RGRR_VQFN20_3P5X3P5
PR301 0.01_1206_1%
PR302 200K_0402_5%
PR303 200K_0402_1%
PR304 47K_0402_1%
PR305 10K_0402_1%
PR306 200K_0402_1%
PR307 75K_0402_1%
PR308 10_1206_5%
PR309 47K_0402_1%
PR310 390K_0603_1%
PR311 64.9K_0603_1%
PR312 2.2_0603_5%
PR313 0_0402_5%
PR314 10K_0402_5%
PR315 0_0402_5%
PR316 0.01_1206_1%
PR317 4.7_1206_5%
PR318 @
PR319 68_0603_5%
PR320 10_0603_5%
PR321 100K_0402_1%
PR322 750_0603_1%
PR323 1M_0402_5%
PR324 316K_0402_1%
PR325 47K_0402_1%
PR326 10K_0402_1%
PR327 10K_0402_1%
PR328 1M_0402_5%
PR329 100K_0402_1%
PR330 10K_0603_1%
PR331 39.2K_0402_1%
PR332 4.7M_0603_1%
PR333 12K_0402_1%
PR334 0_0402_5%
PC301 100P_0402_50V7K
PC302 10U_0805_25V6K @
PC303 10U_0805_25V6K @
PC304 4.7U_0805_25V6-K
PC305 4.7U_0805_25V6-K
PC306 4.7U_0805_25V6-K
PC307 2200P_0402_50V7K
PC308 0.1U_0603_25V7K
PC309 0.1U_0603_25V7K @
PC310 0.1U_0603_25V7K
PC311 0.1U_0603_25V7K
PC312 0.1U_0603_25V7K
PC313 0.1U_0603_25V7K
PC314 1U_0603_25V6M
PC315 1U_0603_25V6M
PC316 0.1U_0603_25V7K
PC317 0.047U_0603_16V7K
PC318 100P_0603_50V8
PC319 10U_0805_25V6K
PC320 10U_0805_25V6K
PC321 680P_0402_50V7K @
PC322 0.1U_0603_25V7K
PC323 0.1U_0603_25V7K
PC1038 0.1U_0603_25V7K
PC1045 470P_0402_50V7K @
Place PC1045 close to PQ312
VCC
ACP
ACN
CMPOUT
GND
ACDET
ACOK
SCL
SDA
IOUT
BTST
REGN
HIDRV
PHASE
LODRV
PAD
BM#
ILIM
CMPIN
SRN
SRP
737_ACP
737_ACN
737_ACDET
ACPRN
737_SCL
737_SDA
ADP_I
737_VCC
737_CMPOUT
737_CMPIN
737_ILIM
BST_CHG
DH_CHG
LX_CHG
DL_CHG
737_SRP
737_SRN
DISCHG_G
PACIN
PACIN_N
PACIN_P
ACOFF
ACOFF-1
ADAPTER_ID
ADAPTER_ID_ON#
ADAPTER_ID_ON#_G
ACIN
ACIN#
EC_SMB_CK1
EC_SMB_DA1
BQ24737_VDD
Security Classification
LC Future Center Secret Data
Issued Date
2012/12/28
Deciphered Date
2012/12/28
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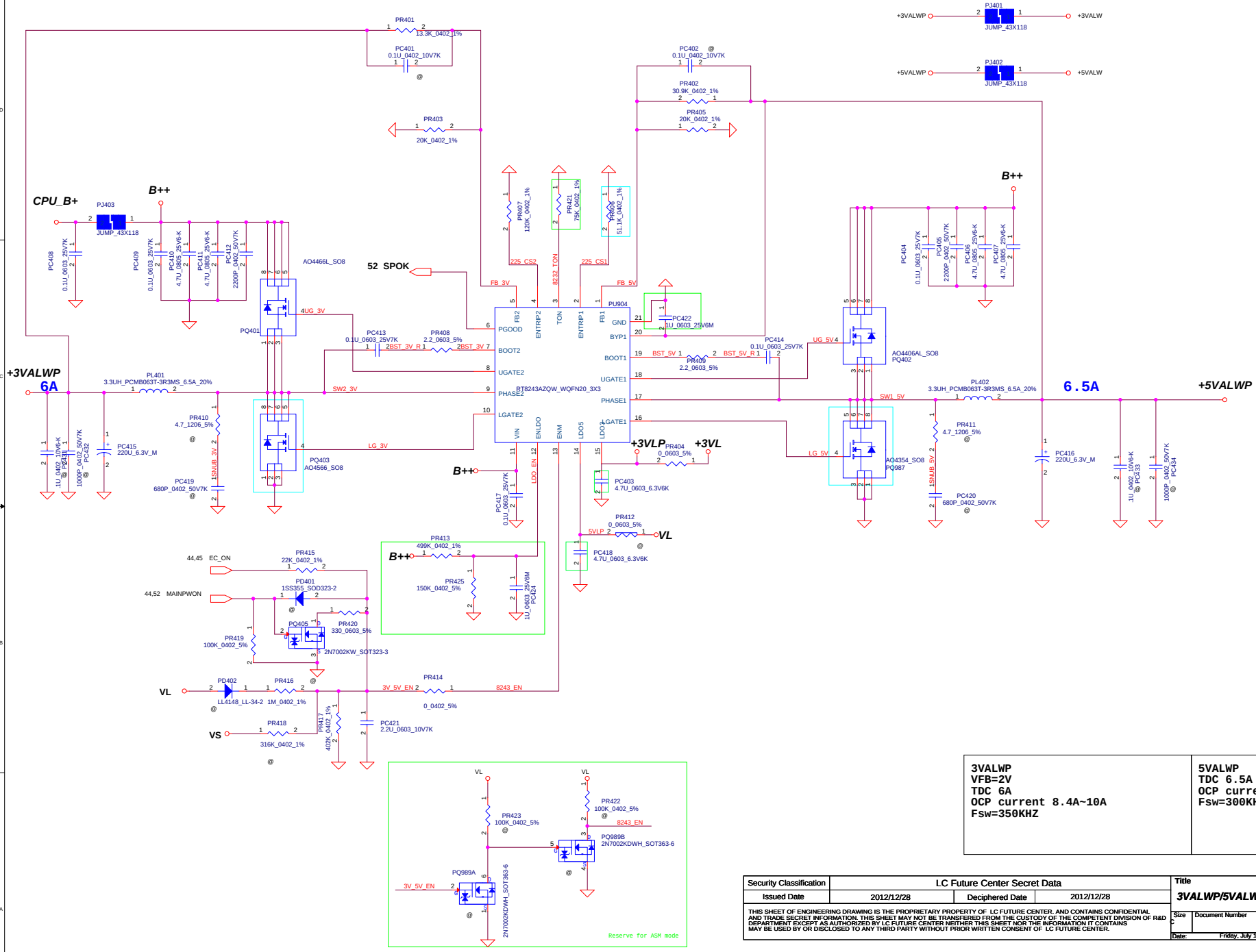
Title
CHARGER
Size
C
Document Number
401025
Rev
1.1
Date:
Friday, July 12, 2013
Sheet
53
of
61



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

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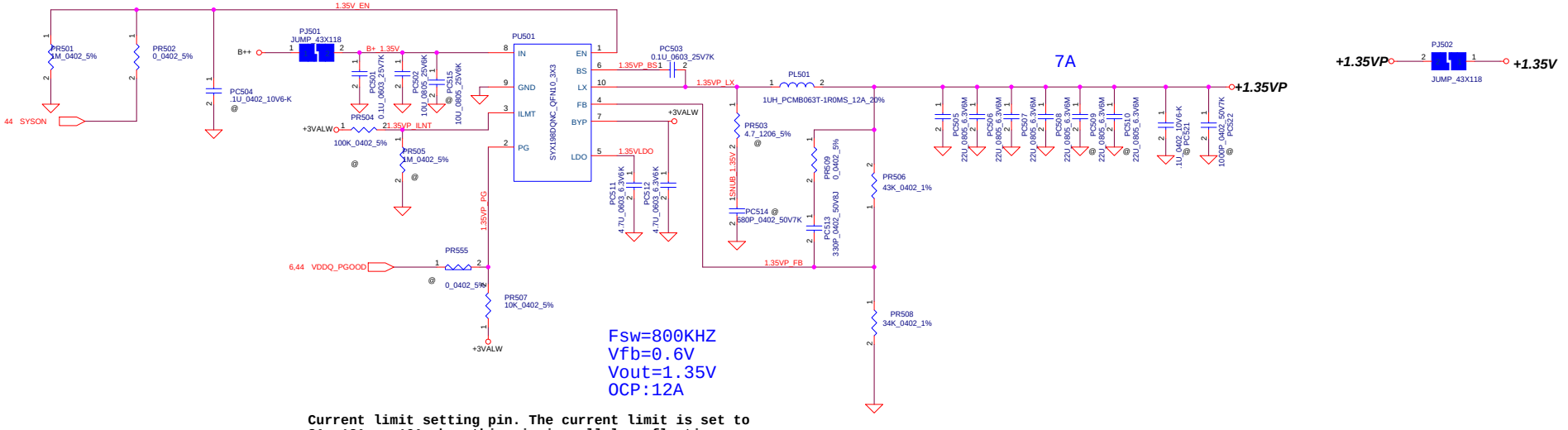
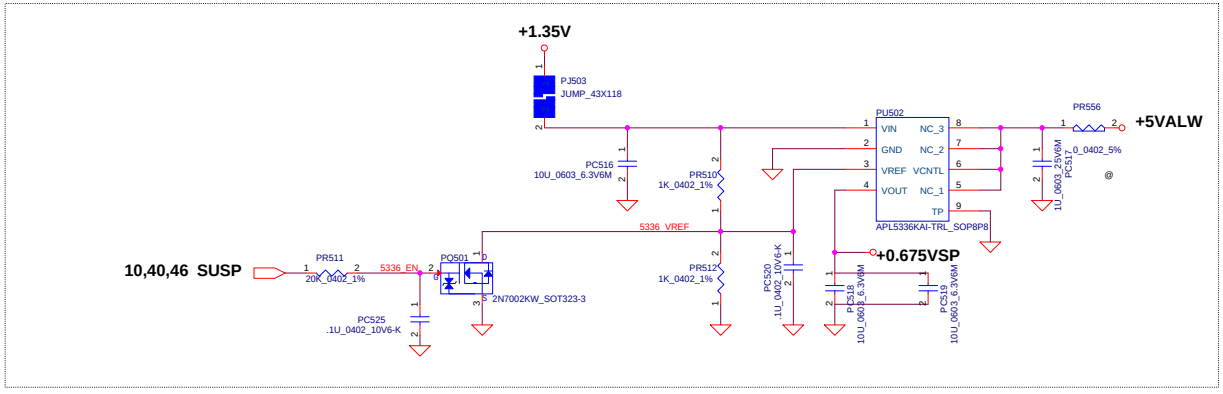
Title: *3VALWP/5VALWP*

Size	Document Number	Rev
C	*401025*	1.1

Date: Friday, July 12, 2013 | Sheet 54 of 61

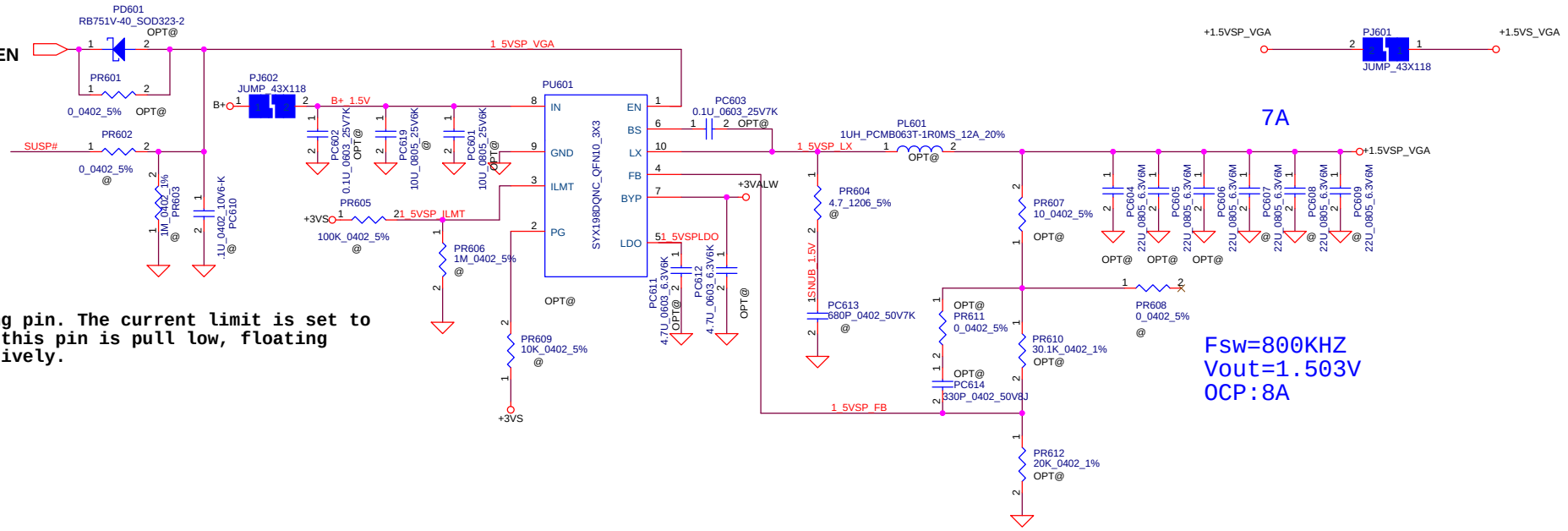




Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

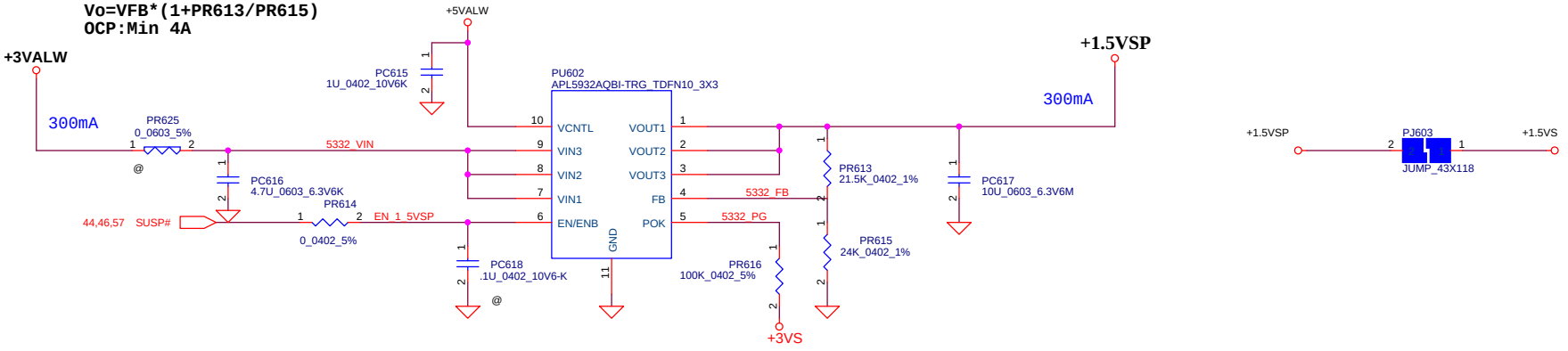
Title	1.35VP/0.675VSP
Size	C
Document Number	401025
Rev	1.1
Date:	Friday, July 12, 2013
Sheet	55 of 61

27,46 FBVDDQ_PWR_EN



Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

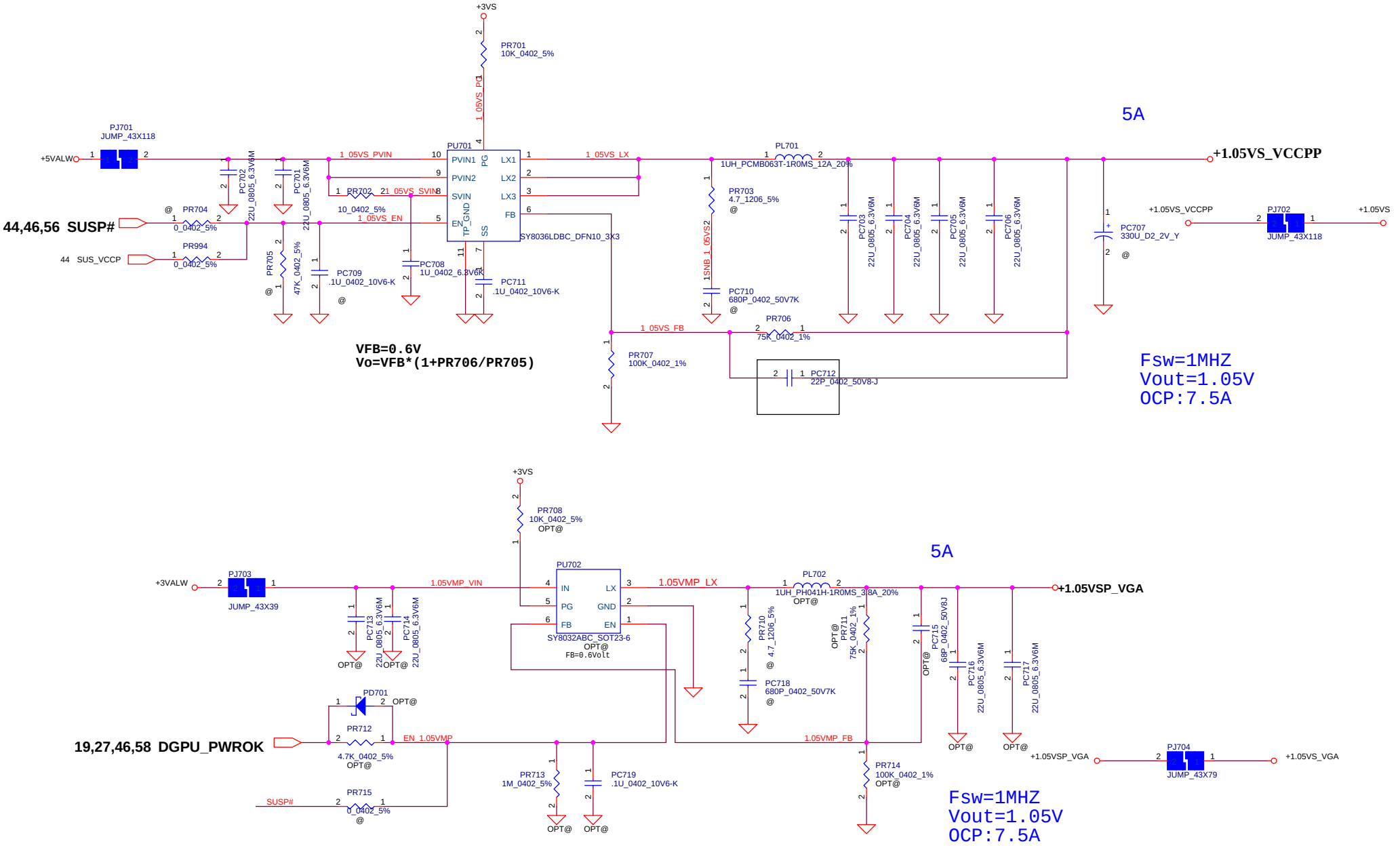
VFB=0.8V
Vo=VFB*(1+PR613/PR615)
OCP:Min 4A



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title: +1.35VS_VGA/+1.5VS

Size: Custom	Document Number: 401025	Rev: 1.1
Date: Friday, July 12, 2013	Sheet 56 of 61	

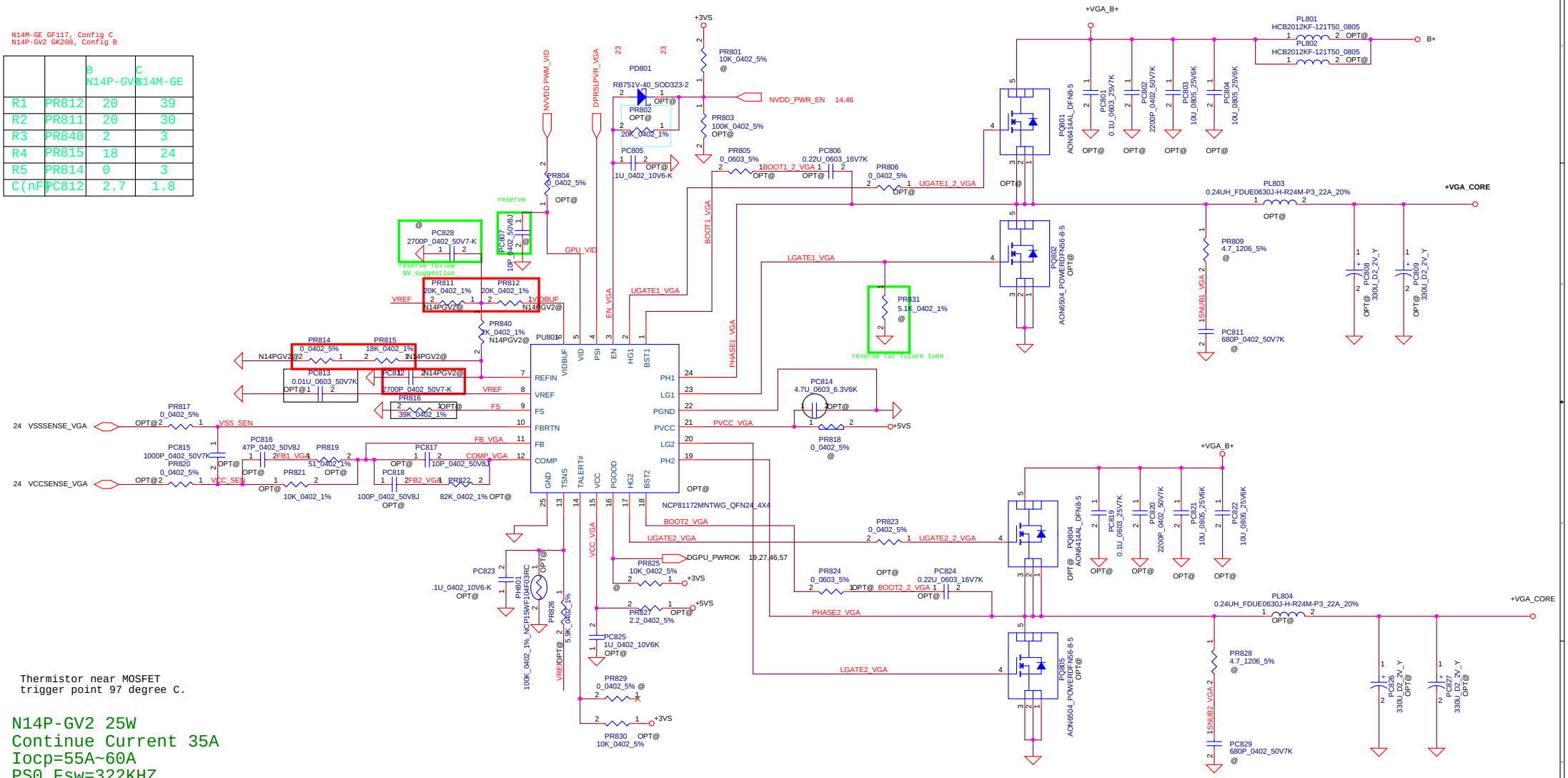


Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title	+1.05VS/+1.05VS_VGA		
Size	Document Number		Rev
Custom	401025		1.1
Date:	Friday, July 12, 2013	Sheet	57 of 61

N14M-GE GF117, Config C
N14P-GV2 GK208, Config B

		B N14P-GV	C N14M-GE
R1	PR812	20	39
R2	PR811	20	30
R3	PR840	2	3
R4	PR815	18	24
R5	PR814	0	3
C(nF)	PC812	2.7	1.8



Thermistor near MOSFET
trigger point 97 degree C.

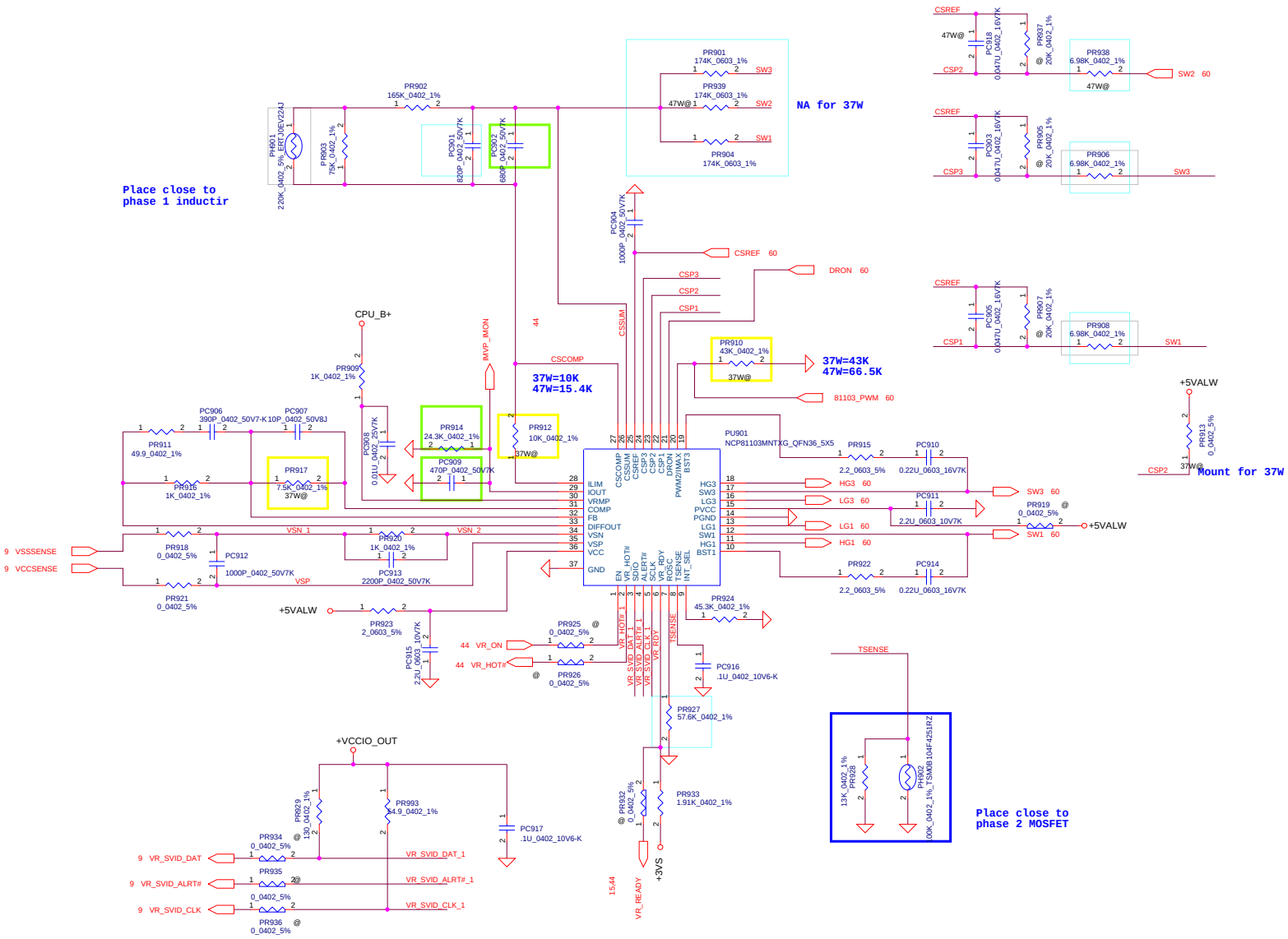
N14P-GV2 25W
Continue Current 35A
Iocp=55A~60A
PS0 Fsw=322KHZ
PS1/PS2 Fsw=475KHZ

Vboot=0.9V

Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

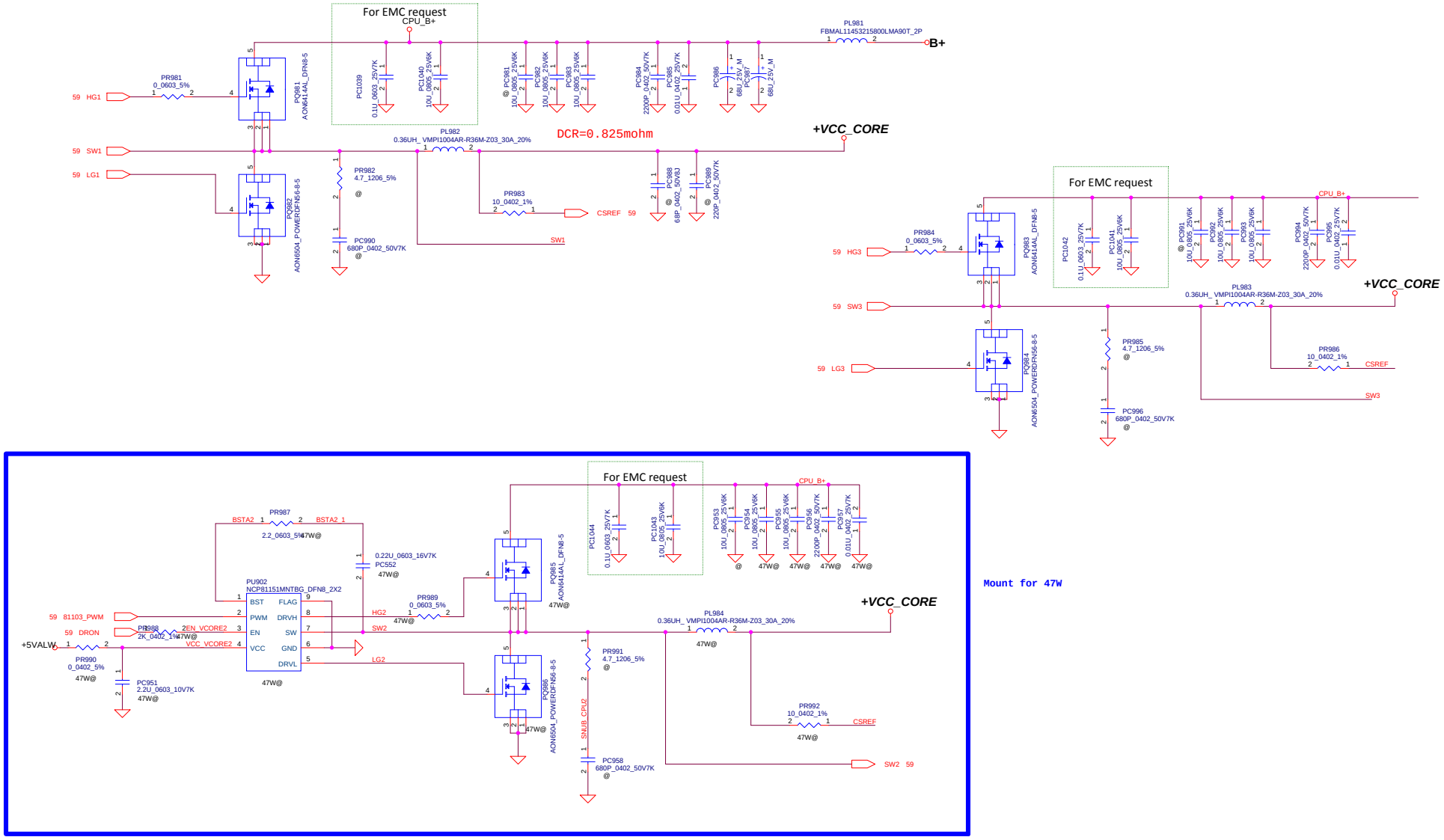
Title: VGA_CORE

Size	Document Number	Rev
Custom	401025	1.1
Date: Friday, July 12, 2013	Sheet 58 of 61	



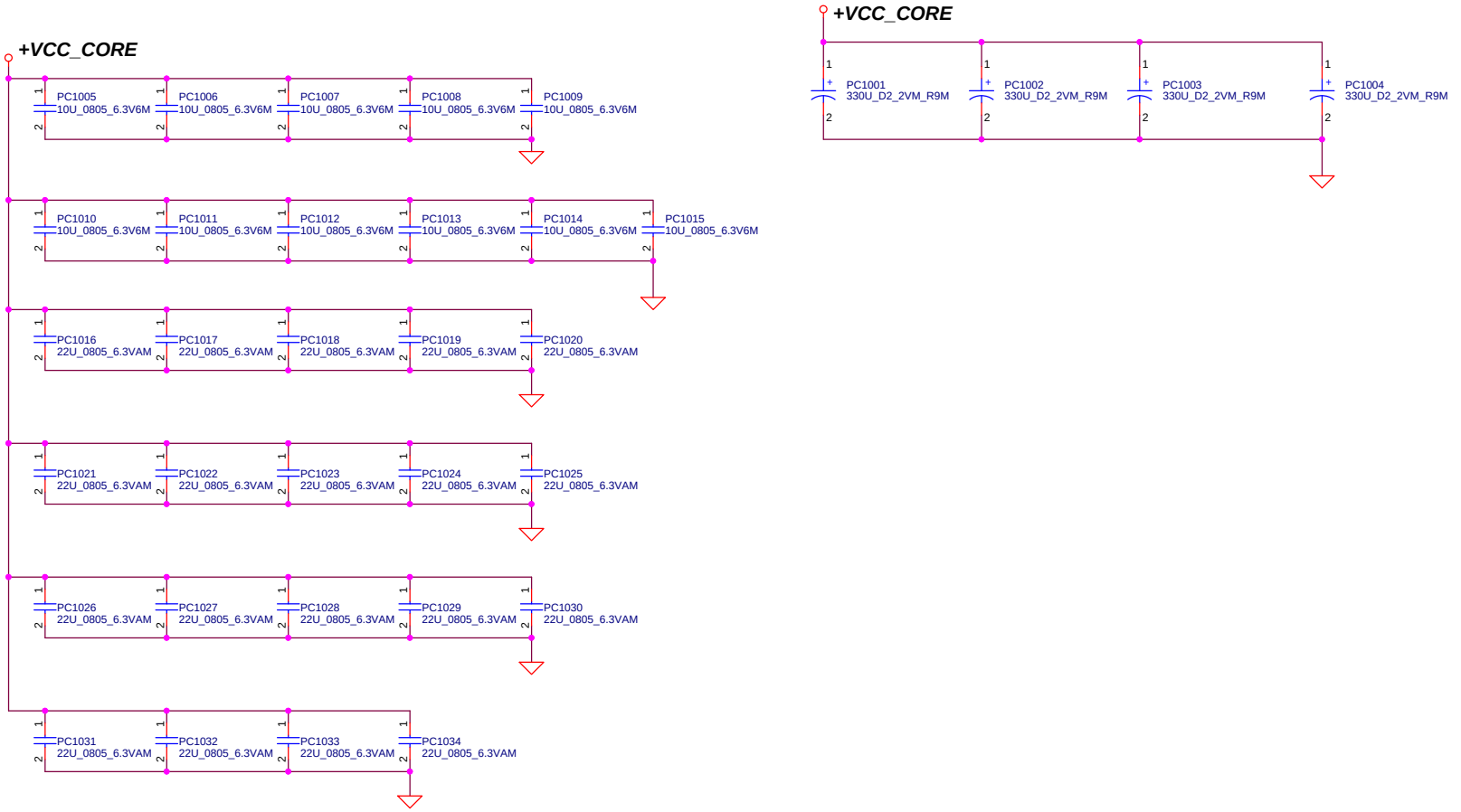
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title	CPU_CORE1
Size	C
Document Number	401025
Rev	1.1
Date:	Friday, July 12, 2013
Sheet	59 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title	CPU_CORE2		
Size	Document Number		Rev
	401025		1.1
Date:	Friday, July 12, 2013	Sheet	60 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/28	Deciphered Date	2012/12/28

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
Custom	401025	1.1

Date: Friday, July 12, 2013 Sheet 61 of 61