AMD BRAZOS
Muxless Discrete/UMA Schematics Document
AMD Ontario CPU FT1
AMD GPU Seymour XT S3
2010-12-01

REV : SA

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX
ROB:ROBSON

<Variant Name>

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Title: Cover Page

Size: A3 | Document Number: B575 | Rev: -1

Date: Friday, March 25, 2011 | Sheet 1 of 103

PROJECT CODE : 91.4PN01.001
PCB P/N : 10332
REVISION : SA

Block Diagram

LAN BD
POWER BD
CR BD
LED BD
BlueTooth MD
FPR BD

CRT 50 — RGB CRT

AMD APU
Zacate-FT1
SINGLE CHANNEL DDR3
DISPLAY PORT X2
DX11 IGP
4 X1 PCIE GEN2 GPP
1 X4 UMI-LINK GEN1
VGA DAC 4,5,6,7,8

DDR III 1066 — DDRIII DIMM1 800/1066 14
DDRIII DIMM2 800/1066 15
DP0 LVDS — LVDS 49
DP1 HDMI — HDMI 51

AMD dGPU
Seymour -XT
83,84,85,86,87
Muxless (Share PCIe x 4)
PCIe x 4 Gen 2
VRAM 88,89
gDDR3
64M*16b*4(512MB)
128Mx16b*4(1GB)

UMIx4

AMD
HUDSON-M1 FCH
PCIE GEN1 I/F (4 x 1)
USB2.0(12) + 1.1(2)
SATAII (3 PORTS)
INT. CLKGEN
AZALIA HD AUDIO
GB MAC
SPI I/F
LPC I/F
HW MONITOR
17,18,19,20,21,22

BD USB x 2
Bluetooth 63
CAMERA 49
Finger Print 64
USB2.0 x 5

PCIE x 1 — GLAN RTL8111E 31 — RJ45 CONN SB
PCIE x 1/USB2.0 x 1 — Mini-Card WLAN 65
SATA x 1/USB2.0 x 1 — Mini-Card WWAN 66 — SIM 67
USB 2.0 x 1 — MB USB x 1 62
USB 2.0 x 1/SATAII x 1 — E-SATA/USB comb 57
SATA x 2 — HDD 56, ODD 55
LPC Bus — LPC debug port 71

CardReader
Realtek
RTS5139
SB
USB2.0
SD/MMC+/MS/
MS Pro/xD SB

Azalia
CODEC
CONEXANT
CX20671
29
AZALIA
Internal DMIC
HP1
MIC IN
I/O BD
1.5W 2CH SPEAKER

KBC
NUVOTON
NPCE791G
27
SPI

Flash ROM 2MB 60
Touch PAD 69
Int. KB 69
Thermal EMC2103-2-AP 28
Fan 28

PCB STACKUP

TOP	——	L1
VCC	————	L2
S	——	L3
S	——	L4
GND	————	L5
BOTTOM	——	L6

VGA RT8208B 92

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_PWR

AMD GPU CORE TPS51218D 47

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

SYSTEM DC/DC TPS51123 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 5V_AUX_S5 3D3V_AUX_S5

TPS51218D 45

INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

DDRIII SUS TPS51218 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

RT9026 46

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3

TPS51218 46

INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

CHARGER BQ24745 40

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR

CPU DC/DC ISL6265C 42

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

GFX Core ISL6265C 45

INPUTS	OUTPUTS
DCBATOUT	VDD_NB

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Title: BLOCK DIAGRAM
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REQUIRED SYSTEM STRAPS ?

	AZ_SDOUT	PCI_CLK1	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1	LPC_CLK2
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT	Enable boot timer function
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)	Disable boot fail timer function DEFAULT

USB Table

Pair	Device
0	Internal #3(MB)
1	WLAN/WiMAX
2	WWAN
3	E-SATS/LUSB
4	BLUETOOTH
5	External #1(IO BD)
6	External #2(IO BD)
7	CAMERA(HS)
8	Finger Print
9	CardReader
10	NC
11	NC
12	NC
13	NC

PCIe Routing

	APU
LANE0	PEG
LANE1	
LANE2	
LANE3	

	FCH
LANE0	LAN
LANE1	~~WWAN~~
LANE2	WLAN
LANE3	~~CardReader~~

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

<Variant Name>

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Title: Table of Content

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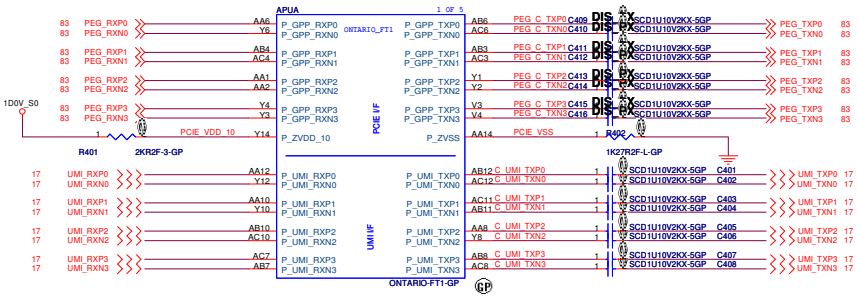

lenovo_PN_102-001093

<Core Design>

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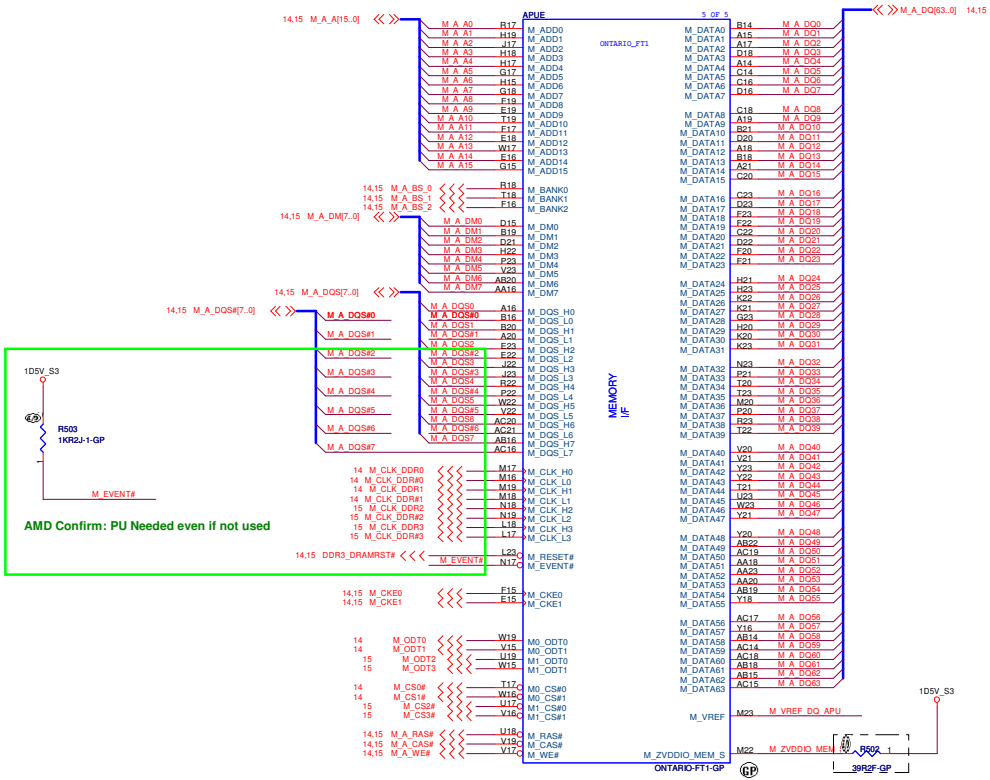
Title	APU 1 of 5(UMI/PCIE)	
Size A3	Document Number B575	Rev -1
Date: Monday, March 28, 2011	Sheet 4 of 103	



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Title: **APU 2 of 5(DDR)**

Size	Document Number	Rev
A3	B575	-1

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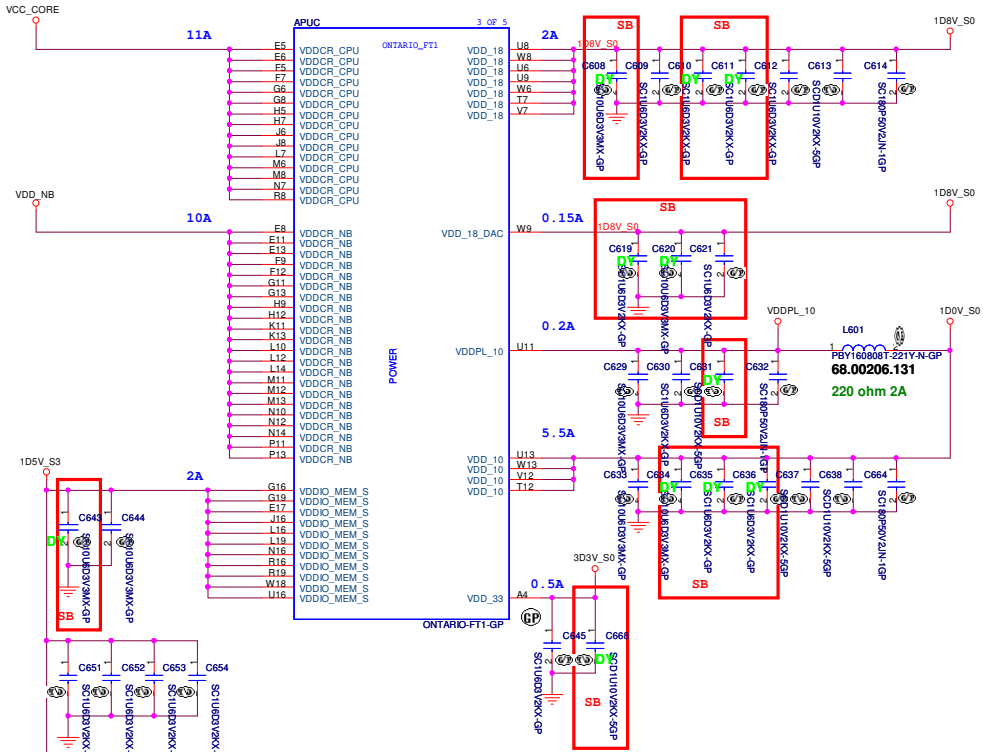

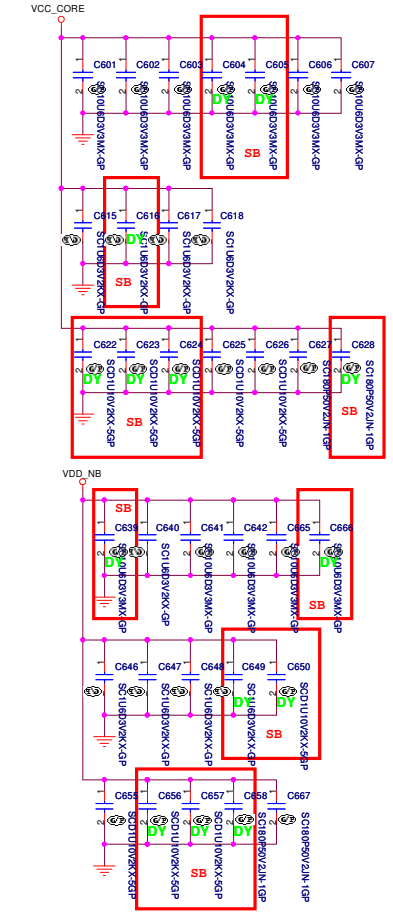

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Title: APU 3 of 5(POWER)

Size	Document Number	Rev
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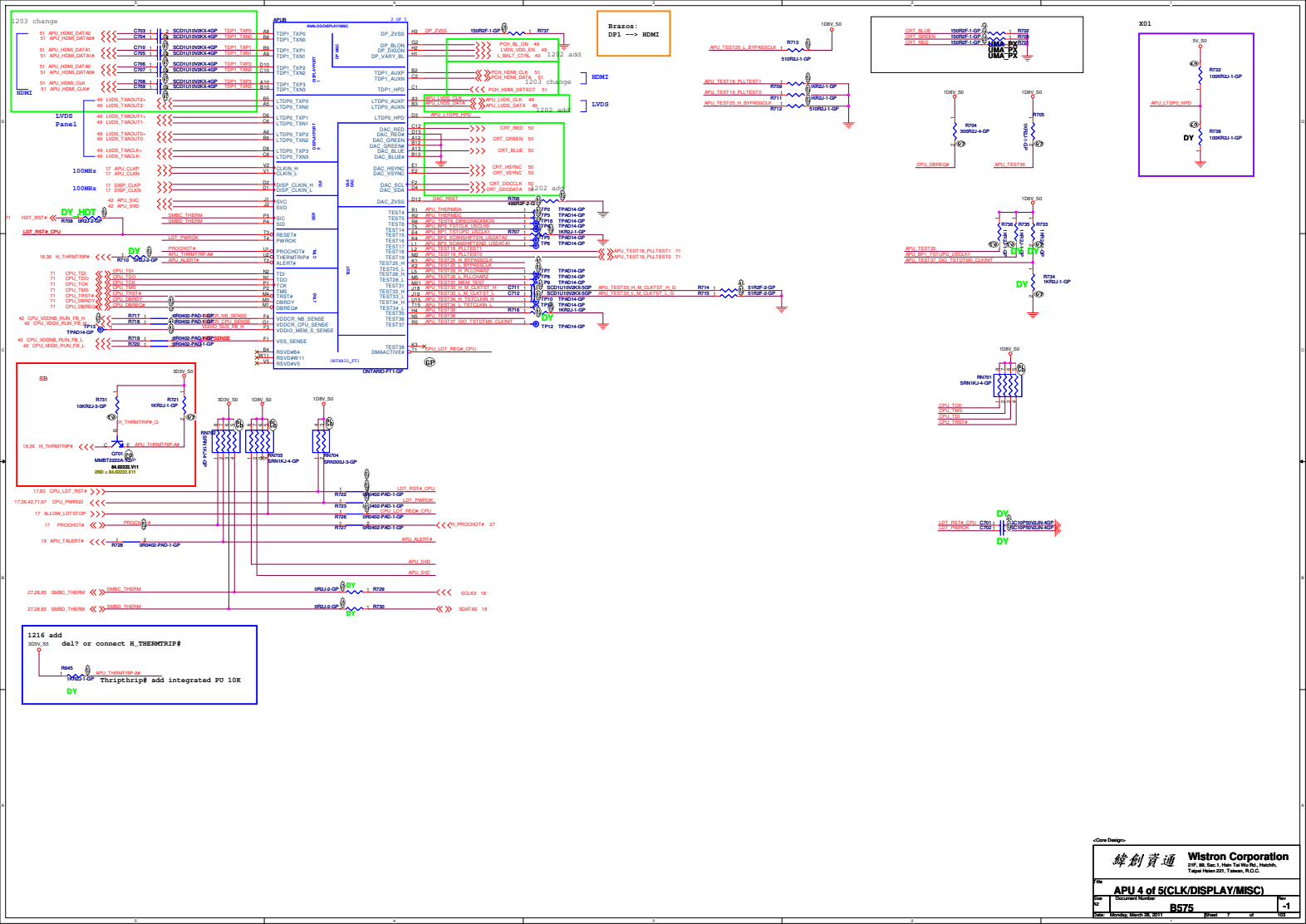
1203 change
HDMI
LVDS
Panel
100MHz
100MHz
DY_HDT
LDT_RST#_CPU
DY
TPAD14-GP
SB
1216 add
3DV_S5
del? or connect H_THERMTRIP#
Thriptrip# add integrated PU 10K
DY
Brazos:
DP1 --> HDMI
1202 add
1203 change
1202 add
1202 add
HDMI
LVDS
UMA_PX
UMA_PX
UMA_PX
X01
5V_S0
APU 4 of 5(CLK/DISPLAY/MISC)
B575
-1
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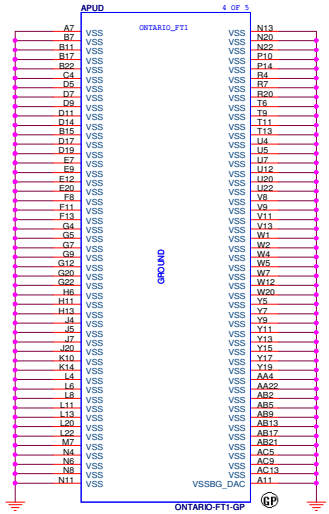
Monday, March 28, 2011



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Title: **APU 5 of 5(VSS)**

Size	Document Number	Rev
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Title: ***G-Sensor***

Size	Document Number	Rev
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Date: Friday, March 25, 2011 Sheet 9 of 103

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Title
G-Sensor

Size	Document Number	Rev
	B575	SA

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Title: ***G-Sensor***

Size	Document Number	Rev
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Date: Friday, March 25, 2011 Sheet 11 of 103

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Title
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Size	Document Number	Rev
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Title
G-Sensor

Size	Document Number	Rev
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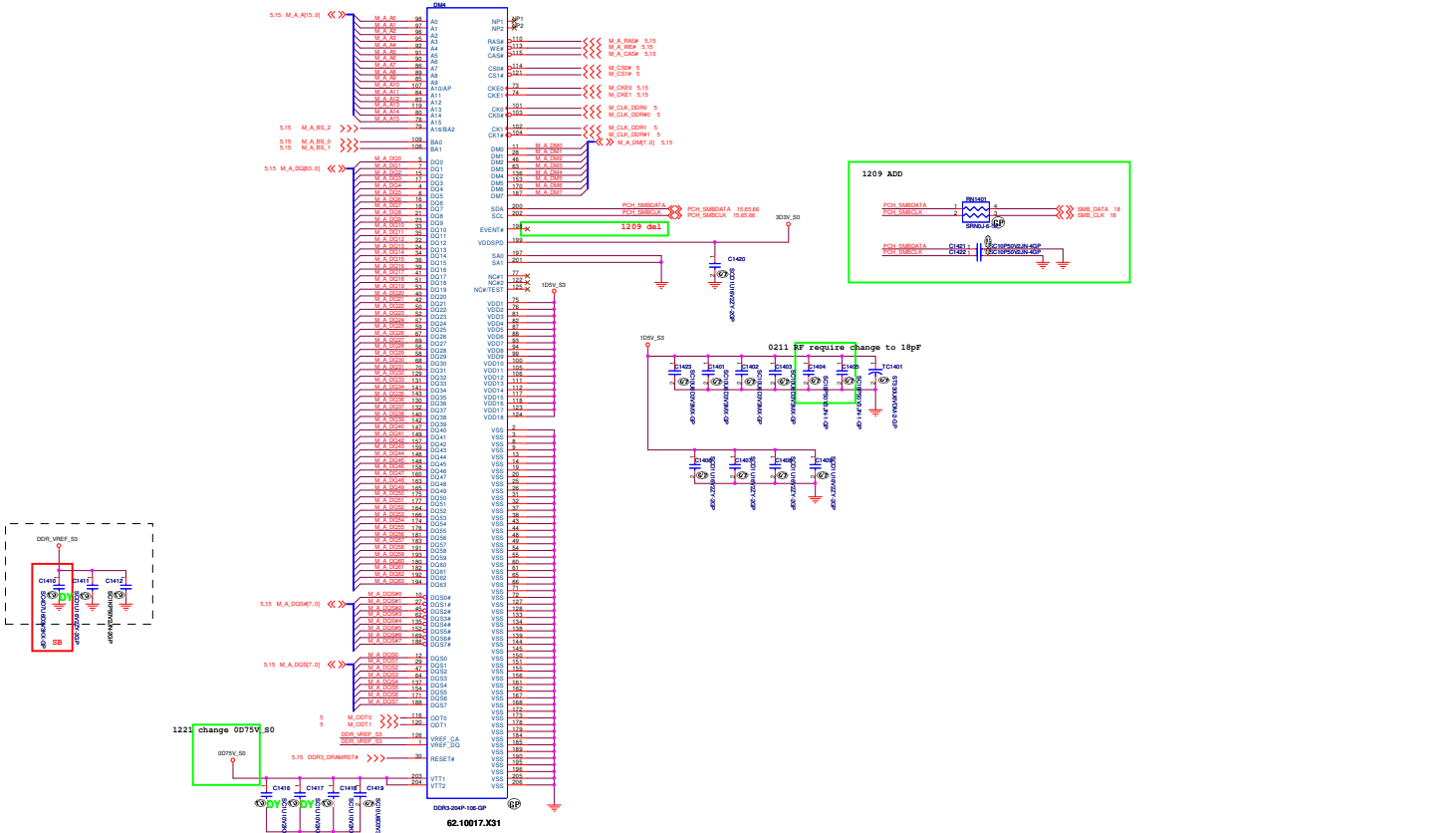
DDR3 SOCKET_1



緯創資通	Wistron Corporation		
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Title	DDR3 Socket1		
Size	Document Number	Rev	
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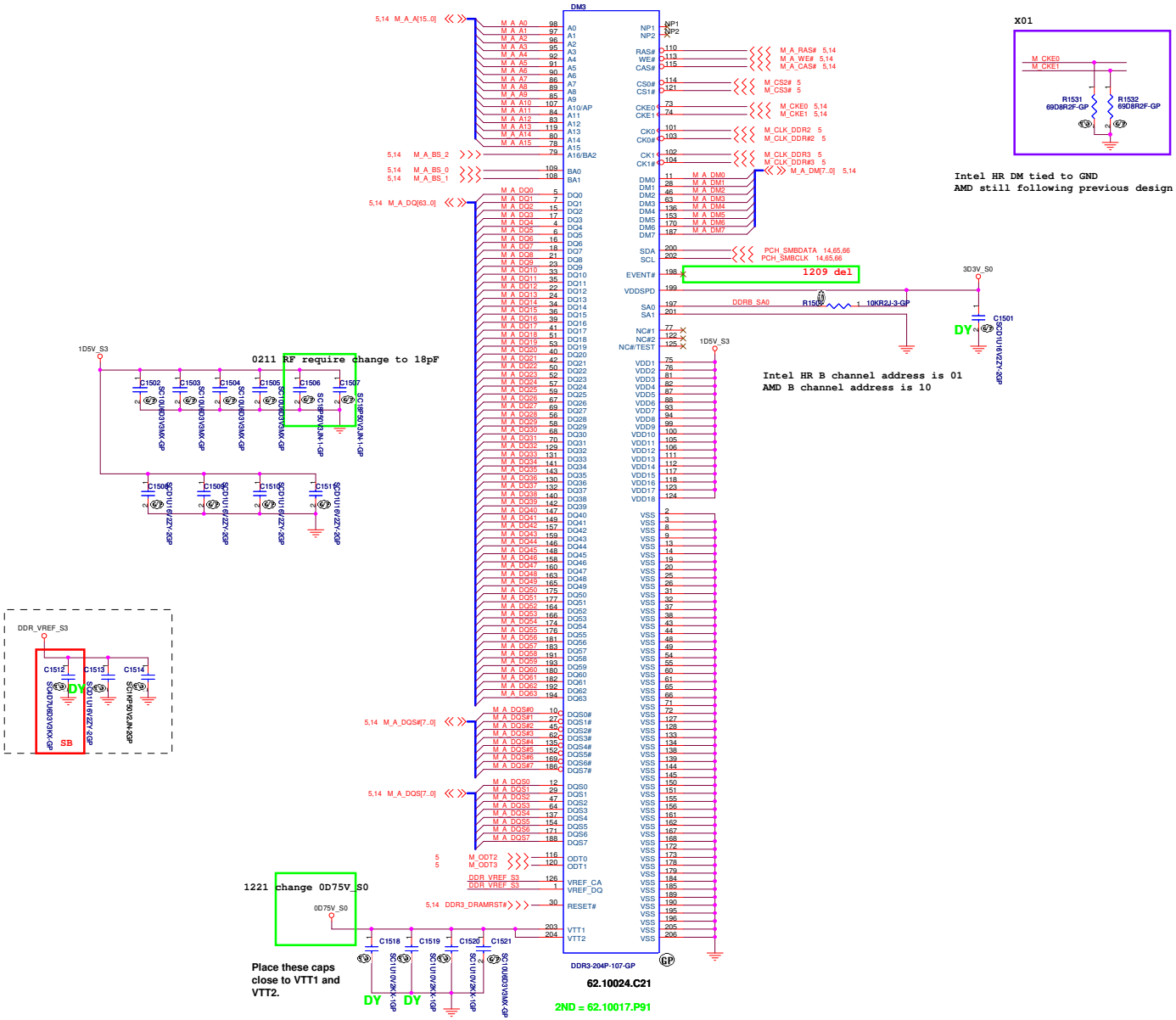
DDR3 SOCKET_2



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Title	DDR3 Socket2		
Size	Document Number		Rev
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Title

DDR3 Socket3

Size	Document Number	Rev
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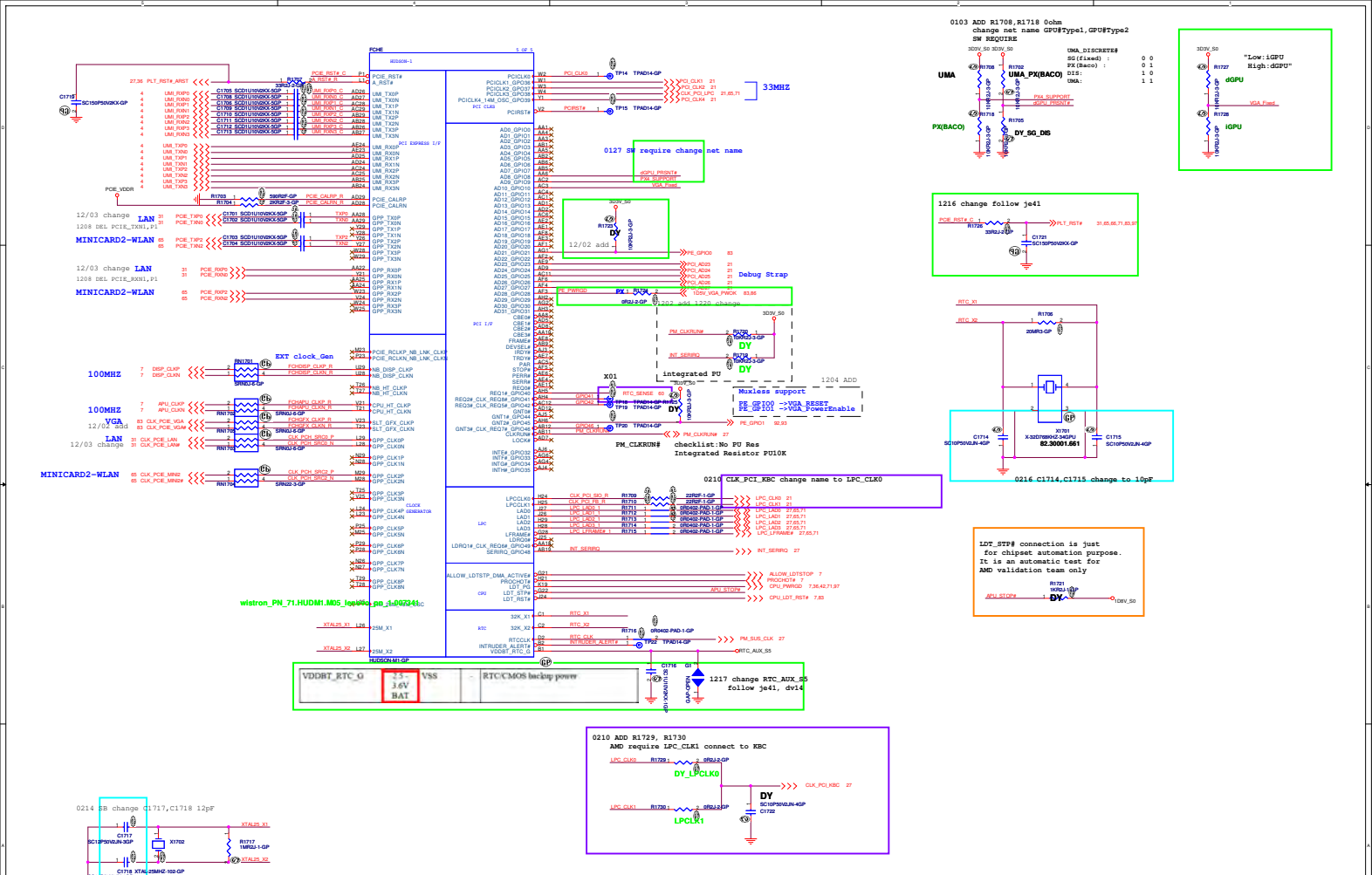

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File	FCH 1 of 6(UMI/CLK/RTC/LPC)
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1209 ADD USB_OC#0
E-SATA / USB

Sandra: Dummy
Standard: AMD recommand external PU

1208 DEL WWAN_CLKREQ#

1205 ADD
DV14 ON, JE41 DY

0318 ADD R1821 DY

0106 EMI ADD ER1810 NEAR PCH

1208 DEL PCIE_CLK_RQ1#

0214 SB ADD R1820 10Kohm PD

Sandra: 1K ohm
Standard: 0 ohm

Sandra: Mount

229 change to USB1.1

USB 1.0 Table

Pair	Device
0	Finger Print
1	NC

USB 2.0 Table

Pair	Device
0	Internal #3(MB)
1	WLAN/WiMAX
2	WWAN
3	E-SATS/LUSB
4	BLUETOOTH
5	External #1(LAN BD)
6	External #2(IO BD)
7	CAMERA(HS)
8	NC
9	CardReader
10	NC
11	NC
12	NC
13	NC

1229 SCLK2, SDATA2 PD 10K
follow dv14

SCLK2, SDATA2 if not used SMBUS or GPIO ,PD 10K

Function	Name	Integrated Resistor	External Resistor	
GA20IN	KA20GATE	8.2K PU	8.2K PU 3.3_S0	
KBRST#	KBRCIN#	8.2K PU	10K PU 3.3_S0	
PME#	EC_SCI#	10K PU	10K PU 3.3_S5	
THRIPTRIP#	PM_THRMTRIP-A#	10K PU	10K PU 3.3_S5	
PCIE_RST2#	FCH_PCIE_RST#	10K PU		?
Gevent5	MEM_Hot#	10K PU		?
Gevent6	EC_SWI#	10K PU	10K PU 3.3_S5	
WAKE#	PCIE_WAKE#	10K PU	10K PU 3.3_S5	
USB_OC0#	USB_OC#0	10K PU		
USB_OC1#	USB_OC#1	10K PU		
USB_OC2#	USB_OC#2	10K PU		
Gevent15#	USB_OC#3	10K PU		
Gevent16#	USB_OC#4	10K PU		
USB_OC5#	USB_OC#5	10K PU		
USB_OC7#	USB_OC#7	10K PU		
IPC_SMI#	EC_SMI#	8.2K PU	10K PU 3.3_S0	
SERIRQ	INT_SERIRQ	8.2K PU	10K PU 3.3_S0	DY
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2K PU		
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2K PU		
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2K PU		
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2K PU		
CLK_REQG	PEG_CLKREQ#	8.2K PU		

DVT 1ST

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FCH 2 of 6(USB/HDA/GPIO)

Size: A2 | Document Number: B575 | Rev: SA

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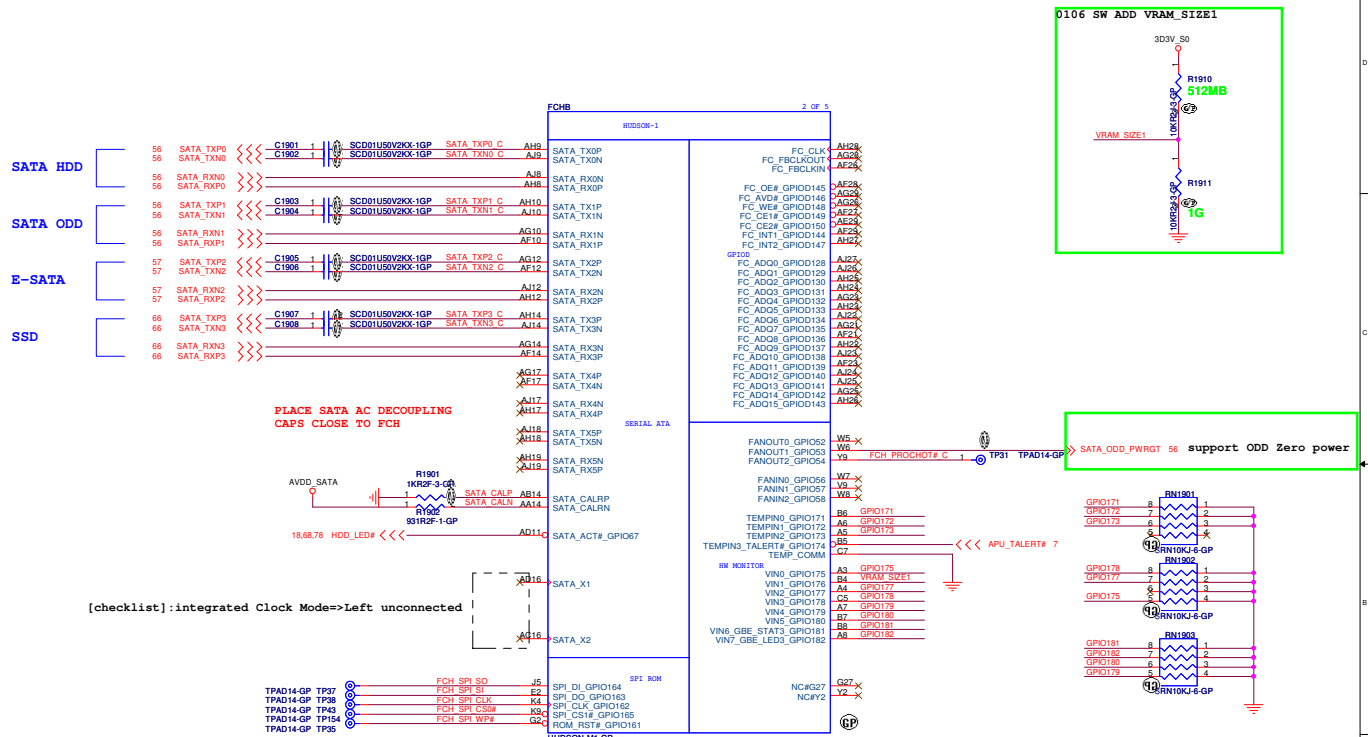

DVT 1ST

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Title: FCH 2 of 6(USB/HDA/GPIO)		
Size: A3	Document Number: B575	Rev: SA
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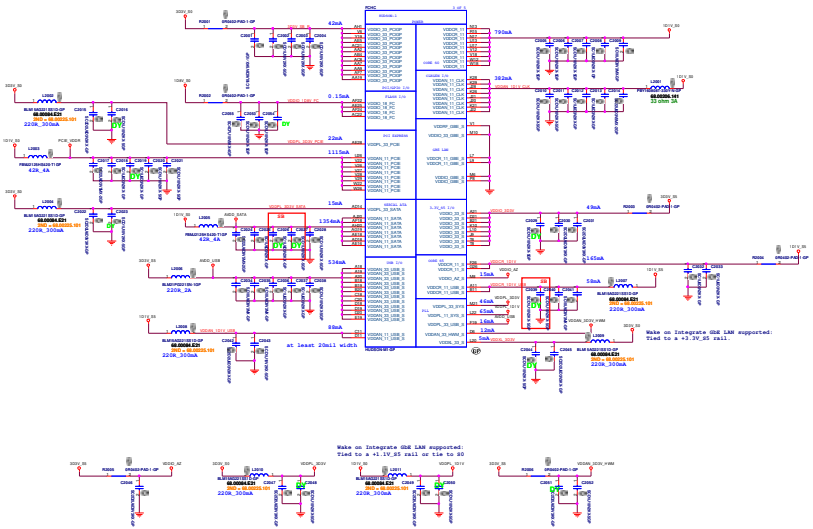

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FCH 4 of 6(PWR)

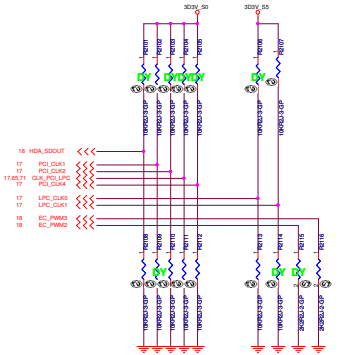
B575

8A

SSID = S.B

REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5
checklist:PU 3.3V_S5
confrim by AMD,following CRB suggestion



REQUIRED SYSTEM STRAPS

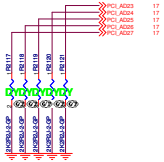
	AZ_SDOUT (ACZ_SDATAOUT_1)	PCI_CLK1	PCI_CLK2	PCI_CLK3 (CLK_PCI_LPC)	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	Low Power Mode	Allow PCIE GEN2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	Performance Mode DEFAULT	Force PCIE GEN1	Watchdog Timer Disabled DEFAULT	iGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USE this pin to determine INT/EXT CLK

TYPE ENABLED	EC_PWM2	EC_PWM3
Reserved	2.2-kohm 5% pull-down	2.2-kohm 5% pull-down
LPC ROM	Not connected.	2.2-kohm 5% pull-down
SPI ROM	2.2-kohm 5% pull-down	Not connected.
Reserved	Not connected.	Not connected.

Note: EC_PWM2, EC_PWM3 default have internal 10kohm PU.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

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Title: FCH 5 of 6(STRAPPINGS)

Size	Document Number	Rev
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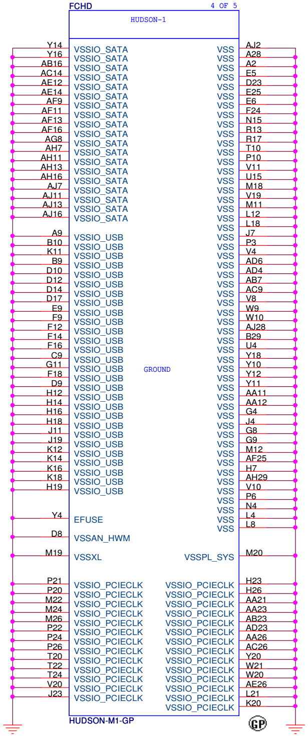

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Title	**FCH 6 of 6(VSS)**	
Size A3	Document Number **B575**	Rev **SA**
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Title: ***G-Sensor***

Size	Document Number	Rev
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Title: ***G-Sensor***

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Date: Friday, March 25, 2011 Sheet 24 of 103

<Core Design>

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Title
G-Sensor

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Title: Power Button

Size	Document Number	Rev
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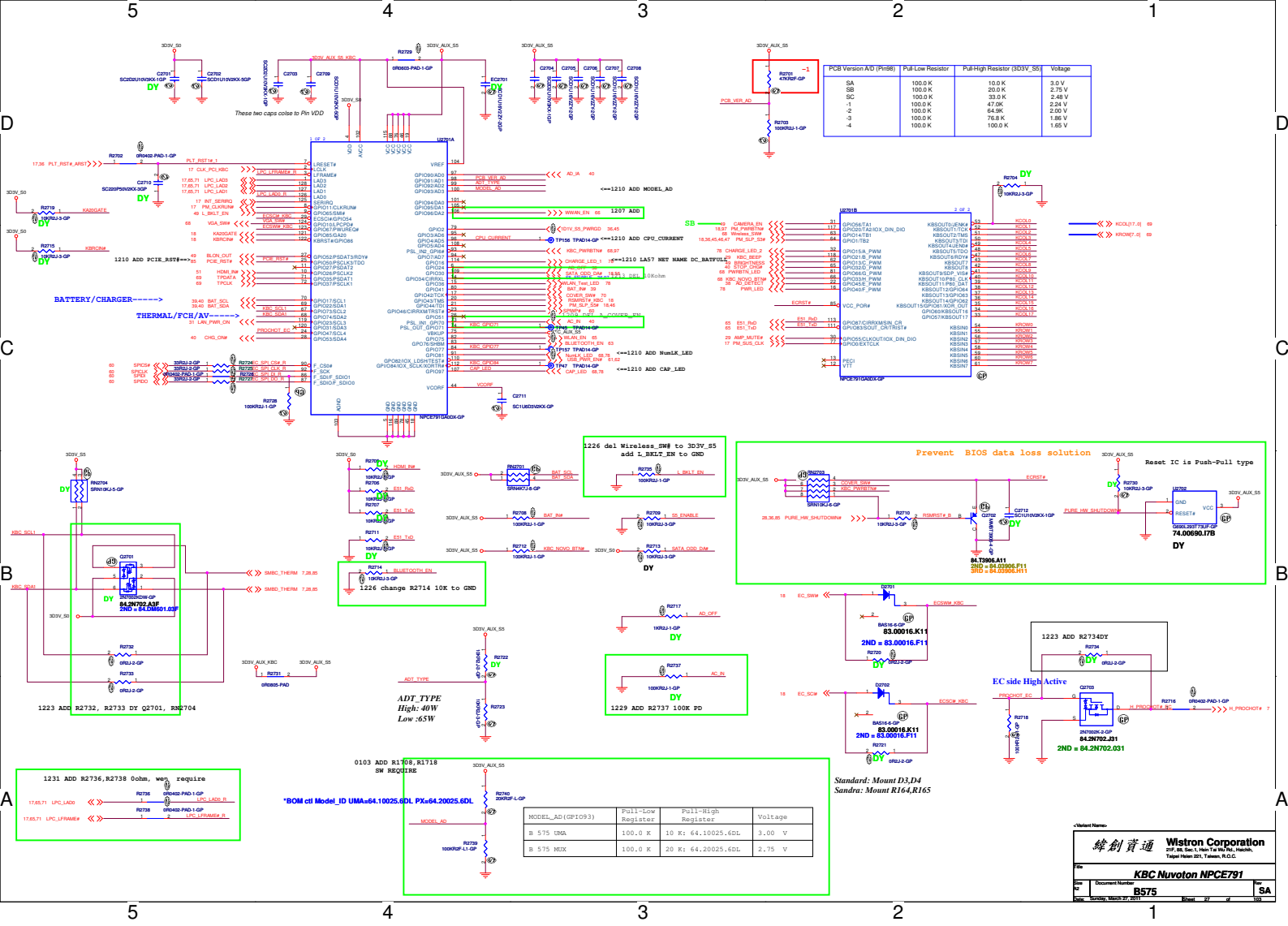
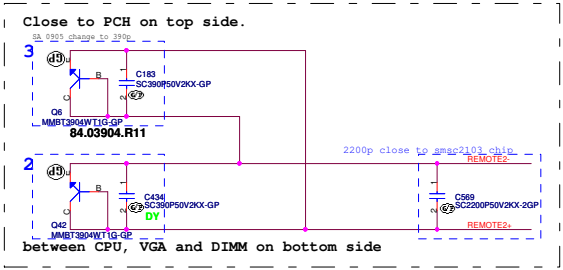
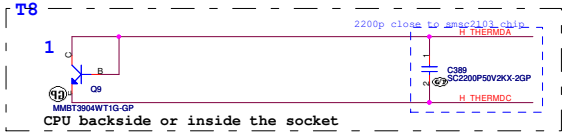

PCB Version A/D (Pin98) | Pull-Low Resistor | Pull-High Resistor (3D3V_S5) | Voltage
SA | 100.0 K | 10.0 K | 3.0 V
SB | 100.0 K | 20.0 K | 2.75 V
SC | 100.0 K | 33.0 K | 2.48 V
-1 | 100.0 K | 47.0K | 2.24 V
-2 | 100.0 K | 64.9K | 2.00 V
-3 | 100.0 K | 76.8 K | 1.86 V
-4 | 100.0 K | 100.0 K | 1.65 V
These two caps colse to Pin VDD
1210 ADD PCIE_RST#==>
BATTERY/CHARGER
THERMAL/FCH/AV
<=1210 ADD MODEL_AD
1207 ADD
<=1210 ADD CPU_CURRENT
<=1210 LA57 NET NAME DC_BATFULL
<=1210 ADD NumLK_LED
<=1210 ADD CAP_LED
SB
Prevent BIOS data loss solution
Reset IC is Push-Pull type
1226 del Wireless_SW# to 3D3V_S5
add L_SKLT_EN to GND
1226 change R2714 10K to GND
ADT_TYPE
High: 40W
Low :65W
1223 ADD R2732, R2733 DY Q2701, RN2704
1223 ADD R2734DY
EC side High Active
1229 ADD R2737 100K PD
1231 ADD R2736,R2738 0ohm, we require
0103 ADD R1708,R1718
SW REQUIRE
*BOM ctl Model_ID UMA=64.10025.6DL PXe64.20025.6DL
Standard: Mount D3,D4
Sandra: Mount R164,R165
MODEL_AD(GPIO93) | Pull-Low Register | Pull-High Register | Voltage
B 575 UMA | 100.0 K | 10 K: 64.10025.6DL | 3.00 V
B 575 MUX | 100.0 K | 20 K: 64.20025.6DL | 2.75 V
緯創資通 Wistron Corporation
KBC Nuvoton NPCE791
B575
SA
Sunday, March 27, 2011

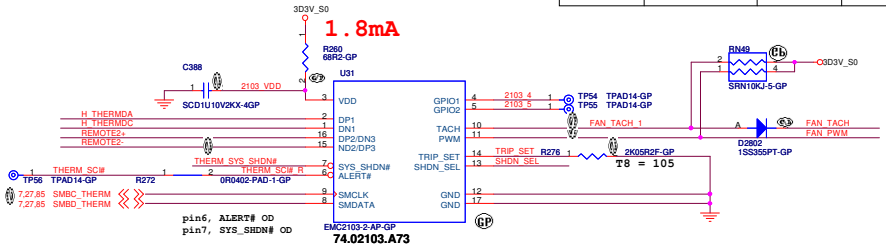


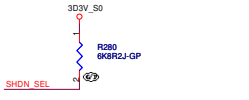


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

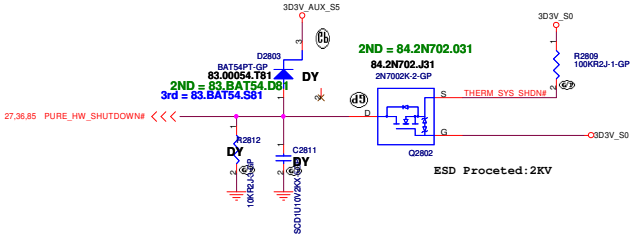
Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11

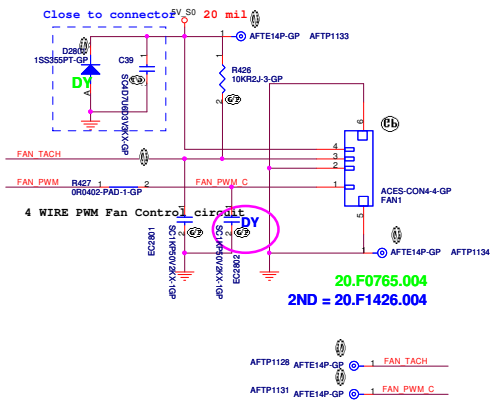




SHDN --> 2N3904 ON External diode



ESD Proceted:2KV



1210 10886-1 D1/D2/R15/R16/C15 DY
EC1/EC2/EC3 100pF
R17/R18 100ohm
C17/C18 100pF
R23/R24 100pF
BOM Control

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

Port Configuration

Port A: Headphone jack
Port B:
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Internal stereo digital mic

Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

1210 ADD 5.1 ohm

Please see Design Guide for audio grounding.

1209 ADD 2pcs 0805 short pad

place them under CODEC bottom

Place EMI components close to audio codec.

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LA57 UMA

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Title: ***reserved***

Size	Document Number	Rev
A4	B575	SA

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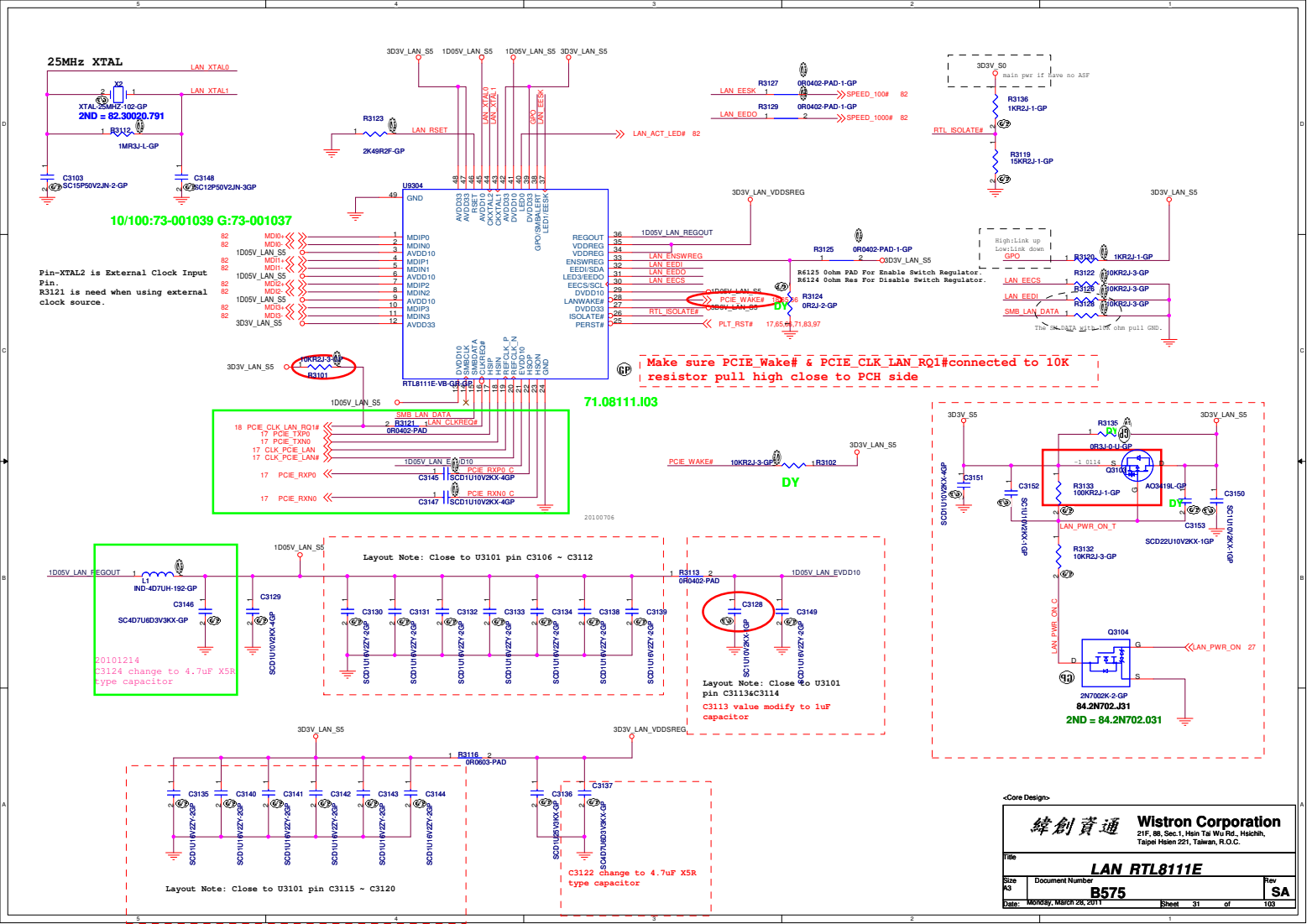

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Title: LAN_RTL8111E

Size	Document Number	Rev
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<Core Design>

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Title

RTS5159 (CARD READER)

Size	Document Number	Rev
A3	**B575**	**SA**

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<Core Design>

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Title: ***Reserved***

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A4	B575	SA

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Title: ***Reserved***

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<Core Design>

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Title

USB3.0

Size	Document Number	Rev
Custom	B575	SA

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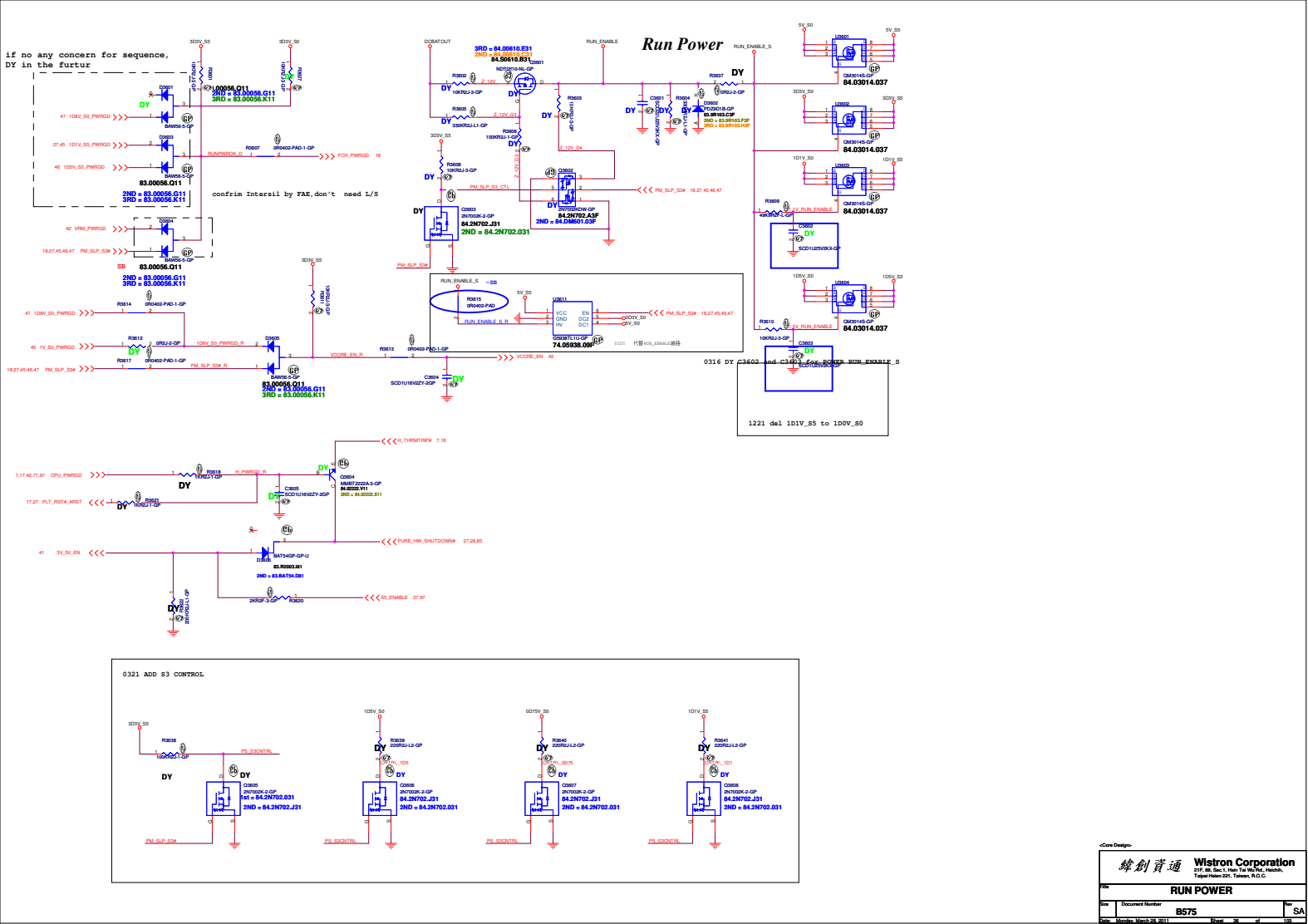

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Title	RUN POWER	
Size	Document Number	Rev
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Title
G-Sensor

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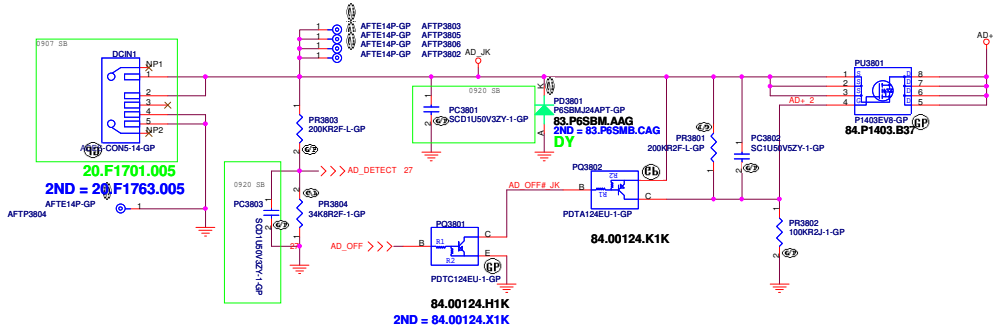
Adaptor in to generate DCBATOUT



JV10-CS

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Title: *DCIN_JACK*		
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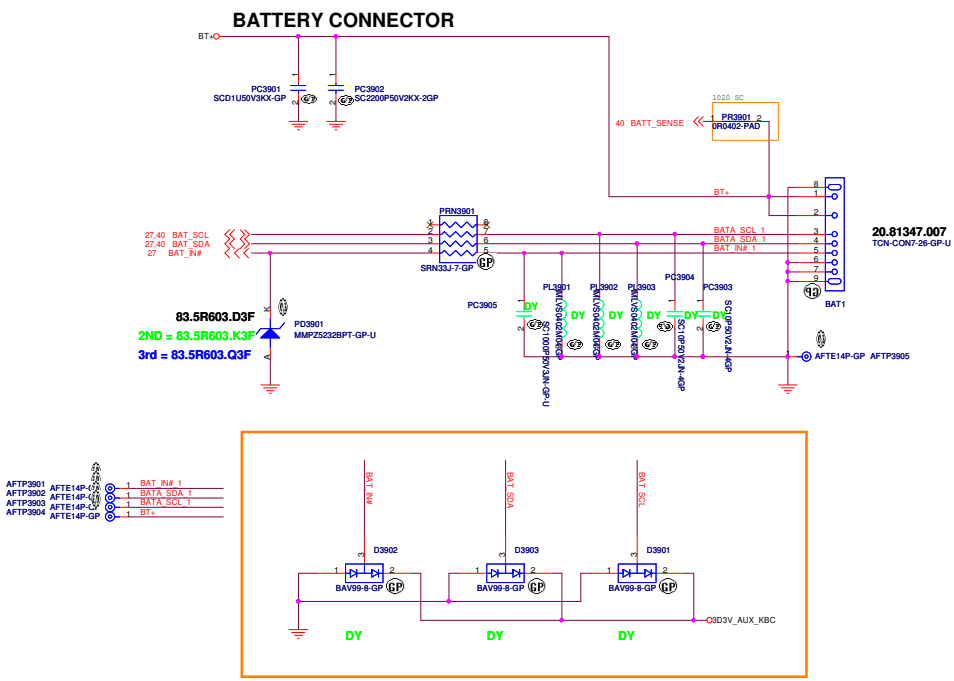

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緯創資通 **Wistron Corporation**

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Title: **AD / BATT CONN**

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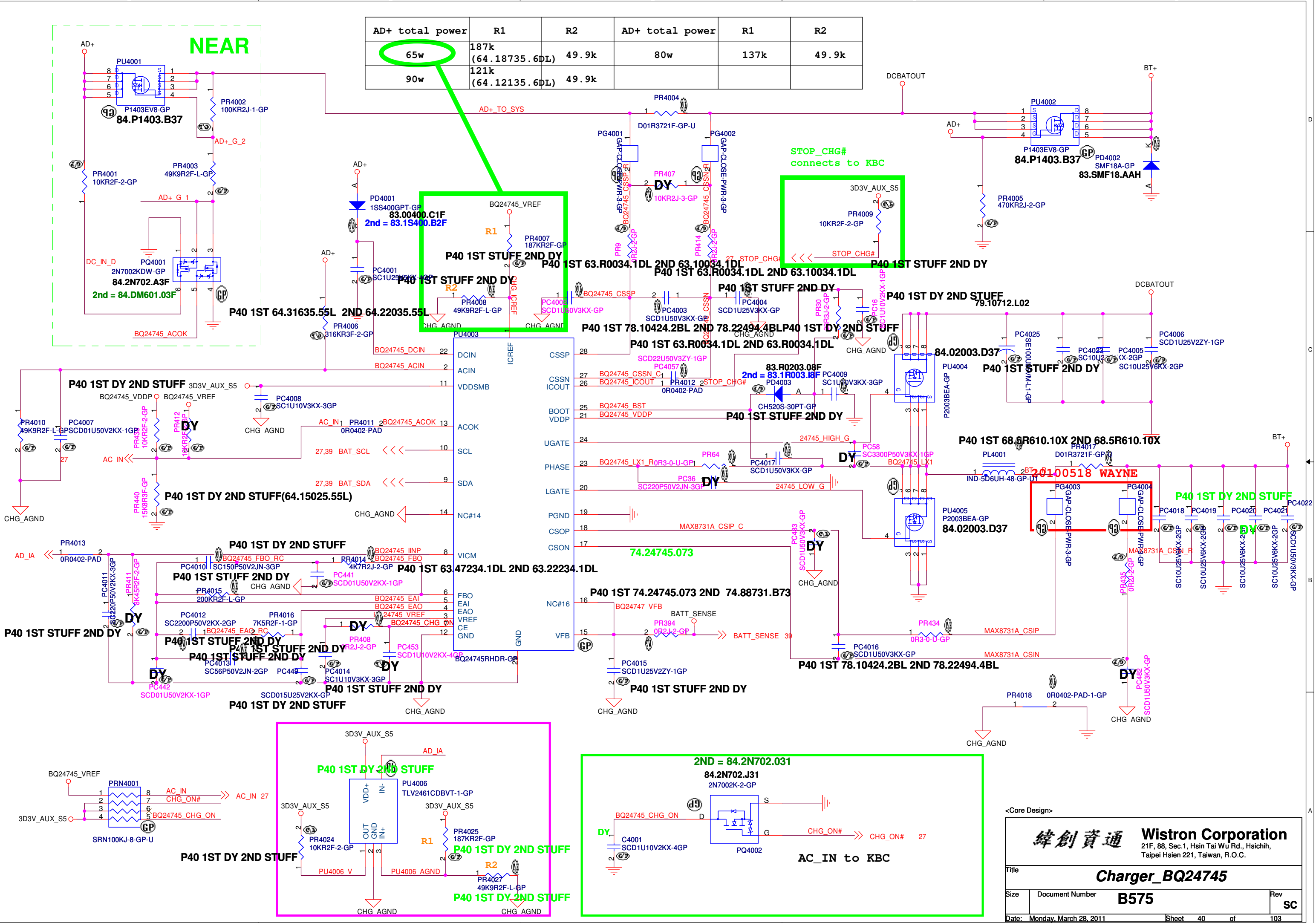
AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k			



NEAR
PU4001
P1403EV8-GP
84.P1403.B37
PR4002
100KR2J-1-GP
AD+_G_2
PR4001
10KR2F-2-GP
PR4003
49K9R2F-L-GP
AD+_G_1
DC_IN_D
PQ4001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
BQ24745_ACOK
AD+_TO_SYS
PD4001
1SS400GPT-GP
83.00400.C1F
2nd = 83.1S400.B2F
PC4001
BQ24745_VREF
PR4007
187KR2F-GP
PR4008
49K9R2F-L-GP
P40 1ST STUFF 2ND DY
P40 1ST 64.31635.55L 2ND 64.22035.55L
PR4006
316KR3F-2-GP
PR4004
D01R3721F-GP-U
PG4001
PG4002
PR407
10KR2J-3-GP
P40 1ST 63.R0034.1DL 2ND 63.10034.1DL
STOP_CHG#
connects to KBC
3D3V_AUX_S5
PR4009
10KR2F-2-GP
STOP_CHG#
DCBATOUT
PU4002
P1403EV8-GP
84.P1403.B37
PD4002
SMF18A-GP
83.SMF18.AAH
PR4005
470KR2J-2-GP
BT+
PU4003
BQ24745RHDR-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ICREF
PC4003
SCD1U50V3KX-GP
PC4004
SCD1U25V3KX-GP
P40 1ST 78.10424.2BL 2ND 78.22494.4BL
P40 1ST 63.R0034.1DL 2ND 63.R0034.1DL
P40 1ST DY 2ND STUFF
79.10712.L02
PC4025
PC4023
PC4005
PC4006
SCD1U25V2ZY-1GP
PU4004
P2003BEA-GP
84.02003.D37
PD4003
CH520S-30PT-GP
83.R0203.08F
2nd = 83.1R003.18F
PC4009
PR4012
0R0402-PAD
P40 1ST 68.6R610.10X 2ND 68.5R610.10X
PL4001
IND-5D6UH-48-GP-U1
PR4017
D01R3721F-GP
20100518 WAYNE
PG4003
PG4004
GAP-CLOSE-PWR-3-GP
PU4005
P2003BEA-GP
84.02003.D37
PC4018
PC4019
PC4020
PC4021
PC4022
74.24745.073
P40 1ST 63.47234.1DL 2ND 63.22234.1DL
P40 1ST 74.24745.073 2ND 74.88731.B73
BATT_SENSE
PR394
PR434
MAX8731A_CSIP
MAX8731A_CSIN
PC4016
SCD1U50V3KX-GP
PC4015
SCD1U25V2ZY-1GP
PR4018
0R0402-PAD-1-GP
CHG_AGND
AD_IA
PR4013
0R0402-PAD
PR4010
49K9R2F-L-GP
PC4007
SCD01U50V2KX-1GP
PC4008
SC1U10V3KX-3GP
PR4011
0R0402-PAD
27,39 BAT_SCL
27,39 BAT_SDA
P40 1ST DY 2ND STUFF(64.15025.55L)
PR440
15K8R3F-GP
PC4010
SC150P50V2JN-3GP
PR4014
4K7R2J-2-GP
PR4015
200KR2F-L-GP
PC4012
SC2200P50V2KX-2GP
PR4016
7K5R2F-1-GP
PC4013
SC56P50V2JN-2GP
PC4014
SC1U10V3KX-3GP
PC442
SCD01U50V2KX-1GP
PC4011
SC220P50V2JN-3GP
3D3V_AUX_S5
AD_IA
PU4006
TLV2461CDBVT-1-GP
PR4024
10KR2F-2-GP
PR4025
187KR2F-GP
PR4027
49K9R2F-L-GP
PU4006_V
PU4006_AGND
BQ24745_VREF
PRN4001
SRN100KJ-8-GP-U
AC_IN
CHG_ON#
BQ24745_CHG_ON
AC_IN 27
2ND = 84.2N702.031
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PQ4002
C4001
SCD1U10V2KX-4GP
CHG_ON# 27
AC_IN to KBC

<Core Design>

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Title: **Charger_BQ24745**

Size | Document Number: **B575** | Rev: SC

Date: Monday, March 28, 2011 | Sheet 40 of 103

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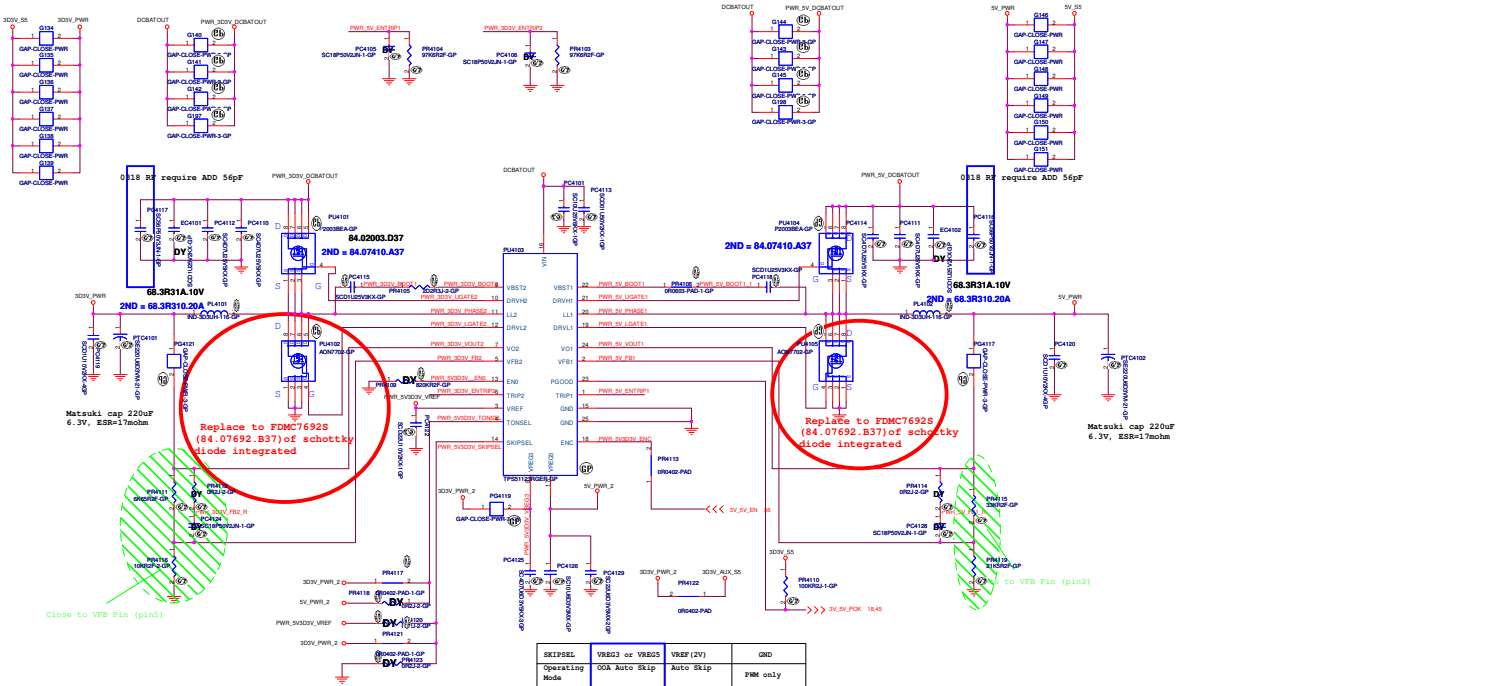

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

<Core Design>
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DC/DC 3D3V5V

Size	Document Number	Rev
	B575	SA

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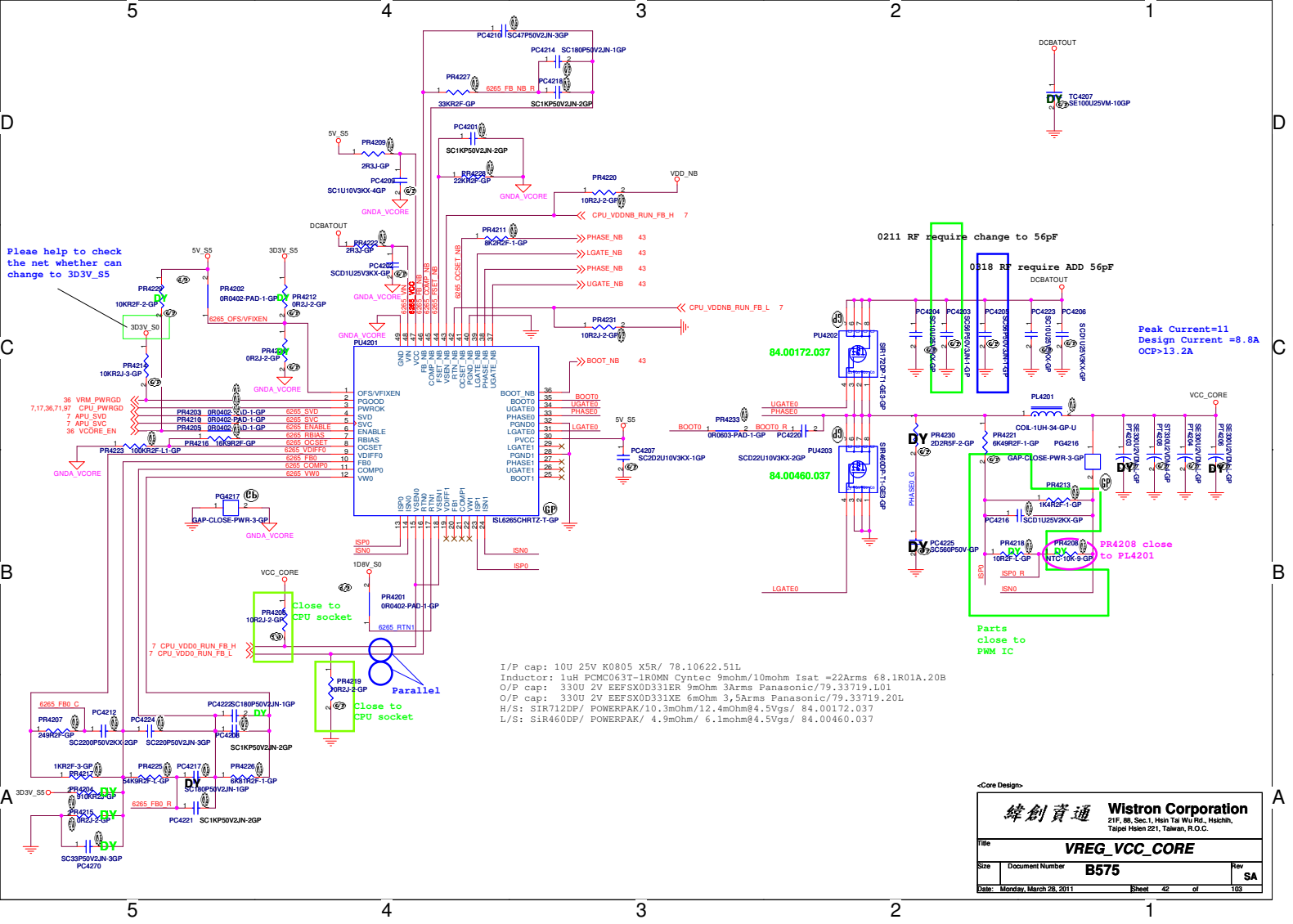

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Title	VREG_VCC_CORE		
Size	Document Number B575		Rev SA
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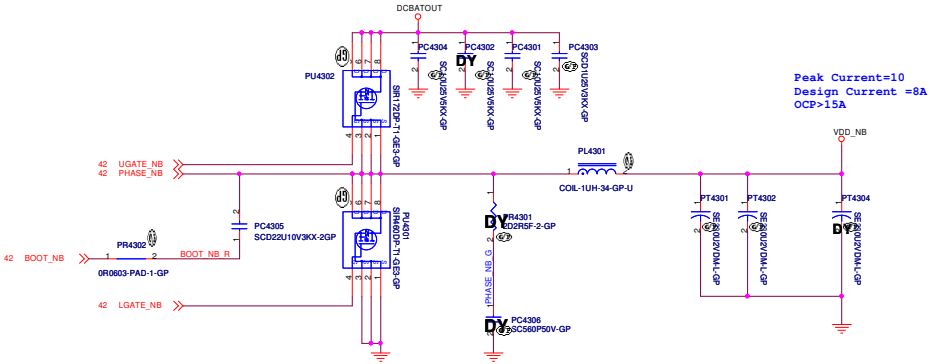

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1uH PCMC063T-1R0MN Cyntec 9mohm/10mohm Isat =22Arms 68.1R01A.20B
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR712DP/ POWERPAK/10.3mOhm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP/ POWERPAK/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

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Title	VREG_VDDNB		
Size	Document Number B575		Rev SA
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Title

Size	Document Number	Rev
	B575	SA

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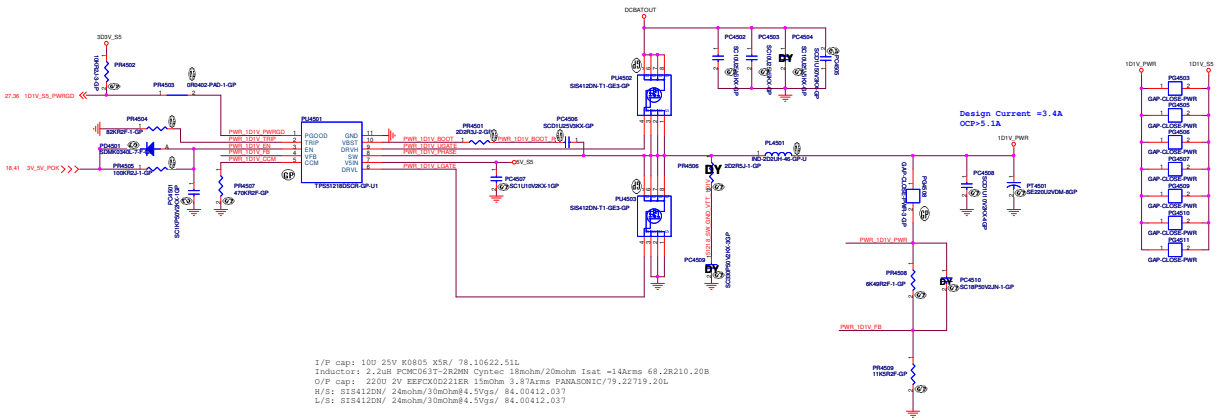

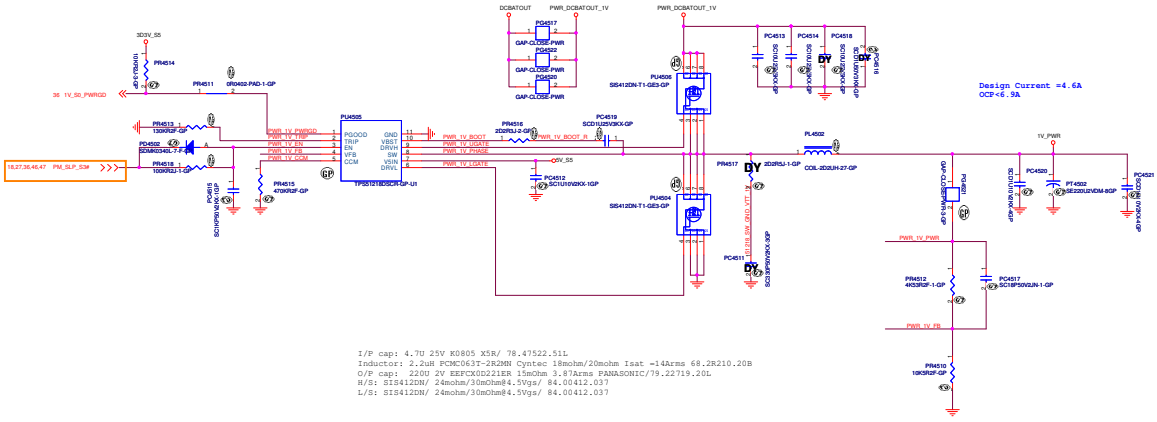

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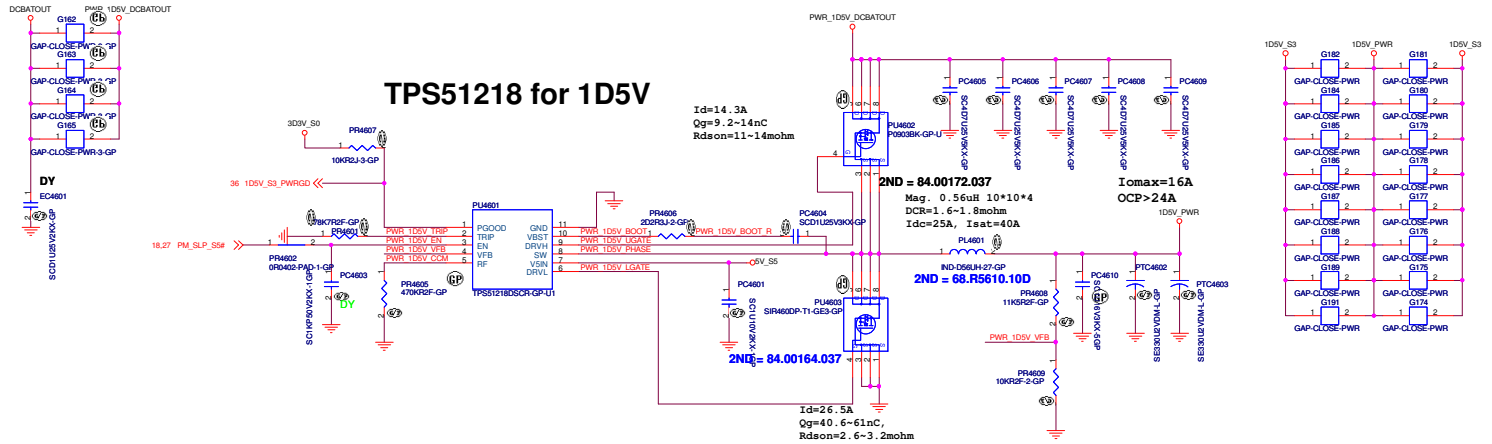
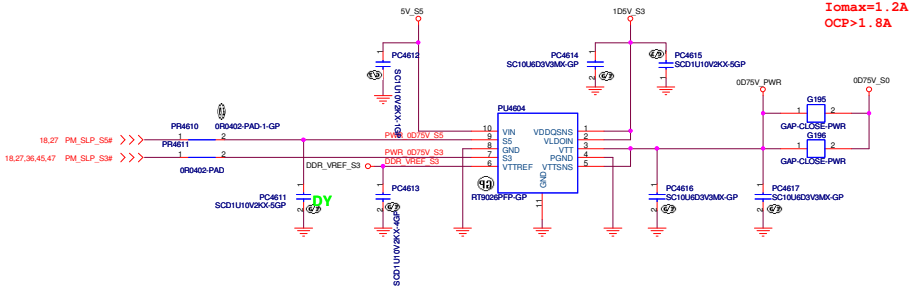
Size	Document Number: B575	Rev: SA
Date: Monday, March 28, 2011	Sheet 45 of 103	





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Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		SA

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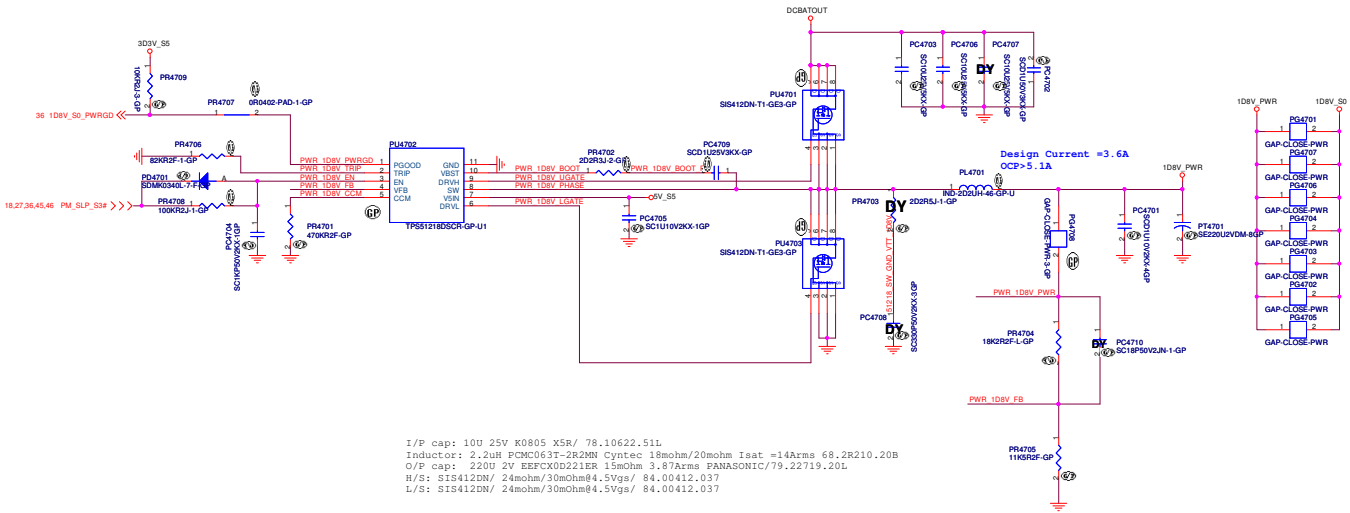

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	TPS51218_1D8V_S0	
Size	Document Number B575	Rev SA
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Title
G-Sensor

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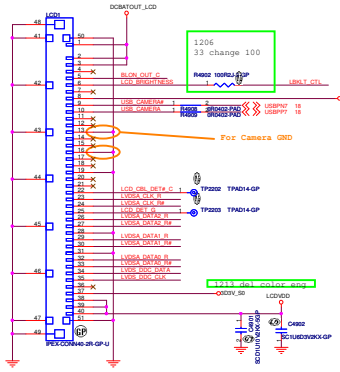
SSID = VIDEO

LVDS CONNECTOR



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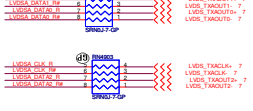
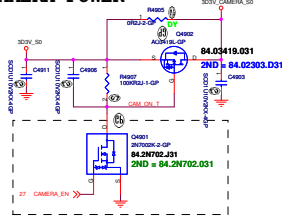


CAMERA POWER



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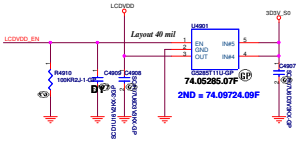
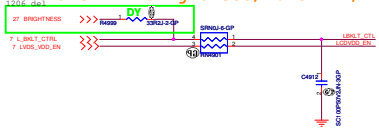
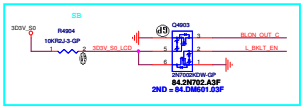
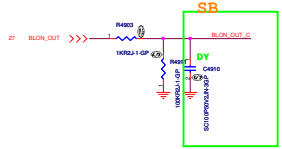


Panel BL brightness/Power En/BL En





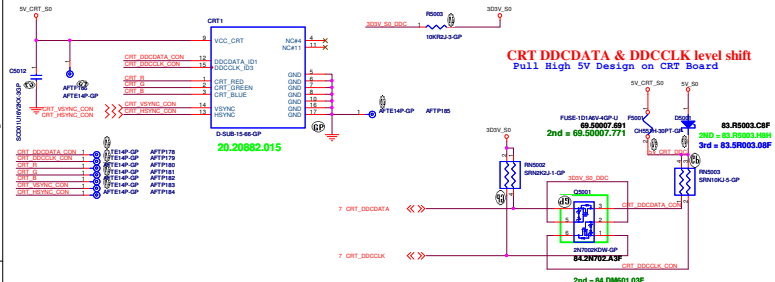


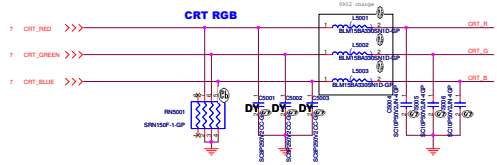
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

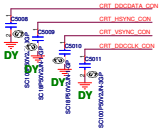
Size	Document Number	Rev
A2	B575	SA

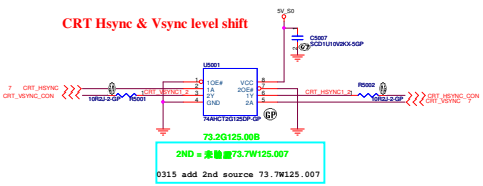
Date: Monday, March 28, 2011 Sheet 49 of 103





Pull high 在CRT





<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN

Size	Document Number	Rev
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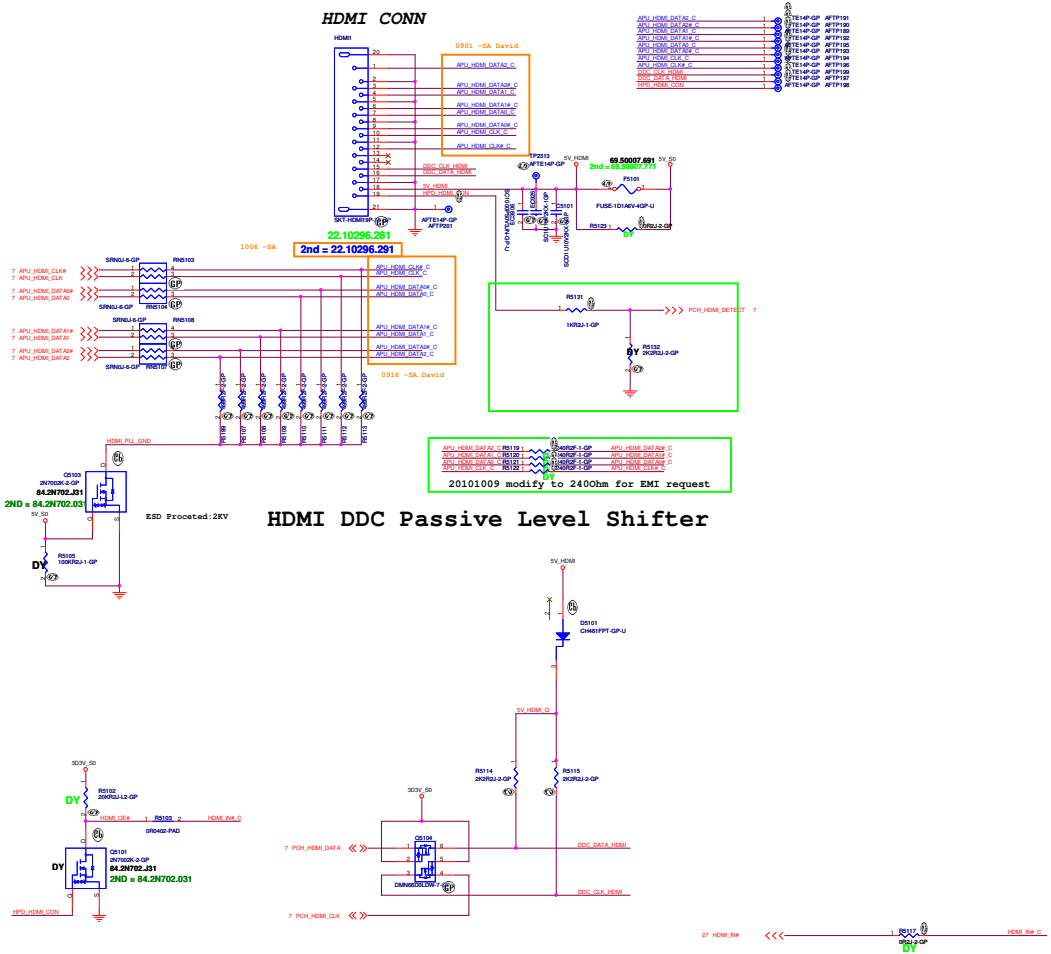
HDMI Level Shifter & CONNECTOR



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter / Conn

Size: A2 | Document Number: B575 | Rev: SA

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size	Document Number	Rev
A4	B575	SA

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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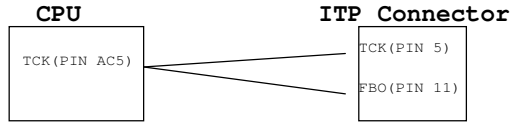
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP

Size: A4 | Document Number: B575 | Rev: SA

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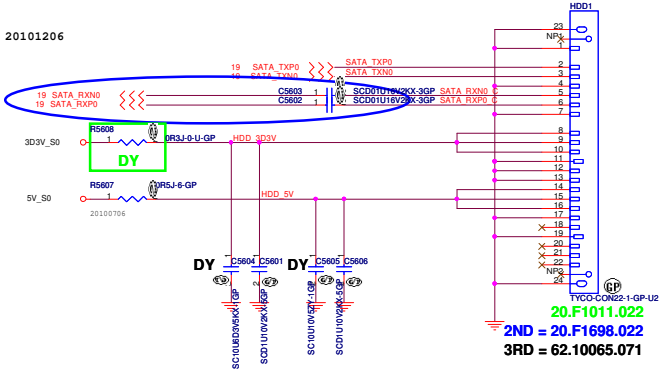
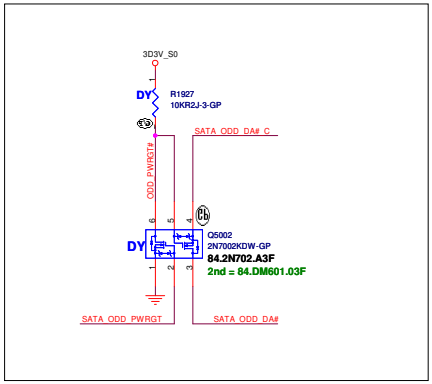
SATA HDD Connector

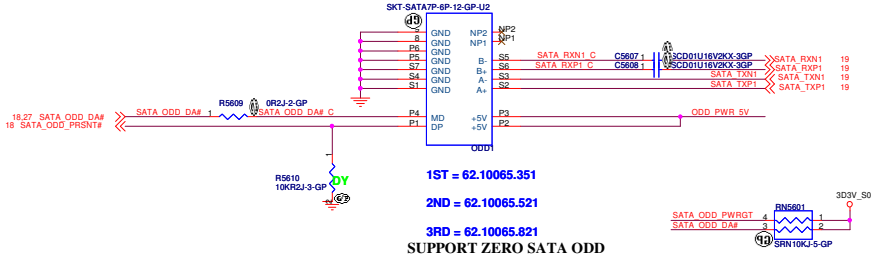




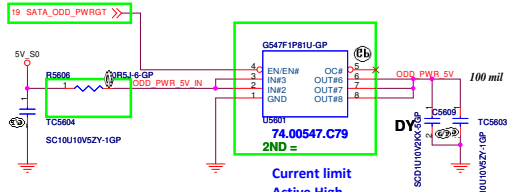
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD CONN

Size: | Document Number: B575 | Rev: SA

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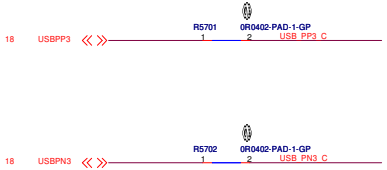

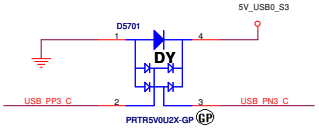

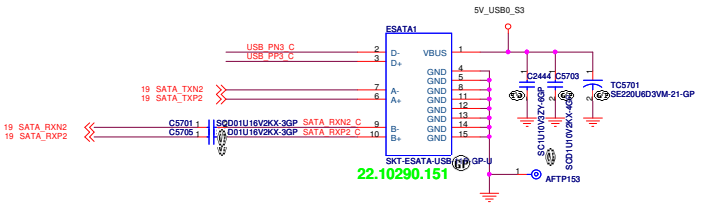

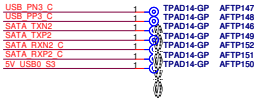

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: E-SATA/LUSB		
Size: A3	Document Number: B575	Rev: SA
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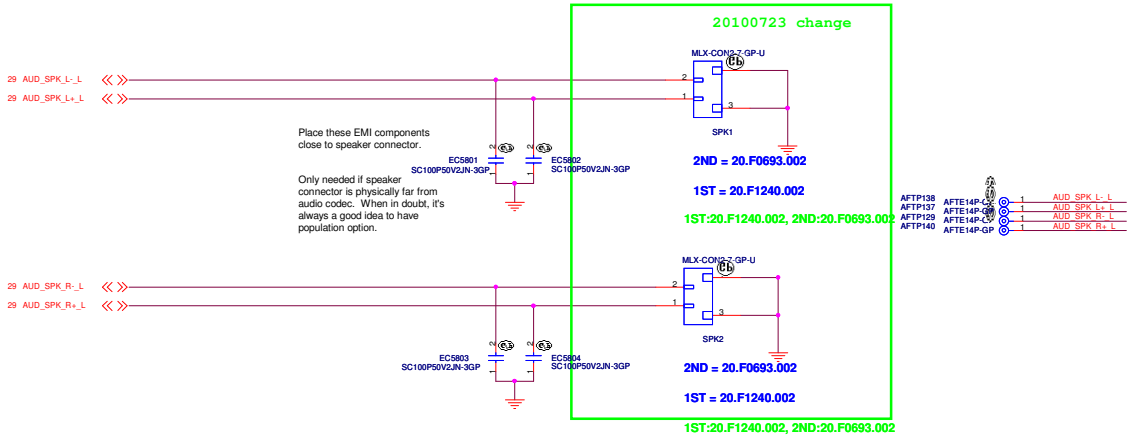

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPEAKER

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Reserved

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
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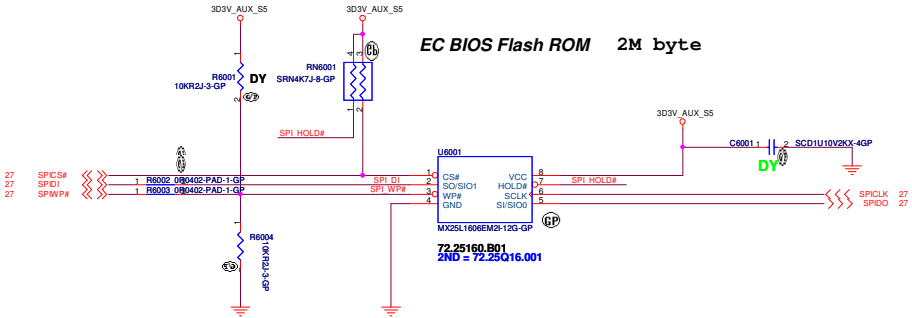
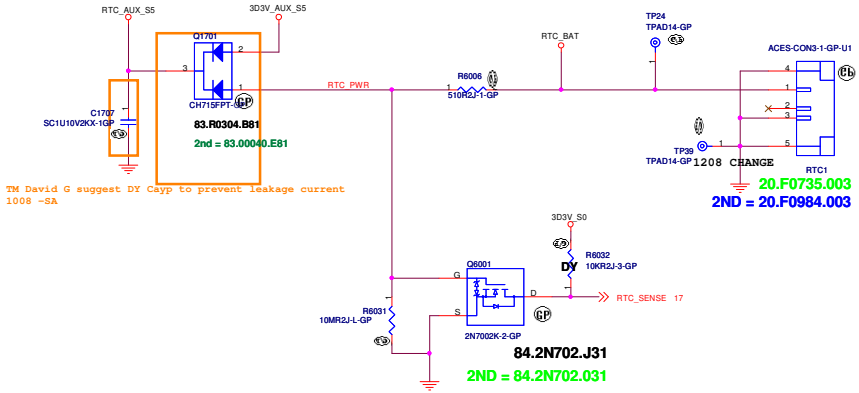
Date: Friday, March 25, 2011 Sheet 59 of 103



DN have eccounter RTC battery no power from field side feedbackfor Larry suggestion,
add Diode when 3.3V_Aux_S5 provide power to FCH RTC

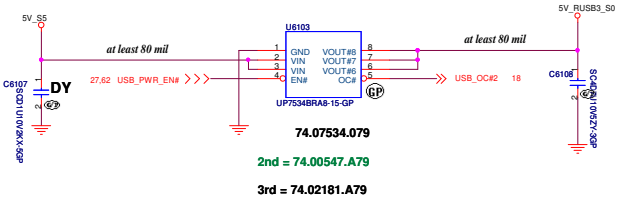


<Core Design>

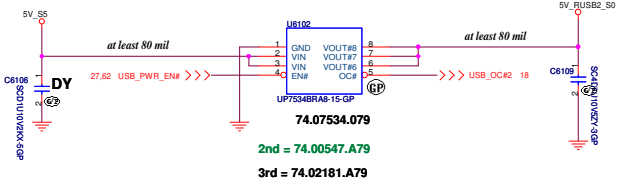
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BIOS / RTC***	
Size	Document Number **B575**	Rev SA
Date: Monday, March 28, 2011	Sheet 60 of 103	

SSID = USB

RJ45_USB Board USB Power



I/O Board USB Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size	Document Number	Rev
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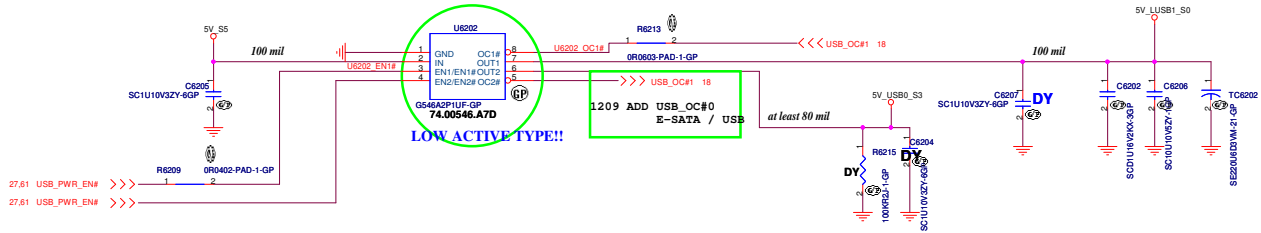
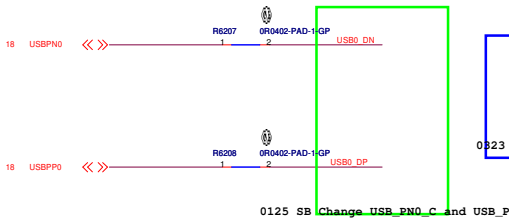
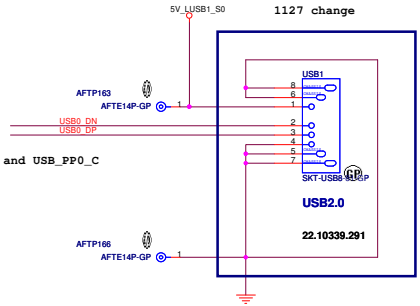
MB USB Port - #3

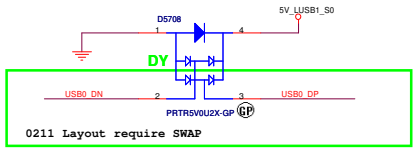
Left Side USB Power Switch

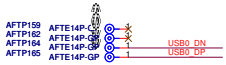




0323 DEL RN6201, net USB_PN0_C and USB_PP0_C







<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CONN

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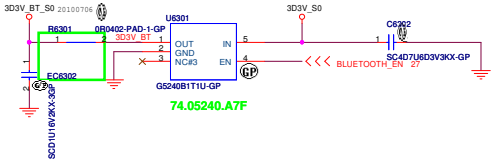
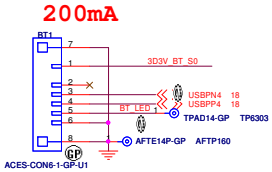
-1_20081002

Bluetooth Power



BT CONN.

EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



20.F0772.006

2ND = 20.F1804.006

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Bluetooth CONN***	
Size	Document Number **B575**	Rev **SA**
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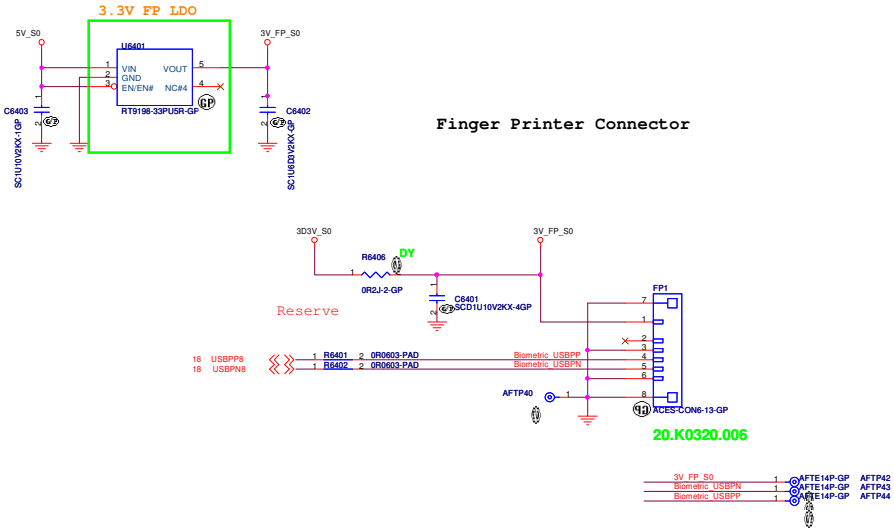

LA57 UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RESERVED**

Size	Document Number	Rev
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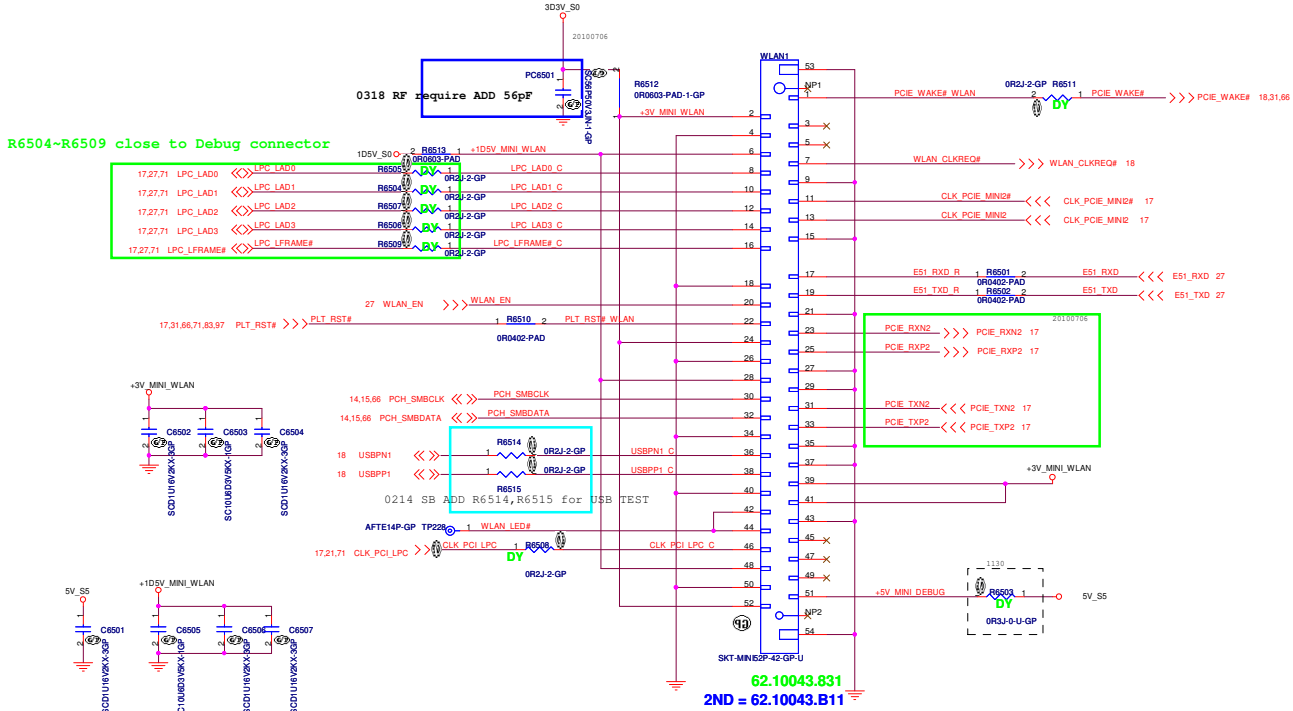
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD WLAN

Size	Document Number	Rev
	B575	SA

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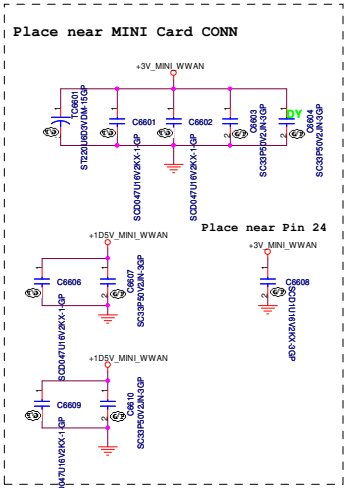
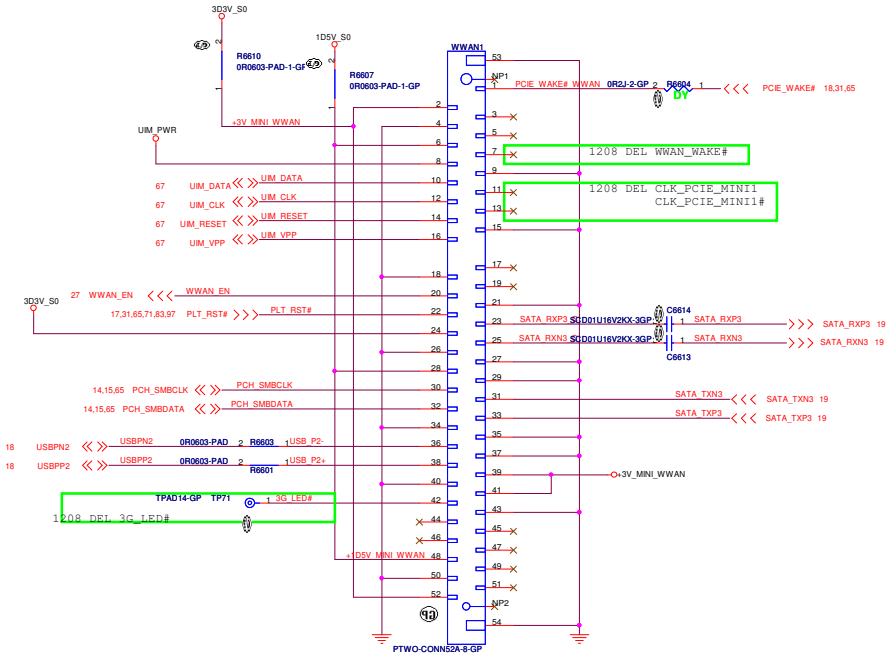
SSID = Wireless

Mini Card Connector(WWAN)





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD WWAN

Size	Document Number	Rev
	B575	SA

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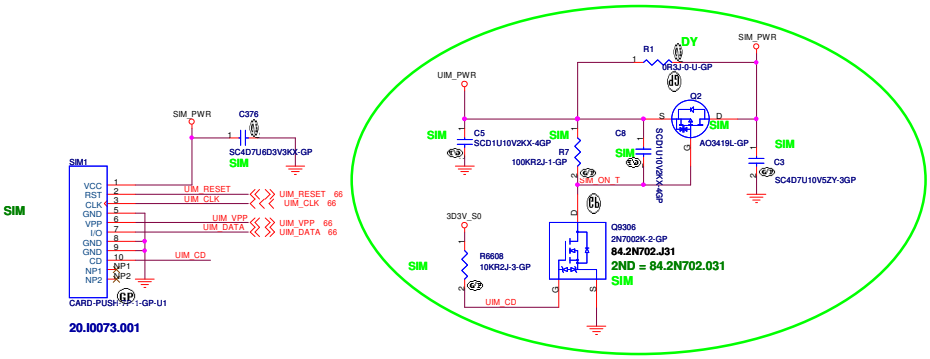

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SIM CARD**

Size	Document Number	Rev
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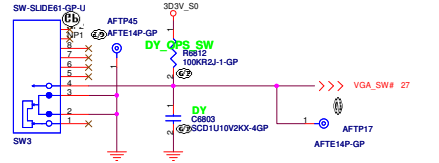
SSID = User.Interface

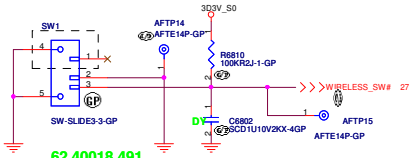


DY_OPS_SW

62.40018.351

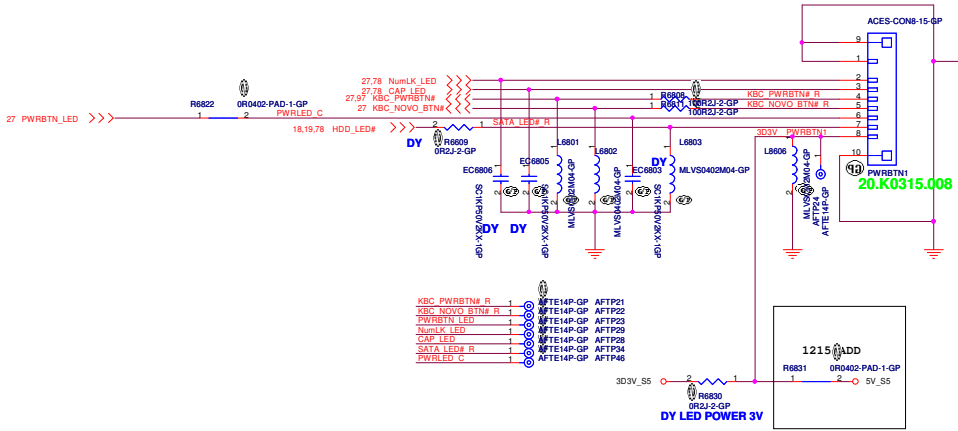
2ND = 62.40018.621

1208 ADD VGA SW



62.40018.491

1208 ADD BT SW



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER BUTTON

Size	Document Number	Rev
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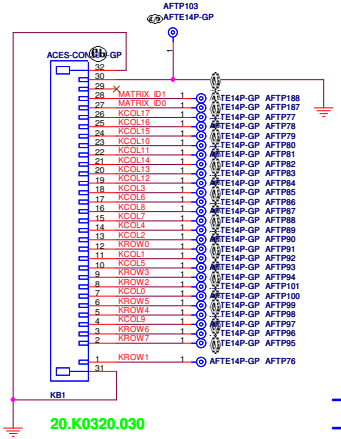
SSID = KBC

Internal KeyBoard Connector



20.K0320.030

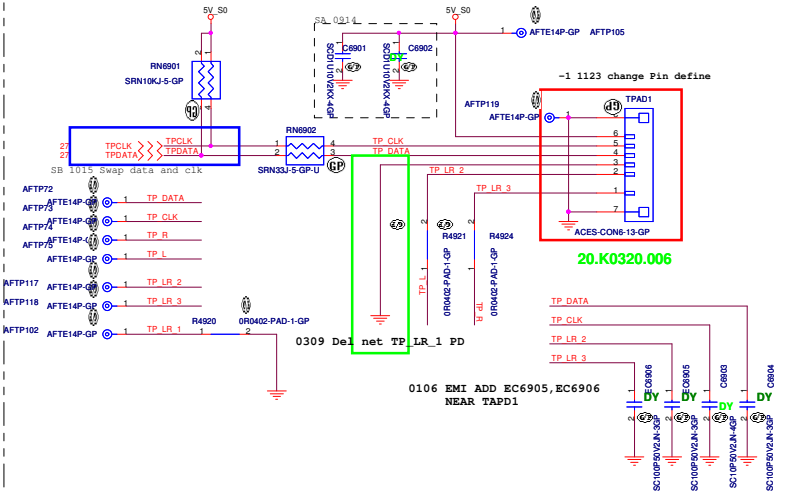
S205少兩PIN,
原廠測點已補上

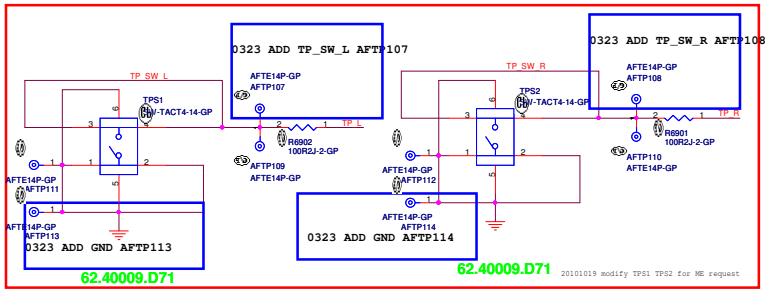
ID KEY MATRIX	SENSE			
	27	28	29	30
	IDO	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

KROW[7..0] 27

KCOL[17..0] 27

SSID = Touch.Pad





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KB/TP CONN

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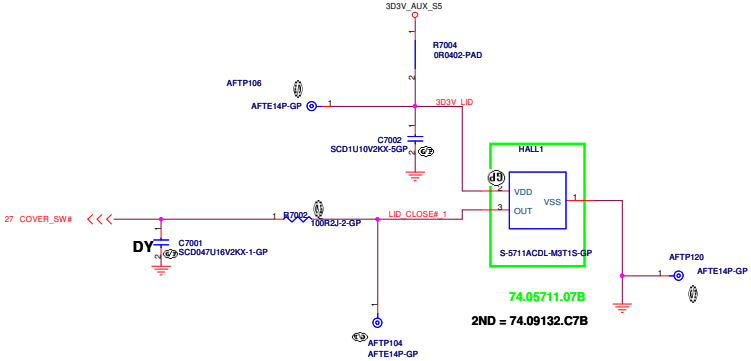
Hall Sensor



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HALL Sensor***

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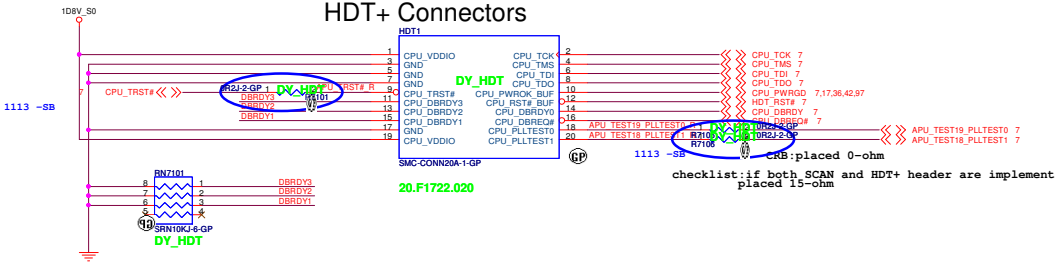
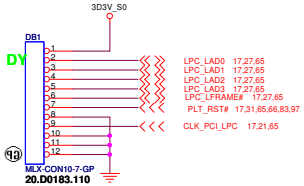
HDT+ Connectors



checklist:if both SCAN and HDT+ header are implement placed 15-ohm

GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug Port

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

CARD Reader CONN

Size	Document Number	Rev
A4	B575	SA

Date: Friday, March 25, 2011 Sheet 74 of 103

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A4	B575	SA

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(Blanking)

LA57 UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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LA57 UMA

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Title: ***Reserved***

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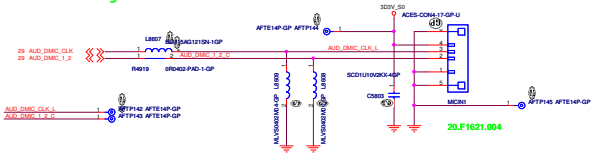
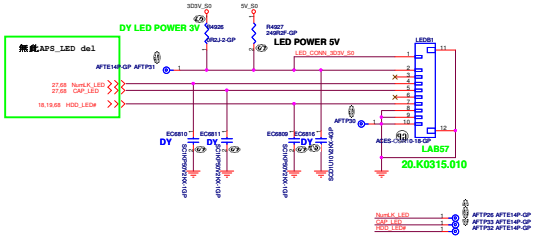
LB575 => Digital MIC

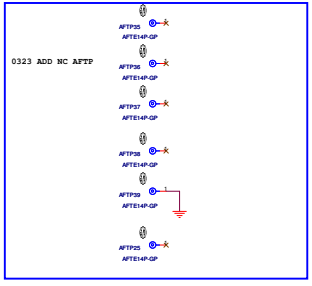
20101019 change L8607 L8608 L8609



LED Bord CONN.



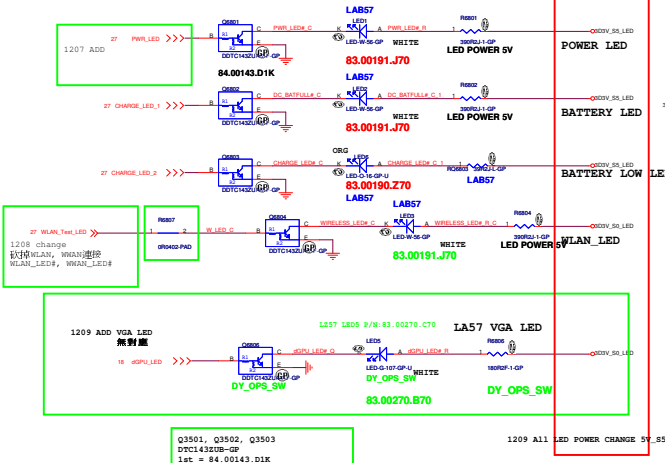
0323 ADD NC AFTP



LED

1209 All LED POWER CHANGE 5V_S5

1207 ADD



1224 ADD 3v OR 5v選擇線路

1209 ADD VGA LED
無對應

Q3501, Q3502, Q3503
DTC143ZUB-GP
1st = 84.00143.D1K
2nd = 84.00143.E1K
3rd =

1209 All LED POWER CHANGE 5V_S5

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REFERENCE

B575

SA

Monday, March 28, 2011

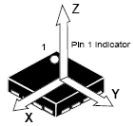
	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Core Design>

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Title: ***G-Sensor***

Size	Document Number	Rev
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LA57 UMA

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Title: *Reserved*

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LA57 UMA

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Title: *Reserved*

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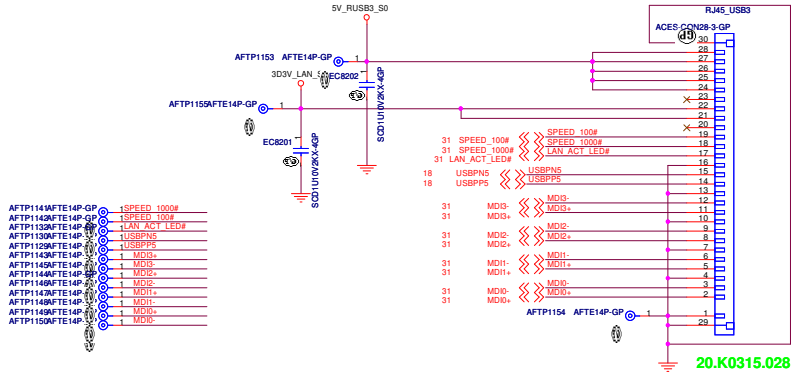
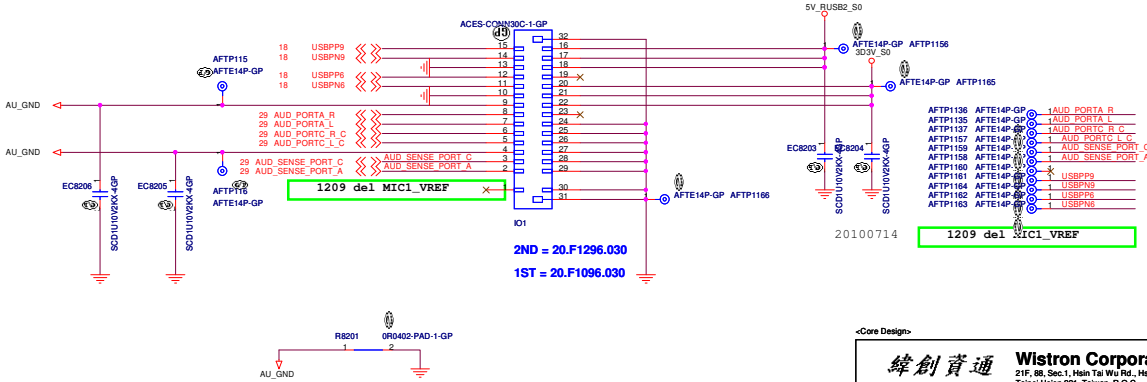
20100728 swap net

RJ45_USB CONN.



Card Reader Board CONN.



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**IO BD CONN**
Size	Document Number: **B575** — Rev: **SA**
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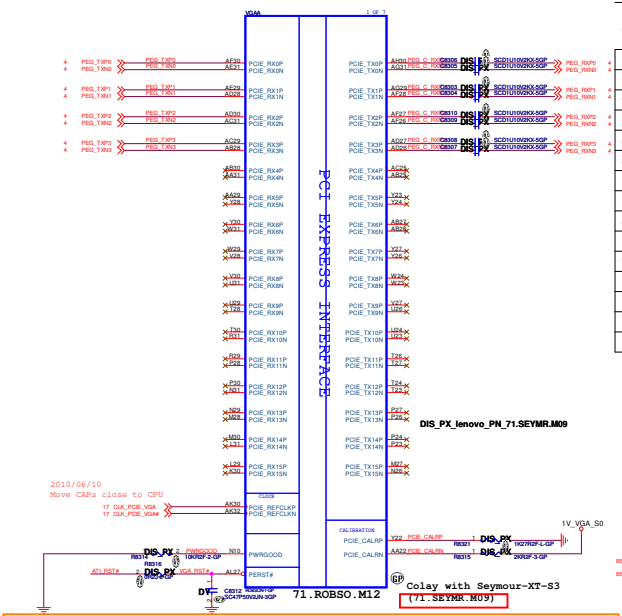


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 1K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	x x x	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	x	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	x	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

2010/06/11

PIN STRAPS

2010/06/11
Need to check

3D3V_VGA_S0

85 TX_PWRS_ENB	R8301	3K/RJ-2-GP
85 TX_DEEMPH_EN	R8302	3K/RJ-2-GP
85 BIF_GEN2_EN_A	R8303	10K/RJ-3-GP
85 GPIO8_ROMSO	R8304	10K/RJ-3-GP
85 VGA_DIS	R8305	10K/RJ-3-GP
85 CONFIG0	R8306	10K/RJ-3-GP
85 CONFIG1	R8307	10K/RJ-3-GP
85 CONFIG2	R8308	10K/RJ-3-GP
85 VGA_CRT_VSYNC	R8309	10K/RJ-3-GP
85 VGA_CRT_HSYNC	R8310	10K/RJ-3-GP
85 BIOS_ROM_EN	R8313	10K/RJ-3-GP
85 GPIO5_AC_BATT	R8318	10K/RJ-3-GP
85 GPIO21_BB_EN	R8317	10K/RJ-3-GP

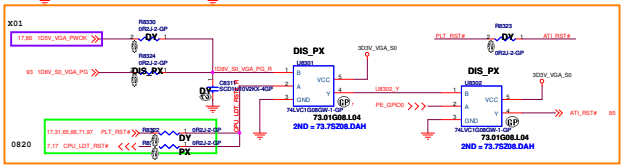
	PE_GPIO0
dGPU mode	H
IGPU	L
IGPU with BACO	H

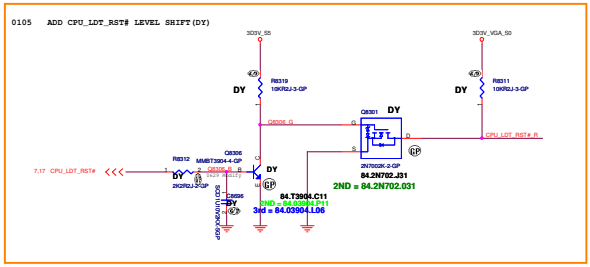
3D3V_VGA_S0

85 JTAG_TMS_VGA	R8325	10K/RJ-3-GP
84 TESTEN	R8326	10K/RJ-3-GP
	R8327	5K1/RF-L1-GP
85 JTAG_TRST#_VGA	R8328	10K/RJ-3-GP
85 JTAG_TCK_VGA	R8329	10K/RJ-3-GP

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC





<Variant Name>

Wistron Corporation
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Title: **GPU PCIE/STRAPPING(1/5)**

Size	Document Number	Rev
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PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

1D5V_VGA_S0

Ra R8410 40D2R2F-GP DIS_PX

Rb R8414 100R2F-L1-GP DIS_PX MVREFDA C8402 SCD1U10V2KX-5GP DIS_PX

1D5V_VGA_S0

Ra R8411 40D2R2F-GP DIS_PX

Rb R8415 100R2F-L1-GP DIS_PX MVREFSA C8403 SCD1U10V2KX-5GP DIS_PX

DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

88 MDA[0..31]

89 MDA[32..63]

VGAC 3 OF 7

MEMORY INTERFACE

MDA0	K27	DQA_0	MAA_0	K17	MAA0 88,89
MDA1	J29	DQA_1	MAA_1	J20	MAA1 88,89
MDA2	H30	DQA_2	MAA_2	H23	MAA2 88,89
MDA3	H32	DQA_3	MAA_3	G23	MAA3 88,89
MDA4	G29	DQA_4	MAA_4	G24	MAA4 88,89
MDA5	F28	DQA_5	MAA_5	H24	MAA5 88,89
MDA6	F32	DQA_6	MAA_6	J19	MAA6 88,89
MDA7	F30	DQA_7	MAA_7	K19	MAA7 88,89
MDA8	C30	DQA_8	MAA_8	J14	MAA8 88,89
MDA9	F27	DQA_9	MAA_9	K14	MAA9 88,89
MDA10	A28	DQA_10	MAA_10	J11	MAA10 88,89
MDA11	C28	DQA_11	MAA_11	J13	MAA11 88,89
MDA12	E27	DQA_12	MAA_12	H11	MAA12 88,89
MDA13	G26	DQA_13	MAA_13	G20	MAA13 88,89
MDA14	D26	DQA_14	MAA_14/BA0	J16	A_BA0 88,89
MDA15	F25	DQA_15	MAA_15/BA1	L15	A_BA1 88,89
MDA16	A25	DQA_16	MAA_BA2	G11	A_BA2 88,89
MDA17	C25	DQA_17			
MDA18	E25	DQA_18	DQMA_0	E32	DQMA0 88
MDA19	D24	DQA_19	DQMA_1	E30	DQMA1 88
MDA20	E23	DQA_20	DQMA_2	A21	DQMA2 88
MDA21	F23	DQA_21	DQMA_3	C21	DQMA3 88
MDA22	D22	DQA_22	DQMA_4	E13	DQMA4 89
MDA23	F21	DQA_23	DQMA_5	D12	DQMA5 89
MDA24	E21	DQA_24	DQMA_6	E3	DQMA6 89
MDA25	D20	DQA_25	DQMA_7	F4	DQMA7 89
MDA26	F19	DQA_26			
MDA27	A19	DQA_27	RDQSA_0	H28	QSAP_0 88
MDA28	D18	DQA_28	RDQSA_1	C27	QSAP_1 88
MDA29	F17	DQA_29	RDQSA_2	A23	QSAP_2 88
MDA30	A17	DQA_30	RDQSA_3	E19	QSAP_3 88
MDA31	C17	DQA_31	RDQSA_4	E15	QSAP_4 89
MDA32	E17	DQA_32	RDQSA_5	D10	QSAP_5 89
MDA33	D16	DQA_33	RDQSA_6	D6	QSAP_6 89
MDA34	F15	DQA_34	RDQSA_7	G5	QSAP_7 89
MDA35	A15	DQA_35			
MDA36	D14	DQA_36	WDQSA_0	H27	QSAN_0 88
MDA37	F13	DQA_37	WDQSA_1	A27	QSAN_1 88
MDA38	A13	DQA_38	WDQSA_2	C23	QSAN_2 88
MDA39	C13	DQA_39	WDQSA_3	C19	QSAN_3 88
MDA40	E11	DQA_40	WDQSA_4	C15	QSAN_4 89
MDA41	A11	DQA_41	WDQSA_5	E9	QSAN_5 89
MDA42	C11	DQA_42	WDQSA_6	G5	QSAN_6 89
MDA43	F11	DQA_43	WDQSA_7	H4	QSAN_7 89
MDA44	A9	DQA_44			
MDA45	C9	DQA_45	ODTA0	L18	ODTA0 88
MDA46	F9	DQA_46	ODTA1	K16	ODTA1 89
MDA47	D8	DQA_47			
MDA48	E7	DQA_48	CLKA0	H26	CLKA0 88
MDA49	A7	DQA_49	CLKA0#	H25	CLKA0# 88
MDA50	C7	DQA_50			
MDA51	F7	DQA_51	CLKA1	G9	CLKA1 89
MDA52	A5	DQA_52	CLKA1#	H9	CLKA1# 89
MDA53	E5	DQA_53			
MDA54	C3	DQA_54	RASA0#	G22	RASA0# 88
MDA55	E1	DQA_55	RASA1#	G17	RASA1# 89
MDA56	G7	DQA_56			
MDA57	G6	DQA_57	CASA0#	G16	CASA0# 88
MDA58	G1	DQA_58	CASA1#		CASA1# 89
MDA59	G3	DQA_59			
MDA60	J6	DQA_60	CSA0#_0	H22	CSA0#_0 88
MDA61	J1	DQA_61	CSA0#_1	J22	
MDA62	J3	DQA_62			
MDA63	J5	DQA_63	CSA1#_0	G13	CSA1#_0 89
			CSA1#_1	K13	
MVREFDA	K26	MVREFDA			
MVREFSA	J26	MVREFSA	CKEA0	K20	CKEA0 88
MEM_CALRN0	J25	MEM_CALRN0	CKEA1	J17	CKEA1 89
TESTEN	K7	TESTEN			
			WEA0#	G25	WEA0# 88
MEM_CALRP1/DPC_CALR	J8	MEM_CALRP1/DPC_CALR	WEA1#	H10	WEA1# 89
MEM_CALRP0	K25	MEM_CALRP0			
			PX_EN	AB16	PX_EN_R
DRAM_RST	L10	DRAM_RST			
CLKTESTA	K8	CLKTESTA	RSVD#G14	G14	
CLKTESTB	L7	CLKTESTB			

ROBSON-1GP

DIS_PX_lenovo_PN_71.SEYMR.M09

71.ROBSO.M12 Colay with Seymour-XT-S3 (71.SEYMR.M01)

1D5V_VGA_S0

1231 change 240ohm F, AMD require

R8403 1 PX 240R2F-1-GP MEM_CALRN0

R8408 1 PX 240R2F-1-GP MEM_CALRP0

DPC_CALR (Park/Robson-S3):
Analog calibration.
Connect DPxx_CALR to GND through a 150-Ω (1%) resistor.

150R2F-1-GP R8407 1 DIS_PX

MEM_CALRP1/DPC_CALR

TESTEN

88,89 MEM_RST

R_MEM_2

R8405 1 DIS_PX DRAM_RST 1 51R2J-2-GP

C8401 SC120P50V2JN-1GP DIS_PX C_MEM

R_MEM_1

R8402 1 DIS_PX 10R2F-L-GP

TPAD14 TP8401 CLKTESTA

TPAD14 TP8402 CLKTESTB

R8409 5K1R2F-2-GP DIS_PX R_MEM_3

R8420 DIS_PX 0R2J-2-GP PX_EN 86

B8421 DIS_PX 10KR2J-3-GP

**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2

C8407 SCD1U10V2KX-5GP DY CLKTESTA_G CLKTESTA

C8406 SCD1U10V2KX-5GP DY CLKTESTB_G CLKTESTB

R8419 DY 51R2J-2-GP

R8418 DY 51R2J-2-GP

For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

2010/07/06
Schematics check list:
A pull-down resistor is required.

<Variant Name>

緯創資通 Wistron Corporation
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Title: GPU Memory(2/5)

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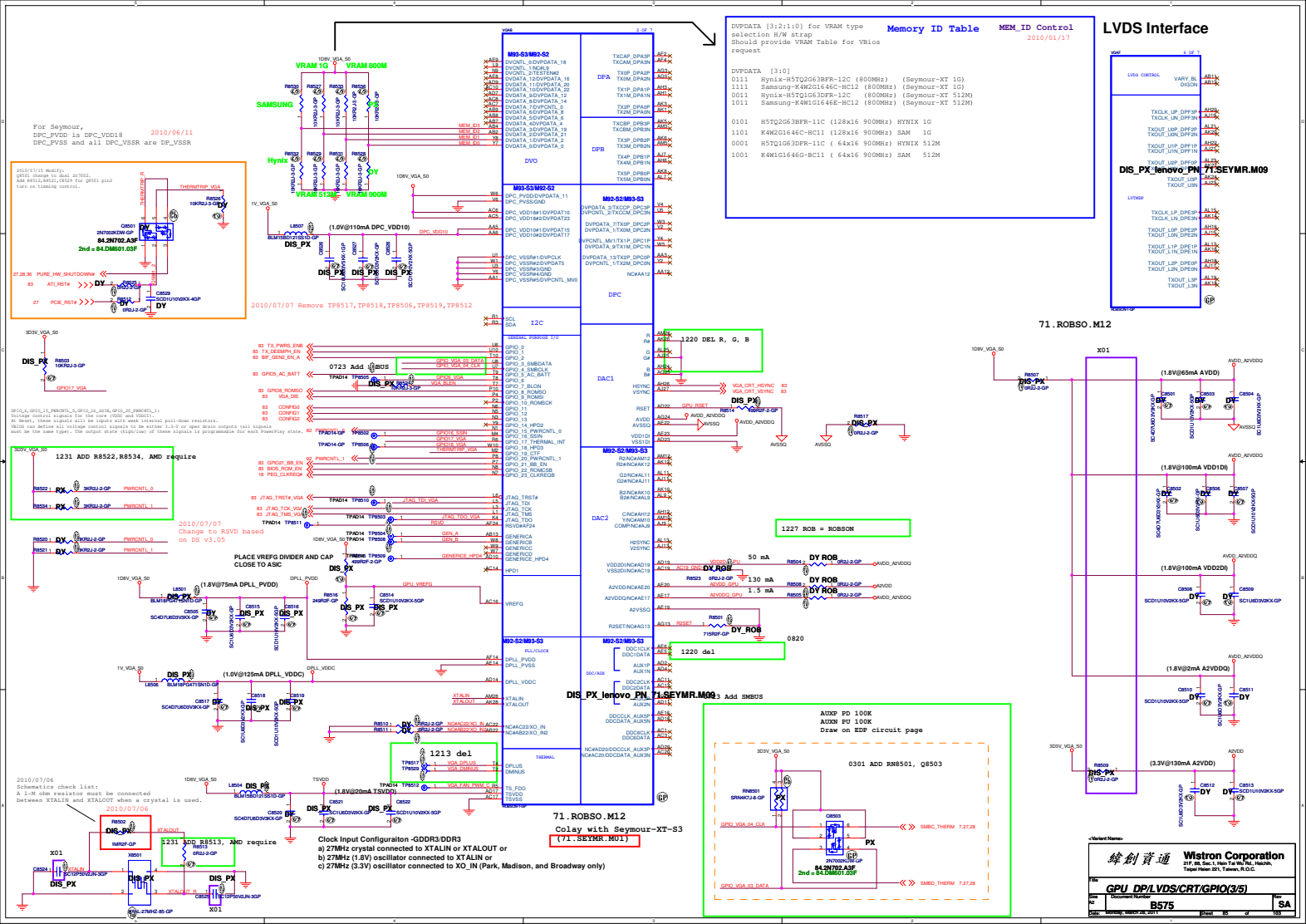
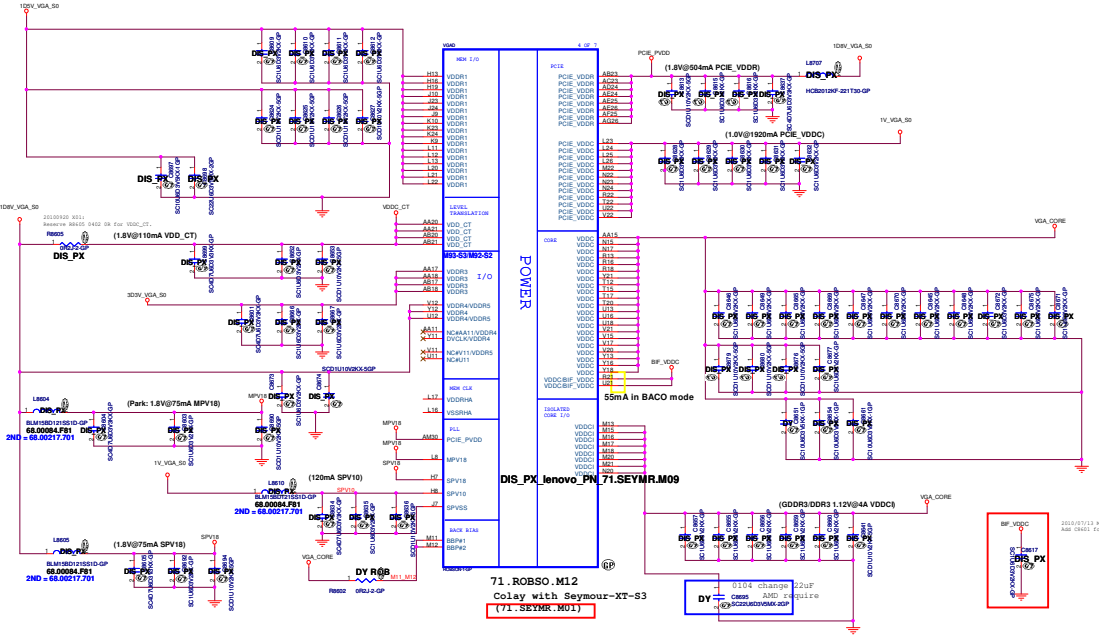
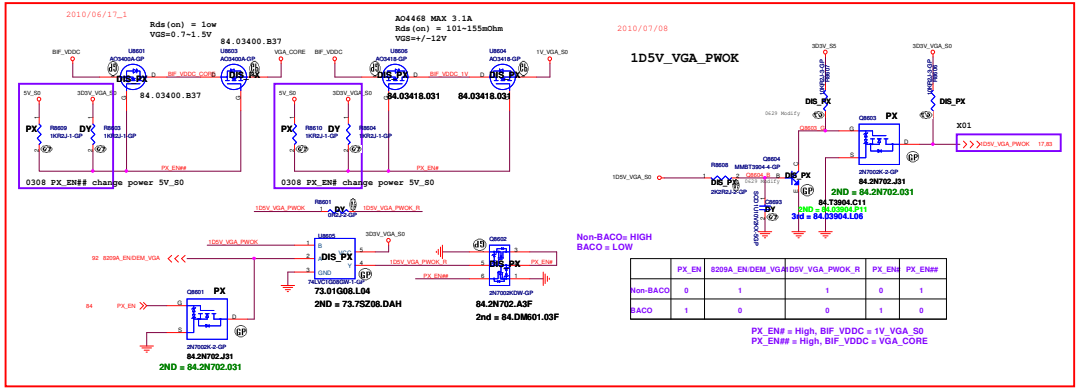

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
Memory ID Table
MEM_ID Control
2010/01/17
DVPDATA [3:0]
0111 Hynix-H5TQ2G63BFR-12C (800MHz) (Seymour-XT 1G)
1111 Samsung-K4W2G1646C-HC12 (800MHz) (Seymour-XT 1G)
0011 Hynix-H5TQ1G63DFR-12C (800MHz) (Seymour-XT 512M)
1011 Samsung-K4W1G1646E-HC12 (800MHz) (Seymour-XT 512M)
0101 H5TQ2G63BFR-11C (128x16 900MHz) HYNIX 1G
1101 K4W2G1646C-HC11 (128x16 900MHz) SAM 1G
0001 H5TQ1G63DFR-11C (64x16 900MHz) HYNIX 512M
1001 K4W1G1646G-BC11 (64x16 900MHz) SAM 512M
LVDS Interface
DIS_PX_lenovo_PN_71.SEYMR.M09
71.ROBSO.M12
VRAM 1G
VRAM 800M
VRAM 512M
VRAM 900M
SAMSUNG
Hynix
For Seymour,
DPC_PVDD is DPC_VDD18 2010/06/11
DPC_PVSS and all DPC_VSSR are DP_VSSR
2010/07/07 Remove TP8517,TP8518,TP8506,TP8519,TP8512
0723 Add 2 BUS
1220 DEL R, G, B
1231 ADD R8522,R8534, AMD require
2010/07/07 Change to RSVD based on DS v3.05
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
1227 ROB = ROBSON
1220 del
1213 del
0301 ADD RN8501, Q8503
AUXP PD 100K
AUXN PD 100K
Draw on EDP circuit page
0820 Add SMBUS
2010/07/06 Schematics check list: A 1-M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.
1231 ADD R8513, AMD require
Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)
71.ROBSO.M12
Colay with Seymour-XT-S3
(71.SEYMR.M01)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GPU DP/LVDS/CRT/GPIO(3/5)
B575
SA





	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN#	PX_EN##
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

UMA 3G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size	Document Number	Rev
A2	B575	SA

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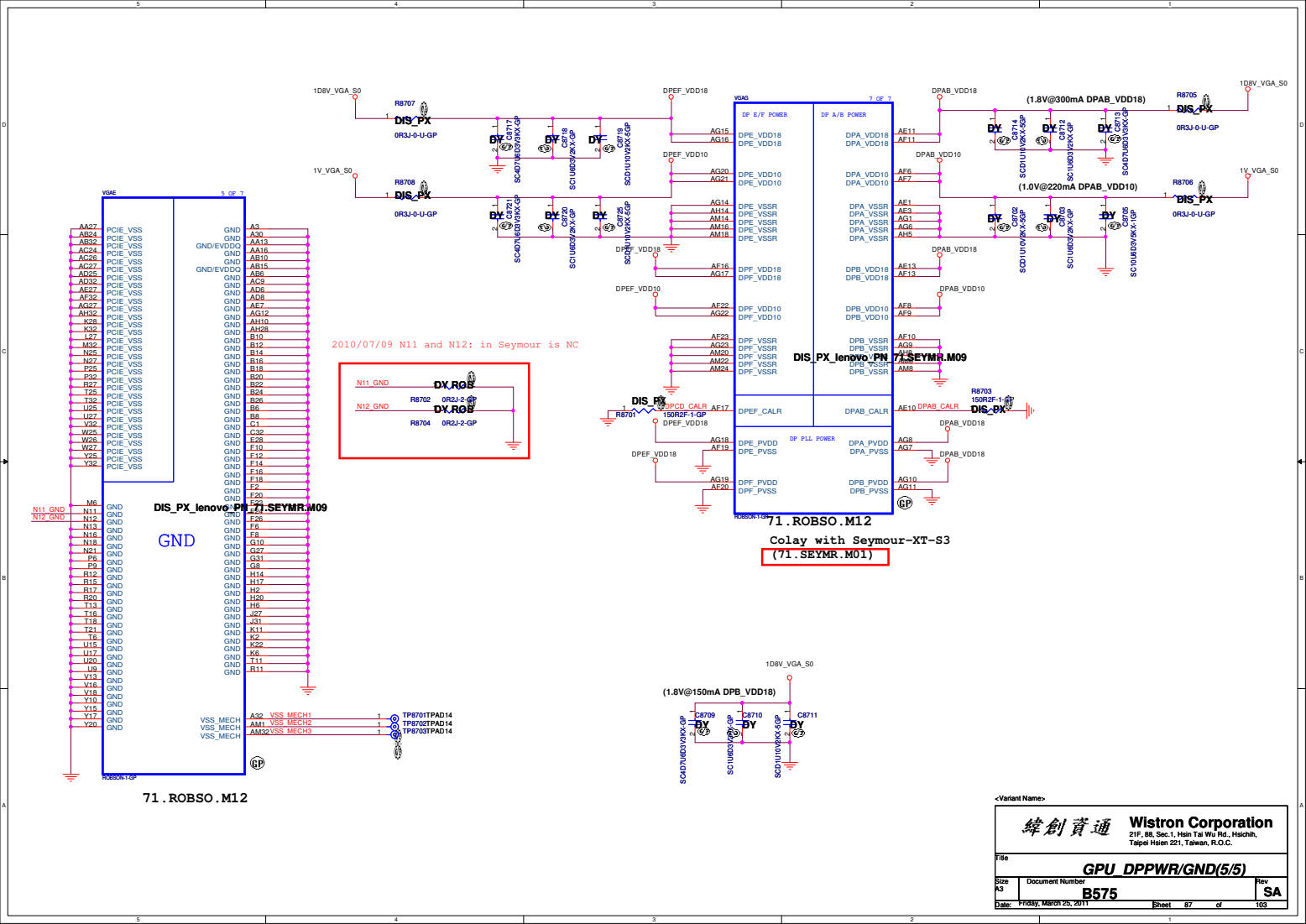

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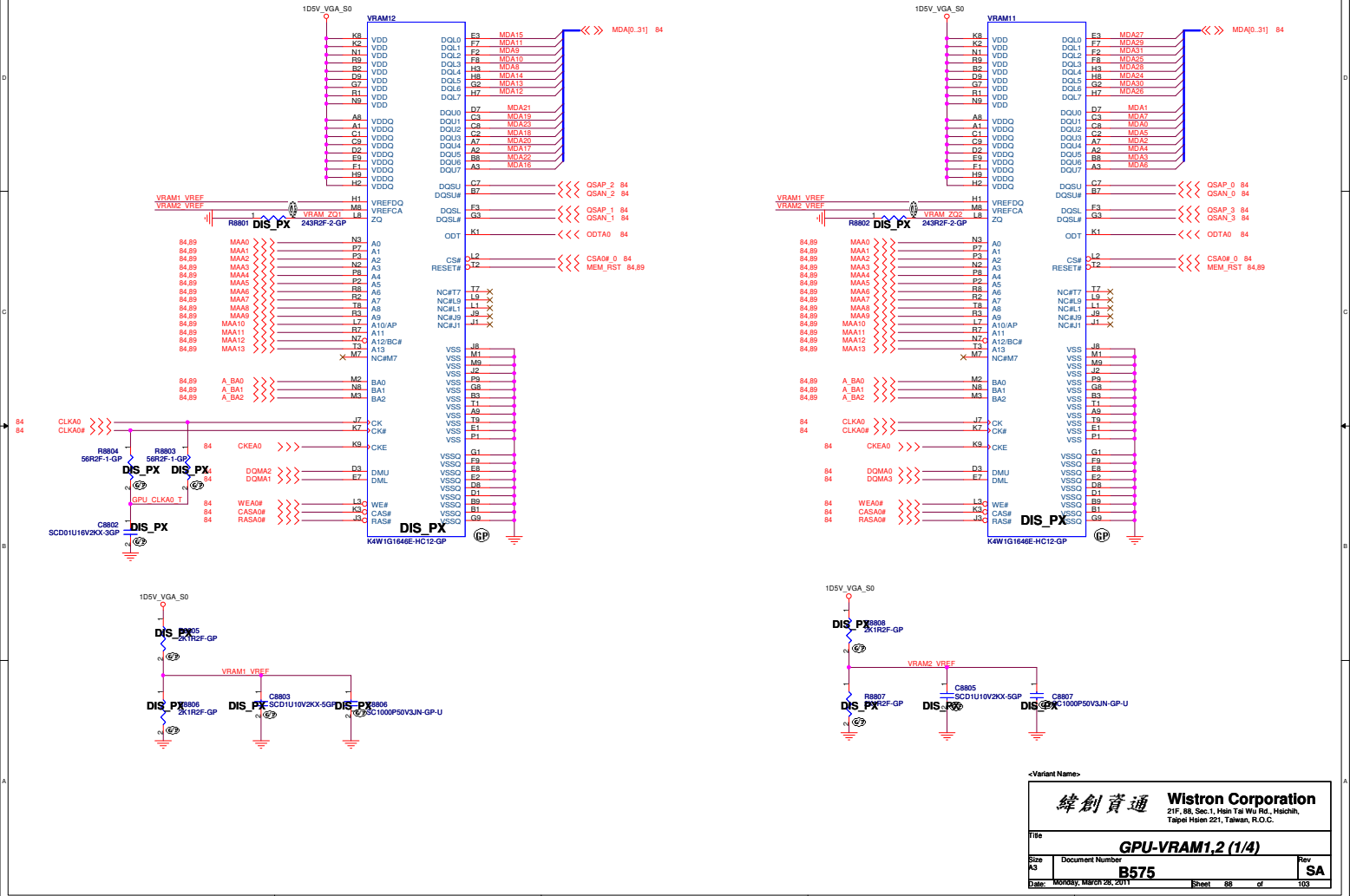

<Variant Name>

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Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
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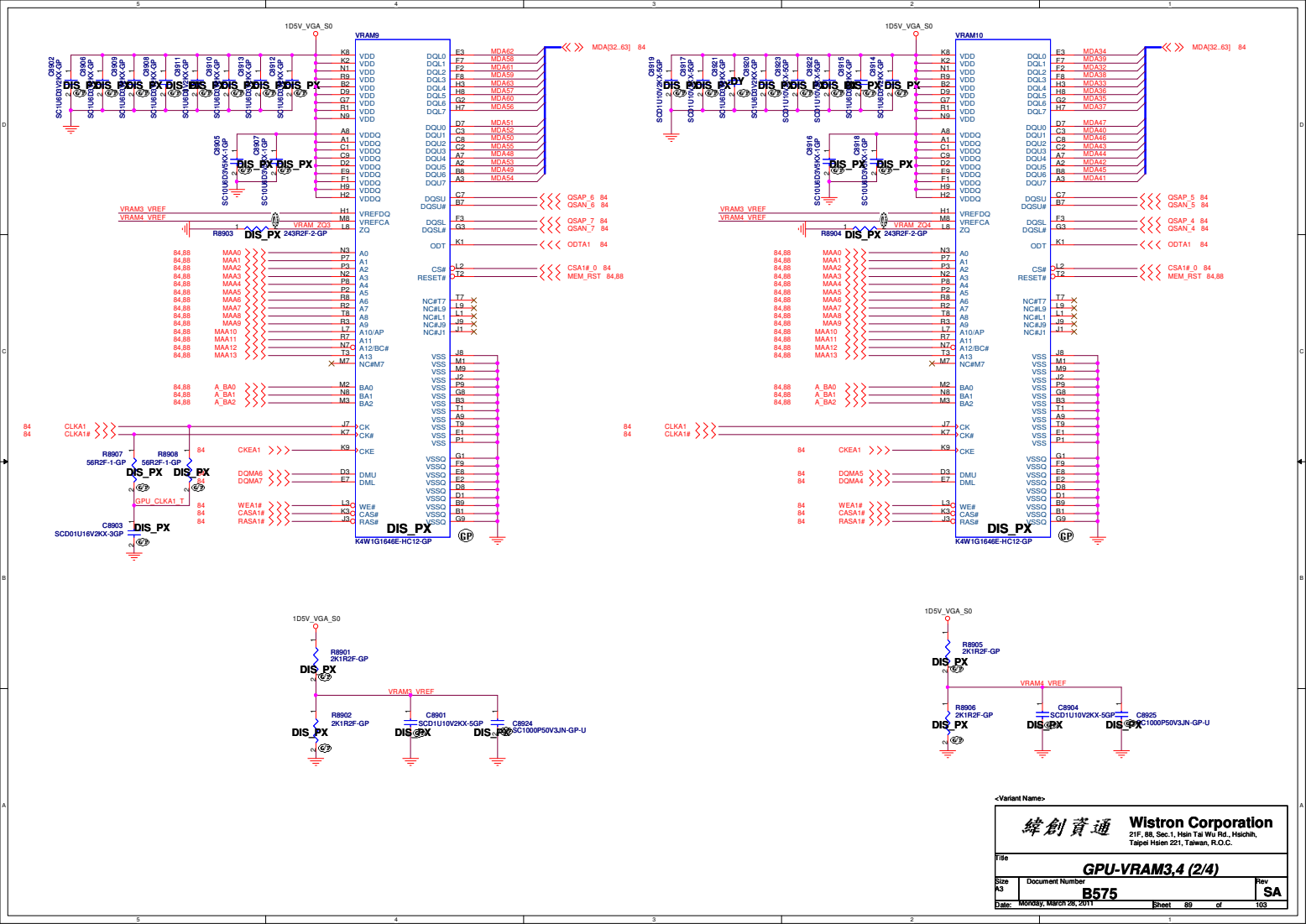

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<Variant Name>

Title: GPU-VRAM3,4 (2/4)

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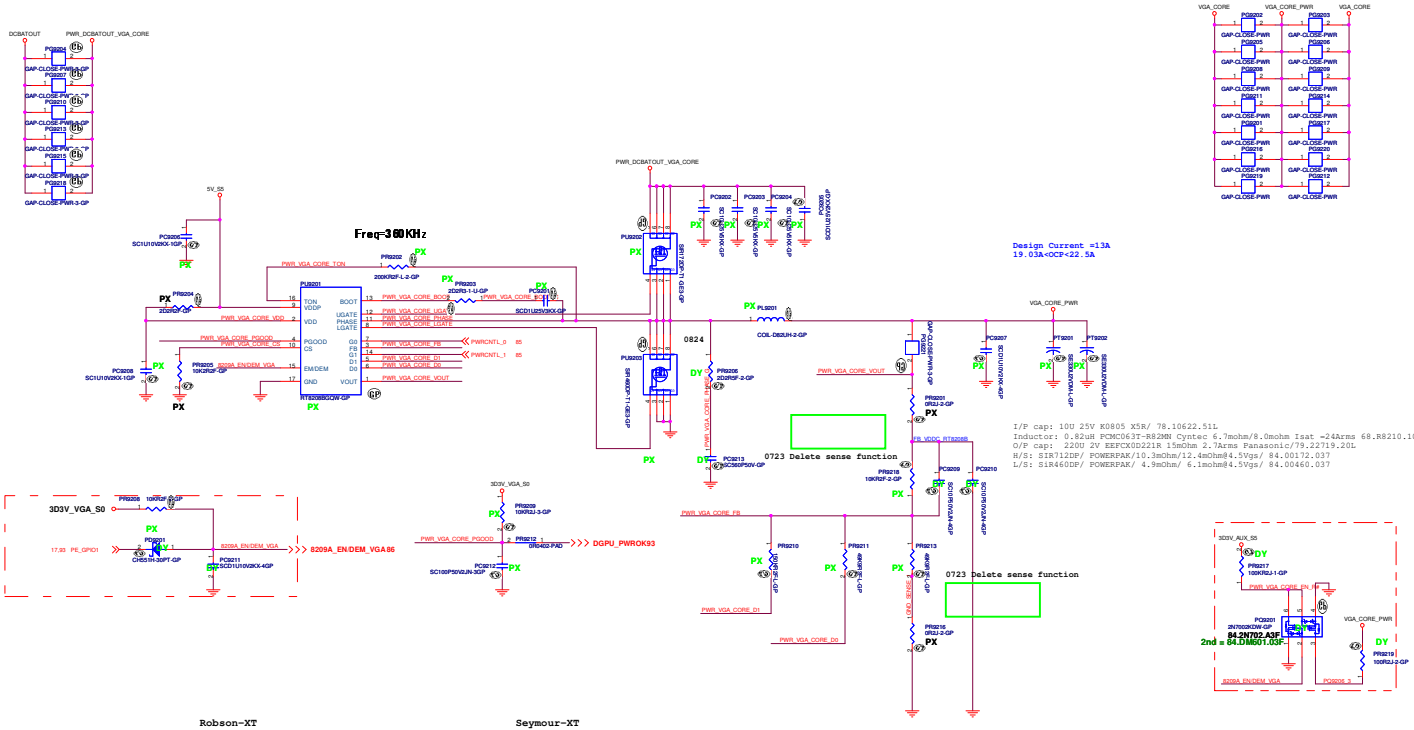
SSID = PWR.Plane.Regulator_VGACORE



Robson-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	H	0.95V
H	L	1.05V
H	H	0.9V

Seymour-XT

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	H	0.95V
H	L	1.05V
H	H	0.9V

Vout=0.75V*(R1+R2)/R2

For ROBSON

PR9210=44K.2K(64.44225.6DL)

PR9211=150K(64.15035.6DL)

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File	RT8208B_+VCC_GFXCORE	
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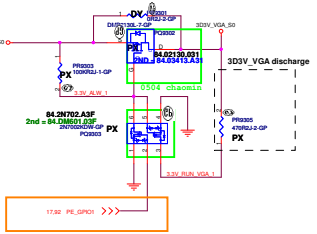
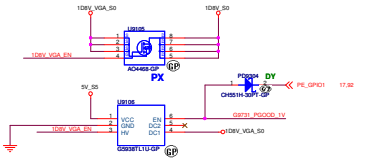
+3VS to 3.3V_DELAY Transfer

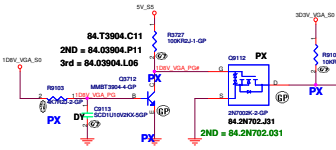


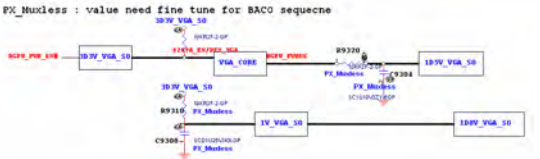
Different To Intel, AMD Is High Active

	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H

G9731 for 1D8V_VGA

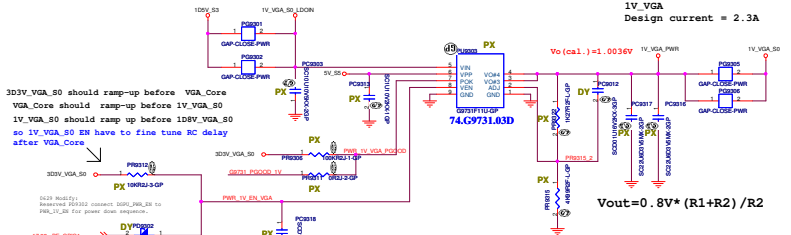






G9731 for 1V_VGA_S0

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

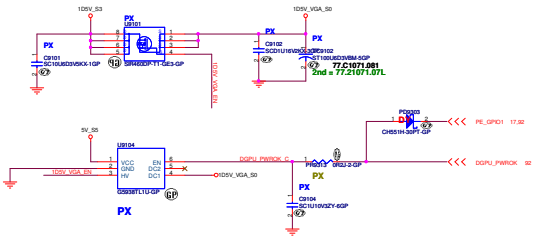


1V_VGA
Design current = 2.3A

Vo(cal.)=1.0036V

Vout=0.8V*(R1+R2)/R2

1D5V_VGA_S0



UMA 3G

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Title: DISCRETE VGA POWER
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<Core Design>

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Title

HDD / ODD CONN

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<Variant Name>

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Title: ***CRT Switch***

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LA57 UMA

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Title

TOUCH PANEL

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CPU Plate

H13 HOLE276R178-GP — ZZ.00PAD.N11
H14 HOLE276R178-GP — ZZ.00PAD.N11
H15 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H10 STF237R128H42-GP — PX — 34.4GD01.101
H11 STF237R128H42-GP — PX — 34.4GD01.101

Structure boss

H1 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H2 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H3 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H5 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H6 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H12 HOLE355X355R111-S1-GP — ZZ.00PAD.571
H7 HOLE335R115-GP — ZZ.00PAD.D01
H8 HOLE335R115-GP — ZZ.00PAD.D01

MiniPCI Std-Off

H4 STF237R113H115-GP — 34.4V802.101

Check test point

3D3V_S0	TPAD14-GP	TP96
3D3V_AUX_S5	TPAD14-GP	TP95
3D3V_S5	TPAD14-GP	TP83
5V_S5	TPAD14-GP	TP82
18,27 PM_PWRBTN#	TPAD14-GP	TP78
7,17,36,42,71 CPU_PWRGD	TPAD14-GP	TP79
27,36 S5_ENABLE	TPAD14-GP	TP80
17,31,65,66,71,83 PLT_RST#	TPAD14-GP	TP81

Test Point放在Dimm Door打開可量測處

H16 GNDPAD — ZZ.NDPAD.XXX
H17 GNDPAD — ZZ.NDPAD.XXX

1216 改過footprint

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN# — TP9701 TPAD40-GP, TP9700 TPAD40-GP

0106 EMI ADD EC CAP

1D5V_S3
EC9706 EC9705 EC9704 EC9703 EC9702 EC9701 — DY — SCD1U25V2KX-GP

0211 SB

DCBATOUT
EC9716 EC9715 EC9714 EC9713 EC9710 EC9709 EC9708 EC9707 EC9712 EC9711 — DY — SCD1U25V2KX-GP

0211 SB EMI require

BT+
EC9716 EC9717 — SCD1U25V2KX-GP

<Core Design>

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Title: SPRING/HALL
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待確認

(Blanking)

<Core Design>

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Title: *Change History*

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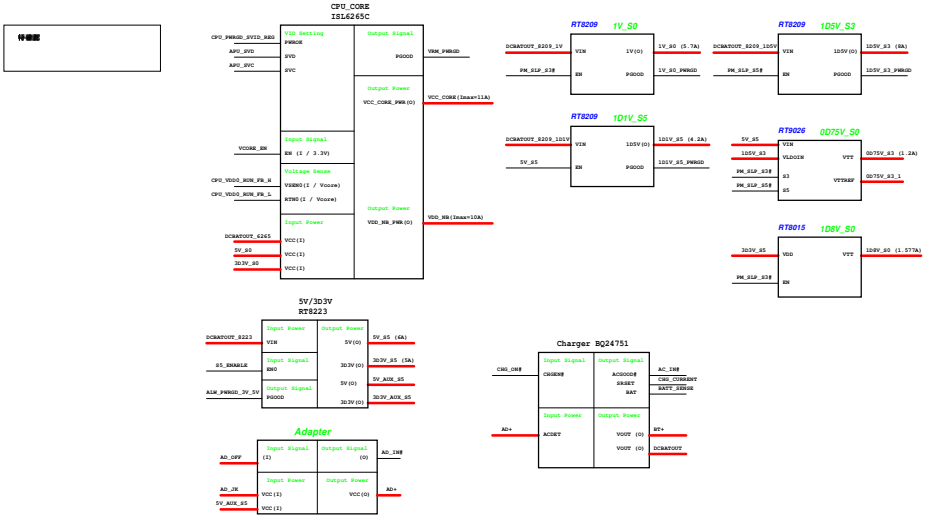
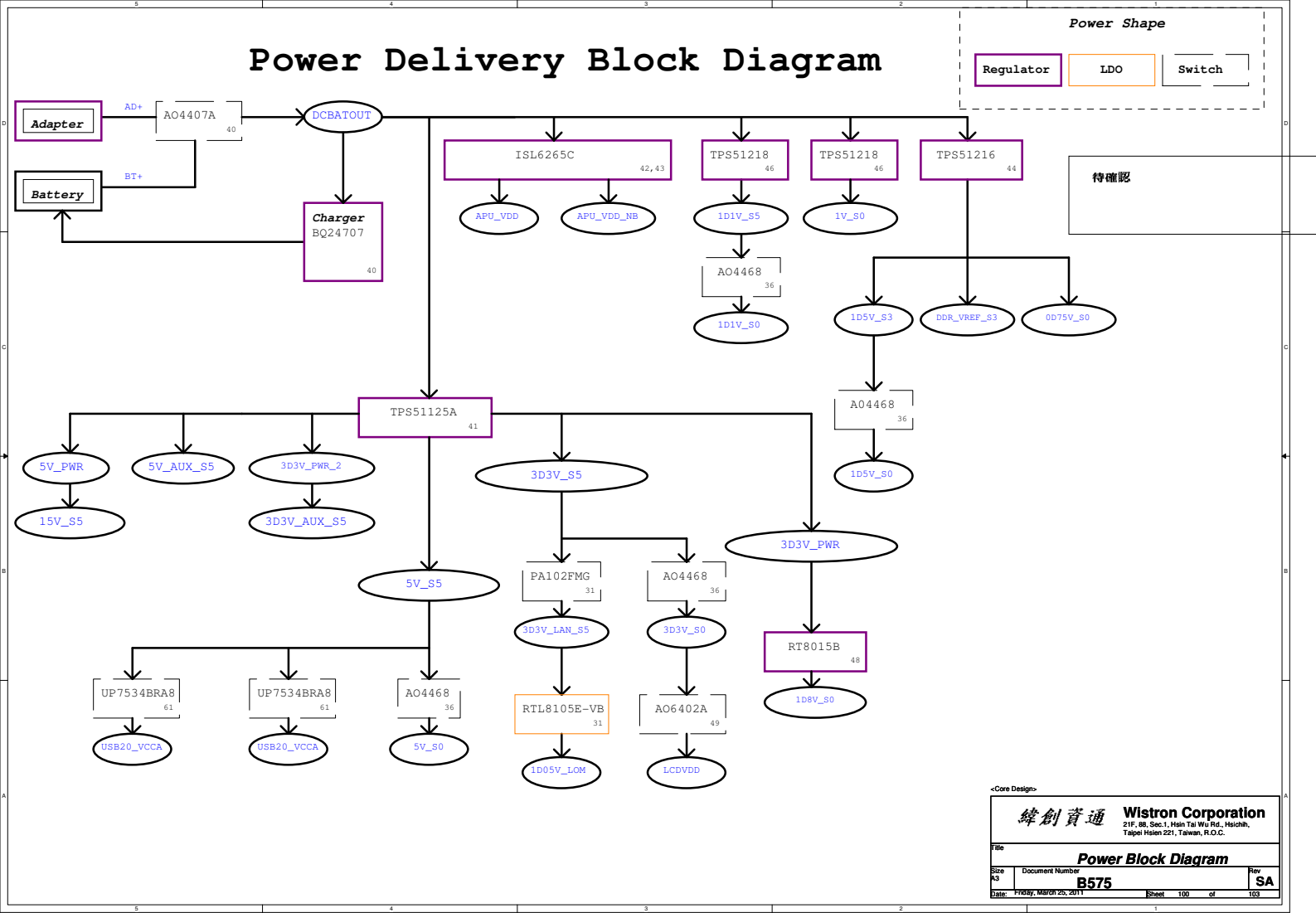


Wistron Corporation
Power Sequence
8575
5A

Power Delivery Block Diagram



<Core Design>

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Title	Power Block Diagram	
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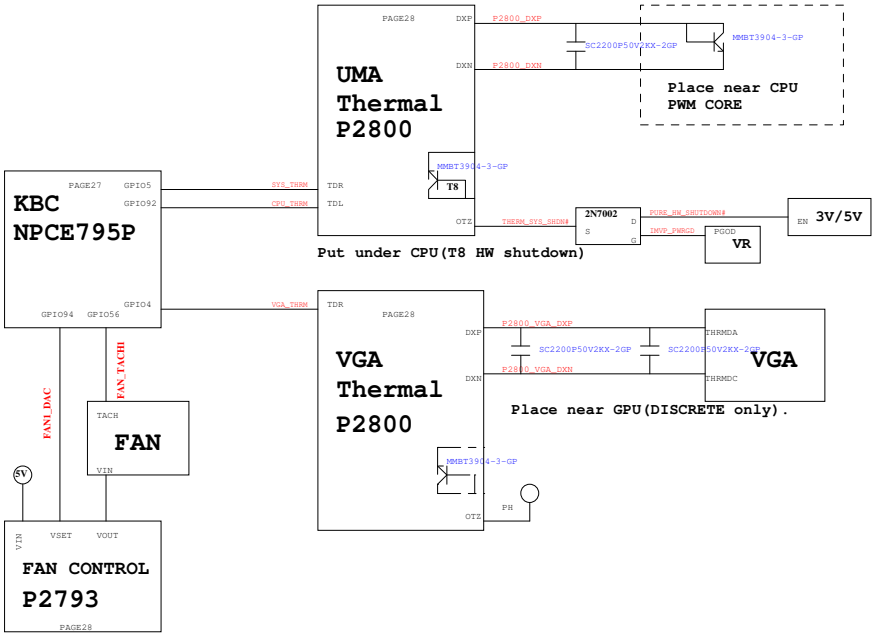
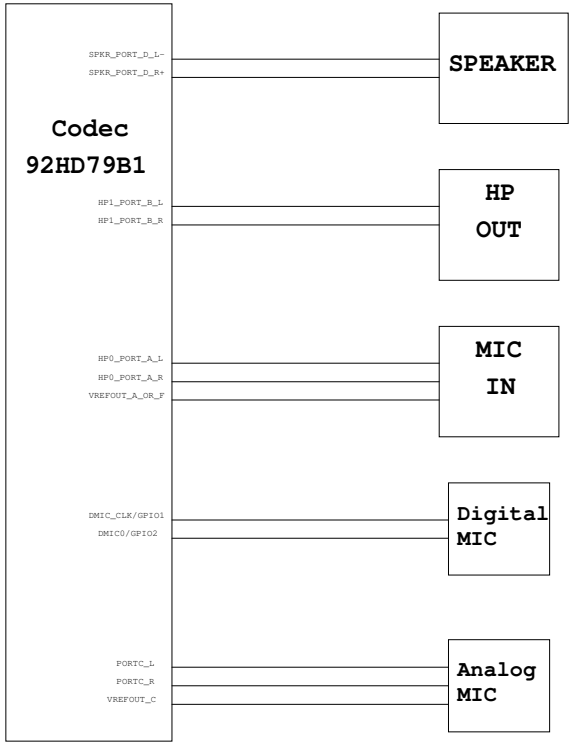
Thermal Block Diagram

待確認



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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+1D5V_MINI_WLAN +1D5V_MINI_WLAN 65

+1D5V_MINI_WWAN +1D5V_MINI_WWAN 66

+3V_MINI_WLAN +3V_MINI_WLAN 65

+3V_MINI_WWAN +3V_MINI_WWAN 66

0D75V_PWR 0D75V_PWR 46

0D75V_S0 0D75V_S0 14,15,36,46

1D05V_LAN_S5 1D05V_LAN_S5 31

1D05V_S0 1D05V_S0 4,6,45

1D1V_PWR 1D1V_PWR 45

1D1V_S0 1D1V_S0 20,36

1D1V_S5 1D1V_S5 20,36,45

1D5V_PWR 1D5V_PWR 46

1D5V_S0 1D5V_S0 29,36,65,66

1D5V_S3 1D5V_S3 5,6,14,15,36,46,93,97

1D5V_VGA_S0 1D5V_VGA_S0 84,86,88,89,93

1D8V_PWR 1D8V_PWR 47

1D8V_S0 1D8V_S0 6,7,17,20,42,47,71,93

1D8V_VGA_S0 1D8V_VGA_S0 85,86,87,93

1V_PWR 1V_PWR 45

1V_VGA_S0 1V_VGA_S0 83,85,86,87,93

1V_VGA_S0_LDOIN 1V_VGA_S0_LDOIN 93

3D3V_AUX_KBC 3D3V_AUX_KBC 27,39

3D3V_AUX_S5 3D3V_AUX_S5 18,27,28,40,41,60,70,92,97

3D3V_BT_S0 3D3V_BT_S0 63

3D3V_CAMERA_S0 3D3V_CAMERA_S0 49

3D3V_LAN_S5 3D3V_LAN_S5 31,82

3D3V_LAN_VDDSREG 3D3V_LAN_VDDSREG 31

3D3V_PWR 3D3V_PWR 41

3D3V_PWR_2 3D3V_PWR_2 41

3D3V_S0 3D3V_S0 6,7,14,15,17,18,19,20,21,27,28,29,31,36,42,46,49,50,51,56,60,63,64,65,66,67,68,71,78,82,93,97

3D3V_S0_LED 3D3V_S0_LED 78

3D3V_S5 3D3V_S5 7,18,20,21,27,31,36,41,42,45,47,68,78,83,86,97

3D3V_S5_LED 3D3V_S5_LED 78

3D3V_VGA_S0 3D3V_VGA_S0 83,85,86,92,93

3V_FP_S0 3V_FP_S0 64

5V_CRT_S0 5V_CRT_S0 50

5V_HDMI 5V_HDMI 51

5V_LUSB1_S0 5V_LUSB1_S0 62

5V_PWR 5V_PWR 41

5V_PWR_2 5V_PWR_2 41

5V_RUSB2_S0 5V_RUSB2_S0 61,82

5V_RUSB3_S0 5V_RUSB3_S0 61,82

5V_S0 5V_S0 7,28,29,36,50,51,56,64,69,78,86

5V_S5 5V_S5 36,41,42,45,46,47,61,62,65,68,78,92,93,97

5V_USB0_S3 5V_USB0_S3 57,62

A2VDD A2VDD 85

AD+ AD+ 38,40

AD_JK AD_JK 38

AUD_3D3V AUD_3D3V 29

AUD_3D3V_1D5V AUD_3D3V_1D5V 29

AUD_5V AUD_5V 29

AVDD_A2VDDQ AVDD_A2VDDQ 85

AVDD_SATA AVDD_SATA 19,20

AVDD_USB AVDD_USB 20

BIF_VDDC BIF_VDDC 86

BQ24745_VREF BQ24745_VREF 40

BT+ BT+ 39,40,97

DCBATOUT DCBATOUT 36,40,41,42,43,45,46,47,49,92,97

DCBATOUT_LCD DCBATOUT_LCD 49

DDR_VREF_S3 DDR_VREF_S3 5,14,15,46

DPAB_VDD10 DPAB_VDD10 87

DPAB_VDD18 DPAB_VDD18 87

DPEF_VDD10 DPEF_VDD10 87

DPEF_VDD18 DPEF_VDD18 87

DPLL_PVDD DPLL_PVDD 85

DPLL_VDDC DPLL_VDDC 85

LCDVDD LCDVDD 49

MPV18 MPV18 86

PCIE_VDDR PCIE_VDDR 17,20

PWR_1D5V_DCBATOUT PWR_1D5V_DCBATOUT 46

PWR_3D3V_DCBATOUT PWR_3D3V_DCBATOUT 41

PWR_5VSD3V_VREF PWR_5VSD3V_VREF 41

PWR_5V_DCBATOUT PWR_5V_DCBATOUT 41

PWR_DCBATOUT_1V PWR_DCBATOUT_1V 45

PWR_DCBATOUT_VGA_CORE PWR_DCBATOUT_VGA_CORE 92

RTC_AUX_S5 RTC_AUX_S5 17,27,60

RTC_BAT RTC_BAT 60

RUN_ENABLE RUN_ENABLE 36

RUN_ENABLE_S RUN_ENABLE_S 36

SIM_PWR SIM_PWR 67

SPV18 SPV18 86

TSVDD TSVDD 85

UIM_PWR UIM_PWR 66,67

VCC_CORE VCC_CORE 6,42

VDD_NB VDD_NB 6,42,43

VDDAN_3D3V_HWM VDDAN_3D3V_HWM 20

VDDC_CT VDDC_CT 86

VDDIO_AZ VDDIO_AZ 20

VDDPL_1D1V VDDPL_1D1V 20

VDDPL_3D3V VDDPL_3D3V 20

VGA_CORE VGA_CORE 86,92

VGA_CORE_PWR VGA_CORE_PWR 92

AU_GND AU_GND 29,82

CHG_AGND CHG_AGND 40

AVSSQ AVSSQ 85

GNDA_VCORE GNDA_VCORE 42

<Variant Name>

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Title: Change History

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