

Compal Confidential

PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2011-02-24

REV: 1 . A

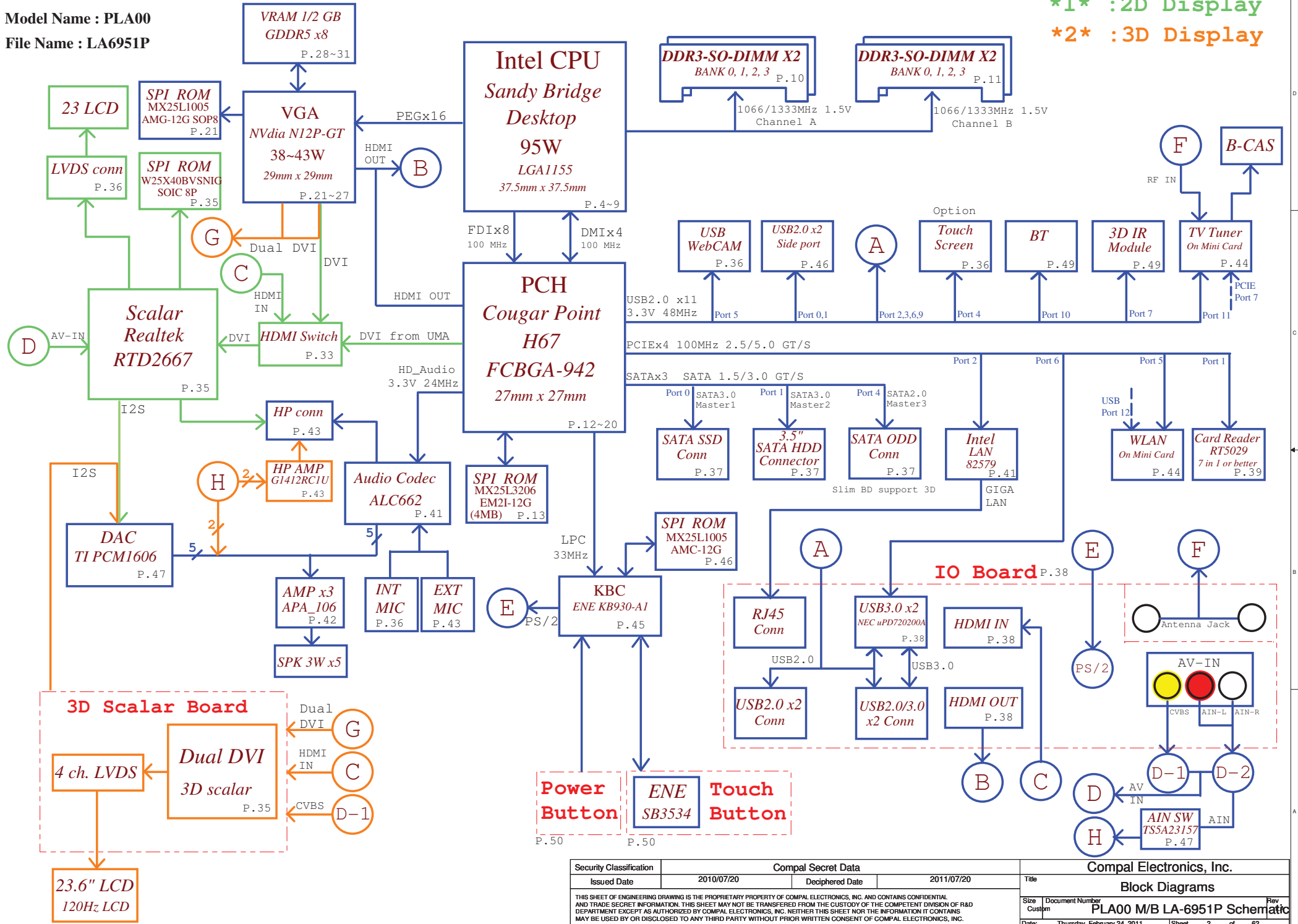
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Model Name : PLA00

File Name : LA6951P

1 :2D Display
2 :3D Display



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Custom				
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Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	ON	ON	OFF
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE	SIGNAL					
	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@ (VRAM:Hynix)
0	1	0	DIS@ (VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

BOARD ID Table

Board ID	Ra/Rb	Vad-bid
AV SKU	R442 100K	3.3V
NON AV SKU	R445 0 ohm	0 V

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
	UHCI3	6	USB 2.0
7		3D IR	
EHCI2	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(WLAN)
	UHCI6	12	Mini Car(TV Tuner
		13	

BTO Option Table

BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
CRT	CRT@
PCM1606	1606@
Samsung VRAM (1G)	x76_SAM@
Hynix VRAM (1G)	x76_HYN@
Samsung VRAM (2G)	x76_SAM2G@
Hynix VRAM (2G)	x76_HYN2G@
AV-IN SKU	AV@
No AV-IN SKU	NON_AV@

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

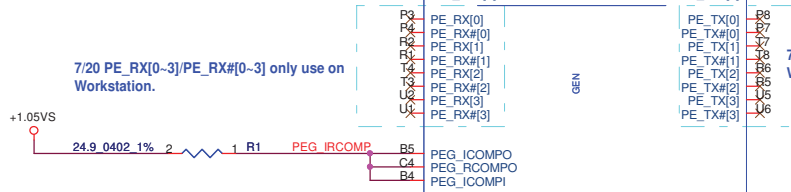
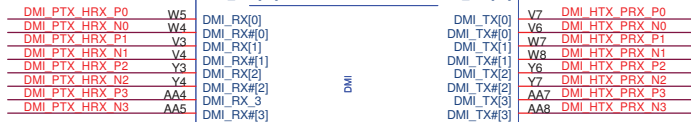
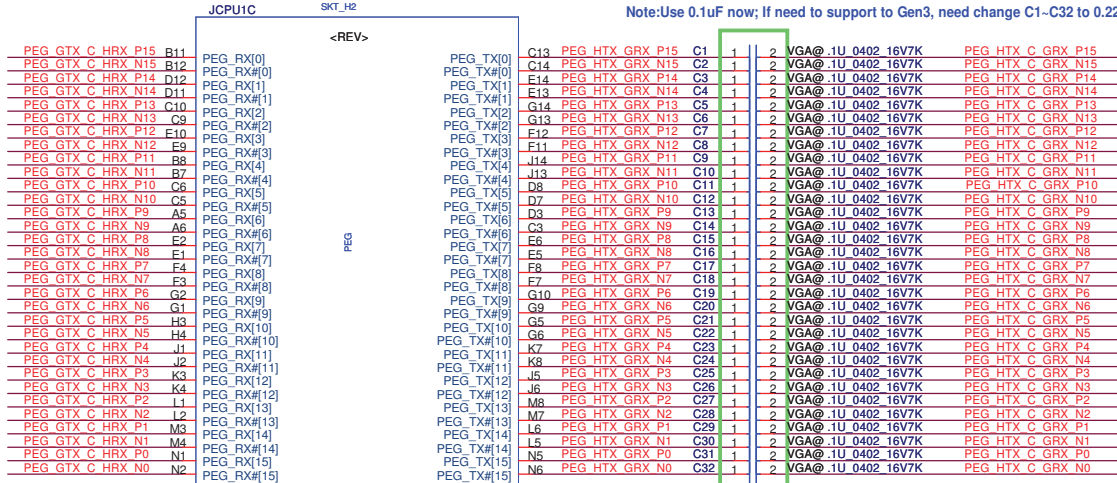
Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

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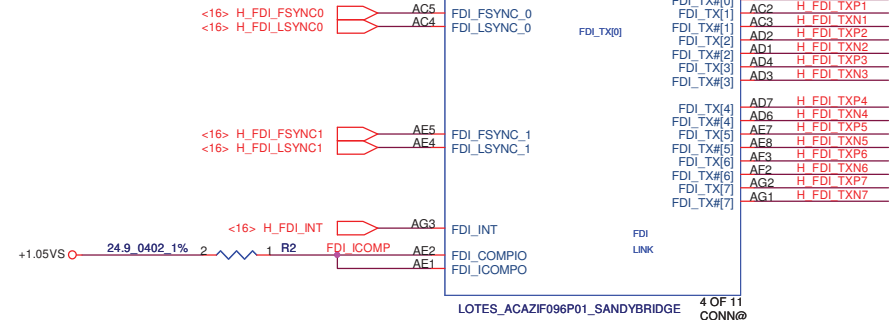
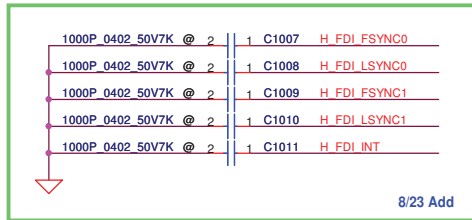
DMI_PTX_HRX_N[0..3] <14>
DMI_PTX_HRX_P[0..3] <14>
DMI_HTX_PRX_N[0..3] <14>
DMI_HTX_PRX_P[0..3] <14>

PEG GTX_C_HRX_P[0..15] <22>
PEG GTX_C_HRX_N[0..15] <22>
PEG HTX_C_GRX_P[0..15] <22>
PEG HTX_C_GRX_N[0..15] <22>

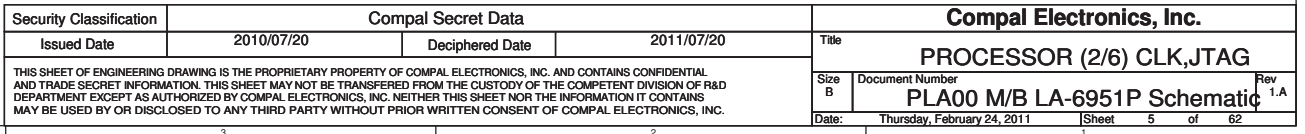
Note:Use 0.1uF now; If need to support to Gen3, need change C1-C32 to 0.22uF.

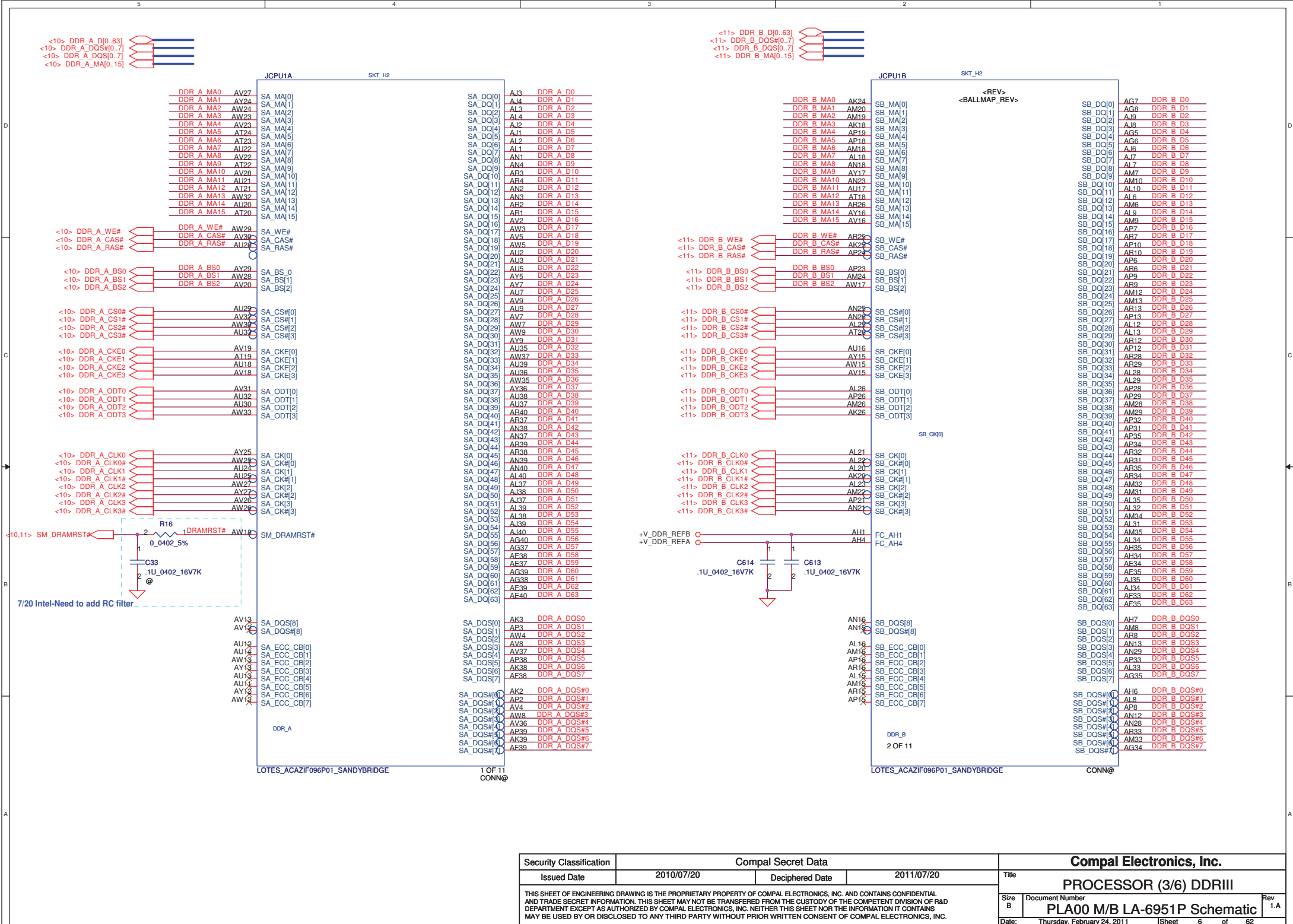


PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - Width/Space (12 mils/15mils)

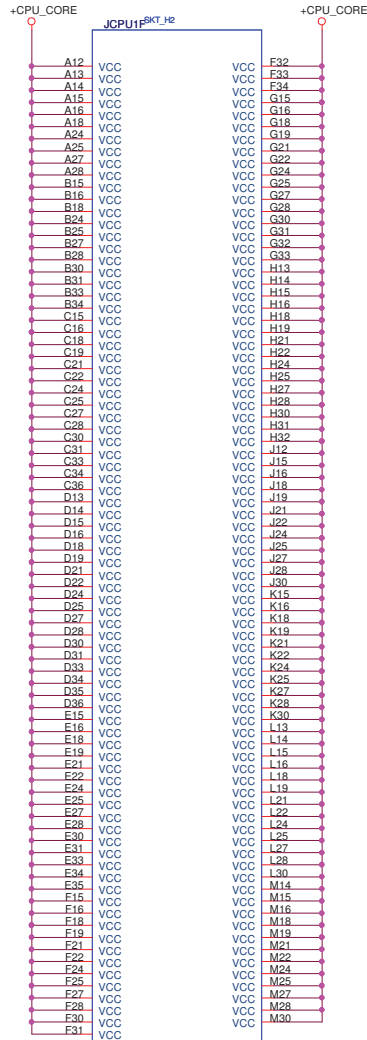


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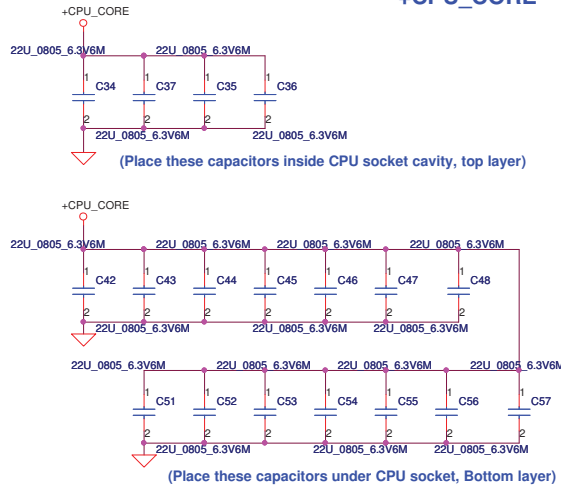


+CPU_CORE:112A



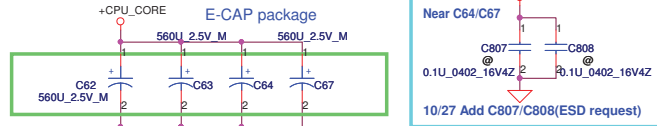
CPU POWER
6 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

+CPU_CORE

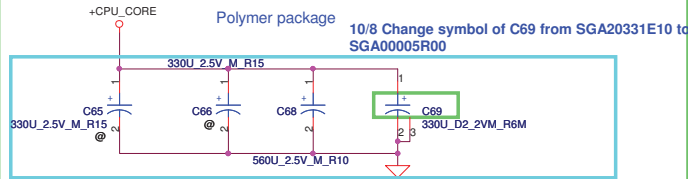


(Place these capacitors inside CPU socket cavity, top layer)

(Place these capacitors under CPU socket, Bottom layer)

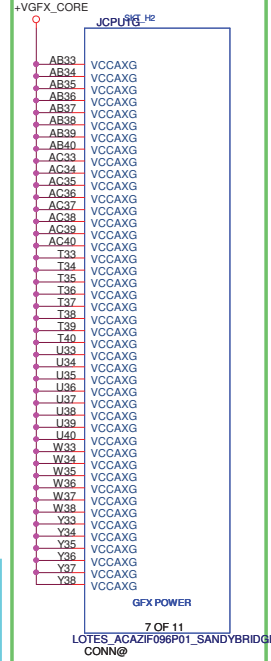


8/24 Change symbol of C62-C63 from SF000001P00 to SF000001K00
(Place C62-C64 capacitors under CPU socket, Top layer)



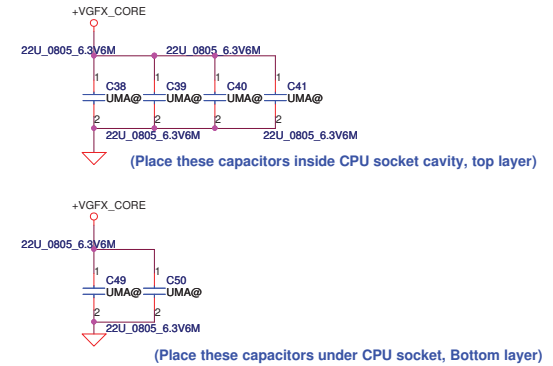
10/23 Change symbol of C65/C66/C68 from SGA20331E10 to SF000002M00
(Place C65-C69 capacitors under CPU socket, Bottom layer)
11/2 Change PN of C68 from SF000002M00 to SF000001K00

+VGFX_CORE:35A



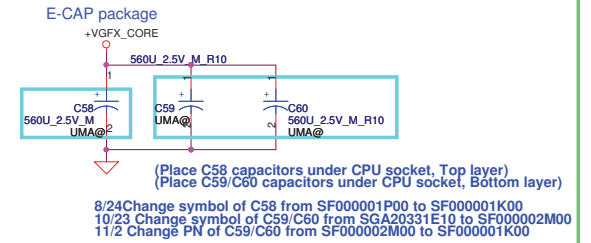
GFX POWER
7 OF 11
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@

+VGFX_CORE

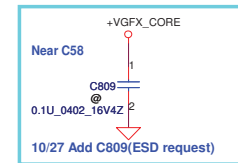


(Place these capacitors inside CPU socket cavity, top layer)

(Place these capacitors under CPU socket, Bottom layer)

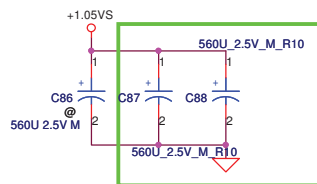
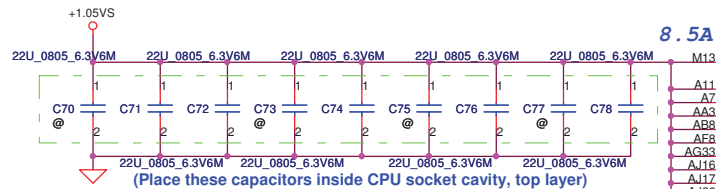


(Place C58 capacitors under CPU socket, Top layer)
(Place C59/C60 capacitors under CPU socket, Bottom layer)
8/24 Change symbol of C58 from SF000001P00 to SF000001K00
10/23 Change symbol of C59/C60 from SGA20331E10 to SF000002M00
11/2 Change PN of C59/C60 from SF000002M00 to SF000001K00



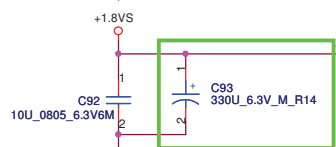
Near C58
0.1U_0402_16V4Z
10/27 Add C89(ESD request)

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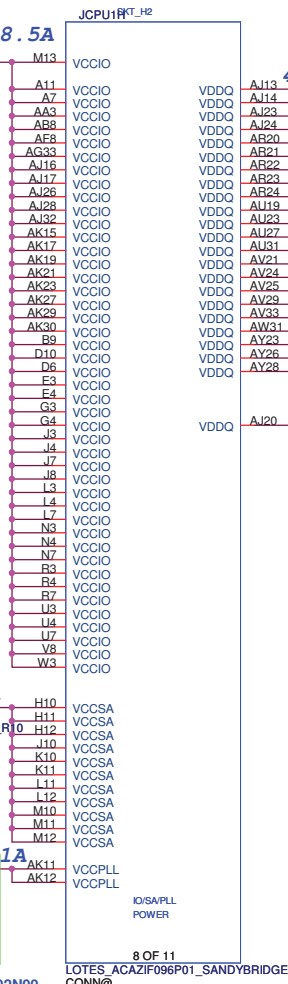


11/2 Change PN of C87/C88 from SF000001P00 to SF000001K00

11/4 Change PN of C91 from SF000001P00 to SF000001K00

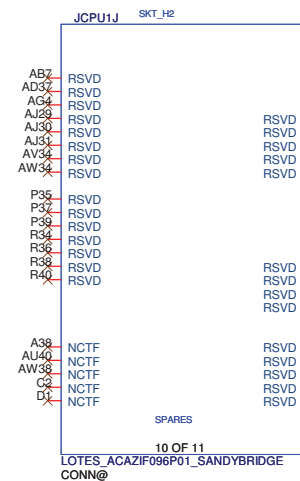
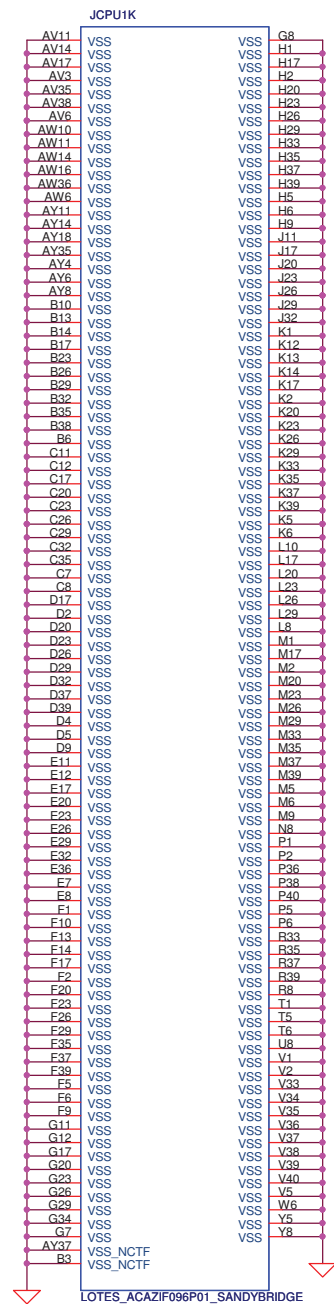
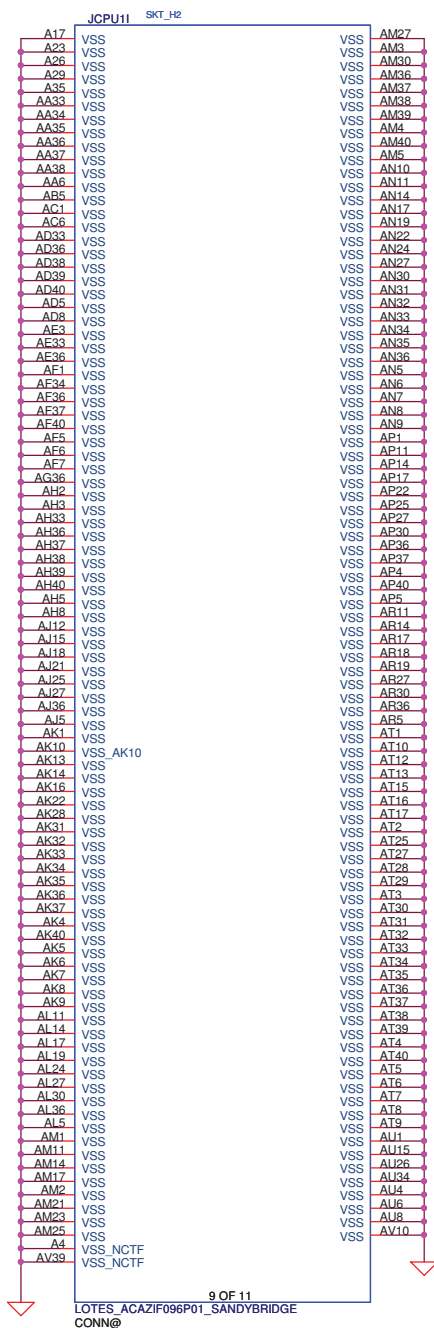


10/23 Change symbol of C93 from SGA00000Y80 to SF000002N00
11/4 Change PN of C93 from SF000002N00 to SF000001G00

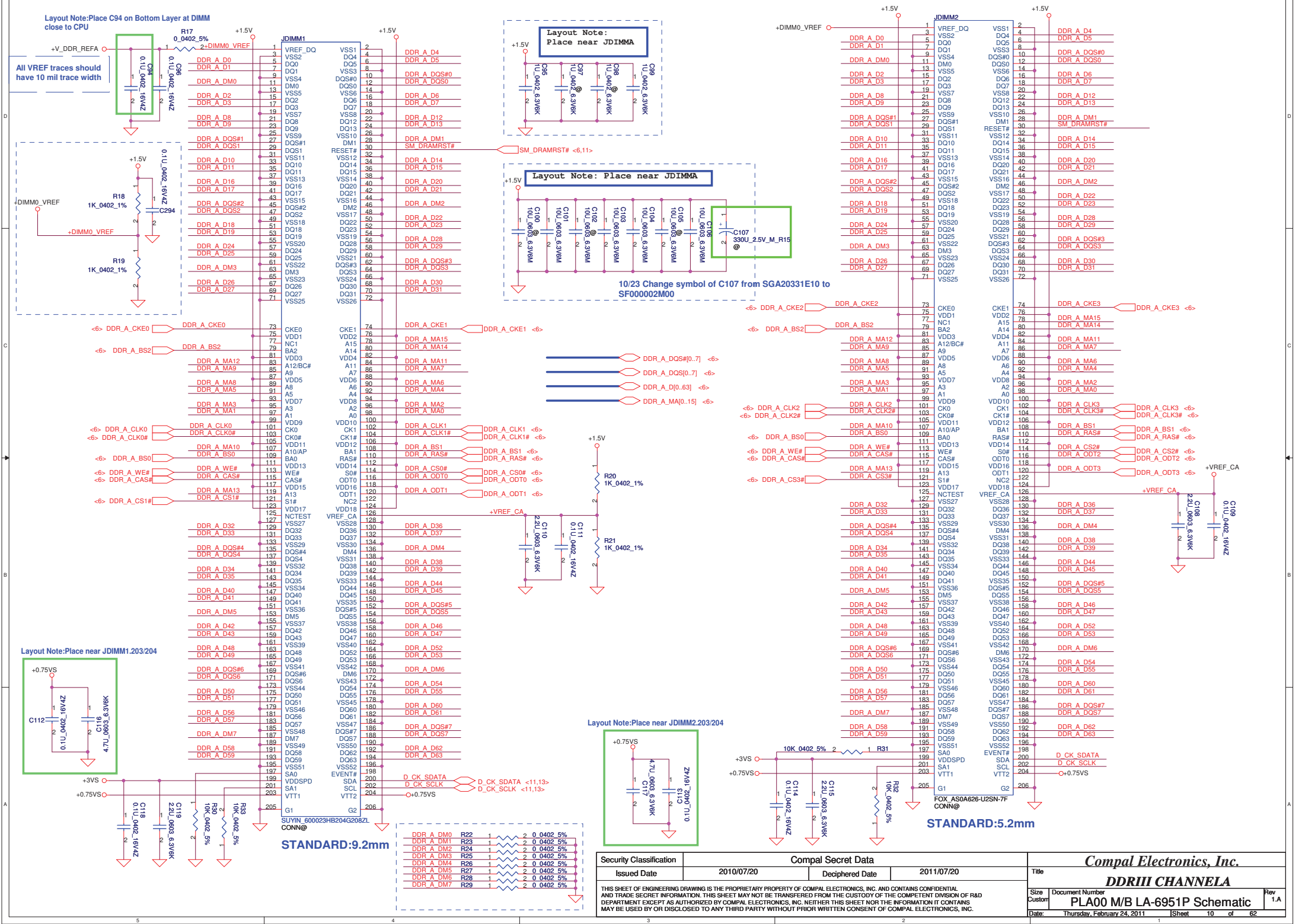


11/2 Change PN of C984/C985 from SF000002000 to SF000001K00

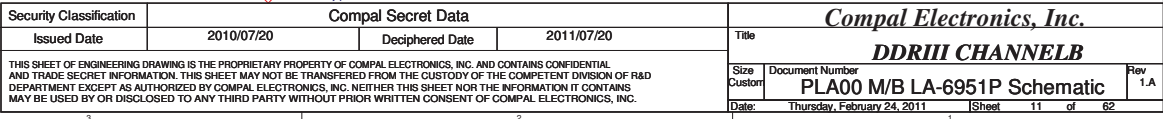
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<41> HDA_BITCLK_AUDIO < R69 1 2 HDA_BITCLK_PCH 33_0402_5%

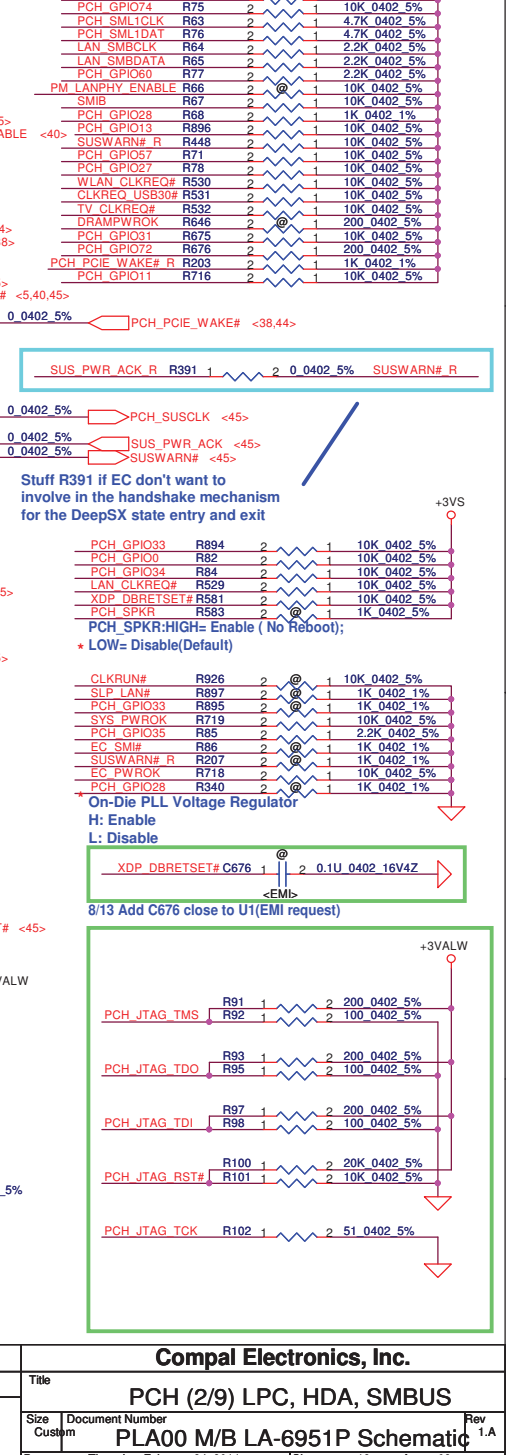
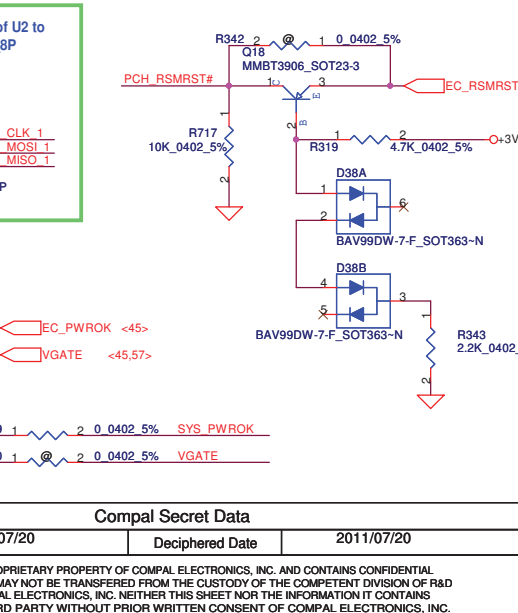
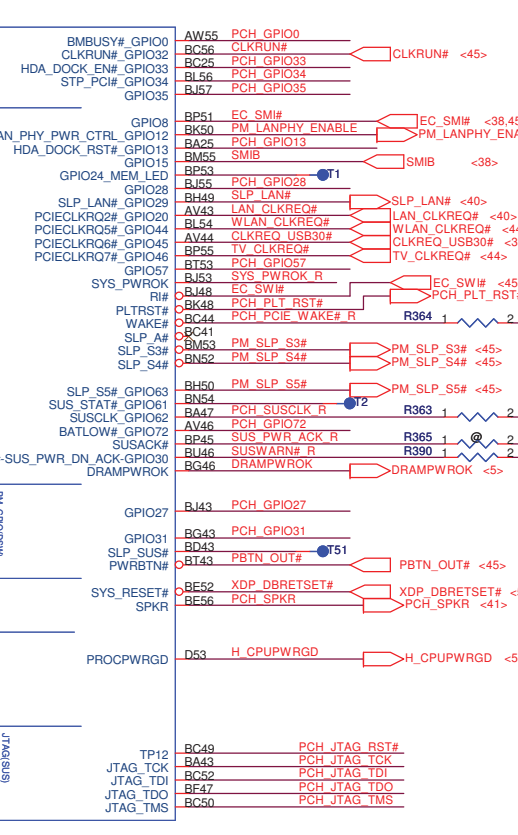
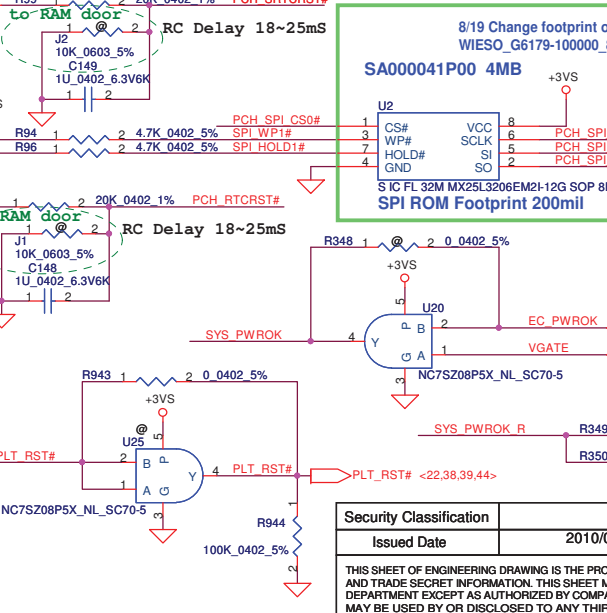
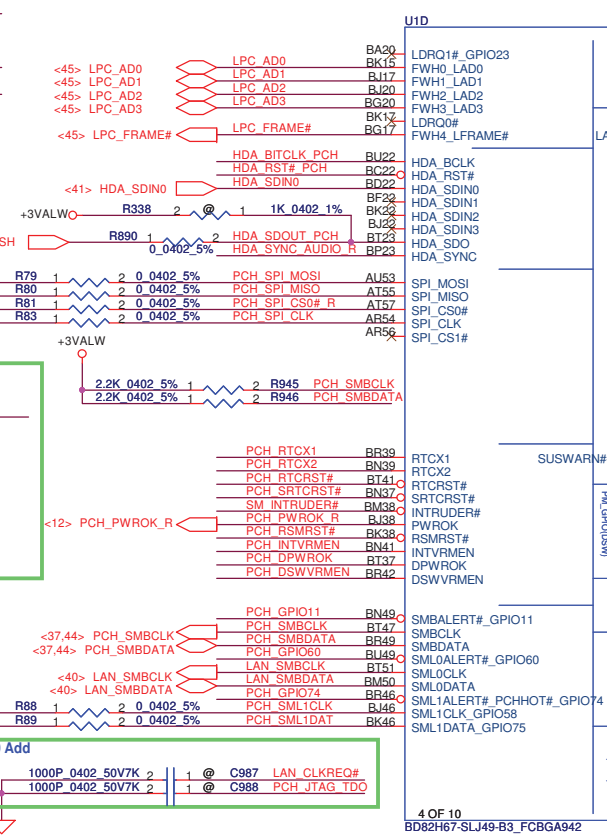
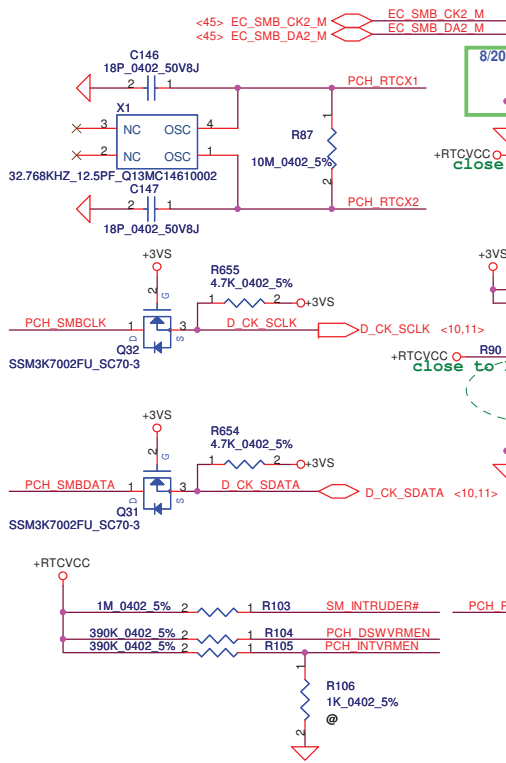
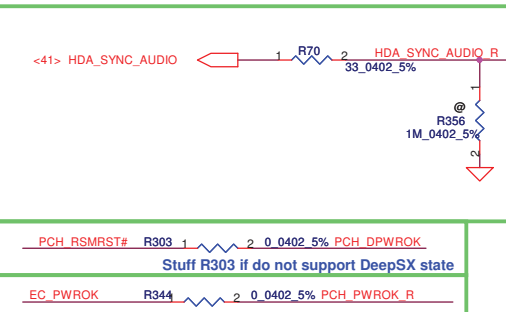
<41> HDA_RST#_AUDIO < R72 1 2 HDA_RST#_PCH 33_0402_5%

<41> HDA_SDOUT_AUDIO < R73 1 2 HDA_SDOUT_PCH 33_0402_5%

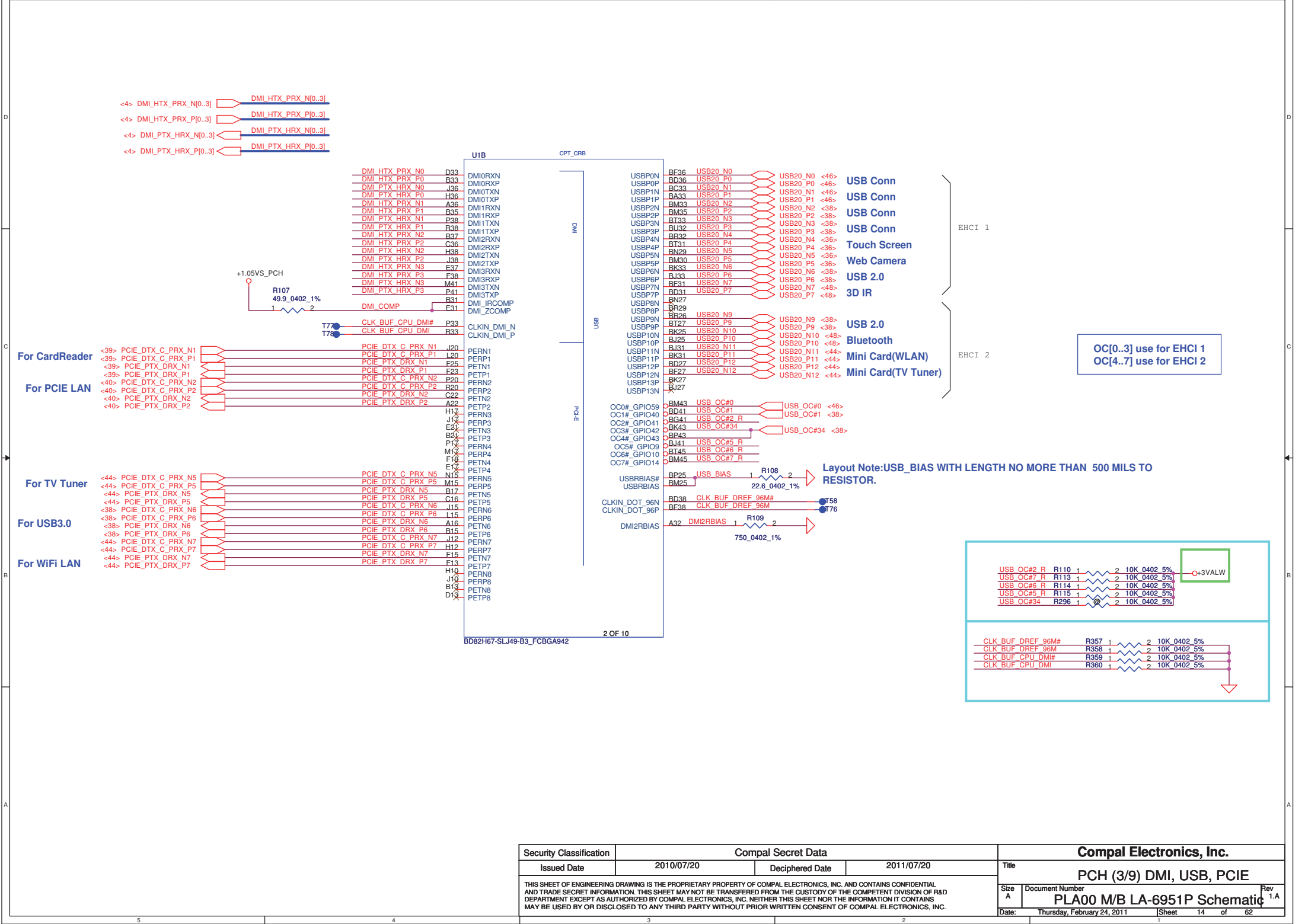
ME debug mode,
this signal has a weak internal pull down

★ Low = Disable (default)
High = Enable (flash descriptor security override)

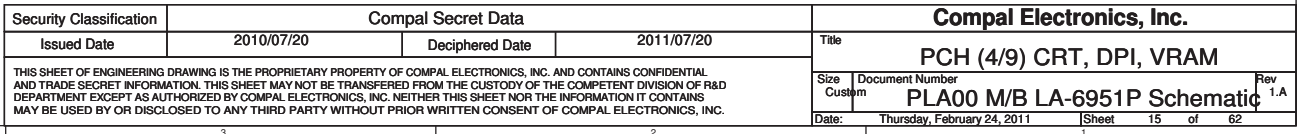
This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
*Need to pull high for Huron River platform

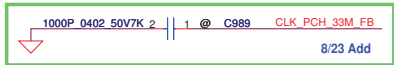
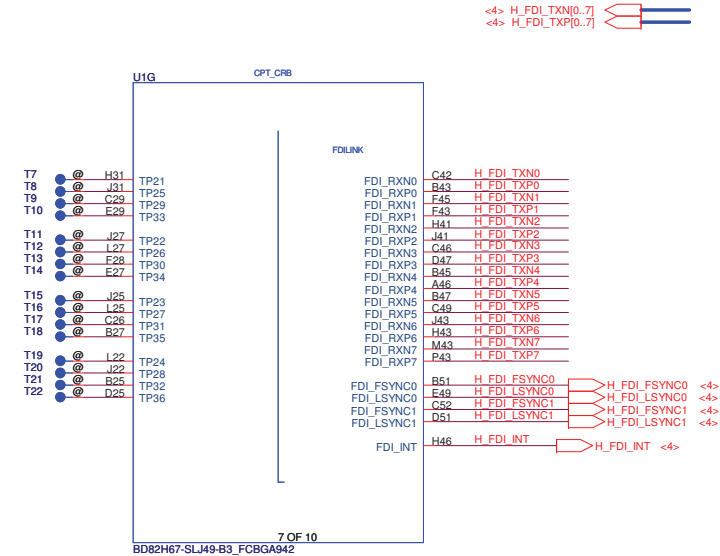
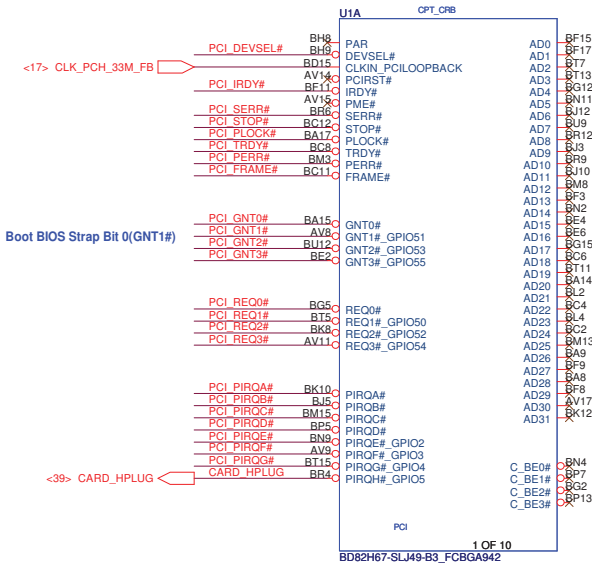
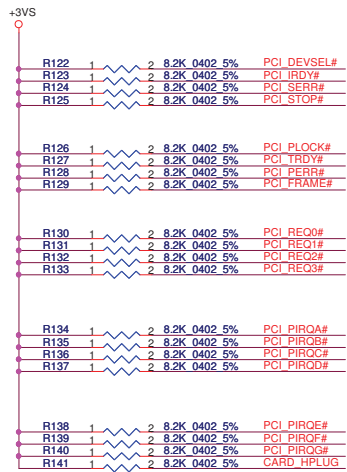


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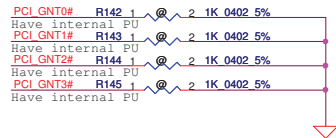


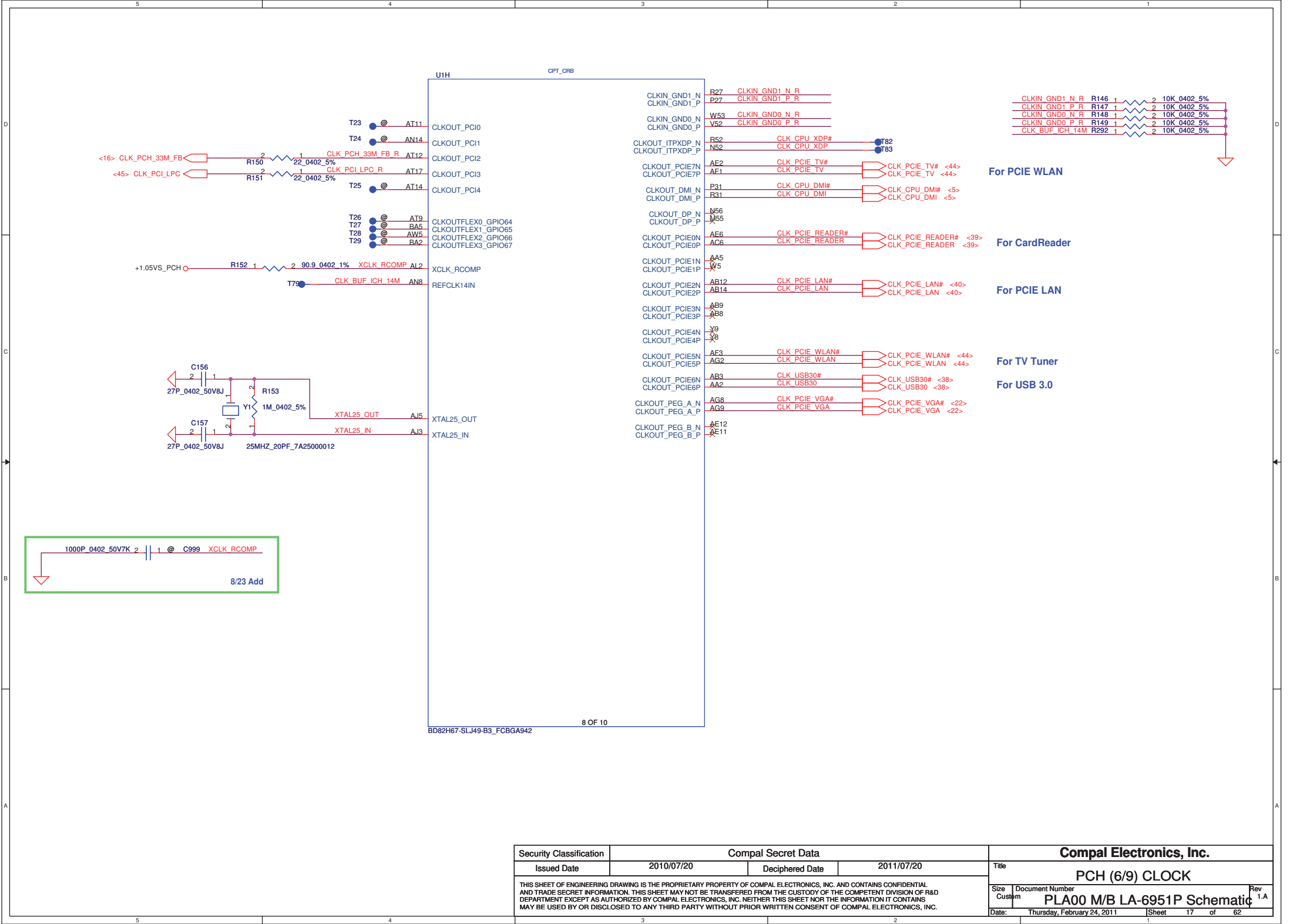
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Size A	Document Number	PLA00 M/B LA-6951P Schematic		Rev	1.A
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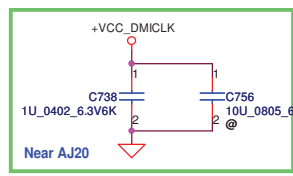
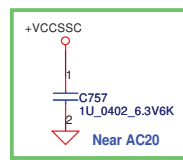
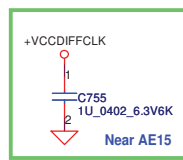
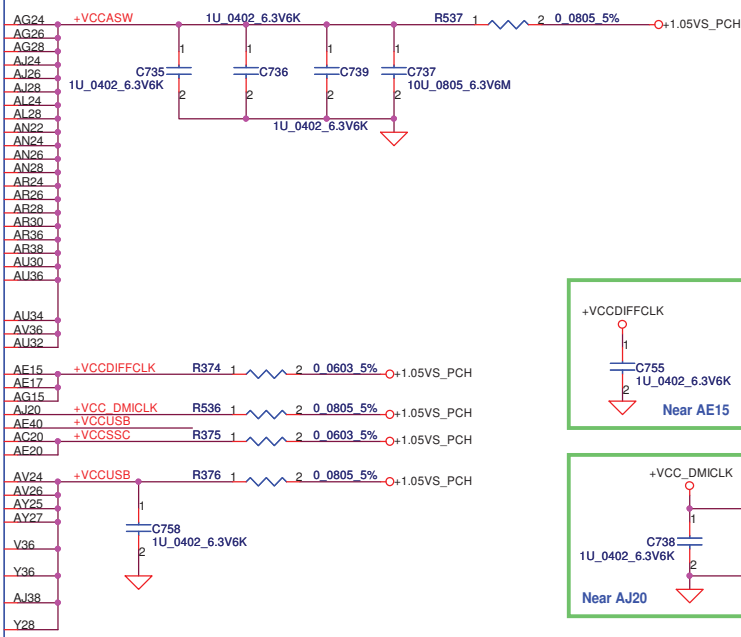
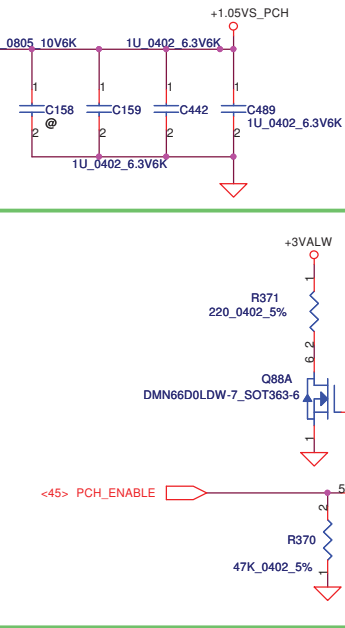
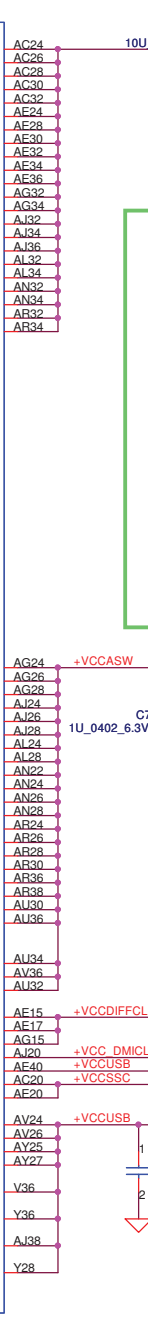
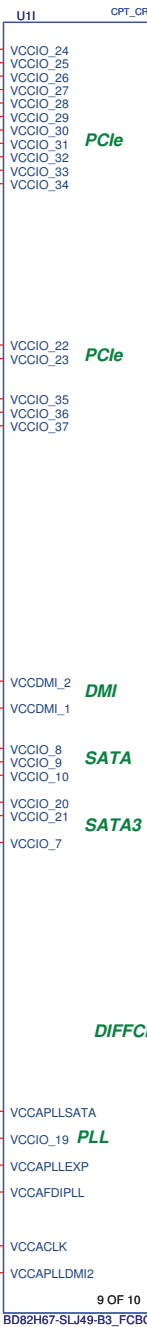
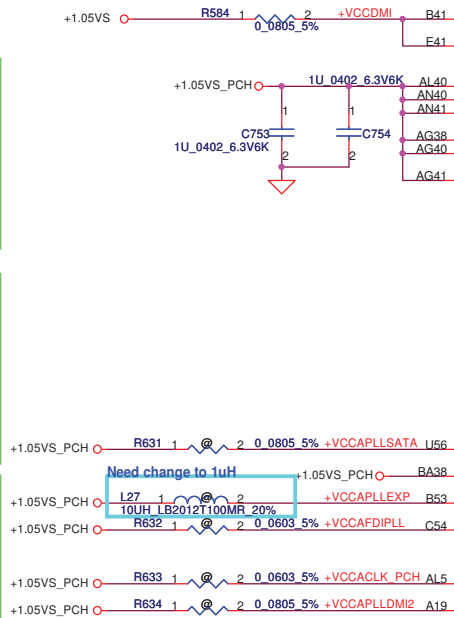
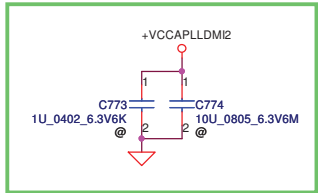
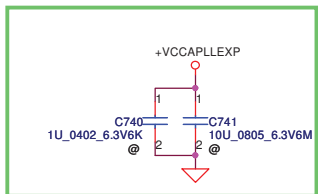
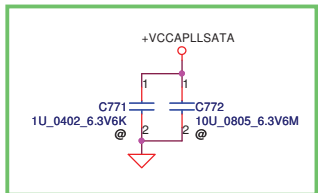
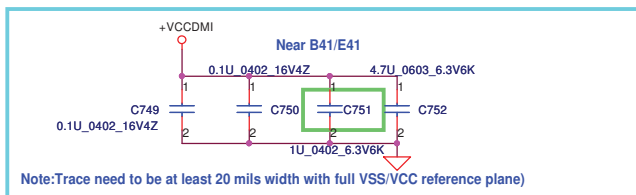
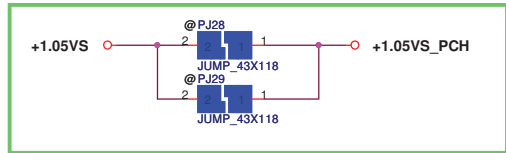
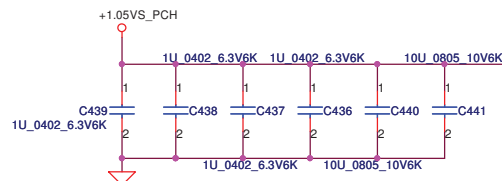


Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

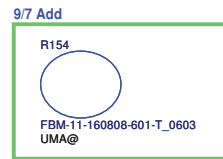
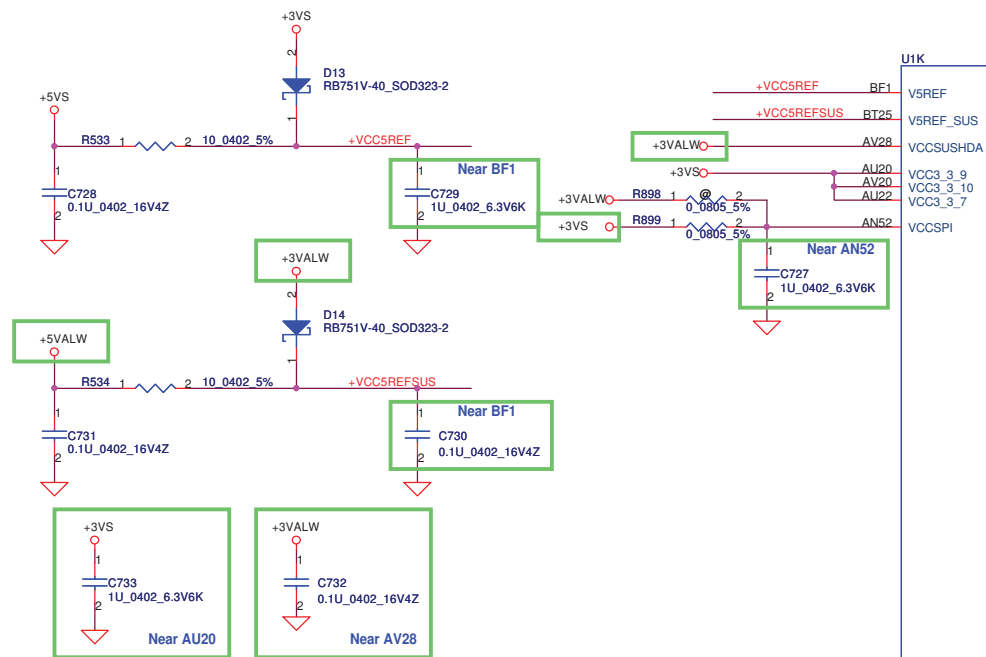




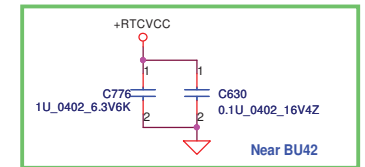
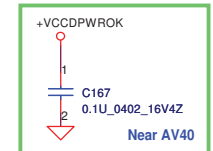
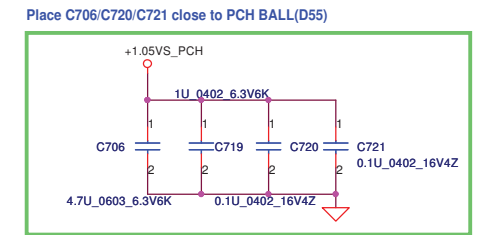
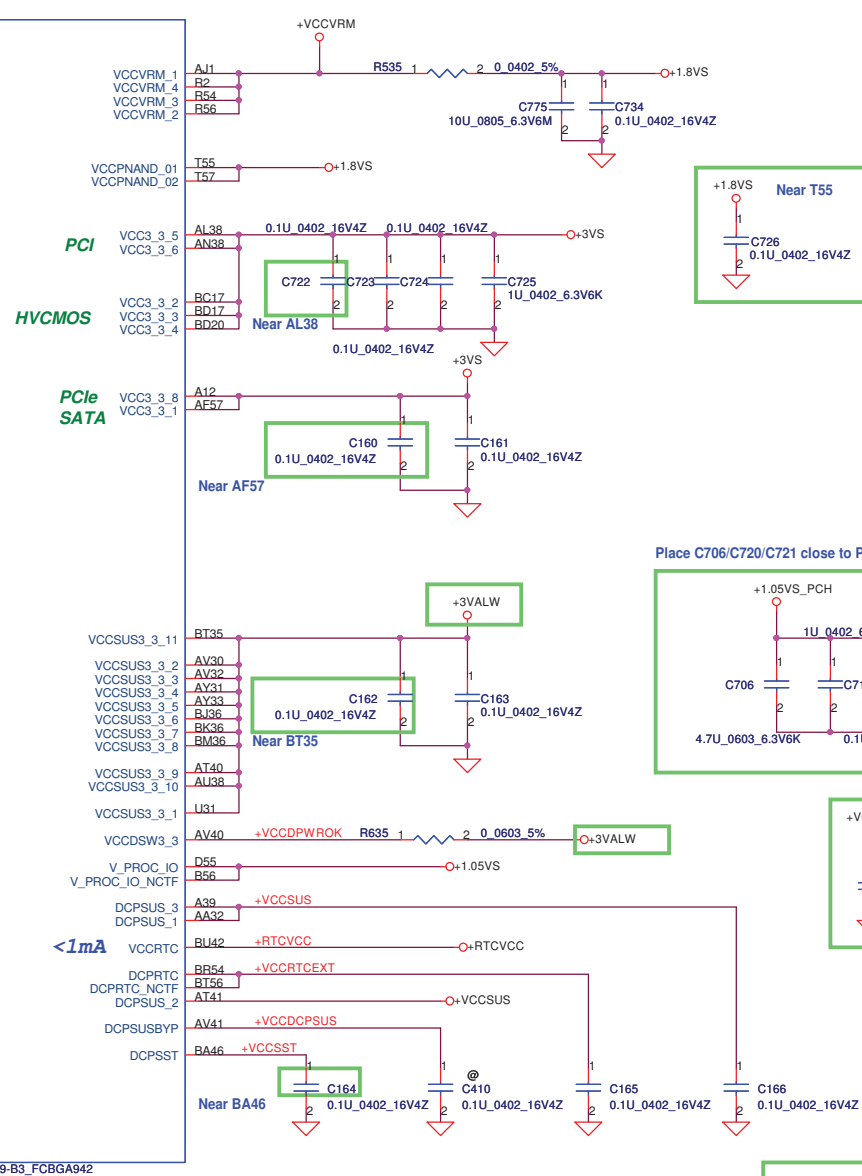
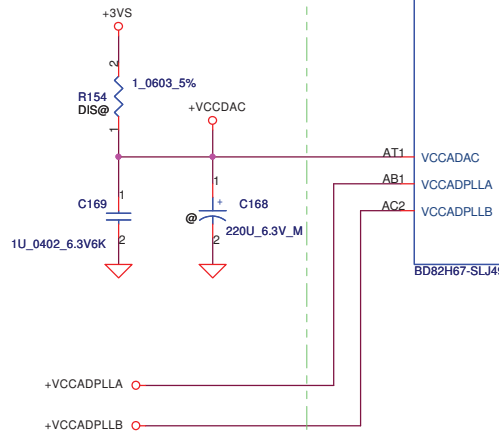
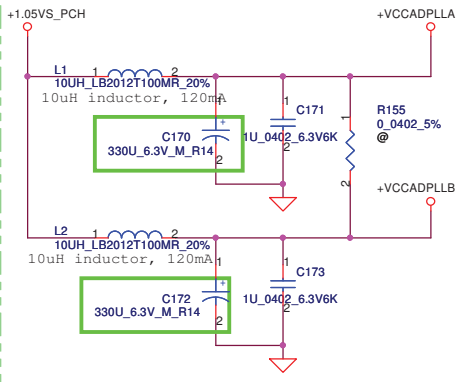
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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
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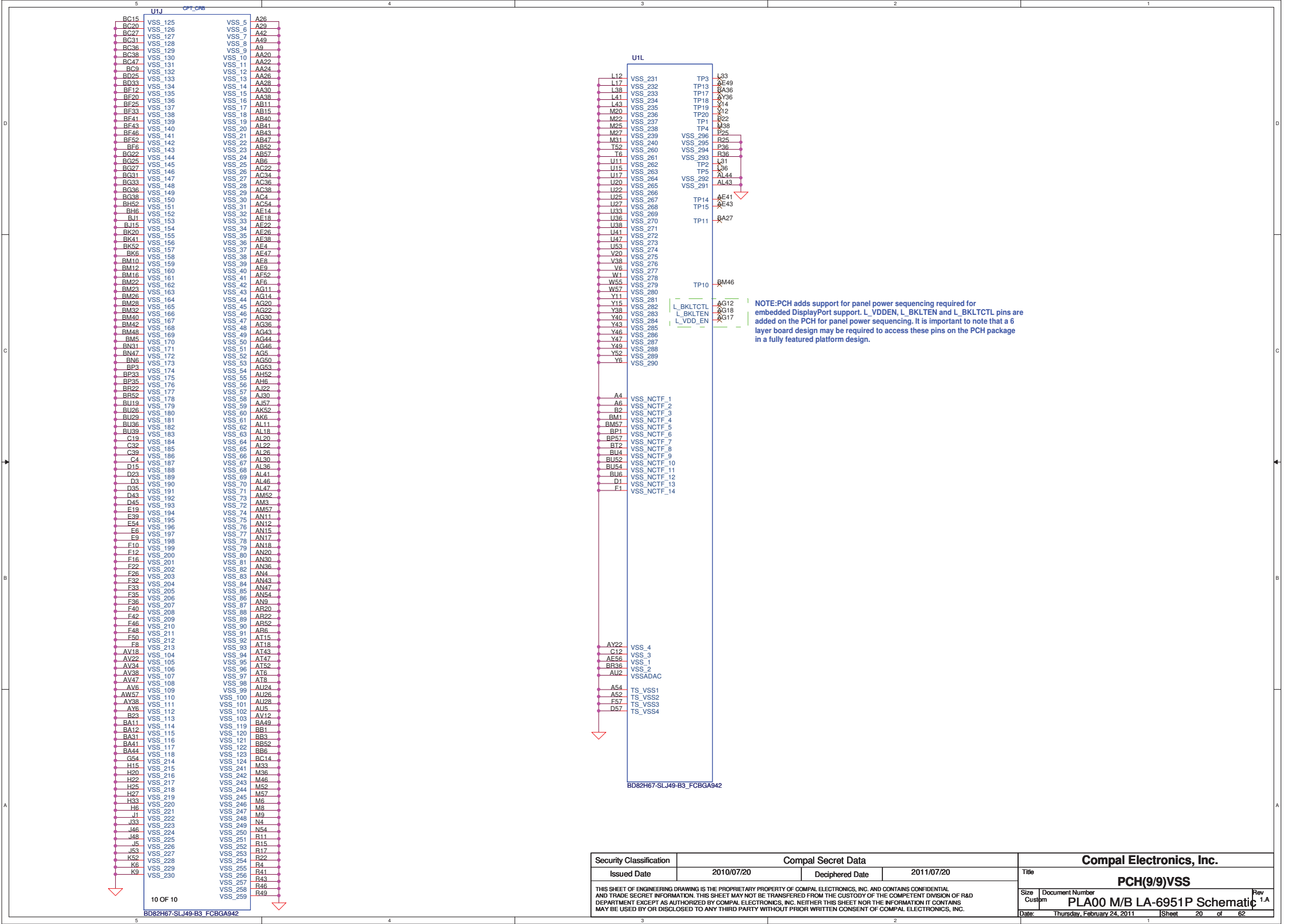
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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
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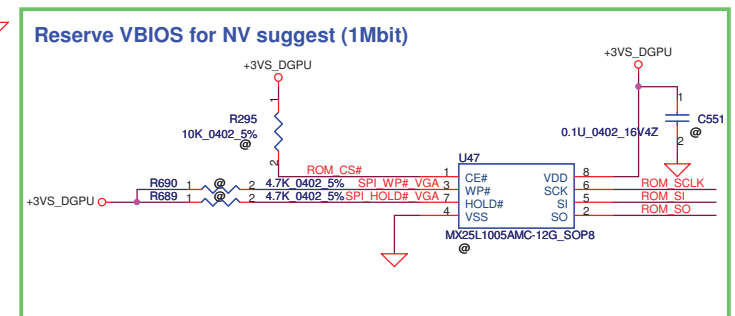
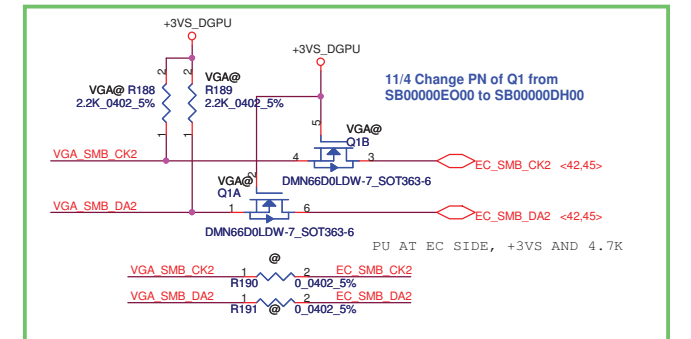
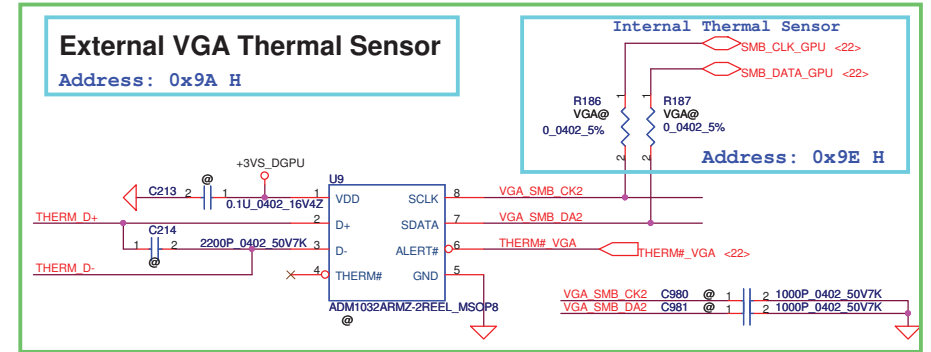
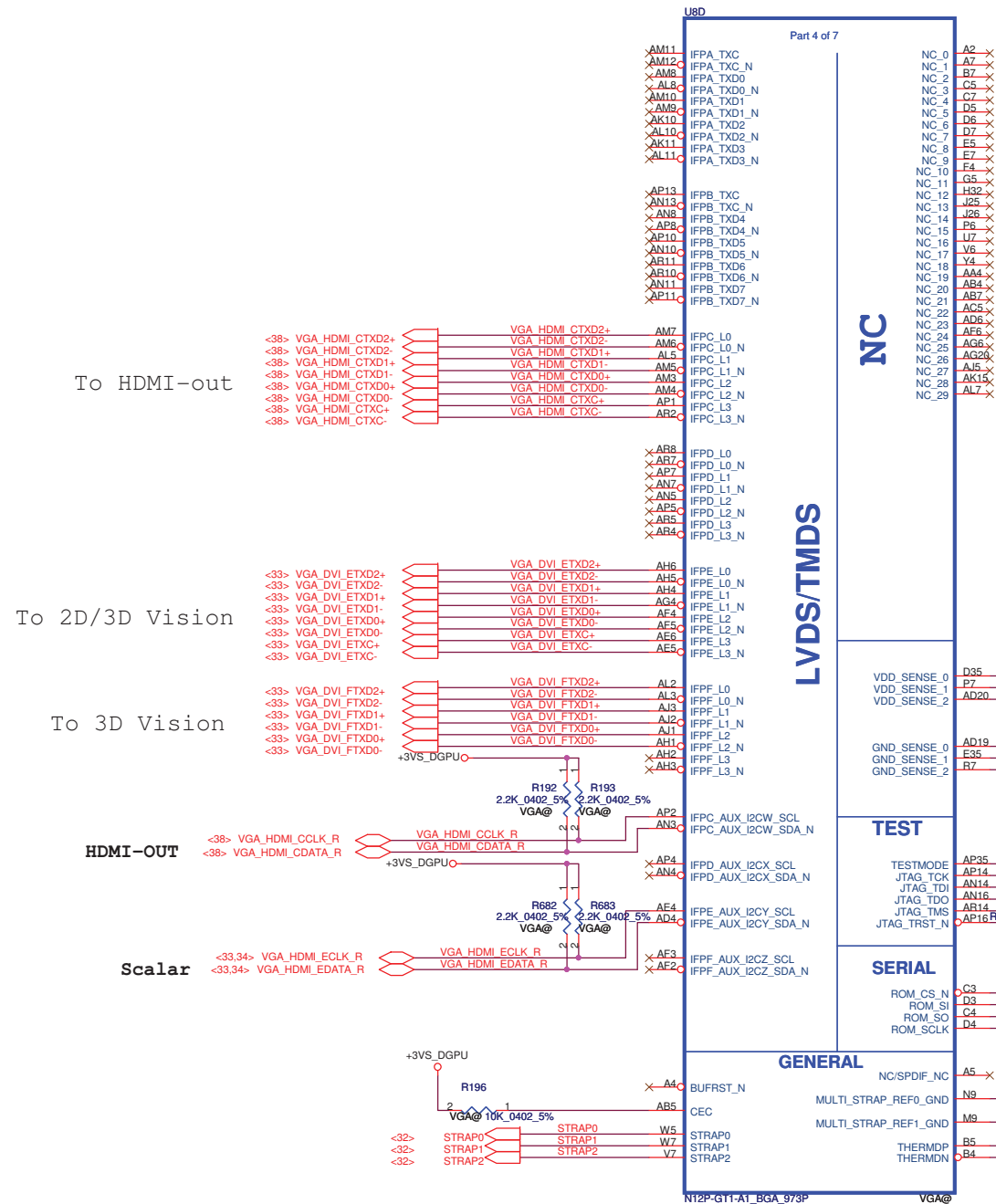


11/4 Change PN of C170/C172 from SF000002Y00 to SF000001G00

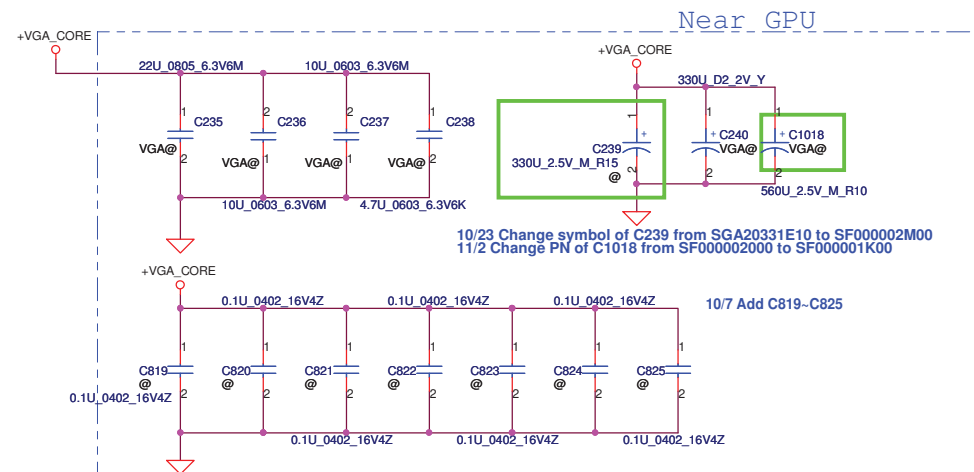
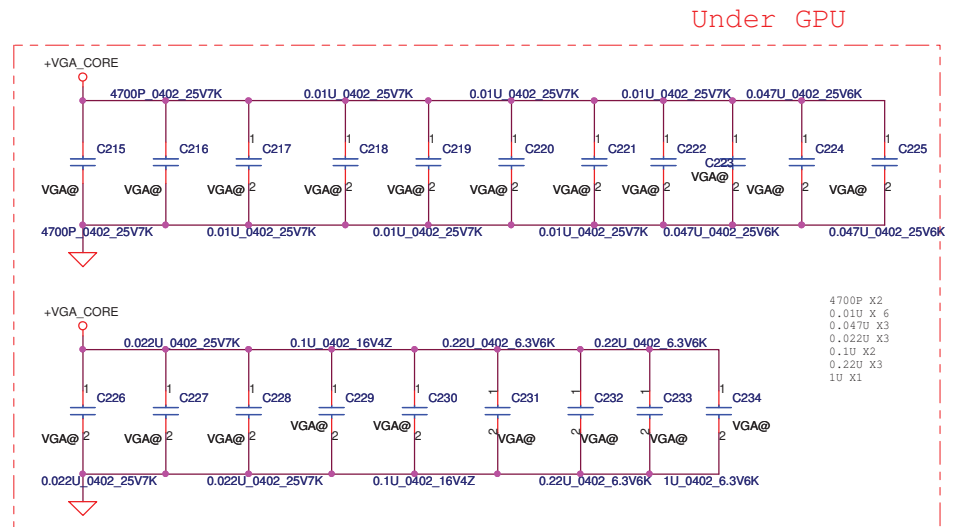
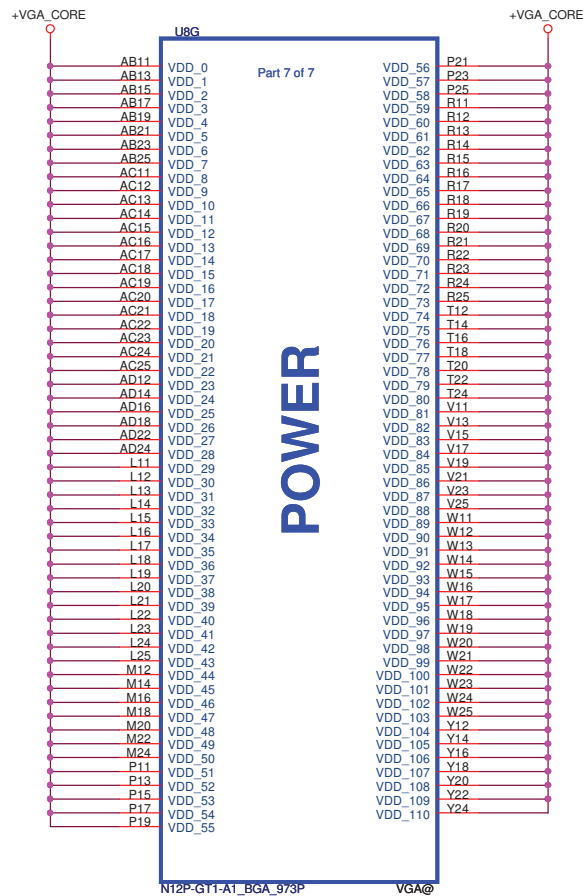


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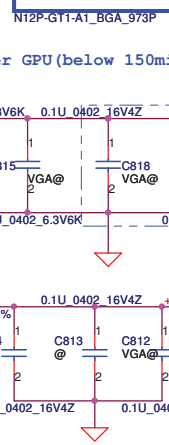
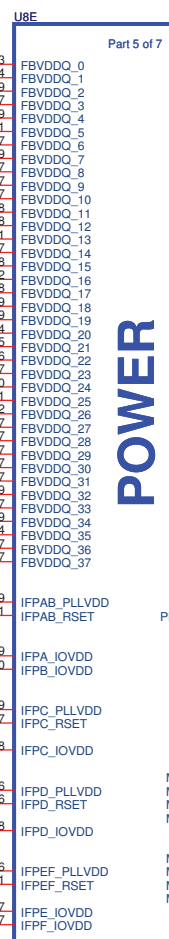
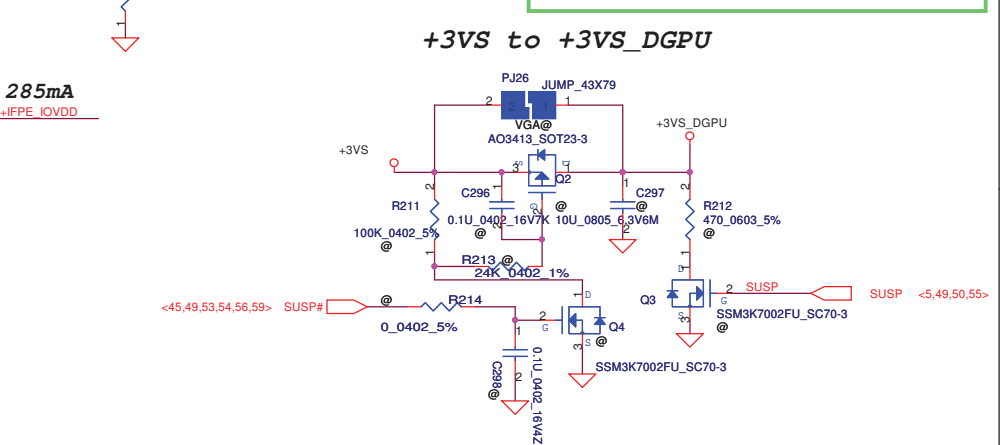
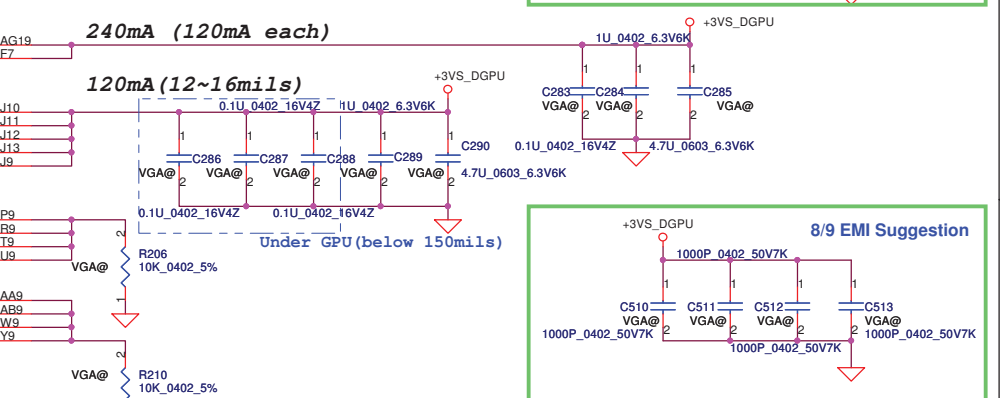
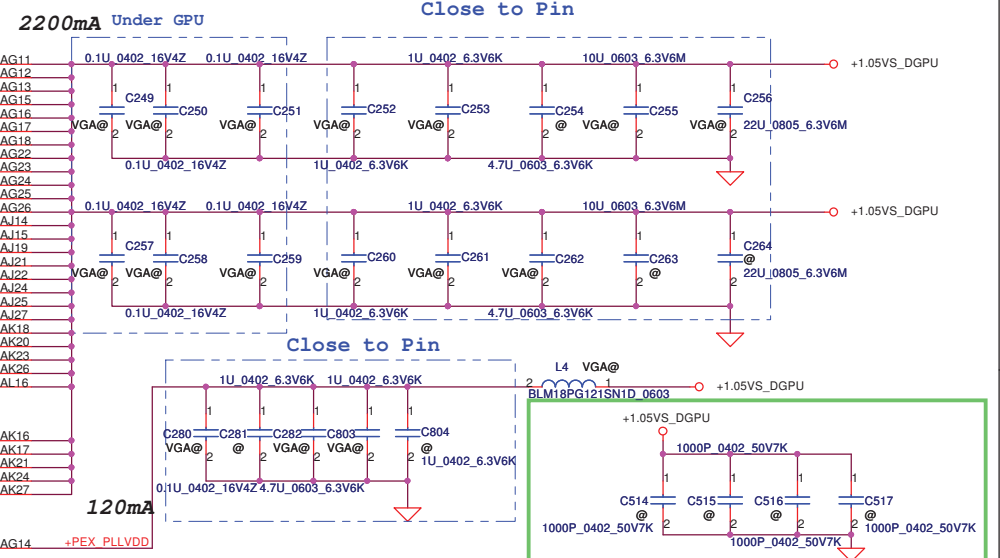
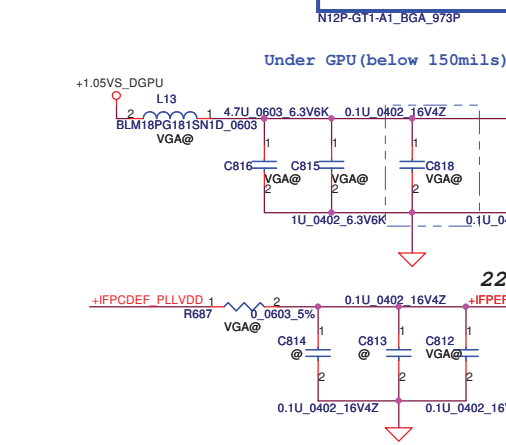
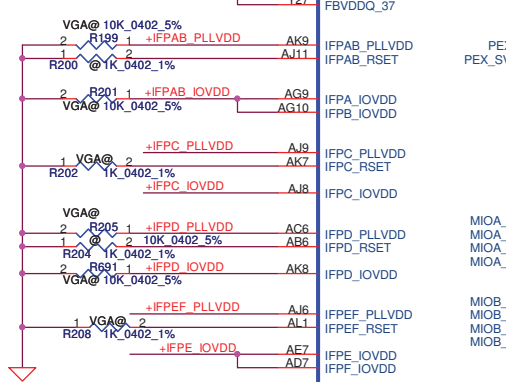
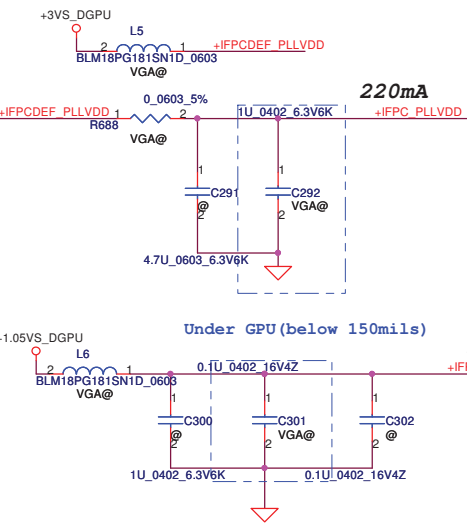
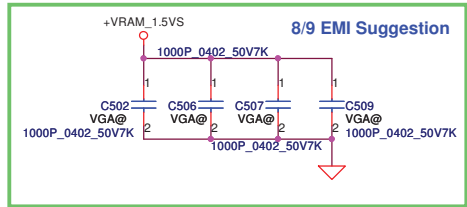
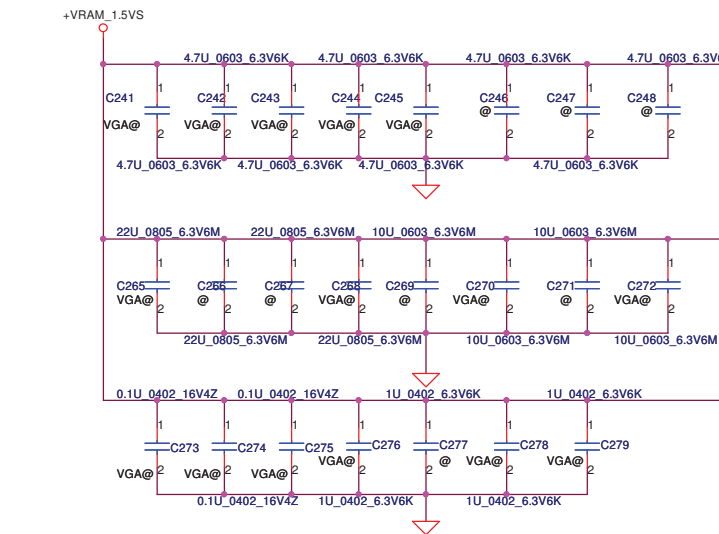




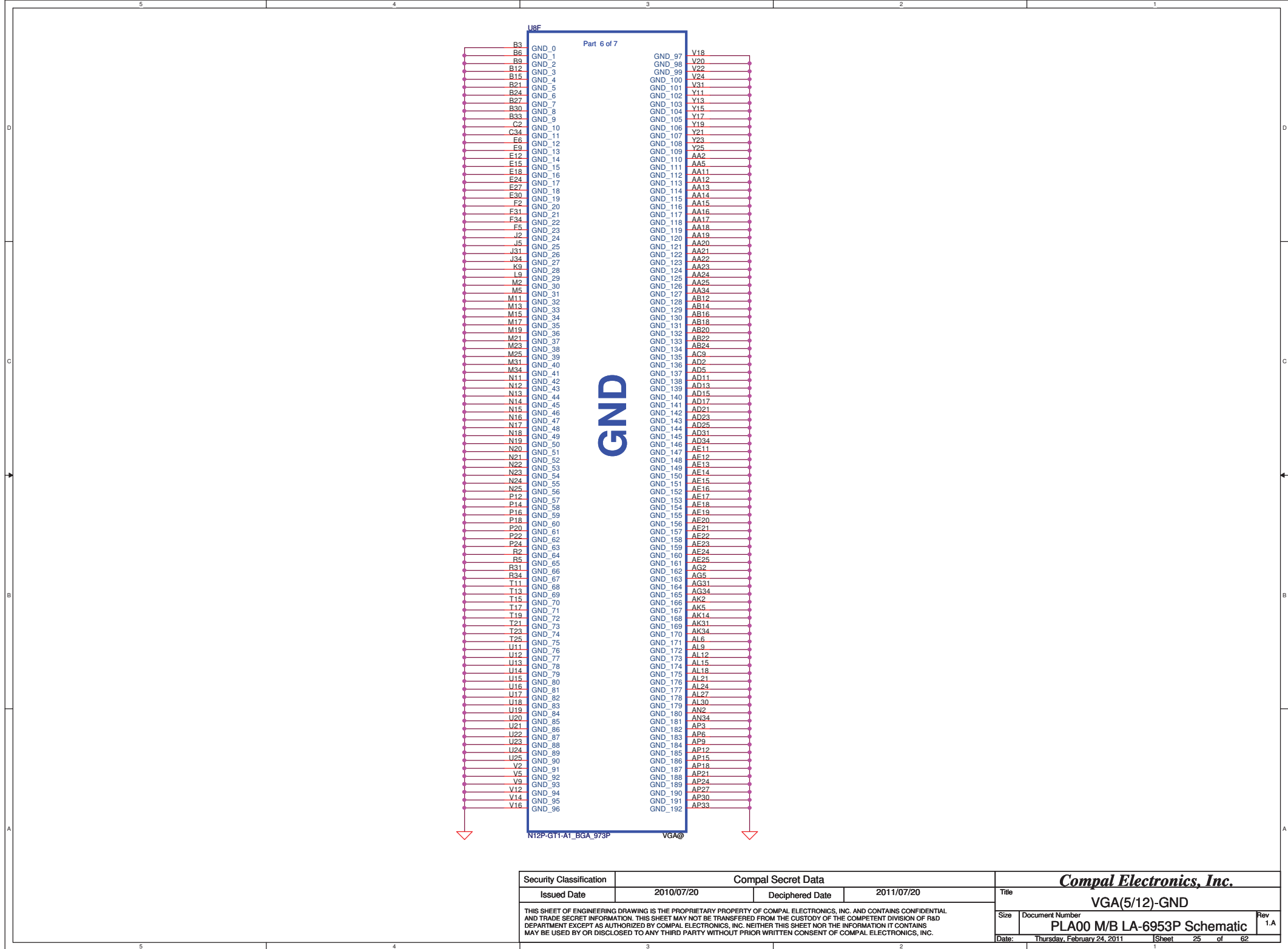
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D

C

B

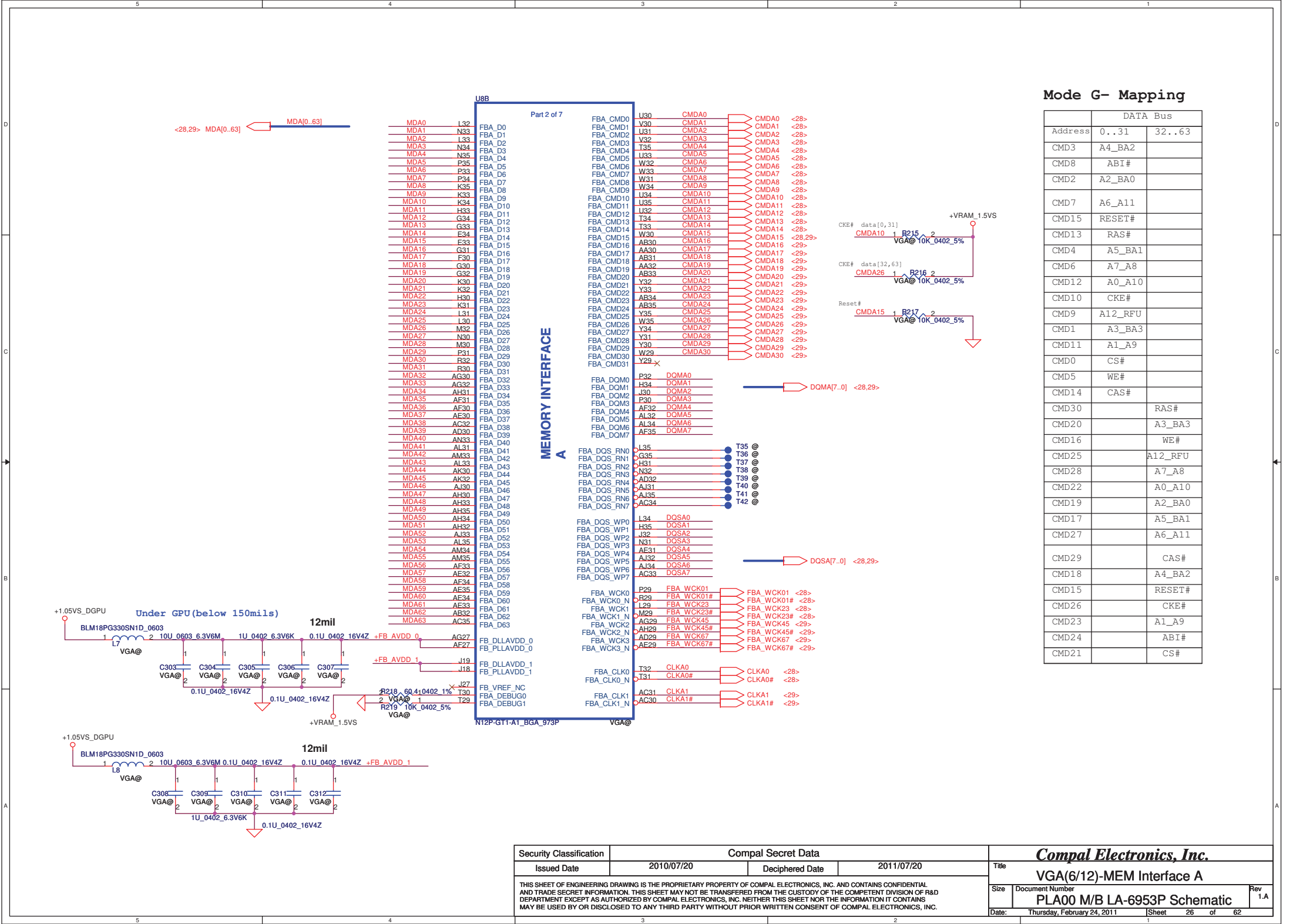
A

D

C

B

A



Mode G- Mapping

Address	DATA Bus
CMD3	A4_BA2
CMD8	ABI#
CMD2	A2_BA0
CMD7	A6_A11
CMD15	RESET#
CMD13	RAS#
CMD4	A5_BA1
CMD6	A7_A8
CMD12	A0_A10
CMD10	CKE#
CMD9	A12_RFU
CMD1	A3_BA3
CMD11	A1_A9
CMD0	CS#
CMD5	WE#
CMD14	CAS#
CMD30	RAS#
CMD20	A3_BA3
CMD16	WE#
CMD25	A12_RFU
CMD28	A7_A8
CMD22	A0_A10
CMD19	A2_BA0
CMD17	A5_BA1
CMD27	A6_A11
CMD29	CAS#
CMD18	A4_BA2
CMD15	RESET#
CMD26	CKE#
CMD23	A1_A9
CMD24	ABI#
CMD21	CS#

<30,31> MDB[0..63]

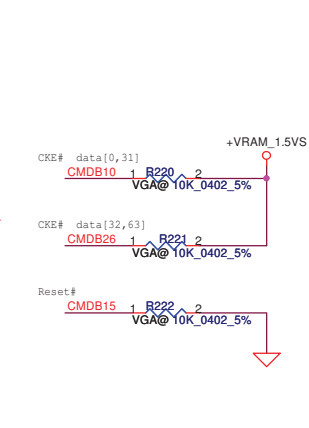
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MDB1 D13
MDB2 A13
MDB3 A14
MDB4 C16
MDB5 B16
MDB6 A17
MDB7 D16
MDB8 C13
MDB9 B11
MDB10 C11
MDB11 A11
MDB12 C10
MDB13 B8
MDB14 B8
MDB15 A8
MDB16 A8
MDB17 F8
MDB18 F10
MDB19 F9
MDB20 D8
MDB21 D8
MDB22 D11
MDB23 E11
MDB24 D12
MDB25 E13
MDB26 F13
MDB27 F14
MDB28 F15
MDB29 F16
MDB30 F16
MDB31 F17
MDB32 D29
MDB33 F27
MDB34 F28
MDB35 E28
MDB36 D26
MDB37 F25
MDB38 D24
MDB39 E25
MDB40 E32
MDB41 E32
MDB42 D33
MDB43 E31
MDB44 C33
MDB45 F29
MDB46 D30
MDB47 E29
MDB48 B29
MDB49 C31
MDB50 C29
MDB51 B31
MDB52 C32
MDB53 B32
MDB54 B35
MDB55 B34
MDB56 A29
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MDB61 D25
MDB62 B25
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U8C

Part 3 of 7

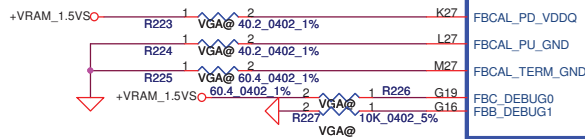
MEMORY INTERFACE C

FBC_CMD0 E18
FBC_CMD1 E19
FBC_CMD2 G17
FBC_CMD3 E19
FBC_CMD4 C19
FBC_CMD5 C19
FBC_CMD6 B17
FBC_CMD7 E20
FBC_CMD8 B19
FBC_CMD9 D20
FBC_CMD9A A19
FBC_CMD10 D19
FBC_CMD11 C20
FBC_CMD12 F20
FBC_CMD13 B20
FBC_CMD14 G21
FBC_CMD15 F22
FBC_CMD16 F24
FBC_CMD17 F23
FBC_CMD18 C25
FBC_CMD19 C23
FBC_CMD20 E22
FBC_CMD21 D21
FBC_CMD22 A23
FBC_CMD23 D22
FBC_CMD24 B23
FBC_CMD25 C22
FBC_CMD26 B22
FBC_CMD27 A22
FBC_CMD28 A20
FBC_CMD29 G20
FBC_CMD30
FBC_CMD31
FBC_DOM0 A16
FBC_DOM1 D10
FBC_DOM2 E11
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FBC_DOM4 D27
FBC_DOM5 D34
FBC_DOM6 A34
FBC_DOM7 D28
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FBC_DQS_RN1 B10
FBC_DQS_RN2 D9
FBC_DQS_RN3 E14
FBC_DQS_RN4 F26
FBC_DQS_RN5 D31
FBC_DQS_RN6 A31
FBC_DQS_RN7 A26
FBC_DQS_WP0 C14
FBC_DQS_WP1 A10
FBC_DQS_WP2 E10
FBC_DQS_WP3 D14
FBC_DQS_WP4 F26
FBC_DQS_WP5 D32
FBC_DQS_WP6 A32
FBC_DQS_WP7 B26
FBC_WCK0 G14
FBC_WCK0_N G15
FBC_WCK1 G11
FBC_WCK1_N G12
FBC_WCK2 G27
FBC_WCK2_N G28
FBC_WCK3 G24
FBC_WCK3_N G25
FBC_CLK0 E17
FBC_CLK0_N D17
FBC_CLK1 D23
FBC_CLK1_N E23
FBB_WCK01# G15
FBB_WCK01# G11
FBB_WCK23# G12
FBB_WCK23# G27
FBB_WCK45# G28
FBB_WCK45# G24
FBB_WCK67# G25
FBB_WCK67# G25
CLKB0# E17
CLKB0# D17
CLKB1# D23
CLKB1# E23



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DQSB[7..0] <30,31>



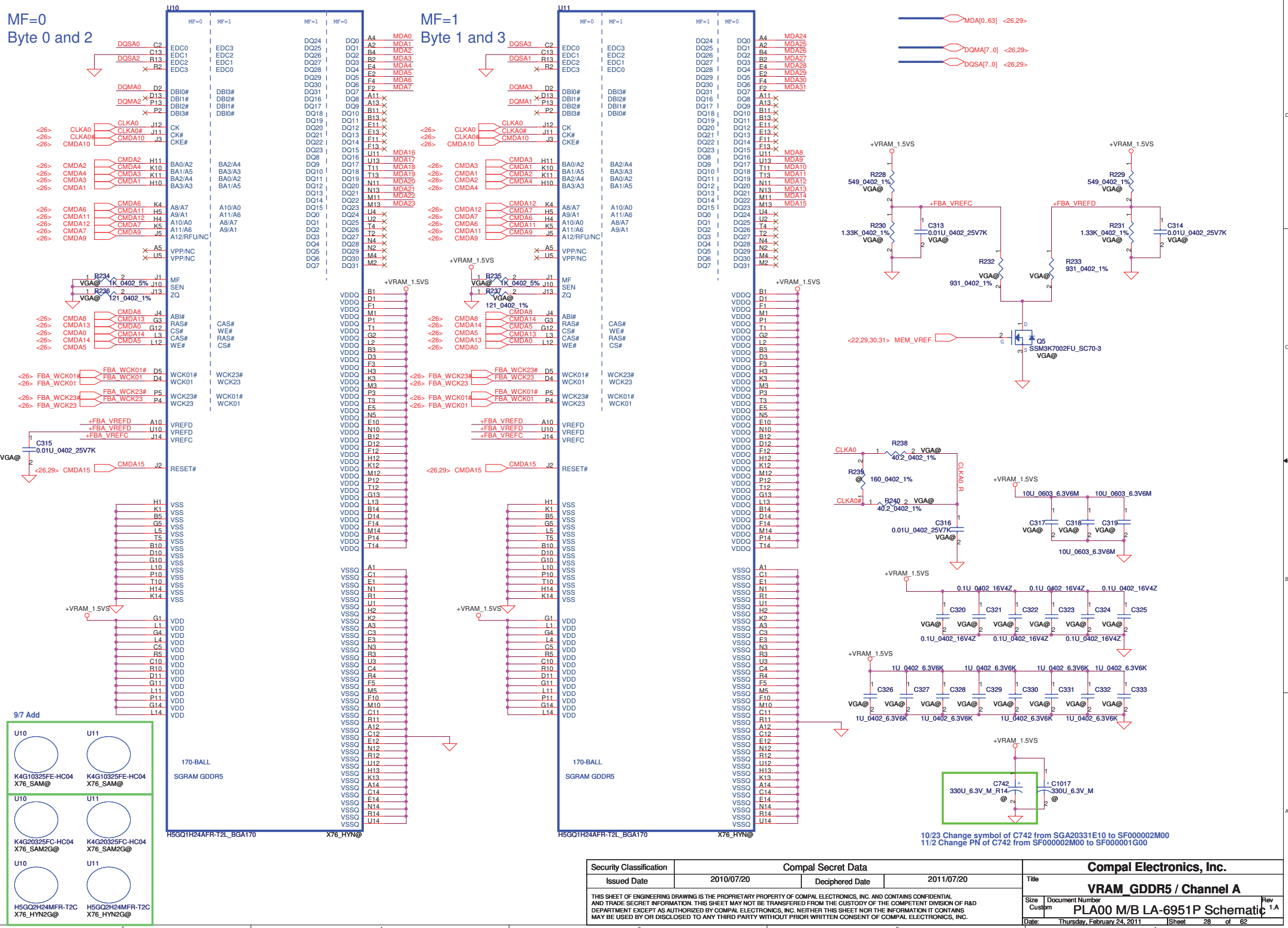
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VGA@

Mode G- Mapping

DATA Bus	
Address	0..31 32..63
CMD3	A4_BA2
CMD8	ABI#
CMD2	A2_BA0
CMD7	A6_A11
CMD15	RESET#
CMD13	RAS#
CMD4	A5_BA1
CMD6	A7_A8
CMD12	A0_A10
CMD10	CKE#
CMD9	A12_RFU
CMD1	A3_BA3
CMD11	A1_A9
CMD0	CS#
CMD5	WE#
CMD14	CAS#
CMD30	RAS#
CMD20	A3_BA3
CMD16	WE#
CMD25	A12_RFU
CMD28	A7_A8
CMD22	A0_A10
CMD19	A2_BA0
CMD17	A5_BA1
CMD27	A6_A11
CMD29	CAS#
CMD18	A4_BA2
CMD15	RESET#
CMD26	CKE#
CMD23	A1_A9
CMD24	ABI#
CMD21	CS#

MF=0
Byte 0 and 2



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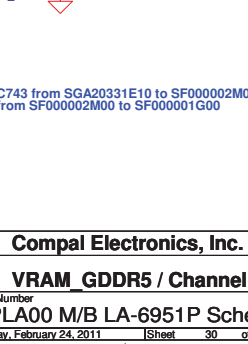
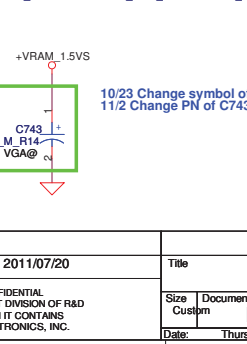
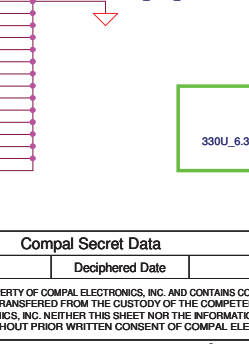
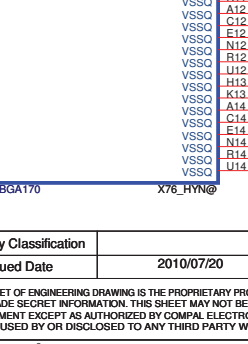
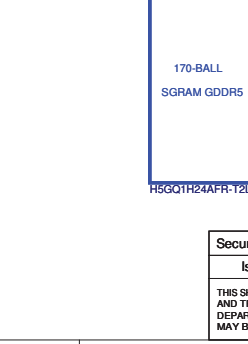
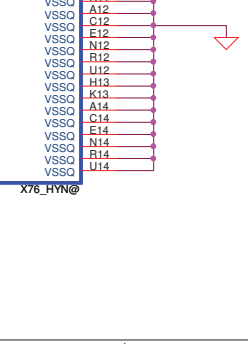
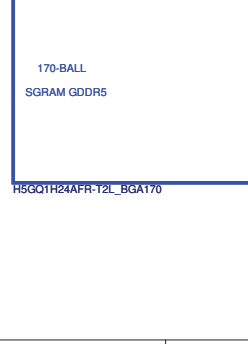
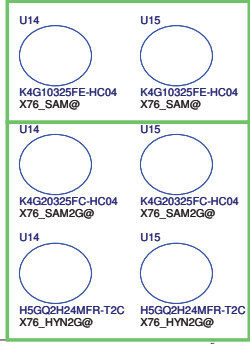
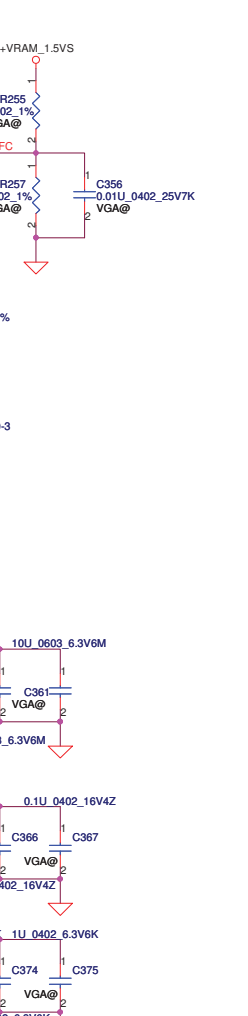
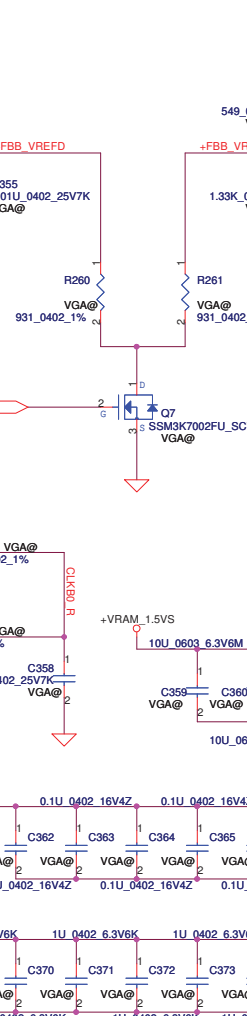
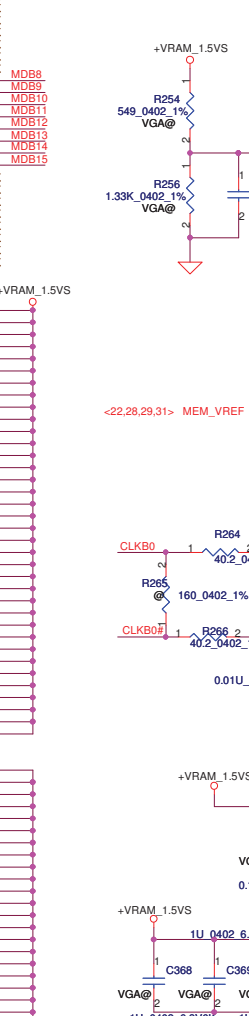
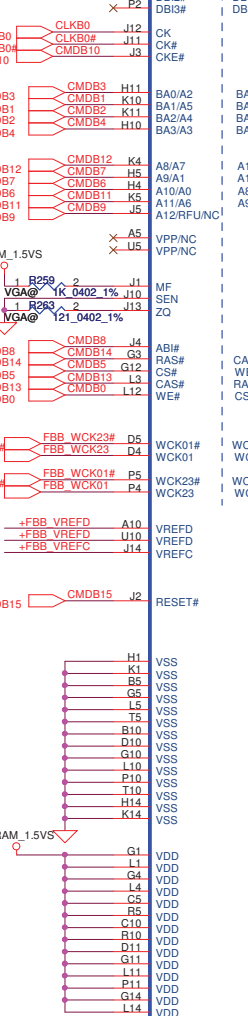
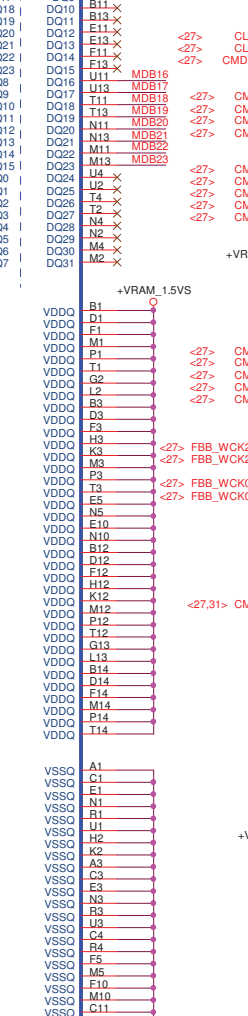
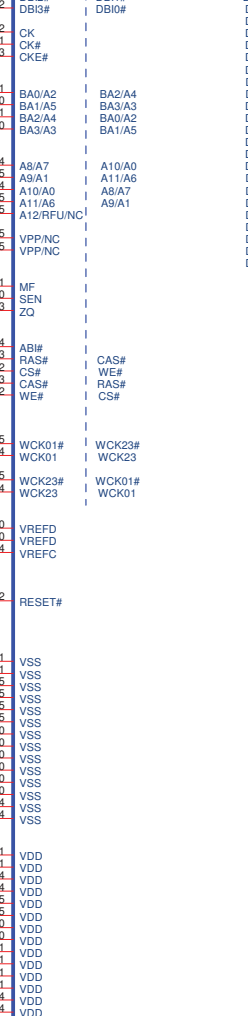
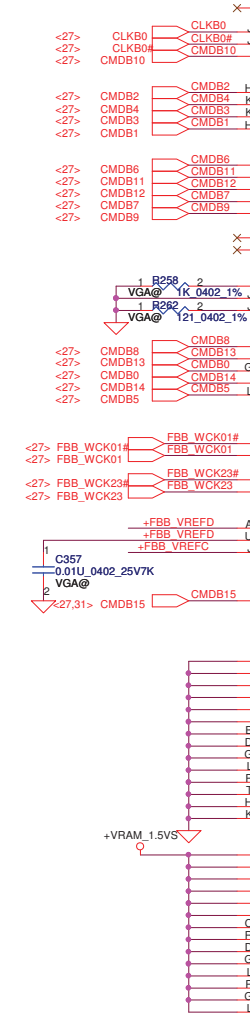


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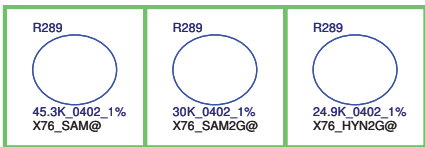
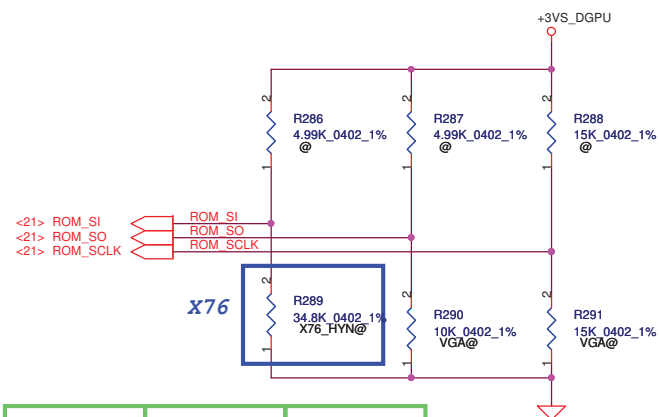
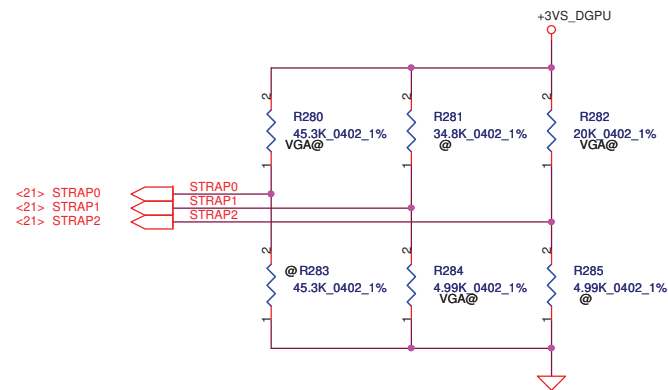
MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

MD[0..63] <27..31>
DOMB[7..0] <27..31>
DOMB[7..0] <27..31>



Security Classification		Compal Secret Data		Title	
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				PLA00 M/B LA-6951P Schematic	
				Date: Thursday, February 24, 2011	Sheet 30 of 62



Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0010	PD 15K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0011	PD 20K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

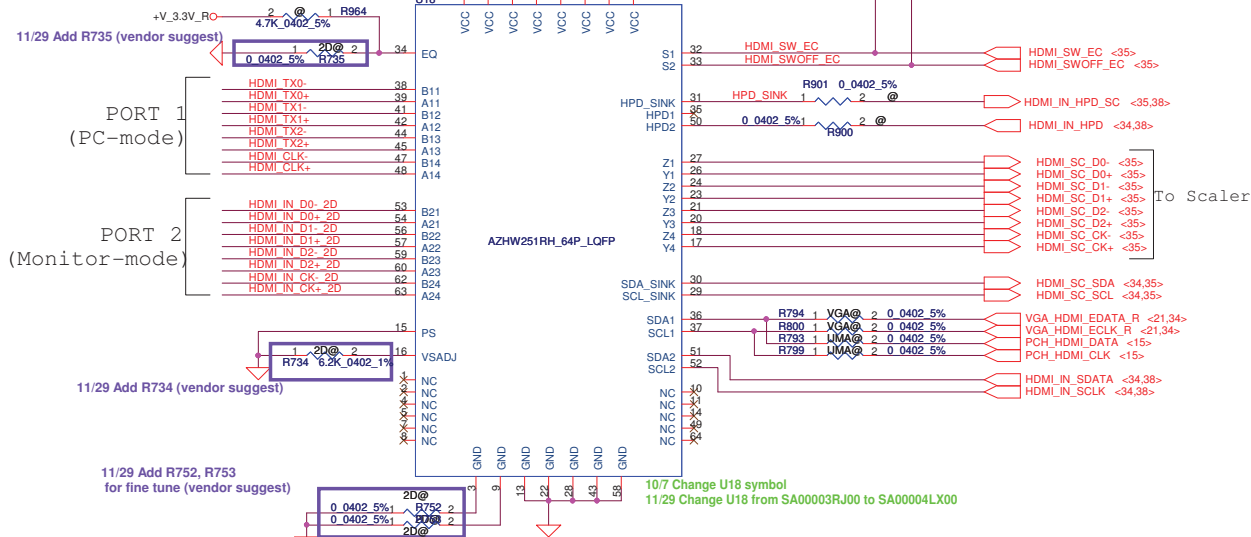
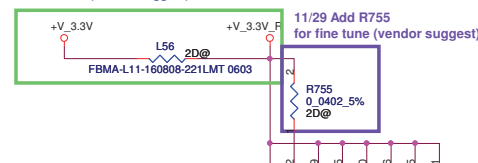
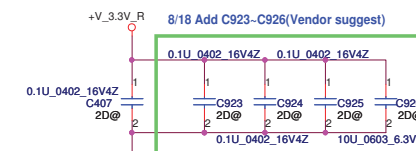
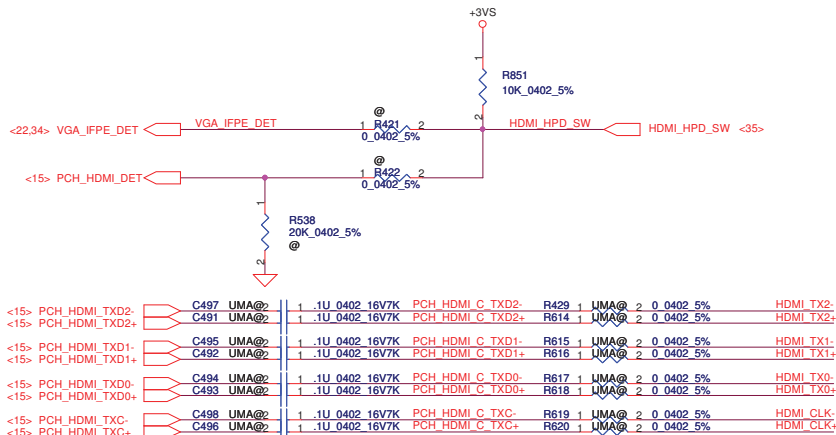
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

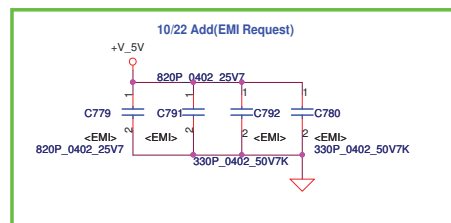
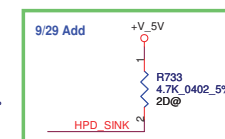
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

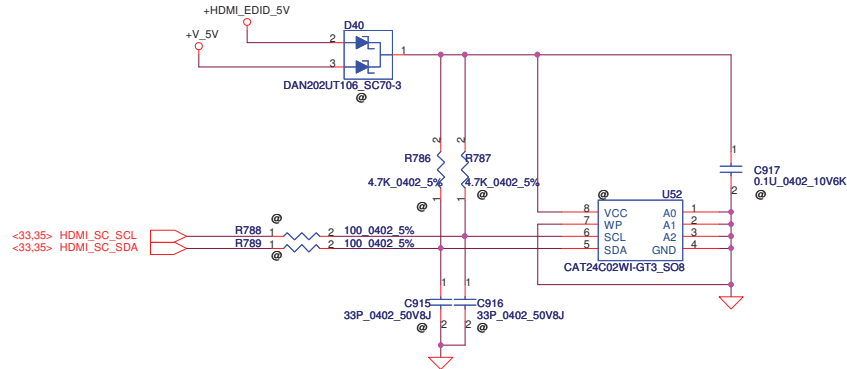
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/07/20	Deciphered Date	2011/07/20	Title
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Size Custom		Document Number		Rev 1.A
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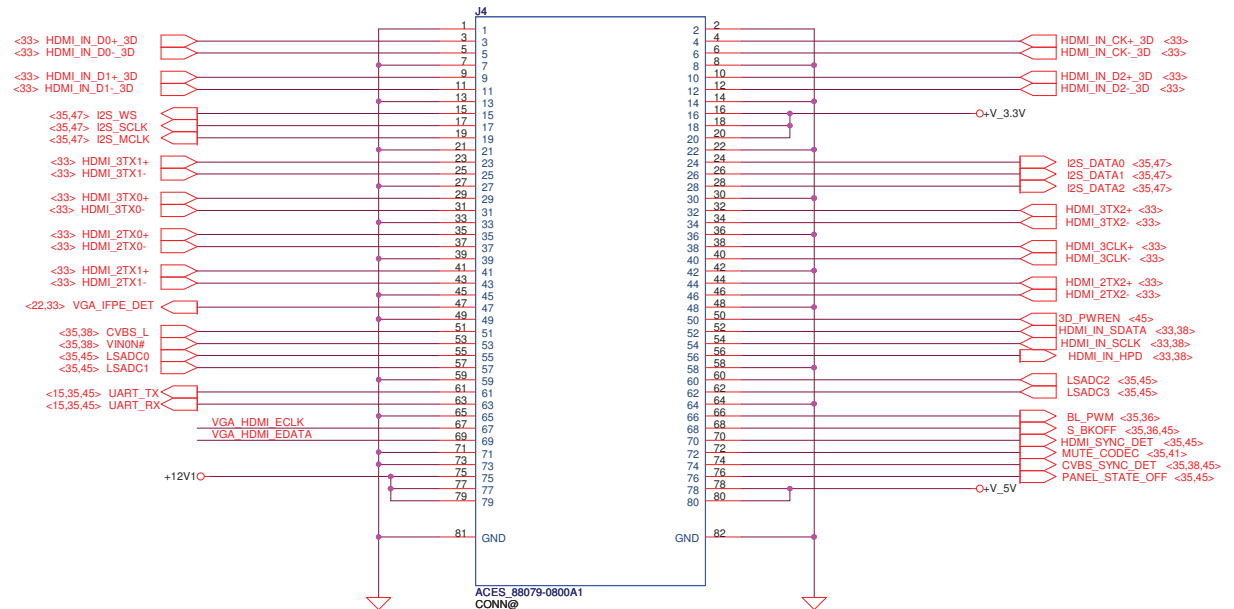
S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1, SDA1
H	L	PORT2/SCL2, SDA2
L	H	All disconnected



0810 Vendor suggest to reserve for EDID debug



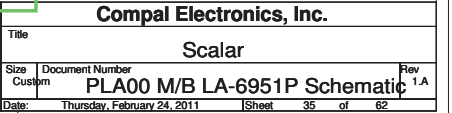
12/11 3D Scaler Pin define update



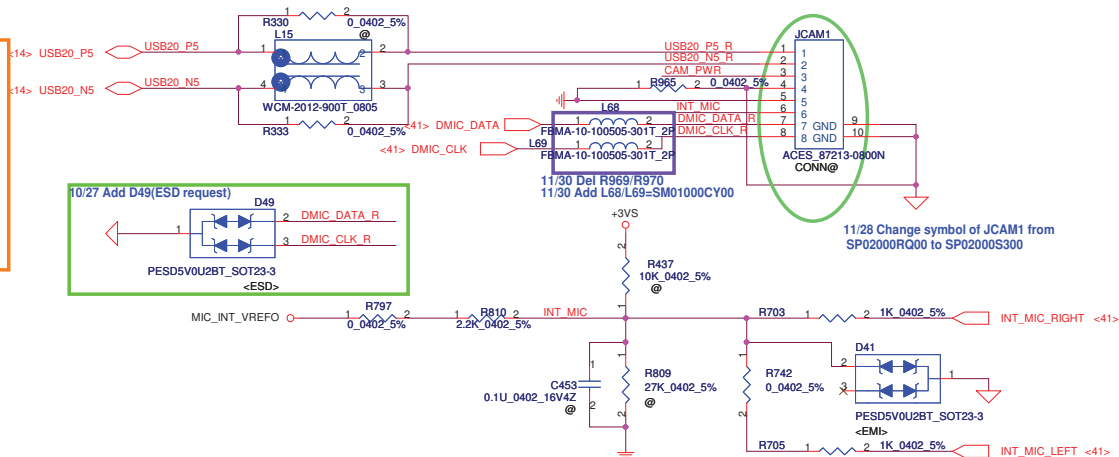
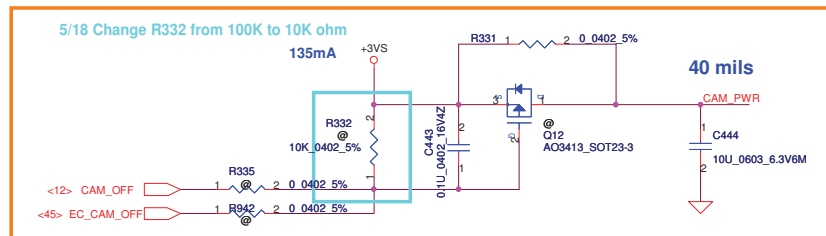
12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)



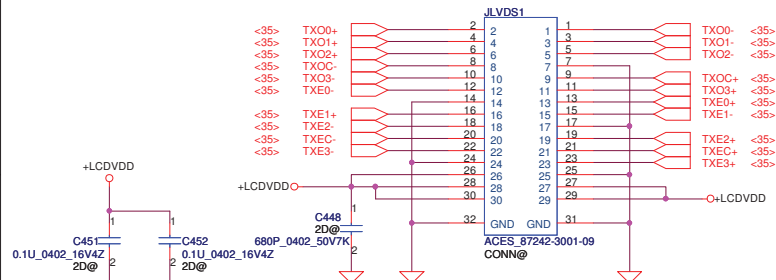
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/07/20				Deciphered Date			
								2011/07/20			
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Title				3D Scaler				Rev			
Size				Document Number				1.A			
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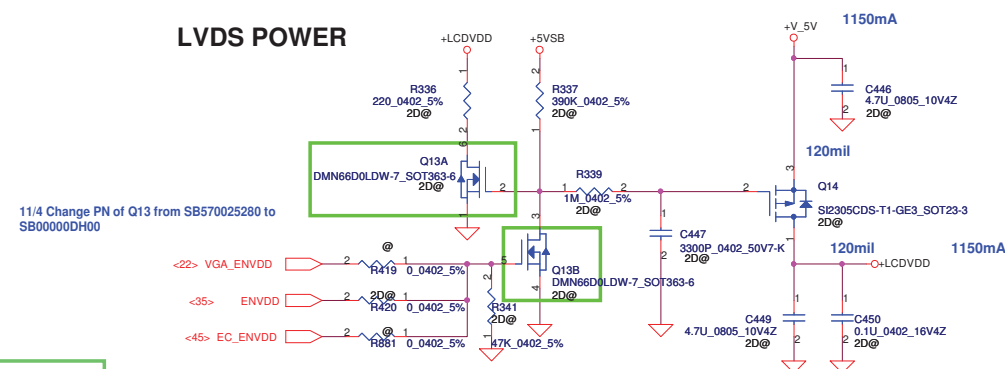
WebCam+Digital Mic



LVDS CONN



LVDS POWER

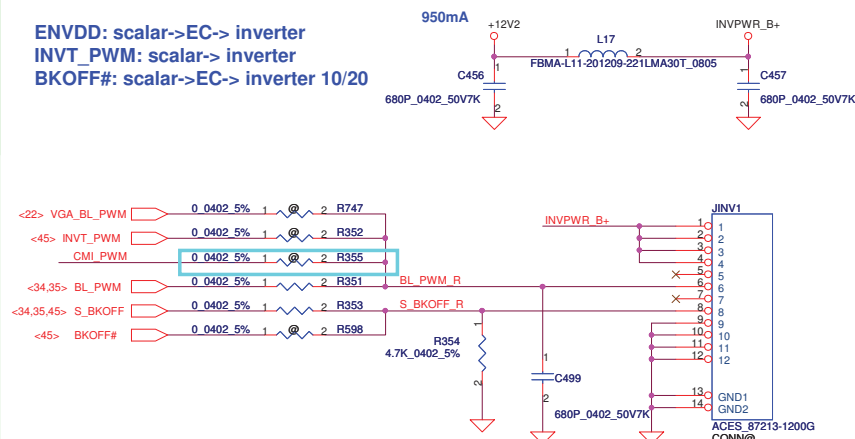


INVERTER

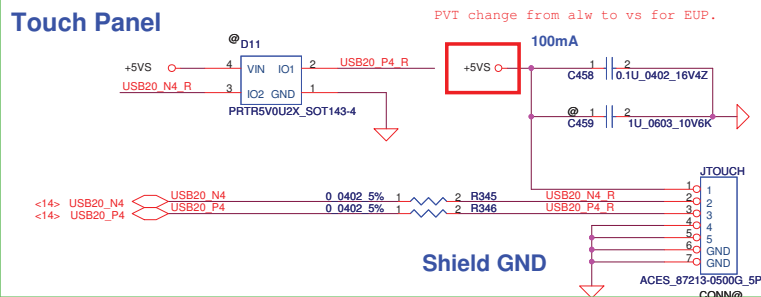
ENVDD: scalar->EC-> inverter

INVT_PWM: scalar-> inverter

BKOFF#: scalar->EC-> inverter 10/20

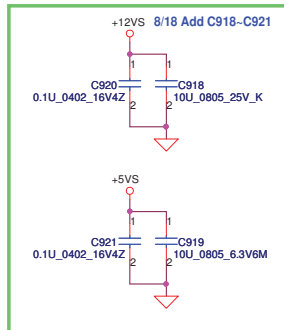


Touch Panel



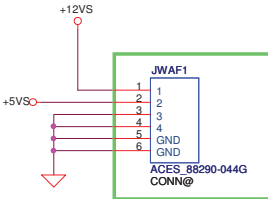
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Issued Date	2010/07/20	Deciphered Date	2011/07/20	LCD CONN. / WebCam
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HDD POWER Conn

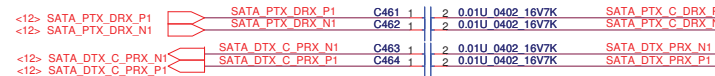


Layout Note: Place C918/C919/C920/C921 close to JWAFER1

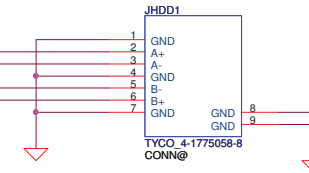
HDD



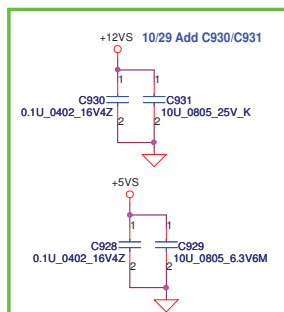
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00



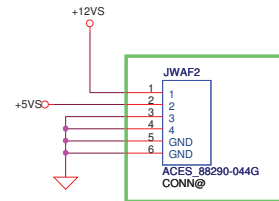
SATA HDD Conn.



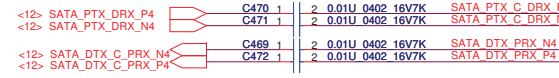
ODD POWER Conn



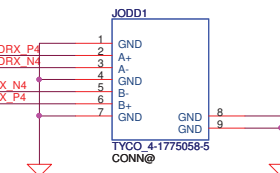
10/28 Add C928/C929
Layout Note: Place C928/C929 close to JWAFER2



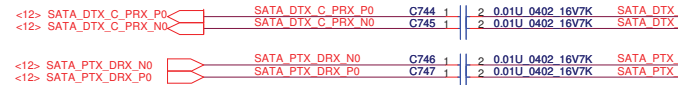
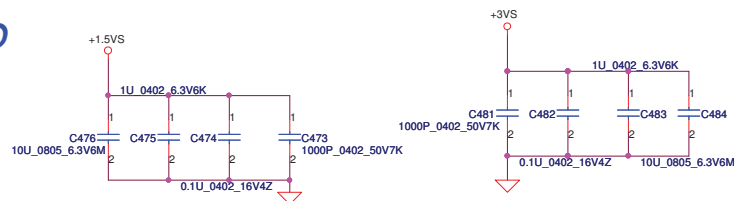
12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00



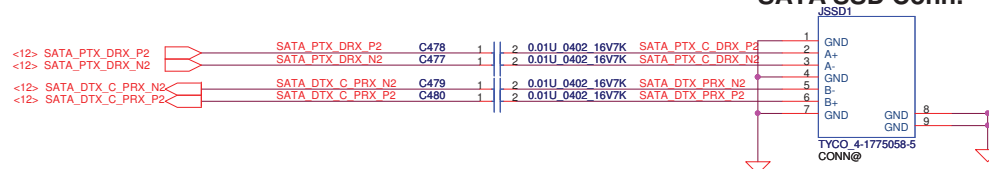
SATA ODD Conn.



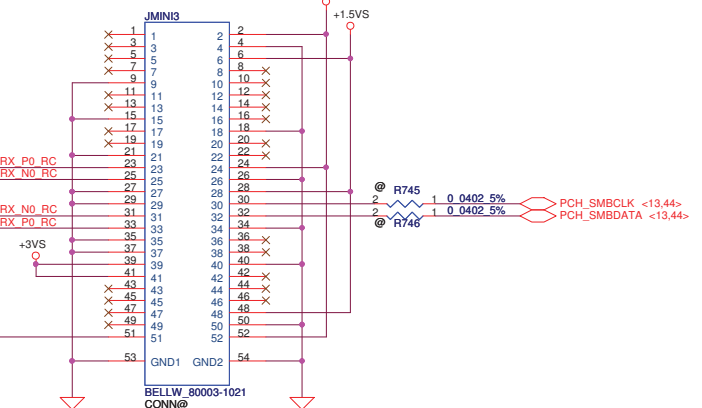
SSD



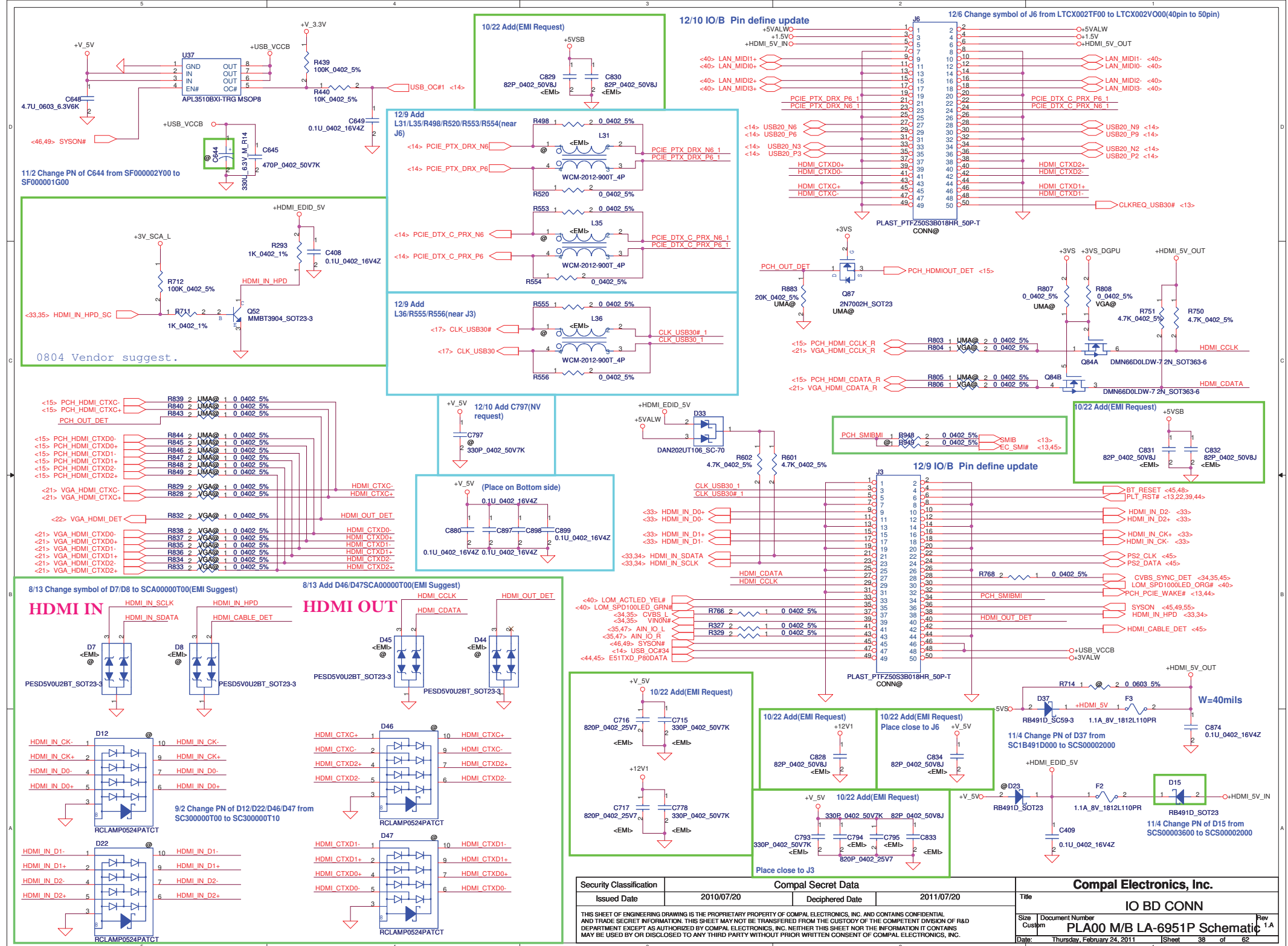
SATA SSD Conn.

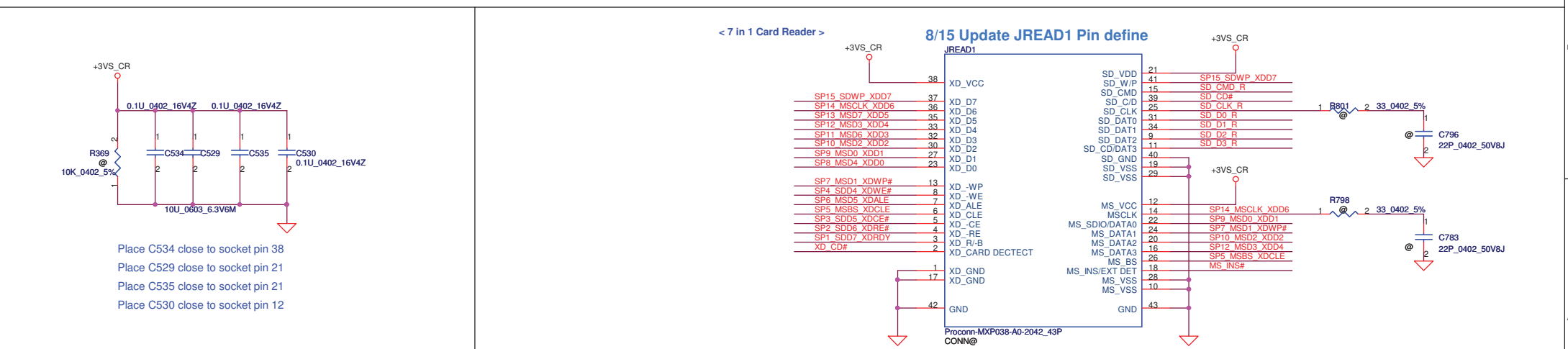
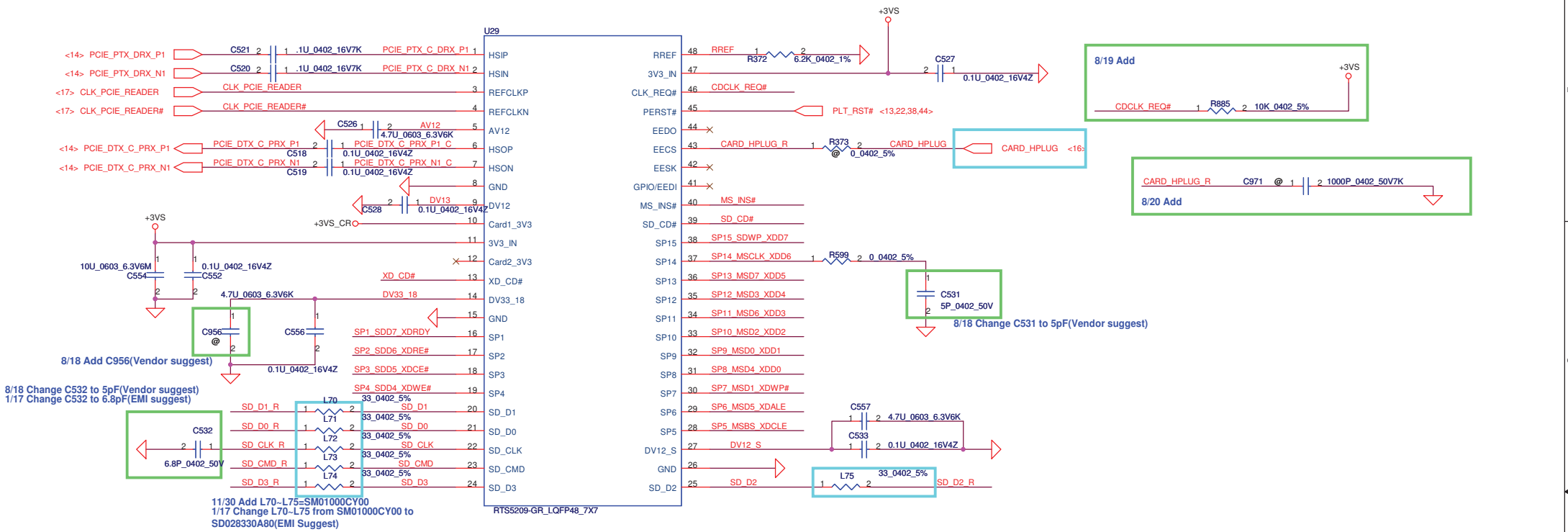


MINI SSD Conn.

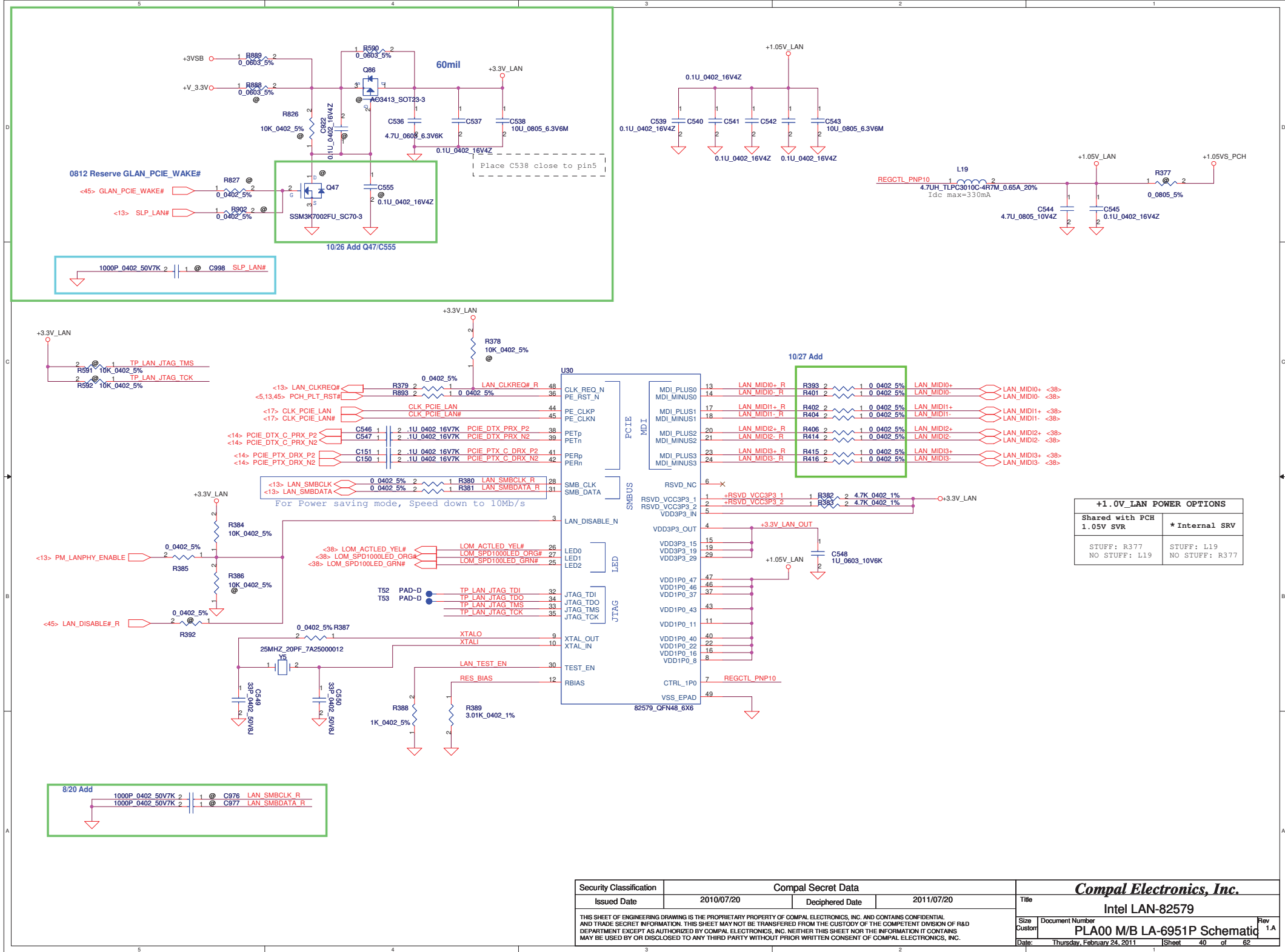


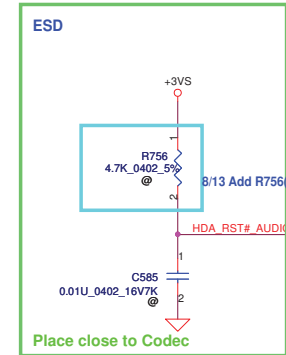
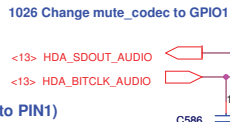
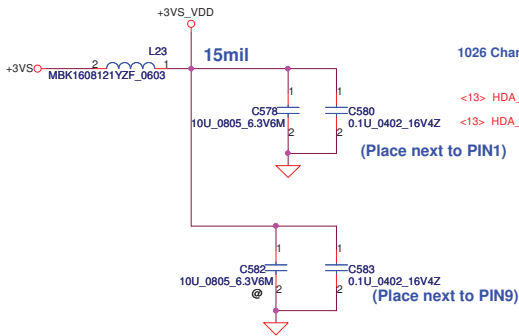
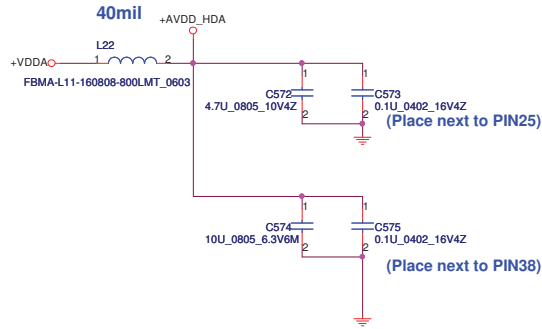
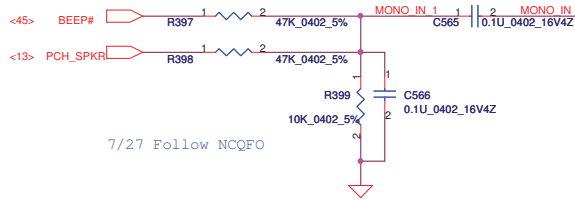
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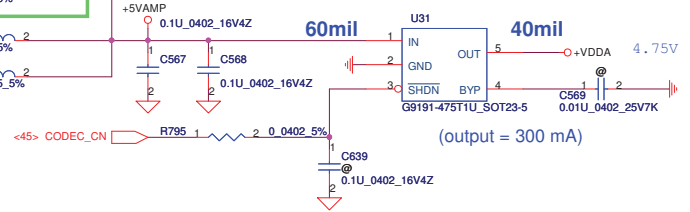
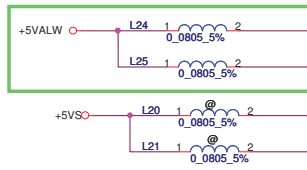


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					Compal Electronics, Inc.
					PCIE-Card Reader-RTS5209
Size	Document Number	Rev			PLA00 M/B LA-6953P Schematic 1.A
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			62		

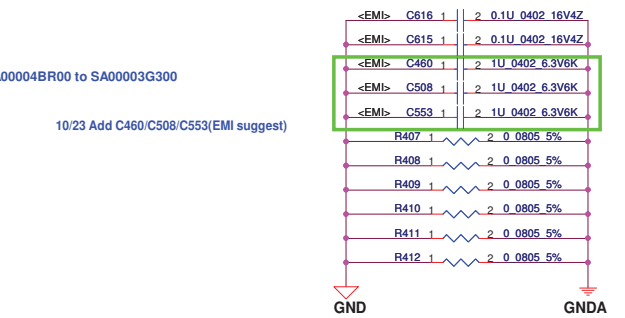
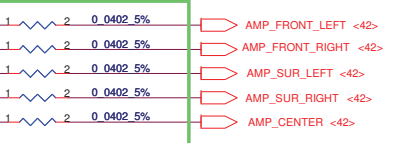
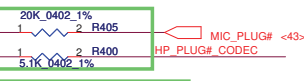
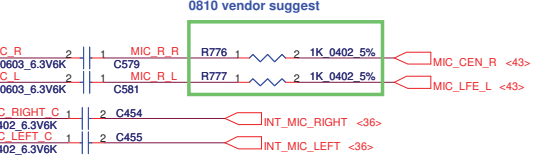
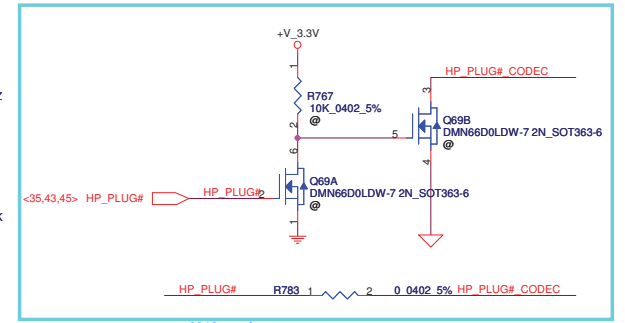
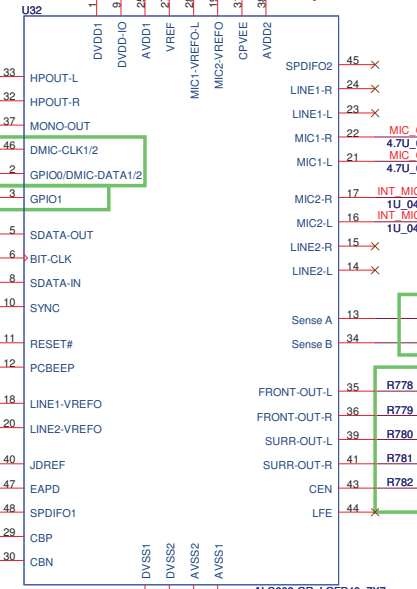
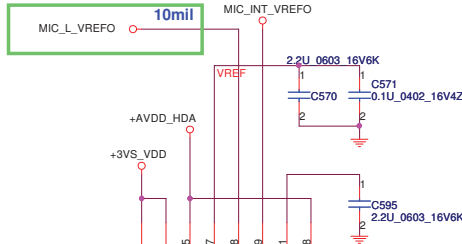




0105 Add L24/L25



1026 DEL MIC_R_VREF0



Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

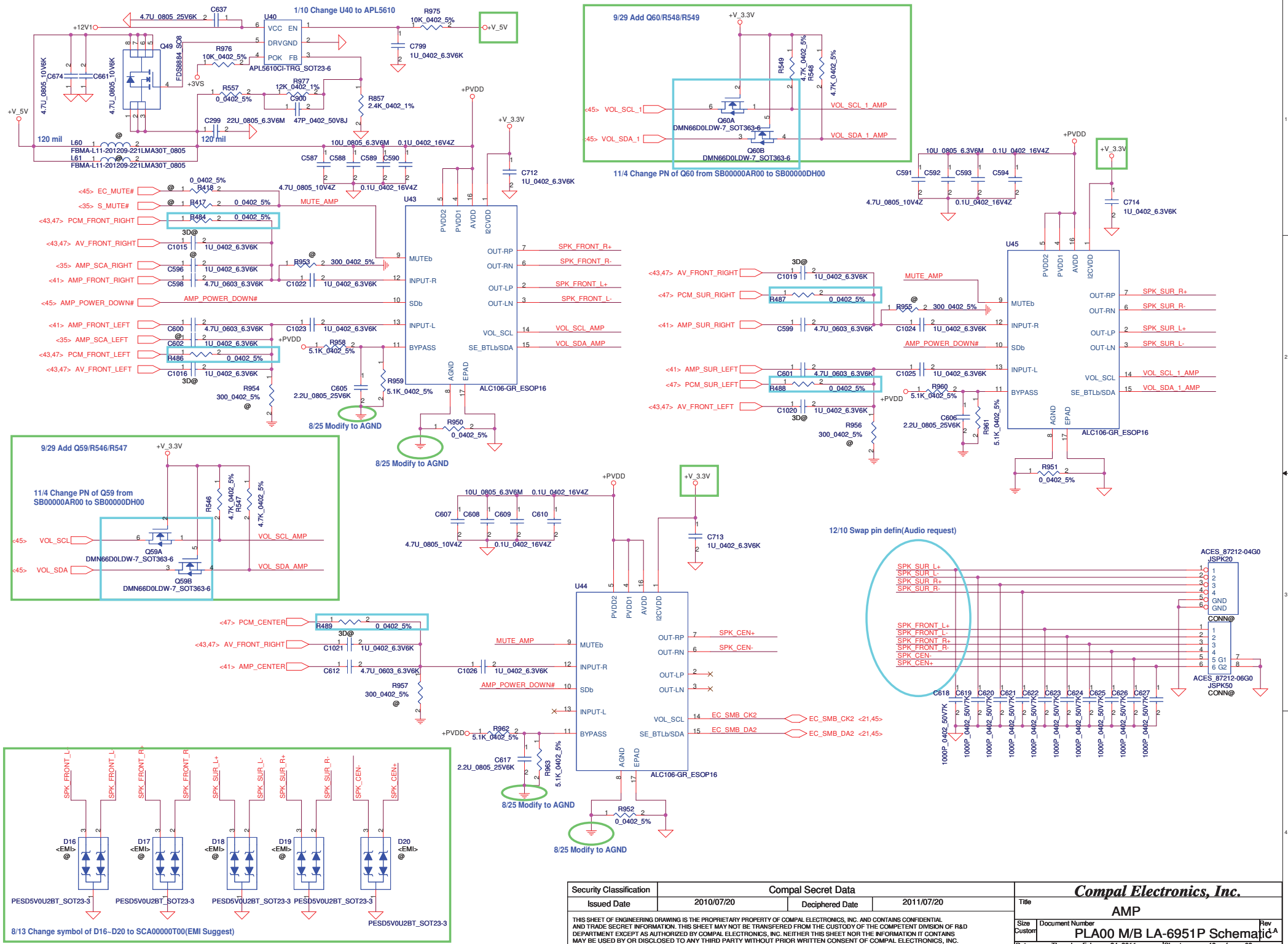
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Date: Thursday, February 24, 2011				Sheet	62

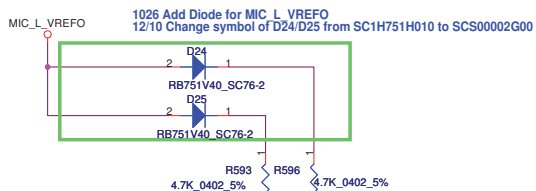
Compal Electronics, Inc.

HD Audio Codec ALC663

PLA00 M/B LA-6951P Schematic

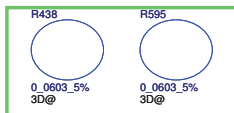
Rev 1.A



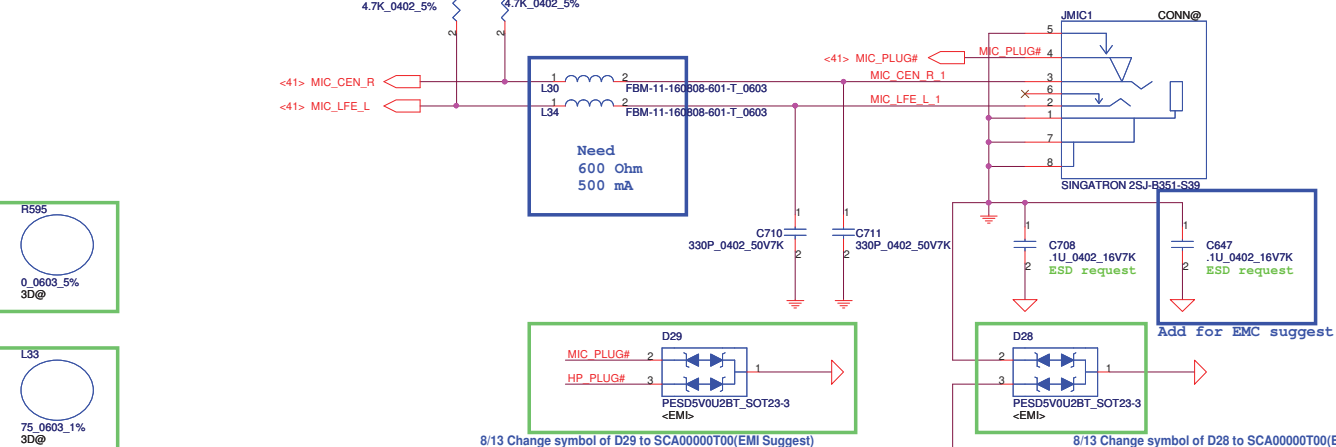
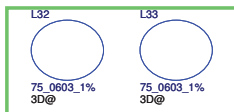


EXT MIC IN

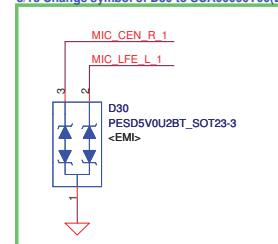
2/18 Add



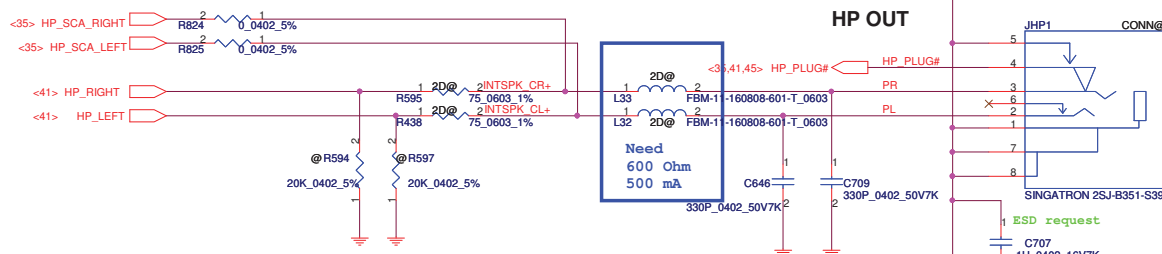
2/24 Add



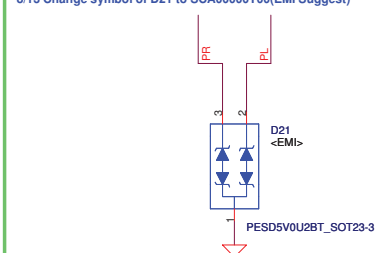
8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)



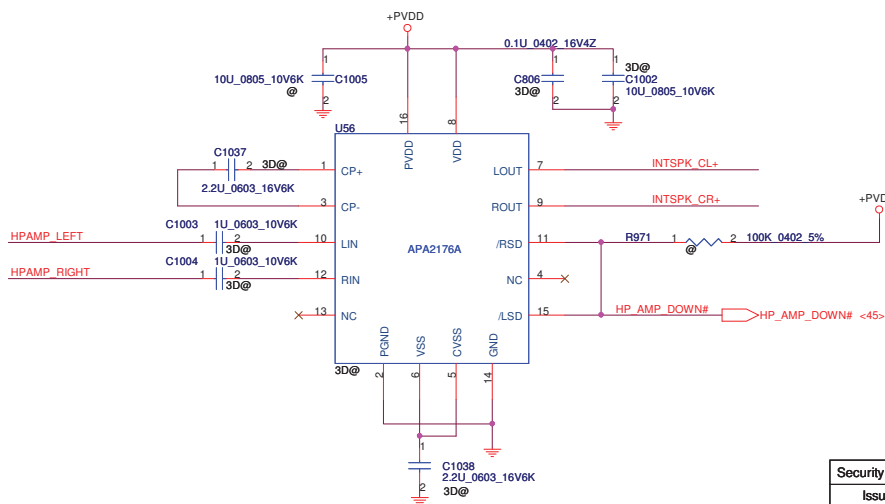
HP OUT



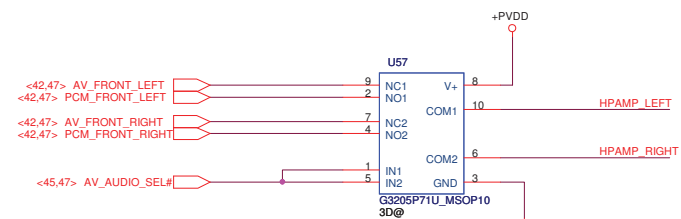
8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)



10/22 Change U56 from SA00001ZW00 to SA00004IS00



12/09 Add U57

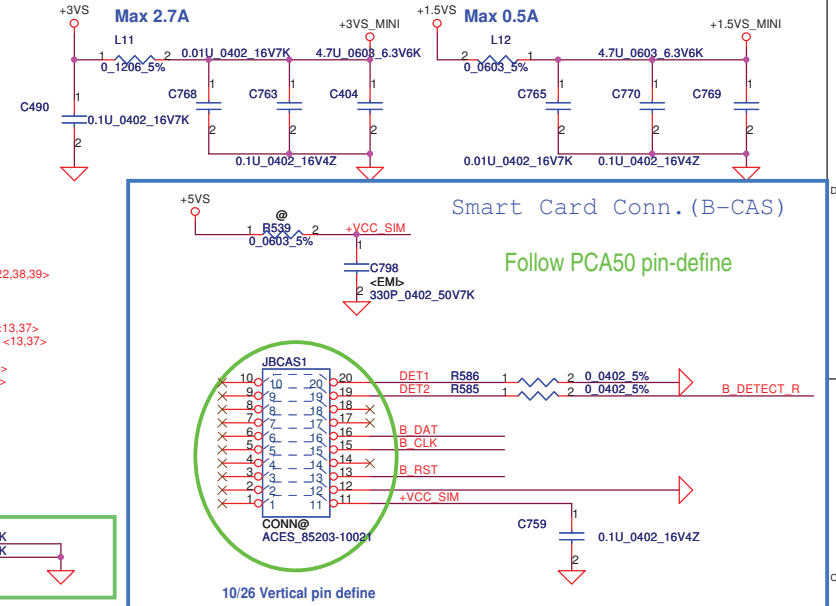
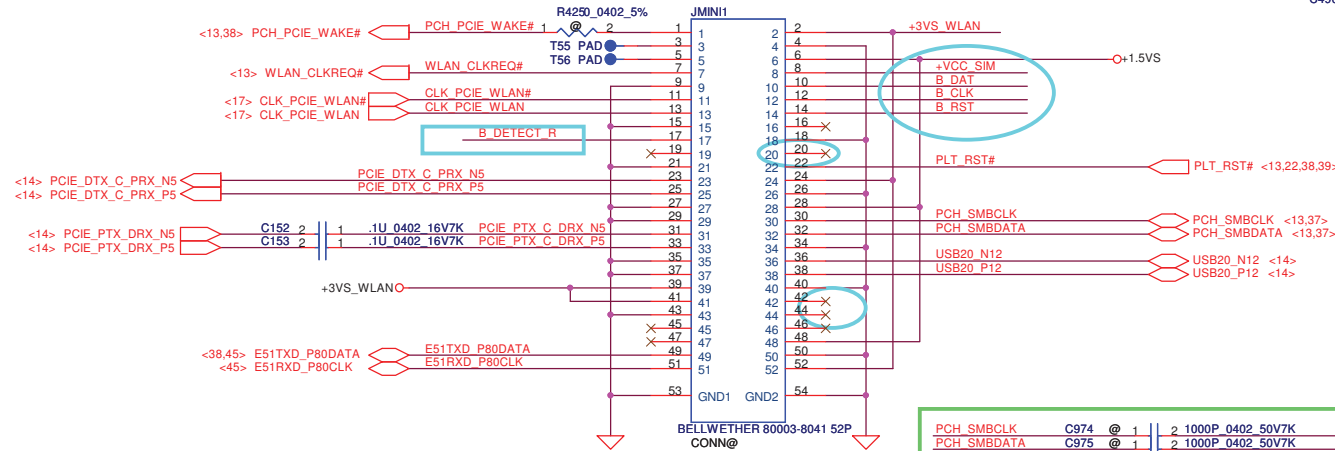


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				Audio Jack		
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MINI (TV)

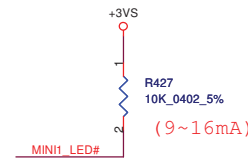
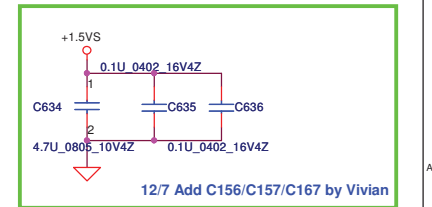
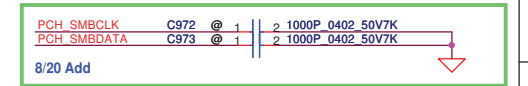
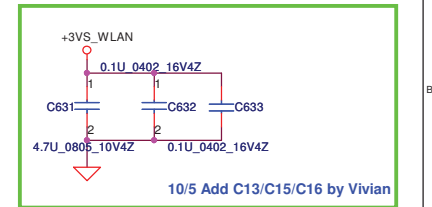
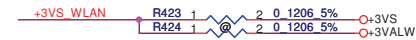
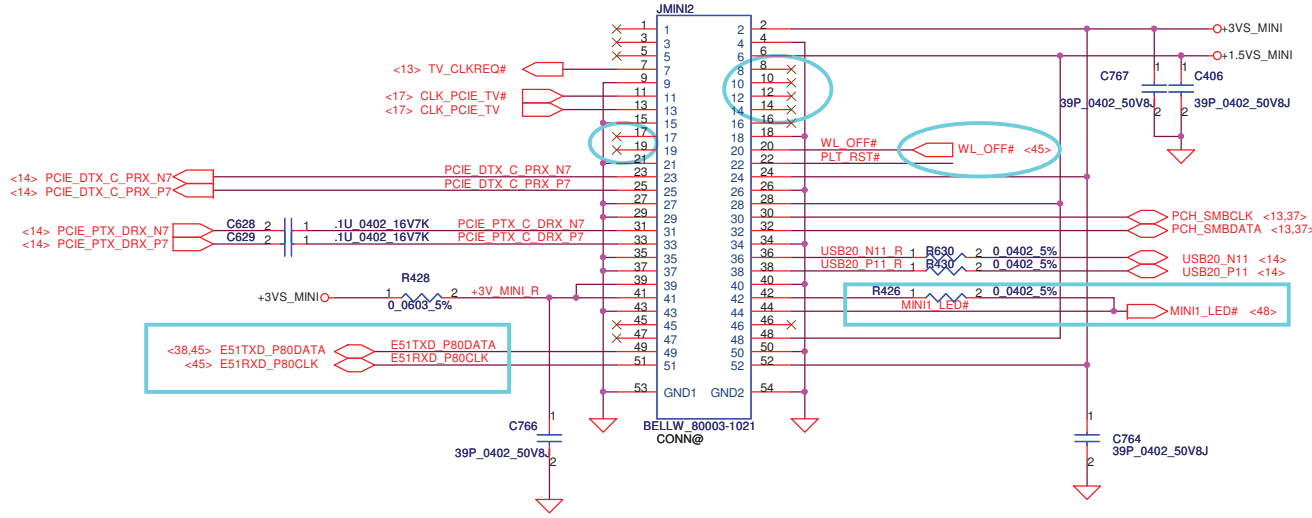
Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA

H=9mm

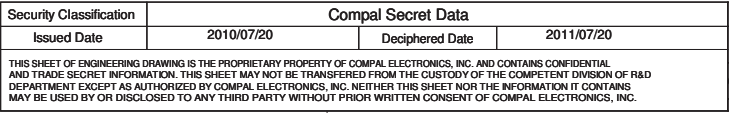


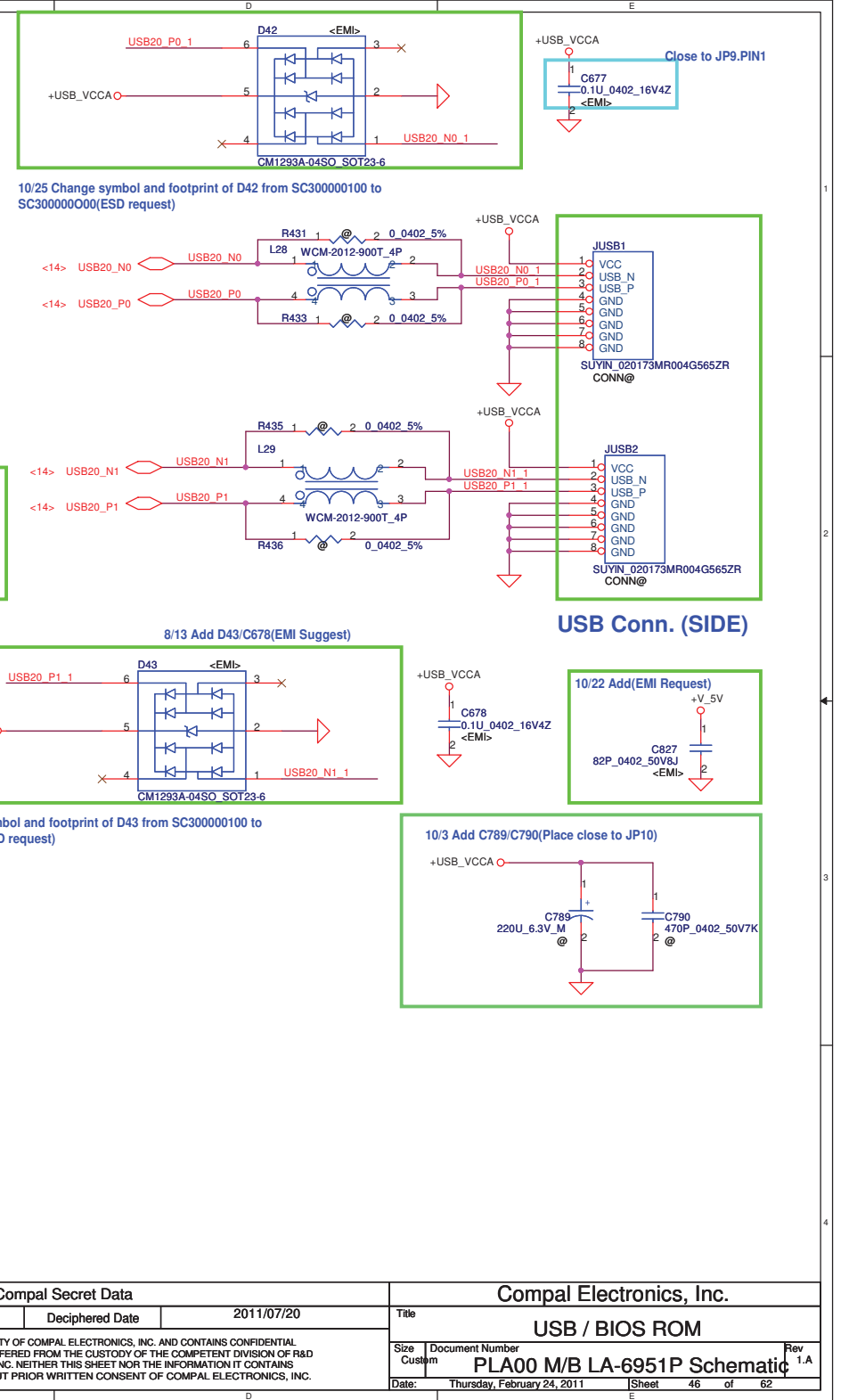
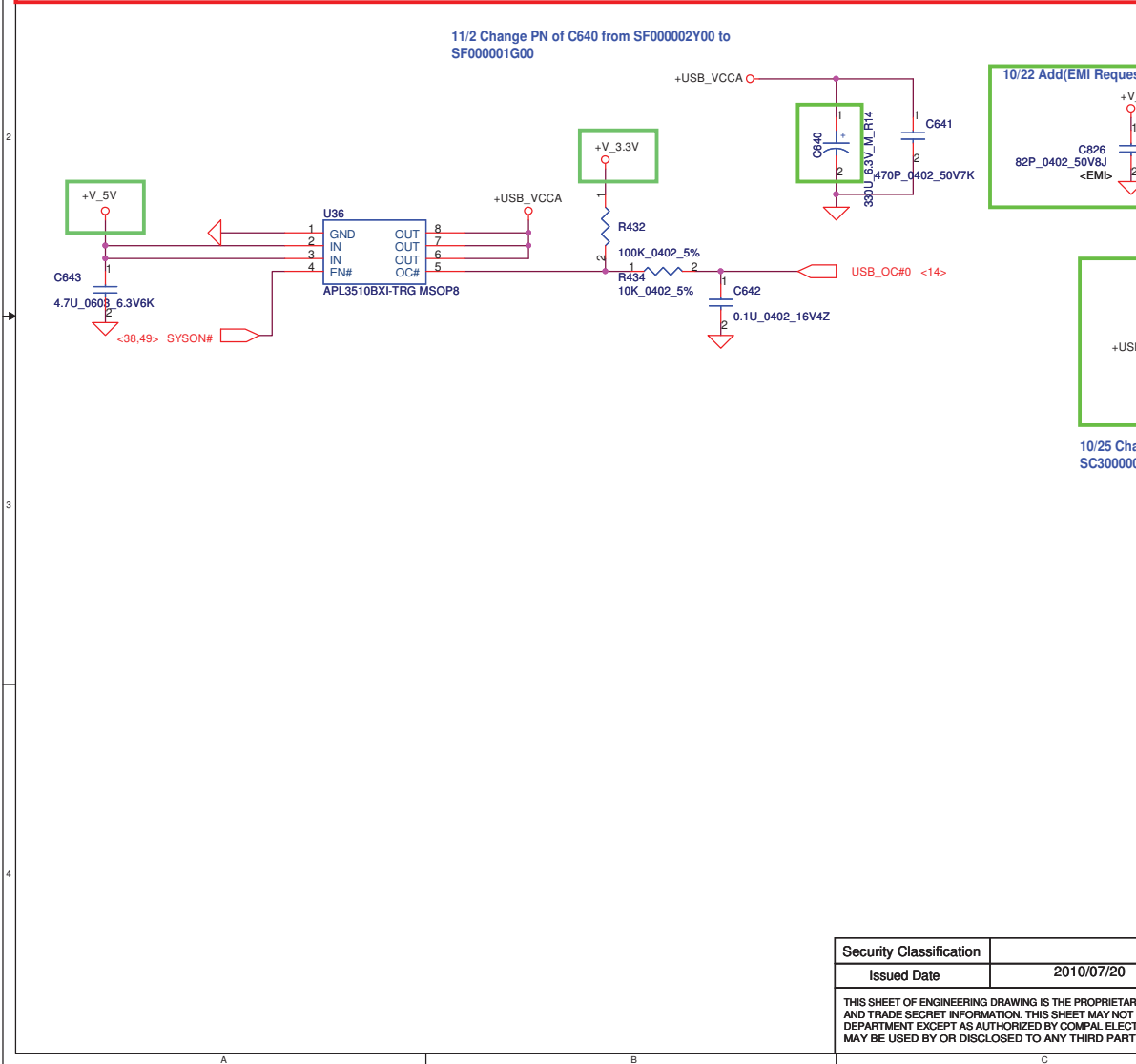
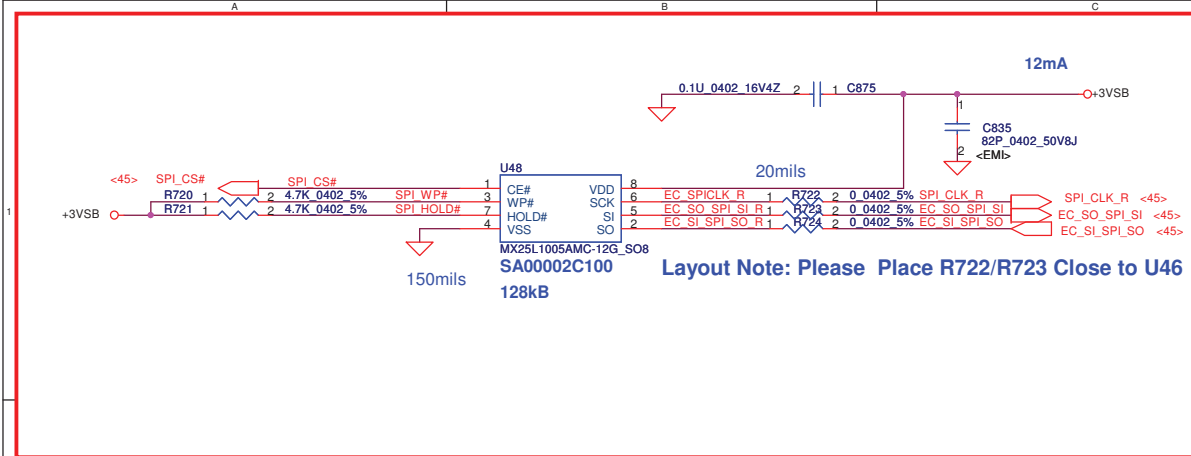
WLAN

H=4mm

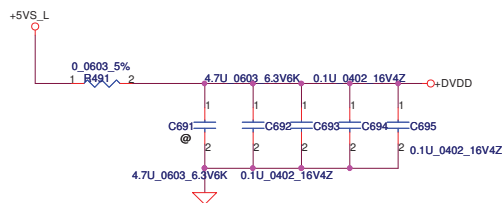
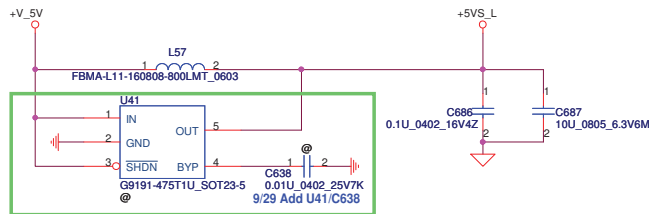


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Size Custom	Document Number	PLA00 M/B LA-6951P Schematic		Rev 1.A	
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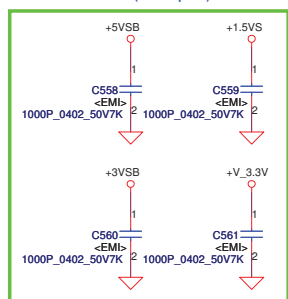




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Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic	Rev	1.A
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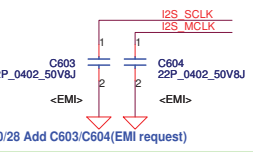
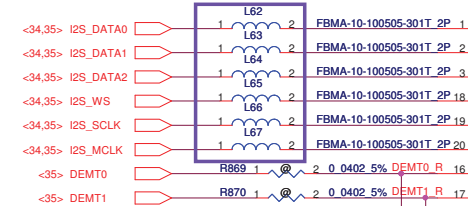


10/27 Add C558-C561(EMI request)

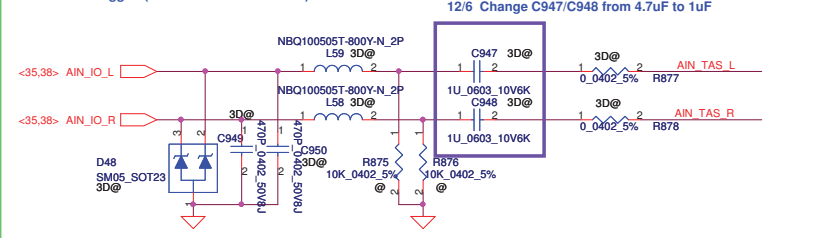


11/30 Del R858-R863

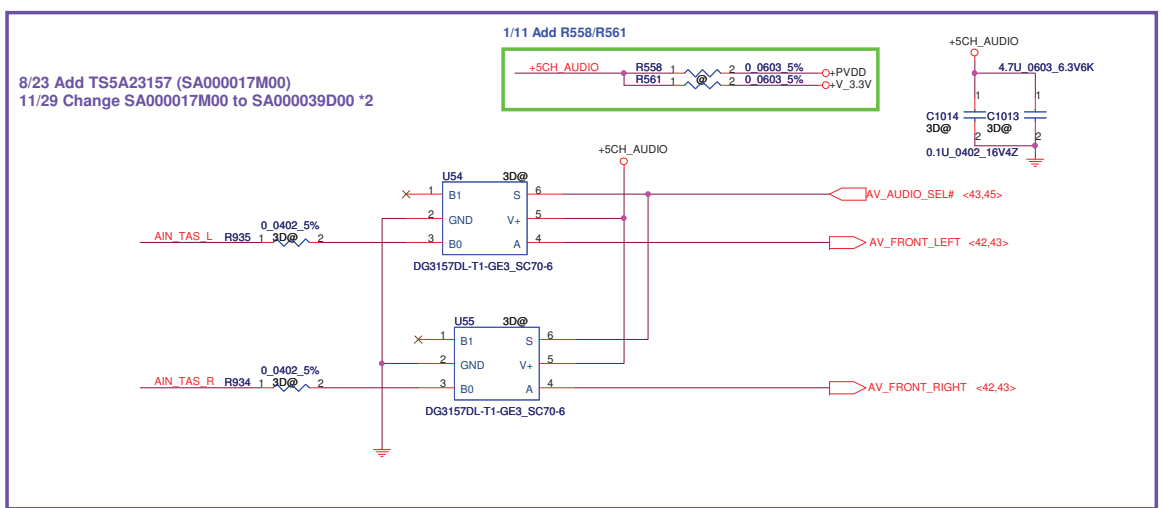
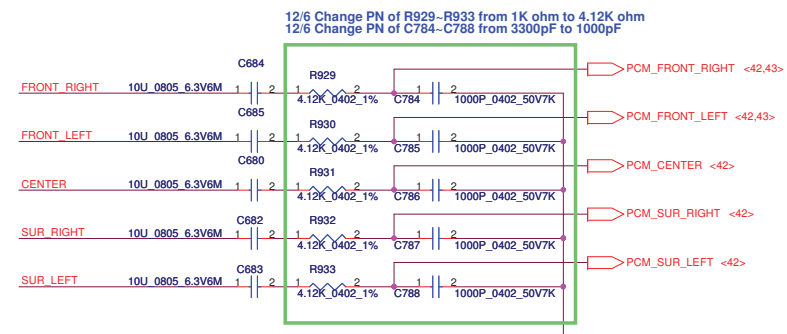
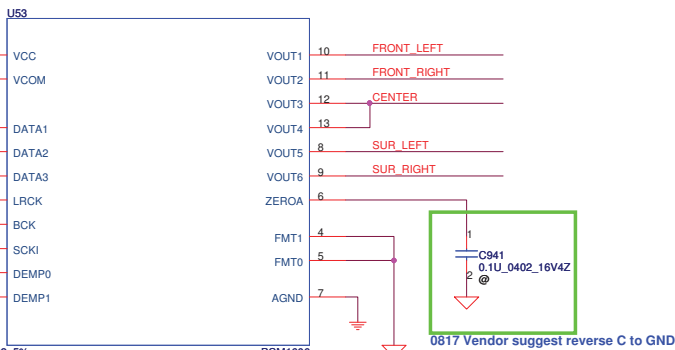
11/30 Add L62-L67=SM01000CY00



0818 Vendor suggest(Close to U42.Pin43/Pin44)



12/6 Change C947/C948 from 4.7uF to 1uF

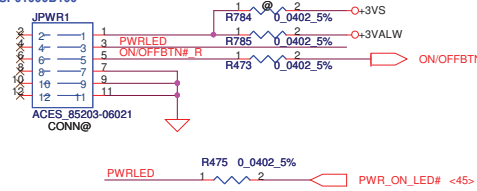


De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

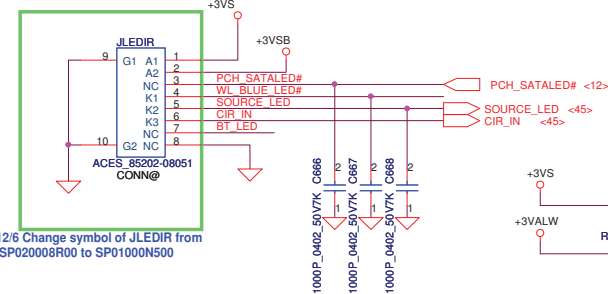
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Custpm	PLA00 M/B LA-6951P Schematic
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Power switch board

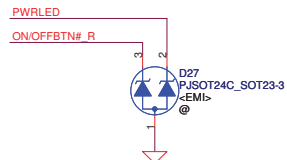
12/6 Change symbol of JPWR1 from SP02000U100 to SP01000B100



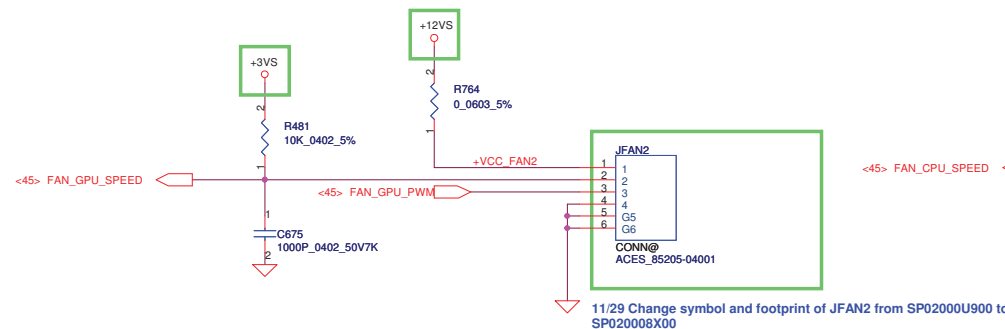
LED board conn.



8/13 Change symbol of D27 to SCA0000E00(EMI Suggest)

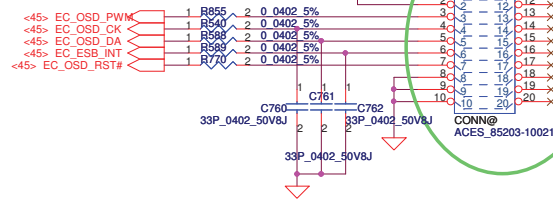


Fan Control circuit

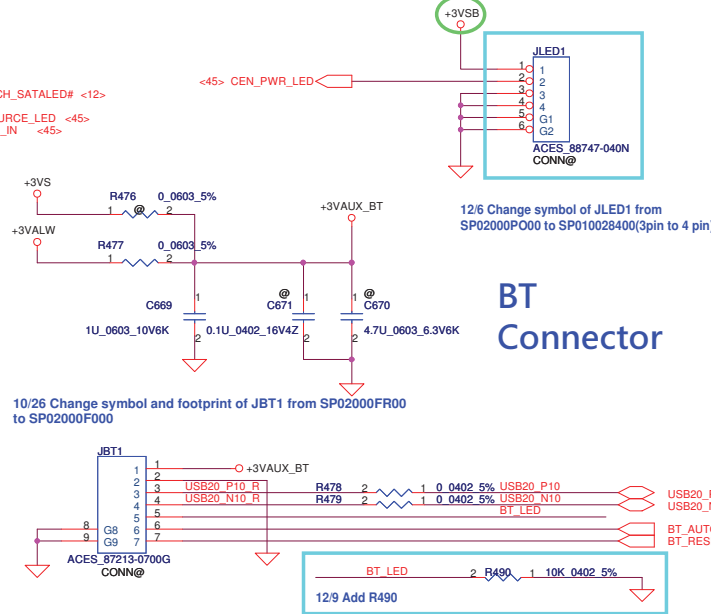


SENSOR BOTTOM

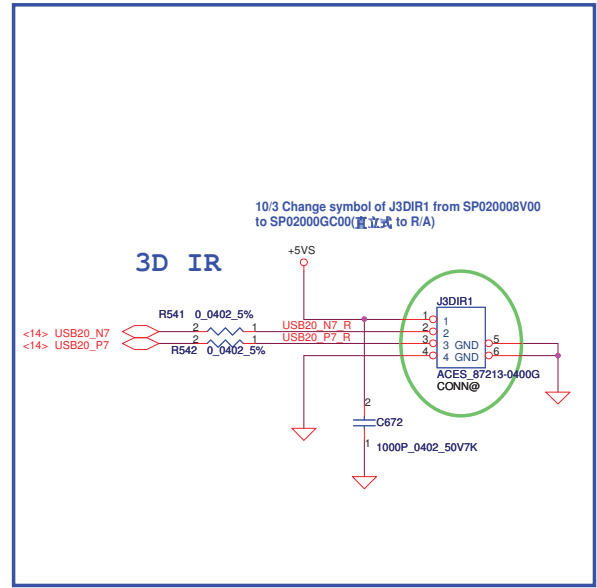
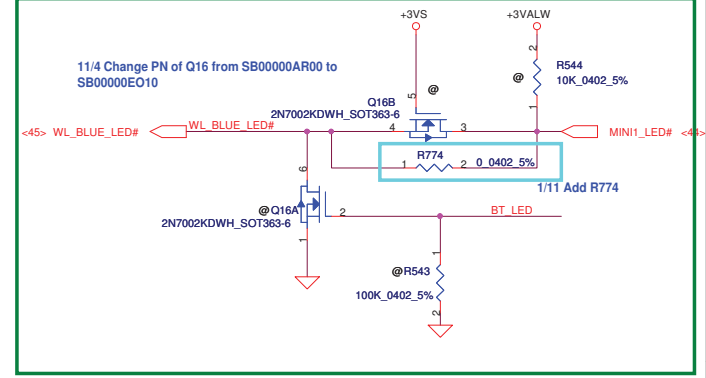
Follow NCQD0



DECO LED board conn.

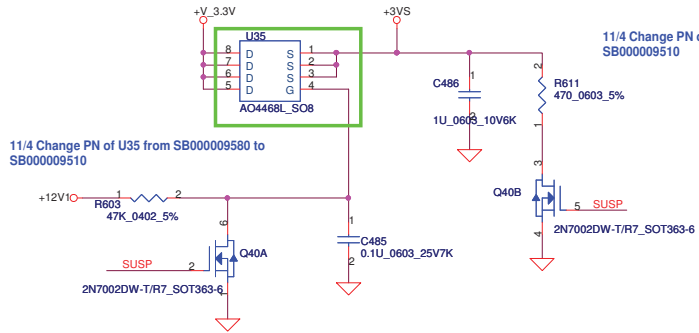


BT Connector

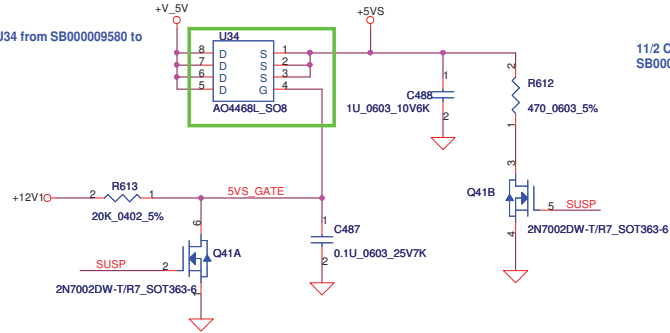


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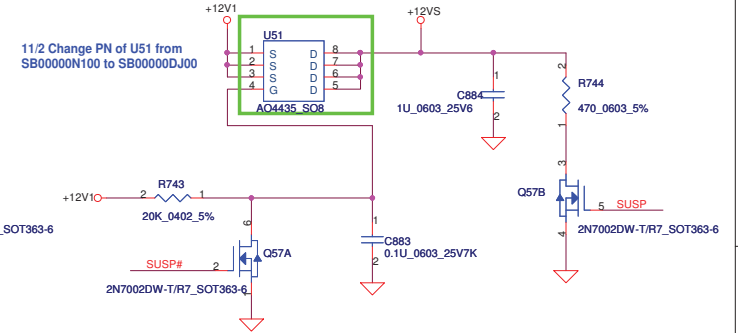
+V_3.3V TO +3VS



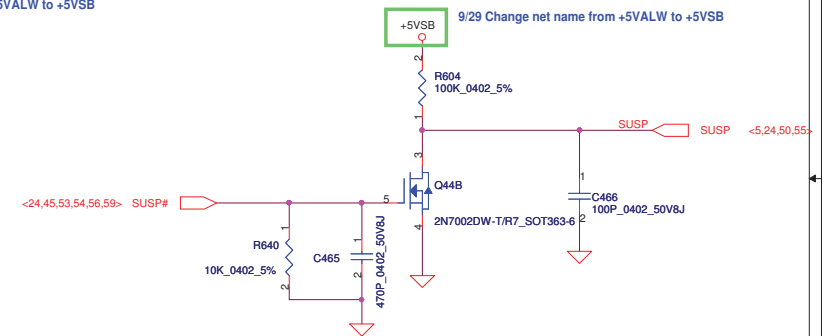
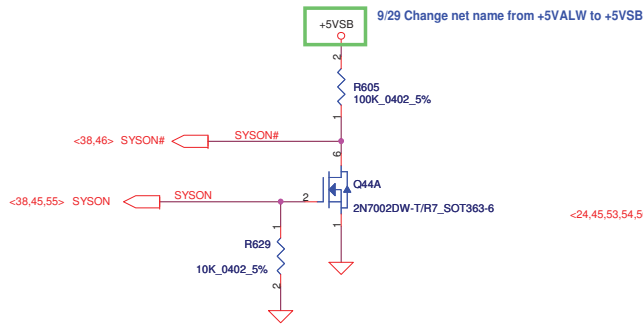
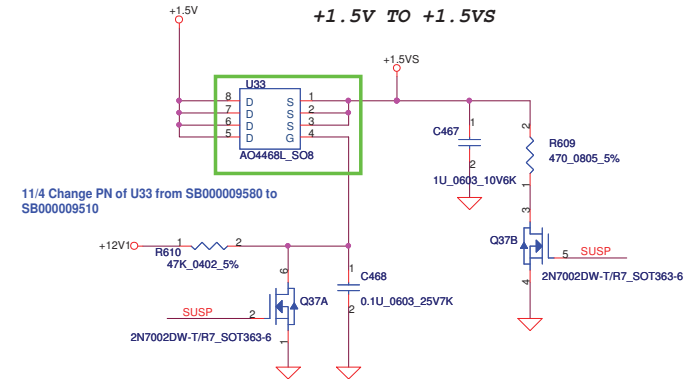
+V_5V TO +5VS



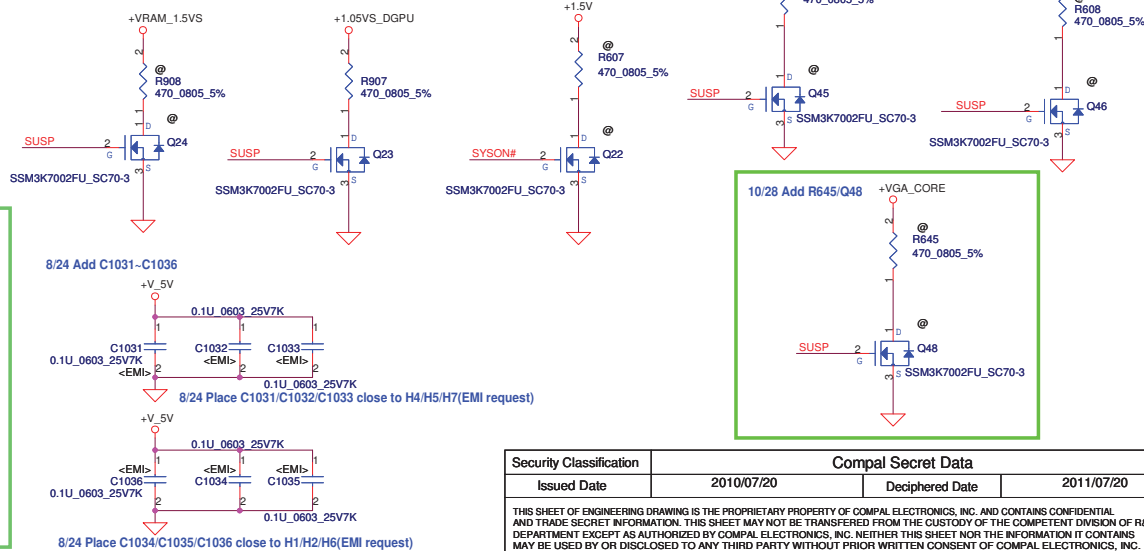
+12V1 TO +12VS



+1.5V TO +1.5VS



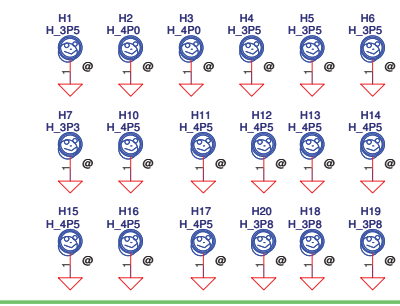
Discharge circuit



NON-PDH



Screw



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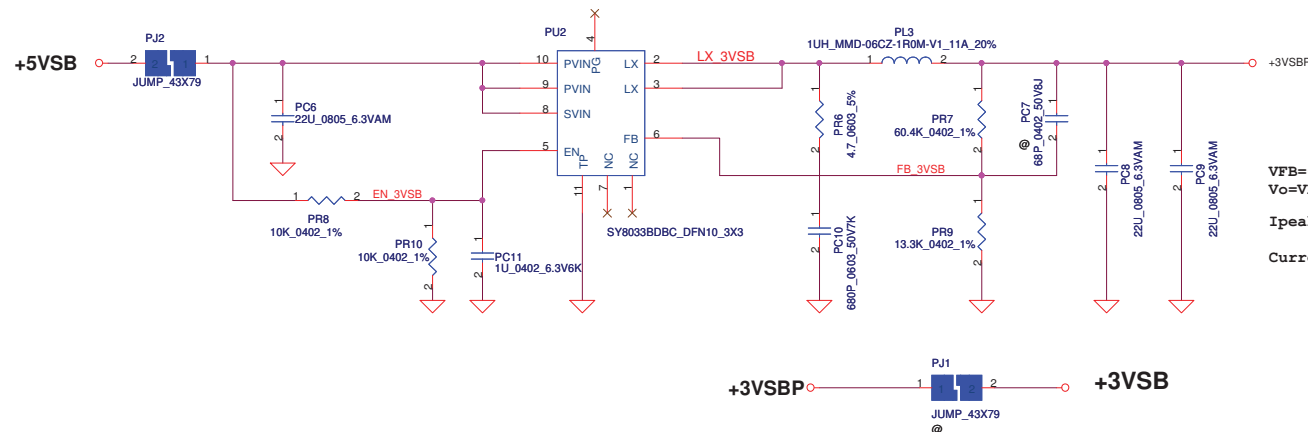
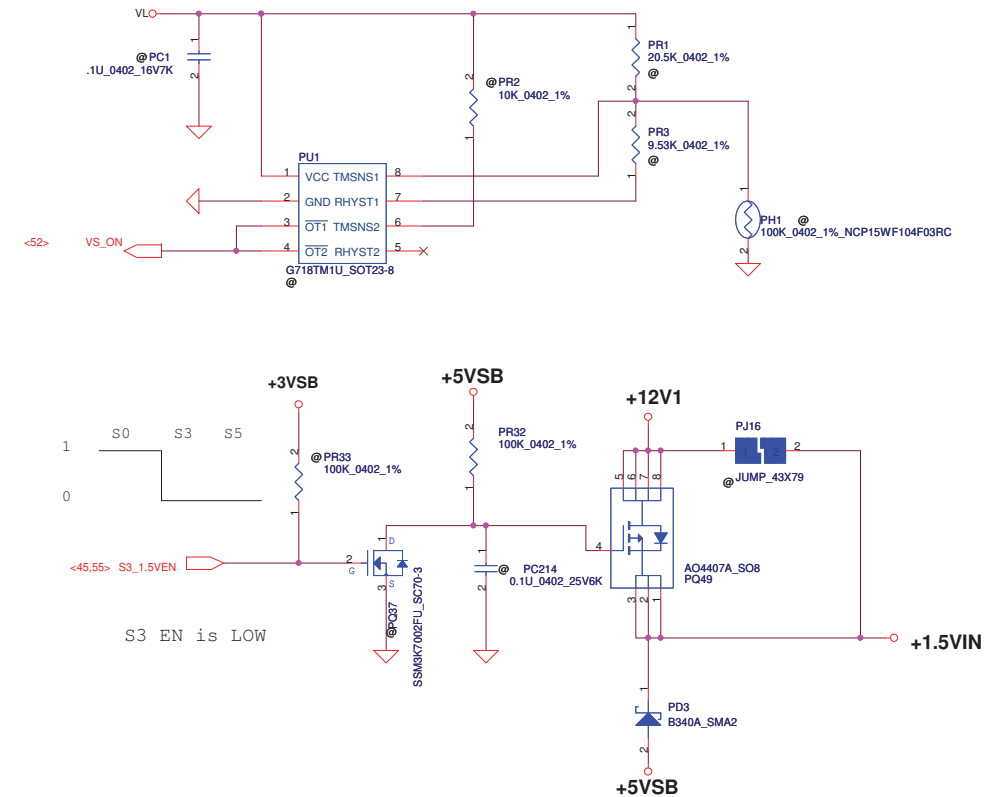
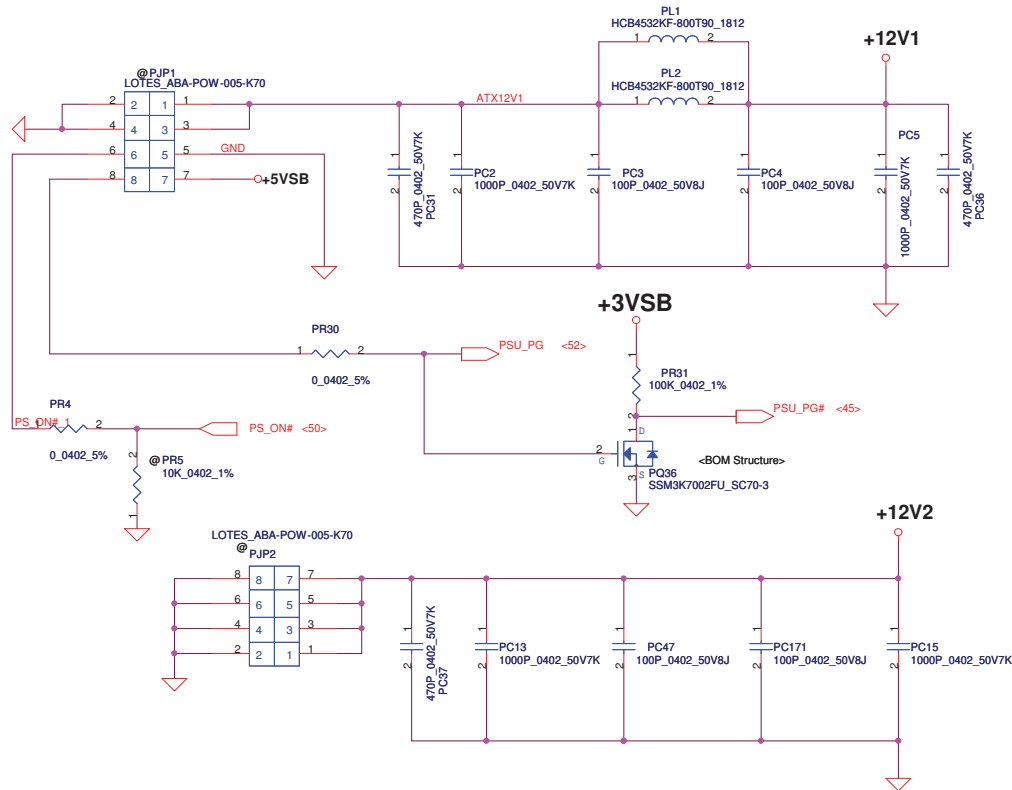
Power Button



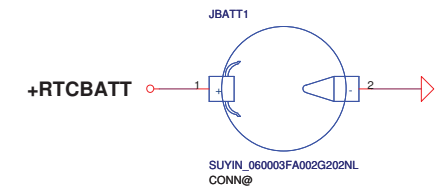
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Issued Date	2010/07/20	Deciphered Date	2011/07/20
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PH1 under CPU botten side :

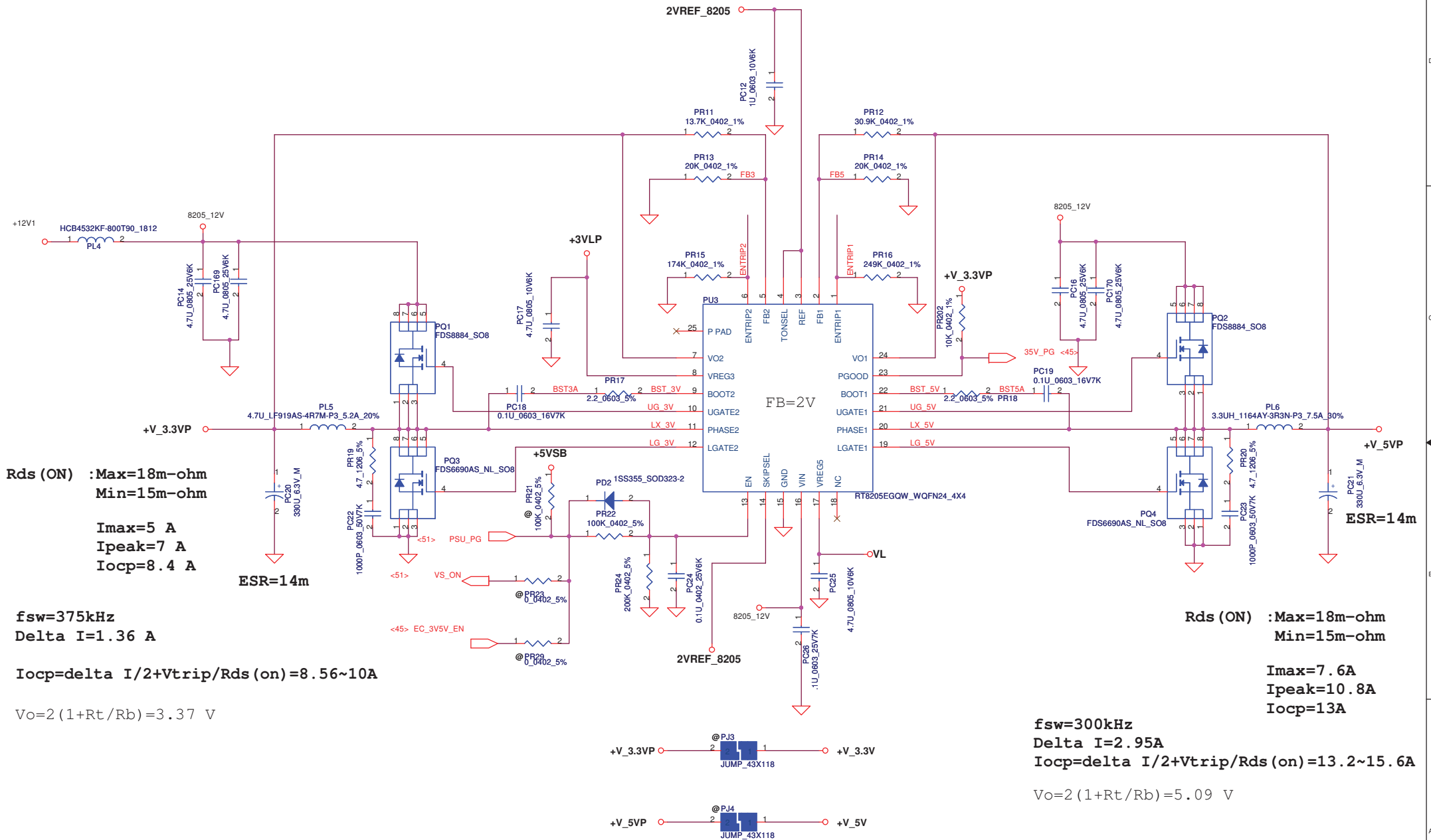
CPU thermal protection at 92 degree C
Recovery at 57 degree C



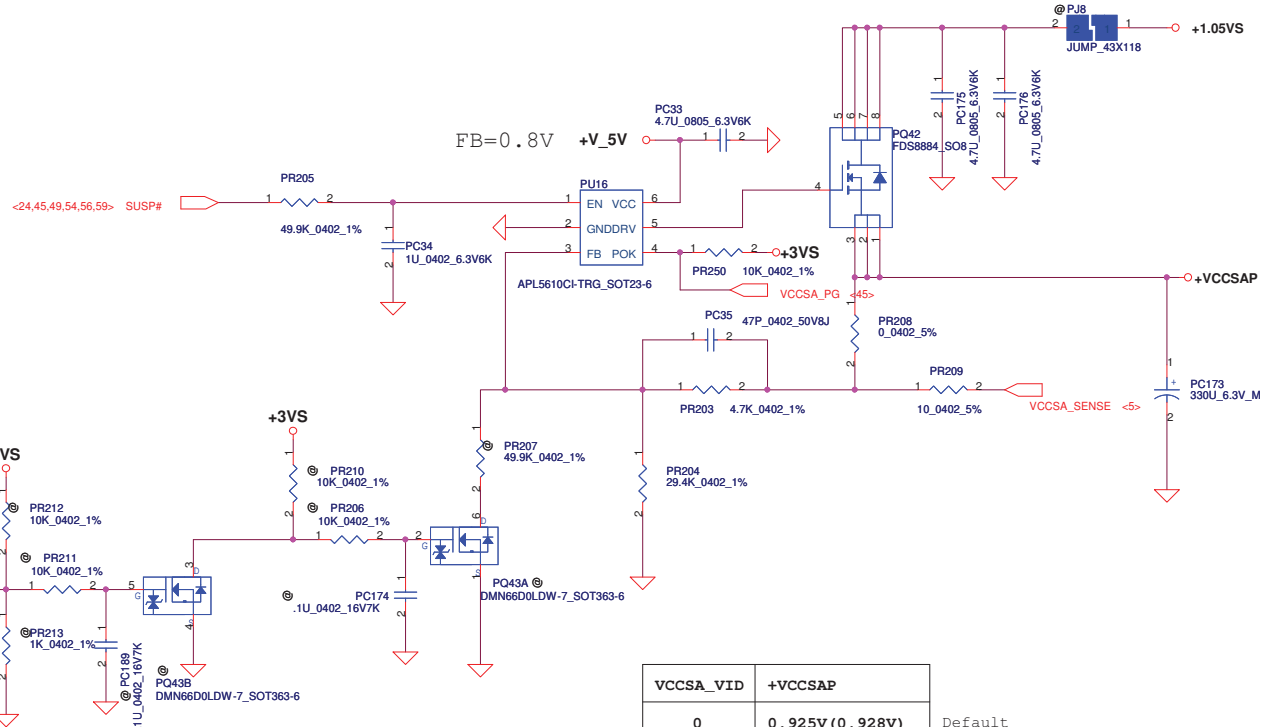
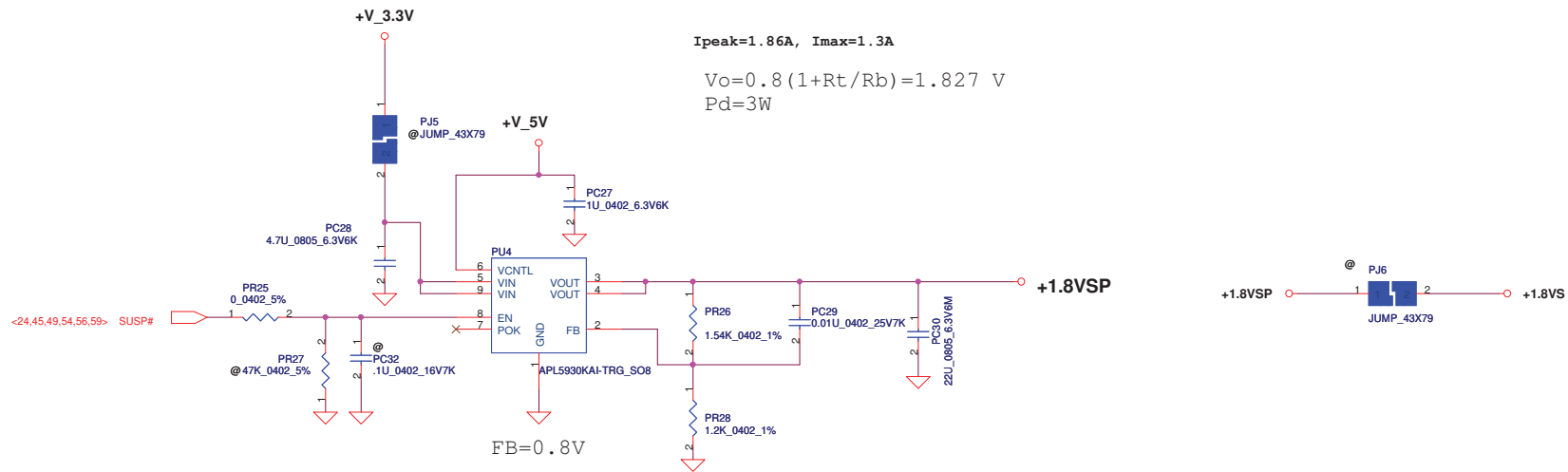
FOR EC suspend
VFB=0.6V
 $V_o = VFB * (1 + PR7/PR9) = 3.318V$
Ipeak=0.062A, Imax=0.045A
Current limit >4A



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				Custom				Rev			
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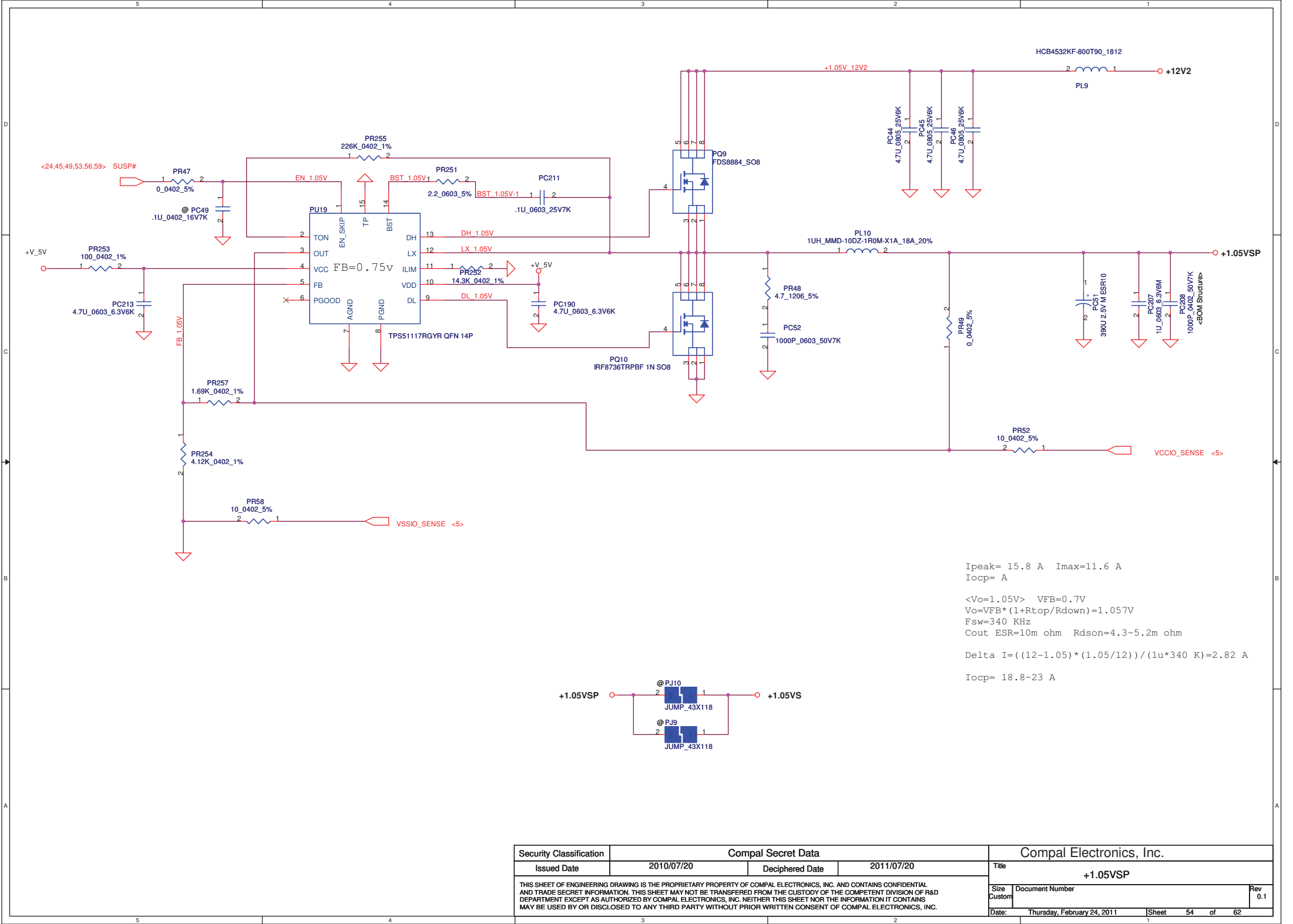


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VCCSA_VID	+VCCSAP
0	0.925V (0.928V)
1	0.85V (0.851V)

Default



Ipeak= 15.8 A Imax=11.6 A
Iocp= A

<Vo=1.05V> VFB=0.7V
Vo=VFB*(1+Rtop/Rdown)=1.057V
Fsw=340 KHz
Cout ESR=10m ohm Rdson=4.3~5.2m ohm

Delta I=((12-1.05)*(1.05/12))/(1u*340 K)=2.82 A

Iocp= 18.8~23 A

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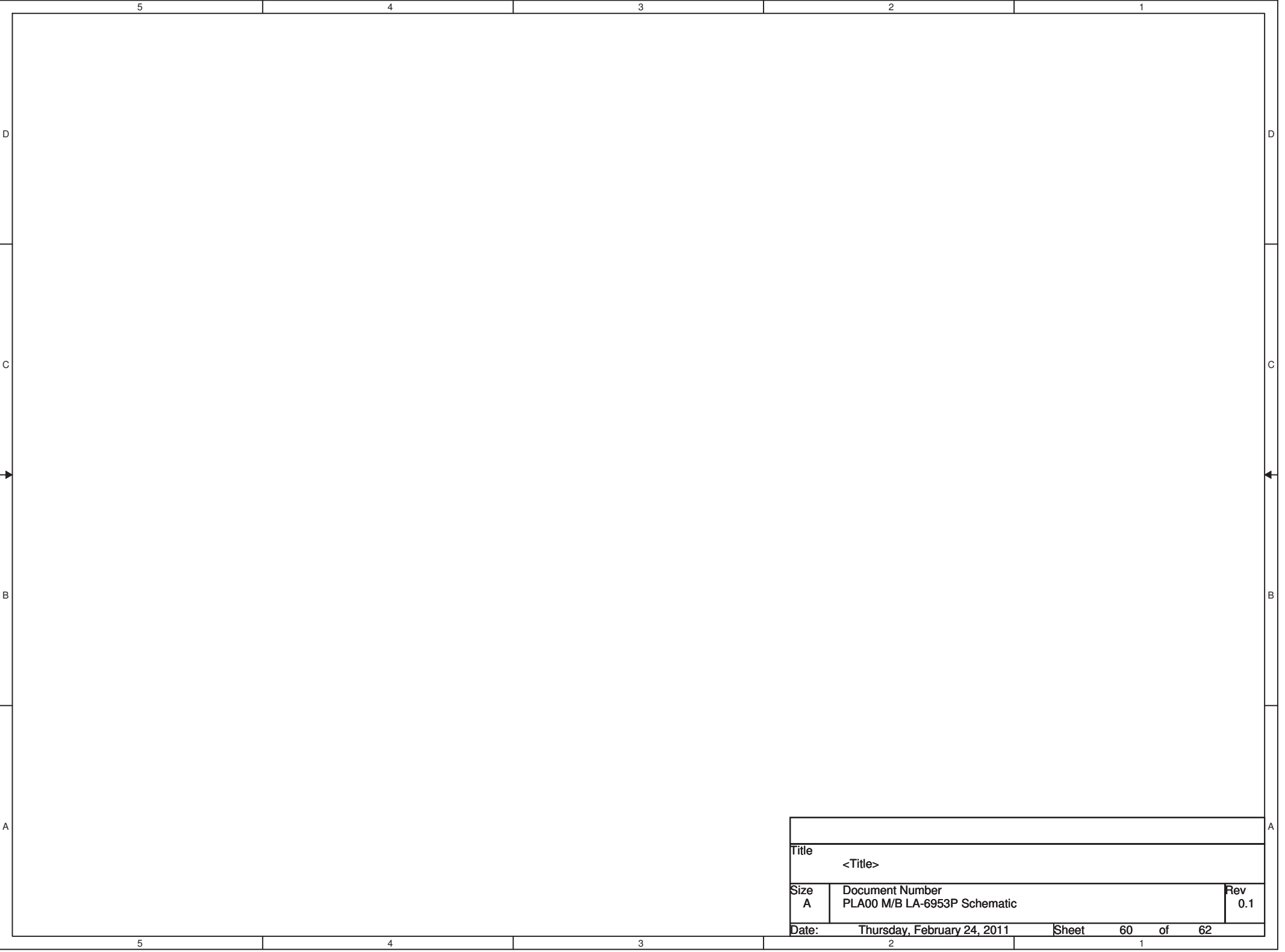
(Default)

Compal Electronics, Inc.

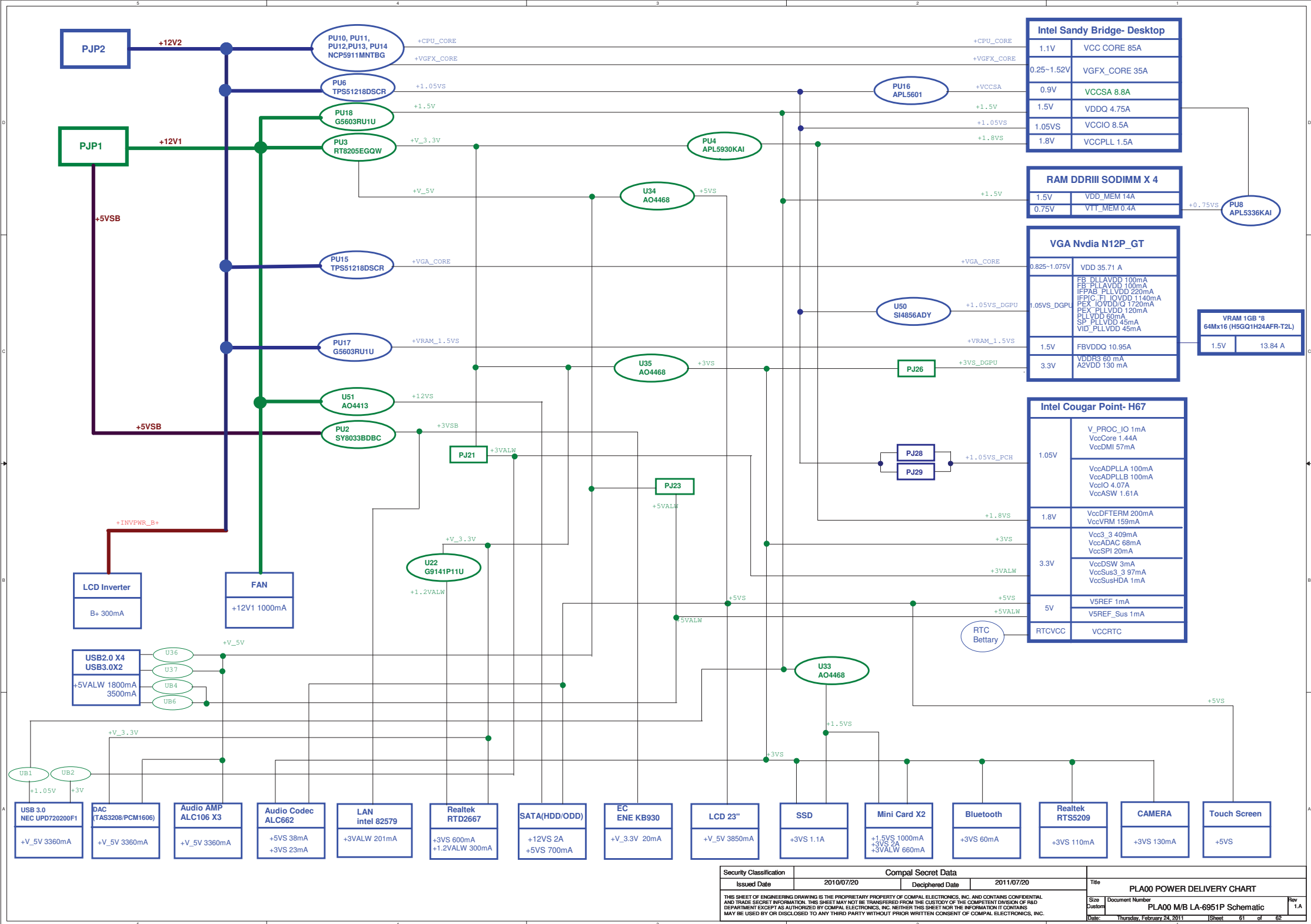
Title	VGA CORE
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Size	Document Number	Rev
Custom		0.1

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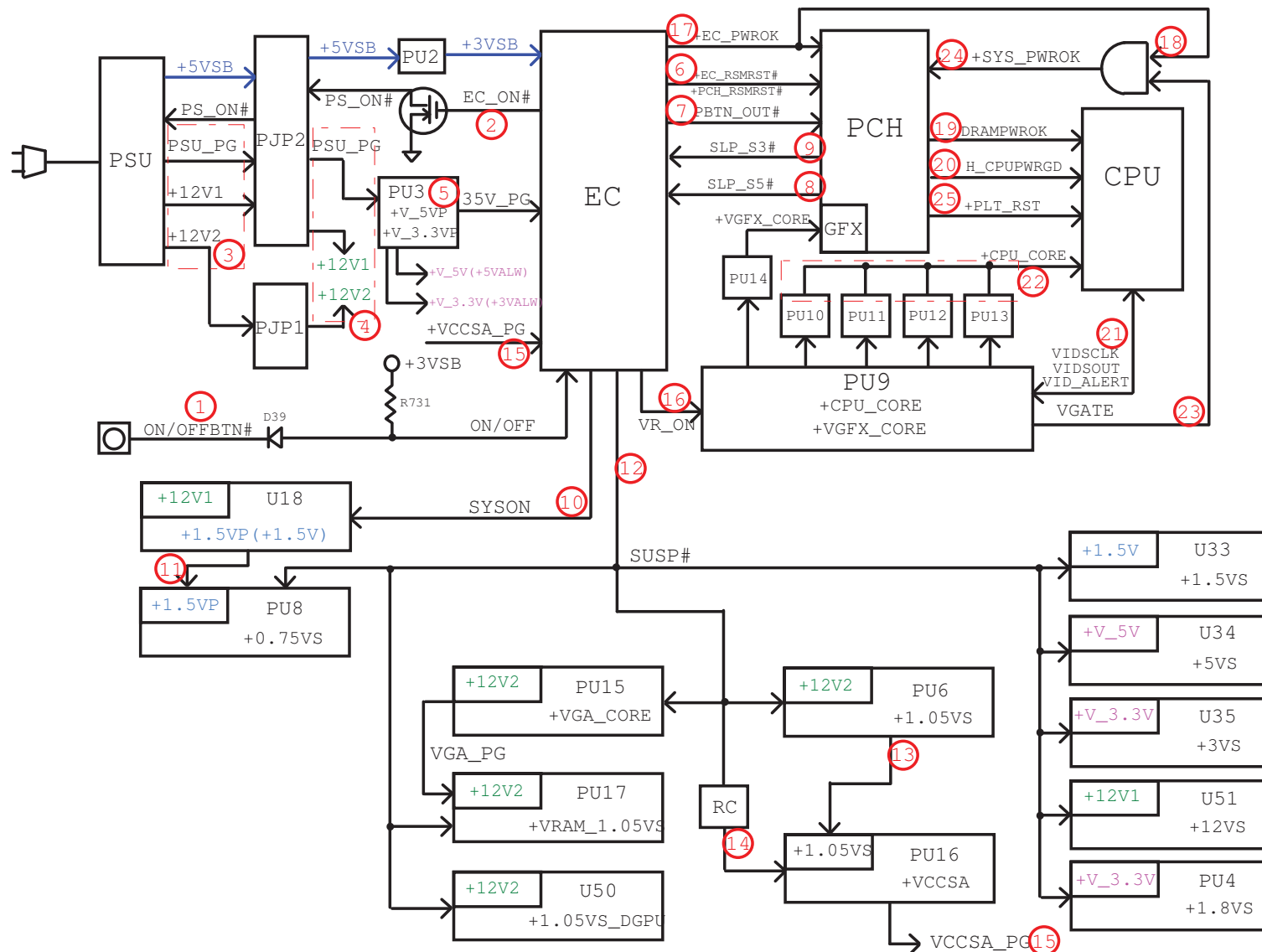


				A
Title				
<Title>				
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COMPAL CONFIDENTIAL

MODEL NAME: *PLA00 Power Sequence Block Diagram (Discrete)*
PCB NAME: *LA6951P*
REVISION: *0.3*
DATE: *2010/10/26*



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