Lenovo IdeaPad B570 Z570 V570

Sandy Bridge

Intel PCH Cougar Point

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A3 | Document Number: LZ57 | Rev: -1

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Block Diagram (UMA/Optimus co-lay)

Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC

USB BD
POWER BD 48.4IH03.08A
Finger Printer BD 48.4IH04.08A
IO BD 48.4IH02.08A
AV BD

##OnMainBoard
VRAM 1GB/512MB 88,89,90,91
DDR3 800MHz
NVIDIA N12P-GE/GV 83,84,85,86,87
PCIe x 16 (Discrete only)
Intel CPU Sandy Bridge DDRIII: 1066/1333/1666 MHz 4,5,6,7,8,9,10
DDRIII 1066/1333/1666 Channel A
DDRIII 1066/1333/1666 Channel B
DDRIII Slot 0 1066/1333/1666 14
DDRIII Slot 1 1066/1333/1666 15
FDI x 4 x 2 (UMA only)
DMI x 4
HDMI 51
LCD 49
CRT 50
HDMI
LVDS
RGB CRT
Intel PCH Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25
BD USB x 2
Bluetooth 63
CAMERA 49
Finger Print 64
USB2.0 x 5
SD/MMC+/MS/ MS Pro/xD 74
CardReader Realtek RTS5139
USB 2.0 x 1
AZALIA
PCIE x 1
GLAN RTL8111E 31
RJ45 CONN 55
PCIE x 1/USB2.0 x 1
Mini-Card WLAN 65
Mini-Card WWAN 66
SIM 66
NEC uPD720200 35
MB USB 3.0 x 1 62
USB 2.0 x 1/SATA x 1
E-SATA/USB comb 57
SATA x 2
HDD 56
ODD 56
SPI
LPC Bus
Flash ROM 4MB 60
LPC debug port 71
KBC NUVOTON NPCE795 27
SMBus
G-Sensor 79
Touch PAD 69
Int. KB 69
Thermal EMC2103-2-AP 28
Fan 28
I/O BD
Internal DMIC
HP1
MIC IN
Azalia CODEC Realtek RTC8111E G1454 29
2CH SPEAKER

SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~~10 kΩ~~ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I2 C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: Table of Content

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_ICOMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

delete R404&RN 401 @20100630

62.10055.321

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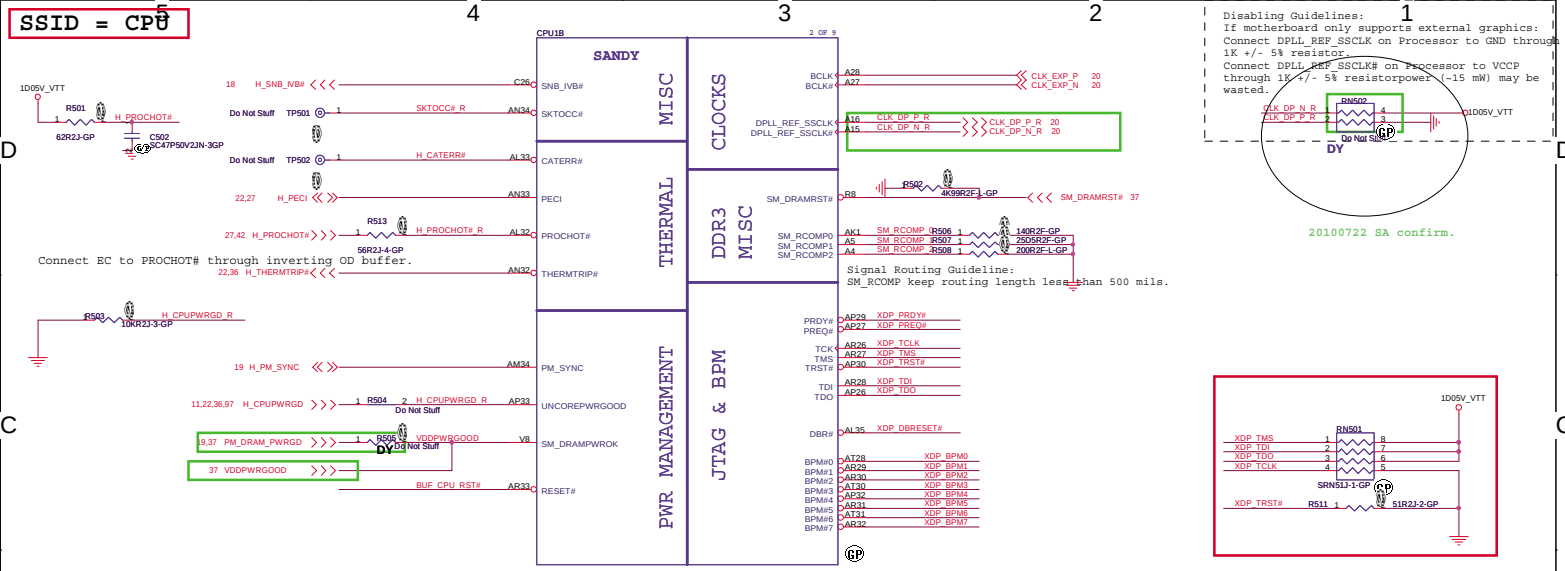
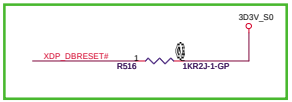
Title: CPU (PCIE/DMI/FDI)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 4 of 102	

SSID = CPU

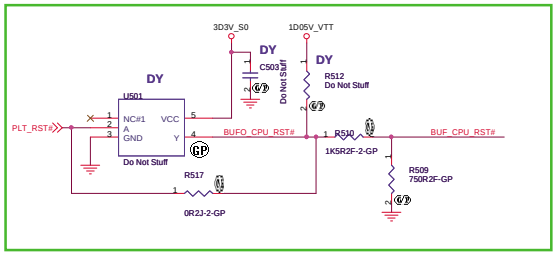


Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

20100722 SA confirm.



20100722 follow Astro add buffer



XDP_PREQ# 11
XDP_PRDY# 11
XDP_BPM0 11
XDP_BPM1 11
XDP_BPM2 11
XDP_BPM3 11
XDP_BPM4 11
XDP_BPM5 11
XDP_BPM6 11
XDP_BPM7 11
XDP_TDO 11
XDP_TDI 11
XDP_TRST# 11
XDP_TCLK 11
XDP_TMS 11
XDP_DBRESET# 11,19

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A3	LZ57	-1

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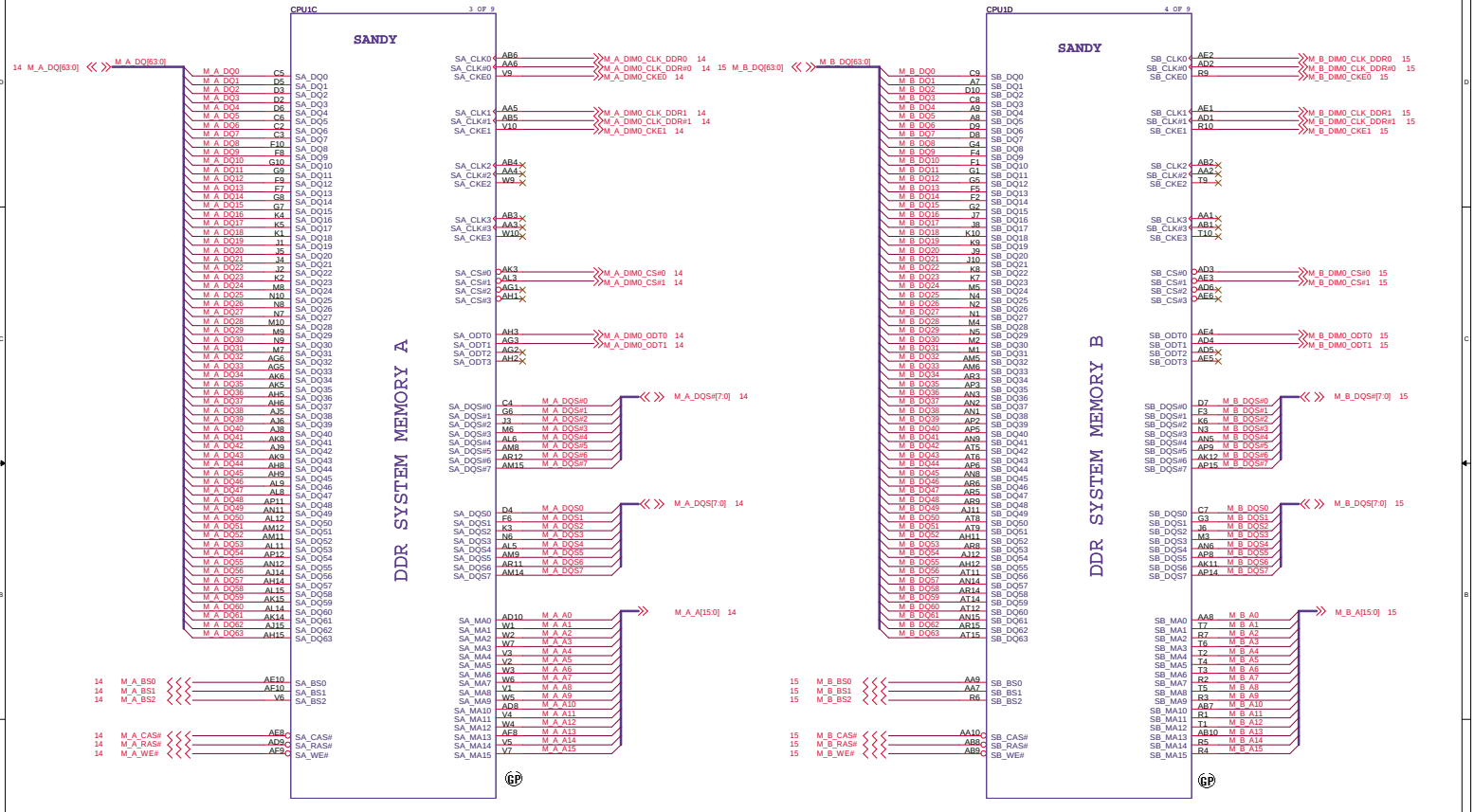
SSID = CPU



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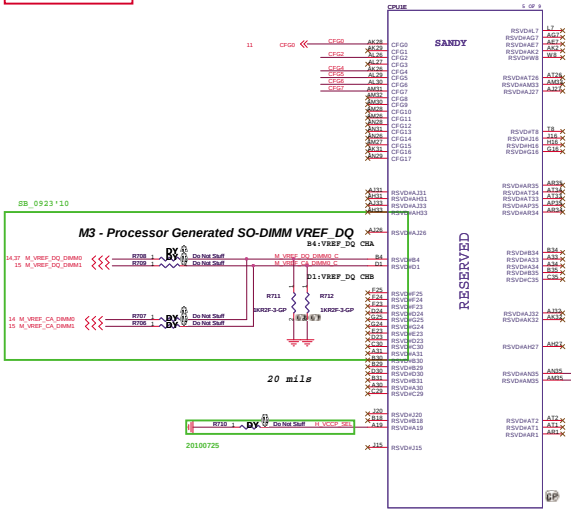
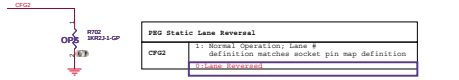
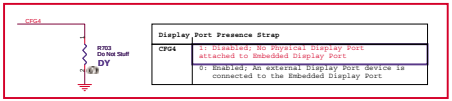
Title	**CPU (DDR)**	
Size: A3	Document Number: **LZ57**	Rev: **-1**
Date: Tuesday, March 29, 2011	Sheet 6 of 102	

SSID = CPU

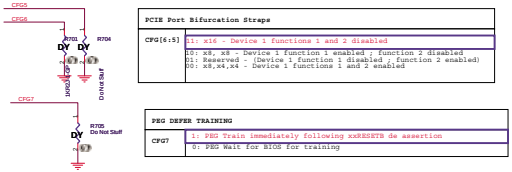




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled / function 2 disabled 01: Reserved - (Device 1 function 1 disabled / function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

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SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

C801 C802 C803 C804 C811 — SC10U6D3V5KX-1GP

C815 C817 C818 C819 C820 — SC10U6D3V5KX-1GP

C816 C821 C822 C823 C824 C825 C826 C827 — SC10U6D3V5KX-1GP

C837 C836 C835 C834 C833 C832 C831 C828 — SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F — SANDY — 6 OF 9

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

PEG AND DDR

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 — VCCIO

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 — SC10U6D3V5KX-1GP — Do Not Stuff / DY

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 — VCCIO

C812 C813 C814 C829 C830 C842 C843 C844 C845 — SC10U6D3V5KX-1GP — Do Not Stuff / DY

J23 — VCCIO

R804 need to close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 1 — 130R2F-1-GP

S-HS_20100610 V1.0

CORE SUPPLY

SVID

VIDALERT# — AJ29 — H_CPU_SVIDALRT# — R803 1 — 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK — AJ30 — H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT — AJ28 — H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

SENSE LINES

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE — AJ35
VSS_SENSE — AJ34
VCCSENSE 42
VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE — B10
VSSIO_SENSE — A10
VCCIO_SENSE 45
VSSIO_SENSE 45

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: LZ57 | Rev: -1

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — 7 OF 9

SANDY

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

VCC_GFXCORE

PROCESSOR VAXG: 24A

VAXG_SENSE
VSSAXG_SENSE

VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

SM_VREF

+V_SM_VREF_CNT
+V_SM_VREF_CNT 37

Close to CPU

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

S-HR_20100609 V1.0

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

TC903 ST330U2VDM-4-GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

R902 Notice:pull-high 100k or 10k
100R2F-L1-GP-U

VCCSA_SENSE
VCCSA_SENSE 48

H_FC_C22 48
VCCSA_SEL 48

RN901
SRN1KJ-7-GP

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

TC902 ST330U2VDM-4-GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

20100721 standard schematic update

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Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: LZ57 | Rev: -1

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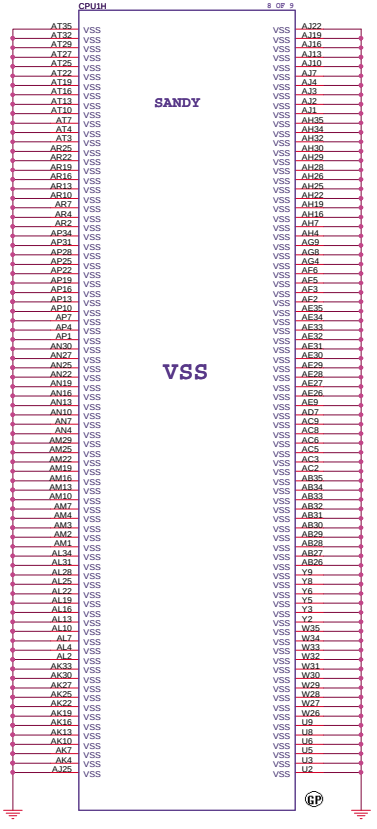
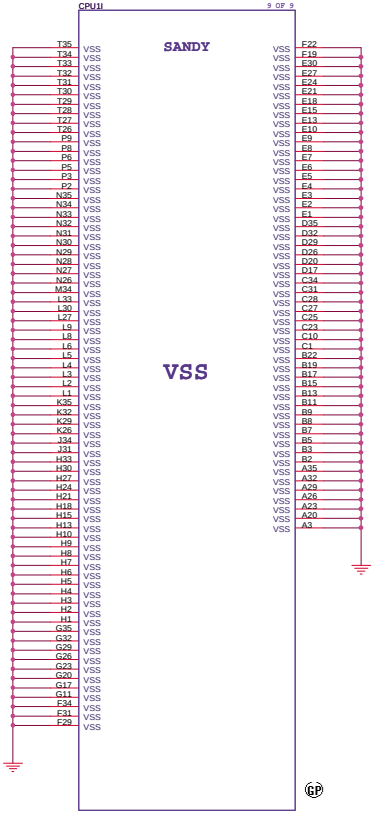
SSID = CPU





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Title	***CPU (VSS)***	
Size A3	Document Number **LZ57**	Rev **-1**
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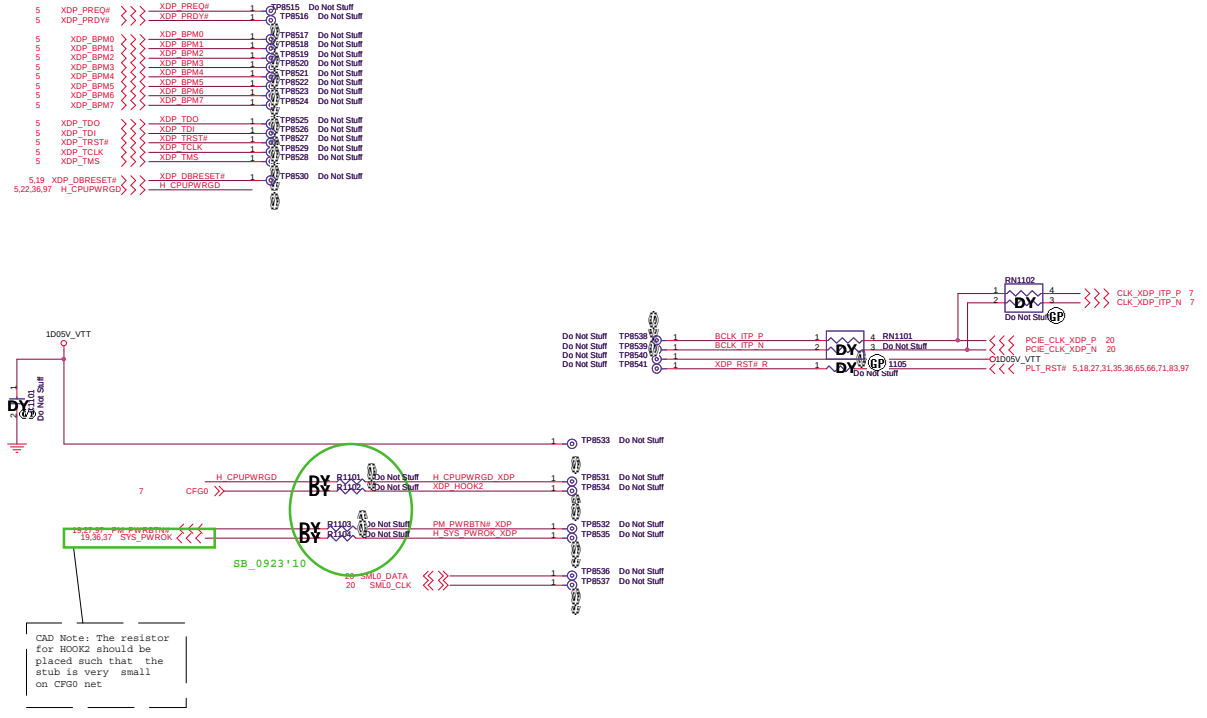

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***XDP***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 11 of 102	

(Blanking)

BOM

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Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 12 of 102

(Blanking)

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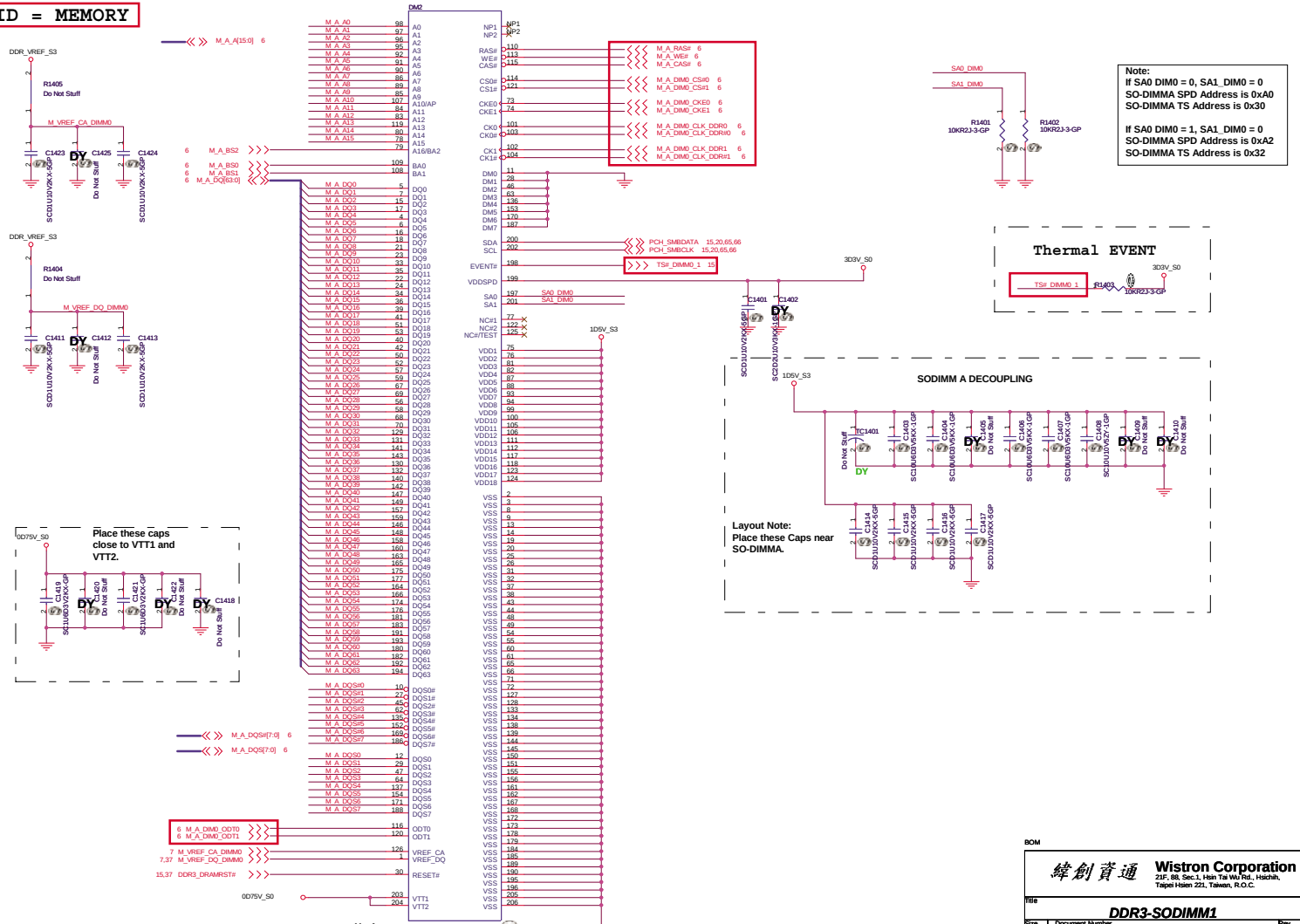
Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 13 of 102

SSID = MEMORY

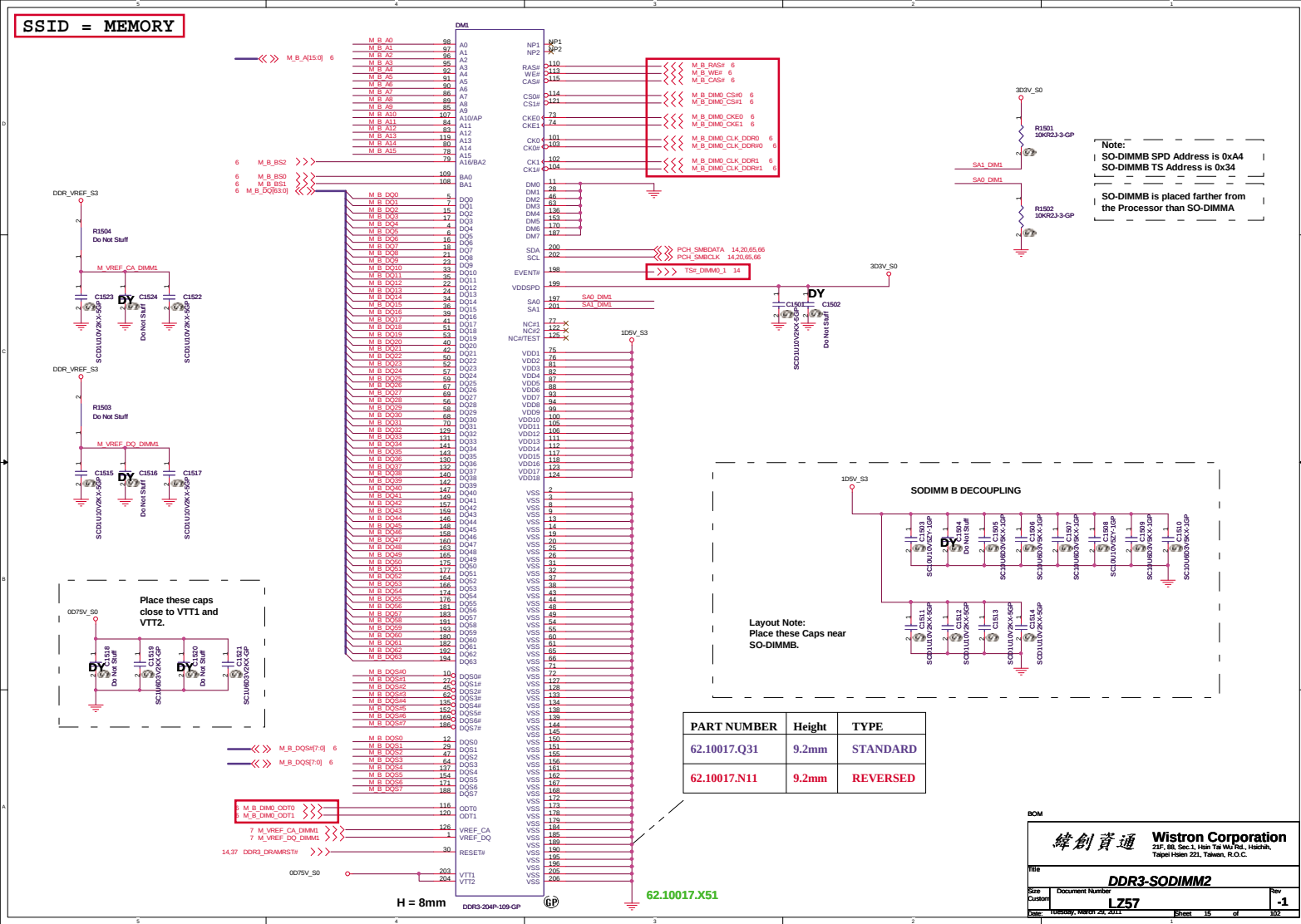


BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
Custom	LZ57	-1
Date: Tuesday, March 29, 2011	Sheet 14 of 102	



PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 15 of 102

(Blanking)

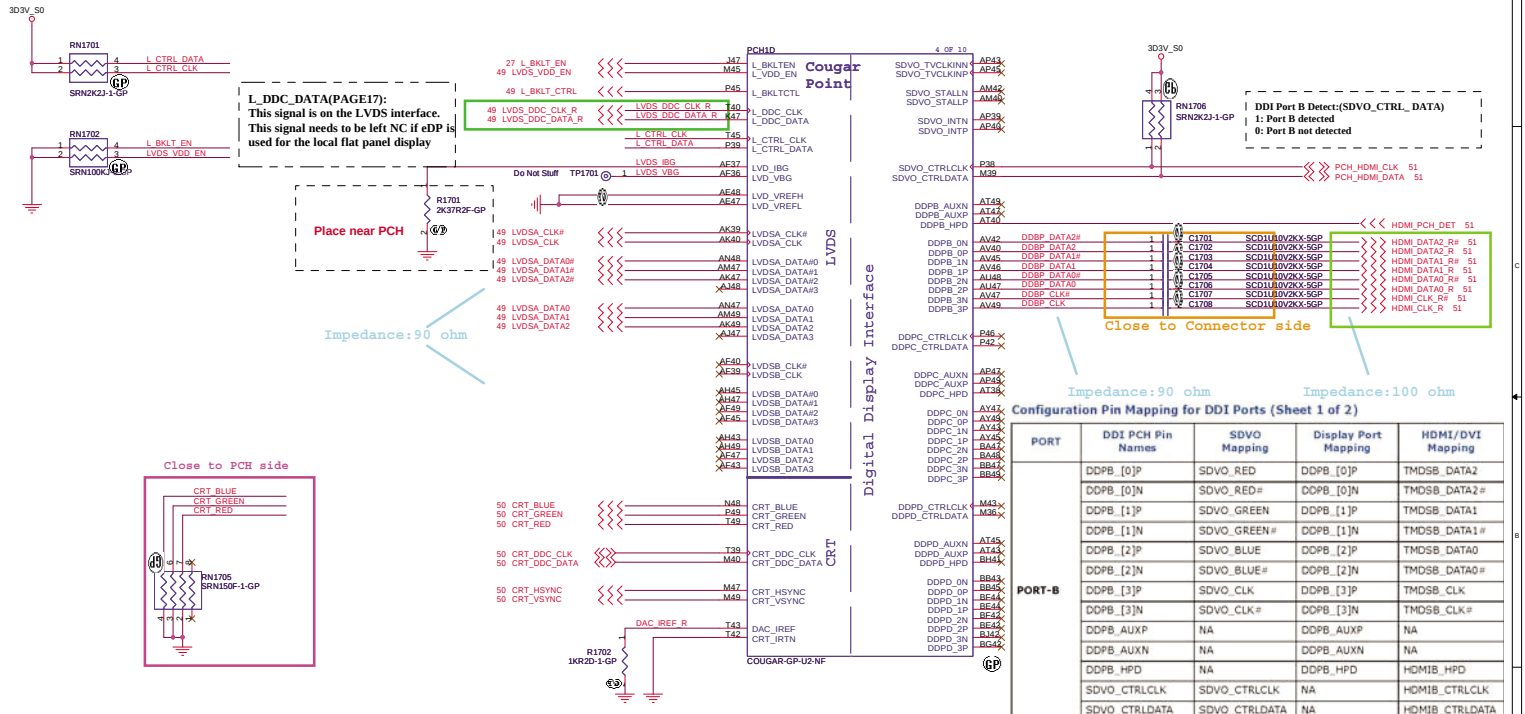
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 17 of 102

SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

+V_NVRAM_VCCQ
R1808 2K2R2J-2-GP
NV_CLE 1 R1809 1KR2J-1-GP H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

RN1801 SRN8K2J-2-GP
INT_PIRQA# 1, INT_PIRQE# 2, INT_PIRQC# 3, INT_PIRQB# 4, 5
10 3D3V_S0, 9 INT_PIRQH#, 8 INT_PIRQG#, 7 INT_PIRQD#, 6 INT_PIRQF#
3D3V_S0

R1801 DY 1 Do Not Stuff PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

PCH1E — Cougar Point — 5 OF 10

RSVD: BG26 TP1, BJ26 TP2, BH25 TP3, BJ16 TP4, BG16 TP5, AH38 TP6, AH37 TP7, AK43 TP8, AK45 TP9, C18 TP10, N30 TP11, H3 TP12, AH12 TP13, AM4 TP14, AM5 TP15, Y13 TP16, K24 TP17, L24 TP18, AB46 TP19, AB45 TP20; B21 TP21, M20 TP22, AY16 TP23, AG46 TP24; BE28 TP25, BC30 TP26, BE32 TP27, BJ32 TP28, BC28 TP29, BE30 TP30, BF32 TP31, BG32 TP32, AY26 TP33, BB26 TP34, AU28 TP35, AY30 TP36, AU26 TP37, AY26 TP38, AY28 TP39, BW30 TP40

NVRAM: RSVD#AY7 AV7, RSVD#AV7 AU3, RSVD#AU3 BG4, RSVD#BG4 AT10, RSVD#AT10 BC8, RSVD#BC8 AU2, RSVD#AU2 AT4, RSVD#AT4 AT3, RSVD#AT3 AT1, RSVD#AT1 AY3, RSVD#AY3 AT5, RSVD#AT5 AV3, RSVD#AV3 AV1, RSVD#AV1 BB1, RSVD#BB1 BA3, RSVD#BA3 BB5, RSVD#BB5 BB3, RSVD#BB3 BB7, RSVD#BB7 BC8, RSVD#BE8 BD4, RSVD#BD4 BF6, RSVD#BF6 AV5, RSVD#AV5 AY1, DF_TVS AV10, RSVD#AV10 AT8, RSVD#AT8 AY5, RSVD#AY5 BA2, RSVD#BA2 AT12, RSVD#AT12 BF3, RSVD#BF3

NV_ALE, NV_CLE, NV_RCOMP 1 TP1803 Do Not Stuff

+V_NVRAM_VCCQ
Danbury Technology: Disabled when Low. Enable when High.
R1810 Do Not Stuff DY
NV_ALE

RN1803 SRN10KJ-5-GP
DGPU_HOLD_RST# 1, DGPU_PWR_EN# 2, 3, 4

USB: USBP0N C24, USBP0P A24, USBP1N C25, USBP1P B25, USBP2N C26, USBP2P A26, USBP3N K28, USBP3P H28, USBP4N E28, USBP4P D28, USBP5N C28, USBP5P A28, USBP6N C29, USBP6P B29, USBP7N N28, USBP7P M28, USBP8N L30, USBP8P K30, USBP9N G30, USBP9P E30, USBP10N C30, USBP10P A30, USBP11N L32, USBP11P K32, USBP12N G32, USBP12P E32, USBP13N C32, USBP13P A32, USBRBIAS# C33, USBRBIAS B33

USB_PN1 62, USB_PP1 62, USB_PN2 64, USB_PP2 64, USB_PN3 63, USB_PP3 63, USB_PN4 66, USB_PP4 66, USB_PN5 82, USB_PP5 82, USB_PN8 57, USB_PP8 57, USB_PN9 82, USB_PP9 82, USB_PN10 82, USB_PP10 82, USB_PN11 65, USB_PP11 65, USB_PN12 49, USB_PP12 49

USB_RBIAS 1 R1811 22D6R2F-L1-GP

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SW programing USB_OC#12_13 for USB 9

OC0#/GPIO59 A14, OC1#/GPIO40 K20, OC2#/GPIO41 B17, OC3#/GPIO42 C16, OC4#/GPIO43 L16, OC5#/GPIO9 A16, OC6#/GPIO10 D14, OC7#/GPIO14 C14

USB_OC#0_1 62, USB_OC#2_3, USB_OC#4_5, USB_OC#6_7, USB_OC#8_9, USB_OC#10_11, USB_OC#12_13, PCH_GPIO14

R1820 0R2J-2-GP LZ57_6L -1_1209'10

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

DGPU_HOLD_RST# 93, DGPU_PWR_EN# 93, DGPU_SELECT# 44, DGPU_PWM_SELECT# 42, BBS_BIT1 47, PCI_GNT3# 49

R1814 DY Do Not Stuff
INT_PIRQA# 40, INT_PIRQB# 38, INT_PIRQC# 39, INT_PIRQD# 38
REQ1#/GPIO50 46, REQ2#/GPIO52 44, REQ3#/GPIO54 40
GNT1#/GPIO51 47, GNT2#/GPIO53 42, GNT3#/GPIO55 49
PIRQE#/GPIO2 42, PIRQF#/GPIO3 40, PIRQG#/GPIO4 42, PIRQH#/GPIO5 44
PME# K10, PLTRST# C6
CLKOUT_PCI0 H49, CLKOUT_PCI1 H43, CLKOUT_PCI2 J48, CLKOUT_PCI3 K42, CLKOUT_PCI4 H40
COUGAR-GP-U2-NF

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

R1802 DY Do Not Stuff BBS_BIT1
R1803 DY Do Not Stuff BBS_BIT0
BBS_BIT0 21

TP1805 Do Not Stuff, TP1804 Do Not Stuff, TP1802 Do Not Stuff

SC_1026'10
78 dGPU_LED, 27,56 SATA_ODD_DAS, USB30_SMI# 35, DCR_EN# 49
R1818 1 INT_PIRQE#, R1813 1 INT_PIRQF#, 0R2J-2-GP
R1815 Do Not Stuff, 2 INT_PIRQH#, R1817 Do Not Stuff

SC_1025'10
65,71 CLK_PCI_LPC, 20 CLK_PCI_FB, 27 CLK_PCI_KBC
R1804 1 22R2J-2-GP CLK_PCI_LPC_R
R1805 1 22R2J-2-GP CLK_PCI_FB_R
R1806 1 22R2J-2-GP CLK_PCI_KBC_R

EC1802 DY Do Not Stuff, EC1801 DY Do Not Stuff

KBC CLK EMI

3D3V_S0
U1801 VCC B, Y A, GND
DY Do Not Stuff
27,31,35,36,65,66,71,83,97 PLT_RST#
PCI_PLTRST#
R1807 1 Do Not Stuff 0R2J-2-GP
C1802 DY Do Not Stuff
R1816 DY
C1801 DY Do Not Stuff
20100629

RN1802 SRN10KJ-L3-GP
USB_OC#2_3 1, USB_OC#4_5 2, USB_OC#6_7 3, USB_OC#10_11 4, 5
10 3D3V_S5, 9 USB_OC#12_13, 8 USB_OC#8_9, 7 PCH_GPIO14, 6 USB_OC#0_1
3D3V_S5

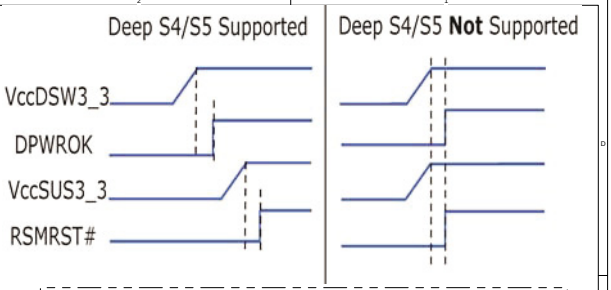
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: LZ57 | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1. VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2. DPWROK and RSMRST# will rise at the same time (connected on board)
3. SLP_SUS# and SUSACK# are left as 'no connect'
4. SUSWARN# used as SUSPWRDNACK/GPIO30

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

20100729

84.2N702.A3F
2nd = 84.DM601.03F

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (DM I/FDI/PM)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 19 of 102	

SSID = PCH

20100705_Standard

65 PCIE_RXN2
65 PCIE_RXP2
65 PCIE_TXN2
65 PCIE_TXP2
C2001 1 SCD1U10V2KX-5GP PCIE_TXN2_C
C2002 1 SCD1U10V2KX-5GP PCIE_TXP2_C

31 PCIE_RXN4
31 PCIE_RXP4
31 PCIE_TXN4
31 PCIE_TXP4
C2005 1 SCD1U10V2KX-5GP PCIE_TXN4_C
C2006 1 SCD1U10V2KX-5GP PCIE_TXP4_C

35 PCIE_RXN5
35 PCIE_RXP5
35 PCIE_TXN5
35 PCIE_TXP5
C2009 1 SCD1U10V2KX-5GP PCIE_TXN5_C
C2010 1 SCD1U10V2KX-5GP PCIE_TXP5_C
USB3.0
USB3.0

PCH1B

Cougar Point

BG34 PERN1 / BJ34 PERP1 / AV32 PETN1 / AU32 PETP1 — W-WAN
BE34 PERN2 / BF34 PERP2 / BB32 PETN2 / AY32 PETP2 — WLAN
BG36 PERN3 / BJ36 PERP3 / AV34 PETN3 / AU34 PETP3 — Card Reader
BE36 PERN4 / BF36 PERP4 / AY34 PETN4 / BB34 PETP4 — LAN
BG37 PERN5 / BJ37 PERP5 / AY36 PETN5 / BB36 PETP5 — USB3.0
BJ38 PERN6 / BG38 PERP6 / AU36 PETN6 / AV36 PETP6 — Intel GBE LAN
BG40 PERN7 / BJ40 PERP7 / AY40 PETN7 / BB40 PETP7 — Dock
BE38 PERN8 / BC38 PERP8 / AV38 PETN8 / AY38 PETP8 — NEW CARD

PCI-E*

2 OF 10

SMBUS

SMBALERT#/GPIO11 E12 — EC_SW# — EC_SW# 27
SMBCLK H14 — SMB_CLK
SMBDATA C9 — SMB_DATA
SML0ALERT#/GPIO60 A12 — DRAMRST_CNTRL_PCH — DRAMRST_CNTRL_PCH 37
SML0CLK C8 — SML0_CLK — SML0_CLK 11
SML0DATA G12 — SML0_DATA — SML0_DATA 11
SML1ALERT#/PCHHOT#/GPIO74 C13 — PCH_GPIO74
SML1CLK/GPIO58 E14 — SML1_CLK — SML1_CLK 27
SML1DATA/GPIO75 M16 — SML1_DATA — SML1_DATA 27

Controller Link

CL_CLK1 M7 — CL_CLK — TP2001 Do Not Stuff
CL_DATA1 T11 — CL_DATA — TP2002 Do Not Stuff
CL_RST1# P10 — CL_RST# — TP2003 Do Not Stuff

CLOCKS

WWAN CLK
WLAN CLK
LAN CLK
USB3.0 CLK

CLKOUT_PCIE0N Y40 / CLKOUT_PCIE0P Y39
CLK_PCIE_WWAN_REQ# — PCIECLKRQ0#/GPIO73 J2
CLKOUT_PCIE1N AB49 / CLKOUT_PCIE1P AB47
65 CLK_PCIE_WLAN# / 65 CLK_PCIE_WLAN
21,65 CLK_PCIE_WLAN_REQ# — PCIECLKRQ1#/GPIO18 M1
CLKOUT_PCIE2N AA48 / CLKOUT_PCIE2P AA47
PCIE_CLK_RQ2# — PCIECLKRQ2#/GPIO20 V10
CLKOUT_PCIE3N Y37 / CLKOUT_PCIE3P Y36
31 CLK_PCIE_LAN# / 31 CLK_PCIE_LAN
19,31 PCIE_CLK_LAN_RQ1# — PCIECLKRQ3#/GPIO25 A8
CLKOUT_PCIE4N Y43 / CLKOUT_PCIE4P Y45
35 CLK_PCIE_USB3# / 35 CLK_PCIE_USB3
USB3_PEGB_CLKREQ# — PCIECLKRQ4#/GPIO26 L12
CLKOUT_PCIE5N V45 / CLKOUT_PCIE5P V46
PCIE_CLK_RQ5# — PCIECLKRQ5#/GPIO44 L14
CLKOUT_PEG_B_N AB42 / CLKOUT_PEG_B_P AB40
22 PEG_B_CLKRQ# — PEG_B_CLKRQ#/GPIO56 E6
CLKOUT_PCIE6N V40 / CLKOUT_PCIE6P V42
PCIE_CLK_RQ6# — PCIECLKRQ6#/GPIO45 T13
CLKOUT_PCIE7N V38 / CLKOUT_PCIE7P V37
CLK_PCIE_NEW_REQ# — PCIECLKRQ7#/GPIO46 K12
CLKOUT_ITPXDP_N AK14 / CLKOUT_ITPXDP_P AK13
11 PCIE_CLK_XDP_N / 11 PCIE_CLK_XDP_P

COUGAR-GP-U2-NF

PEG_A_CLKRQ#/GPIO47 M10 — PEG_CLKREQ#_R — R2003 1 2 Do Not Stuff — PEG_CLKREQ# 83
CLKOUT_PEG_A_N AB37 — CLK_PCIE_VGA# 83
CLKOUT_PEG_A_P AB38 — CLK_PCIE_VGA 83
CLKOUT_DMI_N AV22 — CLK_EXP_N 5
CLKOUT_DMI_P AU22 — CLK_EXP_P 5
CLKOUT_DP_N AM12 — CLK_DP_N_R 5
CLKOUT_DP_P AM13 — CLK_DP_P_R 5
RN2017 Do Not Stuff
CLKIN_DMI_N BF18 — CLK_BUF_EXP_N
CLKIN_DMI_P BE18 — CLK_BUF_EXP_P
CLKIN_GND1_N BJ30 — CLK_BUF_CPYCLK_N
CLKIN_GND1_P BG30 — CLK_BUF_CPYCLK_P
RN2008 SRN10KJ-5-GP
CLKIN_DOT_96N G24 — CLK_BUF_DOT96_N
CLKIN_DOT_96P E24 — CLK_BUF_DOT96_P
CLKIN_SATA_N AK7 — CLK_BUF_CKSSCD_N
CLKIN_SATA_P AK5 — CLK_BUF_CKSSCD_P
REFCLK14IN K45 — CLK_BUF_REF14
CLK_BUF_REF14 — R2017 10KR2J-3-GP
CLKIN_PCILOOPBACK H45 — CLK_PCI_FB — CLK_PCI_FB 18
XTAL25_IN V47 — XTAL25_IN
XTAL25_OUT V49 — XTAL25_OUT
XCLK_RCOMP Y47 — XCLK_RCOMP — R2007 90D9R2F-1-GP — VCCDIFFCLKN

FLEX CLOCKS

CLKOUTFLEX0/GPIO64 K43 — JTAG_TCK — TP2004 Do Not Stuff
CLKOUTFLEX1/GPIO65 F47 — CLK_48_USB30 — TP2005 Do Not Stuff
CLKOUTFLEX2/GPIO66 H47 — LAN_25M — TP2006 Do Not Stuff
CLKOUTFLEX3/GPIO67 K49 — DGPU_PRSNT#

20100706

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2
if more than 2 PCI clocks + PCI loopback are routed.

3D3V_S5

PEG_CLKREQ# R — R2004 10KR2J-3-GP — DY — R2005 Do Not Stuff

SMB_CLK — RN2003 SRN2K2J-1-GP
SMB_DATA
SML0_DATA — RN2004 SRN2K2J-1-GP
SML0_CLK
SML1_CLK — RN2005 SRN2K2J-1-GP
SML1_DATA

20100729 follow CRB change to 1K

DRAMRST_CNTRL_PCH — R2009 1KR2J-1-GP

3D3V_S0

SRN2K2J-1-GP RN2007

2nd = 84.DM601.03F
84.2N702.A3F
2N7002KDW-GP

SMB_DATA — PCH_SMBDATA 14,15,65,66
Q2001
SMB_CLK — PCH_SMBCLK 14,15,65,66

XTAL25_IN — R2008 and C2008 CO-LAY — DY — Do Not Stuff
C2008
R2006 1M1R2J-GP
X2001 SC12P50V2JN-3GP XTAL-25MHZ-102-GP
82.30020.851
2nd = 82.30020.791
C2007 SC12P50V2JN-3GP

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
BG(PX) : 0 0
Optimus(Muxless) : 1 0
UMA
DY
OPS
UMA_DIS# — DGPU_PRSNT — UMA_DIS# 22

CLK_BUF_EXP_N — RN9407 SRN10KJ-6-GP
CLK_BUF_EXP_P
CLK_BUF_DOT96_N — RN9408 SRN10KJ-6-GP
CLK_BUF_DOT96_P
CLK_BUF_CKSSCD_N — RN9406 SRN10KJ-6-GP
CLK_BUF_CKSSCD_P

R2017 RN9407 RN9408 RN9406 need very close to PCH

RN2001 SRN10KJ-6-GP
SUS_PWR_ACK 19,27
PCH_GPIO74
PCIE_CLK_REQ5#
BATLOW# 19

RN2002 SRN10KJ-6-GP
CLK_PCIE_WWAN_REQ#
PCIE_CLK_REQ6#
USB3_PEGB_CLKREQ#
CLK_PCIE_NEW_REQ#

R2011 10KR2J-3-GP — EC_SW#

BOM

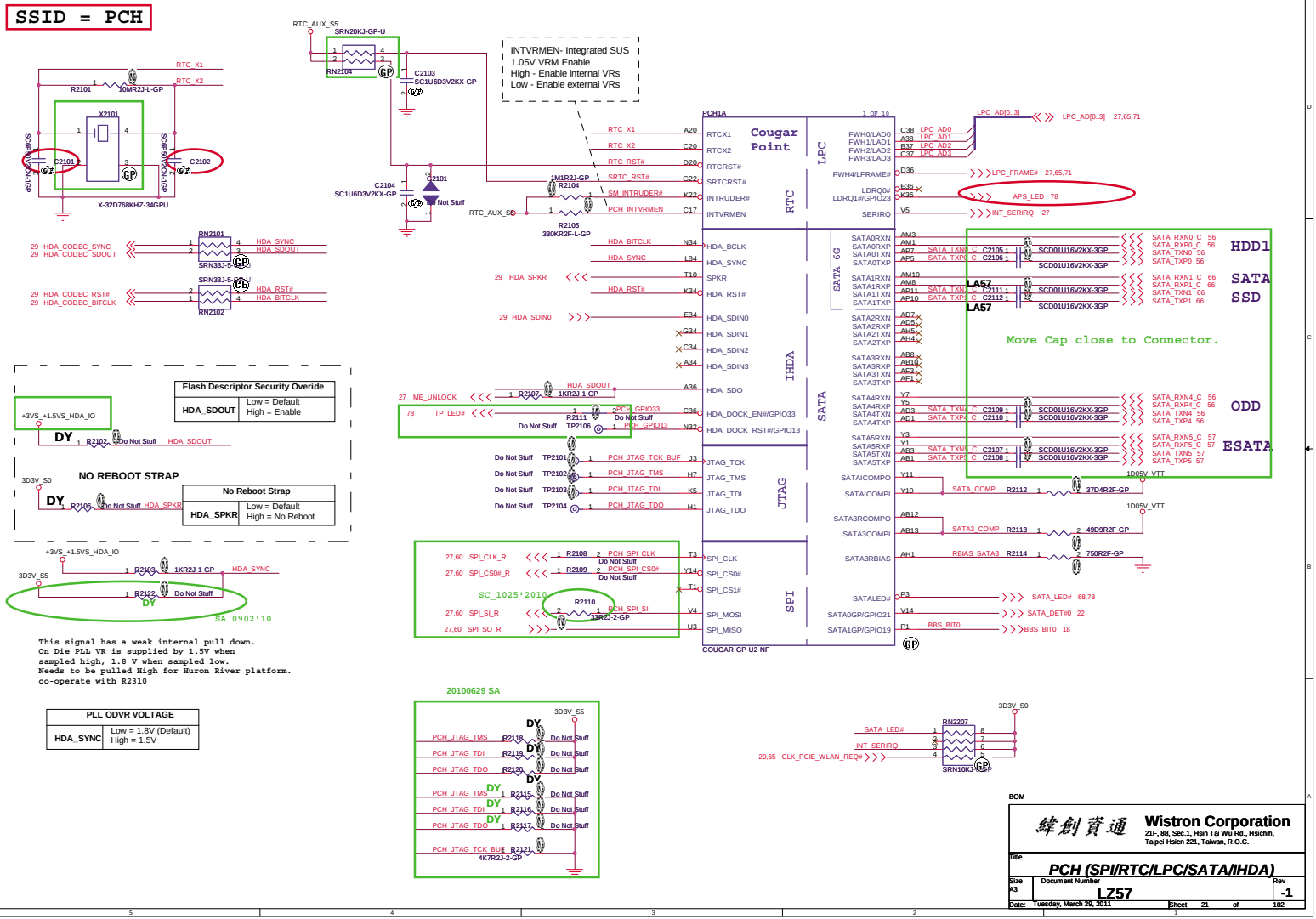
3D3V_S0 — R2016 10KR2J-3-GP — PCIE_CLK_RQ2#

PCIECLKRQ1# and PCIECLKRQ2# support S0 power only

S-HR_20100614 V1.1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	PCH (PCI-E/SMBUS/CLOCK/CL)		
Size A3	Document Number LZ57		Rev -1
Date: Tuesday, March 29, 2011	Sheet 20 of 102		

SSID = PCH



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (SPI/RTC/LPC/SATA/IHDA)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 21 of 102	

SSID = PCH

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Note:
For PCH debug with XDP, need to NO STUFF R2218

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

20100720 SW

SB 0923'10

20100729 follow Annie CRB

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

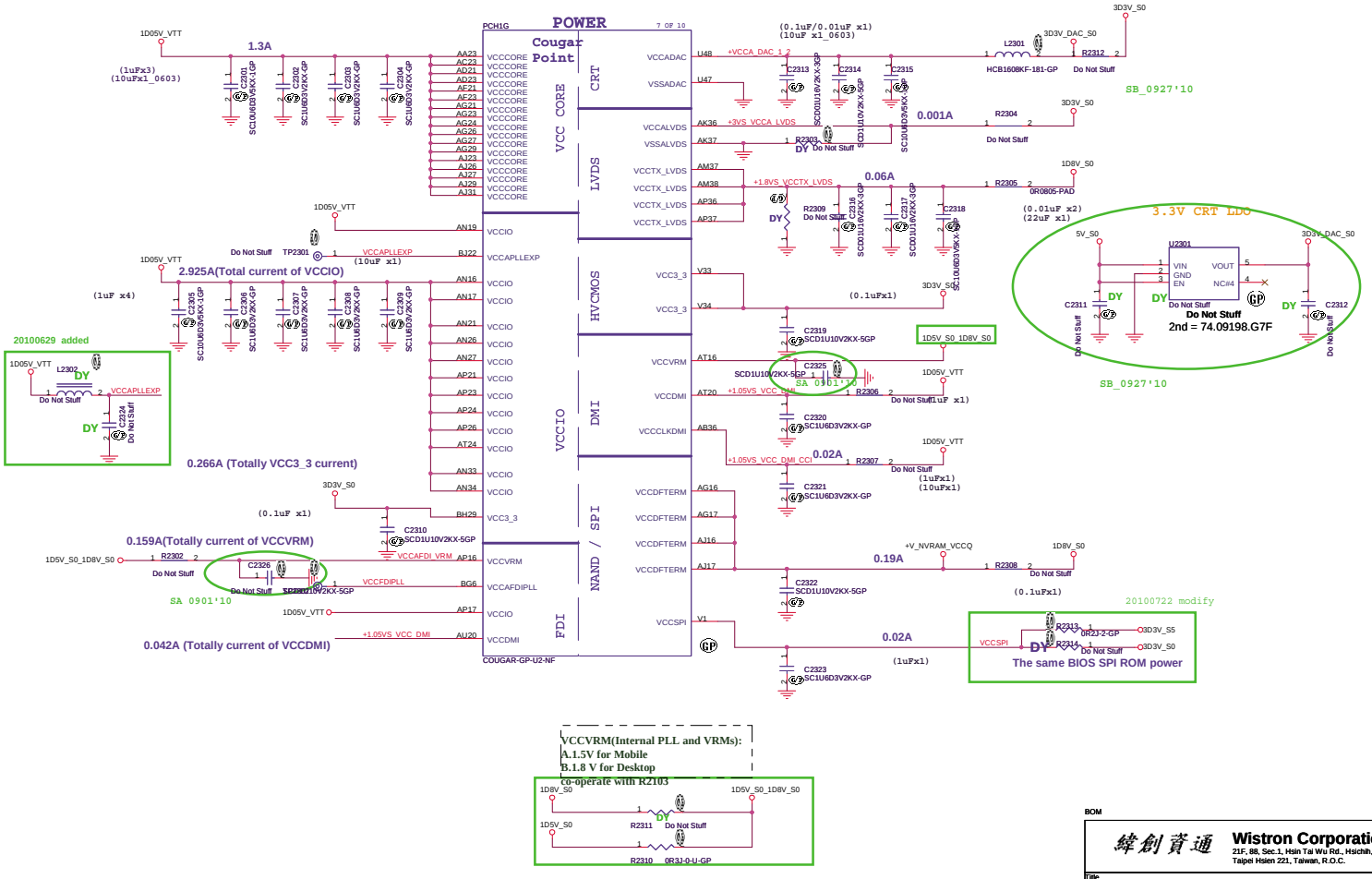
[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: PCH (GPIO/CPU)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 22 of 102	

SSID = PCH 6A



BOM

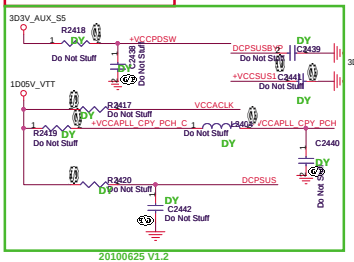
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

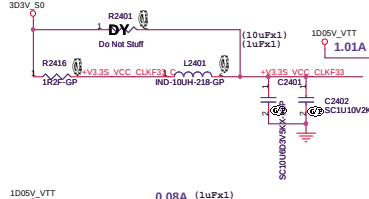
Title: **PCH (POWER1)**

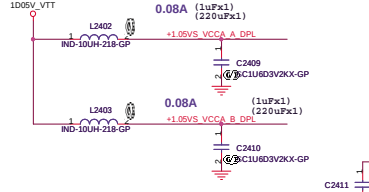
Size	Document Number	Rev
A3	LZ57	-1

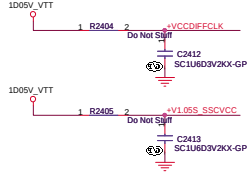
Date: Tuesday, March 29, 2011 Sheet 23 of 102

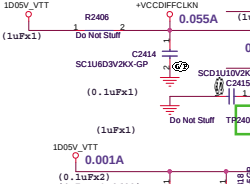
SSID = PCH

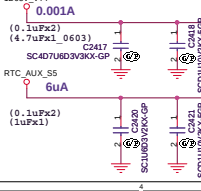






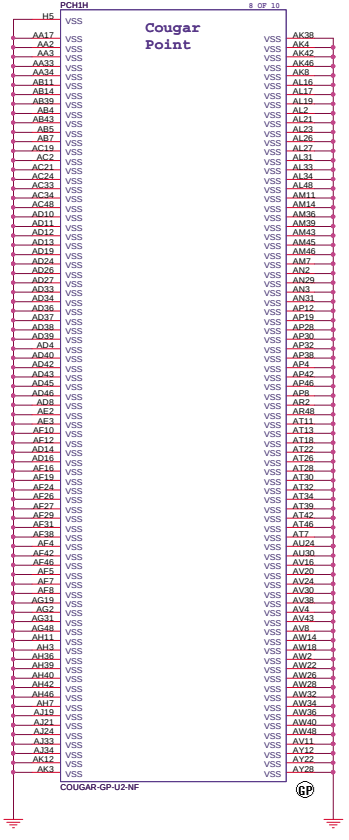


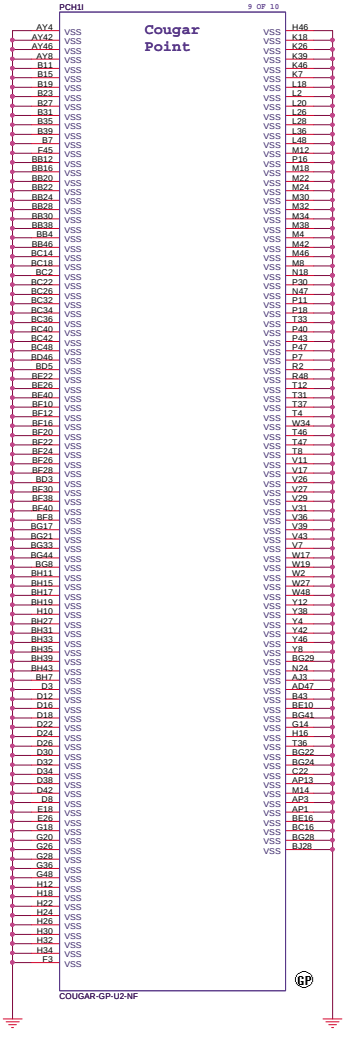




Title	PCH (POWER2)		
Size A3	Document Number LZ57		Rev -1
Date: Tuesday, March 29, 2011	Sheet 24 of 102		

SSID = PCH





BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (VSS)**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 25 of 102

(Blanking)

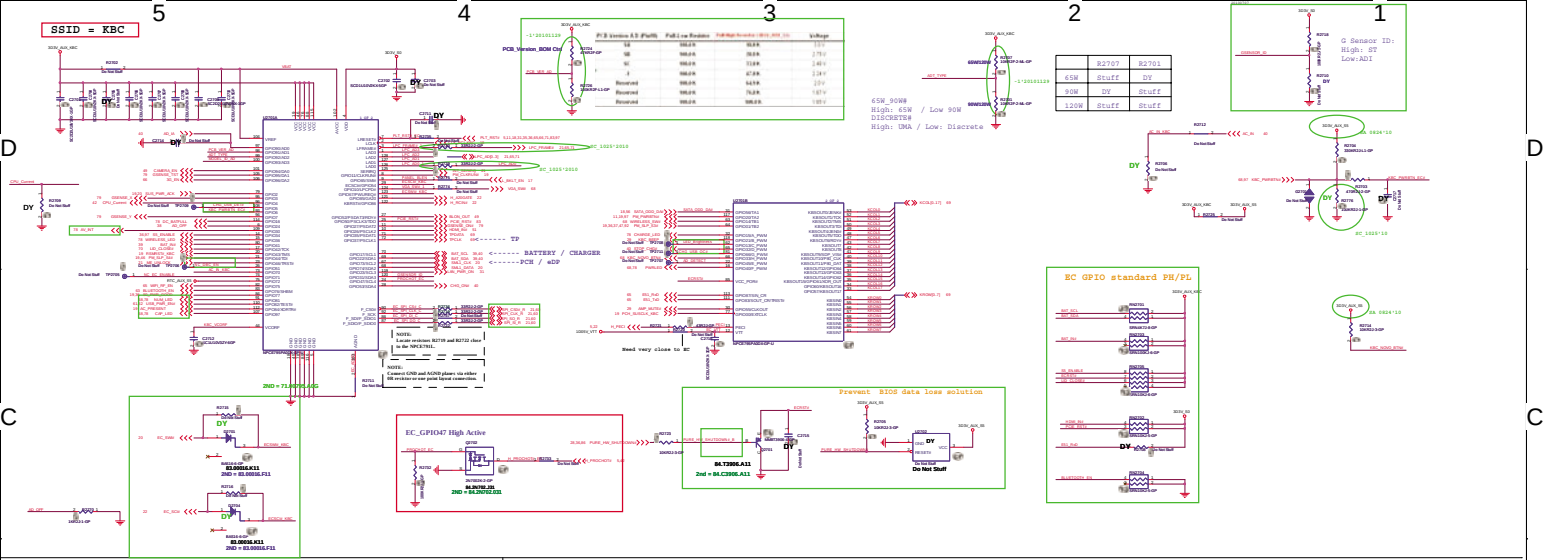
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 26 of 102



	R2707	R2701
65W	Stuff	DY
90W	DY	Stuff
120W	Stuff	Stuff

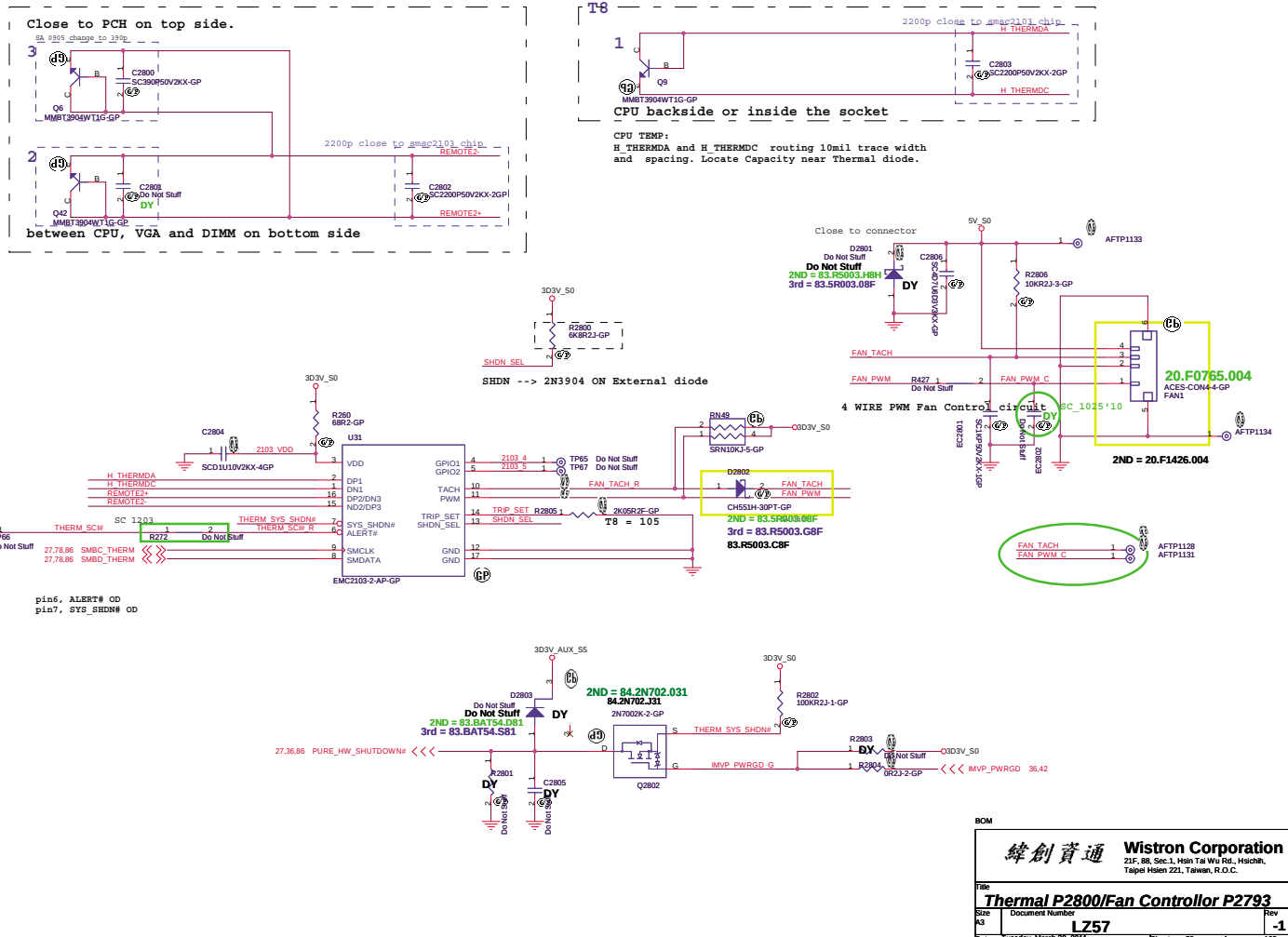
LILI Multi GPIO setting

Model_ID_BOM Ctrl OPS: 64.14335.6DL			
MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/W 57 UMA	100.0 K	44.9 K	2.001 V
V/W 57 OPTIMUS	100.0 K	76.8 K	1.847 V
Z 57 UMA	100.0 K	100.0 K	1.650 V
Z 57 OPTIMUS	100.0 K	143.0 K(64.14335.L01)	1.32 V

		Wistron Corporation	
Title:	KBC Nuvoton NPCE795		
Size:	Document Number: L257		Rev: -1
Date:	Sheet of		

SSID = Thermal

Thermal sensor



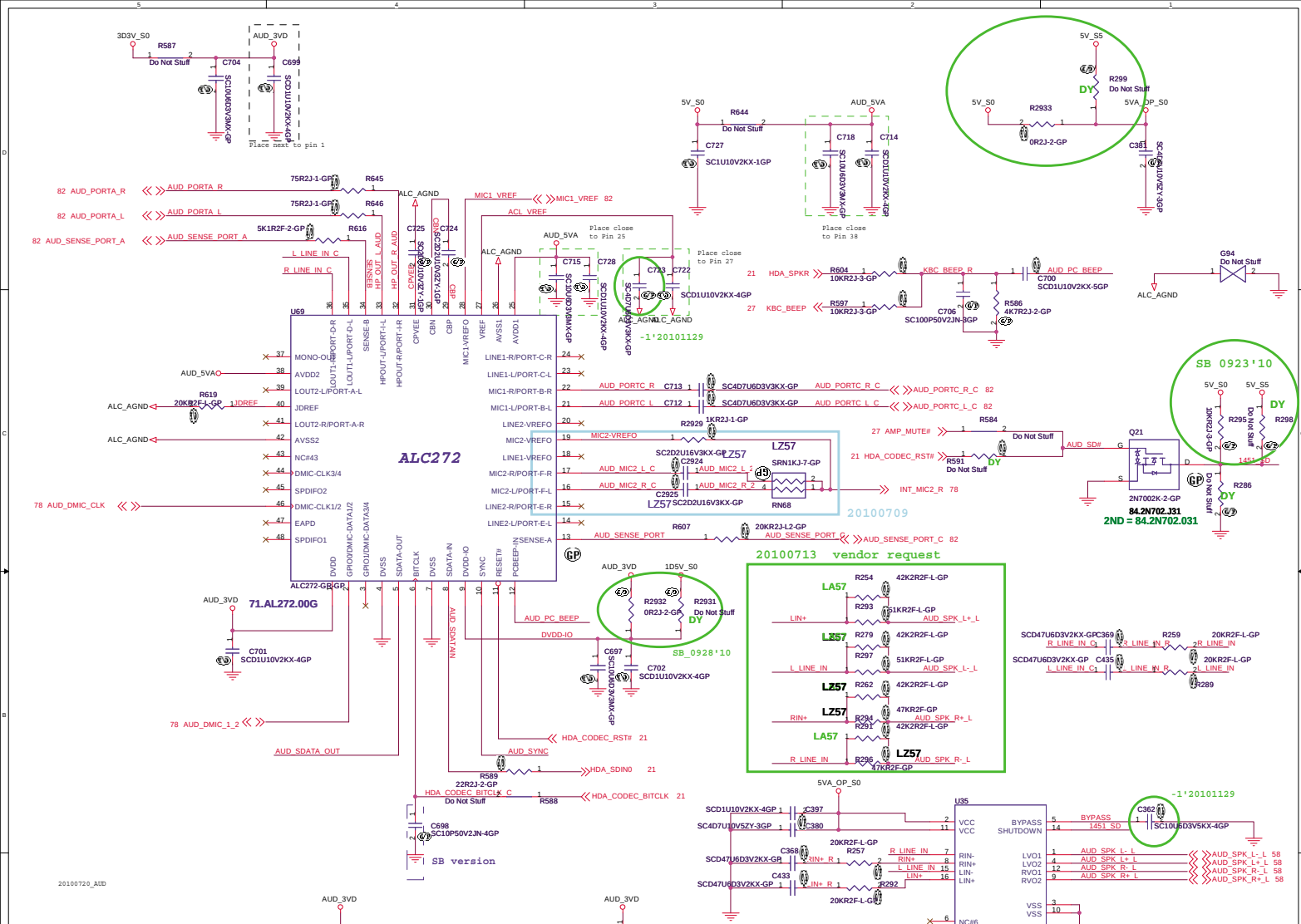
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 28 of 102


ALC272
71.AL272.00G
SB version
SB 0923'10
SB_0928'10
20100713 vendor request
20100709
-1'20101129
84.2N702.031
2ND = 84.2N702.031
Do Not Stuff
Place next to pin 1
Place close to Pin 25
Place close to Pin 27
Place close to Pin 38
AUD_PORTA_R
AUD_PORTA_L
AUD_SENSE_PORT_A
AUD_PORTC_R
AUD_PORTC_L
AUD_SENSE_PORT
AUD_DMIC_CLK
AUD_DMIC_1_2
AUD_SDATA_OUT
AUD_SYNC
AUD_PC_BEEP
HDA_CODEC_RST#
HDA_SDIN0
HDA_CODEC_BITCLK
MIC1_VREF
ACL_VREF
HDA_SPKR
KBC_BEEP
AMP_MUTE#
HDA_CODEC_RST#
INT_MIC2_R
AUD_SD#
LZ57
SRN1KJ-7-GP
RN68
20100720_AUD

blanking

BOM

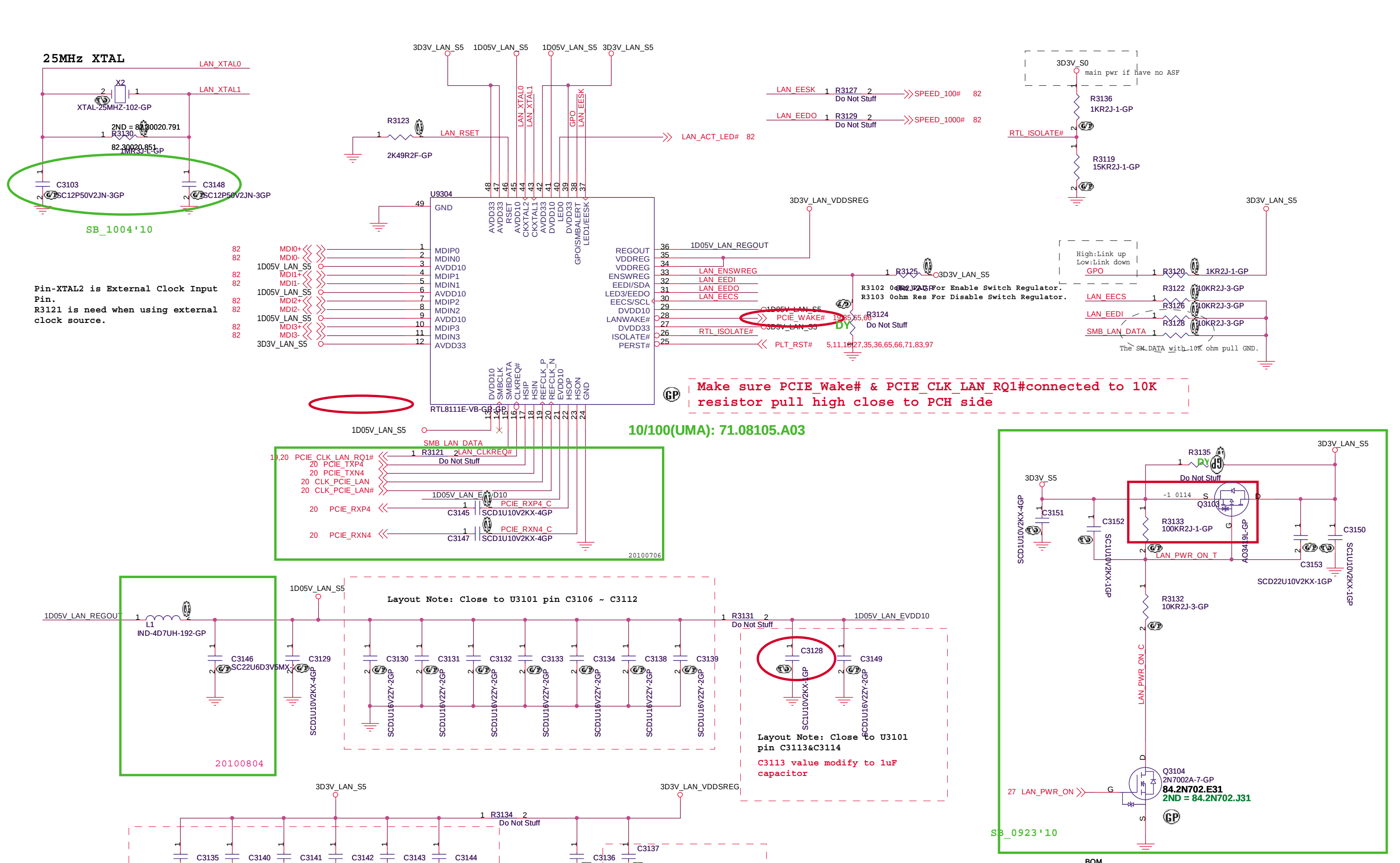
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 30 of 102



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN_RTL8111E
Size A3	Document Number: LA57 — Rev -1
Date: Tuesday, March 29, 2011	Sheet 31 of 102

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 32 of 102

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 33 of 102

(Blanking)

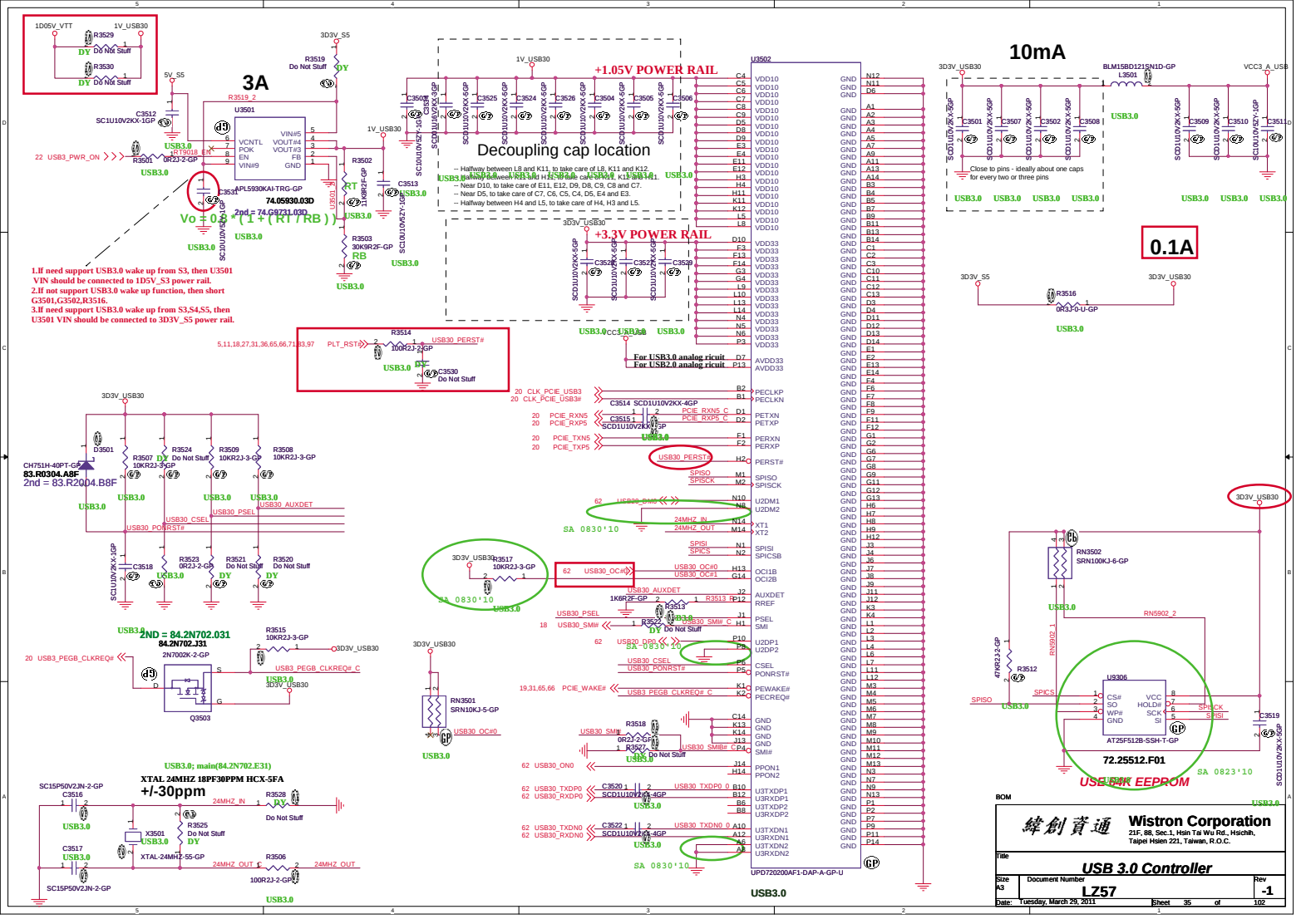
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

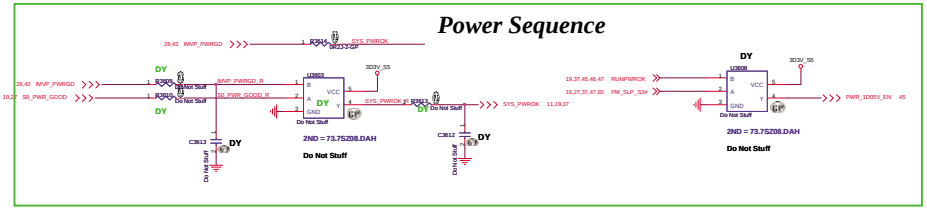
Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 34 of 102

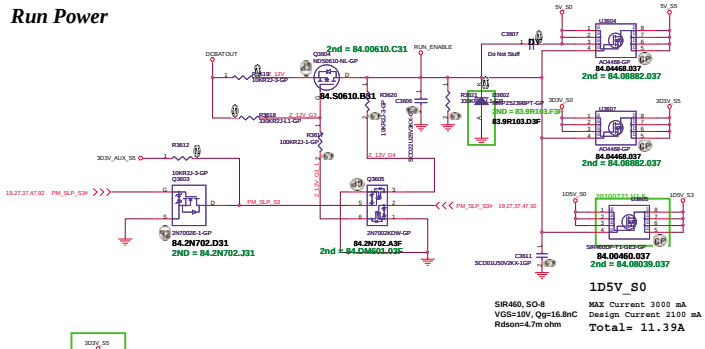

3A
10mA
0.1A
+1.05V POWER RAIL
+3.3V POWER RAIL
Decoupling cap location
-- Halfway between L8 and K11, to take care of L8, K11 and K12
-- Halfway between K11 and K12, to take care of K11, K12 and L11.
-- Near D10, to take care of E11, E12, D9, D8, C9, C8 and C7.
-- Near D5, to take care of C7, C6, C5, C4, D5, E4 and E3.
-- Halfway between H4 and L5, to take care of H4, H3 and L5.
Vo = 0.8 * (1 + (RT / RB))
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 1D5V_S3 power rail.
2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.
2nd = 74.G8731.03D
74.05930.03D
2ND = 84.2N702.031
84.2N702.J31
XTAL 24MHZ 18PF30PPM HCX-5FA
+/-30ppm
USB3.0; main(84.2N702.E31)
USB 64K EEPROM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
USB 3.0 Controller
LZ57
-1
Tuesday, March 29, 2011
35
102

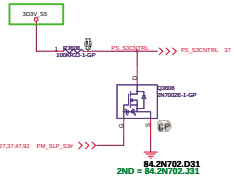
Power Sequence

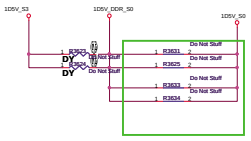


SSID = Reset.Suspend

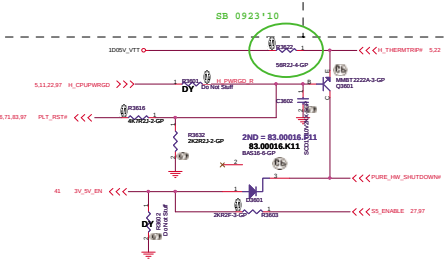
Run Power





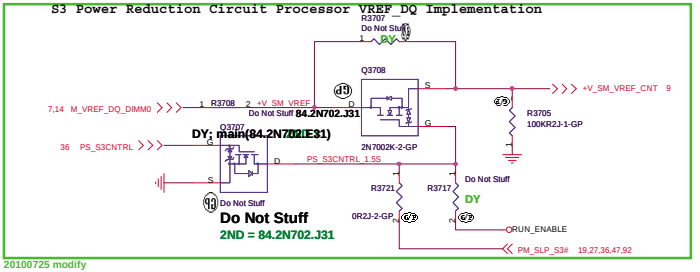


SB 0923'10



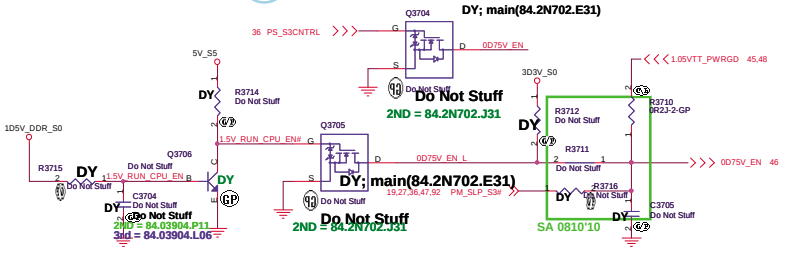
BOM			
緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	Power Plane Enable		
Size A2	Document Number LZ57		Rev -1
Date: Tuesday, March 29, 2011		Sheet 38 of 100	

Close to CPU
S3 Power Reduction Circuit Processor VREF DQ Implementation

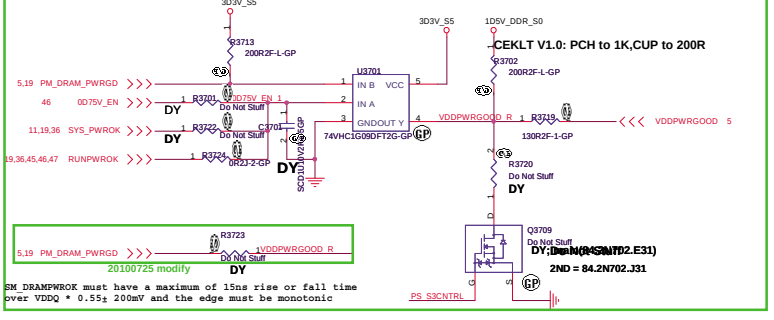


20100725 modify

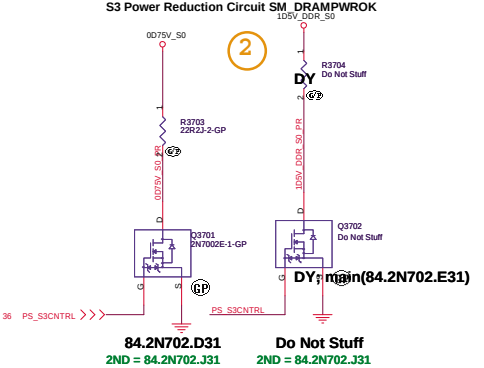
5 S3 Power Reduction X01 20091111



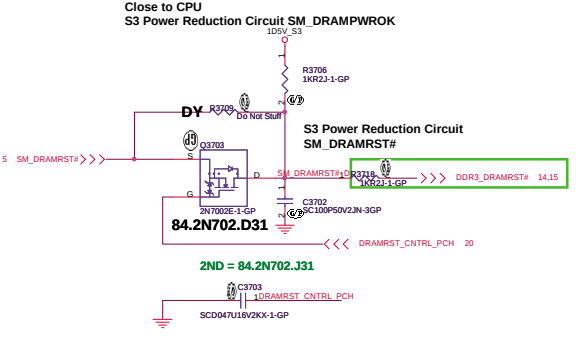
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



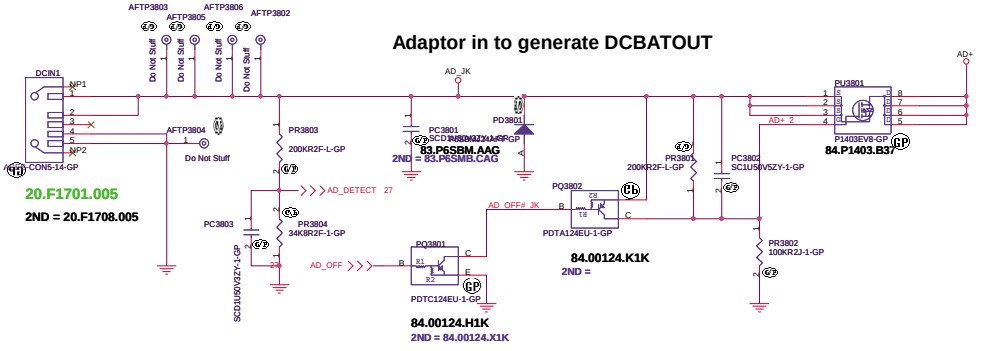
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

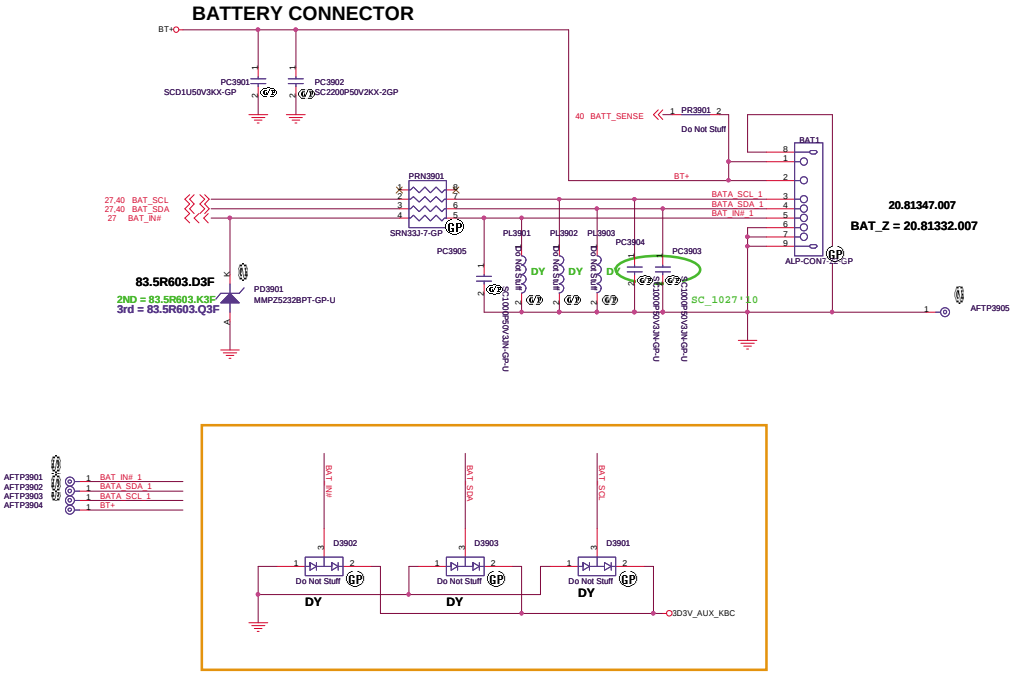
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 37 of 102



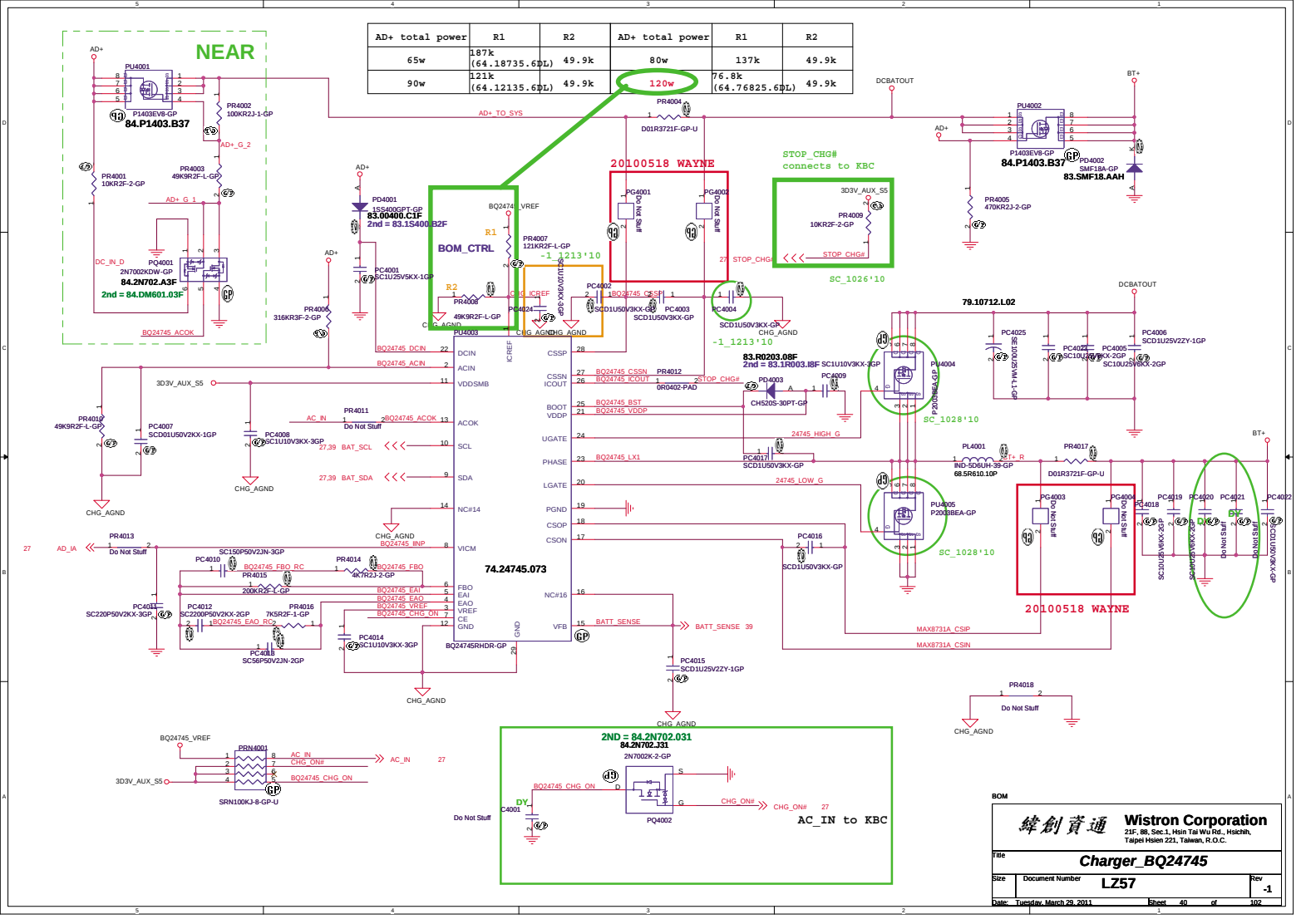
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN_JACK		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 38 of 102	



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BATT_CONN***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 39 of 102	

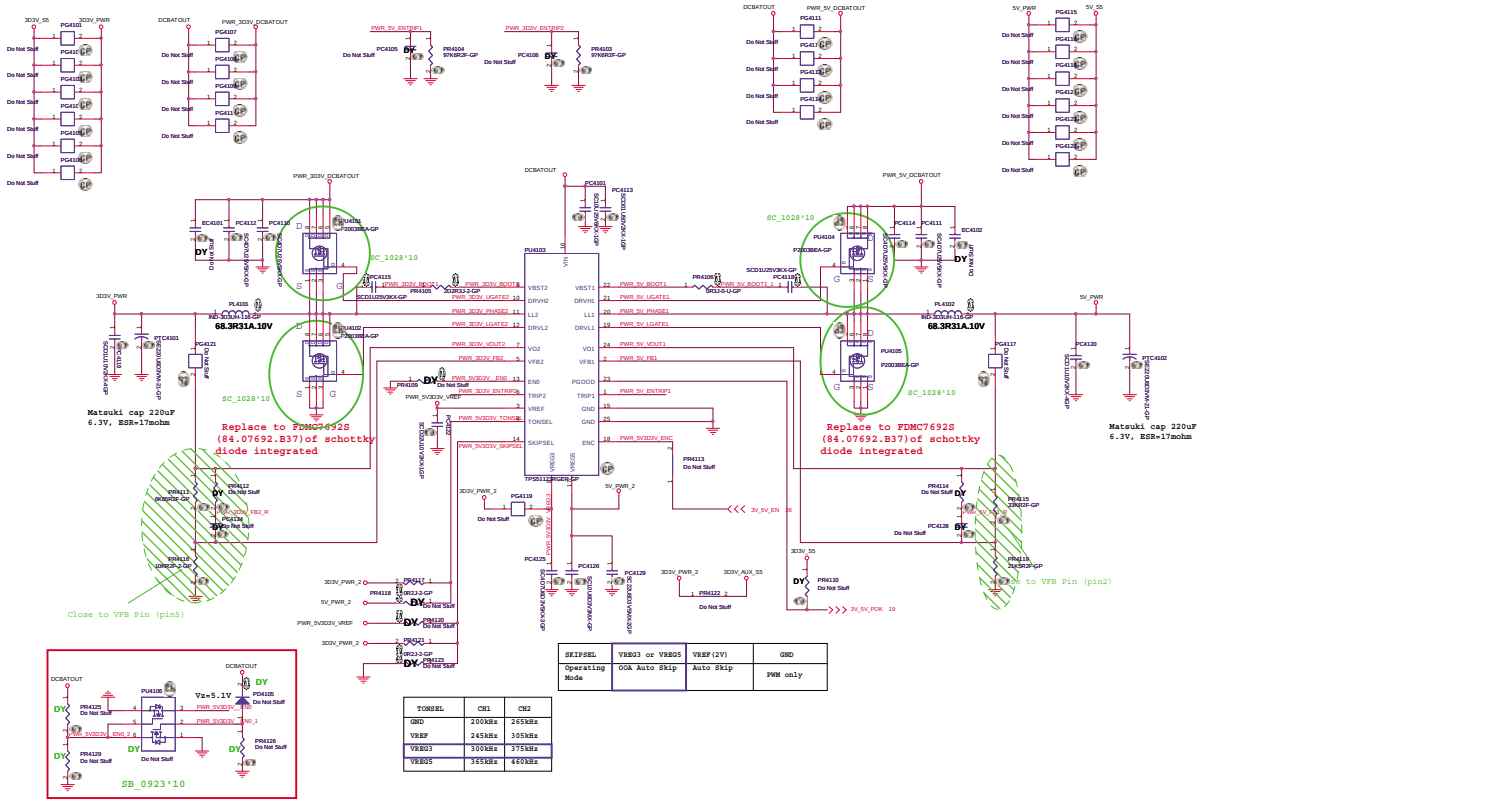


AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k	120w	76.8k (64.76825.6DL)	49.9k

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Charger_BQ24745	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 40 of 102	

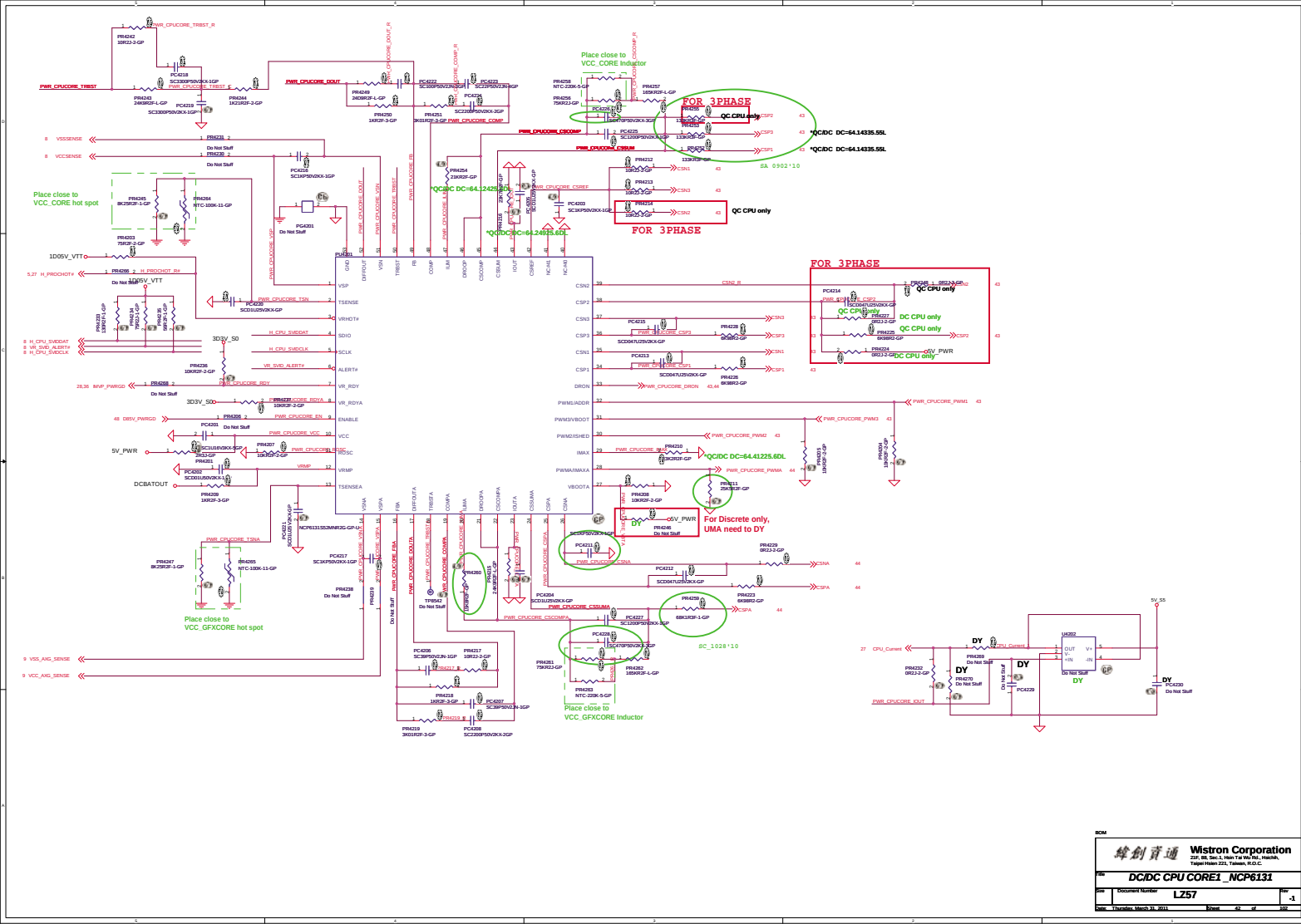
SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

BOM	
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC/DC 3D3V5V
Size	Document Number: LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 41 of 100


Place close to VCC_CORE Inductor
FOR 3PHASE
QC CPU only
*QC/DC DC=64.14335.55L
*QC/DC DC=64.14335.55L
SA 0902'10
Place close to VCC_CORE hot spot
*QC/DC DC=64.12425.2DL
FOR 3PHASE
QC CPU only
*QC/DC DC=64.12425.6DL
FOR 3PHASE
QC CPU only
QC CPU only
DC CPU only
QC CPU only
DC CPU only
5V_PWR
*QC/DC DC=64.41225.6DL
For Discrete only, UMA need to DY
DY
Place close to VCC_GFXCORE hot spot
SC_1028'10
Place close to VCC_GFXCORE Inductor
DY
DY
DY
DY
DY
DY
Wistron Corporation
2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DC/DC CPU CORE1_NCP6131
LZ57
-1
Thursday, March 31, 2011
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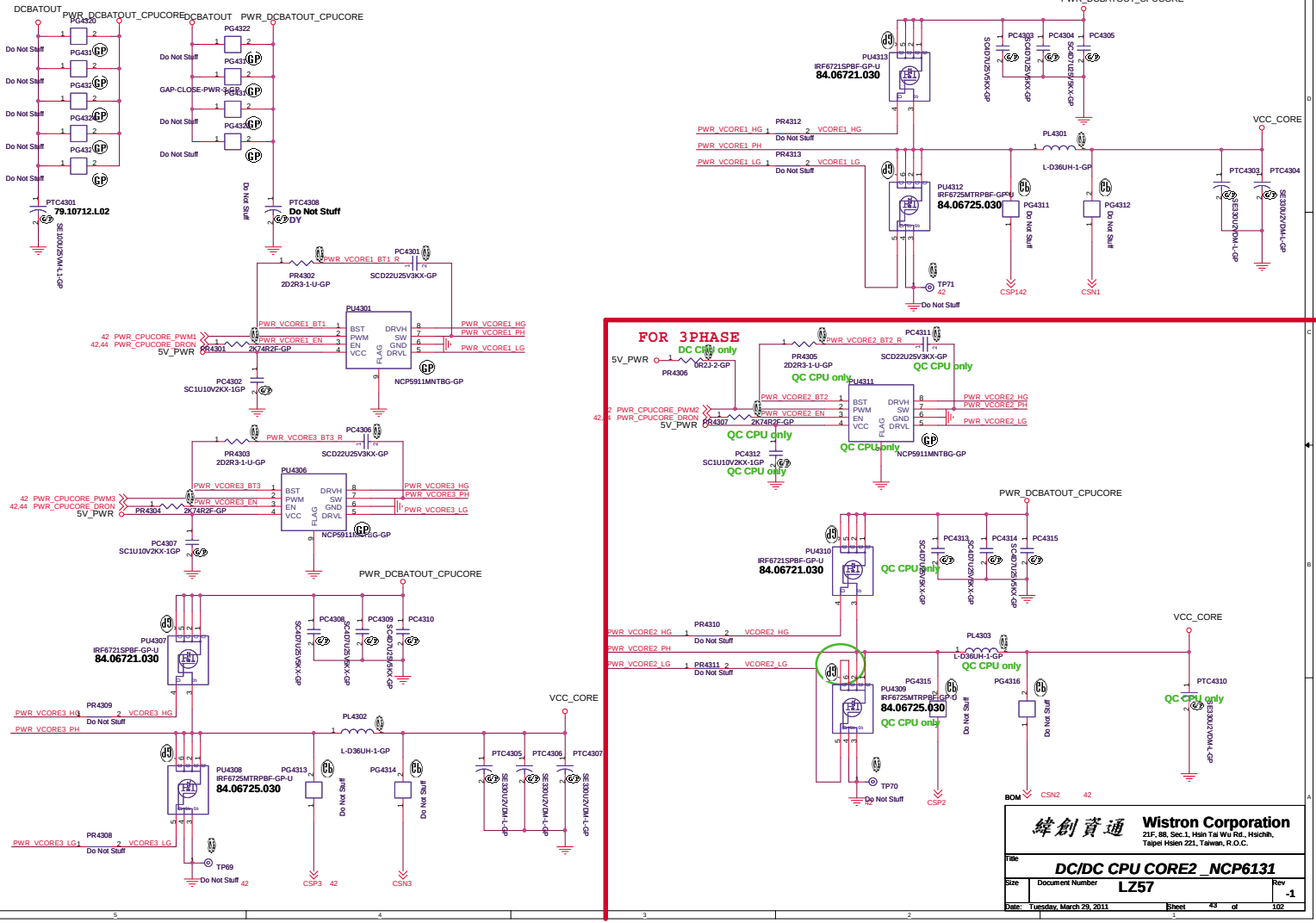
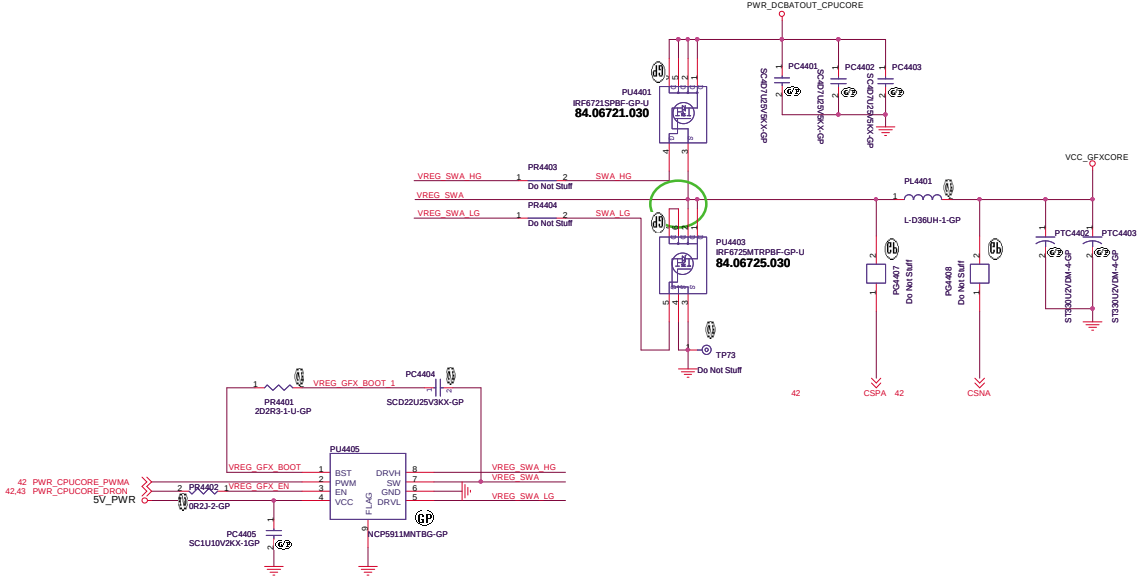
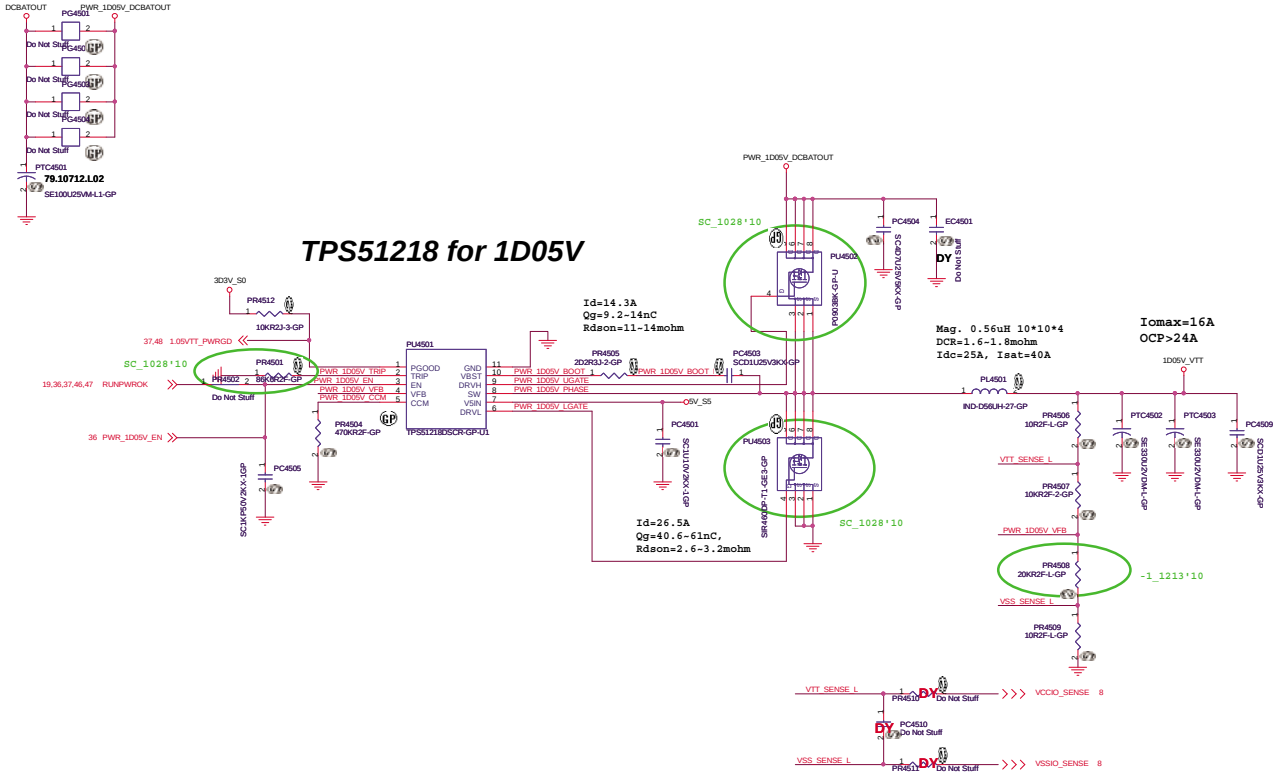

FOR 3PHASE
DC CPU only
QC CPU only
PWR_DCBATOUT_CPUCORE
VCC_CORE
84.06721.030
84.06725.030
79.10712.L02
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC/DC CPU CORE2 _NCP6131
LZ57
Tuesday, March 29, 2011
43 of 102



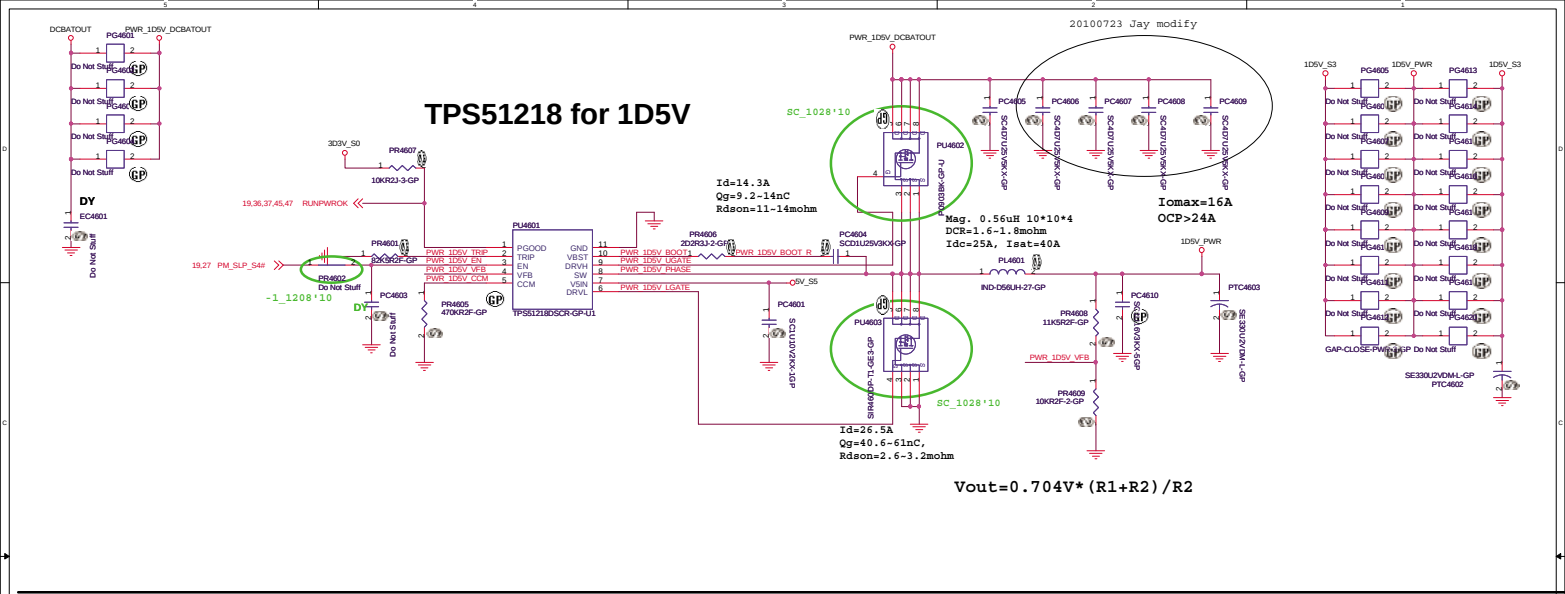
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 44 of 102	



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPS51218_1D05V***	
Size	Document Number	Rev -1
Date: Tuesday, March 29, 2011	Sheet 45 of 102	



BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

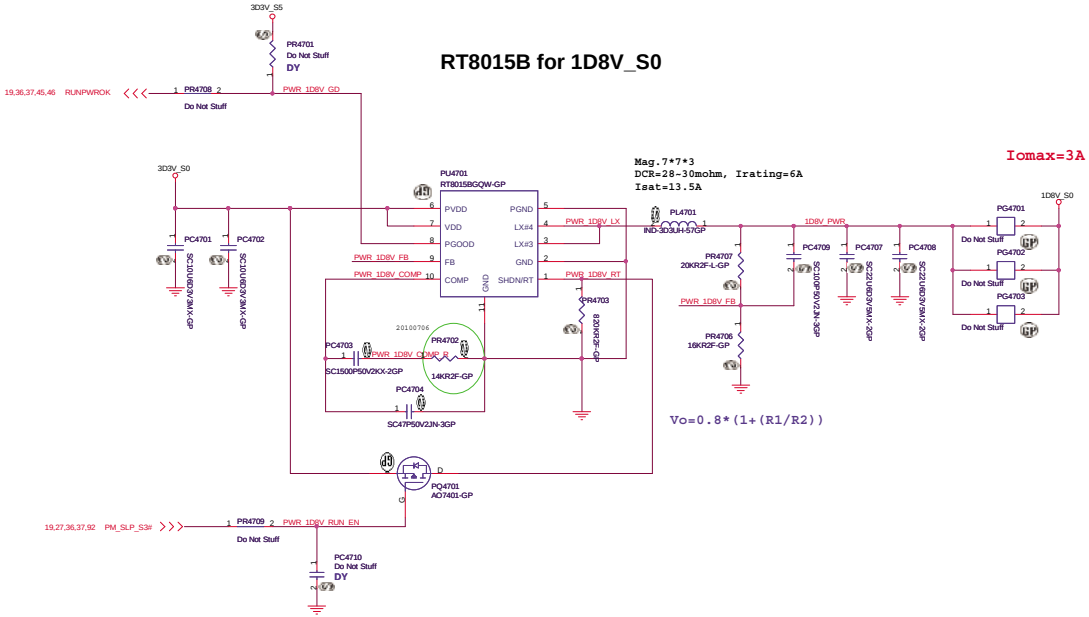
Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size	Document Number	Rev
		-1

Date: Tuesday, March 29, 2011 Sheet 46 of 102

RT9025 for 1D8V_S0

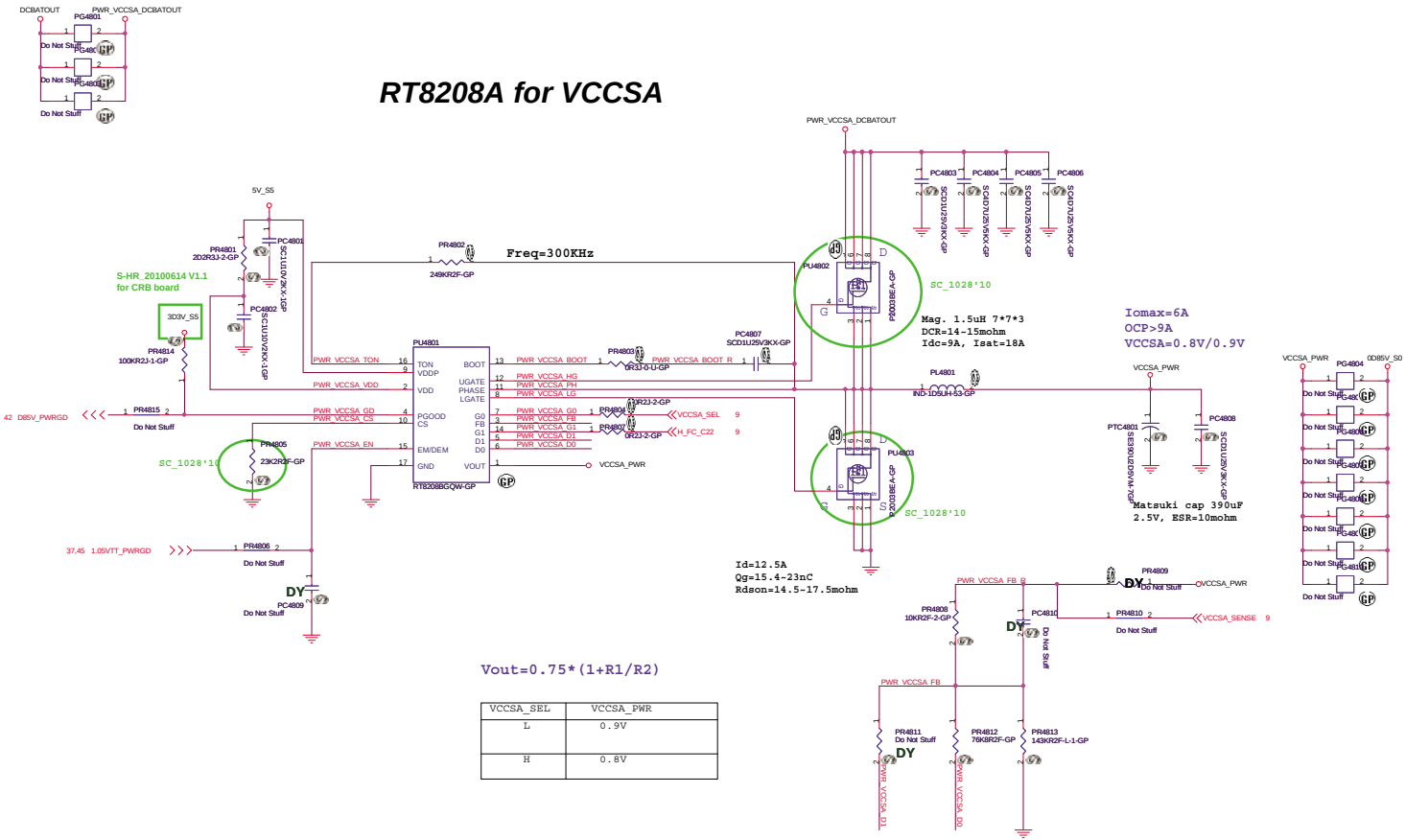
RT8015B for 1D8V_S0



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *1D8V_RT9025*		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 47 of 102	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

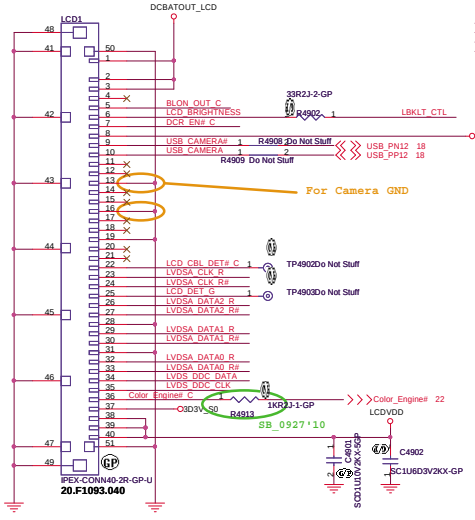
BOM

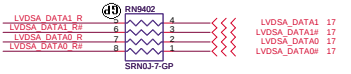
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

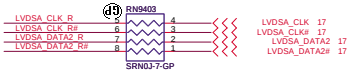
Title	RT8208B_VCCSA	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 48 of 102	

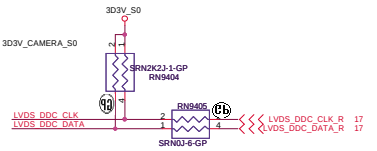
SSID = VIDEO

LVDS CONNECTOR

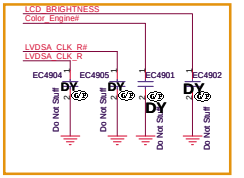


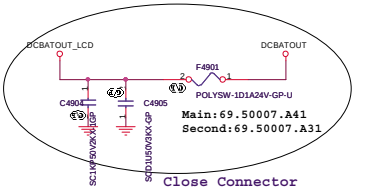


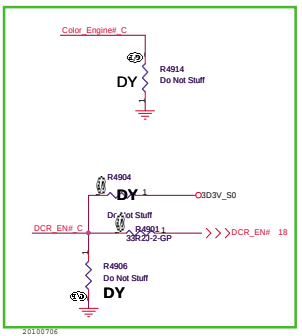




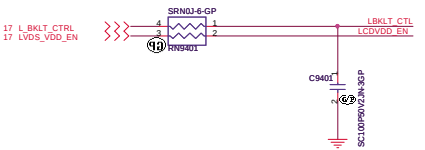
For EMI request
Close to LVDS connector



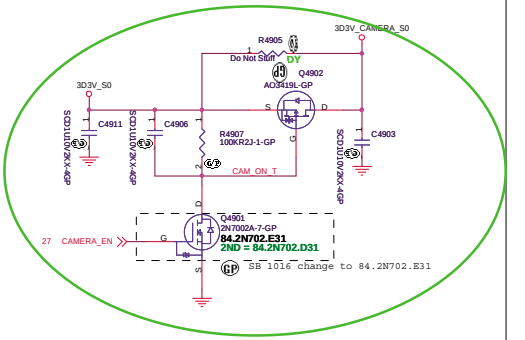




Panel BL brightness/Power En/BL En

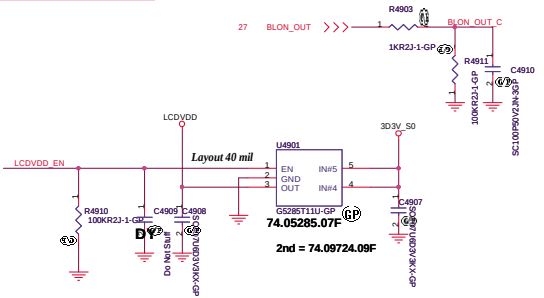


CAMERA POWER



SB 0923'10

SSID = VIDEO



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Connector**

Size	Document Number	Rev
A3	LZ57	-1

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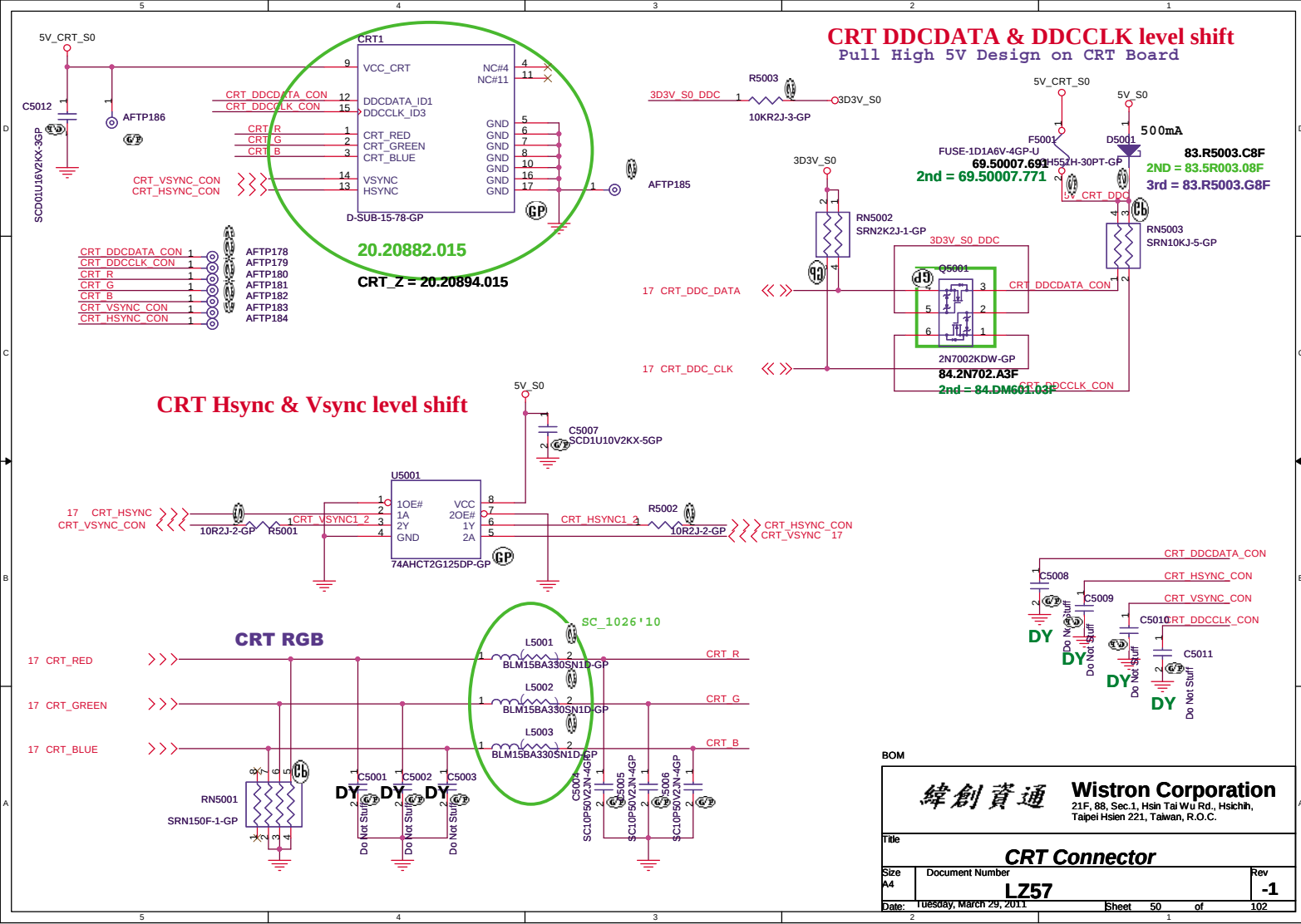
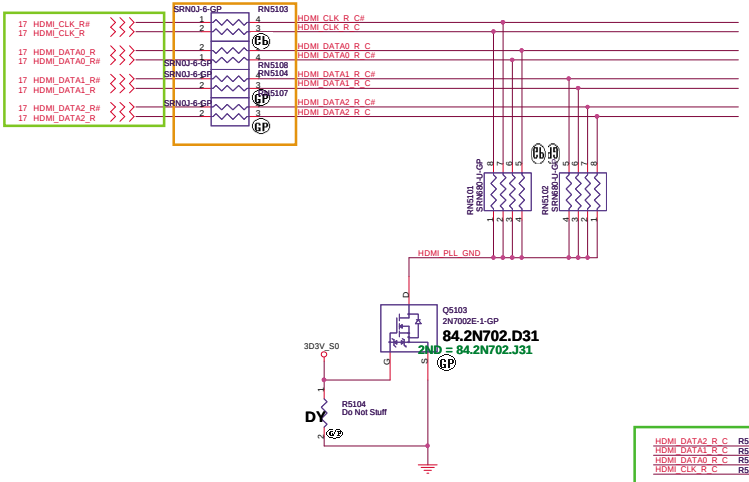

CRT DDCDATA & DDCCLK level shift
Pull High 5V Design on CRT Board
CRT Hsync & Vsync level shift
CRT RGB
5V_CRT_S0
CRT1
VCC_CRT
NC#4
NC#11
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
GND
D-SUB-15-78-GP
AFTP185
AFTP186
C5012
SCD01U16V2KX-3GP
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
CRT_VSYNC_CON
CRT_HSYNC_CON
AFTP178
AFTP179
AFTP180
AFTP181
AFTP182
AFTP183
AFTP184
20.20882.015
CRT_Z = 20.20894.015
3D3V_S0_DDC
3D3V_S0
R5003
10KR2J-3-GP
5V_S0
500mA
F5001
D5001
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
83.R5003.C8F
2ND = 83.5R003.08F
3rd = 83.R5003.G8F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-5-GP
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
17 CRT_DDC_DATA
17 CRT_DDC_CLK
U5001
74AHCT2G125DP-GP
C5007
SCD1U10V2KX-5GP
17 CRT_HSYNC
17 CRT_VSYNC
R5001
R5002
10R2J-2-GP
CRT_HSYNC_CON
CRT_VSYNC_CON
SC_1026'10
L5001
L5002
L5003
BLM15BA330SN1D-GP
17 CRT_RED
17 CRT_GREEN
17 CRT_BLUE
RN5001
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
SC10P50V2JN-4GP
DY
Do Not Stuff
C5008
C5009
C5010
C5011
BOM
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
A4
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 50 of 102

SSID = VIDEO

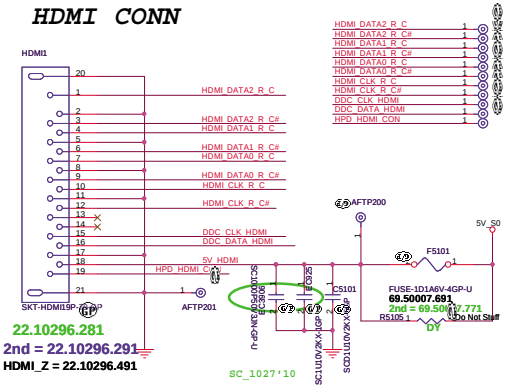
HDMI CONNECTOR

HDMI Passive Level Shifter

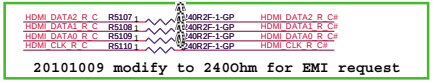
Close to HDMI Connector

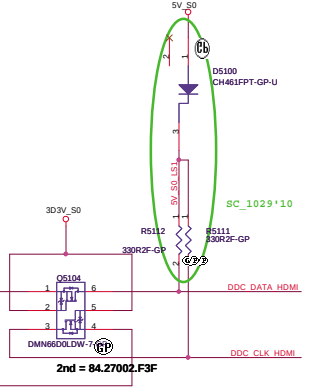


HDMI CONN

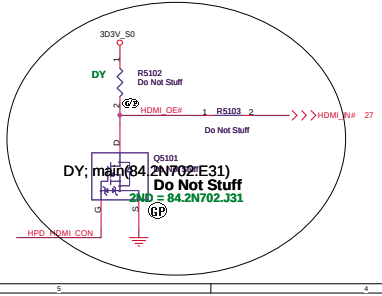


HDMI DDC Passive Level Shifter

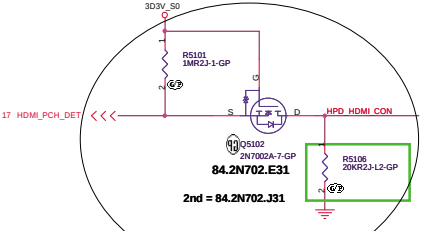




20100727 modify, KBC isn't use.



20100727 follow intel design guide



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 51 of 102

(Blanking)

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 53 of 102

(Blanking)

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

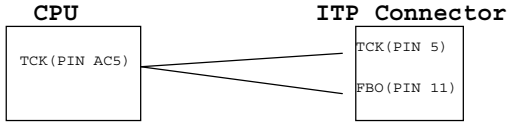
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



BOM

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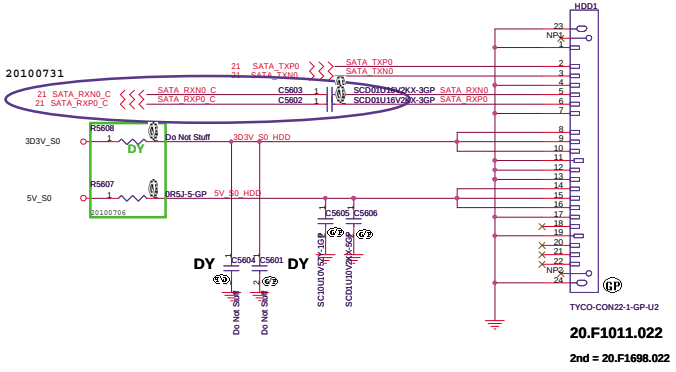
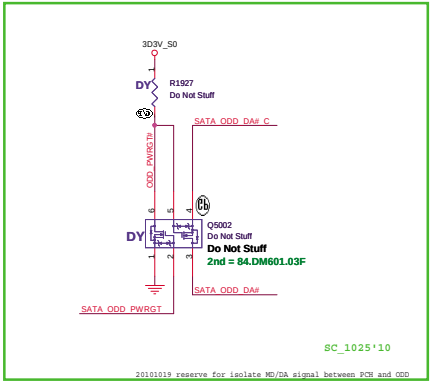
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

SSID = SATA

SATA HDD Connector

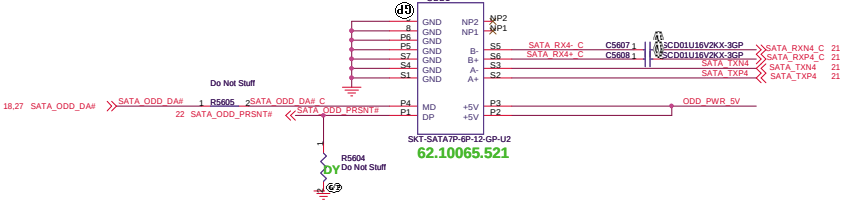


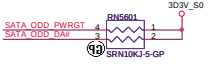


ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

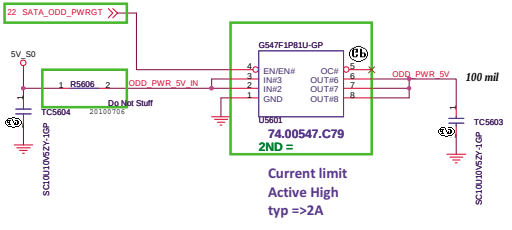
Mars:
Exchange ODD and ESATA differential pair each other.





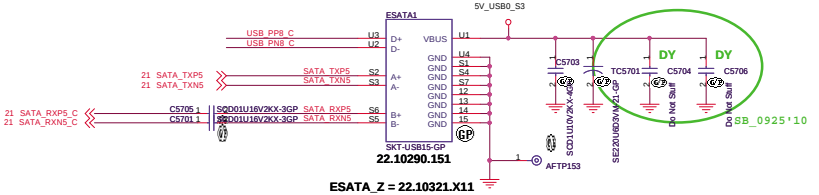
SUPPORT ZERO SATA ODD

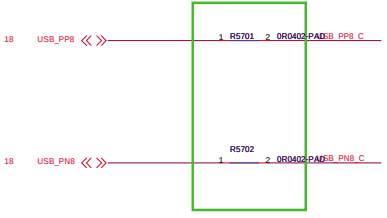
SATA Zero Power ODD

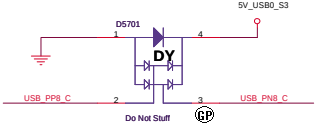


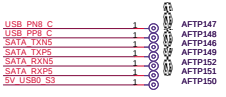
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	





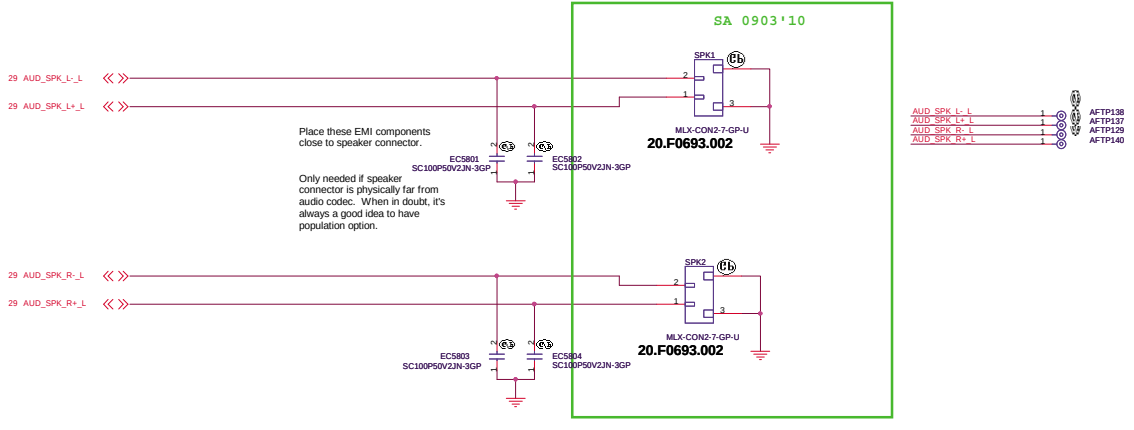




BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**E-SATA/LUSB**	
Size: A3	Document Number: **LZ57**	Rev: **-1**
Date: Tuesday, March 29, 2011	Sheet 57 of 102	

INTERNAL STEREO SPEAKERS



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MIC/SPEAKER/AUDIO JACK***	
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 58 of 102	

Reserved

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	LZ57	-1

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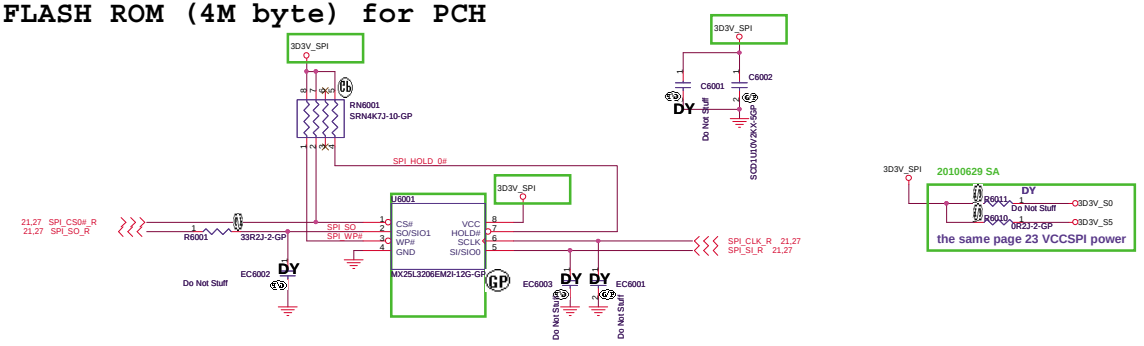
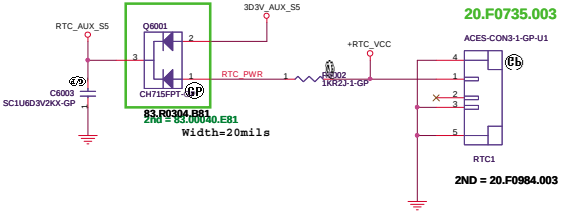
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT

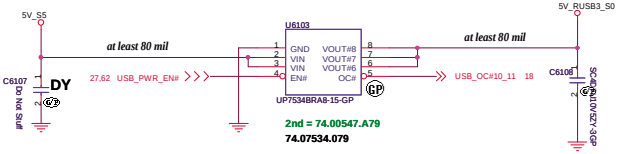


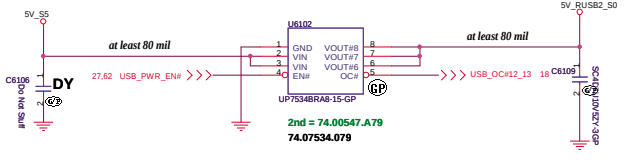
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 60 of 102	

SSID = USB

RJ45_USB Board USB Power



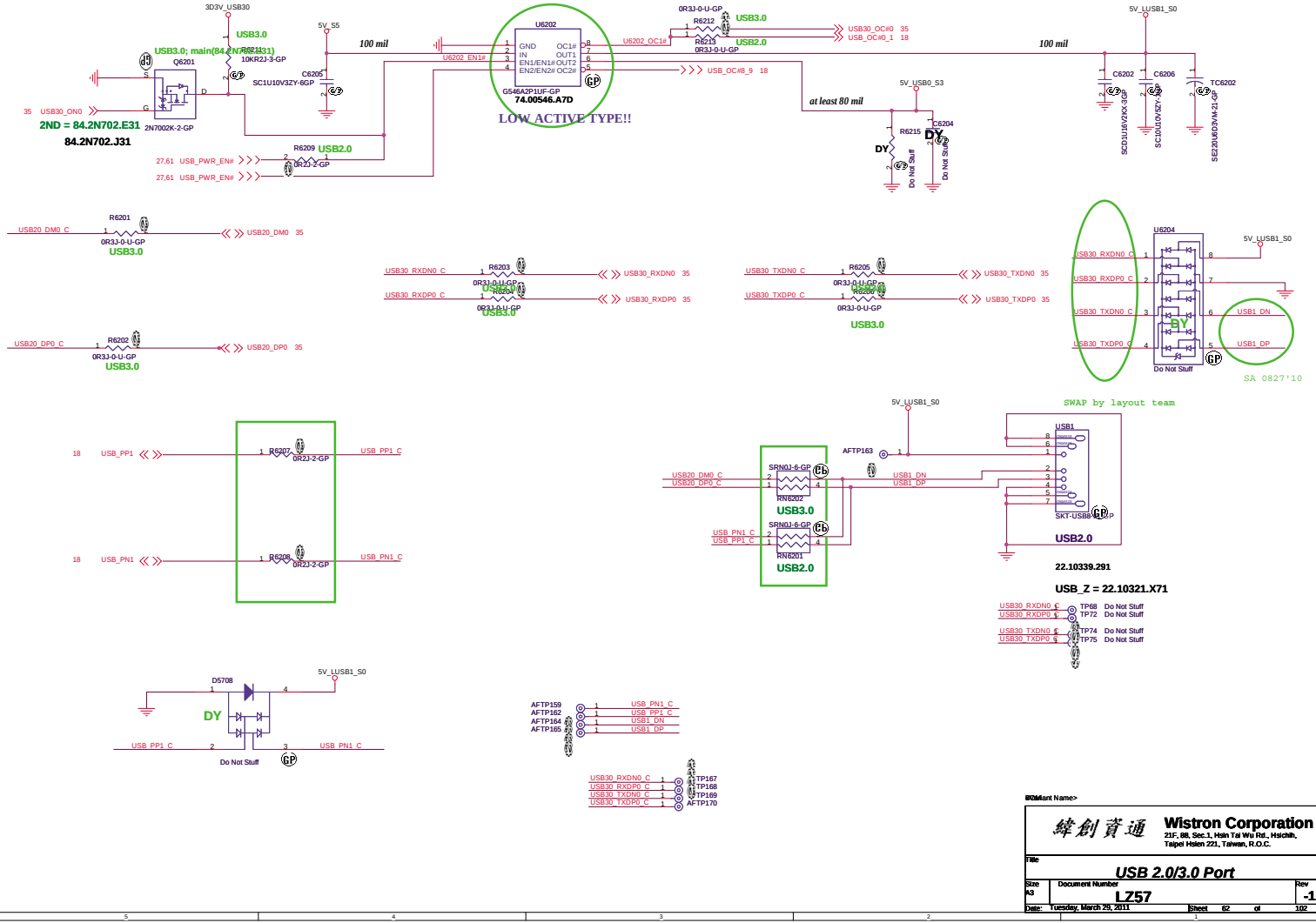


I/O Board USB Power

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB Power SW***
Size: A3	Document Number: LZ57 — Rev: -1
Date: Tuesday, March 29, 2011	Sheet 61 of 102

Left Side USB Power Switch



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 2.0/3.0 Port**

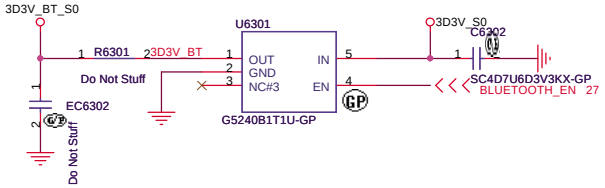
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 62 of 102

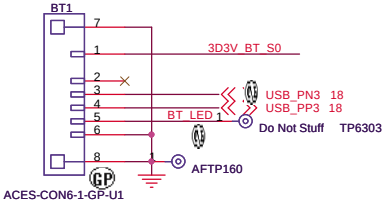
SSID = User.Interface

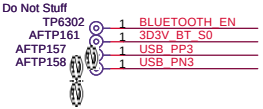
Bluetooth Module conn.

Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



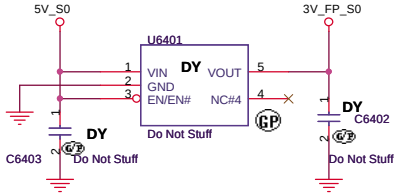


20.F0772.006

2ND = 20.F1804.006

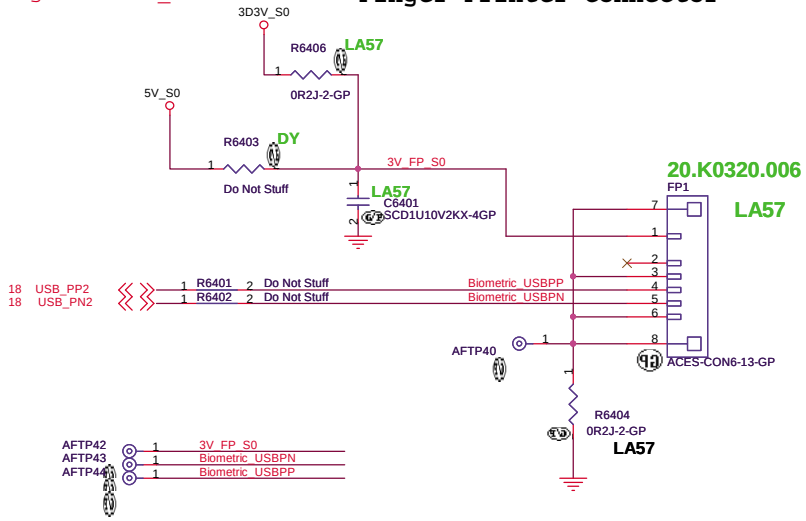
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Bluetooth		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 63 of 102	



LA47 change to 3D3V_S0

Finger Printer Connector



BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

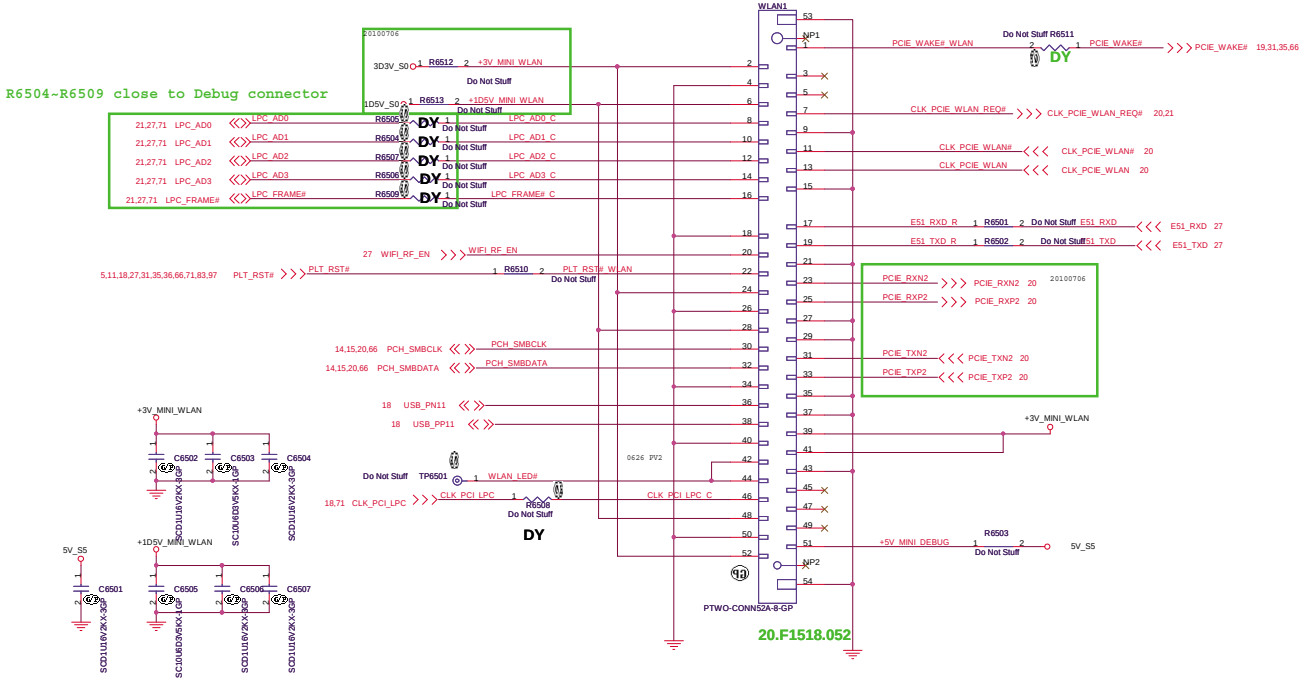
Title: ***RESERVED***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 64 of 102

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

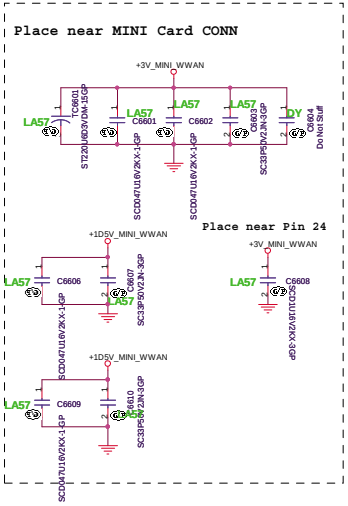


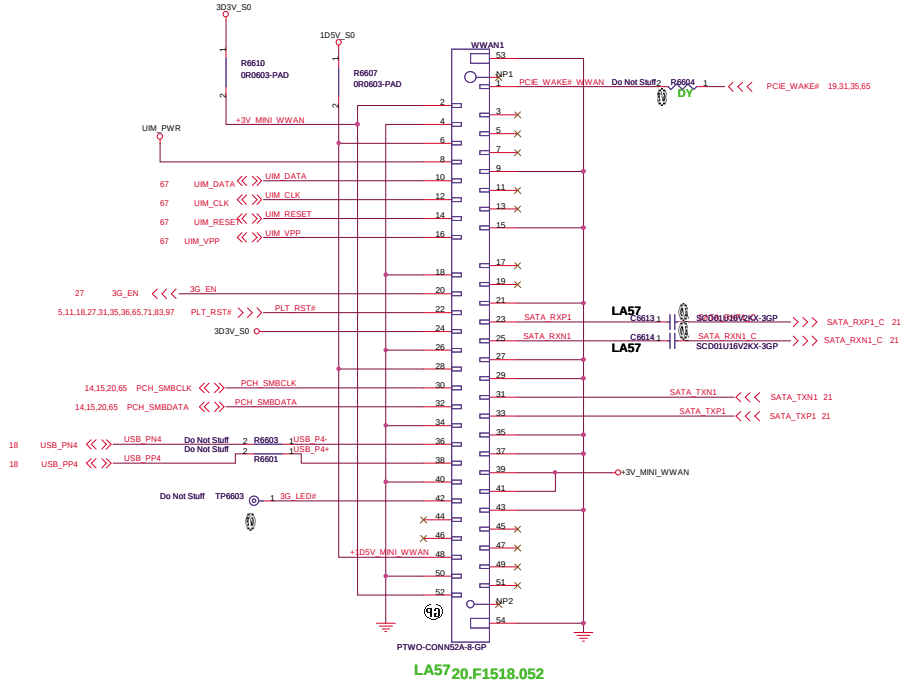
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINICARD(WLAN)/ITP CONN	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 65 of 102	

SSID = Wireless

Mini Card Connector(WWAN)





LA57 20.F1518.052

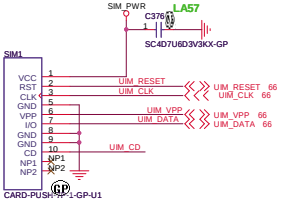
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

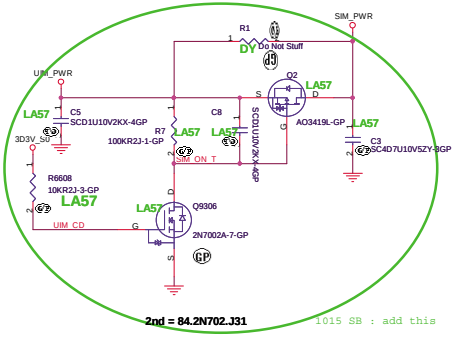
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 66 of 102



LA57

20.I0073.001



2nd = 84.2N702.J31

1015 SB : add this

84.2N702.E31

BOM

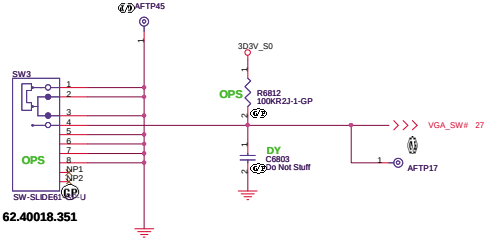
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SIM CARD***

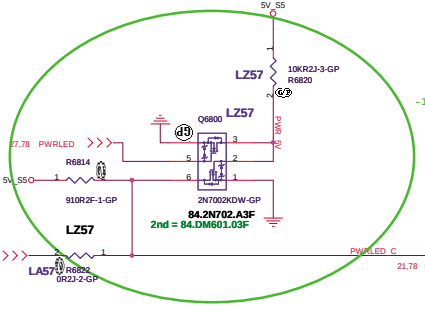
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 67 of 102

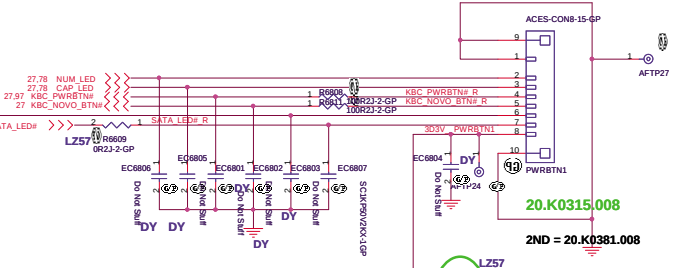
SSID = User.Interface

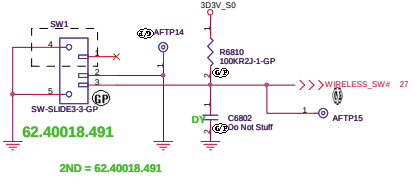


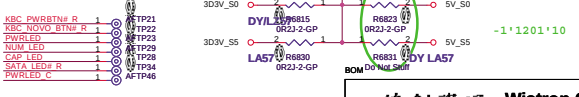
Power button LED(White)



-1_1209'10





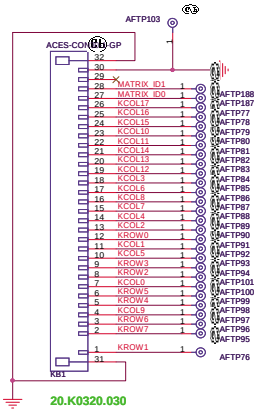


-1'1201'10

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 68 of 102	

SSID = KBC

Internal KeyBoard Connector

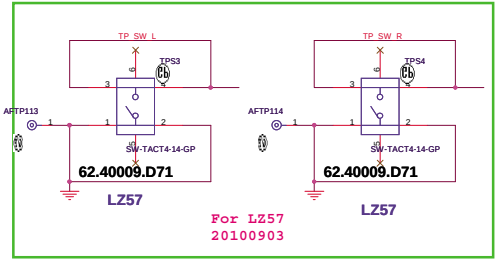


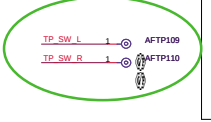
20.K0320.030

ID KEY MATRIX	SENSE			
	27	28	29	30
	IDO	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

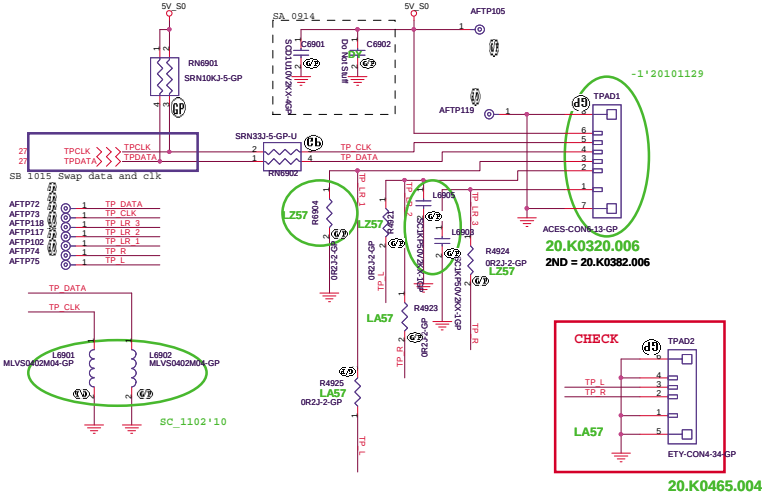
KROW[0..7] 27

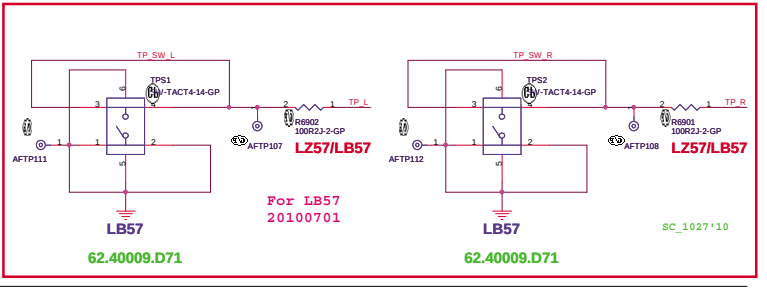
KCOL[0..17] 27





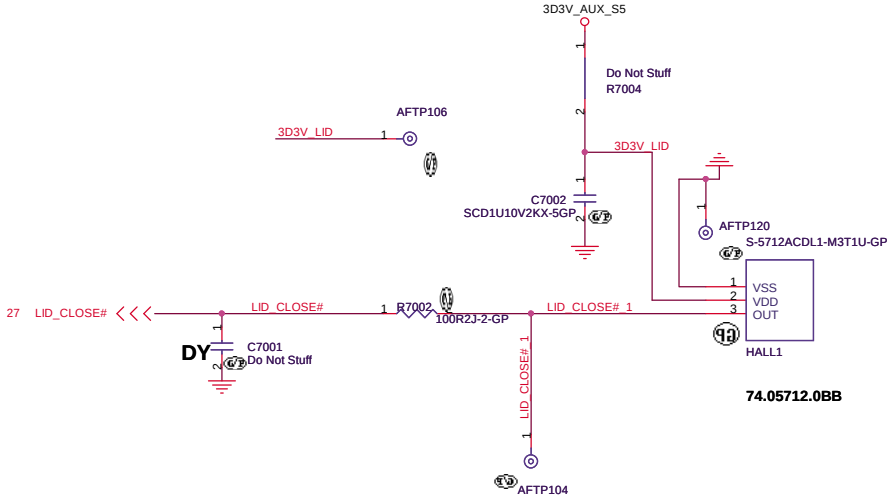
SSID = Touch.Pad





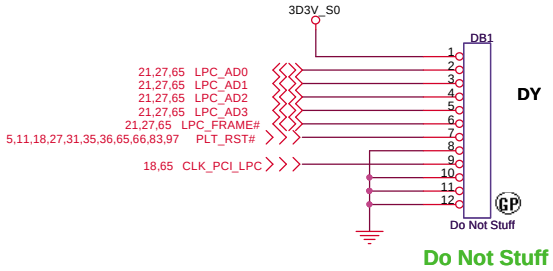
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Key Board/Touch Pad**	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 69 of 102	



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Hall Sensor*		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 70 of 102	



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 71 of 102

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BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 72 of 102

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BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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Date: Tuesday, March 29, 2011 Sheet 73 of 102

BOM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 74 of 102

BOM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

New Card

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 75 of 102

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BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 76 of 102

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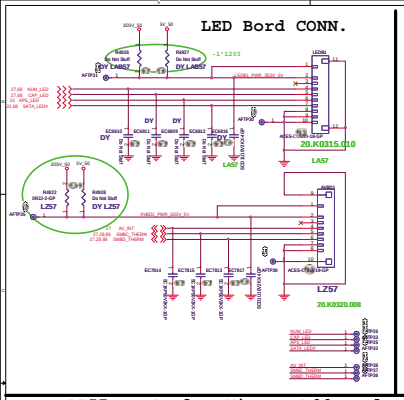
BOM

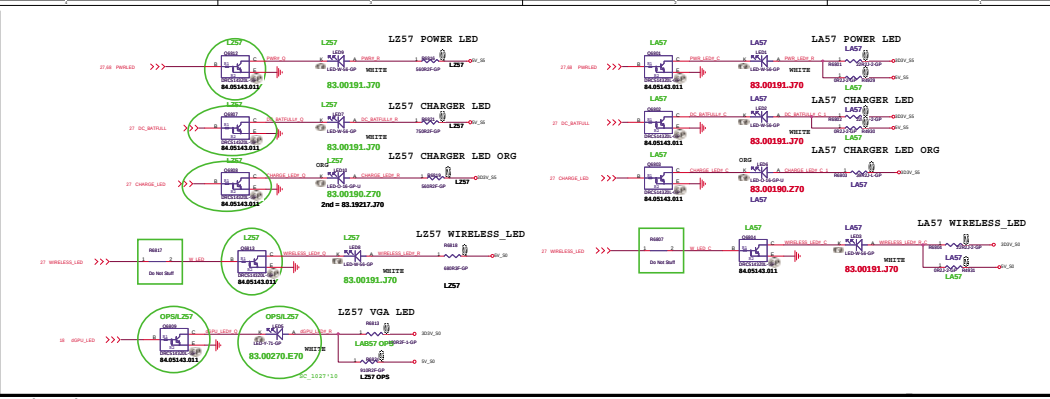
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

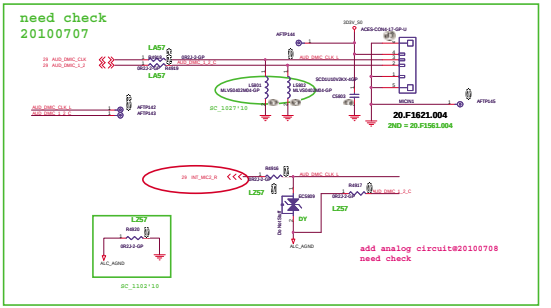
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 77 of 102

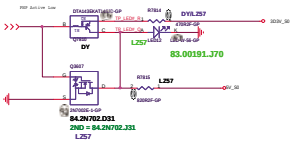




LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic



LZ57 Touch Pad LED



Wistron Corporation
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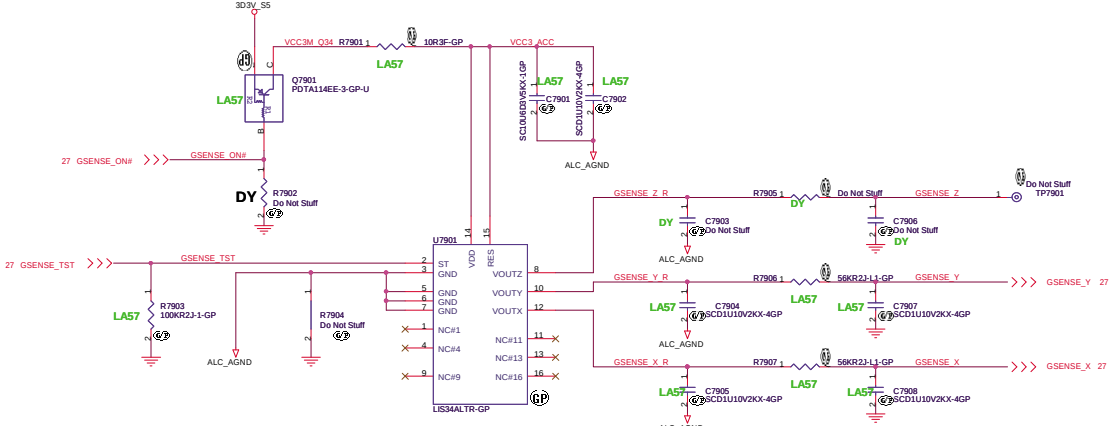
LEDB/LED

LZ57

-1

G-Sensor



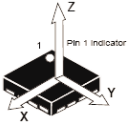
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 79 of 102

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BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

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BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

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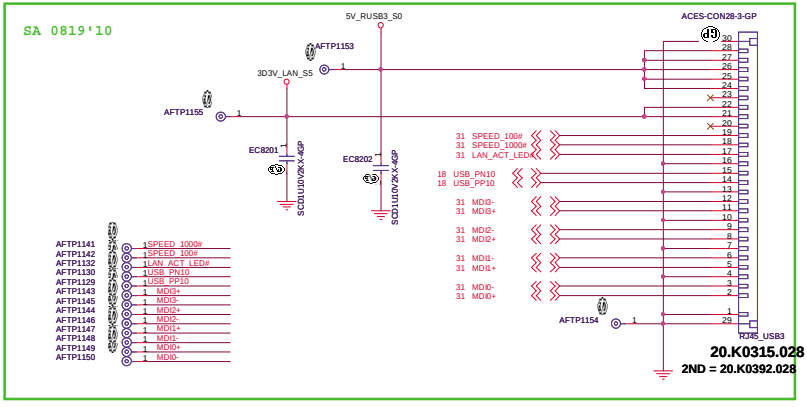
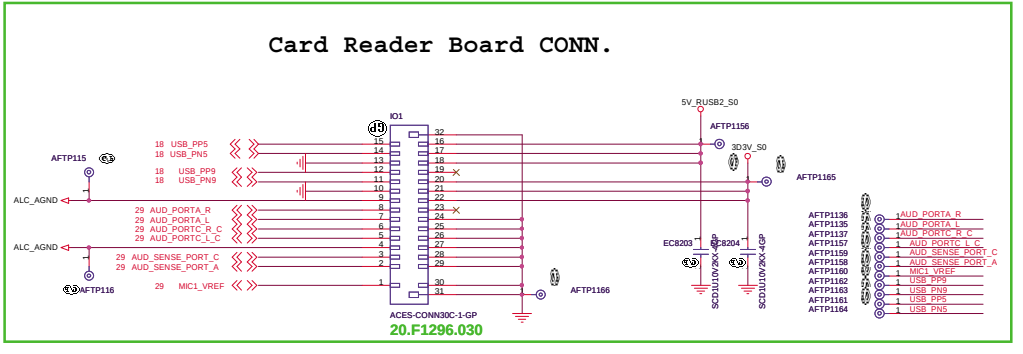
RJ45_USB CONN.



Card Reader Board CONN.



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	LZ57	-1

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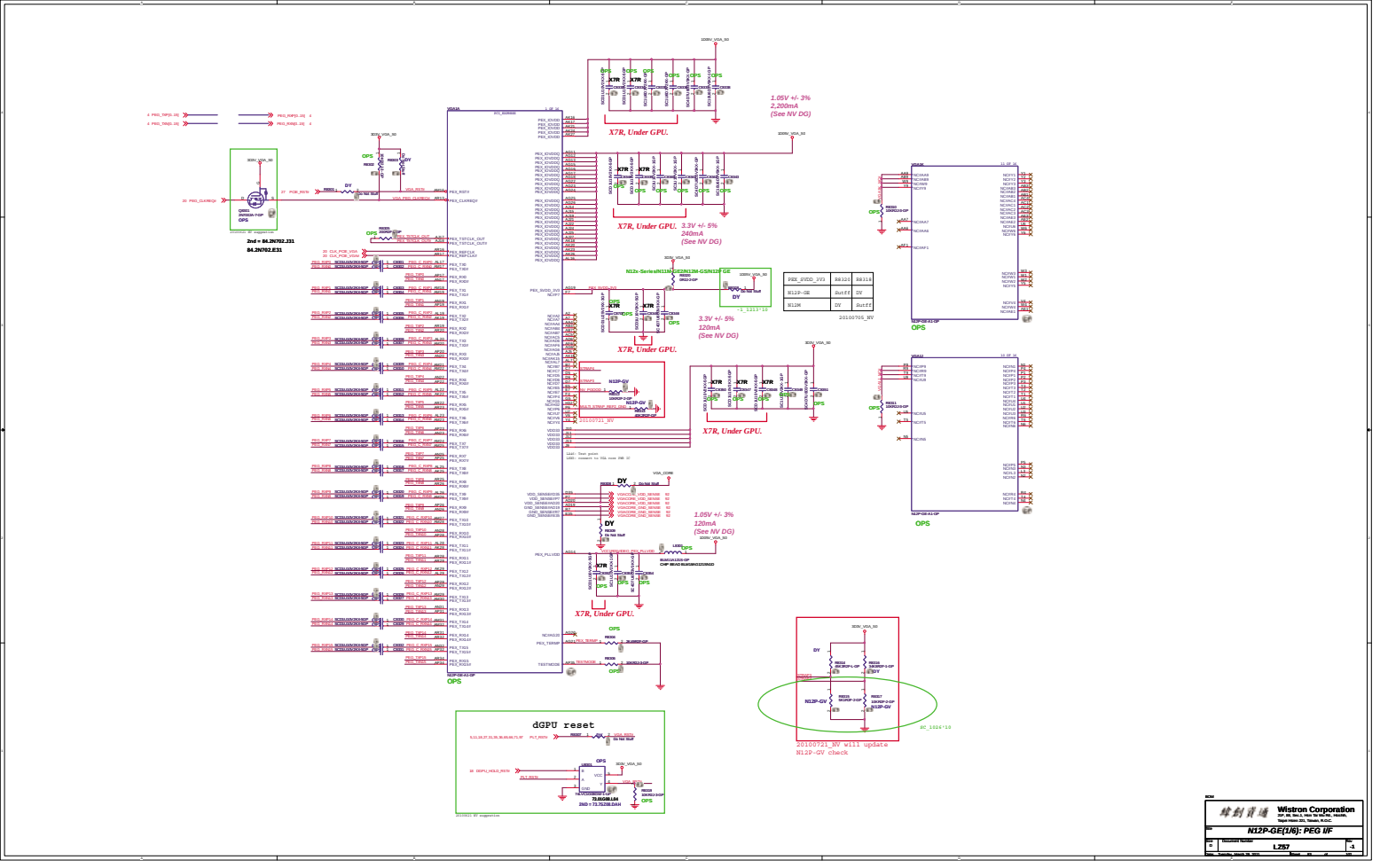
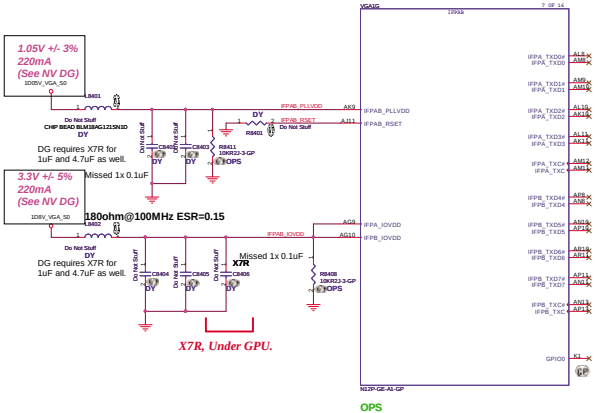


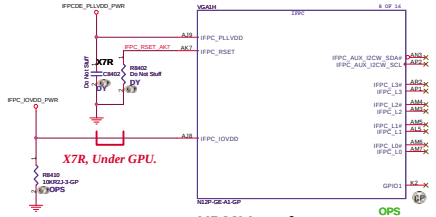
PEX_EVDD_1V0	R8325	88316
N12P-GE	Suff	DY
N12M	DY	Suff

20100706_NV

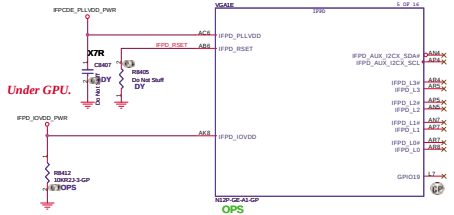
ROM					
緯創資通	Wistron Corporation				
	21F, 88, Sec.1, Xintai 5th Rd, Xizhi, Taipei Hsien 221, Taiwan, R.O.C.				
Title	N12P-GE(1/6): PEG I/F				
Size	Document Number			Rev	
D		LZ57		-3	
Date: Tuesday, March 30, 2010			Sheet 23 of 46		

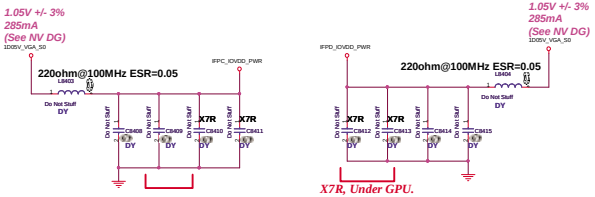
LVDS Interface

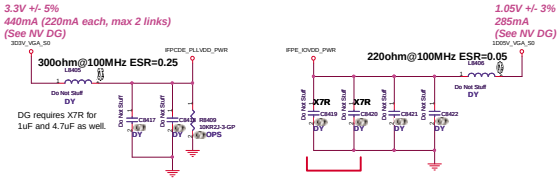


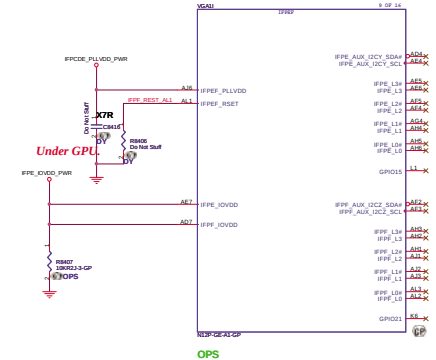


HDMI Interface



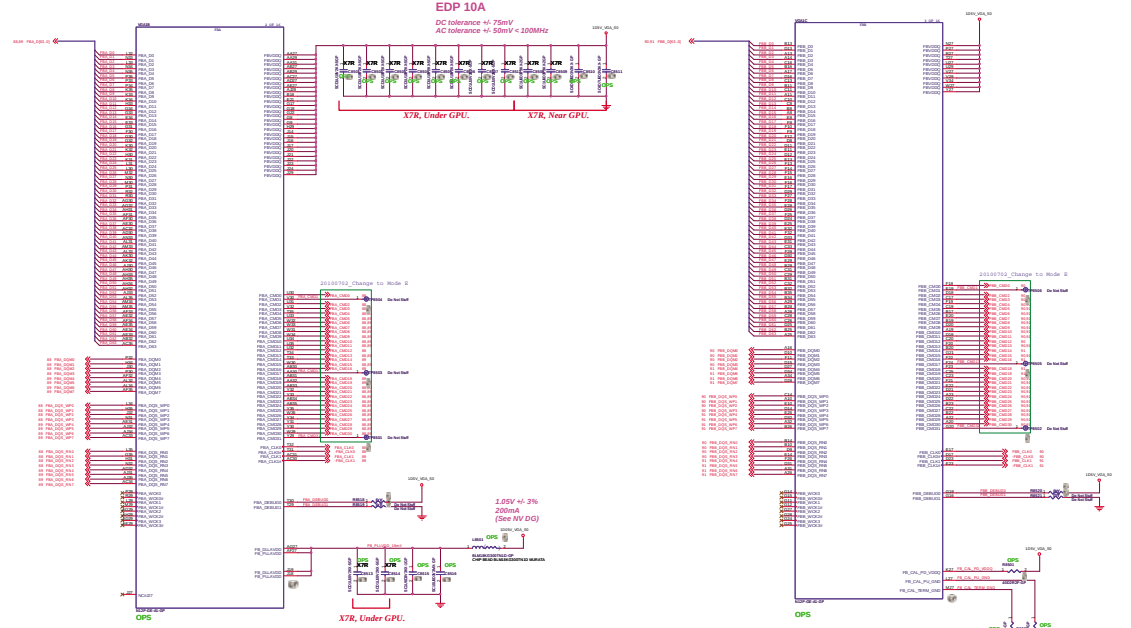


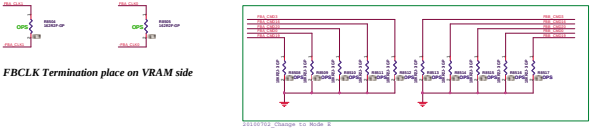




BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: N12P-Q1/Q3 (2/6): DIGITAL OUT		
Size: A2	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 84 of 102	

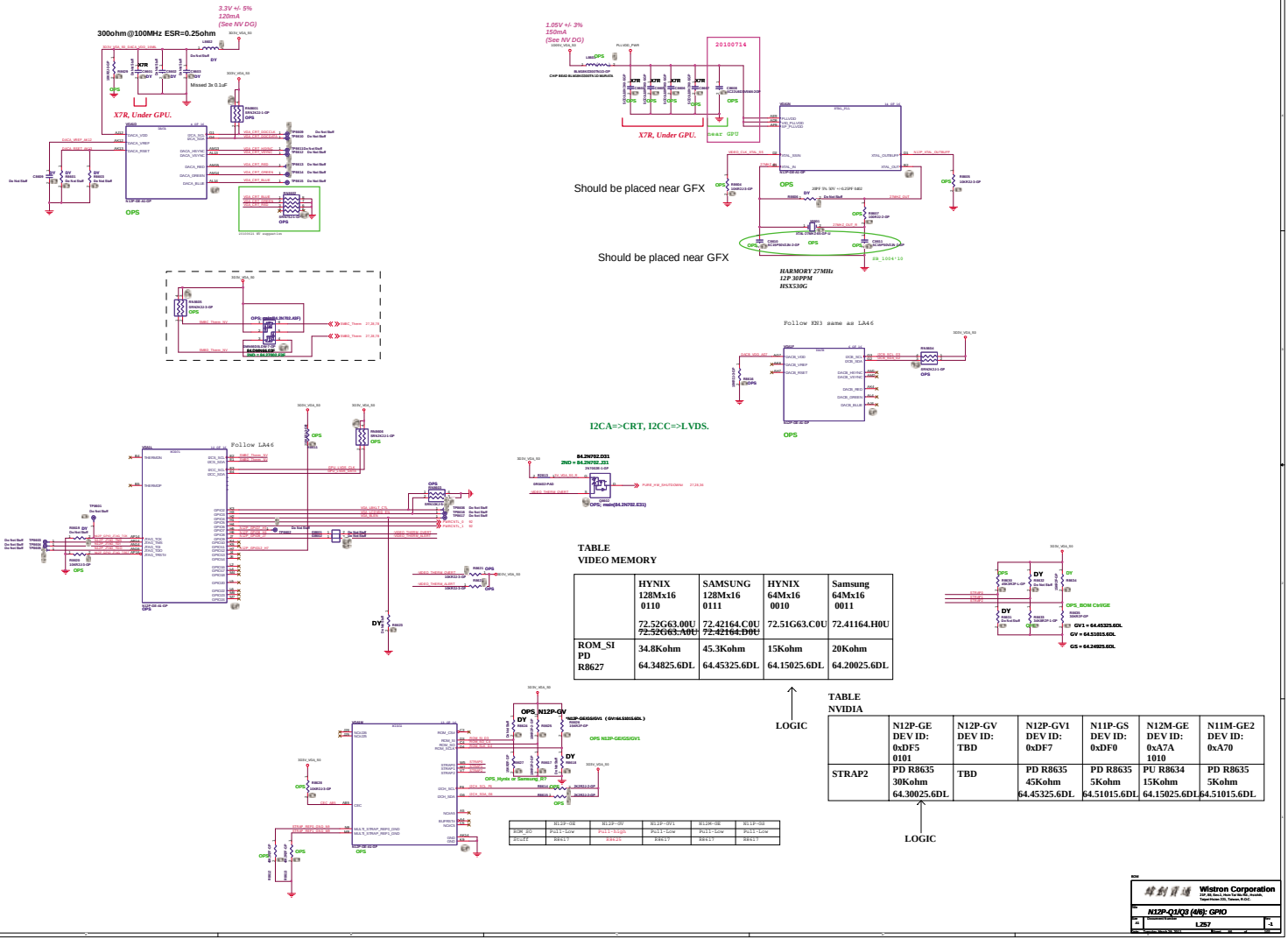




FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

Wistron Corporation			
N12P-Q1/Q3 (3/6): VRAM I/F			
A	L257		3

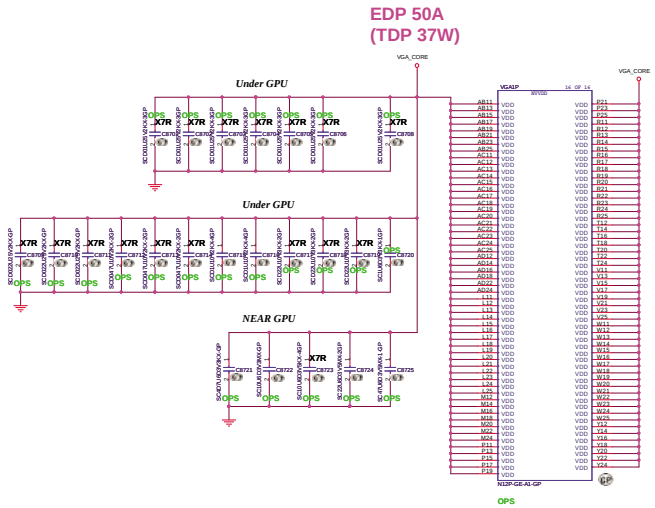


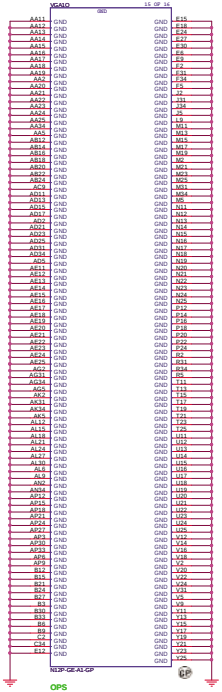
	HYNIX 128Mx16 0110 72.52G63.00U ~~72.52G63.A0U~~	SAMSUNG 128Mx16 0111 72.42164.C0U ~~72.42164.D0U~~	HYNIX 64Mx16 0010 72.51G63.C0U	Samsung 64Mx16 0011 72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

	N12P-GE	N12P-GV	N12P-GV1	N12M-GE	N11P-GS
ROM_SO	Pull-Low	Pull-High	Pull-Low	Pull-Low	Pull-Low
Stuff	R8617	R8625	R8617	R8617	R8617

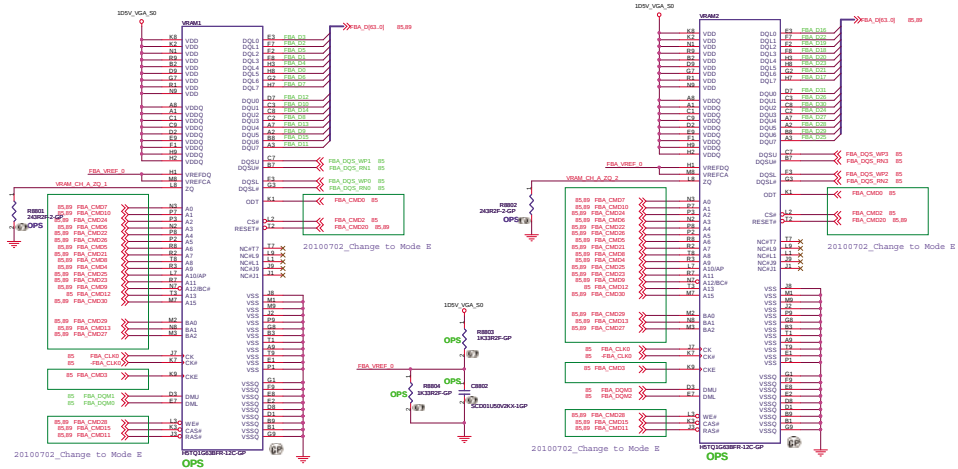
Wistron Corporation
N12P-Q1/Q3 (4/6): GPIO
LZ57





BOM

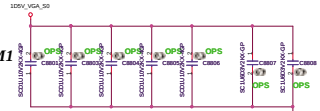
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	N12P-Q1/Q3 (5/6): POWER	
Size: A2	Document Number: LZ57	Rev: -X1
Date: Tuesday, March 29, 2011	Sheet 87 of 100	



FB CMD mapping Mode D-N12x

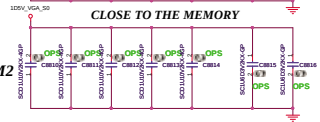
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

FOR VRAM1



CLOSE TO THE MEMORY

FOR VRAM2



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

BOM

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Title: ***VRAM CHANNEL-A***

Size	Document Number	Rev
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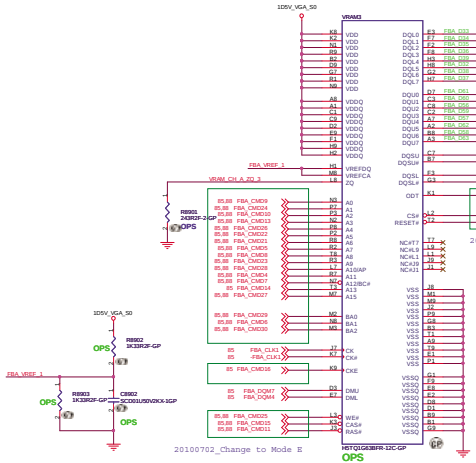
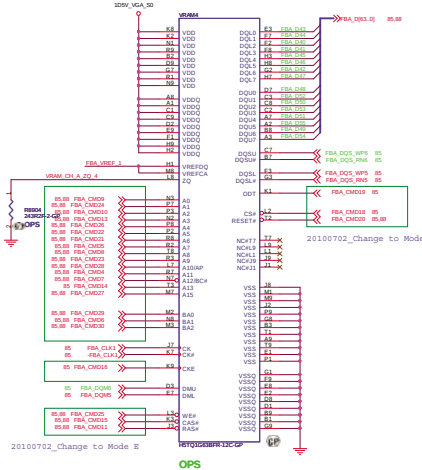
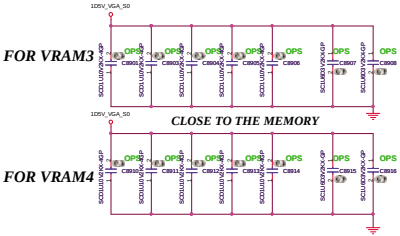




FB CMD mapping Mode D-N12x



VIDEO FRAME BUFFER PORT A

BOM

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File: VRAM CHANNEL-A

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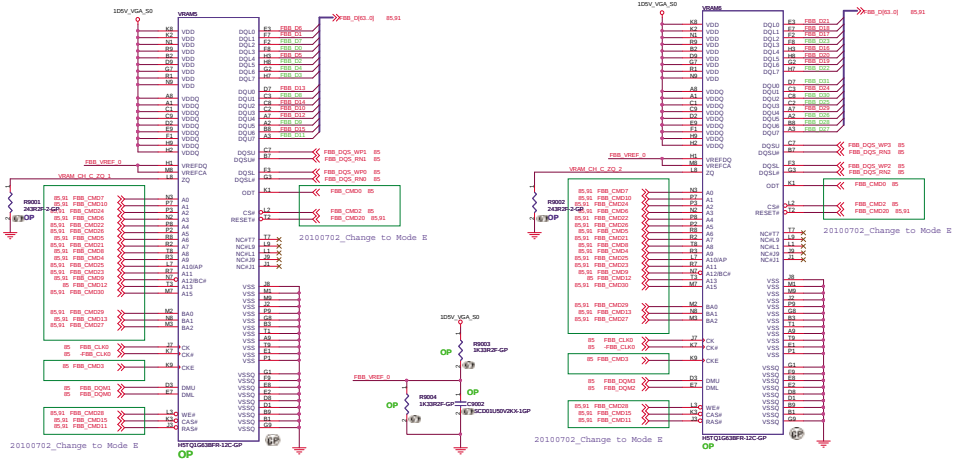
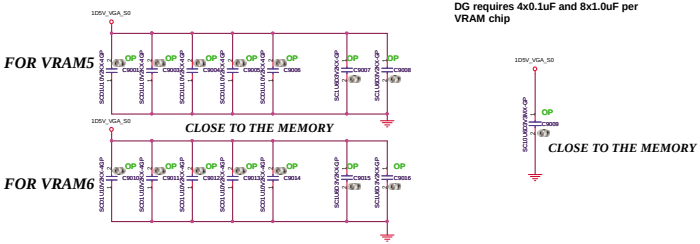


DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

BOM

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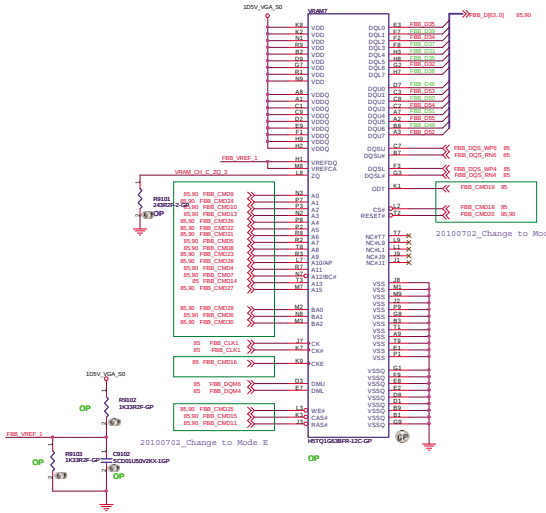
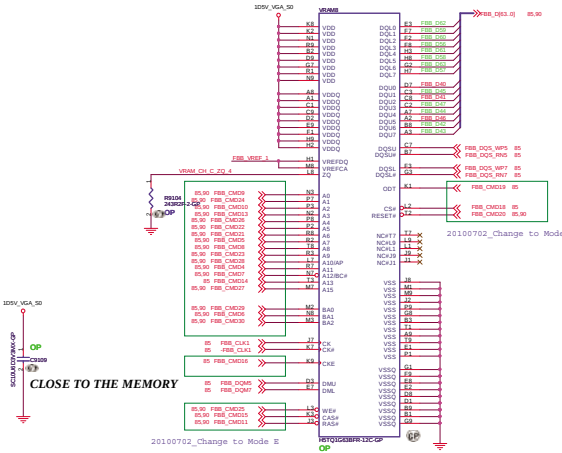
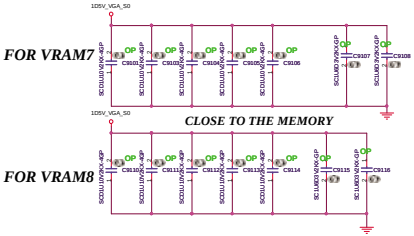
File	VRAM CHANNEL-C
Size	Document Number







VIDEO FRAME BUFFER PORT C

BOM

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Title: VRAM CHANNEL-C

Size	Document Number	Rev
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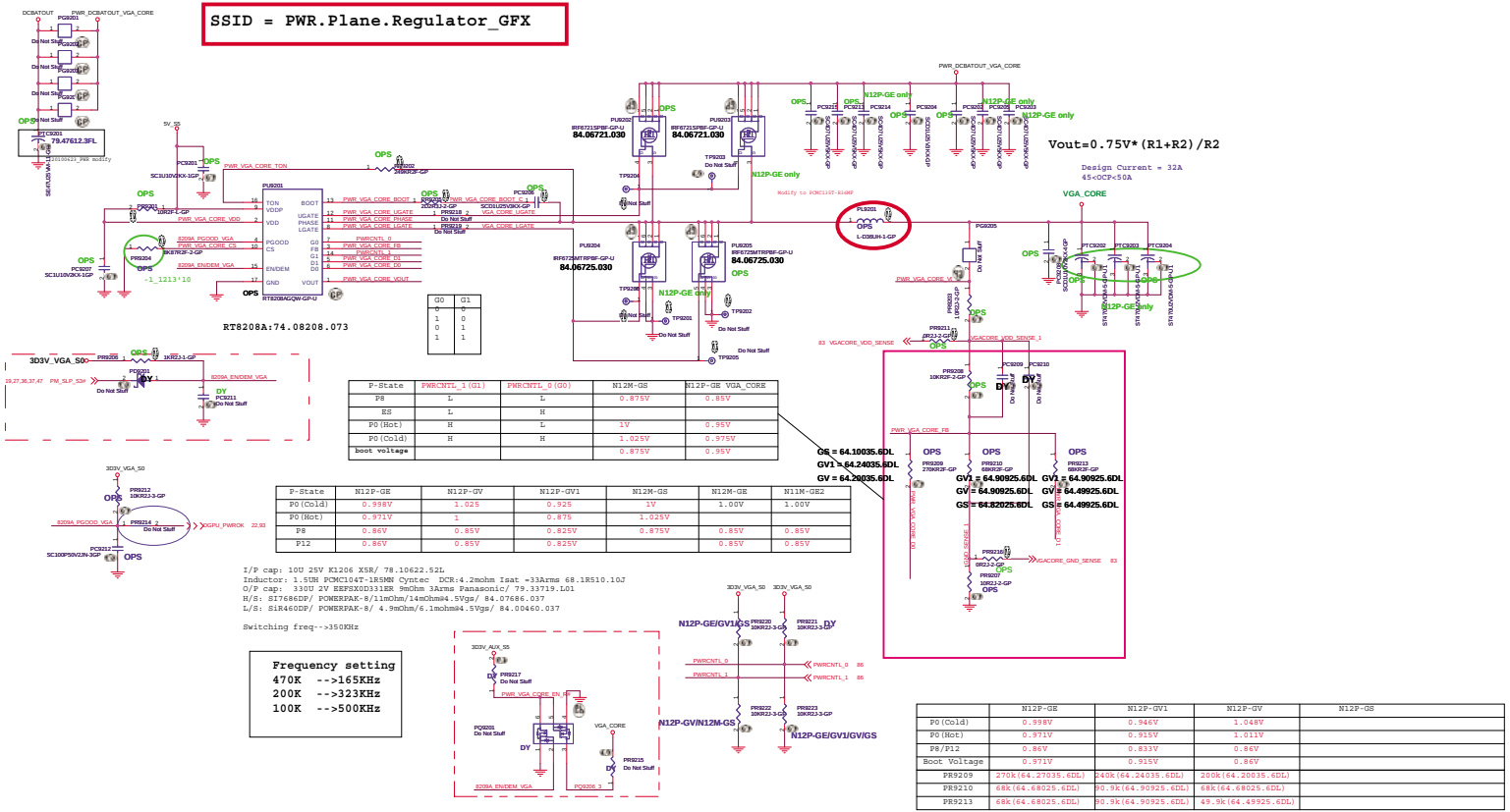
SSID = PWR.Plane.Regulator_GFX



P-State	PWRCNTL_1 (G1)	PWRCNTL_0 (G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
ES	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
P0(Hot)	0.971V	1	0.875	1.025V		
P8	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
P12	0.86V	0.85V	0.825V		0.85V	0.85V

	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
P0(Cold)	0.998V	0.946V	1.048V	
P0(Hot)	0.971V	0.915V	1.011V	
P8/P12	0.86V	0.833V	0.86V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270k(64.27035.6DL)	240k(64.24035.6DL)	200k(64.20035.6DL)	
PR9210	68k(64.68025.6DL)	90.9k(64.90925.6DL)	68k(64.68025.6DL)	
PR9213	68k(64.68025.6DL)	90.9k(64.90925.6DL)	49.9k(64.49925.6DL)	

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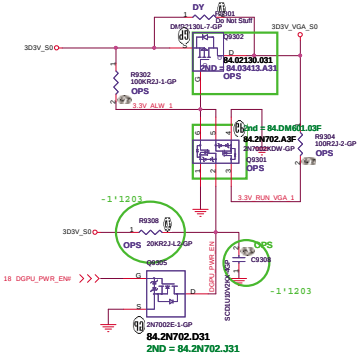
Title: DC/DC_VGA CORE_RT8208B

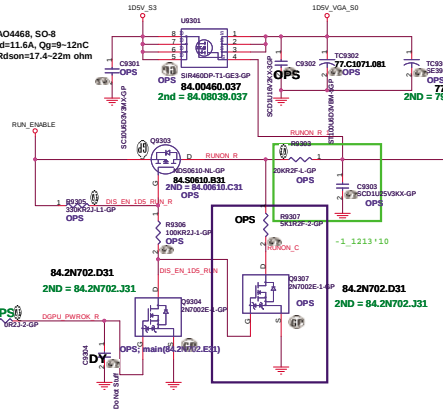
Size: | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 92 of 102

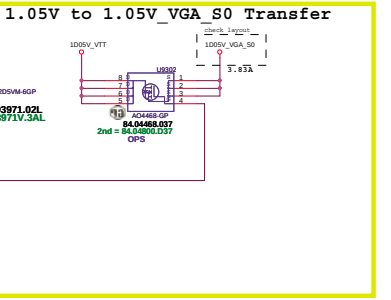
+3VS to 3.3V_DELAY Transfer



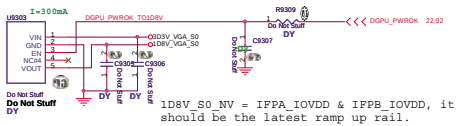
1D5V_VGA_S0



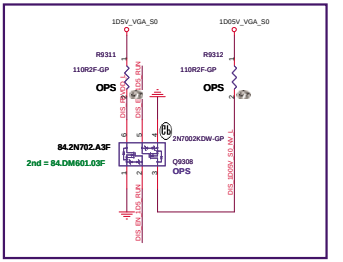
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



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Title: DISCRETE VGA POWER

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Title

LVDS_Switch

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Title: CRT Switch

Size	Document Number	Rev
A3	LZ57	-1

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Title

TOUCH PANEL

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CPU Plate

H13 Do Not Stuff
H14 Do Not Stuff
H15 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff

VGA Std-Off

H10 STF237R128H42-GP
H11 STF237R128H42-GP

OPS

34.4GD01.101 34.4GD01.101

Check test point

3D3V_S0		TP8507	Do Not Stuff
3D3V_AUX_S5		TP8508	Do Not Stuff
3D3V_S5		TP8509	Do Not Stuff
5V_S5		TP8510	Do Not Stuff
11,19,27	PM_PWRBTN#	TP8511	Do Not Stuff
5,11,22,36	H_CPUPWRGD	TP8512	Do Not Stuff
27,36	S5_ENABLE	TP8513	Do Not Stuff
5,11,18,27,31,35,36,65,66,71,83	PLT_RST#	TP8514	Do Not Stuff

Test Point放在Dimm Door打開可量測處

Structure boss

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H12 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

MiniPCI Std-Off

H4 STF237R113H63-GP

34.44P03.101

H16 Do Not Stuff

Do Not Stuff

H17 Do Not Stuff

Do Not Stuff

S1 SPRING-71-GP
S2 SPRING-63-GP
S3 SPRING-63-GP

DY

34.4Y806.001 34.4Y806.001

SC_1101'10

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN#

TP9701 Do Not Stuff
TP9700 Do Not Stuff

POWER TESTING POINT--Bottom

27,68 KBC_PWRBTN#

TP9702 Do Not Stuff
TP9703 Do Not Stuff

AD+

EC9708 EC9709 EC9710 EC9711 EC9712 EC9713

DY Do Not Stuff SCD1U25V2KX-GP

DCBATOUT

EC9720 EC9719 EC9718 EC9717 EC9716 EC9715

DY Do Not Stuff SCD1U25V2KX-GP

AD_JK

SA 0904'10

DCBATOUT

EC9714 SCD1U25V2KX-GP

SA 0809'10

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Title: UNUSED PARTS/EMI Capacitors

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A3	LZ57	-1

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Title

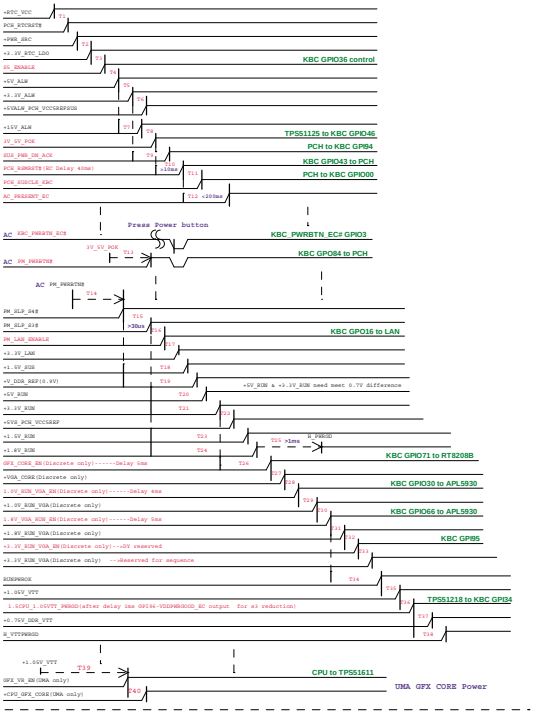
Change History

Size	Document Number	Rev
A4	LZ57	-1

Intel-Power Up Sequence

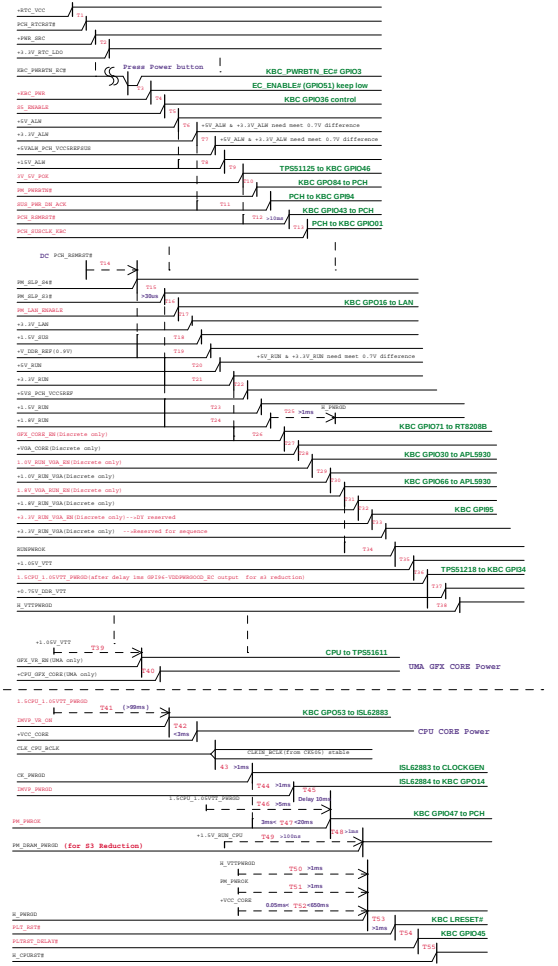
(AC mode)

red word: KBC GPIO

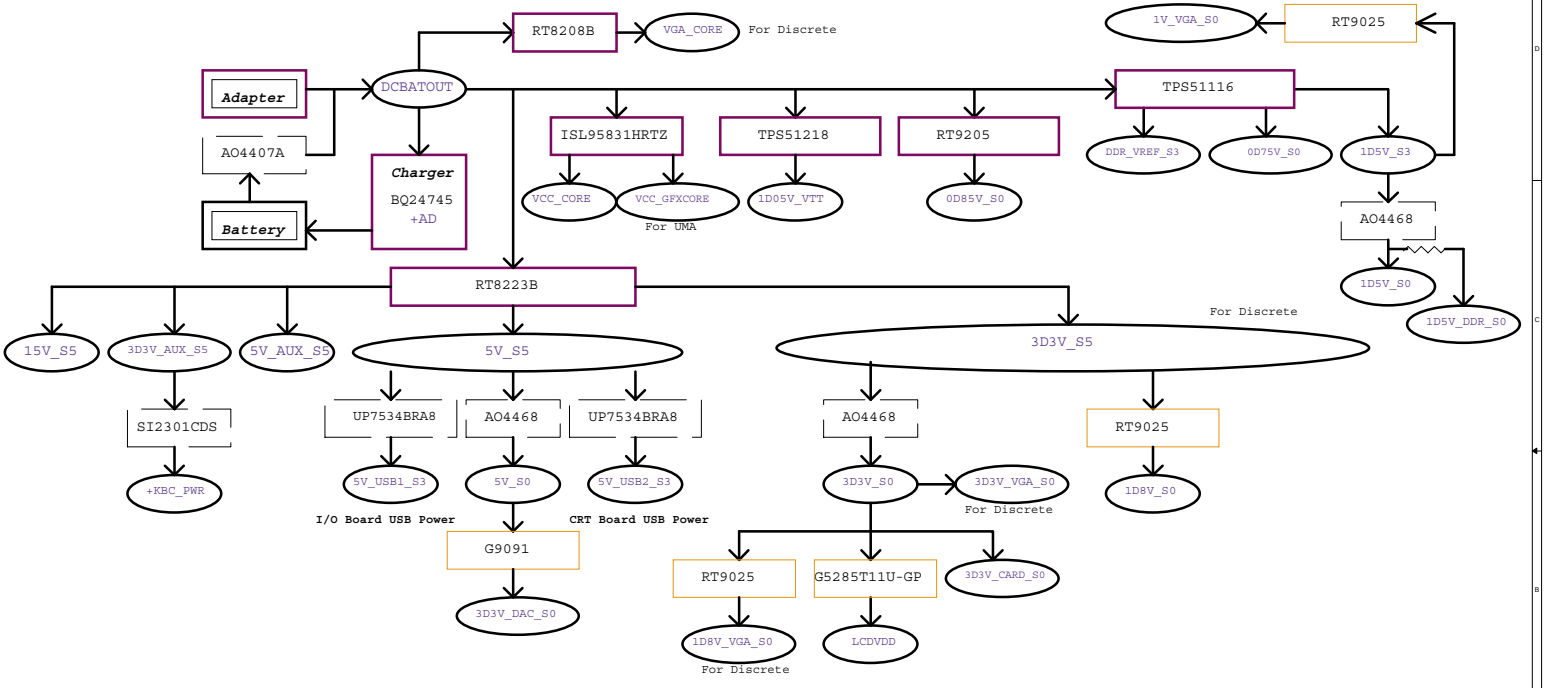


(DC mode)

red word: KBC GPIO



	Wistron Corporation		
	Power Sequence		
	L757		-1



Power Shape

Regulator	LDO	Switch

BOM

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Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	LZ57	-1

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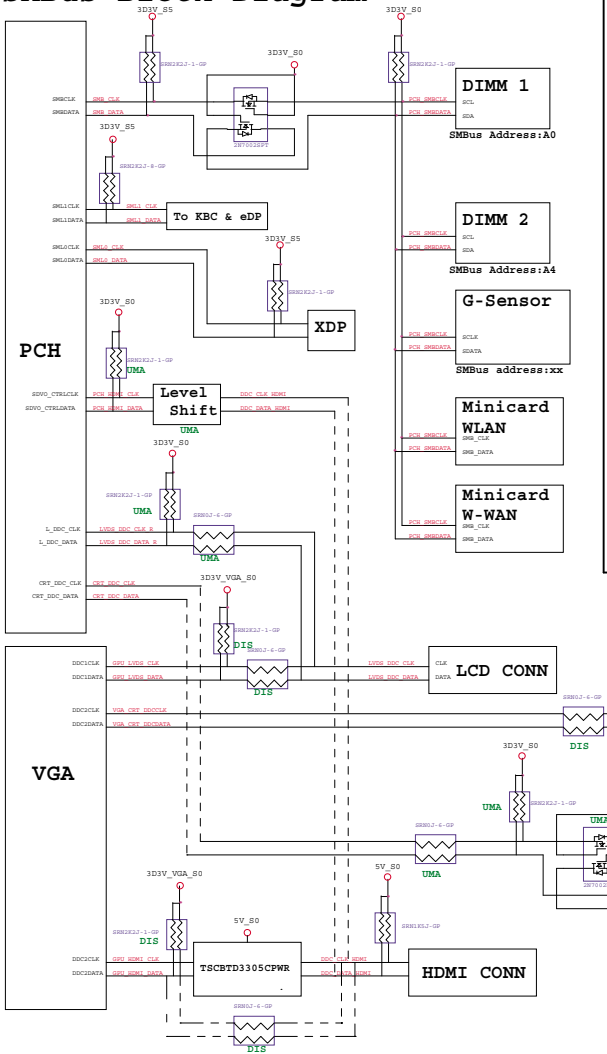
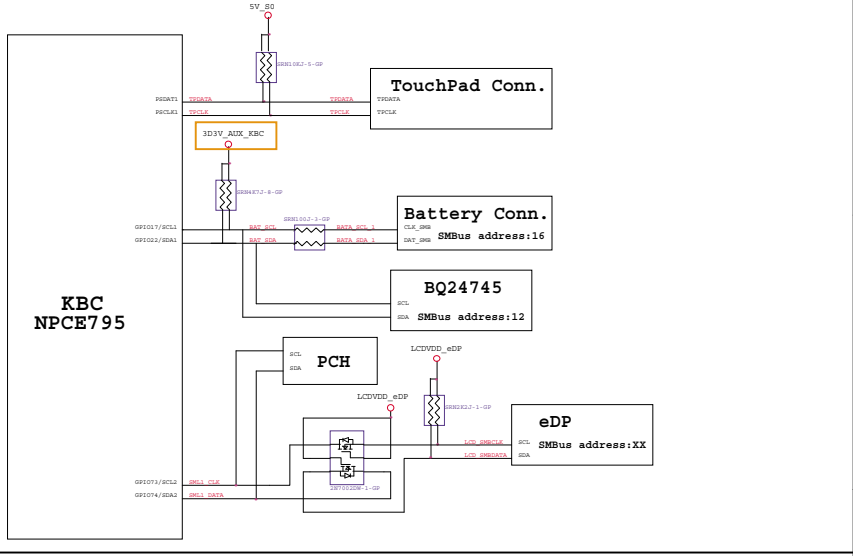
PCH SMBus Block Diagram

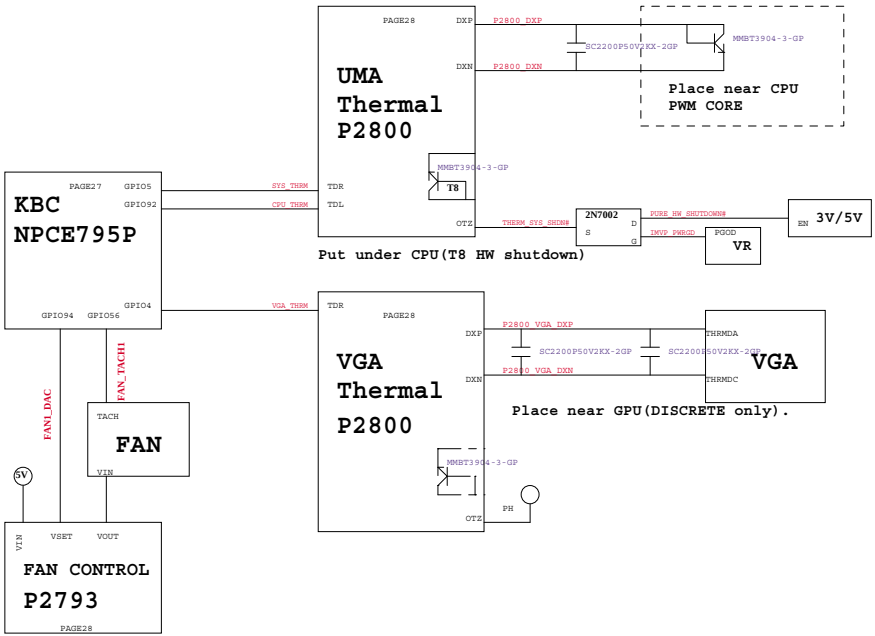


KBC SMBus Block Diagram

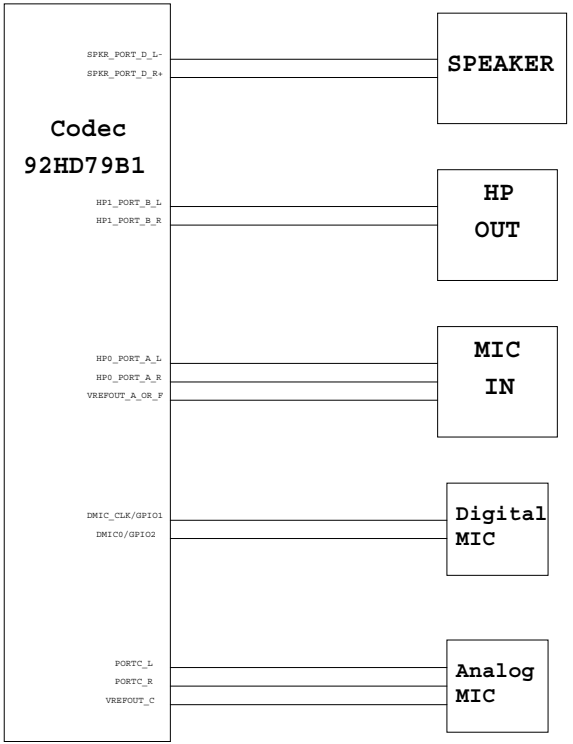


BOM	緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
File	SMBUS Block Diagram		
Size: C	Document Number: LZ57		Rev: -1
Date: Tuesday, March 26, 2013	Sheet 3 of 52		

Thermal Block Diagram



Audio Block Diagram



BOM

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Title: Thermal/Audio Block Diagram		
Size: Custom	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 102 of 102	