Compal Confidential

VIUS5 LA-9001P M/B Schematics Document

AMD FP2 Processor with DDRIII + Husdon M3 FCH
AMD VGA Seymour XT

2012-05-31

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: VAUS5 LA9001P M/B	Rev: 0.3
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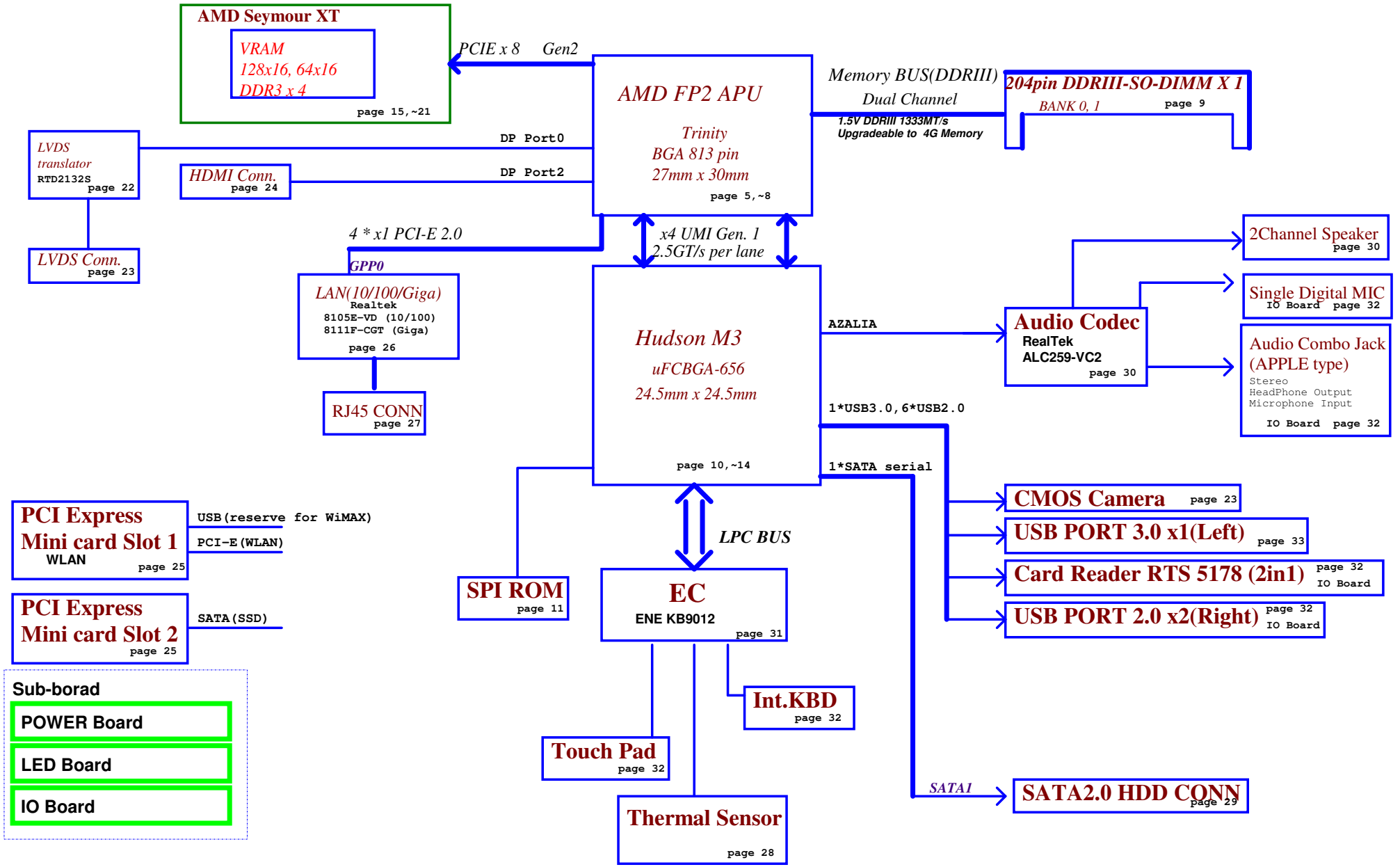

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Title	MB Block Diagram		
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Voltage Rails

power plane / State	+B	+5VALW +3VALW +1.1VALW	+1.5V +1.5V_APU	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +VGA_CORE +3.3VGS +1.8VGS +1.5VGS +1.0VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	0.3
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Ra = R1562
Rb = R1564

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
SMB_EC_CK2_SUS SMB_EC_DA2_SUS	KB9012 +3VALW	X	X	X	X	X	X	X	V +1.5V	X
FCH_SCLK0 FCH_SDATA0	FCH +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS (LV shifter)	V	X	X	X	X	V	X	X	V

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_101xb
SB-TSI(default)	1001_100xb
VGA(thermal)	1000_001xb
RTD2132S	1010_1000b

FCH SM Bus address

Device	Address
DDR DIMM1	1001 000Xb

USB Port Table

USB 2.0	USB 3.0		Port	4 External USB Port
			0	USB Port (Right Side 1)
			1	USB Port (Right Side 2)
			2	Mini Card(WLAN)
			3	Camera
			4	
			5	CardReader
			6	
			7	
			8	
			9	
	XHCI	0	10	USB Port (Left Side)
		1	11	
		2	12	
		3	13	

USB OC MAPPING

OC#	USB Port	
0	USB20 port10	USB30 port0
1	USB20 port0 port1	
2		
3		

APU PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	

FCH PCIE PORT LIST

Port	Device
1	
2	
3	
4	

BOM Structure Table

BOM Structure	BTO Item
A4R1@	A4 BGA APU (R1 compal part)
A4R3@	A4 BGA APU (R3 compal part)
A6R1@	A6 BGA APU (R1 compal part)
A6R3@	A6 BGA APU (R3 compal part)
A8R1@	A8 BGA APU (R1 compal part)
A8R3@	A8 BGA APU (R3 compal part)
A10R1@	A10 BGA APU (R1 compal part)
A10R3@	A10 BGA APU (R3 compal part)
SXTR1@	Seymour XT GPU (R1 compal part)
SXTR3@	Seymour XT GPU (R3 compal part)
A70MR1@	A70 Hudson M3 FCH (R1 compal part)
A70MR3@	A70 Hudson M3 FCH (R3 compal part)
PX@	Common VGA circuit
CMOS@	CMOS Camera part
UMA@	UMA strap pin
GAS@	Gastube
8105@	RTL8105E
GIGA@	RTL8111F
HDMI@	HDMI part
NONAOAC@	No AOAC function
AOAC@	support AOAC function
ME@	ME part
DEBUG@	Debug Switch (MP will remove)
@	Unpop
SSD@	SSD part

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Title: *Notes List*

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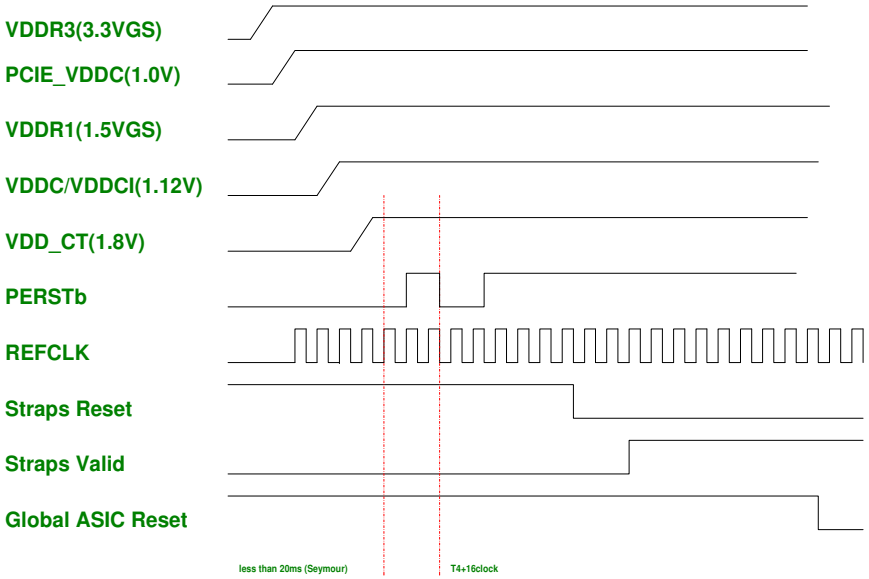
Power-Up/Down Sequence

"Thames" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa). For BACO enabled designs, VDDC must ramp up before VDD_CT at system power up.
- For power down, reversing the ramp-up sequence is recommended



Without BACO option :

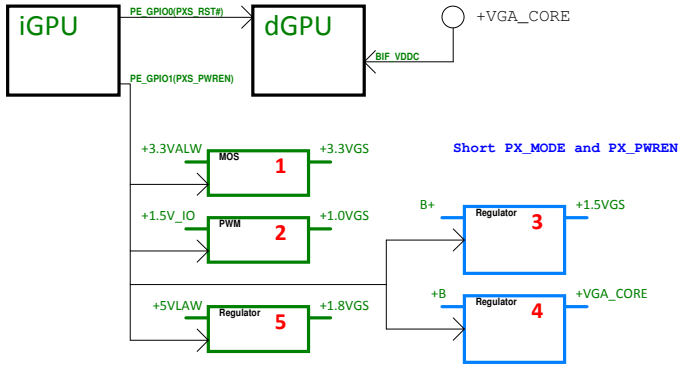
PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28

PX5.0



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Title: VGA Notes List

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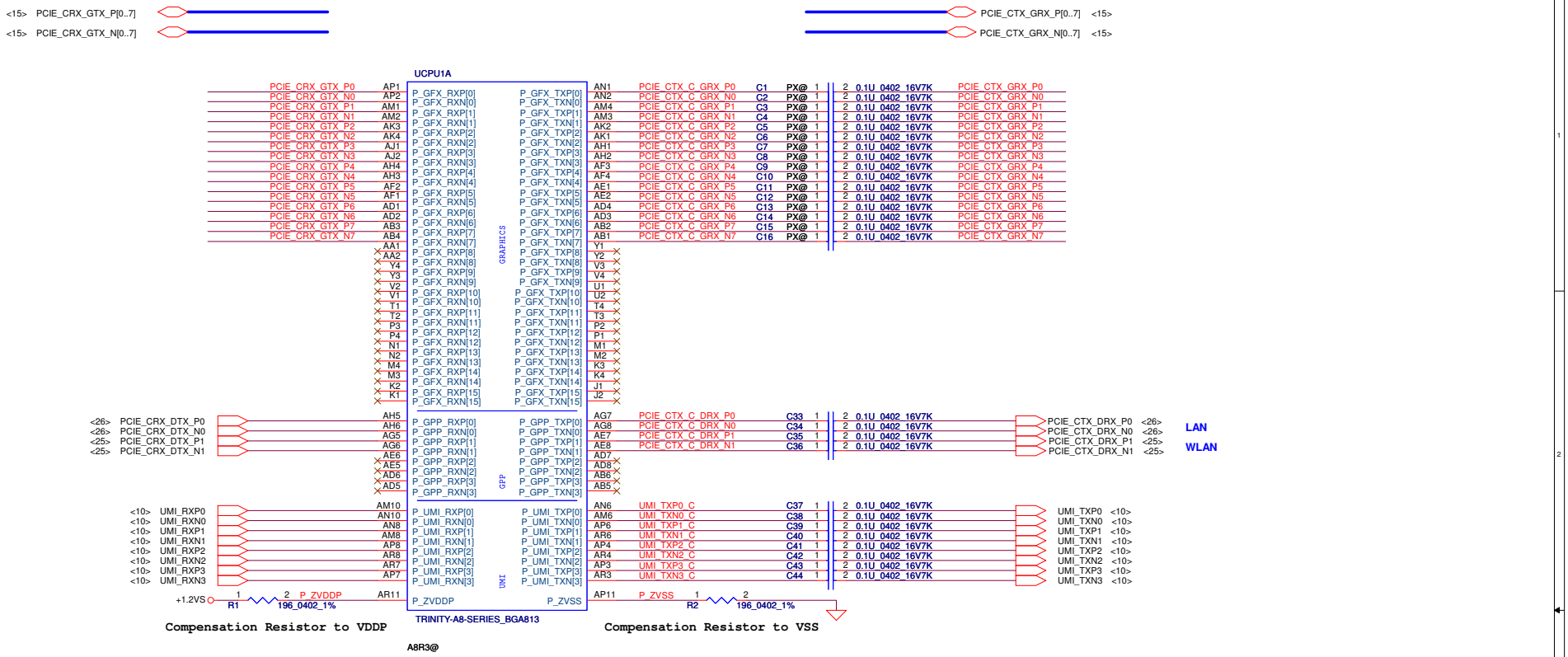
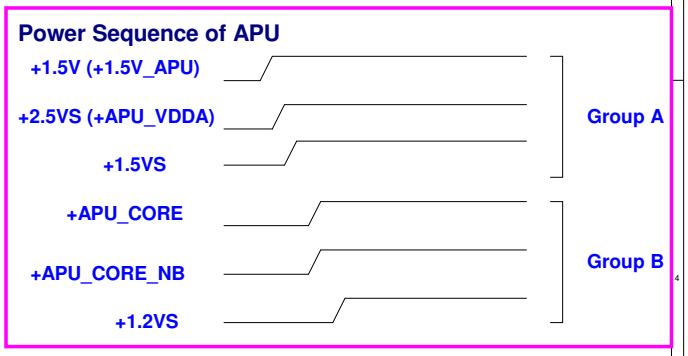


All power supplies in Power Sequencing Group A must be stable and within specification before any power supply in Power Sequencing Group B is greater than 10 percent of its specified typical operating value.

All power supplies in Power Sequencing Group B must be stable and within specification one ms before the assertion of PWROK.

No sequencing relationships are required between the power sequencing groups during S3 entry. DDR3 compatible processors require VDDIO to remain powered and within specification during the S3 sleep state. All other processor power supply planes are powered down during S3.



UCPU1 A4R3@
A4 SERIES ZM198169E2351 1.9G BGA813

UCPU1 A6R3@
A6 SERIES ZM212169E2451 2.1G BGA813

UCPU1 A10R3@
A10 SERIES ZM202268E4451 2G BGA813P

ZZZ1
LA9001P
DA60000TW00

UCPU1 A4R1@
A4 SERIES AM4355SHE23HJ 1.9G BGA813

UCPU1 A6R1@
A6 SERIES AM4455SHE24HJ 2.1G BGA813

UCPU1 A10R1@
A10 SERIES AM4655SIE44HJ 2G BGA813P

UCPU1 A8R1@
A8 SERIES AM4555SHE44HJ 1.6G BGA813

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Title: FP2 PCIE/UMI

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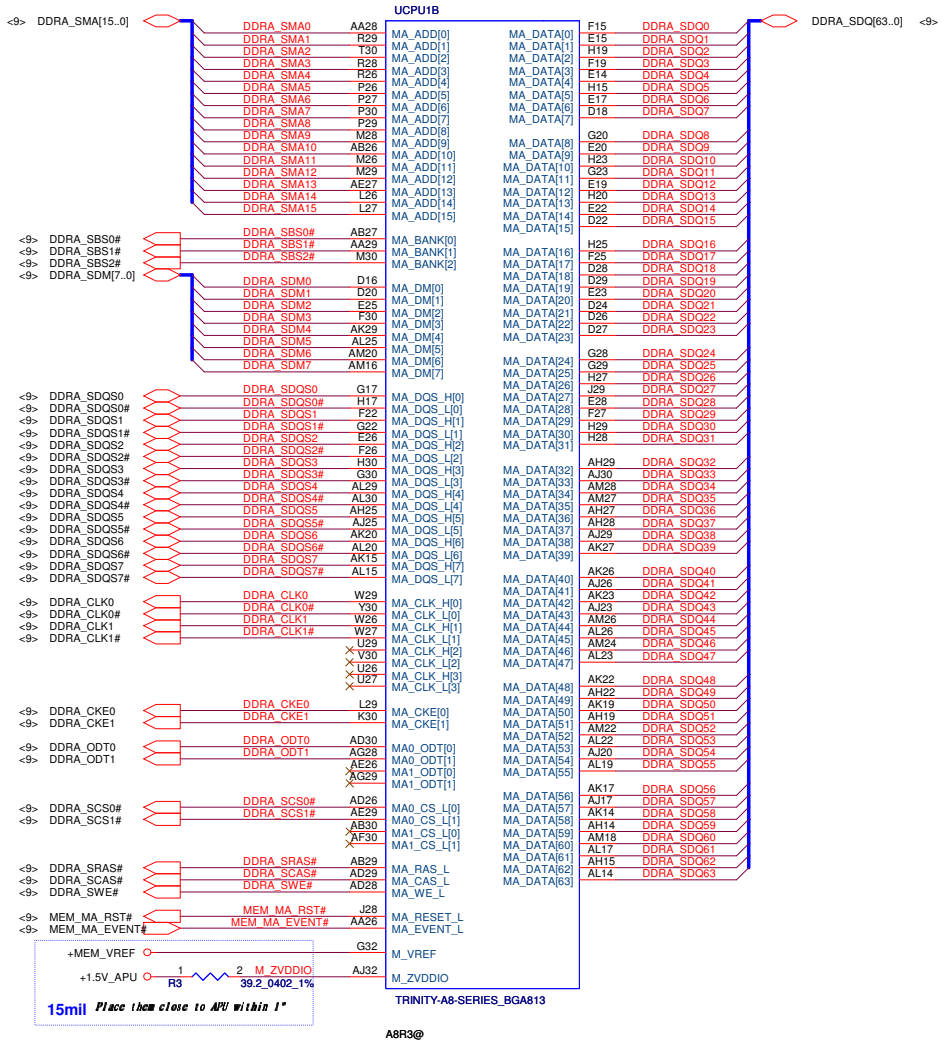

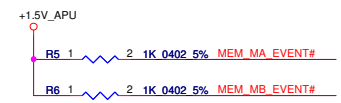

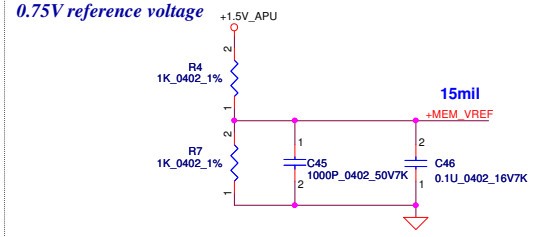

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Compal Electronics, Inc.			
Title: FP2 DDRIII Memory I/F			
Size: B/25 Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
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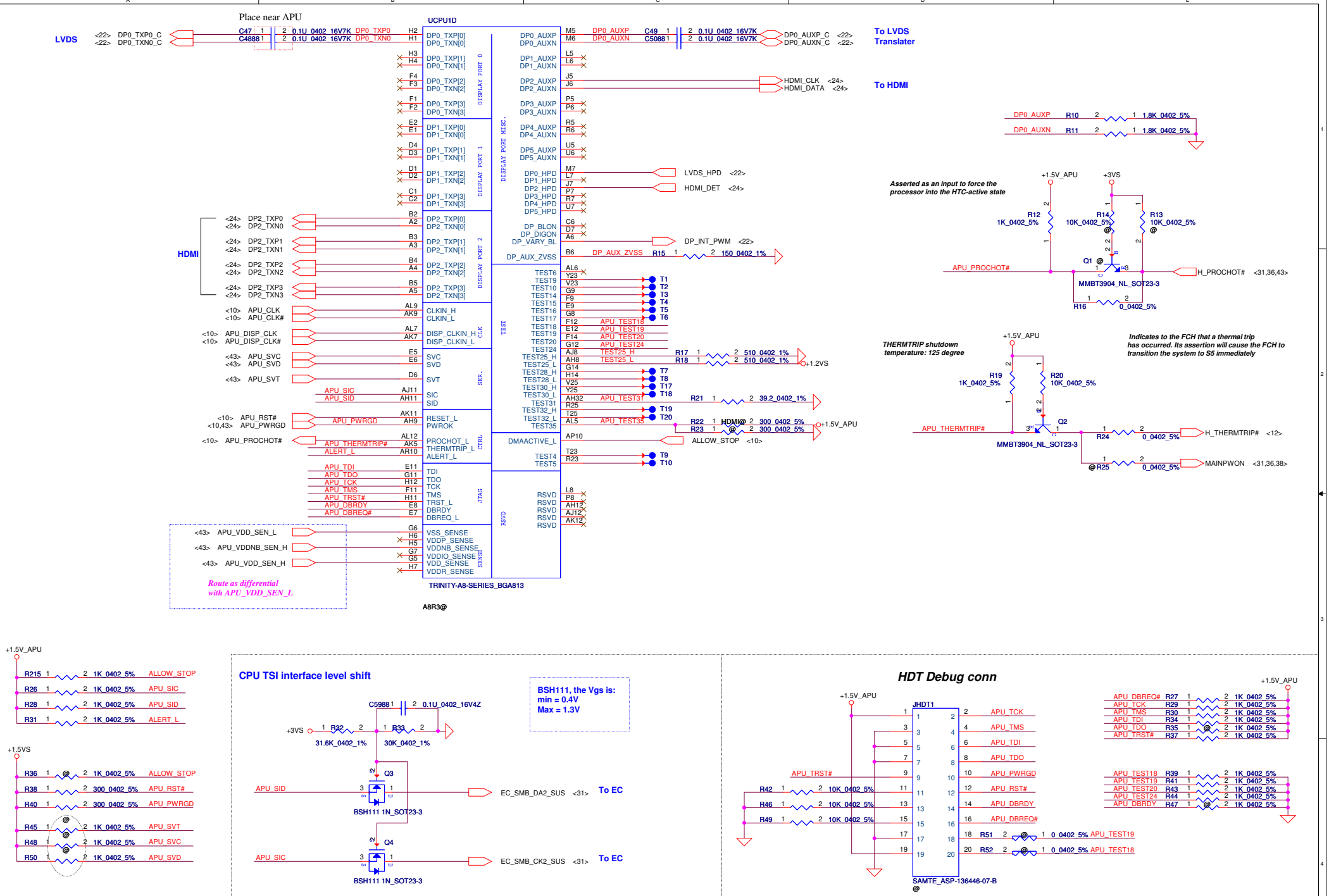

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Compal Electronics, Inc.			
Title	FP2 Display/MISC/HDT		
Size	Document Number		Rev
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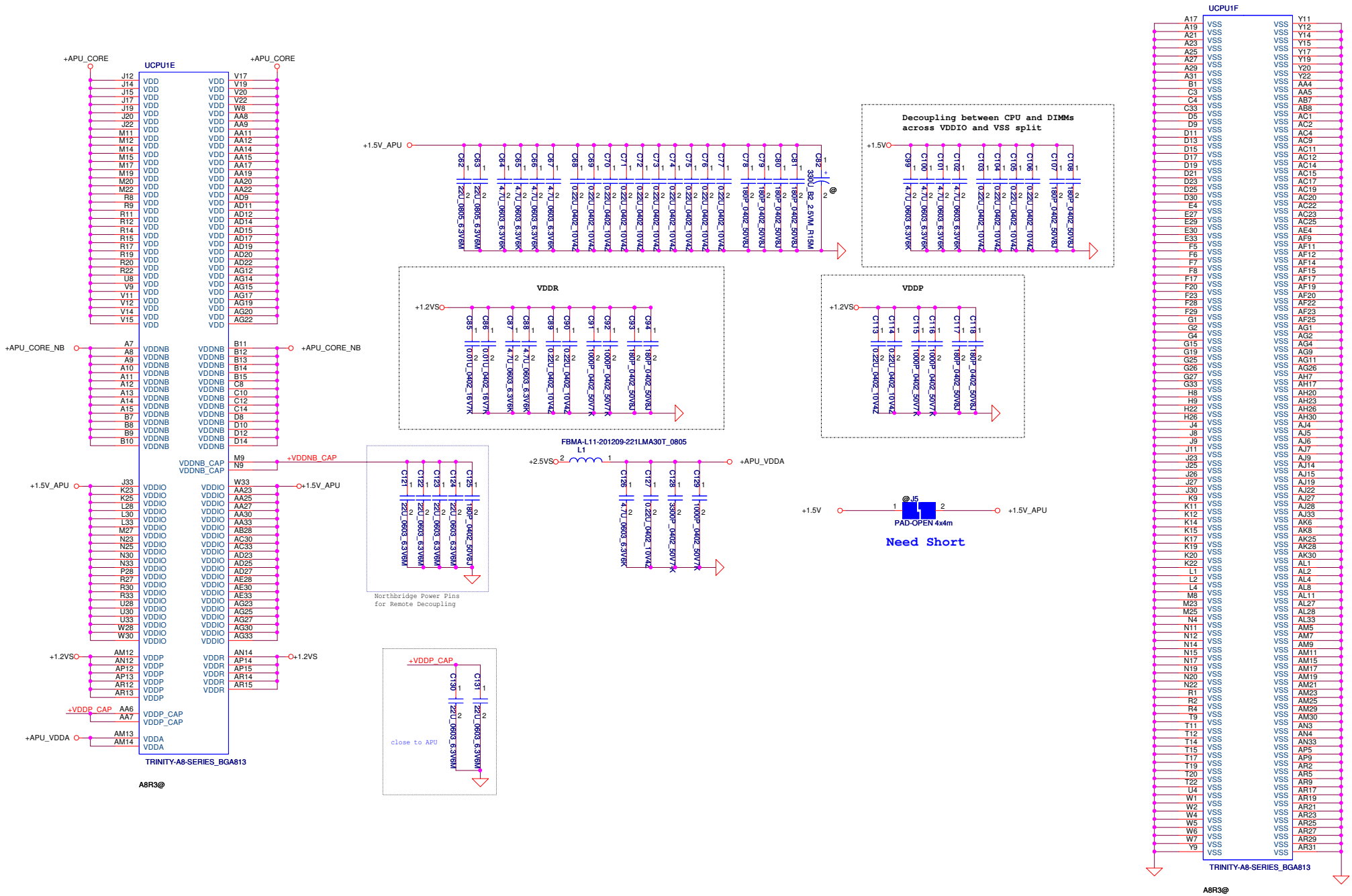

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Title: FP2 PWR / GND

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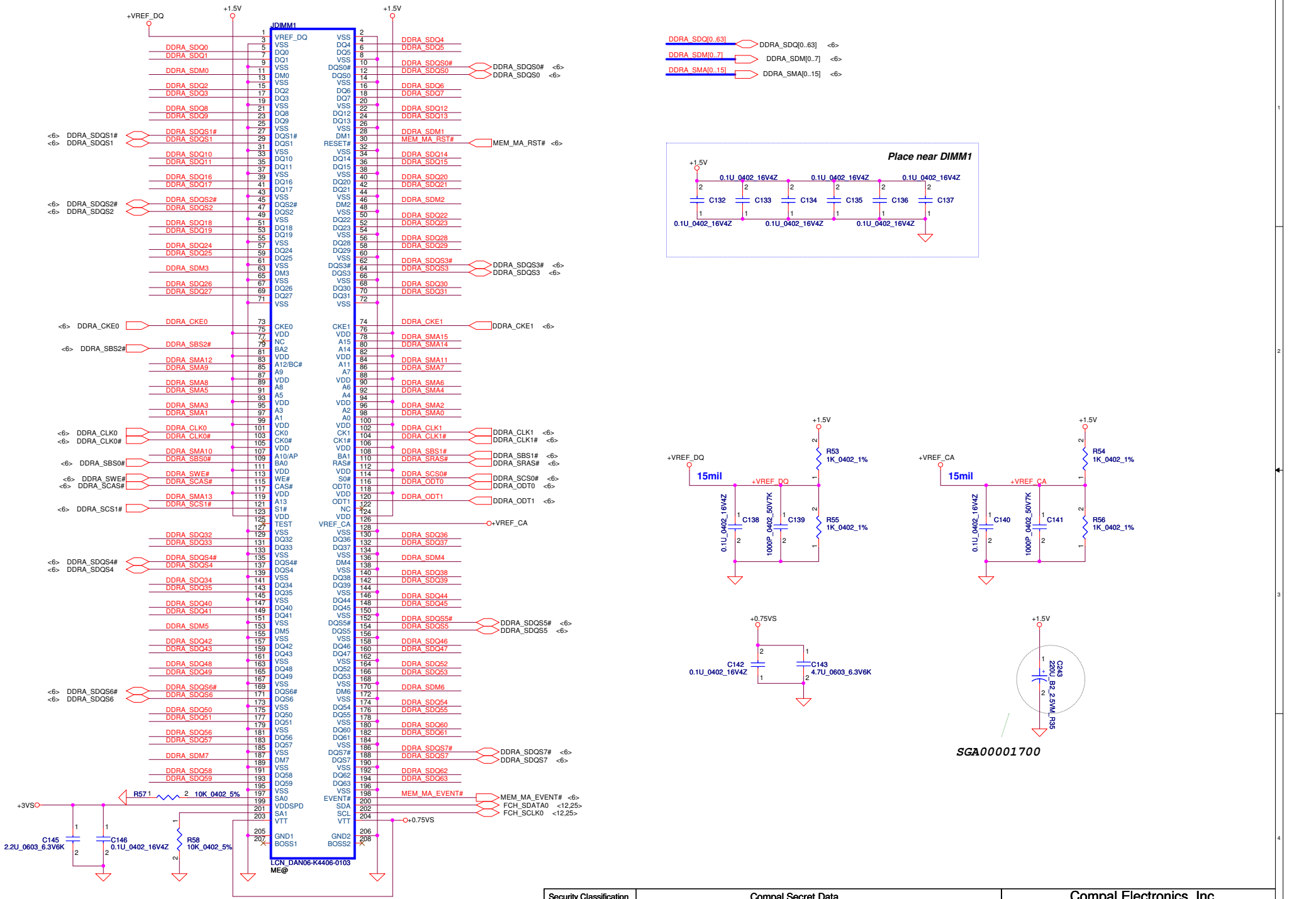

Reverse Type H:4mm

<Address: 00>

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Compal Electronics, Inc.			
Title: DDRIII SO-DIMM 1			
Size: Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
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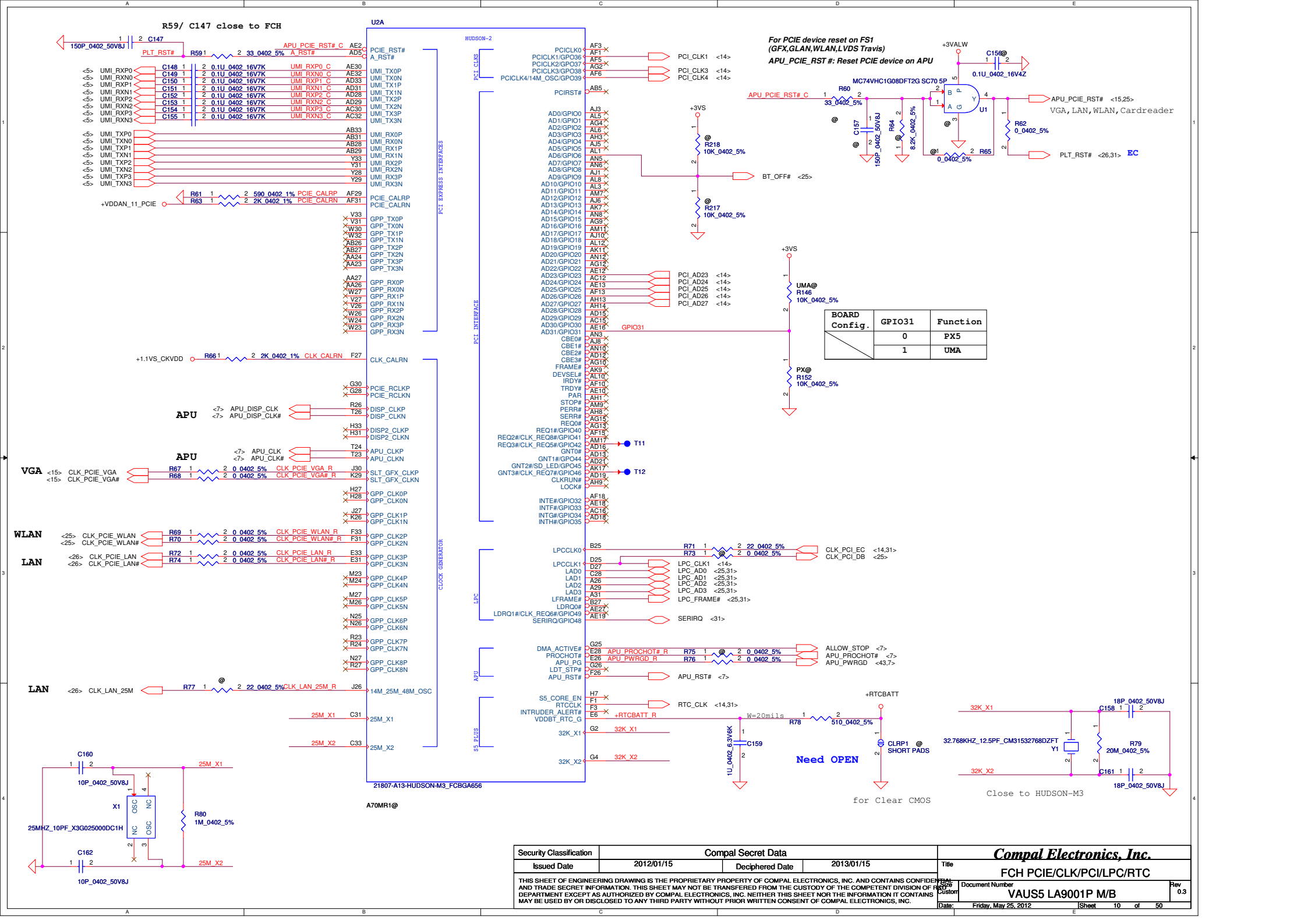

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Title: FCH PCIE/CLK/PCI/LPC/RTC

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

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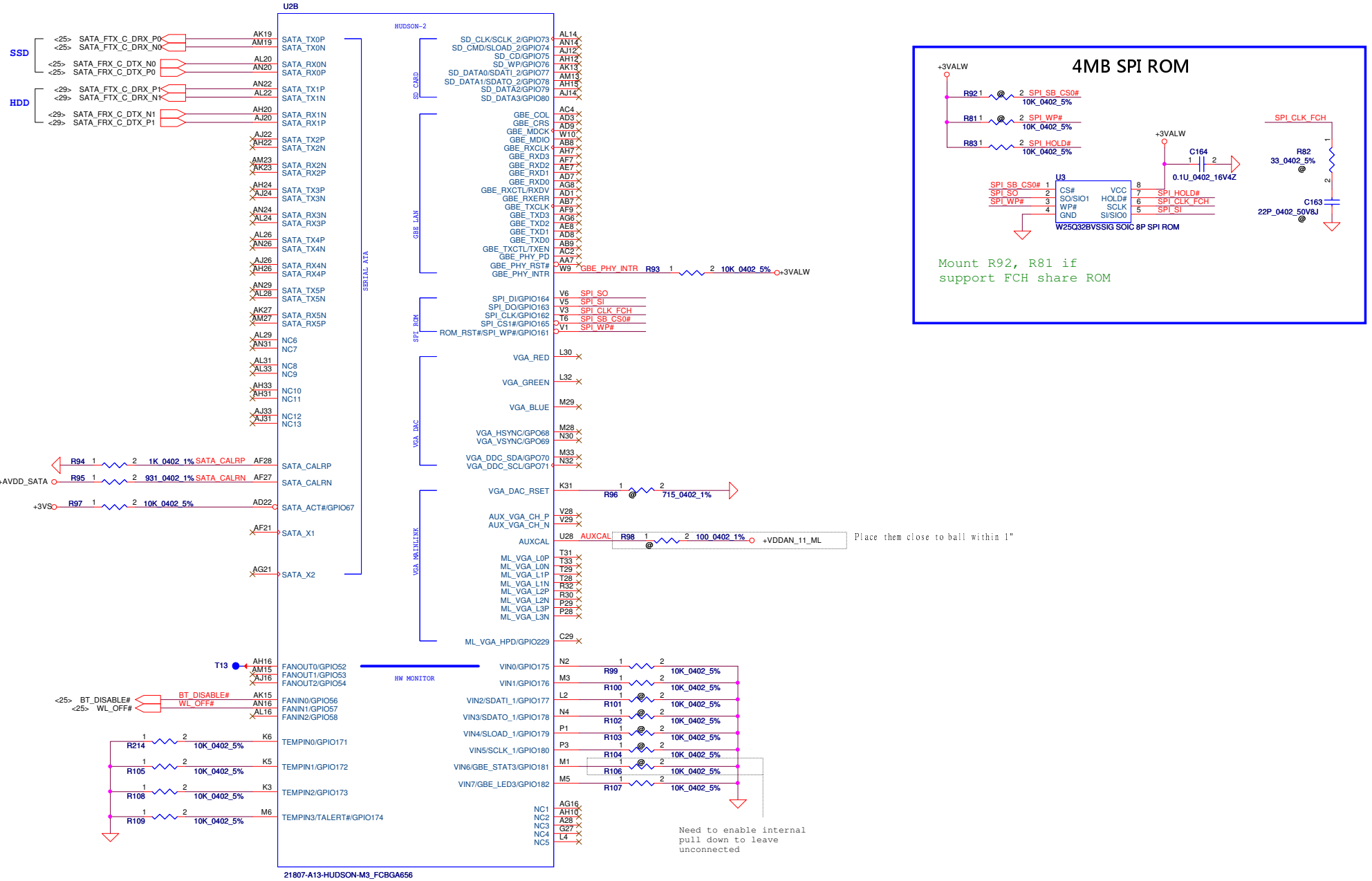

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Compal Electronics, Inc.	
Title	FCH SATA/SPI/VGA/HWM/SD
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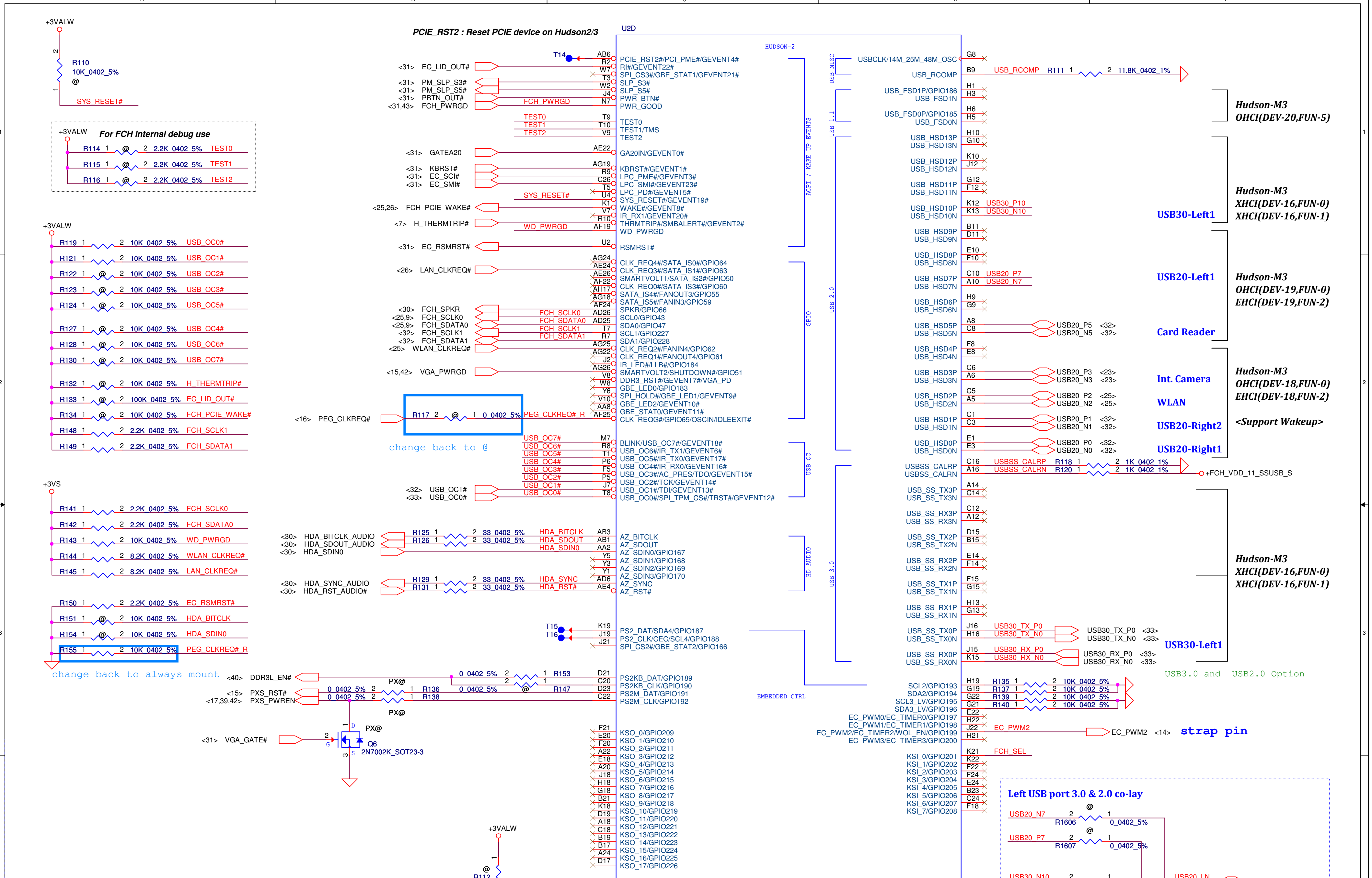

FCH Chip	FCH_SEL
A60M2	Low
A70M3	High

Before setting (for reference)

AMD only support FP2 + A70M3,
@ FCH_SEL function

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Issued Date	2012/01/15	Deciphered Date 2013/01/15	Title: FCH-ACPI/USB/HDA/GPIO

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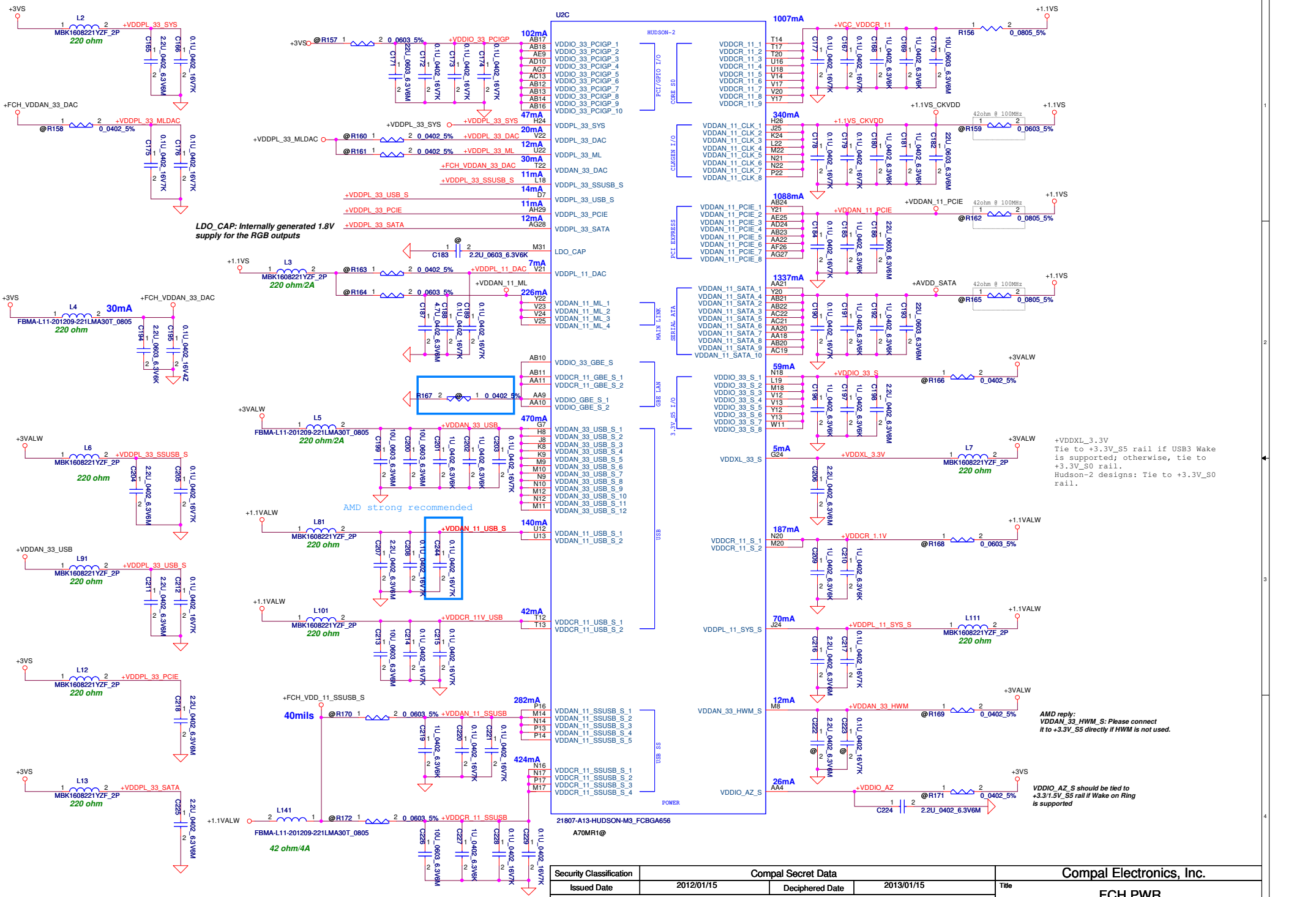

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Compal Electronics, Inc.

Title: FCH PWR

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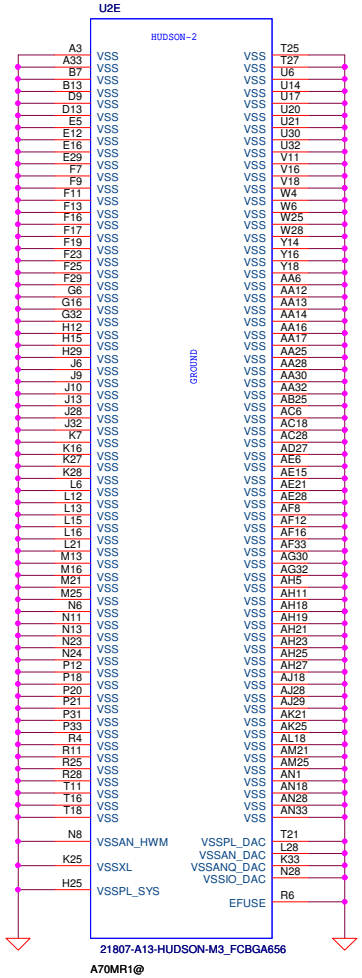
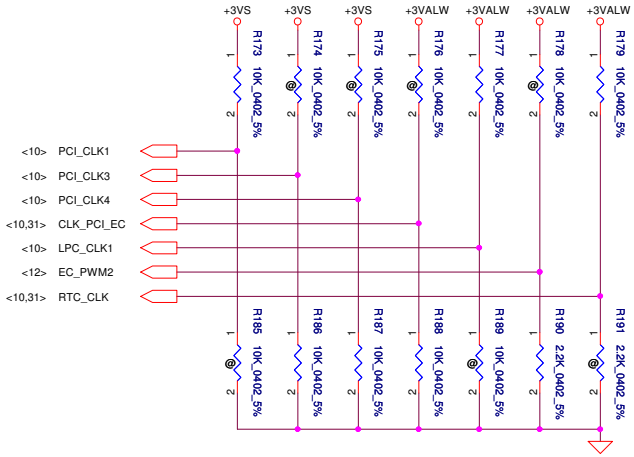


STRAP PINS

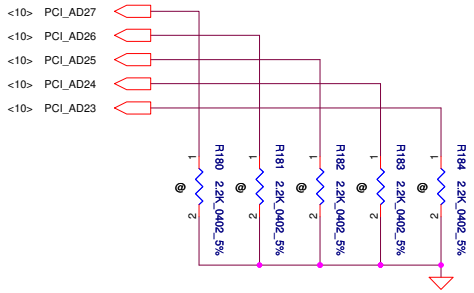
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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Issued Date	2012/01/15	Deciphered Date 2013/01/15	Title: FCH-VSS/Strap

Size: D Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
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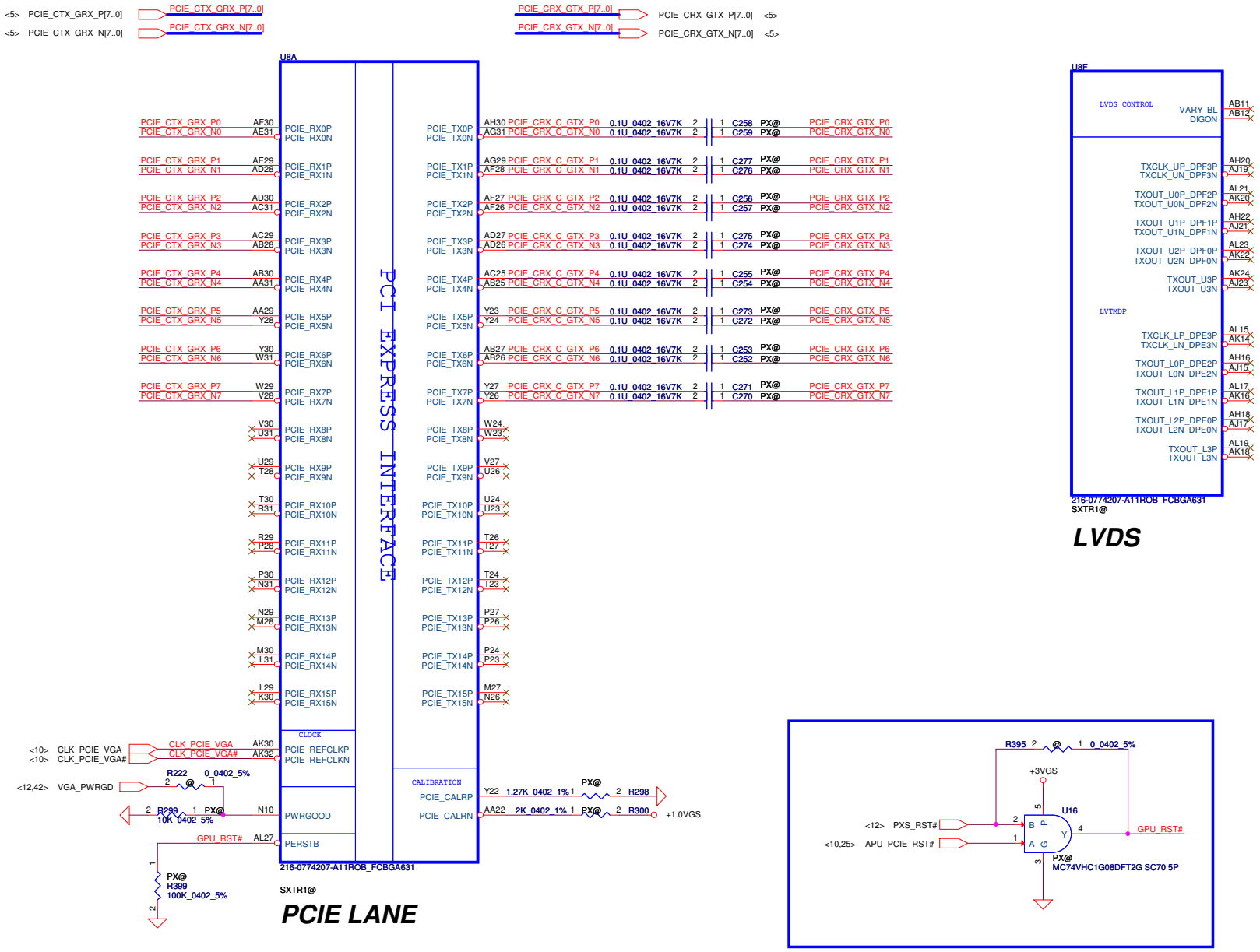

U8 SXTR3@

S IC 216-0809024 A11 SEYMOUR XT S3 C38!

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Compal Electronics, Inc.

Title: SeymourXT-S3 PCIE/LVDS

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

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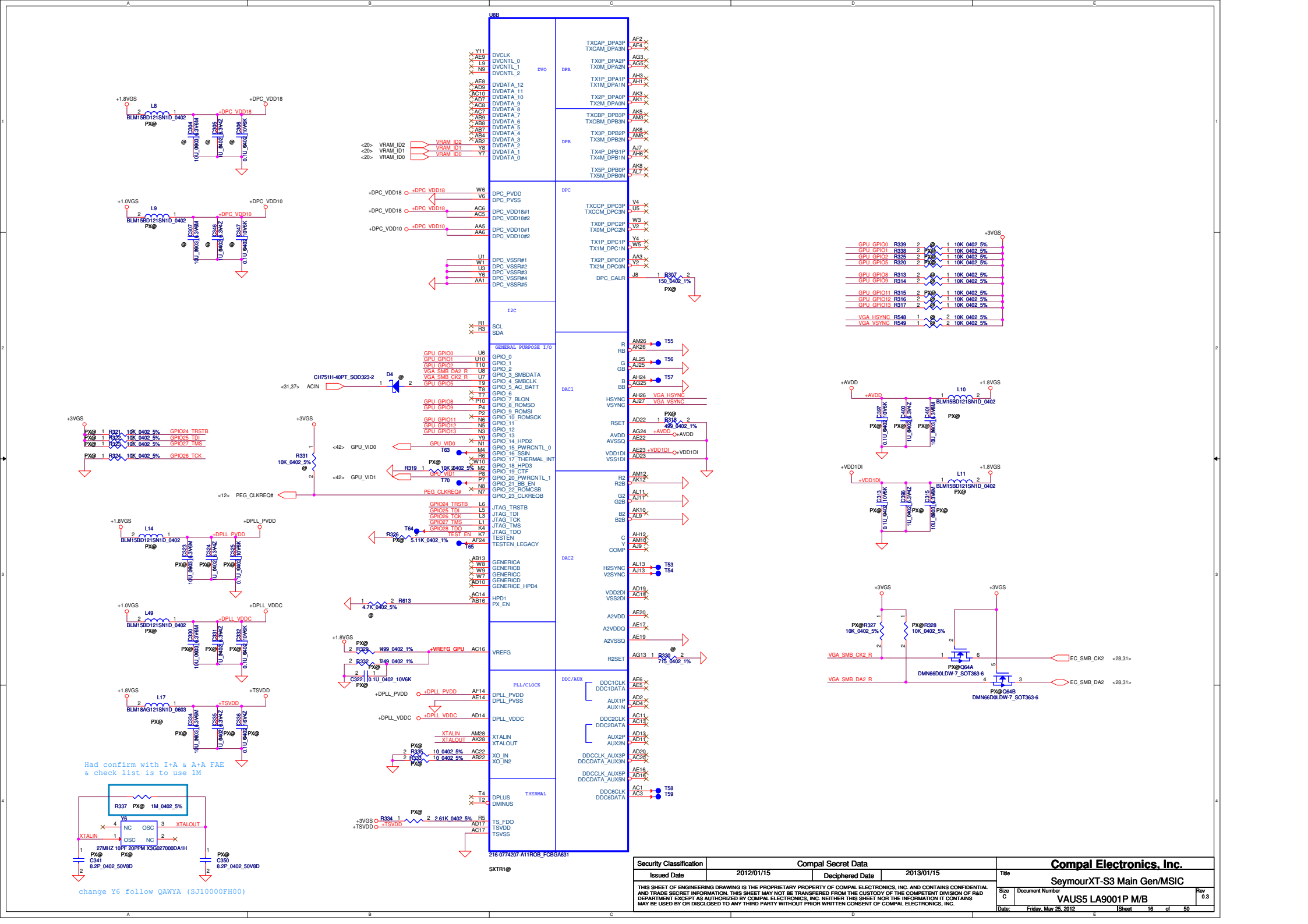

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Compal Electronics, Inc.

Title	SeymourXT-S3 Main Gen/MSIC		
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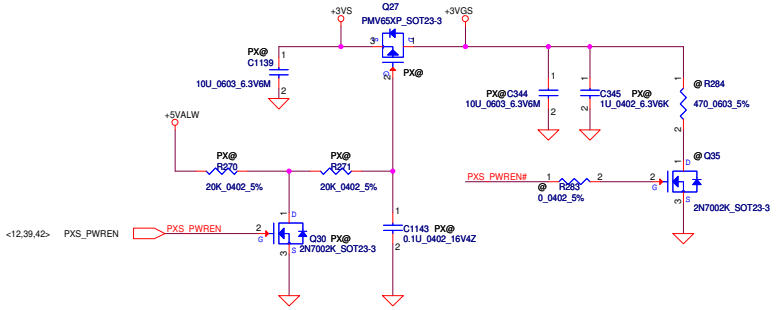
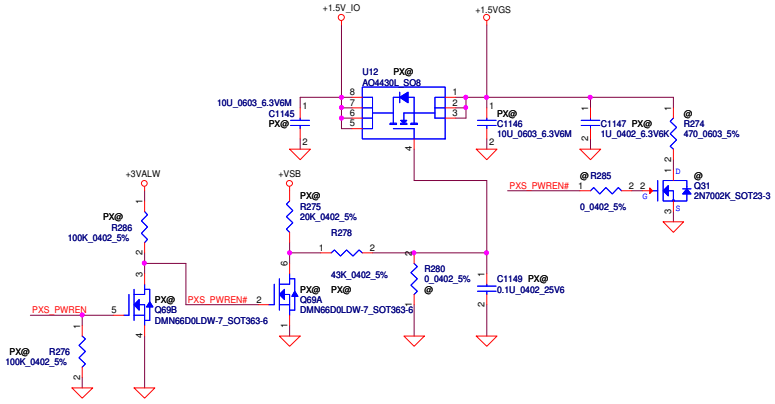
+3.3VS TO +3.3VGS



+1.5V_IO TO +1.5VGS



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Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: SeymourXT-S3 BACO Power

Size	Document Number	Rev
C	VAUS5 LA9001P M/B	0.3

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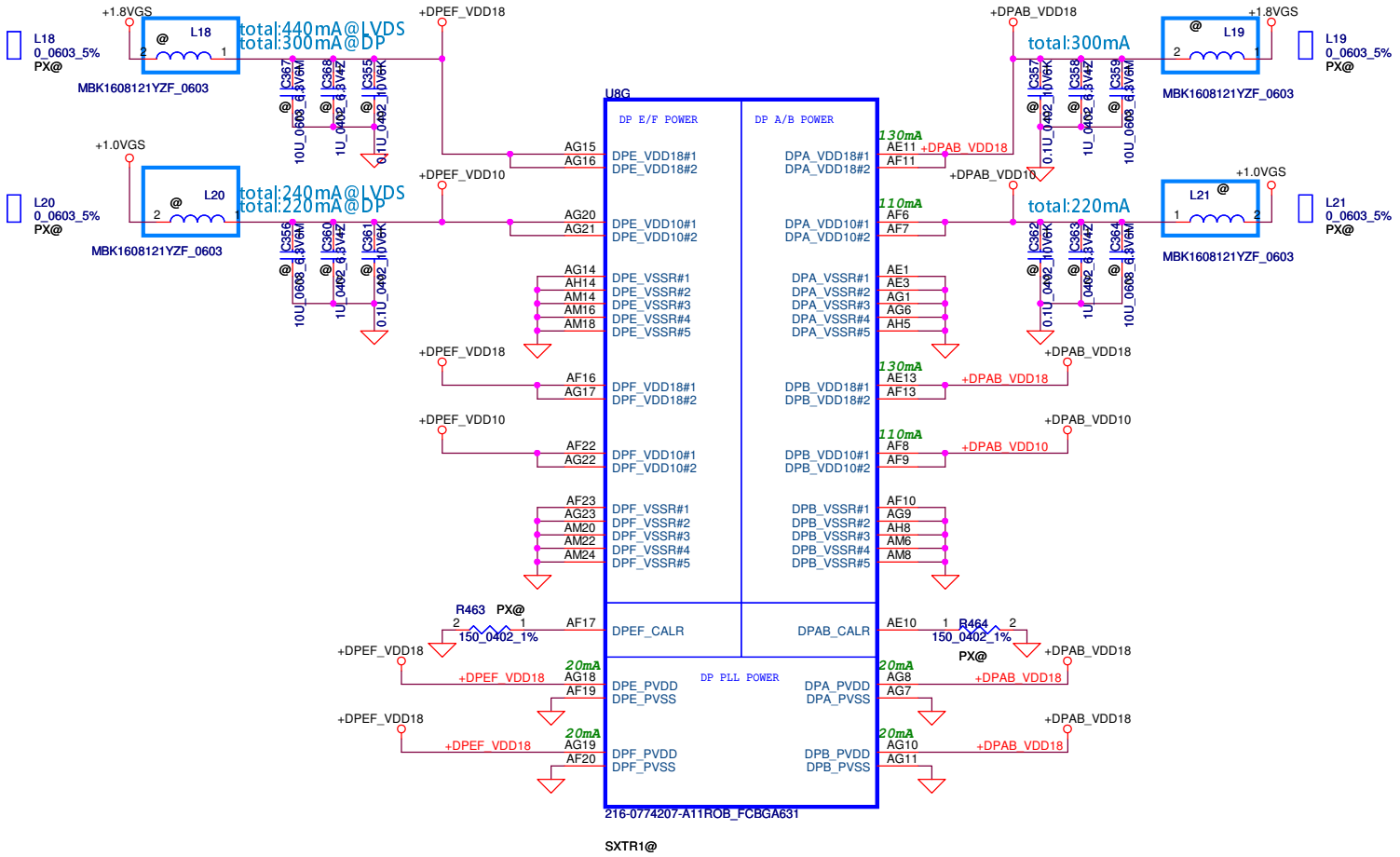

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: SeymourXT-S3 DPX Power

Size	Document Number	Rev
B	VAUS5 LA9001P M/B	0.3

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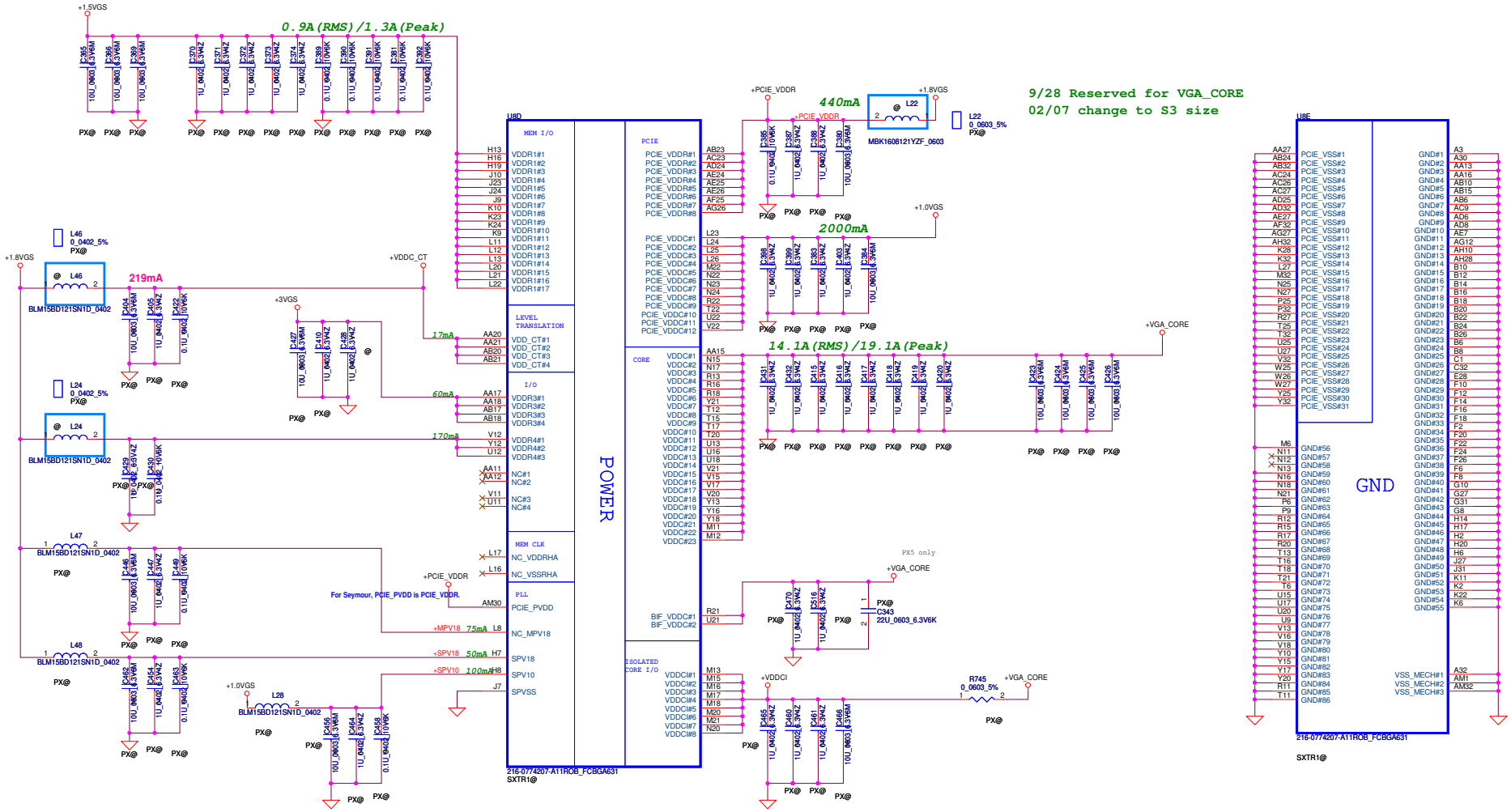

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Title: SeymourXT-S3 Power/GND

Size	Document Number	Rev
C	VAUS5 LA9001P M/B	0.3

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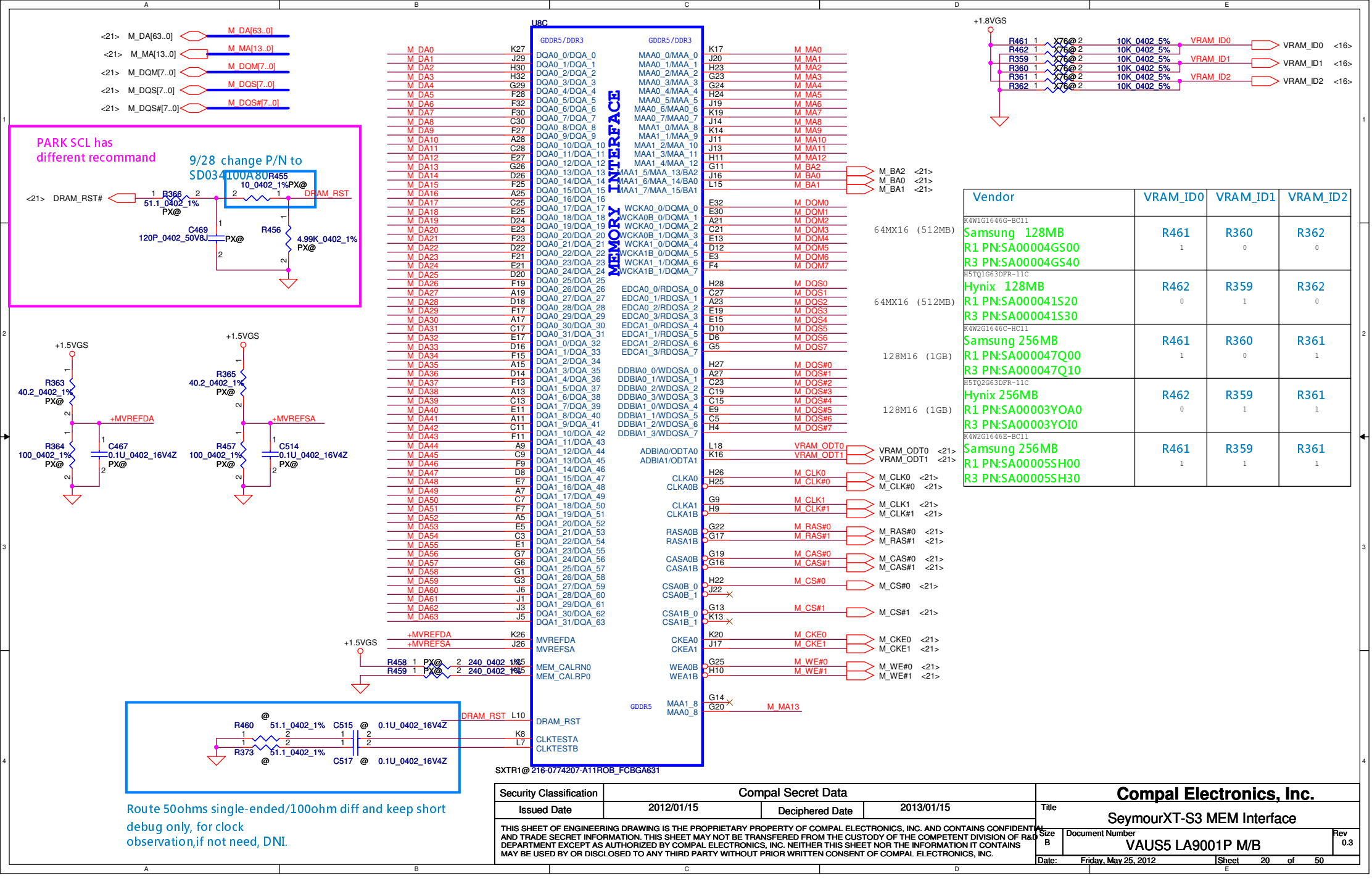


Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 64MX16 (512MB) Samsung 128MB R1 PN:SA00004GS00 R3 PN:SA00004GS40	R461 1	R360 0	R362 0
H5TQ1G63DFR-11C 64MX16 (512MB) Hynix 128MB R1 PN:SA000041S20 R3 PN:SA000041S30	R462 0	R359 1	R362 0
K4W2G1646C-HC11 128M16 (1GB) Samsung 256MB R1 PN:SA000047Q00 R3 PN:SA000047Q10	R461 1	R360 0	R361 1
H5TQ2G63DFR-11C 128M16 (1GB) Hynix 256MB R1 PN:SA00003YOA0 R3 PN:SA00003YOI0	R462 0	R359 1	R361 1
K4W2G1646E-BC11 Samsung 256MB R1 PN:SA00005SH00 R3 PN:SA00005SH30	R461 1	R359 1	R361 1

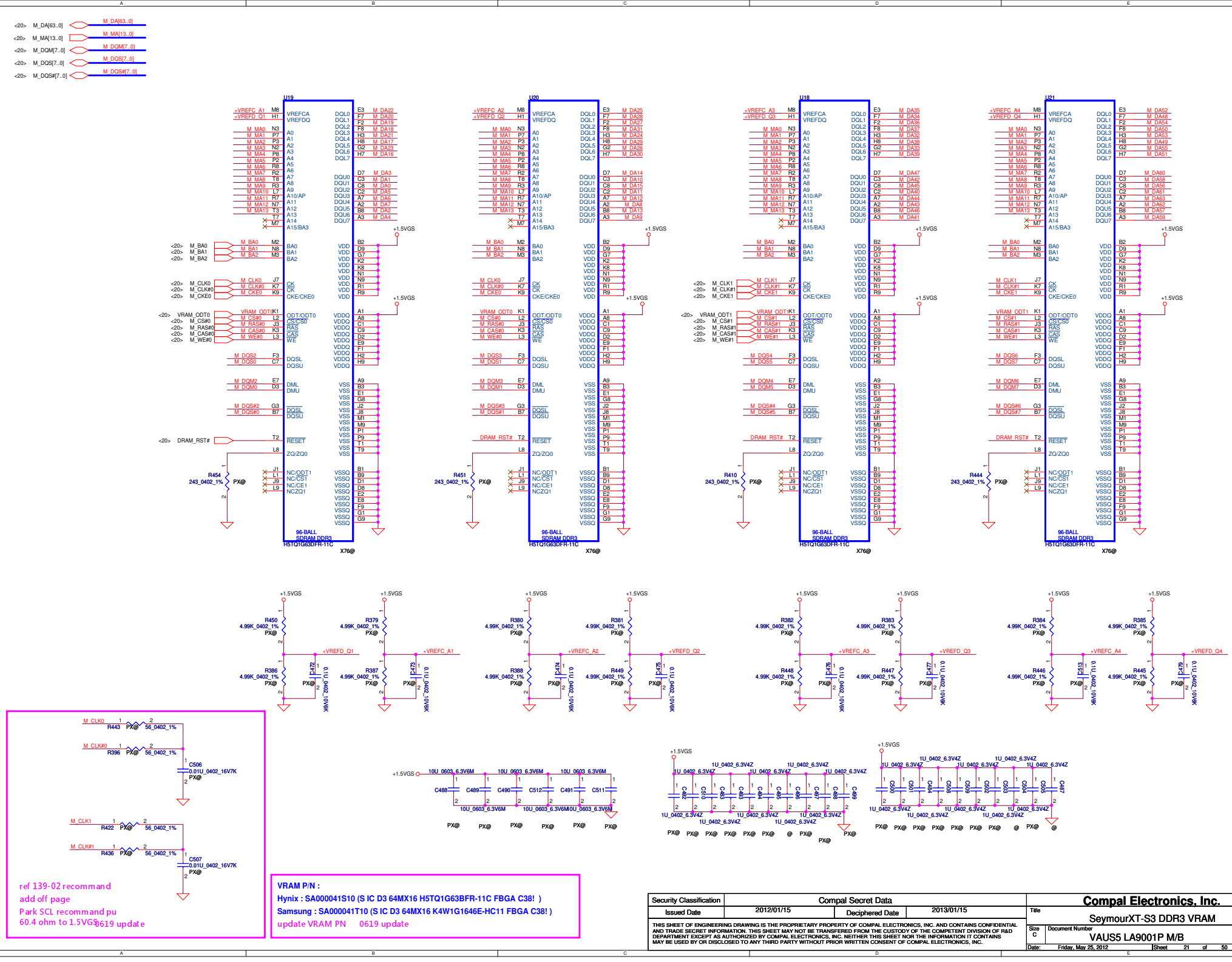
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: SeymourXT-S3 MEM Interface

Size: B | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

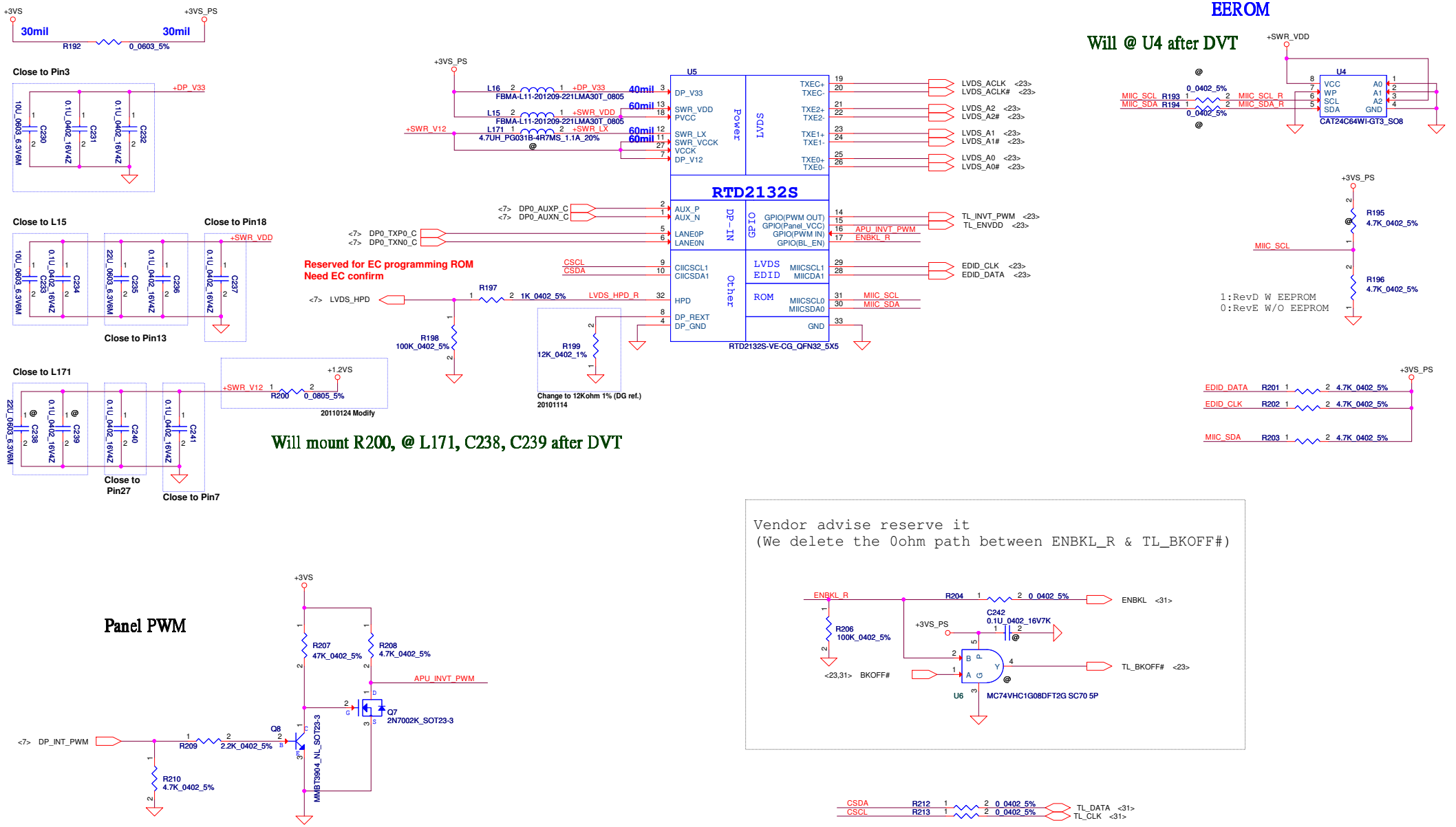
Date: Friday, May 25, 2012 | Sheet 20 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title	SeymourXT-S3 DDR3 VRAM		
Size C	Document Number VAUS5 LA9001P M/B		Rev 0.3
Date: Friday, May 25, 2012		Sheet 21 of 50	



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

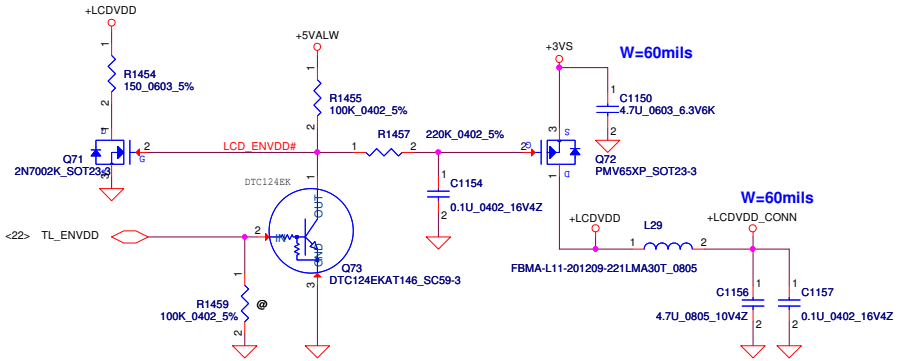
Compal Electronics, Inc.

Title: LVDS Translator - RTD2132S

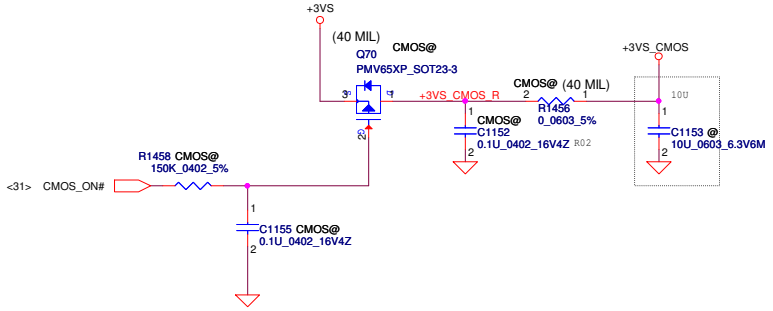
Size	Document Number	Rev
Custom	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 22 of 50

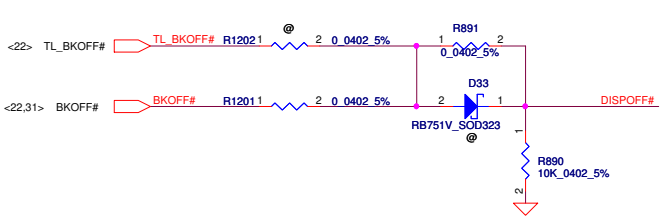
LCD POWER CIRCUIT

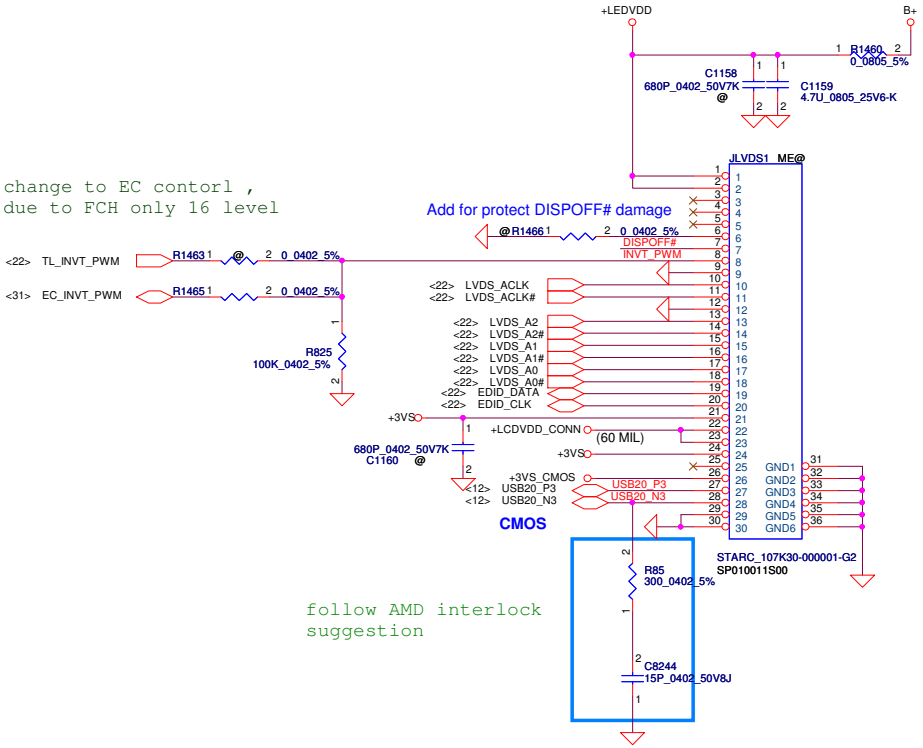


CMOS Camera



VGA LCD/PANEL BD. Conn.





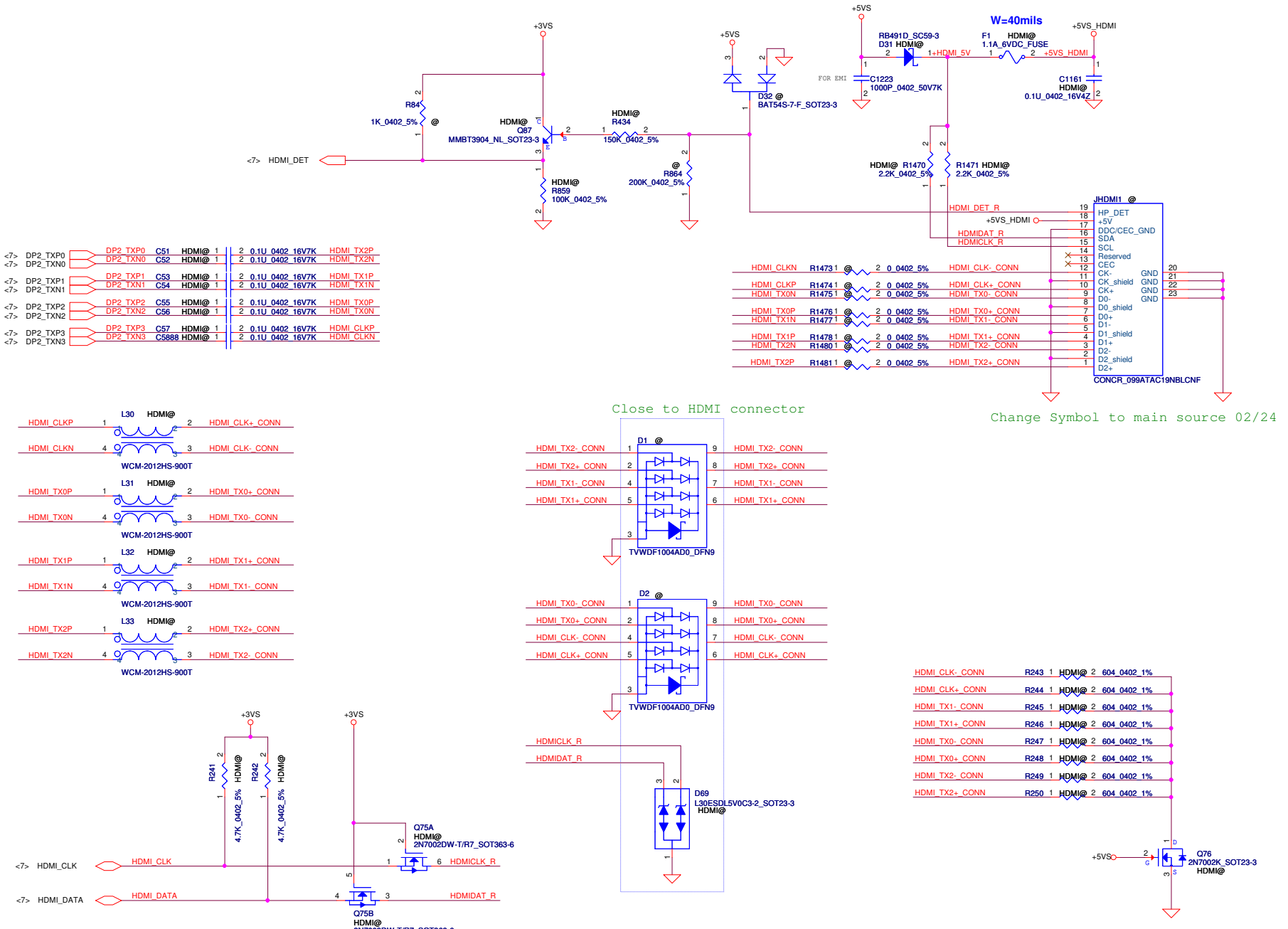
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: LVDS/CAMERA

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

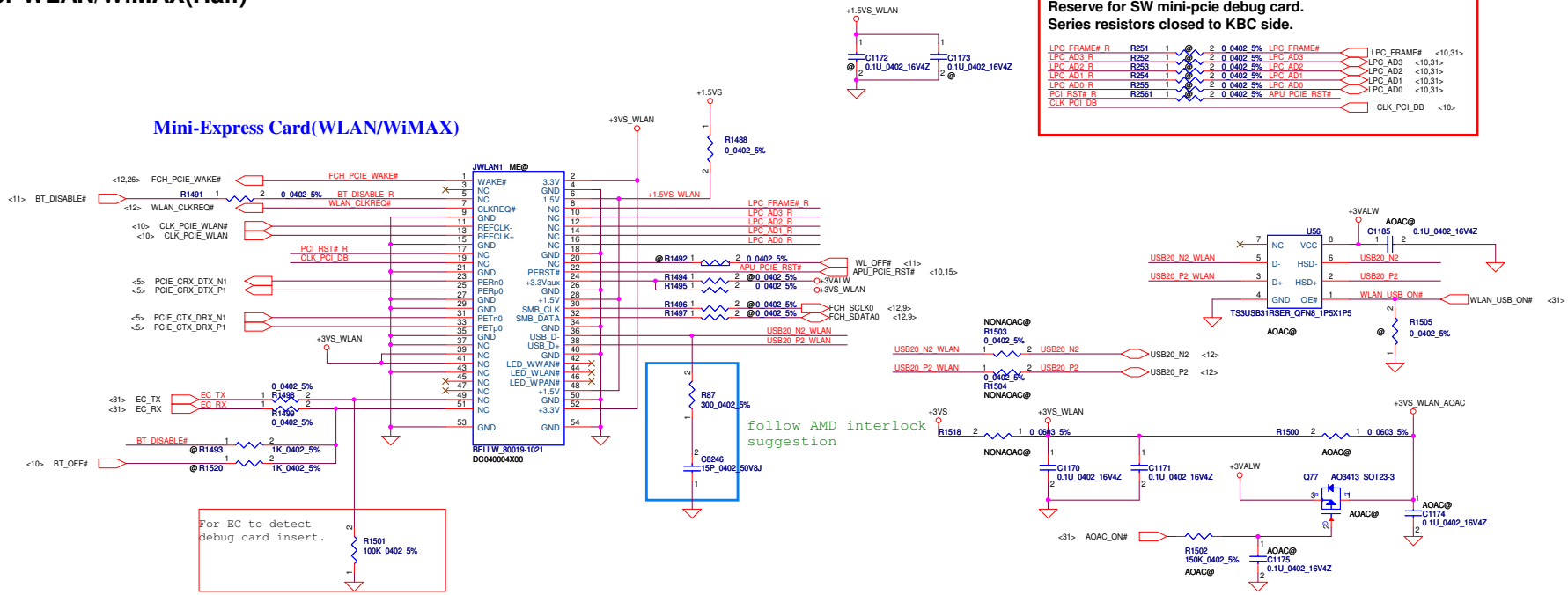
Date: Thursday, May 31, 2012 | Sheet 23 of 50



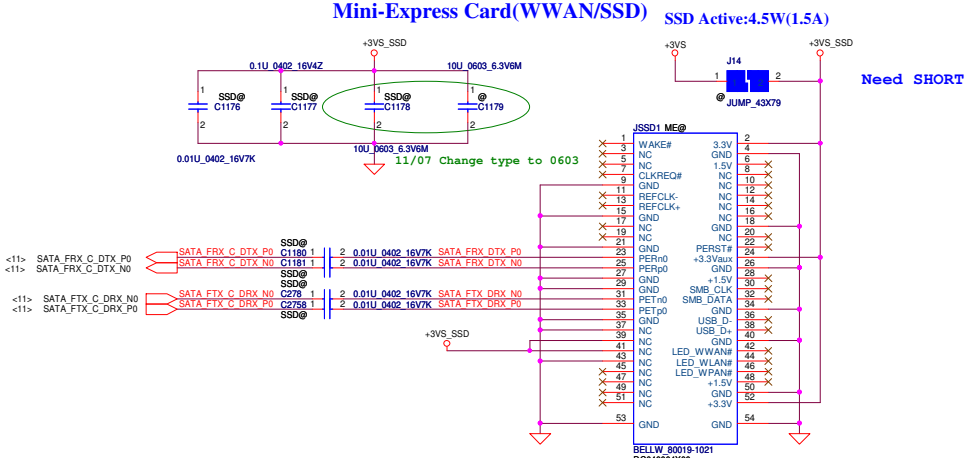
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics,Ltd.			
Title: HDMI CONN			
Size: B (5/5 Custom)	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
Date: Friday, May 25, 2012	Sheet 24 of 50		

Mini-Express Card for WLAN/WiMAX(Half)



Mini-Express Card for SSD(Full)



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.	
Title	Mini-Card
Size	Document Number: VAUS5 LA9001P M/B
Rev	0.3
Date:	Thursday, May 31, 2012
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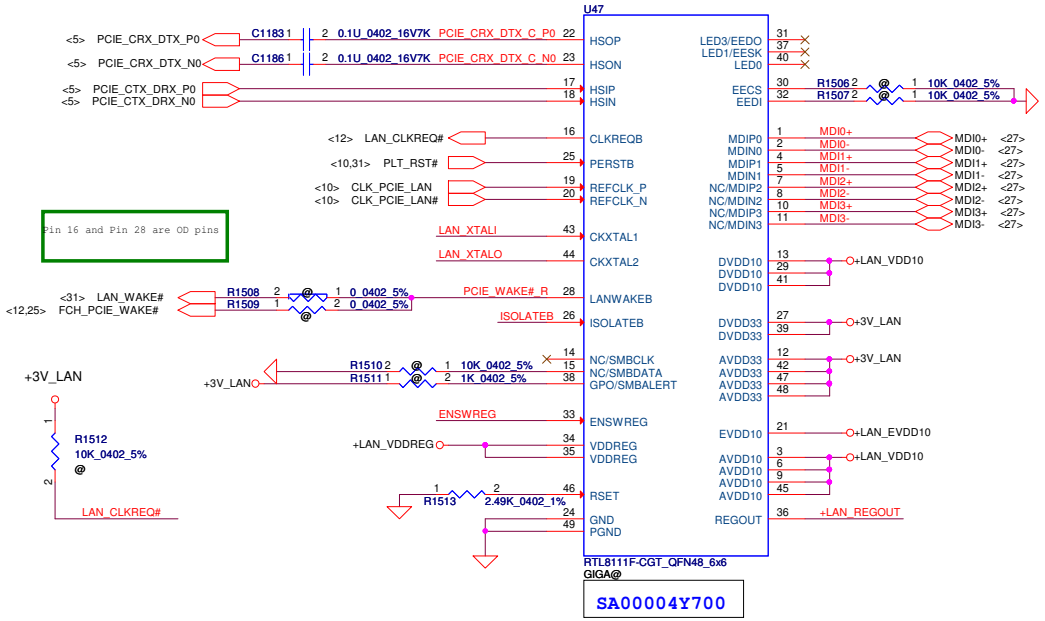
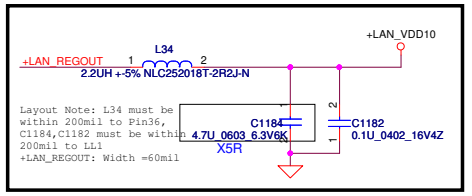
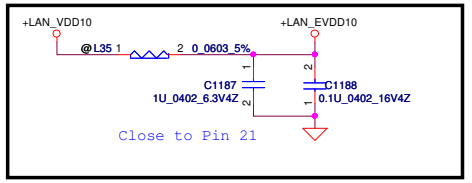
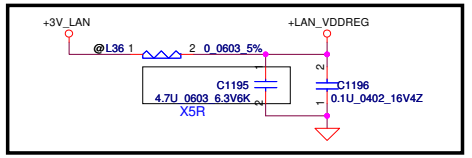
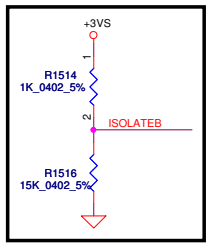
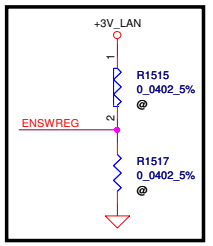




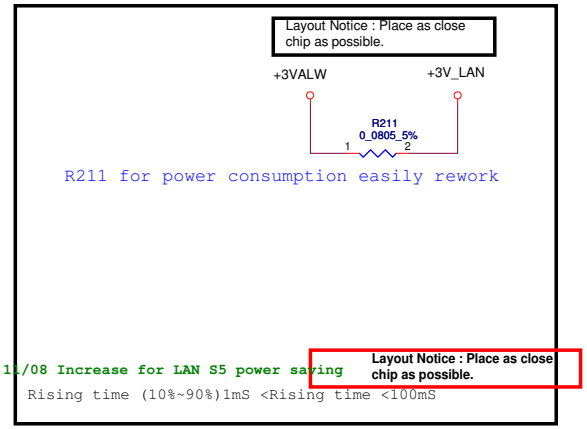


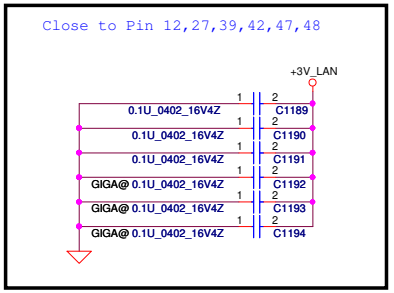


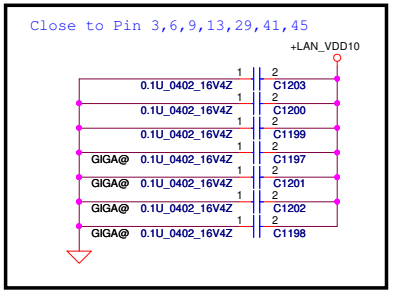




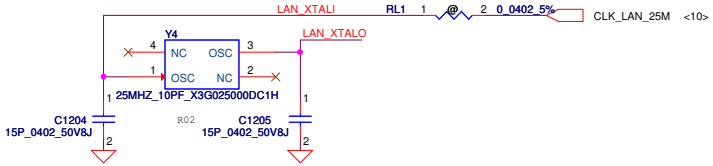
H: Enable internal Regular
L: Disable







Follow Vendor tunning value



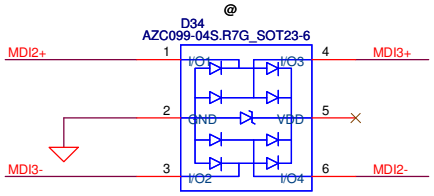
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

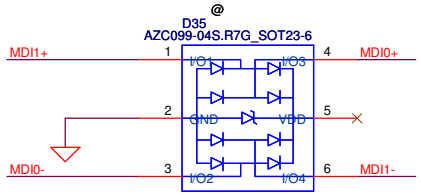
Title: LAN-RTL8111F/8105E

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Tuesday, May 29, 2012 | Sheet 26 of 50



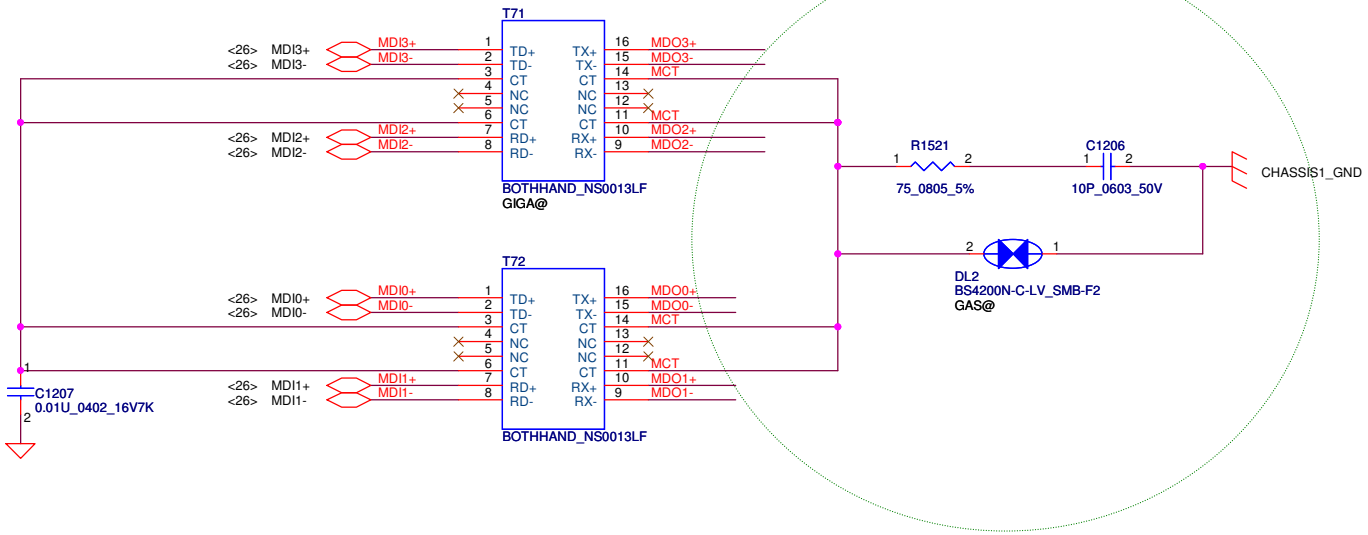
Place Close to T71



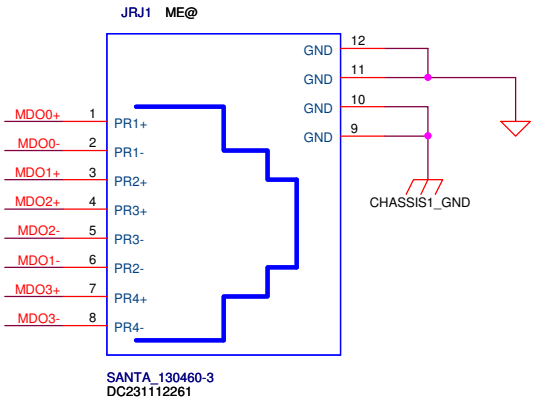
Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

Reserve gas tube for EMI go rural solution



Place Close to T71,T72



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

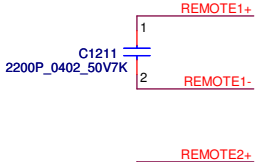
Compal Electronics, Inc.

Title: LAN_Transformer

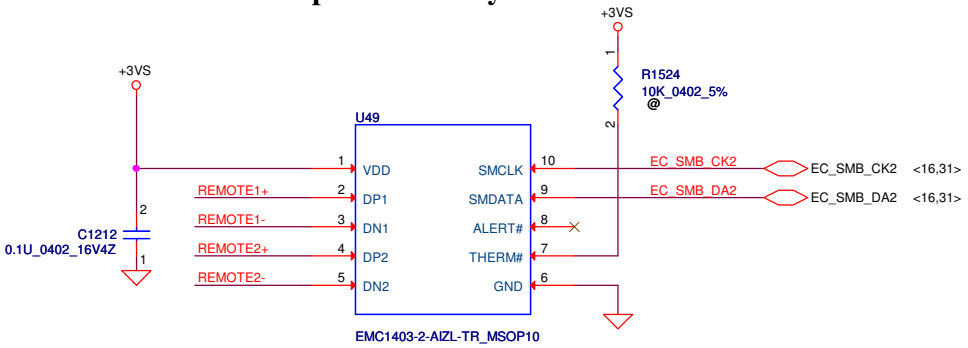
Size: B | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 27 of 50

Close U49

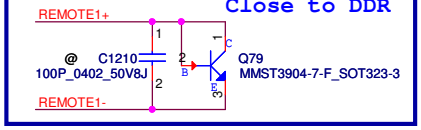


SMSC thermal sensor placed near by VRAM

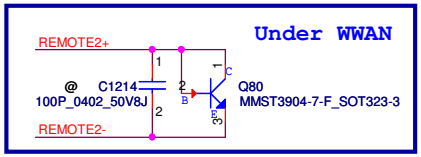


Address 1001_101xb

Close to DDR

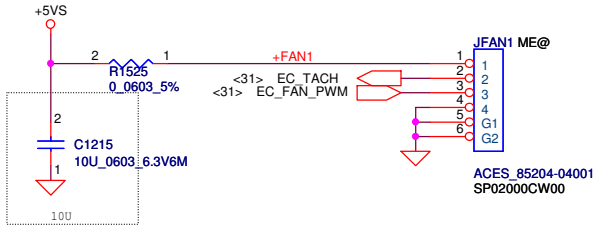


Under WWAN

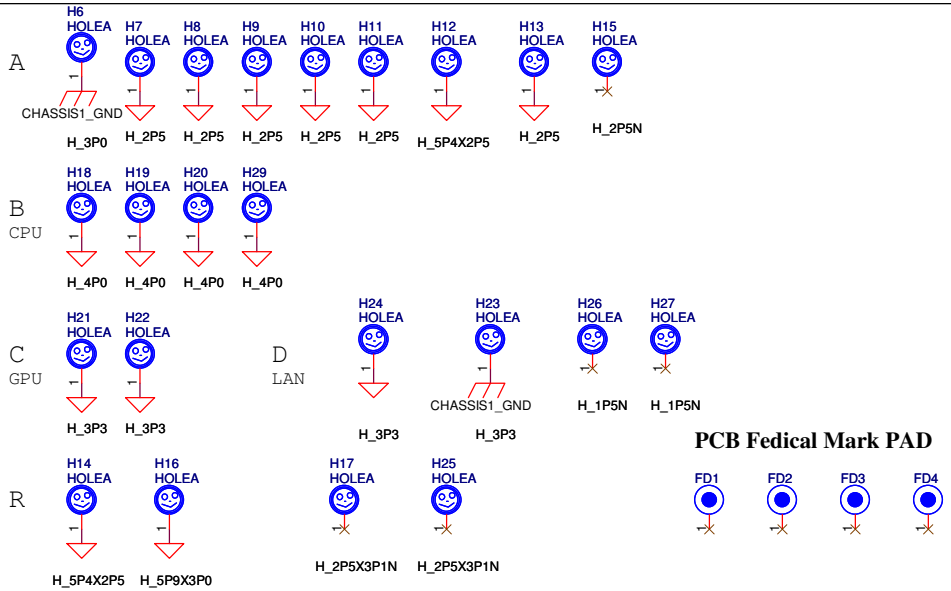


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Screw Hole



PCB Fedical Mark PAD

Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

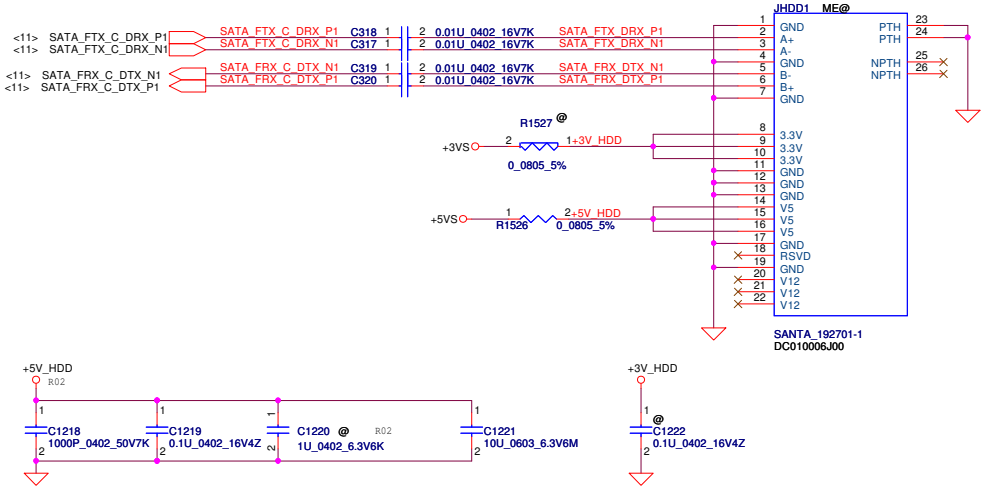
Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

Size: B | Document Number: **VAUS5 LA9001P M/B** | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 28 of 50

SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: HDD Connector

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 29 of 50

600ohms @100MHz 1A
P/N: SM01000BU00

600ohms @100MHz 2A
P/N: SM01000EE00

Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

U50

S IC ALC259-VC2-CG MQFN 48P CODEC

Vendor recommend. 2.2K

Vendor recommend. 2.2u

external MIC

Internal Speaker

Headphone

MIC Sense
R939 place near pin13

Capless HP Sense
R940 place near pin34

0525 EMI request to add C83 and C84.
Close to U50 Audio IC

Place near Pin25

Place near Pin38

Place near Pin1

Place near Pin9

Place next to pin 27

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

wide 25MIL

Reserve for ESD request.

Combo Jack detect (normal open)

PC Beep

EMI

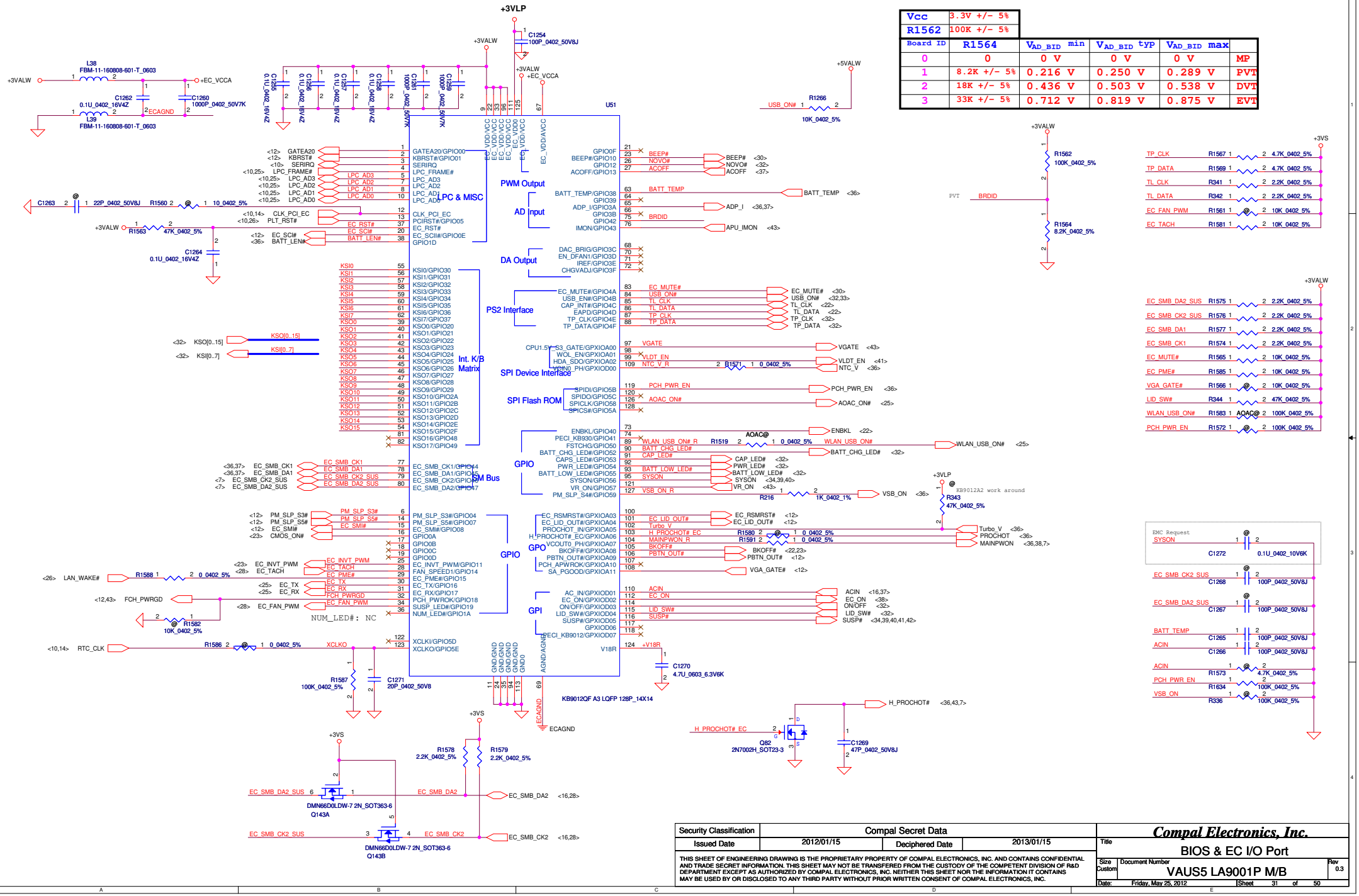
Security Classification	Compal Secret Data	
Issued Date	2012/01/15	Deciphered Date 2013/01/15

Compal Electronics,Ltd.

Title: HD Audio Codec_ALC269Q-VC

Size: C | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 30 of 50


+3VLP
U51
KB9012QF A3 LQFP 128P_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
SM Bus
Vcc 3.3V +/- 5%
R1562 100K +/- 5%
Board ID | R1564 | VAD_BID min | VAD_BID typ | VAD_BID max
0 | 0 | 0 V | 0 V | 0 V | MP
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | PVT
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | DVT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | EVT
Security Classification | Compal Secret Data
Issued Date | 2012/01/15 | Deciphered Date | 2013/01/15
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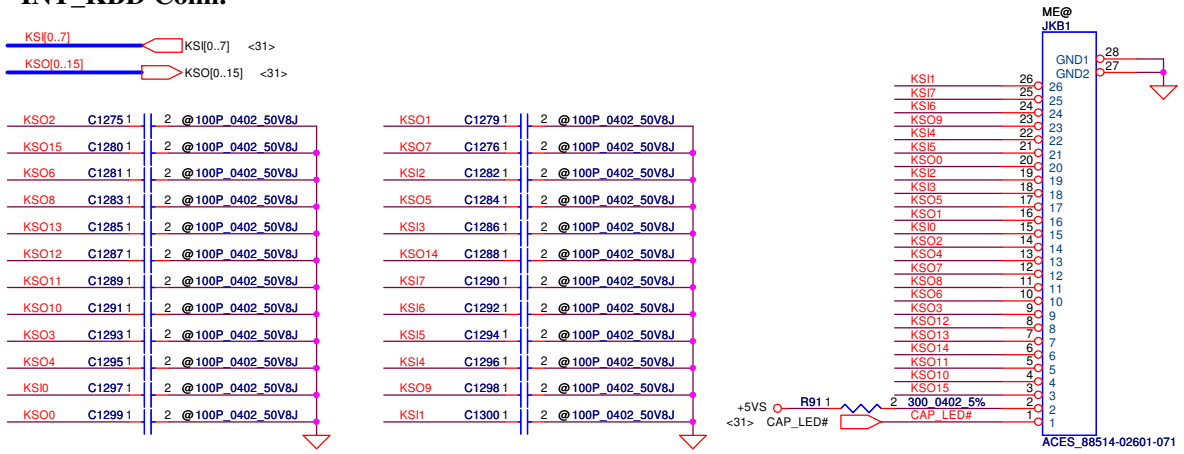
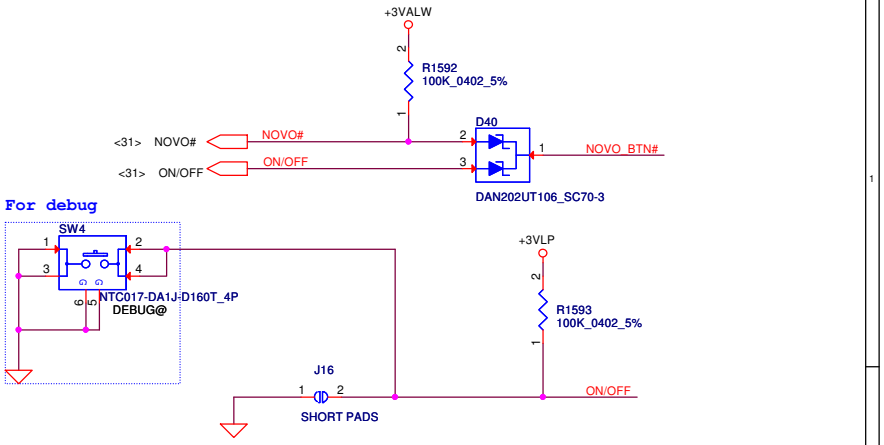
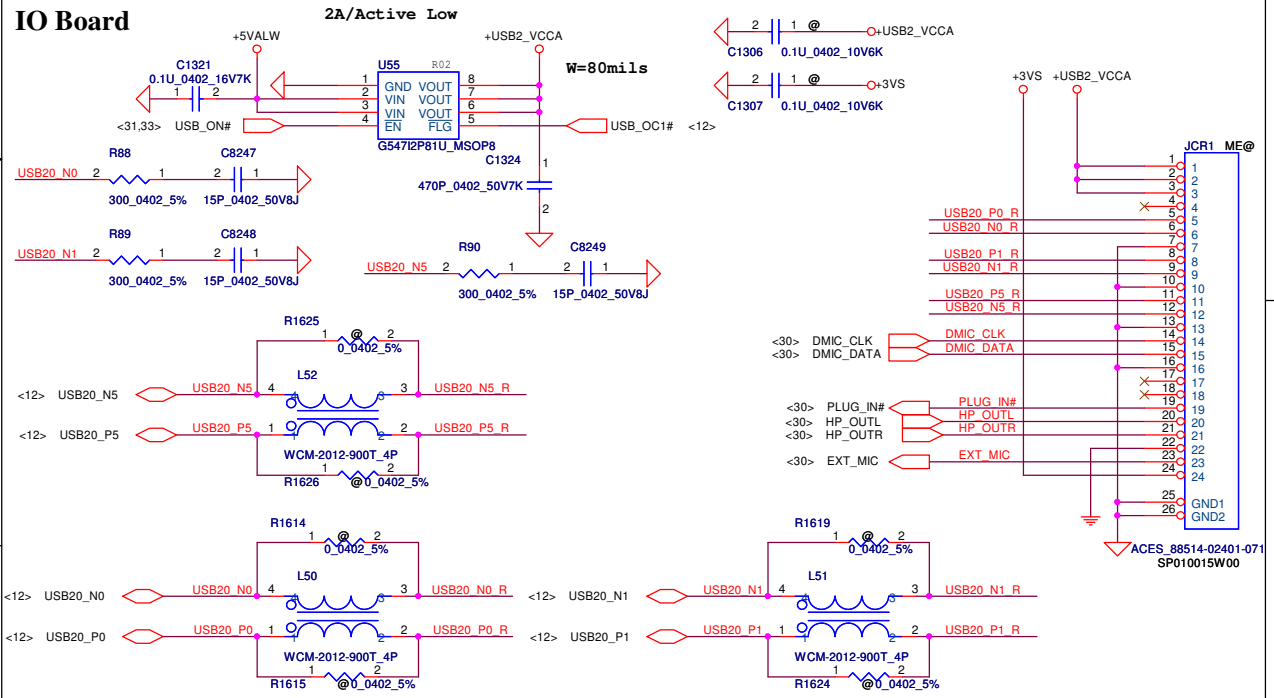
Compal Electronics, Inc.
Title: BIOS & EC I/O Port
Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3
Date: Friday, May 25, 2012 | Sheet 31 of 50

INT_KBD Conn.

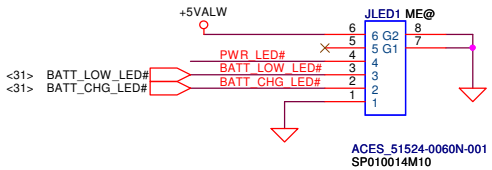




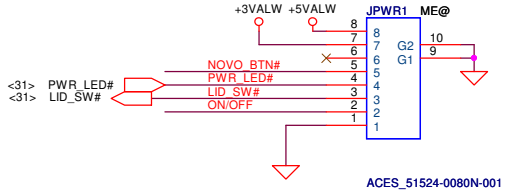
IO Board



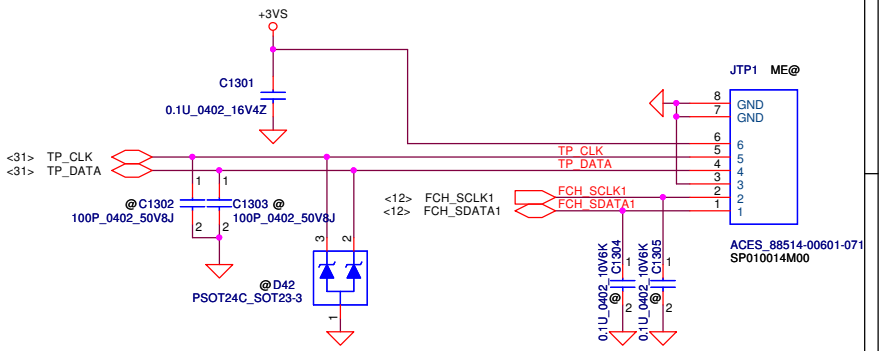
LED Board



Power Board

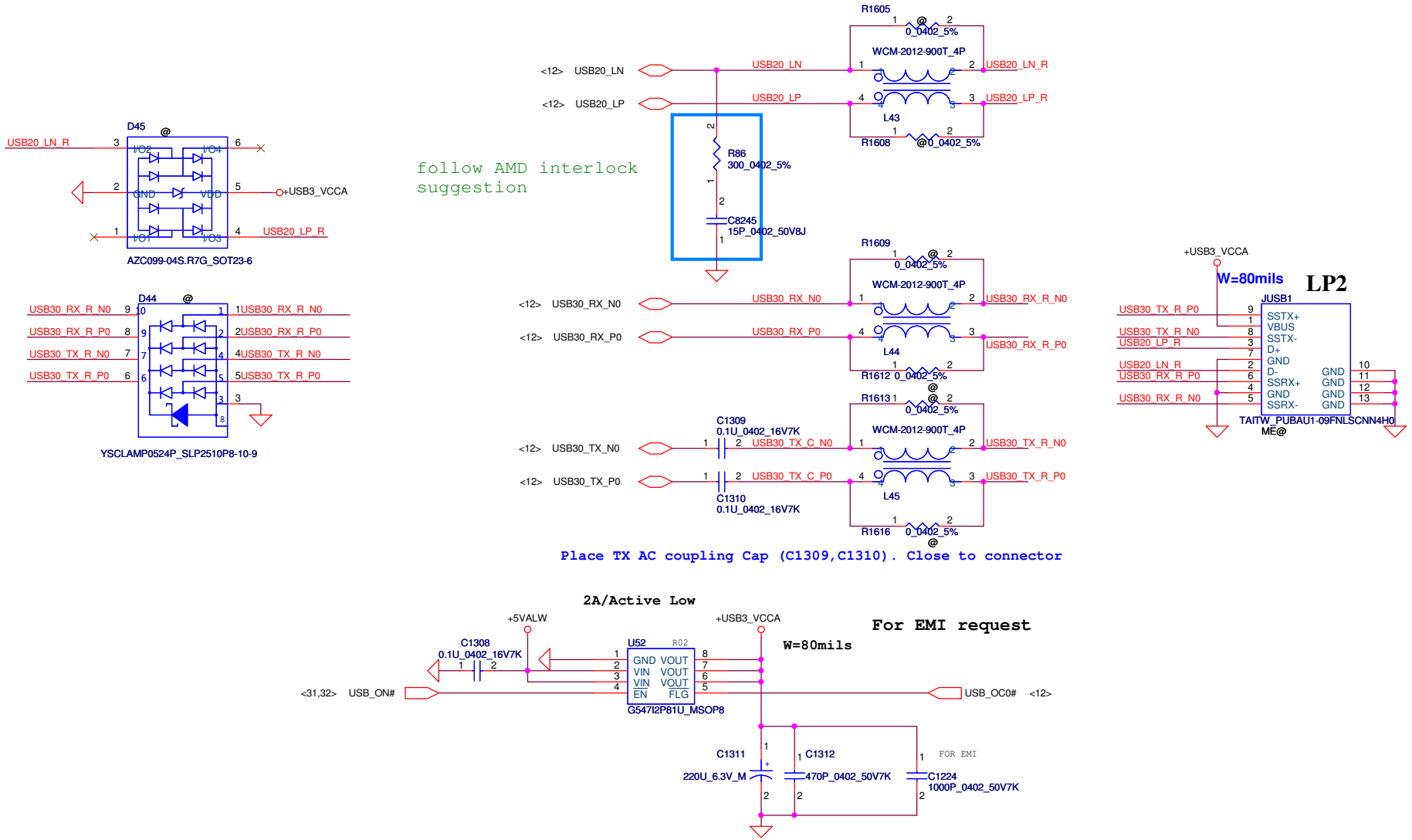


TouchPAD Module



Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

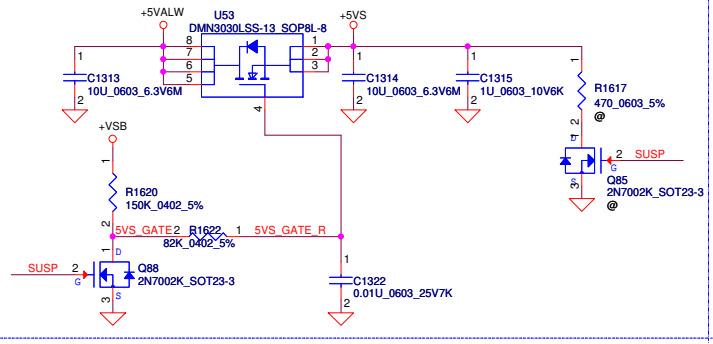
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
Date: Thursday, May 31, 2012	Sheet 32 of 50		



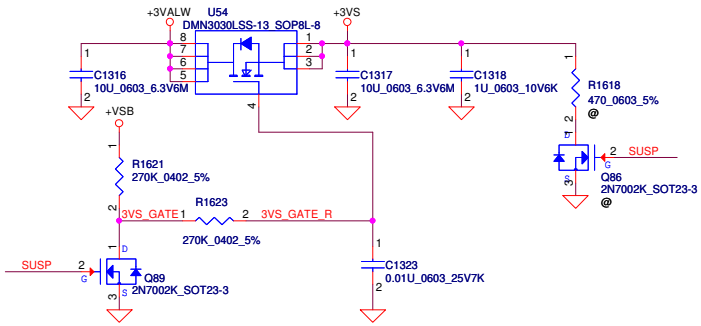
Security Classification	Compal Secret Data For EMI request		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.			
Title: USB3.0 ports			
Size: Custom	Document Number: VAUS5 LA9001P M/B		Rev: 0.3
Date: Thursday, May 31, 2012	Sheet 33 of 50		

+5VALW TO +5VS

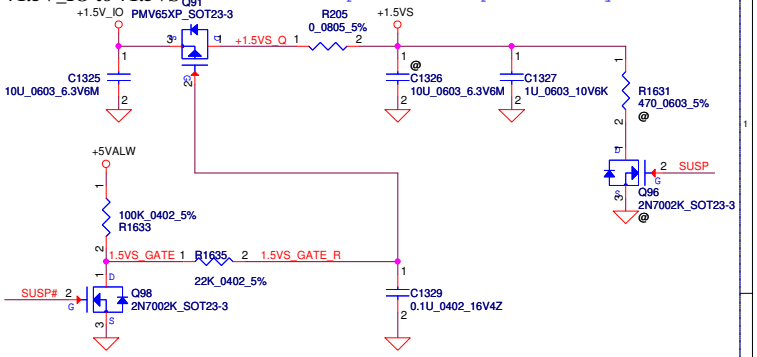


+3VALW TO +3VS

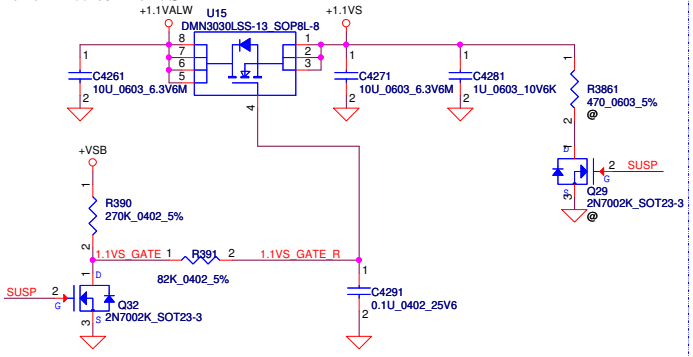


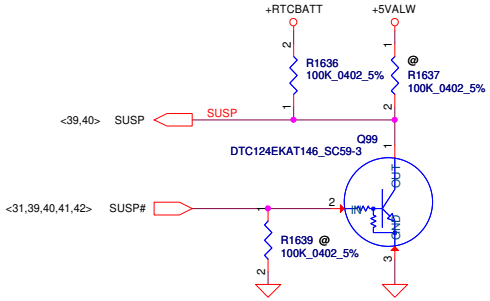
+1.5V_IO to +1.5VS

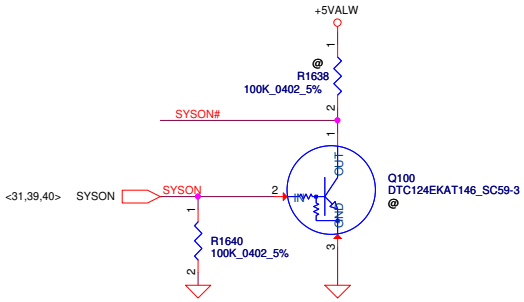
R205 for power consumption easily rework

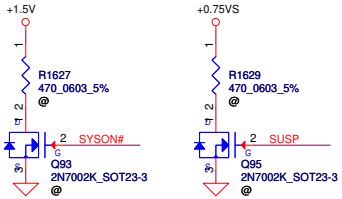


+1.1VALW to +1.1VS









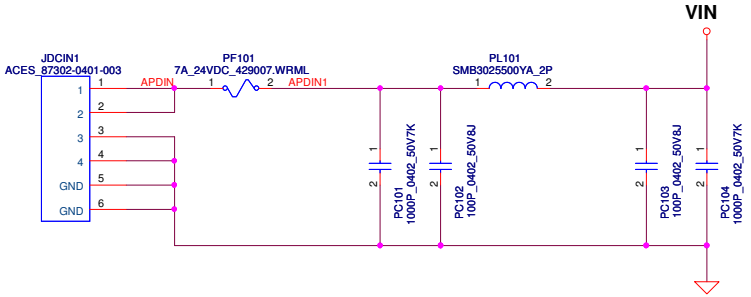
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

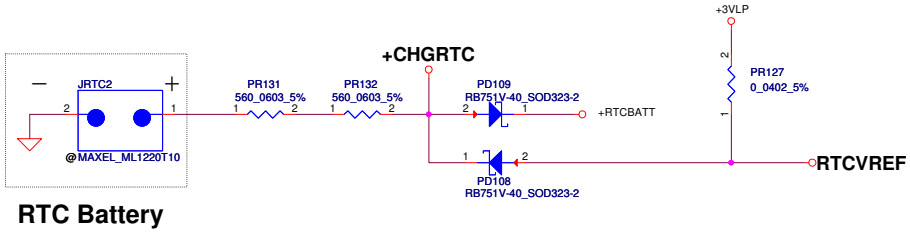
Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size	Document Number	Rev
Custom	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 34 of 50





RTC Battery

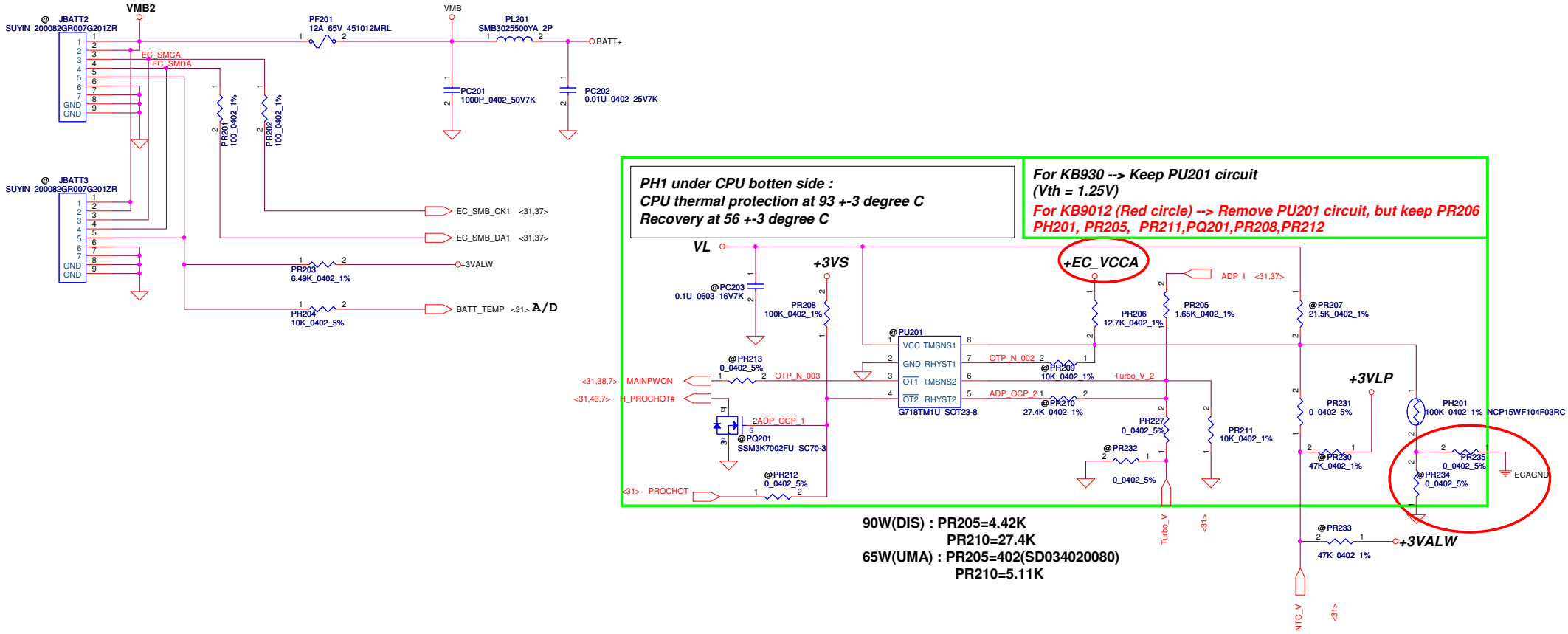
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR DCIN / Vin Detector /Pre-charge

Size: Custom | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 35 of 48



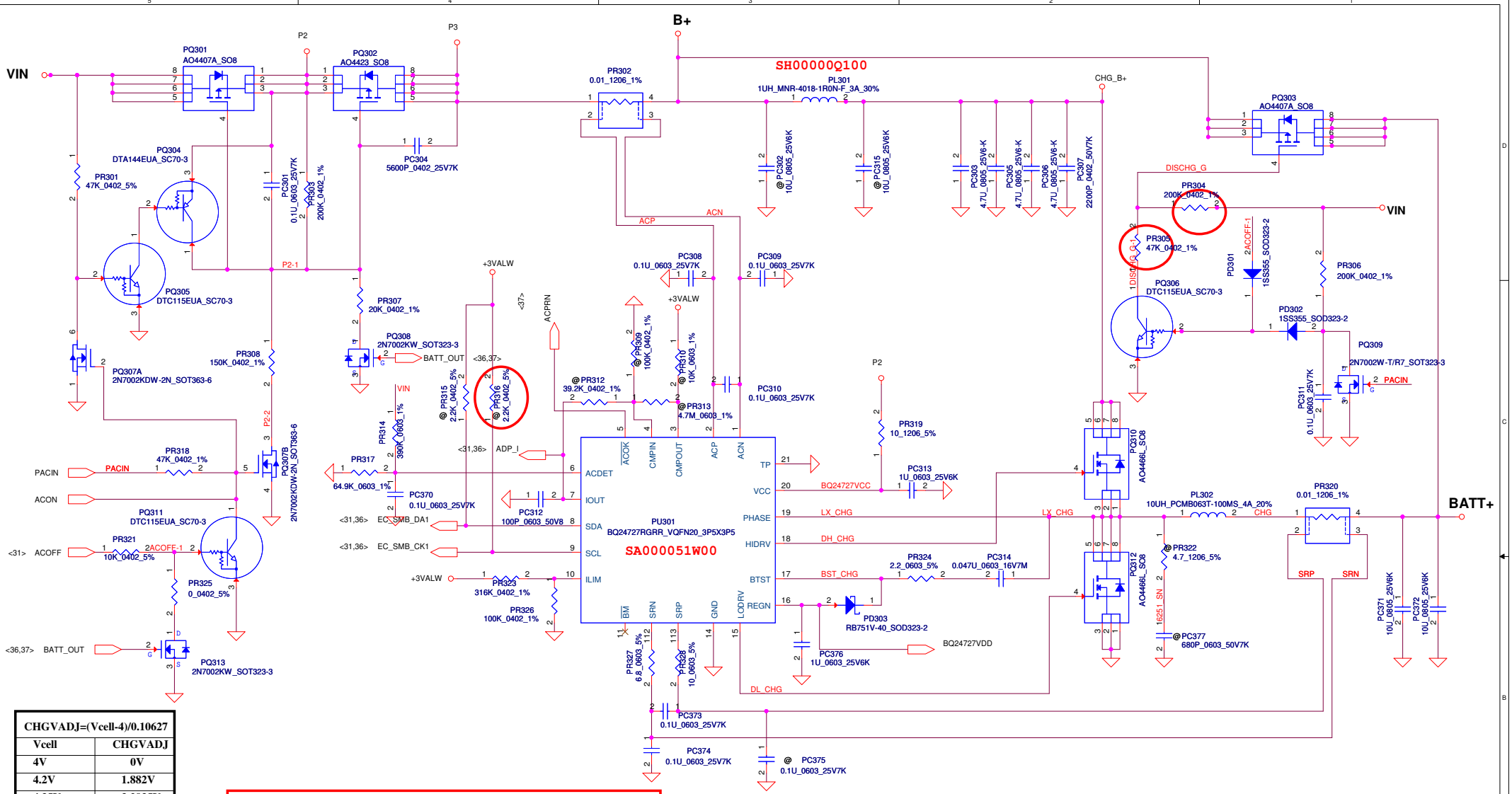
Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
Custom	LA9001P	0.1

Date: Friday, May 25, 2012 Sheet 36 of 48



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

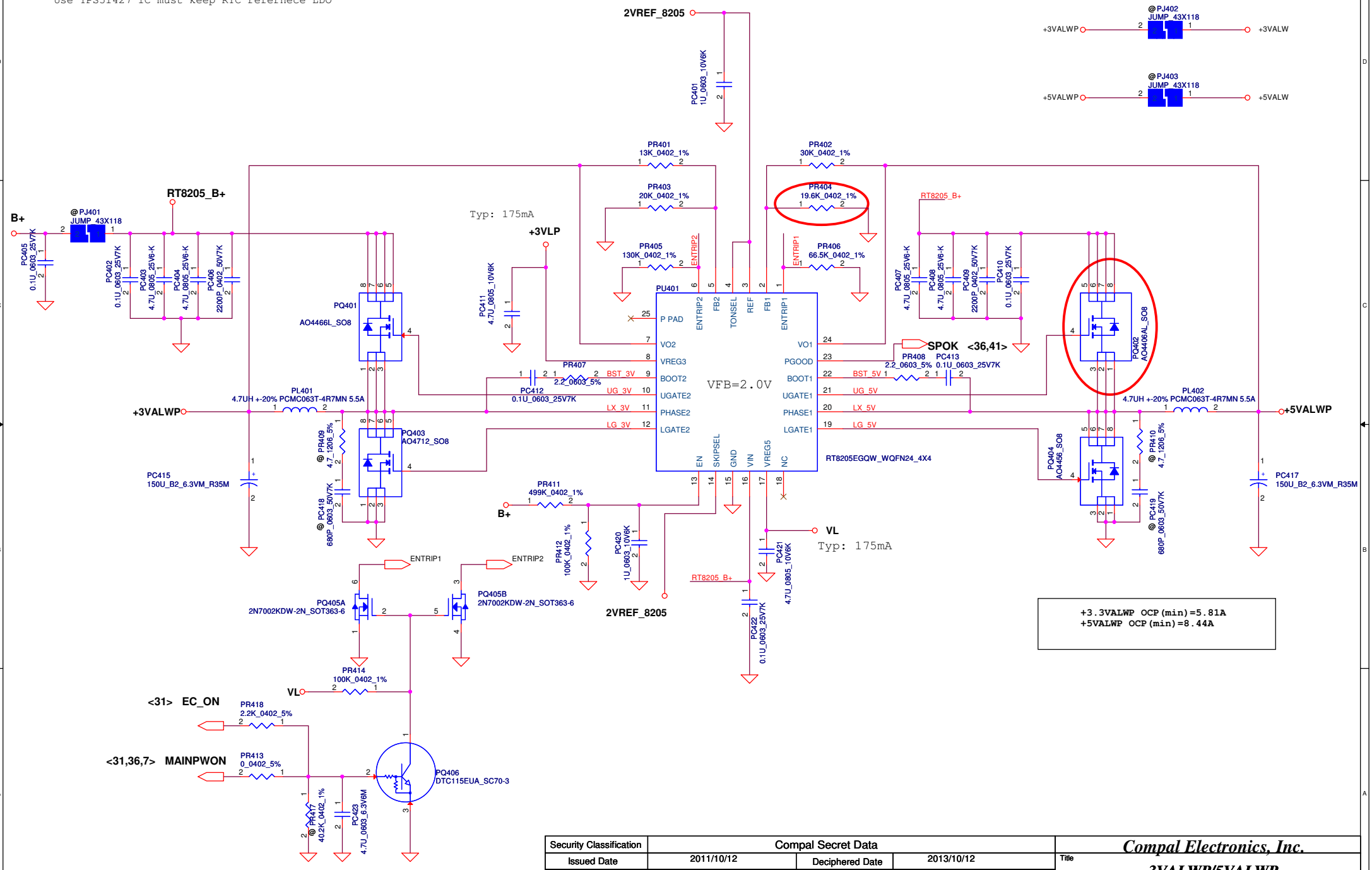
Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 37 of 48

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

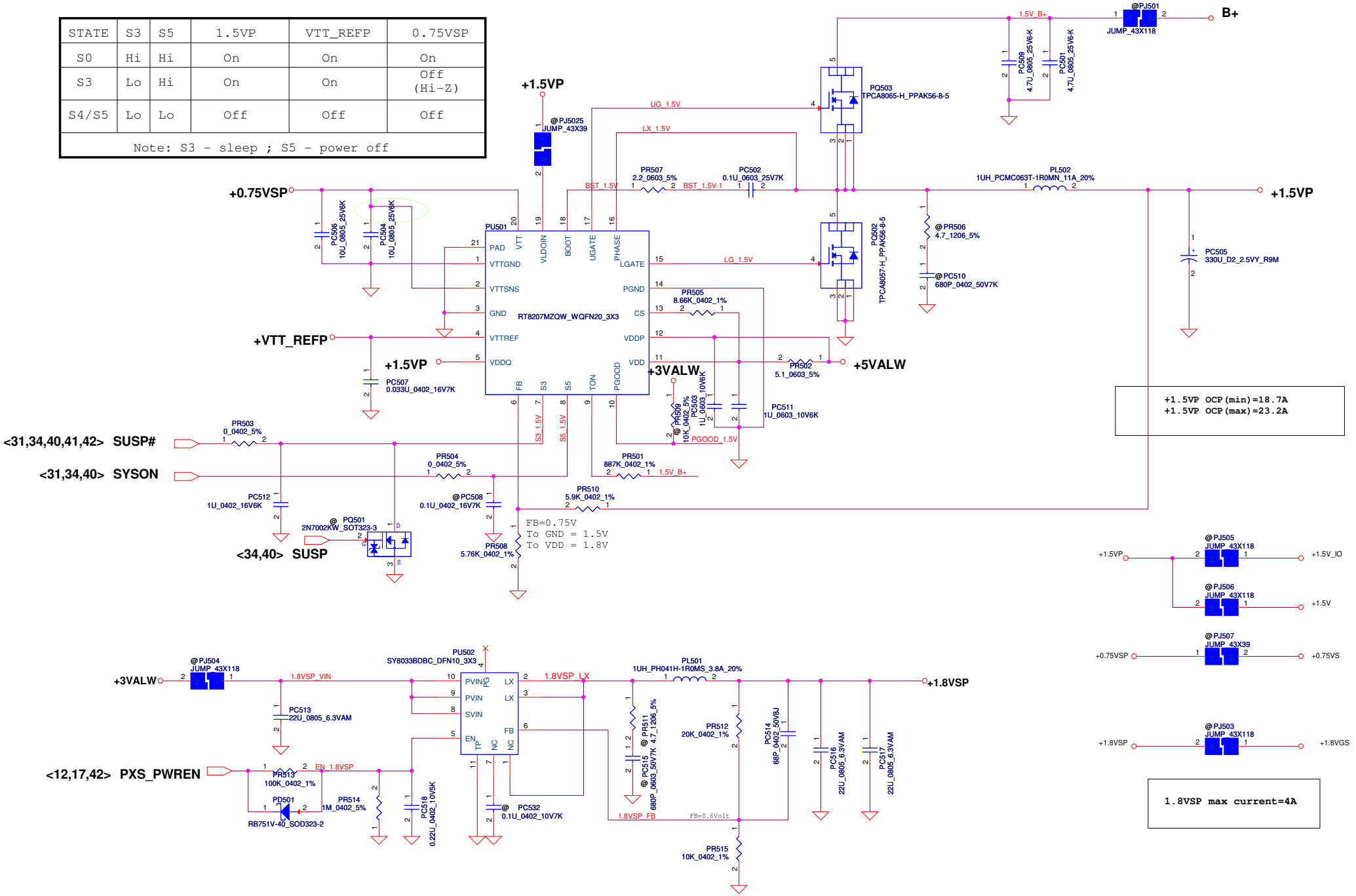
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	LA9001P	0.1

Date: Friday, May 25, 2012 Sheet 38 of 48

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

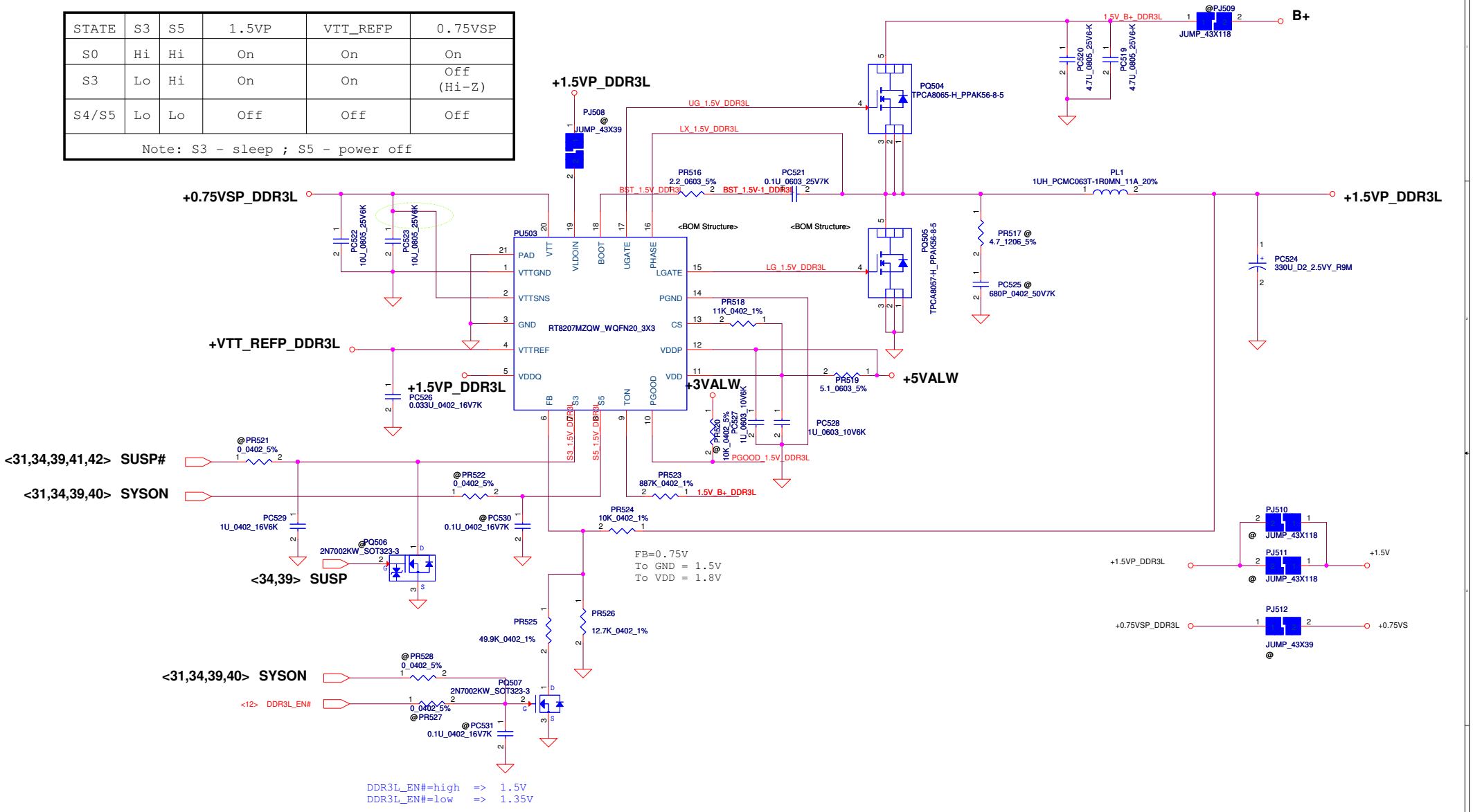
Compal Electronics, Inc.

Title: PWR-+1.5VP/+0.75VSP/+1.8VSP

Size: Custom | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 39 of 48

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



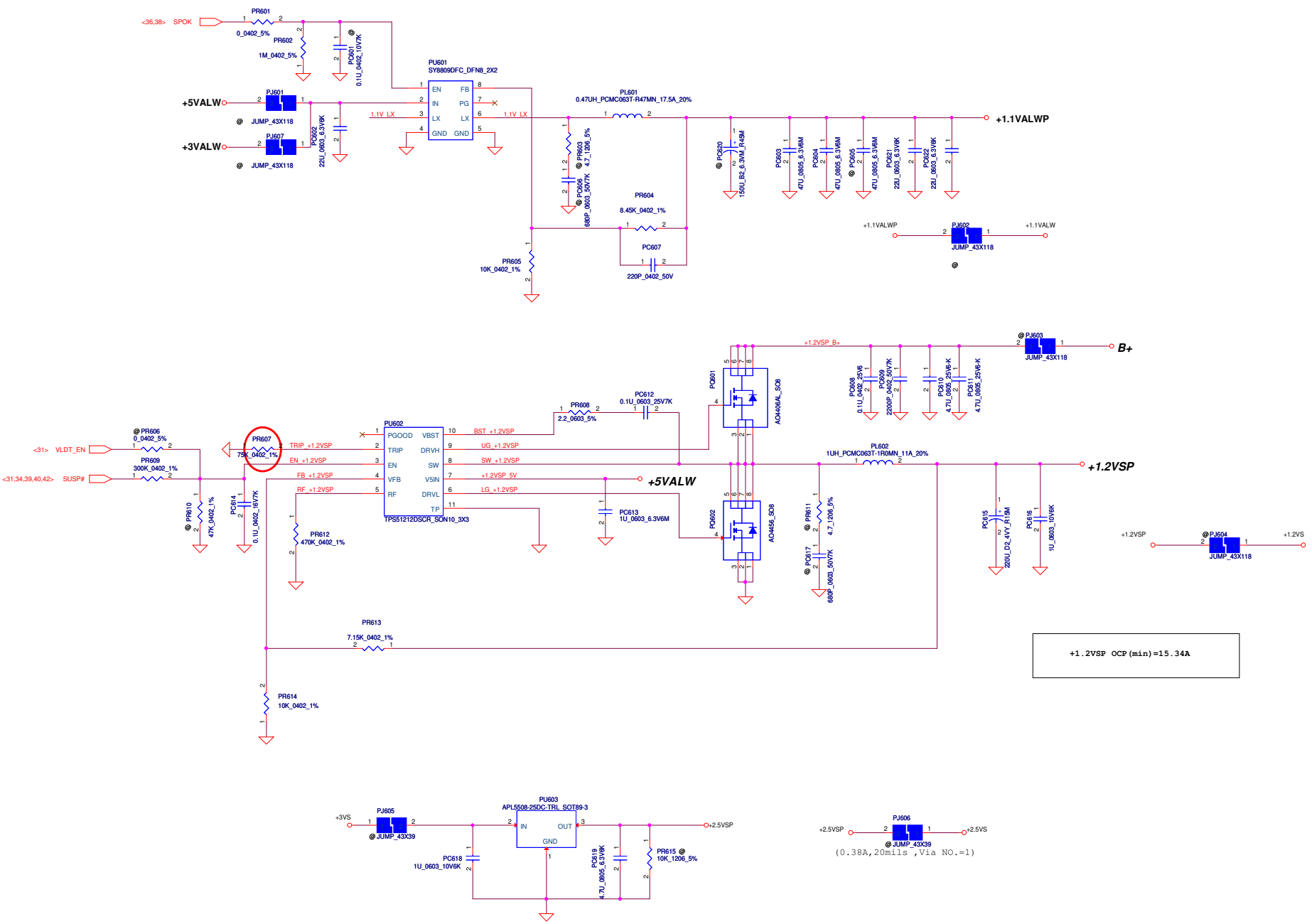
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size	Document Number	Rev
Custom	LA9001P	0.1

Date: Friday, May 25, 2012 Sheet 40 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR +1.1VALWP/+1.2VSP/+2.5VSP

Size	Document Number	Rev
C	LA9001P	0.1

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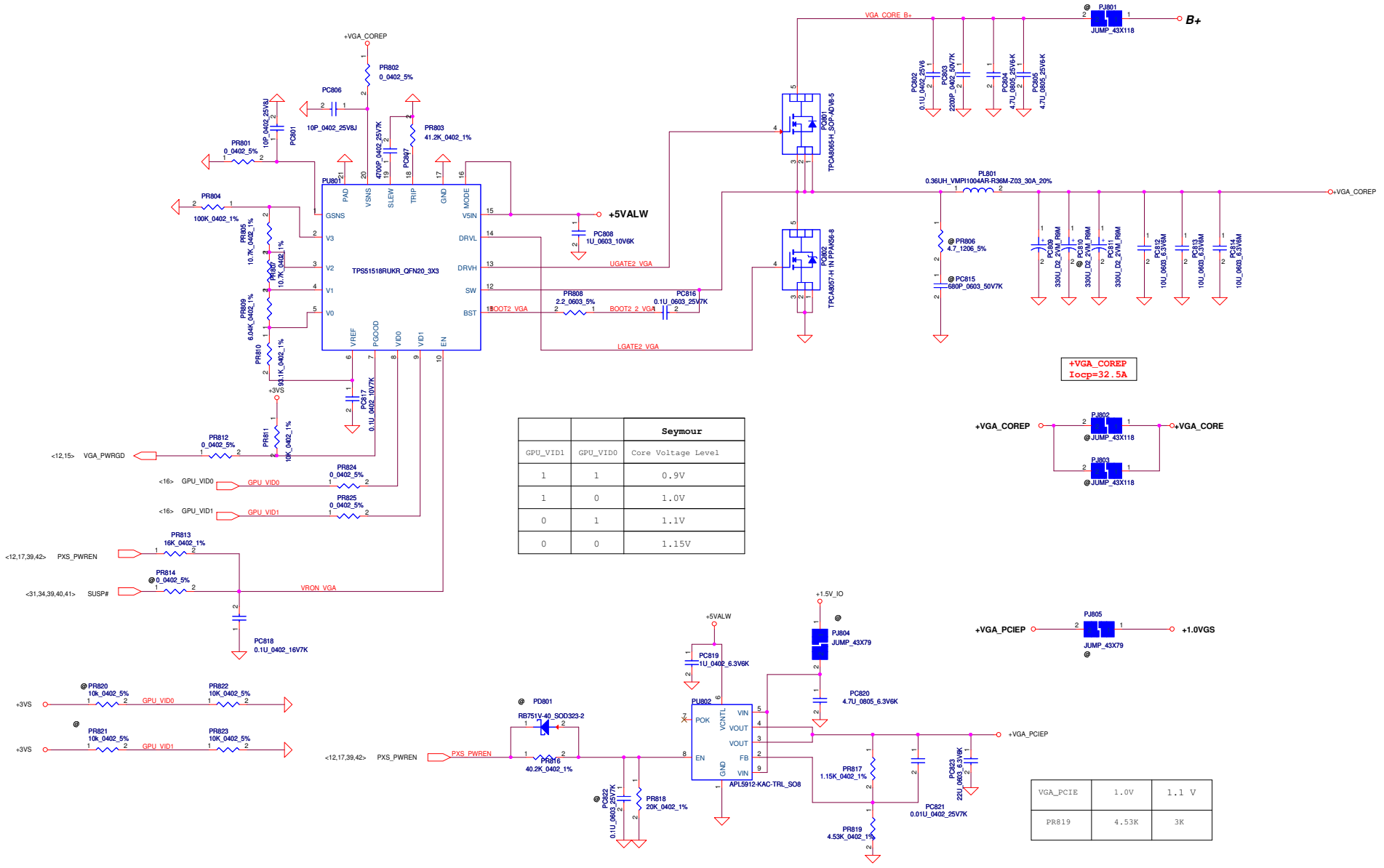


		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

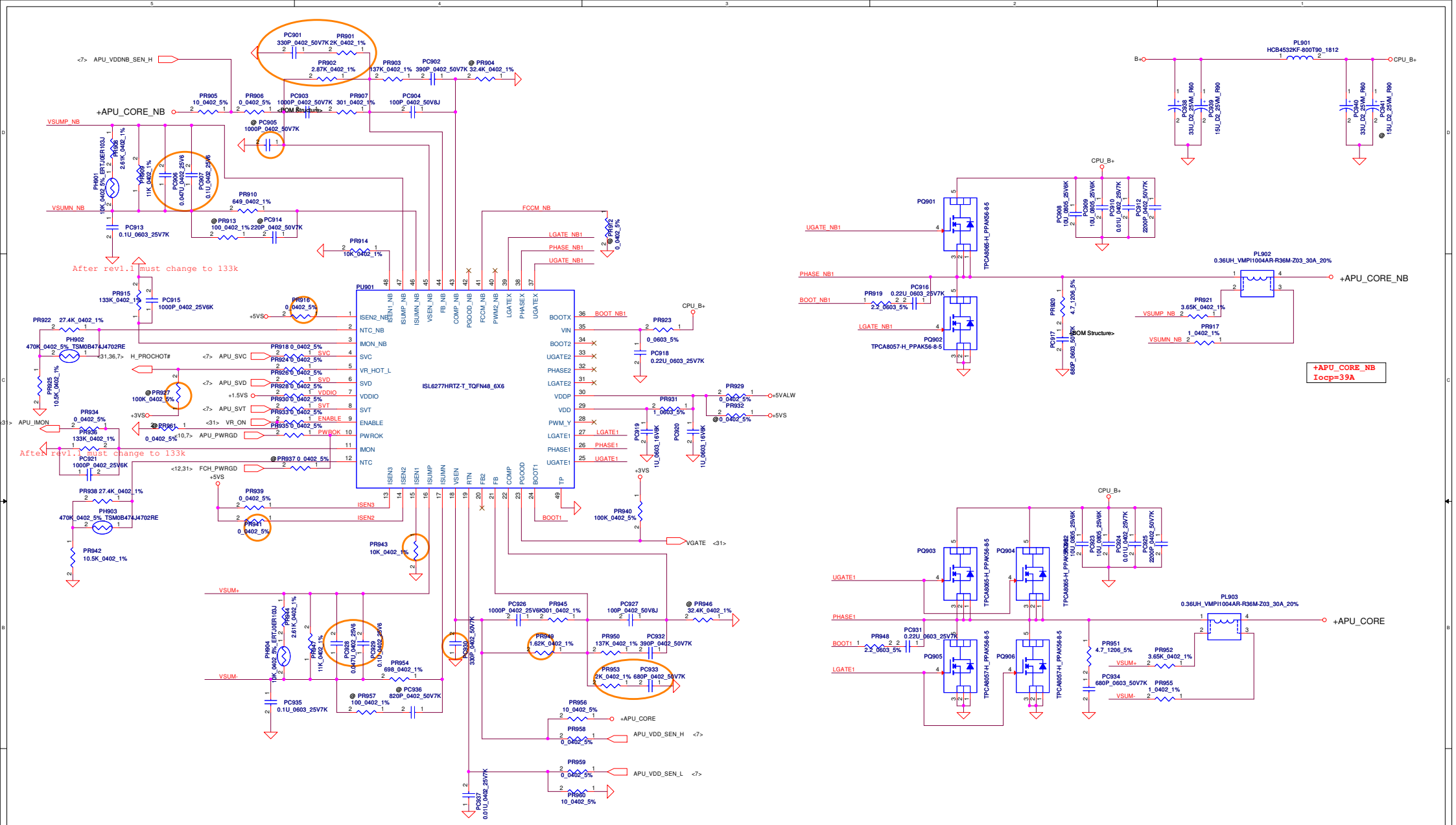
VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

Compal Electronics, Inc.

Title: PWR-VGA_CORE/VGA_PCIE

Size | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 42 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR-CPU_CORE/CPU_CORE_NB

Size	Document Number	Rev
Custom	LA9001P	0.1

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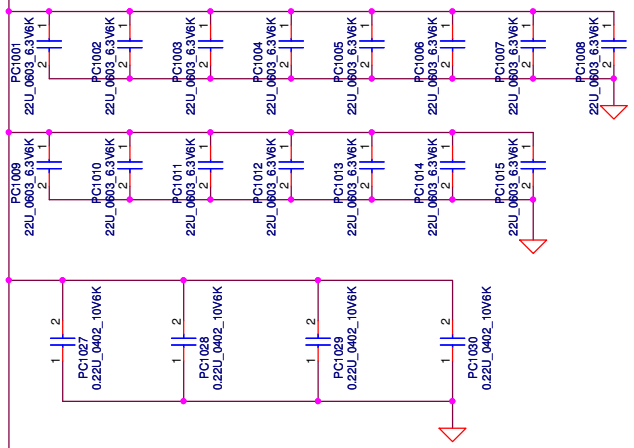
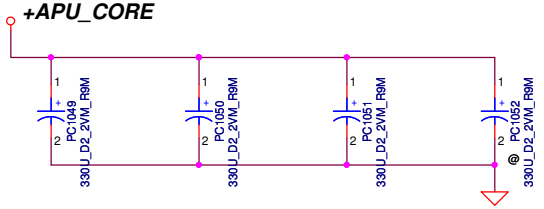
+CPU_CORE

+APU_CORE

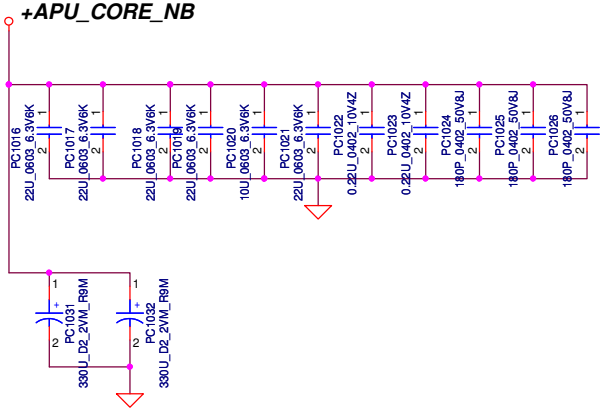


+APU_CORE

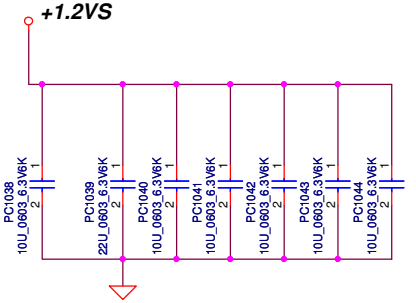


+CPU_CORE_NB

+APU_CORE_NB



+1.2VS



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 44 of 48

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: LA9001P | Rev: 0.1

Date: Friday, May 25, 2012 | Sheet 45 of 48

VAUS5 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	SDV TO SIV NOTE
1	3/22	26	Change C1204, C1205 from SE071120JN0 to SE071120J80	SE071120JN0 is for A58 only	
2	3/22	27	Modify DL2 from @ to GAS@	For Gastube BOM control	
3	3/22	12	Delete FCH_SEL BOM control	AMD formal announce FP2 only support A70M3	
4	3/22	10	Delete U2 A60MR1 BOM control	AMD formal announce FP2 only support A70M3	
5	3/22	12	Change R117 from PX@ to @, change R155 from @ to always mount	Clock request from GPU will not meet power sequence	
6	3/22	12	Change R1606, R1607 from USBL2@ to @, change R1610, R1611 from USBL3@ to always mount	AMD formal announce FP2 only support A70M3	
7	3/26	10	Change GPIO31 pull high from +3VALW to +3VS	This GPIO pin is Core power rail	
8	4/2	07	Add R215 to pull high +1.5V_APU & @ R36	AMD suggest	
9	4/6	24	Add C1223 1000p	For EMI	
10	4/6	33	Add C1224 1000p	For EMI	
11	4/6	26	Change C1204, C1205 from 12p to 15p	For Vendor tunning value	
12	4/6	16	Change C341, C350 from 15p to 8.2p	For Vendor tunning value	
13	4/6	33	Swap D45	For layout	
14	4/9	31	Change R1564 from 33k to 18k	DVT Board ID	
15	4/9	30	Swap JSPK1	For swap speaker cable	
16	4/9	31	Add VSB_ON on GPIO127	For S5 power saving	
17	4/11	29	Change R1527 to R-short	For cost down	
18	4/11	31	Change R1580, R1586 to R-short	For cost down	
19	4/11	13	Change R167 to R-short	For cost down	
20	4/11	31	Change R1591 to always mount	For MainPowerON power control	
21	4/11	7	Change R51, R52 to R-short	For cost down	
22	4/11	12	Change R1610, R1611 to R-short	For cost down	
23	4/11	17	Change R400 to R-short	For cost down	
24	4/11	22	Mount R200, @ L171, C238, C239	For LVDS Translator 1.2 power rail	
25	4/11	26	Change R1515, R1508 to R-short	For cost down	
26	4/11	27	Delete J17, J19	For LAN surge solution change	
27	4/12	5	Change A6, A10 APU R1 PN	From PC sample to PR sample	
28	4/13	17,19	Change BIF_VDDC to VGA_CORE and move C343 to Page 19	For PX5 only	
29	4/16	27	Change CHASSIS2_GND to GND & CHASSIS1_GND	For common LAN surge solution	
30	4/17	33	Mount L43, L44, L45, @ R1605, R1608, R1609, R1612, R1613, R1616	For EMI (USB3.0 choke)	
31	4/17	32	Add L50, L51, L52 @ R1614, R1615, R1619, R1624, R1625, R1626	For EMI (USB2.0 choke from SB to MB)	
32	4/17	30	Change R937, R1548 from 0 ohm to L172, L173 300ohm Bead	For EMI (DMIC DATA , CLK)	
33	4/17	7	Change R26,R28 from 1k to 10k	For APU_SIC, SID 0'C shut down issue workaround	
34	4/18	7	Change back R26,R28 from 10k to 1k, and mount C5988	For APU_SIC, SID 0'C shut down issue	

Compal Electronics, Inc.

Title: HW-PIR

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

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VAUS5 HW PIR List

SIV TO SIT

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	NOTE
1	5/11	16	Change Q64 from SB00000EO10 to SB00000DH00	For BOM reduce	
2	5/11	23	Reserve R1466	For factory requirement to prevent DISPOFF# damage	
3	5/11	25	Add BOM structure SSD@ for SSD function	For BOM option	
4	5/14	24	Reserve ESD component D1,D2 for HDMI signal	For HDMI hot-plug protection	
5	5/21	7 13 25 26 30	0402 R-Shot modify R24,R160,R161,R158,R163,R171,R169,R166,R1491,R1492 0603 R-Shot modify R157,R164,R170,R172,R168,R159,R1529,L35,L36 0805 R-Shot modify R162,R165,R1531	For BOM reduce	
6	5/21	31	Change R1564 from 18K to 8.2K	For Board ID change	
7	5/22	7	Change back R24 from R-shot to 0ohm		
8	5/22	24	Reserve ESD component D69 for HDMI SMBus	For APU damage when HDMI hot-plug	
9	5/24	25	Reserve R1493	For Intel 2230 WLAN Card Support	
10	5/24	20	Add VRAM Samsung 1G K4W2G1646E-BC11 strap setting	For customer request	
11	5/24	24	Un-mount D1, D2		
12	5/24	12	Change back R1610, R1611 footprint to 0ohm		
13	5/25	30	Add C83, C84 for DMIC noise issue	For EMI request	
14	5/25	27	Change DL2 PN to SCV00001D00	For customer request	
15	5/25	10 25	Add BT_OFF# for other BT combo card	For customer request	
16	5/29	26	Un-mount C1197. C1198 and mount C1200,C1203	For LAN power trace rounting	
17	5/29	7	Change Q3,Q4 PN from SB501110010 to SB501380050	For PUR request	
18	5/29	30	Change R1530 PN from SM01000DI00 to SM010005X00	For PUR request	
19	5/31	23 25 32 33	Change C8244,C8245,C8246,C8247,C8248 and C8249 from 10p to 15p	For AMD suggest	

Compal Electronics, Inc.

Title: HW-SIT PIR

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

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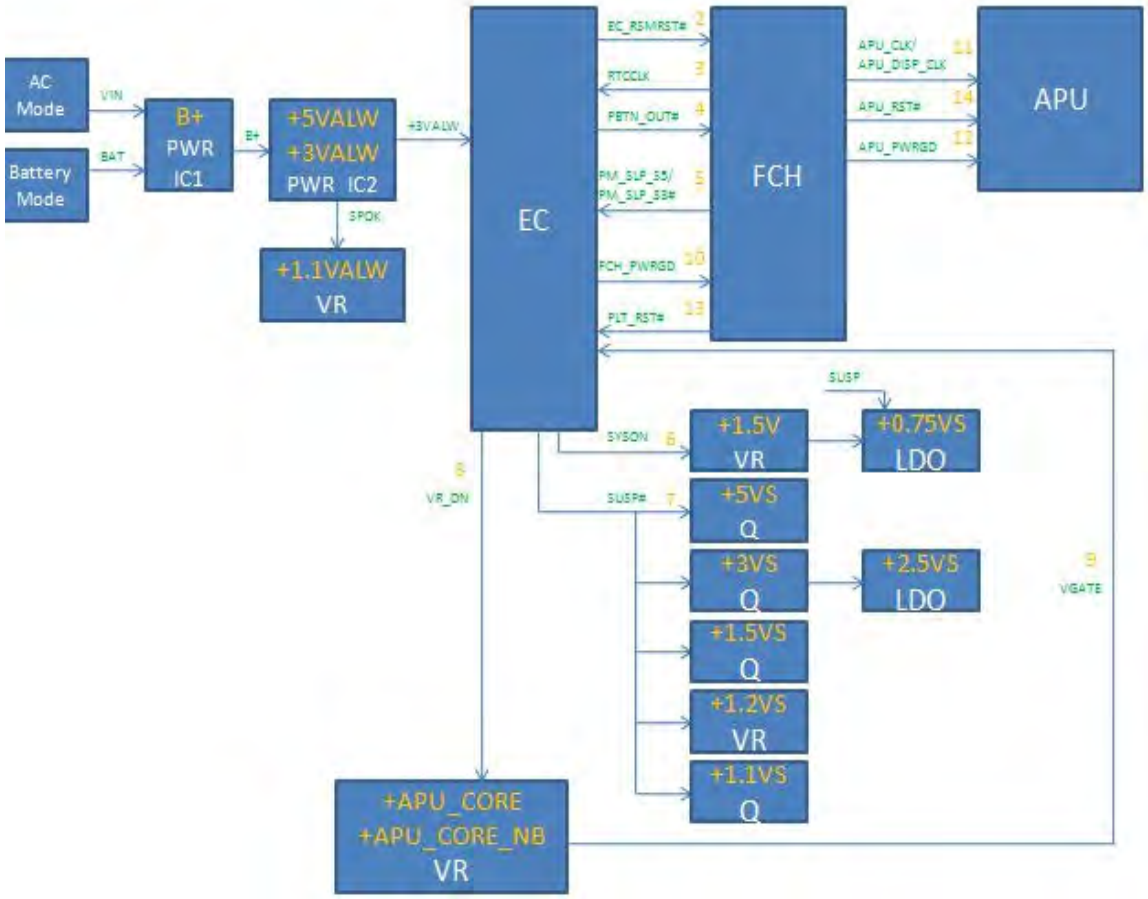
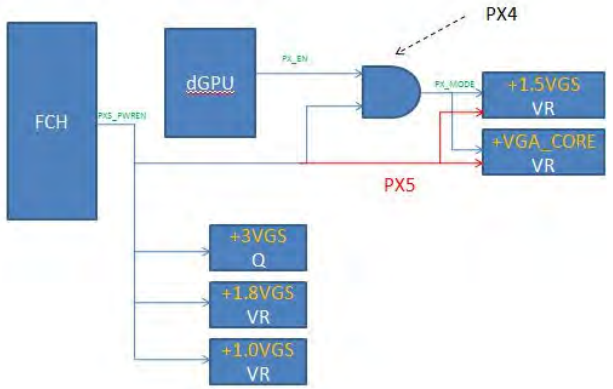
SYSTEM



VGA



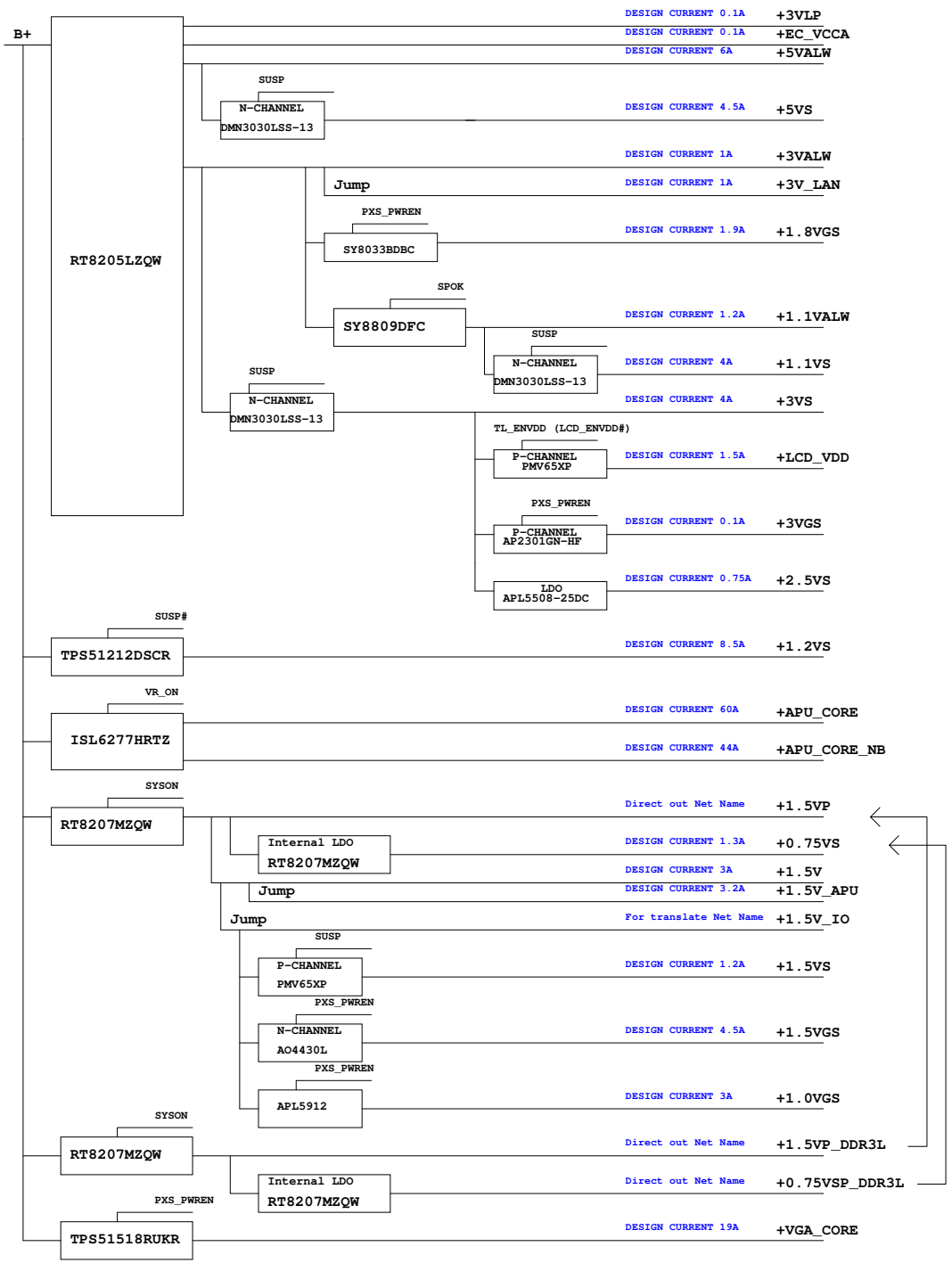
Security Classification	Compal Secret Data		
Issued Date	2012/01/15	Deciphered Date	2013/01/15

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: VAUS5 LA9001P M/B | Rev: 0.3

Date: Friday, May 25, 2012 | Sheet 48 of 50



Security Classification	Compal Secret Data		
Issued Date	2011/12/30	Deciphered Date	2013/10/05

Compal Electronics, Inc.

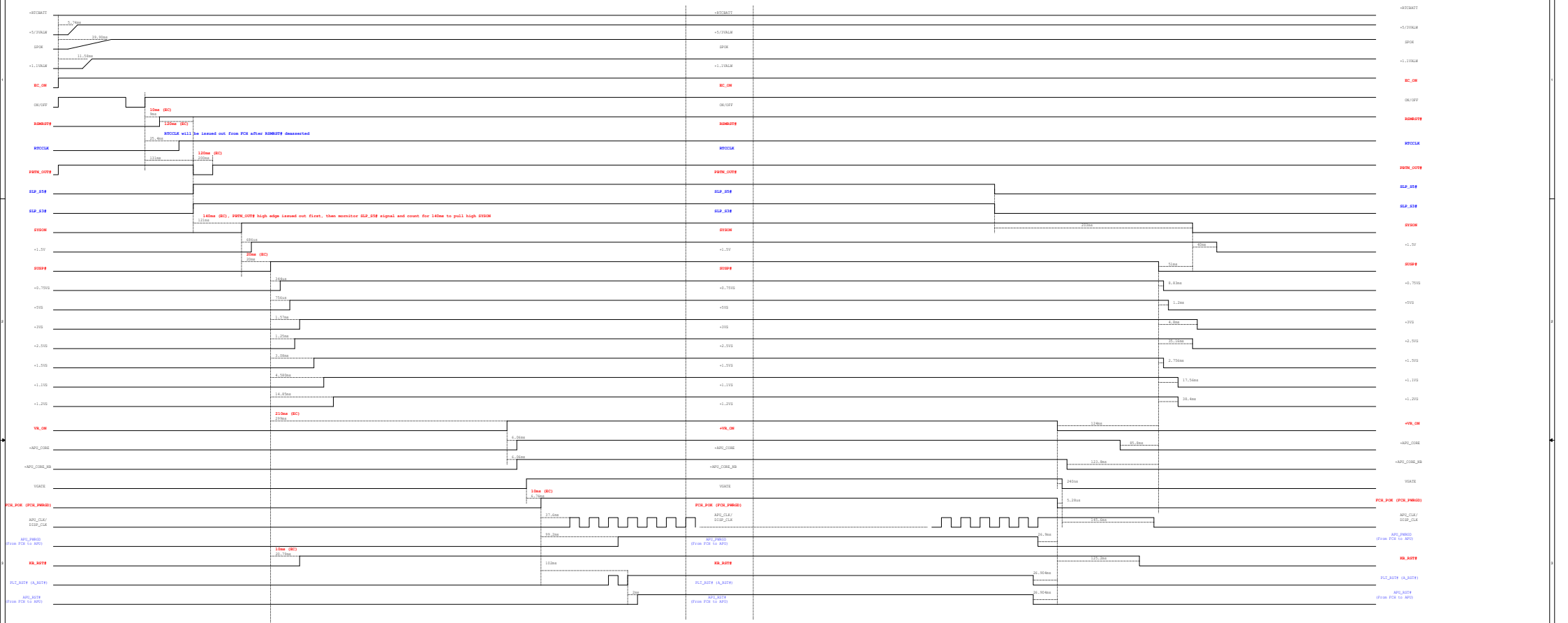
Title: **Power Map**

Size	Document Number	Rev
Custom	VAUS5 LA9001P M/B	0.3

Date: Friday, May 25, 2012 Sheet 49 of 50

VAUS5 Power on / off sequence (AC mode)

S5 – S0 –S5



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.

Title: **S5_Power Sequence**

Size	Document Number	Rev
		0.3

Date: Friday, May 25, 2012 | Sheet 50 of 50