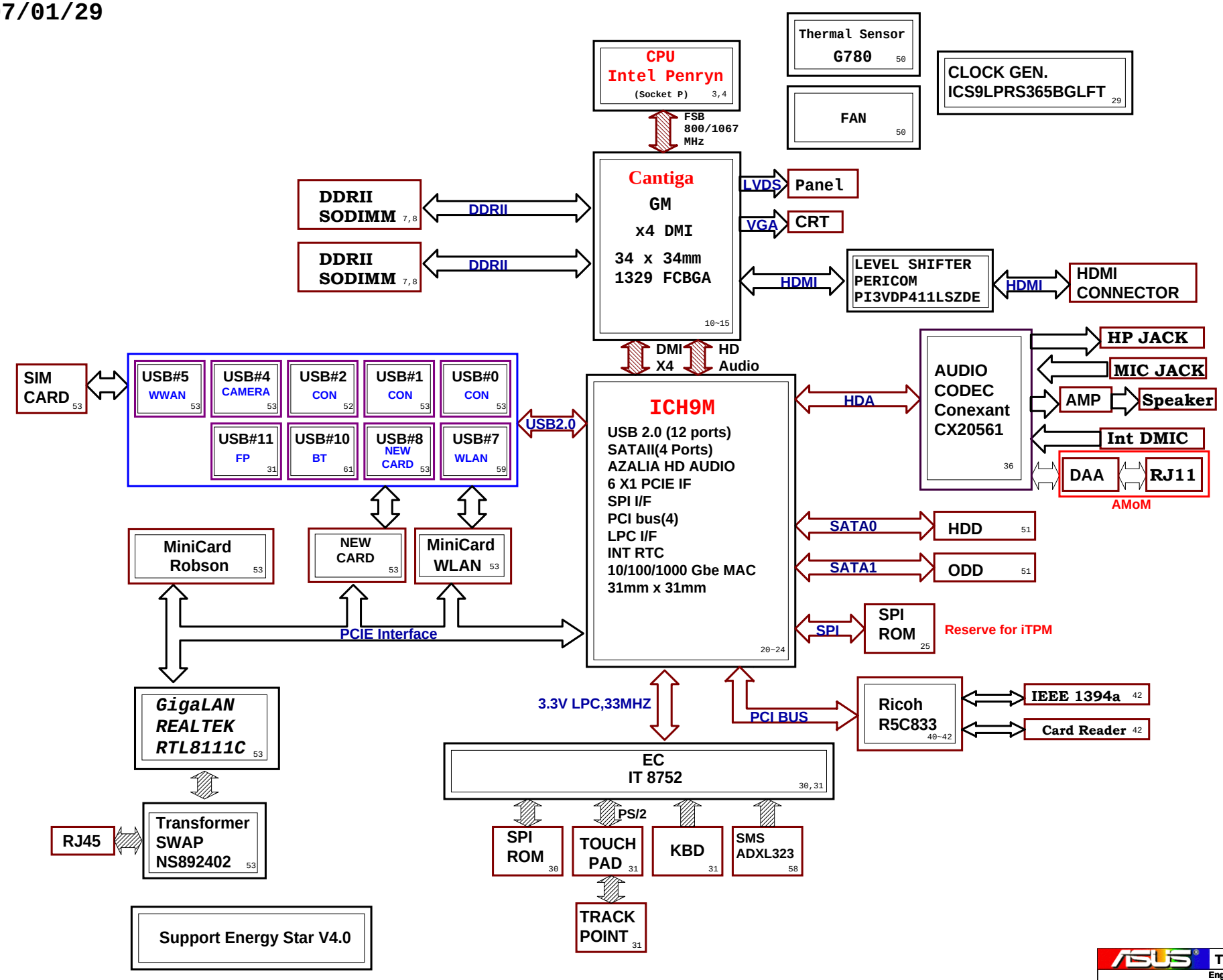
B3 NOTE 13" UMA Block Diagram
2007/01/29



Title : Block Diagram			
Engineer: Peter Lo			
Size: C	Project Name: Rocky30		Rev: 1.0
Date: Tuesday, January 29, 2008	Sheet 1 of 94		

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84	PWR_-****
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87	PWR-SHUTDOWN#(Empty)
88	PWR_CHARGER
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90	PWR_DETECT
91	PWR_LOAD SWITCH
92	PWR_PROTECT
93	PWR_SIGNAL
94	PWR_FLOWCHART

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI		+3VS
GPIO 07	GPI		+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO		+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPI	GPIO36	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDCP_EEPROM_PROTECT#	**+3VS**
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

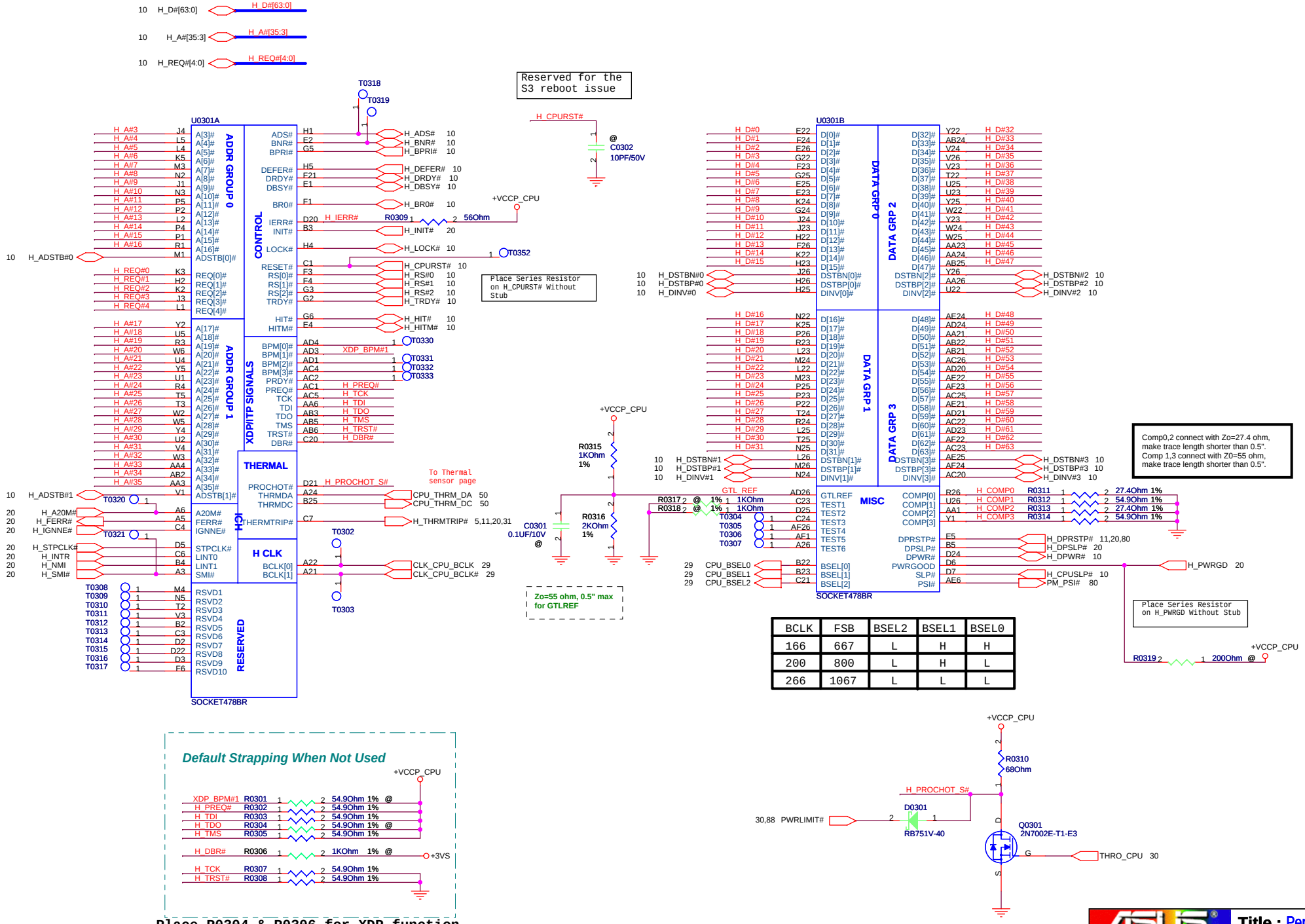
EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	3G_ON#	
GPH2	ALT	LOGO_LED#	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED#	
GPH6	GPO	CAP_LED#	
-	-	-	
GPI0	GPI	NV_OVERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	XOUT	
GPI5	GPI	YOUT	
GPI6	GPI	-	
GPI7	GPI	-	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	-	
GPK0	GPI	-	
GPK1	GPI	-	
GPK2	GPI	-	
GPK3	GPI	-	
GPK4	GPI	-	
GPK5	GPI	-	
GPL0	GPI	APS_PWR_CNT#	
GPL1	GPI	APS_ST#	
GPL2	GPO	USB_PWR_EN#	
GPL3	GPO	-	
GPL4	GPO	-	
GPL5	GPO	AC_ID	
GPL6	GPO	AC_65W	
GPL7	GPO	CHG_LOW_LED#	
GPK6	GPO	-	
GPK7	GPI	-	

ASUS Title : Schematic Information

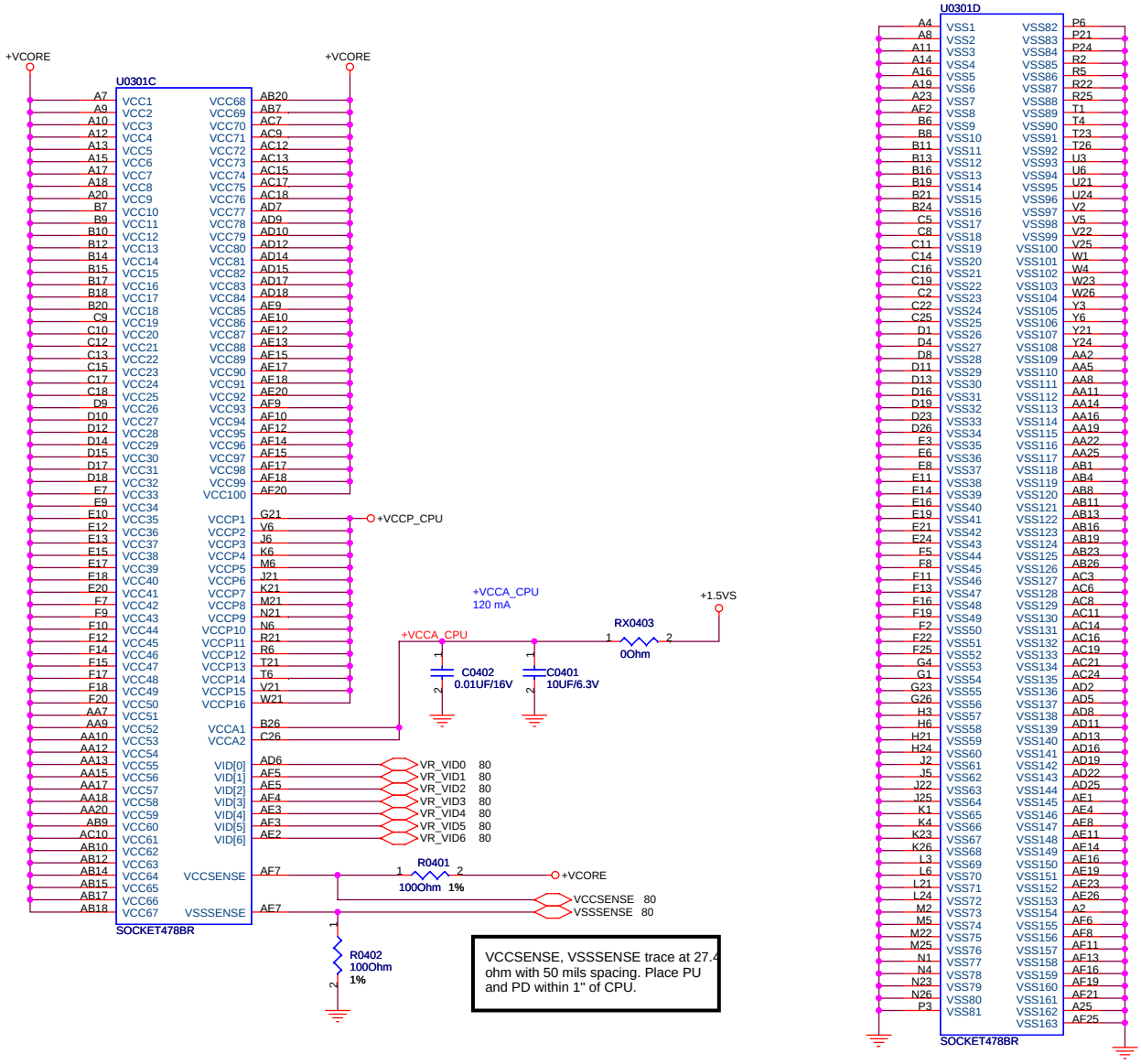
Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

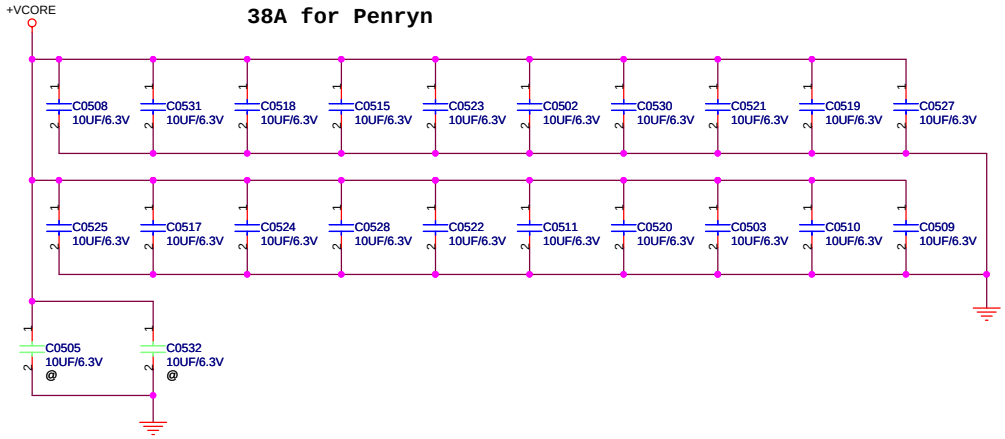
Date: Tuesday, January 15, 2008 Sheet 2 of 94

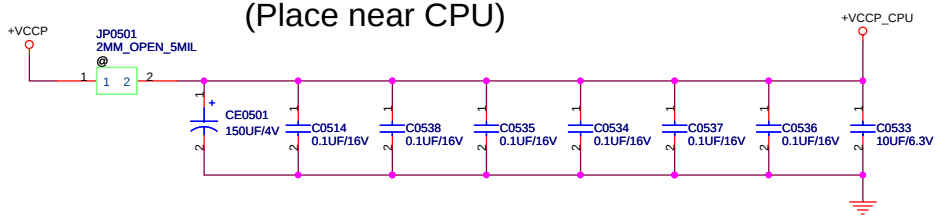


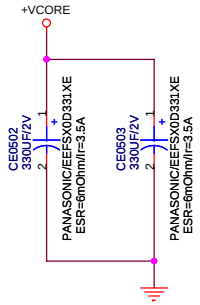
Title : Penryn CPU (1)			
Engineer: Peter Lo			
Size: Custom	Project Name: Rocky30		Rev: 1.0
Date: Monday, February 04, 2008	Sheet 3 of 94		

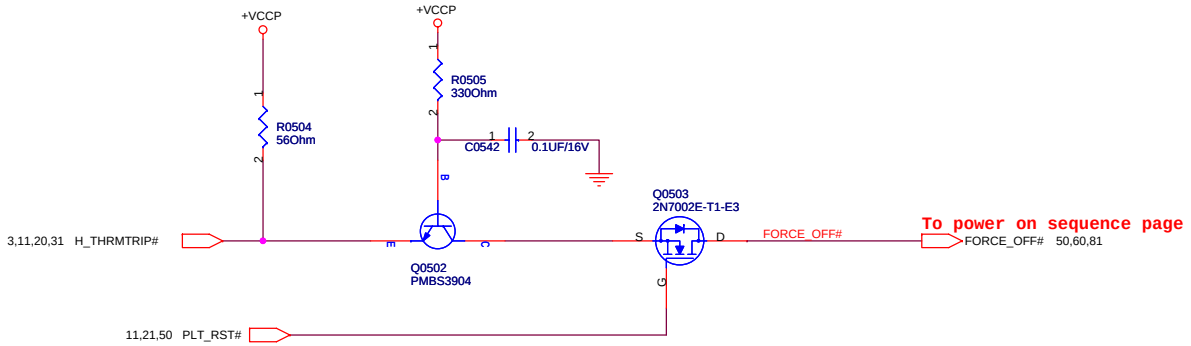


ASUS	Title : Penryn CPU (2)	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 4 of 94	









Thermal Trip signal(From CPU to ICH-9M and sequence)

Title : CPU CAPS		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 5 of 94	

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
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+3VS → +3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

+1.8V → +1.8V 8,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 8,9,11

SMBus Slave Address:A0H

temp_5886_tl01
(12G025M22000LV with 12G025C2200WLV
co-lay symbol)

SMBus Slave Address: A0H

9,12 M_A_A[0..14]

M_A_DQ[0..63] 12

J0701A

M_A_A0	102	A0	DQ0	5	M_A_DQ8
M_A_A1	101	A1	DQ1	7	M_A_DQ9
M_A_A2	100	A2	DQ2	17	M_A_DQ15
M_A_A3	99	A3	DQ3	19	M_A_DQ10
M_A_A4	98	A4	DQ4	4	M_A_DQ12
M_A_A5	97	A5	DQ5	6	M_A_DQ13
M_A_A6	94	A6	DQ6	14	M_A_DQ11
M_A_A7	92	A7	DQ7	16	M_A_DQ14
M_A_A8	93	A8	DQ8	23	M_A_DQ20
M_A_A9	91	A9	DQ9	25	M_A_DQ17
M_A_A10	105	A10/AP	DQ10	35	M_A_DQ22
M_A_A11	90	A11	DQ11	37	M_A_DQ18
M_A_A12	89	A12	DQ12	20	M_A_DQ21
M_A_A13	116	A13	DQ13	22	M_A_DQ19
M_A_A14	86	A14	DQ14	36	M_A_DQ23
	84	A15	DQ15	38	M_A_DQ16
9,12 M_A_BS2	85	A16_BA2	DQ16	43	M_A_DQ6
			DQ17	45	M_A_DQ2
9,12 M_A_BS0	107	BA0	DQ18	55	M_A_DQ1
9,12 M_A_BS1	106	BA1	DQ19	57	M_A_DQ5
9,11 M_CS#0	110	S0#	DQ20	44	M_A_DQ3
9,11 M_CS#1	115	S1#	DQ21	46	M_A_DQ7
11 M_CLK_DDR0	30	CK0	DQ22	56	M_A_DQ0
11 M_CLK_DDR#0	32	CK0#	DQ23	58	M_A_DQ4
11 M_CLK_DDR1	164	CK1	DQ24	61	M_A_DQ29
11 M_CLK_DDR#1	166	CK1#	DQ25	63	M_A_DQ25
9,11 M_CKE0	79	CKE0	DQ26	73	M_A_DQ26
9,11 M_CKE1	80	CKE1	DQ27	75	M_A_DQ31
9,12 M_A_CAS#	113	CAS#	DQ28	62	M_A_DQ24
9,12 M_A_RAS#	108	RAS#	DQ29	64	M_A_DQ28
9,12 M_A_WE#	109	WE#	DQ30	74	M_A_DQ30
M_A_SA0	198	SA0	DQ31	76	M_A_DQ27
M_A_SA1	200	SA1	DQ32	123	M_A_DQ33
8,24,25,29 SMB_CLK_M	197	SCL	DQ33	125	M_A_DQ32
8,24,25,29 SMB_DAT_M	195	SDA	DQ34	135	M_A_DQ34
			DQ35	137	M_A_DQ38
9,11 M_ODT0	114	ODT0	DQ36	124	M_A_DQ37
9,11 M_ODT1	119	ODT1	DQ37	126	M_A_DQ36
			DQ38	134	M_A_DQ35
12 M_A_DM[0..7]			DQ39	136	M_A_DQ39
M_A_DM1	10	DM0	DQ40	141	M_A_DQ40
M_A_DM2	26	DM1	DQ41	143	M_A_DQ41
M_A_DM0	52	DM2	DQ42	151	M_A_DQ43
M_A_DM3	67	DM3	DQ43	153	M_A_DQ42
M_A_DM4	130	DM4	DQ44	140	M_A_DQ45
M_A_DM5	147	DM5	DQ45	142	M_A_DQ44
M_A_DM6	170	DM6	DQ46	152	M_A_DQ46
M_A_DM7	185	DM7	DQ47	154	M_A_DQ47
12 M_A_DQS[0..7]			DQ48	157	M_A_DQ48
M_A_DQS1	13	DQS0	DQ49	159	M_A_DQ53
M_A_DQS2	31	DQS1	DQ50	173	M_A_DQ51
M_A_DQS0	51	DQS2	DQ51	175	M_A_DQ55
M_A_DQS3	70	DQS3	DQ52	158	M_A_DQ49
M_A_DQS4	131	DQS4	DQ53	160	M_A_DQ52
M_A_DQS5	148	DQS5	DQ54	174	M_A_DQ50
M_A_DQS6	169	DQS6	DQ55	176	M_A_DQ54
M_A_DQS7	188	DQS7	DQ56	179	M_A_DQ63
12 M_A_DQS#[0..7]			DQ57	181	M_A_DQ56
M_A_DQS#1	11	DQS#0	DQ58	189	M_A_DQ57
M_A_DQS#2	29	DQS#1	DQ59	191	M_A_DQ59
M_A_DQS#0	49	DQS#2	DQ60	180	M_A_DQ61
M_A_DQS#3	68	DQS#3	DQ61	182	M_A_DQ60
M_A_DQS#4	129	DQS#4	DQ62	192	M_A_DQ58
M_A_DQS#5	146	DQS#5	DQ63	194	M_A_DQ62
M_A_DQS#6	167	DQS#6			
M_A_DQS#7	186	DQS#7			

DDR2_DIMM_200P

M_CLK_DDR0 — C0701 10PF/50V @ — M_CLK_DDR#0

M_CLK_DDR1 — C0702 10PF/50V @ — M_CLK_DDR#1

Place near SO-DIMM_0

R0703 10KOhm, R0704 10KOhm

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these caps near SO DIMM 0

+1.8V

C0703 0.1UF/10V, C0704 0.1UF/10V, C0705 0.1UF/10V, C0706 0.1UF/10V

+3VS

C0707 2.2UF/6.3V, C0708 0.1UF/10V

11 PM_EXTTS#0 — RX0702 0Ohm @ — PM_EXTTS#0_R

M_VREF_MCH

C0709 2.2UF/6.3V, C0710 0.1UF/10V

VREF -> 10/10 mils

J0701B

	112	VDD1	VSS16	18	
	111	VDD2	VSS17	24	
	117	VDD3	VSS18	41	
	96	VDD4	VSS19	53	
	95	VDD5	VSS20	42	
	118	VDD6	VSS21	54	
	81	VDD7	VSS22	59	
	82	VDD8	VSS23	65	
	87	VDD9	VSS24	60	
	103	VDD10	VSS25	66	
	88	VDD11	VSS26	127	
	104	VDD12	VSS27	139	
			VSS28	128	
	199	VDDSPD	VSS29	145	
			VSS30	165	
	83	NC1	VSS31	171	
	120	NC2	VSS32	172	
	50	NC3	VSS33	177	
	69	NC4	VSS34	187	
	163	NCTEST	VSS35	178	
			VSS36	190	
	1	VREF	VSS37	9	
			VSS38	21	
	201	GND0	VSS39	33	
	202	GND1	VSS40	155	
			VSS41	34	
	203	NP_NC1	VSS42	132	
	204	NP_NC2	VSS43	144	
			VSS44	156	
	47	VSS1	VSS45	168	
	133	VSS2	VSS46	2	
	183	VSS3	VSS47	3	
	77	VSS4	VSS48	15	
	12	VSS5	VSS49	27	
	48	VSS6	VSS50	39	
	184	VSS7	VSS51	149	
	78	VSS8	VSS52	161	
	71	VSS9	VSS53	28	
	72	VSS10	VSS54	40	
	121	VSS11	VSS55	138	
	122	VSS12	VSS56	150	
	196	VSS13	VSS57	162	
	193	VSS14			
	8	VSS15			

DDR2_DIMM_200P

SO-DIMM 0 is placed nearer the GMCH than SO-DIMM 1

+1.8V

Layout Note: Place these Caps near SO DIMM 0

C0716 2.2UF/6.3V, C0717 2.2UF/6.3V, C0718 2.2UF/6.3V, C0719 2.2UF/6.3V

+1.8V

CE0701 220UF/4V @ +/-ESR=40mOhm/Ir=1900mA

PLACE NEAR SO-DIMM_0 / SO-DIMM_1

Title: DDR3 SO-DIMM_0			
Engineer: Peter Lo			
Size: Custom	Project Name: Rocky30		Rev: 1.0
Date: Monday, February 04, 2008		Sheet 7 of 94	

+3VS +3VS 3,7,11,14,15,20,22,23,24,25,29,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92

+1.8V +1.8V 7,9,11,13,83,91

M_VREF_MCH M_VREF_MCH 7,9,11

temp_5886_tl02
(12G025032005LV with 12G025022004LV
CO-LAY symbol)

9,12 M_B_A[0..14]

M_B_DQ[0..63] 12

J0801A

SMBus Slave Address:A4H

M_CLK_DDR3
C0801
10PF/50V
@
M_CLK_DDR#3

M_CLK_DDR2
C0802
10PF/50V
@
M_CLK_DDR#2

Place near SO-DIMM_1

M_B_SA0
R0804 10KOhm M_B_SA1
+3VS
R0803
10KOhm

7,24,25,29 SMB_CLK_M
7,24,25,29 SMB_DAT_M

9,11 M_ODT2
9,11 M_ODT3

12 M_B_DM[0..7]

12 M_B_DQS[0..7]

12 M_B_DQS#[0..7]

DDR2_DIMM_200P

+1.8V

Layout Note: Place these Caps near the SO-DIMM_1

C0816 2.2UF/6.3V
C0817 2.2UF/6.3V
C0818 2.2UF/6.3V
C0819 2.2UF/6.3V

+1.8V

Layout Note: Place these Caps near SO DIMM 1

C0807 0.1UF/10V
C0808 0.1UF/10V
C0809 0.1UF/10V
C0810 0.1UF/10V

+3VS

C0811 2.2UF/6.3V
C0812 0.1UF/10V

11 PM_EXTTS#1

RX0802 @
0Ohm
PM_EXTTS#1_R

M_VREF_MCH

C0821 2.2UF/6.3V
C0820 0.1UF/10V

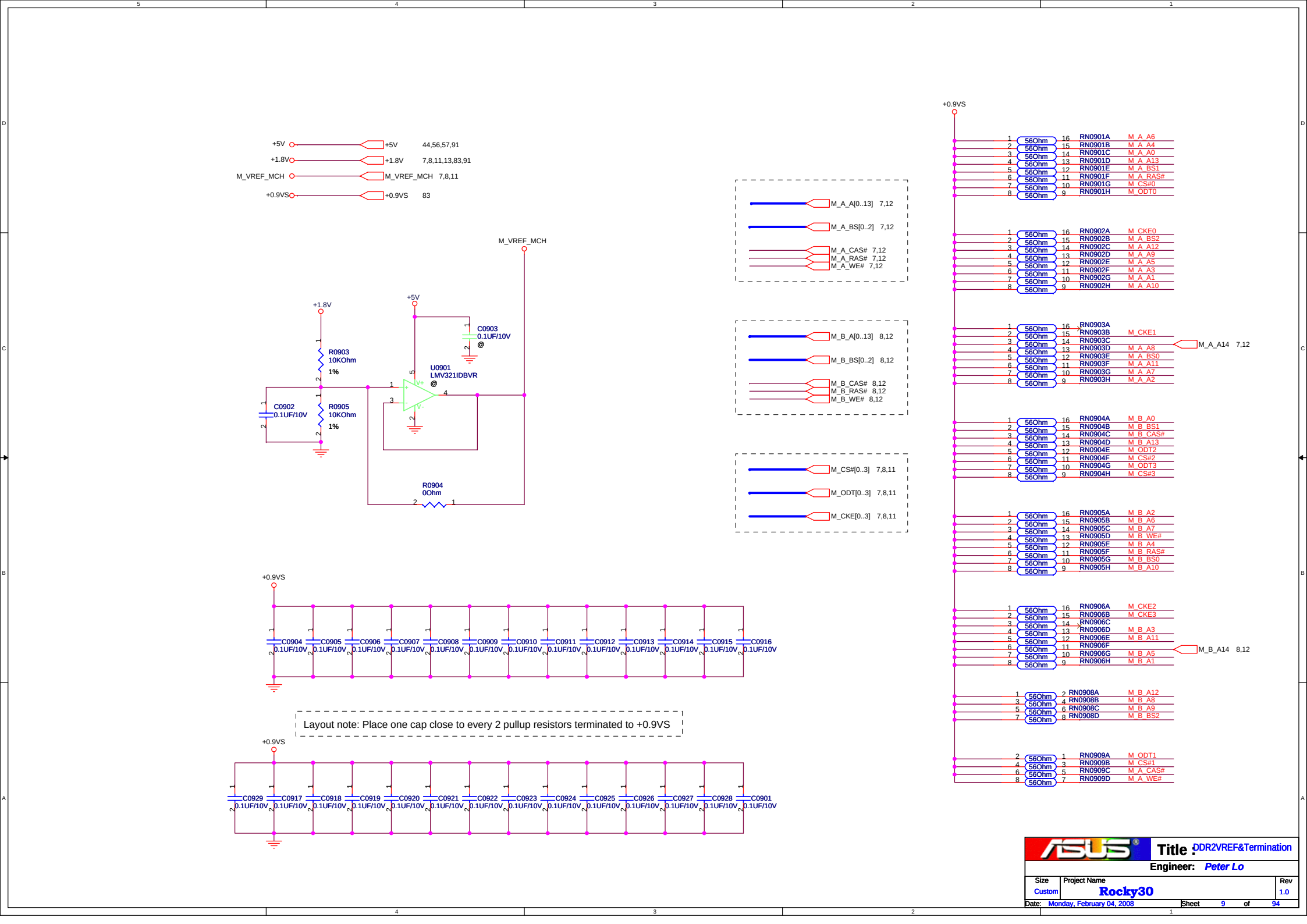
Layout Note: Place these Caps near SO DIMM 1

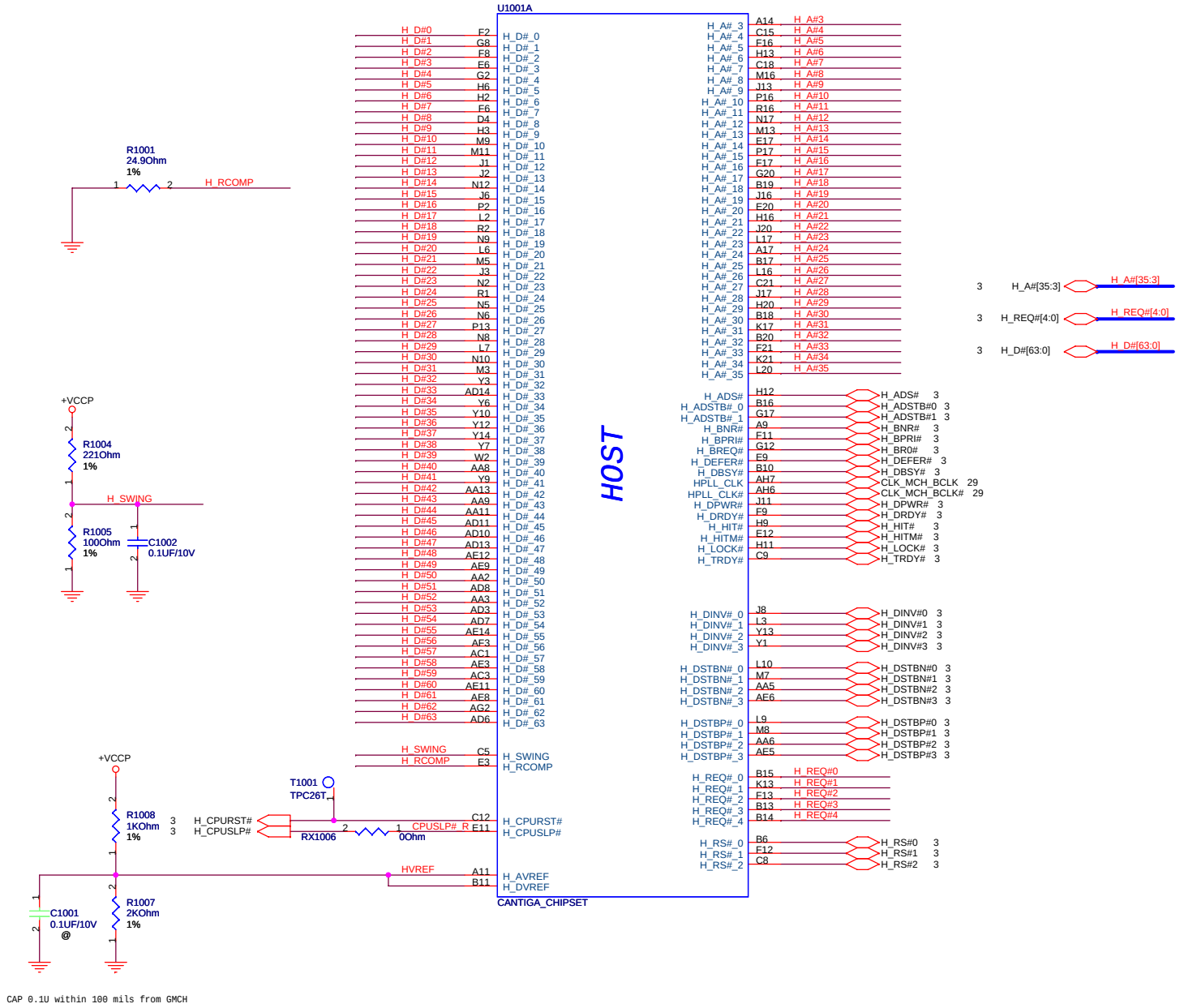
VREF -> 10/10 mils

J0801B

DDR2_DIMM_200P

Title :DDR3 SO-DIMM_1		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 8 of 94	


+5V +5V 44,56,57,91
+1.8V +1.8V 7,8,11,13,83,91
M_VREF_MCH M_VREF_MCH 7,8,11
+0.9VS +0.9VS 83
M_VREF_MCH
+1.8V
+5V
R0903 10KOhm 1%
C0903 0.1UF/10V @
U0901 LMV321IDBVR @
C0902 0.1UF/10V
R0905 10KOhm 1%
R0904 0Ohm
M_A_A[0..13] 7,12
M_A_BS[0..2] 7,12
M_A_CAS# 7,12
M_A_RAS# 7,12
M_A_WE# 7,12
M_B_A[0..13] 8,12
M_B_BS[0..2] 8,12
M_B_CAS# 8,12
M_B_RAS# 8,12
M_B_WE# 8,12
M_CS#[0..3] 7,8,11
M_ODT[0..3] 7,8,11
M_CKE[0..3] 7,8,11
+0.9VS
C0904 0.1UF/10V
C0905 0.1UF/10V
C0906 0.1UF/10V
C0907 0.1UF/10V
C0908 0.1UF/10V
C0909 0.1UF/10V
C0910 0.1UF/10V
C0911 0.1UF/10V
C0912 0.1UF/10V
C0913 0.1UF/10V
C0914 0.1UF/10V
C0915 0.1UF/10V
C0916 0.1UF/10V
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS
+0.9VS
C0929 0.1UF/10V
C0917 0.1UF/10V
C0918 0.1UF/10V
C0919 0.1UF/10V
C0920 0.1UF/10V
C0921 0.1UF/10V
C0922 0.1UF/10V
C0923 0.1UF/10V
C0924 0.1UF/10V
C0925 0.1UF/10V
C0926 0.1UF/10V
C0927 0.1UF/10V
C0928 0.1UF/10V
C0901 0.1UF/10V
+0.9VS
RN0901A M_A_A6
RN0901B M_A_A4
RN0901C M_A_A0
RN0901D M_A_A13
RN0901E M_A_BS1
RN0901F M_A_RAS#
RN0901G M_CS#0
RN0901H M_ODT0
RN0902A M_CKE0
RN0902B M_A_BS2
RN0902C M_A_A12
RN0902D M_A_A9
RN0902E M_A_A5
RN0902F M_A_A3
RN0902G M_A_A1
RN0902H M_A_A10
RN0903A
RN0903B M_CKE1
RN0903C M_A_A14 7,12
RN0903D M_A_A8
RN0903E M_A_BS0
RN0903F M_A_A11
RN0903G M_A_A7
RN0903H M_A_A2
RN0904A M_B_A0
RN0904B M_B_BS1
RN0904C M_B_CAS#
RN0904D M_B_A13
RN0904E M_ODT2
RN0904F M_CS#2
RN0904G M_ODT3
RN0904H M_CS#3
RN0905A M_B_A2
RN0905B M_B_A6
RN0905C M_B_A7
RN0905D M_B_WE#
RN0905E M_B_A4
RN0905F M_B_RAS#
RN0905G M_B_BS0
RN0905H M_B_A10
RN0906A M_CKE2
RN0906B M_CKE3
RN0906C
RN0906D M_B_A3
RN0906E M_B_A11
RN0906F M_B_A14 8,12
RN0906G M_B_A5
RN0906H M_B_A1
RN0908A M_B_A12
RN0908B M_B_A8
RN0908C M_B_A9
RN0908D M_B_BS2
RN0909A M_ODT1
RN0909B M_CS#1
RN0909C M_A_CAS#
RN0909D M_A_WE#
56Ohm
Title : DDR2VREF&Termination
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Monday, February 04, 2008
Sheet 9 of 94



Title :	Cantiga -- CPU (1)
Engineer:	Peter Lo
Size	Custom
Project Name	Rocky30
Rev	1.0
Date:	Monday, February 04, 2008
Sheet	10 of 94

U1001B

RSVD
RSVD1 M36
RSVD2 N36
RSVD3 R33
RSVD4 T33
RSVD5 AH9
RSVD6 AH10
RSVD7 AH12
RSVD8 AH13
RSVD9 K12
RSVD10 AL34
RSVD11 AK34
RSVD12 AN35
RSVD13 AM35
RSVD14 T24
RSVD15 B31
RSVD16 AJ6
RSVD17 M1
RSVD20 AY21
RSVD21 A47
RSVD22 BG23
RSVD23 BF23
RSVD24 BH18
RSVD25 BF18

DDR CONTROL/COMPENSATION
SA_CK_0 AP24 M_CLK_DDR0 7
SA_CK_1 AT21 M_CLK_DDR1 7
SB_CK_0 AV24 M_CLK_DDR2 8
SB_CK_1 AU20 M_CLK_DDR3 8
SA_CK#_0 AR24 M_CLK_DDR#0 7
SA_CK#_1 AR21 M_CLK_DDR#1 7
SB_CK#_0 AU24 M_CLK_DDR#2 8
SB_CK#_1 AV20 M_CLK_DDR#3 8
SA_CKE_0 BC28 M_CKE0 7,9
SA_CKE_1 AY28 M_CKE1 7,9
SB_CKE_0 AY36 M_CKE2 8,9
SB_CKE_1 BB36 M_CKE3 8,9
SA_CS#_0 BA17 M_CS#0 7,9
SA_CS#_1 AY16 M_CS#1 7,9
SB_CS#_0 AV16 M_CS#2 8,9
SB_CS#_1 AR13 M_CS#3 8,9
SA_ODT_0 BD17 M_ODT0 7,9
SA_ODT_1 AY17 M_ODT1 7,9
SB_ODT_0 BF15 M_ODT2 8,9
SB_ODT_1 AY13 M_ODT3 8,9
SM_RCOMP BG22 M_RCOMP
SM_RCOMP# BH21 M_RCOMP# R1112 1% 80.6Ohm
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL R1117 1% 80.6Ohm
SM_VREF AV42 M_VREF_MCH
SM_PWROK AR36
SM_REXT BF17 SM_REXT R1121 499Ohm 1%
SM_DRAMRST# BC36
C1105 0.01UF/16V

CLK
DPLL_REF_CLK B38 CLK_DREF 29
DPLL_REF_CLK# A38 CLK_DREF# 29
DPLL_REF_SSCLK F41 CLK_DREFSS 29
DPLL_REF_SSCLK# F41 CLK_DREFSS# 29
PEG_CLK F43 CLK_MCH_3GPLL 29
PEG_CLK# E43 CLK_MCH_3GPLL# 29

CFG DMI
DMI_RXN_0 AE41 DMI_TXN0 21
DMI_RXN_1 AE37 DMI_TXN1 21
DMI_RXN_2 AE47 DMI_TXN2 21
DMI_RXN_3 AH39 DMI_TXN3 21
DMI_RXP_0 AE40 DMI_TXP0 21
DMI_RXP_1 AE38 DMI_TXP1 21
DMI_RXP_2 AE48 DMI_TXP2 21
DMI_RXP_3 AH40 DMI_TXP3 21
DMI_TXN_0 AE35 DMI_RXN0 21
DMI_TXN_1 AE43 DMI_RXN1 21
DMI_TXN_2 AE46 DMI_RXN2 21
DMI_TXN_3 AH42 DMI_RXN3 21
DMI_TXP_0 AD35 DMI_RXP0 21
DMI_TXP_1 AE44 DMI_RXP1 21
DMI_TXP_2 AE46 DMI_RXP2 21
DMI_TXP_3 AH43 DMI_RXP3 21

GRAPHICS VID
GFX_VID_0 B33 TP_GFX_VID0 T1110
GFX_VID_1 B32 TP_GFX_VID1 T1111
GFX_VID_2 G33 TP_GFX_VID2 T1112
GFX_VID_3 E33 TP_GFX_VID3 T1113
GFX_VID_4 E33 TP_GFX_VID4 T1114
GFX_VR_EN C34 TP_GFX_VREN T1106

PWR
MCH_BSEL0 29 T25 CFG_0
MCH_BSEL1 29 R25 CFG_1
MCH_BSEL2 29 P25 CFG_2
T1102 P20 CFG_3
T1101 P24 CFG_4
MCH_CFG_5 15 C25 CFG_5
MCH_CFG_6 15 N24 CFG_6
MCH_CFG_7 15 M24 CFG_7
T1115 F21 CFG_8
MCH_CFG_9 15 C23 CFG_9
MCH_CFG_10 15 C24 CFG_10
T1107 N21 CFG_11
P21 CFG_12
MCH_CFG_12 15 T21 CFG_13
T1103 R20 CFG_14
T1108 M20 CFG_15
MCH_CFG_16 15 L21 CFG_16
T1104 H21 CFG_17
T1109 P29 CFG_18
R28 CFG_19
MCH_CFG_19 15 T28 CFG_20
PM_SYNC# 22,3,20,80 H_DPRSTP# RX1103 0Ohm R29 B7 PM_DPRSTP#
PM_EXTTS#0 N33 PM_EXT_TS#_0
PM_EXTTS#1 P32 PM_EXT_TS#_1
PWROK 22,30 PM_PWROK RX1102 0Ohm AT40
RSTIN# 5,21,50 PLT_RST# AT11
THERMTRIP# 3,5,20,31 H_THRMTRIP# RX1101 100Ohm T20
DPRSLPVR 22,80 PM_DPRSLPVR RX1104 0Ohm R32

ME
CL_CLK AH37 CL_CLK0 22
CL_DATA AH36 CL_DATA0 22
CL_PWROK AN36 RX1105 0Ohm CL_RST#0 22 PM_PWROK 22,30
CL_RST# AJ35
CL_VREF AH34 CL_VREF
C1106 0.1UF/10V

MISC
DDPC_CTRLCLK N28 T1121
DDPC_CTRLDATA M28 T1122
SDVO_CTRLCLK G36 SDVO_CTRLCLK 48
SDVO_CTRLDATA E36 SDVO_CTRLDATA 48
CLKREQ# K36 CLK_PEG_REQ# 29
ICH_SYNC# H36 MCH_ICH_SYNC# 22
TSATN# B12 T1117 R1126 56Ohm
+VCCP
R1108 1KOhm 1%
R1102 499Ohm 1%

HDA
HDA_BCLK B28 ACZ_BCLK_HDMI 20
HDA_RST# B30 ACZ_RST#_HDMI 20
HDA_SDI B29 ACZ_SDIN2_HDMI_R RX1107 33Ohm 1% ACZ_SDIN2_HDMI 20
HDA_SDO C29 ACZ_SDOUT_HDMI 20
HDA_SYNC A28 ACZ_SYNC_HDMI 20

NC
BG48 NC_1
BF48 NC_2
BD48 NC_3
BC48 NC_4
BH47 NC_5
BG47 NC_6
BE47 NC_7
BH46 NC_8
BF46 NC_9
BG45 NC_10
BH44 NC_11
BH43 NC_12
BH6 NC_13
BH5 NC_14
BC4 NC_15
BH3 NC_16
BF3 NC_17
BH2 NC_18
BG2 NC_19
BE2 NC_20
BG1 NC_21
BF1 NC_22
BD1 NC_23
BC1 NC_24
F1 NC_25

CANTIGA_CHIPSET

+1.8V
R1105 1KOhm 1%
SM_RCOMP_VOH
C1101 2.2UF/6.3V
C1102 0.01UF/16V
R1106 3.01KOhm 1%
SM_RCOMP_VOL
C1103 2.2UF/6.3V
C1104 0.01UF/16V
R1107 1KOhm 1%

+3VS
R1103 10KOhm
R1104 10KOhm
PM_EXTTS#0 7
PM_EXTTS#1 8

T1123 ME_JTAG_TCK
T1124 ME_JTAG_TDI
T1125 ME_JTAG_TDO
T1126 ME_JTAG_TMS

U1001C

L_BKLT_CTRL L32
L_BKLT_EN G32
L_CTRL_CLK M32
L_CTRL_DATA M33
L_DDC_CLK K33
L_DDC_DATA J33
L_VDD_EN M29
LVDS_IBG C44
LVDS_VBG B43
LVDS_VREFH E37
LVDS_VREFL E38
LVDSA_CLK# C41
LVDSA_CLK C40
LVDSB_CLK# B37
LVDSB_CLK A37
LVDSA_DATA#_0 H47
LVDSA_DATA#_1 E46
LVDSA_DATA#_2 G40
LVDSA_DATA#_3 A40
LVDSA_DATA_0 H48
LVDSA_DATA_1 D45
LVDSA_DATA_2 F40
LVDSA_DATA_3 B40
LVDSB_DATA#_0 A41
LVDSB_DATA#_1 H38
LVDSB_DATA#_2 G37
LVDSB_DATA#_3 J37
LVDSB_DATA_0 B42
LVDSB_DATA_1 G38
LVDSB_DATA_2 F37
LVDSB_DATA_3 K37

LVDS

TVA_DAC F25 TV_CVBS_J R1126 75Ohm 1%
TVB_DAC H25 TV_Y_J R1111 75Ohm 1%
TVC_DAC K25 TV_C_J R1114 75Ohm 1%
TV_RTN H24
TV_DCONSEL_0 C31
TV_DCONSEL_1 E32

TV

CRT_BLUE E28
CRT_GREEN G28
CRT_RED J28
CRT_IRTN G29
CRT_DDC_CLK H32
CRT_DDC_DATA J32
CRT_HSYNC J29
CRT_TVO_IREF E29
CRT_VSYNC L29

VGA

PCI-EXPRESS GRAPHICS

PEG_COMPI T37 PEGCOMP R1156 49.9Ohm 1%
PEG_COMPO T36
+VCCP
PEG_RX#_0 H44
PEG_RX#_1 J46
PEG_RX#_2 L44
PEG_RX#_3 L40
PEG_RX#_4 N41
PEG_RX#_5 P48
PEG_RX#_6 N44
PEG_RX#_7 T43
PEG_RX#_8 U43
PEG_RX#_9 Y43
PEG_RX#_10 Y48
PEG_RX#_11 Y36
PEG_RX#_12 AA43
PEG_RX#_13 AD37
PEG_RX#_14 AC47
PEG_RX#_15 AD39
PEG_RX_0 H43
PEG_RX_1 J44
PEG_RX_2 L43
PEG_RX_3 L41 HDMI_DETECT# 48
PEG_RX_4 N40
PEG_RX_5 P47
PEG_RX_6 N43
PEG_RX_7 T42 T1116
PEG_RX_8 U42
PEG_RX_9 Y42
PEG_RX_10 W47
PEG_RX_11 Y37
PEG_RX_12 AA42
PEG_RX_13 AD36
PEG_RX_14 AC48
PEG_RX_15 AD40
PEG_TX#_0 J41 TMDS_B_D2# CX1116 0.1UF/10V DVI_TX5-_C 48
PEG_TX#_1 M46 TMDS_B_D1# CX1114 0.1UF/10V DVI_TX4-_C 48
PEG_TX#_2 M47 TMDS_B_D0# CX1113 0.1UF/10V DVI_TX3-_C 48
PEG_TX#_3 M40 TMDS_B_CLK# CX1112 0.1UF/10V DVI_CLKB-_C 48
PEG_TX#_4 M42
PEG_TX#_5 R48
PEG_TX#_6 N38
PEG_TX#_7 T40
PEG_TX#_8 U37
PEG_TX#_9 U40
PEG_TX#_10 Y40
PEG_TX#_11 AA46
PEG_TX#_12 AA37
PEG_TX#_13 AA40
PEG_TX#_14 AD43
PEG_TX#_15 AC46
PEG_TX_0 J42 TMDS_B_D2 CX1107 0.1UF/10V DVI_TX5+_C 48
PEG_TX_1 L46 TMDS_B_D1 CX1106 0.1UF/10V DVI_TX4+_C 48
PEG_TX_2 M48 TMDS_B_D0 CX1115 0.1UF/10V DVI_TX3+_C 48
PEG_TX_3 M39 TMDS_B_CLK CX1104 0.1UF/10V DVI_CLKB+_C 48
PEG_TX_4 M43
PEG_TX_5 R47
PEG_TX_6 N37
PEG_TX_7 T39
PEG_TX_8 U36
PEG_TX_9 U39
PEG_TX_10 Y39
PEG_TX_11 Y46
PEG_TX_12 AA36
PEG_TX_13 AA39
PEG_TX_14 AD42
PEG_TX_15 AD46

CANTIGA_CHIPSET

T1127 46 LCD_BACKEN
T1119 46 L_BKLT_CTRL
T1120 L_CTRL_DATA
46 EDID_CLK
46 EDID_DAT
+3VS 2.2KOhm RN1125A 2.2KOhm RN1125B
46 LCD_VDD_EN
R1110 2.37KOhm 1%
0Ohm R1123 @
+1.8V
46 LVDS_CLKN
46 LVDS_CLKP
46 LVDS_BCLKN
46 LVDS_BCLKP
46 LVDS_0N
46 LVDS_1N
46 LVDS_2N
46 LVDS_0P
46 LVDS_1P
46 LVDS_2P
46 LVDS_B0N
46 LVDS_B1N
46 LVDS_B2N
46 LVDS_B0P
46 LVDS_B1P
46 LVDS_B2P

45 CRT_DDC_CLK
45 CRT_DDC_DAT
45 DAC_HSYNC RX1106 33Ohm DAC_HSYNC_J
R1119 1.02KOhm CRT_TVO_IREF_J
45 DAC_VSYNC RX1108 33Ohm DAC_VSYNC_J

45 DAC_B
45 DAC_G
45 DAC_R
R1118 150Ohm 1%
R1120 150Ohm 1%
R1115 150Ohm 1%
JP1101 SHORT_PIN CRT_BLUE_J
JP1102 SHORT_PIN CRT_GREEN_J
JP1103 SHORT_PIN CRT_RED_J

Title : Cantiga-DDR2/PEG(2)
Engineer: Peter Lo
Size: Custom
Project Name: Rocky30
Rev: 1.0
Date: Monday, February 04, 2008
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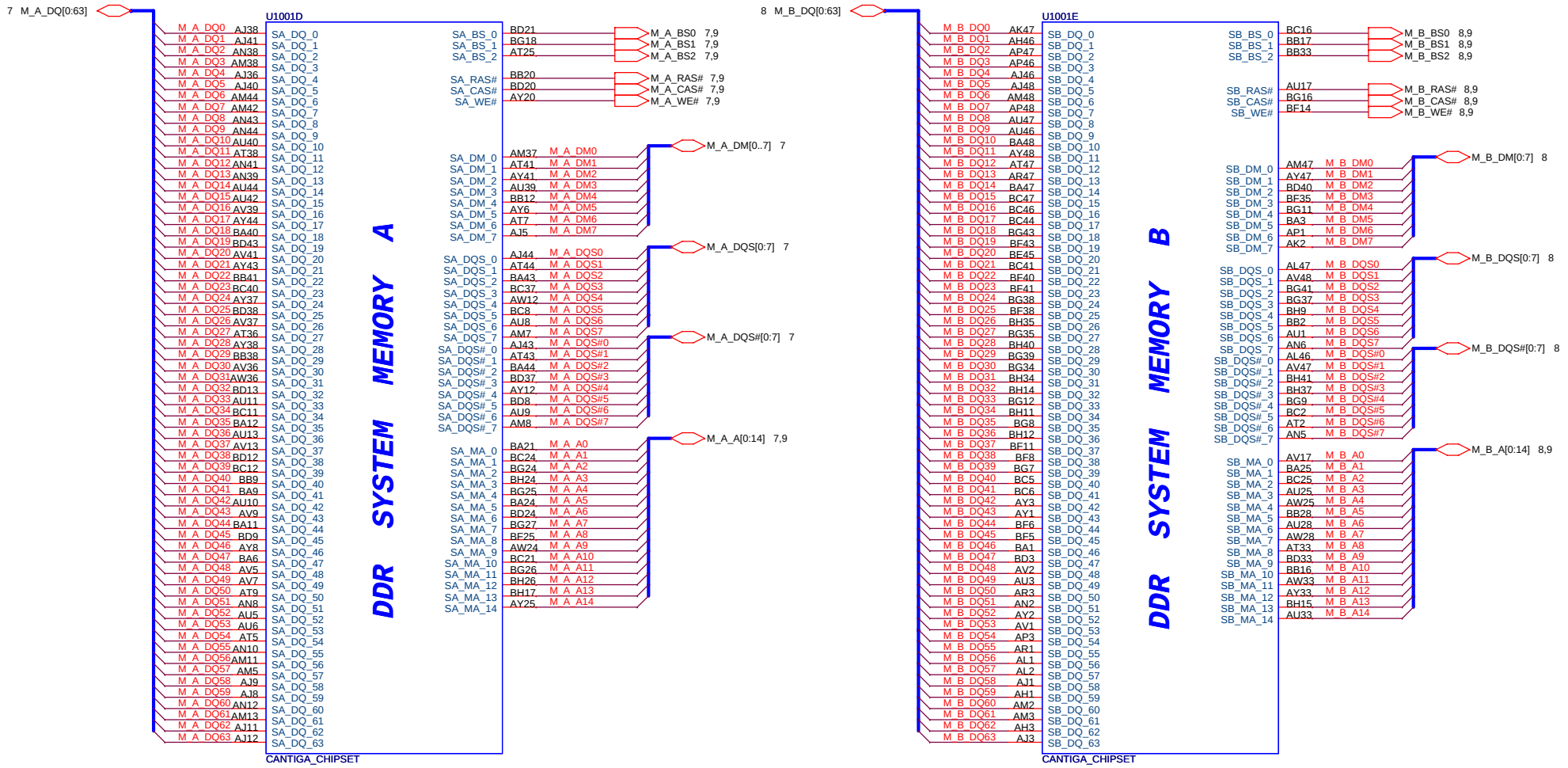
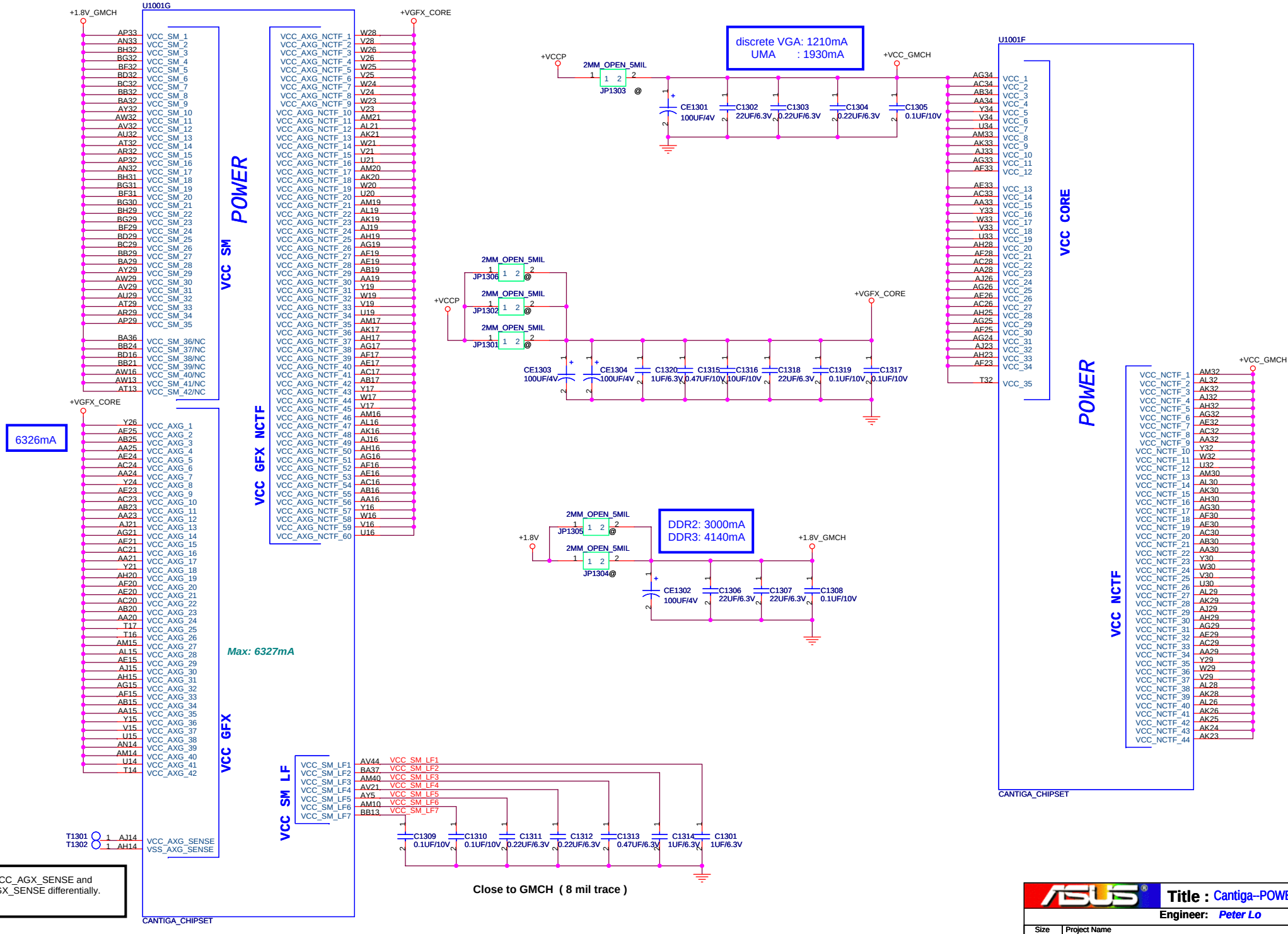
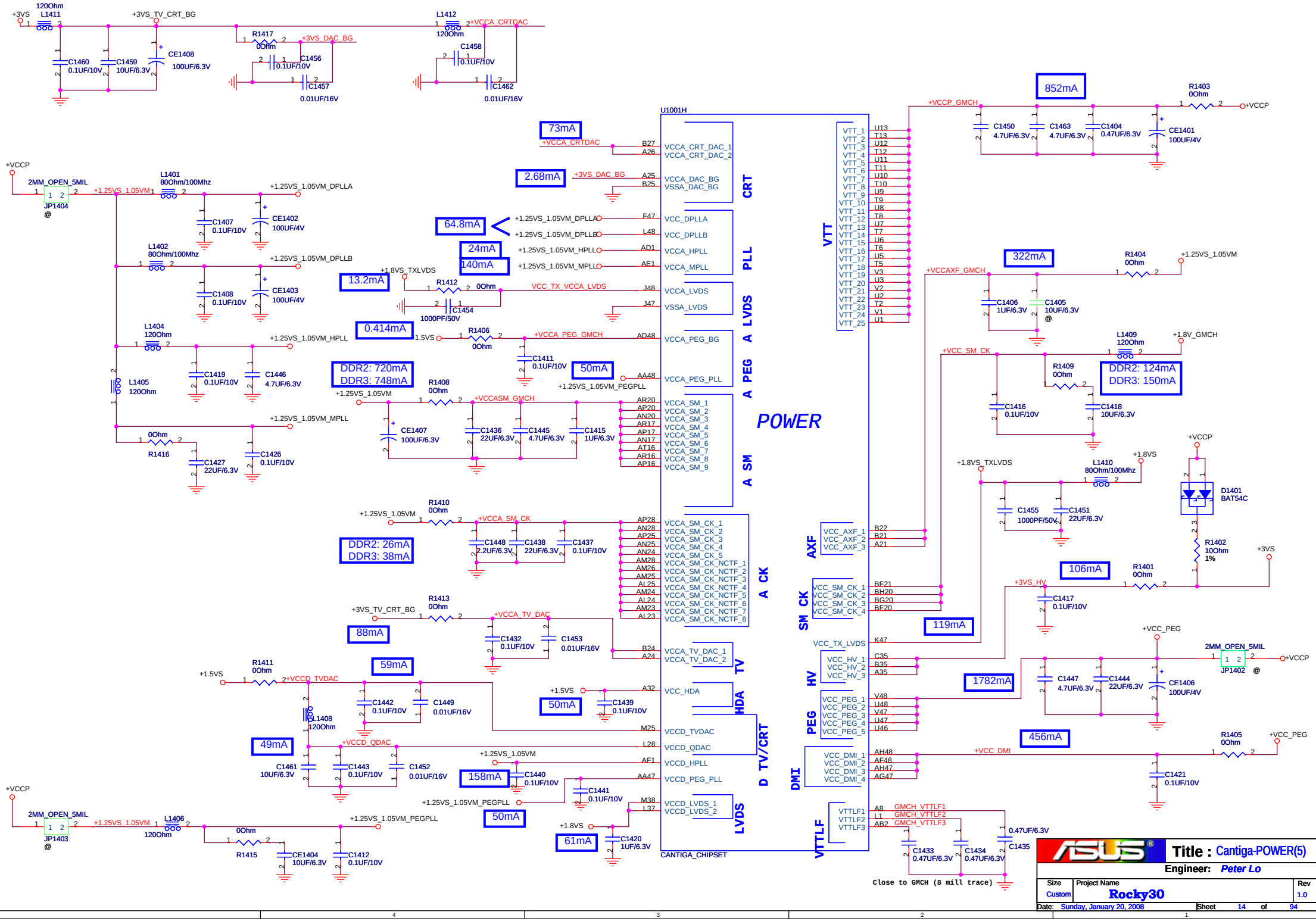


Title : Cantiga--DDR2 (3)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 12 of 94	


U1001G
+1.8V_GMCH
+VGFX_CORE
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
6326mA
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC GFX
Max: 6327mA
T1301
T1302
VCC_AXG_SENSE
VSS_AXG_SENSE
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.
CANTIGA_CHIPSET
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C1309 0.1UF/10V
C1310 0.1UF/10V
C1311 0.22UF/6.3V
C1312 0.22UF/6.3V
C1313 0.47UF/6.3V
C1314 1UF/6.3V
C1301 1UF/6.3V
Close to GMCH (8 mil trace)
discrete VGA: 1210mA
UMA : 1930mA
+VCCP
+VCC_GMCH
2MM_OPEN_5MIL
JP1303 @
CE1301 100UF/4V
C1302 22UF/6.3V
C1303 0.22UF/6.3V
C1304 0.22UF/6.3V
C1305 0.1UF/10V
U1001F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC CORE
JP1306 @
JP1302 @
JP1301 @
CE1303 100UF/4V
CE1304 100UF/4V
C1320 1UF/6.3V
C1315 0.47UF/10V
C1316 10UF/10V
C1318 22UF/6.3V
C1319 0.1UF/10V
C1317 0.1UF/10V
JP1305 @
JP1304@
DDR2: 3000mA
DDR3: 4140mA
+1.8V
CE1302 100UF/4V
C1306 22UF/6.3V
C1307 22UF/6.3V
C1308 0.1UF/10V
CANTIGA_CHIPSET
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
POWER
Title : Cantiga--POWER (4)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Sunday, January 20, 2008
Sheet 13 of 94



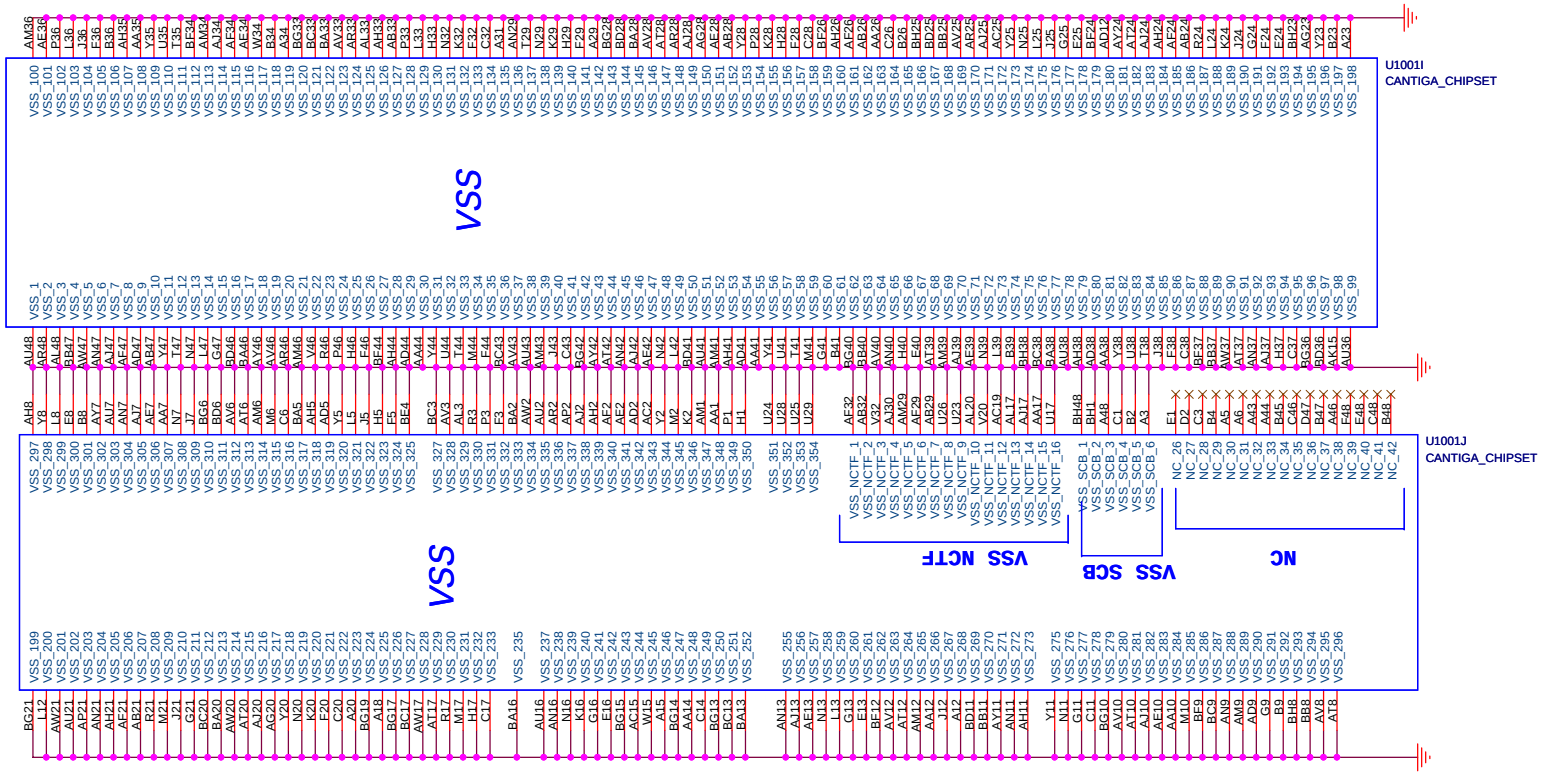
ASUS

Title : Cantiga-POWER(5)

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Sunday, January 20, 2008 Sheet 14 of 94



11 MCH_CFG_5 — R1509 2.21KOhm @ 1%

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

11 MCH_CFG_6 — R1514 2.21KOhm @ 1%

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

11 MCH_CFG_7 — R1511 2.21KOhm @ 1%

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite

HIGH = With confidentiality (Default)

LOW = Without confidentiality

11 MCH_CFG_9 — R1512 2.21KOhm @ 1%

CFG9 : PCIE GRAPHIC LANE

LOW = Reverse Lanes

HIGH = Normal Operation (Default)

11 MCH_CFG_16 — R1507 2.21KOhm @ 1%

CFG16 : FSB Dynamic ODT

HIGH = Ensable (Default)

LOW = Disable

11 MCH_CFG_10 — R1508 2.21KOhm @ 1%

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

11 MCH_CFG_12 — R1513 2.21KOhm @ 1%

11 MCH_CFG_13 — R1510 2.21KOhm @ 1%

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

+3VS — R1503 4.02KOhm @ 1% — 11 MCH_CFG_19

CFG19 : DMI Lane Reversal

LOW = NORMAL (default)

HIGH = Reverse Lanes

+3VS — R1506 4.02KOhm @ 1% — 11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational (Default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

Title : Cantiga-GND		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 15 of 94	

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 16 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 17 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

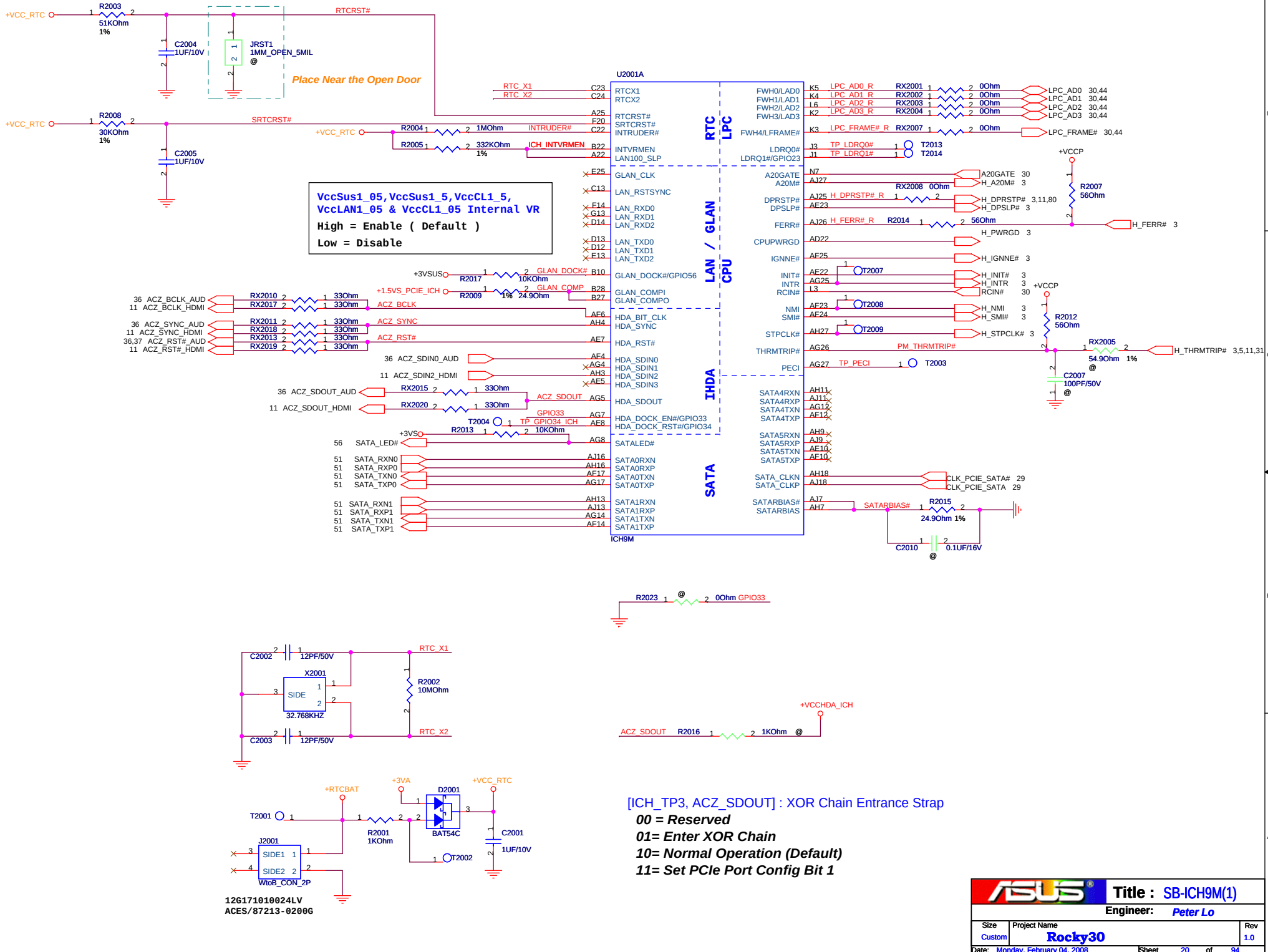
Date: Thursday, October 18, 2007 Sheet 18 of 94

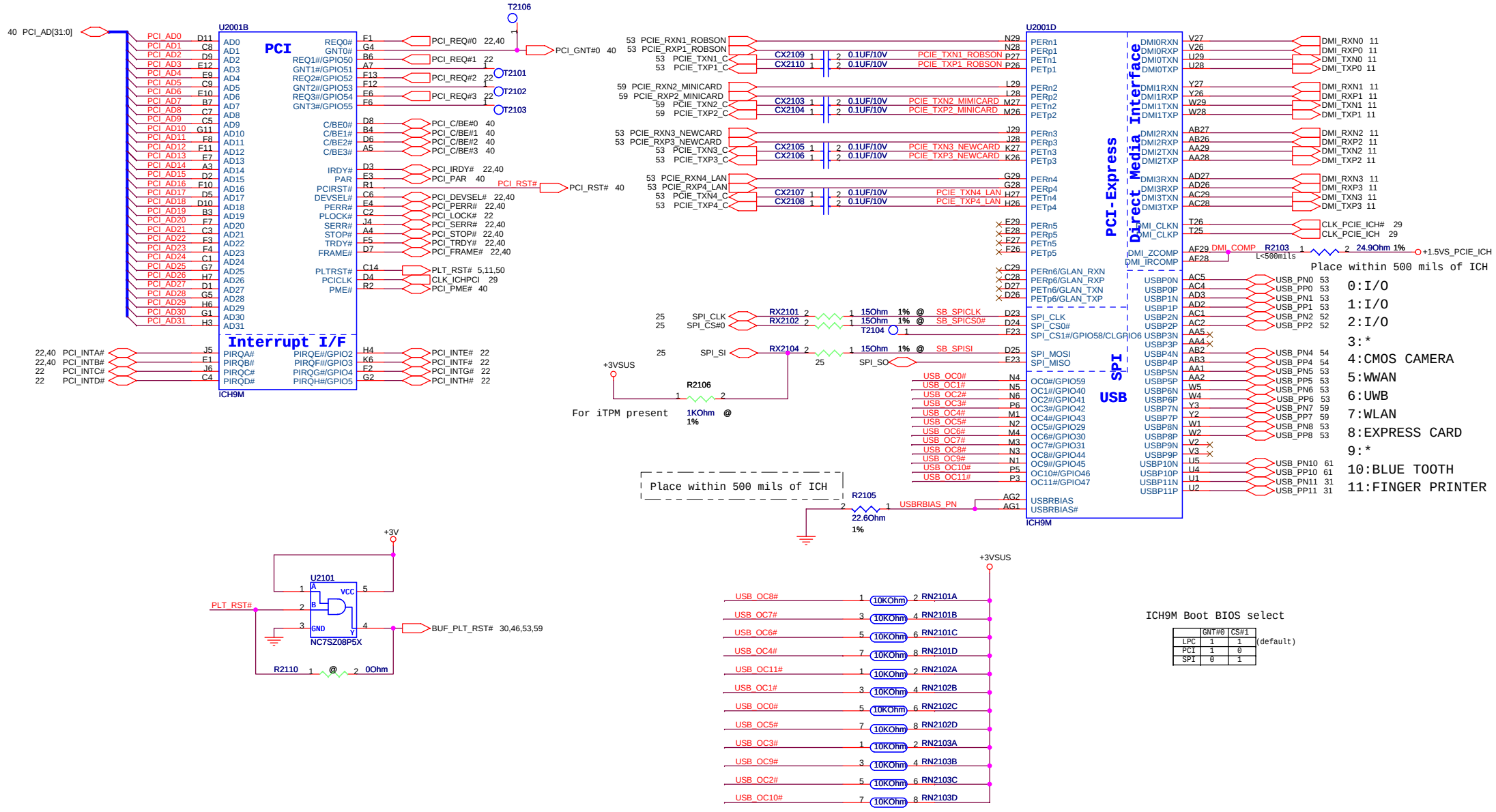
Title : ***

Engineer: Peter Lo

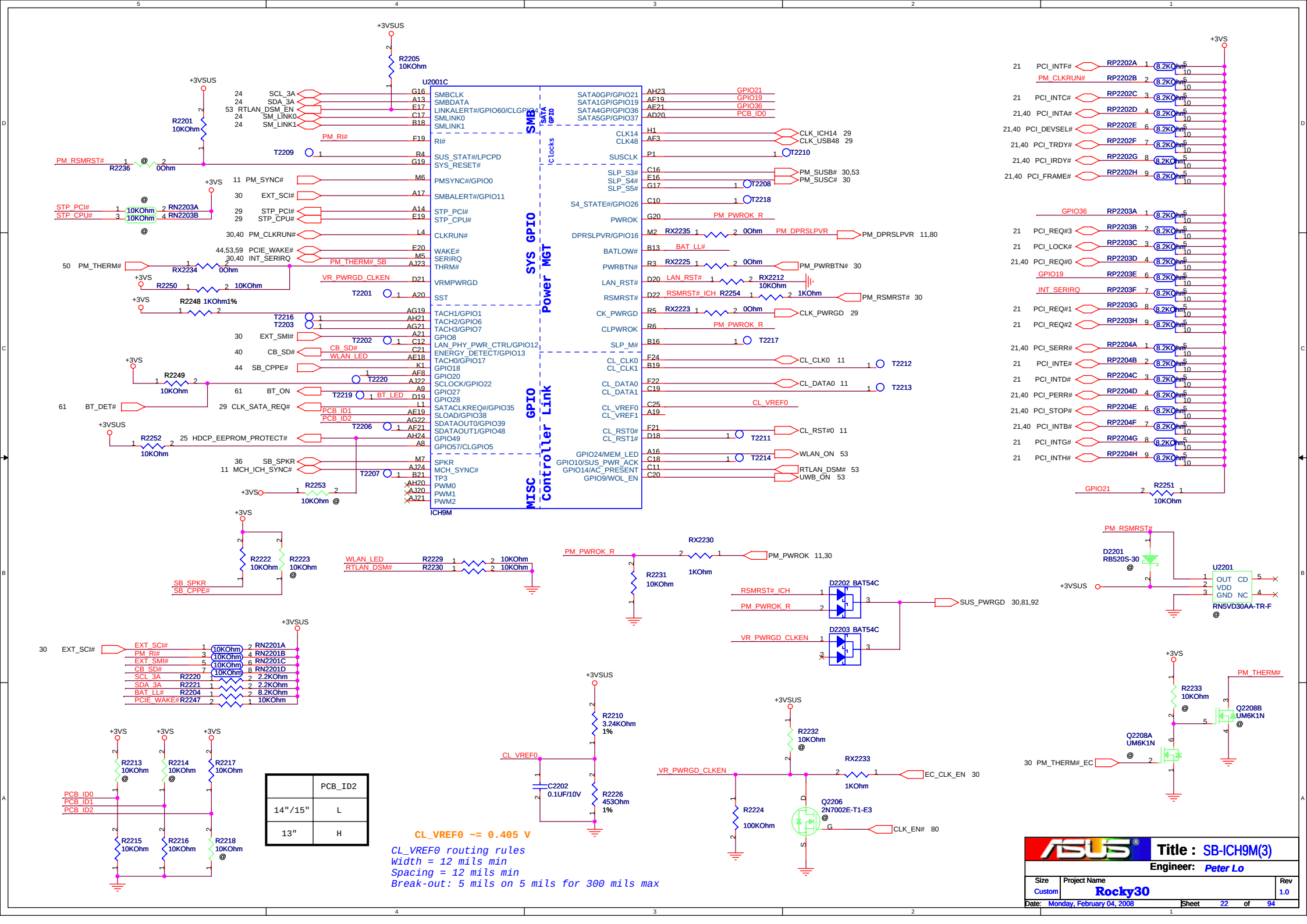
Size	Project Name	Rev
B	Rocky30	1.0

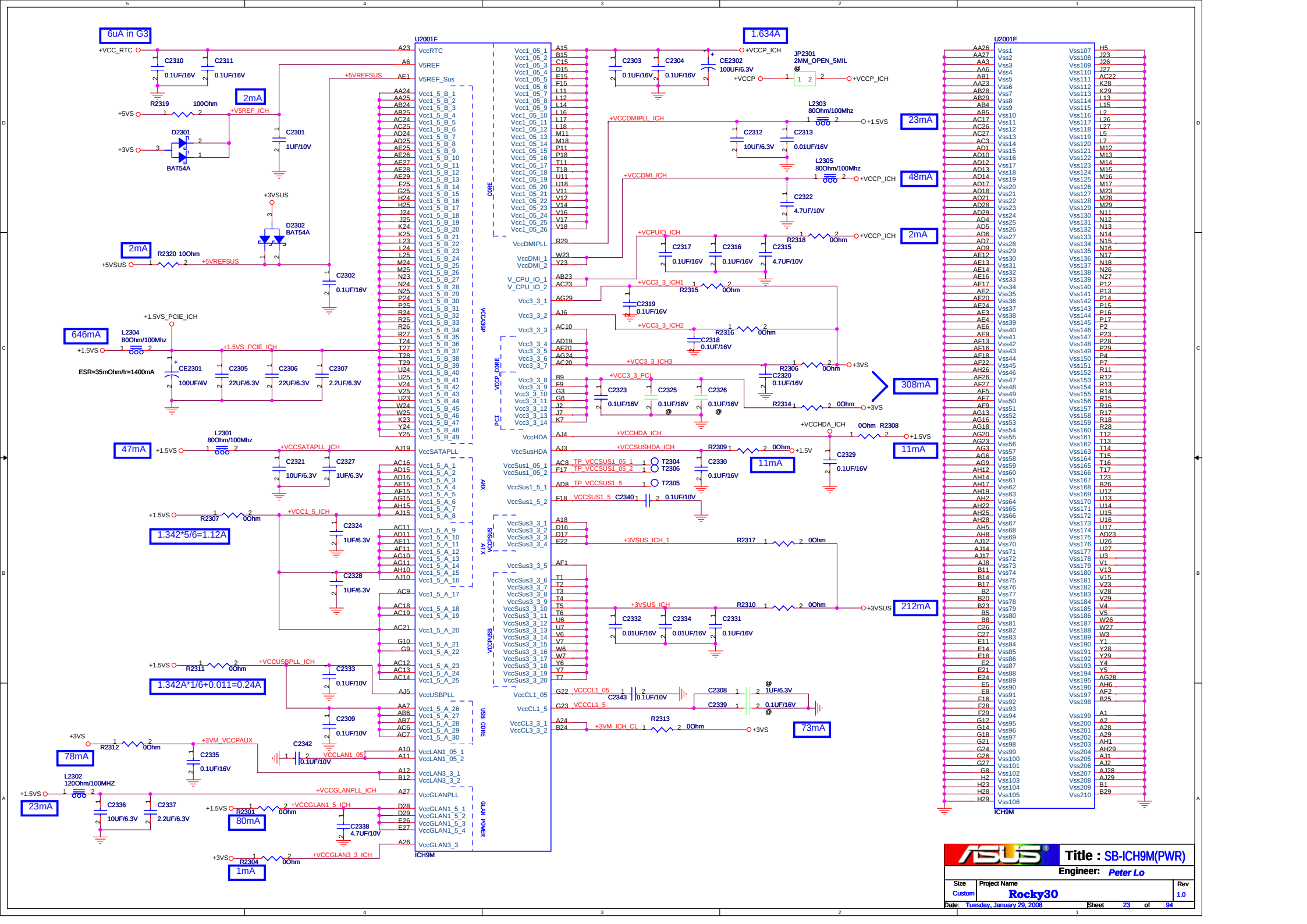
Date: Thursday, October 18, 2007 Sheet 19 of 94


R2003 51KOhm 1%
C2004 1UF/10V
JRST1 1MM_OPEN_5MIL @
Place Near the Open Door
RTCRST#
R2008 30KOhm 1%
C2005 1UF/10V
SRTCRST#
R2004 1MOhm
R2005 332KOhm 1%
INTRUDER#
ICH_INTVRMEN
VccSus1_05,VccSus1_5,VccCL1_5,
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
U2001A
RTC_X1
RTC_X2
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
CPU
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA
ICH9M
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_AD0_R
LPC_AD1_R
LPC_AD2_R
LPC_AD3_R
LPC_FRAME#_R
TP_LDRQ0#
TP_LDRQ1#
T2013
T2014
RX2001 0Ohm
RX2002 0Ohm
RX2003 0Ohm
RX2004 0Ohm
RX2007 0Ohm
LPC_AD0 30,44
LPC_AD1 30,44
LPC_AD2 30,44
LPC_AD3 30,44
LPC_FRAME# 30,44
+VCCP
R2007 56Ohm
RX2008 0Ohm
H_DPRSTP# 3,11,80
H_DPSLP# 3
H_FERR# 3
R2014 56Ohm
H_PWRGD 3
H_IGNNE# 3
T2007
H_INIT# 3
H_INTR 3
RCIN# 30
T2008
H_NMI 3
H_SMI# 3
T2009
H_STPCLK# 3
R2012 56Ohm
PM_THRMTRIP#
RX2005 54.9Ohm 1%
H_THRMTRIP# 3,5,11,31
C2007 100PF/50V @
TP_PECI
T2003
CLK_PCIE_SATA# 29
CLK_PCIE_SATA 29
R2015 24.9Ohm 1%
C2010 0.1UF/16V @
+3VSUS
R2017 10KOhm
GLAN_DOCK#
GLAN_COMP
+1.5VS_PCIE_ICH
R2009 24.9Ohm 1%
36 ACZ_BCLK_AUD
11 ACZ_BCLK_HDMI
ACZ_BCLK
RX2010 33Ohm
RX2017 33Ohm
36 ACZ_SYNC_AUD
11 ACZ_SYNC_HDMI
36,37 ACZ_RST#_AUD
11 ACZ_RST#_HDMI
ACZ_SYNC
ACZ_RST#
RX2011 33Ohm
RX2018 33Ohm
RX2013 33Ohm
RX2019 33Ohm
36 ACZ_SDIN0_AUD
11 ACZ_SDIN2_HDMI
36 ACZ_SDOUT_AUD
11 ACZ_SDOUT_HDMI
ACZ_SDOUT
RX2015 33Ohm
RX2020 33Ohm
GPIO33
T2004
TP_GPIO34_ICH
R2013 10KOhm
+3VS
56 SATA_LED#
51 SATA_RXN0
51 SATA_RXP0
51 SATA_TXN0
51 SATA_TXP0
51 SATA_RXN1
51 SATA_RXP1
51 SATA_TXN1
51 SATA_TXP1
R2023 @ 0Ohm GPIO33
C2002 12PF/50V
X2001
SIDE
32.768KHZ
C2003 12PF/50V
R2002 10MOhm
RTC_X1
RTC_X2
+VCCHDA_ICH
ACZ_SDOUT
R2016 1KOhm @
+RTCBAT
+3VA
+VCC_RTC
T2001
R2001 1KOhm
D2001
BAT54C
T2002
C2001 1UF/10V
J2001
SIDE1
SIDE2
WtoB_CON_2P
12G171010024LV
ACES/87213-0200G
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
Title : SB-ICH9M(1)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Monday, February 04, 2008
Sheet 20 of 94

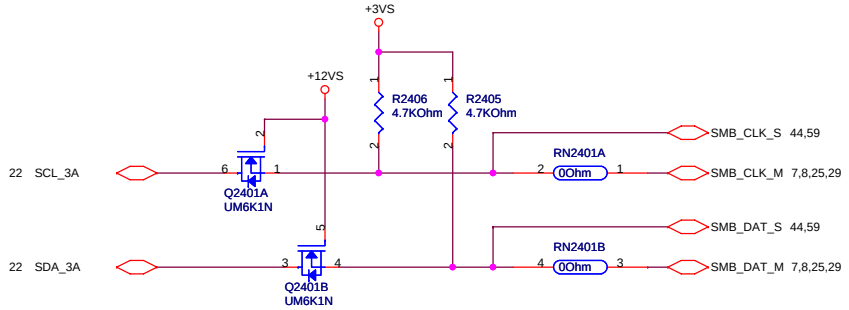


Title :	SB-ICH9M(2)
Engineer:	Peter Lo
Size	Custom
Project Name	Rocky30
Rev	1.0
Date:	Monday, February 04, 2008
Sheet	21 of 94


U2001C
ICH9M
SMB
GPIO
SATA GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
I C Locks
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
+3VSUS
+3VS
R2205 10KOhm
R2201 10KOhm
R2236 0Ohm
RN2203A 10KOhm
RN2203B 10KOhm
RX2234 0Ohm
R2250 10KOhm
R2248 1KOhm1%
R2249 10KOhm
R2252 10KOhm
R2253 10KOhm @
T2209
T2201
T2216
T2203
T2202
T2220
T2219
T2206
T2207
SCL_3A
SDA_3A
RTLAN_DSM_EN
SM_LINK0
SM_LINK1
PM_RI#
PM_SYNC#
EXT_SCI#
STP_PCI#
STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THERM#
VR_PWRGD_CLKEN
EXT_SMI#
CB_SD#
WLAN_LED
SB_CPPE#
BT_ON
BT_LED
CLK_SATA_REQ#
PCB_ID1
PCB_ID2
HDCP_EEPROM_PROTECT#
SB_SPKR
MCH_ICH_SYNC#
BT_DET#
RX2235 0Ohm
RX2225 0Ohm
RX2223 0Ohm
RX2212 10KOhm
RX2254 1KOhm
PM_PWROK_R
LAN_RST#
RSMRST_ICH
PM_DPRSLPVR
PM_PWRBTN#
PM_RSMRST#
CLK_PWRGD
CL_CLK0
CL_DATA0
CL_VREF0
CL_RST0#
WLAN_ON
RTLAN_DSM#
UWB_ON
T2210
T2208
T2218
T2217
T2212
T2213
T2211
T2214
PM_SUSB# 30,53
PM_SUSC# 30
CLK_ICH14 29
CLK_USB48 29
PCB_ID0
GPIO21
GPIO19
GPIO36
PM_DPRSLPVR 11,80
PM_PWRBTN# 30
PM_RSMRST# 30
CLK_PWRGD 29
CL_CLK0 11
CL_DATA0 11
CL_RST#0 11
WLAN_ON 53
RTLAN_DSM# 53
UWB_ON 53
RP2202A 8.2KOhm
RP2202B 8.2KOhm
RP2202C 8.2KOhm
RP2202D 8.2KOhm
RP2202E 8.2KOhm
RP2202F 8.2KOhm
RP2202G 8.2KOhm
RP2202H 8.2KOhm
RP2203A 8.2KOhm
RP2203B 8.2KOhm
RP2203C 8.2KOhm
RP2203D 8.2KOhm
RP2203E 8.2KOhm
RP2203F 8.2KOhm
RP2203G 8.2KOhm
RP2203H 8.2KOhm
RP2204A 8.2KOhm
RP2204B 8.2KOhm
RP2204C 8.2KOhm
RP2204D 8.2KOhm
RP2204E 8.2KOhm
RP2204F 8.2KOhm
RP2204G 8.2KOhm
RP2204H 8.2KOhm
R2251 10KOhm
PCI_INTF#
PM_CLKRUN#
PCI_INTC#
PCI_INTA#
PCI_DEVSEL#
PCI_TRDY#
PCI_IRDY#
PCI_FRAME#
PCI_REQ#3
PCI_LOCK#
PCI_REQ#0
INT_SERIRQ
PCI_REQ#1
PCI_REQ#2
PCI_SERR#
PCI_INTE#
PCI_INTD#
PCI_PERR#
PCI_STOP#
PCI_INTB#
PCI_INTG#
PCI_INTH#
R2222 10KOhm
R2223 10KOhm @
R2229 10KOhm
R2230 10KOhm
RX2230
R2231 10KOhm
1KOhm
PM_PWROK 11,30
D2202 BAT54C
D2203 BAT54C
SUS_PWRGD 30,81,92
D2201 RB520S-30 @
U2201
RN5VD30AA-TR-F @
RN2201A 10KOhm
RN2201B 10KOhm
RN2201C 10KOhm
RN2201D 10KOhm
R2220 2.2KOhm
R2221 2.2KOhm
R2204 8.2KOhm
R2247 10KOhm
R2213 10KOhm @
R2214 10KOhm @
R2217 10KOhm
R2215 10KOhm
R2216 10KOhm
R2218 10KOhm @
PCB_ID0
PCB_ID1
PCB_ID2
R2210 3.24KOhm 1%
C2202 0.1UF/10V
R2226 453Ohm 1%
CL_VREF0
R2232 10KOhm @
RX2233 1KOhm
R2224 100KOhm
Q2206 2N7002E-T1-E3 @
EC_CLK_EN 30
CLK_EN# 80
R2233 10KOhm @
Q2208B UM6K1N @
Q2208A UM6K1N @
PM_THERM#_EC
PCB_ID2 | PCB_ID1 | PCB_ID0
14"/15" | L | L
13" | H | H
CL_VREF0 ~= 0.405 V
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
Title : SB-ICH9M(3)
Engineer: Peter Lo
Size: Custom
Project Name: Rocky30
Rev: 1.0
Date: Monday, February 04, 2008
Sheet 22 of 94


6uA in G3
2mA
2mA
646mA
47mA
1.342*5/6=1.12A
1.342A*1/6+0.011=0.24A
78mA
23mA
80mA
1mA
1.634A
23mA
48mA
2mA
308mA
11mA
212mA
73mA
U2001F
U2001E
ICH9M
Title : SB-ICH9M(PWR)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.0
Date: Tuesday, January 29, 2008
Sheet 23 of 94

ICH9-M



ICH9M

NEWCARD,WLAN

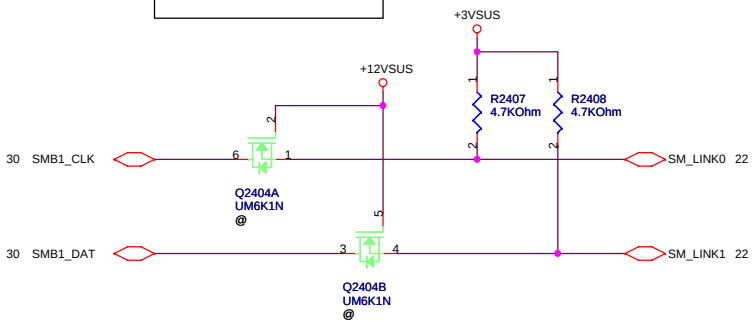
CLOCK GEN
SO-DIMM0 , SO-DIMM1

NEWCARD,WLAN

CLOCK GEN
SO-DIMM0 , SO-DIMM1

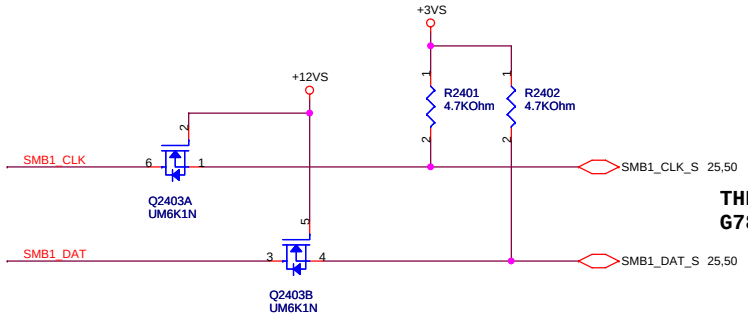
EC

Don't support iAMT
Remove ME-EC SMBus.



EC

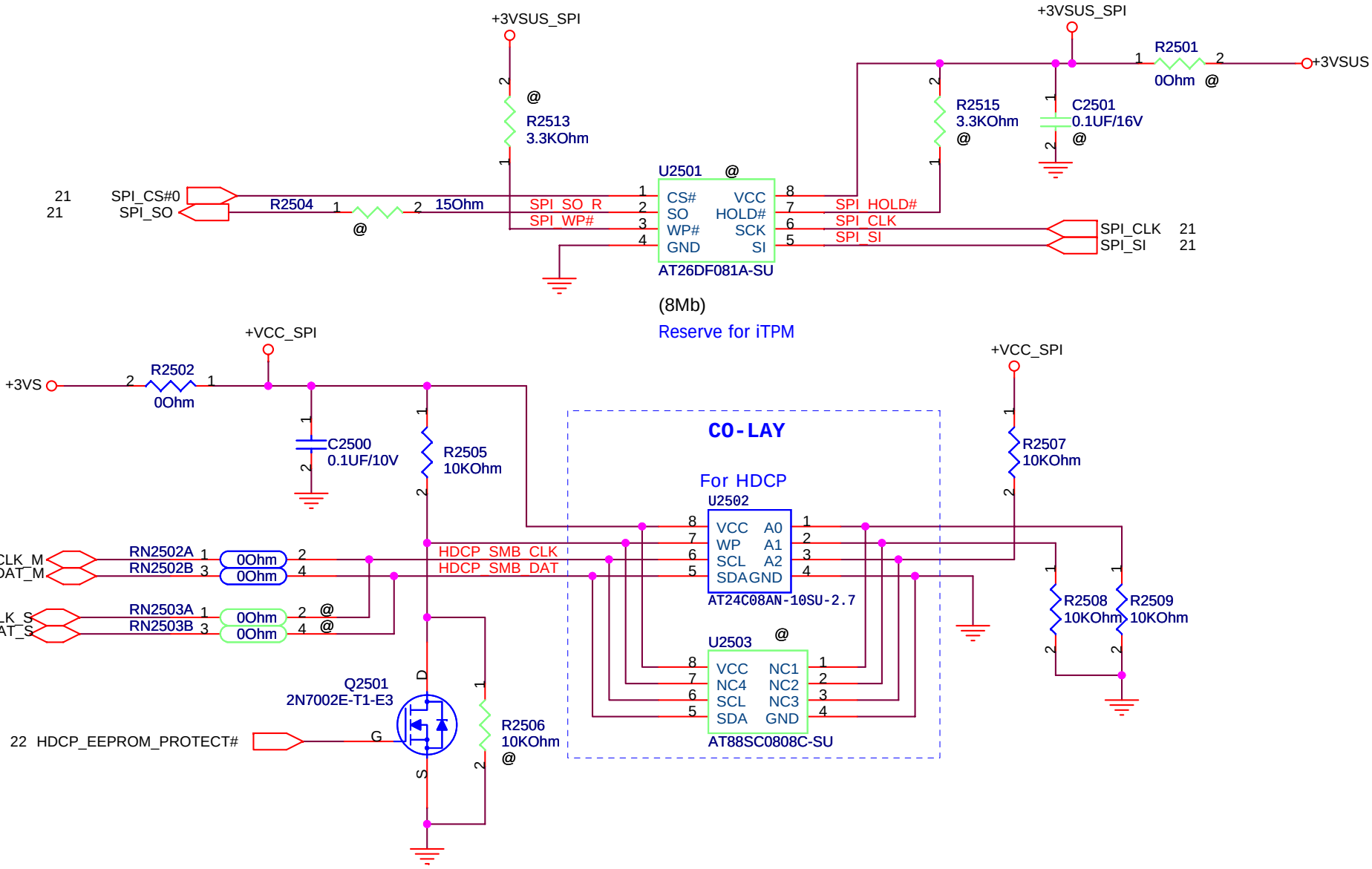
SB



EC

THERMAL IC
G781,G781-1

Title : ICH9M-Other		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 24 of 94	



U2502-AT24C08A :
Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509
Nostuff : R2505

U2503-AT88SC0808C :
Stuff : U2503
Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

ASUS	Title : SPI ROM	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 25 of 94	

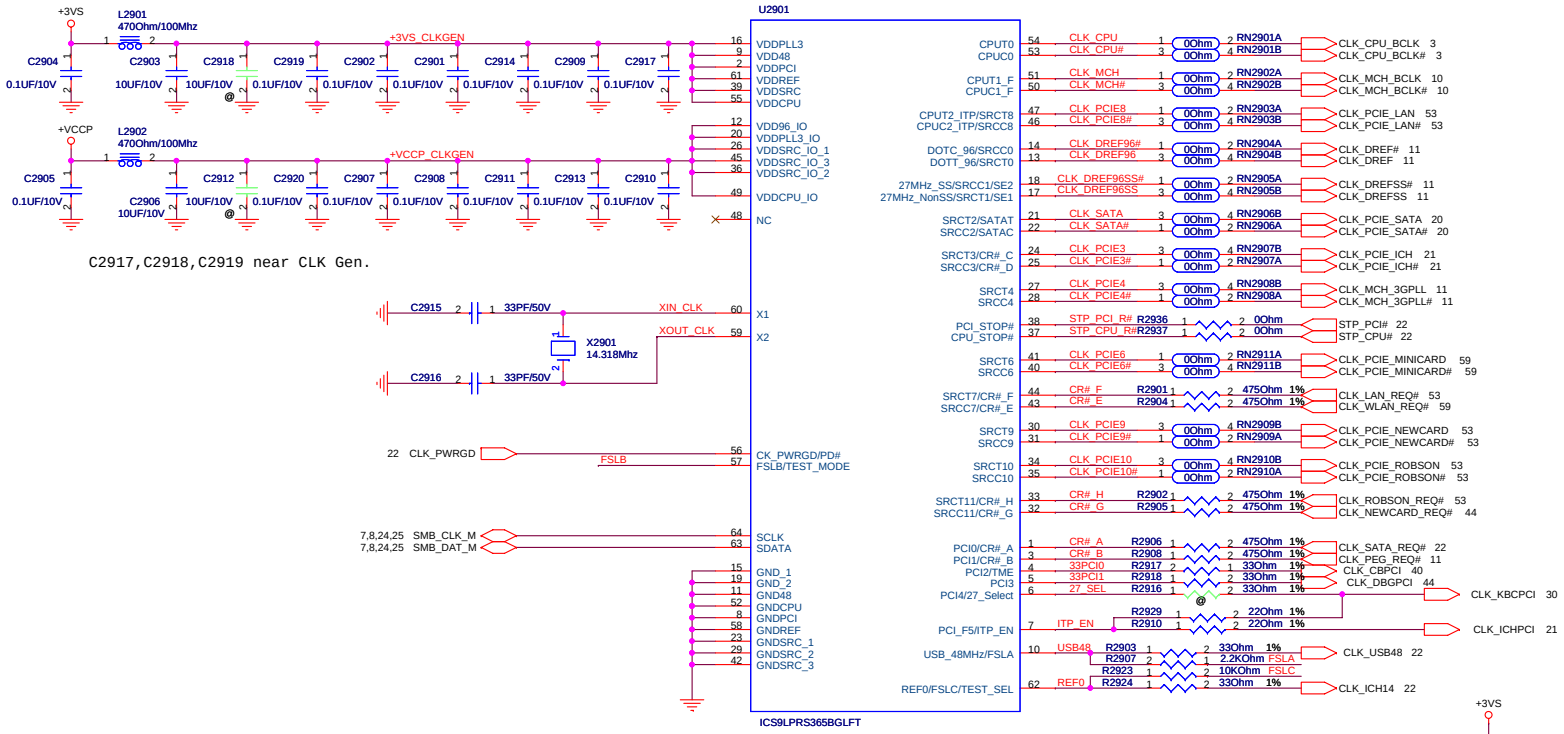
Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	26 of 94

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	27 of 94

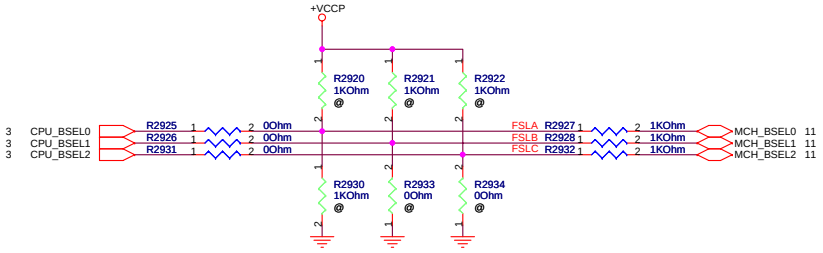
Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	28 of 94

+VCCP → +VCCP 5,10,11,13,14,20,23,80,82

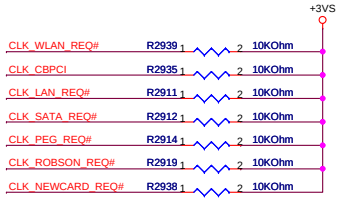
+3VS → +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92



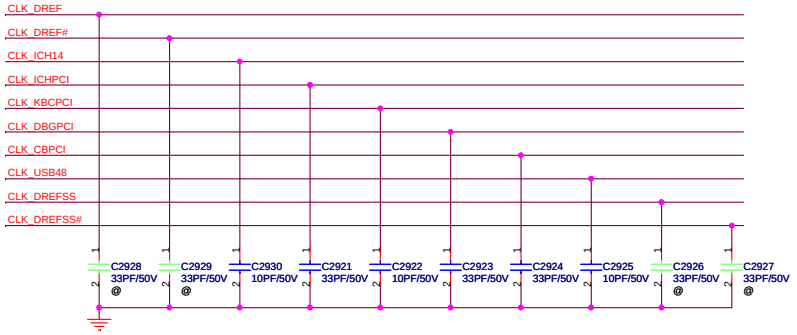
C2917,C2918,C2919 near CLK Gen.



	FSLC	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



C2921, C2922, C2923, C2924, C2925, C2926,
C2927, C2928, C2929, C2930 near CLK Gen.

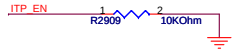


CR#_A	0 = SRC 0 1 = SRC 2 SATA
CR#_B	0 = SRC 1 1 = SRC 4 MCH
CR#_C	0 = SRC 0 1 = SRC 2
CR#_D	0 = SRC 1 1 = SRC 4
CR#_E	SRC 6 WLAN
CR#_F	SRC 8 LAN
CR#_G	SRC 9 New Card
CR#_H	SRC 10 Robson

Latched Input Select

0 = SRC 8
1 = CPU_ITP CLK

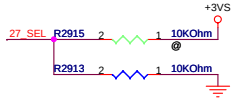
Decide pin 46,47



27_Select =0,
pin#13/14=DOT96;
pin#17/18=LCD_SST;

Decide pin 13/14,17/18

27_Select =1,
pin#13/14=SRC0;
pin#17/18=27MHz non-spread SE clock;



For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.

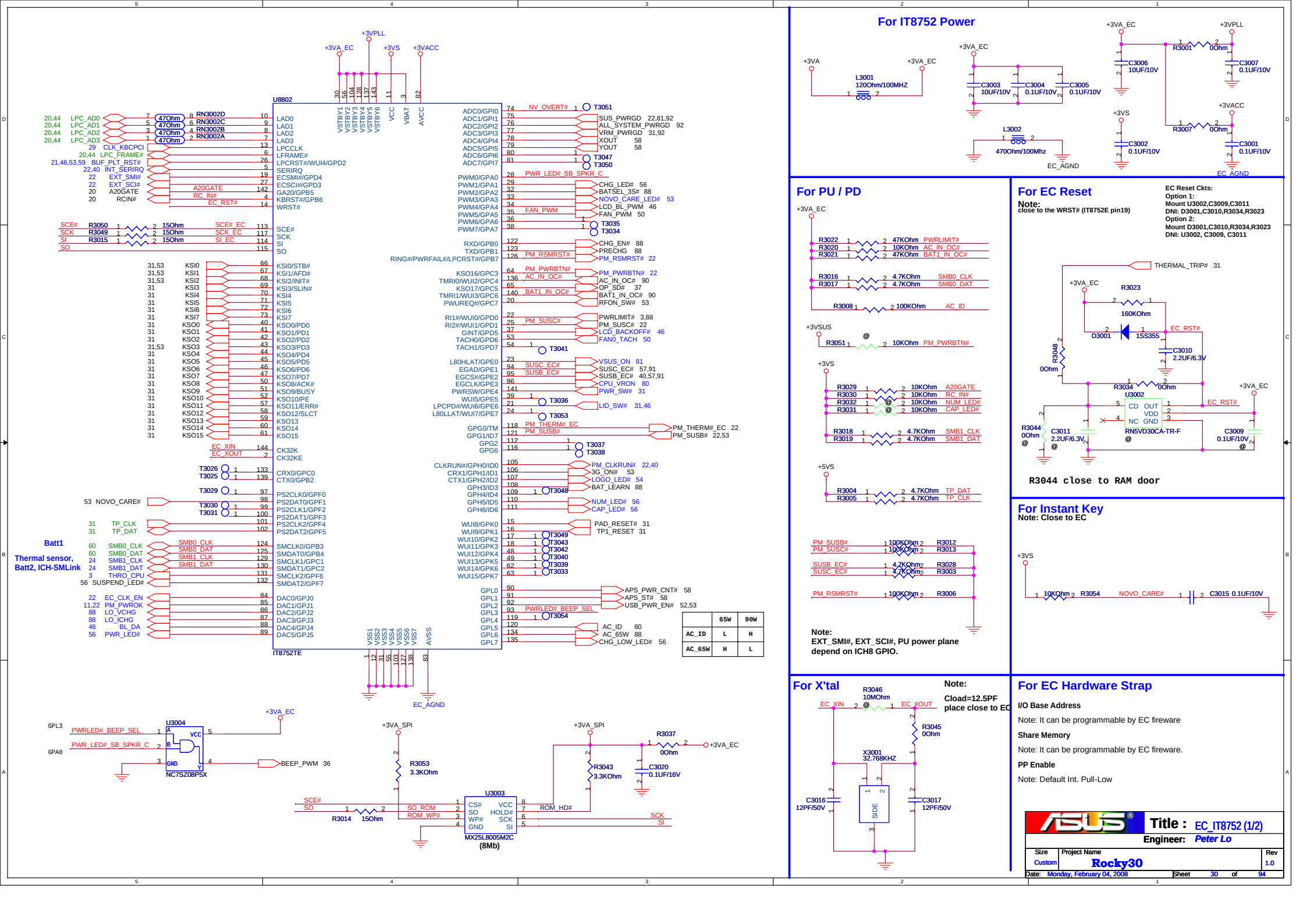
ASUS

Title : ICS9LPR365

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 29 of 94



	65W	90W
AC_ID	L	H
AC_65W	H	L

For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R3044 close to RAM door

For Instant Key

Note: Close to EC

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

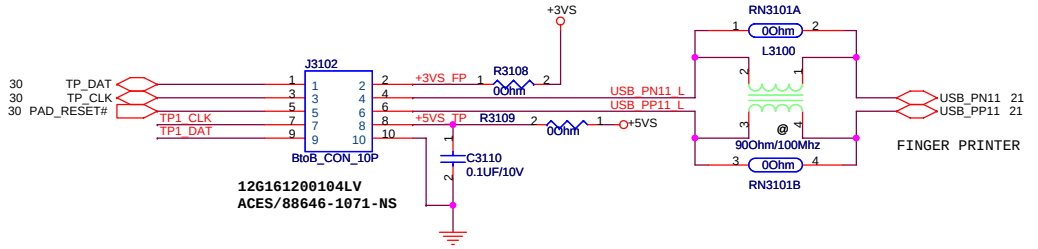
PP Enable

Note: Default Int. Pull-Low

Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 30 of 94	

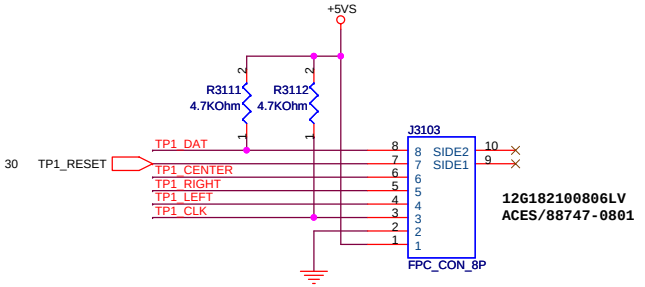
Title : EC_IT8752 (1/2)
Engineer: *Peter Lo*

TOUCH PAD CONN

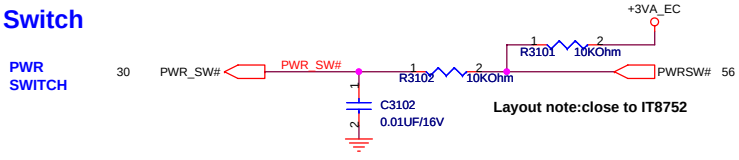


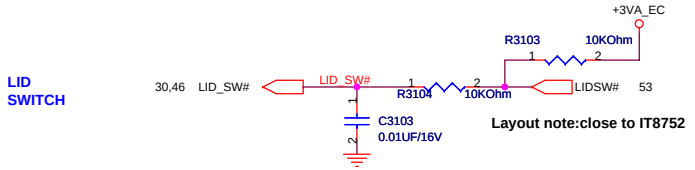
TP : Touch Pad
TP1: Track Point

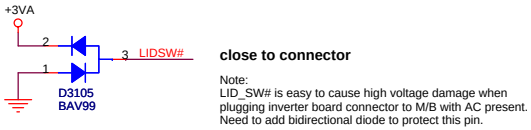
TRACK POINT CONN



For Switch

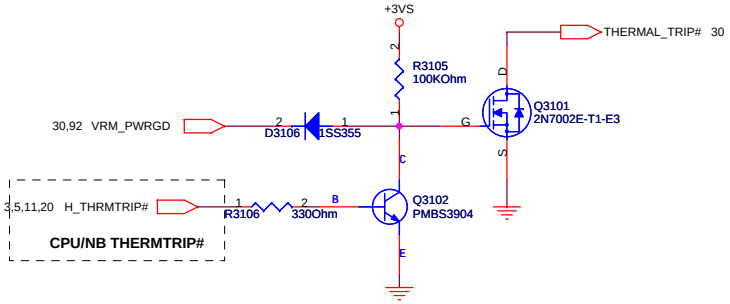




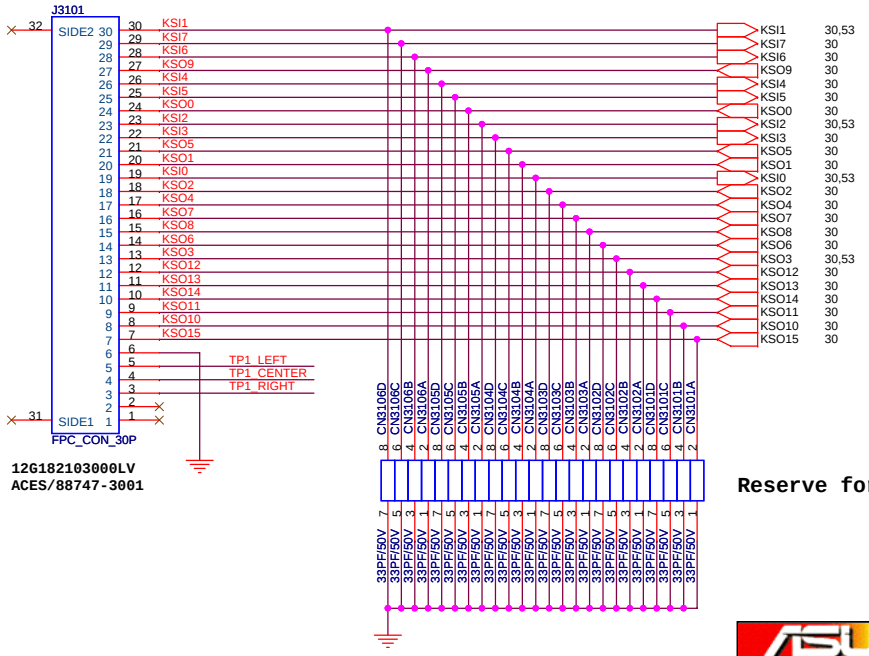


Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

For Thermal Control Method



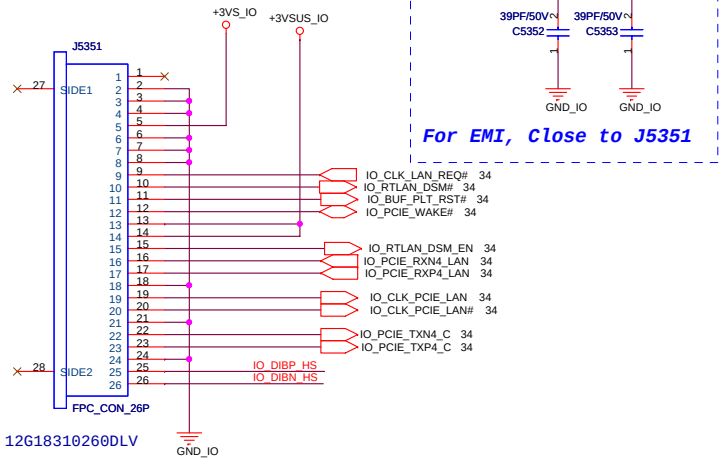
Keyboard Connector

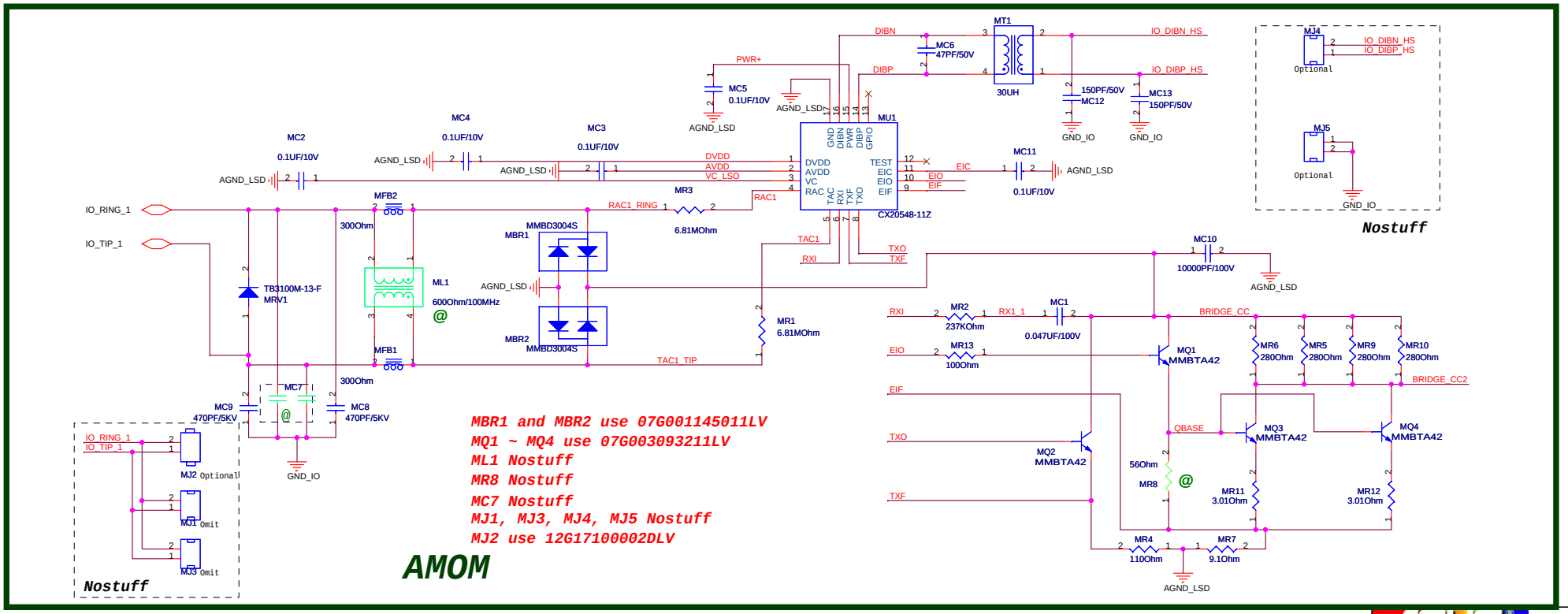


Title :	EC_IT8752 (2/2)
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date:	Monday, February 04, 2008
Sheet	31 of 94

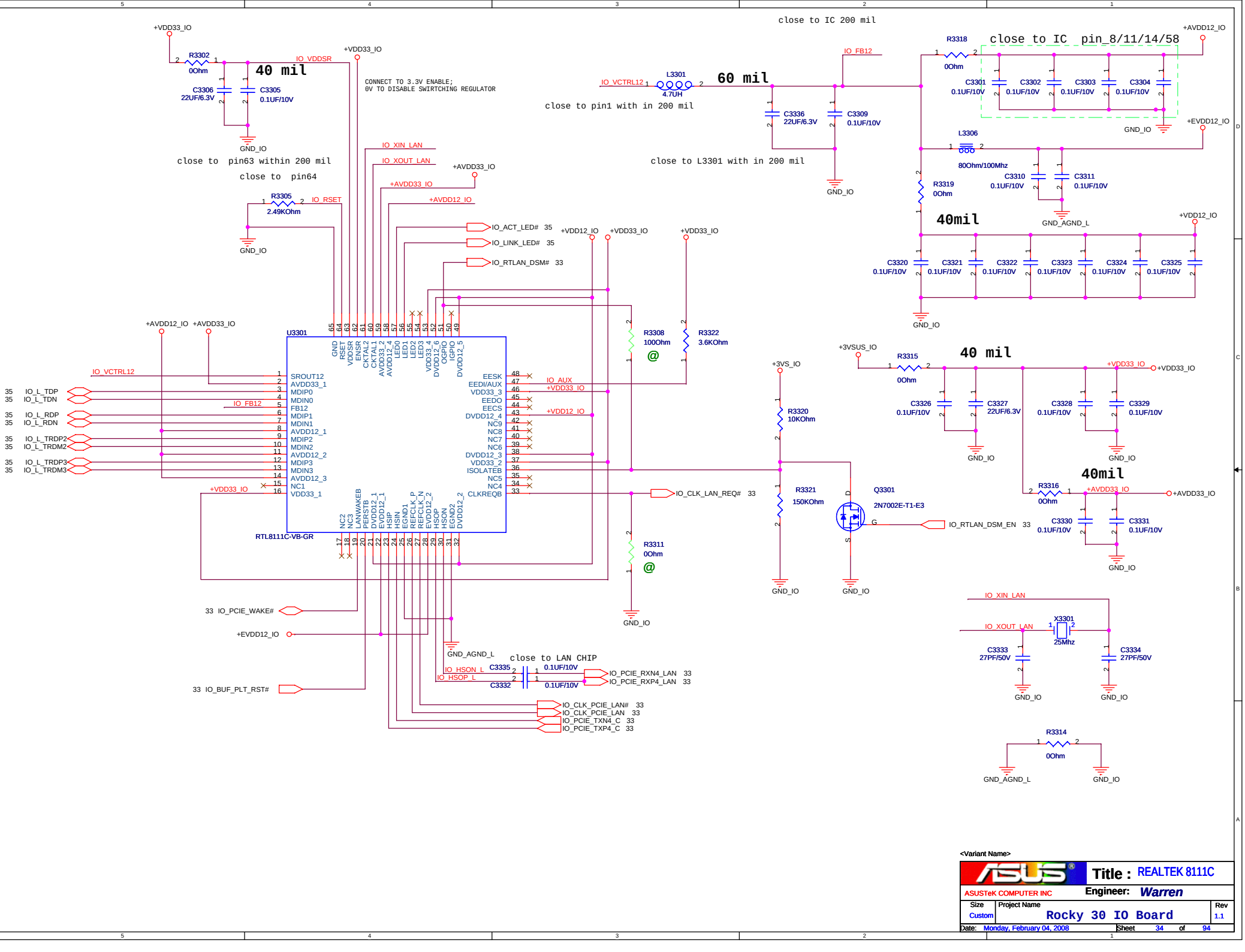
Title :	*
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date:	Sunday, January 20, 2008
Sheet	32 of 94

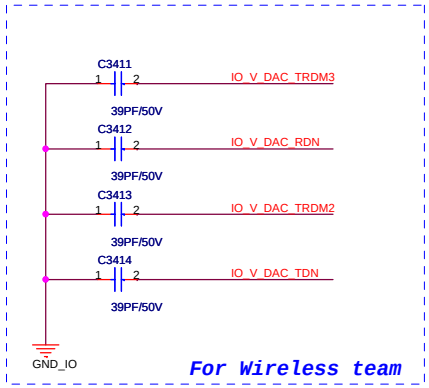
IO BOARD

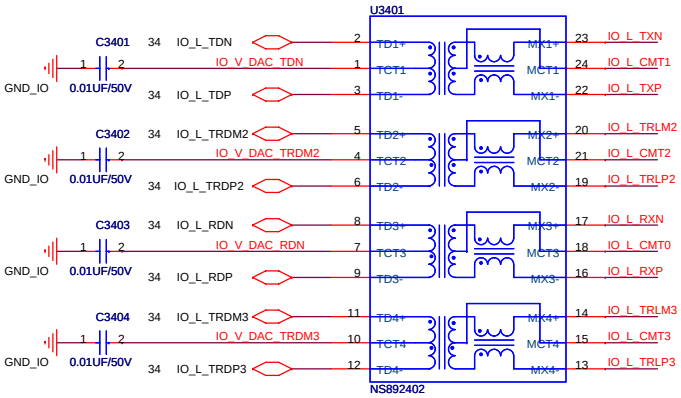




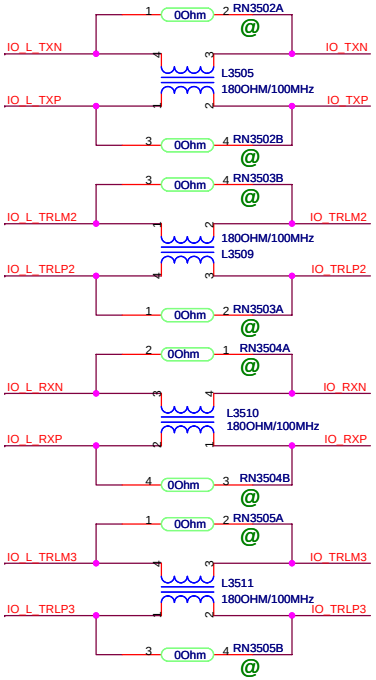
ASUSALPHA ODM NB1	Title : IO BRD CONN&DAA	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 30 IO Board	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 33 of 94	

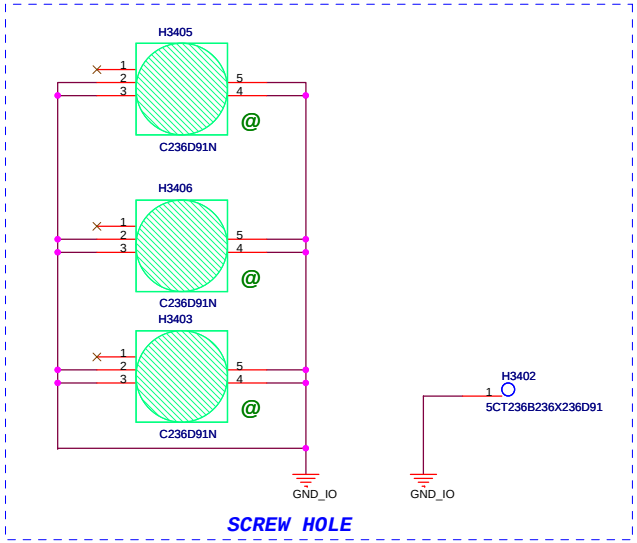

close to IC 200 mil
close to IC pin_8/11/14/58
close to pin1 with in 200 mil
close to L3301 with in 200 mil
close to pin63 within 200 mil
close to pin64
close to LAN CHIP
CONNECT TO 3.3V ENABLE;
0V TO DISABLE SWIRTCHING REGULATOR
40 mil
60 mil
40mil
RTL8111C-VB-GR
U3301
+VDD33_IO
+AVDD12_IO
+EVDD12_IO
+VDD12_IO
+3VS_IO
+3VSUS_IO
GND_IO
GND_AGND_L
IO_XIN_LAN
IO_XOUT_LAN
IO_FB12
IO_RSET
IO_VCTRL12
IO_AUX
IO_ACT_LED# 35
IO_LINK_LED# 35
IO_RTLAN_DSM# 33
IO_CLK_LAN_REQ# 33
IO_RTLAN_DSM_EN 33
33 IO_PCIE_WAKE#
33 IO_BUF_PLT_RST#
IO_HSON_L
IO_HSOP_L
IO_PCIE_RXN4_LAN 33
IO_PCIE_RXP4_LAN 33
IO_CLK_PCIE_LAN# 33
IO_CLK_PCIE_LAN 33
IO_PCIE_TXN4_C 33
IO_PCIE_TXP4_C 33
R3302 0Ohm
R3305 2.49KOhm
R3308 100Ohm @
R3322 3.6KOhm
R3320 10KOhm
R3321 150KOhm
R3311 0Ohm @
R3318 0Ohm
R3319 0Ohm
R3315 0Ohm
R3316 0Ohm
R3314 0Ohm
L3301 4.7UH
L3306 80Ohm/100Mhz
Q3301 2N7002E-T1-E3
X3301 25Mhz
C3306 22UF/6.3V
C3305 0.1UF/10V
C3336 22UF/6.3V
C3309 0.1UF/10V
C3301 0.1UF/10V
C3302 0.1UF/10V
C3303 0.1UF/10V
C3304 0.1UF/10V
C3310 0.1UF/10V
C3311 0.1UF/10V
C3320 0.1UF/10V
C3321 0.1UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 0.1UF/10V
C3329 0.1UF/10V
C3330 0.1UF/10V
C3331 0.1UF/10V
C3333 27PF/50V
C3334 27PF/50V
C3335 0.1UF/10V
C3332 0.1UF/10V
SROUT12
AVDD33_1
MDIP0
MDIN0
FB12
MDIP1
MDIN1
AVDD12_1
MDIP2
MDIN2
AVDD12_2
MDIP3
MDIN3
AVDD12_3
NC1
VDD33_1
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
DVDD12_4
NC9
NC8
NC7
NC6
DVDD12_3
VDD33_2
ISOLATEB
NC5
NC4
CLKREQB
GND
RSET
VDDSR
RXER
CKTAL2
CKTAL1
AVDD33_2
AVDD12_4
LED0
LED1
LED2
LED3
VDD33_4
DVDD12_6
OGPIO
IGPIO
DVDD12_5
NC2
WAKE#
PERST#
DVDD12_1
EVDD12_1
HSIP
HSIN
EGND1
REFCLK_P
REFCLK_N
EVDD12_2
HSOP
HSON
EGND2
DVDD12_2
<Variant Name>
Title : REALTEK 8111C
ASUSTeK COMPUTER INC
Engineer: Warren
Size Custom
Project Name Rocky 30 IO Board
Rev 1.1
Date: Monday, February 04, 2008
Sheet 34 of 94

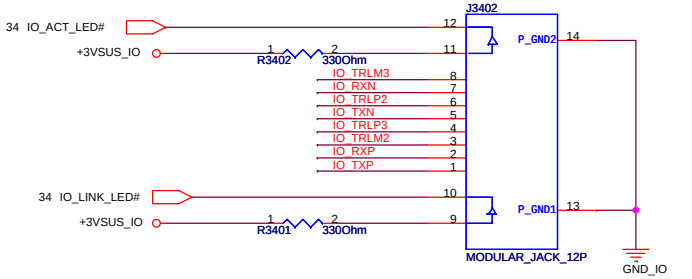




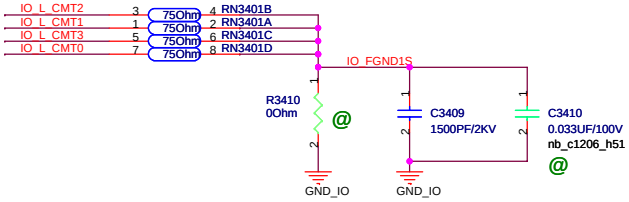
Transformer close CN3402

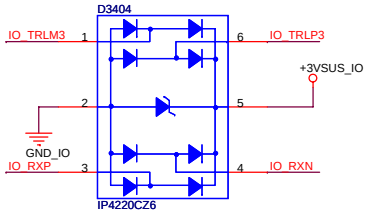


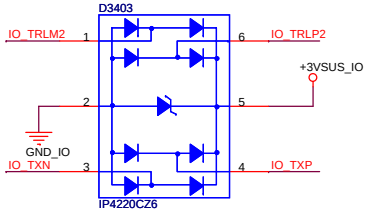




12G148301089LV
ALLTOP/C100Q2-10806-L







<variant_name>

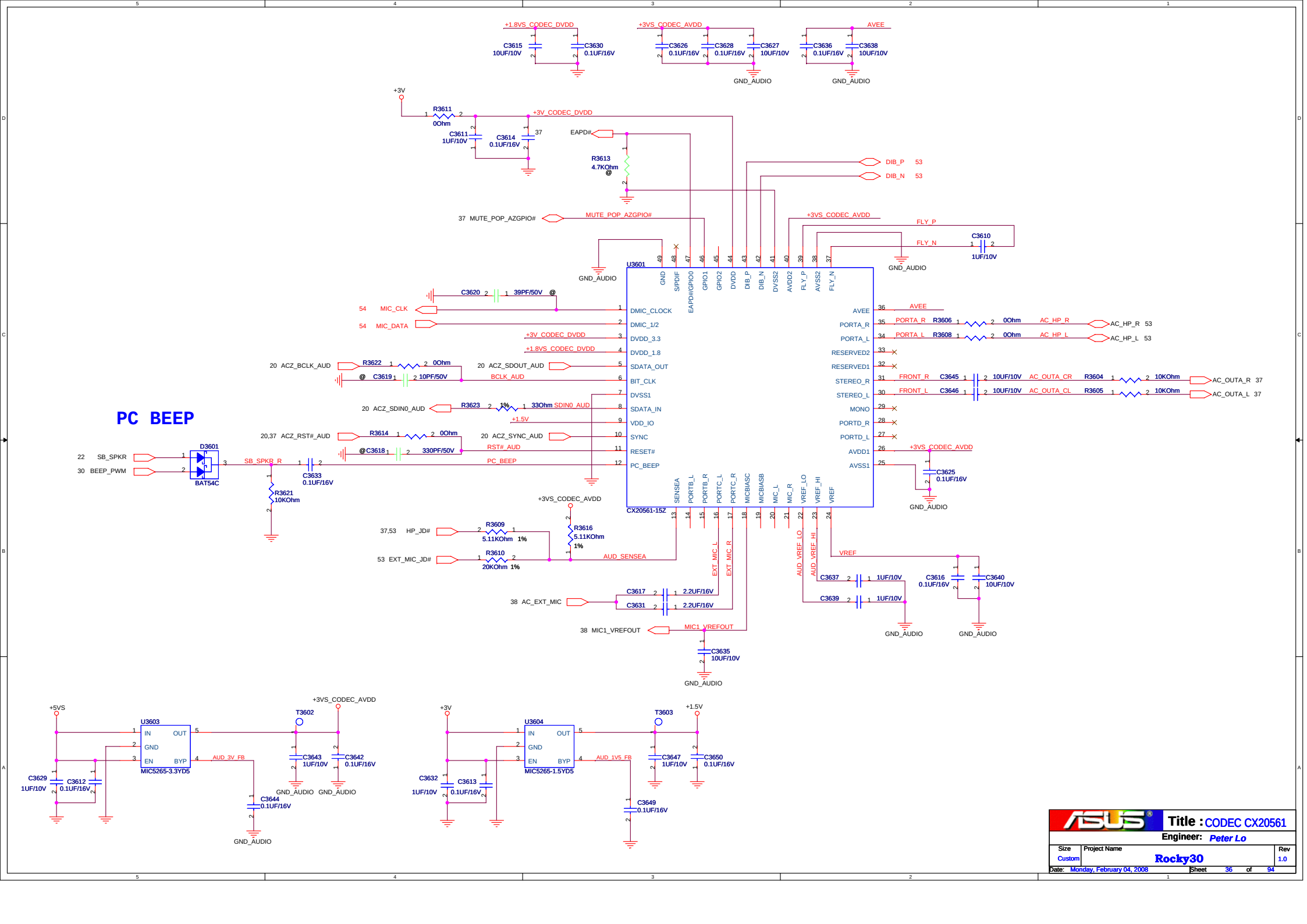
ASUSTeK COMPUTER INC

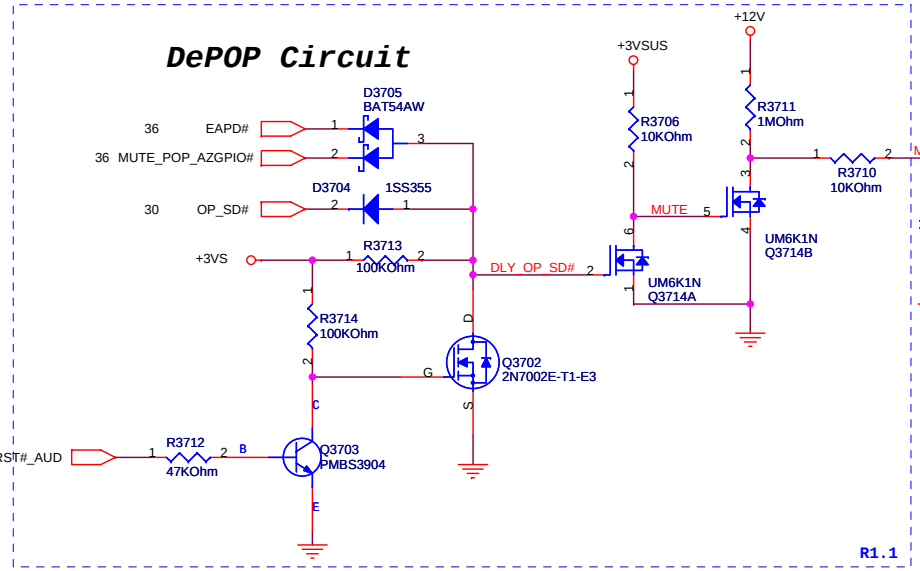
Title : LAN-RJ45

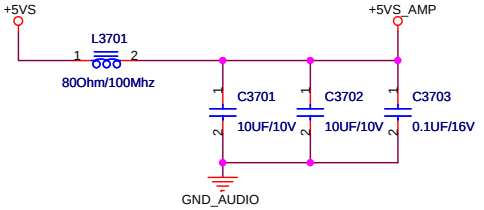
Engineer: Warren

Size	Project Name	Rev
Custom	Rocky 30 IO Board	1.1

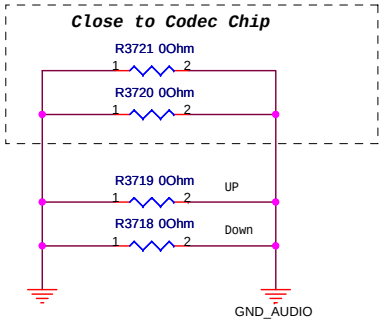
Date: Monday, February 04, 2008 Sheet 35 of 94


PC BEEP
U3601
CX20561-15Z
U3603
MIC5265-3.3YD5
U3604
MIC5265-1.5YD5
D3601
BAT54C
Title : CODEC CX20561
Engineer: Peter Lo
Project Name
Rocky30
Size
Custom
Rev
1.0
Date: Monday, February 04, 2008
Sheet 36 of 94

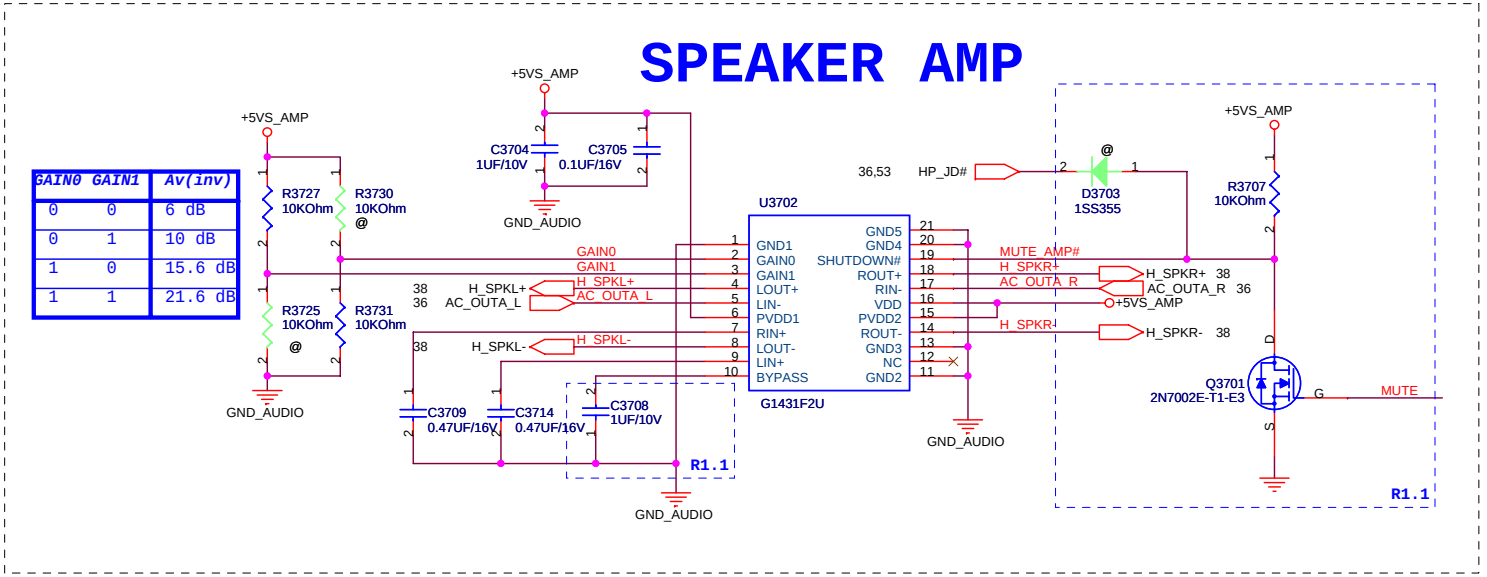




JACK GND

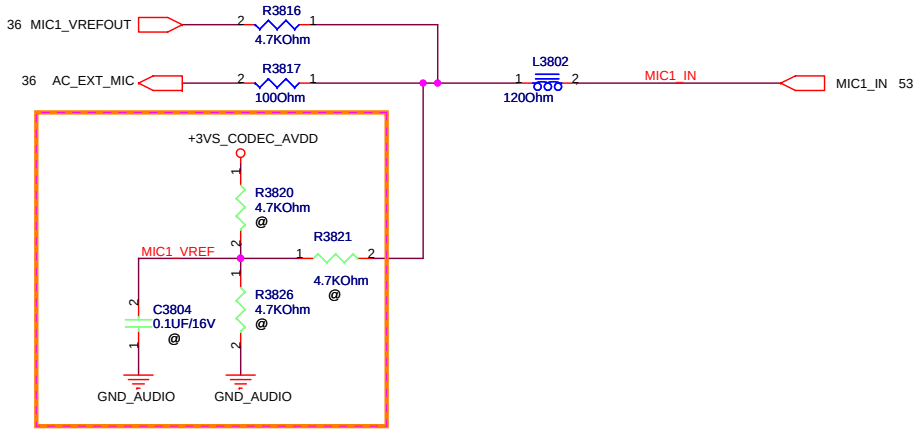


SPEAKER AMP



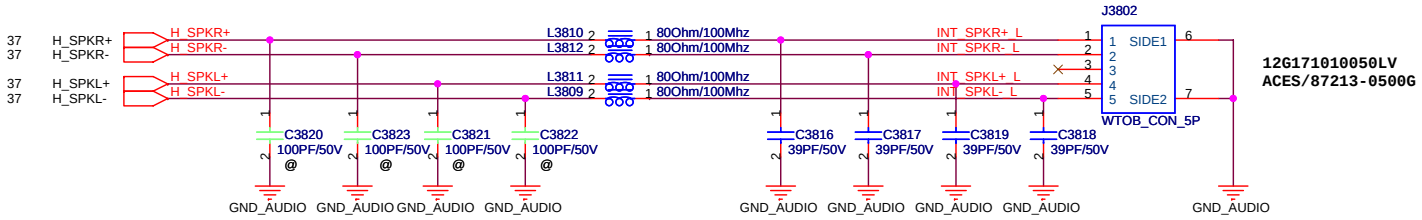
Title : AUDIO AMP		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 37 of 94	

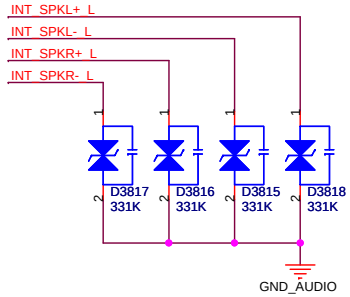
EXT MICROPHONE



Reserved the external MIC bias(T filter).

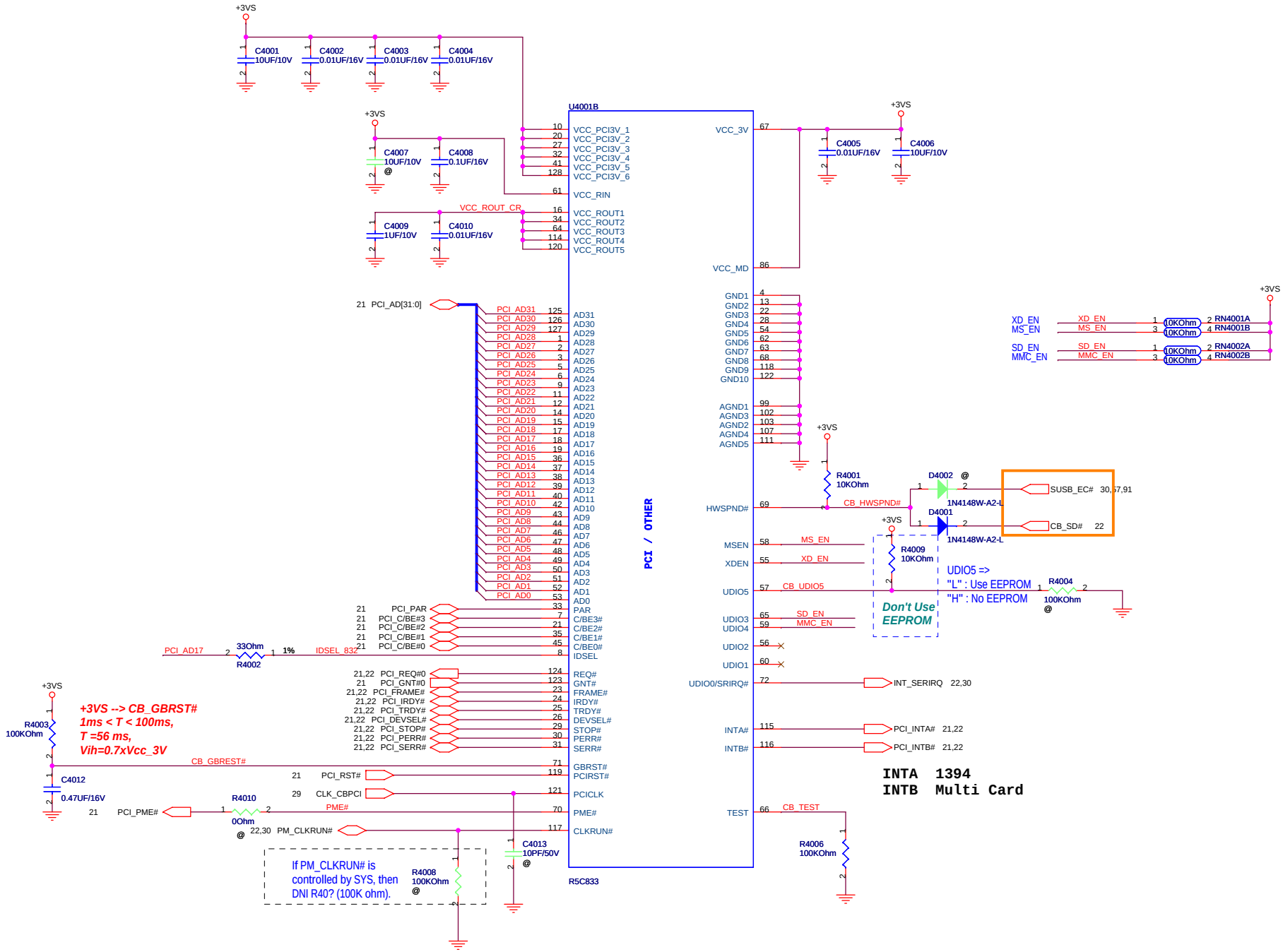
SPEAKER CONNECTOR



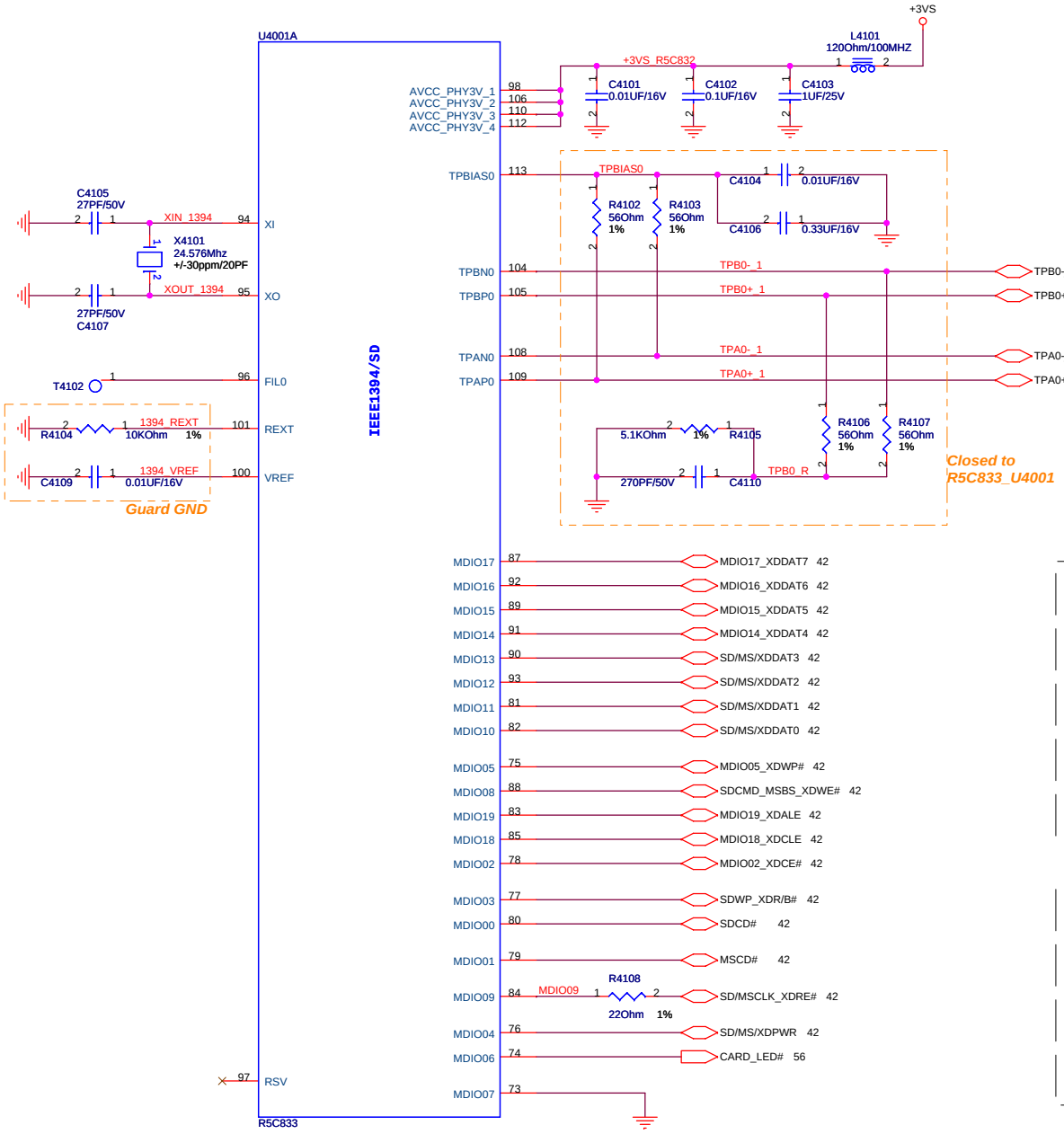


Title : MIC&LINEIN		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 38 of 94	

Title :	***
Engineer:	Peter Lo
Size: Custom	Project Name: Rocky30
Rev:	1.0
Date: Thursday, October 18, 2007	Sheet 39 of 94



Title : CARDBUS R5C833 (1)		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 40 of 94	




```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```

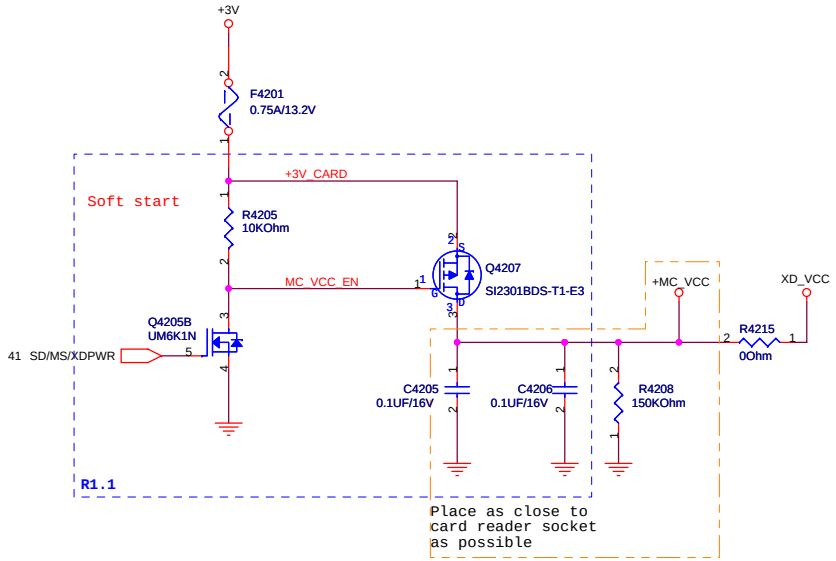
ASUS

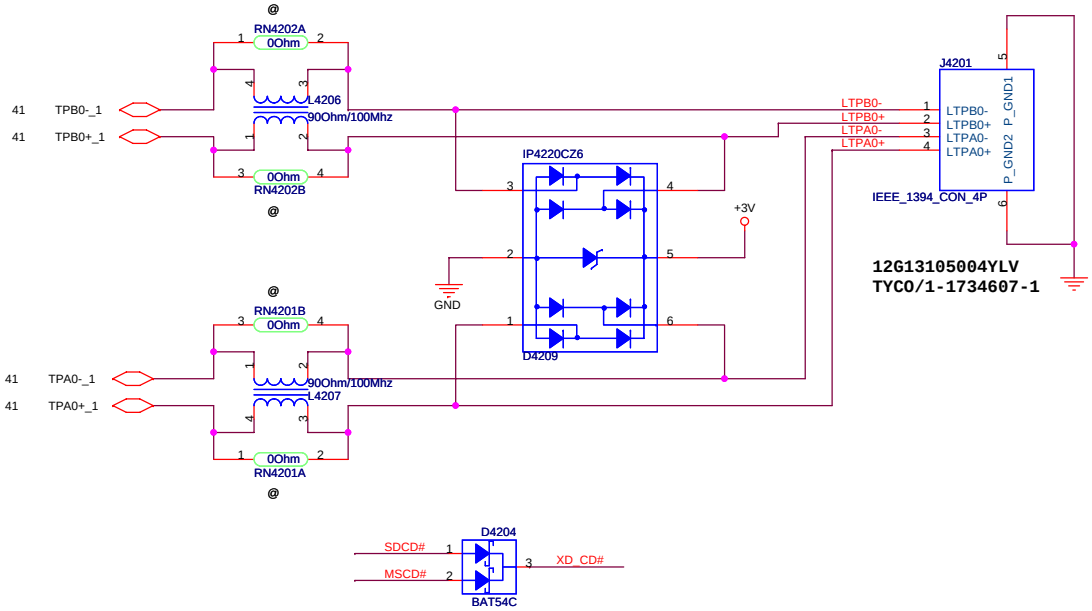
Title : CARDBUS R5C833 (2)

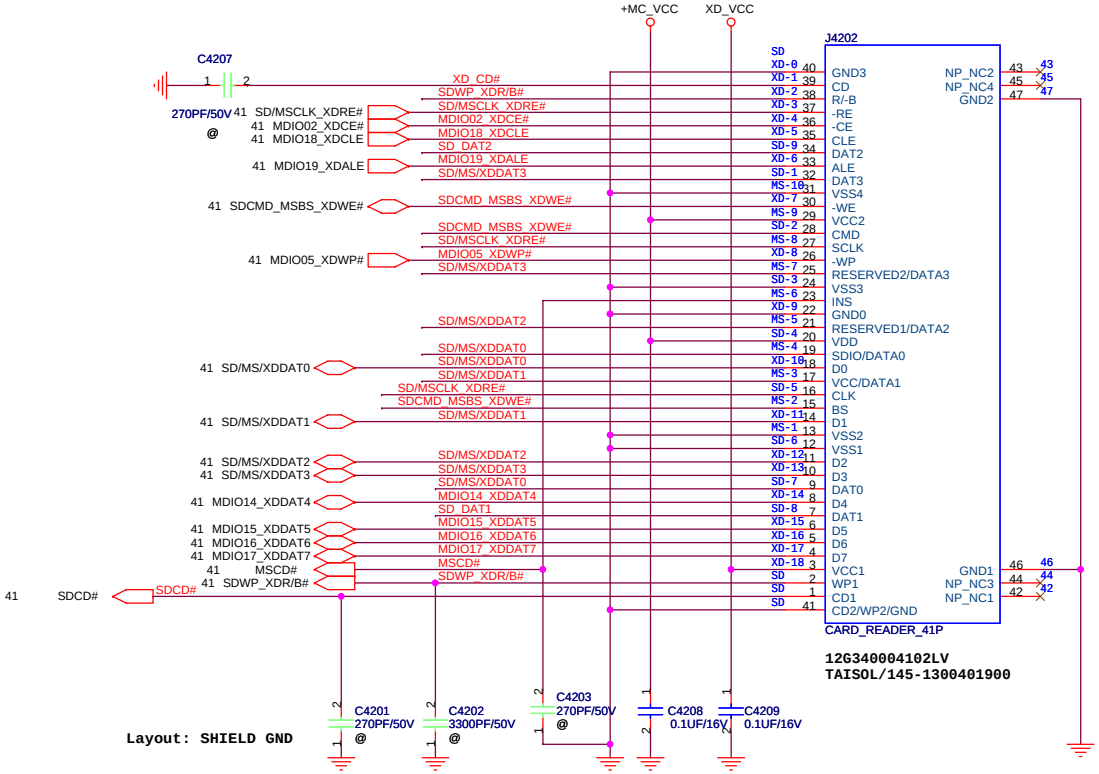
Engineer: Peter Lo

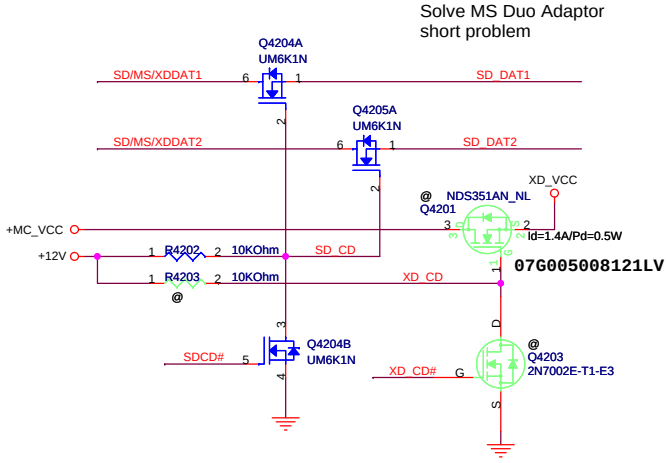
Size	Project Name	Rev
Custom	Rocky30	1.0

Date: Monday, February 04, 2008 Sheet 41 of 94





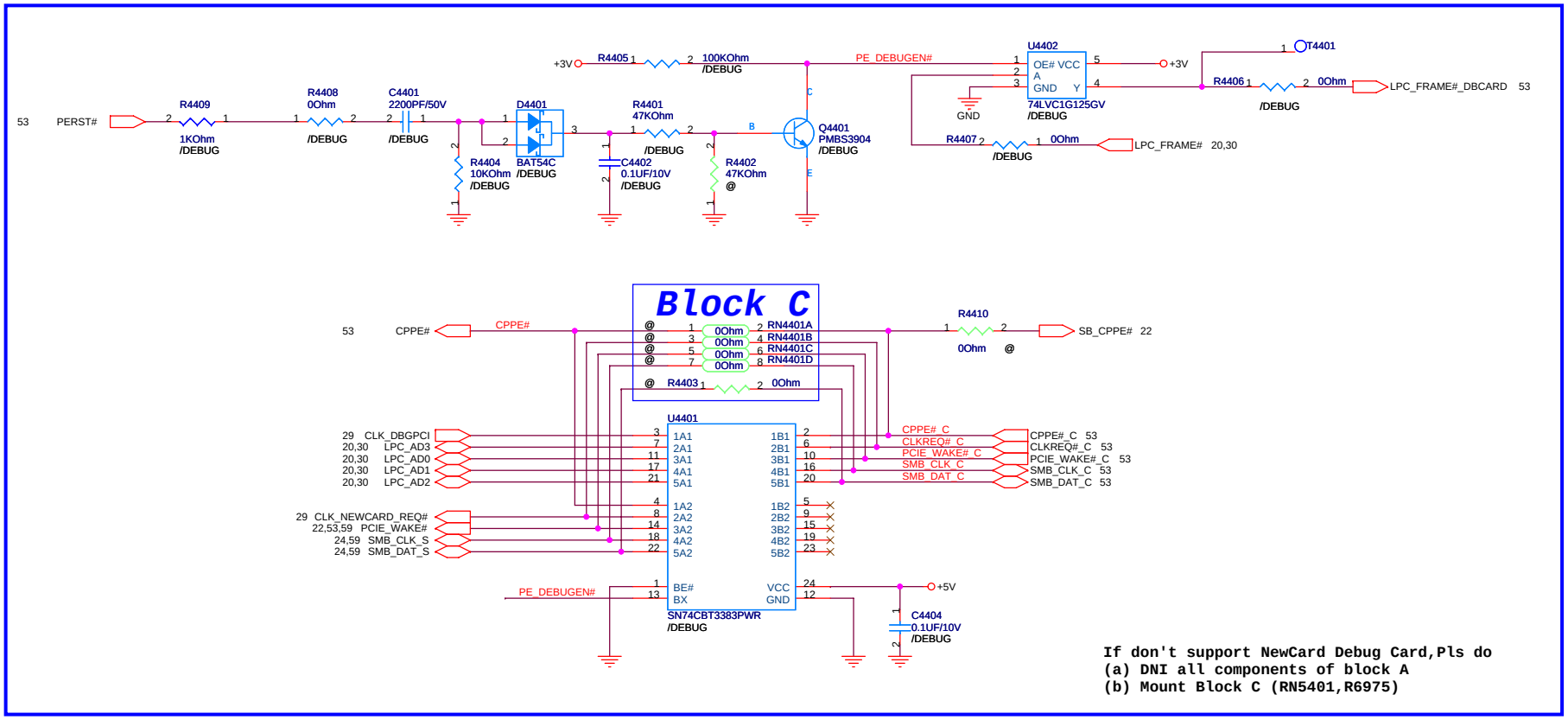


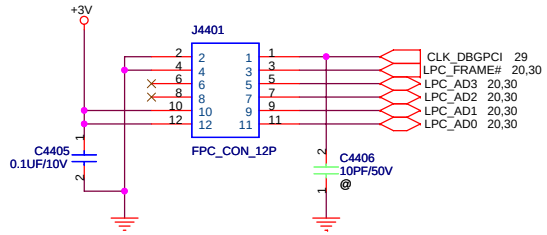


ASUS	Title : 1394 & CardReader	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 42 of 94	

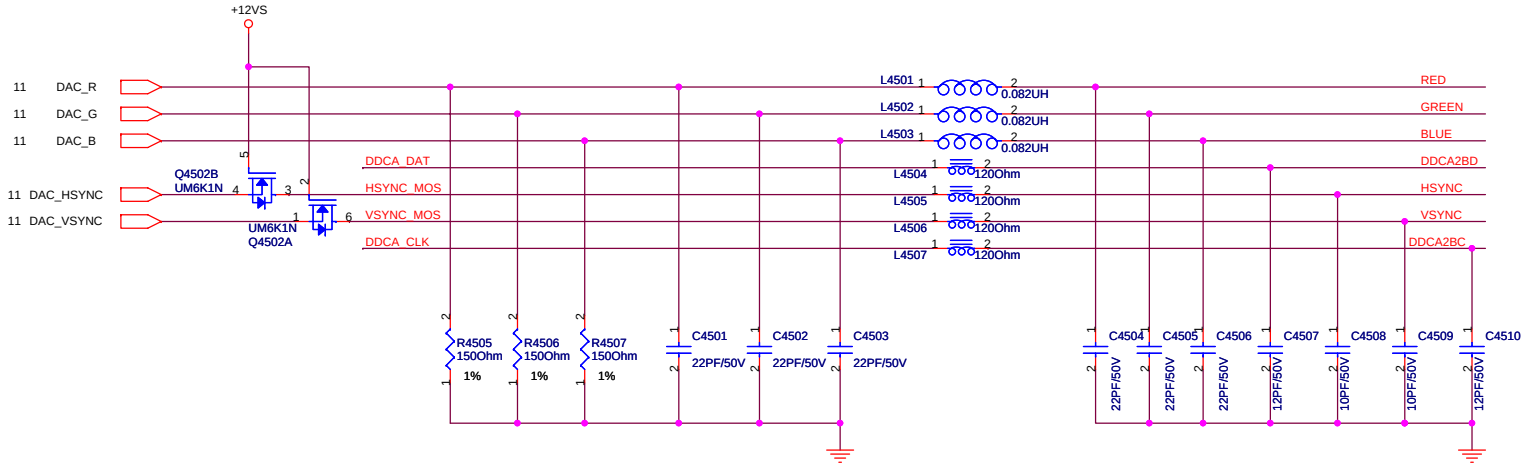
Title :	****
Engineer:	*Peter Lo*
Size: Custom	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 43 of 94

Block A

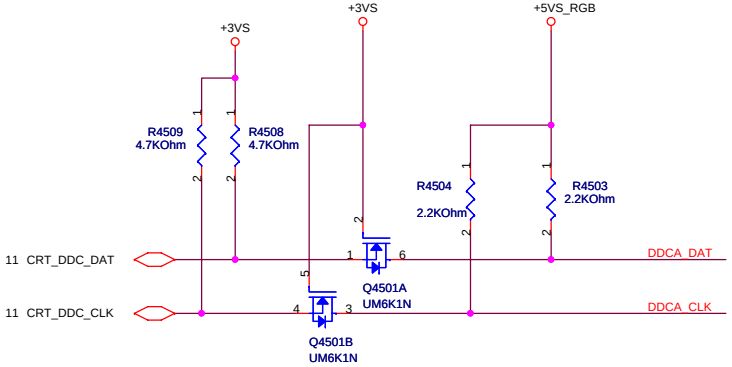


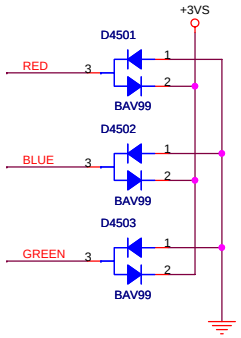


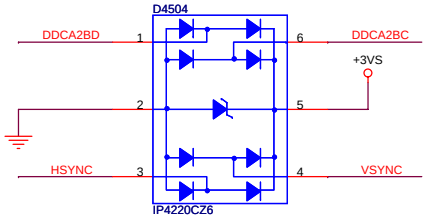
ASUS	Title : DEBUG	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 44 of 94	

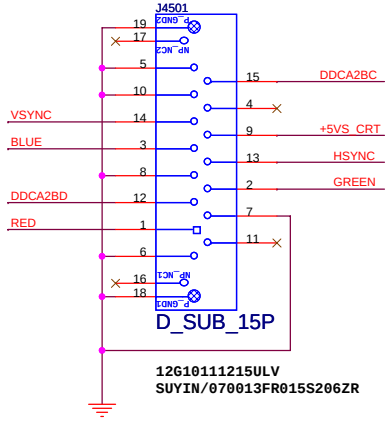


PLACE ESD Diodes near VGA port





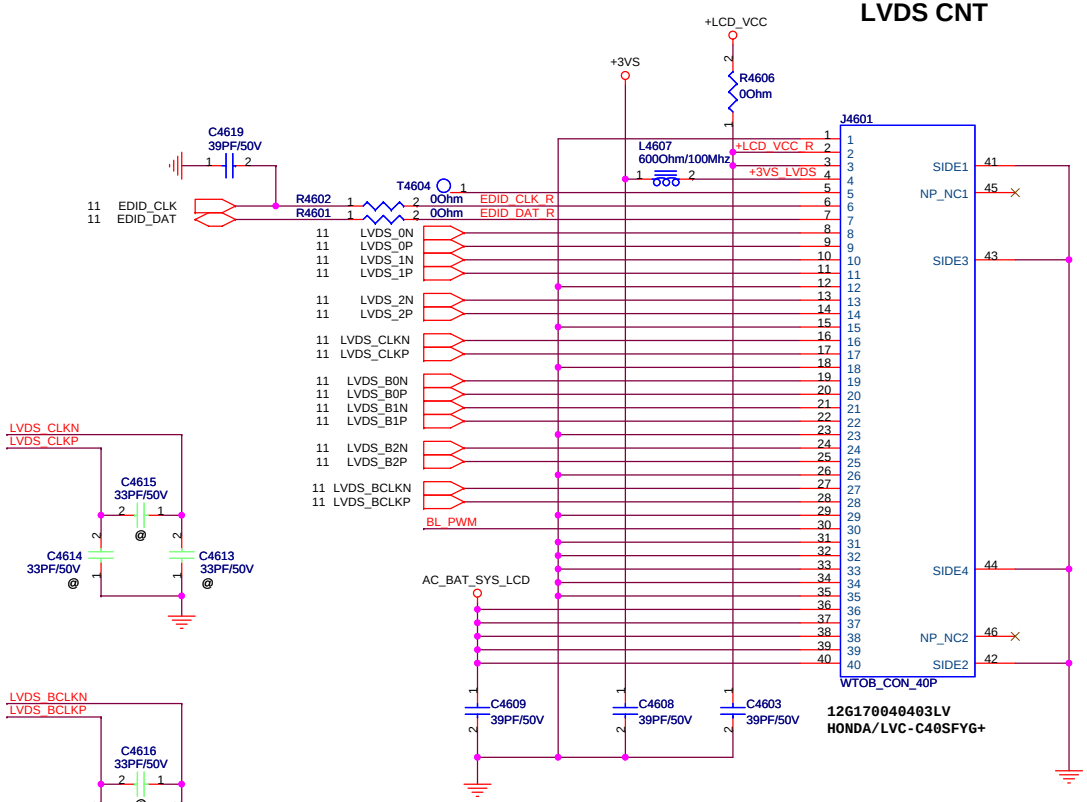


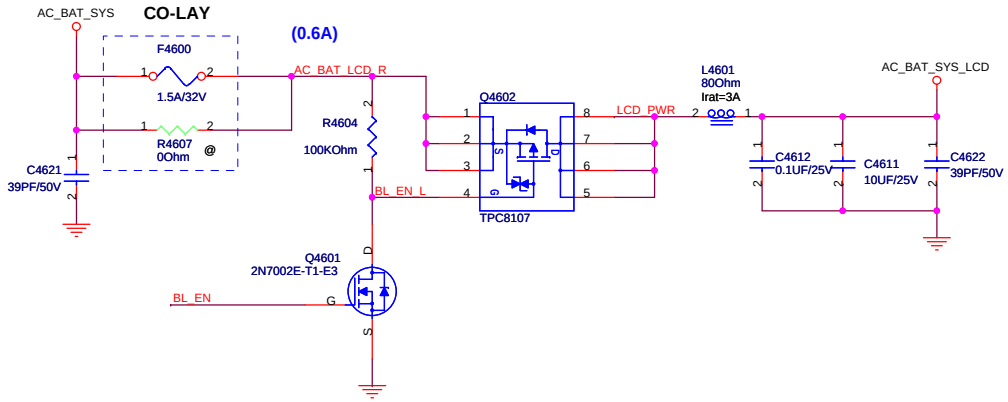


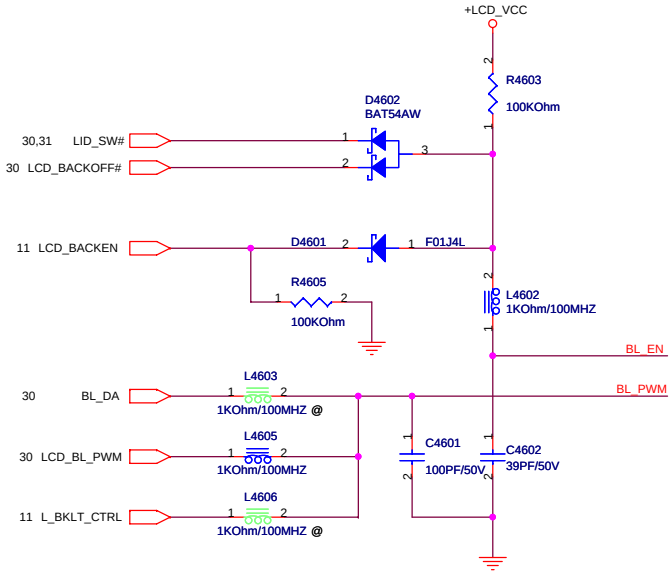
12G10111215ULV
SUYIN/070013FR015S206ZR

Title : CRT		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 45 of 94	

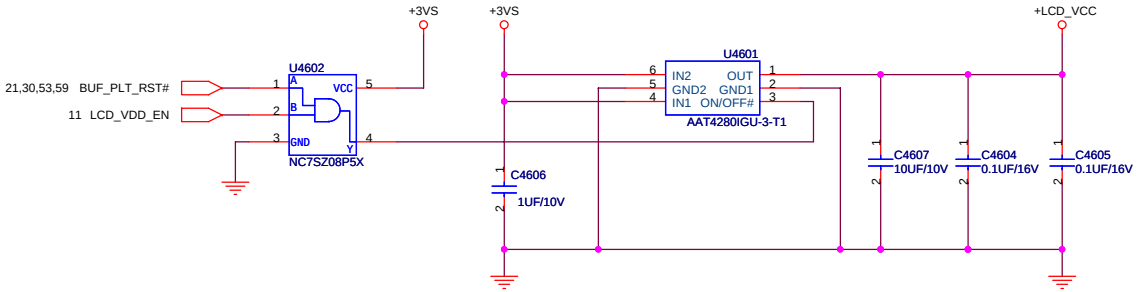
LVDS CNT





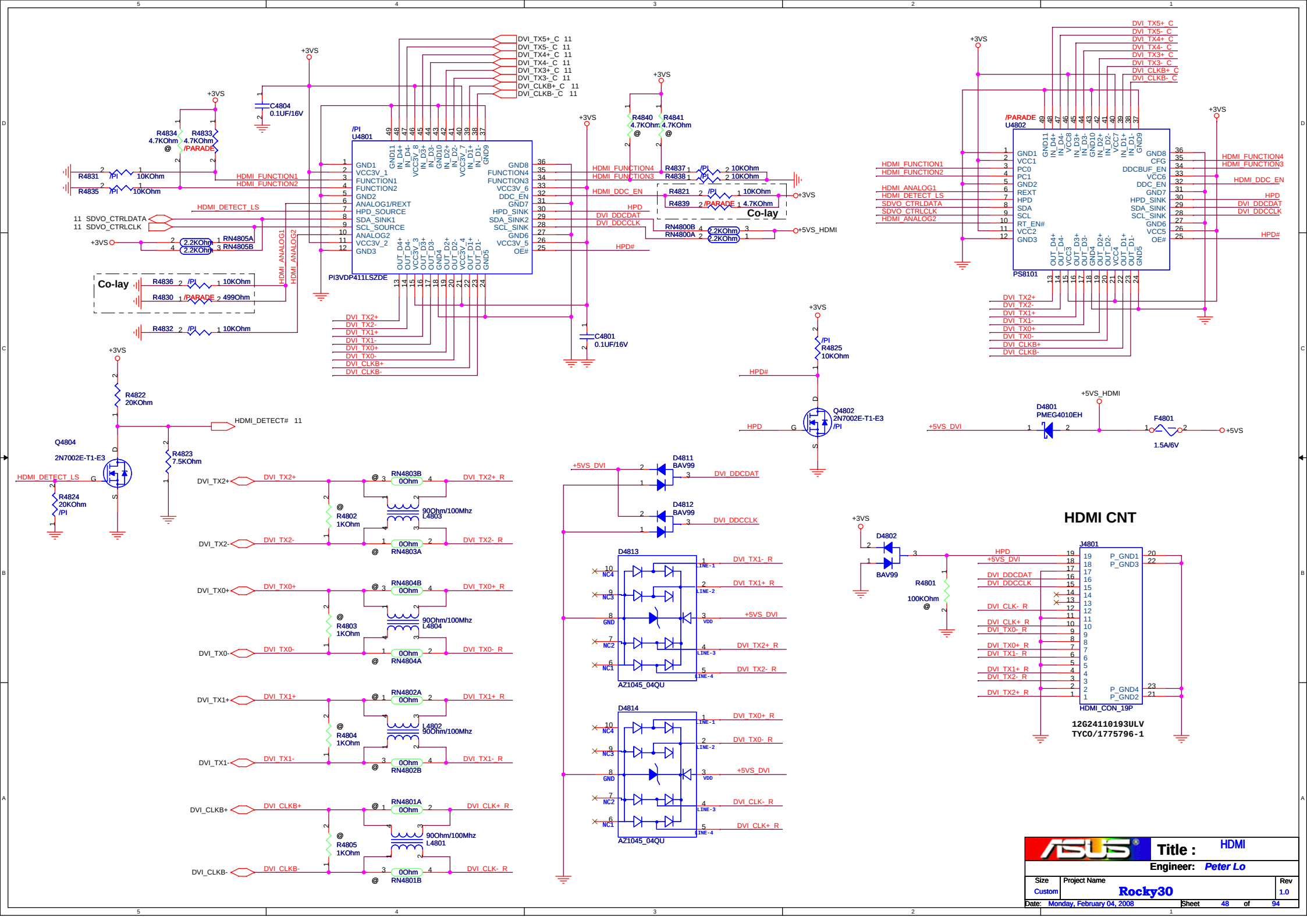


Power Switch for LCD Power



Title : LVDS & Inverter CON		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 46 of 94	

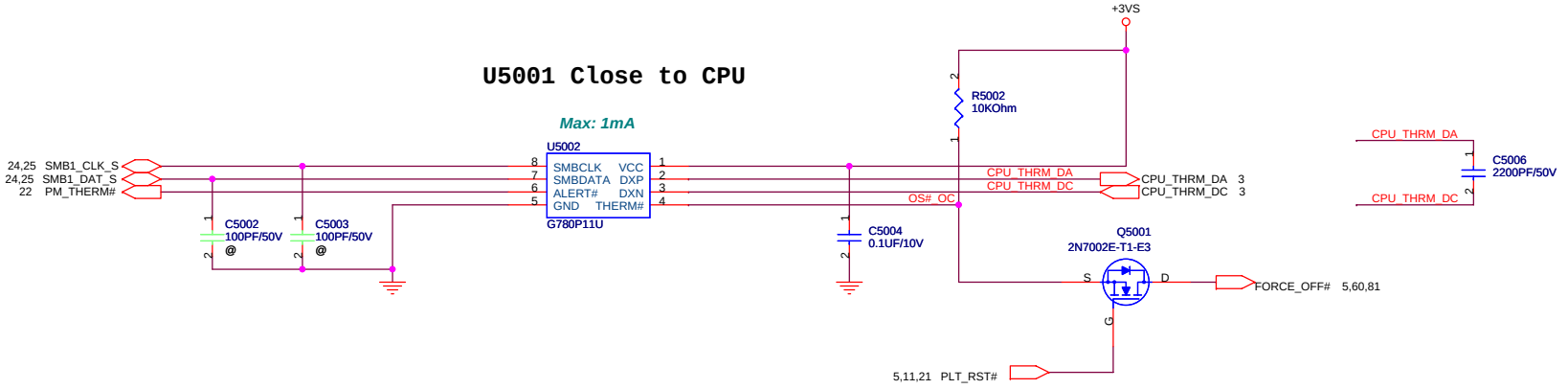
Title :	***
Engineer:	Peter Lo
Size: C	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 47 of 94

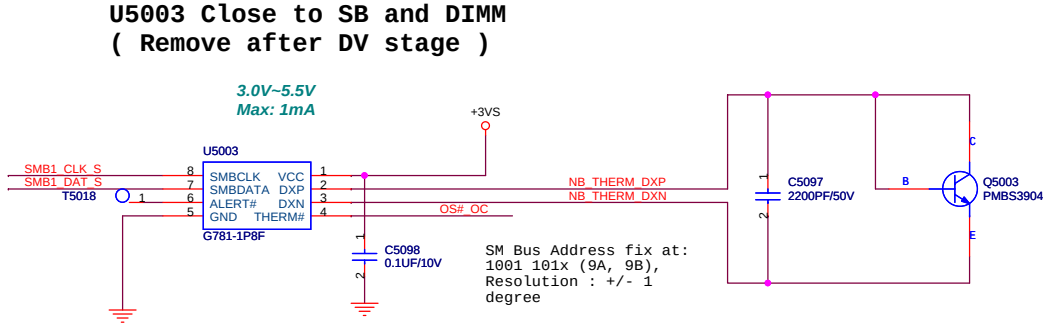


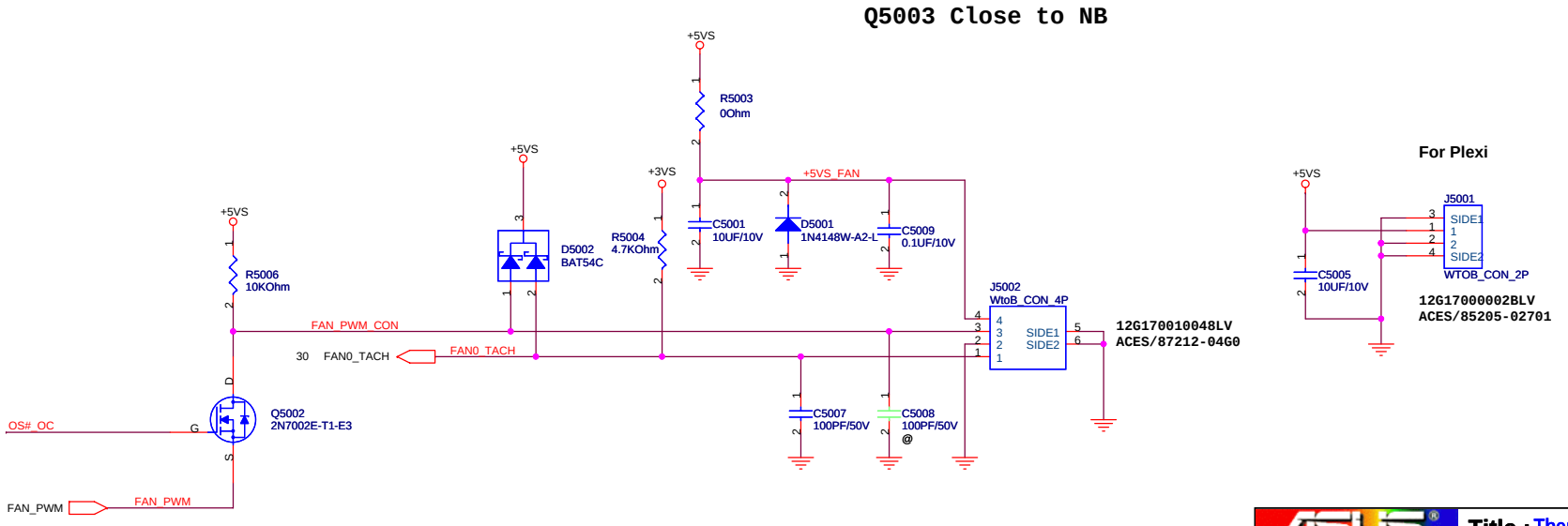
Title :	HDMI	
Engineer:	Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 48 of 94	

Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	49 of 94

Thermal Sensor

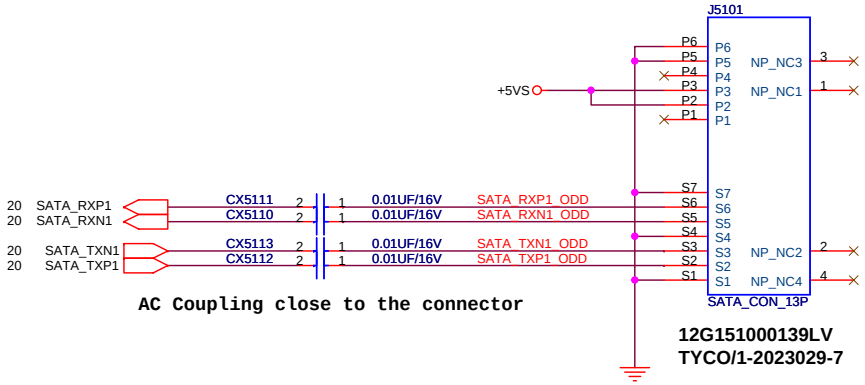






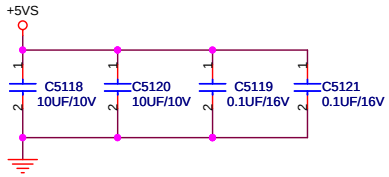
Title : Thermal & Fan		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 50 of 94	

ODD CON

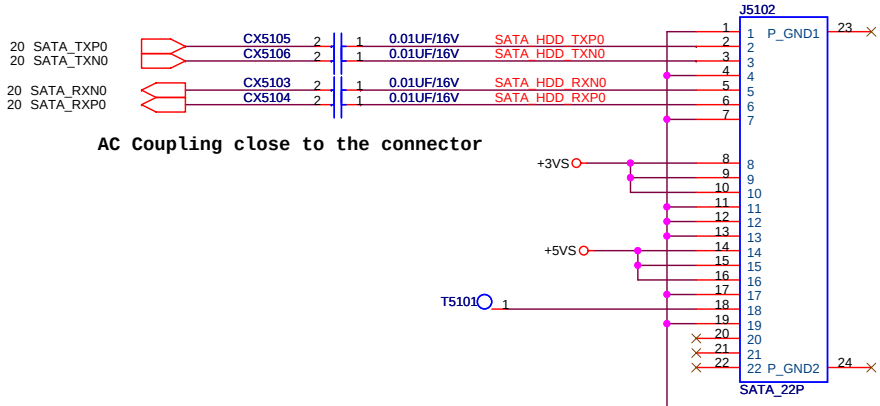


AC Coupling close to the connector

12G151000139LV
TYCO/1-2023029-7

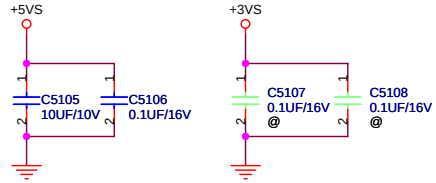


SATA HDD CON

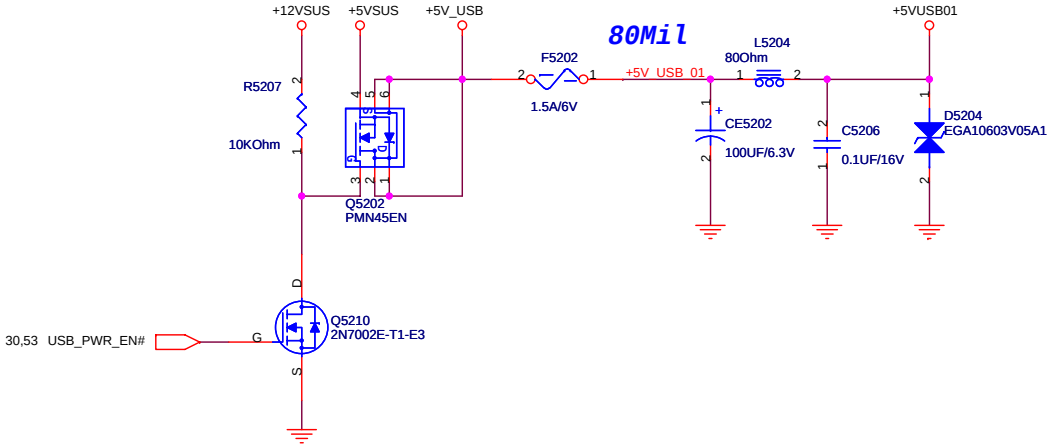


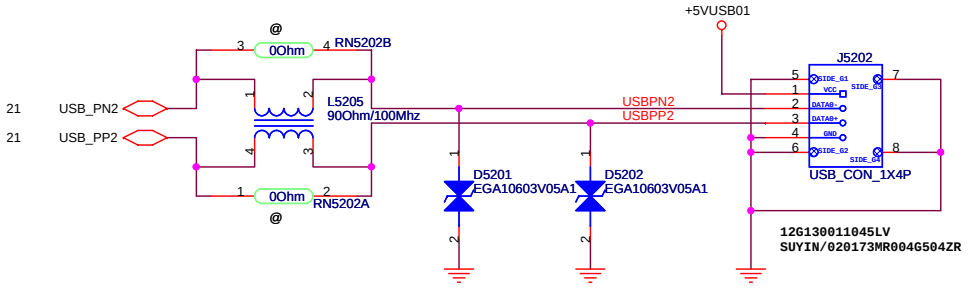
AC Coupling close to the connector

12G15111022PLV
TYCO/1735544-1



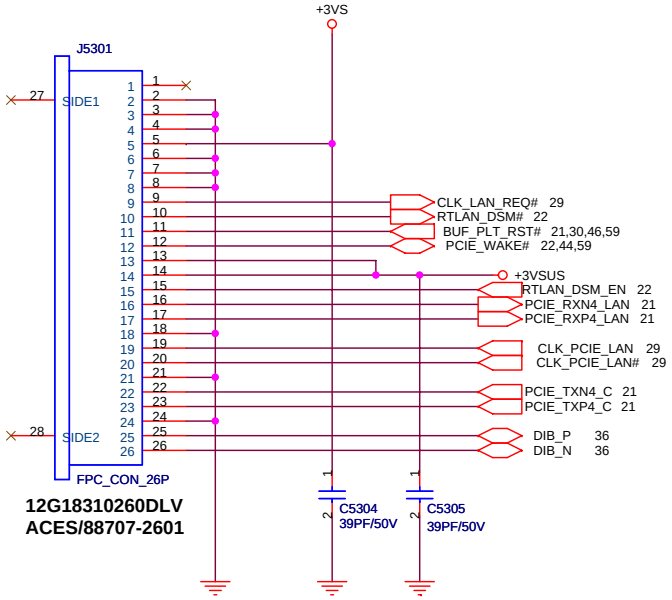
Title : Sata HDD & Swap Bay		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 51 of 94	





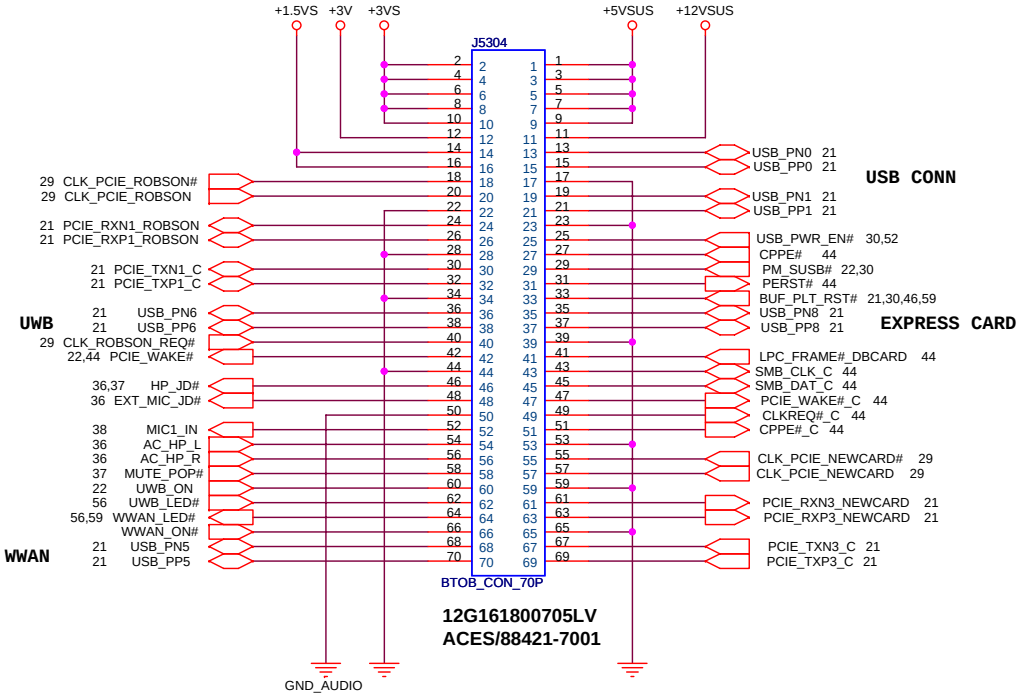
Title : USB CONN		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 52 of 94	

IO BOARD



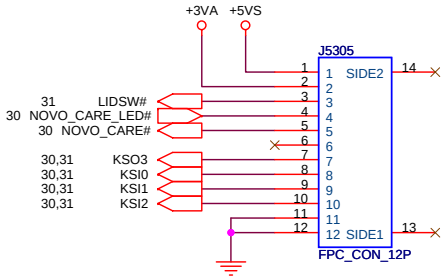
12G18310260DLV
ACES/88707-2601

SMALL BOARD

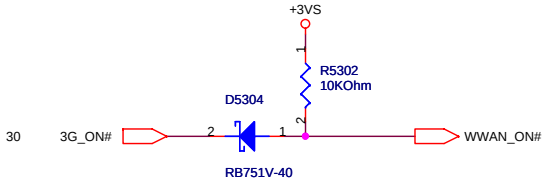


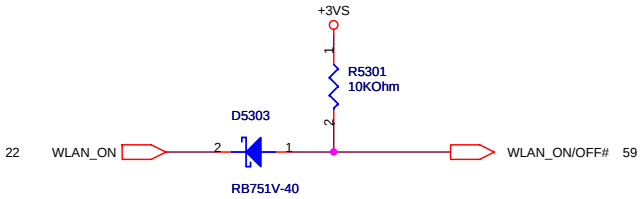
12G161800705LV
ACES/88421-7001

For Media Control Board

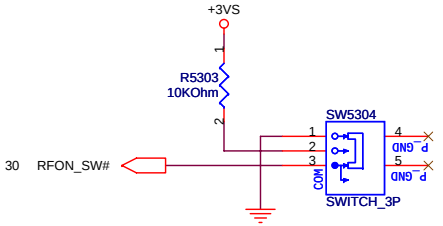


12G18310120BLV
ACES/88278-1200L



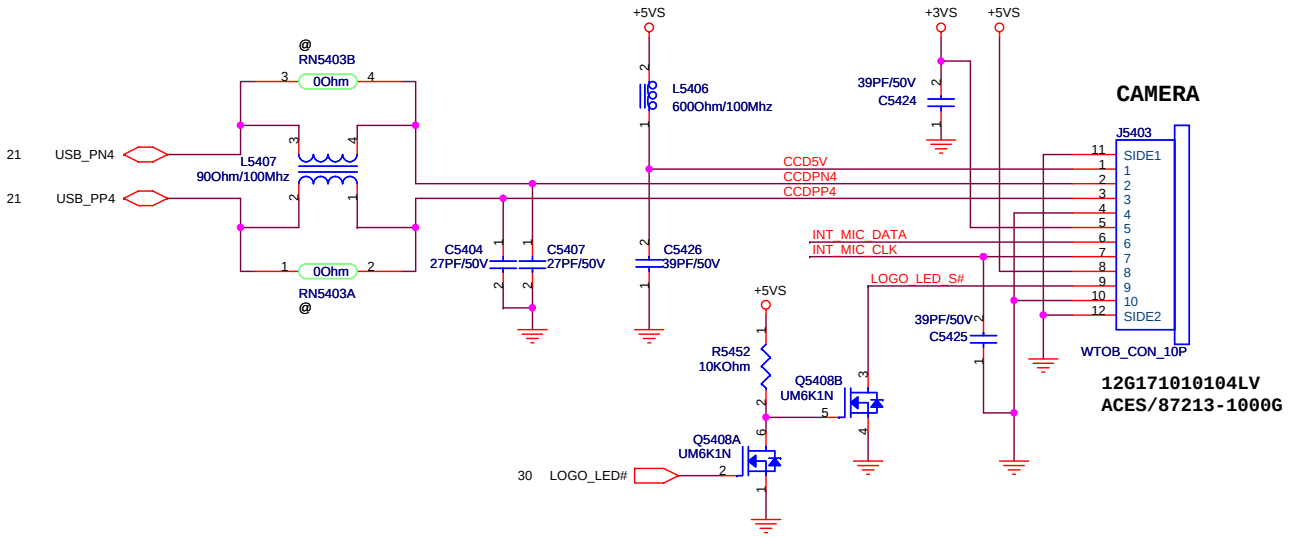


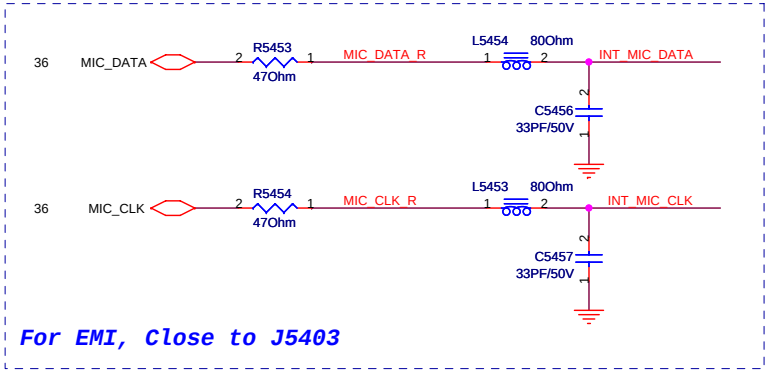
Wireless Switch



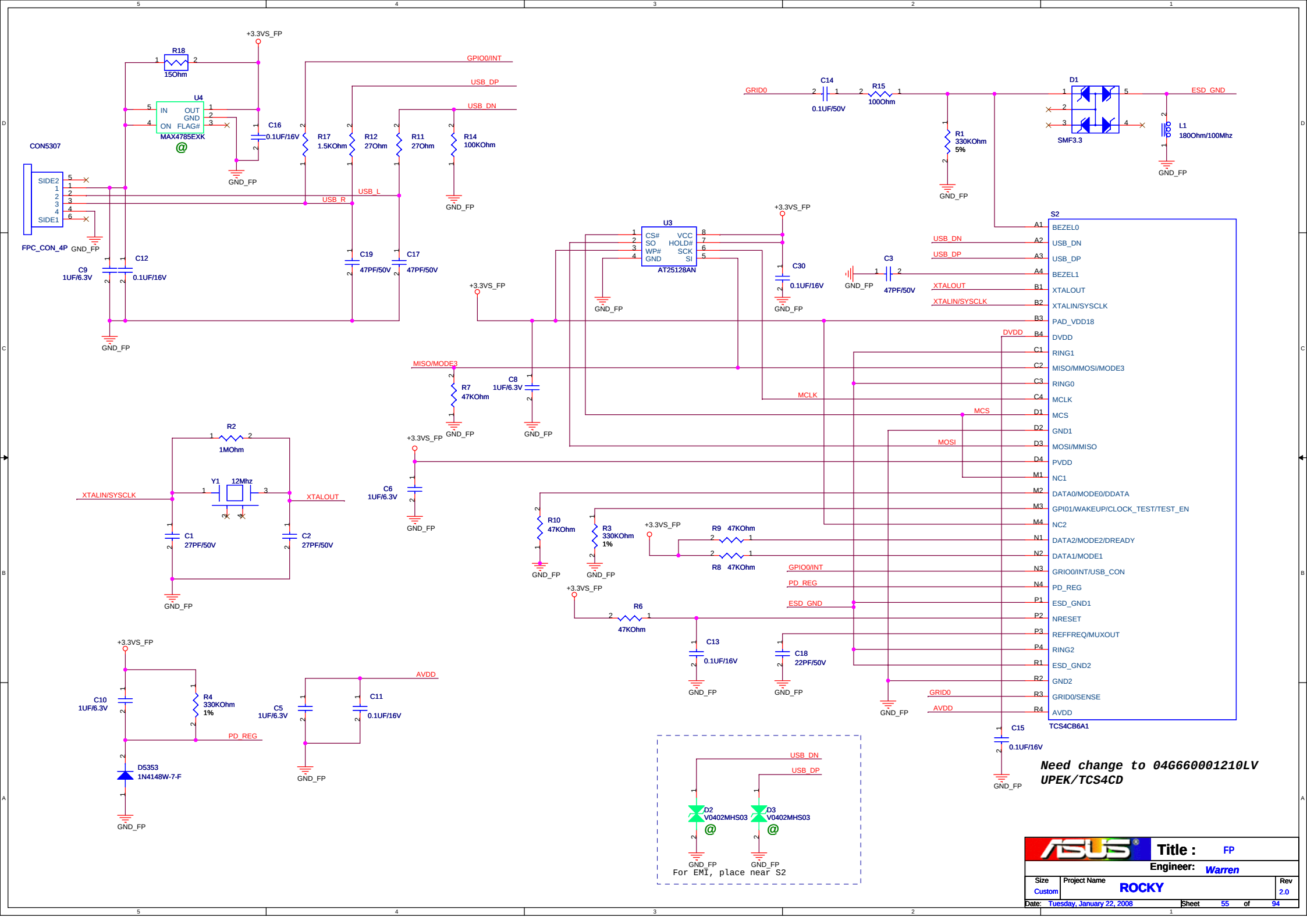
12G091070031LV
ALPS/SSSS710603

Title : IO BOARD		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 53 of 94	

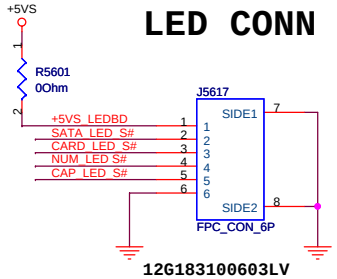




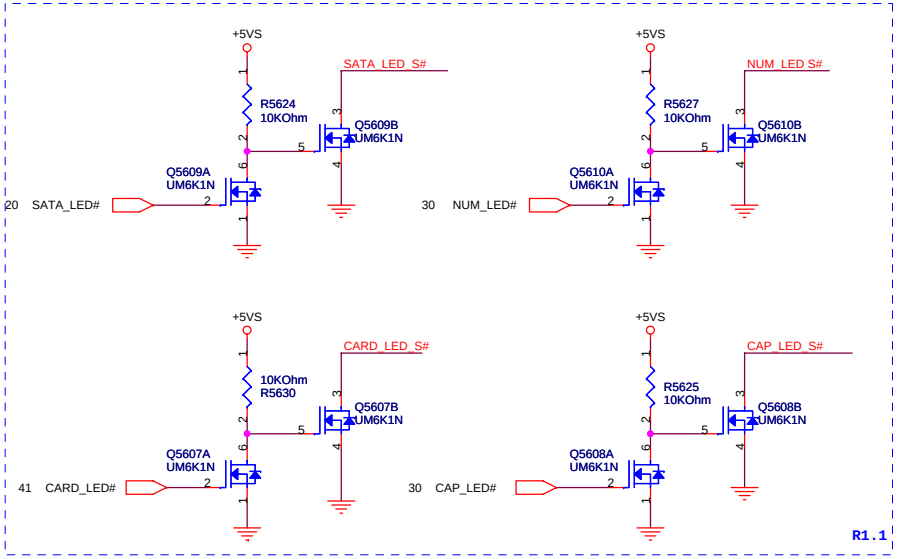
Title : CAMERA		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 54 of 94	

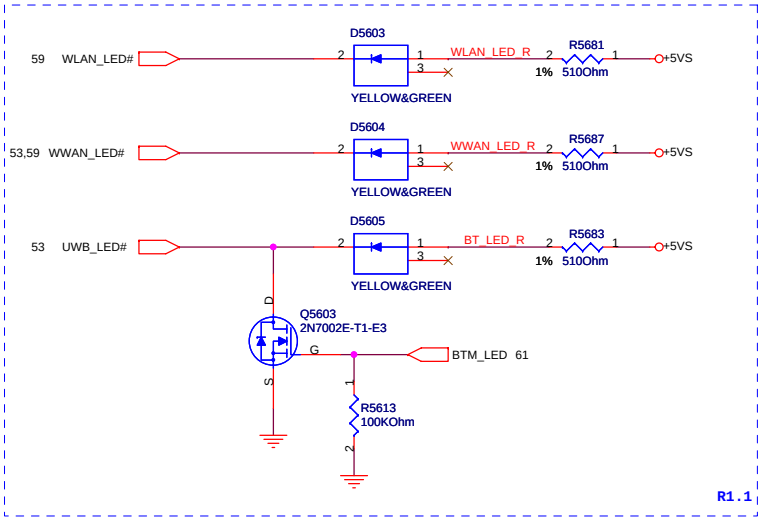

+3.3VS_FP
R18
15Ohm
U4
IN
OUT
GND
ON
FLAG#
MAX4785EXK
@
C16
0.1UF/16V
GND_FP
GPIO0/INT
USB_DP
USB_DN
R17
1.5KOhm
R12
27Ohm
R11
27Ohm
R14
100KOhm
CON5307
SIDE2
SIDE1
FPC_CON_4P
USB_L
USB_R
C9
1UF/6.3V
C12
0.1UF/16V
C19
47PF/50V
C17
47PF/50V
GRID0
C14
0.1UF/50V
R15
100Ohm
D1
SMF3.3
ESD_GND
L1
180Ohm/100Mhz
R1
330KOhm
5%
U3
CS#
SO
WP#
GND
VCC
HOLD#
SCK
SI
AT25128AN
C30
0.1UF/16V
C3
47PF/50V
S2
BEZEL0
USB_DN
USB_DP
BEZEL1
XTALOUT
XTALIN/SYSCLK
PAD_VDD18
DVDD
RING1
MISO/MMOSI/MODE3
RING0
MCLK
MCS
GND1
MOSI/MMISO
PVDD
NC1
DATA0/MODE0/DDATA
GPI01/WAKEUP/CLOCK_TEST/TEST_EN
NC2
DATA2/MODE2/DREADY
DATA1/MODE1
GRIO0/INT/USB_CON
PD_REG
ESD_GND1
NRESET
REFFREQ/MUXOUT
RING2
ESD_GND2
GND2
GRID0/SENSE
AVDD
TCS4CB6A1
C15
0.1UF/16V
MISO/MODE3
R7
47KOhm
C8
1UF/6.3V
MCLK
MCS
MOSI
R2
1MOhm
Y1
12Mhz
XTALIN/SYSCLK
XTALOUT
C1
27PF/50V
C2
27PF/50V
C6
1UF/6.3V
R10
47KOhm
R3
330KOhm
1%
R9
47KOhm
R8
47KOhm
GPIO0/INT
PD_REG
ESD_GND
R6
47KOhm
C13
0.1UF/16V
C18
22PF/50V
C10
1UF/6.3V
R4
330KOhm
1%
C5
1UF/6.3V
C11
0.1UF/16V
AVDD
D5353
1N4148W-7-F
D2
V0402MHS03
D3
V0402MHS03
For EMI, place near S2
Need change to 04G660001210LV
UPEK/TCS4CD
Title : FP
Engineer: Warren
Size Custom
Project Name ROCKY
Rev 2.0
Date: Tuesday, January 22, 2008
Sheet 55 of 94

LED CONN

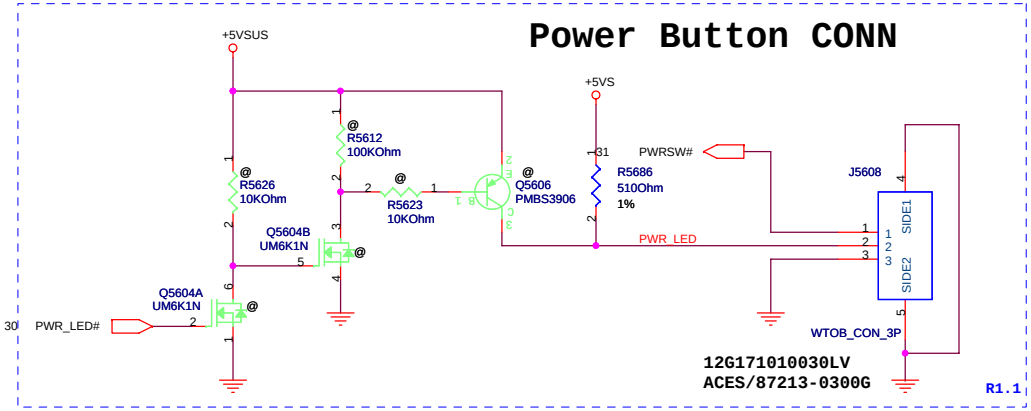


12G183100603LV
ACES/88278-06001

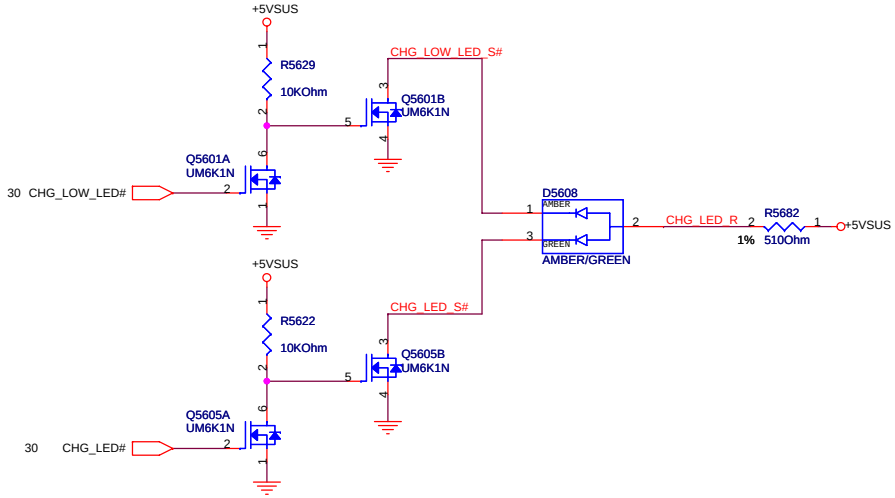


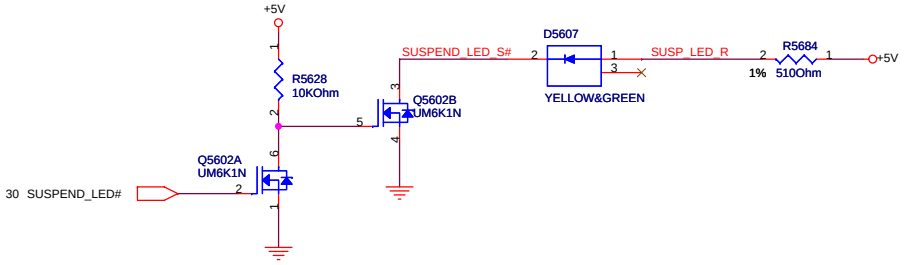


Power Button CONN

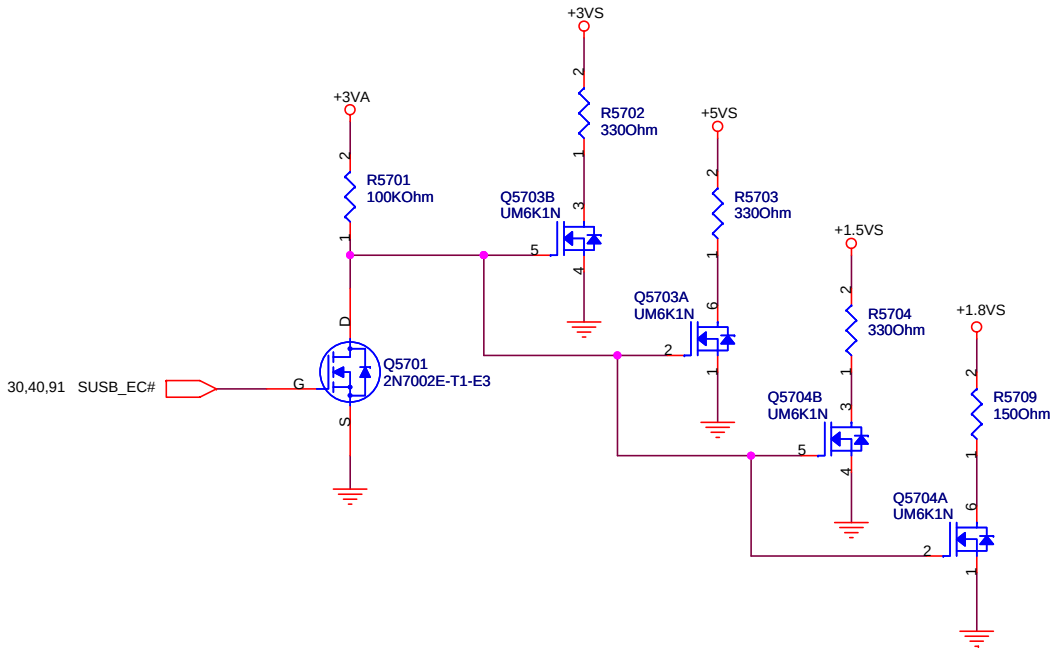


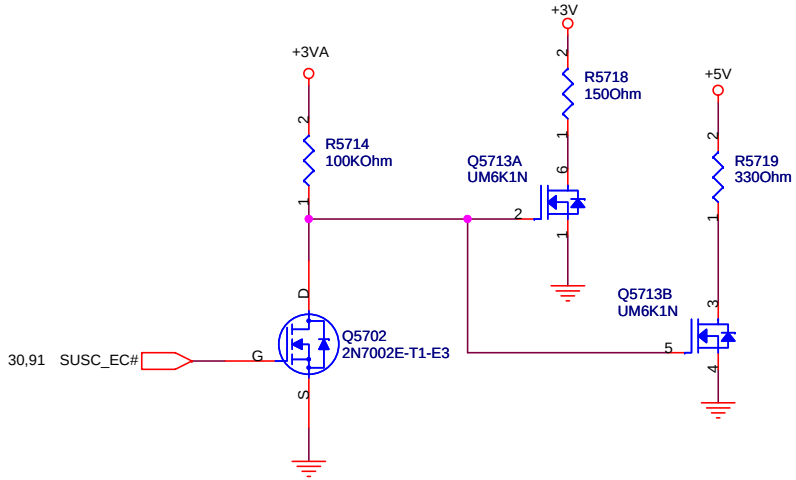
12G171010030LV
ACES/87213-0300G
R1.1



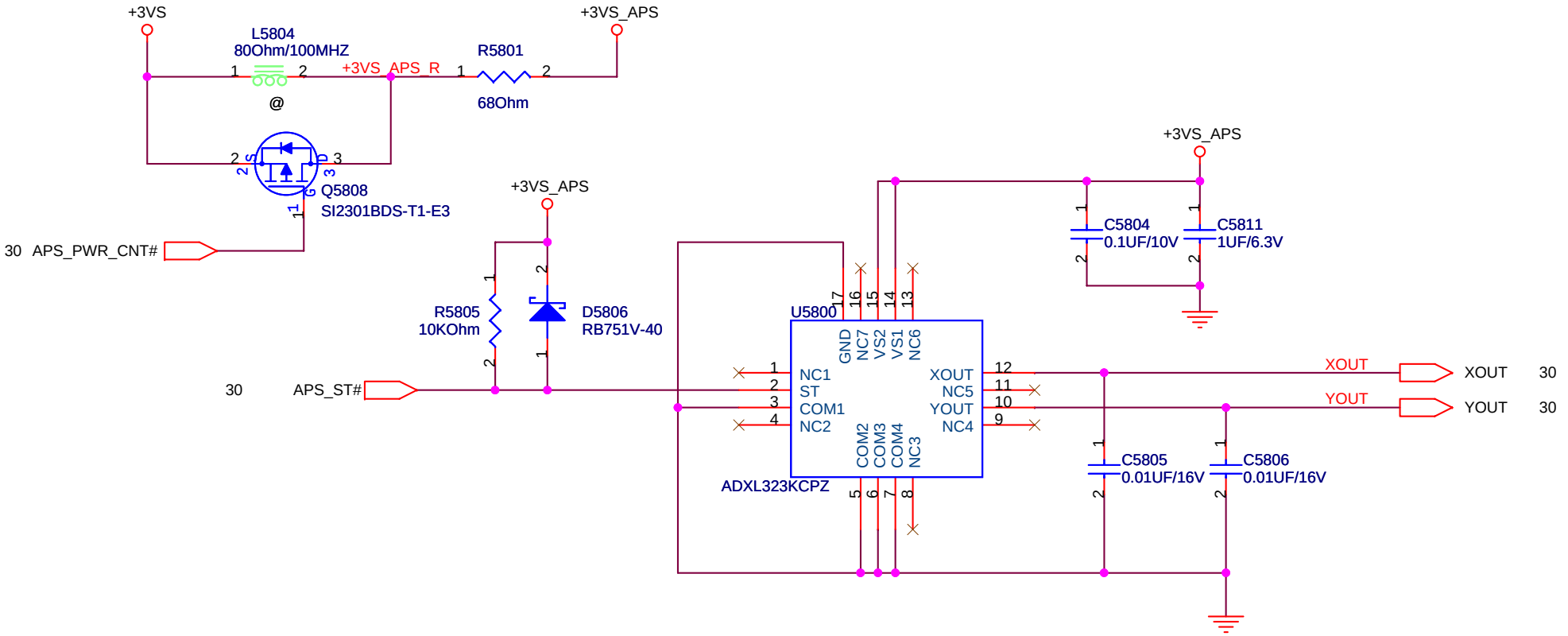


Title : LED/SW		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 56 of 94	

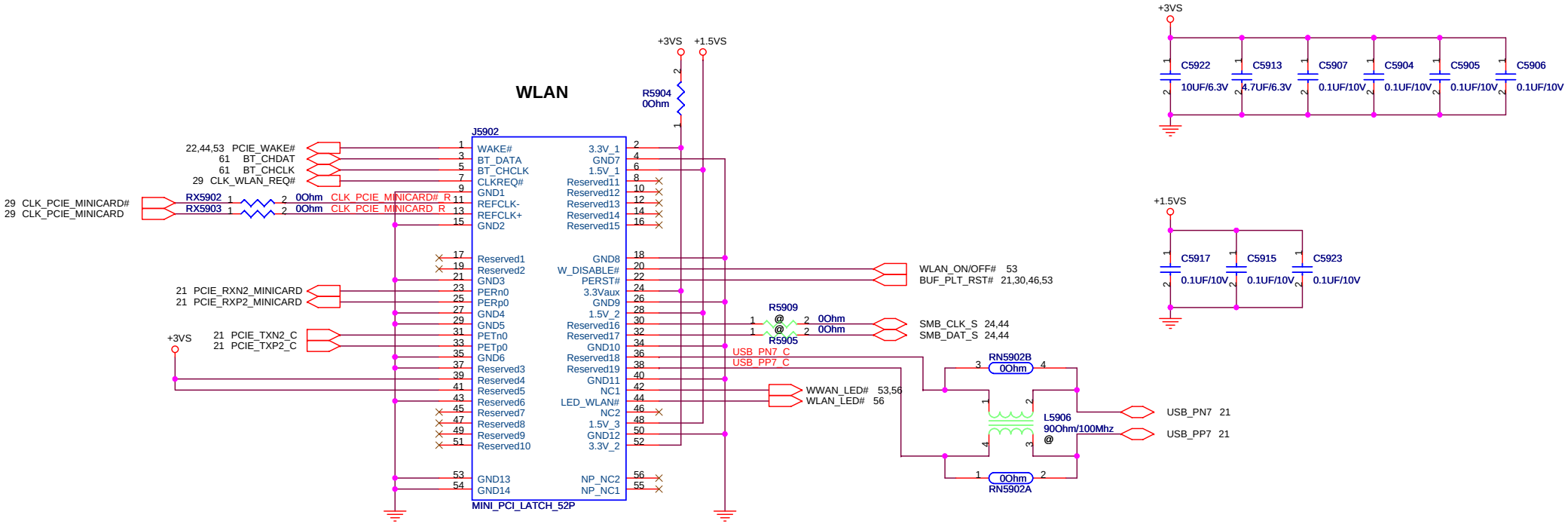




Title : DISCHARGE		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 57 of 94	

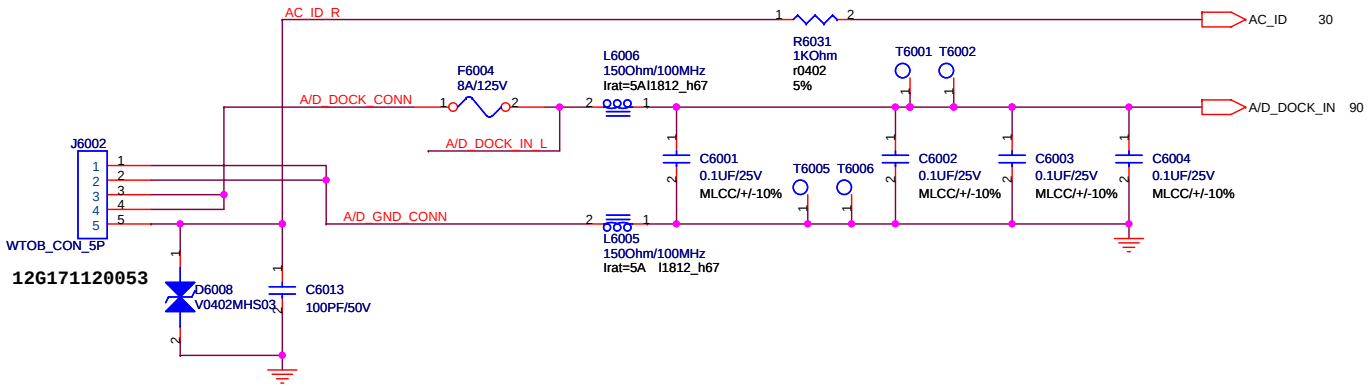


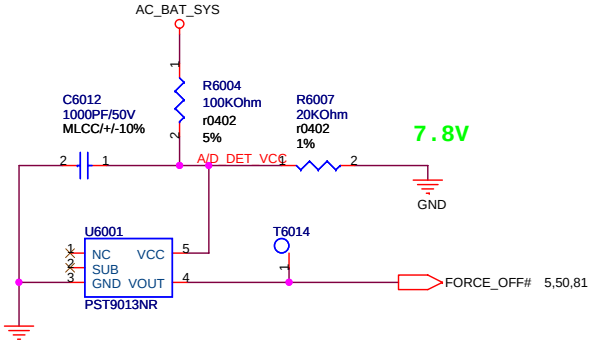
ASUS	Title : SMS	
	Engineer: *Peter Lo*	
Size: A	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 58 of 94	



Title : Mini Card		
Engineer: Peter Lo		
Size: B	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 59 of 94	

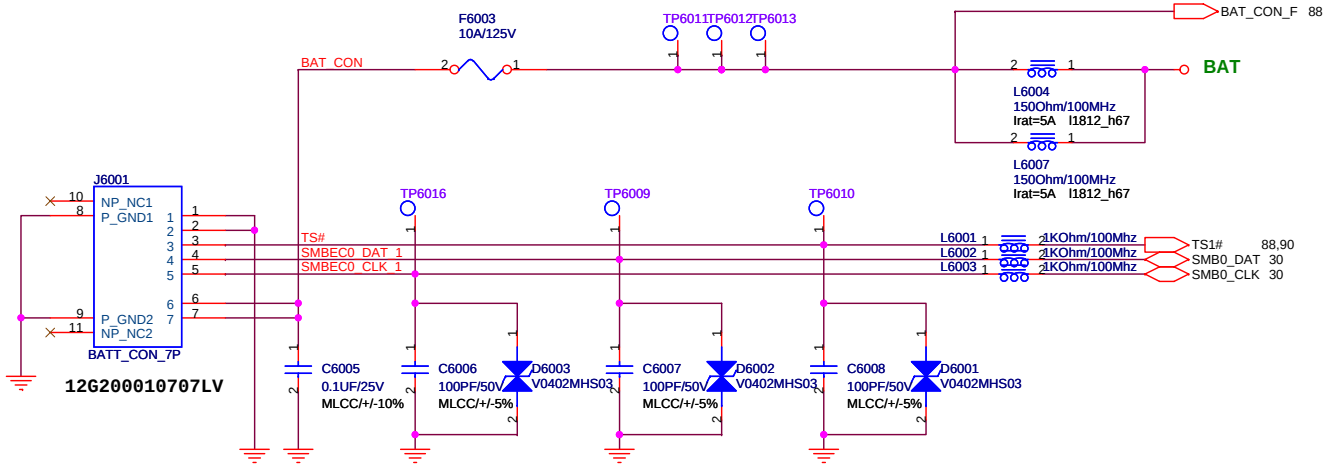
DC IN CONN





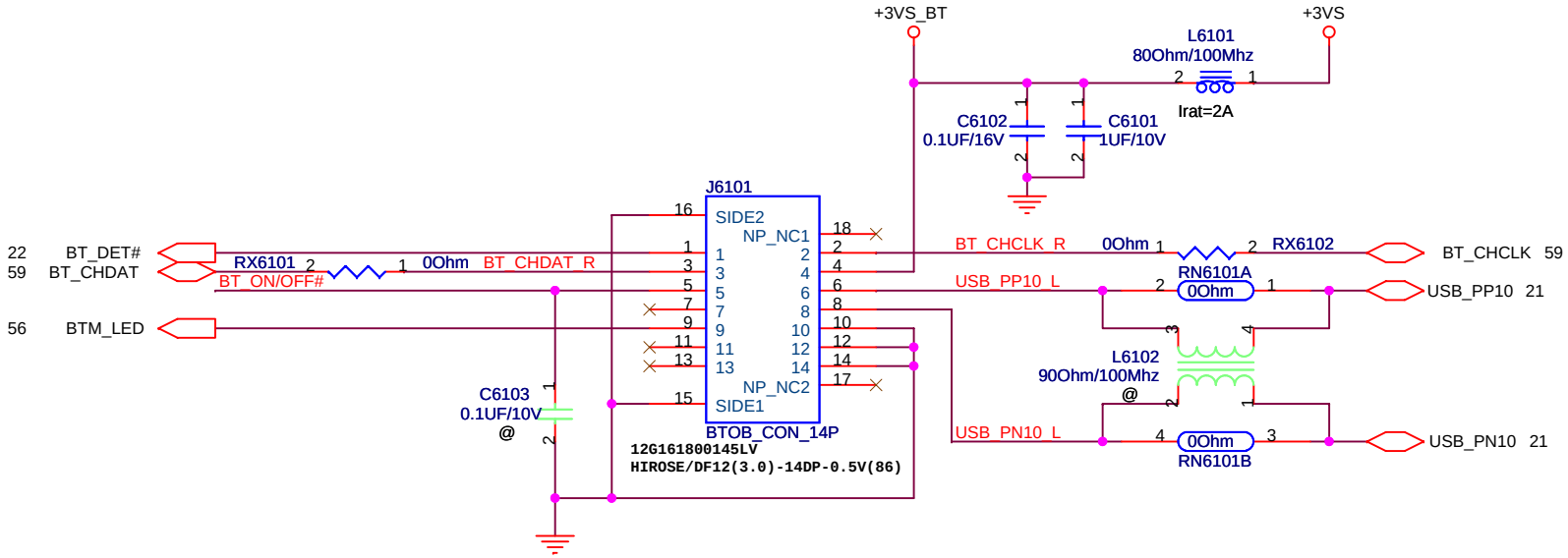
Without Battery & Pull out Adapter

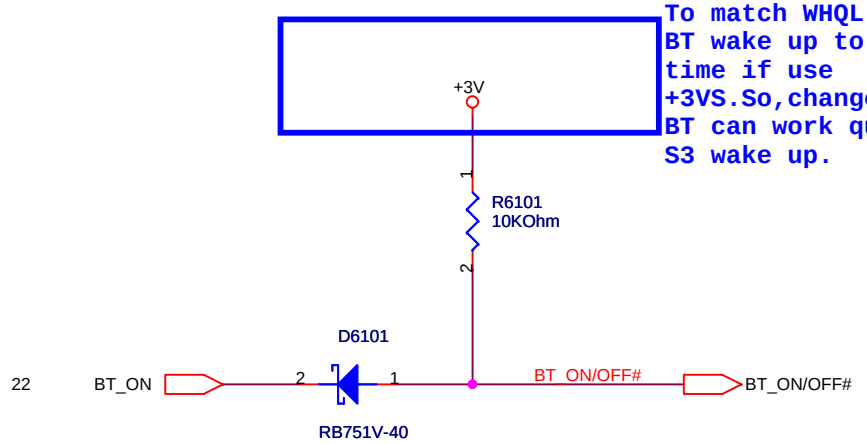
Battery CONN



Title : DC Jack & Battery CONN		
Engineer: Kevin Chang		
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 60 of 94	

Blue Tooth





To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

From GPIO27 ICH9

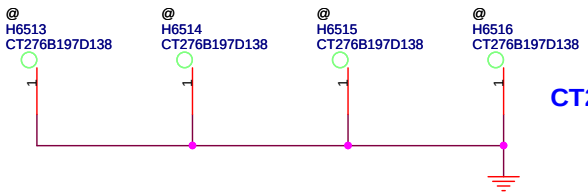
Title : BlueTooth		
Engineer: Peter Lo		
Size: A4	Project Name: Rocky30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 61 of 94	

Title :	***
Engineer:	*Peter Lo*
Size: A4	Project Name: **Rocky30**
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 62 of 94

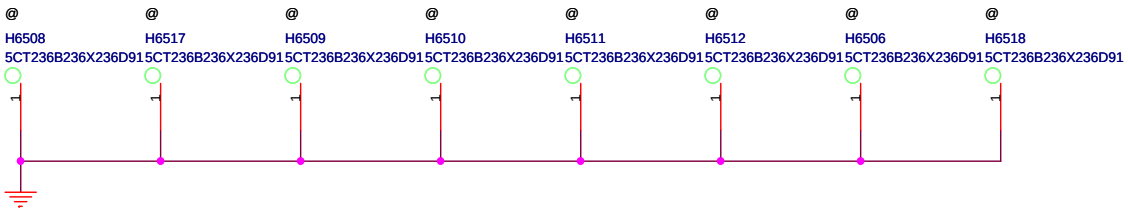
Title :	***
Engineer:	Peter Lo
Size: A4	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 63 of 94

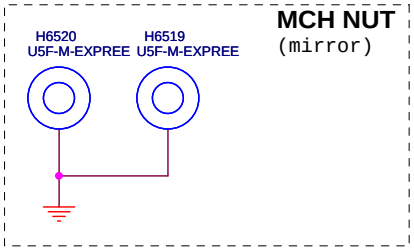
Title :	
Engineer:	Peter Lo
Size: A	Project Name: Rocky30
Rev:	1.0
Date:	Thursday, October 18, 2007
Sheet	64 of 94

CPU



TOP 5CT236B236X236D91 PTH





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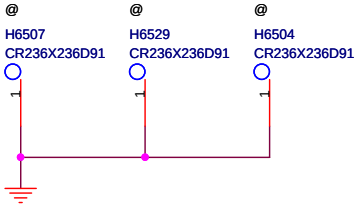
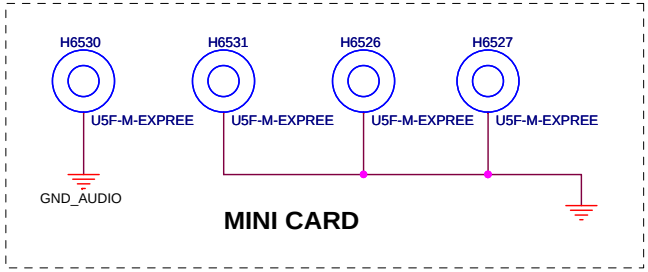
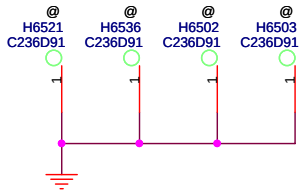


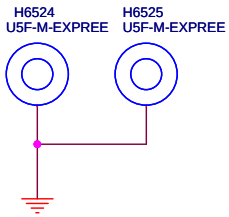
BOT 5CT236B236X236D91 PTH



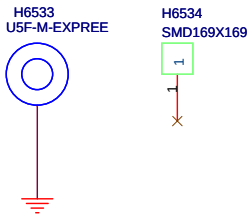
C236D91 PTH



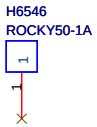
For Fan Stand Off
C236B189D150 PTH (mirror)



For KB Stand Off
C236B189D150 PTH

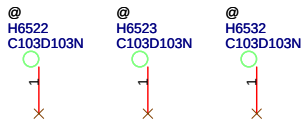


For BT StandOff



TOOLING HOLE

For ICT

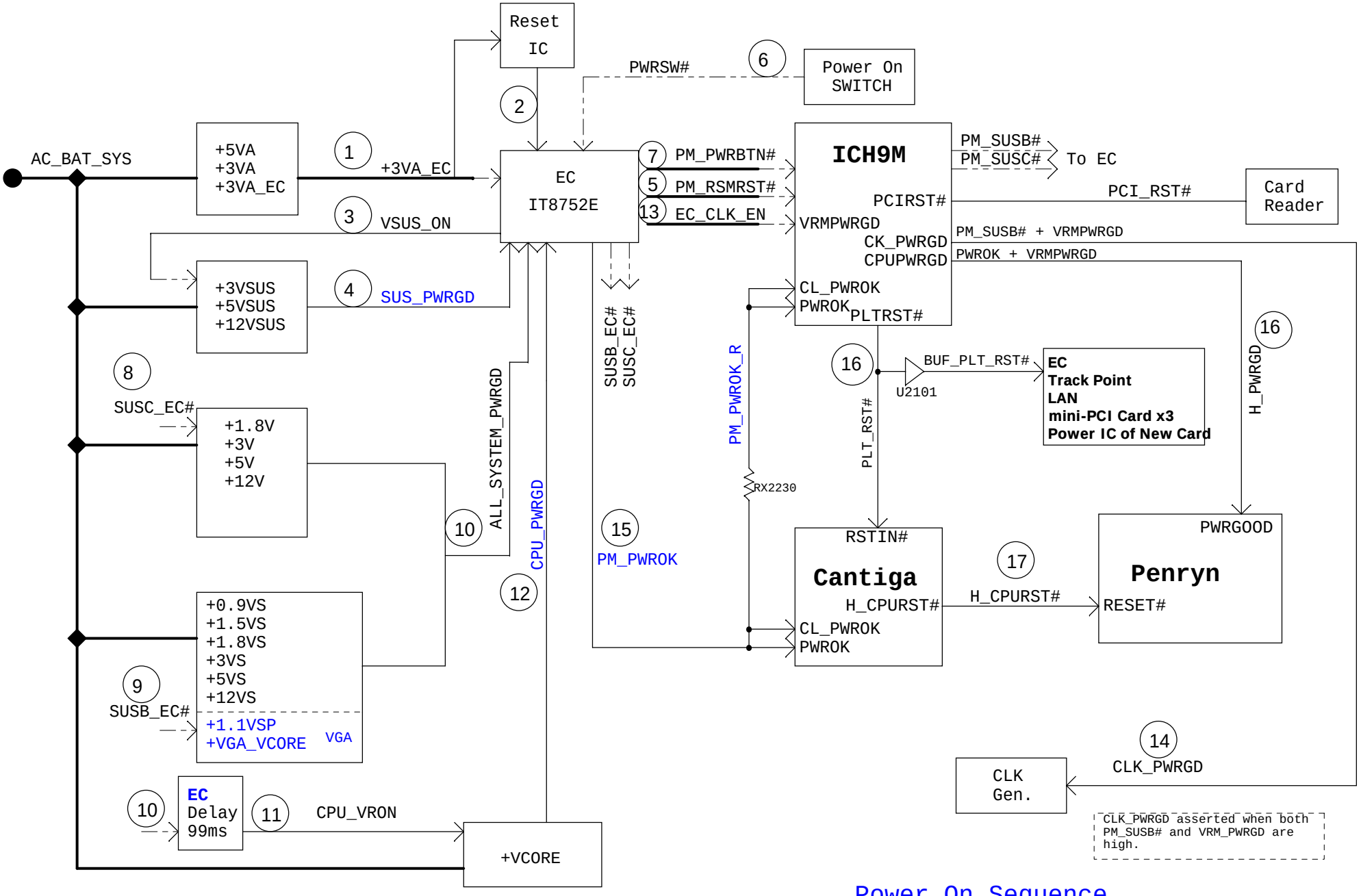


Title: MDC NUT & Hinksink NUT		
Engineer: Peter Lo		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Tuesday, January 22, 2008	Sheet 65 of 94	

Title :	***
Engineer:	*Peter Lo*
Size: Custom	Project Name: Rocky30
Rev: 1.0	
Date: Thursday, October 18, 2007	Sheet 66 of 94

Title : ***		
Engineer: *Peter Lo*		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Thursday, October 18, 2007	Sheet 67 of 94	

Title : ***		
Engineer: *Peter Lo*		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Thursday, October 18, 2007	Sheet 68 of 94	



Power On Sequence

1 → 17

ASUS	Title : Power Sequence	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Monday, November 05, 2007	Sheet 69 of 94	

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 70 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 71 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 72 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 73 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 74 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 75 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 76 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 77 of 94

Title : ***

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 78 of 94

Title :

Engineer: Peter Lo

Size	Project Name	Rev
A	Rocky30	1.0

Date: Thursday, October 18, 2007 Sheet 79 of 94

IMVP6 CPU VCORE REGULATOR

3.3V level logic level: DPRSLPVR, SHDN#

1.05V level logic: VID, PSI#, DPRSTP#

POUT=(VCSN2-VGNDS)x(CSP1-CNS1+CSP2-CSN2)/16.67mV

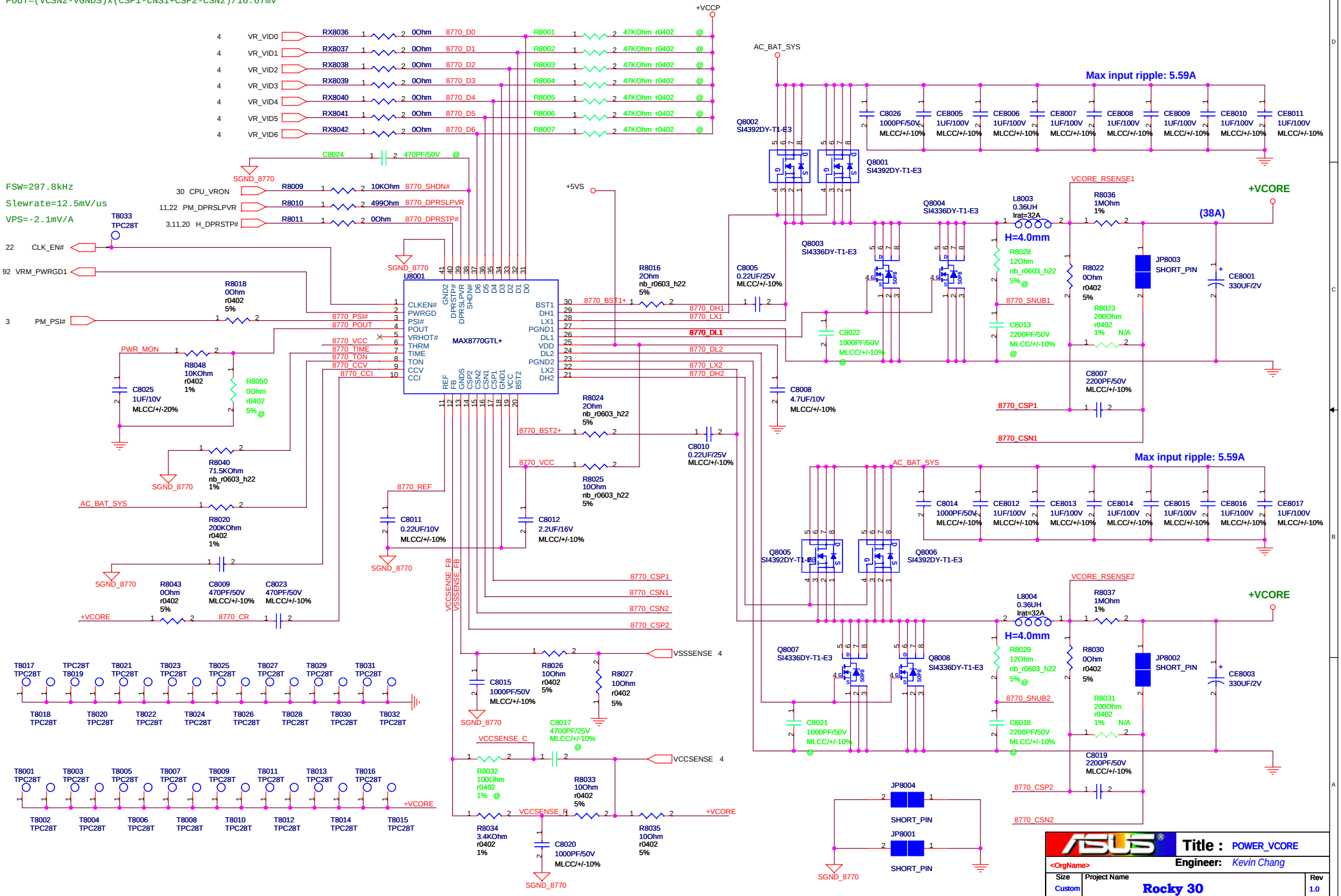
FSW=297.8kHz

Slewrate=12.5mV/us

VPS=-2.1mV/A

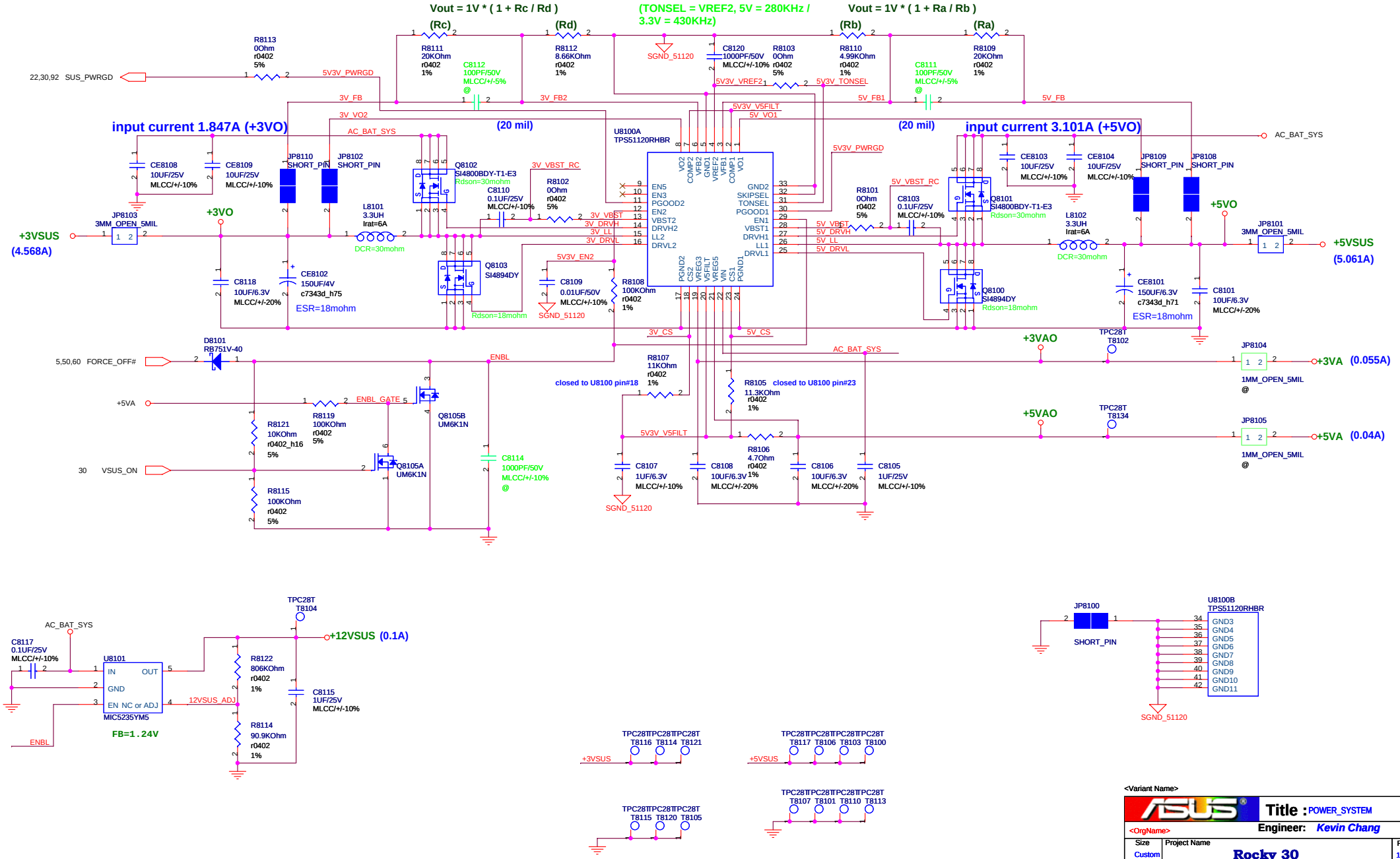
Max input ripple: 5.59A

Max input ripple: 5.59A



Title :	POWER_VCORE
<OrgName>	Engineer: Kevin Chang
Size: Custom	Project Name: Rocky 30
Rev	1.0
Date: Monday, February 04, 2008	Sheet 80 of 94

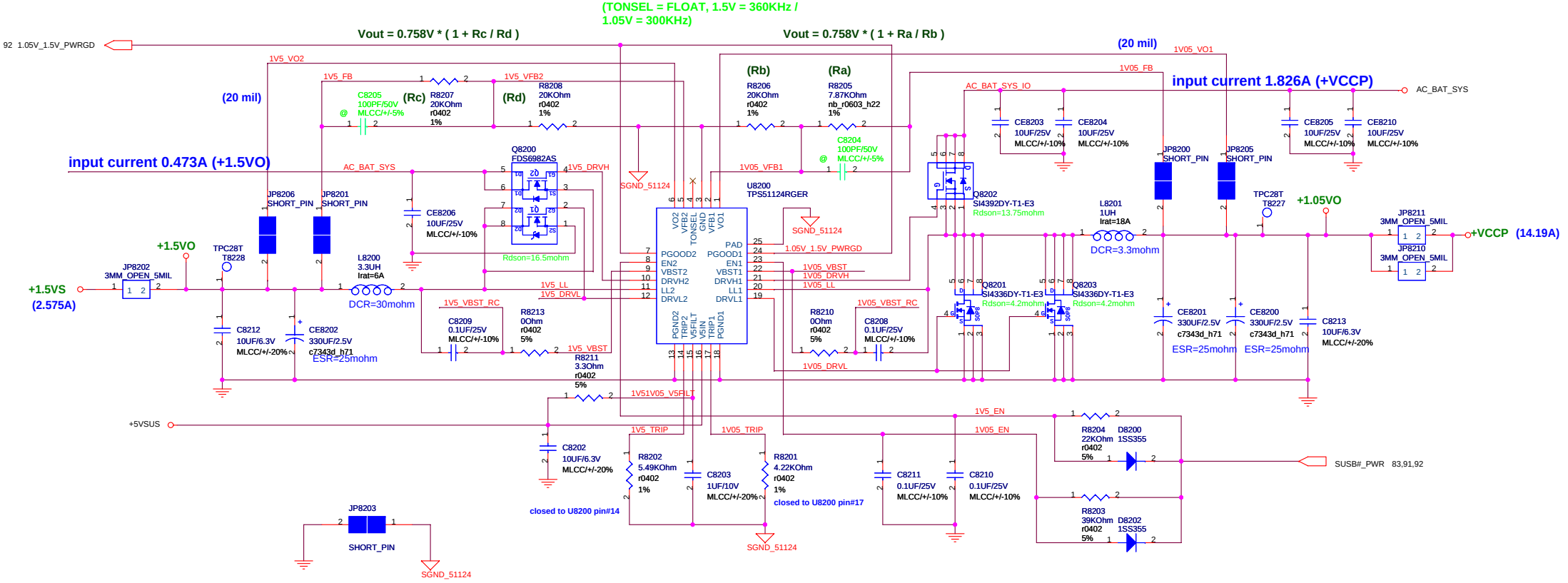
+5V / +3.3V POWER SUPPLY



<variant_name>

Title : POWER_SYSTEM		
<OrgName>	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 81 of 94	

+1.5VS / +VCCP POWER SUPPLY



<Variant Name>

ASUS

Title : POWER_I/O_1.5VS & 1.05VS

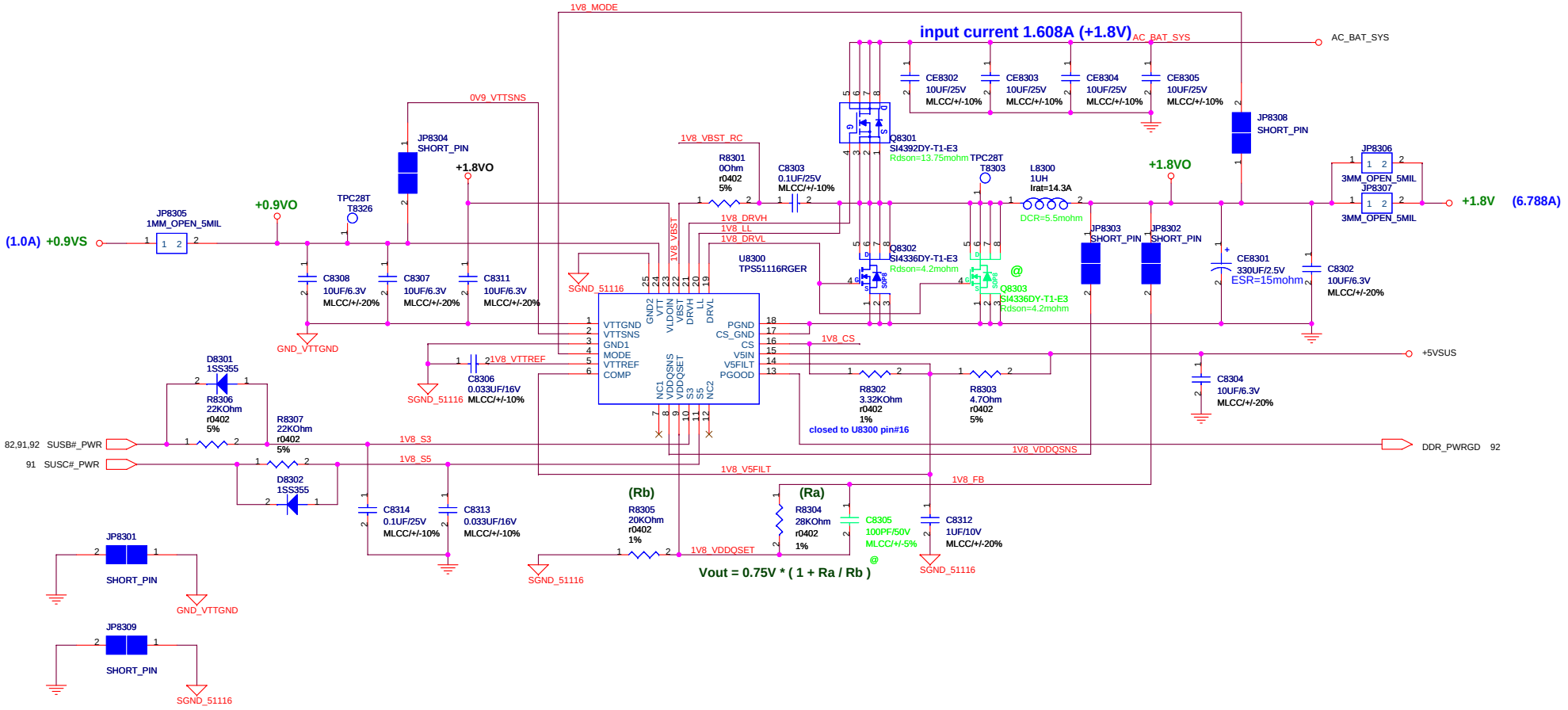
<OrgName>

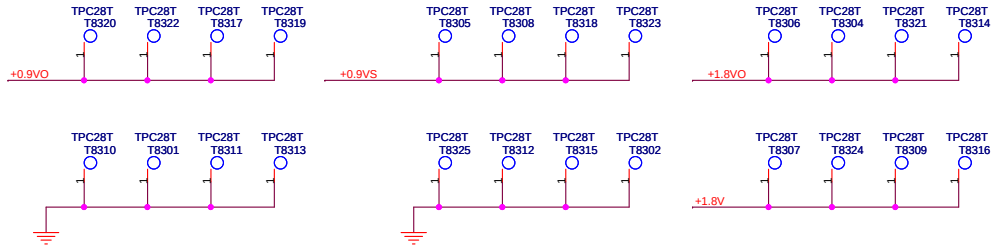
Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.0

Date: Monday, February 04, 2008 Sheet 82 of 94

+1.8V / +0.9VS POWER SUPPLY





<Variant Name>

Title : POWER_I/O_DDR & VTT

<OrgName>

Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.0

Date: Monday, February 04, 2008 Sheet 83 of 94

Title : PWR_-****

Engineer:

<OrgName>

Size	Project Name	Rev
A4	Rocky30	1.0

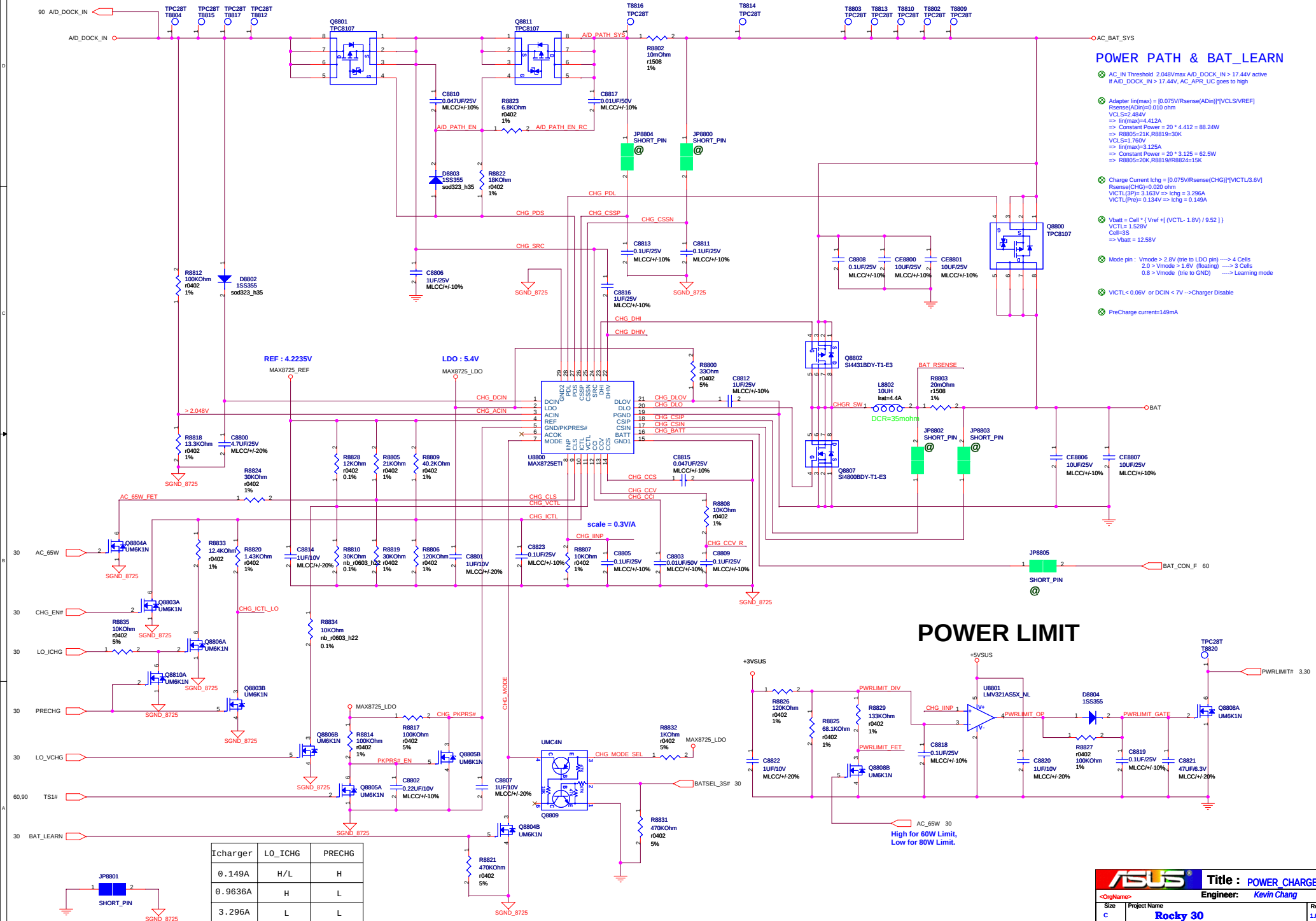
Date: Saturday, January 26, 2008 Sheet 84 of 94

Title :		
Engineer: Kevin Chang		
<OrgName>		
Size: Custom	Project Name: Rocky30	Rev: 1.0
Date: Friday, January 11, 2008	Sheet 85 of 94	

Title : PWR_-****		
<OrgName>	Engineer: Kevin Chang	
Size A4	Project Name Rocky30	Rev 1.0
Date: Friday, January 11, 2008	Sheet 86 of 94	

Title : POWER_SHUTDOWN#				
Engineer: <OrgName>				
Size: A4	Project Name: Rocky30			Rev: 1.0
Date: Saturday, January 26, 2008		Sheet 87 of 94		

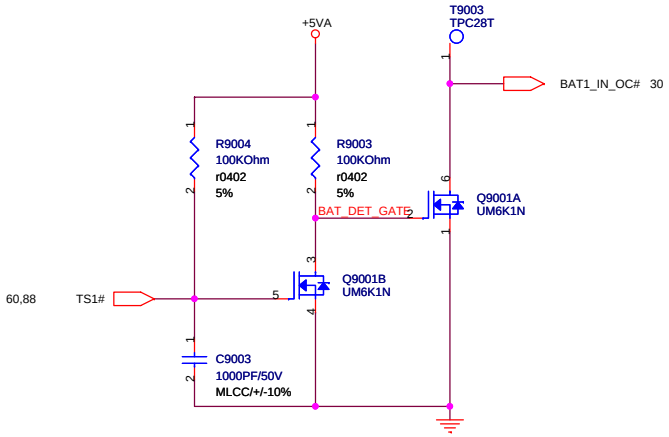
BATTERY CHARGER



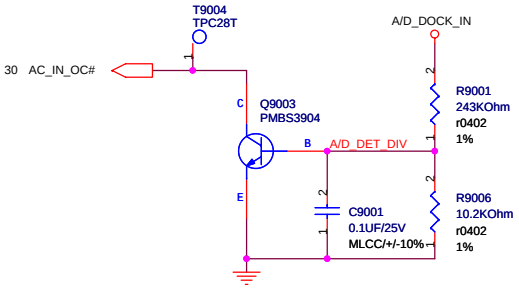
Title :	POWER_CHARGER	
<OrgName>	Engineer:	Kevin Chang
Size: C	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 88 of 94	

Title :	TFT-LCD DRIVE
<OrgName>	Engineer:
Size: A4	Project Name: Rocky30
Rev: 1.0	
Date: Friday, January 11, 2008	Sheet 89 of 94

BATTERY IN DETECT

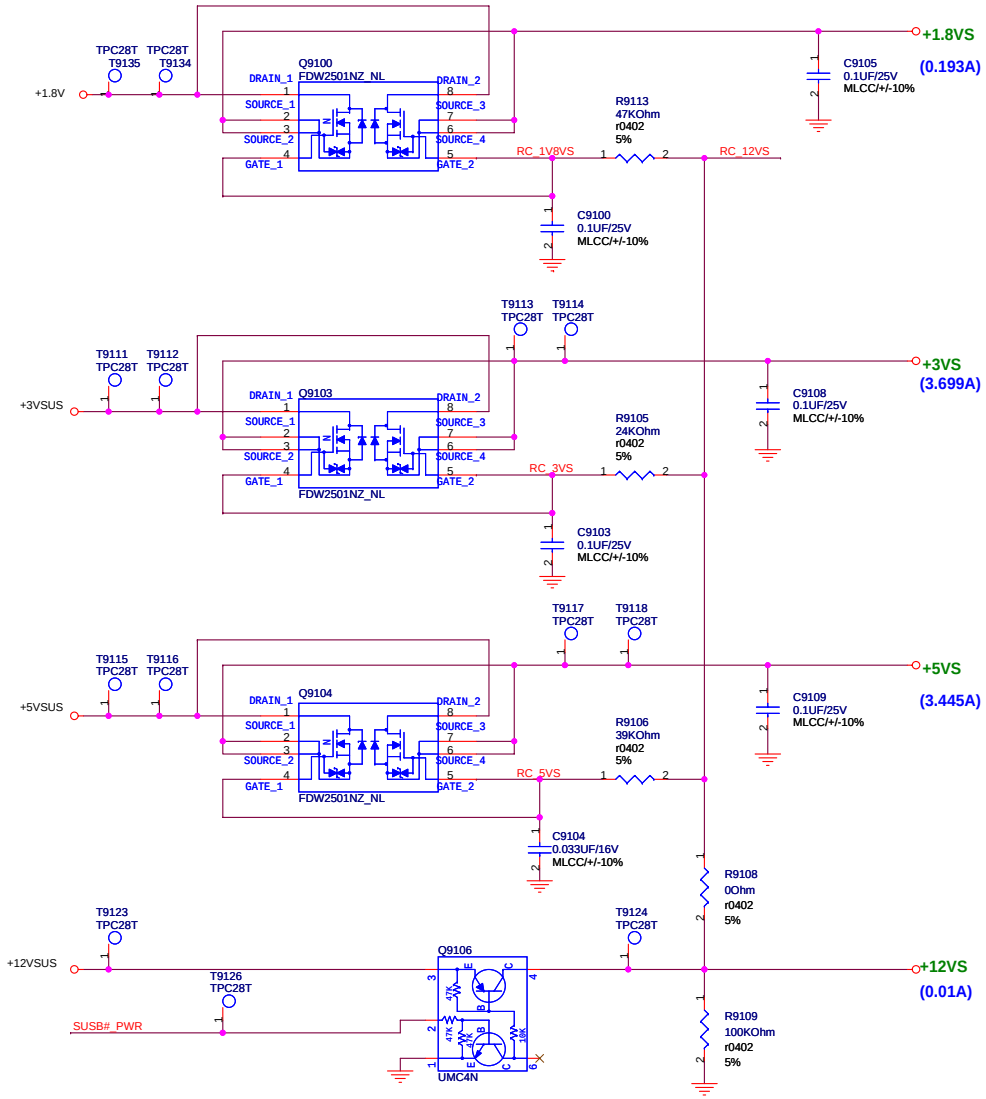


ADAPTER IN DETECT

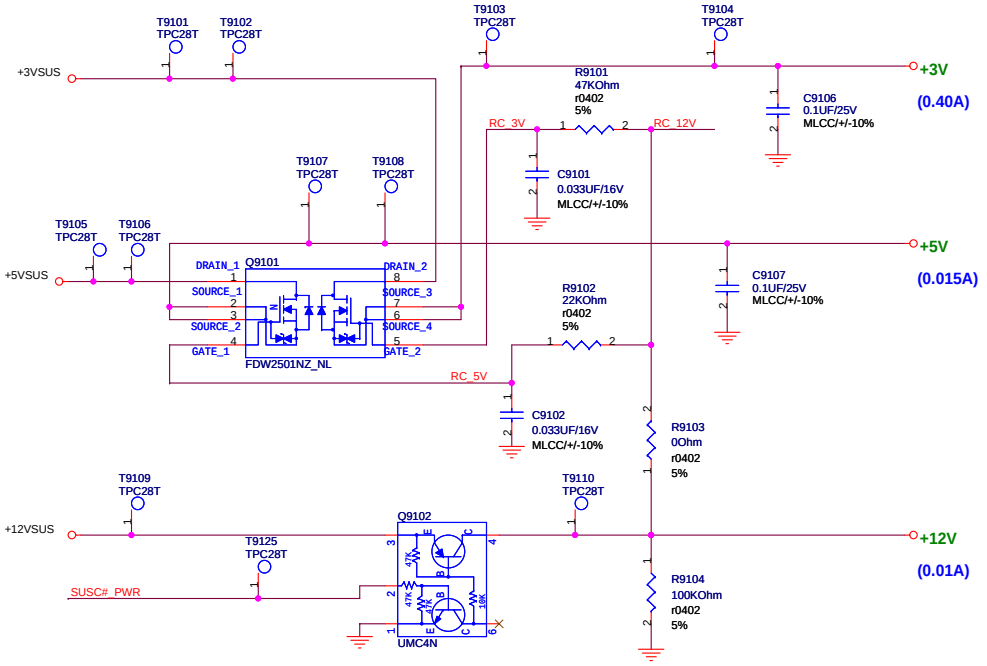


Title : POWER_DETECT		
<OrgName>	Engineer: Kevin Chang	
Size: A3	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 90 of 94	

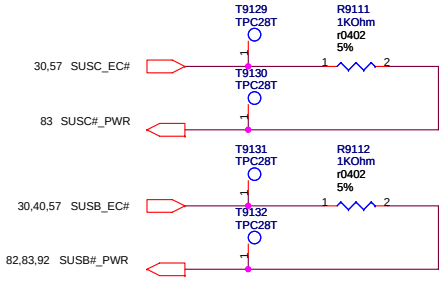
SUSB#_PWR Load SW



SUSC#_PWR Load SW

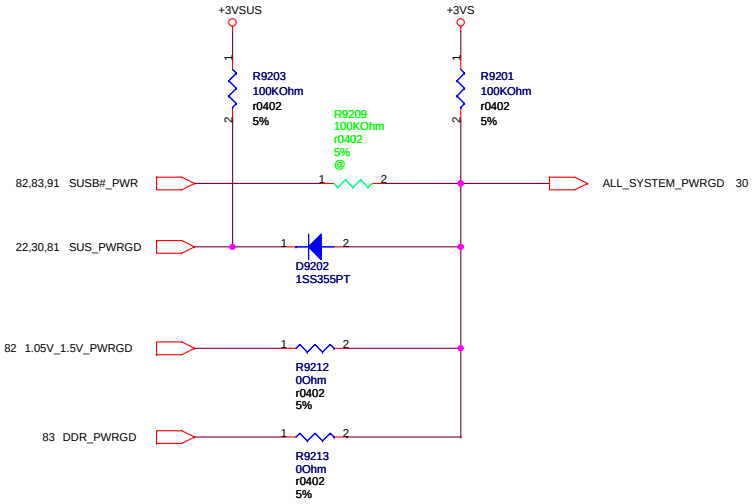


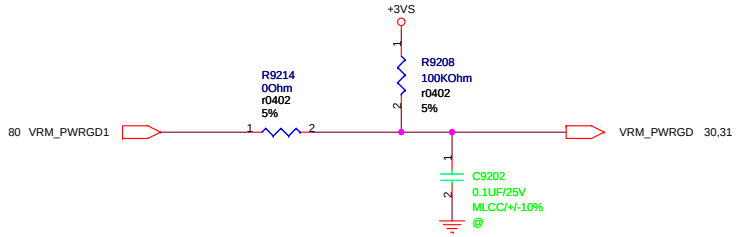
Enable Signal



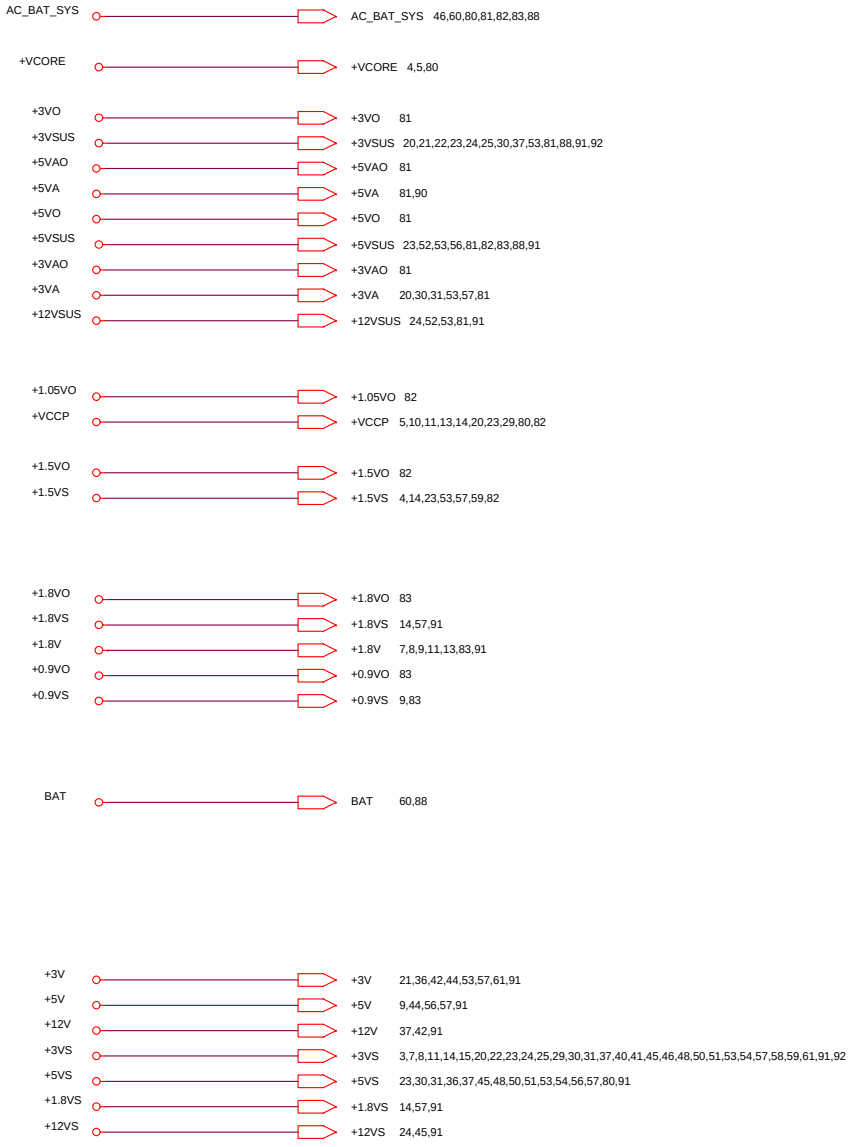
ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 91 of 94	

POWER GOOD DETECTER

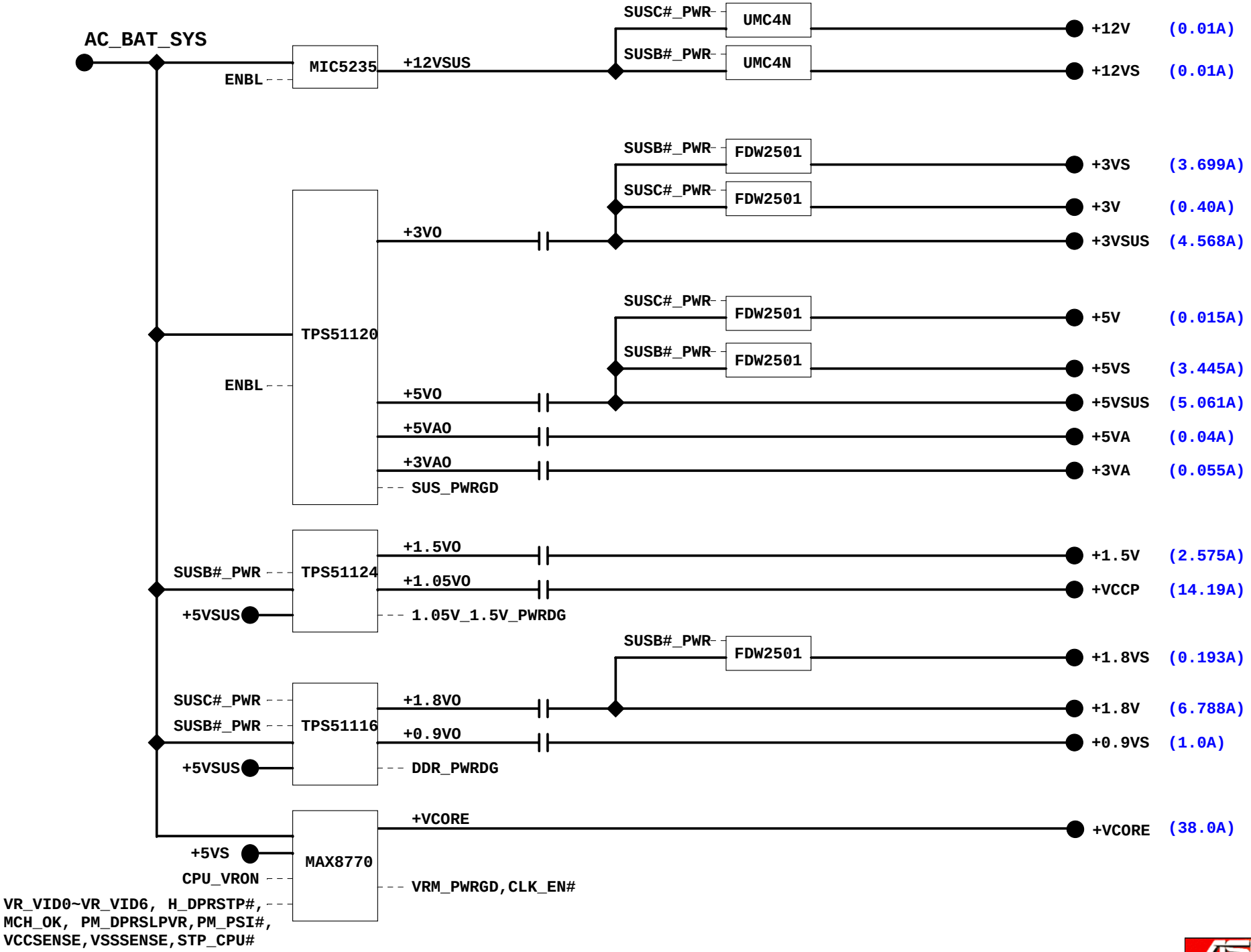




Title : POWER_PROTECT		
Engineer: Kevin Chang		
<OrgName>		
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 92 of 94	



<OrgName>	Title : POWER_SIGNAL	
	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.0
Date: Monday, February 04, 2008	Sheet 93 of 94	



Title : POWER_FLOWCHART			
<OrgName>	Engineer: Kevin Chang		
Size: Custom	Project Name: Rocky 30		Rev: 1.0
Date: Saturday, January 26, 2008	Sheet 94 of 94		