LCFC Confidential

KENOBI NM-A821 Rev2.0 Schematic

Intel KabyLake Processor with DDR4 + PCH-LP
NVIDA N16V-GMR GDDR3 2GB
2016-08-24 Rev2.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: COVER PAGE

Size	Document Number	Rev
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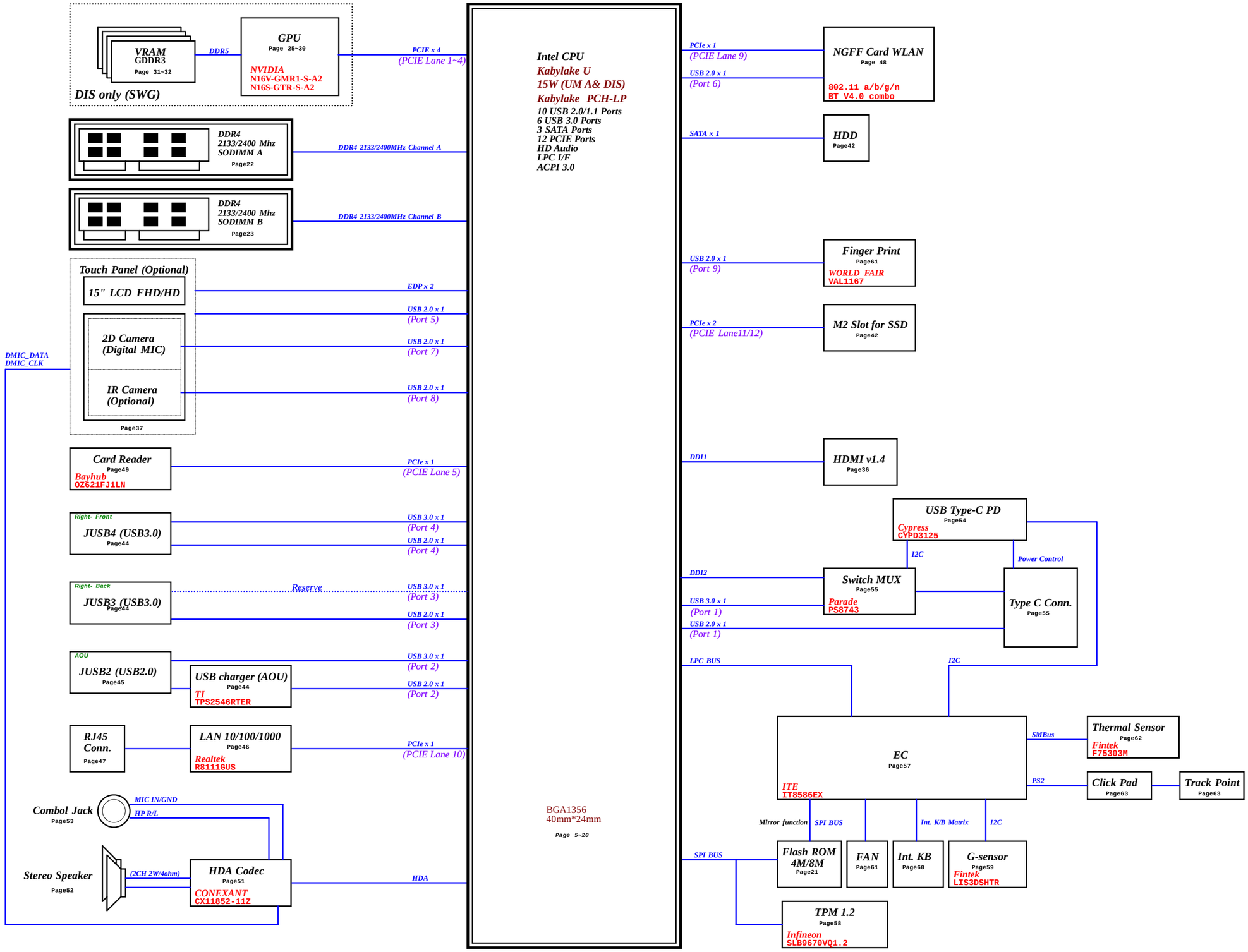
Kenobi KBL U Block Diagram



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	BLOCK DIAGRAM		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+ +3VL	+3VALW +5VALW +1VALW +1.8VALW	+2.5V +1.2V +VCC_STG	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VGA_CORE +3VS_VGA +1.5VS_VGA +3VS_AON +1VS_VGA +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#	SYSON
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	HIGH
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	HIGH
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF	LOW
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF	LOW

SMBUS Control Table

	SOURCE	Main VGA	BATT (Charger)	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	LAN PHY	G sensor	USB Type-C
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580F +3VL	X	X	X	X	X	X	X	X	X	V +3VPD_VDD
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	V +3VS_GS	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	X	X	X	V +5VS	X	X	X
PCH_SML1CLK PCH_SML1DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	X	X

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
SSD@	SSD setting
FRP@	Finger printer setting
TYPEC@	For USB Type-C function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
MIRROR@	For mirror function
NGC6@	For VGA Non GC6 function
GC6@	For VGA GC6 function

USB2 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3
4	JUSB4
5	Touch Panel
6	BT
7	CMOS
8	IR CAMERA
9	FP/Smart

USB3 Port

Port	Device
1	JUSB1 TYPE-C
2	JUSB2
3	JUSB3
4	JUSB4

PCIE Port

Port	Device
1	GPU
2	GPU
3	GPU
4	GPU
5	CardReader
6	X
7	X
8	X
9	WLAN
10	LAN
11	M.2 SSD
12	M.2 SSD

SATA Port

Port	Device
1	HDD
2	X
3	X
4	X

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Title: NOTE LIST

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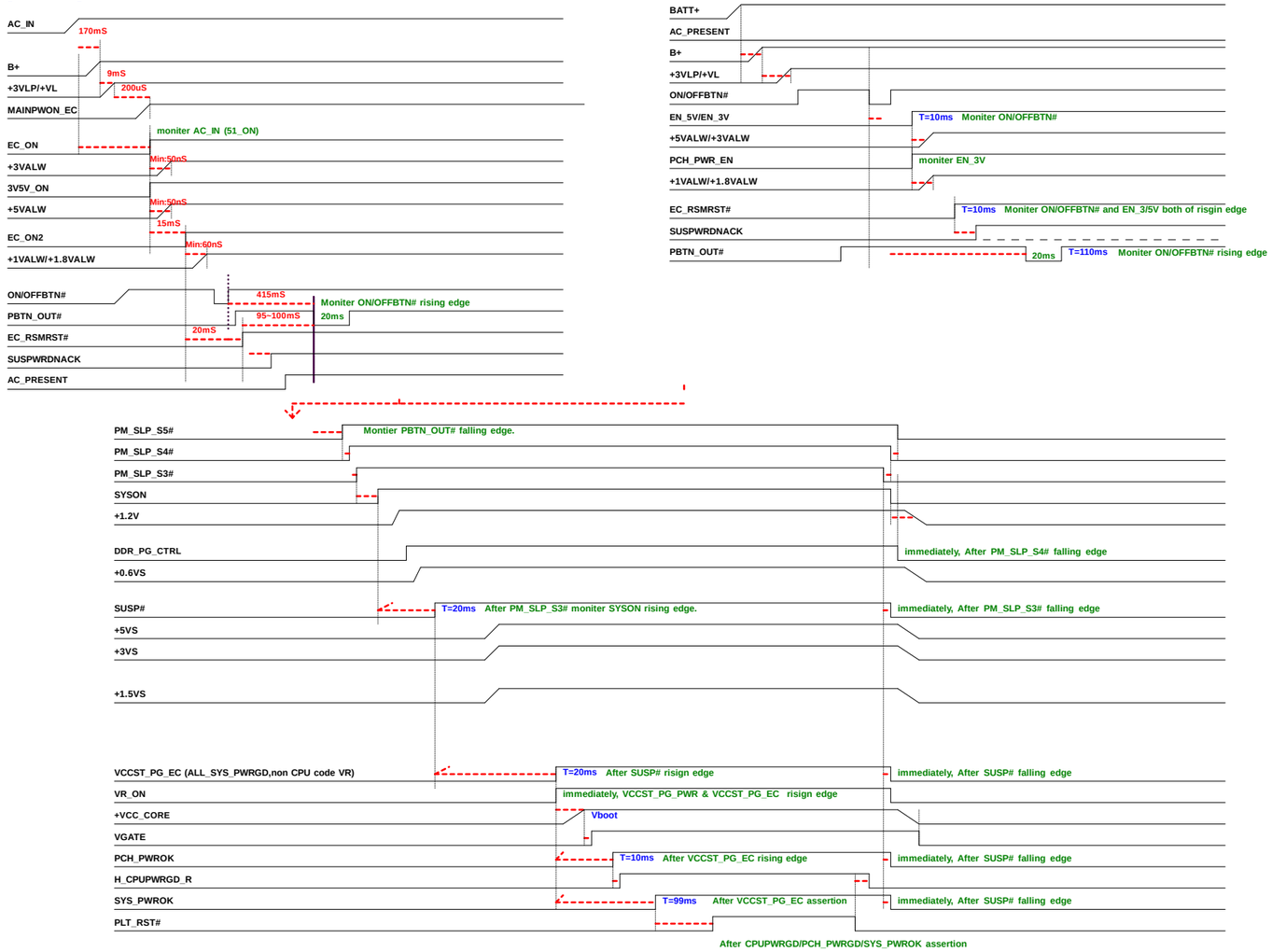
[KENOBI PWR Sequence_SKL-U_DDR4_Non-Deep Sx]

[AC Mode]



[DC Mode]

Security Classification	LC Future Center Secret Data		
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Title: Power Sequence

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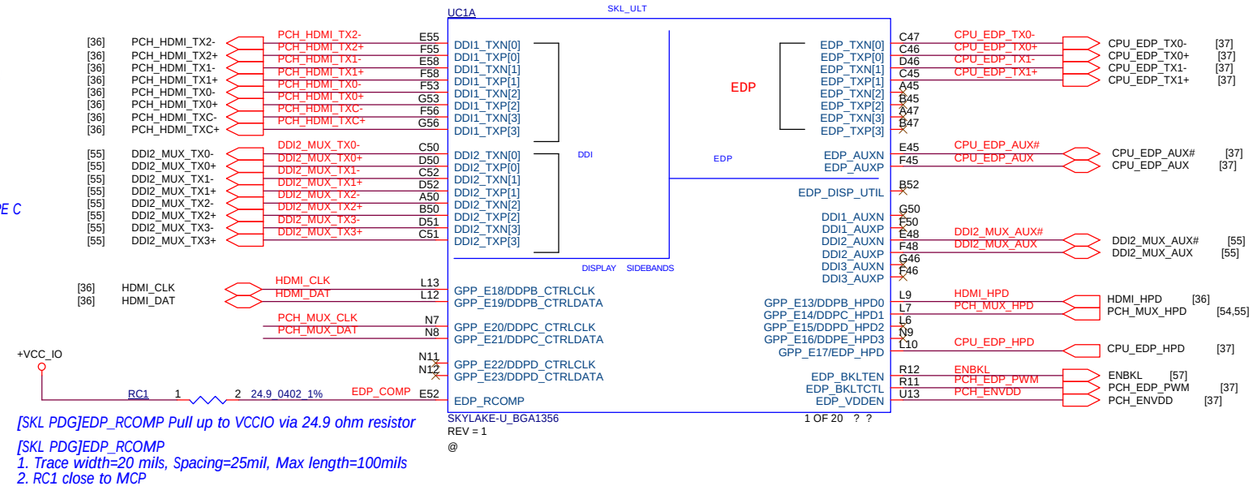
HDMI

USB TYPE C

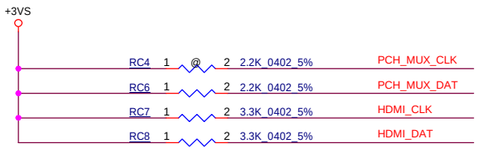


[SKL PDG]EDP_RCOMP Pull up to VCCIO via 24.9 ohm resistor

[SKL PDG]EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC1 close to MCP

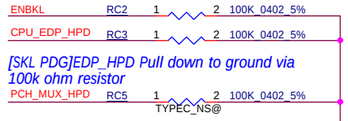
EDP

DDPB_CTRLDATA, DDPC_CTRLDATA Internal PD 20K



20160218
Staff RC7/RC8 for HDMI detect issue

DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.



[SKL PDG]EDP_HPD Pull down to ground via 100k ohm resistor

20160824
Change RC5 from @ to TYPEC_NS@
(Only for Non Type-C SKU)

Title: **KBL(1/16):DDI/EDP**

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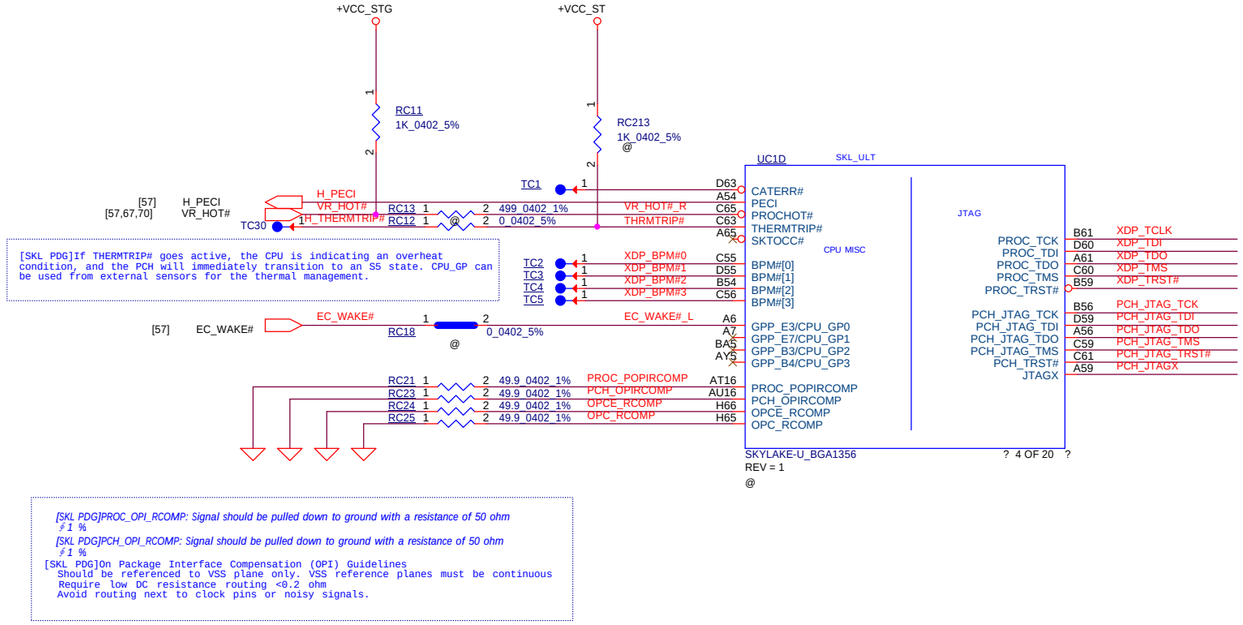
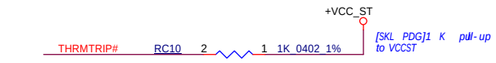
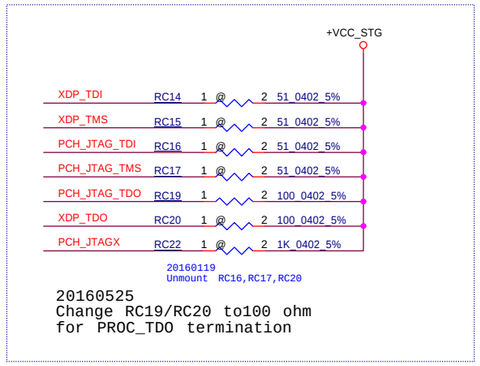
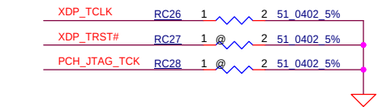








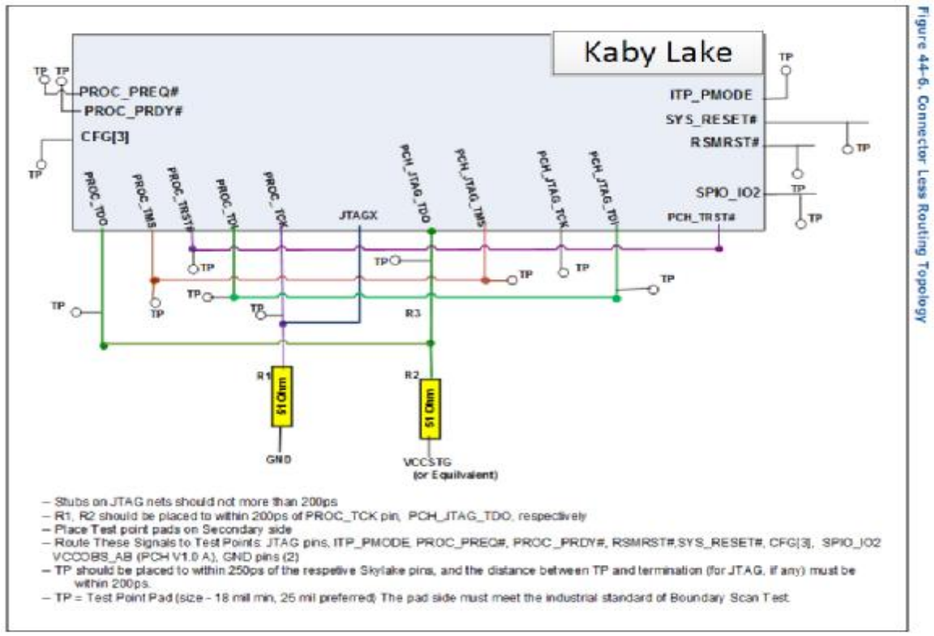
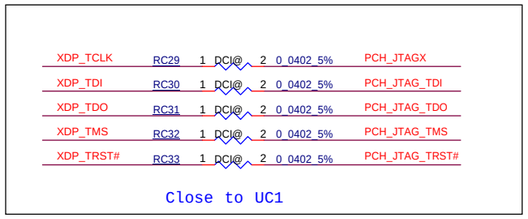


Figure 4-4-6. Connector Less Routing Topology

– Stubs on JTAG nets should not more than 200ps
– R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2 VCCDBS_AB (PCH V1.0 A), GND pins (2)
– TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
– TP = Test Point Pad (size – 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test



Termination option

XDP_TCLK

PROC_TCK Termination:
51 ohm +/- 5% pull down to GNG (Ground)
Placed to within 200ps (1100 mil) or PROC_TCK pin

PCH_JTAG_TDO

PCH_JTAG_TDO Termination:
51ohm +/- 5% pull up to VccSTG or equivalent.
Placed to within 200ps (1100 mil) or PCH_JTAG_TDO pin

Title: KBL(2/16):MISC/JTAG

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TABLE

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[8]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
	AU70	DDR0_DQ[14]	DDR0_DQ[14]
	AU69	DDR0_DQ[15]	DDR0_DQ[15]
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[36]
	BA65	DDR0_DQ[20]	DDR0_DQ[38]
	AY65	DDR0_DQ[21]	DDR0_DQ[39]
	BA63	DDR0_DQ[22]	DDR0_DQ[40]
	BB63	DDR0_DQ[23]	DDR0_DQ[41]
	BA61	DDR0_DQ[24]	DDR0_DQ[42]
	AW61	DDR0_DQ[25]	DDR0_DQ[43]
	BB59	DDR0_DQ[26]	DDR0_DQ[44]
	AW59	DDR0_DQ[27]	DDR0_DQ[45]
	BB61	DDR0_DQ[28]	DDR0_DQ[46]
	AY61	DDR0_DQ[29]	DDR0_DQ[47]
	BA59	DDR0_DQ[30]	DDR0_DQ[0]
	AY59	DDR0_DQ[31]	DDR0_DQ[1]
	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[36]	DDR1_DQ[3]
	BB39	DDR0_DQ[38]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[39]	DDR1_DQ[8]
	BB37	DDR0_DQ[38]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
	BA33	DDR0_DQ[46]	DDR1_DQ[14]
	BB33	DDR0_DQ[47]	DDR1_DQ[15]
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[36]
	BB31	DDR0_DQ[52]	DDR1_DQ[38]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[39]
	BB29	DDR0_DQ[55]	DDR1_DQ[40]
	AY27	DDR0_DQ[56]	DDR1_DQ[41]
	AW27	DDR0_DQ[57]	DDR1_DQ[42]
	AY25	DDR0_DQ[58]	DDR1_DQ[43]
	AW25	DDR0_DQ[59]	DDR1_DQ[44]
	BB27	DDR0_DQ[60]	DDR1_DQ[45]
	BA27	DDR0_DQ[61]	DDR1_DQ[46]
	BA25	DDR0_DQ[62]	DDR1_DQ[47]
	BB25	DDR0_DQ[63]	DDR1_DQ[48]

TABLE

	Pin	Interleave	Non-Interleave
Block 0	AM70	DDR0_DQSN[0]	DDR0_DQSN[0]
	AM69	DDR0_DQSP[0]	DDR0_DQSP[0]
	AT69	DDR0_DQSN[1]	DDR0_DQSN[1]
	AT70	DDR0_DQSP[1]	DDR0_DQSP[1]
Block 2	BA64	DDR0_DQSN[2]	DDR0_DQSN[4]
	AY64	DDR0_DQSP[2]	DDR0_DQSP[4]
	AY60	DDR0_DQSN[3]	DDR0_DQSN[5]
	BA60	DDR0_DQSP[3]	DDR0_DQSP[5]
Block 4	BA38	DDR0_DQSN[4]	DDR1_DQSN[0]
	AY38	DDR0_DQSP[4]	DDR1_DQSP[0]
	AY34	DDR0_DQSN[5]	DDR1_DQSN[1]
	BA34	DDR0_DQSP[5]	DDR1_DQSP[1]
Block 6	BA30	DDR0_DQSN[6]	DDR1_DQSN[4]
	AY30	DDR0_DQSP[6]	DDR1_DQSP[4]
	AY26	DDR0_DQSN[7]	DDR1_DQSN[5]
	BA26	DDR0_DQSP[7]	DDR1_DQSP[5]

TABLE

Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

[22] DDR_A_D[63..0]

UC1B

SKL_ULT

DDR_A_D0 AL71 DDR0_DQ[0]
DDR_A_D1 AL68 DDR0_DQ[1]
DDR_A_D2 AN68 DDR0_DQ[2]
DDR_A_D3 AN69 DDR0_DQ[3]
DDR_A_D4 AL70 DDR0_DQ[4]
DDR_A_D5 AL69 DDR0_DQ[5]
DDR_A_D6 AN70 DDR0_DQ[6]
DDR_A_D7 AN71 DDR0_DQ[7]
DDR_A_D8 AR70 DDR0_DQ[8]
DDR_A_D9 AR68 DDR0_DQ[9]
DDR_A_D10 AU71 DDR0_DQ[10]
DDR_A_D11 AU68 DDR0_DQ[11]
DDR_A_D12 AR71 DDR0_DQ[12]
DDR_A_D13 AR69 DDR0_DQ[13]
DDR_A_D14 AU70 DDR0_DQ[14]
DDR_A_D15 AU69 DDR0_DQ[15]
DDR_A_D16 BB65 DDR0_DQ[16]/DDR0_DQ[32]
DDR_A_D17 AW65 DDR0_DQ[17]/DDR0_DQ[33]
DDR_A_D18 AW63 DDR0_DQ[18]/DDR0_DQ[34]
DDR_A_D19 AY63 DDR0_DQ[19]/DDR0_DQ[35]
DDR_A_D20 BA65 DDR0_DQ[20]/DDR0_DQ[36]
DDR_A_D21 AY65 DDR0_DQ[21]/DDR0_DQ[37]
DDR_A_D22 BA63 DDR0_DQ[22]/DDR0_DQ[38]
DDR_A_D23 BB63 DDR0_DQ[23]/DDR0_DQ[39]
DDR_A_D24 BA61 DDR0_DQ[24]/DDR0_DQ[40]
DDR_A_D25 AW61 DDR0_DQ[25]/DDR0_DQ[41]
DDR_A_D26 BB59 DDR0_DQ[26]/DDR0_DQ[42]
DDR_A_D27 AW59 DDR0_DQ[27]/DDR0_DQ[43]
DDR_A_D28 BB61 DDR0_DQ[28]/DDR0_DQ[44]
DDR_A_D29 AY61 DDR0_DQ[29]/DDR0_DQ[45]
DDR_A_D30 BA59 DDR0_DQ[30]/DDR0_DQ[46]
DDR_A_D31 AY59 DDR0_DQ[31]/DDR0_DQ[47]
DDR_A_D32 AY39 DDR0_DQ[32]/DDR1_DQ[0]
DDR_A_D33 AW39 DDR0_DQ[33]/DDR1_DQ[1]
DDR_A_D34 AY37 DDR0_DQ[34]/DDR1_DQ[2]
DDR_A_D35 AW37 DDR0_DQ[35]/DDR1_DQ[3]
DDR_A_D36 BB39 DDR0_DQ[36]/DDR1_DQ[4]
DDR_A_D37 BA39 DDR0_DQ[37]/DDR1_DQ[5]
DDR_A_D38 BA37 DDR0_DQ[38]/DDR1_DQ[6]
DDR_A_D39 BB37 DDR0_DQ[39]/DDR1_DQ[7]
DDR_A_D40 AY35 DDR0_DQ[40]/DDR1_DQ[8]
DDR_A_D41 AW35 DDR0_DQ[41]/DDR1_DQ[9]
DDR_A_D42 AY33 DDR0_DQ[42]/DDR1_DQ[10]
DDR_A_D43 AW33 DDR0_DQ[43]/DDR1_DQ[11]
DDR_A_D44 BB35 DDR0_DQ[44]/DDR1_DQ[12]
DDR_A_D45 BA35 DDR0_DQ[45]/DDR1_DQ[13]
DDR_A_D46 BA33 DDR0_DQ[46]/DDR1_DQ[14]
DDR_A_D47 BB33 DDR0_DQ[47]/DDR1_DQ[15]
DDR_A_D48 AY31 DDR0_DQ[48]/DDR1_DQ[32]
DDR_A_D49 AW31 DDR0_DQ[49]/DDR1_DQ[33]
DDR_A_D50 AY29 DDR0_DQ[50]/DDR1_DQ[34]
DDR_A_D51 AW29 DDR0_DQ[51]/DDR1_DQ[35]
DDR_A_D52 BB31 DDR0_DQ[52]/DDR1_DQ[36]
DDR_A_D53 BA31 DDR0_DQ[53]/DDR1_DQ[37]
DDR_A_D54 BA29 DDR0_DQ[54]/DDR1_DQ[38]
DDR_A_D55 BB29 DDR0_DQ[55]/DDR1_DQ[39]
DDR_A_D56 AY27 DDR0_DQ[56]/DDR1_DQ[40]
DDR_A_D57 AW27 DDR0_DQ[57]/DDR1_DQ[41]
DDR_A_D58 AY25 DDR0_DQ[58]/DDR1_DQ[42]
DDR_A_D59 AW25 DDR0_DQ[59]/DDR1_DQ[43]
DDR_A_D60 BB27 DDR0_DQ[60]/DDR1_DQ[44]
DDR_A_D61 BA27 DDR0_DQ[61]/DDR1_DQ[45]
DDR_A_D62 BA25 DDR0_DQ[62]/DDR1_DQ[46]
DDR_A_D63 BB25 DDR0_DQ[63]/DDR1_DQ[47]

DDR CH - A

SKYLAKE-U_BGA1356
REV = 1
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DDR0_CKN[0] AU53 DDR_A_DDRCLK0_1866M# → DDR_A_DDRCLK0_1866M# [22]
DDR0_CKP[0] AT53 DDR_A_DDRCLK0_1866M → DDR_A_DDRCLK0_1866M [22]
DDR0_CKN[1] AU55 DDR_A_DDRCLK1_1866M# → DDR_A_DDRCLK1_1866M# [22]
DDR0_CKP[1] AT55 DDR_A_DDRCLK1_1866M → DDR_A_DDRCLK1_1866M [22]

DDR0_CKE[0] BA56 DDR_A_CKE0 → DDR_A_CKE0 [22]
DDR0_CKE[1] BB56 DDR_A_CKE1 → DDR_A_CKE1 [22]
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 DDR_A_CS0# → DDR_A_CS0# [22]
DDR0_CS#[1] AU43 DDR_A_CS1# → DDR_A_CS1# [22]
DDR0_ODT[0] AT45 DDR_A_ODT0 → DDR_A_ODT0 [22]
DDR0_ODT[1] AT43 DDR_A_ODT1 → DDR_A_ODT1 [22]

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 DDR_A_MA5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 DDR_A_MA9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 DDR_A_MA6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 DDR_A_MA8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 DDR_A_MA7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 DDR_A_BG0
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 DDR_A_MA12 → DDR_A_BG0 [22]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 DDR_A_MA11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 DDR_A_ACT_N
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 DDR_A_BG1 → DDR_A_ACT_N [22], DDR_A_BG1 [22]

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 DDR_A_MA13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 DDR_A_MA15
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 DDR_A_MA14
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 DDR_A_MA16
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52 DDR_A_BA0
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 DDR_A_MA2 → DDR_A_BA0 [22]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 DDR_A_BA1
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 DDR_A_MA10 → DDR_A_BA1 [22]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 DDR_A_MA1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 DDR_A_MA0
DDR0_MA[3] BA50 DDR_A_MA3
DDR0_MA[4] BB52 DDR_A_MA4

DDR0_DQSN[0] AM70 DDR_A_DQS#0
DDR0_DQSP[0] AM69 DDR_A_DQS0
DDR0_DQSN[1] AT69 DDR_A_DQS#1
DDR0_DQSP[1] AT70 DDR_A_DQS1
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 DDR_A_DQS#2
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 DDR_A_DQS2
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 DDR_A_DQS#3
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 DDR_A_DQS3
DDR0_DQSN[4]/DDR1_DQSN[0] BA38 DDR_A_DQS#4
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 DDR_A_DQS4
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 DDR_A_DQS#5
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 DDR_A_DQS5
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 DDR_A_DQS#6
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 DDR_A_DQS6
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 DDR_A_DQS#7
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 DDR_A_DQS7

DDR0_ALERT# AW50 DDR_A_ALERT_N → DDR_A_ALERT_N [22]
DDR0_PAR AT52 DDR_A_PARITY → DDR_A_PARITY [22]

DDR_VREF_CA AY67 DDR4_VREF_CA_CPU_A → DDR4_VREF_CA_CPU_A [22]
DDR0_VREF_DQ AY68 DDR4_VREF_DQ_CPU_A → TC31 1
DDR1_VREF_DQ BA67 DDR4_VREF_DQ_CPU_B → DDR4_VREF_DQ_CPU_B [23]

DDR_VTT_CNTL AW67 DDR_PG_CTRL

DDR_A_MA0
DDR_A_MA1
DDR_A_MA2
DDR_A_MA3
DDR_A_MA4
DDR_A_MA5
DDR_A_MA6
DDR_A_MA7
DDR_A_MA8
DDR_A_MA9
DDR_A_MA10
DDR_A_MA11
DDR_A_MA12
DDR_A_MA13
DDR_A_MA14
DDR_A_MA15
DDR_A_MA16
→ DDR_A_MA[0..16] [22]

DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7
→ DDR_A_DQS#[0..7] [22]

DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7
→ DDR_A_DQS[0..7] [22]

+1.2V
+3VALW
+3VS

UC2
74AUP1G07GF_SOT891-6_1X1
1 NC1
2 A
3 GND
6 Vcc
5 NC2
4 Y

DDR_PG_CTRL

RC34 100K_0402_5%
RC214 100K_0402_5% @

SM_PG_CTRL [69]

CC1 0.1U_0402_10V7-K

20160118
Reserve RC214 for leakage issue

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(3/16):DDR4 CH.A

Size: Custom | Document Number: KENOBI | Rev: 2.0

Date: Thursday, August 25, 2016 | Sheet 7 of 82

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AF85	DDR1_DQ[0]	DDR0_DQ[16]
	AF84	DDR1_DQ[1]	DDR0_DQ[17]
	AK85	DDR1_DQ[2]	DDR0_DQ[18]
	AK84	DDR1_DQ[3]	DDR0_DQ[19]
	AF88	DDR1_DQ[4]	DDR0_DQ[20]
	AF87	DDR1_DQ[5]	DDR0_DQ[21]
	AK87	DDR1_DQ[6]	DDR0_DQ[22]
	AK86	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT86	DDR1_DQ[16]	DDR0_DQ[48]
	AU86	DDR1_DQ[17]	DDR0_DQ[49]
	AP85	DDR1_DQ[18]	DDR0_DQ[50]
	AN85	DDR1_DQ[19]	DDR0_DQ[51]
	AN88	DDR1_DQ[20]	DDR0_DQ[52]
	AP88	DDR1_DQ[21]	DDR0_DQ[53]
	AT85	DDR1_DQ[22]	DDR0_DQ[54]
	AU85	DDR1_DQ[23]	DDR0_DQ[55]
	AT81	DDR1_DQ[24]	DDR0_DQ[56]
	AU81	DDR1_DQ[25]	DDR0_DQ[57]
	AP80	DDR1_DQ[26]	DDR0_DQ[58]
	AN80	DDR1_DQ[27]	DDR0_DQ[59]
	AN81	DDR1_DQ[28]	DDR0_DQ[60]
	AP81	DDR1_DQ[29]	DDR0_DQ[61]
	AT80	DDR1_DQ[30]	DDR0_DQ[62]
	AU80	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AR40	DDR1_DQ[36]	DDR1_DQ[20]
	AP40	DDR1_DQ[37]	DDR1_DQ[21]
	AP37	DDR1_DQ[38]	DDR1_DQ[22]
	AR37	DDR1_DQ[39]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]
	AU30	DDR1_DQ[41]	DDR1_DQ[25]
	AT30	DDR1_DQ[42]	DDR1_DQ[26]
	AR33	DDR1_DQ[43]	DDR1_DQ[27]
	AP33	DDR1_DQ[44]	DDR1_DQ[28]
	AR30	DDR1_DQ[45]	DDR1_DQ[29]
	AP30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

TABLE

	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AH65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR61	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

TABLE

Pin	DDR3L	LPDDR3	DDR4
AY45	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_MA[2]	DDR1_CAB[5]	DDR1_MA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

[23] DDR_B_D[0..63]

UC1C

SKL_ULT

DDR_B_D0 AF65
DDR_B_D1 AF64
DDR_B_D2 AK65
DDR_B_D3 AK64
DDR_B_D4 AF66
DDR_B_D5 AF67
DDR_B_D6 AK67
DDR_B_D7 AK66
DDR_B_D8 AF70
DDR_B_D9 AF68
DDR_B_D10 AH71
DDR_B_D11 AH68
DDR_B_D12 AF71
DDR_B_D13 AF69
DDR_B_D14 AH70
DDR_B_D15 AH69
DDR_B_D16 AT66
DDR_B_D17 AU66
DDR_B_D18 AP65
DDR_B_D19 AN65
DDR_B_D20 AN66
DDR_B_D21 AP66
DDR_B_D22 AT65
DDR_B_D23 AU65
DDR_B_D24 AT61
DDR_B_D25 AU61
DDR_B_D26 AP60
DDR_B_D27 AN60
DDR_B_D28 AN61
DDR_B_D29 AP61
DDR_B_D30 AT60
DDR_B_D31 AU60
DDR_B_D32 AU40
DDR_B_D33 AT40
DDR_B_D34 AT37
DDR_B_D35 AU37
DDR_B_D36 AR40
DDR_B_D37 AP40
DDR_B_D38 AP37
DDR_B_D39 AR37
DDR_B_D40 AT33
DDR_B_D41 AU33
DDR_B_D42 AU30
DDR_B_D43 AT30
DDR_B_D44 AR33
DDR_B_D45 AP33
DDR_B_D46 AR30
DDR_B_D47 AP30
DDR_B_D48 AU27
DDR_B_D49 AT27
DDR_B_D50 AT25
DDR_B_D51 AU25
DDR_B_D52 AP27
DDR_B_D53 AN27
DDR_B_D54 AN25
DDR_B_D55 AP25
DDR_B_D56 AT22
DDR_B_D57 AU22
DDR_B_D58 AU21
DDR_B_D59 AT21
DDR_B_D60 AN22
DDR_B_D61 AP22
DDR_B_D62 AP21
DDR_B_D63 AN21

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
DDR1_DQ[34]/DDR1_DQ[18]
DDR1_DQ[35]/DDR1_DQ[19]
DDR1_DQ[36]/DDR1_DQ[20]
DDR1_DQ[37]/DDR1_DQ[21]
DDR1_DQ[38]/DDR1_DQ[22]
DDR1_DQ[39]/DDR1_DQ[23]
DDR1_DQ[40]/DDR1_DQ[24]
DDR1_DQ[41]/DDR1_DQ[25]
DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]

DDR CH - B

SKYLAKE-U_BGA1356
REV = 1
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DDR1_CKN[0] AN45
DDR1_CKN[1] AN46
DDR1_CKP[0] AP45
DDR1_CKP[1] AP46
DDR1_CKE[0] AN56
DDR1_CKE[1] AP55
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53
DDR1_CS#[0] BB42
DDR1_CS#[1] AY42
DDR1_ODT[0] BA42
DDR1_ODT[1] AW42

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46
DDR1_MA[3] BB46
DDR1_MA[4] BA47

DDR1_DQSN[0]/DDR0_DQSN[2] AH66
DDR1_DQSP[0]/DDR0_DQSP[2] AH65
DDR1_DQSN[1]/DDR0_DQSN[3] AG69
DDR1_DQSP[1]/DDR0_DQSP[3] AG70
DDR1_DQSN[2]/DDR0_DQSN[6] AR66
DDR1_DQSP[2]/DDR0_DQSP[6] AR65
DDR1_DQSN[3]/DDR0_DQSN[7] AR61
DDR1_DQSP[3]/DDR0_DQSP[7] AR60
DDR1_DQSN[4]/DDR1_DQSN[2] AT38
DDR1_DQSP[4]/DDR1_DQSP[2] AR38
DDR1_DQSN[5]/DDR1_DQSN[3] AT32
DDR1_DQSP[5]/DDR1_DQSP[3] AR32
DDR1_DQSN[6] AR25
DDR1_DQSP[6] AR27
DDR1_DQSN[7] AR22
DDR1_DQSP[7] AR21

DDR1_ALERT# AN43
DDR1_PAR AP43
DRAM_RESET# AT13
DDR_RCOMP[0] AR18
DDR_RCOMP[1] AT18
DDR_RCOMP[2] AU18

DDR_B_DDRCLK0_1866M# AN45
DDR_B_DDRCLK1_1866M# AN46
DDR_B_DDRCLK0_1866M AP45
DDR_B_DDRCLK1_1866M AP46
DDR_B_CKE0 AN56
DDR_B_CKE1 AP55
DDR_B_CS0# BB42
DDR_B_CS1# AY42
DDR_B_ODT0 BA42
DDR_B_ODT1 AW42
DDR_B_MA5 AY48
DDR_B_MA9 AP50
DDR_B_MA6 BA48
DDR_B_MA8 BB48
DDR_B_MA7 AP48
DDR_B_BG0 AP52
DDR_B_MA12 AN50
DDR_B_MA11 AN48
DDR_B_ACT_N AN53
DDR_B_BG1 AN52
DDR_B_MA13 BA43
DDR_B_MA15 AY43
DDR_B_MA14 AY44
DDR_B_MA16 AW44
DDR_B_BA0 BB44
DDR_B_MA2 AY47
DDR_B_BA1 BA44
DDR_B_MA10 AW46
DDR_B_MA1 AY46
DDR_B_MA0 BA46
DDR_B_MA3 BB46
DDR_B_MA4 BA47
DDR_B_DQS#0 AH66
DDR_B_DQS0 AH65
DDR_B_DQS#1 AG69
DDR_B_DQS1 AG70
DDR_B_DQS#2 AR66
DDR_B_DQS2 AR65
DDR_B_DQS#3 AR61
DDR_B_DQS3 AR60
DDR_B_DQS#4 AT38
DDR_B_DQS4 AR38
DDR_B_DQS#5 AT32
DDR_B_DQS5 AR32
DDR_B_DQS#6 AR25
DDR_B_DQS6 AR27
DDR_B_DQS#7 AR22
DDR_B_DQS7 AR21
DDR_B_ALERT_N AN43
DDR_B_PARITY AP43
DDR4_DRAMRST_N AT13
SM_RCOMP0 AR18
SM_RCOMP1 AT18
SM_RCOMP2 AU18

DDR_B_DDRCLK0_1866M# [23]
DDR_B_DDRCLK1_1866M# [23]
DDR_B_DDRCLK0_1866M [23]
DDR_B_DDRCLK1_1866M [23]
DDR_B_CKE0 [23]
DDR_B_CKE1 [23]
DDR_B_CS0# [23]
DDR_B_CS1# [23]
DDR_B_ODT0 [23]
DDR_B_ODT1 [23]
DDR_B_BG0 [23]
DDR_B_ACT_N [23]
DDR_B_BG1 [23]
DDR_B_BA0 [23]
DDR_B_BA1 [23]
DDR_B_ALERT_N [23]
DDR_B_PARITY [23]

RC36 1 2 121_0402_1%
RC38 1 2 80.6_0402_1%
RC39 1 2 100_0402_1%

[KBL PDG]for DDR4 COMPENSATION
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

DDR_B_MA0
DDR_B_MA1
DDR_B_MA2
DDR_B_MA3
DDR_B_MA4
DDR_B_MA5
DDR_B_MA6
DDR_B_MA7
DDR_B_MA8
DDR_B_MA9
DDR_B_MA10
DDR_B_MA11
DDR_B_MA12
DDR_B_MA13
DDR_B_MA14
DDR_B_MA15
DDR_B_MA16
→ DDR_B_MA[0..16] [23]

DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7
→ DDR_B_DQS#[0..7] [23]

DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7
→ DDR_B_DQS[0..7] [23]

+1.2V
2
RC35
470_0402_5%
1
DDR4_DRAMRST_N
1 2
RC37
0_0402_5%
DDR4_DRAMRST# [22,23]
@

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Issued Date	2015/09/01	Deciphered Date	2016/12/31

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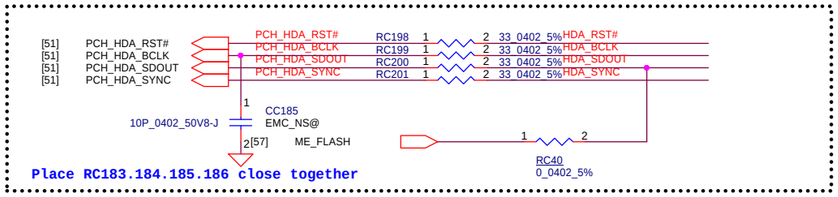
Title: KBL(4/16):DDR4 CH.B

LCFC

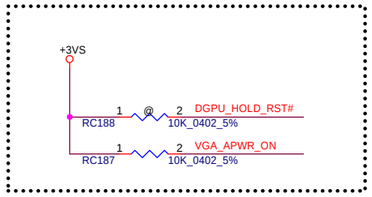
Size: Custom | Document Number: KENOBI | Rev: 2.0

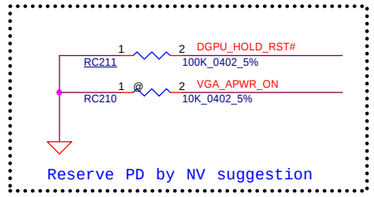
Date: Thursday, August 25, 2016 | Sheet 8 of 82

[KBL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in
the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.



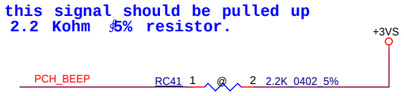
20160408
1.Unstaff RC188 and Staff RC211 with 100K resistor





Note:
SPKR (PC_BEEP) has an integrated weak pull-down resistor (20 K ohm nominal) to disable Top-Block Sway by default.

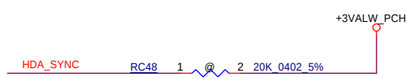
To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 Kohm ±5% resistor.

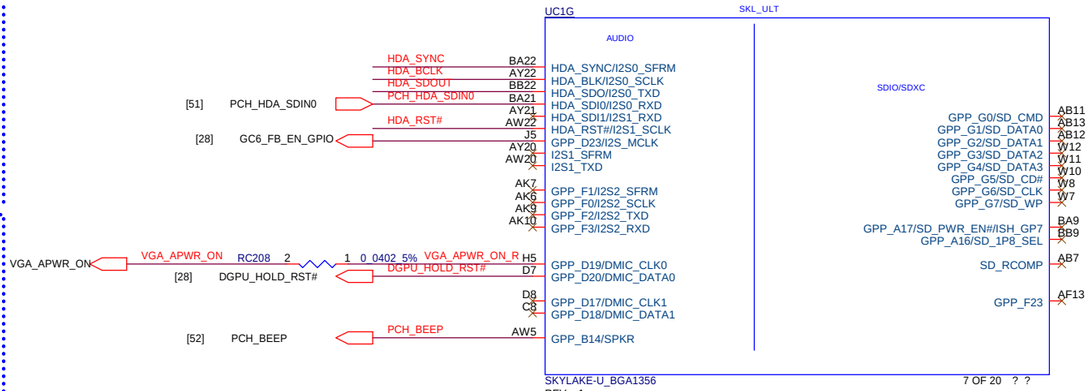


Note:
Internal PD 20K

Note:
HDA_SDO should only be asserted high via external pull-up to 3.3A rail in manufacturing/debug environments ONLY.

Note:
Internal PD 20K





[SKL PDG] internal SD Card

Not support internal SD card. Remove SD_RCOMP

Security Classification	LC Future Center Secret Data		
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Title: KBL(5/16):HDA/SDIO

Size: Custom | Document Number: KENOBI | Rev: 2.0

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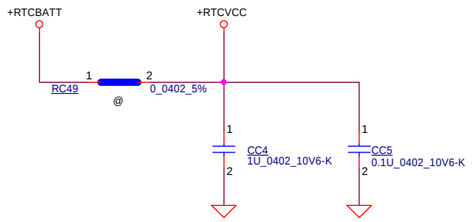
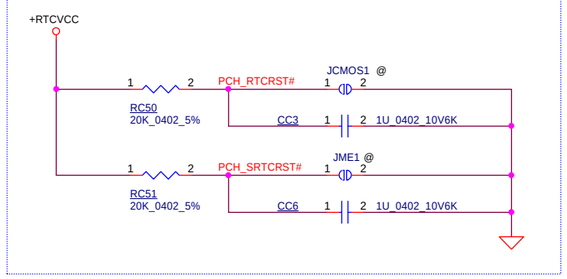
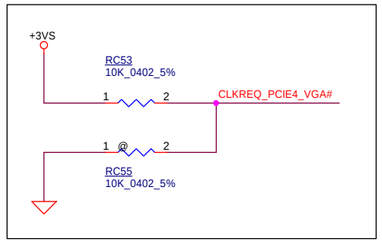
RTC External Circuit

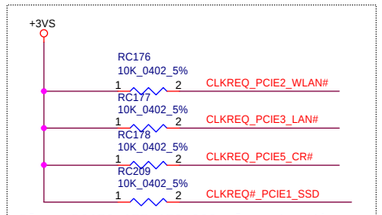
+RTCBATT, +RTCVCC
Trace width = 20mils



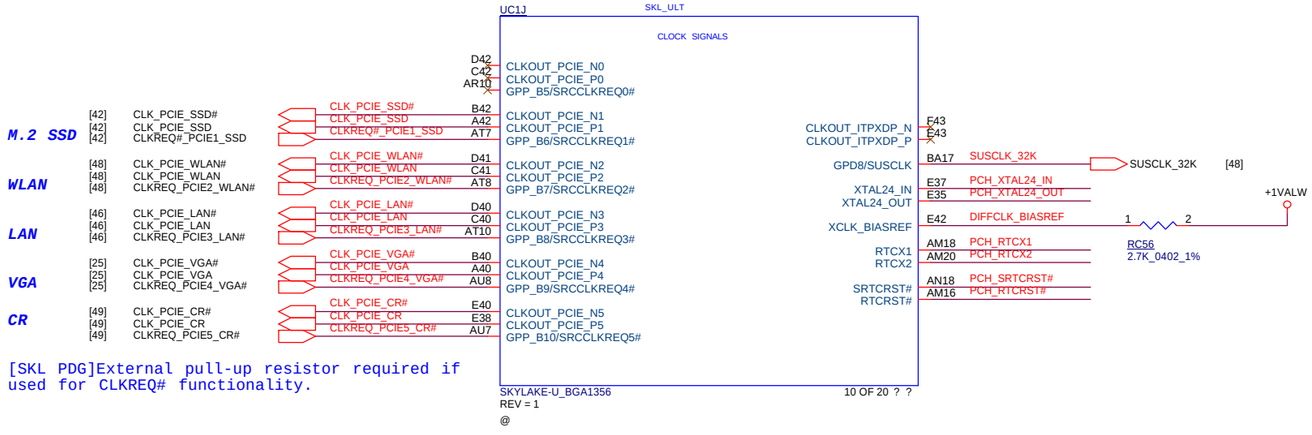
JCMOS, JME Setting, Need Under DDR Door





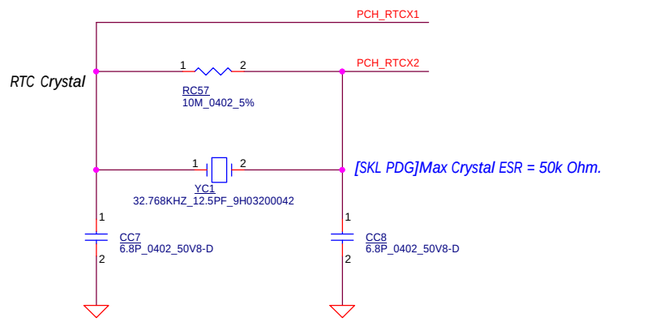


Place RC176,177,178,209 close together



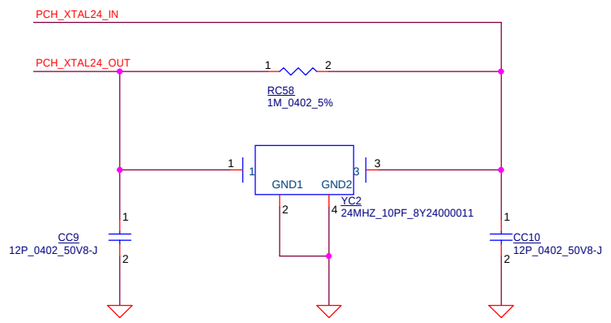
[SKL PDG]External pull-up resistor required if used for CLKREQ# functionality.

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.



20160127
Change CC7/CC8 to 6.8p by vender suggestion

[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	KBL(6/16):CLOCK SIGNALS		
Size	Document Number		Rev
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Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH
SMBALERT# — RC59 1 — 2 — 1K_0402_5%

GPP_C2, Internal PD 20K

JTAG ODT

SPI0_MOSI

+3VALW_PCH
SPI_SI — RC62 1 @ 2 — 8.2K_0402_5%

+3VALW_PCH
SPI_SO — RC65 1 @ 2 — 8.2K_0402_5%

GPP_C5, Internal PD 20K

*L: LPC
H: eSPI

+3VALW_PCH
SML0ALERT# — RC67 1 @ 2 — 1K_0402_5%

close to CPU

UC1E — SKL_ULT

SPI - FLASH
[21,58] SPI_CLK — AV2 SPI0_CLK
[21,58] SPI_SO — AW3 SPI0_MISO
[21,58] SPI_SI — AV3 SPI0_MOSI
[21] SPI_IO2 — AW2 SPI0_IO2
[21] SPI_IO3 — AU4 SPI0_IO3
[21] SPI_CS0#_8MB — AU3 SPI0_CS0#
SPI_CS1#_4MB — AU2 SPI0_CS1#
[58] SPI_CS2#_TPM — AU1 SPI0_CS2#

SPI - TOUCH
M2 GPP_D1/SPI1_CLK
M3 GPP_D2/SPI1_MISO
J4 GPP_D3/SPI1_MOSI
V1 GPP_D21/SPI1_IO2
V2 GPP_D22/SPI1_IO3
M1 GPP_D0/SPI1_CS#

[25] All_GPU_PWRGD — RC107 1 — 2 0_0402_5% — All_GPU_PWRGD_R
[28] GPU_EVENT# — GPU_EVENT#
[57] EC_SCI# — EC_SCI#

C LINK
[48] CL_CLK_WLAN — G3 CL_CLK
[48] CL_DATA_WLAN — G2 CL_DATA
[48] CL_RST_WLAN# — G1 CL_RST#

[57] KBRST# — KBRST# — AW13 GPP_A0/RCIN#

CC183 EMC_NS@ — 10P_0402_50V8-J
[57,58] SERIRQ — SERIRQ — AY11 GPP_A6/SERIRQ

SKYLAKE-U_BGA1356
REV = 1
@

SMBUS, SMLINK
R7 GPP_C0/SMBCLK — PCH_SMB_CLK
R8 GPP_C1/SMBDATA — PCH_SMB_DATA
R10 GPP_C2/SMBALERT# — SMBALERT#
R9 GPP_C3/SML0CLK
W2 GPP_C4/SML0DATA
W1 GPP_C5/SML0ALERT# — SML0ALERT#
W3 GPP_C6/SML1CLK — PCH_SML1CLK
V3 GPP_C7/SML1DATA — PCH_SML1DATA
AM7 GPP_B23/SML1ALERT#/PCHHOT# — SML1ALERT#

LPC
AY13 GPP_A1/LAD0/ESPI_IO0 — LPC_AD0 [57]
BA13 GPP_A2/LAD1/ESPI_IO1 — LPC_AD1 [57]
BB13 GPP_A3/LAD2/ESPI_IO2 — LPC_AD2 [57]
AY12 GPP_A4/LAD3/ESPI_IO3 — LPC_AD3 [57]
BA12 GPP_A5/LFRAME#/ESPI_CS# — LPC_FRAME# [57]
BA11 GPP_A14/SUS_STAT#/ESPI_RESET# — SUS_STAT#

AW9 GPP_A9/CLKOUT_LPC0/ESPI_CLK — PCH_PCI_CLK_R
AY9 GPP_A10/CLKOUT_LPC1
AW11 GPP_A8/CLKRUN# — CLKRUN#

5 OF 20 ? ?

RC63 0_0402_5% — TC7
RC64 22_0402_5% — CLK_PCI_EC [57]
RC66 8.2K_0402_5% — +3VS
CC184 EMC_NS@ — 10P_0402_50V8-J

Close to UC1

DIMM1, DIMM2, Security EEPROM, Click Pad

EC,dGPU,Thermal Sensor

Place RC179,180,181 close together

+3VS
+3VALW_PCH
RC179 1 — 2 10K_0402_5% SERIRQ
RC180 1 — 2 10K_0402_5% EC_SCI#
RC181 1 — 2 10K_0402_5% KBRST#
RC72 1 — 2 4.7K_0402_5% CP_SMB_CLK
RC76 1 — 2 4.7K_0402_5% CP_SMB_DAT
RC212 1 — 2 10K_0402_5% GPU_EVENT#

PCH_SMB_CLK — RC71 1 — 2 2.2K_0402_1%
PCH_SMB_DATA — RC73 1 — 2 2.2K_0402_1%
PCH_SMLICLK — RC74 1 — 2 2.2K_0402_1%
PCH_SML1DATA — RC75 1 — 2 2.2K_0402_1%

Add RC212 PU by NV suggestion

SML1ALERT# — RC77 1 @ 2 1K_0402_5%

SB00000YS00
2N7002KDWH_SOT363-6
QC1A

PCH_SMB_CLK — CP_SMB_CLK [22,23,63]

+3VS

Plan to remove QC1 after SDV

PCH_SMB_DATA — CP_SMB_DAT [22,23,63]

QC1B
2N7002KDWH_SOT363-6
SB00000YS00

SB00000YS00
2N7002KDWH_SOT363-6
QC2A

+3VS
PCH_SML1CLK — EC_SMB_CK3 [28,57,59,62]

PCH_SML1DATA — EC_SMB_DA3 [28,57,59,62]

QC2B
2N7002KDWH_SOT363-6
SB00000YS00

Security Classification	LC Future Center Secret Data		
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Title: KBL(7/16):LPC/SPI/SMBUS/CL

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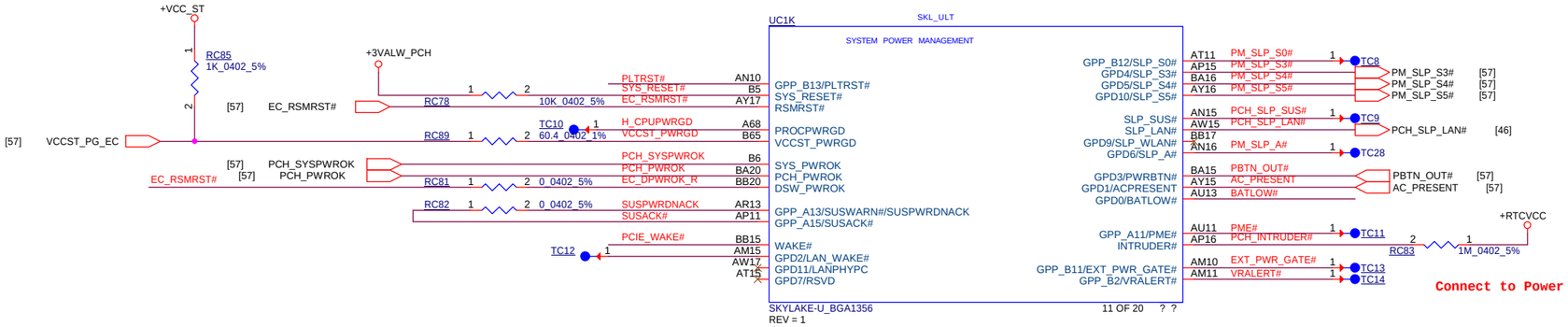
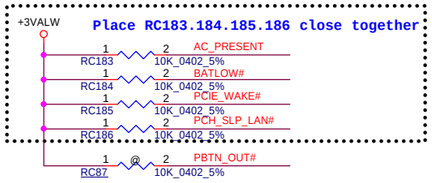
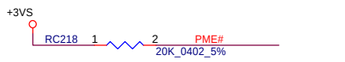
Date: Thursday, August 25, 2016 Sheet 11 of 82

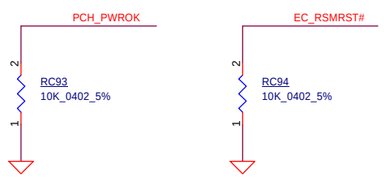


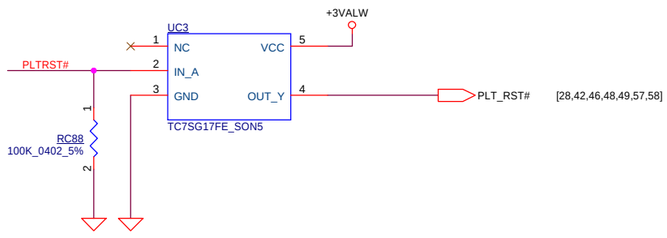
Connect to Power





20160408
1.Add RC218 for PME# by BIOS request





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(8/16):SYSTEM PM

Size	Document Number	Rev
Custom	KENOBI	2.0

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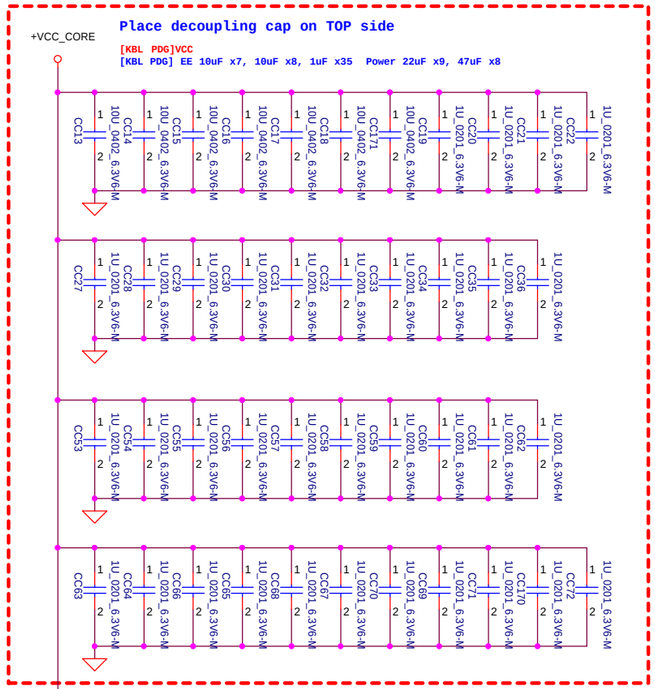

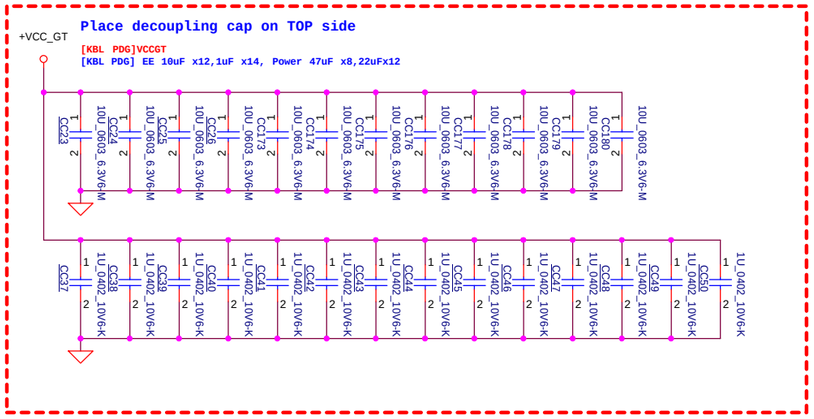

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(9/16):Decoupling**

Size	Document Number	Rev
Custom	KENOBI	2.0

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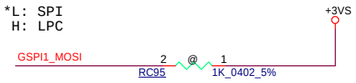
GPP_B22, Internal PD 20K

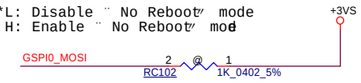
*L: SPI
H: LPC



To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K ±5 % resistor

GPP_B18, Internal PD 20K

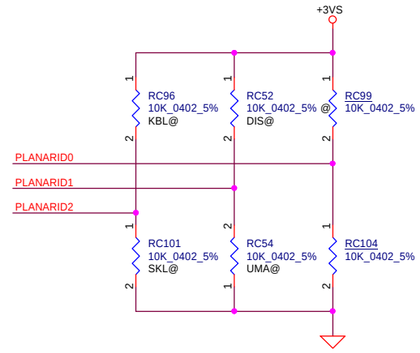
*L: Disable "No Reboot" mode
H: Enable "No Reboot" mode

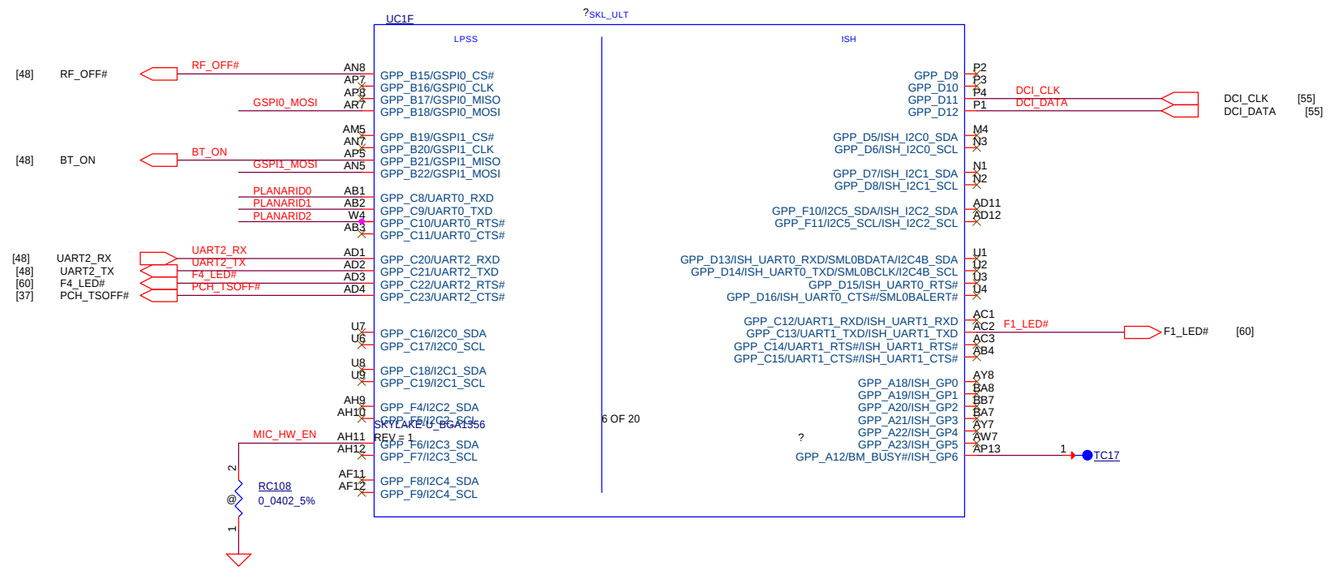


To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K ±5 % resistor

Project ID

	PLANARID0 (GPP_C8)	PLANARID1 (GPP_C9)	PLANARID2 (GPP_C10)	
L	14"	UMA	Skylake	
H	15"	DIS	Kabylake	





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(10/16):GPIO/CPU/MISC

Size	Document Number	Rev
Custom	KENOBI	2.0

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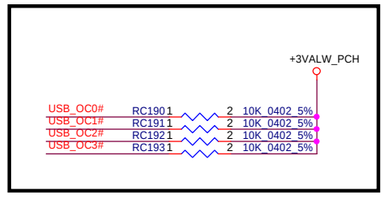
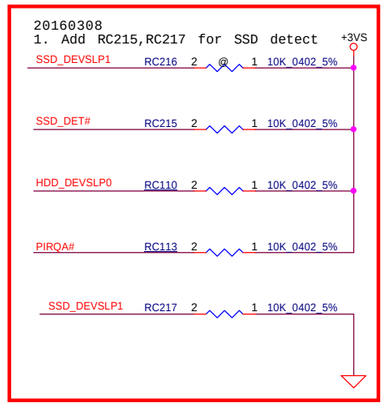
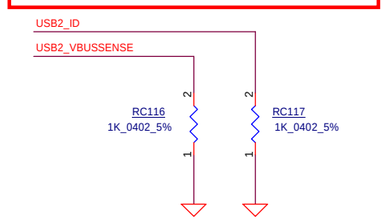
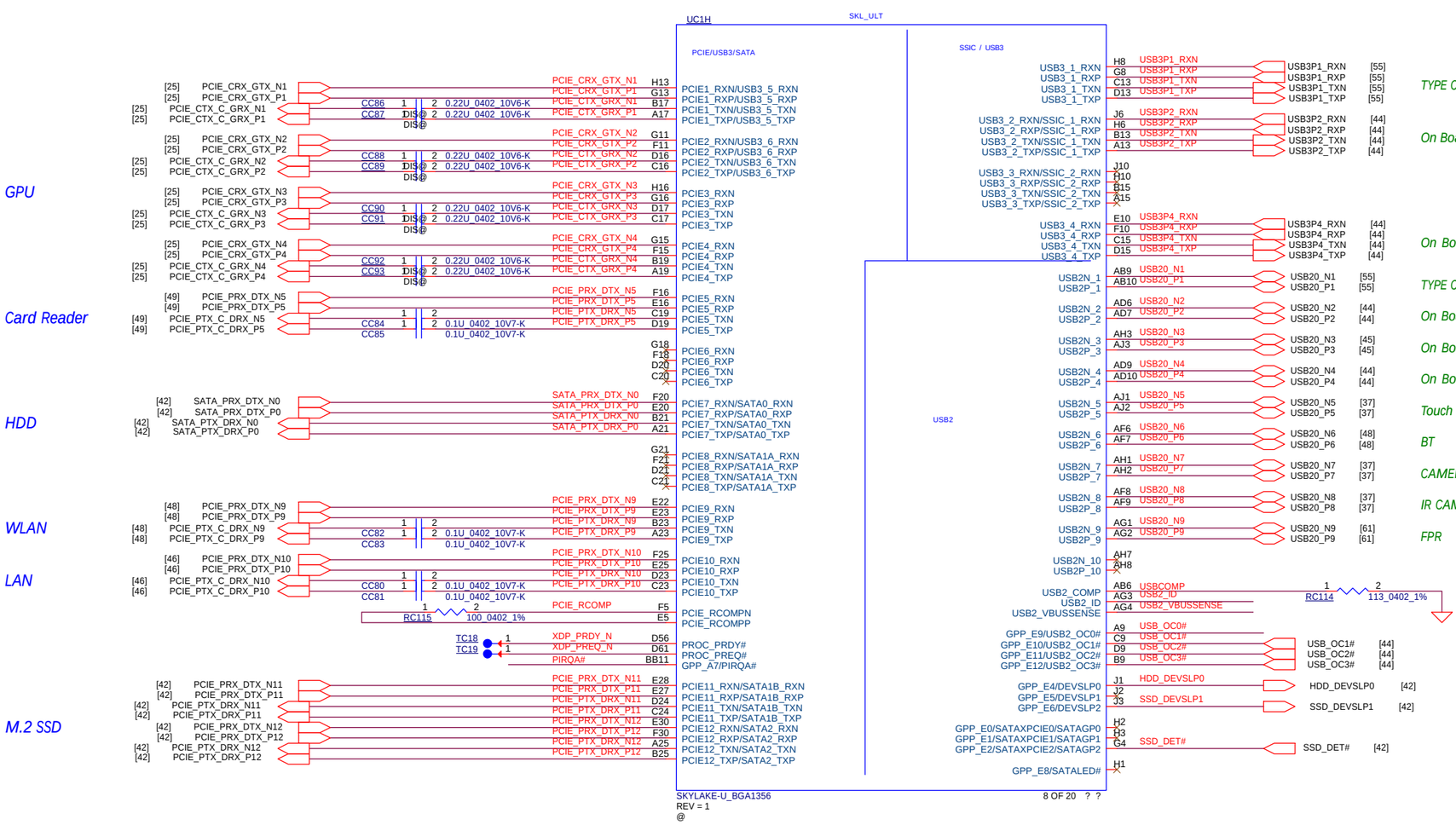
	USB Port Number
USB_OC0#	Reserve
USB_OC1#	Port2
USB_OC2#	Port3
USB_OC3#	Port4









Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: KBL(11/16):PCIE/USB/SATA

Size	Document Number	Rev
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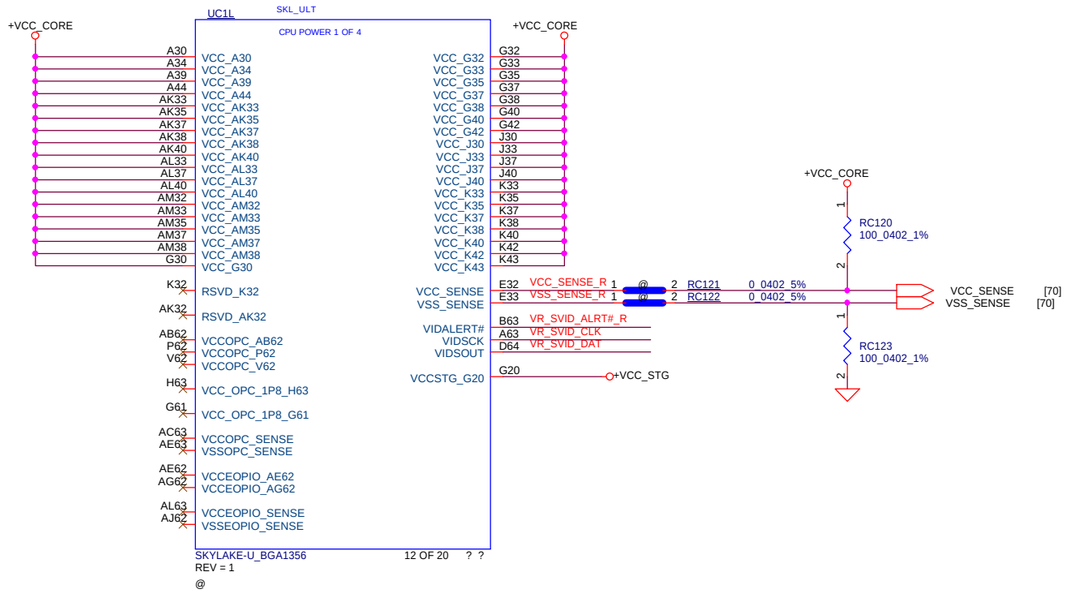
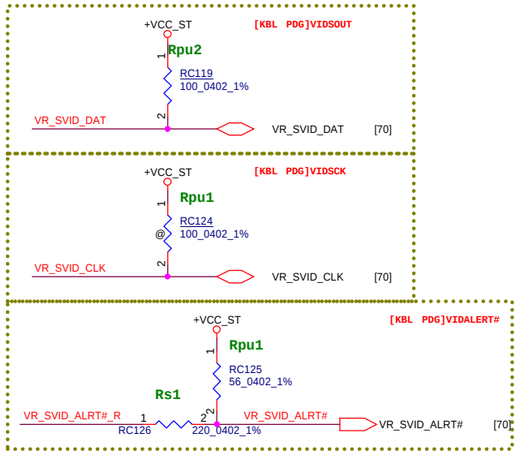
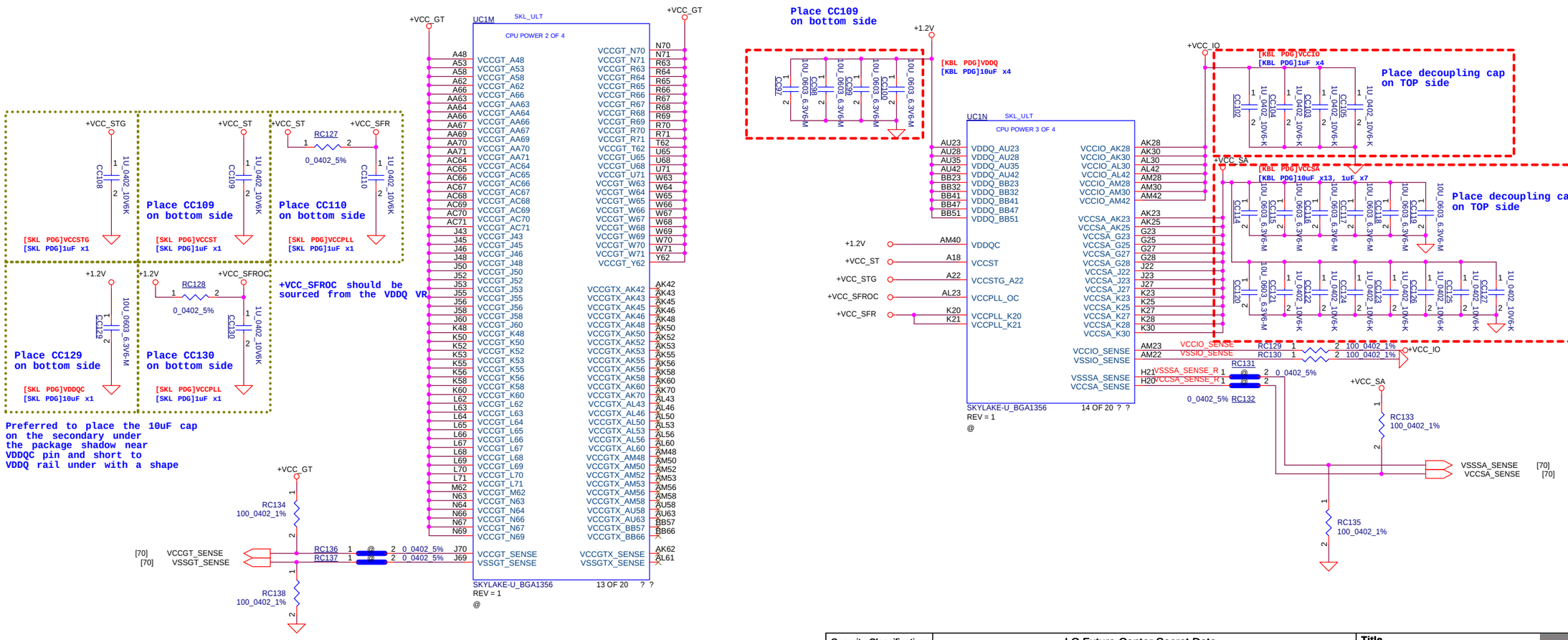
Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	







Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(12/16):POWER**

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Reserve for Sense Resistor

+1.8VALW — RC139 0_0603_5% — +1.8VALW_PCH
+3VALW — RC140 0_0805_5% — +3VALW_PCH
+1VALW — RC141 0_0805_5% — +1VALW_PCH
+1VALW — RC202 0_0805_5% — +VCC_MPHYGT

+VCC_MPHYGT — RC1451 0_0402_5% — +VCC_AMPHYPLL
+1VALW_PCH — RC1461 0_0402_5% — +1VALW_PLL

CC132 please close to N18

+VCC_MPHYGT — CC132 1U_0402_10V6K

[SKL PDG]VccAPLLEBB
[SKL PDG]1uF x1
[SKL PDG]Close N18,
Placement type:Edge<3mm(118mil)

VccMPHYGT(Mod PHY Externally Gated Primary 1.0 V: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.)

CC133 & CC134 please close to N15

+VCC_MPHYGT — CC133 1U_0402_10V6K; CC134 47U_0805_6.3V6-M

[SKL PDG]VccMPHYGT
[SKL PDG]1uF x1
[SKL PDG]Close N15,
Placement type:Edge<3mm(118mil)
[SKL PDG]47uF x1
[SKL PDG]Close N15,
Placement type:Edge<10mm(394mil)

SRAM Primary Well 1.0 V. Dedicated SRAM rail and can have on board power down gate control.

CC136 please close to AF20

+VCC_MPHYGT — @CC136 1U_0402_10V6K

[SKL PDG]VccSRAM
[SKL PDG]1uF x1
[SKL PDG]Close AF20,
Placement type:Edge<10mm(394mil)

Mod PHY Always On Primary 1.0 V: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic

CC137 please close to K17

+1VALW_PCH — CC137 1U_0402_10V6K

[SKL PDG]VccMPHYAON
[SKL PDG]1uF x1
[SKL PDG]Close K17,
Placement type:Edge<3mm(118mil)

Primary Well 1.0 V: For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.

please close to AG15 , Y16 & T16

+3VALW_PCH — CC140 1U_0402_10V6K; CC141 1U_0402_10V6K; CC142 1U_0402_10V6K

CC143 please close to AB19

+1VALW_PCH — CC143 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]1uF x1
[SKL PDG]Close AB19,
Placement type:Edge<10mm(394mil)

+1VALW_PCH
CC181 22U_0603_6.3V6-M; CC131 22U_0603_6.3V6-M
CC182 22U_0603_6.3V6-M; CC135 22U_0603_6.3V6-M

UC1O — SKL_ULT — CPU POWER 4 OF 4

+PCH_CORE	AB19 VCCPRIM_1P0_AB19; AB20 VCCPRIM_1P0_AB20; P18 VCCPRIM_1P0_P18	1100mA
	AF18 VCCPRIM_CORE_AF18; AF19 VCCPRIM_CORE_AF19; V20 VCCPRIM_CORE_V20; V21 VCCPRIM_CORE_V21	500mA
+DCPDSW	AL1 DCPDSW_1P0	22mA
+VCC_MPHYGT	K17 VCCMPHYAON_1P0_K17; L1 VCCMPHYAON_1P0_L1	
	N15 VCCMPHYGT_1P0_N15; N16 VCCMPHYGT_1P0_N16; N17 VCCMPHYGT_1P0_N17; P15 VCCMPHYGT_1P0_P15; P16 VCCMPHYGT_1P0_P16	1500mA
+VCC_AMPHYPLL	K15 VCCAMPHYPLL_1P0_K15; L15 VCCAMPHYPLL_1P0_L15	88mA
+1VALW_PLL	V15 VCCAPLL_1P0	26mA
+VCC_DSW3P3	AB17 VCCPRIM_1P0_AB17; Y18 VCCPRIM_1P0_Y18	
	AD17 VCCDSW_3P3_AD17; AD18 VCCDSW_3P3_AD18; AJ17 VCCDSW_3P3_AJ17	118mA
+VCC_HDA	AJ19 VCCHDA	68mA
+3V_SPI	AJ16 VCCSPI	
+3VALW_PRIM	AF20 VCCSRAM_1P0_AF20; AF21 VCCSRAM_1P0_AF21; T19 VCCSRAM_1P0_T19; T20 VCCSRAM_1P0_T20	565mA
	AJ21 VCCPRIM_3P3_AJ21	75mA
	AK20 VCCPRIM_1P0_AK20	33mA
	N18 VCCAPLLEBB	33mA

SKYLAKE-U_BGA1356
REV = 1
@
15 OF 20 ? ?

+3VALW_PCH	AK15 VCCPGPPA; AG15 VCCPGPPB; Y16 VCCPGPPC; Y15 VCCPGPPD; T16 VCCPGPPE; AF16 VCCPGPPF; AD15 VCCPGPPG	85mA
+1.8VALW_PCH	V19 VCCPRIM_3P3_V19	161mA
+3VALW_PRIM	T1 VCCPRIM_1P0_T1	135mA
+1VALW_PCH	AA1 VCCATS_1P8	
+1.8VALW_PCH	AK17 VCCRTCPRIM_3P3	
+3VALW_RTCPRIM	AK19 VCCRTC_AK19; BB14 VCCRTC_BB14	
+RTCVCC	BB10 DCPRTC	
+DCPRTC	A14 VCCCLK1	
	K19 VCCCLK2	
	L21 VCCCLK3	
	N20 VCCCLK4	
	L19 VCCCLK5	
	A10 VCCCLK6	
	AN11 GPP_B0/CORE_VID0; AN13 GPP_B1/CORE_VID1	T1; T2

Primary Well 3.3 V

+3VALW_PCH — RC147 0_0402_5% — +3VALW_PRIM; CC145 1U_0402_10V6K

[SKL PDG]VCCPRIM
[SKL PDG]1uF x1
[SKL PDG]Close V19,
Placement type:Edge<3mm(118mil)

HD Audio Power 3.3 V, 1.8 V, 1.5 V. For Intel High Definition Audio.

+3VALW_PCH — RC148 0_0402_5% — +VCC_HDA; CC147 1U_0402_10V6K

[SKL PDG]VccHDA
[SKL PDG]1uF x1
[SKL PDG]Close AJ19,
Placement type:Edge<10mm(394mil)

Thermal Sensor Primary Well 1.8 V

+1.8VALW_PCH — CC144 1U_0402_10V6K

[SKL PDG]VccATS
[SKL PDG]1uF x1
[SKL PDG]Close AA1,
Placement type:Edge<10mm(394mil)

Deep Sx Well 1.0 V: This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.

+DCPDSW — CC148 1U_0402_10V6K

[SKL PDG]DcpDSW
[SKL PDG]1uF x1
[SKL PDG]Close AL1,
Placement type:Edge<3mm(118mil)

RTC de-coupling capacitor only. This rail should NOT be driven.

+DCPRTC — CC146 0.1U_0402_10V6-K

[SKL PDG]DcpRTC
[SKL PDG]0.1uF x1
[SKL PDG]Close BB10,
Placement type:Edge<3mm(118mil)

+VCC_AMPHYPLL — @CC149 1U_0402_10V6K

Core Logic Primary Well: This rail scales from 0.85 V to 1.0 V.

+1VALW — RC151 0_0805_5% — +PCH_CORE; CC150 1U_0402_10V6K

[SKL PDG]VccPRIM_Core
[SKL PDG]1uF x1
[SKL PDG]Close AF18,
Placement type:Edge<10mm(394mil)

Deep Sx Well for GPD GPIOs and USB2

+3VALW_PCH — RC152 0_0402_5% — +VCC_DSW3P3

[SKL PDG]VccDSW

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+3VALW_PCH — RC150 0_0402_5% — +3VALW_RTCPRIM; CC151 1U_0402_10V6K; CC152 0.1U_0402_10V6K; CC153 0.1U_0402_10V6K

[SKL PDG]VccRTCPRIM
[SKL PDG]1uF x1,0.1uF x2
[SKL PDG]Close AK17,
Placement type:Edge<3mm(118mil)

RTC Logic Primary Well 3.3 V. This power supplies the RTC internal VRM. It will be off during Deep Sx mode.

+RTCVCC — CC154 1U_0402_10V6K

[SKL PDG]VccRTC
[SKL PDG]1uF x1
[SKL PDG]Close AK19,
Placement type:Edge<3mm(118mil)

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Title: **KBL(13/16):POWER**

Size	Document Number	Rev
A2	**KENOBI**	2.0

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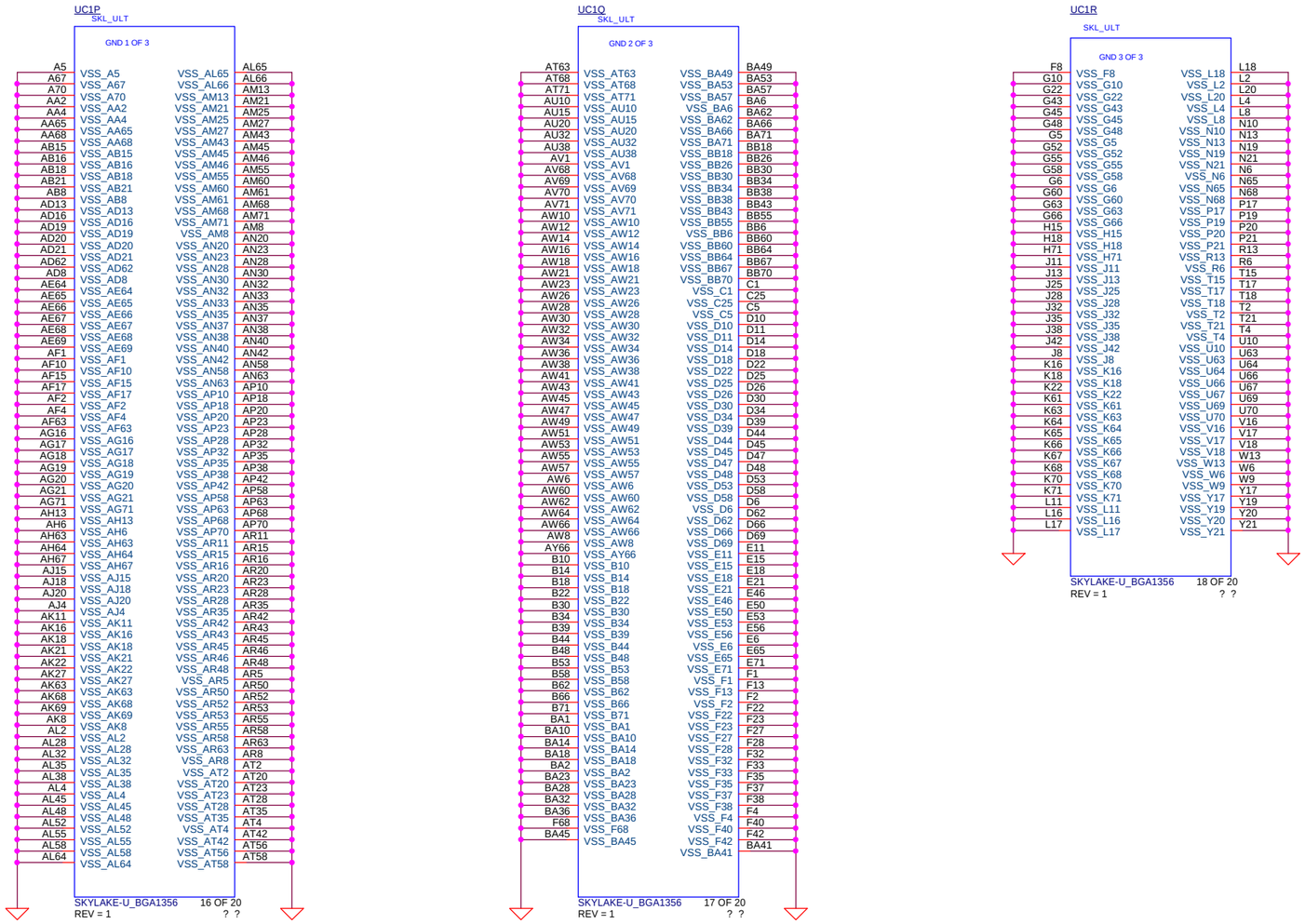

Title: KBL(14/16):GND

Size	Document Number	Rev
Custom	KENOBI	2.0

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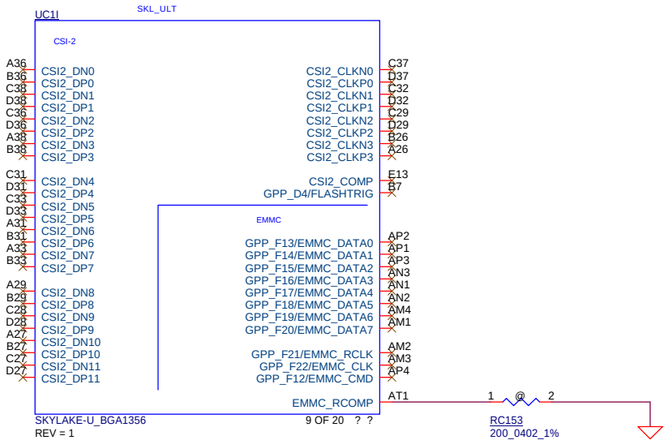

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KBL(15/16):CSI-2/EMMC**

Size	Document Number	Rev
Custom	KENOBI	2.0

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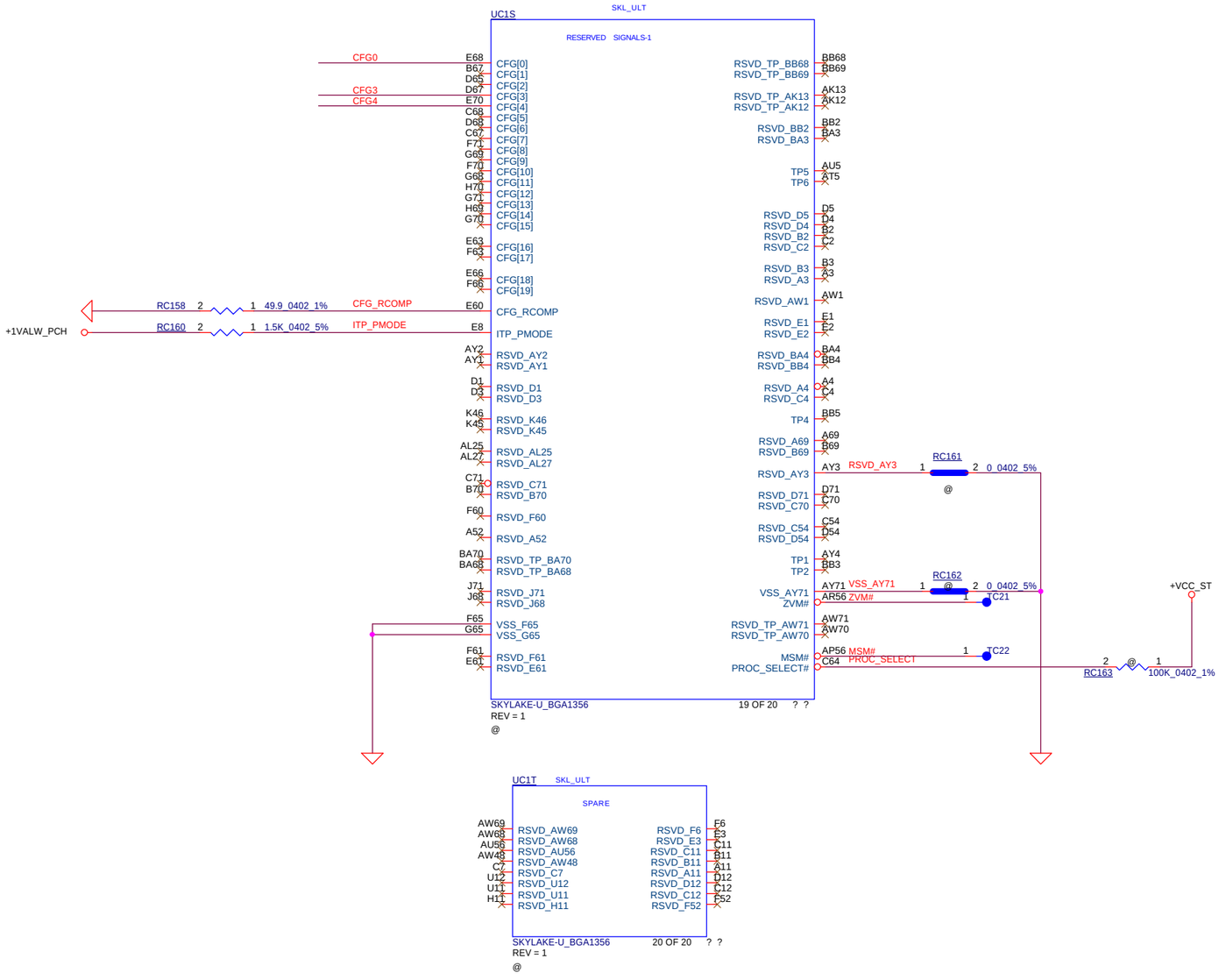

[SKL EDS]

CFG0

+VCC_IO

CFG0 — RC154 2 @ 1 1K_0402_5%

RC155 2 @ 1 1K_0402_1%

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG4

+VCC_IO

CFG4 — RC156 2 @ 1 1K_0402_5%

RC157 2 1 1K_0402_1%

*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

CFG3

CFG3 — RC159 1 @ 2 1K_0402_5%

CFG3 require >= 0.5"
CPU Debug Consent Strap

TABLE

CFG0 : Stall Reset Sequence
after PCU PLL Lock until de-asserted
1 : No Stall
0 : Stall

CFG4 : eDP Enable
1 : Disabled
0 : Enabled

Title: KBL(16/16):CFG/RESERVED

Size	Document Number	Rev
Custom	KENOBI	2.0

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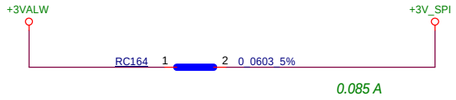
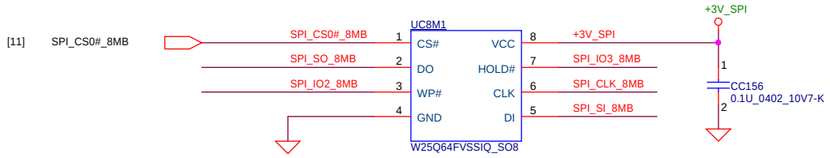
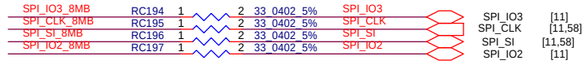


4MB(32Mb) Reserve

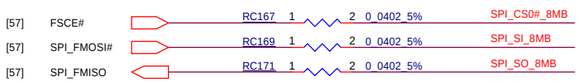


Place RC194,195,196,197 close together



Near SPI ROM

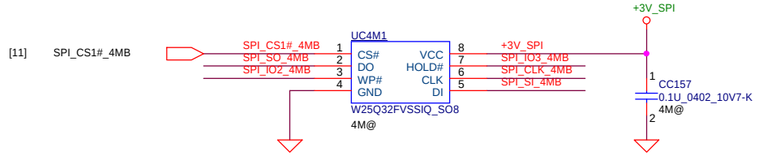
Mirror Code



Close to SPI ROM (UC8M1).

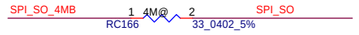
8MB(64Mb)

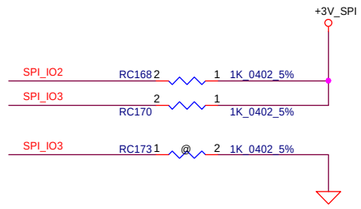
[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM



Place RC203,204,205,206 close together

Near SPI ROM





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **SPI ROM**

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD1 10U_0603_6.3V6-M
CD2 10U_0603_6.3V6-M
CD3 10U_0603_6.3V6-M
CD4 10U_0603_6.3V6-M
CD5 10U_0603_6.3V6-M
CD6 10U_0603_6.3V6-M
CD7 10U_0603_6.3V6-M
CD8 10U_0603_6.3V6-M

+1.2V

CD14 1U_0402_6.3V6-K
CD15 1U_0402_6.3V6-K
CD16 1U_0402_6.3V6-K
CD17 1U_0402_6.3V6-K
CD18 1U_0402_6.3V6-K
CD19 1U_0402_6.3V6-K
CD20 1U_0402_6.3V6-K
CD21 1U_0402_6.3V6-K
CD26 @ 330U_D2_2VM_R9M

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+2.5V

CD9 10U_0603_6.3V6-M
CD10 10U_0603_6.3V6-M
CD11 1U_0402_6.3V6-K
CD12 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+0.6VS

CD22 10U_0603_6.3V6-M
CD23 10U_0603_6.3V6-M
CD24 1U_0402_6.3V6-K
CD63 1U_0402_6.3V6-K
CD64 1U_0402_6.3V6-K
CD65 1U_0402_6.3V6-K

DDR_A_D[0..63] [7]
DDR_A_MA[0..16] [7]
DDR_A_DQS#[0..7] [7]
DDR_A_DQS[0..7] [7]

JDIMM1A ME@ — FOX_AS0A826-H4RB-7H

DDR_A_D5	1	VSS_1	VSS_2	2	DDR_A_D0
	3	DQ5	DQ4	4	
DDR_A_D1	5	VSS_3	VSS_4	6	DDR_A_D4
	7	DQ1	DQ0	8	
DDR_A_DQS#0	9	VSS_5	VSS_6	10	
DDR_A_DQS0	11	DQS0_C	DM0_n/DBI0_n	12	
DDR_A_D2	13	DQS0_t	VSS_7	14	DDR_A_D6
	15	VSS_8	DQ6	16	
DDR_A_D7	17	DQ7	VSS_9	18	DDR_A_D3
	19	VSS_10	DQ2	20	
DDR_A_D9	21	DQ3	VSS_11	22	DDR_A_D8
	23	VSS_12	DQ12	24	
DDR_A_D12	25	DQ13	VSS_13	26	DDR_A_D13
	27	VSS_14	DQ8	28	
	29	DQ9	VSS_15	30	DDR_A_DQS#1
	31	VSS_16	DQS1_c	32	DDR_A_DQS1
DDR_A_D10	33	DM1_n/DBI1_n	DQS1_t	34	
	35	VSS_17	VSS_18	36	DDR_A_D11
DDR_A_D15	37	DQ15	DQ14	38	
	39	VSS_19	VSS_20	40	DDR_A_D14
DDR_A_D16	41	DQ10	DQ11	42	
	43	VSS_21	VSS_22	44	DDR_A_D17
DDR_A_D20	45	DQ21	DQ20	46	
	47	VSS_23	VSS_24	48	DDR_A_D21
DDR_A_DQS#2	49	DQ17	DQ16	50	
DDR_A_DQS2	51	VSS_25	VSS_26	52	
	53	DQS2_c	DM2_n/DBI2_n	54	
DDR_A_D23	55	DQS2_t	VSS_27	56	DDR_A_D22
	57	VSS_28	DQ22	58	
DDR_A_D18	59	DQ23	VSS_29	60	DDR_A_D19
	61	VSS_30	DQ18	62	
DDR_A_D25	63	DQ19	VSS_31	64	DDR_A_D29
	65	VSS_32	DQ28	66	
DDR_A_D24	67	DQ29	VSS_33	68	DDR_A_D28
	69	VSS_34	DQ24	70	
	71	DQ25	VSS_35	72	DDR_A_DQS#3
	73	VSS_36	DQS3_c	74	DDR_A_DQS3
	75	DM3_n/DBI3_n	DQS3_t	76	
DDR_A_D30	77	VSS_37	VSS_38	78	DDR_A_D31
	79	DQ30	DQ31	80	
DDR_A_D26	81	VSS_39	VSS_40	82	DDR_A_D27
	83	DQ26	DQ27	84	
	85	VSS_41	VSS_42	86	
	87	CB5/NC	CB4/NC	88	
	89	VSS_43	VSS_44	90	
	91	CB1/NC	CB0/NC	92	
	93	VSS_45	VSS_46	94	
DDR_A_DQS#8	95	DQS8_c	DM8_n/DBI8_n/NC	96	
DDR_A_DQS8	97	DQS8_t	VSS_47	98	
	99	VSS_48	CB6/NC	100	
	101	CB2/NC	VSS_49	102	
	103	VSS_50	CB7/NC	104	
	105	CB3/NC	VSS_51	106	
	107	VSS_52	RESET_n	108	DDR4_DRAMRST# [8,23]
DDR_A_CKE0	109	CKE0	CKE1	110	DDR_A_CKE1 [7]
DDR_A_BG1	111	VDD_1	VDD_2	112	
DDR_A_BG0	113	BG1	ACT_n	114	DDR_A_ACT_N
	115	BG0	ALERT_n	116	DDR_A_ALERT_N
DDR_A_MA12	117	VDD_3	VDD_4	118	
DDR_A_MA9	119	A12	A11	120	DDR_A_MA11
	121	A9	A7	122	DDR_A_MA7
DDR_A_MA8	123	VDD_5	VDD_6	124	
DDR_A_MA6	125	A8	A5	126	DDR_A_MA5
	127	A6	A4	128	DDR_A_MA4
	129	VDD_7	VDD_8	130	

JDIMM1B ME@ — FOX_AS0A826-H4RB-7H

DDR_A_MA3	131	A3	A2	132	DDR_A_MA2
DDR_A_MA1	133	A1	EVENT_n/NF	134	EVENT_n_1
	135	VDD_9	VDD_10	136	
DDR_A_DDRCLK0_1866M	137	CK0_t	CK1_t/NF	138	DDR_A_DDRCLK1_1866M
DDR_A_DDRCLK0_1866M#	139	CK0_c	CK1_c/NF	140	DDR_A_DDRCLK1_1866M#
	141	VDD_11	VDD_12	142	
DDR_A_PARITY	143	Parity	A0	144	DDR_A_MA0
	145	BA1	A10/AP	146	
DDR_A_BA1	147	VDD_13	VDD_14	148	DDR_A_MA10
DDR_A_CS0#	149	CS0_n	BA0	150	DDR_A_BA0
DDR_A_MA14	151	A14/WE_n	A16/RAS_n	152	DDR_A_MA16
	153	VDD_15	VDD_16	154	
DDR_A_ODT0	155	ODT0	A15/CAS_n	156	DDR_A_MA15
DDR_A_CS1#	157	CS1_n	A13	158	DDR_A_MA13
	159	VDD_17	VDD_18	160	
DDR_A_ODT1	161	ODT1	C0/CS2_n/NC	162	
	163	VDD_19	VREFCA	164	M_VREF_CA_DIMMA
	165	C1/CS3_n/NC	SA2	166	SA2_CHA_P
DDR_A_D37	167	VSS_53	VSS_54	168	
	169	DQ37	DQ36	170	DDR_A_D33
DDR_A_D32	171	VSS_55	VSS_56	172	DDR_A_D36
	173	DQ33	DQ32	174	
DDR_A_DQS#4	175	VSS_57	VSS_58	176	
DDR_A_DQS4	177	DQS4_c	DM4_n/DBI4_n	178	
DDR_A_D38	179	DQS4_t	VSS_59	180	
	181	VSS_60	DQ39	182	DDR_A_D35
DDR_A_D39	183	DQ38	VSS_61	184	
	185	VSS_62	DQ35	186	DDR_A_D34
DDR_A_D40	187	DQ34	VSS_63	188	
	189	VSS_64	DQ45	190	DDR_A_D41
DDR_A_D44	191	DQ44	VSS_65	192	
	193	VSS_66	DQ41	194	DDR_A_D45
	195	DQ40	VSS_67	196	
	197	VSS_68	DQS5_c	198	DDR_A_DQS#5
DDR_A_D43	199	DM5_n/DBI5_n	DQS5_t	200	DDR_A_DQS5
	201	VSS_69	VSS_70	202	
DDR_A_D46	203	DQ46	DQ47	204	DDR_A_D42
	205	VSS_71	VSS_72	206	
DDR_A_D49	207	DQ42	DQ43	208	DDR_A_D47
	209	VSS_73	VSS_74	210	
DDR_A_D52	211	DQ52	DQ53	212	DDR_A_D48
	213	VSS_75	VSS_76	214	
	215	DQ49	DQ48	216	DDR_A_D53
DDR_A_DQS#6	217	VSS_77	VSS_78	218	
DDR_A_DQS6	219	DQS6_c	DM6_n/DBI6_n	220	
DDR_A_D50	221	DQS6_t	VSS_79	222	
	223	VSS_80	DQ54	224	DDR_A_D54
DDR_A_D55	225	DQS5	VSS_81	226	
	227	VSS_82	DQ50	228	DDR_A_D51
DDR_A_D56	229	DQ51	VSS_83	230	
	231	VSS_84	DQ60	232	DDR_A_D57
DDR_A_D60	233	DQ61	VSS_85	234	
	235	VSS_86	DQ57	236	DDR_A_D61
	237	DQ56	VSS_87	238	
	239	VSS_88	DQS7_c	240	DDR_A_DQS#7
DDR_A_D59	241	DM7_n/DBI7_n	DQS7_t	242	DDR_A_DQS7
	243	VSS_89	VSS_90	244	
DDR_A_D58	245	DQ62	DQ63	246	DDR_A_D63
	247	VSS_91	VSS_92	248	
CP_SMB_CLK	249	DQ58	DQ59	250	DDR_A_D62
	251	VSS_93	VSS_94	252	
	253	SCL	SDA	254	CP_SMB_DAT
	255	VDDSPD	SA0	256	SA0_CHA_P
	257	VPP_1	VTT	258	
	259	VPP_2	SA1	260	SA1_CHA_P
	261	GND_1	GND_2	262	

RD5 240_0402_1%

DDR_A_DDRCLK0_1866M [7]
DDR_A_DDRCLK0_1866M# [7]
DDR_A_PARITY [7]
DDR_A_BA1 [7]
DDR_A_CS0# [7]
DDR_A_ODT0 [7]
DDR_A_CS1# [7]
DDR_A_ODT1 [7]

DDR_A_DDRCLK1_1866M [7]
DDR_A_DDRCLK1_1866M# [7]
DDR_A_BA0 [7]

RD6 10K_0402_5% @ SA0_CHA_P — RD9 0_0402_5%
RD7 10K_0402_5% @ SA1_CHA_P — RD10 0_0402_5%
RD8 10K_0402_5% @ SA2_CHA_P — RD11 0_0402_5%

SPD Address = 0H

RD12 0_0402_5% @ — [11,23,63] CP_SMB_CLK / CP_SMB_DAT [11,23,63]

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

CD29 0.1U_0402_10V7-K
CD30 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

CD27 2.2U_0402_6.3V6-M
CD28 0.1U_0402_10V7-K

RF

RD1 1K_0402_1%
RD2 2_0402_1%
RD3 1K_0402_1%
RD4 24.9_0402_1%
CD13 0.022U_0402_25V7-K
CD25 0.1U_0402_16V7-K @

[7] DDR4_VREF_CA_CPU_A — M_VREF_CA_DIMMA

RD13 240_0402_1%
RD14 240_0402_1%

DDR_A_DQS#8
DDR_A_DQS8

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Place 10uF/1uF decoupling cap, 4 near each side of the DIMM connector close to VDD pins.
330uF placeholder

[KBL PDG]VDDQ
[KBL PDG] EE 10uF x16, 1uF x16. 330uF x1

+1.2V

CD34 10U_0603_6.3V6-M
CD35 10U_0603_6.3V6-M
CD36 10U_0603_6.3V6-M
CD37 10U_0603_6.3V6-M
CD38 10U_0603_6.3V6-M
CD39 10U_0603_6.3V6-M
CD40 10U_0603_6.3V6-M
CD41 10U_0603_6.3V6-M

CD49 1U_0402_6.3V6-K
CD50 1U_0402_6.3V6-K
CD51 1U_0402_6.3V6-K
CD52 1U_0402_6.3V6-K
CD53 1U_0402_6.3V6-K
CD54 1U_0402_6.3V6-K
CD55 1U_0402_6.3V6-K
CD56 1U_0402_6.3V6-K
CD57 330U_D2_2VM_R9M

Place decoupling cap on DRAM side.

[KBL PDG]VPP
[KBL PDG] EE 10uF x2, 1uF x2.

+0.6VS

CD32 10U_0603_6.3V6-M
CD33 10U_0603_6.3V6-M
CD42 1U_0402_6.3V6-K

Place decoupling on the VTT plane close to SODIMM

[KBL PDG]VTT
[KBL PDG] EE 10uF x2, 1uF x4.

+2.5V

CD45 10U_0603_6.3V6-M
CD46 10U_0603_6.3V6-M
CD47 1U_0402_6.3V6-K
CD48 1U_0402_6.3V6-K
CD68 1U_0402_6.3V6-K
CD66 1U_0402_6.3V6-K
CD67 1U_0402_6.3V6-K

Layout Node:
Place Close DIMMs

DDR_B_D[0..63] [8]
DDR_B_MA[0..16] [8]
DDR_B_DQS#[0..7] [8]
DDR_B_DQS[0..7] [8]

JDIMM2A ME@

DDR_B_D13	3	VSS_1	VSS_2	4	DDR_B_D8
DDR_B_D12	5	DQ5	DQ4	6	DDR_B_D9
	7	VSS_3	VSS_4	8	
DDR_B_DQS#1	9	DQ1	DQ0	10	
DDR_B_DQS1	11	VSS_5	VSS_6	12	
	13	DQS0_C	DM0_n/DBIO_n	14	
DDR_B_D10	15	DQS0_t	VSS_7	16	DDR_B_D15
	17	VSS_8	DQ6	18	
DDR_B_D14	19	DQ7	VSS_9	20	DDR_B_D11
DDR_B_D4	21	VSS_10	DQ2	22	
	23	DQ3	VSS_11	24	DDR_B_D1
DDR_B_D0	25	VSS_12	DQ12	26	
	27	DQ13	VSS_13	28	DDR_B_D5
	29	VSS_14	DQ8	30	
	31	DQ9	VSS_15	32	DDR_B_DQS#0
	33	VSS_16	DQS1_c	34	DDR_B_DQS0
	35	DM1_n/DBI1_n	DQS1_t	36	
DDR_B_D6	37	VSS_17	VSS_18	38	DDR_B_D3
DDR_B_D2	39	DQ15	DQ14	40	
	41	VSS_19	VSS_20	42	DDR_B_D7
DDR_B_D21	43	DQ10	DQ11	44	
	45	VSS_21	VSS_22	46	DDR_B_D20
DDR_B_D16	47	DQ21	DQ20	48	
	49	VSS_23	VSS_24	50	DDR_B_D17
DDR_B_DQS#2	51	DQ17	DQ16	52	
DDR_B_DQS2	53	VSS_25	VSS_26	54	
	55	DQS2_c	DM2_n/DBI2_n	56	
DDR_B_D18	57	DQS2_t	VSS_27	58	DDR_B_D23
	59	VSS_28	DQ22	60	
DDR_B_D22	61	DQ23	VSS_29	62	DDR_B_D19
	63	VSS_30	DQ18	64	
DDR_B_D29	65	DQ19	VSS_31	66	DDR_B_D28
	67	VSS_32	DQ28	68	
DDR_B_D25	69	DQ29	VSS_33	70	DDR_B_D24
	71	VSS_34	DQ24	72	
	73	DQ25	VSS_35	74	DDR_B_DQS#3
	75	VSS_36	DQS3_c	76	DDR_B_DQS3
	77	DM3_n/DBI3_n	DQS3_t	78	
DDR_B_D30	79	VSS_37	VSS_38	80	DDR_B_D31
DDR_B_D26	81	DQ30	DQ31	82	
	83	VSS_39	VSS_40	84	DDR_B_D27
	85	DQ26	DQ27	86	
	87	VSS_41	VSS_42	88	
	89	CB5/NC	CB4/NC	90	
	91	VSS_43	VSS_44	92	
	93	CB1/NC	CB0/NC	94	
DDR_B_DQS#8	95	VSS_45	VSS_46	96	
DDR_B_DQS8	97	DQS8_c	DBI8_n	98	
	99	DQS8_t	VSS_47	100	
	101	VSS_48	CB6/NC	102	
	103	CB2/NC	VSS_49	104	
	105	VSS_50	CB7/NC	106	
	107	CB3/NC	VSS_51	108	
DDR_B_CKE0	109	VSS_52	RESET_n	110	DDR4_DRAMRST# [8,22]
	111	CKE0	CKE1	112	DDR_B_CKE1 [8]
DDR_B_BG1	113	VDD_1	VDD_2	114	
DDR_B_BG0	115	BG1	ACT_n	116	DDR_B_ACT_N [8]
	117	BG0	ALERT_n	118	DDR_B_ALERT_N [8]
DDR_B_MA12	119	VDD_3	VDD_4	120	DDR_B_MA11
DDR_B_MA9	121	A12	A11	122	DDR_B_MA7
	123	A9	A7	124	
DDR_B_MA8	125	VDD_5	VDD_6	126	DDR_B_MA5
DDR_B_MA6	127	A8	A5	128	DDR_B_MA4
	129	A6	A4	130	
		VDD_7	VDD_8		

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SP071407011

[8] DDR_B_CKE0
[8] DDR_B_BG1
[8] DDR_B_BG0

SPD Address = 2H

RD20 10K_0402_5% @ SA0_CHB_P
RD21 10K_0402_5% SA1_CHB_P
RD22 10K_0402_5% @ SA2_CHB_P
RD23 0_0402_5%
RD24 0_0402_5% @
RD25 0_0402_5%

JDIMM2B ME@

DDR_B_MA3	131	A3	A2	132	DDR_B_MA2
DDR_B_MA1	133	A1	EVENT_n	134	EVENT_n_2
	135	VDD_9	VDD_10	136	
DDR_B_DDRCLK0_1866M	137	CK0_t	CK1_t	138	DDR_B_DDRCLK1_1866M
DDR_B_DDRCLK0_1866M#	139	CK0_c	CK1_c	140	DDR_B_DDRCLK1_1866M#
	141	VDD_11	VDD_12	142	
DDR_B_PARITY	143	Parity	A0	144	DDR_B_MA0
	145		A10/AP	146	DDR_B_MA10
DDR_B_BA1	147	BA1	VDD_14	148	
DDR_B_CS0#	149	VDD_13	BA0	150	DDR_B_BA0
DDR_B_MA14	151	CS0_n	RAS_n/A16	152	DDR_B_MA16
	153	WE_n/A14	VDD_16	154	
DDR_B_ODT0	155	VDD_15	CAS_n/A15	156	DDR_B_MA15
DDR_B_CS1#	157	ODT0	A13	158	DDR_B_MA13
	159	CS1_n		160	
DDR_B_ODT1	161	VDD_17	VDD_18	162	
	163	ODT1	C0/CS2_n/NC	164	M_VREF_CA_DIMMB
	165	VDD_19	VREFCA	166	SA2_CHB_P
	167	C1/CS3_n/NC	RFU	168	
DDR_B_D37	169	VSS_53	VSS_54	170	DDR_B_D36
DDR_B_D33	171	DQ37	DQ36	172	DDR_B_D32
	173	VSS_55	VSS_56	174	
DDR_B_DQS#4	175	DQ33	DQ32	176	
DDR_B_DQS4	177	VSS_57	VSS_58	178	
DDR_B_D34	179	DQS4_c	DM4_n/DBI4_n	180	
	181	DQS4_t	VSS_59	182	DDR_B_D35
DDR_B_D38	183	VSS_60	DQ39	184	
	185	DQ38	VSS_61	186	DDR_B_D39
	187	VSS_62	DQ35	188	
DDR_B_D41	189	DQ34	VSS_63	190	DDR_B_D45
	191	VSS_64	DQ45	192	
DDR_B_D40	193	DQ44	VSS_65	194	DDR_B_D44
	195	VSS_66	DQ41	196	
	197	DQ40	VSS_67	198	DDR_B_DQS#5
	199	VSS_68	DQS5_c	200	DDR_B_DQS5
	201	DM5_n/DBI5_n	DQS5_t	202	
DDR_B_D43	203	VSS_69	VSS_70	204	DDR_B_D42
DDR_B_D47	205	DQ46	DQ47	206	
	207	VSS_71	VSS_72	208	DDR_B_D46
DDR_B_D53	209	DQ42	DQ43	210	
	211	VSS_73	VSS_74	212	DDR_B_D52
DDR_B_D48	213	DQ52	DQ53	214	
	215	VSS_75	VSS_76	216	DDR_B_D49
	217	DQ49	DQ48	218	
DDR_B_DQS#6	219	VSS_77	VSS_78	220	
DDR_B_DQS6	221	DQS6_c	DM6_n/DBI6_n	222	
	223	DQS6_t	VSS_79	224	DDR_B_D51
DDR_B_D50	225	VSS_80	DQ54	226	
	227	DQ55	VSS_81	228	DDR_B_D54
DDR_B_D55	229	VSS_82	DQ50	230	
	231	DQ51	VSS_83	232	DDR_B_D56
DDR_B_D60	233	VSS_84	DQ60	234	
	235	DQ61	VSS_85	236	DDR_B_D57
DDR_B_D61	237	VSS_86	DQ57	238	
	239	DQ56	VSS_87	240	DDR_B_DQS#7
	241	VSS_88	DQS7_c	242	DDR_B_DQS7
	243	DM7_n/DBI7_n	DQS7_t	244	
DDR_B_D59	245	VSS_89	VSS_90	246	DDR_B_D62
DDR_B_D58	247	DQ62	DQ63	248	
	249	VSS_91	VSS_92	250	DDR_B_D63
	251	DQ58	DQ59	252	
	253	VSS_93	VSS_94	254	
CP_SMB_CLK	255	SCL	SDA	256	CP_SMB_DAT
VDDSPD_2	257	VDDSPD	SA0	258	SA0_CHB_P
	259	VPP_1	Vtt	260	SA1_CHB_P
		VPP_2	SA1		
	261	GND_1	GND_2	262	

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RD19 240_0402_1%
RD26 0_0402_5%

[11,22,63] CP_SMB_CLK
CP_SMB_DAT [11,22,63]

[KBL PDG]VDDSPD
[KBL PDG] EE 0.1uF x1, 2.2uF x1.

CD60 0.1U_0402_10V7-K
CD61 2.2U_0402_6.3V6-M

Place decoupling cap close to DIMM

CD58 2.2U_0402_6.3V6-M @
CD59 0.1U_0402_10V7-K @

RD15 1K_0402_1%
RD16 2_0402_1%
RD17 1K_0402_1%
RD18 24.9_0402_1%
CD43 0.022U_0402_25V7-K
CD44 0.1U_0402_16V7-K @

[7] DDR4_VREF_DQ_CPU_B
M_VREF_CA_DIMMB

RD27 240_0402_1%
RD28 240_0402_1%

DDR_B_DQS#8
DDR_B_DQS8

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQSP[8:0] DDR0_DQSN[8:0] DDR1_DQSP[8:0] DDR1_DQSN[8:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4/-R5	Diff	The 9th signals[8] are applicable for UDIMM/ SODIM module with ECC in S and H-processor line processors

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

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Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_AON	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VS_AON	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_AON	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_AON	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VS_AON	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VS_AON				
STRAP3	+3VS_AON				
STRAP4	+3VS_AON				

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GPU	FB Memory (GDDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR	Samsung	K4W4G1646E-BC1A(E-Die)256MX16	PD 24.9K SD03424928T	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5TC4G63CFR-N0C(C-Die)256Mx16	PD 30.1K SD03430128T							
	Micron	MT41J256M16LY-091G:N	PD 20K SD02820028T							

Title: *VGA NOTE*

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B	*KENOBI*	2.0

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[15] PCIE_CTX_C_GRX_N[1..4]
[15] PCIE_CTX_C_GRX_P[1..4]
PCIE_CTX_C_GRX_N[1..4]
PCIE_CTX_C_GRX_P[1..4]
[15] PCIE_CRX_GTX_N[1..4]
[15] PCIE_CRX_GTX_P[1..4]
PCIE_CRX_GTX_N[1..4]
PCIE_CRX_GTX_P[1..4]

+3VS_AON
RV19 1 2 10K_0402_5%
@

UV1A
COMMON
1/14 PCI_EXPRESS

DIS@
[28] VGA_PEX_RST# VGA_PEX_RST# 1 2 RV11 0_0402_5%

[10] CLK_PCIE_VGA
[10] CLK_PCIE_VGA#
CLK_PCIE_VGA
CLK_PCIE_VGA#

PCIE_CRX_GTX_P1 CV8 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N1 CV9 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_P2 CV10 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N2 CV11 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_P3 CV12 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N3 CV13 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_P4 CV21 1 2 DIS@ 0.22U_0402_10V6-K
PCIE_CRX_GTX_N4 CV22 1 2 DIS@ 0.22U_0402_10V6-K

AB6	PEX_WAKE*_NC		
AC7	PEX_RST*		
AC6	PEX_CLKREQ*	CLKREQ_VGA#	
AE8	PEX_REFCLK		
AD8	PEX_REFCLK*		
AC9	PEX_TX0	PCIE_CRX_C_GTX_P1	
AB9	PEX_TX0*	PCIE_CRX_C_GTX_N1	
AG6	PEX_RX0	PCIE_CTX_C_GRX_P1	
AG7	PEX_RX0*	PCIE_CTX_C_GRX_N1	
AB10	PEX_TX1	PCIE_CRX_C_GTX_P2	
AC10	PEX_TX1*	PCIE_CRX_C_GTX_N2	
AF7	PEX_RX1	PCIE_CTX_C_GRX_P2	
AE7	PEX_RX1*	PCIE_CTX_C_GRX_N2	
AD11	PEX_TX2	PCIE_CRX_C_GTX_P3	
AC11	PEX_TX2*	PCIE_CRX_C_GTX_N3	
AE9	PEX_RX2	PCIE_CTX_C_GRX_P3	
AF9	PEX_RX2*	PCIE_CTX_C_GRX_N3	
AC12	PEX_TX3	PCIE_CRX_C_GTX_P4	
AB12	PEX_TX3*	PCIE_CRX_C_GTX_N4	
AG9	PEX_RX3	PCIE_CTX_C_GRX_P4	
AG10	PEX_RX3*	PCIE_CTX_C_GRX_N4	

NC FOR GM108

AB13	NC_AB13
AC13	NC_AC13
AF10	NC_AF10
AE10	NC_AE10
AD14	NC_AD14
AC14	NC_AC14
AE12	NC_AE12
AF12	NC_AF12
AC15	NC_AC15
AB15	NC_AB15
AG12	NC_AG12
AG13	NC_AG13
AB16	NC_AB16
AC16	NC_AC16
AF13	NC_AF13
AE13	NC_AE13

NC FOR GF117/GK208/GM108

AD17	NC_AD17
AC17	NC_AC17
AE15	NC_AE15
AF15	NC_AF15
AC18	NC_AC18
AB18	NC_AB18
AG15	NC_AG15
AG16	NC_AG16
AB19	NC_AB19
AC19	NC_AC19
AF16	NC_AF16
AE16	NC_AE16
AD20	NC_AD20
AC20	NC_AC20
AE18	NC_AE18
AF18	NC_AF18
AC21	NC_AC21
AB21	NC_AB21
AG18	NC_AG18
AG19	NC_AG19
AD23	NC_AD23
AE23	NC_AE23
AF19	NC_AF19
AE19	NC_AE19
AF24	NC_AF24
AE24	NC_AE24
AE21	NC_AE21
AF21	NC_AF21
AG24	NC_AG24
AG25	NC_AG25
AG21	NC_AG21
AG22	NC_AG22

N15S-GM-A1_FCBGA595
DIS@

Under GPU / Near GPU / Midway between GPU and power supply

+1VS_VGA

PEX_IOVDD_1	AA22	1U_0402_6.3VA-K	CV1
PEX_IOVDD_2	AB23		
PEX_IOVDD_3	AC24	4.7U_0603_6.3VA-K	CV3
PEX_IOVDD_4	AD25		
PEX_IOVDD_5	AE26	10U_0603_6.3V6-M	CV4
PEX_IOVDD_6	AE27		
		22U_0603_6.3V6-M	CV6

PEX_IOVDDQ_1	AA10	1U_0402_6.3VA-K	CV14
PEX_IOVDDQ_2	AA12		
PEX_IOVDDQ_3	AA13	4.7U_0603_6.3VA-K	CV16
PEX_IOVDDQ_4	AA16		
PEX_IOVDDQ_5	AA18	10U_0603_6.3V6-M	CV18
PEX_IOVDDQ_6	AA19		
PEX_IOVDDQ_7	AA20	22U_0603_6.3V6-M	CV19
PEX_IOVDDQ_8	AA21		
PEX_IOVDDQ_9	AB22		
PEX_IOVDDQ_10	AC23		
PEX_IOVDDQ_11	AD24		
PEX_IOVDDQ_12	AE25		
PEX_IOVDDQ_13	AF26		
PEX_IOVDDQ_14	AF27		

NVVDD Decoupling

Capacitor Type	GB2B-64	
	NV DG	Actual
4.7uF_0603	1	1
1uF_0402	1	1
22uF_0805	1	1
10uF_0805	1	1

NC FOR GF119

PEX_PLL_HVDD_1	AA8	0.1U_0402_16V7-K	CV23
PEX_PLL_HVDD_2	AA9		
PEX_SVDD_3V3	AB8	4.7U_0603_6.3VA-K	CV24
		4.7U_0603_6.3VA-K	CV25

+3VS_AON
Place near GPU

+VGA_CORE

VDD_SENSE	F2	100_0402_1%	RV2 DIS@
GND_SENSE	F1	100_0402_1%	RV3 DIS@

GFXCORE_VDD_SENSE_D [75]
GFXCORE_GND_SENSE_D [75]
to VGA CORE Power IC sense pin

+3VS_AON
[28,75] DGFX_PWRGD DGFX_PWRGD 2
[79] VDDQPWRGD VDDQPWRGD 3
DV1
1
All_GPU_PWRGD
All_GPU_PWRGD [11]
RV21 10K_0402_5% DIS@
BAT54AW_SOT323-3
DIS@
+3VS
RV9222 DIS@ 10K_0402_5% VDDQPWRGD

NV Suggest
+3VS_AON
+3VS_AON
RV5 10K_0402_5% DIS@
DIS@
[10] CLKREQ_PCIE4_VGA#
CLKREQ_VGA#
QV1
2N7002KW_SOT323-3
RV9 @ 10K_0402_5%
1 2 0_0402_5%
RV139 @

PEX_TSTCLK	AF22	PEX_TSTCLK	RV6 @ 1 2 200_0402_5%
PEX_TSTCLK*	AE22	PEX_TSTCLK#	
PEX_PLLVDD_1	AA14	0.1U_0402_16V7-K	CV26
PEX_PLLVDD_2	AA15	1U_0402_6.3VA-K	CV27
TESTMODE	AD9	GPU_TESTMODE	RV8 10K_0402_5% DIS@
PEX_TERMP	AF25	GPU_PEX_TERMP	2.49K_0402_1% RV10 DIS@

Under GPU / Near GPU
+1VS_VGA

0.1U_0402_16V7-K	CV26	DIS@	
1U_0402_6.3VA-K	CV27	DIS@	
4.7U_0603_6.3VA-K	CV28	DIS@	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/28	Deciphered Date	2016/08/27

Title	N16S-GT PCIE		
Size	Document Number		Rev
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UV1K

N15S-GM-A1_FCBGA_595P
COMMON

3/14 DACA

	GF117/GM108
NC_W5	NC
NC_AE2	TSEN_VREF
NC_AF2	NC

GF117	GM108/GK208	
NC	I2CA_SCL	B7
NC	I2CA_SDA	A7
NC	NC_AE3	AE3
NC	NC_AE4	AE4
NC	NC_AG3	AG3
NC	NC_AF4	AF4
NC	NC_AF3	AF3
GM108 GF117	GK208	

N15S-GM-A1_FCBGA595

UV1G

N15S-GM-A1_FCBGA_595P
COMMON

4/14 IFPAB

NC_AA6 — NC_V7 — NC_W7 — NC_W6 — NC_Y6

NC FOR GF117/GM108

NC FOR GF117/GM108

NC_AC4	AC4
NC_AC3	AC3
NC_Y3	Y3
NC_Y4	Y4
NC_AA2	AA2
NC_AA3	AA3
NC_AA1	AA1
NC_AB1	AB1
NC_AA5	AA5
NC_AA4	AA4
NC_AB4	AB4
NC_AB5	AB5
NC_AB2	AB2
NC_AB3	AB3
NC_AD2	AD2
NC_AD3	AD3
NC_AD1	AD1
NC_AE1	AE1
NC_AD5	AD5
NC_AD4	AD4

GF117	
NC	GPIO14 B3

IFPAB

N15S-GM-A1_FCBGA595

UV1J

N15S-GM-A1_FCBGA_595P
COMMON

7/14 IFPEF

NC_J7 — NC_K7 — NC_K6 — NC_H6 — NC_J6

IFPE

NC FOR GF117/GK208/GM108

GF119/GK208		
DVI-DL	DVI-SL/HDMI	DP
I2CY_SDA	I2CY_SDA	NC_J3 J3
I2CY_SCL	I2CY_SCL	NC_J2 J2
TXC	TXC	NC_J1 J1
TXC	TXC	NC_K1 K1
TXD0	TXD0	NC_K3 K3
TXD0	TXD0	NC_K2 K2
TXD1	TXD1	NC_M3 M3
TXD1	TXD1	NC_M2 M2
TXD2	TXD2	NC_M1 M1
TXD2	TXD2	NC_N1 N1
NC FOR GK208		

NC FOR GF117/GM108

HPD_E	HPD_E	GPIO18 C2
NC FOR GF117		

GF119/GK208		
DVI-DL	DVI-SL/HDMI	DP
	I2CZ_SDA	NC_H4 H4
	I2CZ_SCL	NC_H3 H3
TXC		NC_J5 J5
TXC		NC_J4 J4
TXD3	TXD0	NC_K5 K5
TXD3	TXD0	NC_K4 K4
TXD4	TXD1	NC_L4 L4
TXD4	TXD1	NC_L3 L3
TXD5	TXD2	NC_M5 M5
TXD5	TXD2	NC_M4 M4
NC FOR GK208		

NC FOR GF117/GM108

HPD_F		GPIO19 F7
NC FOR GF117		

IFPF

N15S-GM-A1_FCBGA595

UV1I

N15S-GM-A1_FCBGA_595P
COMMON

6/14 IFPD

NC_U6 — NC_T7 — NC_R7 — NC_R6

IFPD

NC FOR GF117/GM108

NC FOR GF117/GM108

GF119/GK208	
DVI/HDMI	DP
I2CX_SDA	NC_P4 P4
I2CX_SCL	NC_P3 P3
TXC	NC_R5 R5
TXC	NC_R4 R4
TXD0	NC_T5 T5
TXD0	NC_T4 T4
TXD1	NC_U4 U4
TXD1	NC_U3 U3
TXD2	NC_V4 V4
TXD2	NC_V3 V3

GF117	
NC	GPIO17 D4

N15S-GM-A1_FCBGA595

UV1H

N15S-GM-A1_FCBGA_595P
COMMON

5/14 IFPC

IFPC

NC_T6 — NC_M7 — NC_N7 — NC_P6

NC FOR GF117/GM108

NC FOR GF117/GM108

GF119/GK208	
DVI/HDMI	DP
I2CW_SDA	NC_N5 N5
I2CW_SCL	NC_N4 N4
TXC	NC_N3 N3
TXC	NC_N2 N2
TXD0	NC_R3 R3
TXD0	NC_R2 R2
TXD1	NC_R1 R1
TXD1	NC_T1 T1
TXD2	NC_T3 T3
TXD2	NC_T2 T2

GF117	
NC	GPIO15 C3

N15S-GM-A1_FCBGA595

Title: ***N16S-GT DP Power***

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UV1B

N15S-GM-A1_FCBGA_595P

COMMON

2/14 FBA

[31,32] FBA_D[63..0]

FBA_D0	E18	FBA_D0
FBA_D1	F18	FBA_D1
FBA_D2	E16	FBA_D2
FBA_D3	F17	FBA_D3
FBA_D4	D20	FBA_D4
FBA_D5	D21	FBA_D5
FBA_D6	F20	FBA_D6
FBA_D7	E21	FBA_D7
FBA_D8	E15	FBA_D8
FBA_D9	D15	FBA_D9
FBA_D10	F15	FBA_D10
FBA_D11	F13	FBA_D11
FBA_D12	C13	FBA_D12
FBA_D13	B13	FBA_D13
FBA_D14	E13	FBA_D14
FBA_D15	D13	FBA_D15
FBA_D16	B15	FBA_D16
FBA_D17	C16	FBA_D17
FBA_D18	A13	FBA_D18
FBA_D19	A15	FBA_D19
FBA_D20	B18	FBA_D20
FBA_D21	A18	FBA_D21
FBA_D22	A19	FBA_D22
FBA_D23	C19	FBA_D23
FBA_D24	B24	FBA_D24
FBA_D25	C23	FBA_D25
FBA_D26	A25	FBA_D26
FBA_D27	A24	FBA_D27
FBA_D28	A21	FBA_D28
FBA_D29	B21	FBA_D29
FBA_D30	C20	FBA_D30
FBA_D31	C21	FBA_D31
FBA_D32	R22	FBA_D32
FBA_D33	R24	FBA_D33
FBA_D34	T22	FBA_D34
FBA_D35	R23	FBA_D35
FBA_D36	N25	FBA_D36
FBA_D37	N26	FBA_D37
FBA_D38	N23	FBA_D38
FBA_D39	N24	FBA_D39
FBA_D40	V23	FBA_D40
FBA_D41	V22	FBA_D41
FBA_D42	T23	FBA_D42
FBA_D43	U22	FBA_D43
FBA_D44	Y24	FBA_D44
FBA_D45	AA24	FBA_D45
FBA_D46	Y22	FBA_D46
FBA_D47	AA23	FBA_D47
FBA_D48	AD27	FBA_D48
FBA_D49	AB25	FBA_D49
FBA_D50	AD26	FBA_D50
FBA_D51	AC25	FBA_D51
FBA_D52	AA27	FBA_D52
FBA_D53	AA26	FBA_D53
FBA_D54	W26	FBA_D54
FBA_D55	Y25	FBA_D55
FBA_D56	R26	FBA_D56
FBA_D57	T25	FBA_D57
FBA_D58	N27	FBA_D58
FBA_D59	R27	FBA_D59
FBA_D60	V26	FBA_D60
FBA_D61	V27	FBA_D61
FBA_D62	W27	FBA_D62
FBA_D63	W25	FBA_D63

[31,32] FBA_DQM[7..0]

FBA_DQM0	D19	FBA_DQM0
FBA_DQM1	D14	FBA_DQM1
FBA_DQM2	C17	FBA_DQM2
FBA_DQM3	C22	FBA_DQM3
FBA_DQM4	P24	FBA_DQM4
FBA_DQM5	W24	FBA_DQM5
FBA_DQM6	AA25	FBA_DQM6
FBA_DQM7	U25	FBA_DQM7

[31,32] FBA_DQS[7..0]

FBA_DQS0	E19	FBA_DQS_WP0
FBA_DQS1	C15	FBA_DQS_WP1
FBA_DQS2	B16	FBA_DQS_WP2
FBA_DQS3	B22	FBA_DQS_WP3
FBA_DQS4	R25	FBA_DQS_WP4
FBA_DQS5	W23	FBA_DQS_WP5
FBA_DQS6	AB26	FBA_DQS_WP6
FBA_DQS7	T26	FBA_DQS_WP7

[31,32] FBA_DQS#[7..0]

FBA_DQS#0	F19	FBA_DQS_RN0
FBA_DQS#1	C14	FBA_DQS_RN1
FBA_DQS#2	A16	FBA_DQS_RN2
FBA_DQS#3	A22	FBA_DQS_RN3
FBA_DQS#4	P25	FBA_DQS_RN4
FBA_DQS#5	W22	FBA_DQS_RN5
FBA_DQS#6	AB27	FBA_DQS_RN6
FBA_DQS#7	T27	FBA_DQS_RN7

NC — FB_CLAMP

GF119

F3 GPU_FB_CLAMP

RV12 DIS@ 10K_0402_5%

FBA_CMD0	C27	FBA_CSA0#
FBA_CMD1	C26	
FBA_CMD2	E24	FBA_ODTA0
FBA_CMD3	F24	FBA_CKEA0
FBA_CMD4	D27	FBA_MA14
FBA_CMD5	D26	FBA_RST#
FBA_CMD6	F25	FBA_MA9
FBA_CMD7	F26	FBA_MA7
FBA_CMD8	F23	FBA_MA2
FBA_CMD9	G22	FBA_MA0
FBA_CMD10	G23	FBA_MA4
FBA_CMD11	G24	FBA_MA1
FBA_CMD12	F27	FBA_BA0
FBA_CMD13	G25	FBA_WE#
FBA_CMD14	G27	
FBA_CMD15	G26	FBA_CAS#
FBA_CMD16	M24	FBA_CSA1#
FBA_CMD17	M23	
FBA_CMD18	K24	FBA_ODTA1
FBA_CMD19	K23	FBA_CKEA1
FBA_CMD20	M27	FBA_MA13
FBA_CMD21	M26	FBA_MA8
FBA_CMD22	M25	FBA_MA6
FBA_CMD23	K26	FBA_MA11
FBA_CMD24	K22	FBA_MA5
FBA_CMD25	J23	FBA_MA3
FBA_CMD26	J25	FBA_BA2
FBA_CMD27	J24	FBA_BA1
FBA_CMD28	K27	FBA_MA12
FBA_CMD29	K25	FBA_MA10
FBA_CMD30	J27	FBA_RAS#
FBA_CMD31	J26	

FBA_CSA0# → FBA_CSA0# [31]

FBA_ODTA0 → FBA_ODTA0 [31]

FBA_CKEA0 → FBA_CKEA0 [31]

FBA_RST# → FBA_RST# [31,32]

FBA_BA0 → FBA_BA0 [31,32]

FBA_WE# → FBA_WE# [31,32]

FBA_CAS# → FBA_CAS# [31,32]

FBA_CSA1# → FBA_CSA1# [32]

FBA_ODTA1 → FBA_ODTA1 [32]

FBA_CKEA1 → FBA_CKEA1 [32]

FBA_BA2 → FBA_BA2 [31,32]

FBA_BA1 → FBA_BA1 [31,32]

FBA_RAS# → FBA_RAS# [31,32]

FBA_MA[0..14] [31,32]

GF117/GF119 GK208

NC — FBA_CMD32

FBA_DEBUG0 — FBA_CMD34

FBA_DEBUG1 — FBA_CMD35

B19 FBA_CMD32

F22 FBA_CMD34

J22 FBA_CMD35

RV17 RV18 @0_0402_5% For Debug

+1.5VS_VGA

FBA_CLK0	D24	FBA_CLKA0
FBA_CLK0*	D25	FBA_CLKA0#
FBA_CLK1	N22	FBA_CLKA1
FBA_CLK1*	M22	FBA_CLKA1#

FBA_CLKA0 → FBA_CLKA0 [31]

FBA_CLKA0# → FBA_CLKA0# [31]

FBA_CLKA1 → FBA_CLKA1 [32]

FBA_CLKA1# → FBA_CLKA1# [32]

FBA_WCK01	D18	
FBA_WCK01*	C18	
FBA_WCK23	D17	
FBA_WCK23*	D16	
FBA_WCK45	Y24	
FBA_WCK45*	U24	
FBA_WCK67	V24	
FBA_WCK67*	V25	

GF119 — FB_PLLAVDD_1

NC — FB_PLLAVDD_2

FB_PLLAVDD — FB_DLLAVDD

GF117

F16 FB_PLL

P22

H22

LV3 DIS@ MPZ1608S300AT_2P~D

+1VS_VGA

0.1U_0402_16V7-K CV39 DIS@

0.1U_0402_16V7-K CV40 DIS@

0.1U_0402_16V7-K CV41 DIS@

22U_0603_6.3V6-M CV42 DIS@

Under GPU

FBA_RST#

FBA_ODTA0

FBA_ODTA1

FBA_CKEA0

FBA_CKEA1

RV13 DIS@ 10K_0402_5%

RV14 10K_0402_5%

RV15 DIS@ 10K_0402_5%

RV16 10K_0402_5%

RV20 DIS@ 10K_0402_5%

PTP1

1 D23 FB_VREF

Test_Point_12MIL

N15S-GM-A1_FCBGA595

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/28	Deciphered Date	2016/08/27

Title: *N16S-GT MEM Interface*

Size	Document Number	Rev
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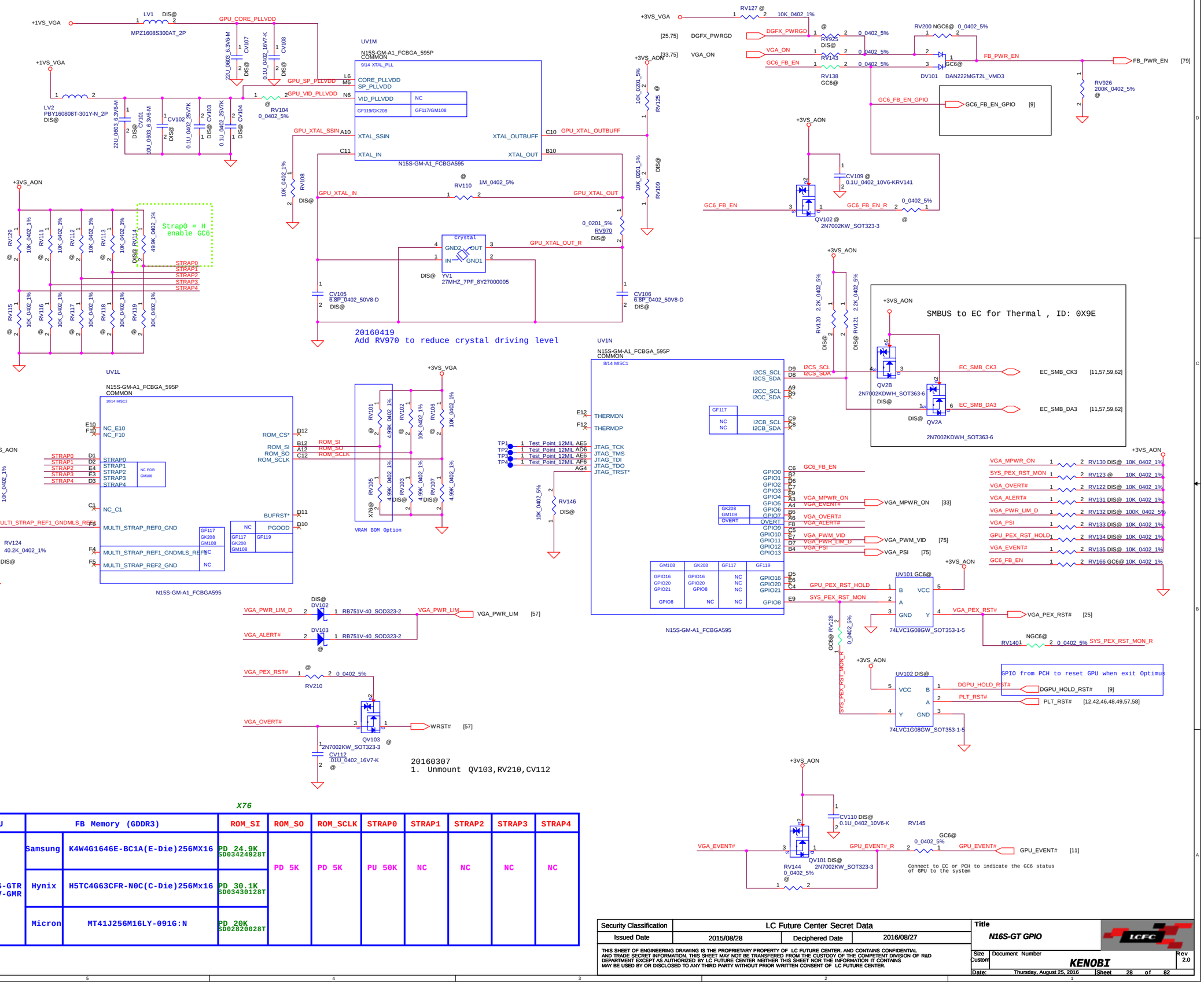

X76

GPU	FB Memory (GDDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR	Samsung	K4W4G1646E-BC1A(E-Die)256MX16	PD 24.9K SD03424928T	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
	Hynix	H5TC4G63CFR-N0C(C-Die)256Mx16	PD 30.1K SD03430128T							
	Micron	MT41J256M16LY-091G:N	PD 20K SD02820028T							

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/28	Deciphered Date	2016/08/27

Title	N16S-GT GPIO		
Size	Document Number	KENOBI	Rev 2.0
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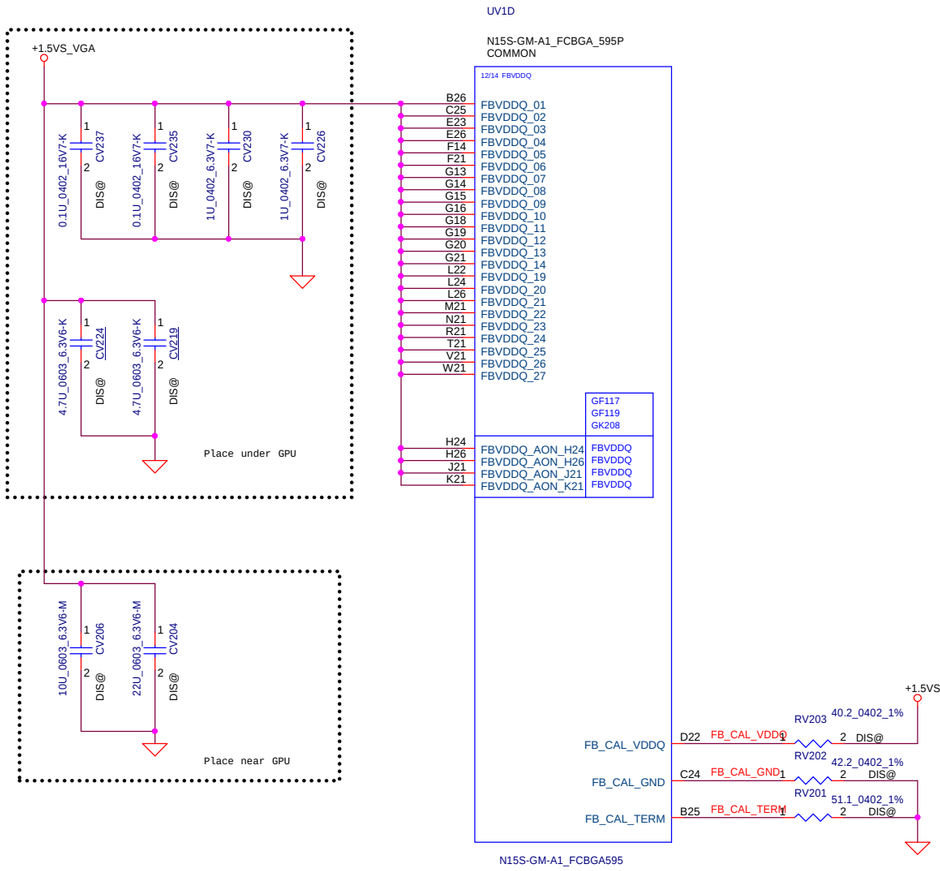

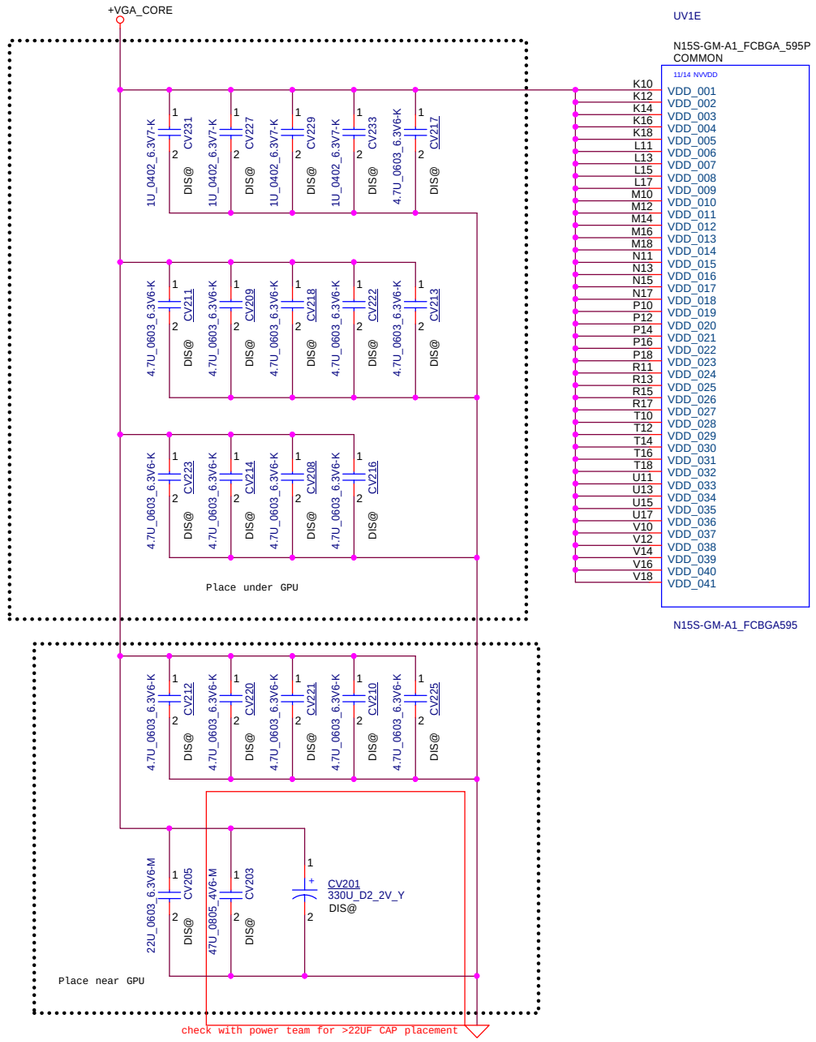

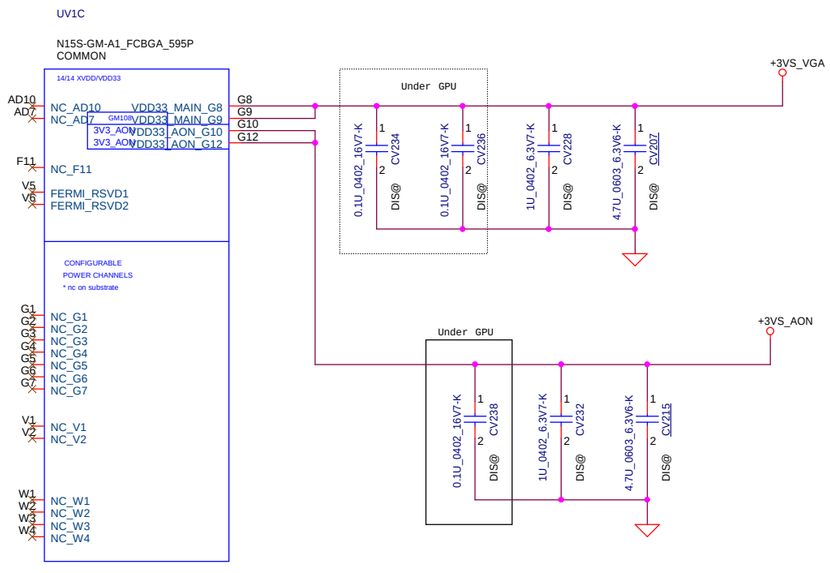

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UV1F

N15S-GM-A1_FCBGA_595P
COMMON

13/14 GND

A2	GND_001	GND_071	M13
AB17	GND_005	GND_072	M15
AB20	GND_006	GND_073	M17
AB24	GND_007	GND_074	N10
AC2	GND_008	GND_075	N12
AC22	GND_009	GND_076	N14
AC26	GND_010	GND_077	N16
AC5	GND_011	GND_078	N18
AC8	GND_012	GND_079	P11
AD12	GND_013	GND_080	P13
AD13	GND_014	GND_081	P15
A26	GND_002	GND_082	P17
AD15	GND_015	GND_083	P2
AD16	GND_016	GND_084	P23
AD18	GND_017	GND_085	P26
AD19	GND_018	GND_086	P5
AD21	GND_019	GND_087	R10
AD22	GND_020	GND_088	R12
AE11	GND_021	GND_089	R14
AE14	GND_022	GND_090	R16
AE17	GND_023	GND_091	R18
AE20	GND_024	GND_092	T11
AB11	GND_003	GND_093	T13
AF1	GND_025	GND_094	T15
AF11	GND_026	GND_095	T17
AF14	GND_027	GND_096	U10
AF17	GND_028	GND_097	U12
AF20	GND_029	GND_098	U14
AF23	GND_030	GND_099	U16
AF5	GND_031	GND_100	U18
AF8	GND_032	GND_101	U2
AG2	GND_033	GND_102	U23
AG26	GND_034	GND_103	U26
AB14	GND_004	GND_104	U5
B1	GND_035	GND_105	V11
B11	GND_036	GND_106	V13
B14	GND_037	GND_107	V15
B17	GND_038	GND_108	V17
B20	GND_039	GND_109	Y2
B23	GND_040	GND_110	Y23
B27	GND_041	GND_111	Y26
B5	GND_042	GND_112	Y5
B8	GND_043		
E11	GND_044		
E14	GND_045		
E17	GND_046		
E2	GND_047		
E20	GND_048		
E22	GND_049		
E25	GND_050		
E5	GND_051		
E8	GND_052		
H2	GND_053		
H23	GND_054		
H25	GND_055		
H5	GND_056		
K11	GND_057		
K13	GND_058		
K15	GND_059		
K17	GND_060		
L10	GND_061		
L12	GND_062		
L14	GND_063		
L16	GND_064		
L18	GND_065		
L2	GND_066		
L23	GND_067		
L25	GND_068		
L5	GND_069	GND_AA7	AA7
M11	GND_070	GND_AB7	AB7

N15S-GM-A1_FCBGA595

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Title: *N16S-GT GND*

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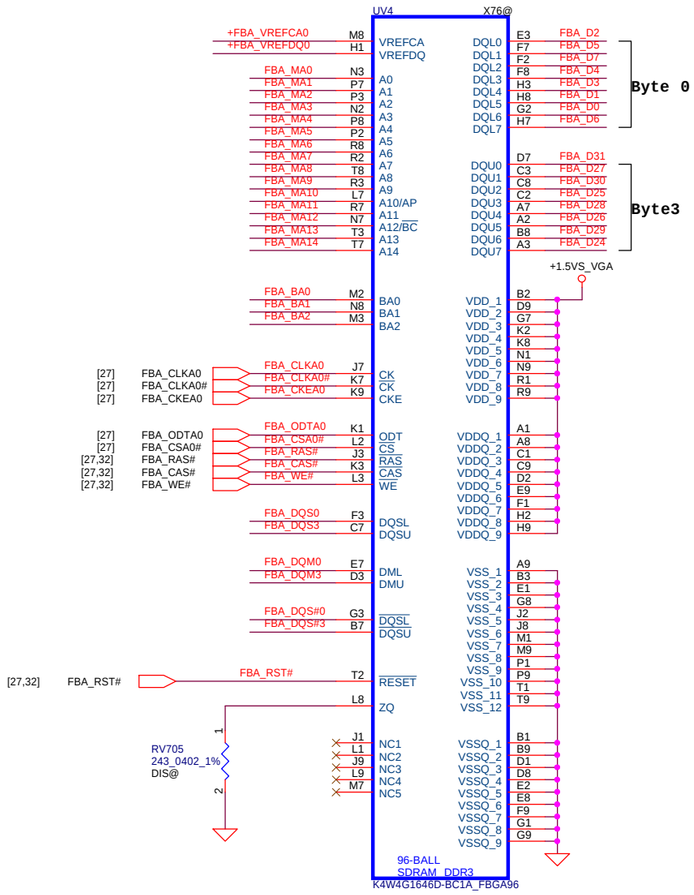
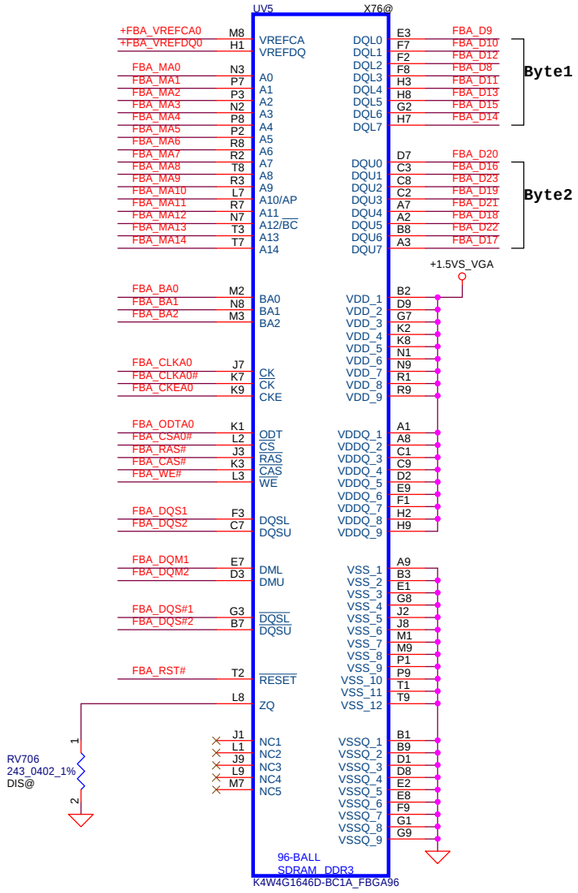
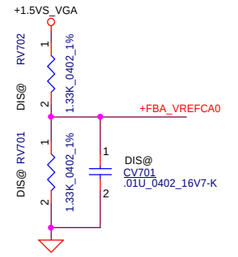
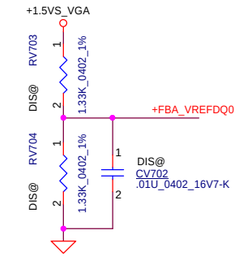
Memory Partition A - Lower 32 bits

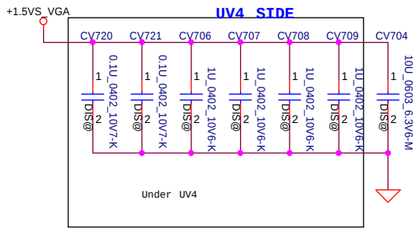


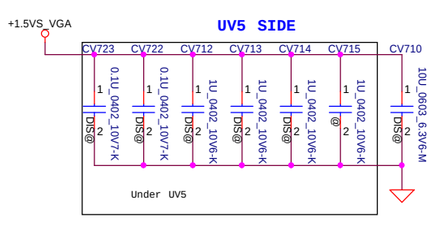


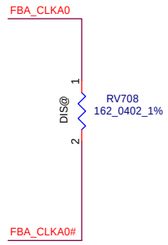
FBA_MA[14..0] [27,32]
FBA_BA[2..0] [27,32]
FBA_DQS[7..0] [27,32]
FBA_DQM[7..0] [27,32]
FBA_DQS#[7..0] [27,32]
FBA_D[0..63] [27,32]











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Title	N16S-GT DDR3L VRAM L	
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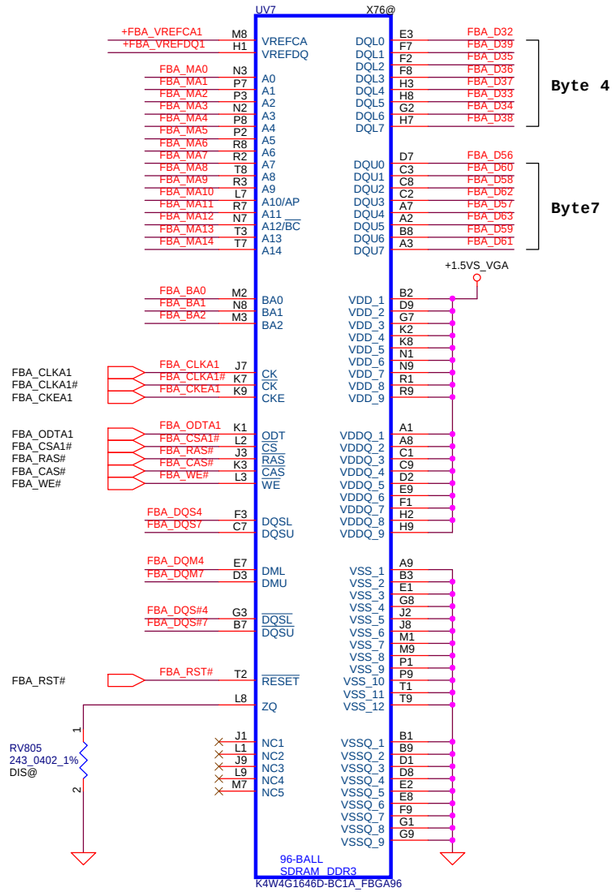
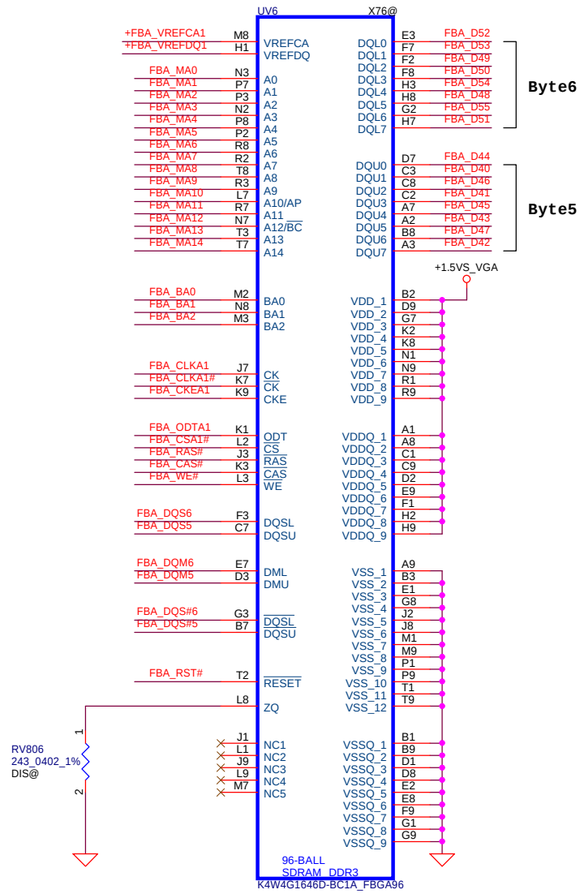
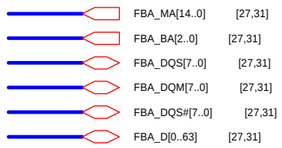
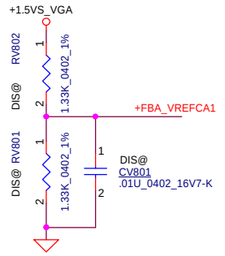
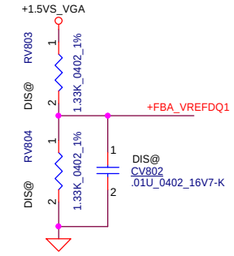
Memory Partition A - Upper 32 bits

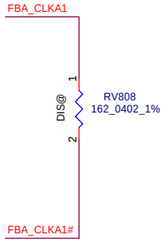


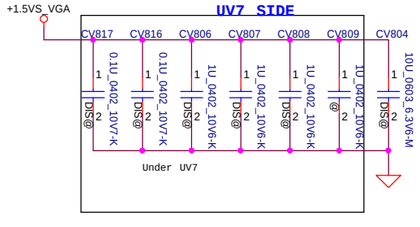


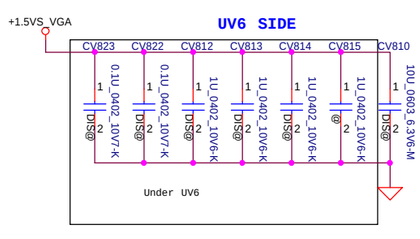












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Title	N16S-GT DDR3L VRAM U	
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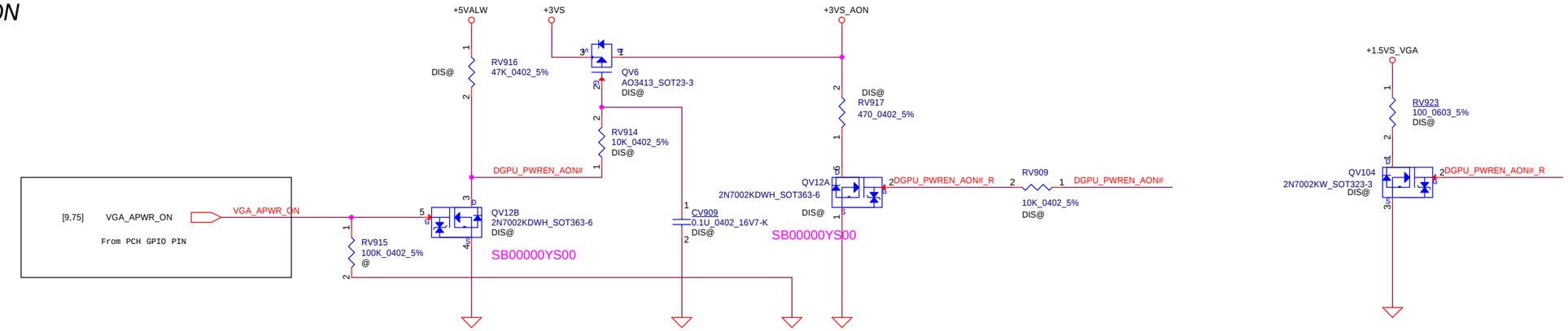
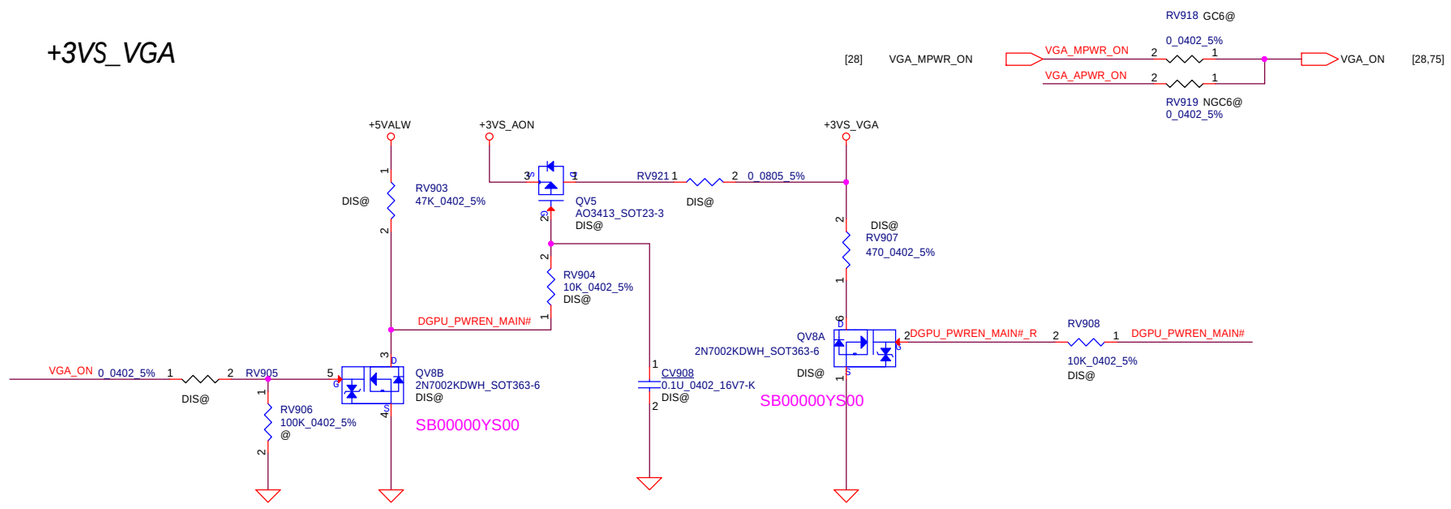
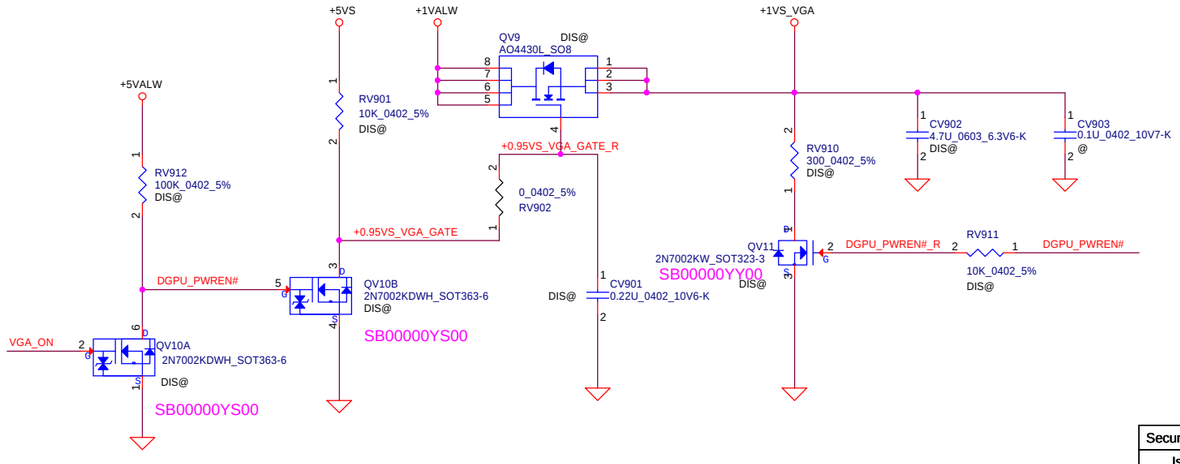
+3VS to +3VS_AON



+3VS_VGA



+1VALW to +1VS_VGA



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Title: *N16S-GT swich power*

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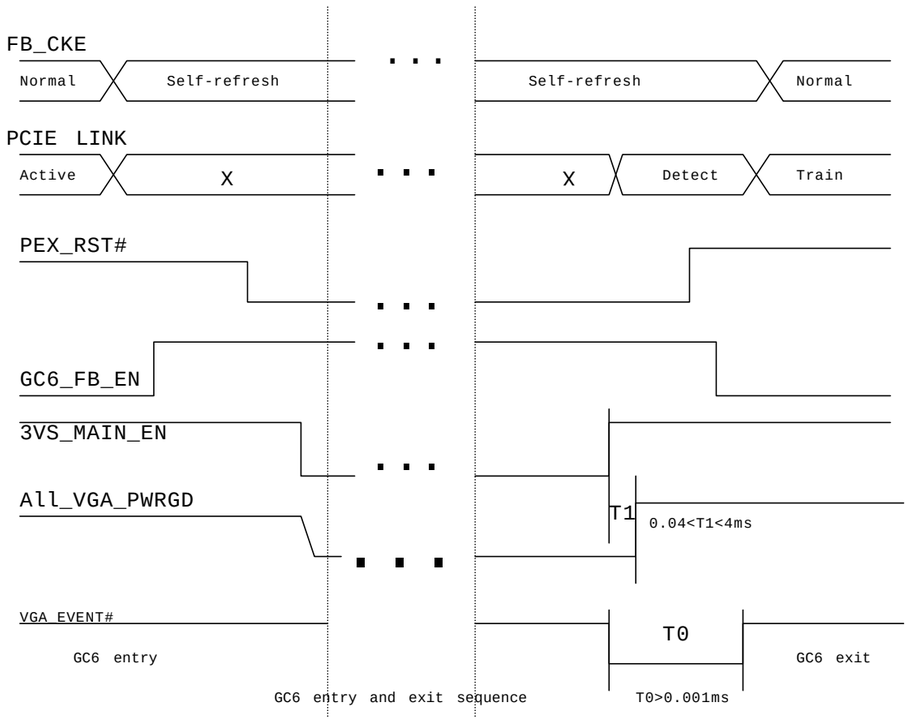
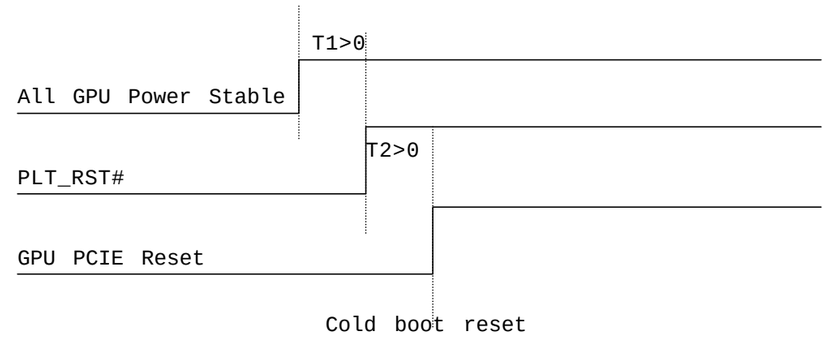
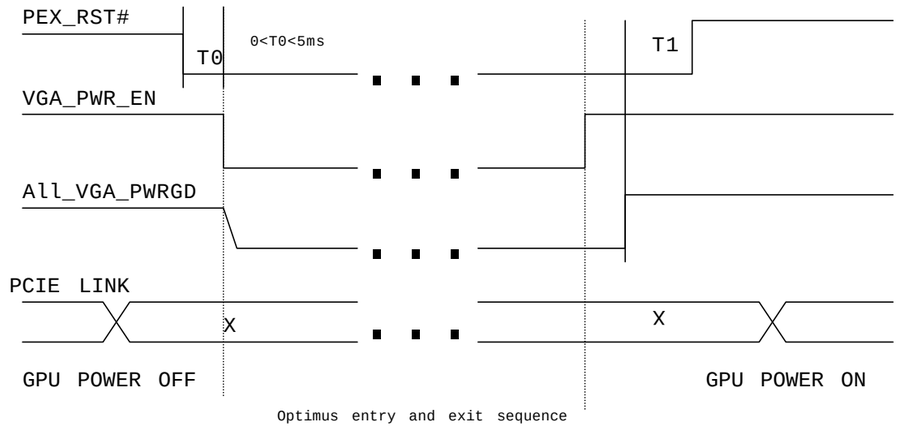
GPIO	I/O	Functional Description	I/O Termination
GPIO0	O	FB Enable for GC6 2.0, Open source	10K pull-down
GPIO1	O	Memory voltage control	Pull-up/pull down to set the FBVDD/Q boot voltage
GPIO2	O	Panel Backlight PWM Brightness Control	100K pull down
GPIO3	O	Panel Power Enable	100K pull down
GPIO4	O	Panel Backlight Enable	100K pull down
GPIO5	O	GPU Power Sequence for GC6 2.0, Open Drain	10k pull-up to 3V3_AON
GPIO6	I	GPU wake signal for GC6 2.0	10k pull-up to 3V3_AON
GPIO7	O	3D Vision L/R signal	100K pull down
GPIO8	O	System side PCIe rest monitor	10k pull-up to 3V3_AON
GPIO9	I/O	Active low thermal alert, open drain	10k pull-up to 3V3_AON
GPIO10	O	Memory VREF Control	100K pull down
GPIO11	O	GPU Core VDD PWM control signal	
GPIO12	I	AC power detect or power supply overdraw input	100k pull-up to 3V3_AON
GPIO13	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase
GPIO14	I	Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI	
GPIO15	I	Hot Plug Detect for IFPC	
GPIO16	I	Active Low Frame Lock, Open Drain	10k pull-up to 3V3_AON
GPIO17	I	Hot Plug Detect for IFPD	
GPIO18	I	Hot Plug Detect for IFPE	
GPIO19	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	
GPIO20	O	Reserved	
GPIO21	O	GPU PCIe self-reset control, Open Drain	10k pull-up to 3V3_AON
OVERT	I/O	Catastrophic Over Temperature	100k pull-up to 3V3_AON







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Title: **GPU GPIO table & sequence**

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Title: ***Blank***

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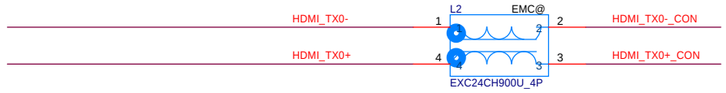
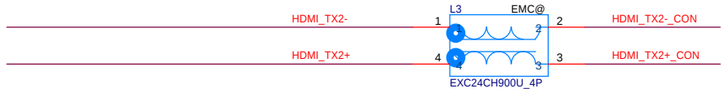
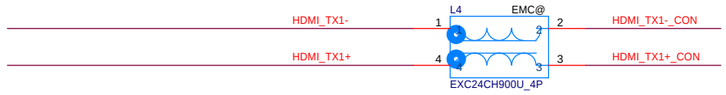
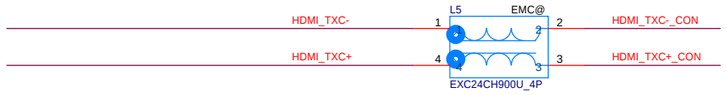
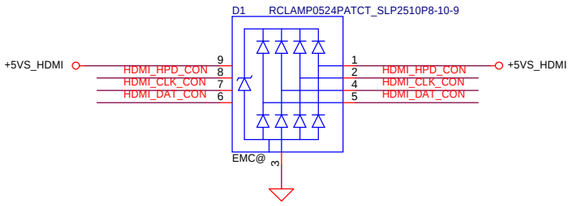
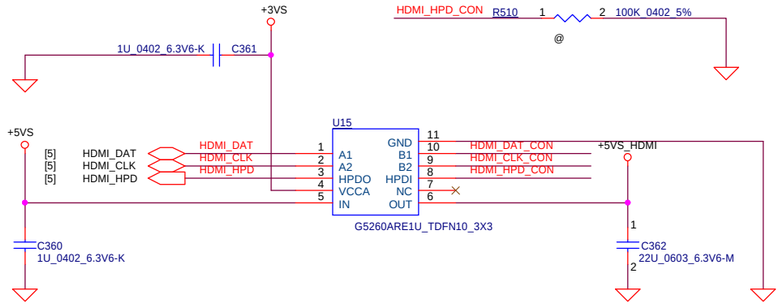


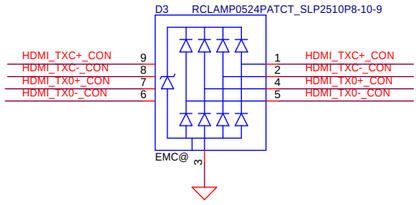


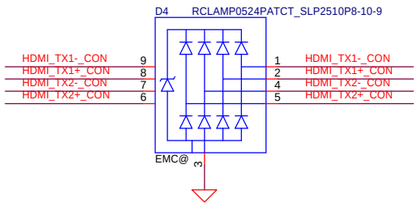


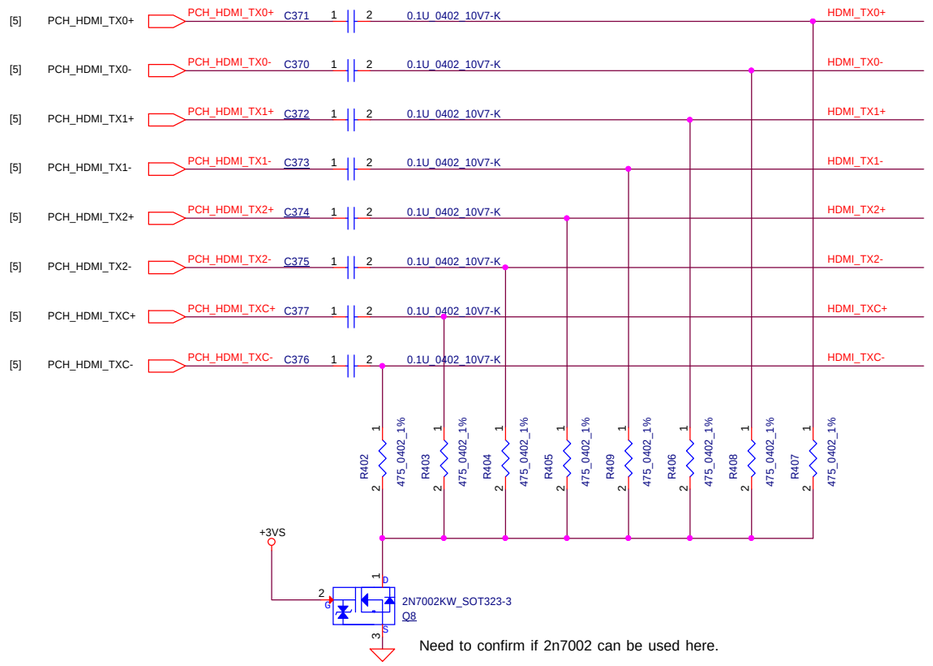




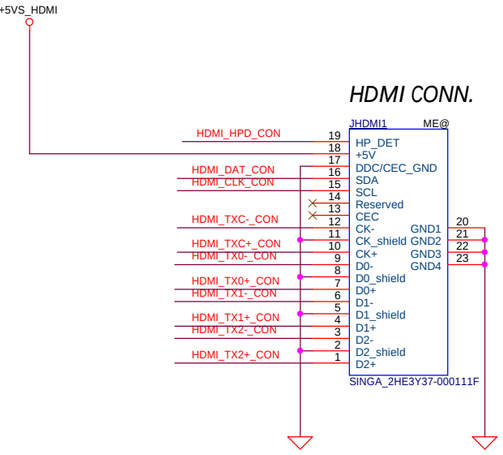








Need to confirm if 2n7002 can be used here.



HDMI CONN.

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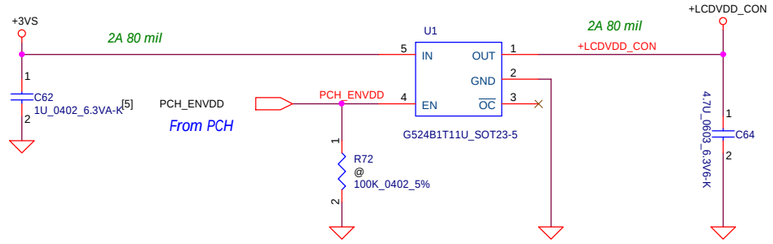
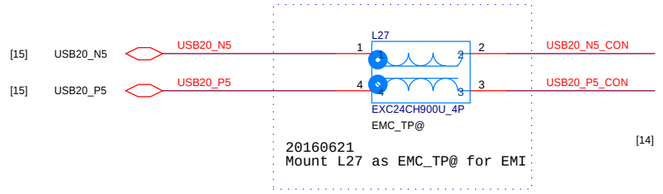
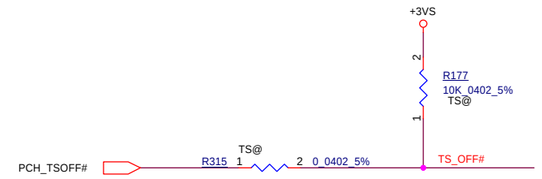
LCDVDD Circuit

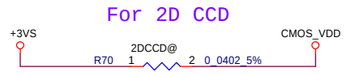


Touch Panel

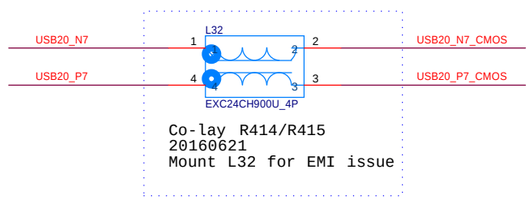


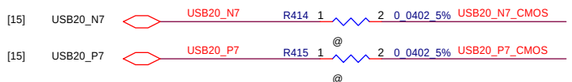


CMOS Camera



CMOS USB Port





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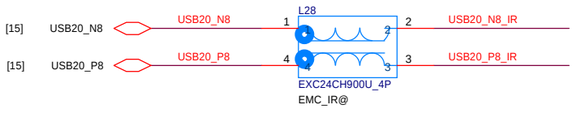
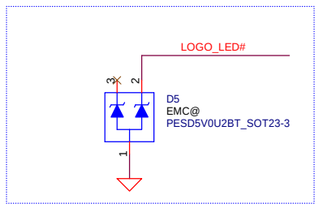
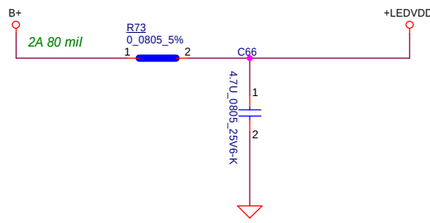
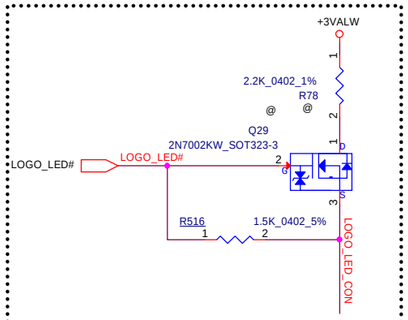
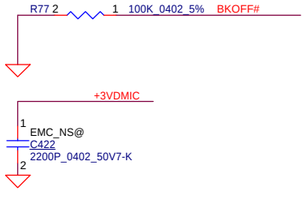


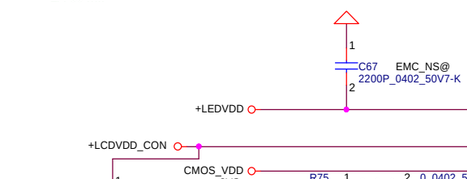
ESD request











eDP CONN.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	eDP CONN		
Size	Document Number		Rev
Custom	KENOBI		2.0
Date:	Thursday, August 25, 2016	Sheet	37 of 82

BLANK

Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2014/09/07

Title: ***HDMI RP***

Size	Document Number	Rev
Custom	***KENOBI***	2.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title

CRT CONN

Size	Document Number	Rev
Custom	***KENOBI***	2.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: ***DP to VGA***

Size	Document Number	Rev
Custom	***KENOBI***	2.0

Date: Thursday, August 25, 2016 Sheet 40 of 82

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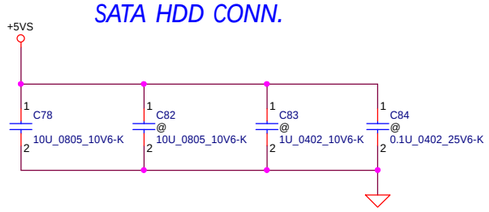
Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: ***Mux IC***

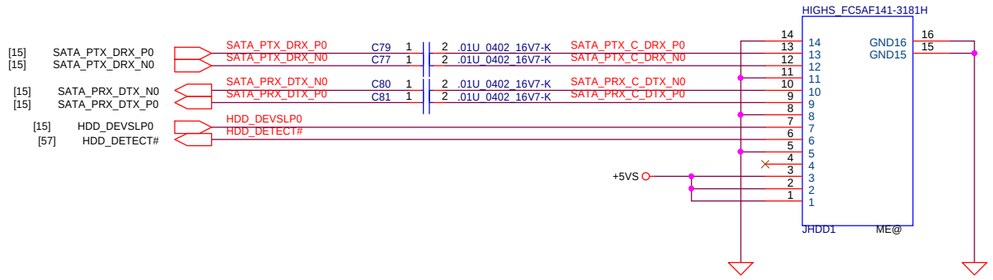
Size: Custom | Document Number: ***KENOBI*** | Rev: 2.0

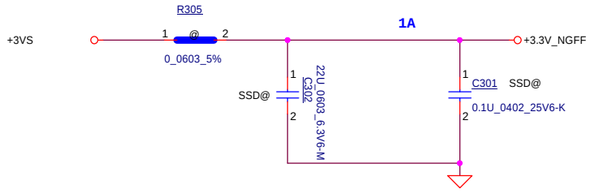
Date: Thursday, August 25, 2016 | Sheet 41 of 82

SATA HDD CONN.

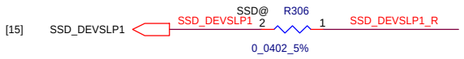


SATA HDD CONN.

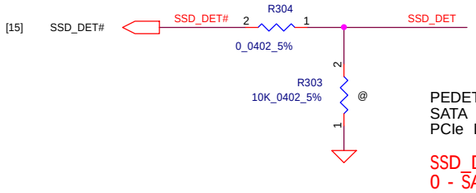




M.2 SSD(SATA/PCIE)

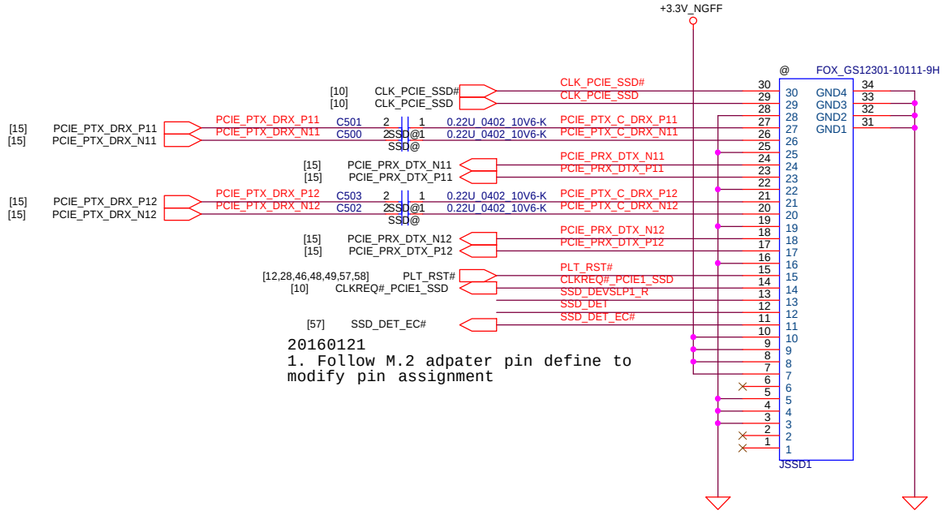


20160308
1. Remove R300,R301,R302 and put it to CPU side



PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open

SSD_DET#
0 - SATA
1 - PCIE



20160121
1. Follow M.2 adpater pin define to modify pin assignment

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: SATA HDD

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Security Classification	LC Future Center Secret Data		
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Title

ODD

Size	Document Number	Rev
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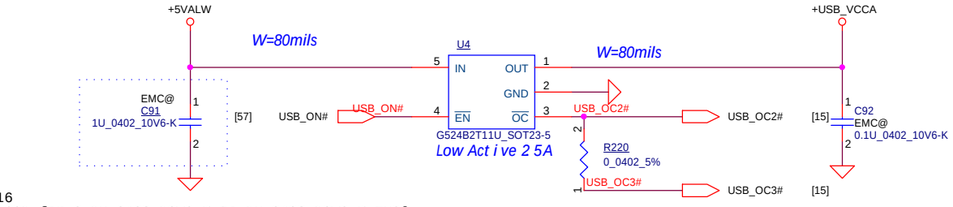
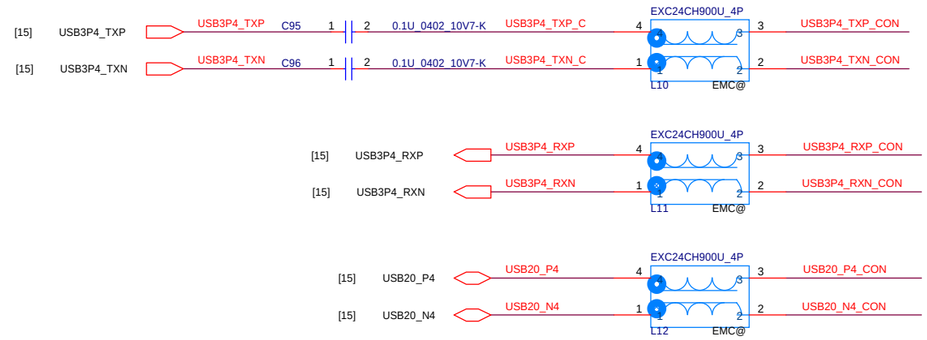
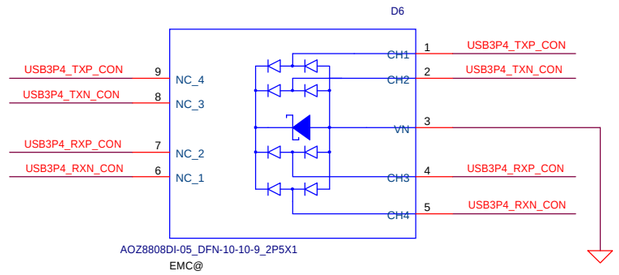
USB3 PORT4

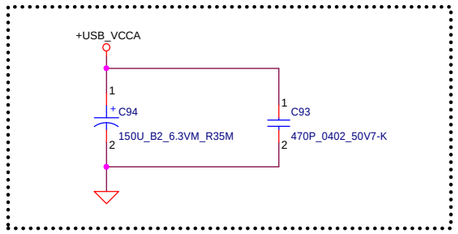
POWER SWITCH

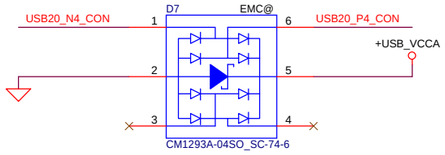


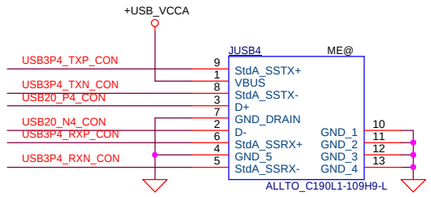
20160616
Change C91 for 0.1U_0402_10V6-K to 1U_0402_10V6-K EMC@



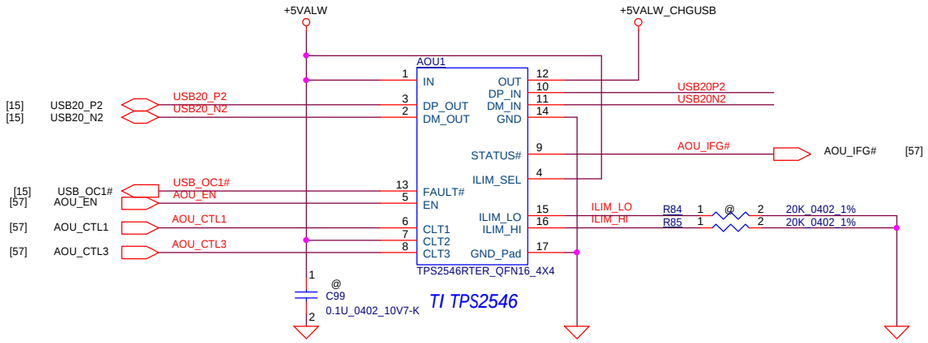




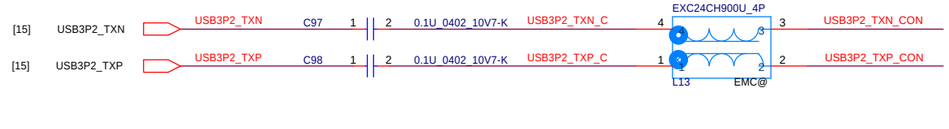


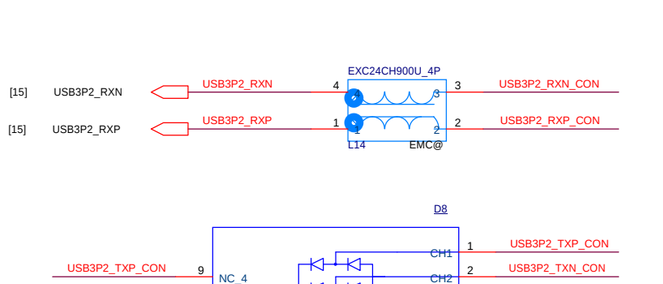


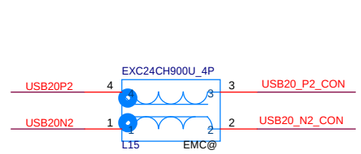
PORT2(AOU)

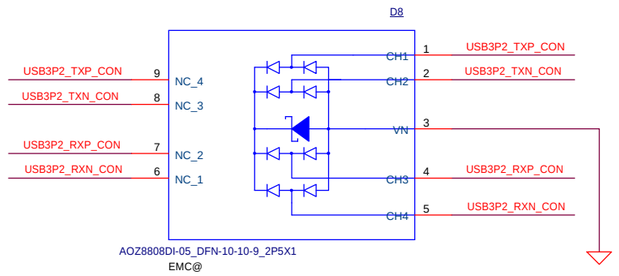


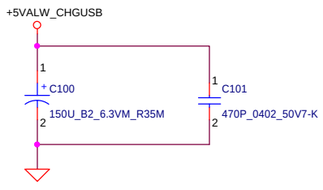
	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	**DCH**	OUT held low
*	1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	**SDP2**	Data Connected
*	1	1	0	X	**SDP1**	Data Connected
*	0	1	0	X	**SDP1**	Data Connected
	1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active

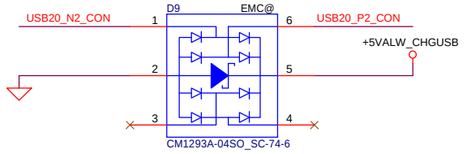


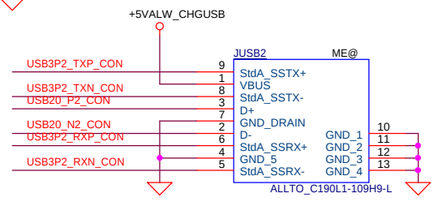












Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **USB3 PORT1/PORT2(AOU)**

Size	Document Number	Rev
Custom	KENOBI	2.0

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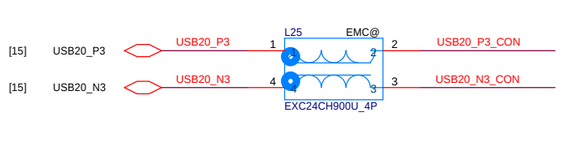
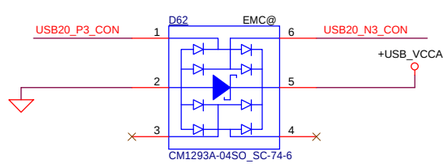
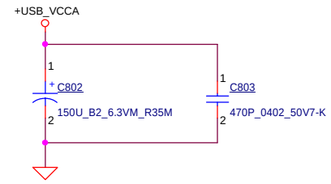
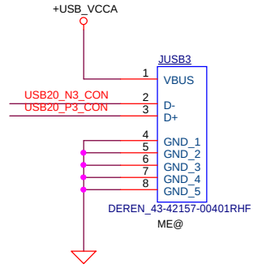
USB3 PORT3









Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: **USB PORT3**

Size	Document Number	Rev
Custom	KENOBI	2.0

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+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms<Spec<100m s

width : 40 mils

+3VALW
+3VALW_LAN
RL18 1 2 0_0805_5%
LP2301ALT1G_SOT23-3
CL7 QL2 CL8
0.1U_0402_10V7-K
CL2 CL3 4.7U_0603_6.3V6-K
CL4 CL5 0.1U_0402_10V7-K
[12] PCH_SLP_LAN#
RL5 1 @ 2 47K_0402_5%
Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

+3VALW_LAN
+LAN_VDDREG
RL1 1 2 0_0603_5%
CL1 4.7U_0603_6.3V6-K
CL6 0.1U_0402_10V7-K

+3VALW_LAN
+3VS
RL2 10K_0402_5% @
QL1 2N7002KW_SOT323-3
LAN_CLKREQ#_R
CLKREQ_PCIE3_LAN# [10]
RL4 1 2 0_0402_5%

+3VALW_LAN
RL6 10K_0402_5%
[57] LAN_WAKE#
RL7 1 2 0_0402_5%
LAN_WAKE#_R

CL10 close to Pin18
CL9 close to Pin17

[15] PCIE_PRX_DTX_P10
[15] PCIE_PRX_DTX_N10
PCIE_PRX_DTX_P10 CL9 1 2 0.1U_0402_10V7-K PCIE_PRX_DTX_C_P10
PCIE_PRX_DTX_N10 CL10 1 2 0.1U_0402_10V7-K PCIE_PRX_DTX_C_N10
[12,28,42,48,49,57,58] PLT_RST#

UL1

+3VALW_LAN	11	AVDD33_1	
+3VALW_LAN	32	AVDD33_2	
PCIE_PRX_DTX_C_P10	17	HSOP	
PCIE_PRX_DTX_C_N10	18	HSON	
PLT_RST#	19	PERSTB	
ISOLATE#	20	ISOLATEB	
LAN_WAKE#_R	21	LANWAKEB	
+LAN_VDDREG	23	VDDREG	
+LAN_REGOUT	24	REGOUT	
RJ45_LINKUP#	25	LED2	
LED1	26	LED1/GPO	
RJ45_ACTIVITY#	27	LED0	
LAN_XTALO	28	CKXTAL1	
LAN_XTALI	29	CKXTAL2	
	33	GND	
		RSET	31 RSET

	3	AVDD10_1	+LAN_VDD10
	8	AVDD10_2	+LAN_VDD10
	30	AVDD10_3	+LAN_VDD10
	22	DVDD10	+LAN_VDD10
MDIP0	1	MDIP0	MDI_0+
MDIN0	2	MDIN0	MDI_0-
MDIP1	4	MDIP1	MDI_1+
MDIN1	5	MDIN1	MDI_1-
MDIP2	6	MDIP2	MDI_2+
MDIN2	7	MDIN2	MDI_2-
MDIP3	9	MDIP3	MDI_3+
MDIN3	10	MDIN3	MDI_3-
HSIP	13	HSIP	PCIE_PTX_C_DRX_P10
HSIN	14	HSIN	PCIE_PTX_C_DRX_N10
CLKREQB	12	CLKREQB	LAN_CLKREQ#_R
REFCLK_P	15	REFCLK_P	CLK_PCIE_LAN
REFCLK_N	16	REFCLK_N	CLK_PCIE_LAN#
RSET	31	RSET	

RTL8111GUS-CG_QFN32_4X4

MDI_0+ [47] MDI_0- [47]
MDI_1+ [47] MDI_1- [47]
MDI_2+ [47] MDI_2- [47]
MDI_3+ [47] MDI_3- [47]
PCIE_PTX_C_DRX_P10 [15] PCIE_PTX_C_DRX_N10 [15]
CLK_PCIE_LAN [10] CLK_PCIE_LAN# [10]

RL10 2.49K_0402_1%

+3VS
RL8 1K_0402_5%
ISOLATE#
RL9 15K_0402_5%

+3VALW_LAN
RL19 10K_0402_5%
LED1

TL2 1 RJ45_LINKUP#
TL3 1 LED1
TL4 1 RJ45_ACTIVITY#

[47] RJ45_LINKUP#
[47] RJ45_ACTIVITY#

LAN_XTALI
LAN_XTALO
YL1
OSC1 GND2
GND1 OSC2
25MHZ_10PF_7V25000014
CL11 12P_0402_50V8-J
CL12 12P_0402_50V8-J

+LAN_VDD10
+LAN_REGOUT
LL1
2.2UH_EP-22AM05B02_2A_20%
CL14 4.7U_0603_6.3V6-K
CL15 0.1U_0402_10V7-K
CL16 0.1U_0402_10V7-K
CL17 0.1U_0402_10V7-K
CL18 0.1U_0402_10V7-K
CL19 0.1U_0402_10V7-K
CL20 1U_0402_10V6-K @

Layout Note: LL1 must be within 200mil to Pin24, CL14,CL15 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

Close to Pin3, 8, 22, 30
LAYOUT NEED CHECK
Close to Pin22(Reserved)

Security Classification	LC Future Center Secret Data		
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Title: GBE LAN PHY

Size	Document Number	Rev
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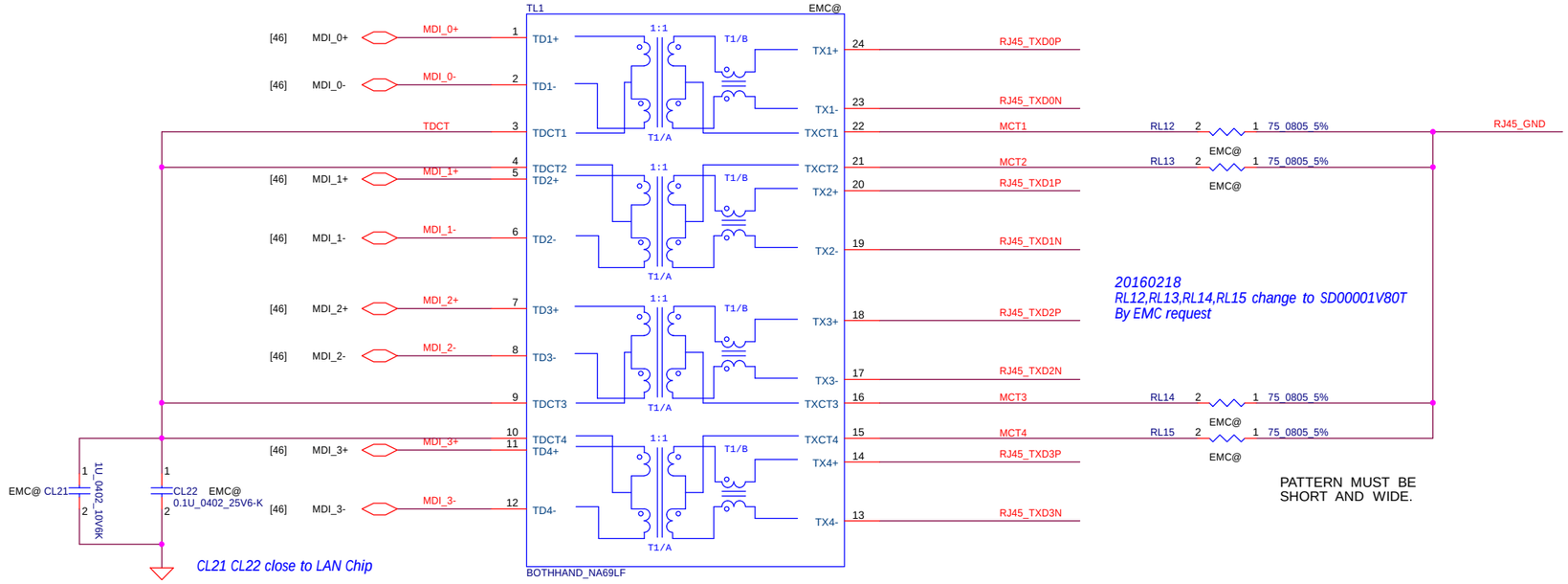
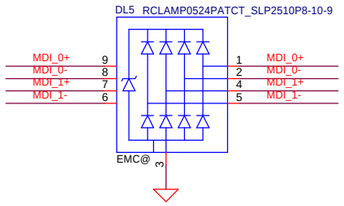
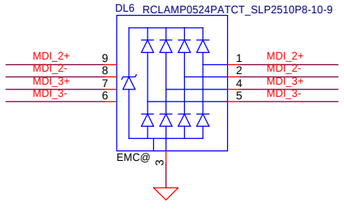
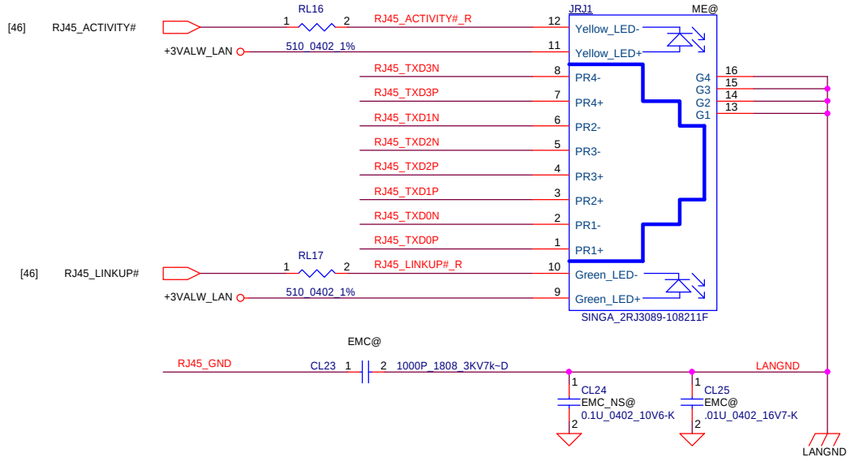






RJ-45 Conn.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: RJ45 CONN

Size	Document Number	Rev
Custom	KENOBI	2.0

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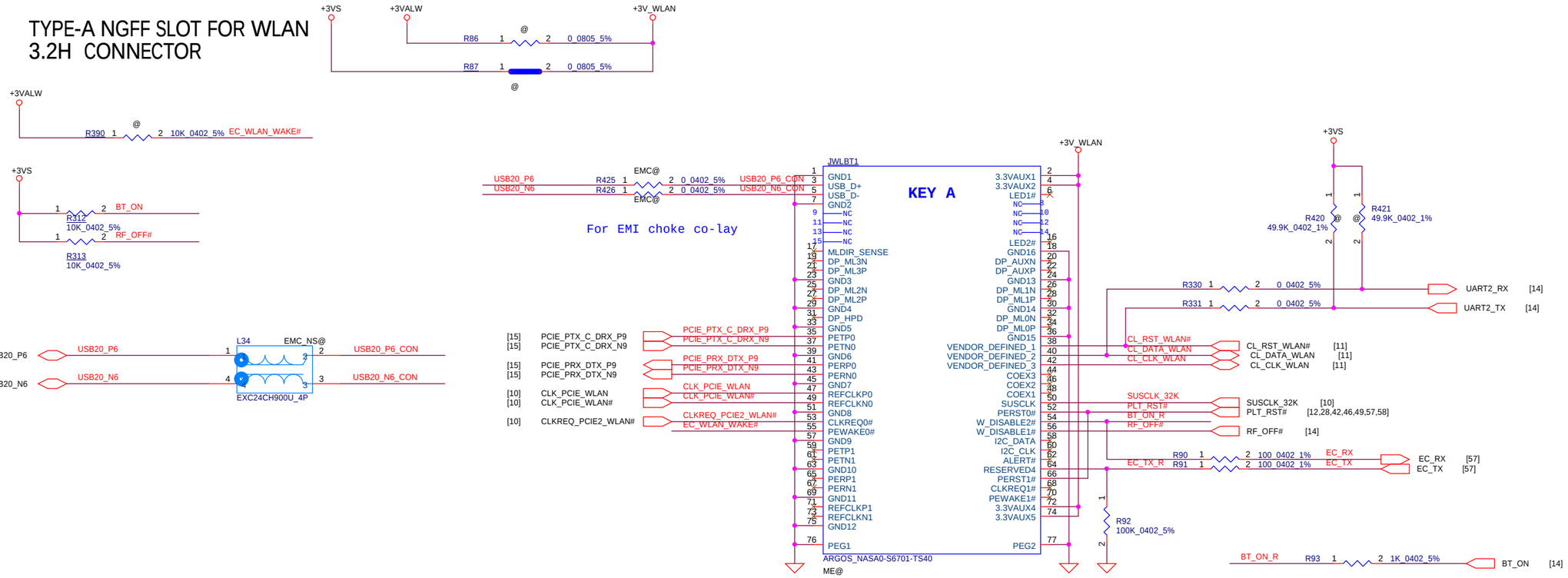
TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title	WWAN/WLAN NGFF CONN.		
Size: Custom	Document Number: KENOBI		Rev: 2.0
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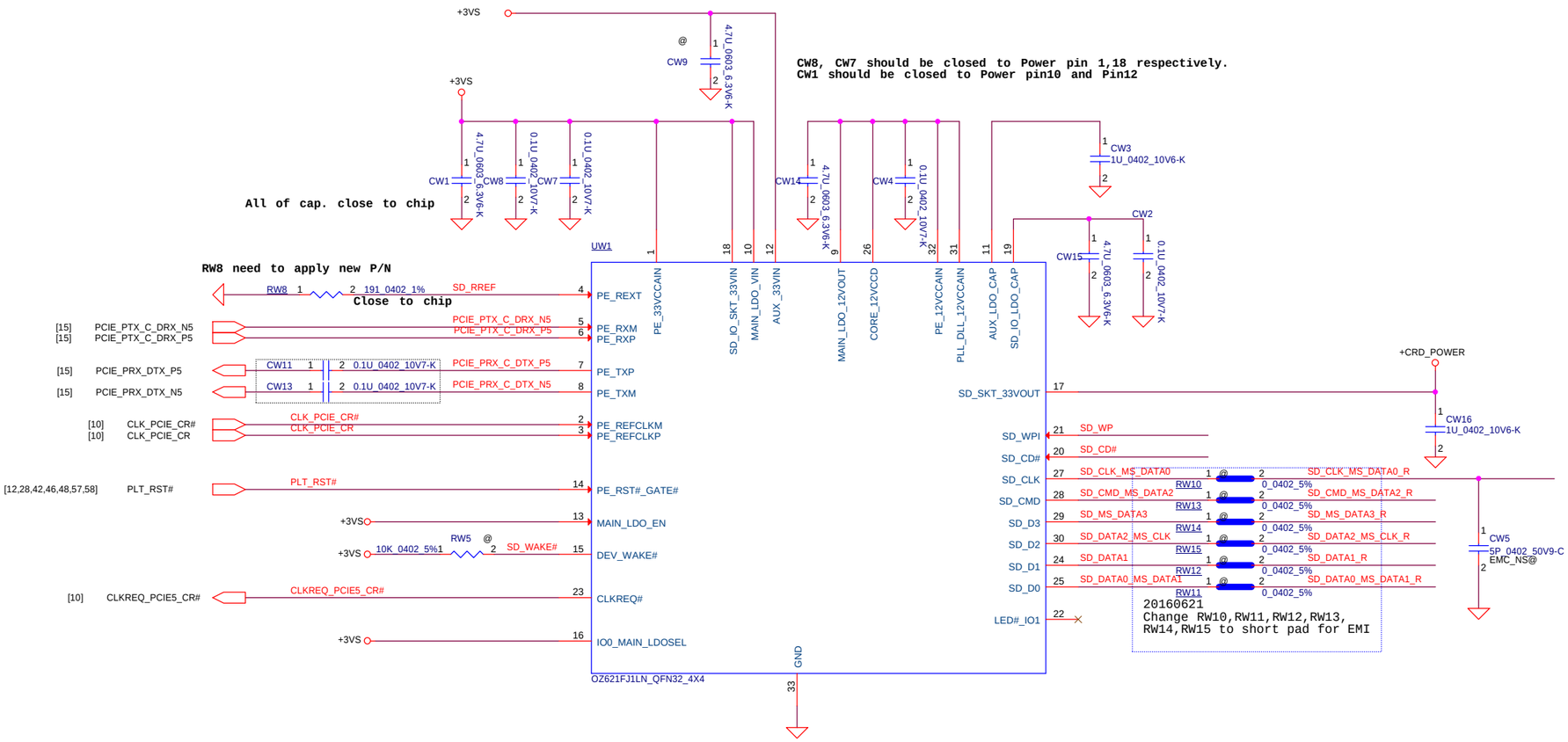

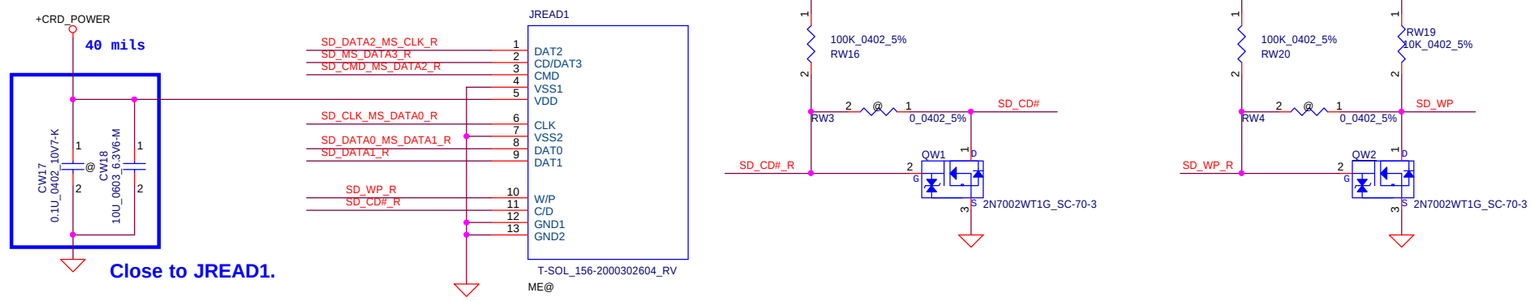

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **Card Reader**

Size	Document Number	Rev
Custom	KENOBI	2.0

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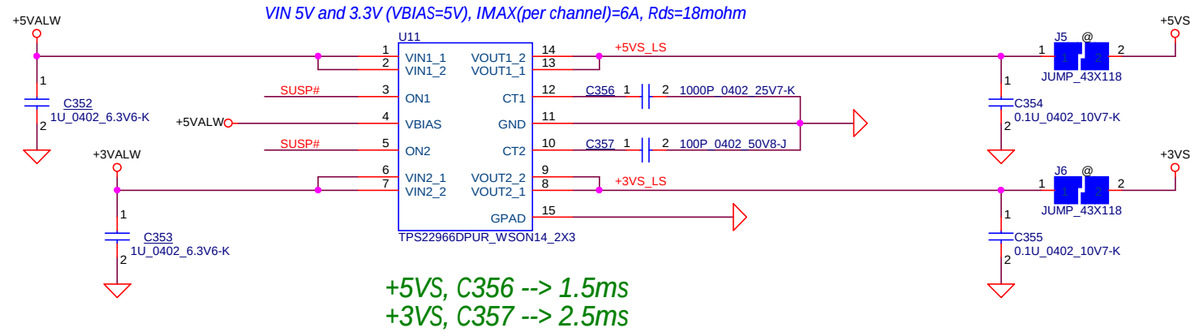
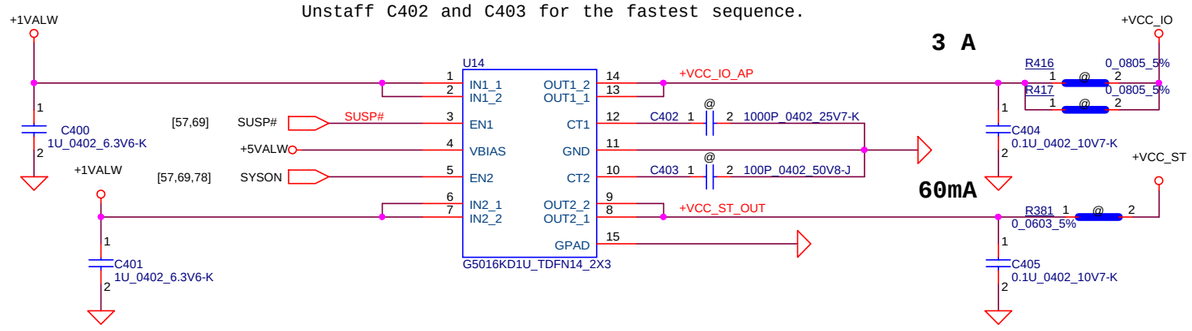
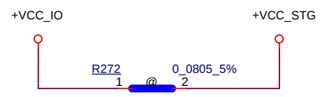
Load Switch
+5VALW To +5VS
+3VALW To +3VS



+1VALW to +VCC_IO_AP & +VCC_ST

Unstaff C402 and C403 for the fastest sequence.





Slew Rate=10uS<TR<65us

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: *DC V TO VS/ V-PCH/VM*

Size	Document Number	Rev
Custom	*KENOBI*	2.0

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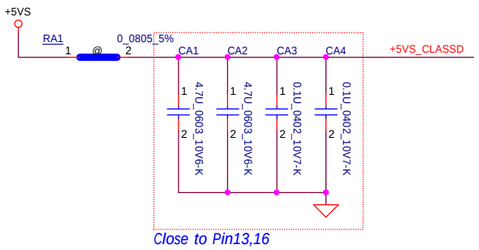
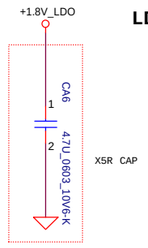
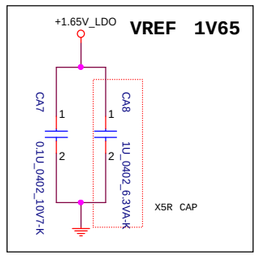
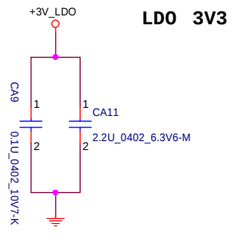
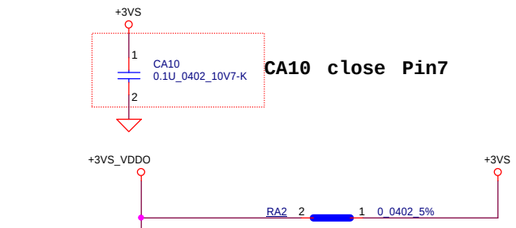
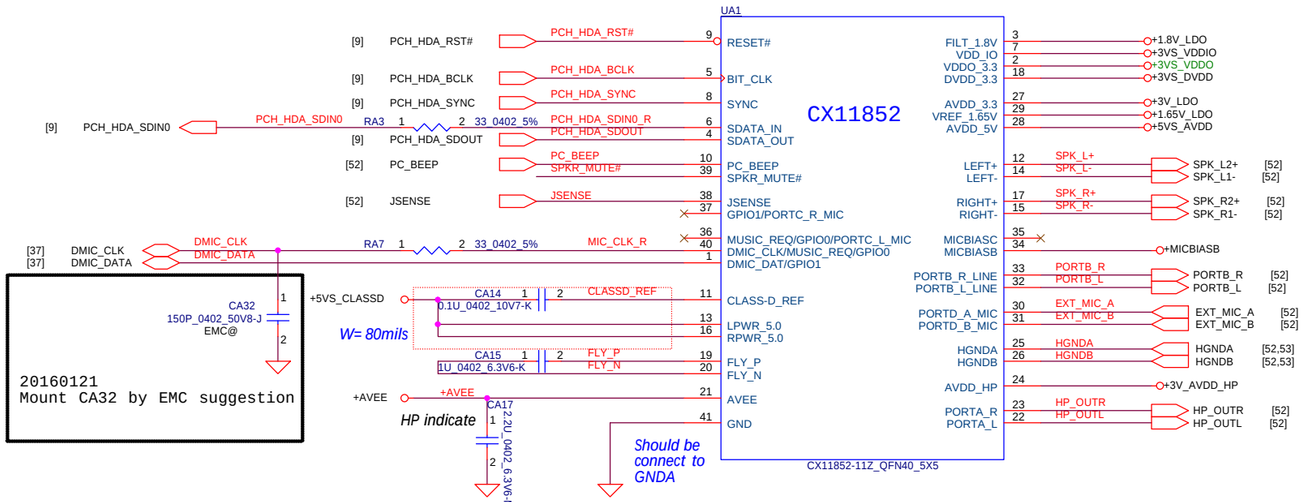


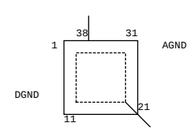




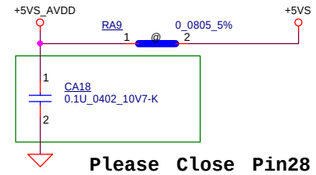


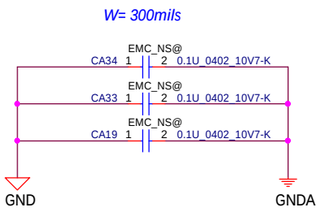


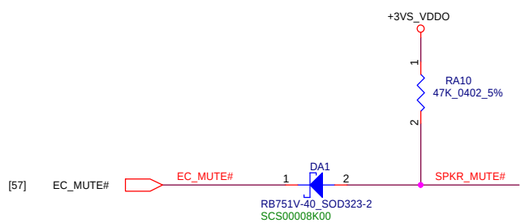


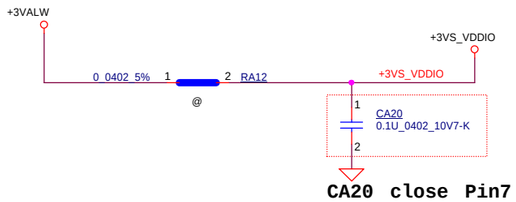


Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA









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Title: **Audio Codec**

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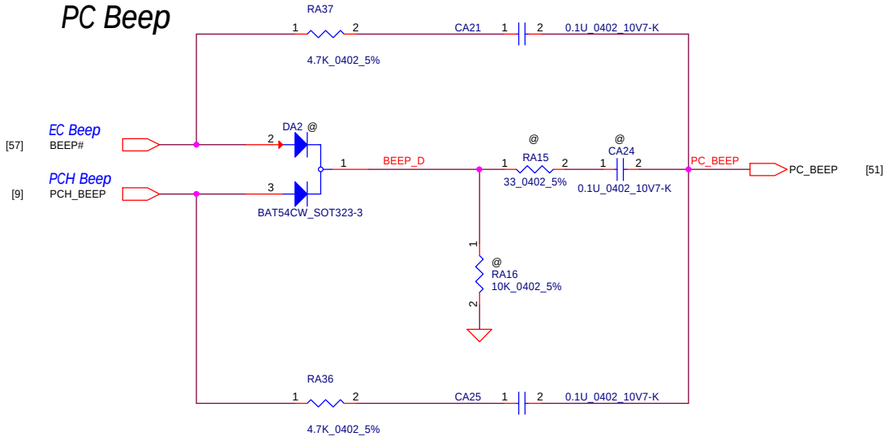
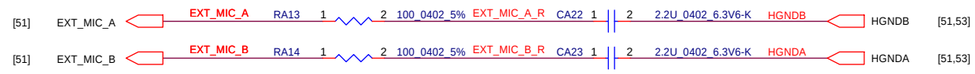
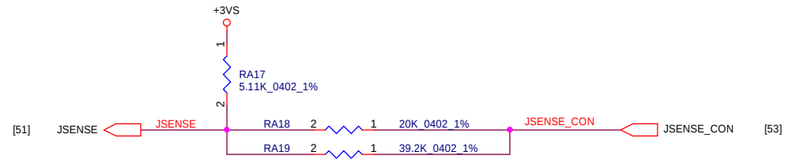
PC Beep



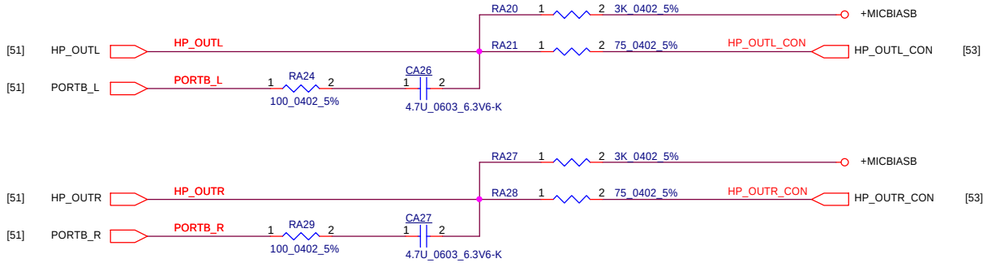
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA





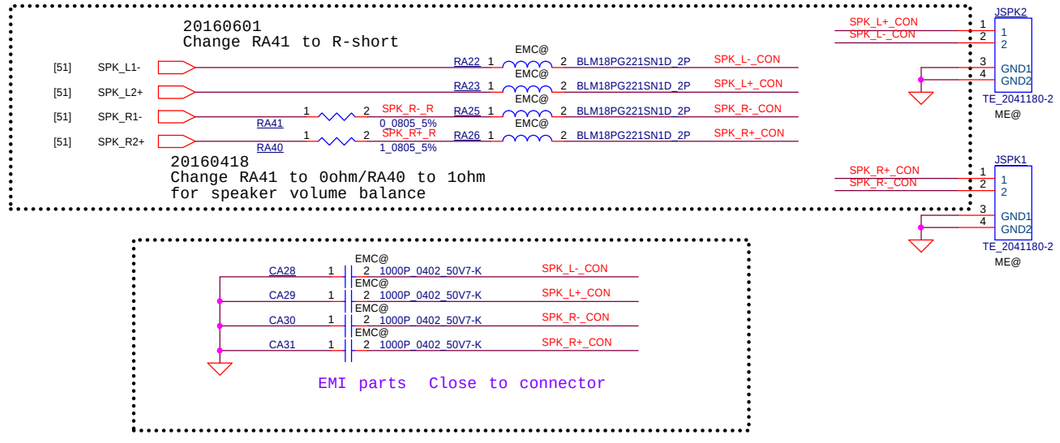
HeadPhone/LINE OUT



Speaker OUT

Need Lenght Match

SPK CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **HP/MIC JACK/Speaker**

Size	Document Number	Rev
Custom	KENOBI	2.0

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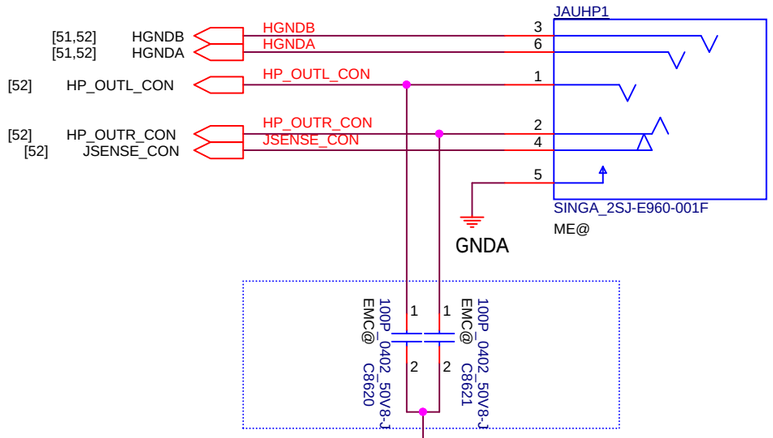
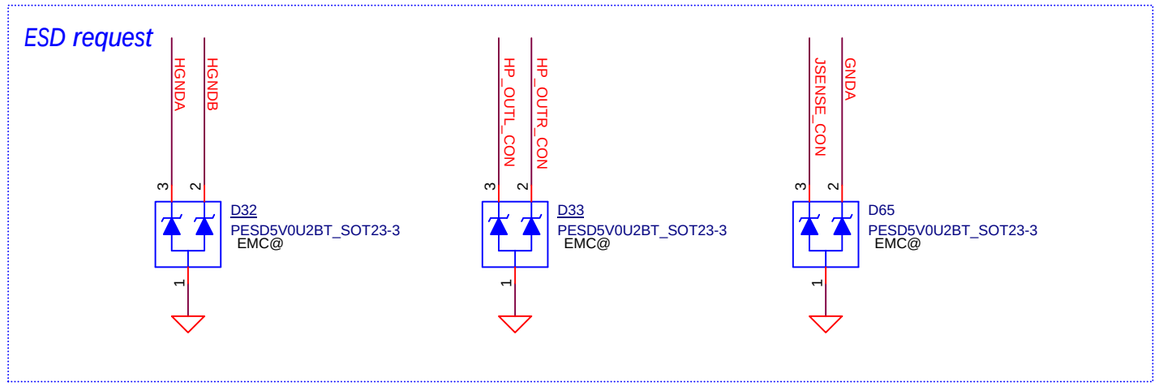
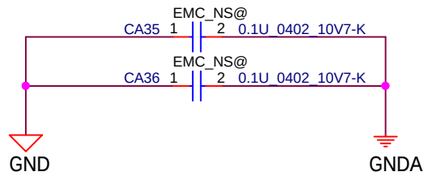


Vendor suggestion. Reserve for EMI.
Close to JAUHP.





Security Classification	LC Future Center Secret Data		
Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title: **AUDIO JACK**

Size	Document Number	Rev
B	KENOBI	2.0

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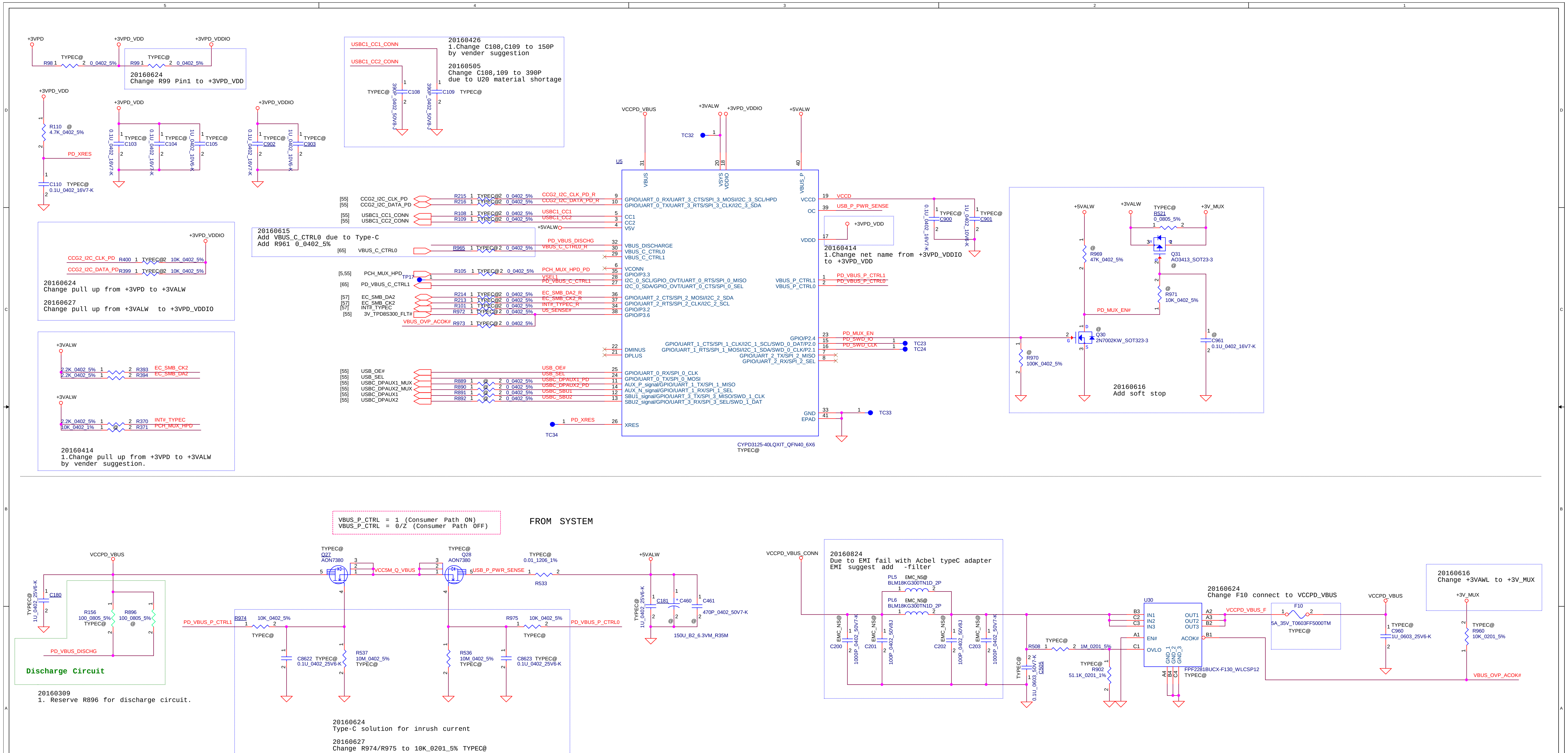
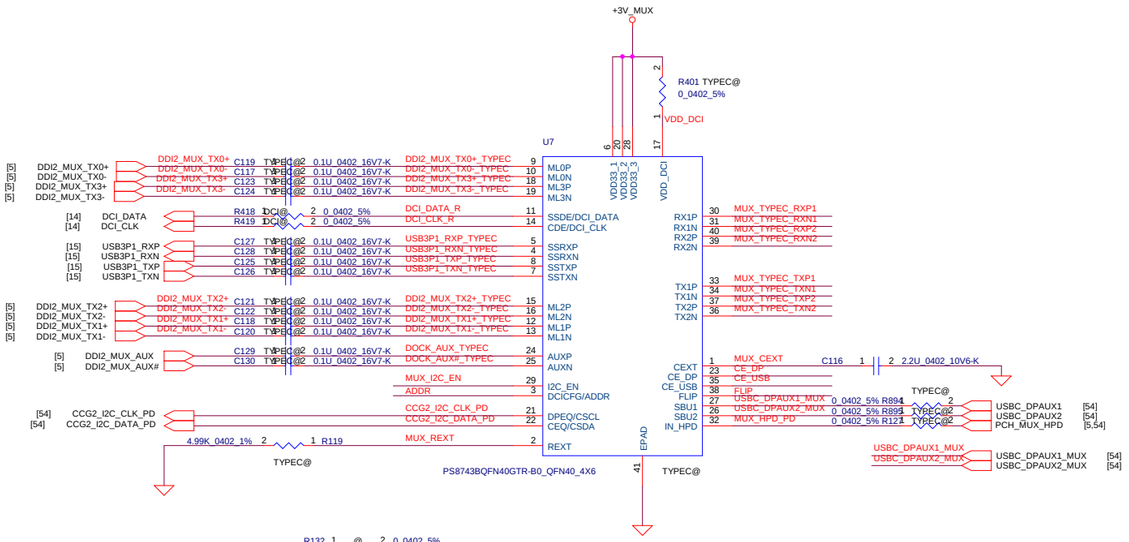
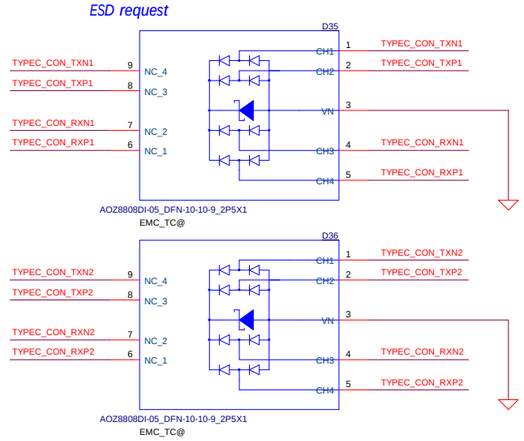


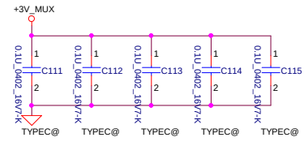
Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

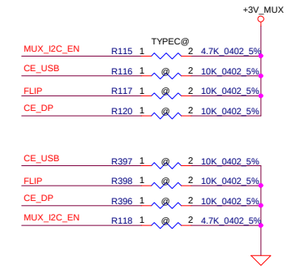
Title: **TYPE-C_Controller**

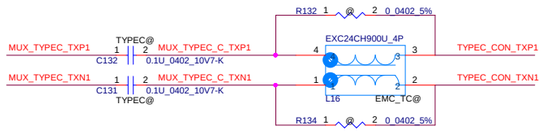
Size: Custom | Document Number: KENOBI | Rev: 2.0

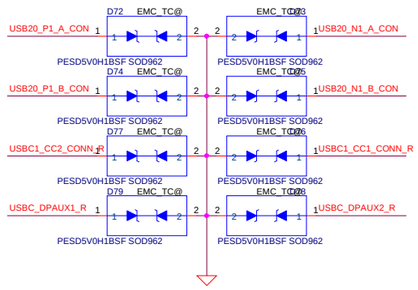


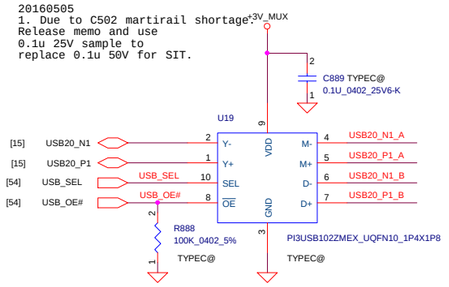


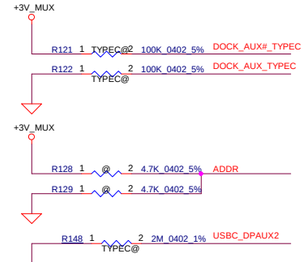


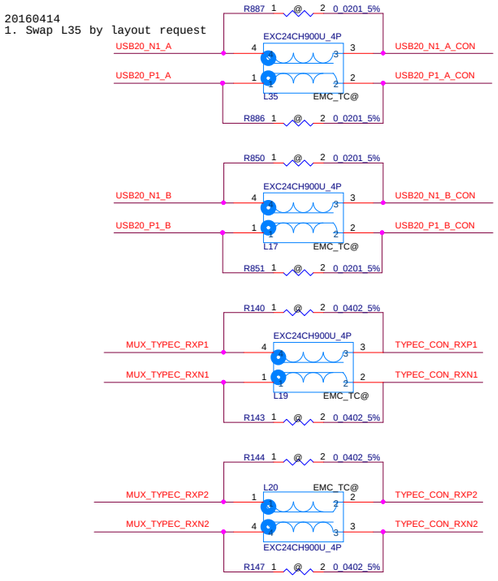


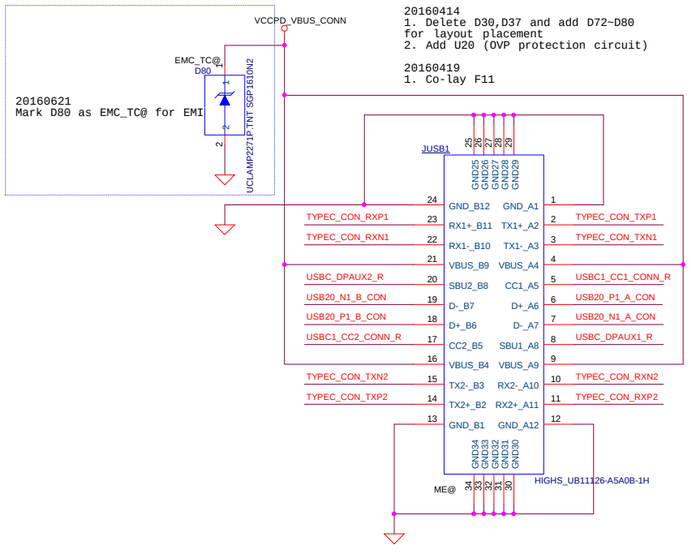


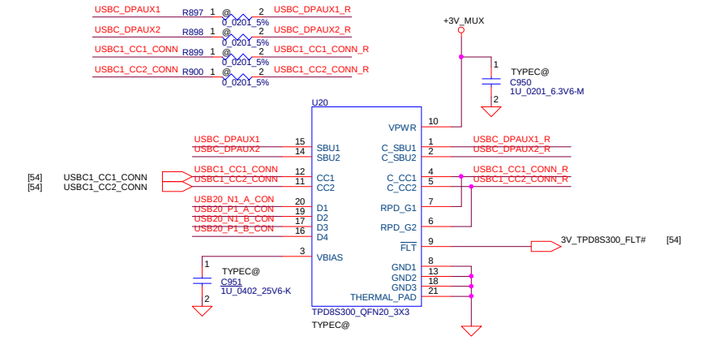












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Title: TYPE-C_MUX

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Issued Date	2015/10/5	Deciphered Date	2016/12/31

Title

DOCKING/ DCIN CONN

Size	Document Number	Rev
Custom	***KENOBI***	2.0
Date: Thursday, August 25, 2016	Sheet 56 of 82	

20160127
1. Add TEMBER_DETECT# circuit
2. Change Resistor value

20160307
Stuff CE11 for WRST singal

20160419
Change RE2 to 18K
for SIT board ID

Vcc	3.3V +/- 5%				
RE1	100K +/- 1%				
Board ID	RE2	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

All capacitors close to EC

Close to EC

minimum trace width 12 mil

IT8586E/AX
LQFP-128

IT8586E-AX_LQFP128_14X14
SA00005W940

IT8586E/FX LQFP

Un-stuff if not necessary.

Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)

1. Version CX : Don't Support Mirror Code
   Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
   "H" --> Enable
   "L" --> Disable (Default)
*

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Title: EC

Size: A2 | Document Number: KENOBI | Rev: 2.0

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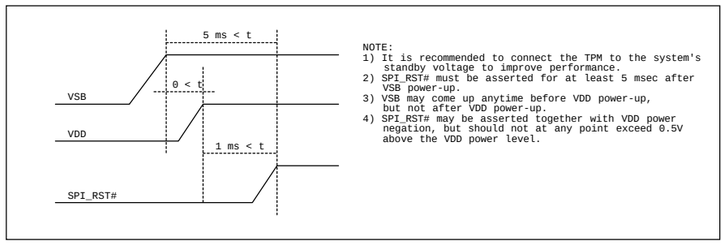
TPM IC

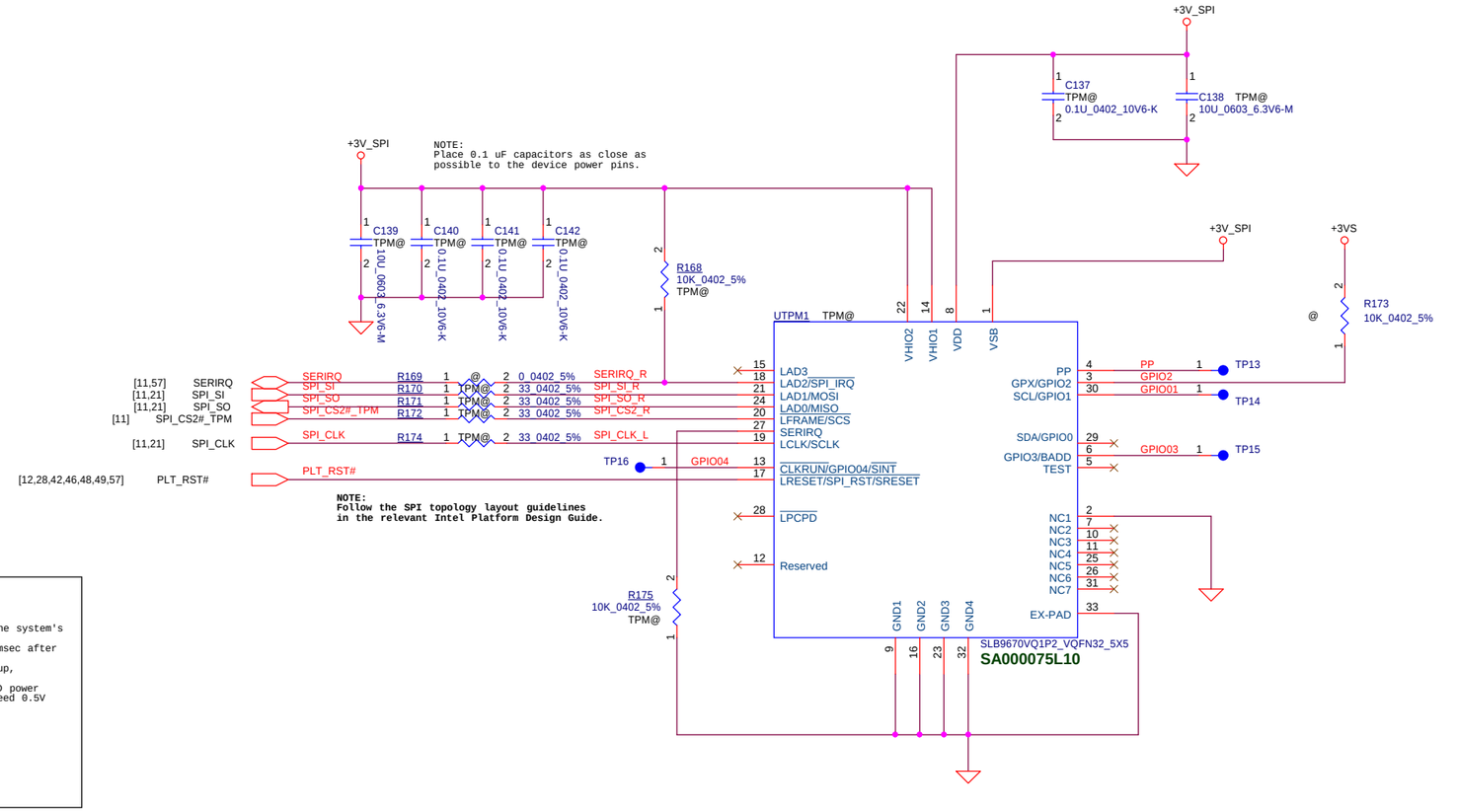
TABLE

Pin No	TCG PTP Spec (x38)	Infineon SLB9670VQ1.2 FW 6.10	ST Micro ST33HTPM2E32AAB9	Nuvoton NPCT650LB0YX
1	VDD	VDD	NC	VSB
2	GND	GND	GND	NC
3	GPIO	NC	NC	GPX/GPIO2
4	GPIO	NC	PP	PP
5	NC	NC	NC	TEST
6	VNC/GPIO	GPIO	NC	GPIO3
7	GPIO/VDD	PP	GPIO	NC
8	VDD	VDD	NC	VDD
9	GND	GND	NC	GND
10	VNC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	Reserved
13	VNC/GPIO	NC	NC	GPIO4
14	VDD	NC	NC	VDD
15	NC	NC	NC	DNC
16	GND	NC	NC	GND
17	SPI_RST#	RST#	SPI_RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK
20	SPI_CS#	CS#	SPI_CS#	SCS#
21	MOSI	MOSI	MOSI	MOSI
22	VDD	VDD	VPS	VDD
23	GND	GND	NC	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	(SERIRQ)
28	NC	NC	NC	DNC
29	VNC/GPIO	NC	NC	GPIO0
30	VNC/GPIO	NC	NC	GPIO1
31	VNC	NC	NC	NC
32	GND	GND	NC	GND

Follow THP1_SWG_SIT_EC005, update TPM table

NOTE:
Check timing sequence in SDV phase.





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: TPM

Size	Document Number	Rev
Custom	KENOBI	2.0

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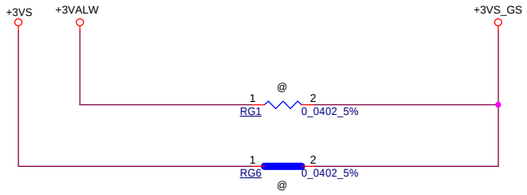


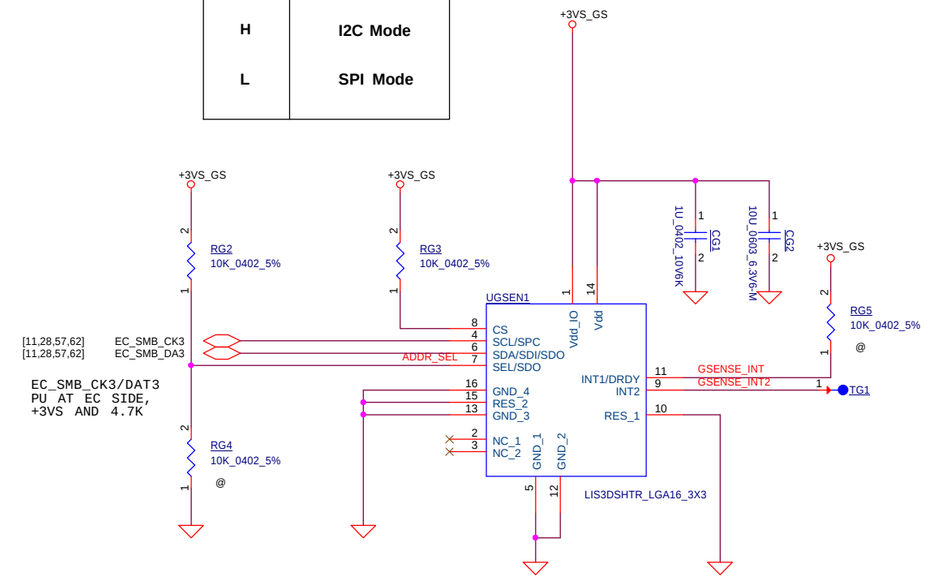
APS G-Sensor

TABLE

P/N	ADDR_SEL	Address
LIS3DSHTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: G SENSOR

Size: Custom | Document Number: KENOBI | Rev: 2.0

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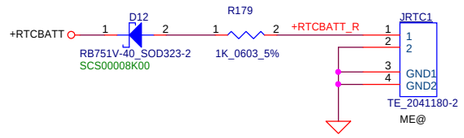
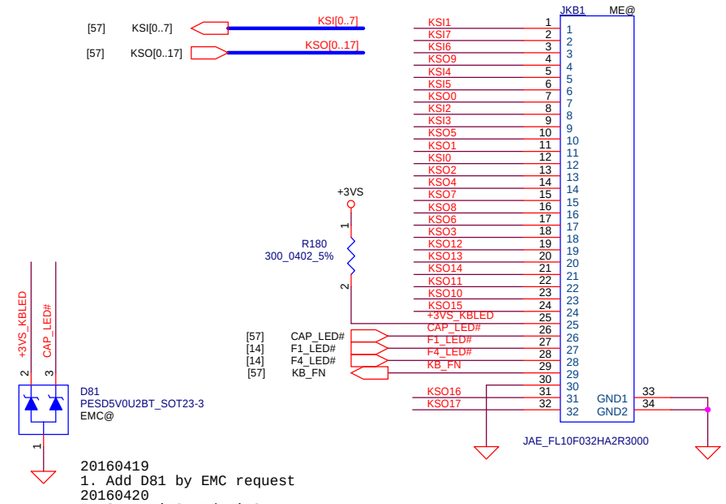
RTC CONN.



KB CONN




```
20160419
1. Add D81 by EMC request
20160420
1. Swap pin2 and pin3
```

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: **KB/RTC/TOUCH PAN CONN.**

Size	Document Number	Rev
Custom	KENOBI	2.0

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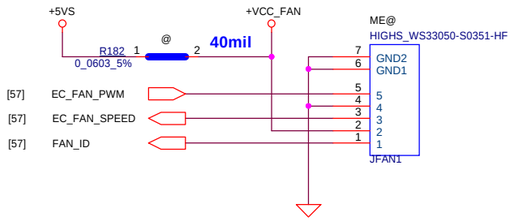
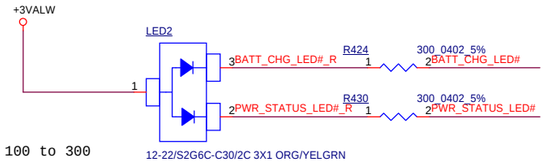
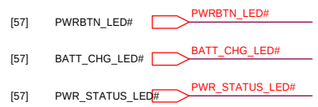
FAN CONN.

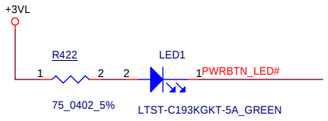


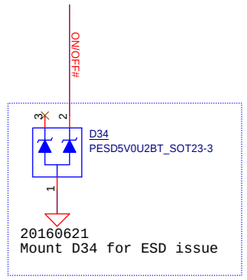
PWR BTN

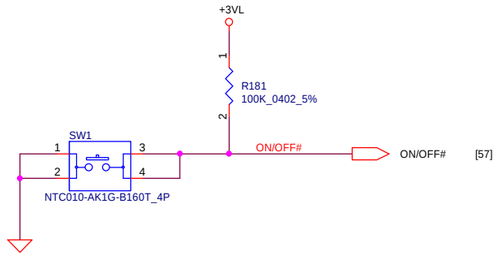




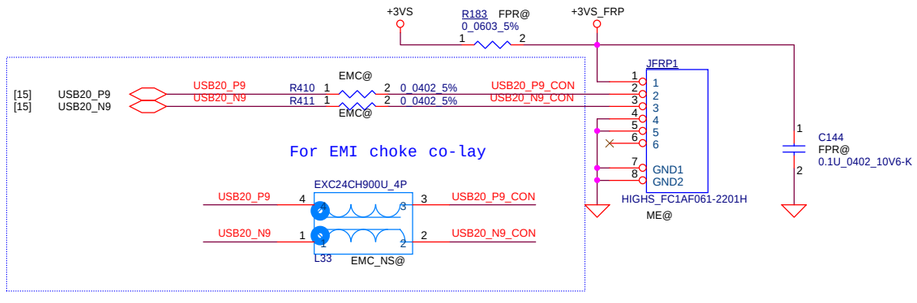
20160424
1. Change R430/R423 from 100 to 300 ohm for LED brightness
2. Change R422 from 100 to 75 ohm for LED brightness

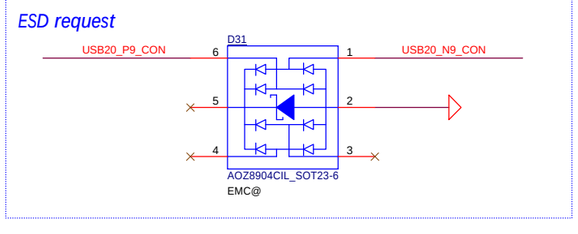




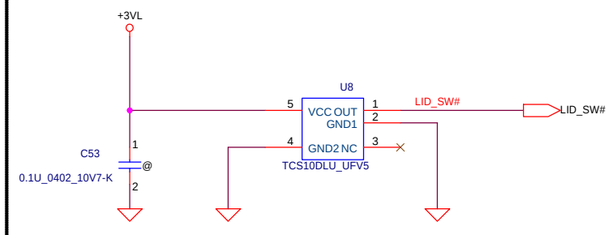


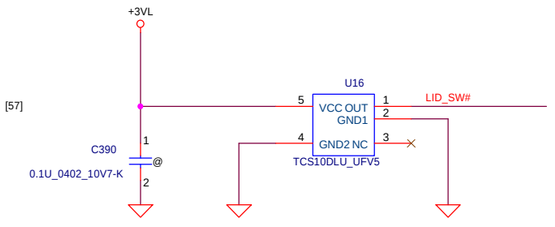
FingerPrint CONN.





Lid Switch





Title: PBTN/LID/FP/FAN CONN.

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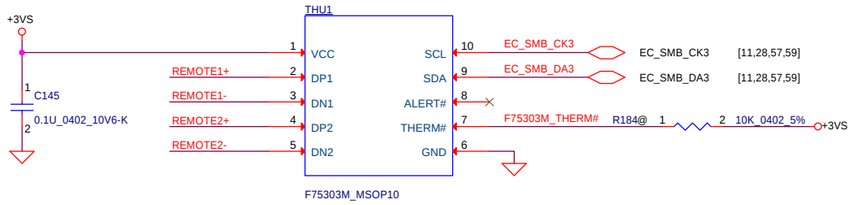
Thermal Sensor
placed near by VRAM

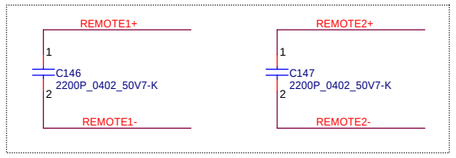


Address 1001_101xb

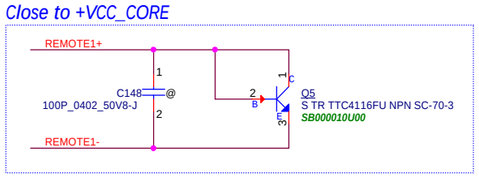
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

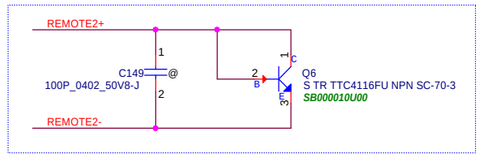
Close to U1

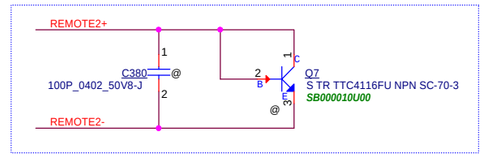


Close to +VCC_CORE



Close JDIMM1&JDIMM2





Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: ***Thermal Sensor***

Size	Document Number	Rev
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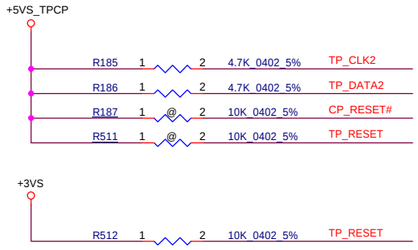
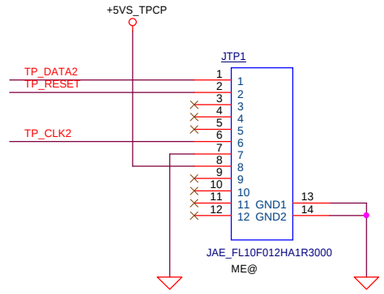
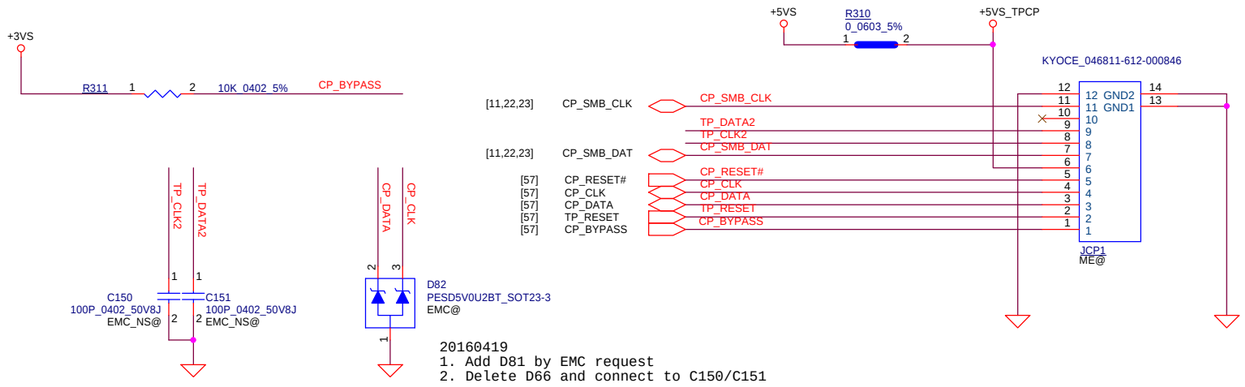


Track point



Click Pad



20160414
1. Change JCP1 foot print

20160419
1. Add D81 by EMC request
2. Delete D66 and connect to C150/C151

Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title: CP/TPOINTCONN.

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Screw Hole

H1 — PAD_CB6P0D3P3
H2 — PAD_CB6P0D3P3
H3 — PAD_CB6P0D3P3
H4 — PAD_CB6P0D3P3
H5 — PAD_C5P0D2P5
H6 — PAD_C6P0D2P5
H7 — PAD_CT5P0B6P0D2P5
H8 — PAD_C6P0D2P5
H9 — PAD_C5P5D2P5X3P0
H10 — PAD_C6P0D2P5X3P0
H11 — PAD_CT5P0B6P0D2P5X3P0
H12 — PAD_C6P0D2P5X3P0
H13 — PAD_C6P0D2P5
H14 — PAD_CT8P0B6P0D2P5
H15 — PAD_CT8P0B5P0D2P5
H16 — PAD_O3P0X2P5D3P0X2P5N

20160419
Change H9/H10/H11/H12 footprint

H17 — PAD_C6P0D3P3
H18 — PAD_CT6P0D3P2
H19 — PAD_CT6P0D3P2
H20 — PAD_CT6P0D3P2
H21 — PAD_C6P0D2P5
H22 — PAD_CT5P0B6P0D2P5
H23 — PAD_SHAPET7P0X10P0CB6P0D2P5
H24 — PAD_SHAPET7P0X10P0CB6P0D2P5

Center Zero

H25 — H_2P5N

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

Title: **P64-PLM/SCREW HOLE**

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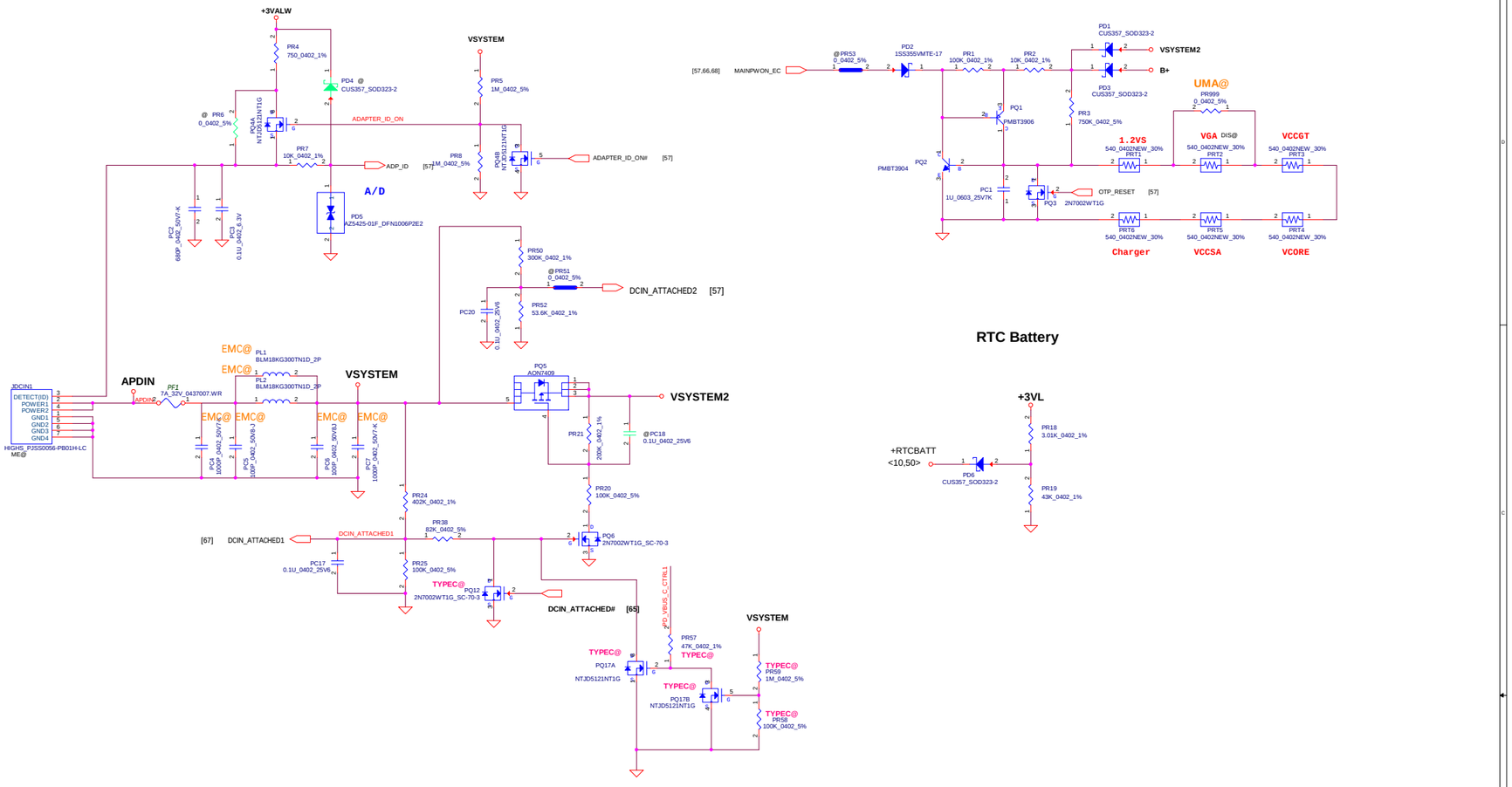

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Title: *DCIN / VIN Detector*

Size	Document Number	Rev
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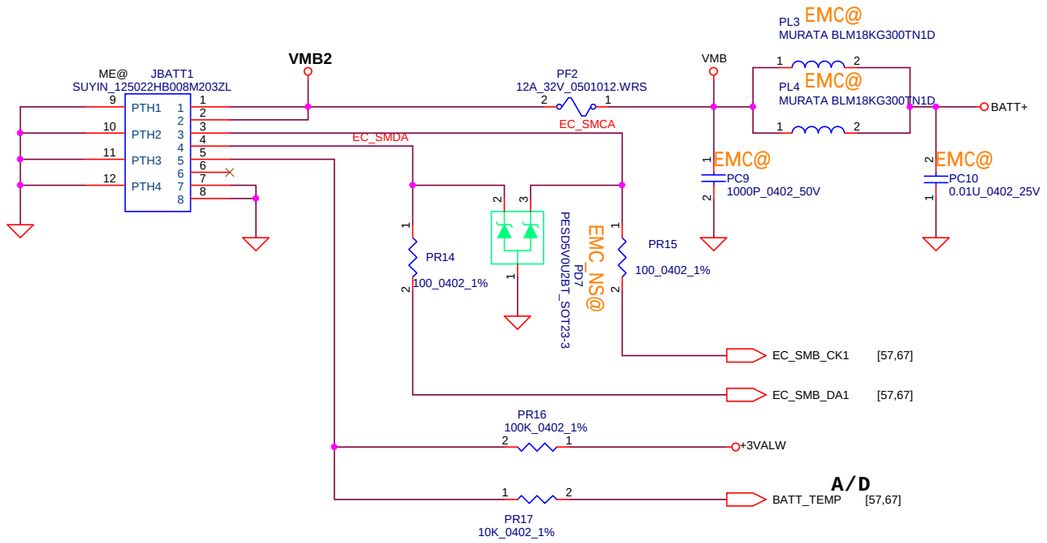
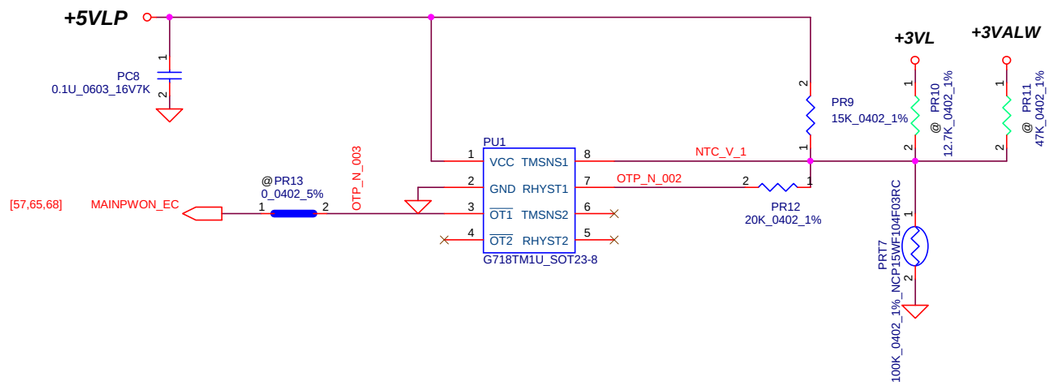


PRT7 under CPU bottom side for CPU thermal protection. This is for thermal team request.



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Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	***BATTERY CONN/OTP***		
Size: Custom	Document Number: ***KENOBI***		Rev: 2.0
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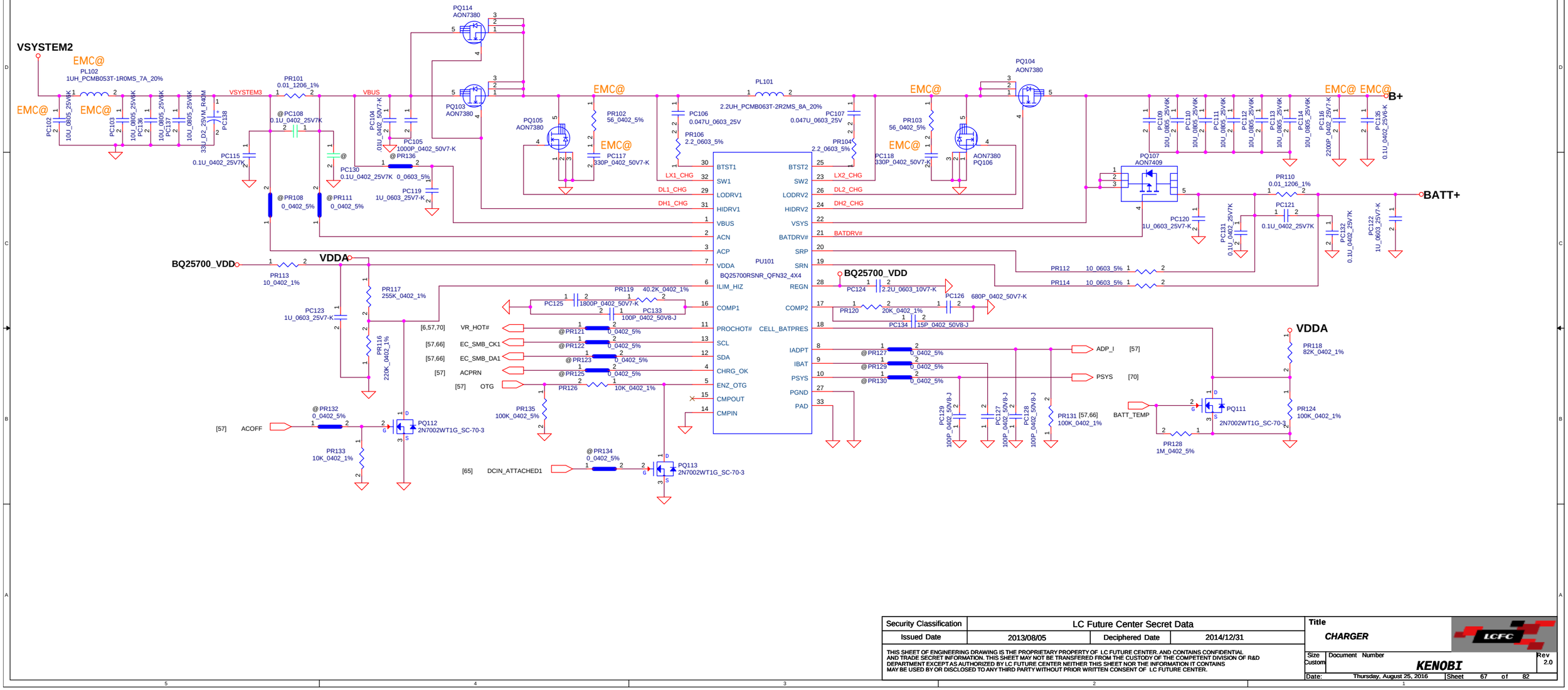

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **CHARGER**

Size	Document Number	Rev
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+3VALW
FSW=750 KHz
TDC:8A
OCP:11A

B+
@ PJ201
JUMP_43X79
EMC@ EMC@ RF_NS@
PC232 2200P_0402_25V7-K
PC201 0.1U_0402_25V6-K
PC230 47P_0402_50V8-J
PC202 10U_0805_25V6-K
PR201 1M_0402_5%
+3V_VIN
PU201
SYX198BQNC_QFN10_3X3
EN2 PG +3V_PWRGD
IN BS +3VBS
GND LX +3VLX
EN1 OUT +3VALW_OUT
FB LDO
3V5V_ON
+3VALW_FB
@ PR202 0_0603_5%
PC203 0.1U_0603_25V7-M
PR203 @ 0_0402_5%
PR205 @ 0_0402_5%
100mA
+3VL
PC208 4.7U_0603_6.3V6-K
PL201 2.2UH_PCMB063T-2R2MS_8A_20%
+3VALW_P
EMC@ EMC@
EMC_NS@
PR204 4.7_0603_5%
EMC_NS@
PC209 680P_0402_50V7K
PC204 22U_0805_6.3V6-M
PC205 22U_0805_6.3V6-M
PC206 22U_0805_6.3V6-M
PC207 22U_0805_6.3V6-M
PC210 2200P_0402_25V7-K
PC211 0.1U_0402_25V6
PJ202 8A
@JUMP_43X118
+3VALW
[57] EC_ON
EC_ON
PR206 2.2K_0402_1%
+3VL
PR217 47K_0402_1%
PR216 47K_0402_1%
@ PC213 0.1U_0402_25V6-K
PR208 1M_0402_5%
PC212 0.01U_0402_25V7-K
PR207 1K_0402_1%
[57,65,66] MAINPWON_EC
NTJD5121NT1G
NTJD5121NT1G
PQ201A
NTJD5121NT1G
PQ201B

+5VALW
FSW=750 KHz
TDC:8A
OCP:11A

B+
@ PJ203
JUMP_43X79
RF_NS@ EMC@ EMC@
PC231 47P_0402_50V8-J
PC233 2200P_0402_25V7-K
PC215 0.1U_0402_25V6-K
PC214 10U_0805_25V6-K
PC216 10U_0805_25V6-K
PU202
SYX198CQNC_QFN10_3X3
IN PG +5V_PWRGD
GND BS +5VBS
VCC LX +5VLX
EN OUT +5VALW_OUT
FB LDO
+5V_VIN
3V5V_ON
+5VFB
PC218 1U_0603_25V6M
+5V_VCC
@ PR209 100K_0402_5%
@ PR210 0_0402_5%
@ PR211 0_0402_5%
@ PR212 0_0603_5%
PC217 0.1U_0603_25V7-M
PR213 @ 0_0402_5%
100mA
+5VLP
PC225 4.7U_0603_6.3V6-K
PL202 2.2UH_PCMB063T-2R2MS_8A_20%
+5VALW_P
EMC@ EMC@
EMC_NS@
PR214 4.7_0603_5%
EMC_NS@
PC226 680P_0402_50V7K
PC219 22U_0805_6.3V6-M
PC220 22U_0805_6.3V6-M
PC221 22U_0805_6.3V6-M
PC222 22U_0805_6.3V6-M
PC223 22U_0805_6.3V6-M
PC224 22U_0805_6.3V6-M
PC227 2200P_0402_25V7-K
PC228 0.1U_0402_25V6
PJ204 8A
@JUMP_43X118
+5VALW
PC229 6800P_0402_25V7-K
PR215 1K_0402_1%

6800pf soft start 2ms
47nf soft start 7ms

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Title: **3VALWP/5VALWP**

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1.2V
TDC: 12A
OCP: 15A
Fsw: 300KHz

+0.6VS
TDC: 1.5A

B+ PJ304 @JUMP_43X79 B+_1.2V
PC302 10U_0805_25V6-K
PC303 10U_0805_25V6-K
PC304 0.1U_0402_25V6
PC307 2200P_0402_25V
PC305 47P_0402_50V8-J
PC306 68P_0402_50V8J
EMC@ EMC@ RF_NS@ RF_NS@

PJ301 @JUMP_43X118
PJ302 @JUMP_43X118
+1.2VP → +1.2V
PJ303 @JUMP_43X39
+0.6VSP → +0.6VS

PC301 10U_0603_6.3V6M
+1.2VP

PR301 100K_0402_1%
PR302 255K_0402_1%
+1.2VP +0.6VSP
+0.6VSP
PC308 10U_0603_6.3V6M
PC309 0.1U_0402_6.3V7-K

PQ301 AON7408L
PR303 2.2_0603_5%
PC310 0.22U_0603_25V7K
DH_1.2V

PL301 1UH_PCMC063T-1R0MN_+-20%
LX_1.2V
DL_1.2V

PU301 RT8231AGQW
PGND VID CS VLDOIN VTT PAD VTTGND VTTSNS GND VTTREF VDD PGOOD
BOOT UGATE PHASE LGATE VDDQ FB TON S5 S3

+1.2VP EMC@ EMC@
PC312 2200P_0402_25V7-K
PC313 0.1U_0402_25V6
PC311 330U_D2_2V_R9M
PC314 @ 470P_0402_50V7K
PR305 6.04K_0402_1%
PR307 10K_0402_1%
EMC_NS@ PR304 4.7_0603_5%
EMC_NS@ PC317 680P_0402_50V7K

PQ302 AON7380

VTTREF_0.6V
PR306 5.1_0603_5%
+5VALW
PC315 0.033U_0402_16V7K
PC316 1U_0402_10VA-K

@PR308 100K_0402_1% +3VS
PR310 @0_0402_5% SM_PG_CTRL [7]
@PR311 0_0402_5% SUSP# [50,57]
@PC318 0.1U_0402_6.3V7-K

PR309 887K_0402_1% TON_1.2V
S5_1.2V
S3_1.2V
FB_1.2V
B+_1.2V

[50,57,78] SYSON
@PR312 0_0402_5%
@PR313 47K_0402_5%
@PC319 0.1U_0402_16V

Title	+1.2V/+0.6VS	
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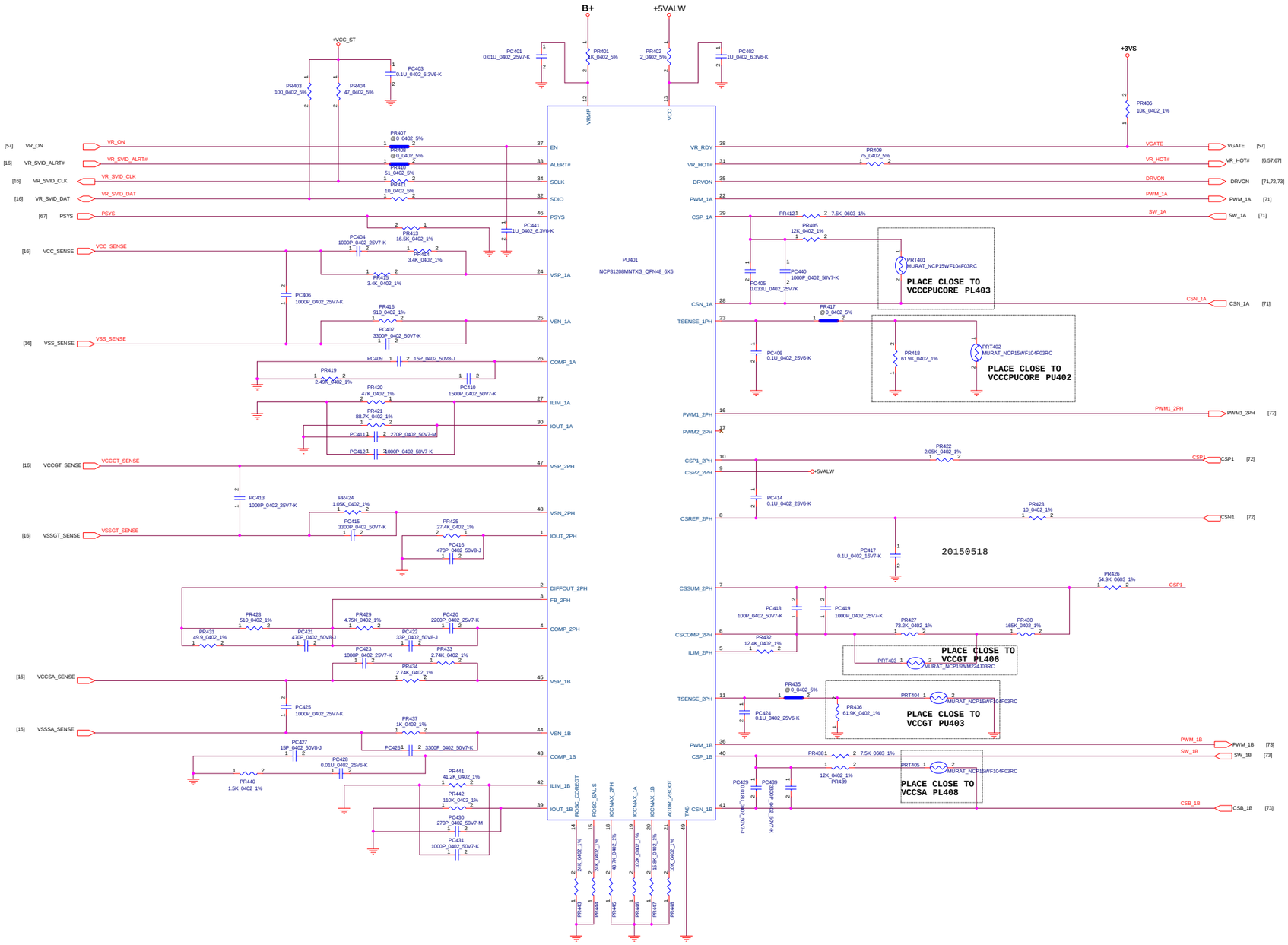

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Size	Document Number		Rev
D	KENOBI		2.0
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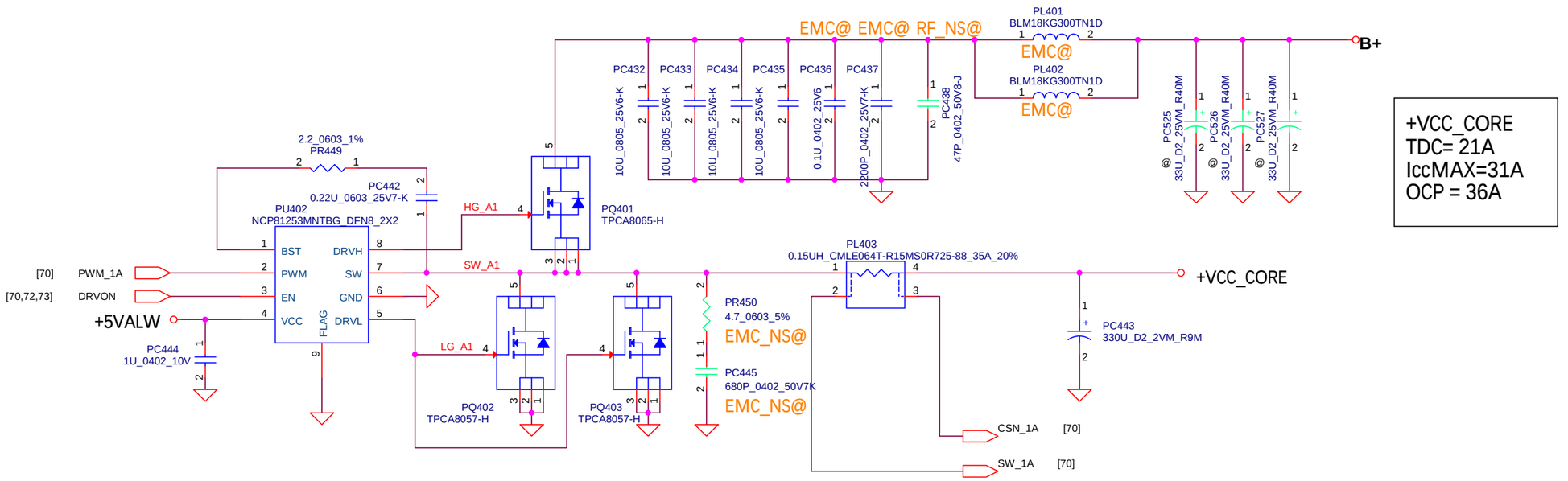

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_CORE*

Size	Document Number	Rev
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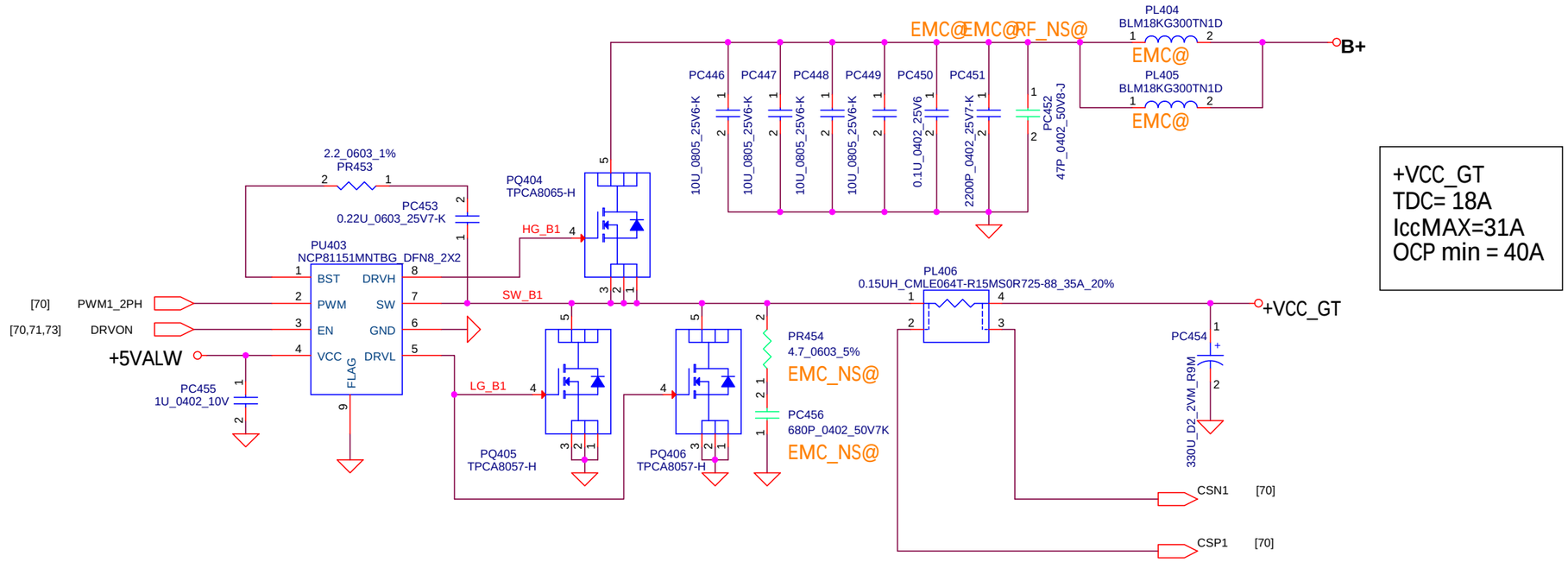

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+VCC_GT*

Size	Document Number	Rev
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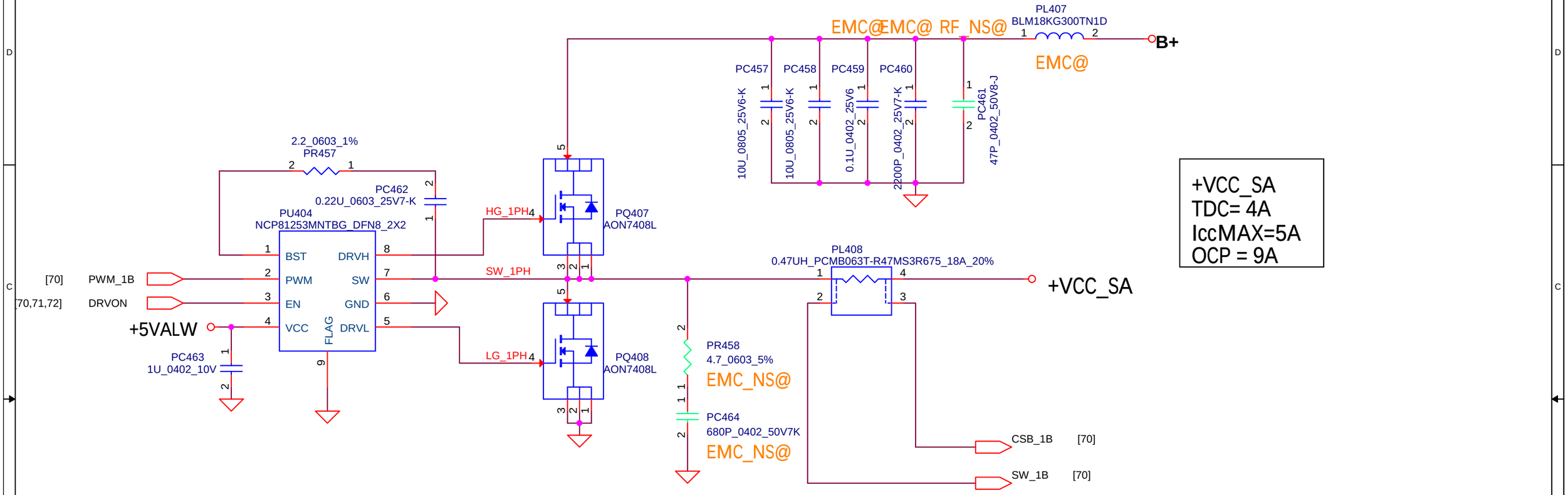

Title			
+VCC_SA			
Size: Custom	Document Number: KENOBI		Rev: 2.0
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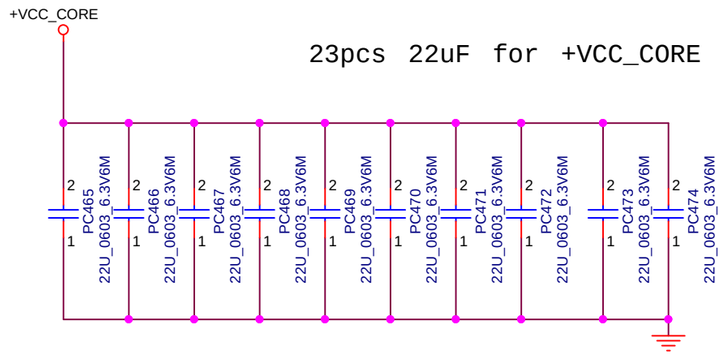
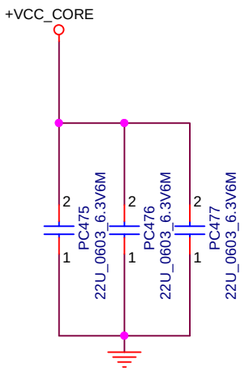
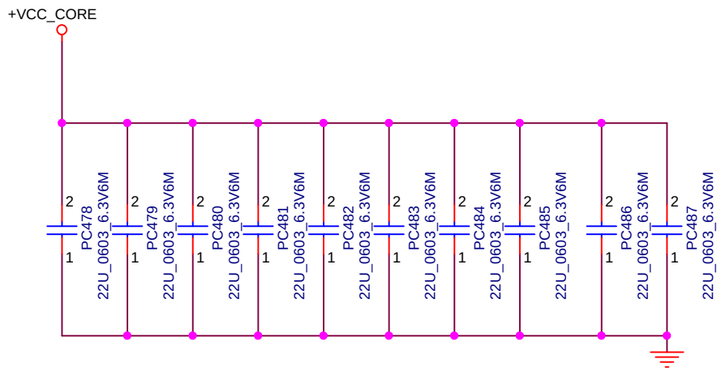
Based on PDDG rev 0.7 Table 5-1.

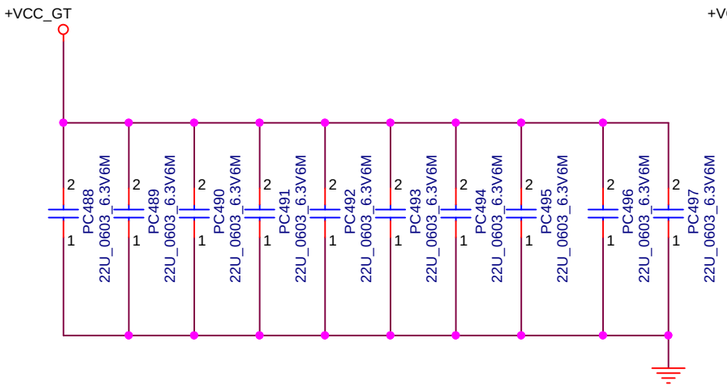
23pcs 22uF for +VCC_CORE

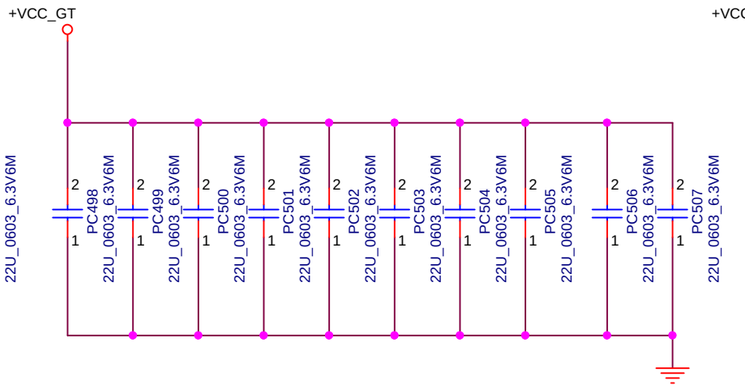


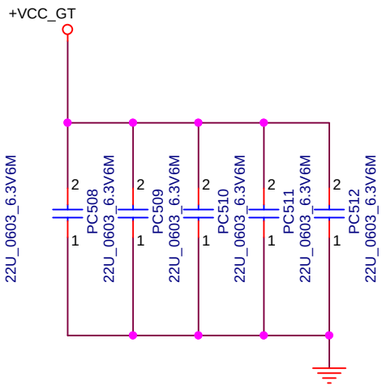




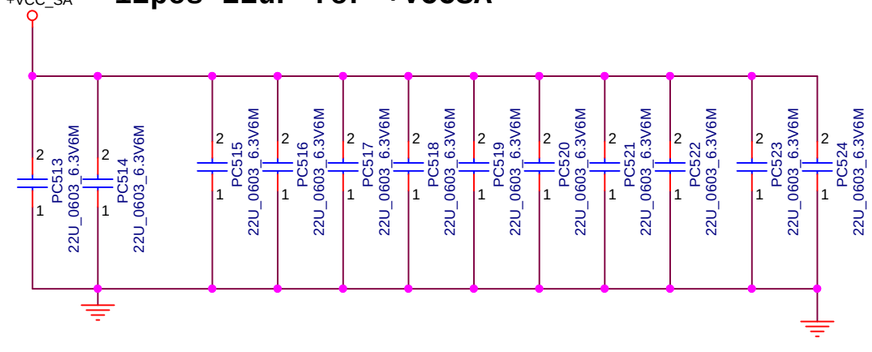
25pcs 22uF for +VCC_GT







12pcs 22uF for +VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

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B	KENOBI	2.0

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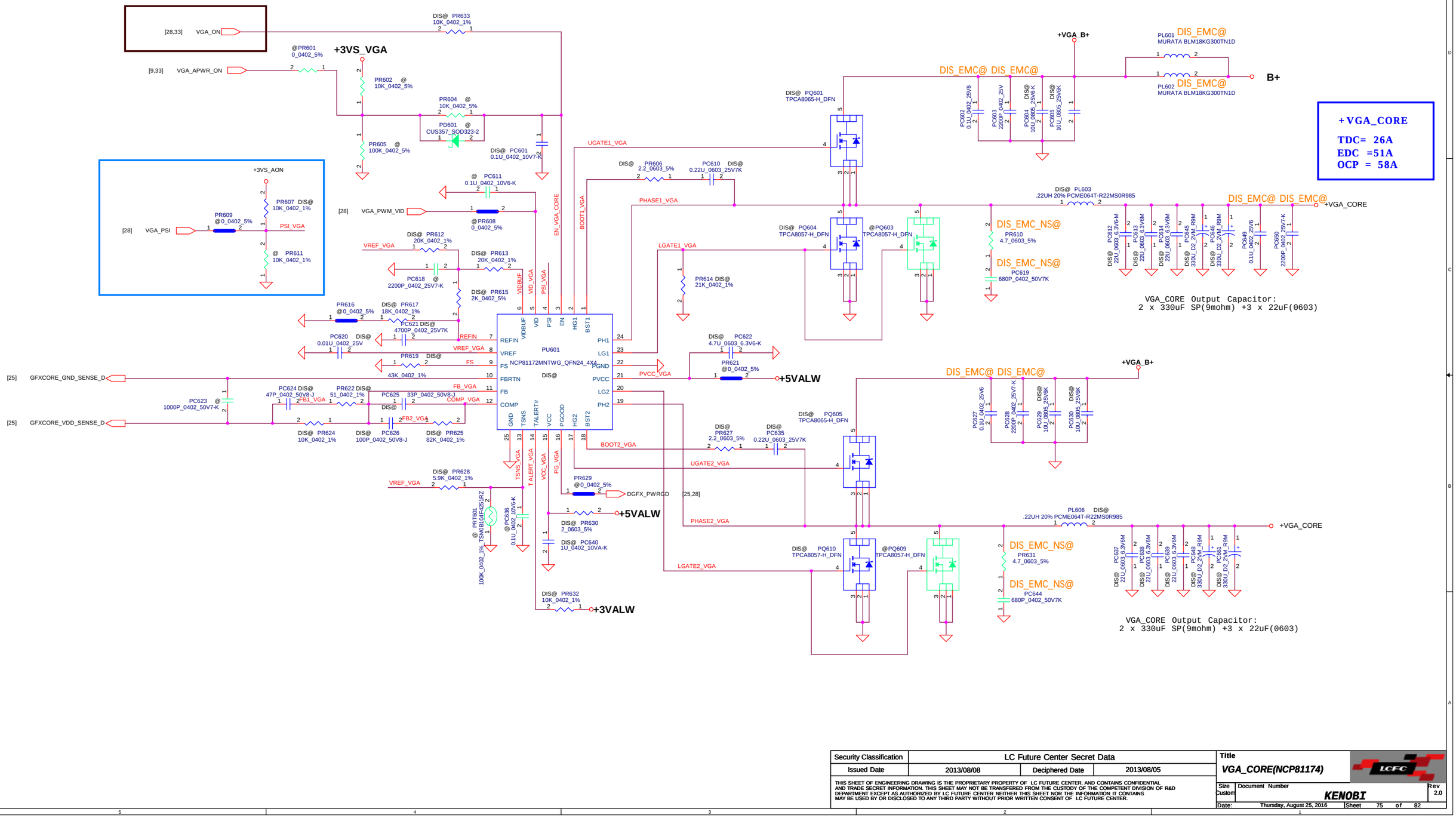

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	VGA_CORE(NCP81174)		
Size	Document Number		Rev
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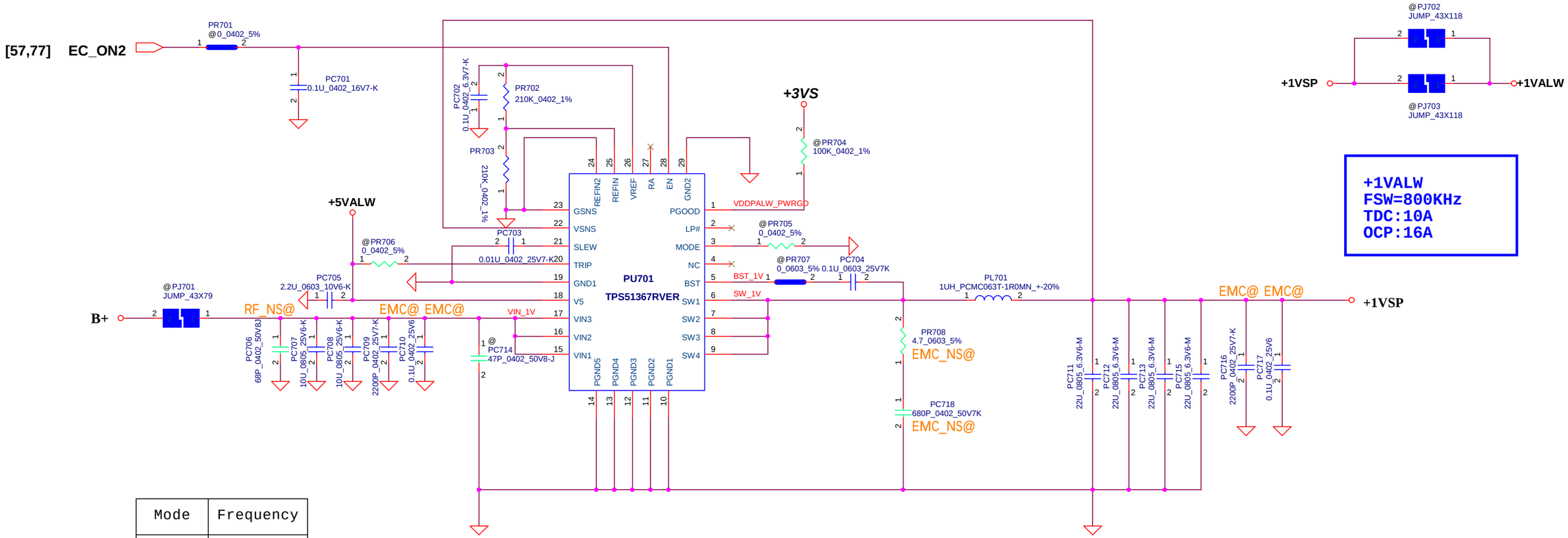

Mode	Frequency
GND	400KHz
Float	800KHz

Title	+1VALW		
Size: Custom	Document Number: KENOBI		Rev: 2.0
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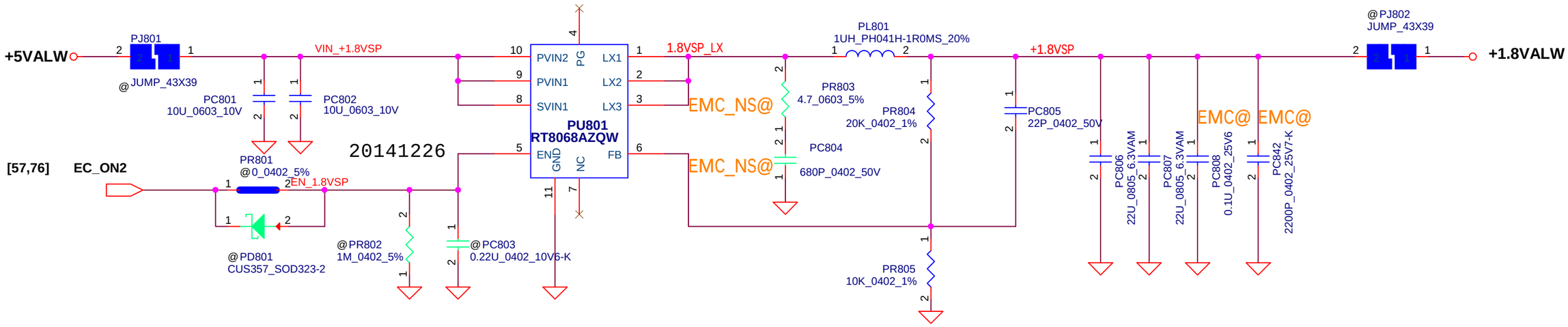
+1.8VALW
TDC: 1A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	*+1.8VALW*		
Size: Custom	Document Number: ***KENOBI***		Rev: 2.0
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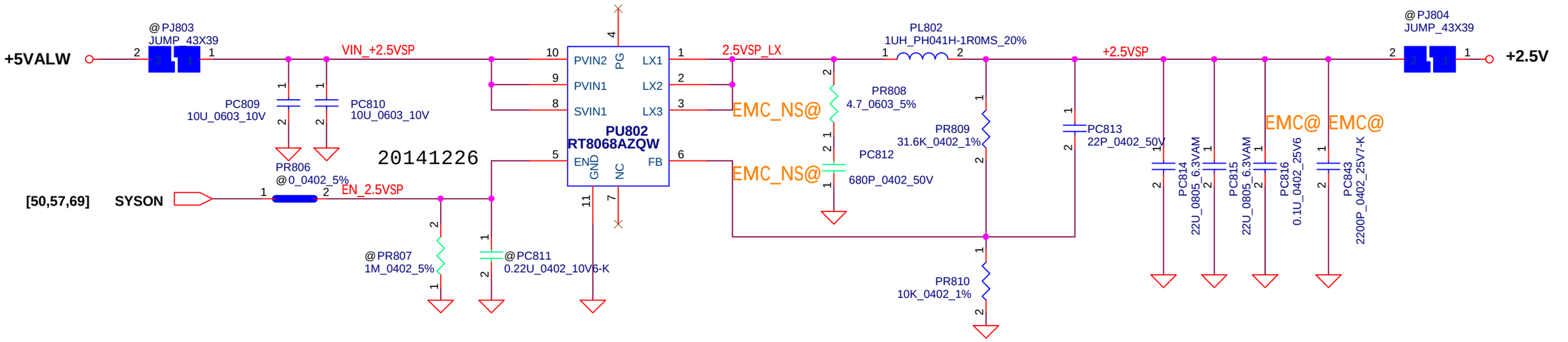
+2.5V
TDC: 2A
Fsw: 1MHz



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+2.5V		
Size	Document Number		Rev
Custom	KENOBI		2.0
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+1.5VS_VGA
TDC: 6.8A
OCP: 12A
Fsw: 650KHz

@PD802
CUS357_SOD323-2

DIS@ PR811
100K_0402_1%

[28] FB_PWR_EN

DIS@
PR812
200K_0402_1%

DIS@
PC817
0.1U_0402_16V

B+

PJ805
@JUMP_43X79

DIS@ DIS_EMC@ DIS_EMC@

PC818 10U_0805_25V
PC819 0.1U_0402_25V
PC844 2200P_0402_25V7-K

PU803
SYX198DQNC
IN, EN, BS, GND, LX, ILMT, FB, BYP, PG, LDO

BS_1.5VSP
SW_1.5VSP
FB_1.5VSP
+3VALW

+3VS

@ PR814
0_0402_5%

@ PR815
100K_0402_1%

@ PR816
0_0402_5%

PR827
@0_0402_5%

[25] VDDQPWRGD

DIS@
PC820 4.7U_0402_6.3V6-M
PC821 4.7U_0402_6.3V6-M

@PR813
0_0603_5%

DIS@
PC822
0.1U_0603_25V7K

DIS@ PL803
1UH_PCMC063T-1R0MN_+-20%

PR820
4.7_0603_5%

DIS_EMC_NS@

PC823
680P_0402_50V

DIS_EMC_NS@

DIS@
PC824
330P_0402_50V

DIS@
PR817
1K_0402_1%

PR818
30.9K_0402_1%
DIS@

DIS@
PR819
20K_0402_1%

+1.5VSP

DIS@
PC825 22U_0805_6.3V6-M
PC826 22U_0805_6.3V6-M
PC827 22U_0805_6.3V6-M
PC828 22U_0805_6.3V6-M

PC829 2200P_0402_25V
PC830 0.1U_0402_25V6

DIS_EMC@ DIS_EMC@

@PJ806
JUMP_43X118

+1.5VS_VGA

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: *+1.5VS_VGA*

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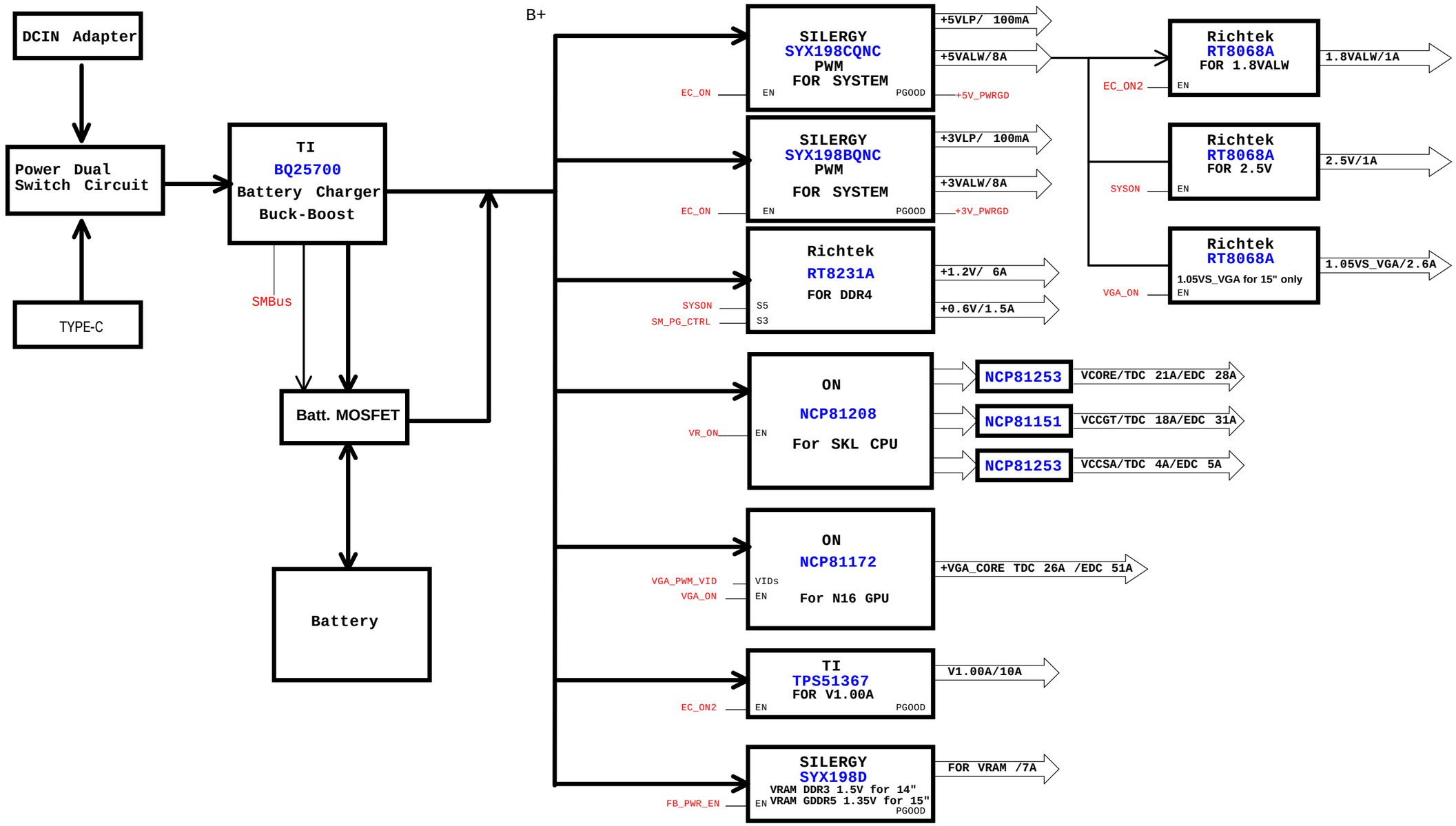

Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title: *Power Block Diagram*

Size	Document Number	Rev
Custom	KENOBI	2.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title

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Size	Document Number	Rev
Custom	***KENOBI***	2.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/09/01	Deciphered Date	2016/12/31

Title

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Custom	***KENOBI***	2.0
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