

Genesis-1 Block Diagram

LGS-1 91.4RQ01.001

JULY. 18, 2011

PCB Layer Stackup

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:VCC
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector

BQ24760 75

INPUTS	OUTPUTS
VINT20	CHARGER_OUT12

System DC/DC

TPS51220ARSN 79

VINT20	VCC5M
	VCC3M

CPU DC/DC

VT1318M/VT1324S 80

VCC5M_OUT	VCCCPUCORE
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GMCH GFX CORE

VT1324S 81

VCC5M_OUT	VCCGFXCORE
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VCC1R5B

VT355FCX 86

VCC5M_OUT	VCC1R5B
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VCC0R675B

MAX1510 87

VCC1R35A

VT356FCX 88

VCC5M_OUT	VCC1R35A
VCC1R35A	VCC0R675B

VCC1R8B

BD9139 89

VCC5M_OUT	VCC1R8B
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VCC1R05AMT

VT356FCX 85

VCC5M_OUT	VCC1R05LAN
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VCC1R05B_VTT

VT356 84

VCC5M_OUT	VCC1R05B_VTT
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VCCSA

VT371 90

VCC5M_OUT	VCCSA
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Title

Block Diagram

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A3

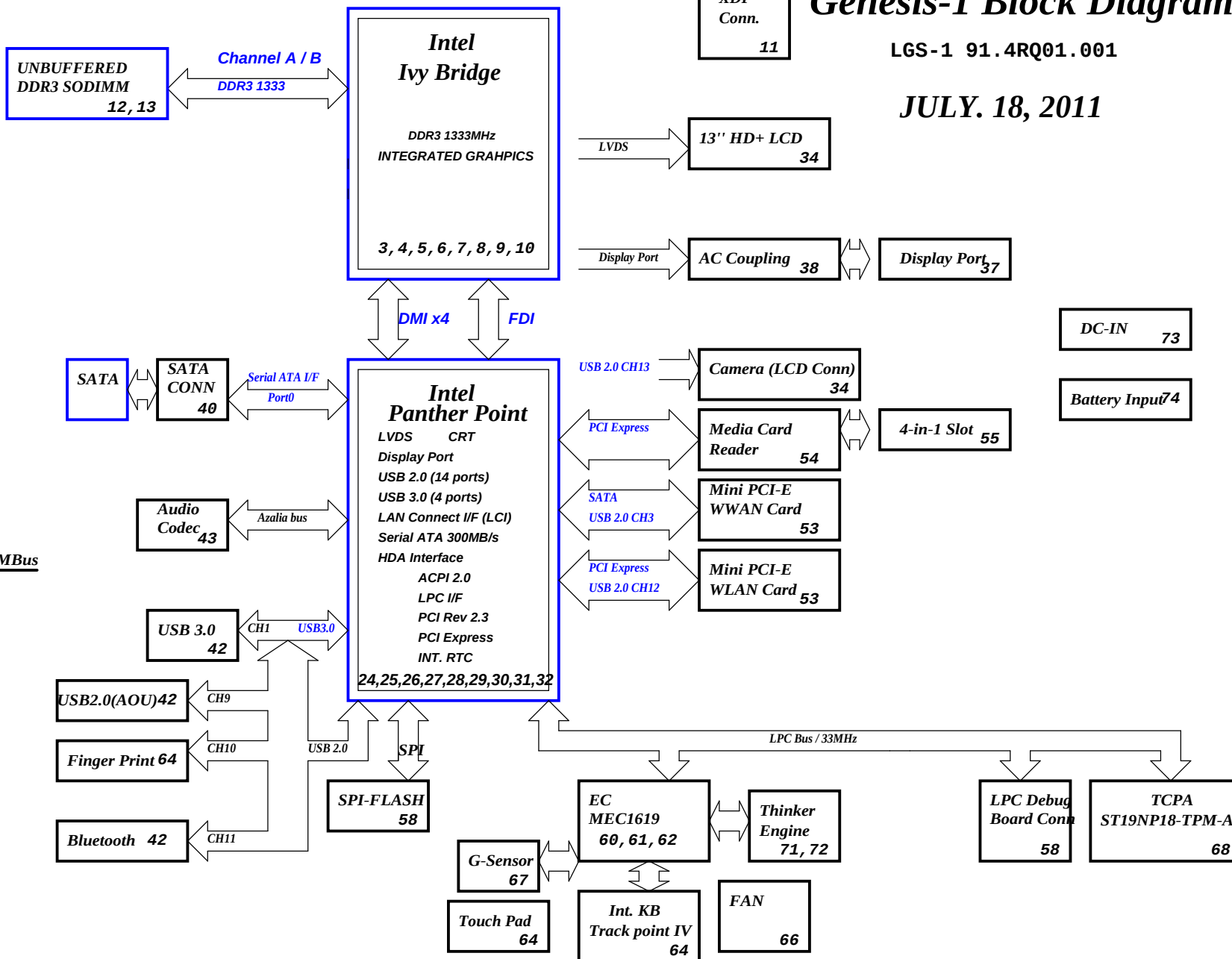
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is

Capacitor type + value + rating + size + tolerance + material

SCD1U10V2MX-1

SC=> SMT Ceramic, TC=> POS cap or SP cap

D1U => 0.1uF

10V => the voltage rating is 10V

2=> 0402, 3=>0603, 5=>0805

M=>tolerance M, K, Z

X=> X7R/X5R, Y=> Y5V

-1 => symbol version, nonsense to EE characteristic

PLANAR_ID[3..0]

IBEXPEAK-M	39	38	48	49	Planar ID Version	Planar PCB Version
PLANAR_IDn	3	2	1	0		
	0	0	0	0	Genesis-1 initial	N/A
	0	0	0	1	FVT	N/A
	0	0	1	0	SIT	SC
	0	0	1	1		
	0	1	0	0		
	0	1	0	1		
	0	1	1	0		
	0	1	1	1		
	1	0	0	0		
	1	0	0	1		
	1	0	1	0		

EC HISTORY

[illegible]

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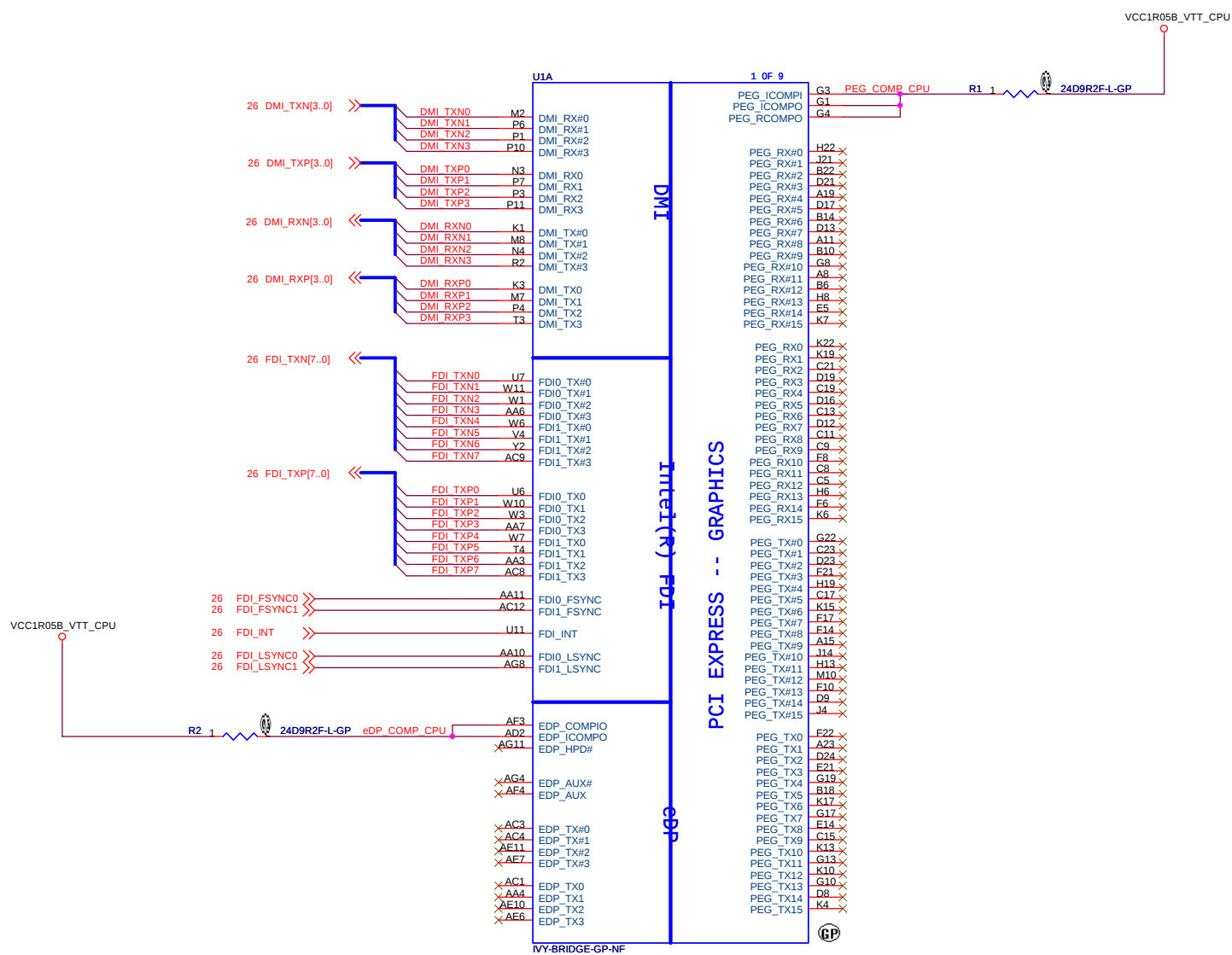
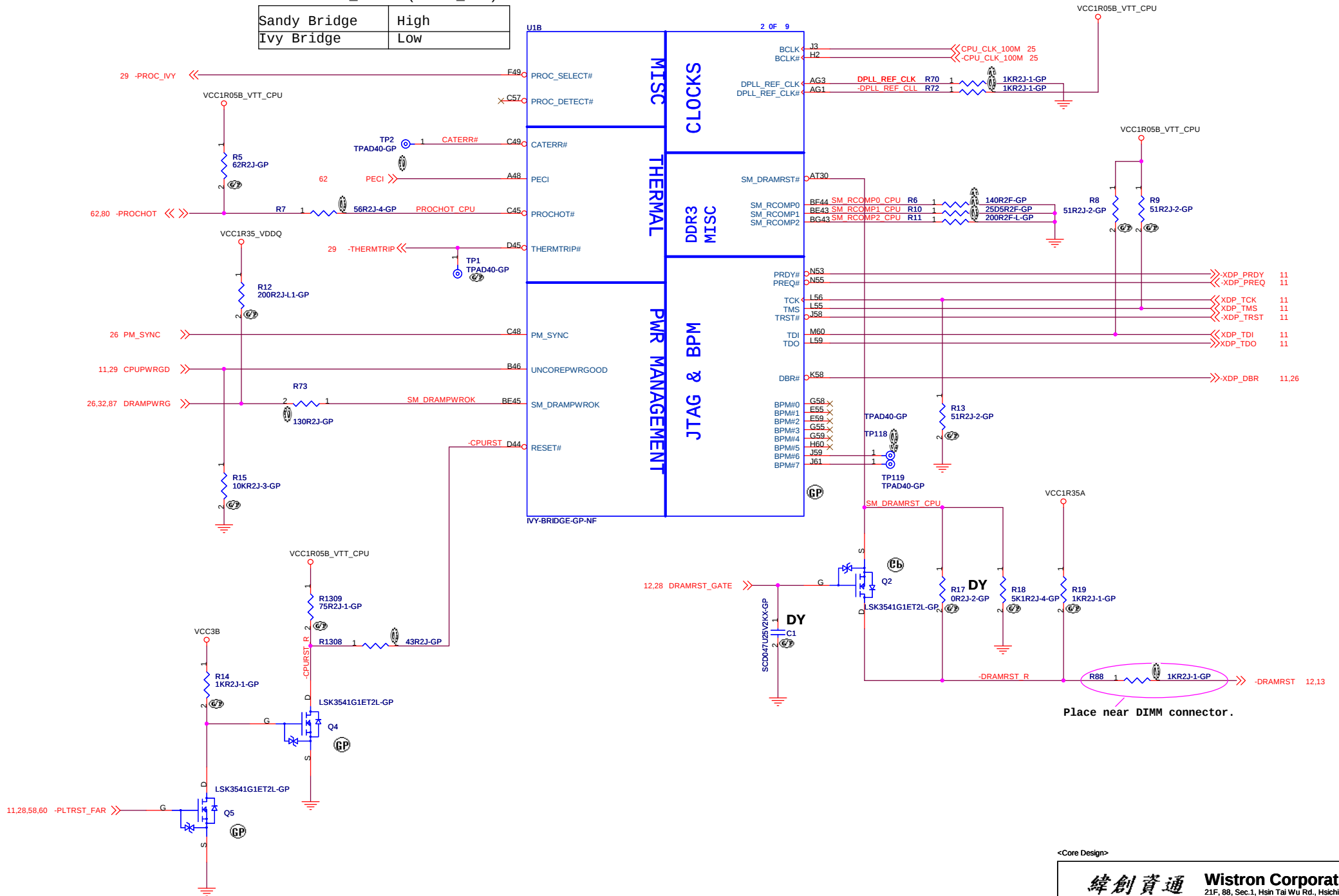
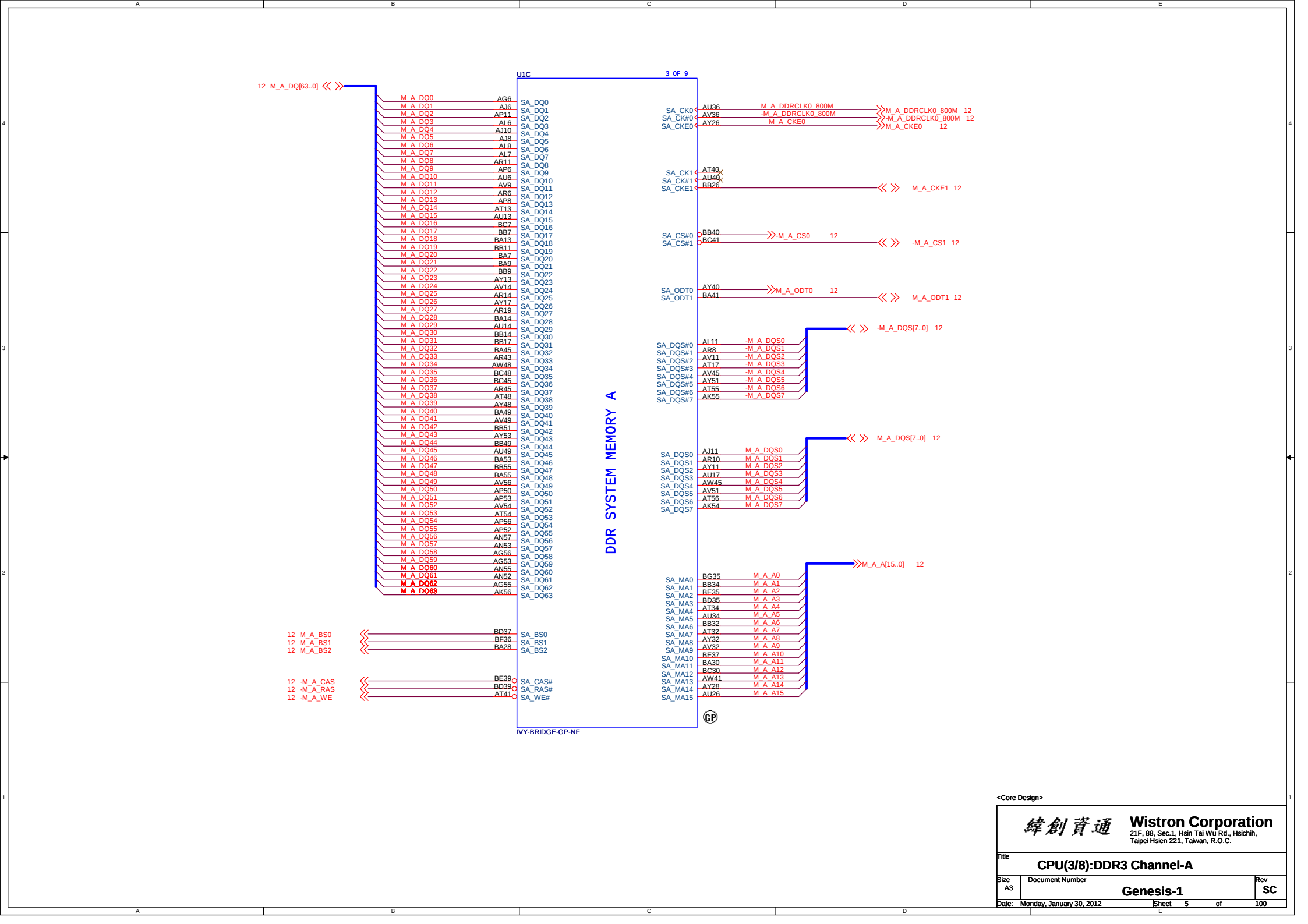


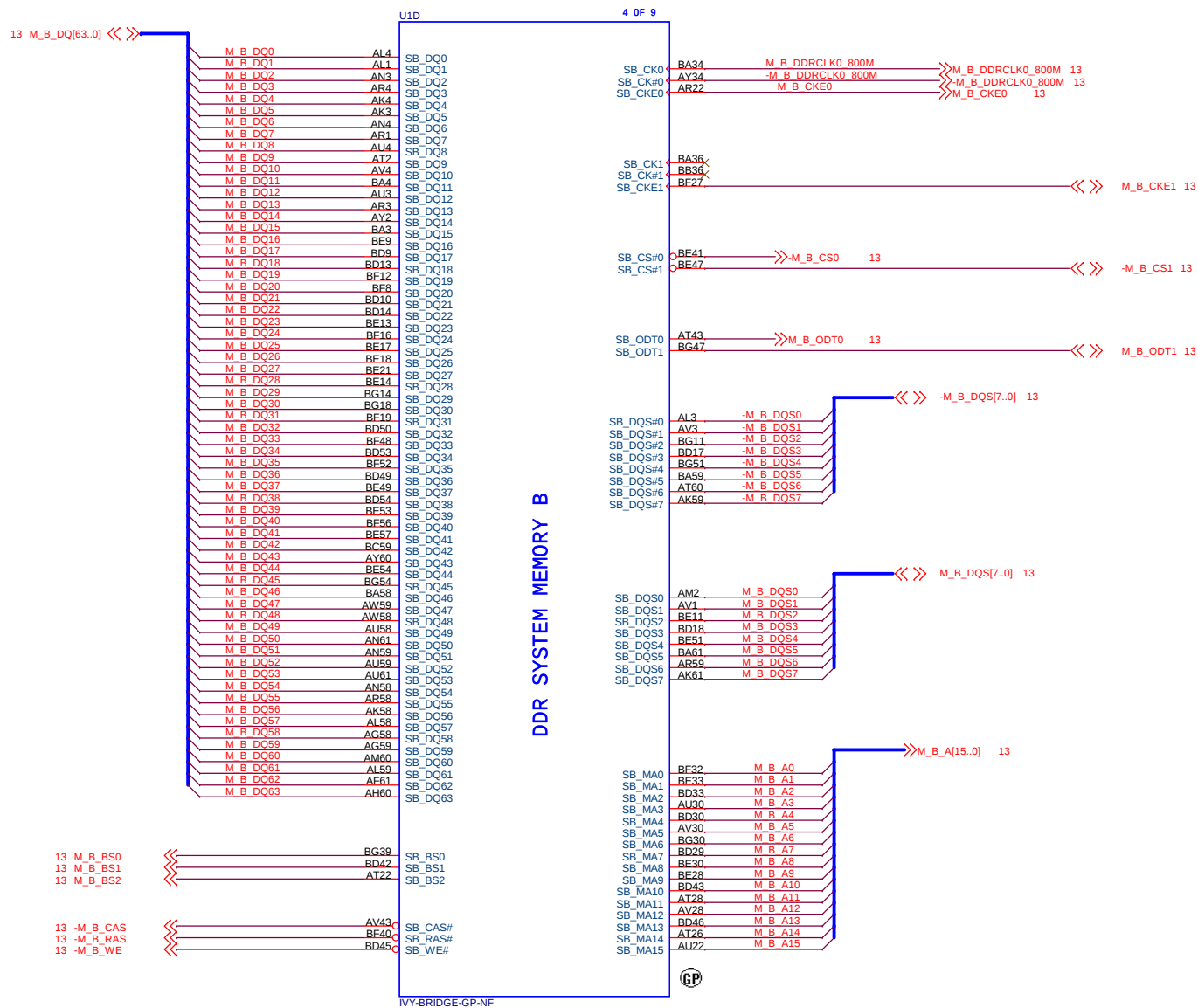
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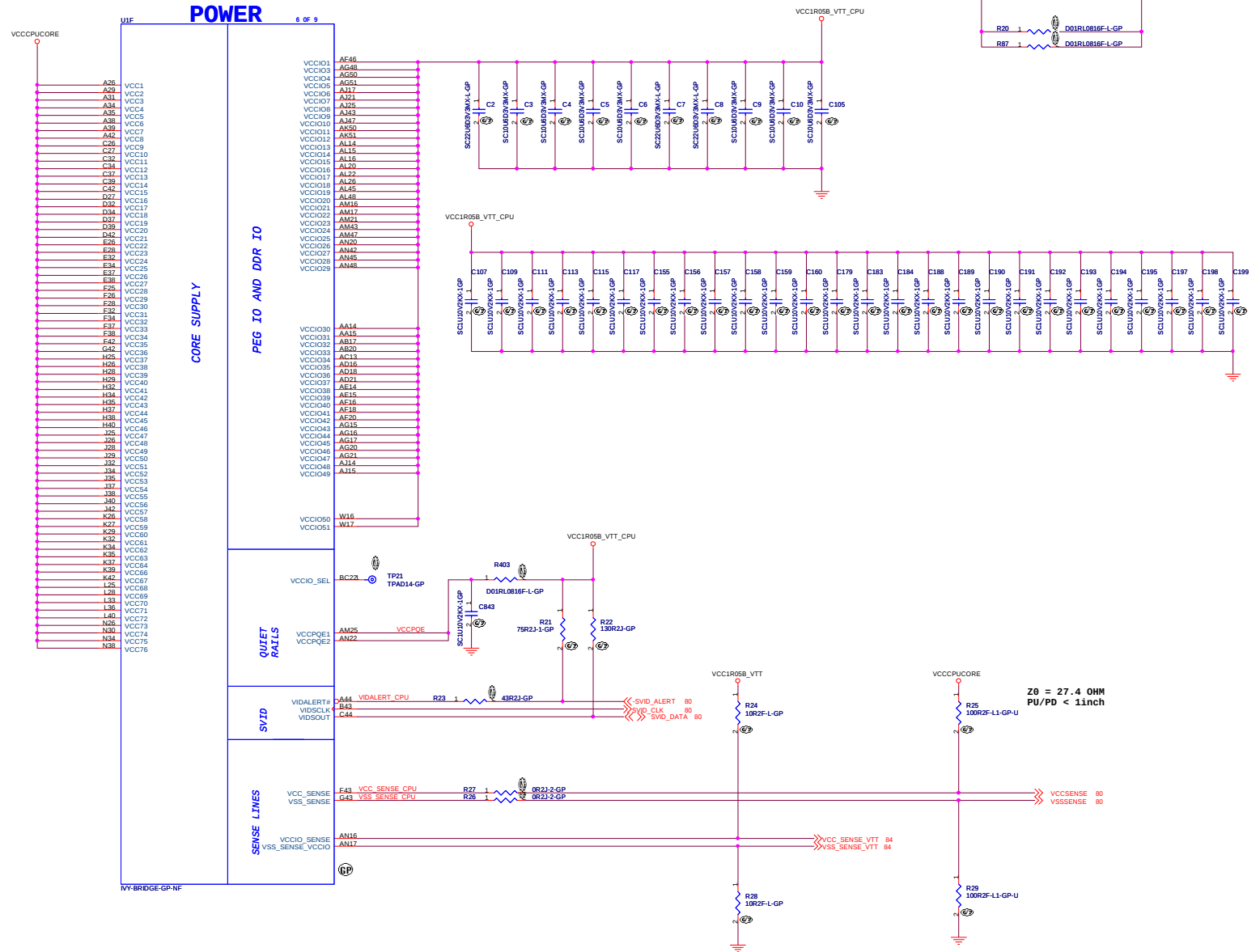
Sandy Bridge	High
Ivy Bridge	Low

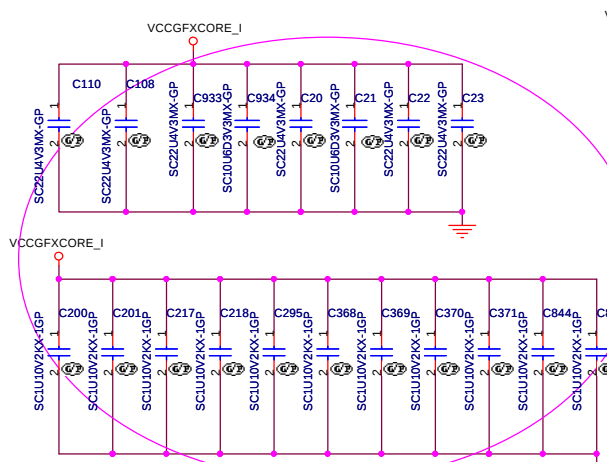


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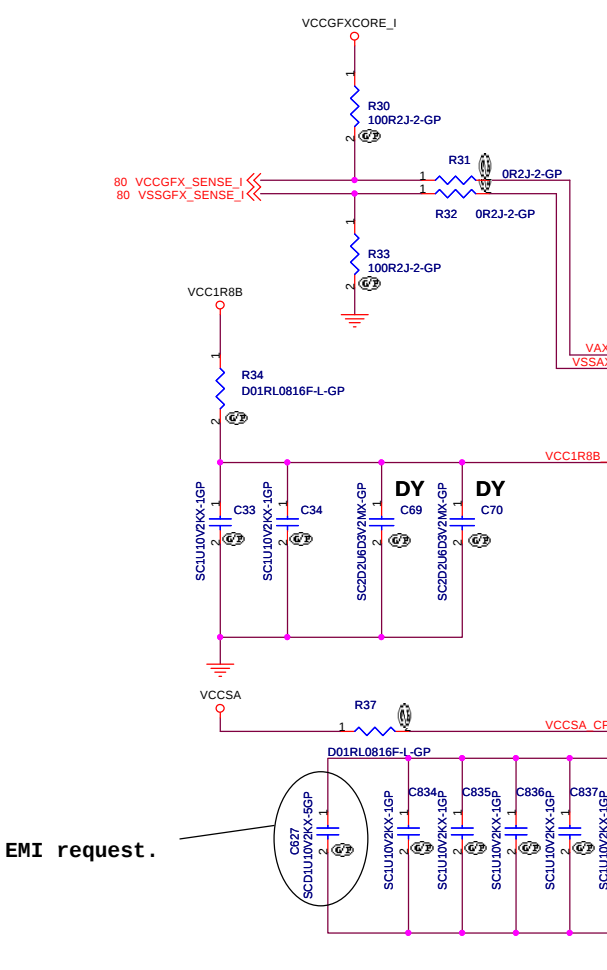




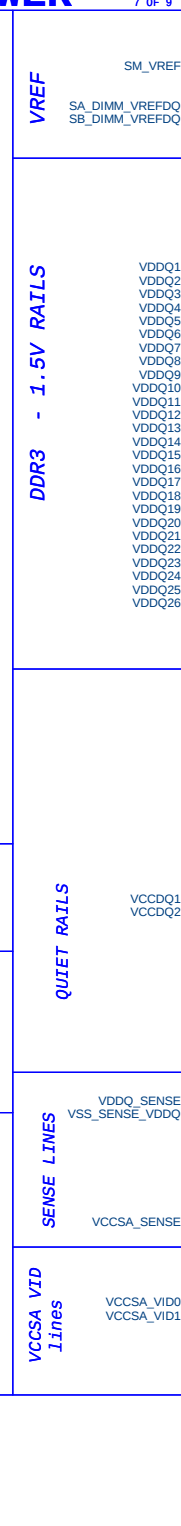
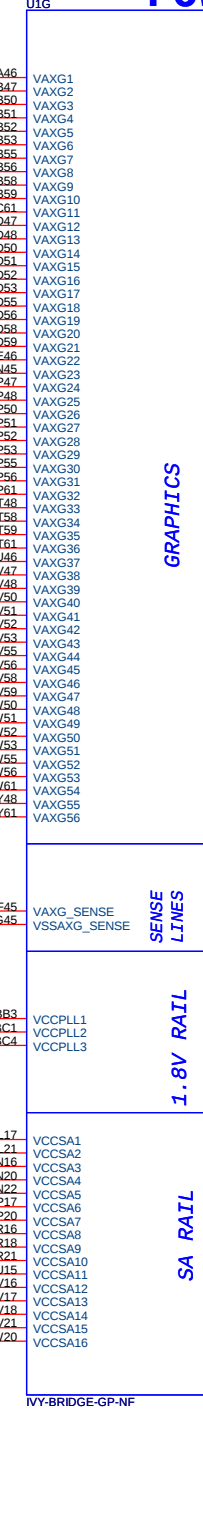




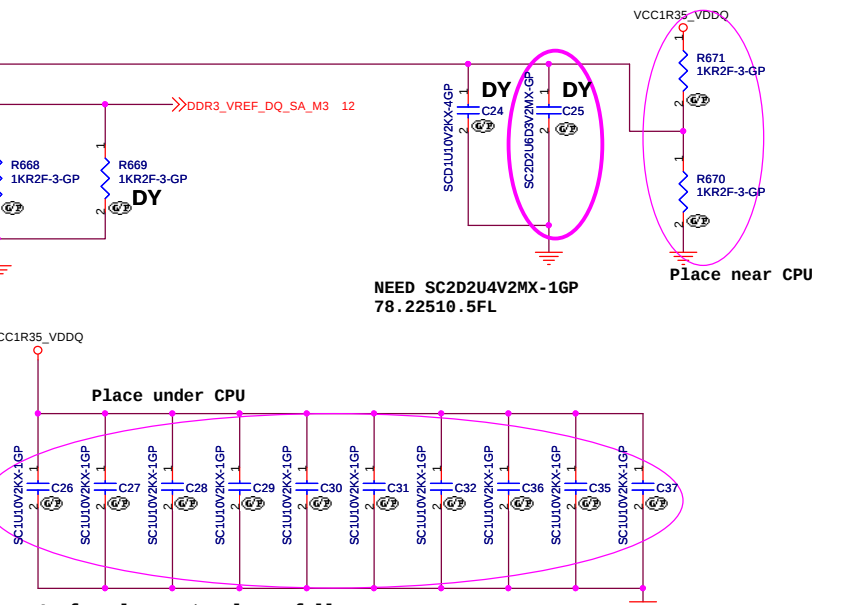
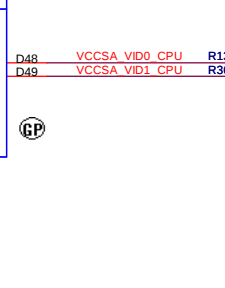
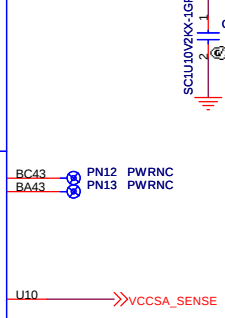
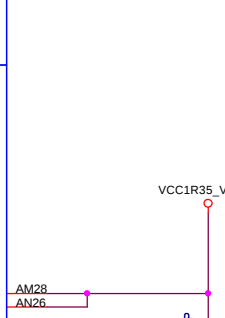
As for placement, please follow
"Chief River Platform Power Delivery Design Guide"
(Intel DocNo.458544)



- AA46 VAXG1
- AB47 VAXG2
- AB50 VAXG3
- AB51 VAXG4
- AB52 VAXG5
- AB53 VAXG6
- AB55 VAXG7
- AB56 VAXG8
- AB58 VAXG9
- AB59 VAXG10
- AC61 VAXG11
- AD47 VAXG12
- AD48 VAXG13
- AD50 VAXG14
- AD51 VAXG15
- AD52 VAXG16
- AD53 VAXG17
- AD56 VAXG18
- AD58 VAXG19
- AD59 VAXG20
- AE46 VAXG21
- N45 VAXG22
- P47 VAXG23
- P48 VAXG24
- P50 VAXG25
- P51 VAXG26
- P52 VAXG27
- P53 VAXG28
- P56 VAXG29
- P61 VAXG31
- T48 VAXG32
- T58 VAXG34
- T59 VAXG35
- U48 VAXG36
- V47 VAXG37
- V48 VAXG38
- V50 VAXG40
- V51 VAXG41
- V52 VAXG42
- V53 VAXG43
- V56 VAXG44
- V58 VAXG45
- V59 VAXG46
- W50 VAXG48
- W51 VAXG49
- W52 VAXG50
- W53 VAXG51
- W55 VAXG52
- W56 VAXG53
- W61 VAXG54
- Y48 VAXG55
- Y61 VAXG56



- VDDQ1 AJ28
- VDDQ2 AJ33
- VDDQ3 AJ36
- VDDQ4 AJ40
- VDDQ5 AL30
- VDDQ6 AL34
- VDDQ7 AL38
- VDDQ8 AL42
- VDDQ9 AM33
- VDDQ10 AM38
- VDDQ11 AM40
- VDDQ12 AN30
- VDDQ13 AN34
- VDDQ14 AN38
- VDDQ15 AR26
- VDDQ16 AR28
- VDDQ17 AR30
- VDDQ18 AR32
- VDDQ19 AR34
- VDDQ20 AR36
- VDDQ21 AR40
- VDDQ22 AV41
- VDDQ23 BA40
- VDDQ24 BB28
- VDDQ25 BG33
- VDDQ26 BG33



As for placement, please follow
"Huron River Platform Power Delivery Design Guide Rev1.0"
(Intel DocNo.439028)



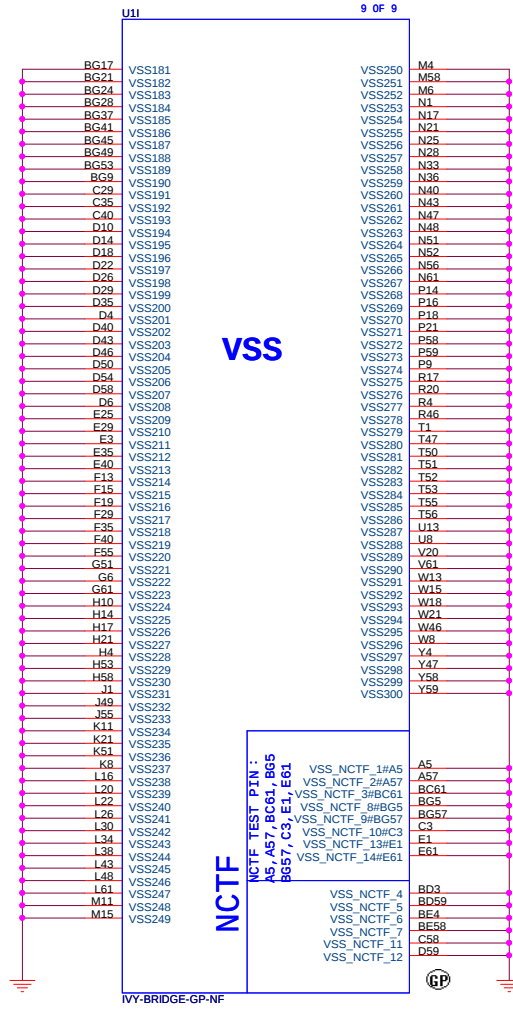
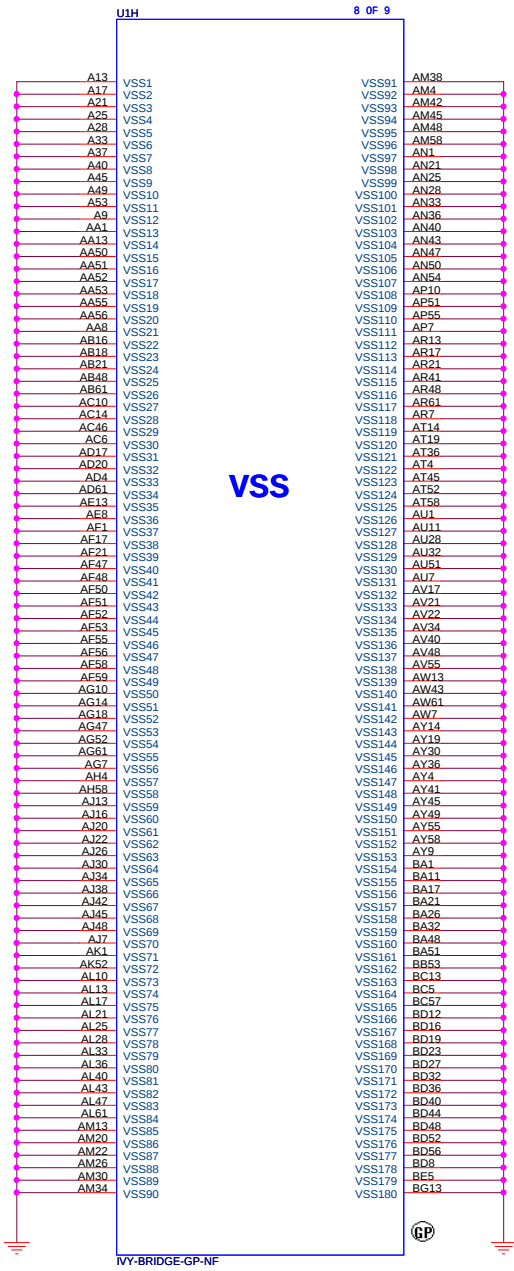
	VCCSA_SEL0	VCCSA_SEL1	VCCSA
Sandy Bridge	LOW 0 0	0 1	0.90V 0.80V
Ivy Bridge	High 1 1	0 1	0.725V 0.675V

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Title: CPU(6/8):Graphics Power

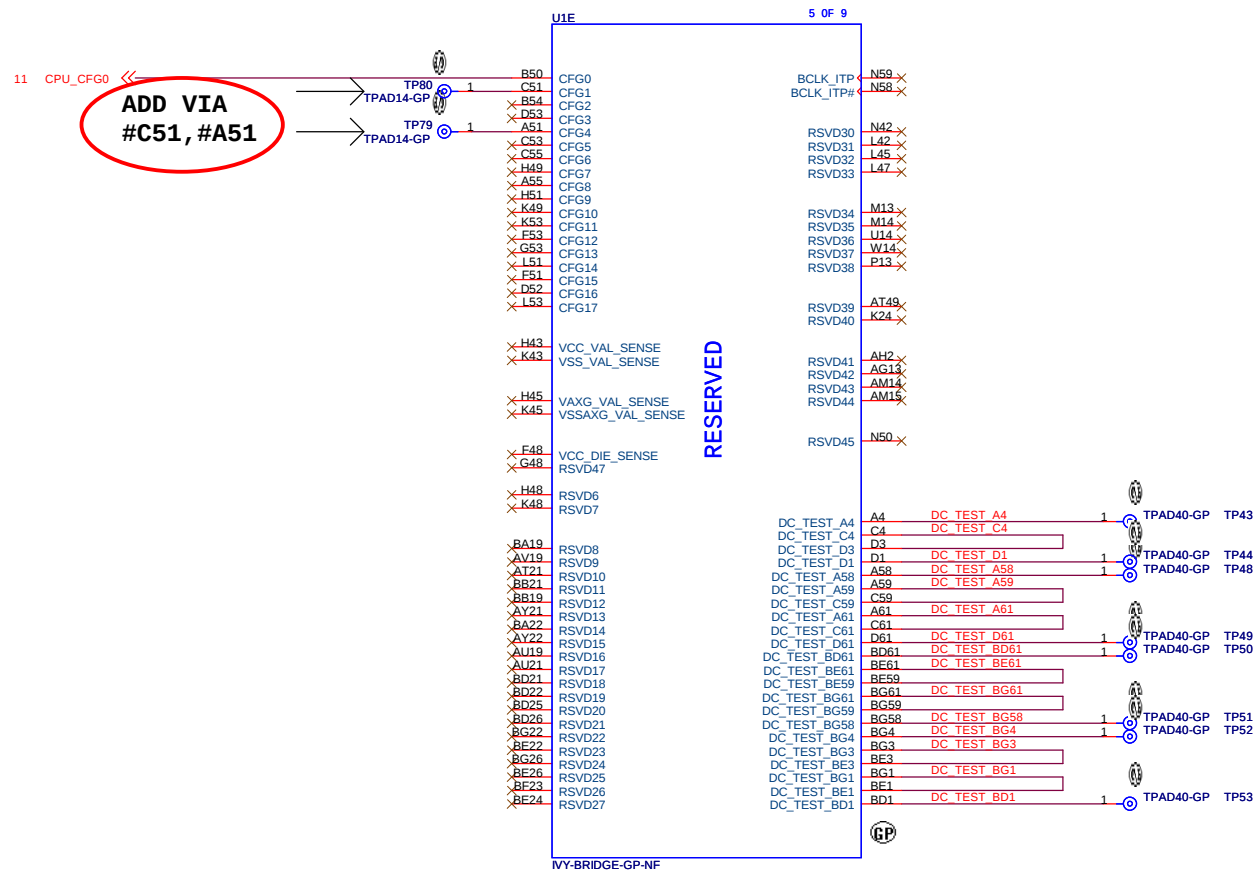
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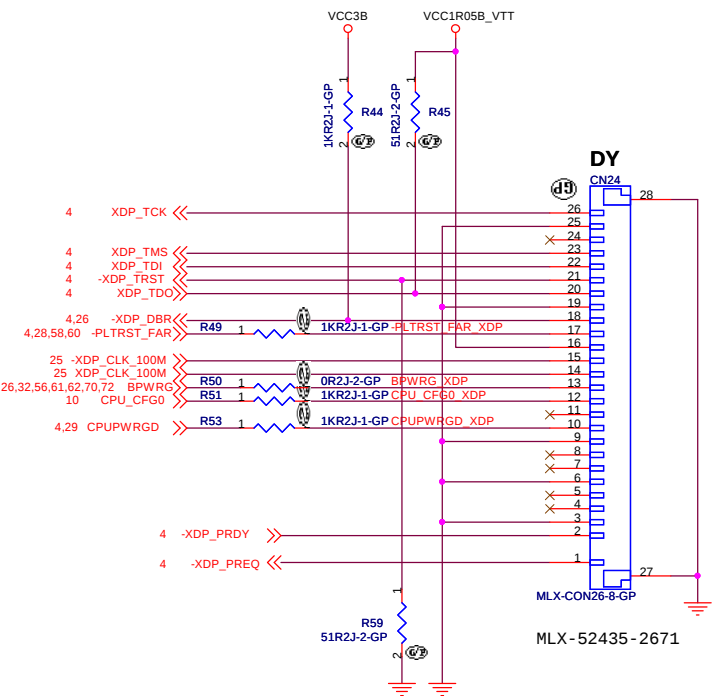


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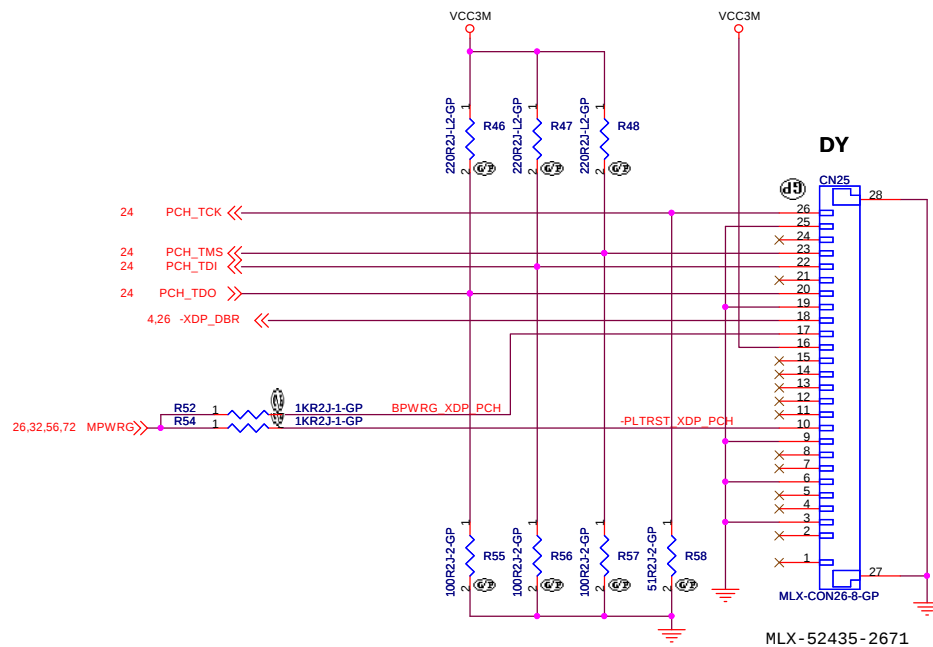


DEBUG Interface for Processor.

XDP1 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TD0	R45	ASM	DY
TRST#	R59	ASM	ASM
DBRST#	R44	ASM	ASM
RESET#	R49	ASM	DY
CFG0	R51	ASM	DY
PWRGD	R53	ASM	DY
BPWRG	R50	ASM	DY
	CN24	ASM	DY

PDV Logic



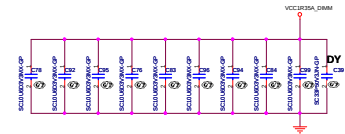
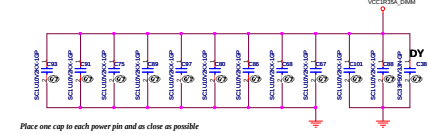
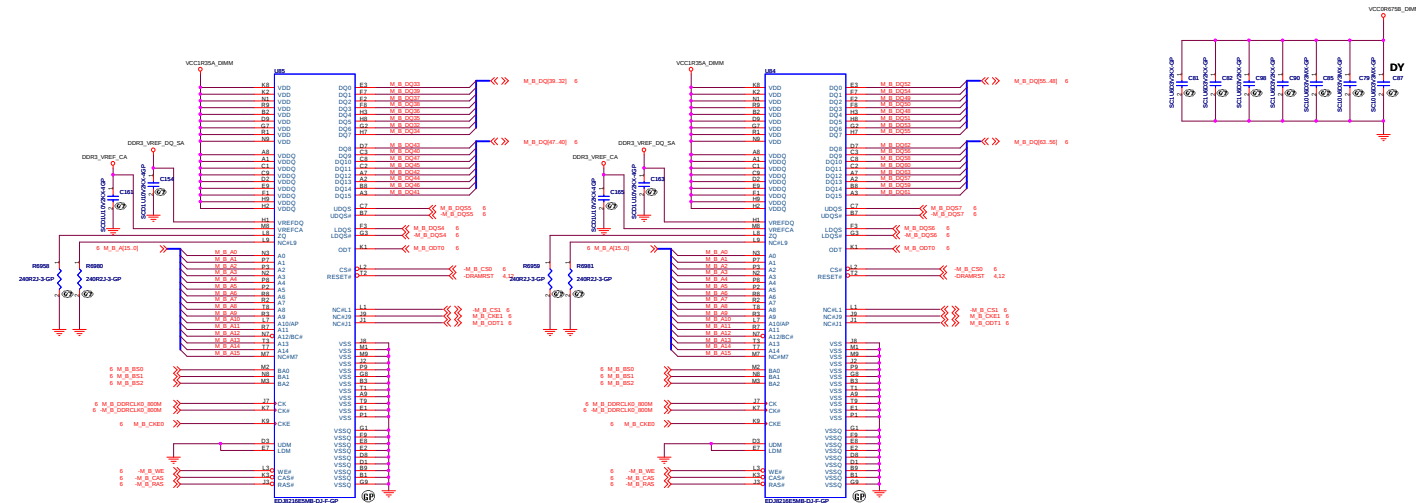
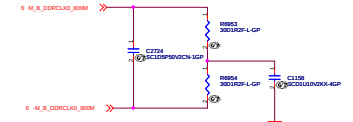
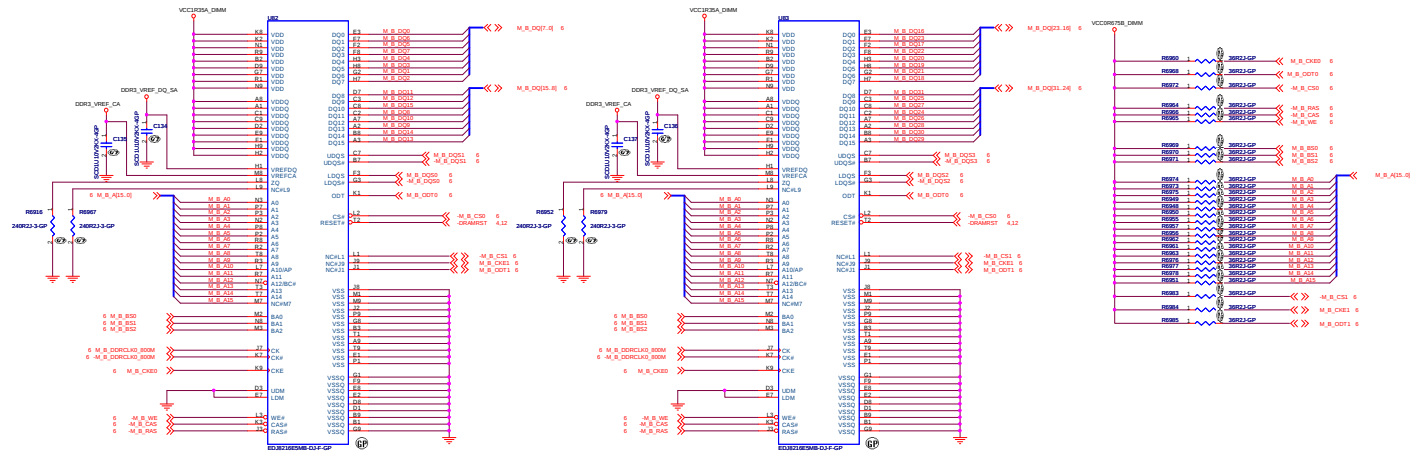
DEBUG Interface for PCH.

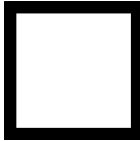
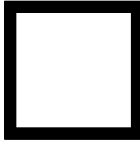
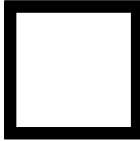
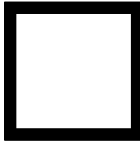
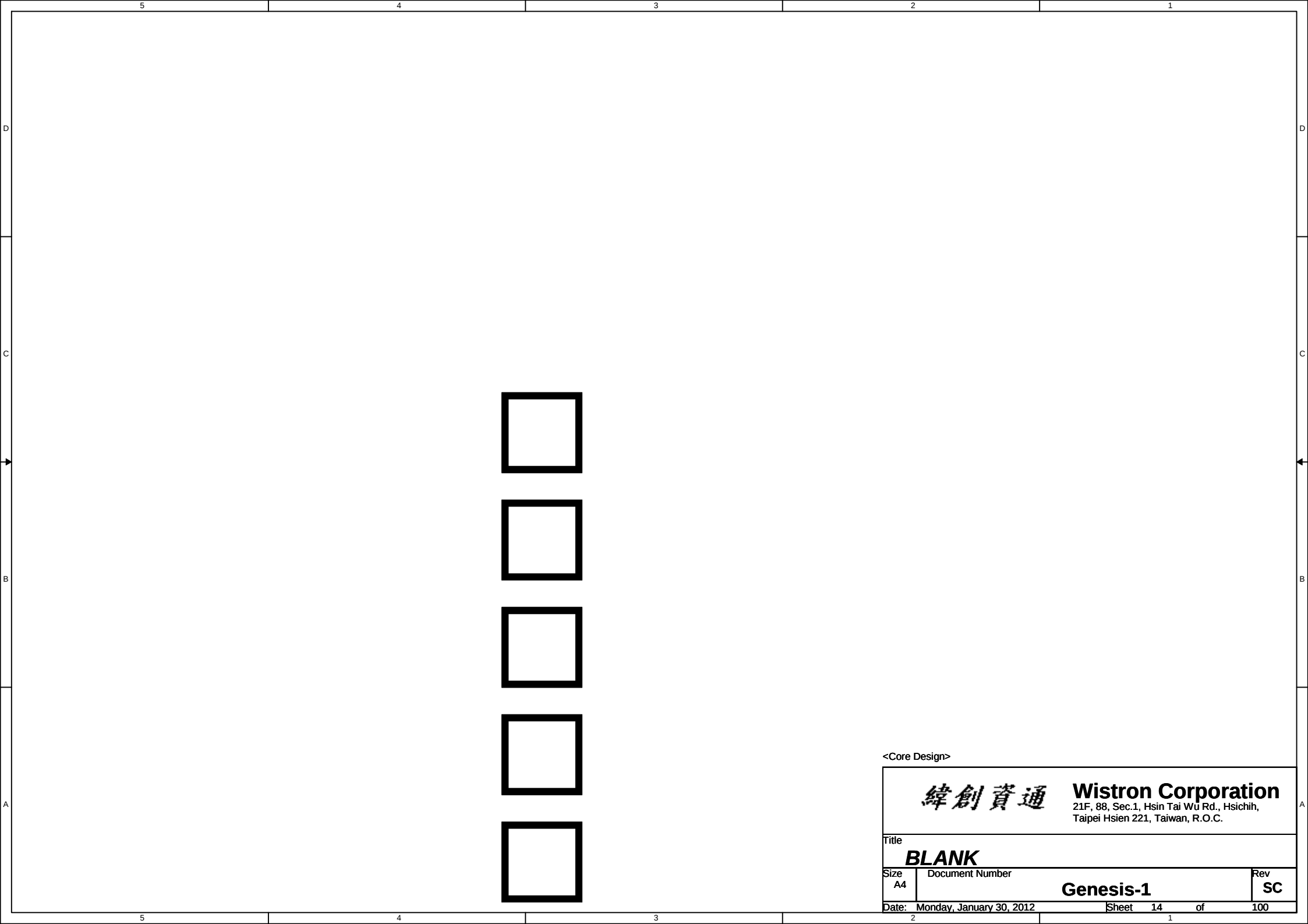
XDP2 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TD0	R46	220	DY
	R55	100	DY
TMS	R48	220	DY
	R57	100	DY
TDI	R47	220	DY
	R56	100	DY
TCK	R58	51	51
MPWRG	R52	ASM	DY
	R54	ASM	DY
	CN25	ASM	DY

PDV Logic

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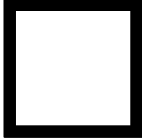
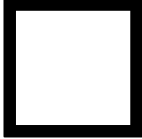
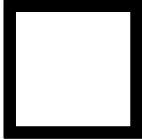
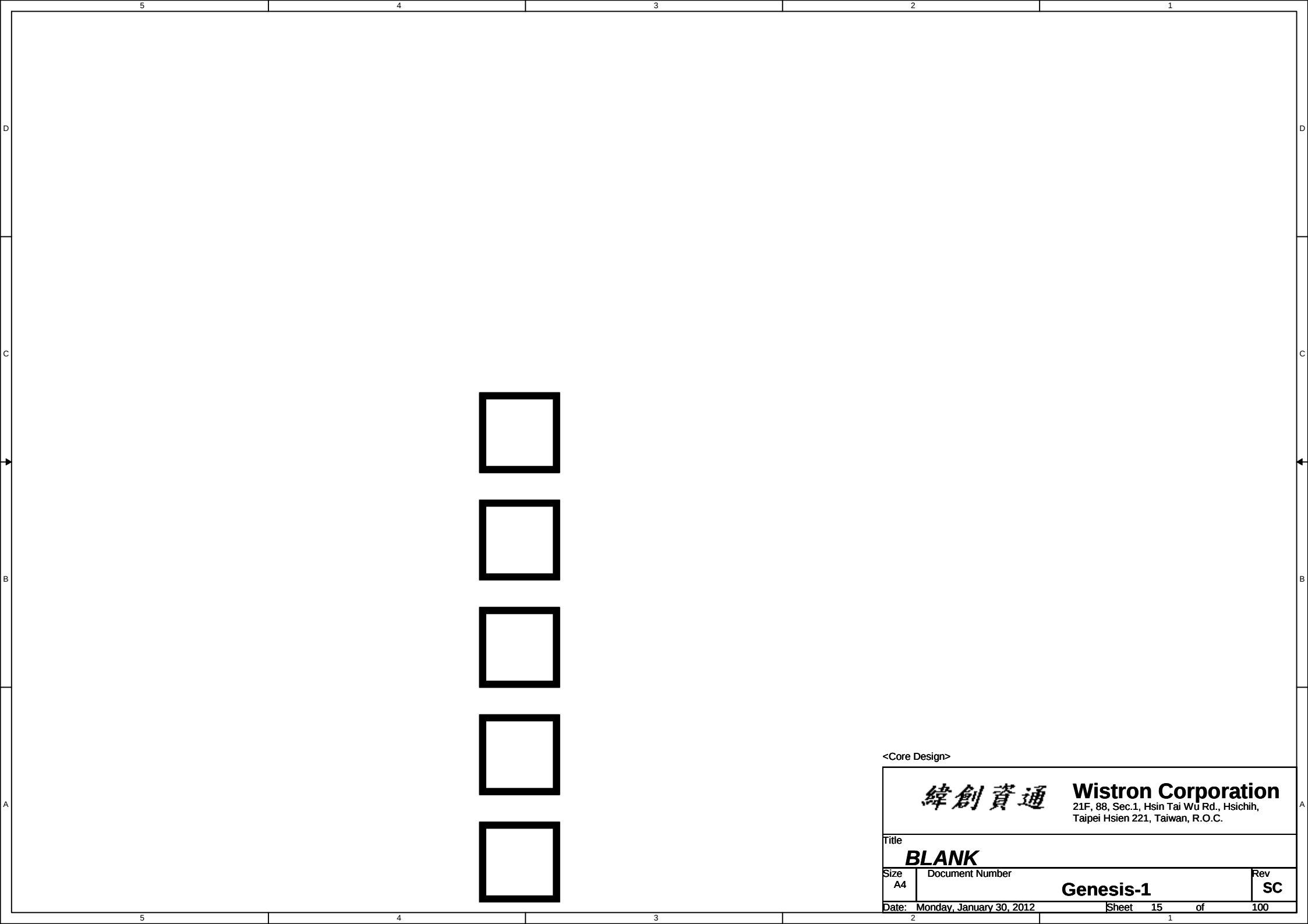
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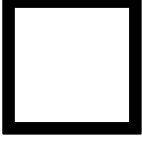
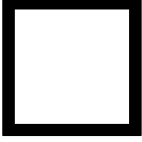
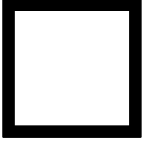
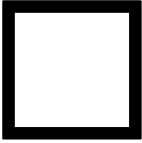
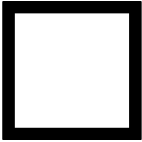
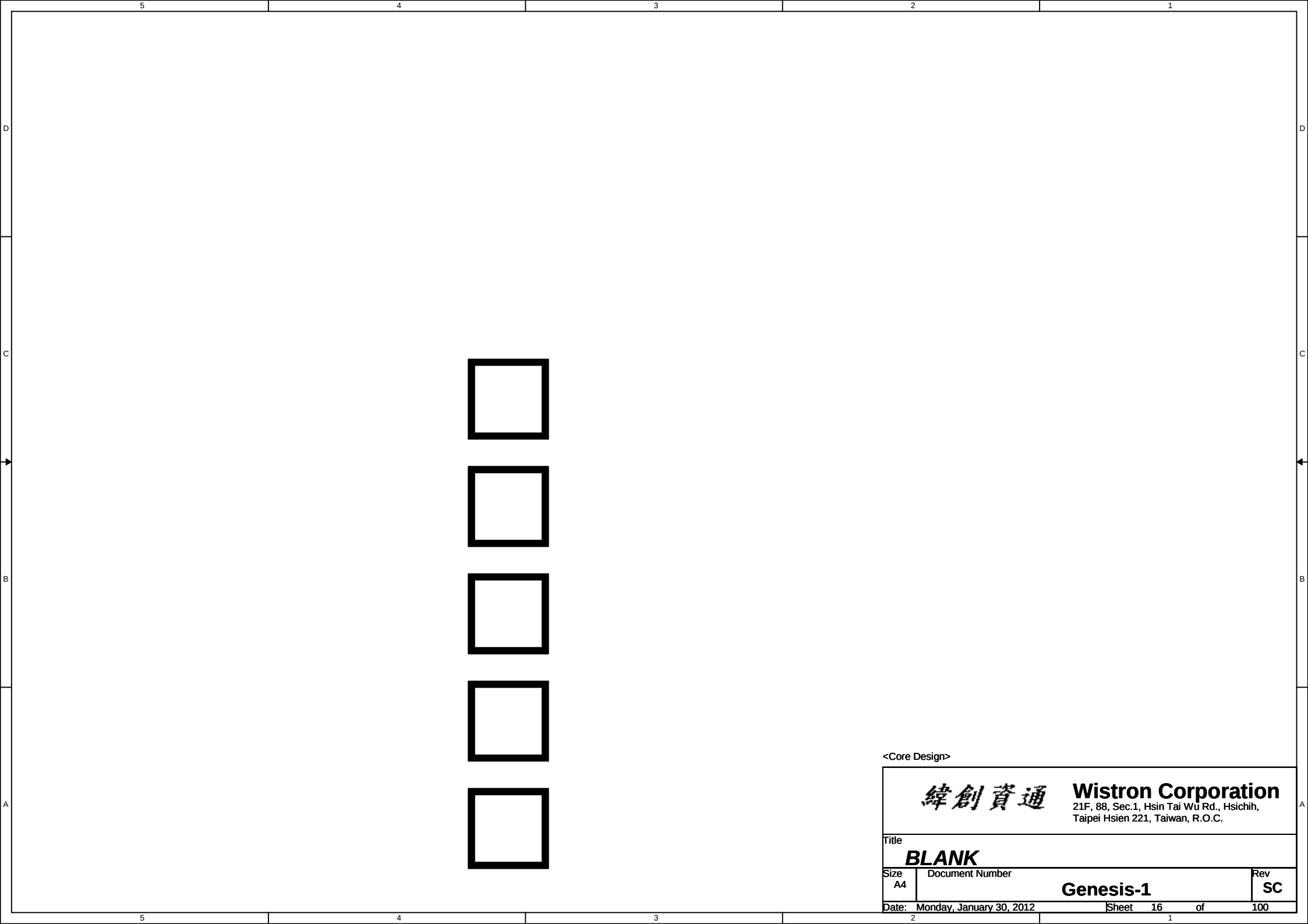
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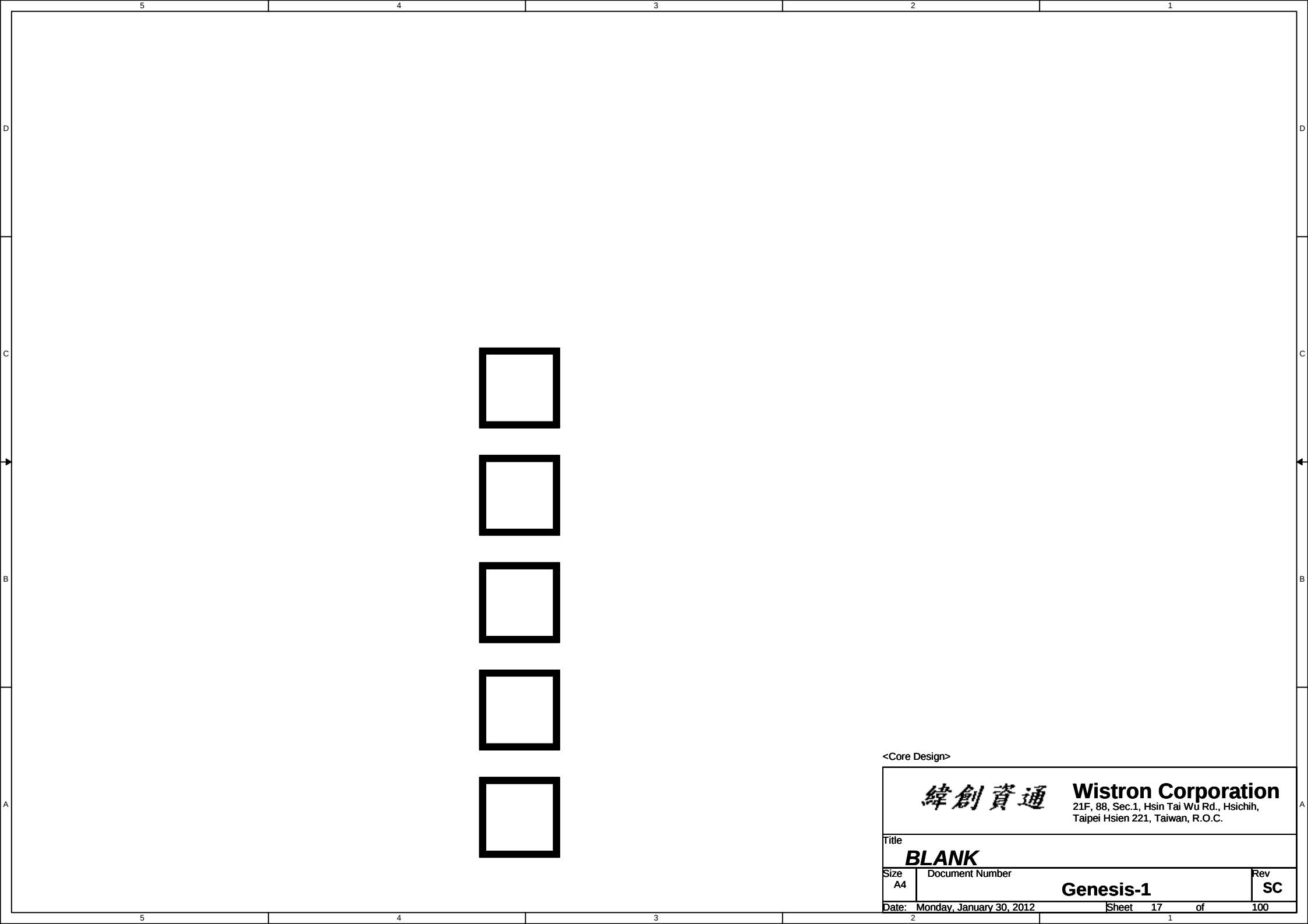
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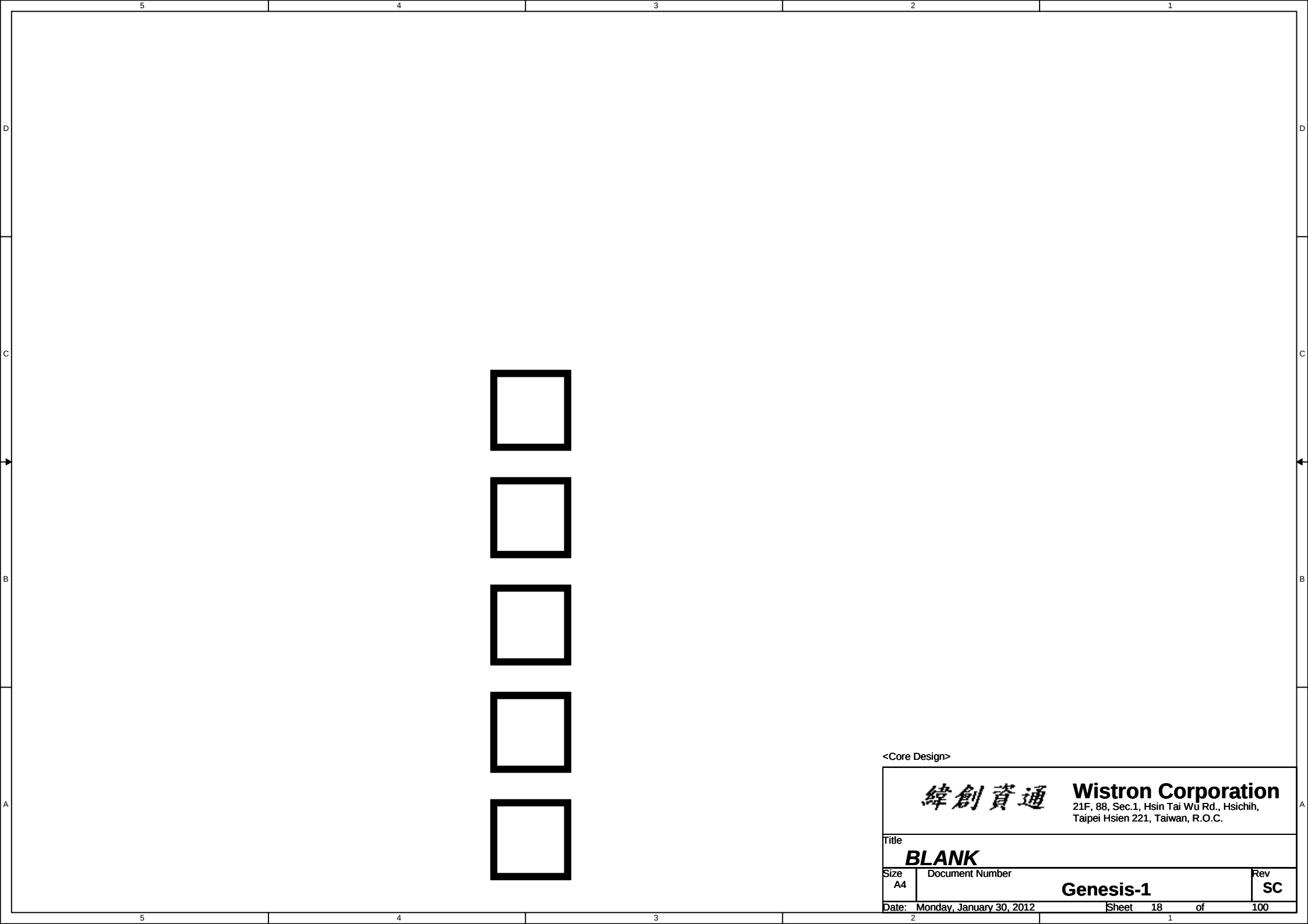
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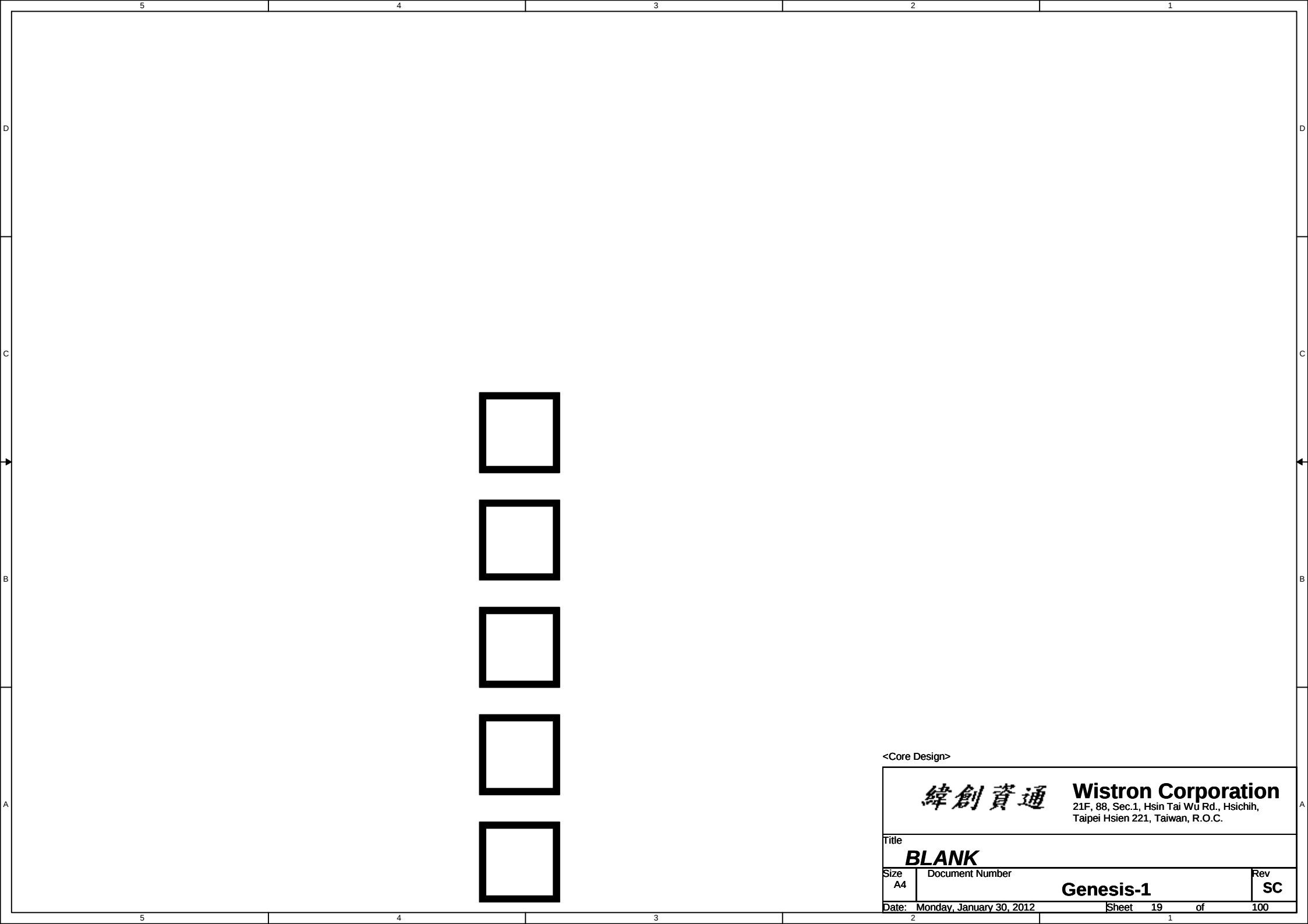
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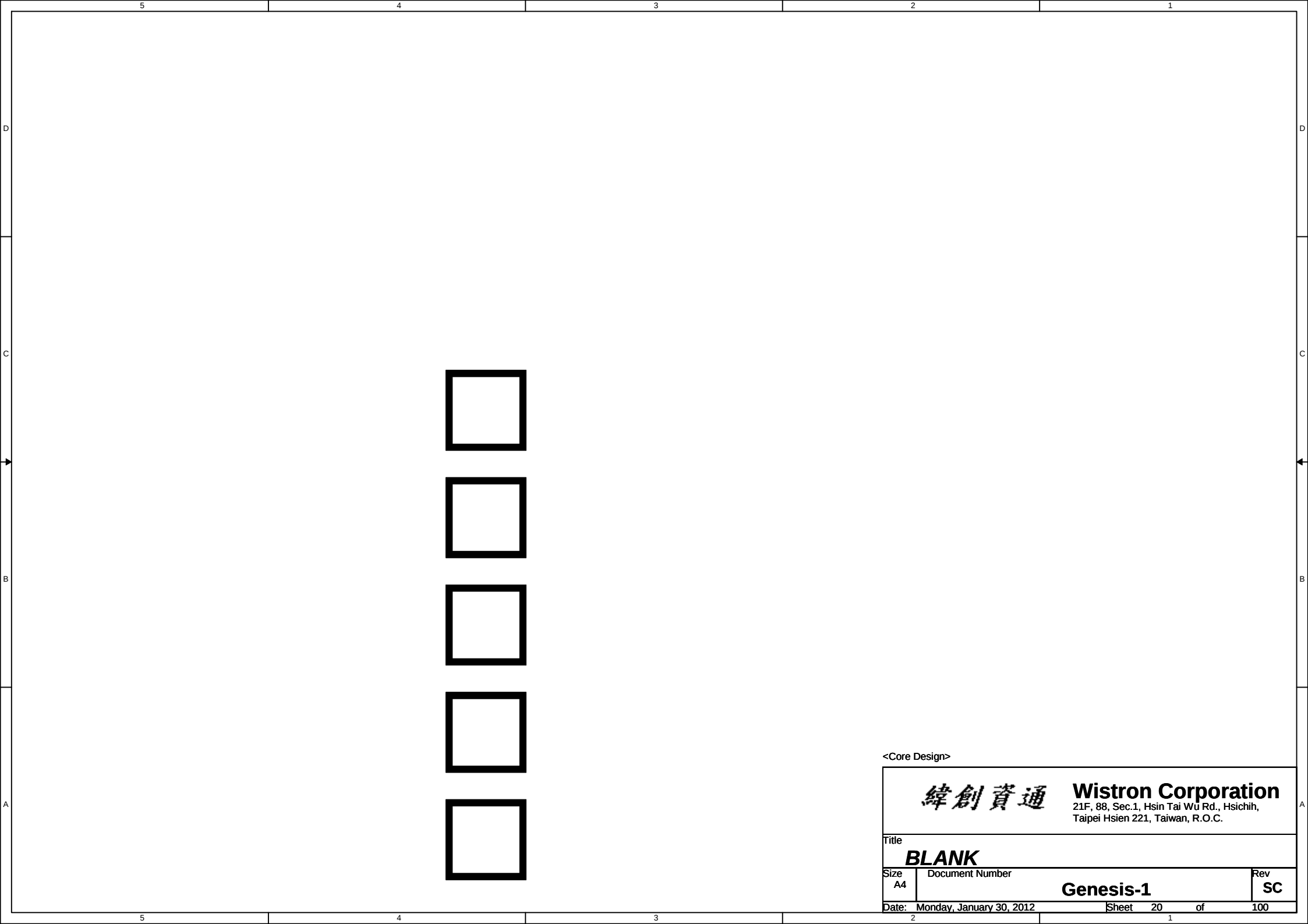


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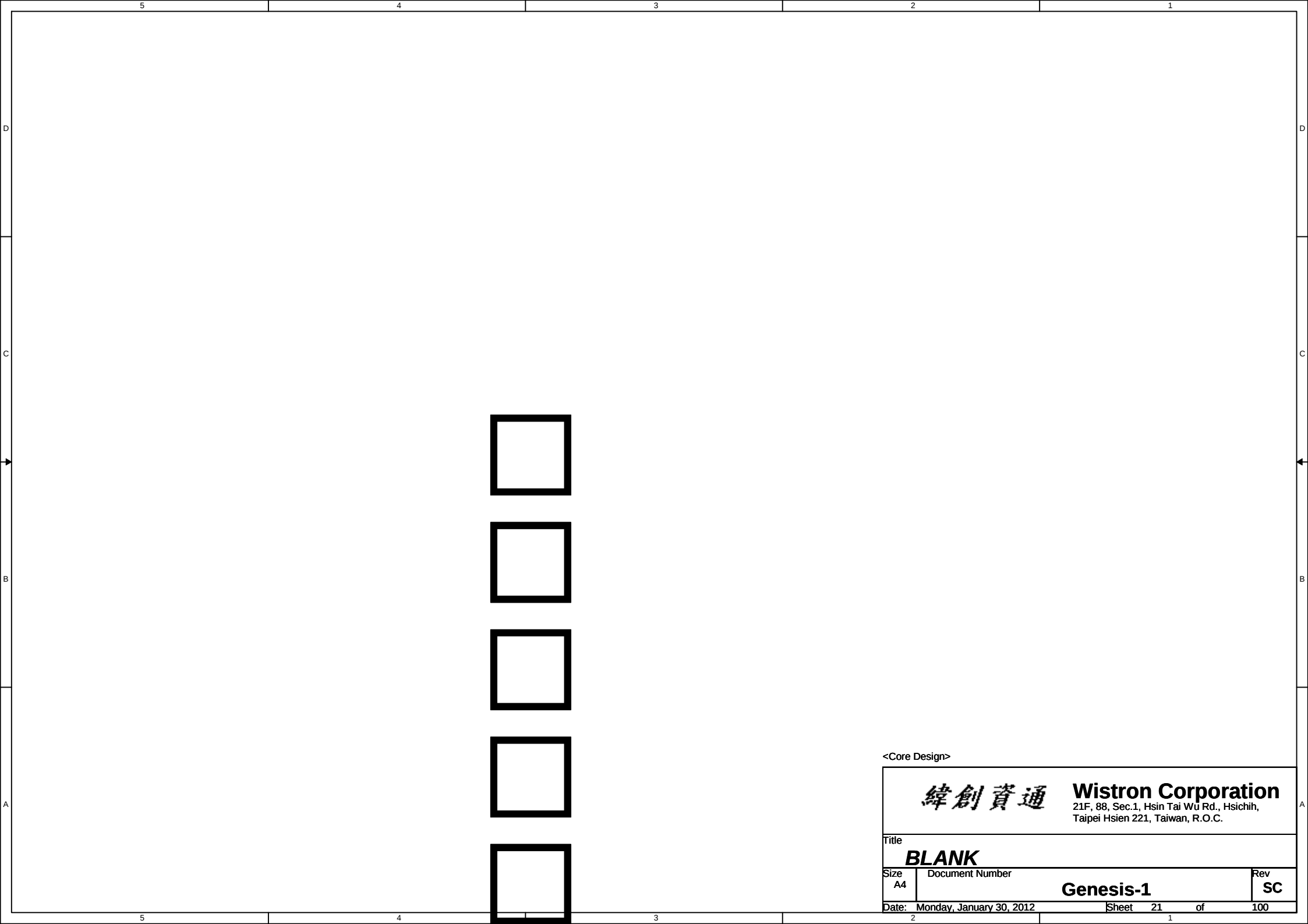
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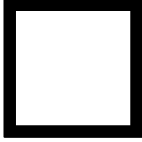
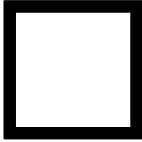
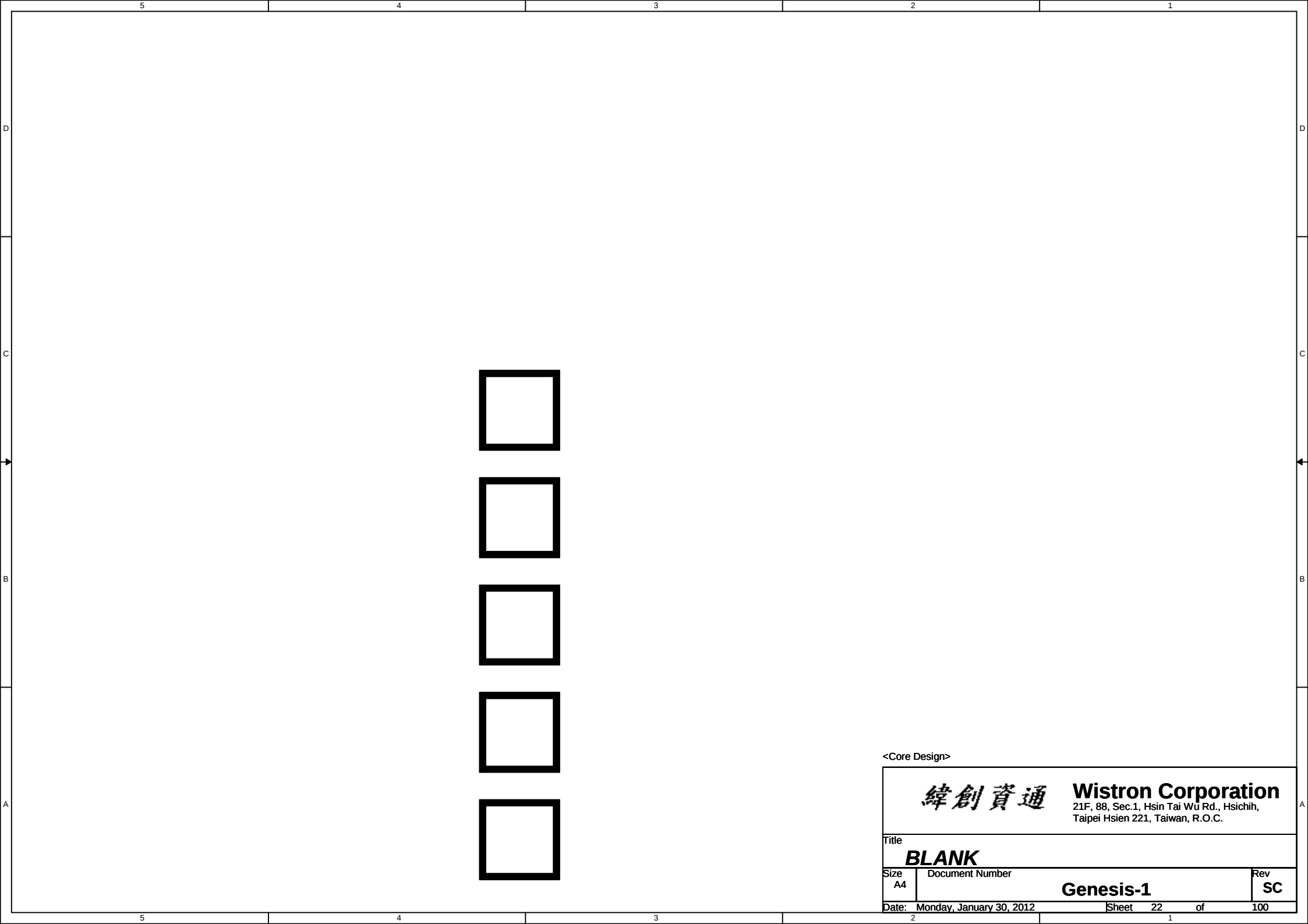
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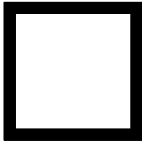
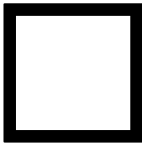
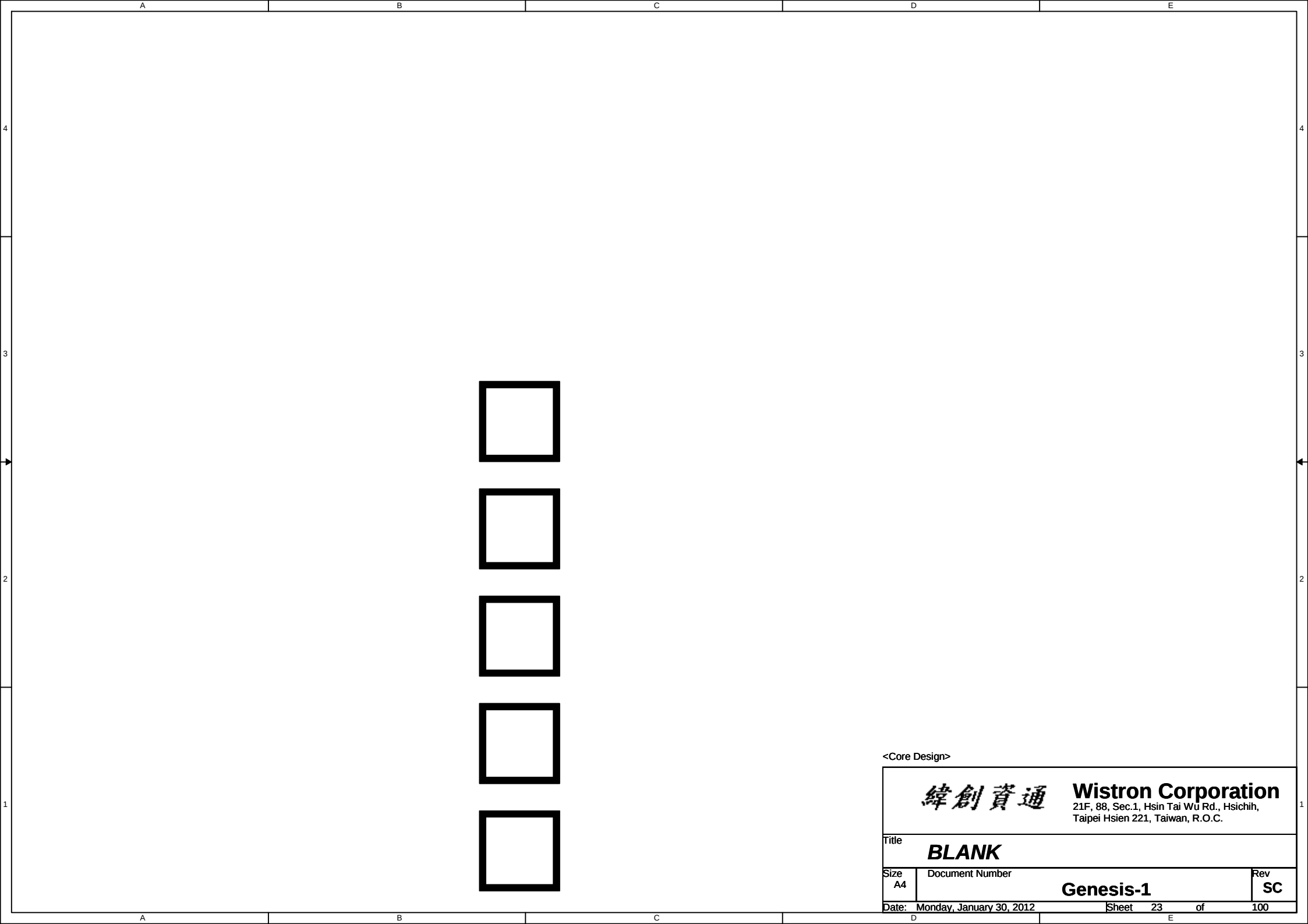
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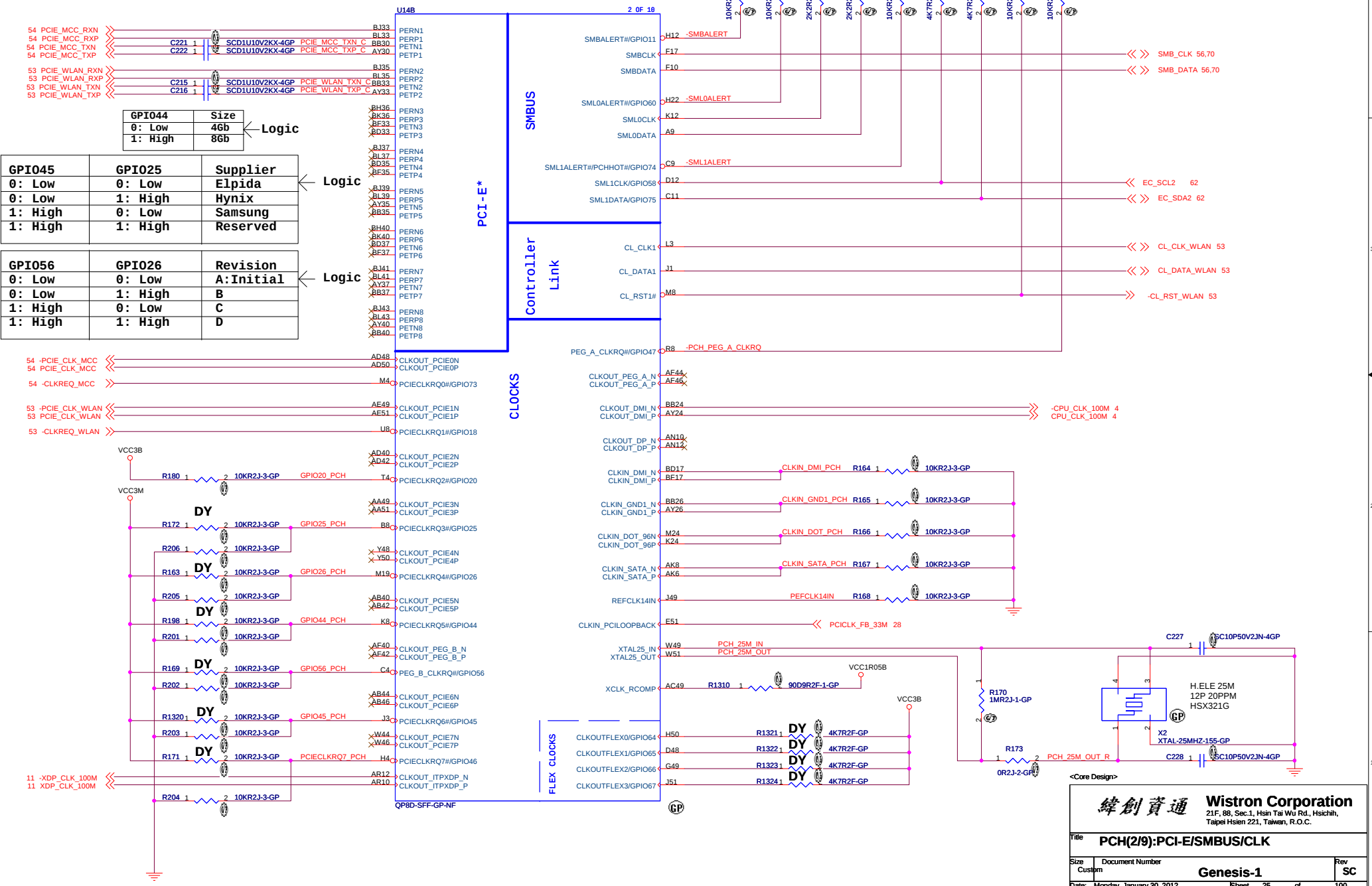
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Genesis-1

Rev
SC

Date: Monday, January 30, 2012

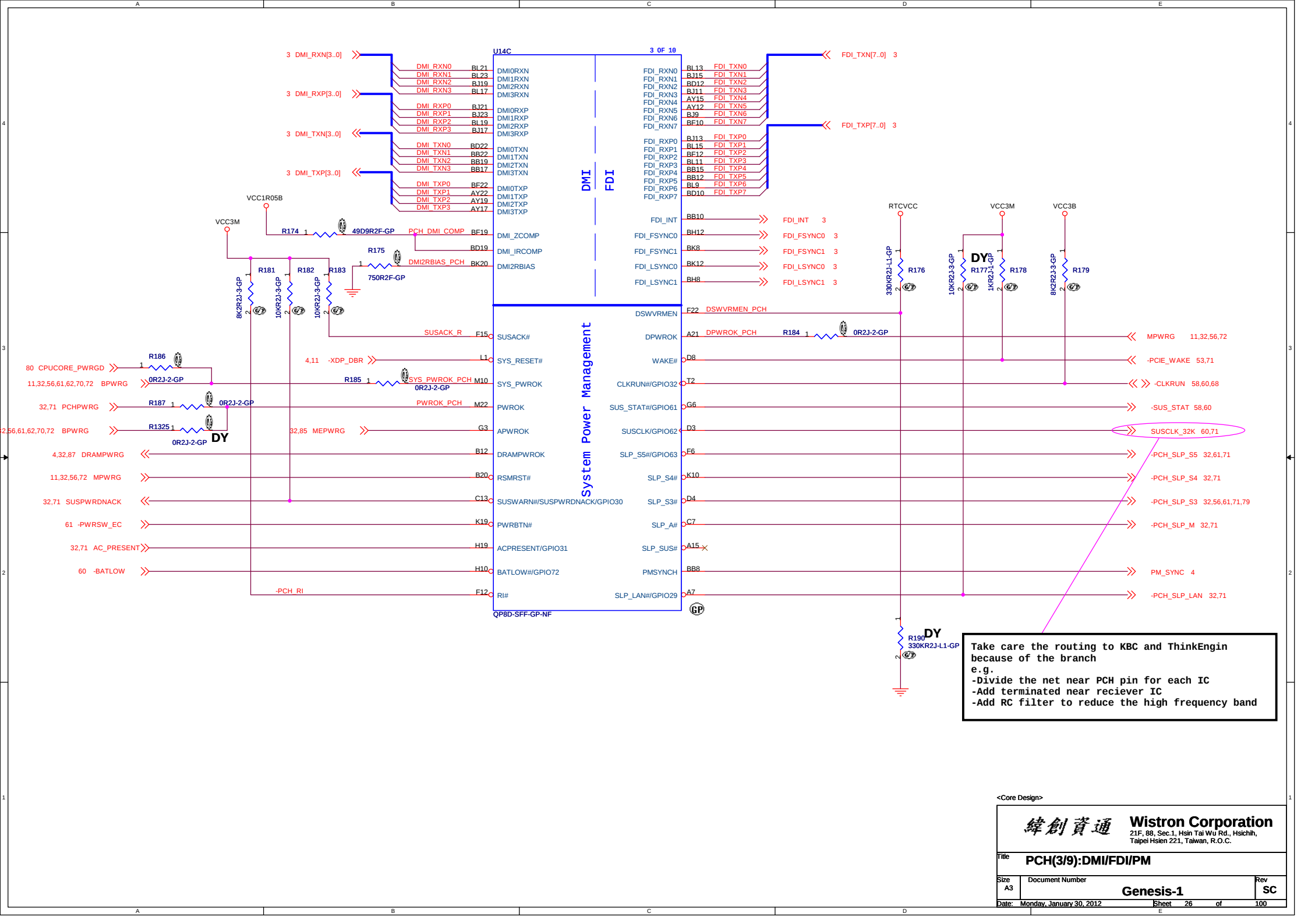
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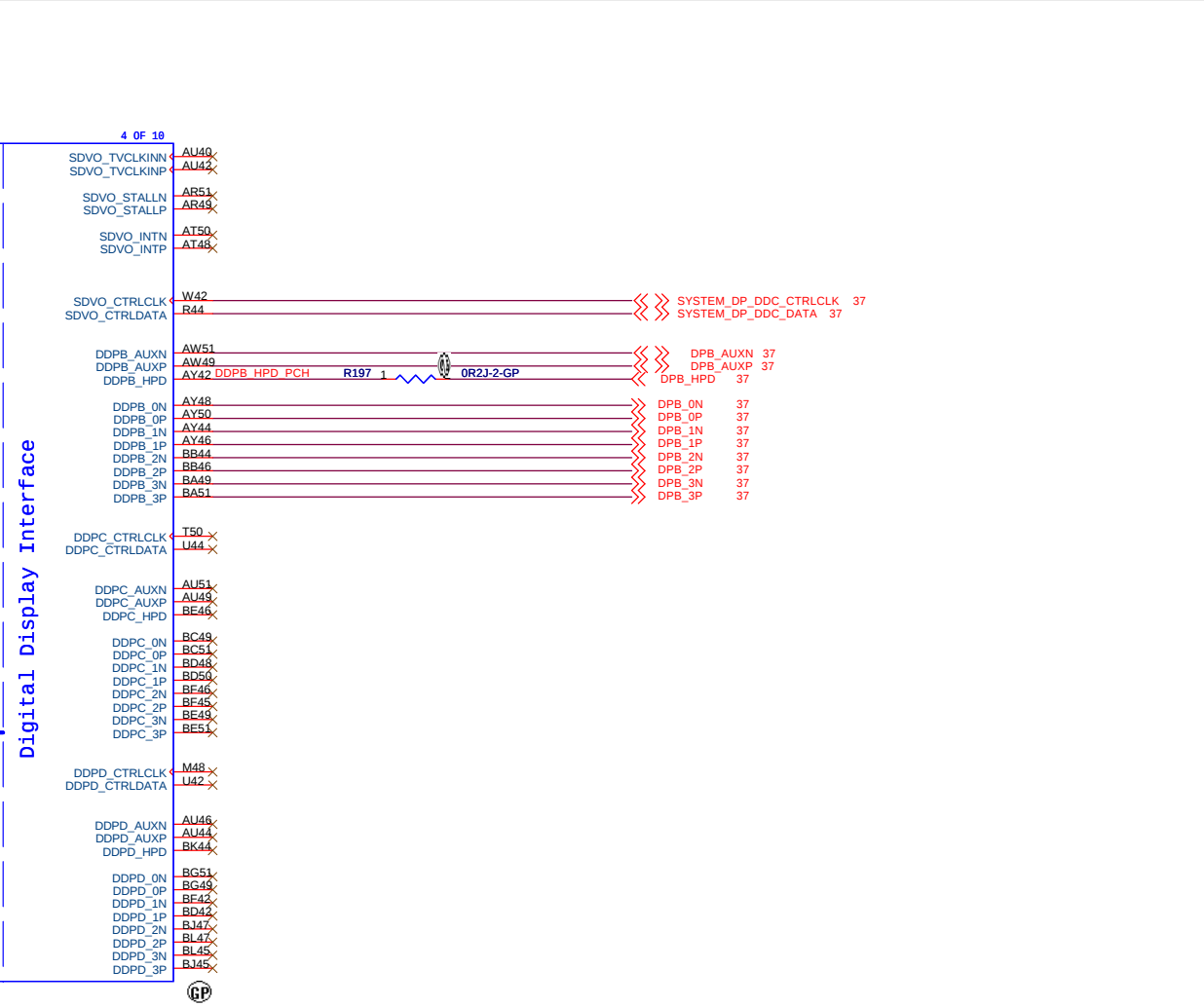
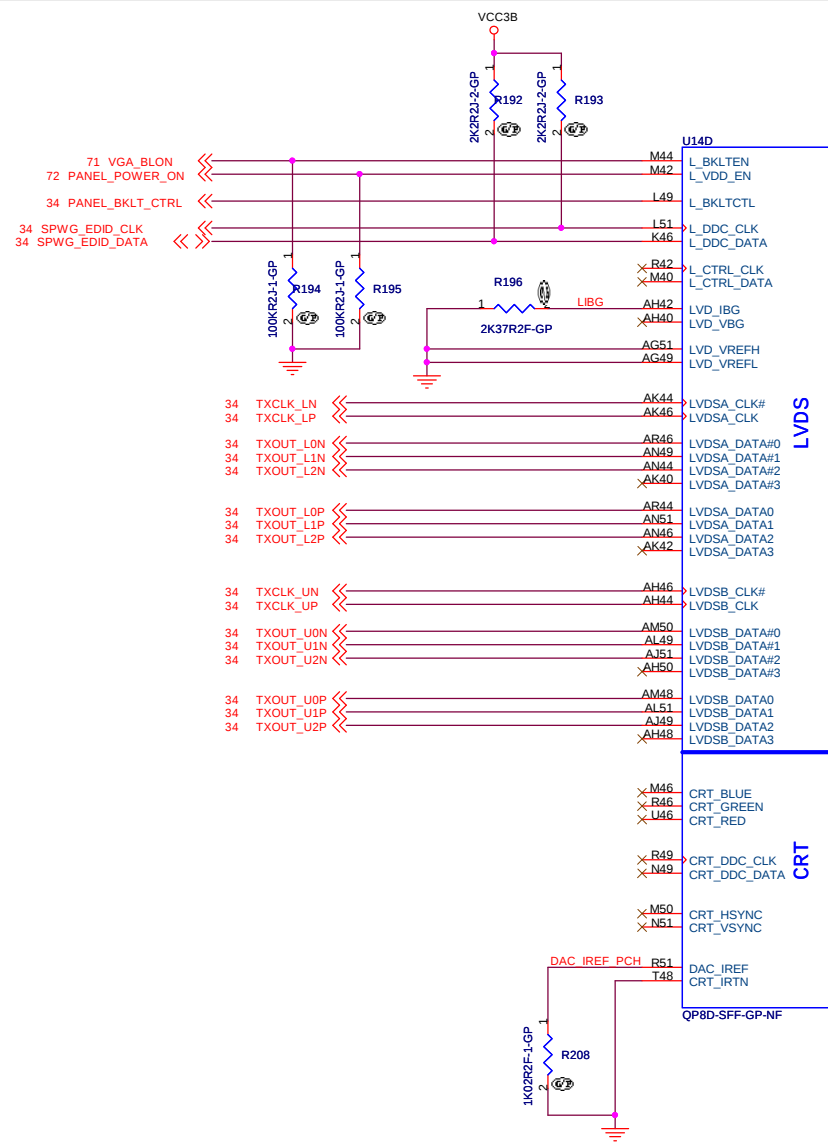


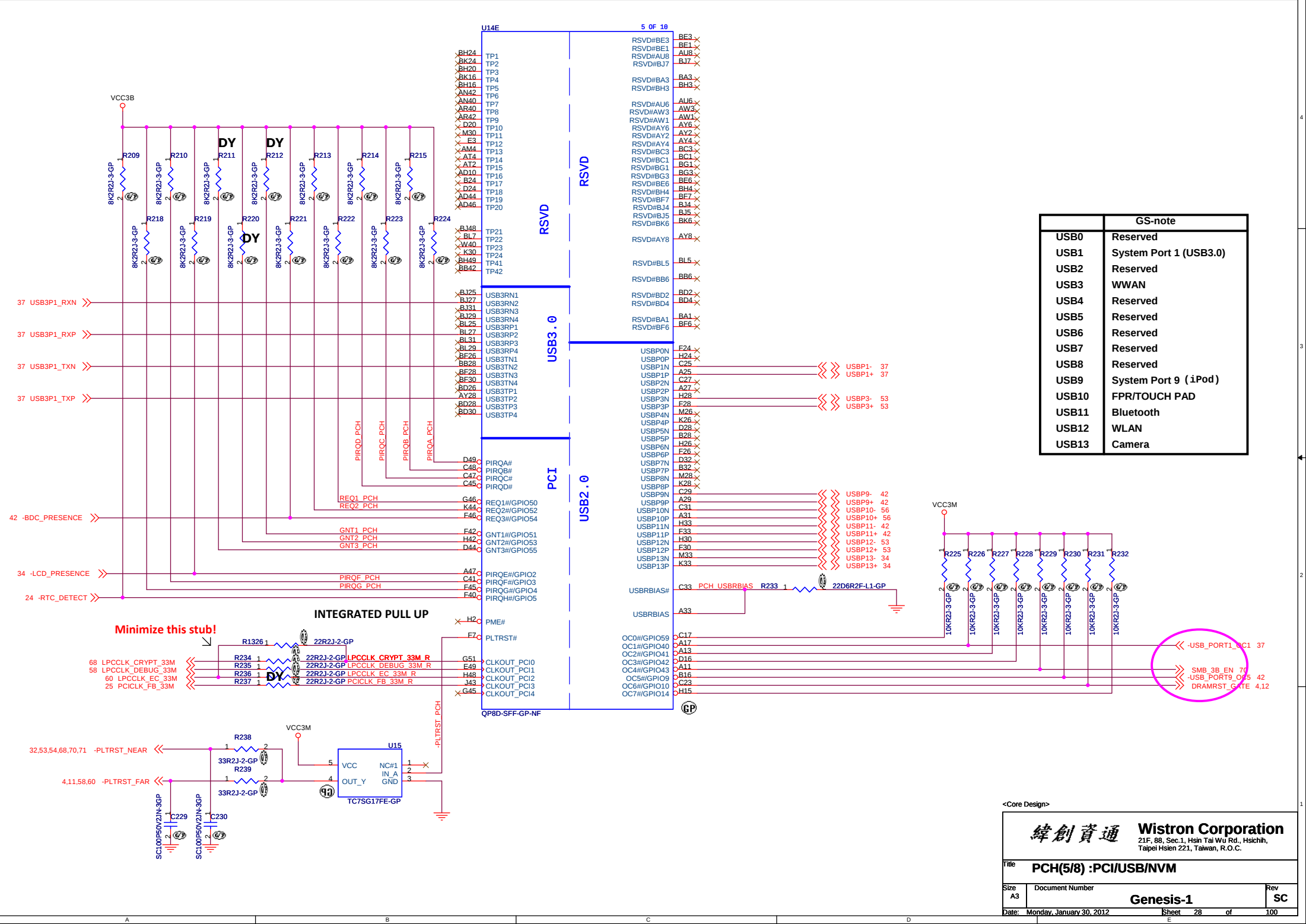
GPIO44	Size
0: Low	46b
1: High	86b

GPIO45	GPIO25	Supplier
0: Low	0: Low	Elpida
0: Low	1: High	Hynix
1: High	0: Low	Samsung
1: High	1: High	Reserved

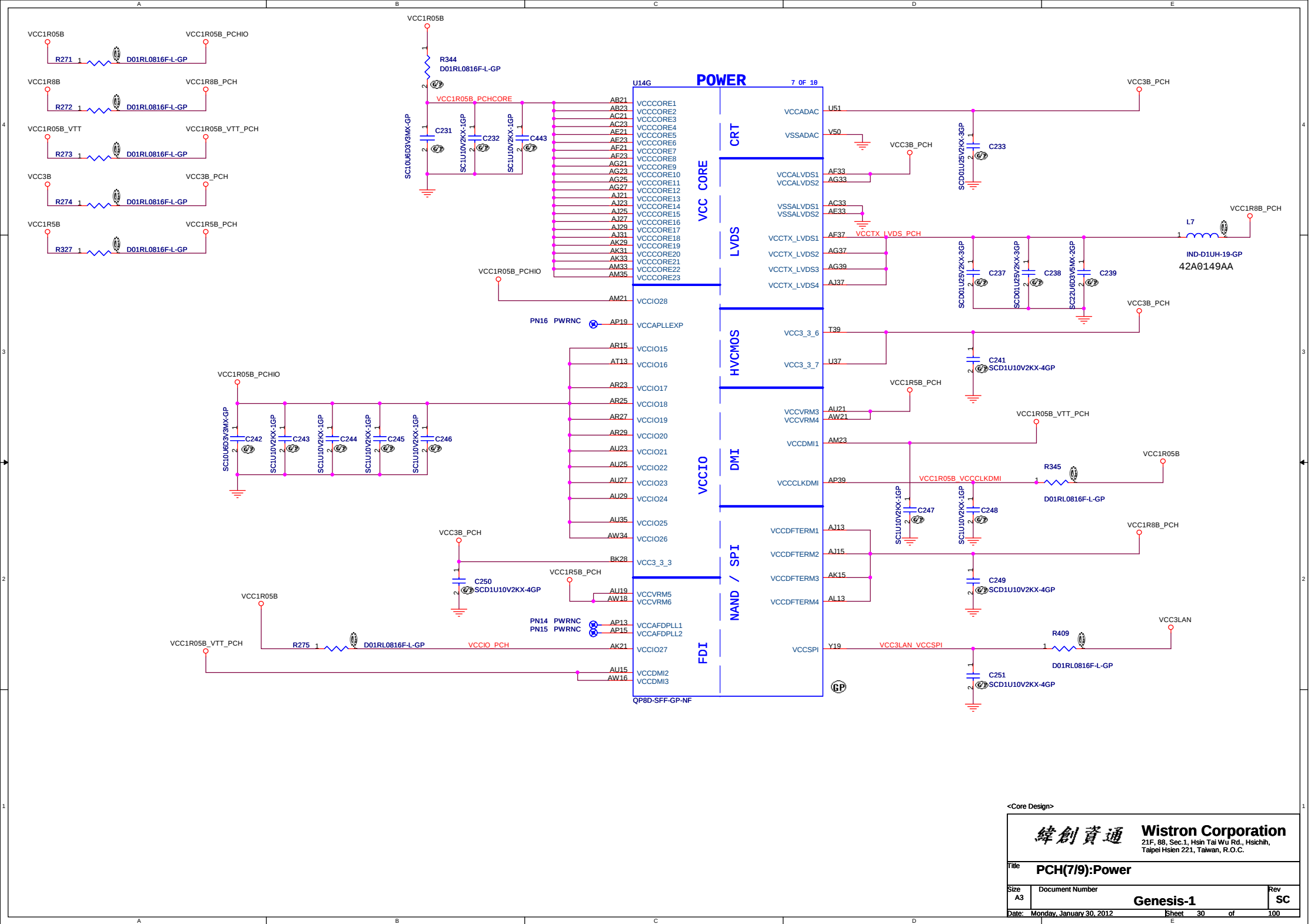
GPIO56	GPIO26	Revision
0: Low	0: Low	A:Initial
0: Low	1: High	B
1: High	0: Low	C
1: High	1: High	D

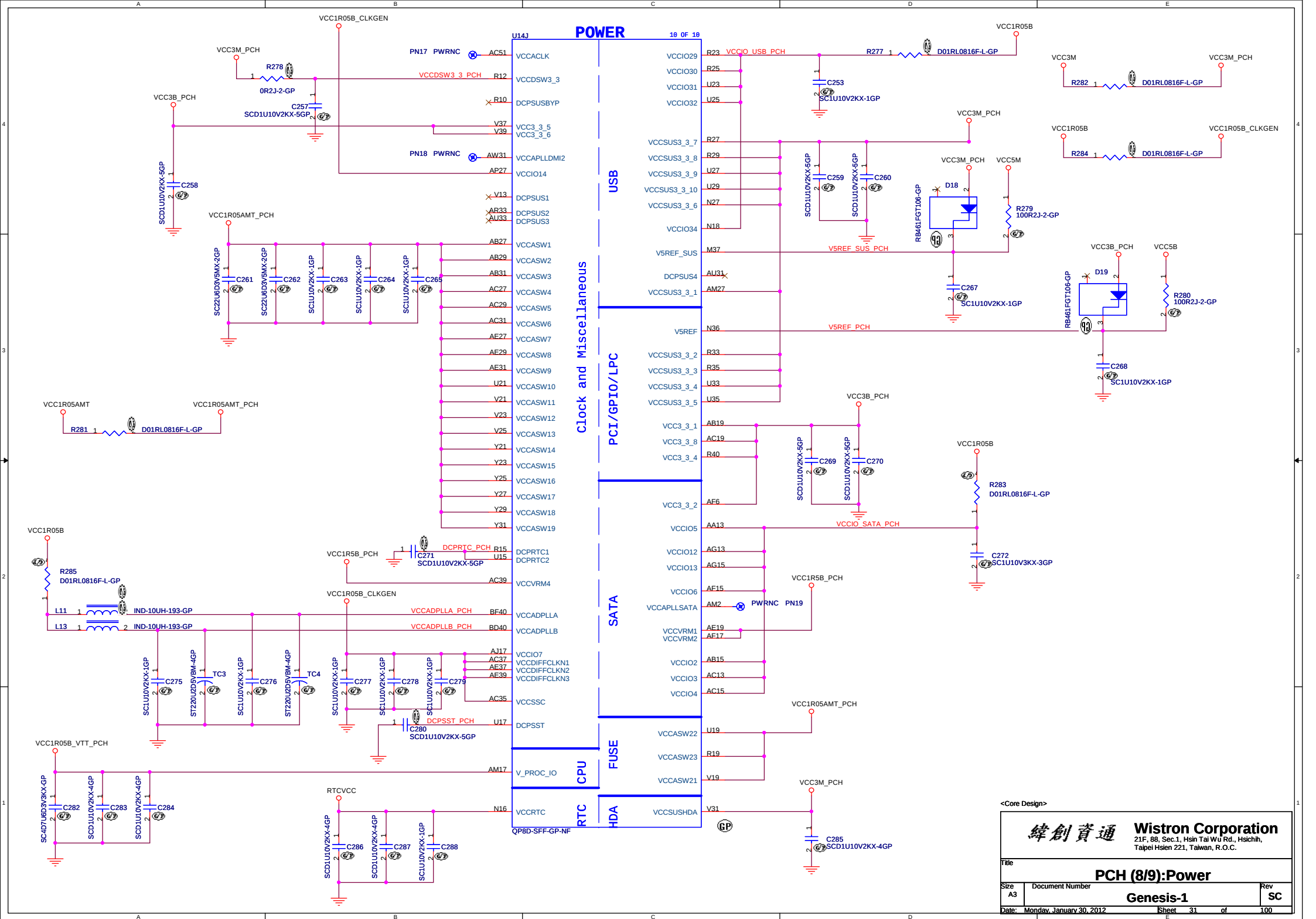




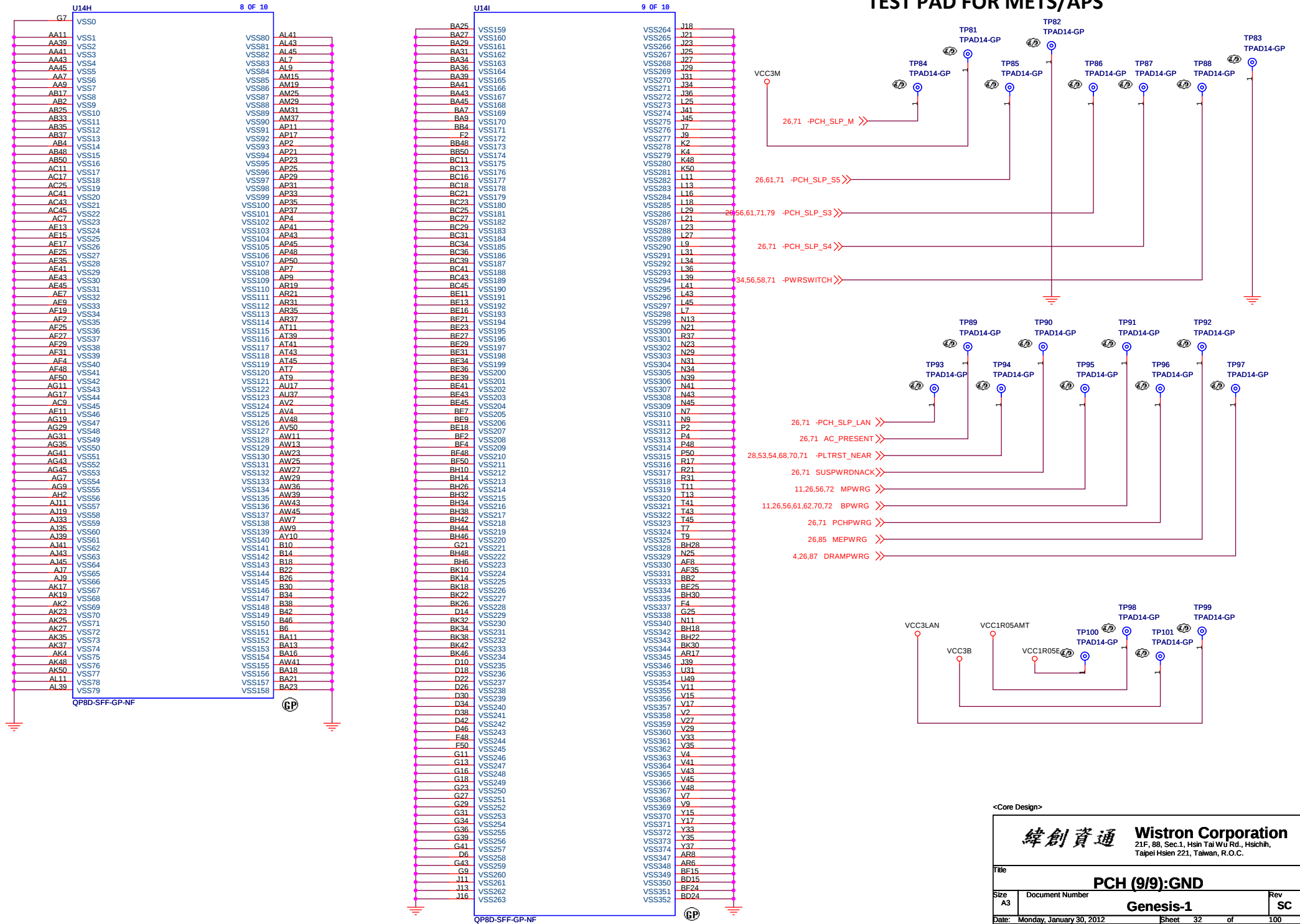


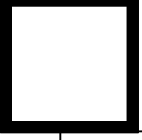
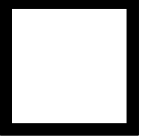
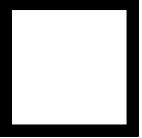
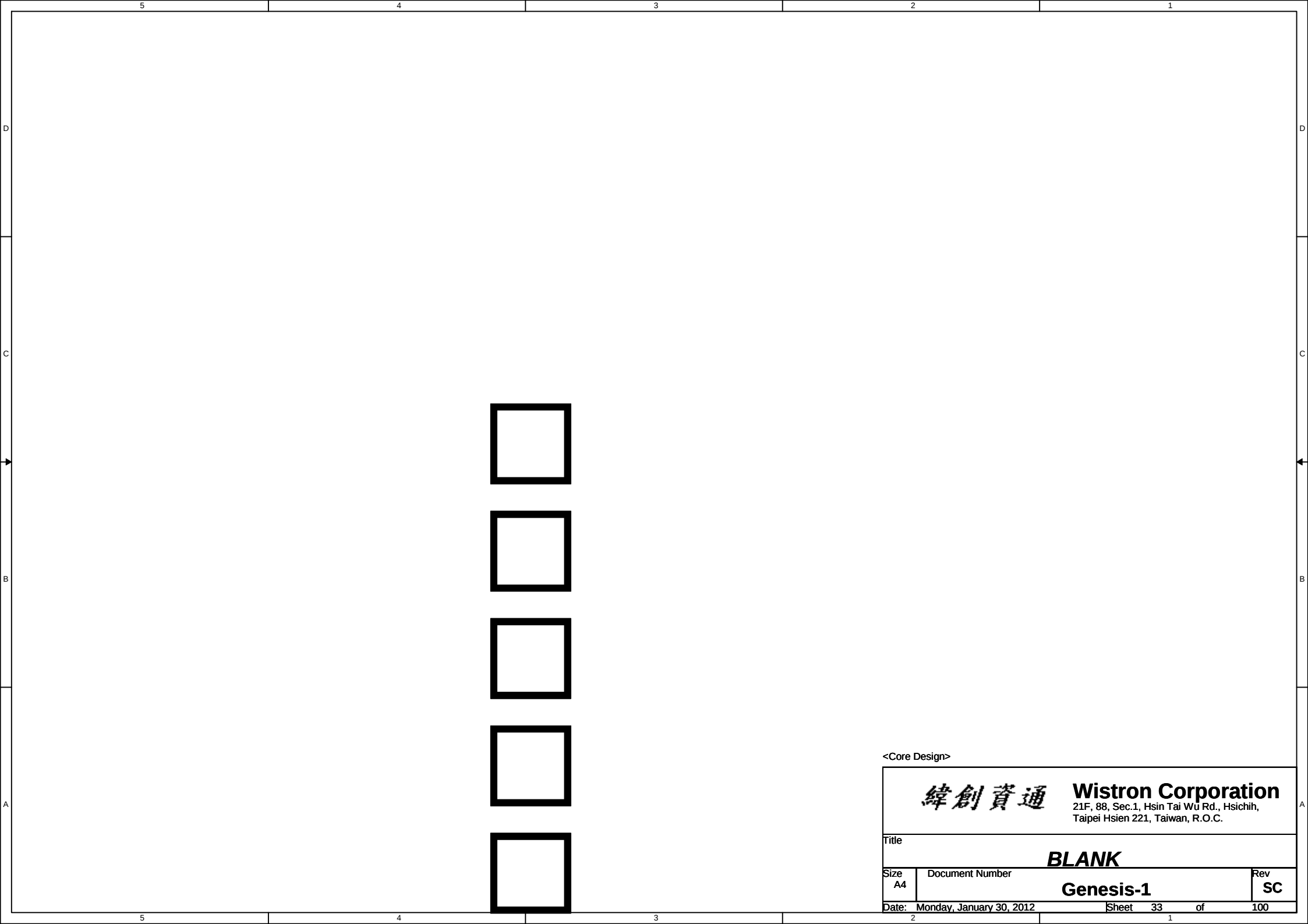
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USB0	Reserved
USB1	System Port 1 (USB3.0)
USB2	Reserved
USB3	WWAN
USB4	Reserved
USB5	Reserved
USB6	Reserved
USB7	Reserved
USB8	Reserved
USB9	System Port 9 (iPod)
USB10	FPR/TOUCH PAD
USB11	Bluetooth
USB12	WLAN
USB13	Camera





TEST PAD FOR METS/APS



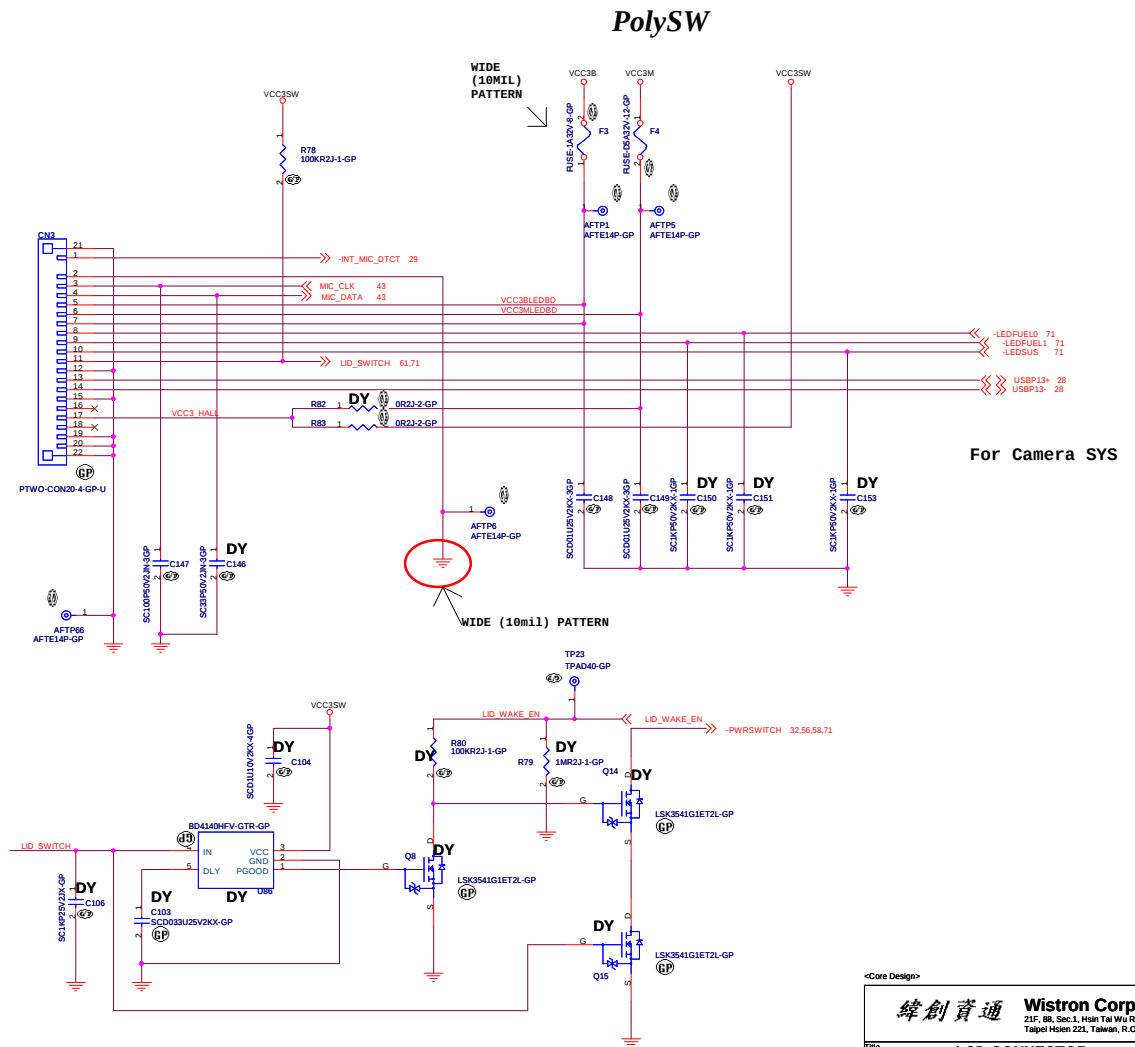
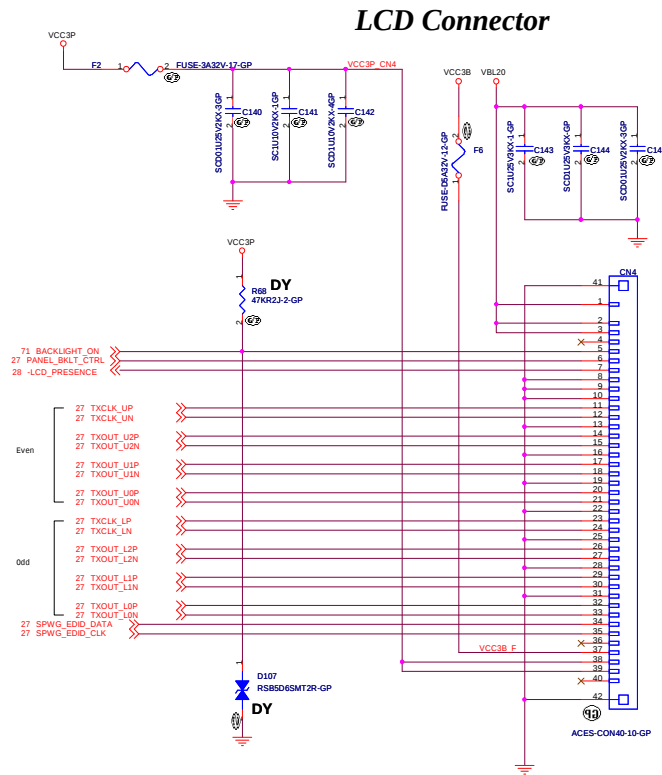
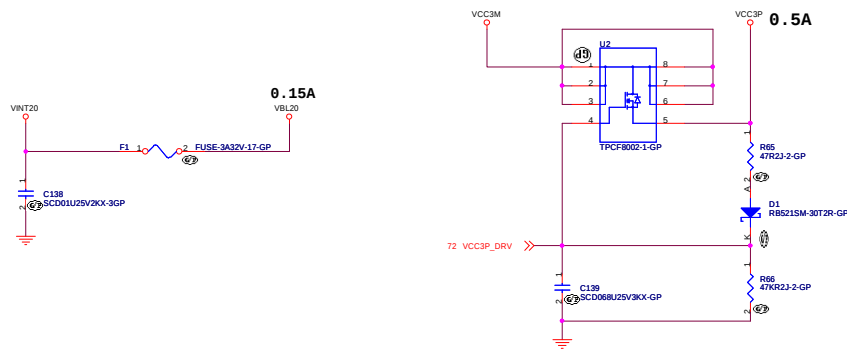


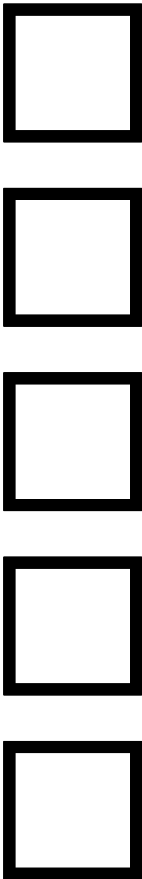
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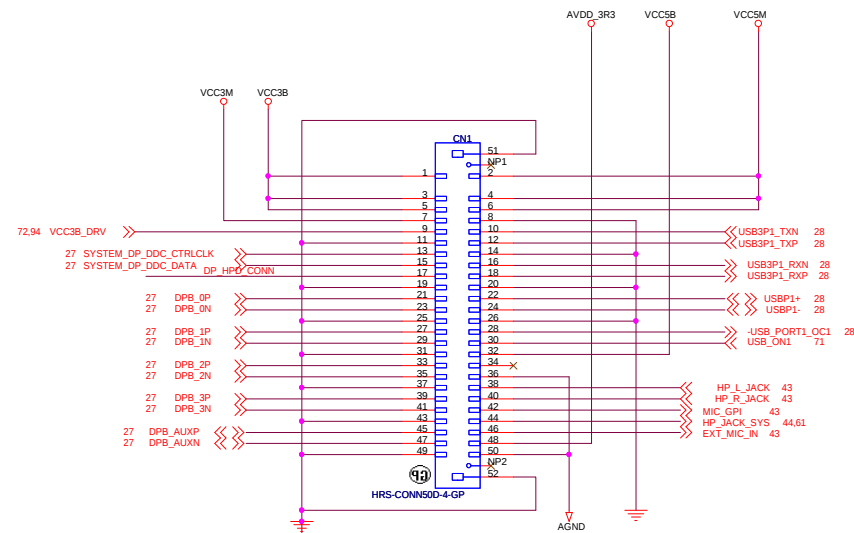
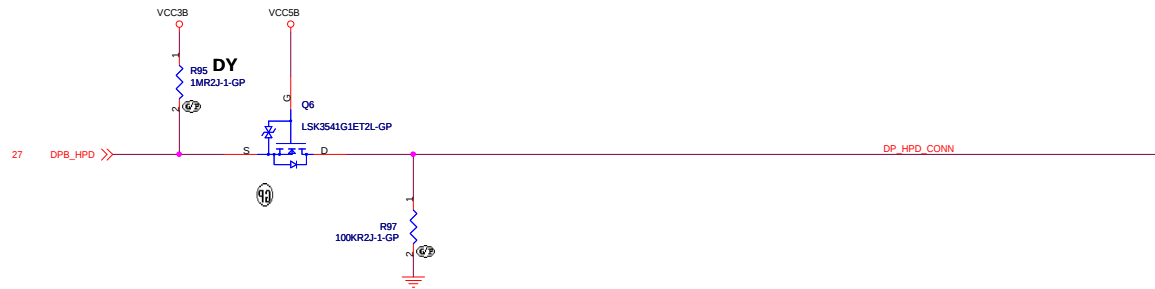
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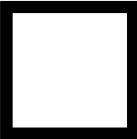
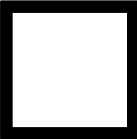
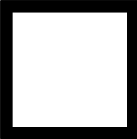
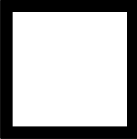
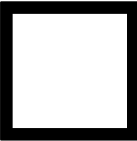
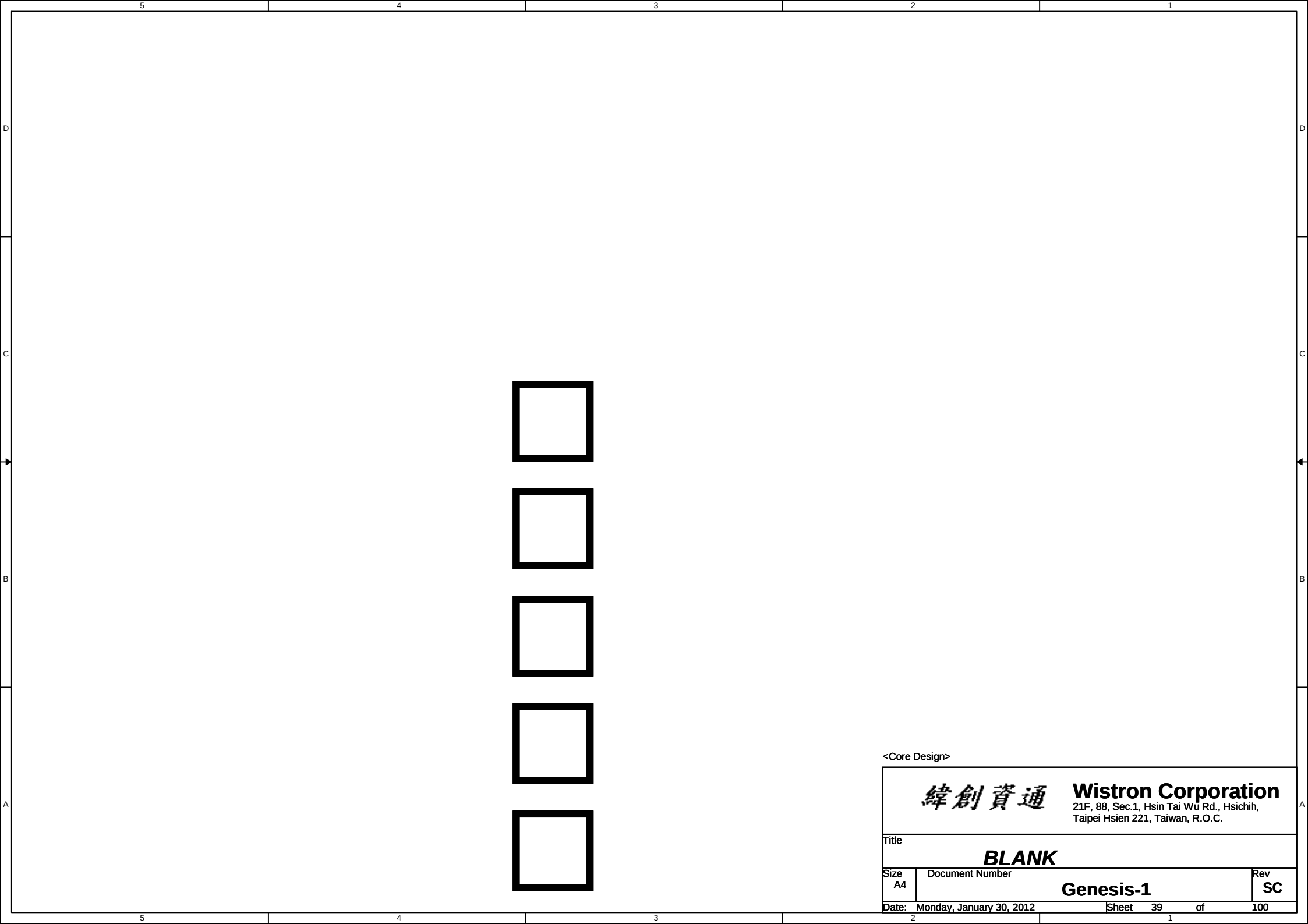
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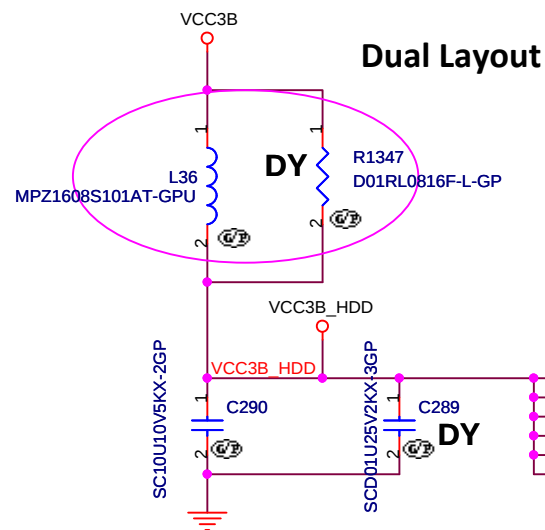
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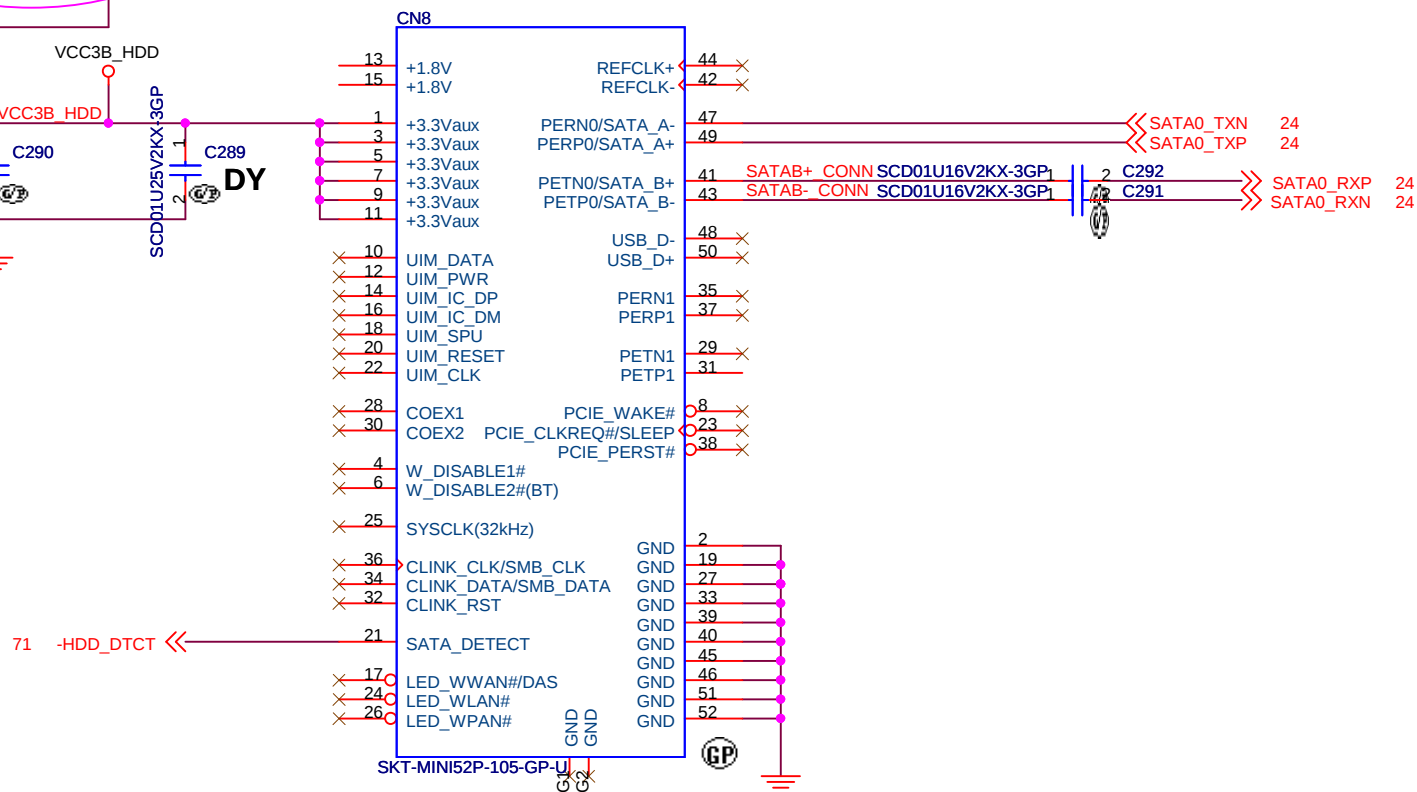


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SATA CONN



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Title

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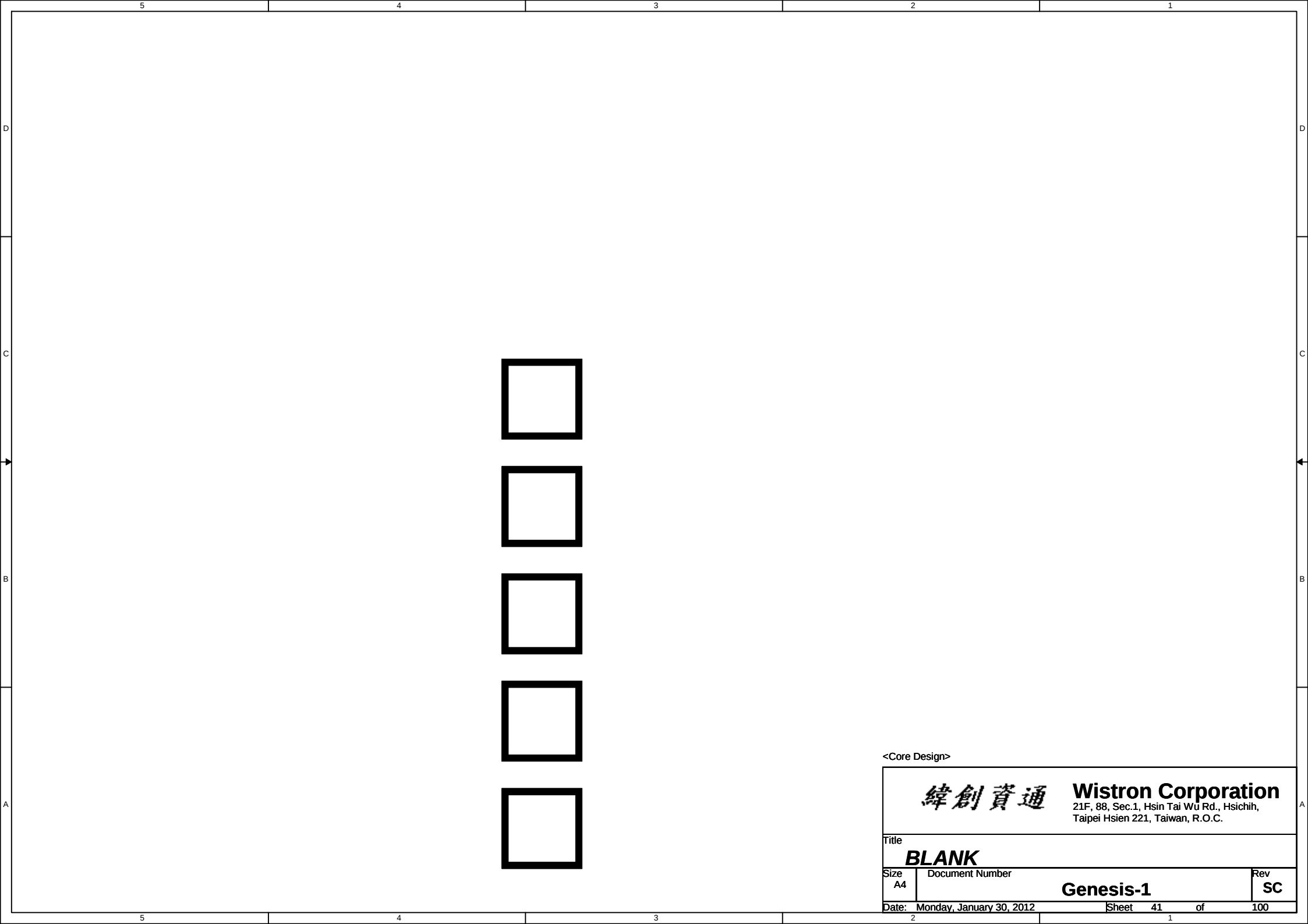
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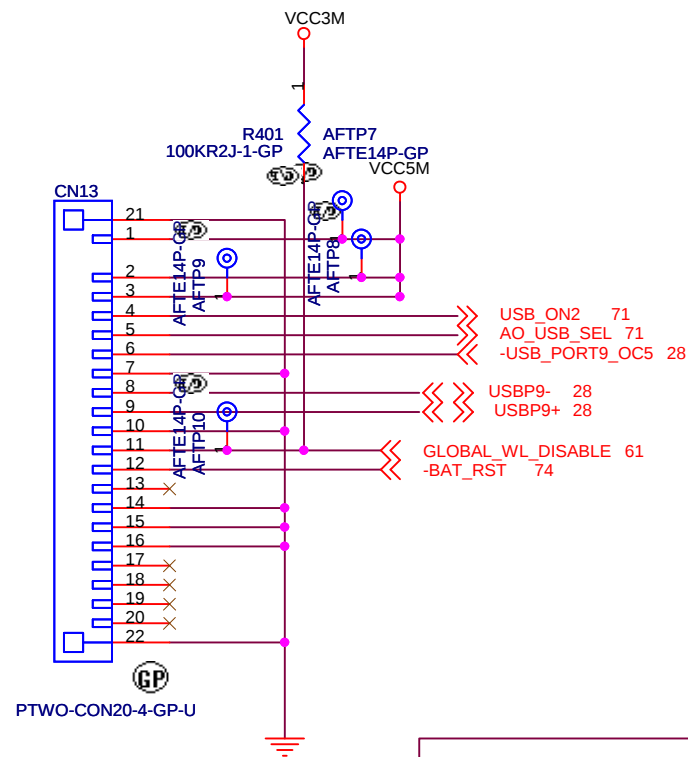
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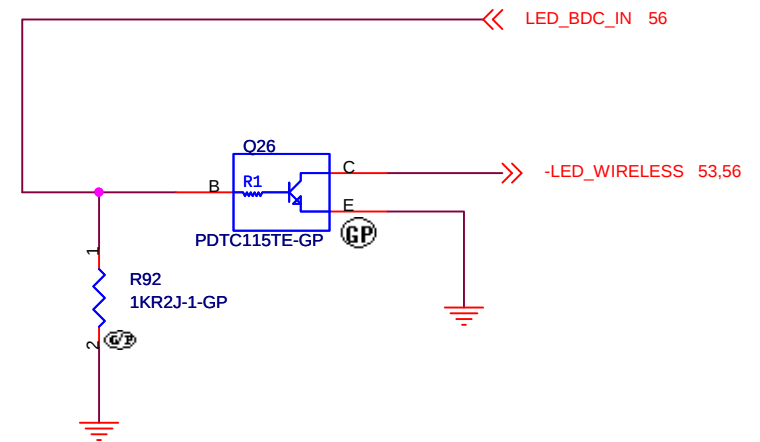
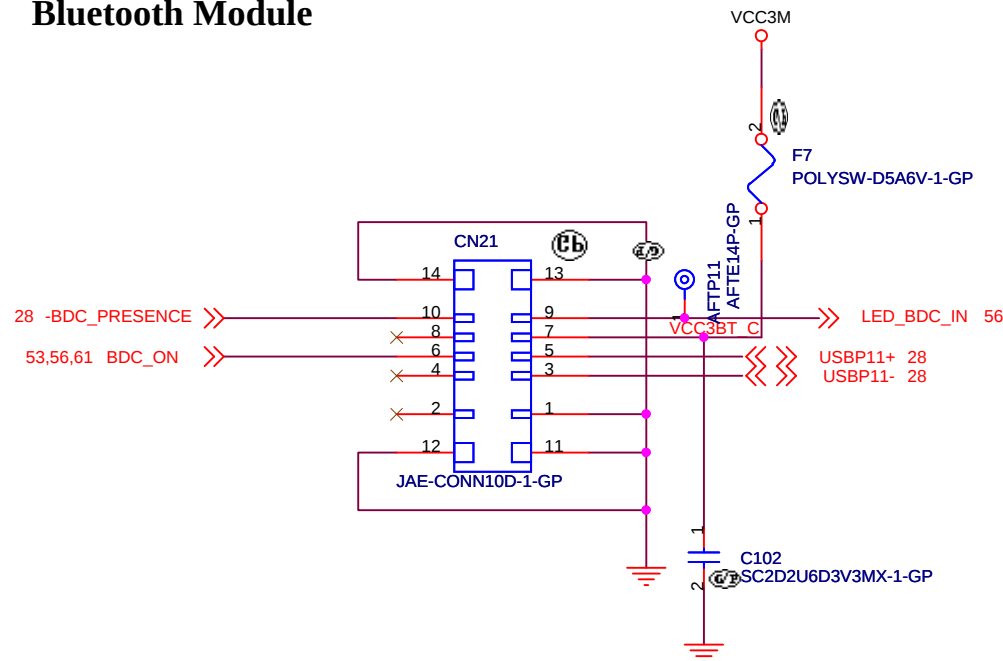
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Bluetooth Module



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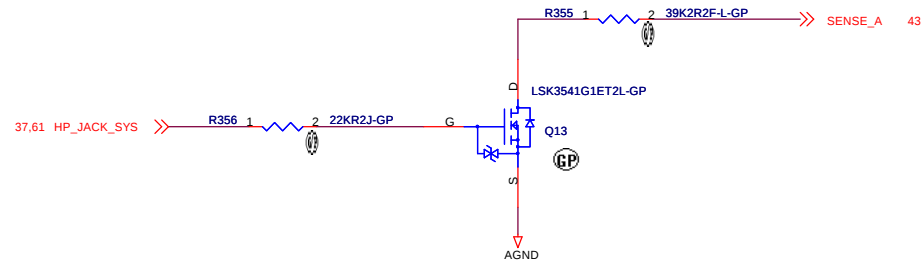
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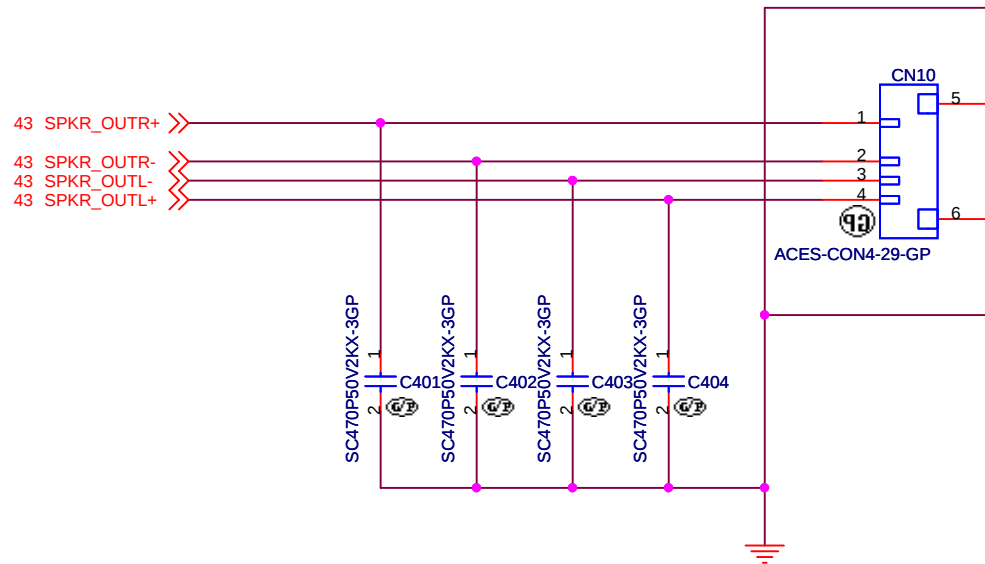
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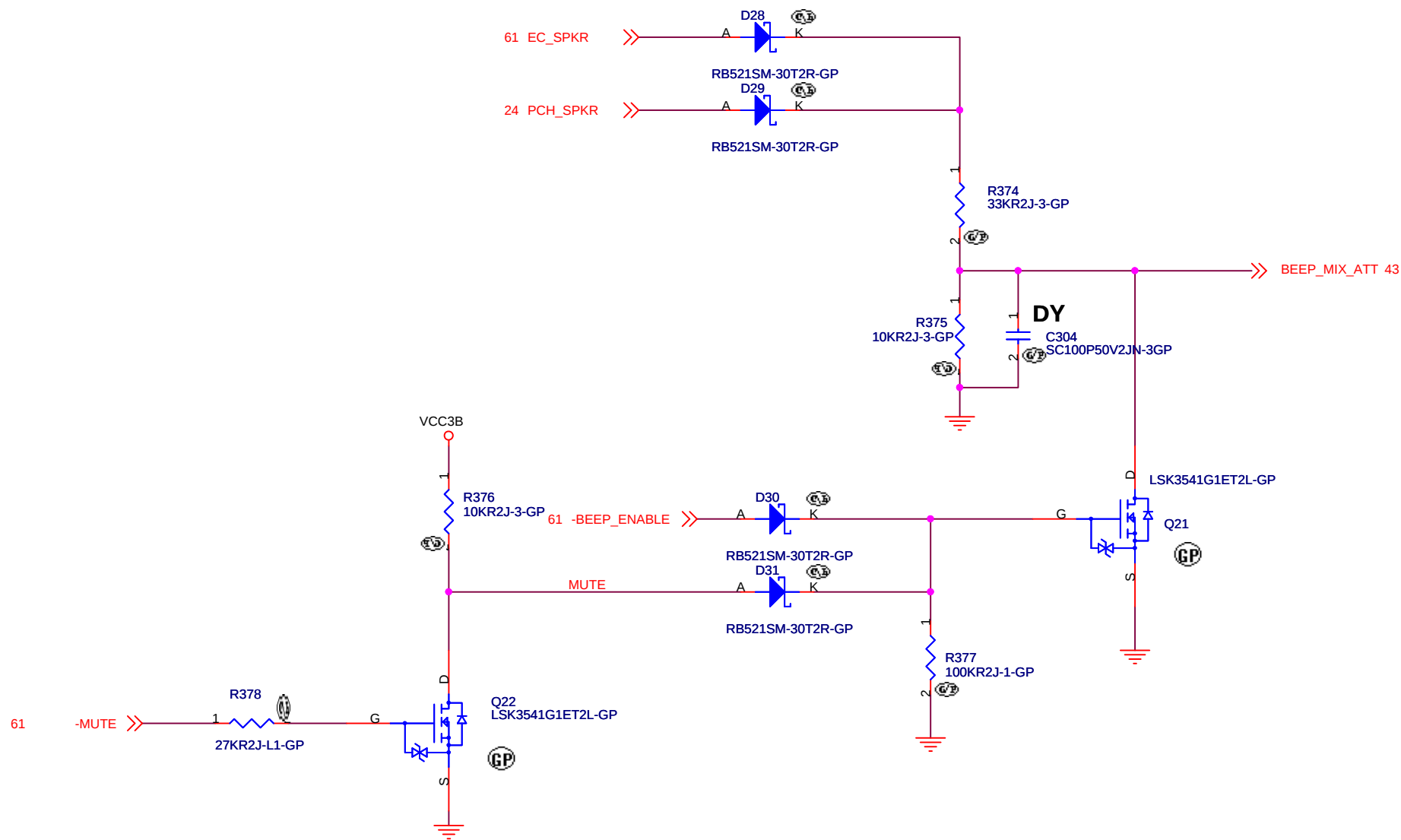
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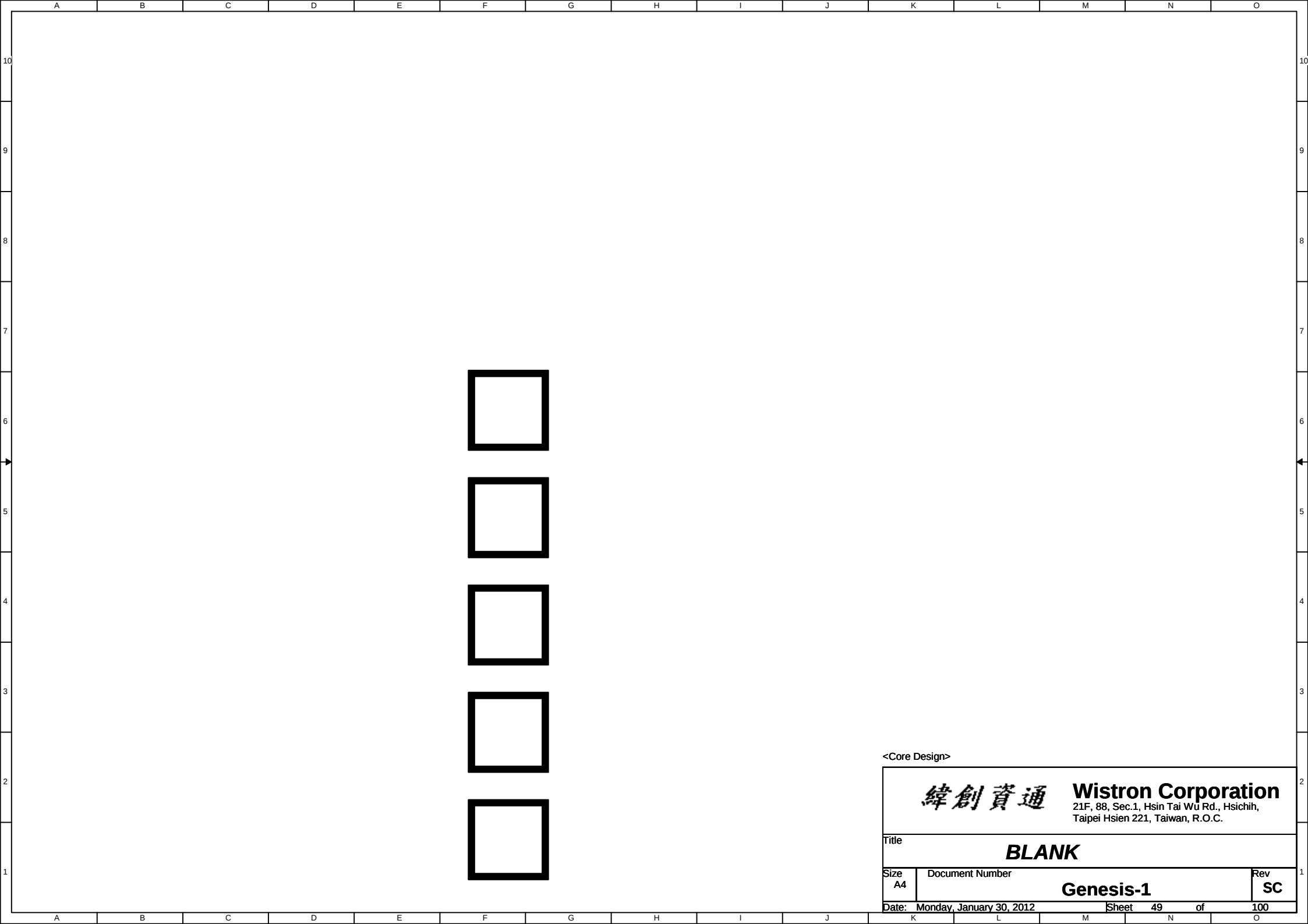
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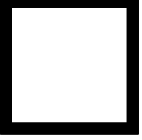
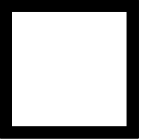
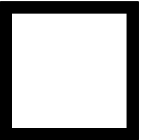
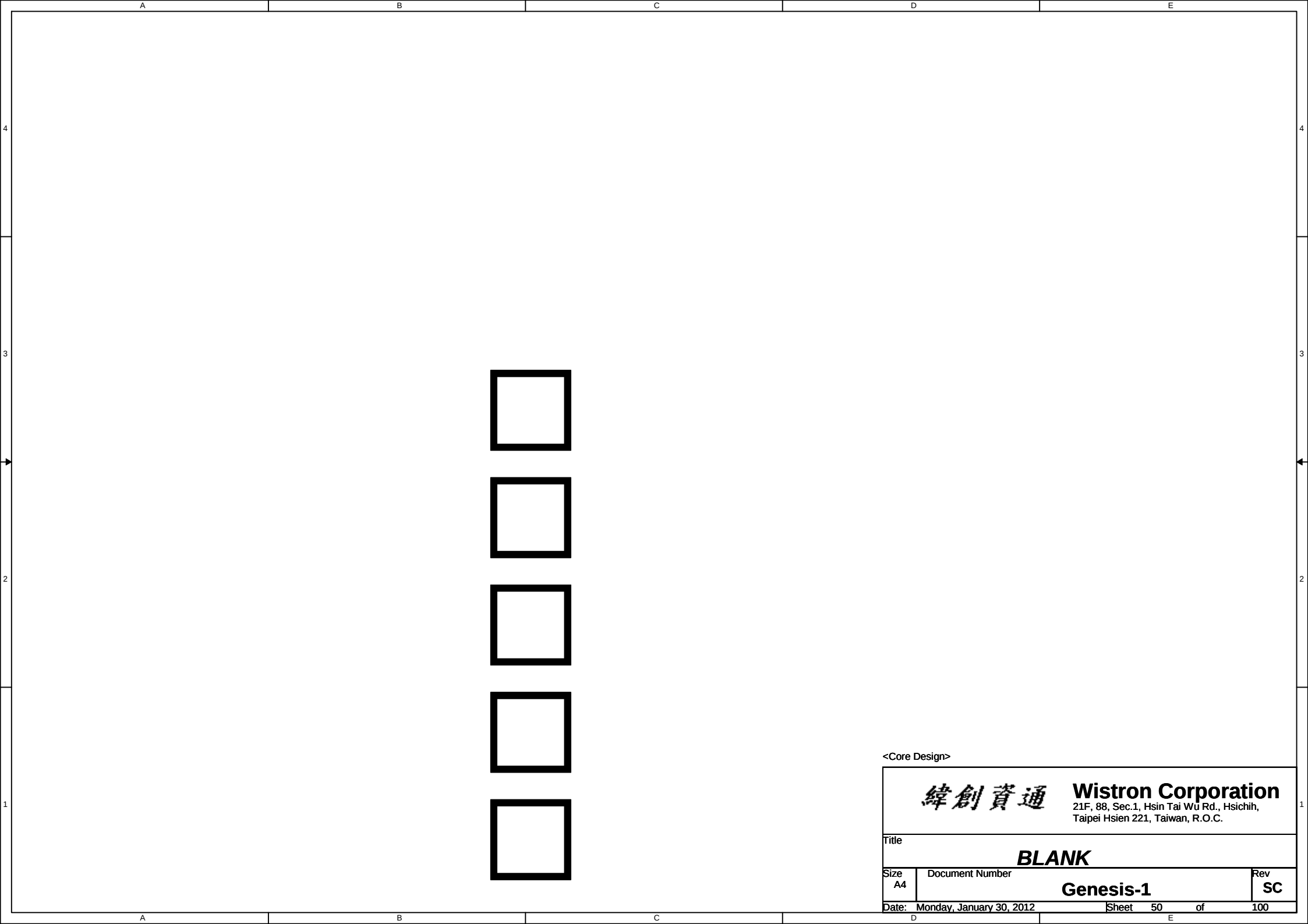
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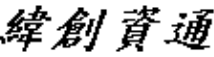


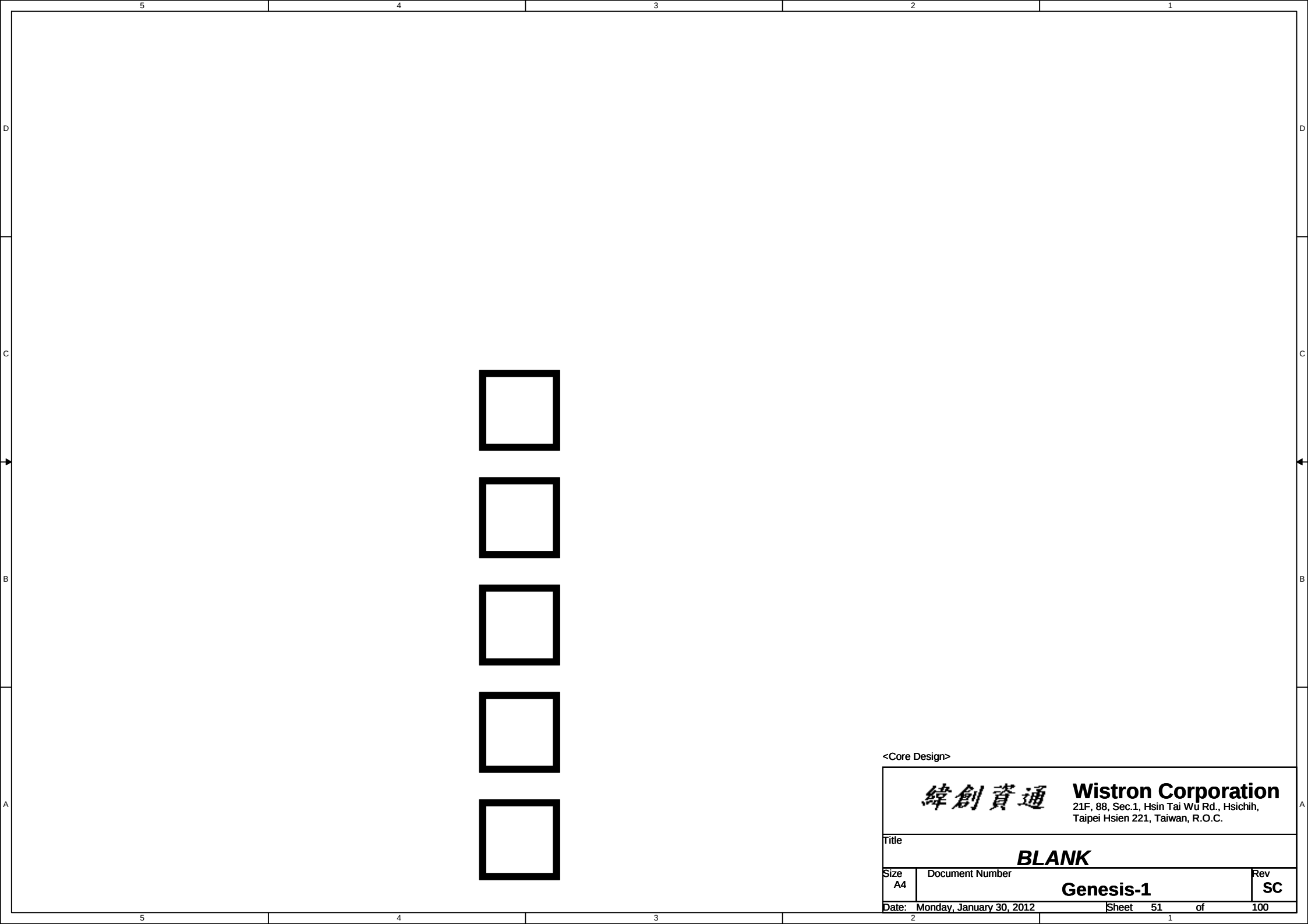
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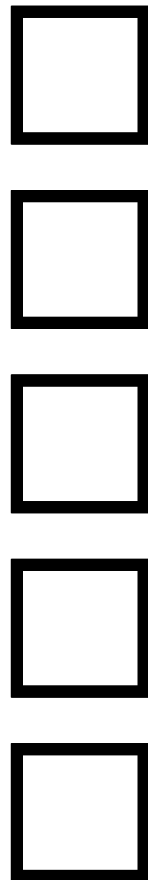
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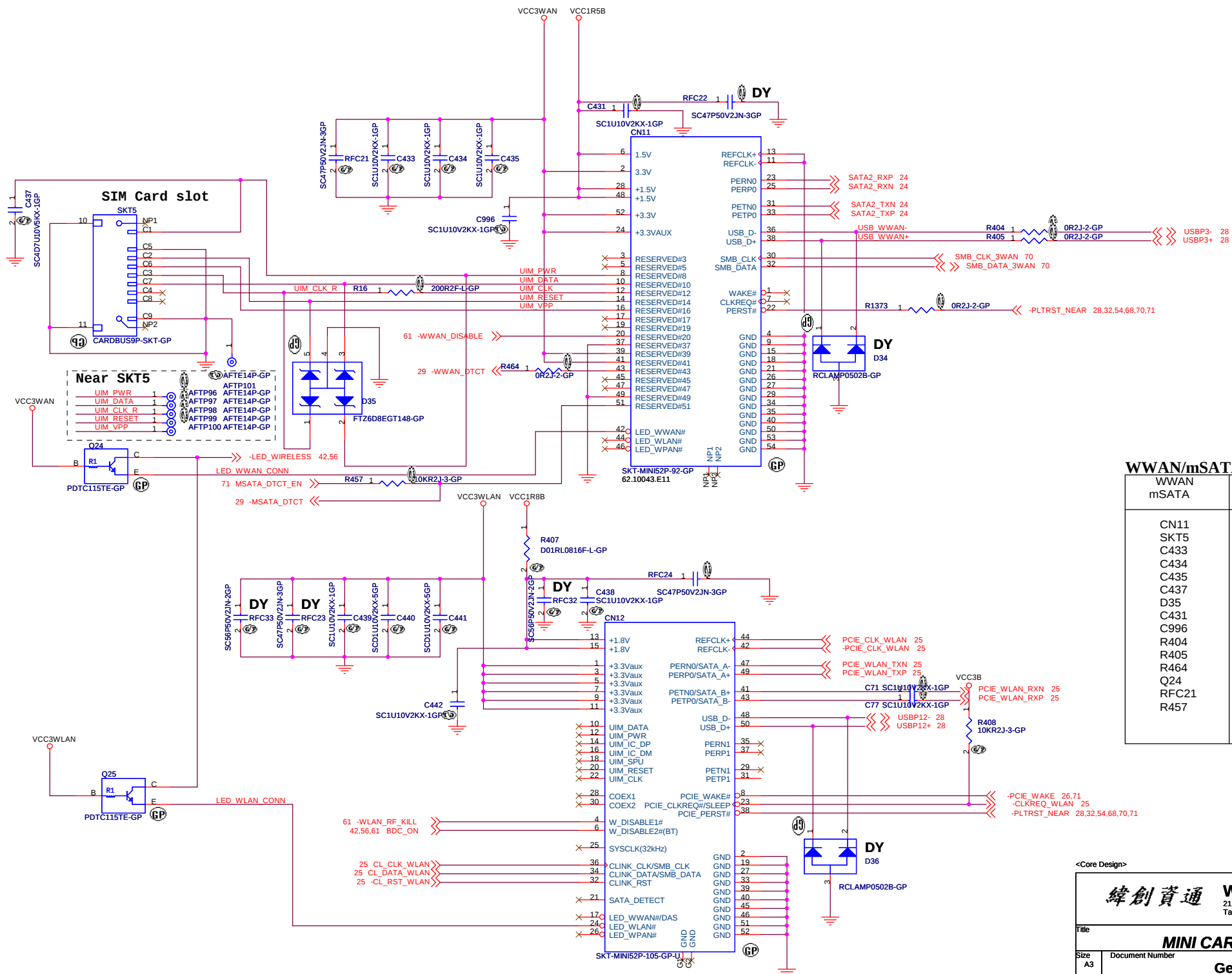
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WWAN/mSATA CONTROL TABLE

WWAN mSATA	YES	NO
CN11	ASM	DY
SKT5	ASM	DY
C433	ASM	DY
C434	ASM	DY
C435	ASM	DY
C437	ASM	DY
D35	ASM	DY
C431	ASM	DY
C996	ASM	DY
R404	ASM	DY
R405	ASM	DY
R464	ASM	DY
Q24	ASM	DY
RFC21	ASM	DY
R457	ASM	DY

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Title

MINI CARD SLOT

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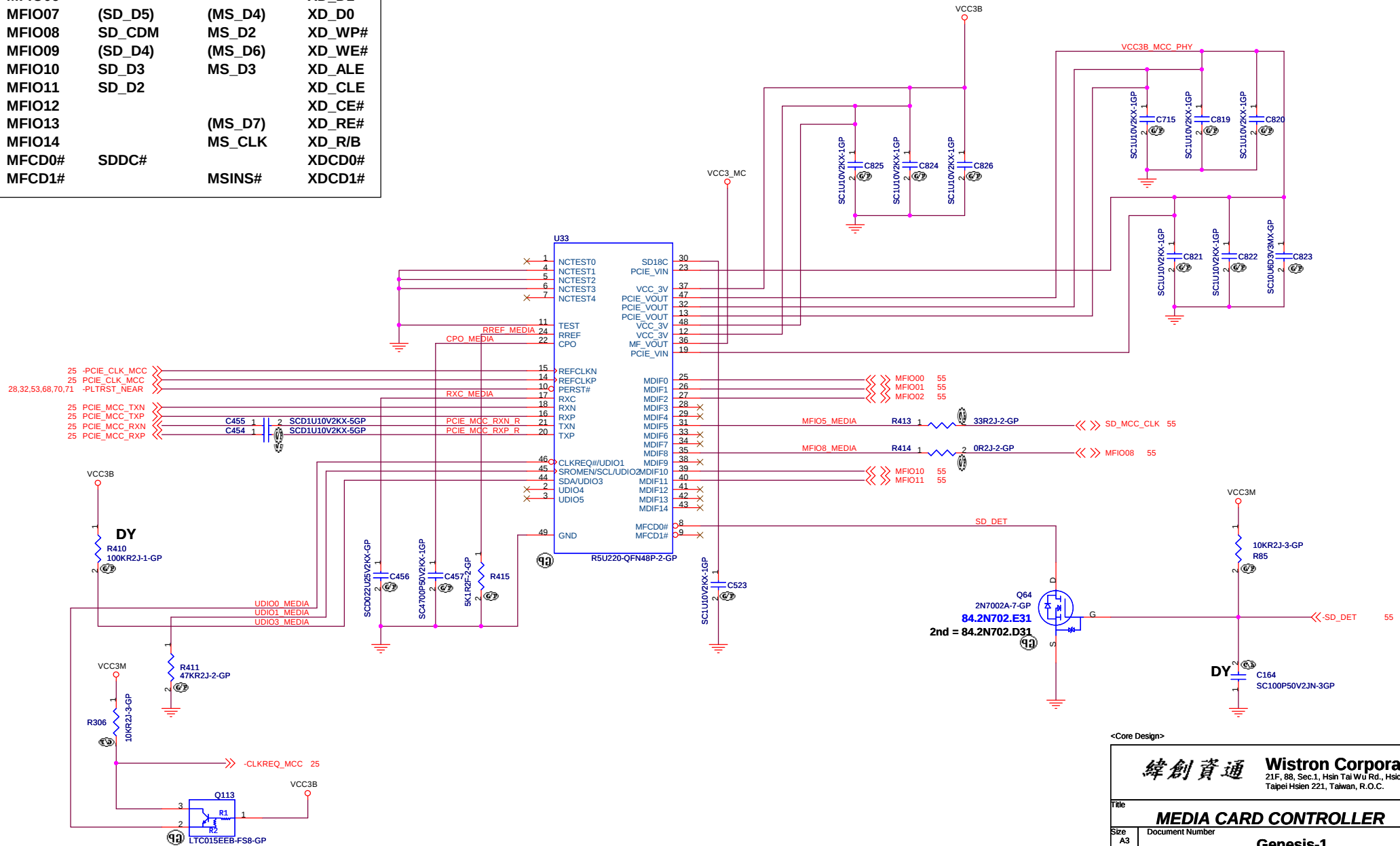
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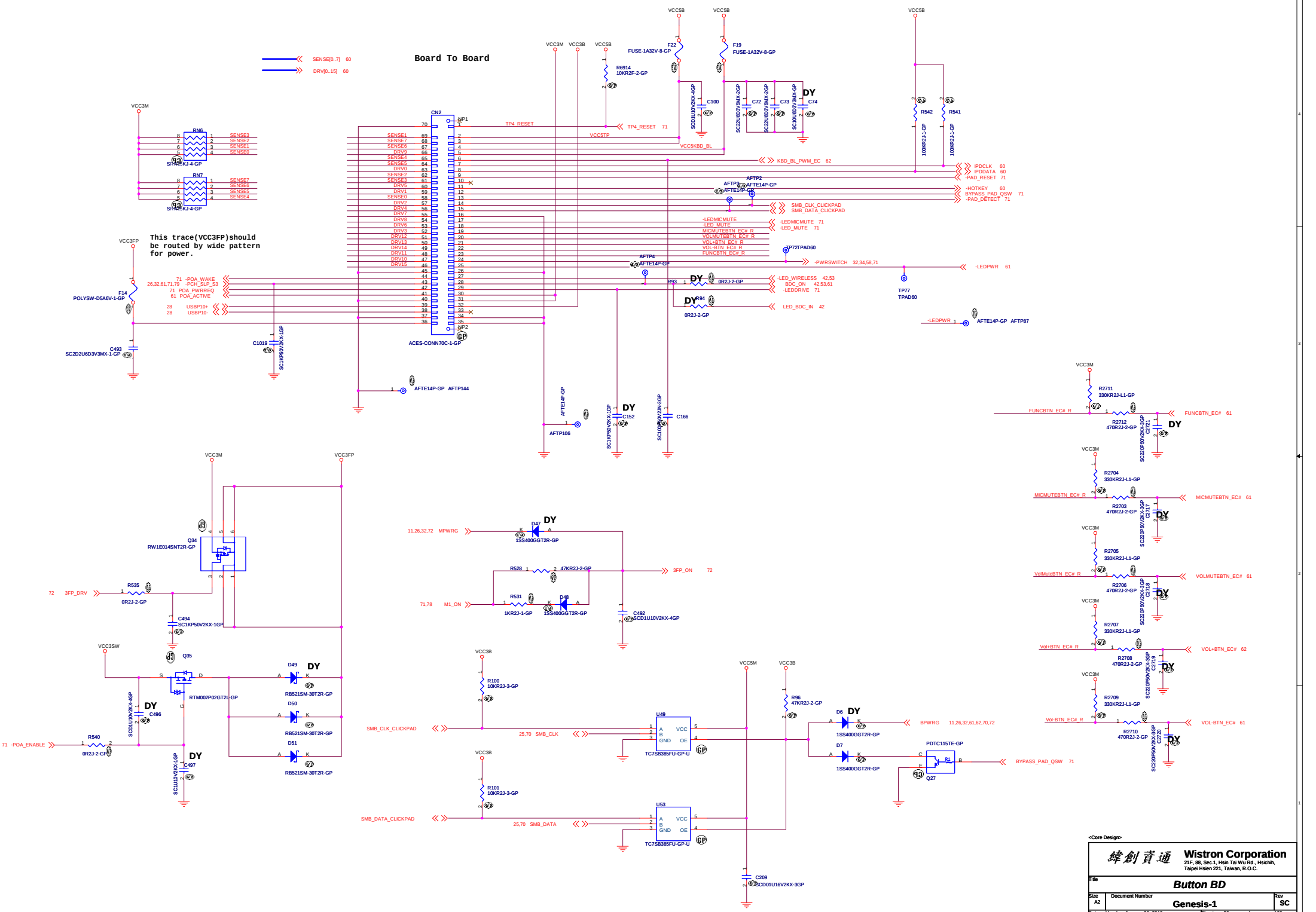
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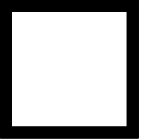
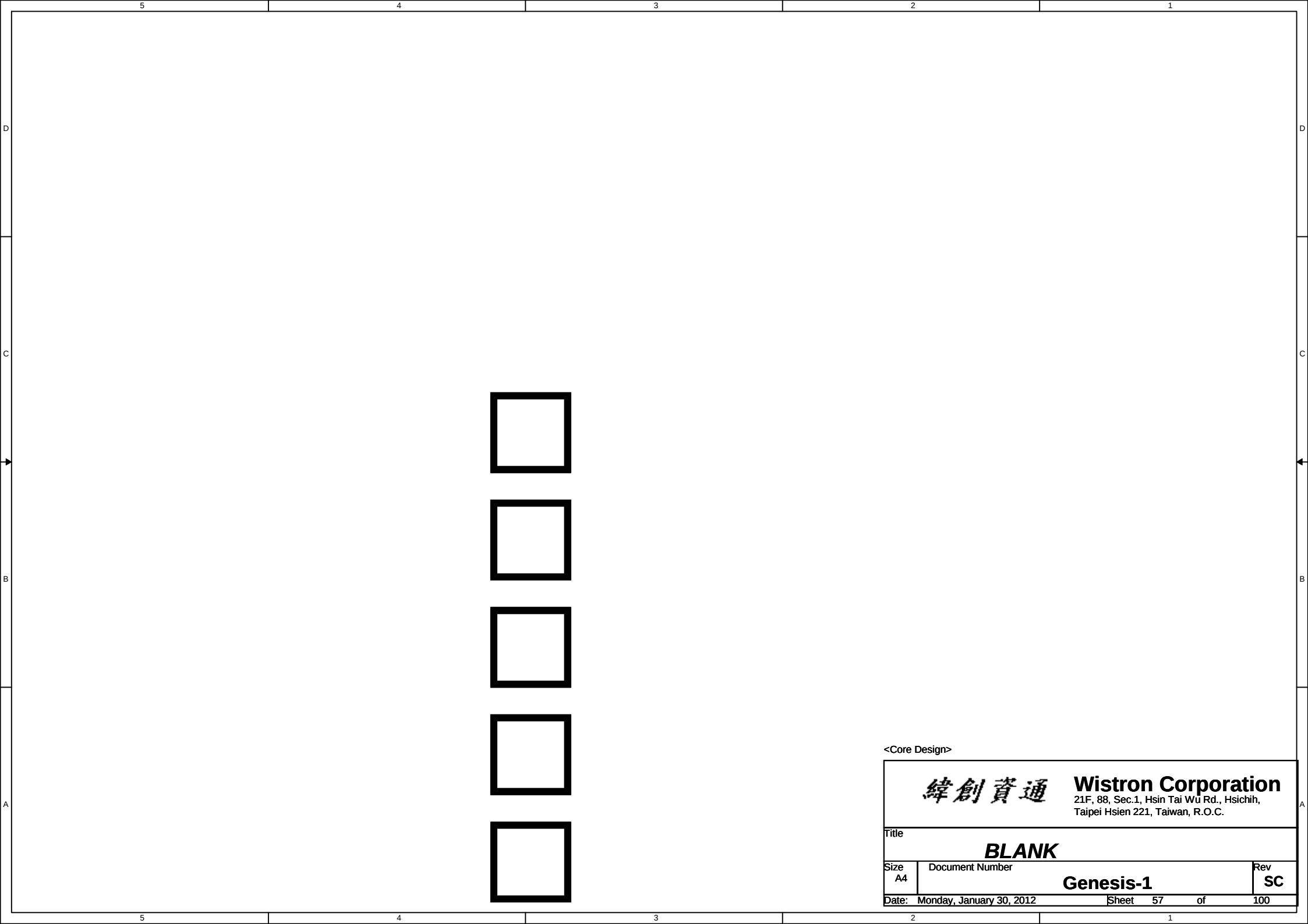
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Genesis-1

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MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#



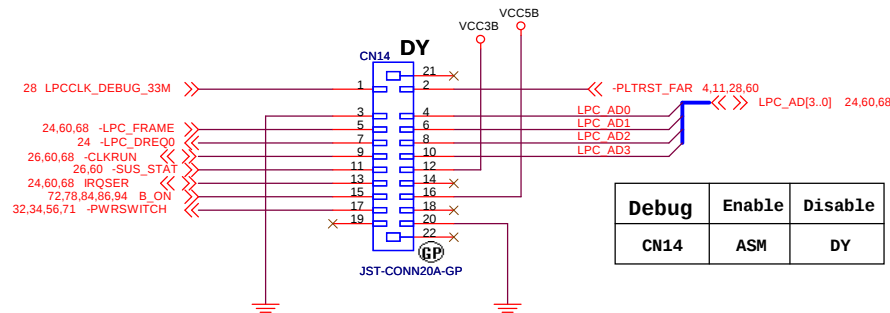




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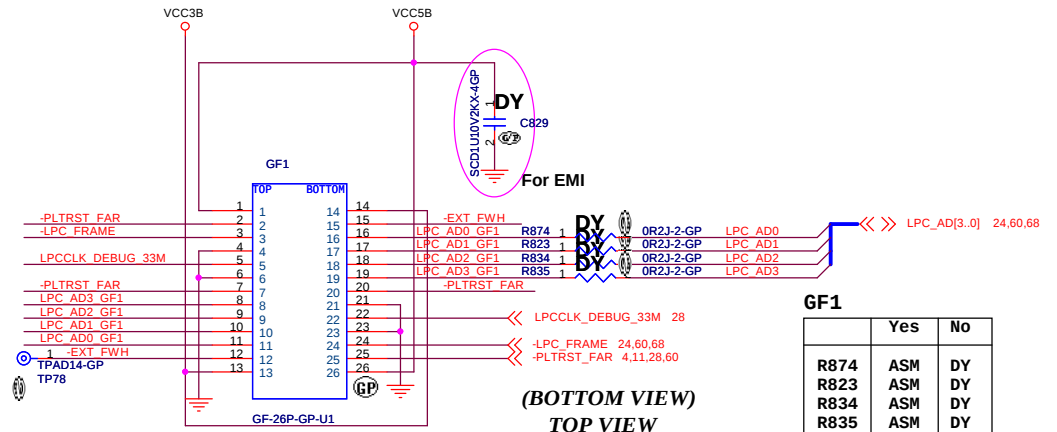
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Debug card connector



Debug	Enable	Disable
CN14	ASM	DY

Golden Finger for Debug Board



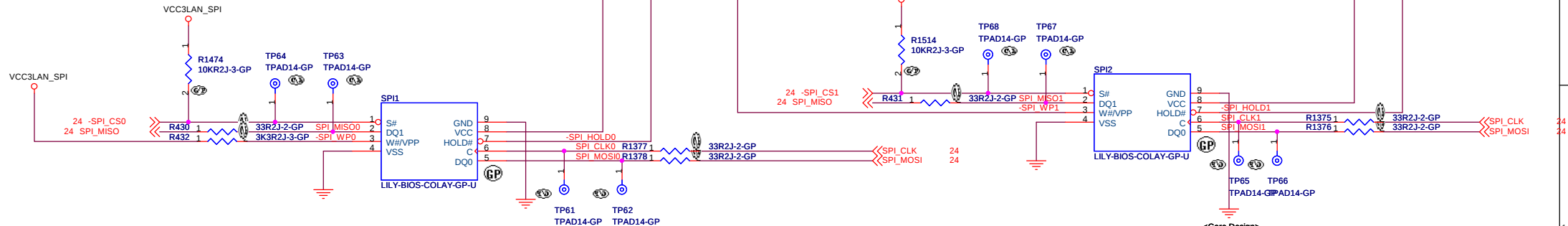
4M

S08	Marcronix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Eon	EN25QH32-104HIP	72.02532.B01
	Numonyx	N25Q032A13ESEC0	72.25Q32.C01
8M			
S08	Marcronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Eon	EN25QH64-104HIP	72.02564.001
	Numonyx	N25Q064A13ESEC0	72.25Q64.G01
16M			
WS08	Marcronix	MX25L12836EZNI-10G	wait for P/N
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF8C0	

Configuration Table

	CONFIG-1 16MB	CONFIG-2 12MB	CONFIG-3 8MB
SPI1	16MB	8MB	8MB
SPI2	DY	4MB	DY
R429	DY	ASM	DY
R431	DY	ASM	DY
R433	DY	ASM	DY
R1375	DY	ASM	DY
R1376	DY	ASM	DY
C471	DY	ASM	DY
R1514	DY	ASM	DY
R149(p24)	DY	ASM	DY

Logic



SO8 and WSON8 are both supported!

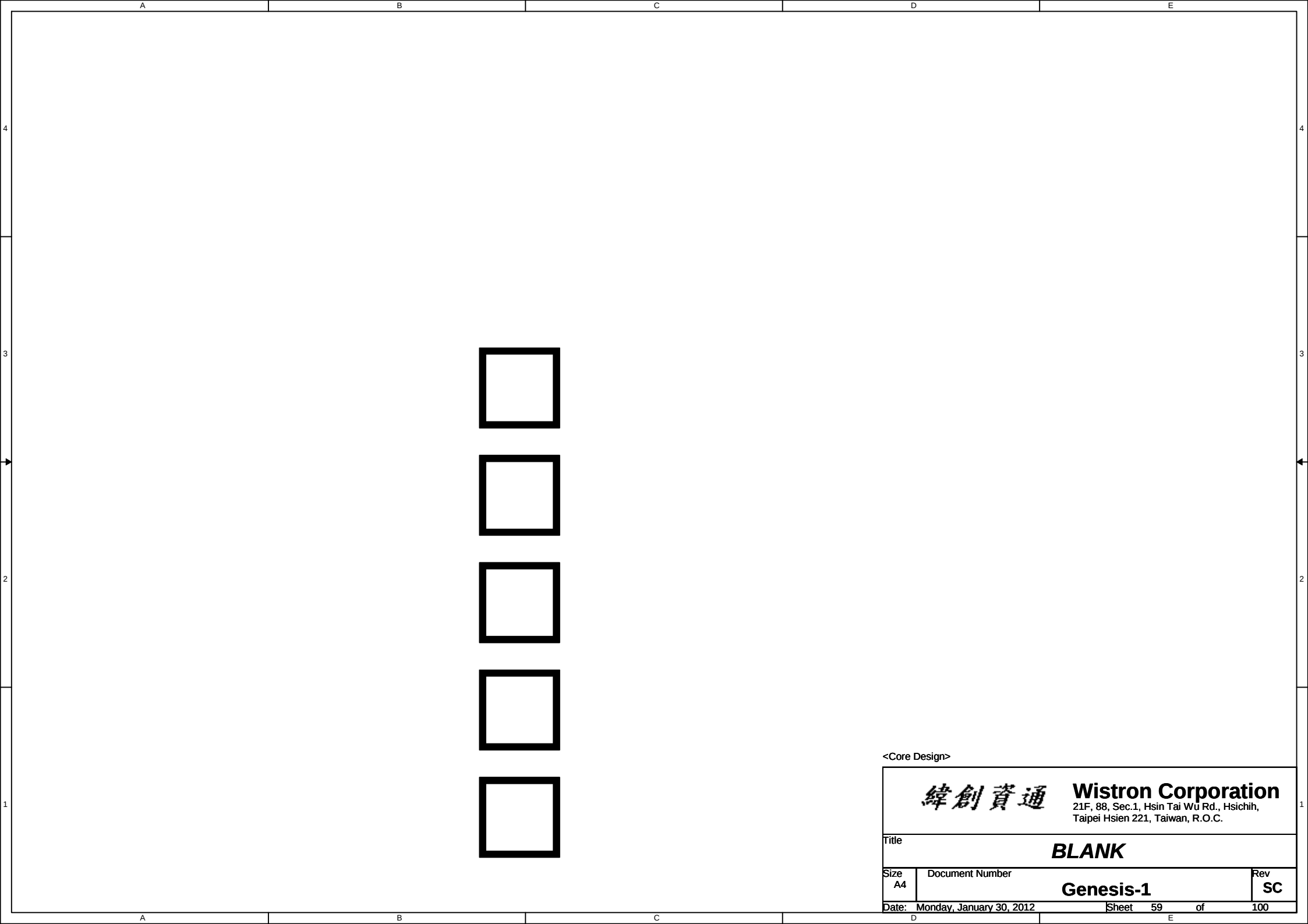
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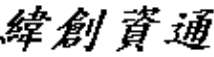
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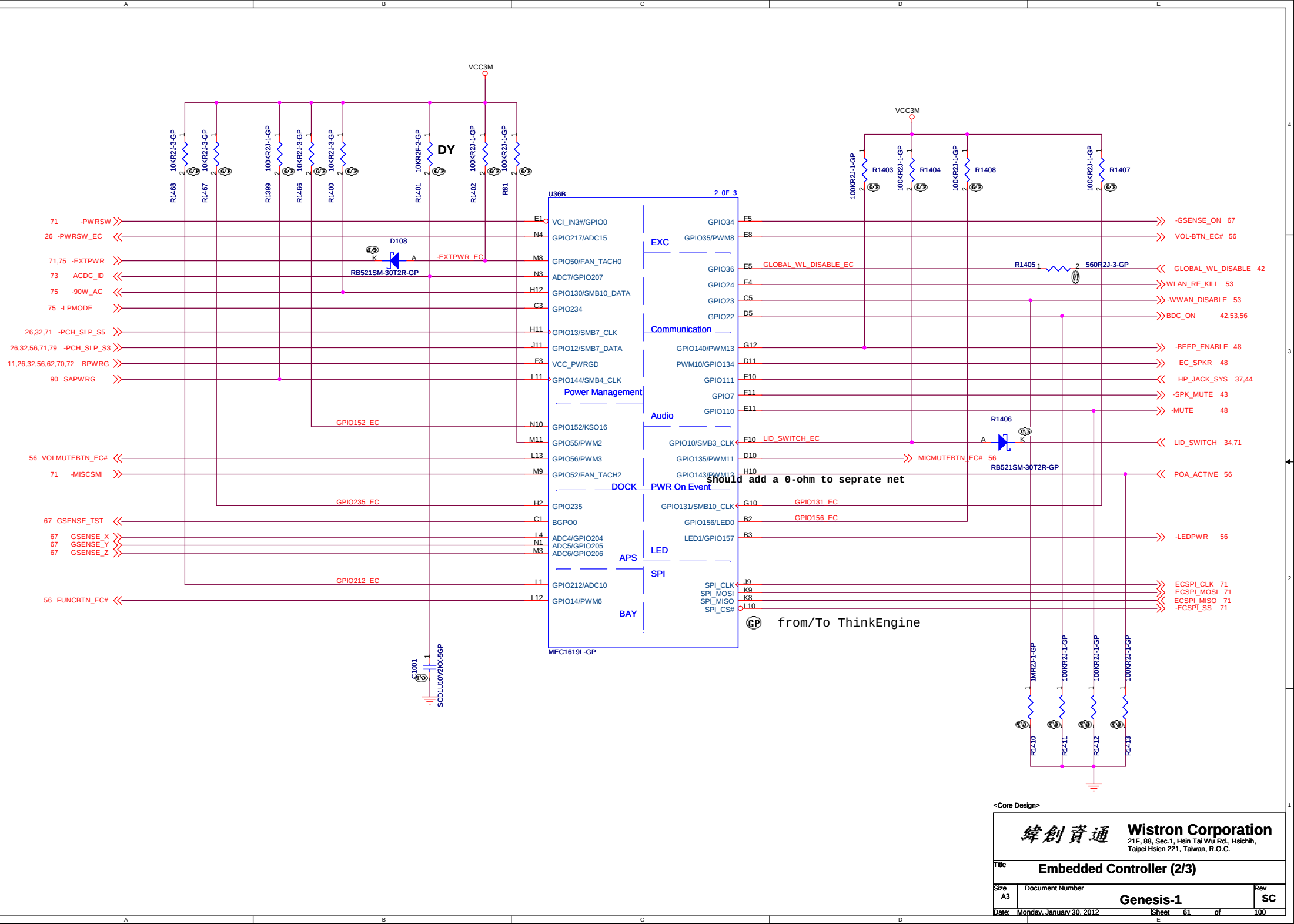
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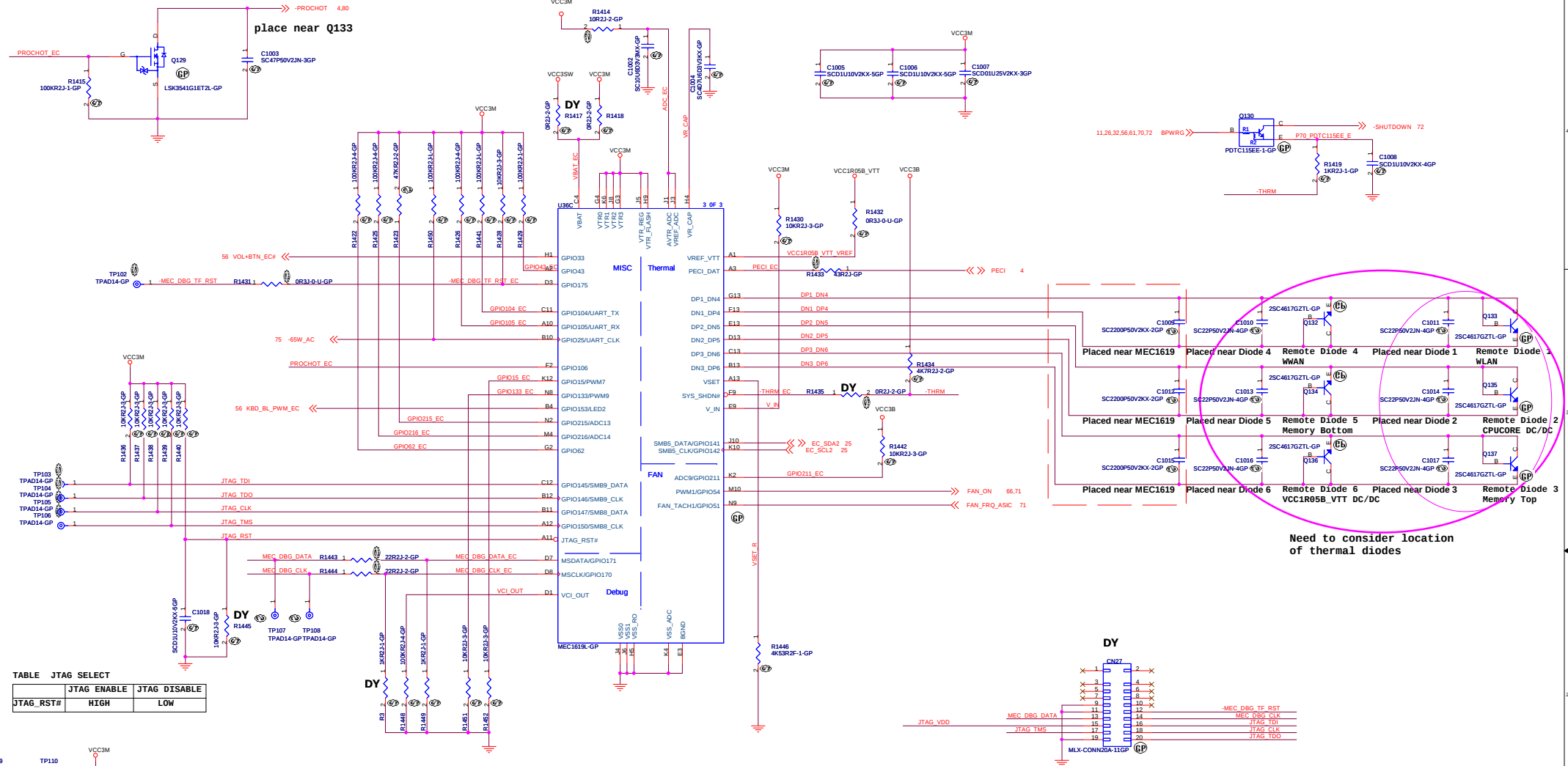


TABLE JTAG SELECT

JTAG_ENABLE	JTAG_DISABLE
JTAG_RST#	HIGH
	LOW

JTAG debug port

Enable	Disable
R1440	DY
R1445	ASM
R1454	ASM

↑
LOGIC

trace FIFO debug port

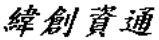
Enable	Disable
R1443	ASM
R1444	ASM
R3	DY

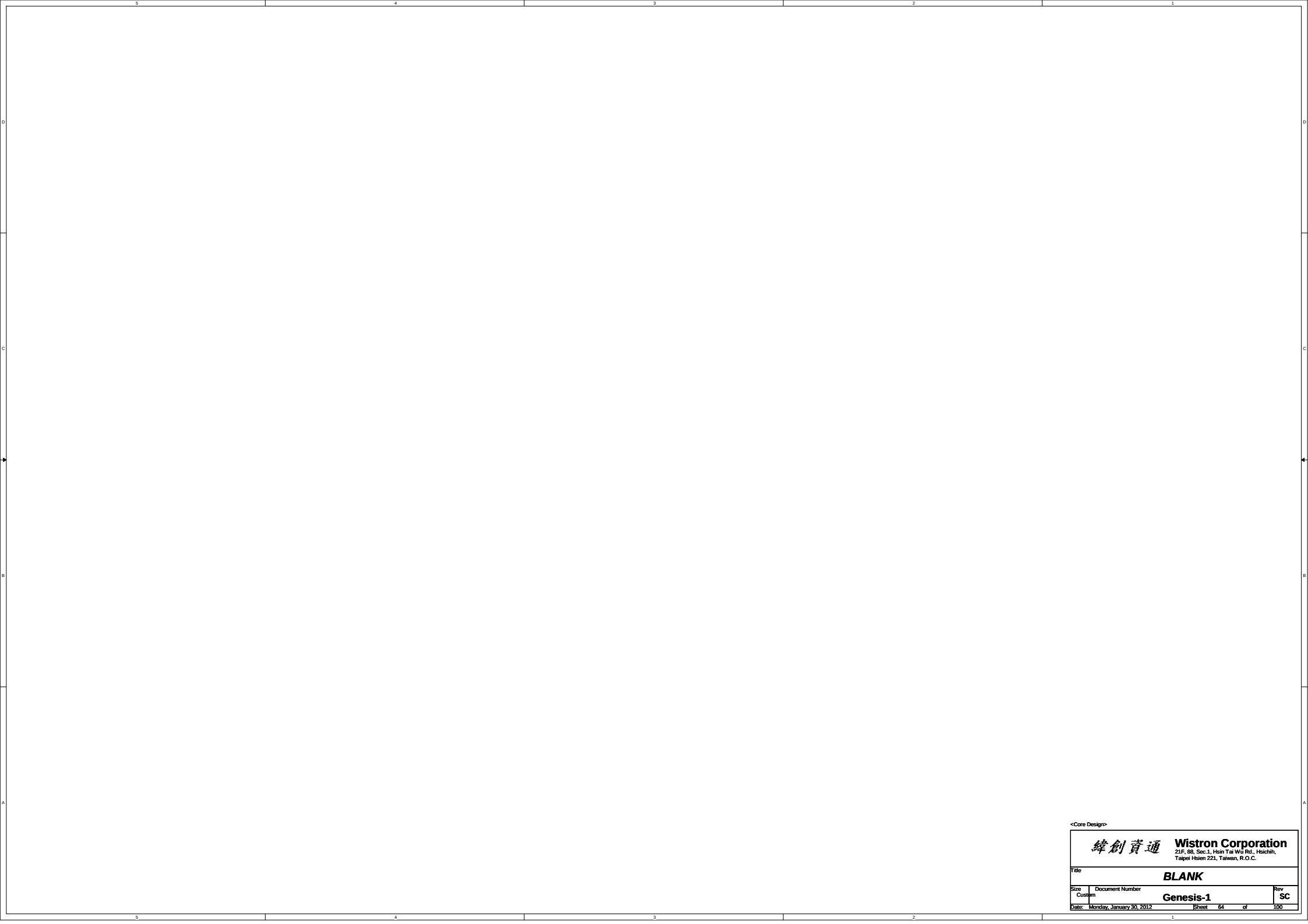
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LOGIC

Need to consider location of thermal diodes

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D

D

C

C

B

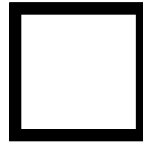
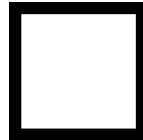
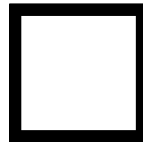
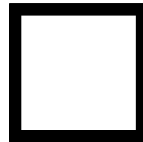
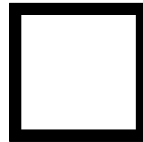
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A

A

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Wistron Corporation
215, 22nd, Sec. 1, Hsin-Tai W. Rd., Hsin-Tai

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

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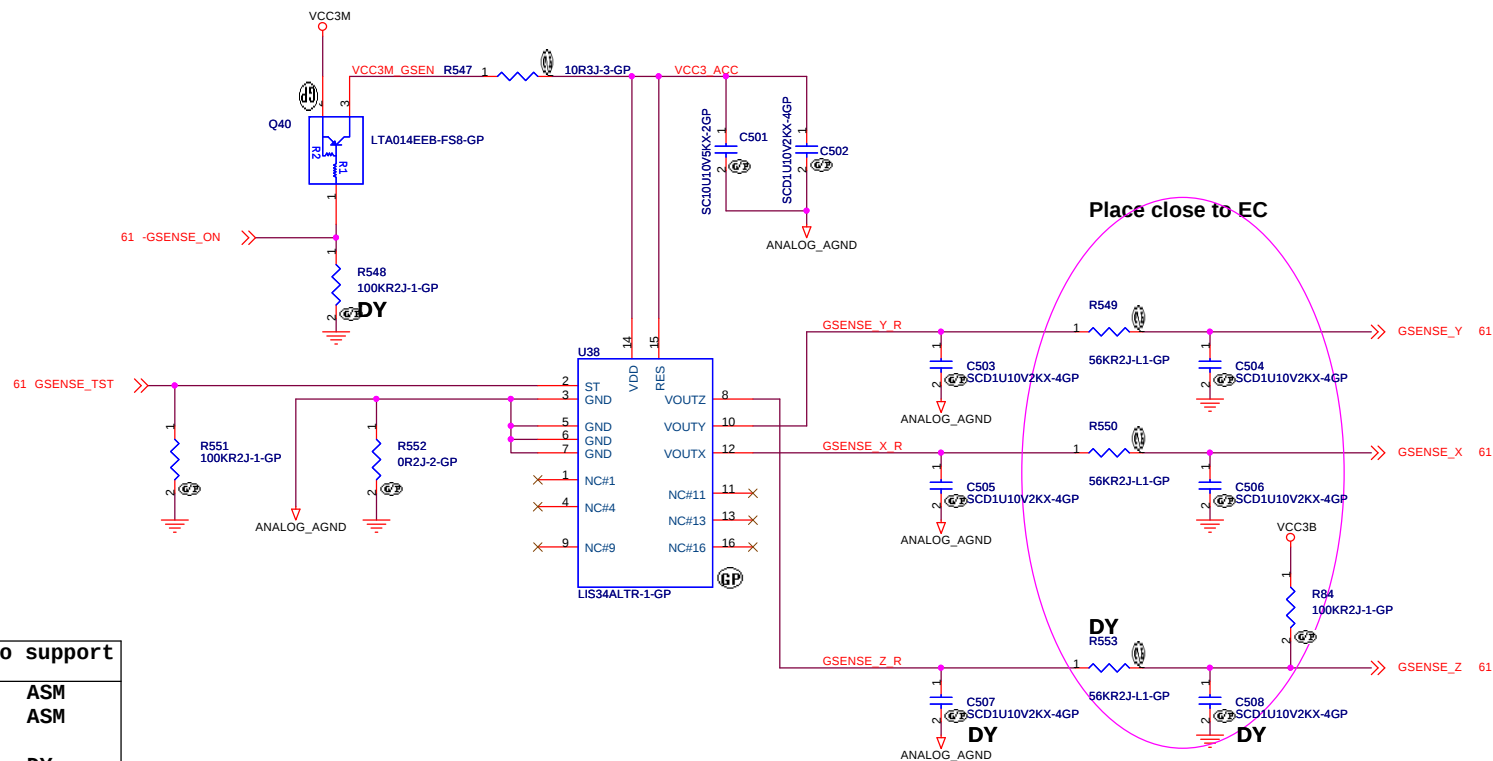
Document Number

Genesis-1

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G-sensor	support	no support
R548	DY	ASM
R551	ASM	ASM
U38	ASM	DY
Q40	ASM	DY
R547	ASM	DY
C501	ASM	DY
C502	ASM	DY
R552	ASM	DY
C503	ASM	DY
R549	ASM	DY
C504	ASM	DY
C505	ASM	DY
R550	ASM	DY
C506	ASM	DY
C507	DY	DY
R553	DY	DY
C508	DY	DY
R84	ASM	ASM

U38

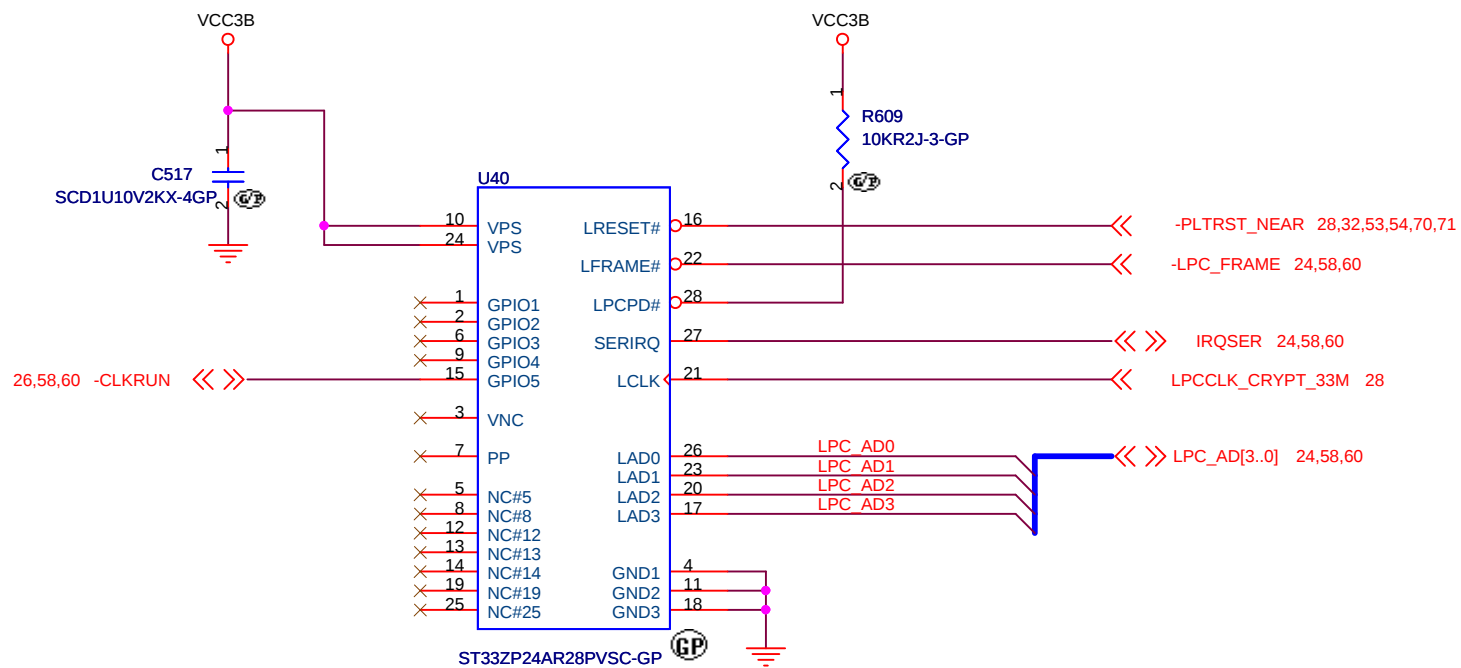
Primary	STMicro LIS34AL	41R0828AA
Second	Kionix KXTC8-2850	74.KXTC8.0BZ
Third		

Layout Comment :

(1) Avoid routing under DCDC switching area.

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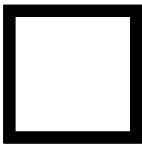
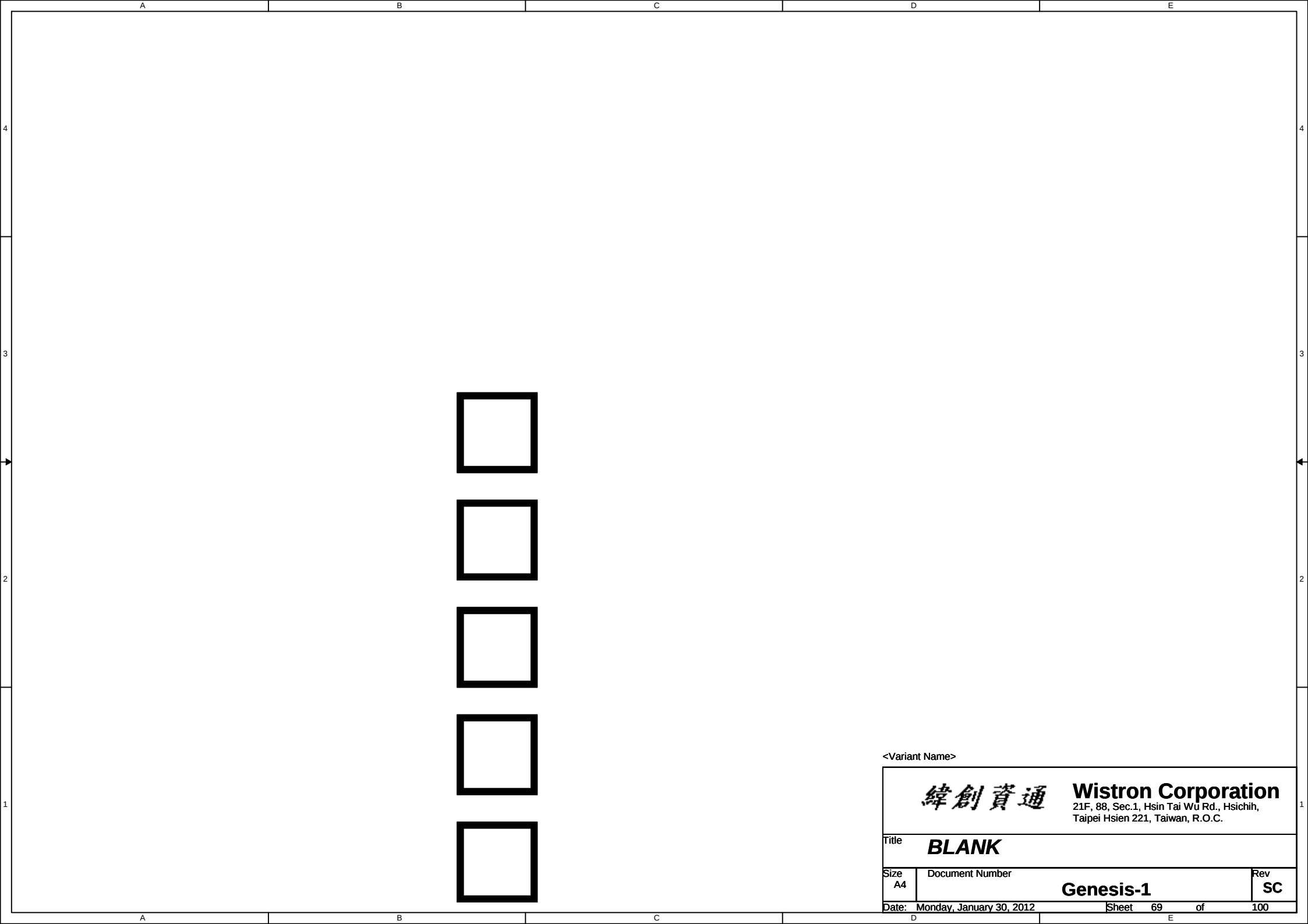
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Title		
G-SENSOR		
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TPM P/N		Firmware
SDV / FVT	ST33ZP24AR28PVRC	1.2.C.0
SIT	ST33ZP24AR28PVSC	1.2.D.0

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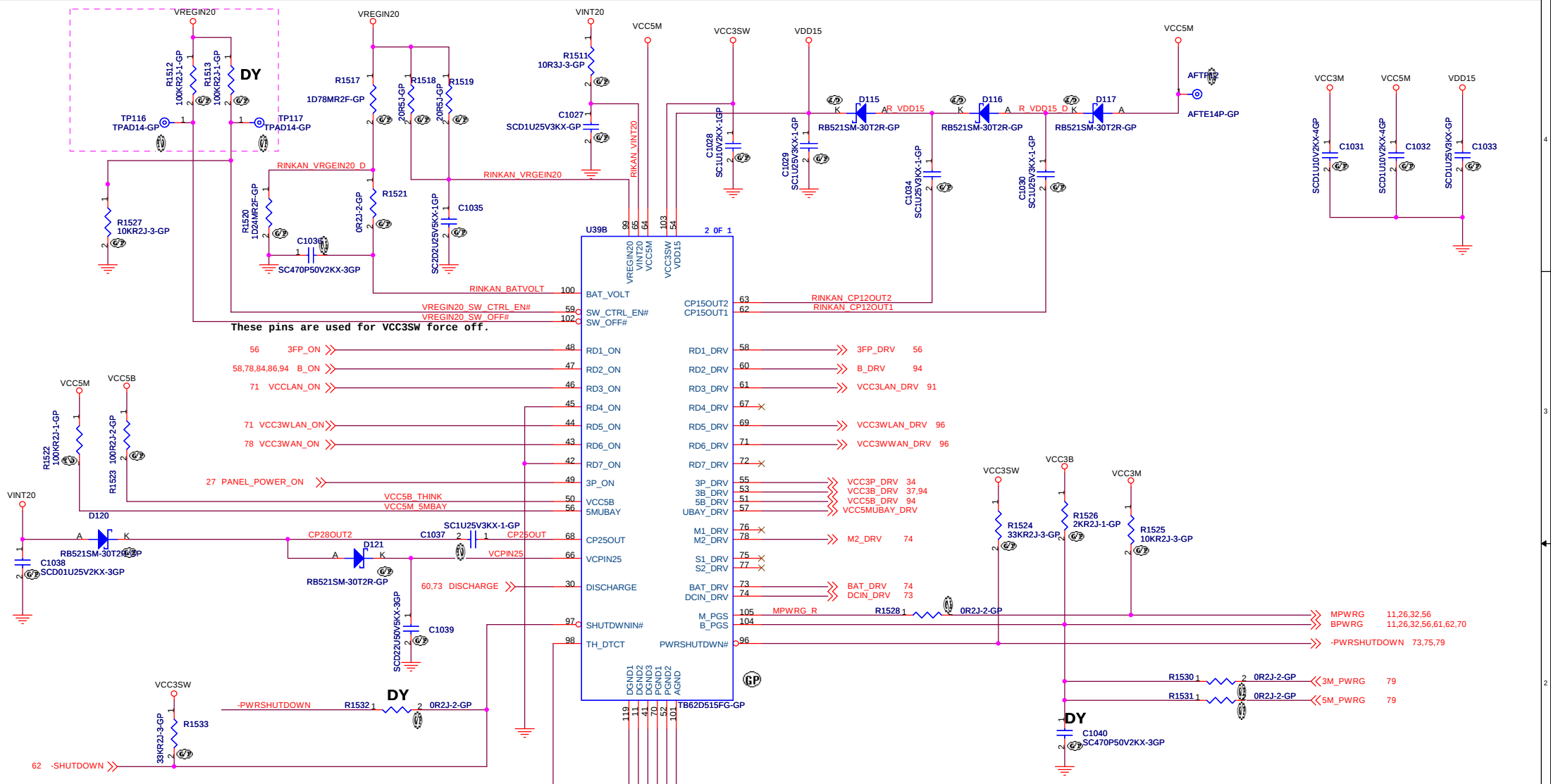
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Wistron Corporation
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Genesis-1



These pins are used for VCC3SW force off.

PTC Placement List

	PTC Position
RT2	VCC3M_DC/DC_High_side_FET (Q88)
RT3	VCC5M_DC/DC_High_side_FET (Q86 or Q87)
RT8	DCIN_PWR20F_FET (Q51)
RT1	CHARGER_OUT12_FET (Q75)
RT7	M_BAT_PWR_A_FET (Q62)
RT4	VCCCPUCORE_Driver-1 (U47)
RT10	VCCGFXCORE_Driver (U50)
RT9	CPU_Die (U1)

<Variant Name>

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Think Engine (2/2)

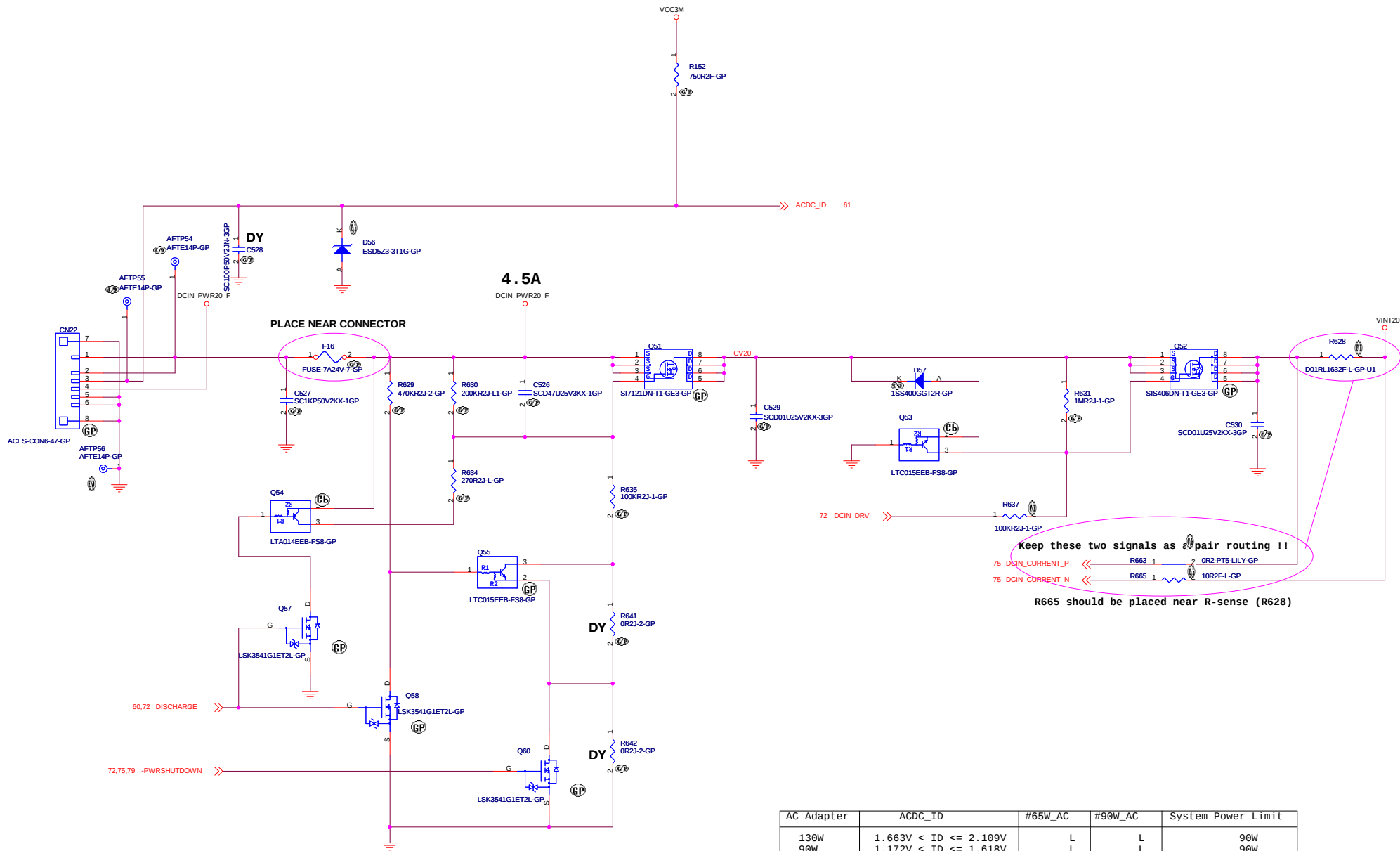
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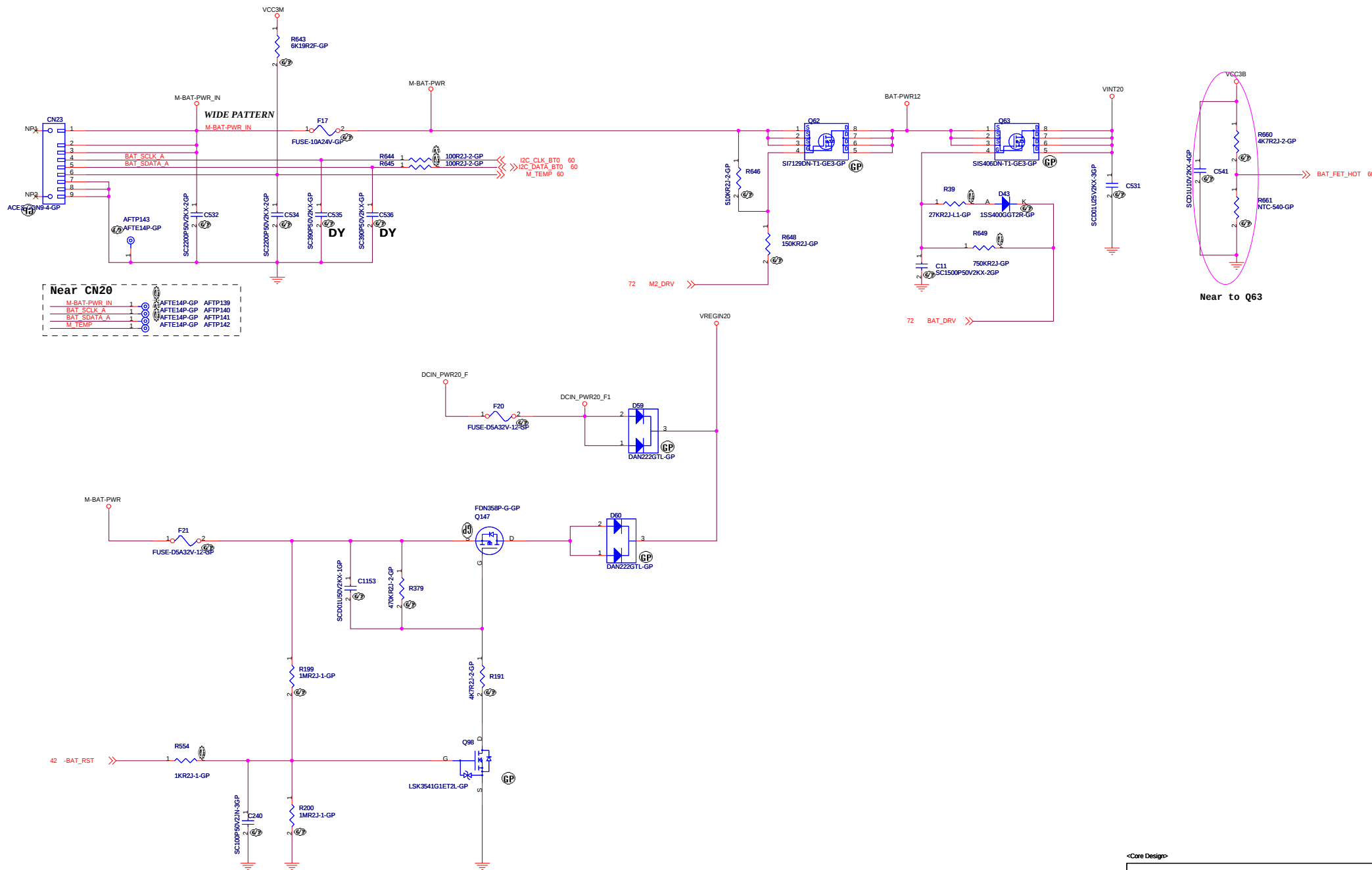
AC Adapter	ACDC_ID	#65W_AC	#90W_AC	System Power Limit
130W	1.663V < ID <= 2.109V	L	L	90W
90W	1.172V < ID <= 1.618V	L	L	90W
65W	0.693V < ID <= 1.134V	L	H	65W
45W	0.234V < ID <= 0.663V	H	H	45W

PEAK SHIFT	YES	NO
R641	NO-ASM	ASM
R629	ASM	NO-ASM
Q58	ASM	NO-ASM
Q55	ASM	NO-ASM

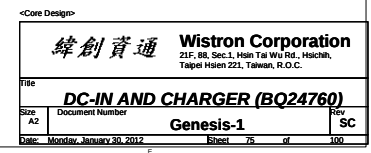
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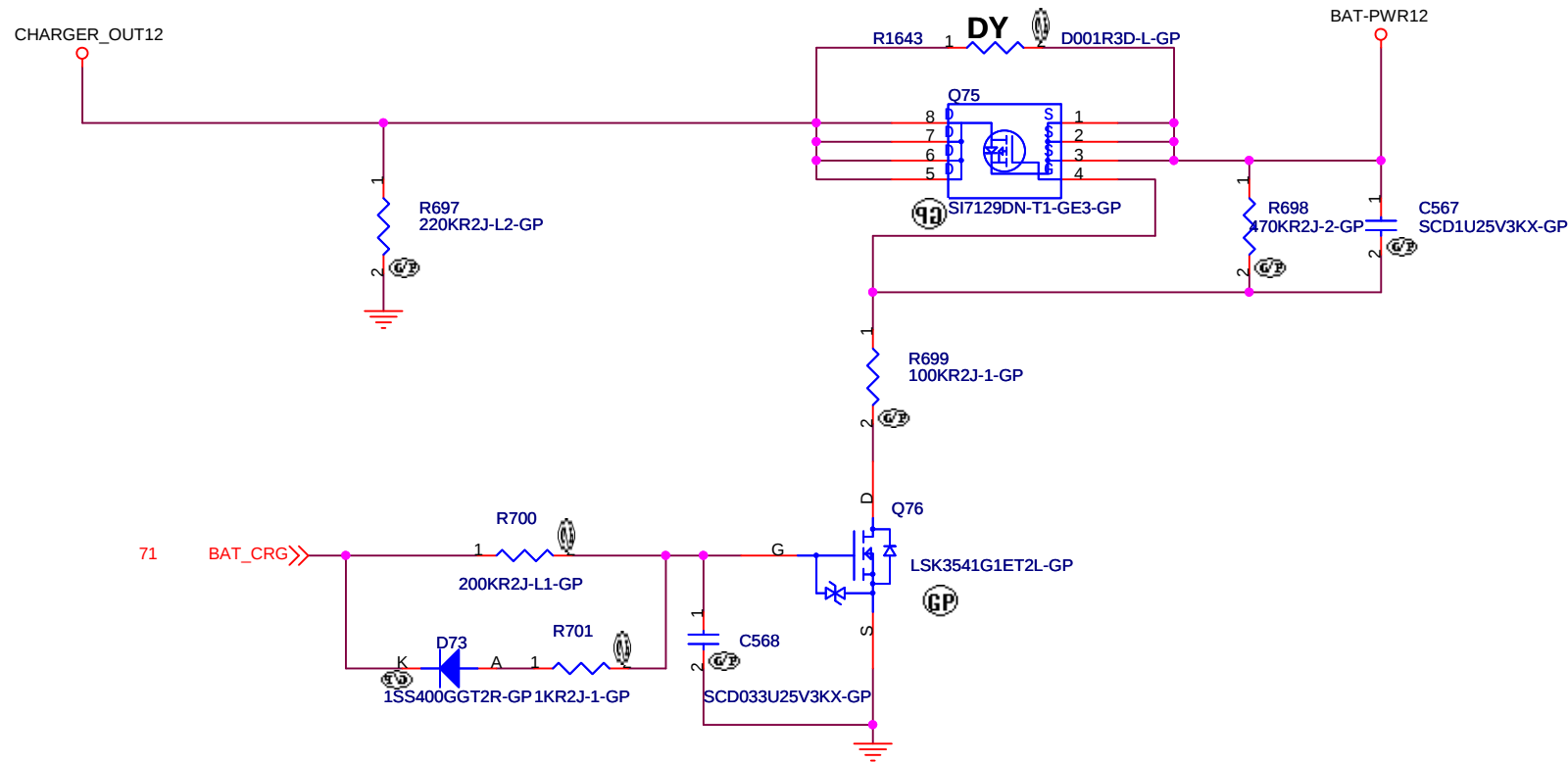
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CHARGER SELECT

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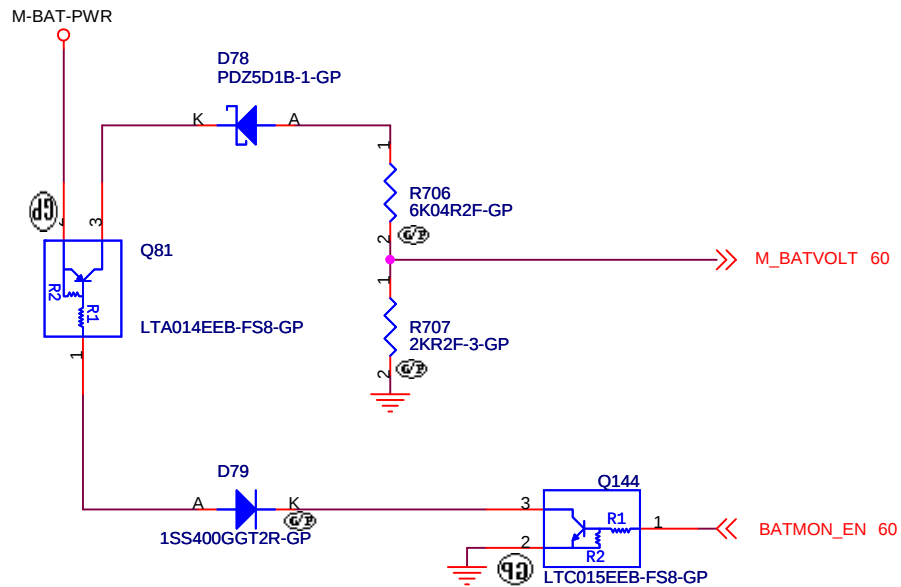
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SC

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$$V_{OUT} = 0.249 (V_{BAT} - 5)$$



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BATTERY MONITOR

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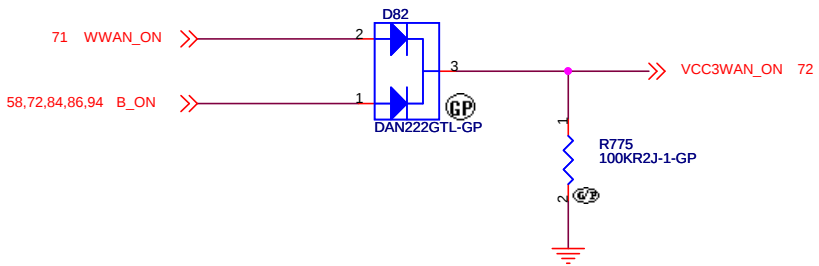
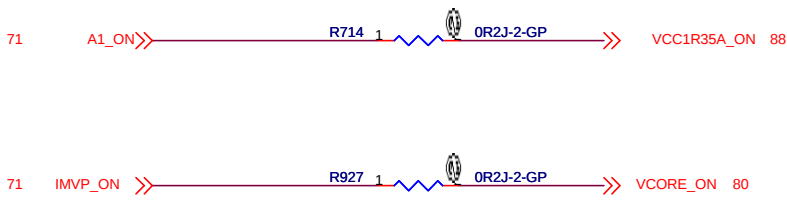
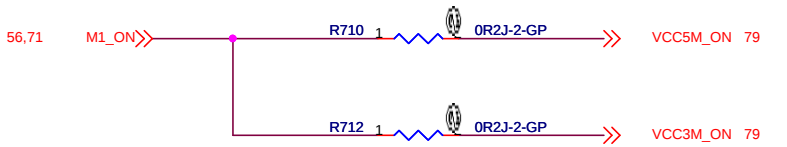
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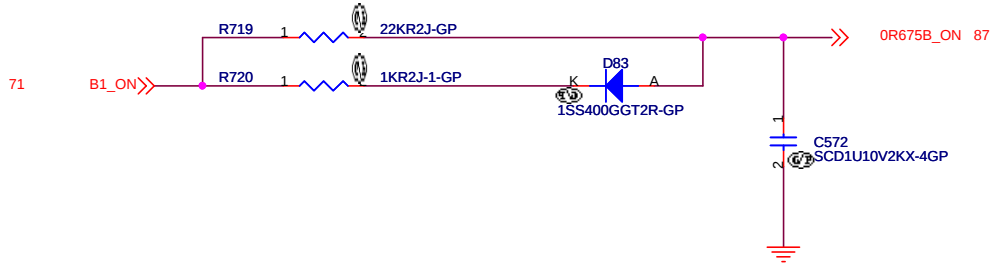
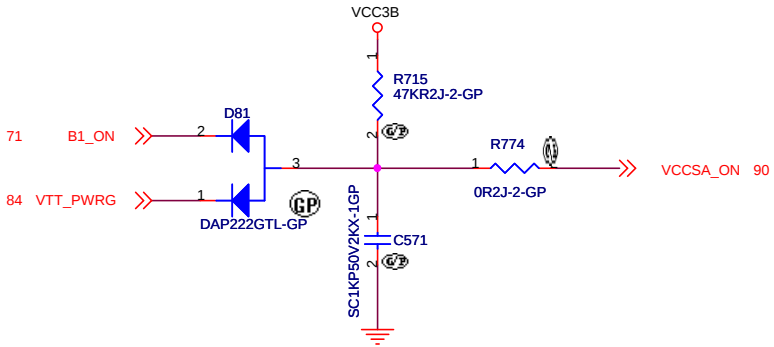
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100



AOAC	YES	NO
D82	ASM	DY
R775	ASM	ASM
	100Kohm	0ohm

Logic



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POWER SEQUENCE

Size

Document Number

Rev

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Genesis-1

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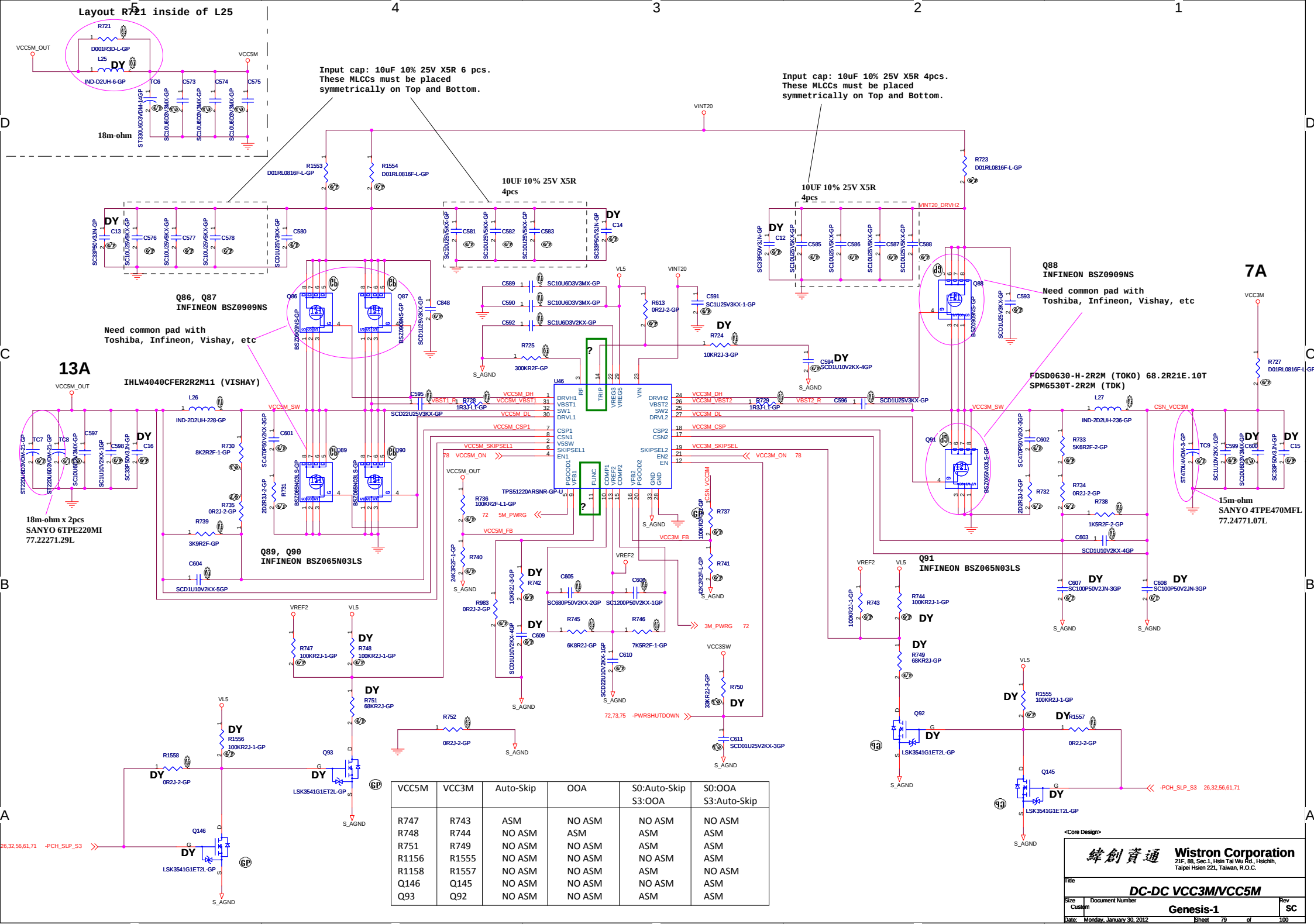
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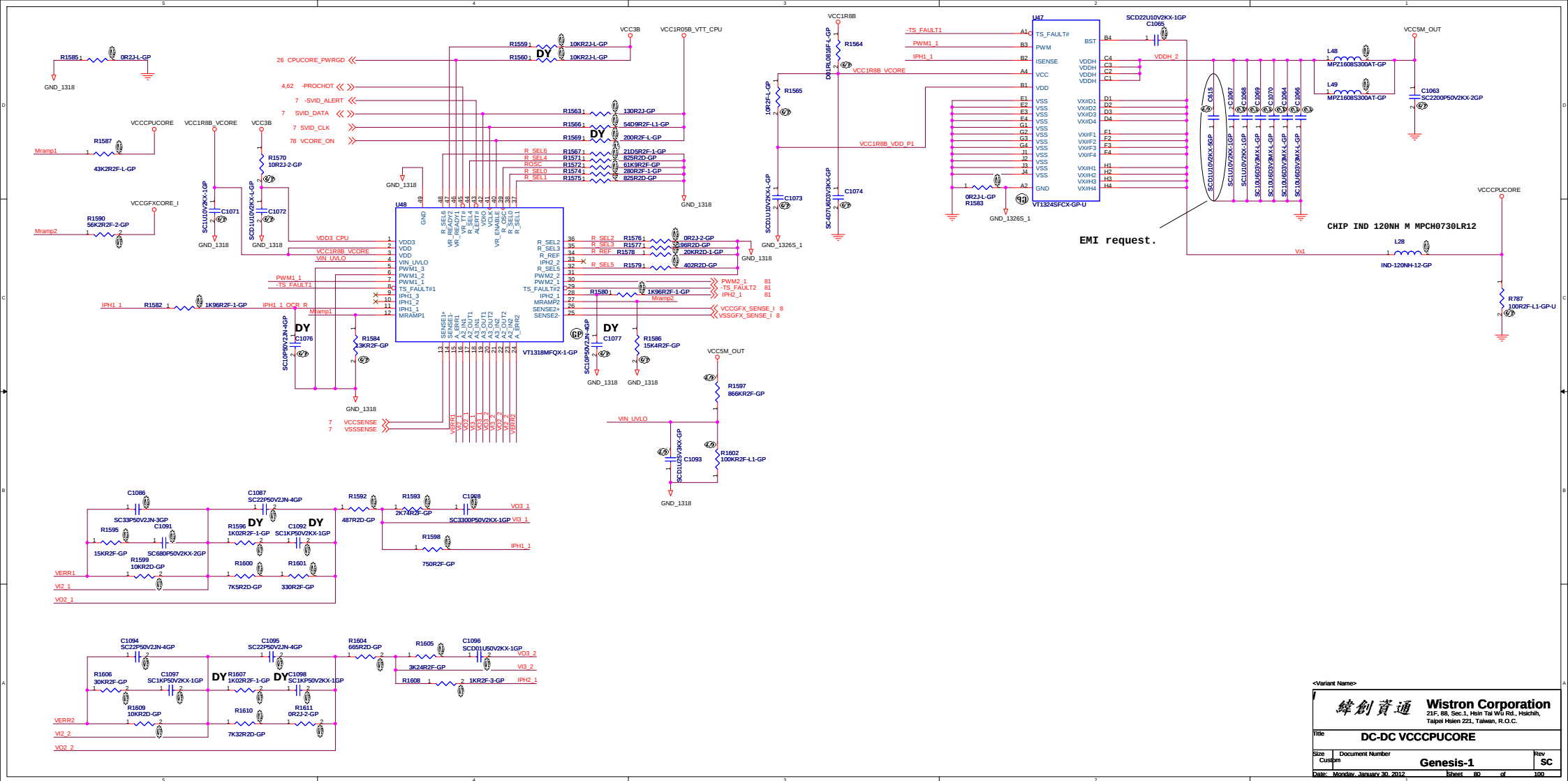
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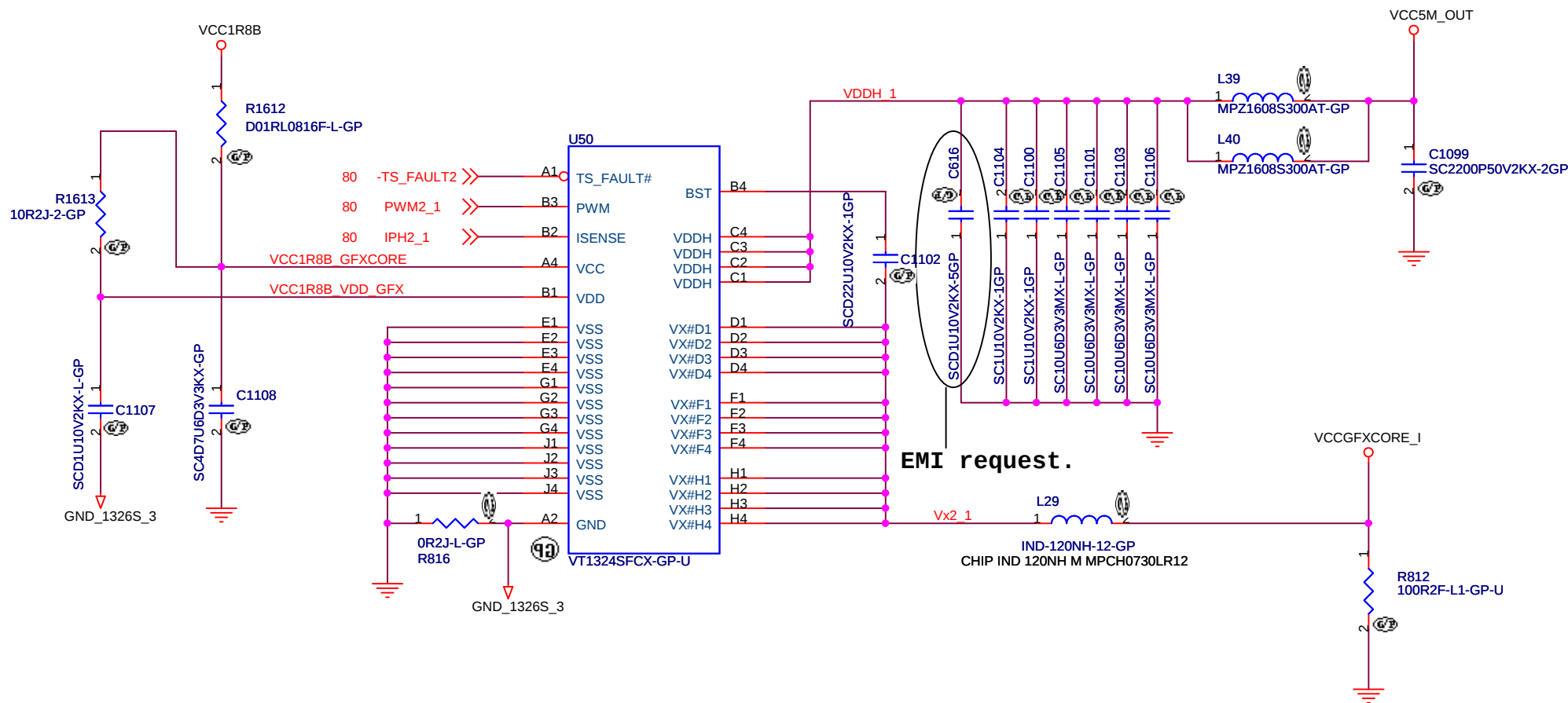
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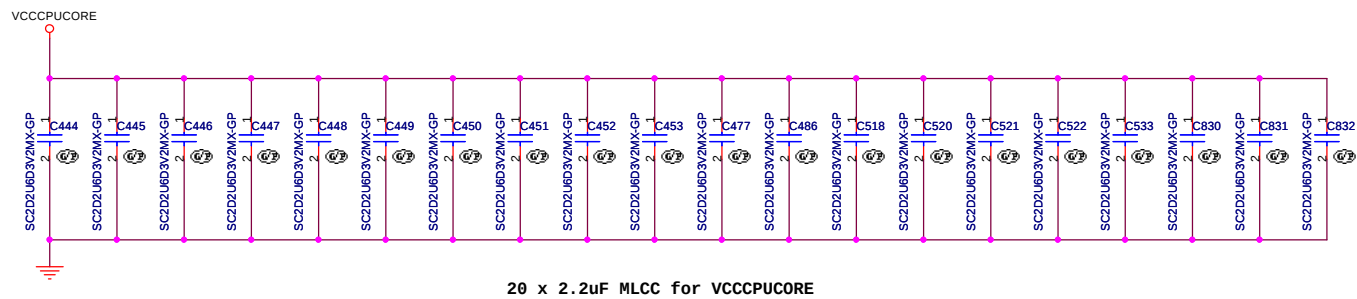
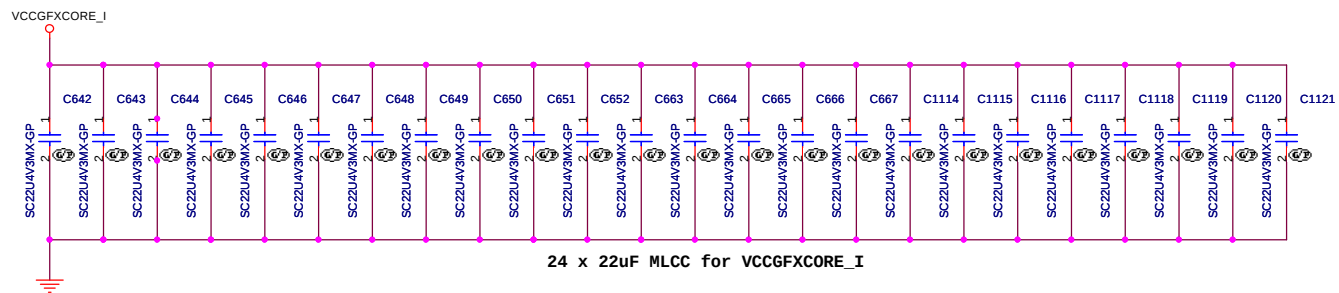
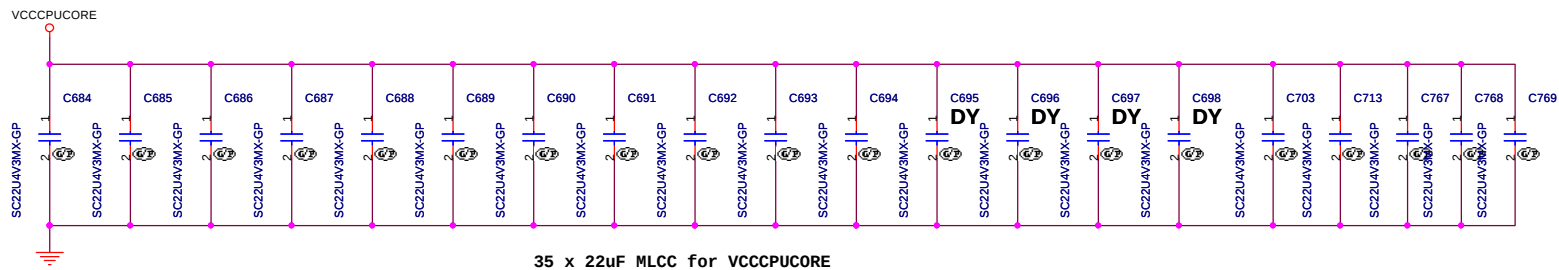
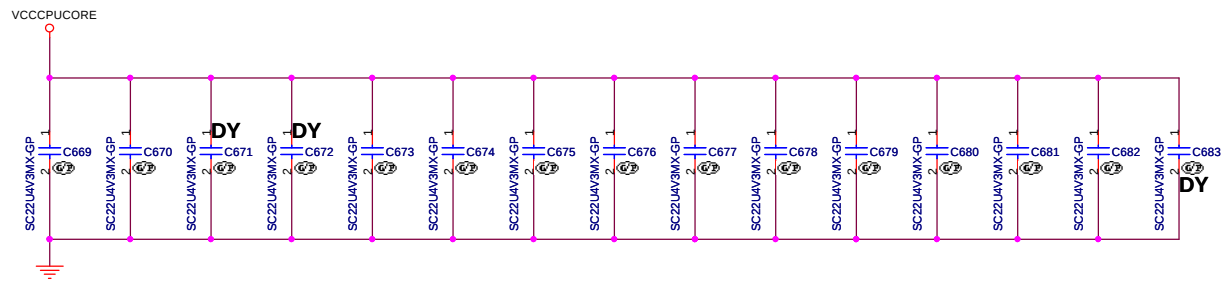
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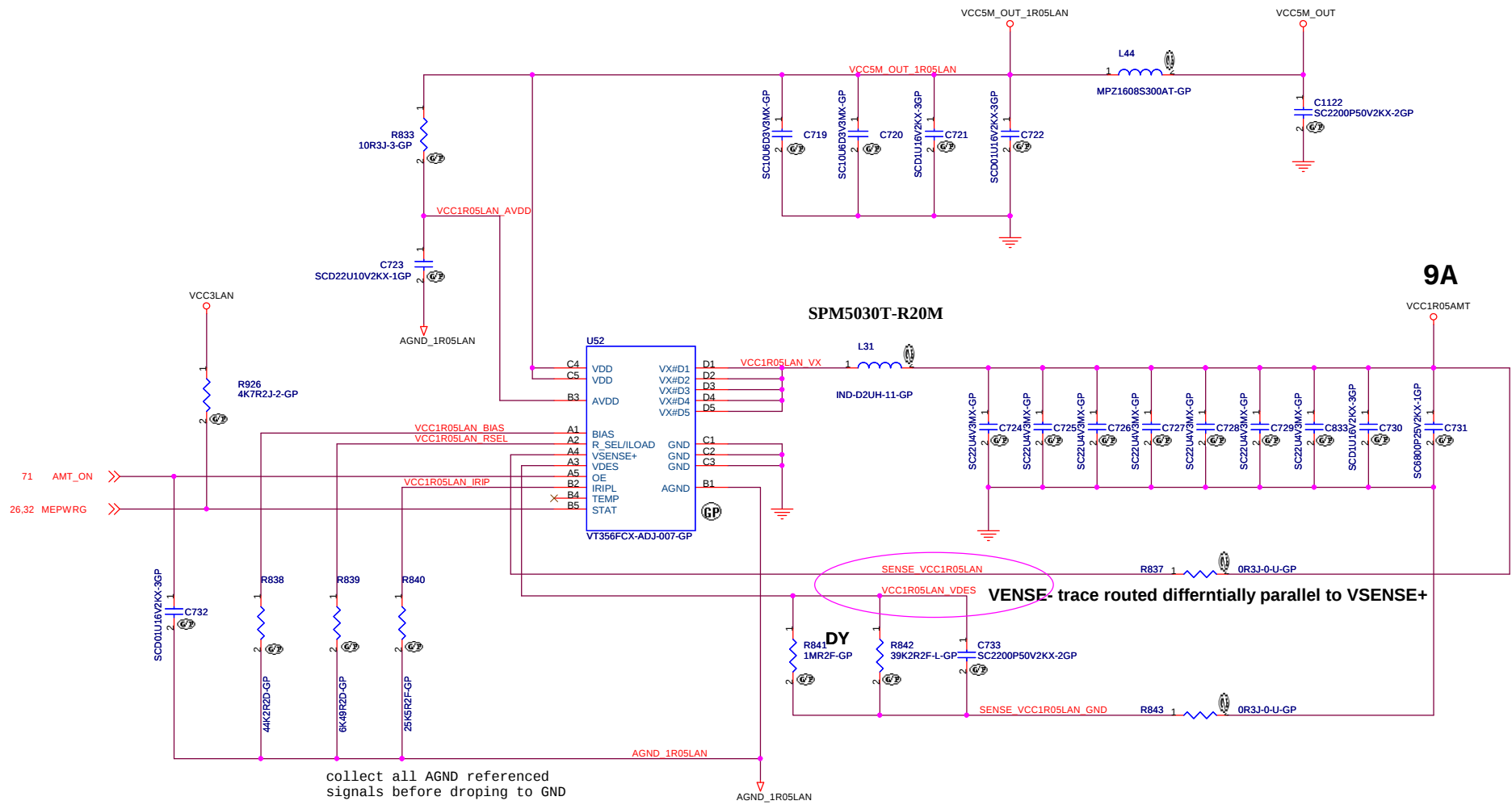
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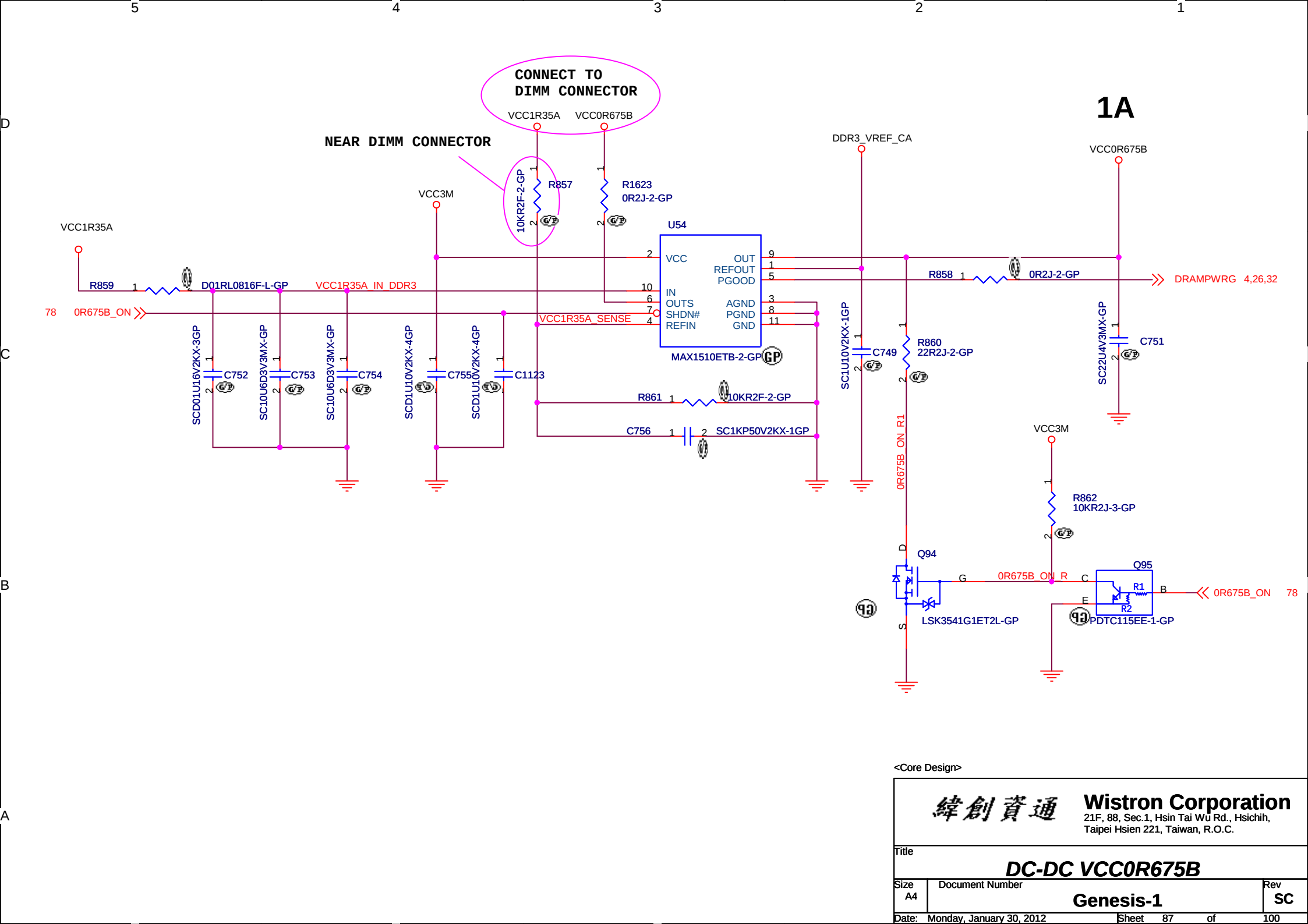


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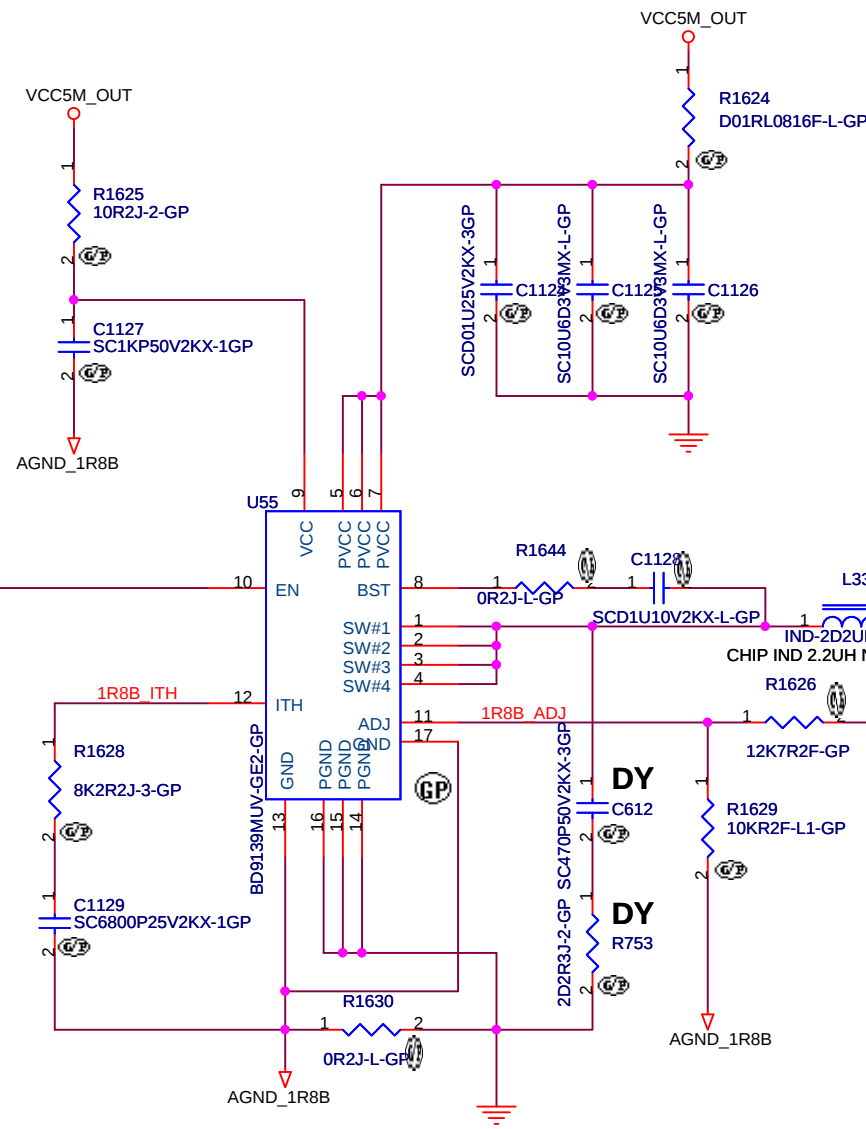
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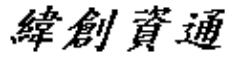
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L33

supplier	Vendor P/N	Wistron P/N
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Taiyo-Yuden	NRS5024T-2R2NMGJ	68.2R21E.10F

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DC-DC VCC1R8B

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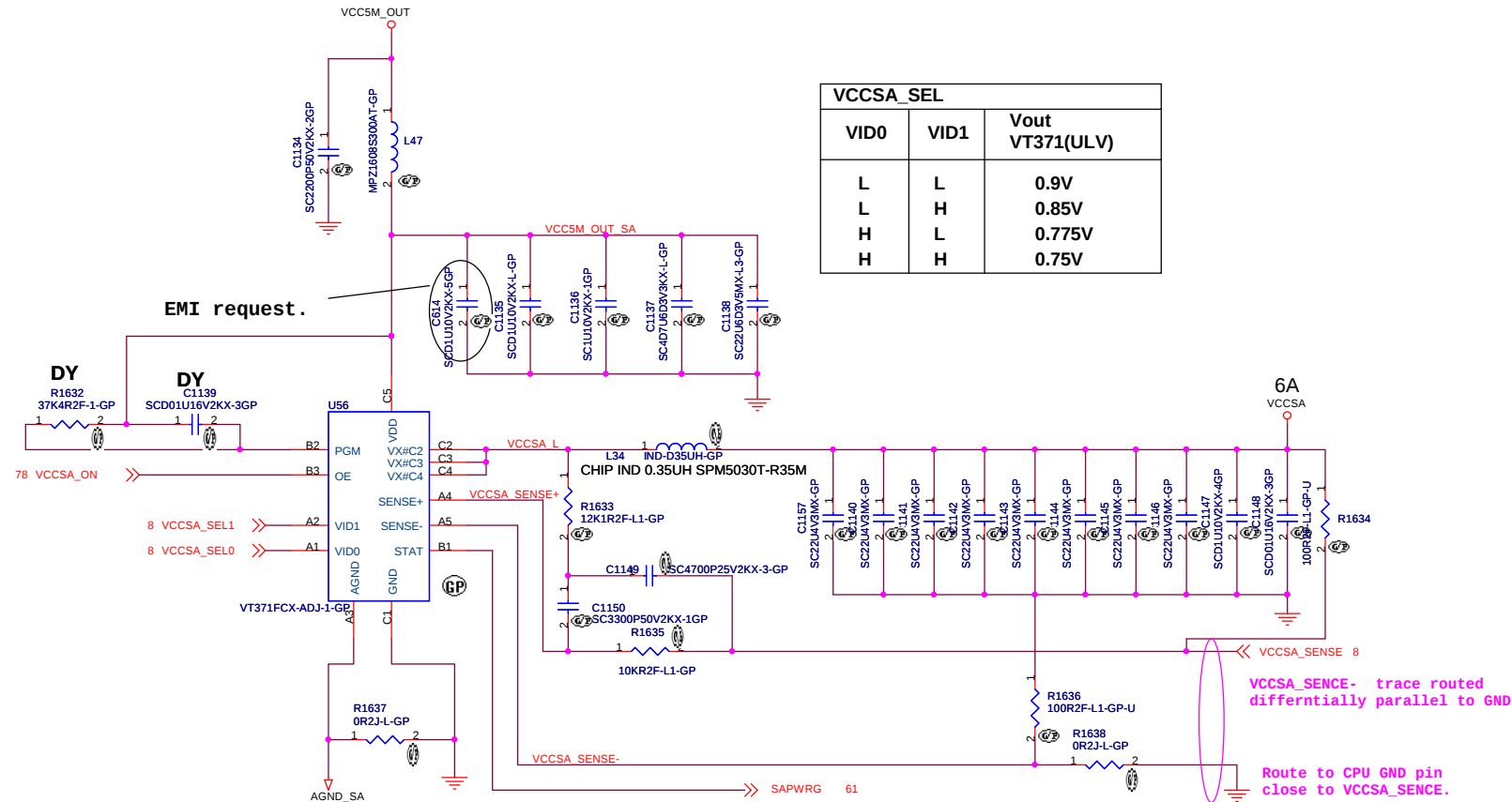
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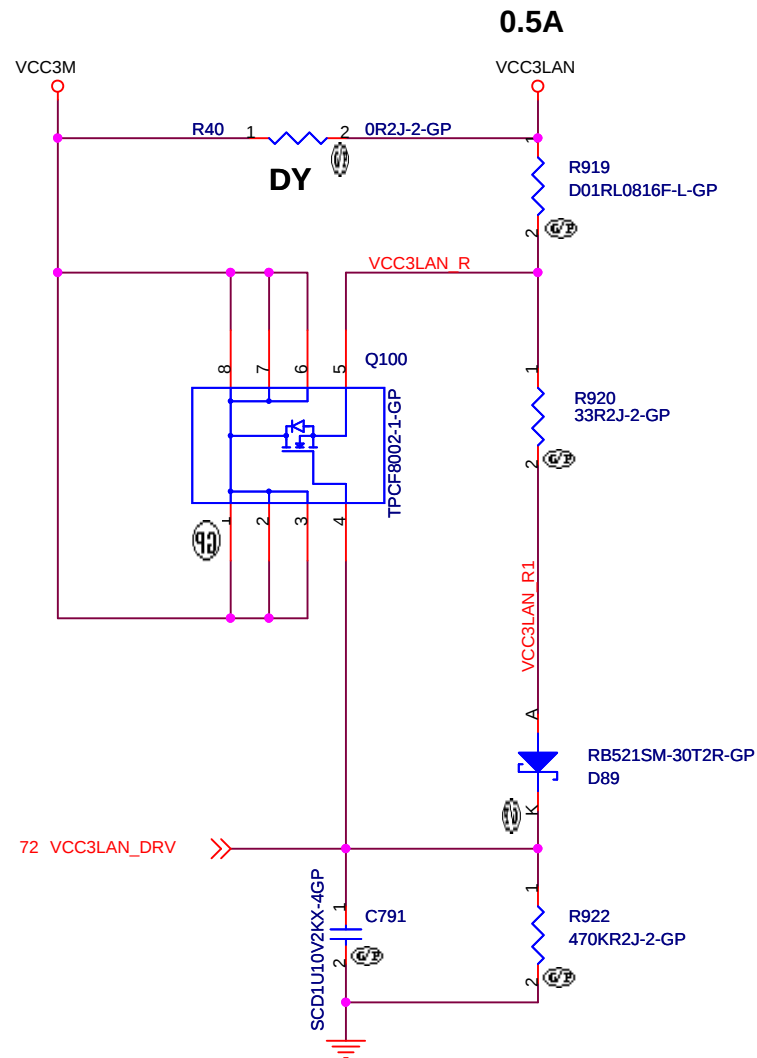
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LOAD SW LAN

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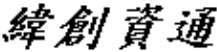
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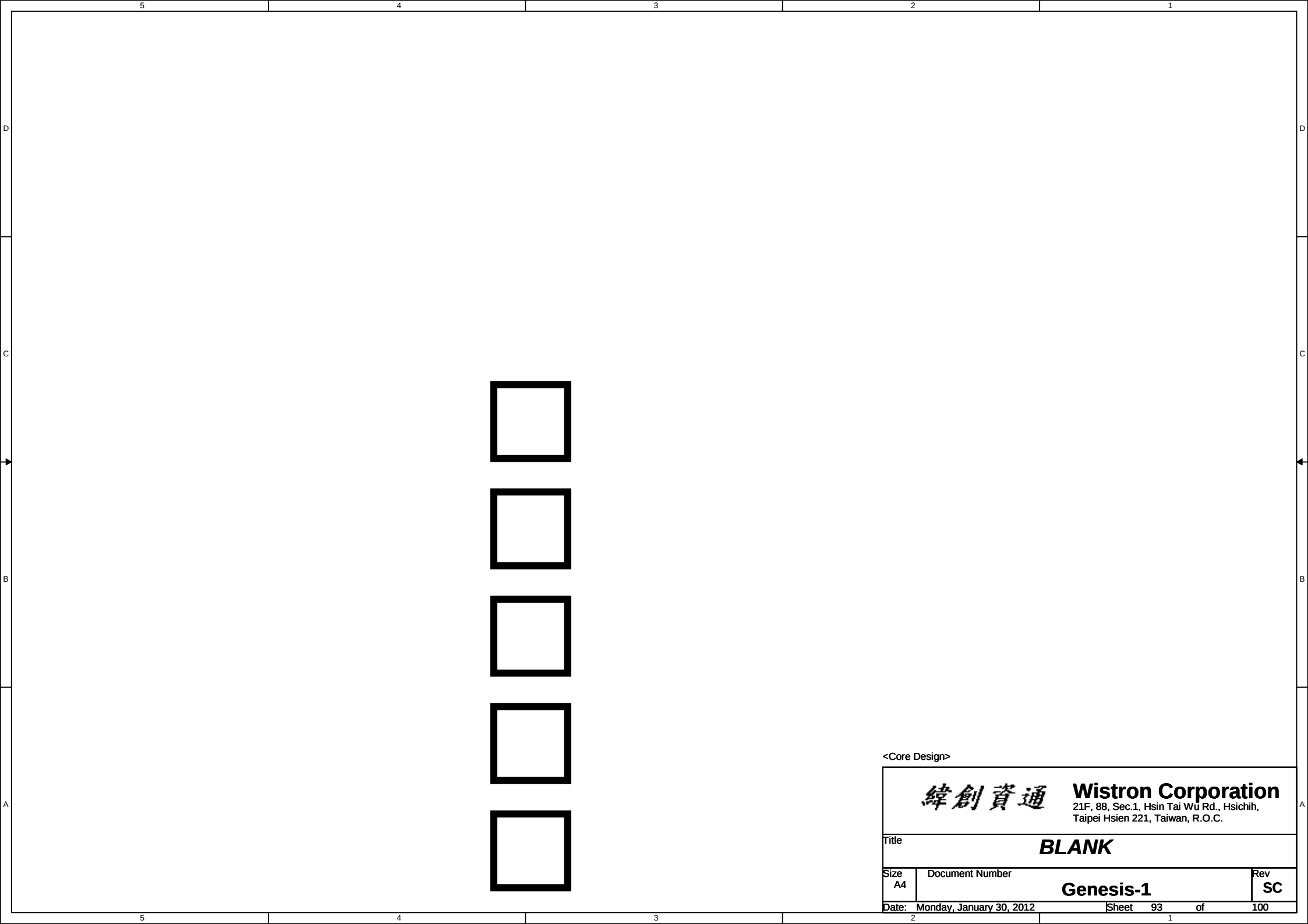
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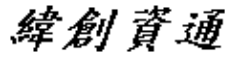
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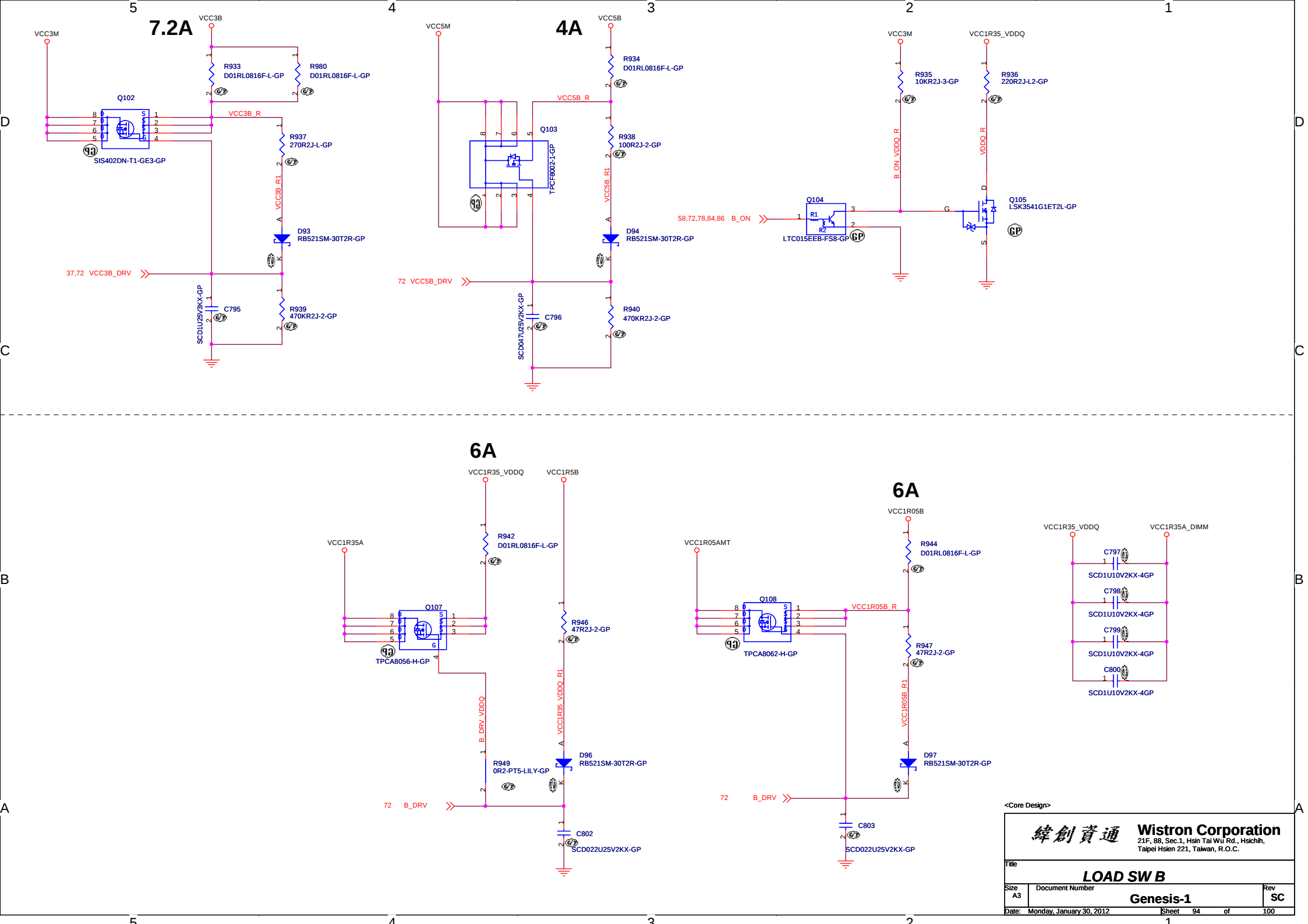


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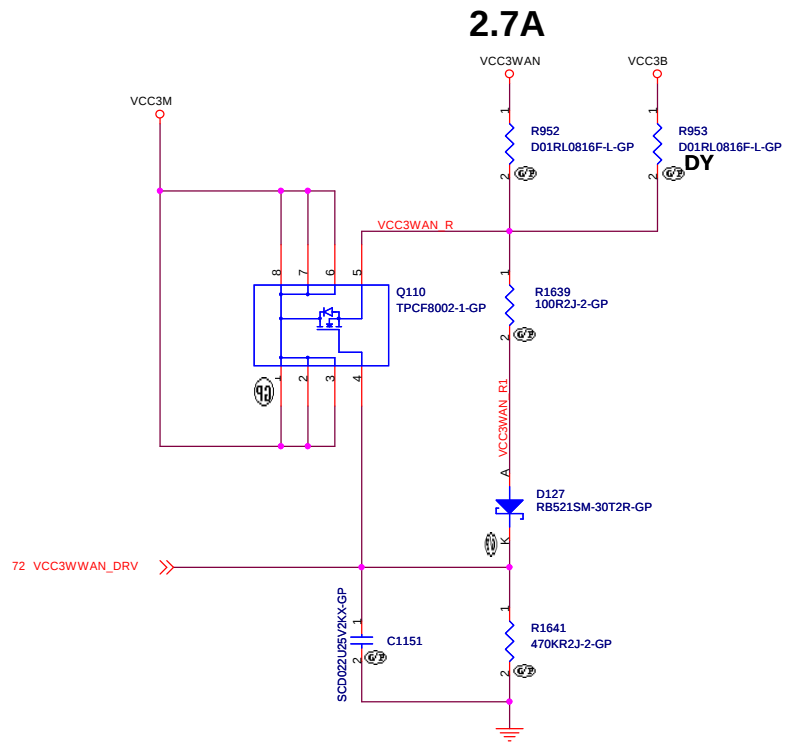
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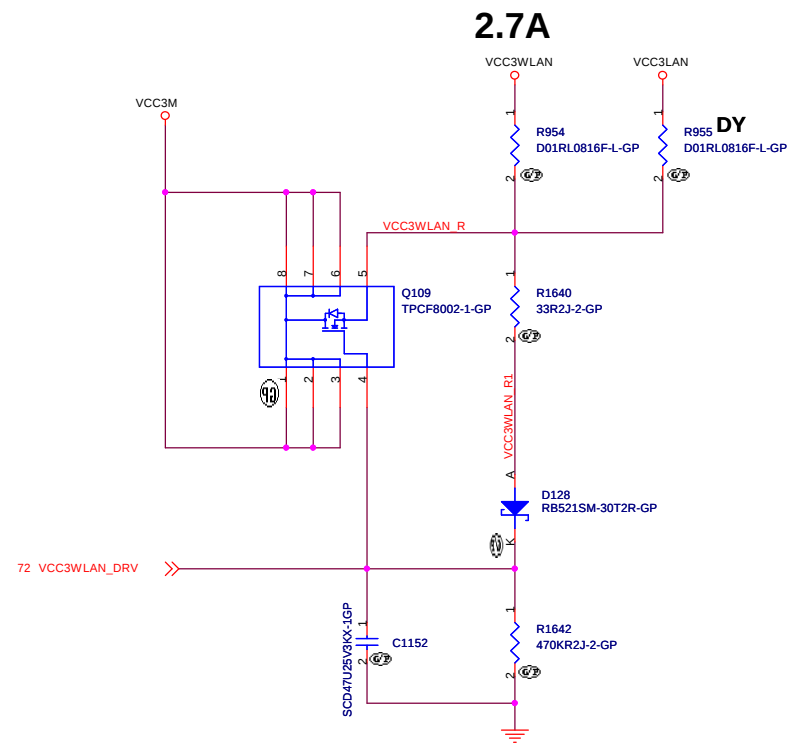
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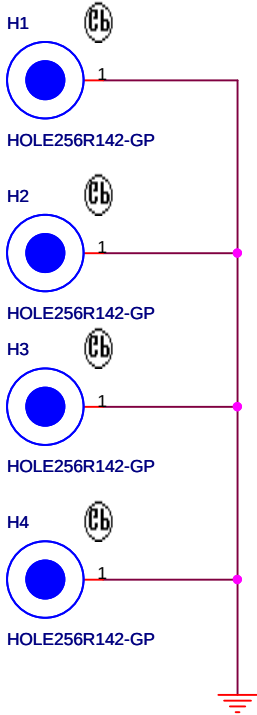
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C1151	ASM	DY

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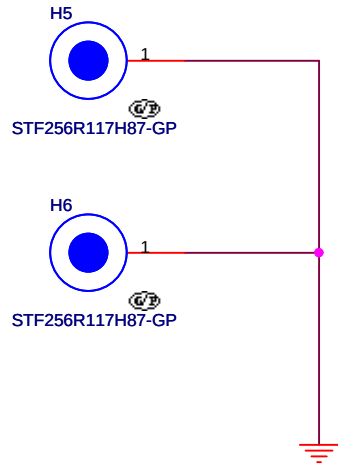


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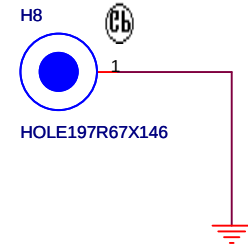
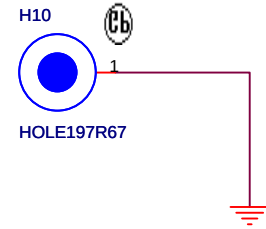
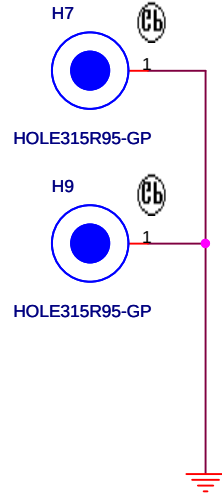
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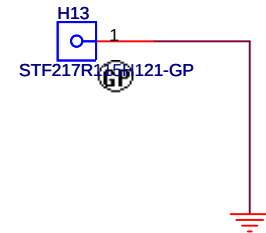
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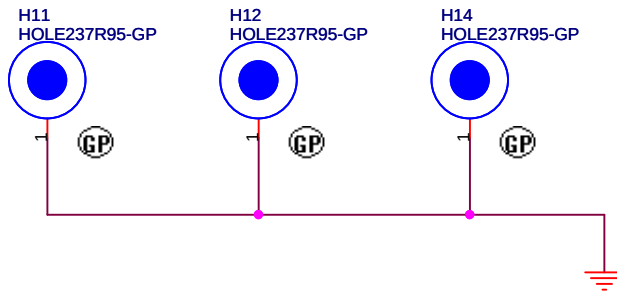
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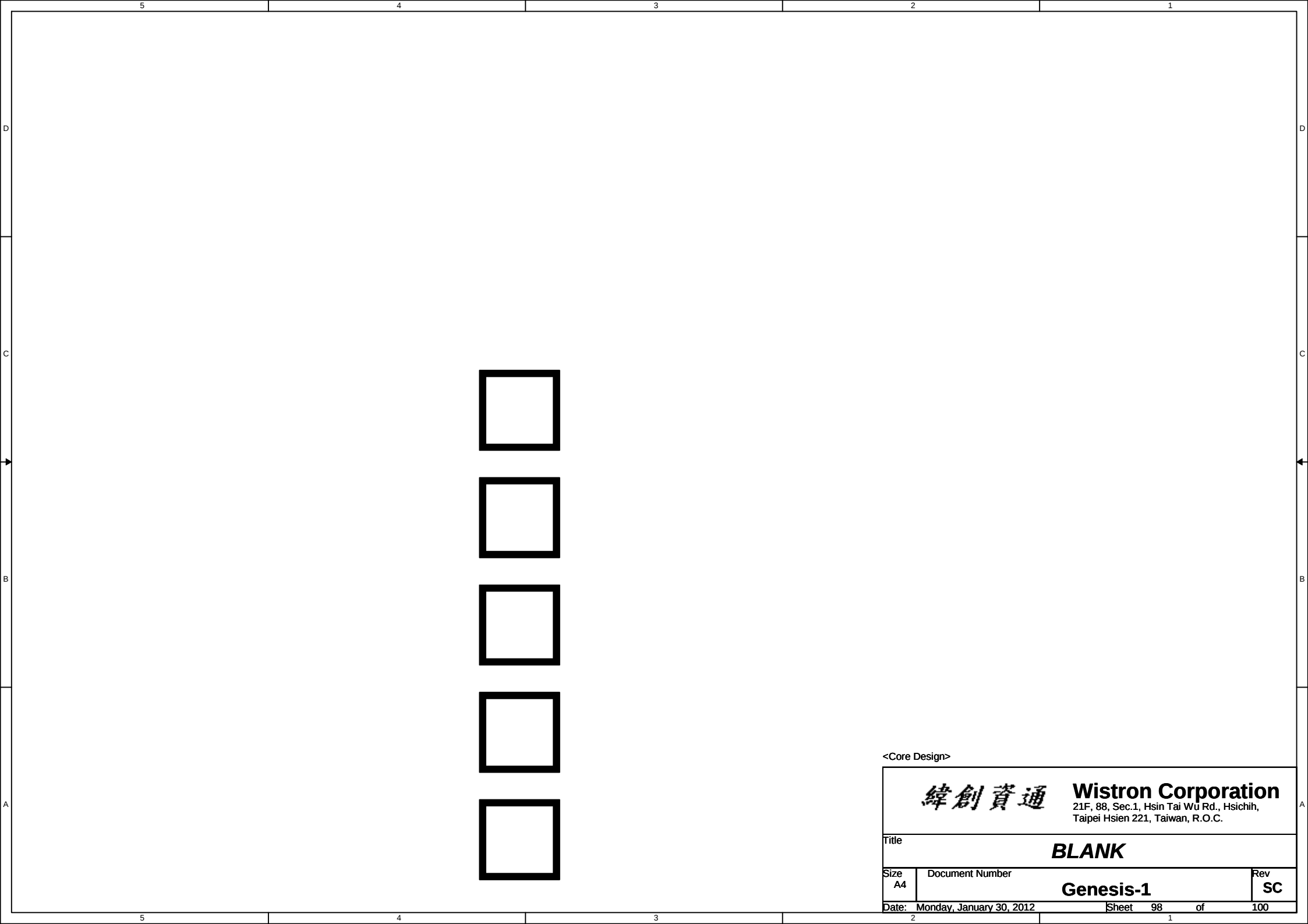


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Taipei Hsien 221, Taiwan, R.O.C.

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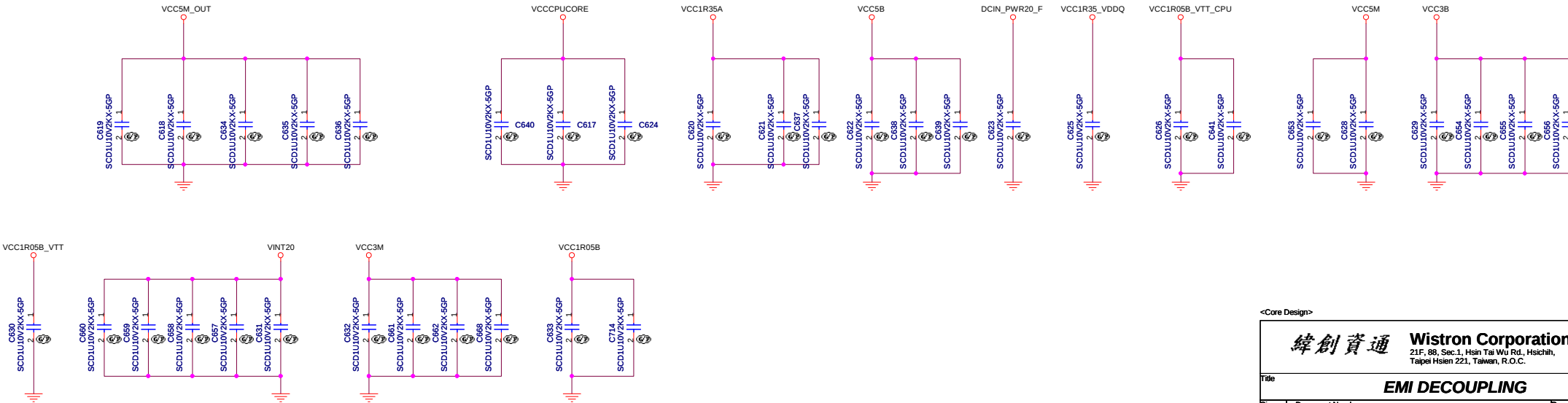
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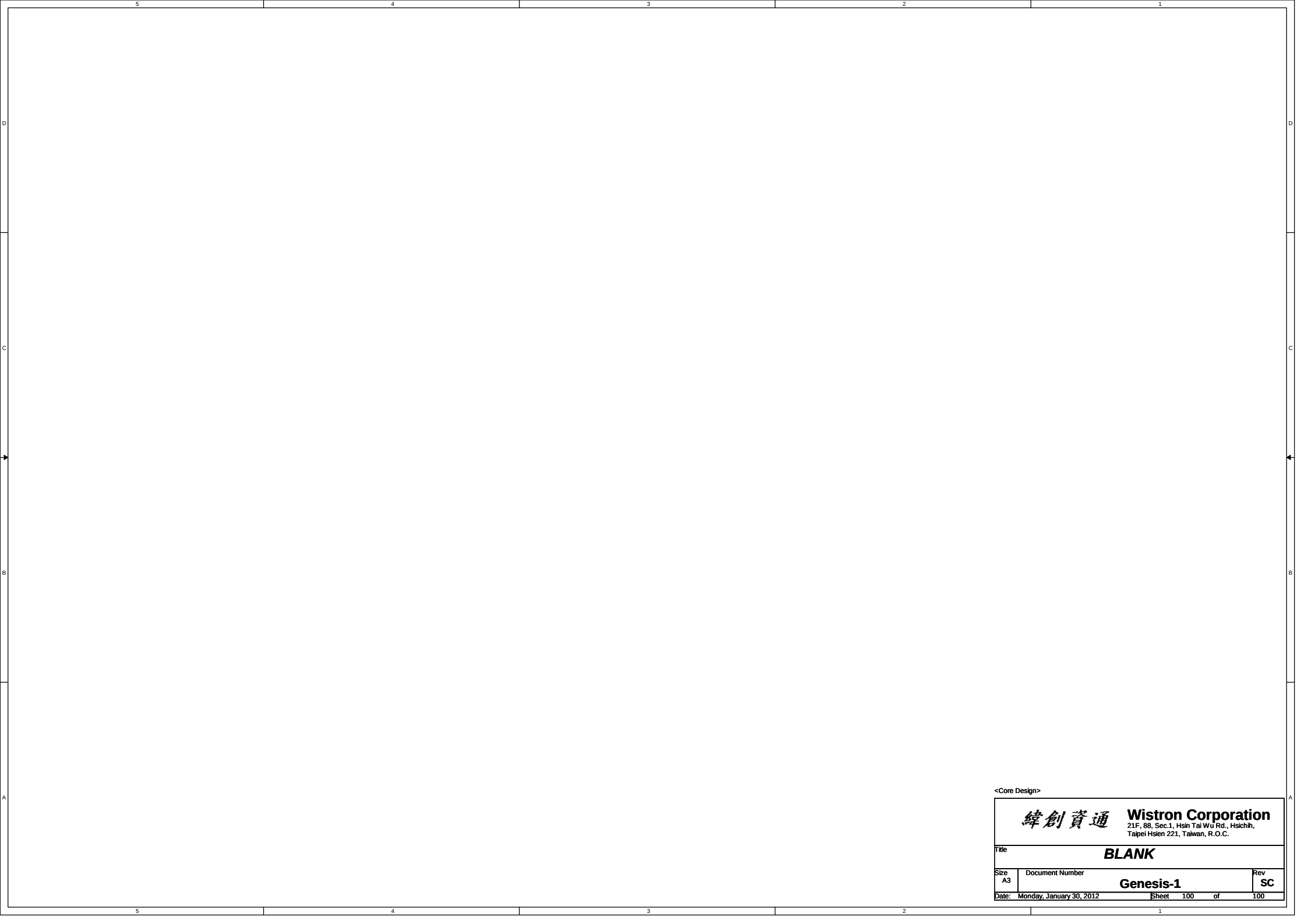
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RF decoupling caps

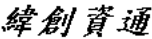
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Long power trace EMI decoupling caps





<Core Design>

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