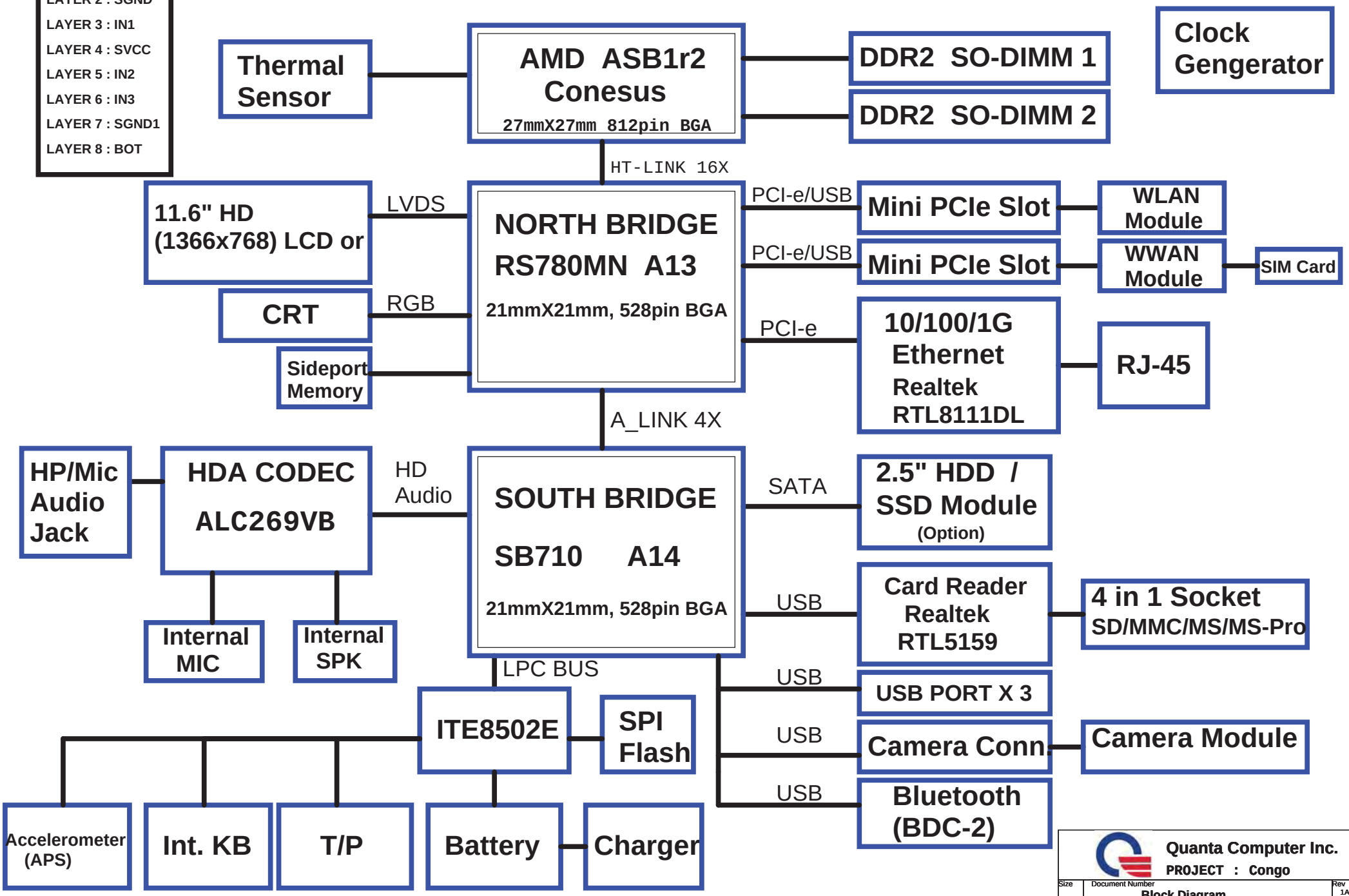
MK-Note Block Diagram -- AMD CONGO

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



Quanta Computer Inc.
PROJECT : Congo

Size	Document Number	Rev
	Block Diagram	1A
Date: Thursday, October 22, 2009	Sheet 1 of 42	

CLK_GEN_SLG8SP628

+3V — L40 BLM18EG601SN1D_6 — +3V_CLK_VDD — 3.3V(250mA)

C484 22U/6.3V_8 | C325 0.1U/10V_4 | C286 0.1U/10V_4 | C287 0.1U/10V_4 | C285 0.1U/10V_4 | C315 0.1U/10V_4 | C347 0.1U/10V_4 | C354 0.1U/10V_4

+1.2V — L27 BLM18AG601SN1D_6 — +1.2V_CLK_VDDIO — 1.2V(53mA)

C339 22U/6.3V_8 | C284 0.1U/10V_4 | C288 0.1U/10V_4 | C321 0.1U/10V_4 | C342 0.1U/10V_4 | C353 0.1U/10V_4

ICS9LPRS480	P/N : ALPRS480000
SLG8SP628	P/N : AL8SP628000
RTM880N-796	P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

+3V — L39 BLM18AG601SN1D_6 — +3V_CLK_48 — 3.3V(53mA) — C483 2.2U/6.3V_6

U18 — QFN64 — SLG8SP628

VDDDOT, VDDSRC, VDDATIG, VDDSB_SRC, VDDSATA, VDDCPU, VDDHTT, VDDREF, VDD48 ← +3V_CLK_VDD

VDDSRC_IO0, VDDSRC_IO1, VDDATIG_IO, VDDSB_SRC_IO, VDDCPU_IO ← +1.2V_CLK_VDDIO

GND48, GNDDOT, GNDSRC0, GNDSRC1, GNDATIG, GNDSB_SRC, GNDSATA, GNDCPU, GNDHTT, GNDREF

C338 33P/50V_4 — CG_XIN — Y4 14.318MHZ — CG_XOUT — C350 33P/50V_4

CG_XIN, CG_XOUT → X1, X2

11,15,27 PCLK_SMB, 11,15,27 PDAT_SMB → SMBCLK, SMBDAT

CLK_PD# → PD#

+3V_CLK_VDD — R222 8.2K_4 — CLK_PD#

T59 CLKREQ0# → CLKREQ0#
T53 CLKREQ1# → CLKREQ1#
T49 CLKREQ2# → CLKREQ2#
T54 CLKREQ3# → CLKREQ3#
T48 CLKREQ4# → CLKREQ4#

TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9 (65 66 67 68 69 70 71 72 73 74)

CPUK8_0T, CPUK8_0C: 50 CLK_CPUP_R, 49 CLK_CPUN_R — RP32 — 0_4P2R_4 — R186 *261/F_4 — CLK_CPUP 5, CLK_CPUN 5 — To CPU Diff 200MHz

ATIG0T, ATIG0C, ATIG1T, ATIG1C: 30 CLK_NBGFXP_R, 29 CLK_NBGFXN_R — RP33 — 0_4P2R_4 — CLK_NBGFXP 8, CLK_NBGFXN 8 — To NB Diff 100MHz

SB_SRC0T, SB_SRC0C, SB_SRC1T, SB_SRC1C: 37 CLK_SBREFP_R, 36 CLK_SBREFN_R — RP30 — 0_4P2R_4 — CLK_SBREFP 8, CLK_SBREFN 8 — To NB Diff 100MHz
32 CLK_SBSRCP_R, 31 CLK_SBSRCN_R — RP31 — 0_4P2R_4 — CLK_SBSRCP 10, CLK_SBSRCN 10 — To SB Diff 100MHz

SRC0T, SRC0C, SRC1T, SRC1C, SRC2T, SRC2C, SRC3T, SRC3C, SRC4T, SRC4C:
22 NBGPP_CLKP_R — T61
21 NBGPP_CLKN_R — T63
20 CLK_PCIE_NEW_R — T60
19 CLK_PCIE_NEW#_R — T62
15 CLK_PCIE_WLANP_R — RP37 — 0_4P2R_4 — CLK_PCIE_WLANP 23, CLK_PCIE_WLANN 23 — To Mini PCIE Slot (WLAN)
14 CLK_PCIE_WLANN-R
13 CLK_PCIE_WANP_R — RP36 — 0_4P2R_4 — CLK_PCIE_WANP 24, CLK_PCIE_WANN 24 — To Mini PCIE Slot (WWAN)
12 CLK_PCIE_WANN_R
9 CLK_PCIE_LANP_R — RP35 — 0_4P2R_4 — CLK_PCIE_LANP 19, CLK_PCIE_LANN 19 — To LAN Controller
8 CLK_PCIE_LANN_R

SRC6T/SATAT, SRC6C/SATAC, SRC7T/27M_SS, SRC7C/27M_NS:
42 — T42
41 — T44
6 — T64
5 — T65

HTT0T/66M, HTT0C/66M: 54 NBHT_REFCLKP_R, 53 NBHT_REFCLKN_R — RP34 — 0_4P2R_4 — HT_REFCLKP 8, HT_REFCLKN 8 — To NB Diff 100MHz

48MHz_0: 64 CLK_48M_USB_R — R274 22_4, R275 *22_4 — CLK_48M_USB 11, CLK_48M_USB_CR 22 — To SB 48MHz, To RTS5159 48MHz

EC A57

REF0/SEL_HTT66, REF1/SEL_SATA, REF2/SEL_27: 59 SEL_HTT66, 58 SEL_SATA, 57 SEL_27 — R205 33_4, R279 158/F_4 — EXT_SB_OSC 10, EXT_NB_OSC 8 — To SB 14.318MHz, To NB 14.318MHz

R278 90.9/F_4

R4004/R4005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15

RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

EC A30

+3V — R165 10K_4 — 19 PCIE_REQ_LAN# — CLKREQ4#

+3V — R164 10K_4 — 24 PCIE_REQ_WWAN# — CLKREQ3#

+3V — R176 10K_4 — 23 PCIE_REQ_WLAN# — CLKREQ2#

+3V_CLK_VDD — R214 *8.2K_4 — SEL_SATA, SEL_HTT66, SEL_27 — R237 8.2K_4, R248 8.2K_4, R280 8.2K_4

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0 *	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

CLK_48M_USB_R — C355 *10P_4
SEL_SATA — C313 *10P_4
SEL_27 — C359 *10P_4

EMI Cap placement close IC

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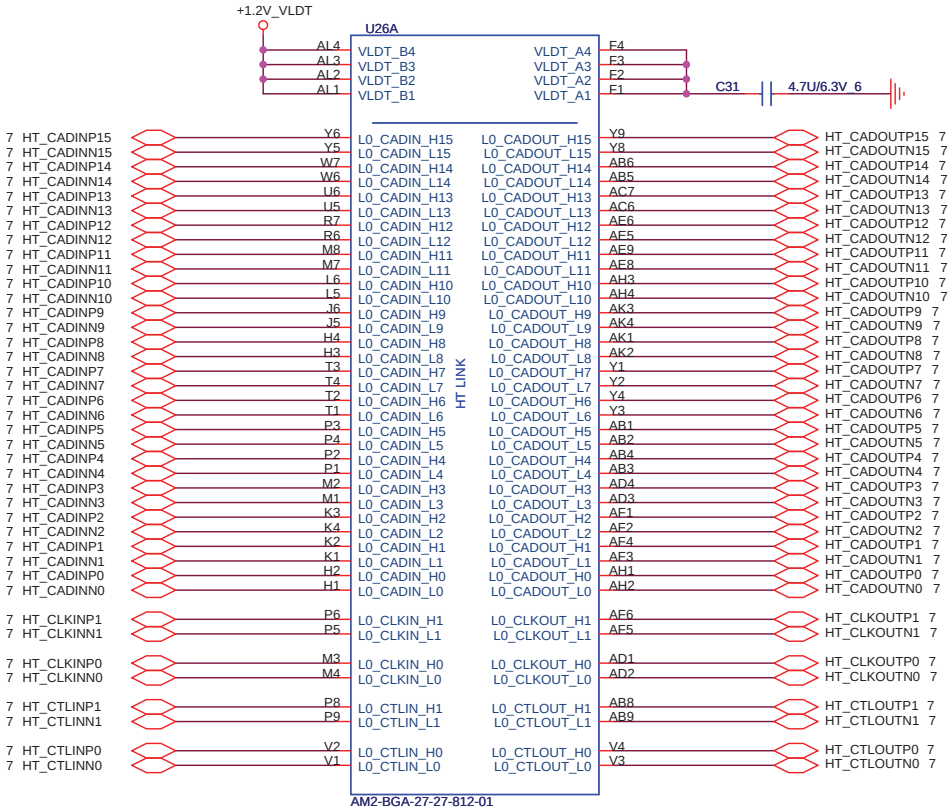
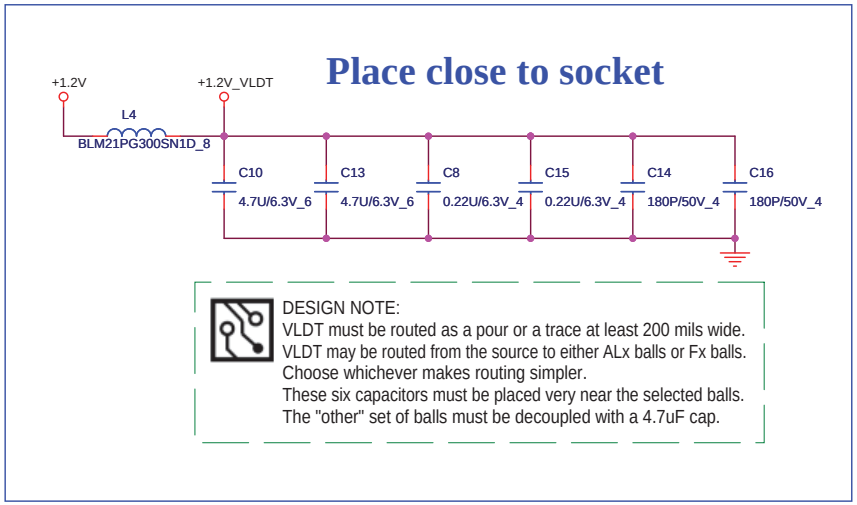
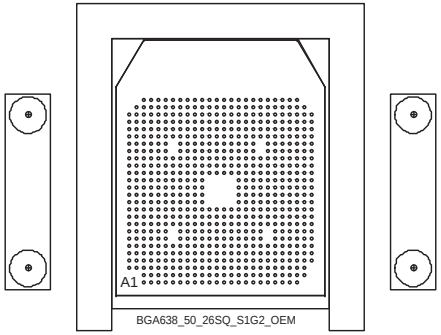
Size	Document Number	Rev
	CLOCK GEN SLG8SP628	1A
Date: Thursday, October 22, 2009	Sheet 2 of 42	







CPU

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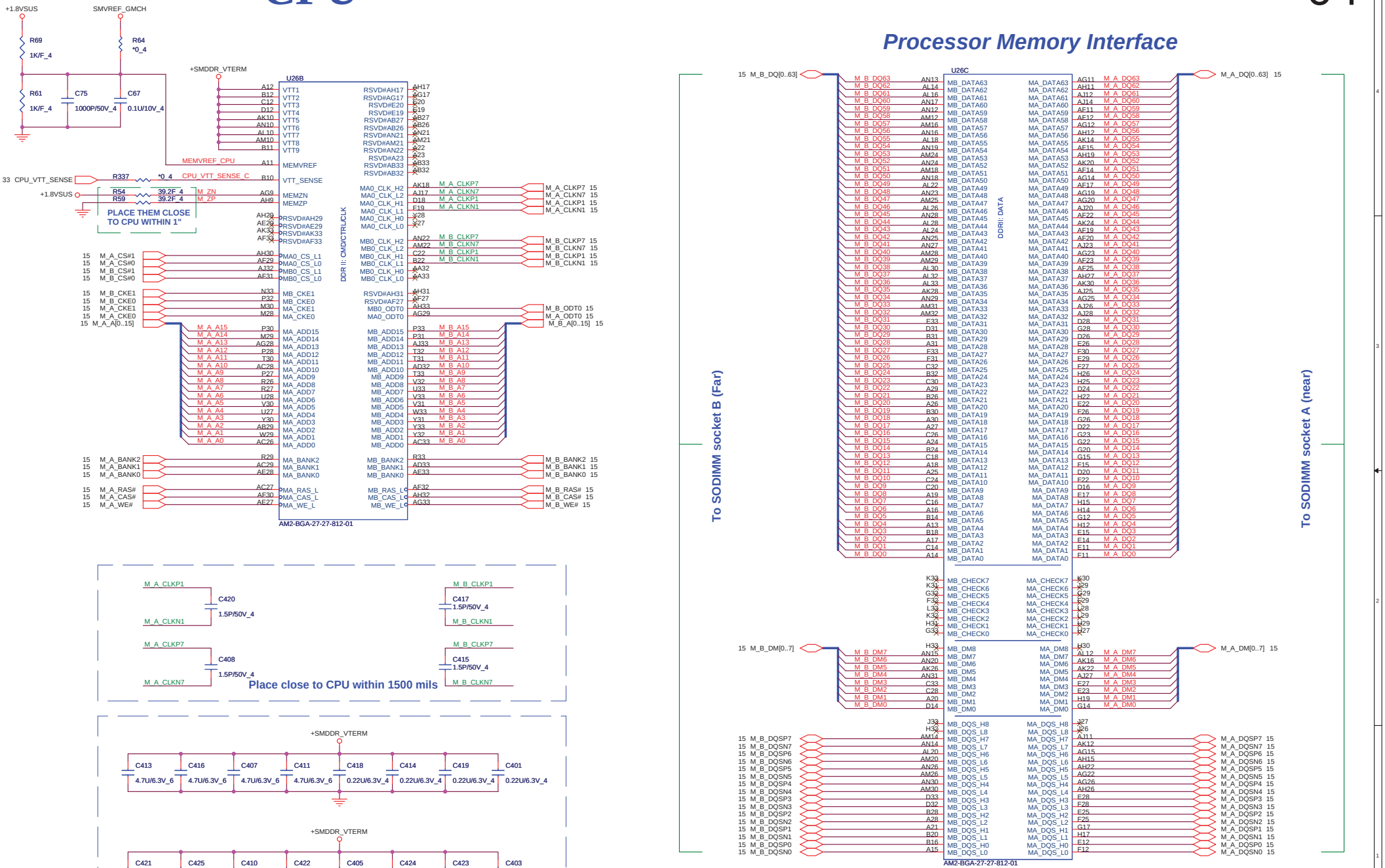
Size	Document Number	Rev
	K8G BGA HT I/F 1/4	1A
Date: Thursday, October 22, 2009	Sheet 3 of 42	

CPU

Processor Memory Interface



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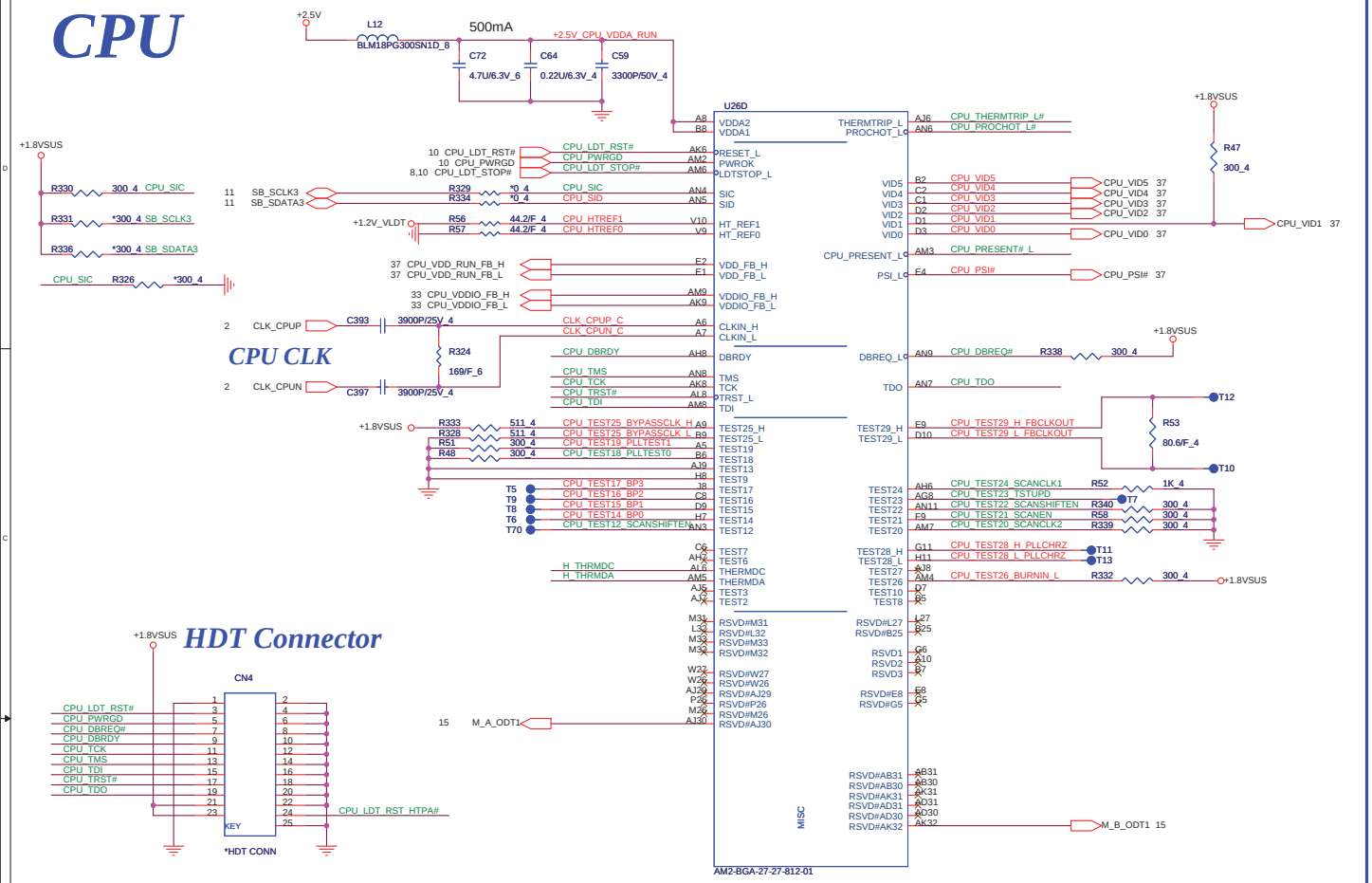
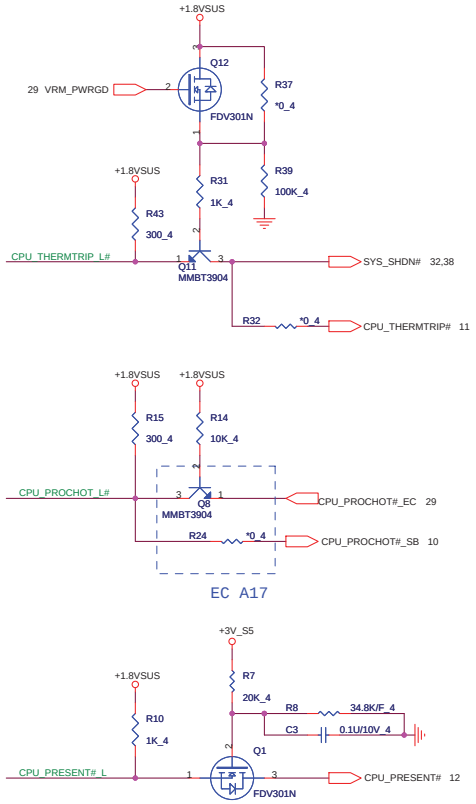
PROJECT : Congo			
Size	Document Number		Rev
	K8G BGA DDR2 MEMORY I/F 2/4		1A
Date: Thursday, October 22, 2009		Sheet 4 of 42	

CPU

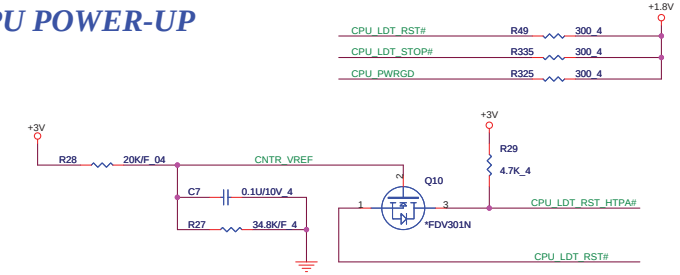


HDT Connector

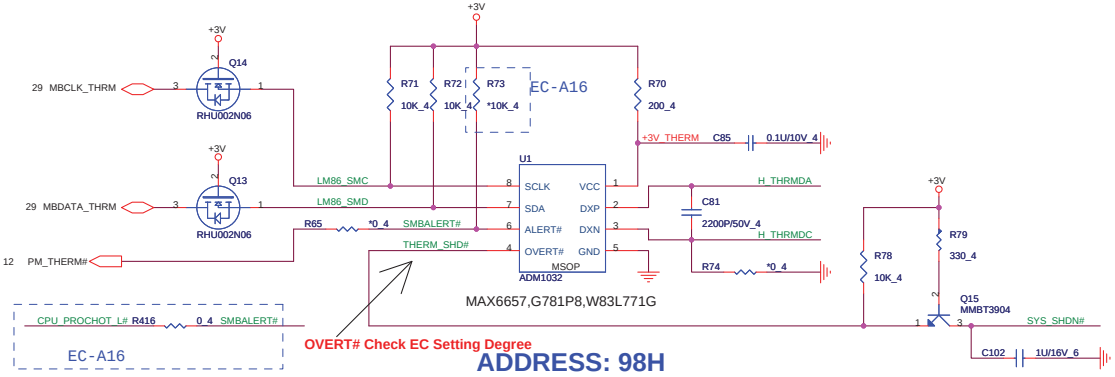
CPU THERM



CPU POWER-UP



CPU H/W MONITOR



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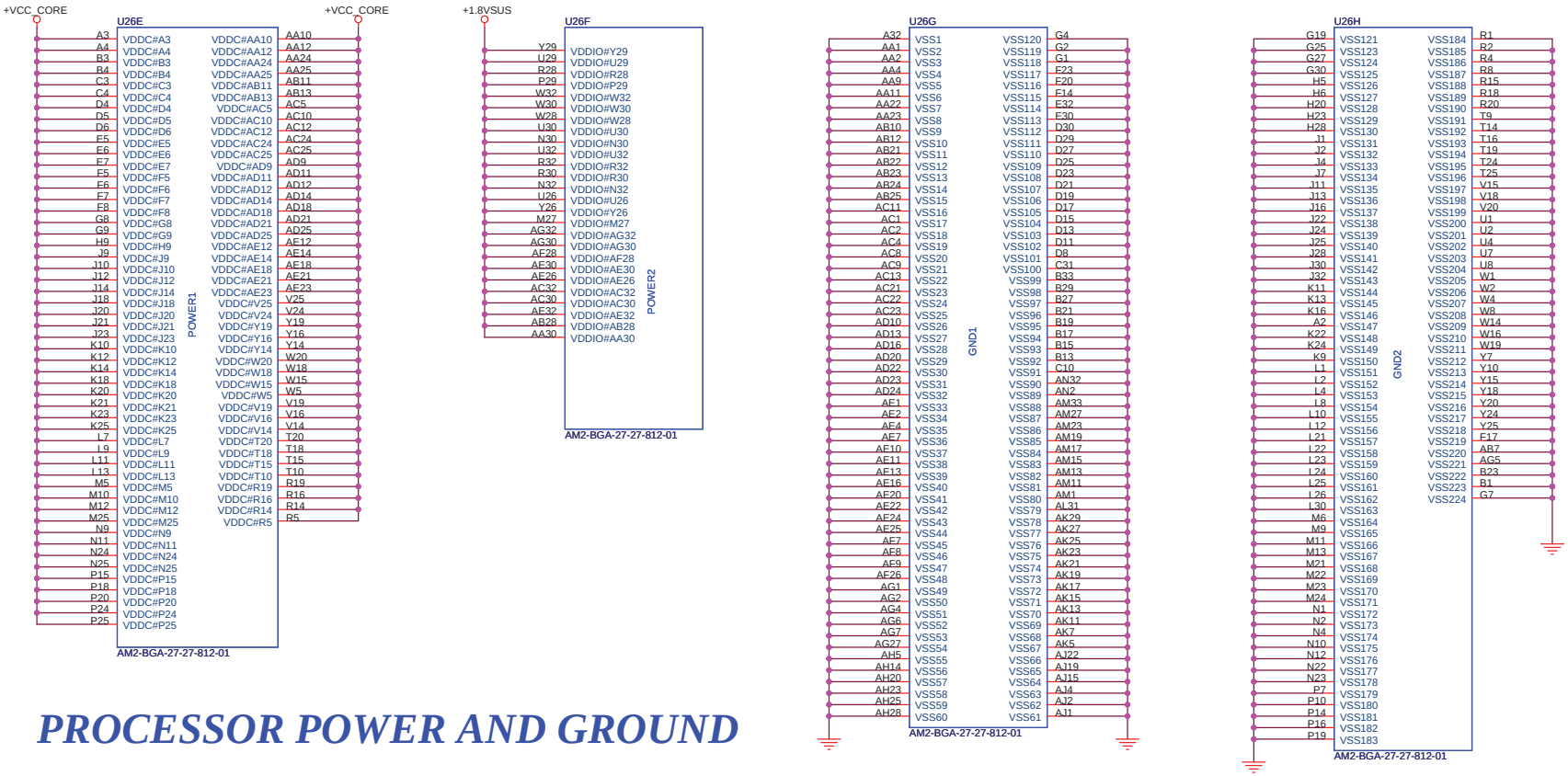
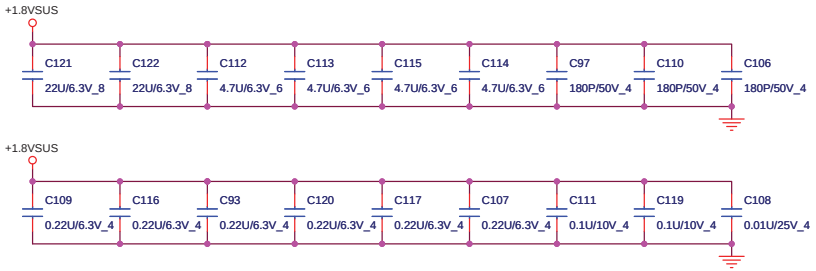
Size | Document Number | Rev
K8G BGA CTRL & DEBUG 3/4 | 1A
Date: Thursday, October 22, 2009 | Sheet 5 of 42

CPU

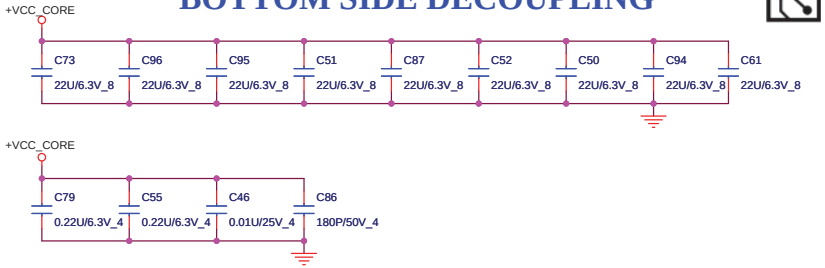


PROCESSOR POWER AND GROUND

DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



BOTTOM SIDE DECOUPLING



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PROJECT : Congo

Size	Document Number	Rev
	K8G BGA PWR & GND 4/4	1A

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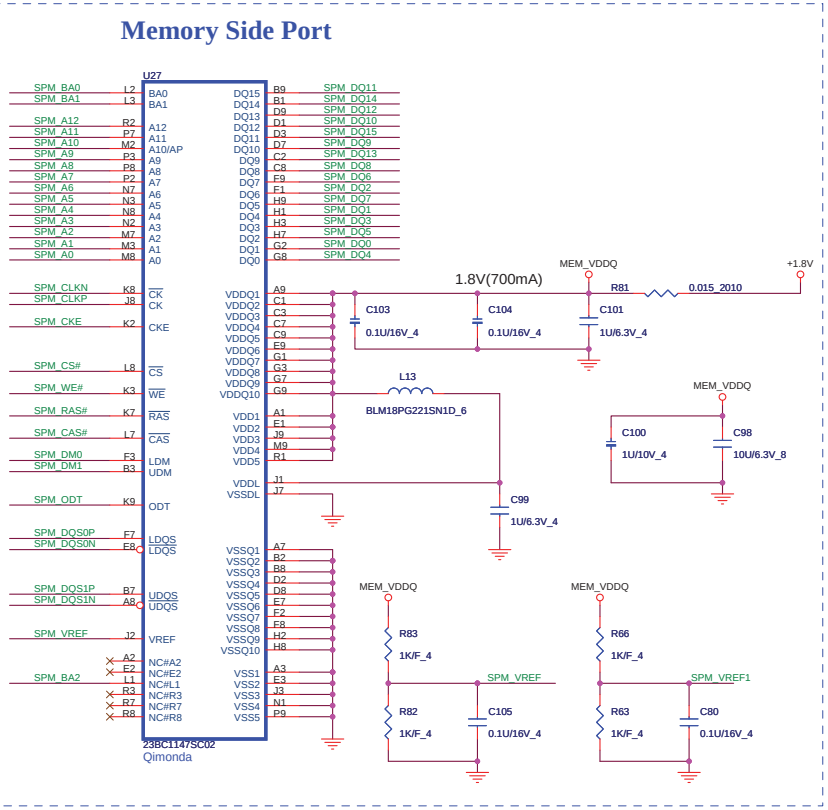
RS780

RS780 Display Port Support (muxed on GFX)

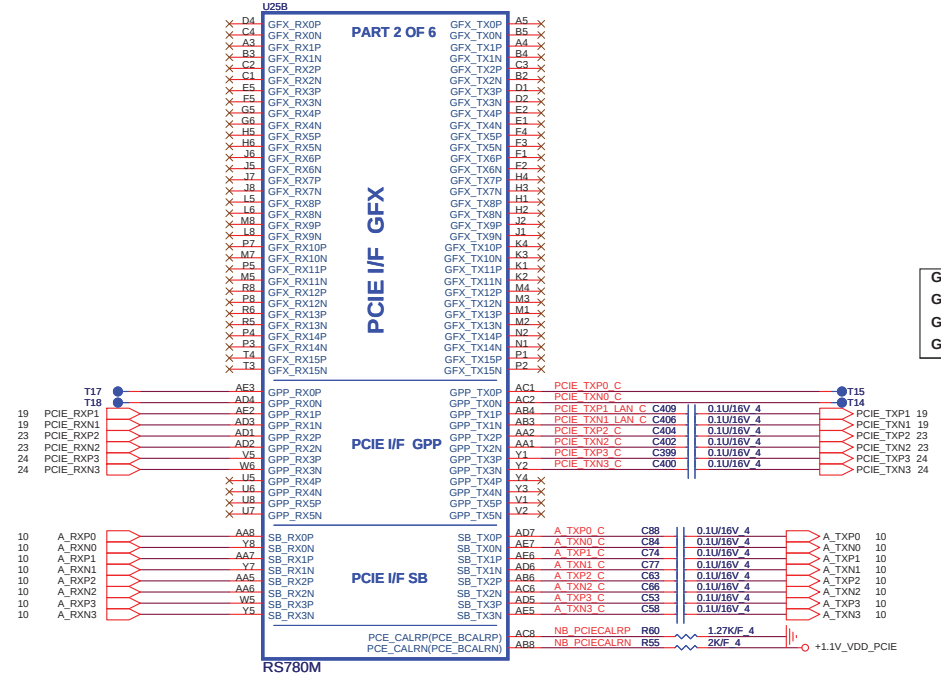
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

GPP0	X
GPP1	PCIE LAN(Atheros)
GPP2	Wireless Lan
GPP3	WWAN

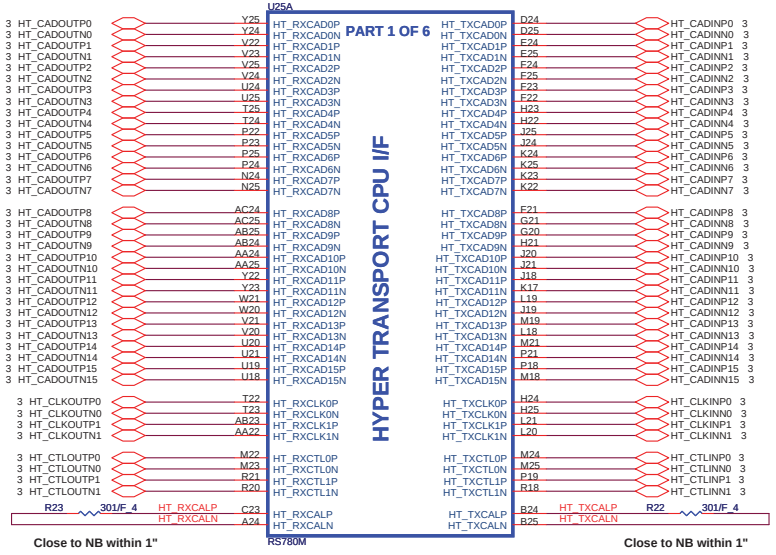
Memory Side Port



U25B — RS780M



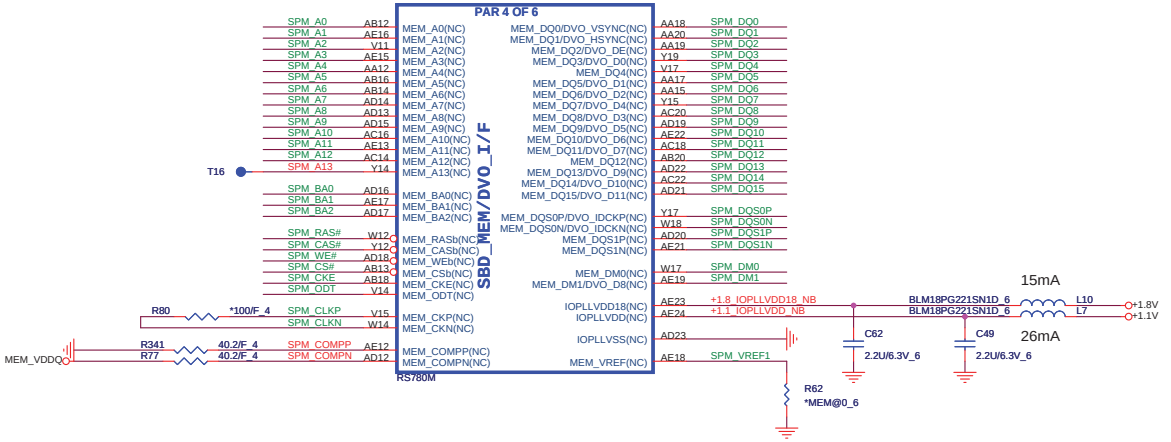
U25A — RS780M



Close to NB within 1"

Close to NB within 1"

U25D — SB_MEM/DVO_I/F



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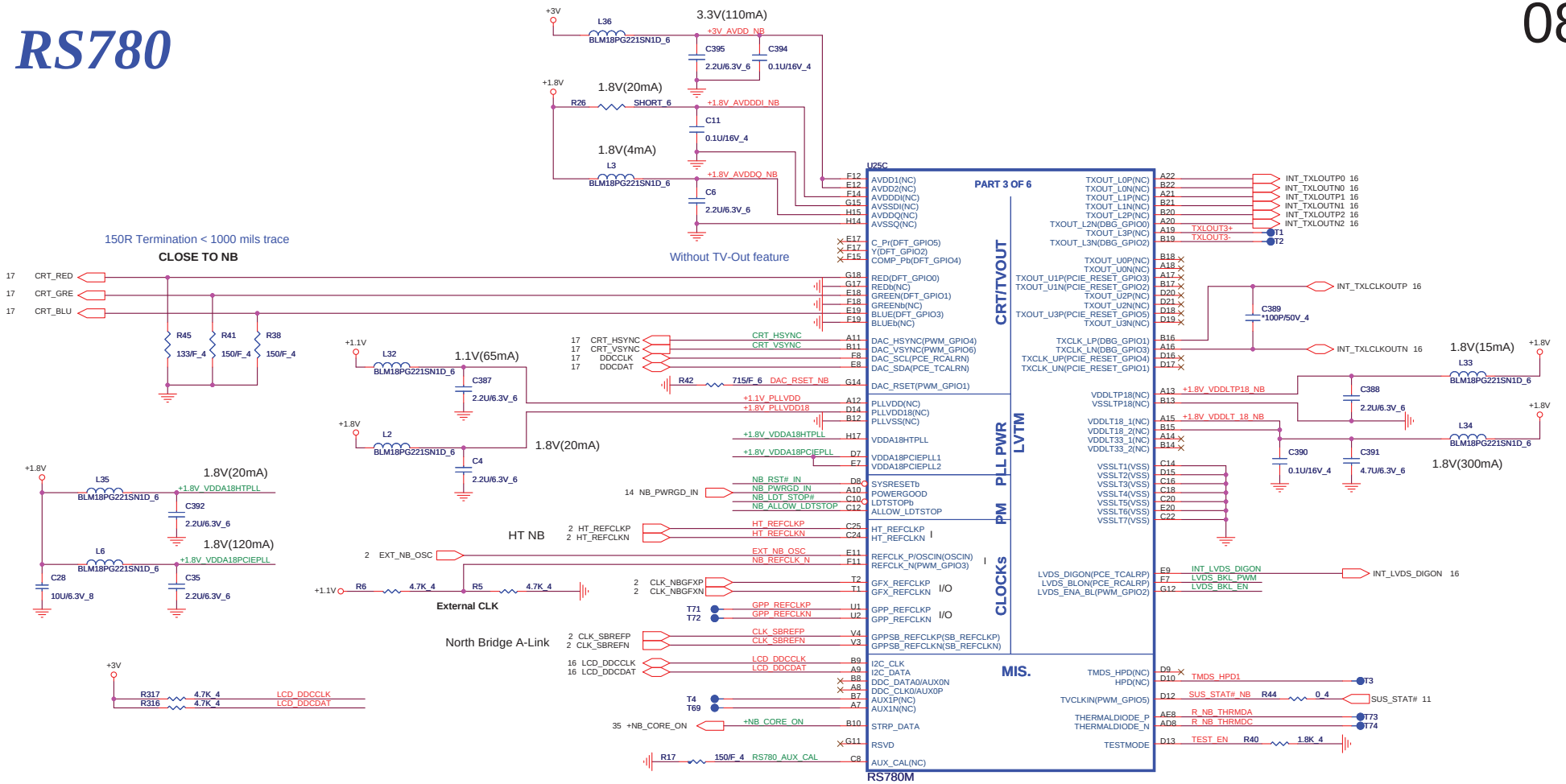
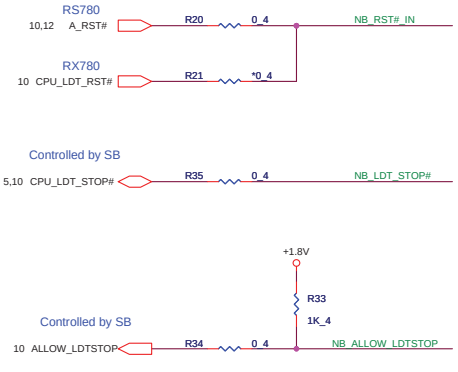
PROJECT : Congo			
Size	Document Number		Rev
	RS780-HT LINK/PCIE/MEM I/F 1/3		1A
Date: Thursday, October 22, 2009		Sheet 7 of 42	

RS780

08



North Bridge RESET

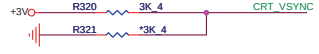


STRAP DEBUG BUS GPIO

RS780M: Enables Side port memory

For Side Port Enables/Disable
0 : Enable(Default) 1 : Disable

STRAP_DEBUG_BUS_GPIO_ENABLEb

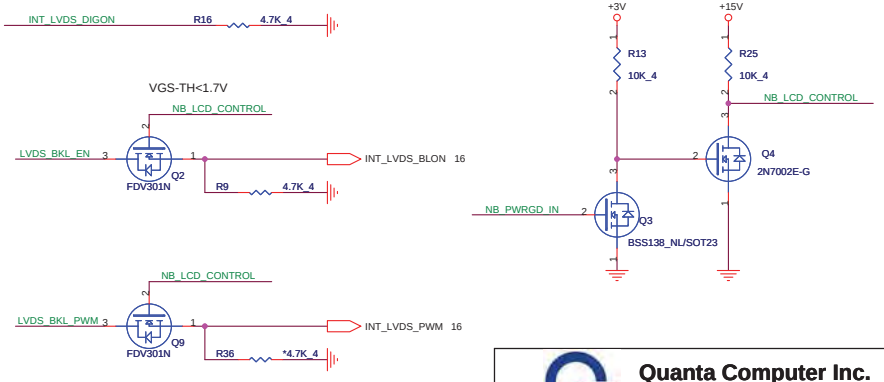


Enables the Test Debug Bus using GPIO.(RS780 -->VSYNC#)
1 : Enable(Defult) 0 : Disable

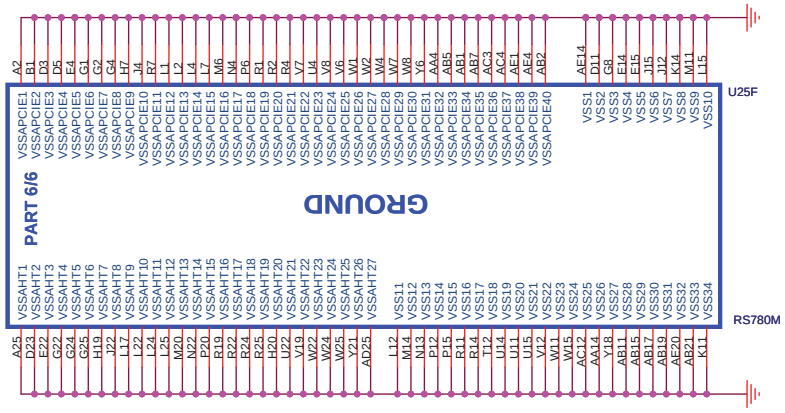
AUX CAL Value need update

Northbridge Core Voltage
1 : 1.0V 0 : 1.1V (default)

LVDS BLON

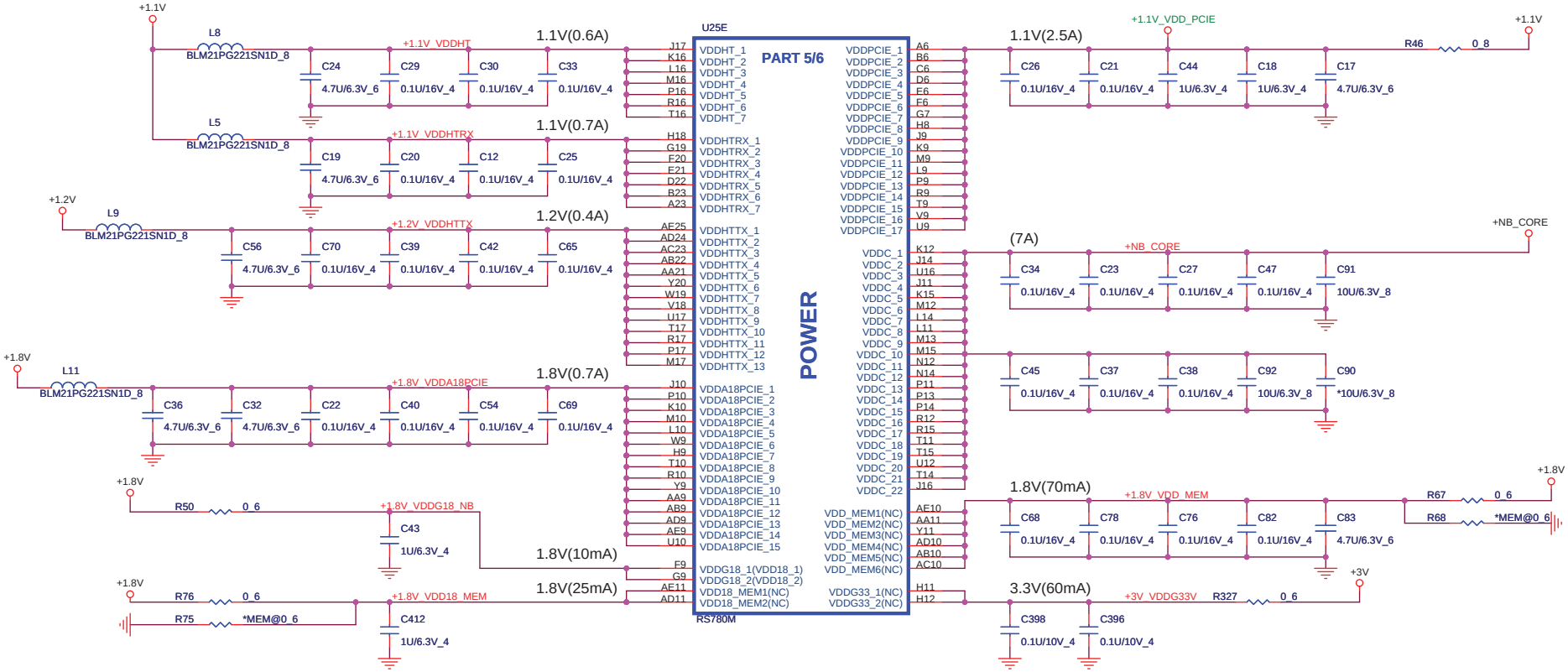


Quanta Computer Inc.			
PROJECT : Congo			
Size	Document Number		Rev
	RS780-SYSTEM/STRAPS I/F 2/3		1A
Date: Thursday, October 22, 2009		Sheet 8 of 42	



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



RS780

Quanta Computer Inc.		
PROJECT : Congo		
Size	Document Number: RS780-POWER/GND 3/3	Rev: 1A
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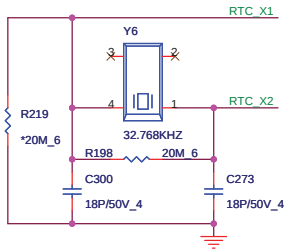
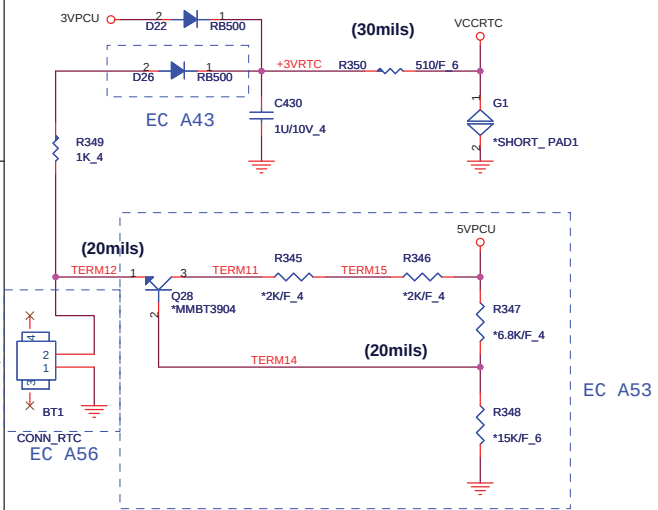
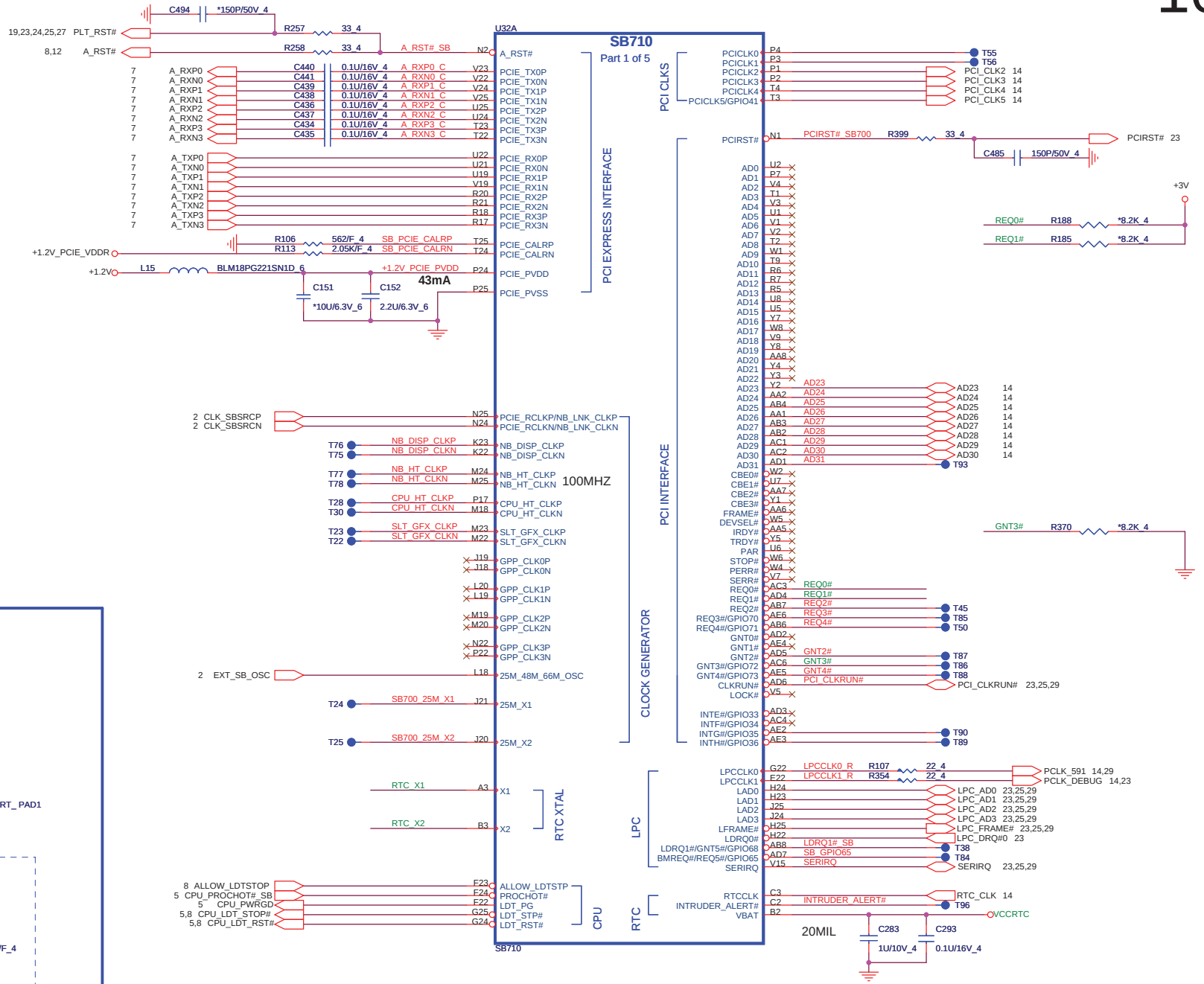
SB710

RTC XTAL



RTC





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PROJECT : Congo
Size | Document Number: SB710-PCIE/PCI/CPU/LPC 1/4 | Rev 1A
Date: Thursday, October 22, 2009 | Sheet 10 of 42

SB710

EMI

CLK_48M_USB — R172 *10_4 — C269 *10p/50V_4

SB710 (U32D) — Part 4 of 5

48MHz

USBCLK/14M_25M_48M_OSC — C8 — CLK_48M_USB — CLK_48M_USB 2

USB_RCOMP — G8 — USB_RCOMP_SB — R163 11.8K/F_6

Input

ACPI / WAKE UP EVENTS

T58	E1	PCI_PME#/GEVENT4#
T95	F2	RI#/EXTEVNT0# (RI#)
T36	H7	SLP_S2/GPM9# (SLP_S2)
29 PM_SLP_S3#	F5	SLP_S3#
29 PM_SLP_S4#	G1	SLP_S4#
29 DNBSWON#	H2	PWR_BTN#
14 SB_PWRGD_IN	H1	PWR_GOOD
8 SUS_STAT#	K3	SUS_STAT# (SUS_STAT#)
R242 *2.2K_4 SB_TEST2	H5	TEST2
+3V_S5 — R253 *2.2K_4 SB_TEST1	H4	TEST1
R252 *2.2K_4 SB_TEST0	H3	TEST0
29 GATEA20	V15	GA20IN/GEVENT0#
29 RCIN#	W15	KBRST#/GEVENT1#
29 SCI#	K4	LPC_PME#/GEVENT3#
29 KBSMI#	K24	LPC_SMI#/EXTEVNT1#
T94	F1	S3_STATE/GEVENT5#
	J2	SYS_RESET#/GPM7# (SYS_RST#)
23,29 WAKE#	H6	WAKE#/GEVENT8#
T97	F2	BLINK/GPM6# (GPM6#)
5 CPU_THERMTRIP#	J6	SMBALERT#/THRMTRIP#/GEVENT2#
14 WD_PWRGD	W14	NB_PWRGD
29 ICH_RSMRST#	D3	RSMRST#

USB MISC / USB 1.1

	E6	USB_FSD13P
	E7	USB_FSD13N
	F7	USB_FSD12P
	E8	USB_FSD12N
	H11	USB_HSD11P
	J10	USB_HSD11N
	E11	USB_HSD10P
	F11	USB_HSD10N
	A11	USB_HSD9P
	B11	USB_HSD9N

EC A25

	C10	USB_HSD8P — USBP5+ 23
	D10	USB_HSD8N — USBP5- 23

Min-Card(WLAN)

	G11	USB_HSD7P — USBP7+ 16
	H12	USB_HSD7N — USBP7- 16

CCD

	E12	USB_HSD6P — USBP6+ 22
	E14	USB_HSD6N — USBP6- 22

3 IN 1 CARD READER (MMC)

EC A25

	C12	USB_HSD5P
	D12	USB_HSD5N
	B12	USB_HSD4P — USBP2+ 21
	A12	USB_HSD4N — USBP2- 21

USB3 Connector

	G12	USB_HSD3P — USBP3+ 25
	G14	USB_HSD3N — USBP3- 25

EC A25 BLUETOOTH

	H14	USB_HSD2P — USBP4+ 24
	H15	USB_HSD2N — USBP4- 24

Min-Card(WWAN)

	A13	USB_HSD1P — USBP1+ 21
	B13	USB_HSD1N — USBP1- 21

USB2 Connector

	B14	USB_HSD0P — USBP0+ 21
	A14	USB_HSD0N — USBP0- 21

USB1 Connector

GPIO / USB 2.0

BOARD_ID2	AE18	SATA_IS0#/GPIO10
BOARD_ID1	AD18	CLK_REQ3#/SATA_IS1#/GPIO6
BOARD_ID0	AA19	SMARTVOLT/SATA_IS2#/GPIO4
	W17	CLK_REQ0#/SATA_IS3#/GPIO0
BT_ON	V17	CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
T29	W20	CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
T27	W21	SPKR/GPIO2
18 ACZ_SPKR	AA18	SCL0/GPOC0# (PCLK_SMB)
2,15,27 PCLK_SMB	W18	SDA0/GPOC1# (PDAT_SMB)
2,15,27 PDAT_SMB	K1	SCL1/GPOC2# (SB_SMBCLK1)
	K2	SDA1/GPOC3# (SB_SMBDATA1)
R155 10K_4	AA20	DDC1_SCL/GPIO9 (BOARD_ID3)
	Y18	DDC1_SDA/GPIO8
CPULLB#	C1	LLB#/GPIO66
16 LCD_BK_OFF	Y19	SHUTDOWN#/GPIO5 (LCD_BK_OFF)
	G5	DDR3_RST#/GEVENT7#

EC A01

D2: 15 CPU_MEMHOT# — CH501H-40PT — CPU_MEMHOT#_IN

USB OC

T43	B9	USB_OC6#/IR_TX1/GEVENT6# (USBOC5_GPM5)
T33	B8	USB_OC5#/IR_TX0/GPM5# (USBOC4_GPM4)
T35	A8	USB_OC4#/IR_RX0/GPM4# (USBOC3_GPM3)
21 USBOC2#	A9	USB_OC3#/IR_RX1/GPM3#
21 USBOC1#	E5	USB_OC2#/GPM2#
21 USBOC0#	F8	USB_OC1#/GPM1#
	E4	USB_OC0#/GPM0#

HD AUDIO

ACZ_BCLK	M1	AZ_BITCLK
ACZ_SDOUT	M2	AZ_SDOUT
18 ACZ_SDIN0	J7	AZ_SDIN0/GPIO42
T37	J8	AZ_SDIN1/GPIO43
T41	L8	AZ_SDIN2/GPIO44
T92	M3	AZ_SDIN3/GPIO46
ACZ_SYNC	L6	AZ_SYNC
14 ACZ_RST#	M4	AZ_RST# (ACZ_RST#)
	L5	AZ_DOCK_RST#/GPM8#

INTEGRATED uC

	G20	IMC_GPIO18
	G21	IMC_GPIO19
	D25	IMC_GPIO20
	D24	IMC_GPIO21
	C25	IMC_GPIO22
	C24	IMC_GPIO23
	B25	IMC_GPIO24
	C23	IMC_GPIO25
	B24	IMC_GPIO26
	B23	IMC_GPIO27
	A23	IMC_GPIO28
	C22	IMC_GPIO29
	A22	IMC_GPIO30
	B22	IMC_GPIO31
	B21	IMC_GPIO32
	A21	IMC_GPIO33
	D20	IMC_GPIO34
	C20	IMC_GPIO35
	A20	IMC_GPIO36
	B20	IMC_GPIO37
	B19	IMC_GPIO38
	A19	IMC_GPIO39
	D18	IMC_GPIO40
	C18	IMC_GPIO41

INTEGRATED uC

	H19	IMC_GPIO0
	H20	IMC_GPIO1
	H21	SPI_CS2#/IMC_GPIO2
T20	F25	IDE_RST#/F_RST#/IMC_GPO3
	D22	IMC_GPIO4
	E24	IMC_GPIO5
	E25	IMC_GPIO6
	D23	IMC_GPIO7

IMC_GPIO

	A18	IMC_GPIO8 — BT_DET# 25
	B18	IMC_GPIO9 — WWAN_OFF# 24
IMC_PWM0/IMC_GPIO10	F21	CCD_ON 16
SCL2/IMC_GPIO11	D21	SB_SCLK2
SDA2/IMC_GPIO12	F19	SB_SDATA2
SCL3_LV/IMC_GPIO13	E20	SB_SCLK3 5
SDA3_LV/IMC_GPIO14	F21	SB_SDATA3 5
IMC_PWM1/IMC_GPIO15	E19	
IMC_PWM2/IMC_GPO16	D19	SB_GPIO16 14
IMC_PWM3/IMC_GPO17	E18	SB_GPIO17 14

SPI/LPC define

WLAN_OFF# 23

3G card detect

+3V_S5 — SCL1/SDATA1 is 3V/S5 tolerance, AMD datasheet define it

R357	2.2K_4	SB_SCLK2
R358	2.2K_4	SB_SDATA2
R236	2.2K_4	SB_SMBCLK1
R235	2.2K_4	SB_SMBDATA1
R221	47K_4	CPULLB#

+3V — SCL0/SDATA0 is 3V tolerance, AMD datasheet define it

R153	2.2K_4	PCLK_SMB
R148	2.2K_4	PDAT_SMB
R212	4.7K_4	SUS_STAT#

G2: 2 — 1 — SYS_RST# — *SHORT_ PAD1

HD Audio Interface

EC A32

18 ACZ_BITCLK_AUDIO — R273 INDUCTOR — ACZ_BCLK — C352 10p/50V_4 — R269 *10K_4 — To Azalia

18 ACZ_SDOUT_AUDIO — R245 33_4 — ACZ_SDOUT — C322 *10p/50V_4 — R232 *10K_4

18 ACZ_SYNC_AUDIO — R211 33_4 — ACZ_SYNC — C320 *10p/50V_4

18 ACZ_RST#_AUDIO — R261 33_4 — ACZ_RST#

MB ID Selection Table

BOARD_ID	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
DV	H	H	H	H
SIT	L	L	L	L
SVT	L	L	L	H
SOVP	L	L	H	L

MB ID

+3V

R143	1K_4	BOARD_ID0	R142	*10K_4
R132	1K_4	BOARD_ID1	R131	*10K_4
R139	1K_4	BOARD_ID2	R145	*10K_4
R110	1K_4	BOARD_ID3	R111	*10K_4

EC A18

Quanta Computer Inc.

PROJECT : Congo

Size	Document Number	Rev
	SB710-ACPI/GPIO/USB 2/4	1A

Date: Thursday, October 22, 2009 Sheet 11 of 42

SB710

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

SATA HDD

U32B

SB710
Part 2 of 5

SERIAL ATA

20 SATA_TXP0 — C456 0.01U/25V_4 — SATA_TXP0_C — AD9 SATA_TX0P
20 SATA_TXN0 — C455 0.01U/25V_4 — SATA_TXN0_C — AE9 SATA_TX0N
20 SATA_RXN0 — C454 0.01U/25V_4 — SATA_RXN0_C — AB10 SATA_RX0N
20 SATA_RXP0 — C453 0.01U/25V_4 — SATA_RXP0_C — AC10 SATA_RX0P
T83 — AE10 SATA_TX1P
T82 — AD10 SATA_TX1N
T80 — AD11 SATA_RX1N
T81 — AE11 SATA_RX1P
T31 — AB12 SATA_TX2P
T34 — AC12 SATA_TX2N
T32 — AE12 SATA_RX2N
T79 — AD12 SATA_RX2P
AD13 SATA_TX3P
AE13 SATA_TX3N
AB14 SATA_RX3N
AC14 SATA_RX3P
AE14 SATA_TX4P
AD14 SATA_TX4N
AD15 SATA_RX4N
AE15 SATA_RX4P
AB16 SATA_TX5P
AC16 SATA_TX5N
AE16 SATA_RX5N
AD16 SATA_RX5P

ATA 66/100/133

IDE_IORDY AA24
IDE_IRQ AA25
IDE_A0 Y22
IDE_A1 AB23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AD25
IDE_IOR# AC25
IDE_IOW# AC24
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE22
IDE_D3/GPIO18 AC22
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AC20
IDE_D10/GPIO25 AD20
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23

SPI ROM

SPI_DI/GPIO12 G6
SPI_DO/GPIO11 D2
SPI_CLK/GPIO47 D1
SPI_HOLD#/GPIO31 E4
SPI_CS#/GPIO32 E3
LAN_RST#/GPIO13 U15 — LAN_RST# R259 *0_4 — A_RST# 8,10
ROM_RST#/GPIO14 J1 — ROM_RST# — T91

FANOUT0/GPIO3 M8 — SB_FANOUT0 — T39
FANOUT1/GPIO48 M5 — SB_FANOUT1 — T47
FANOUT2/GPIO49 M7 — SB_FANOUT2 — T40

HW MONITOR

FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8
TEMP_COMM C6
TEMPIN0/GPIO61 B6 — T57
TEMPIN1/GPIO62 A6 — T46
TEMPIN2/GPIO63 A5 — T52
TEMPIN3/TALERT#/GPIO64 B5 — PM_THERM# 5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4 — VIN3 — 0_4 R367 — CPU_PRESENT# 5
VIN4/GPIO57 D5 — VIN4 — T51
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7

SATA PWR

R159 1K/F_4 — SATA_RBIAS_PN — V12 SATA_CAL
SATA_X1 — Y12 SATA_X1
SATA_X2 — AA12 SATA_X2
27 SATA_LED# — W11 SATA_ACT#/GPIO67
+1.2V_PLLVDD_SATA — AA11 PLLVDD_SATA
+3V_XTLVDD_SATA — W12 XTLVDD_SATA

C183 27P/50V_4 — SATA_X1 — Y1 25MHZ — R112 10M_6 — SATA_X2 — C178 27P/50V_4

NOTE:
Resister IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

+1.2V — 1.2V (93mA) — L23 BLM18PG221SN1D_6 — +1.2V_PLLVDD_SATA — C238 2.2U/6.3V_6 — C237 *1U/10V_4

+3V — 3.3V (6mA) — L21 BLM18PG221SN1D_6 — 1mA — +3V_XTLVDD_SATA — C220 1U/10V_4

Place near ball

3.3V (5mA)

AVDD F6 — AVDD_HWM — C270 0.1U/10V_4 — C264 *2.2U/6.3V_6 — R166 0_6 — +3V_S5
AVSS G7

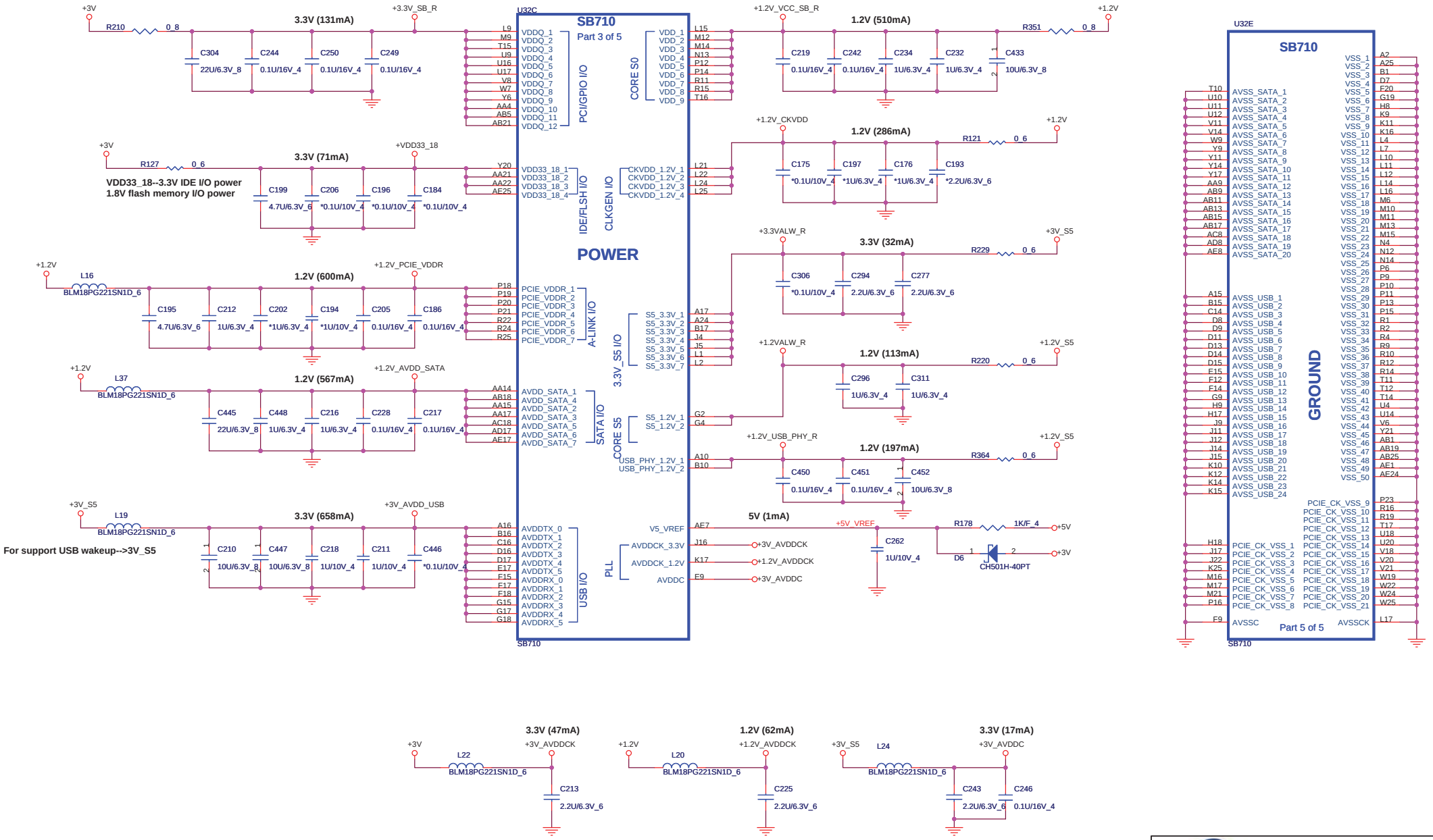
SB710

Quanta Computer Inc.
PROJECT : Congo

Size	Document Number	Rev
	SB710-SATAI/IDE/HWM/SPI 3/4	1A
Date: Thursday, October 22, 2009	Sheet 12 of 42	

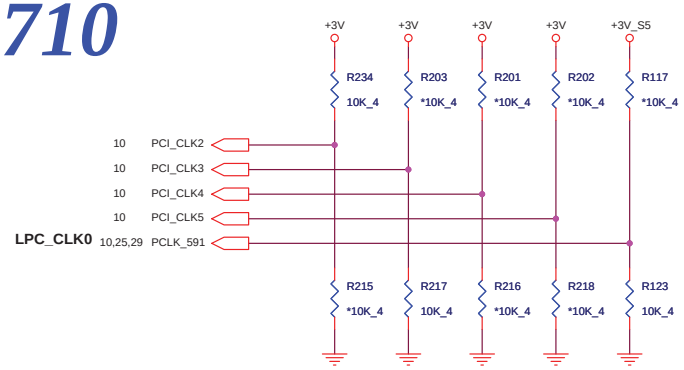
SB710

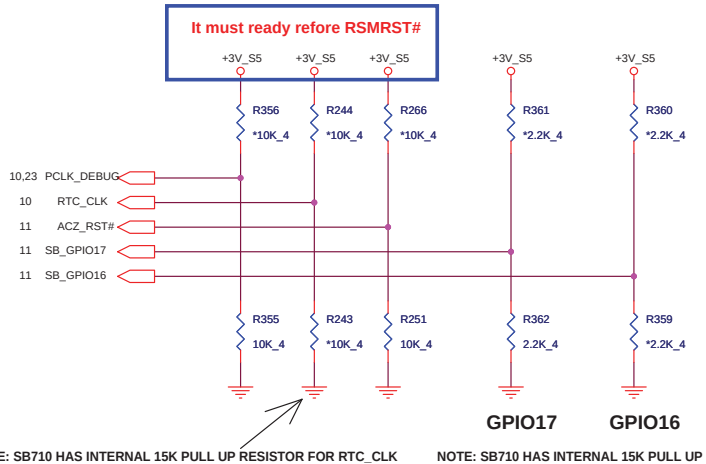
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



Quanta Computer Inc.	
PROJECT : Congo	
Size	Document Number: SB710-PWR/DECOUPLING 4/4 — Rev 1A
Date: Thursday, October 22, 2009	Sheet 13 of 42

SB710





NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR SB_GPIO16,SB_GPIO17.

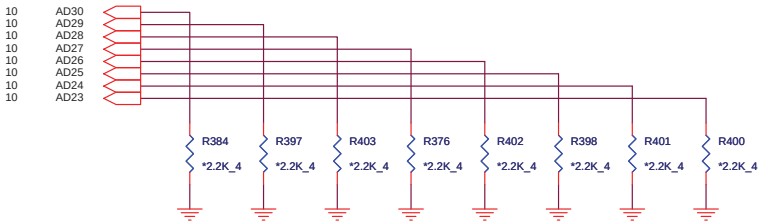
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0
PULL HIGH	BOOTFAIL TIMER ENABLED DEFAULT	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT

	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	

DEBUG STRAPS

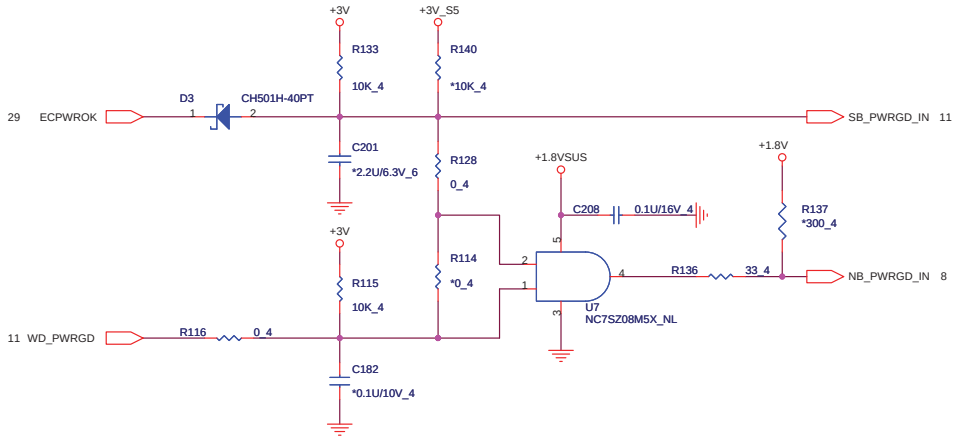
SB710 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



REQUIRED STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29	PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED		
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS		RESERVED	RESERVED

NB/SB POWER GOOD CIRCUIT



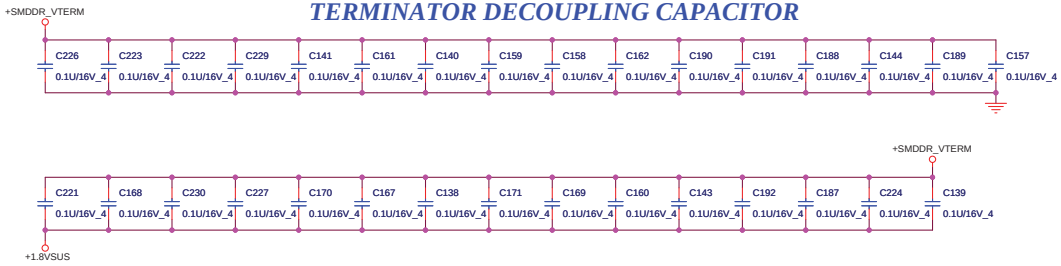
Quanta Computer Inc.

PROJECT : Congo

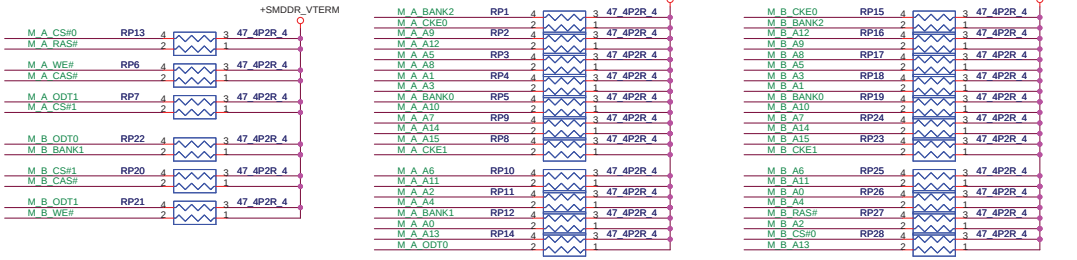
Size	Document Number	Rev
	SB710-STRAPS & PWRGD	1A

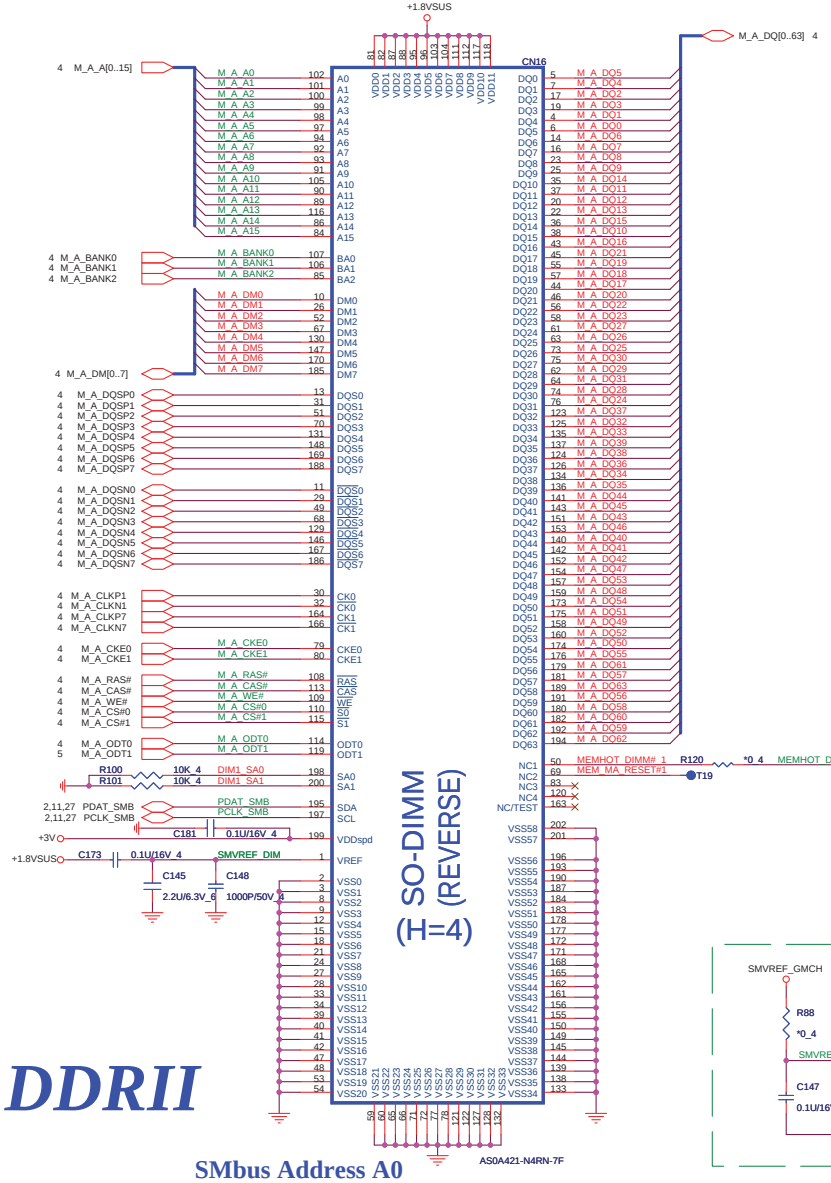
Date: Thursday, October 22, 2009 Sheet 14 of 42

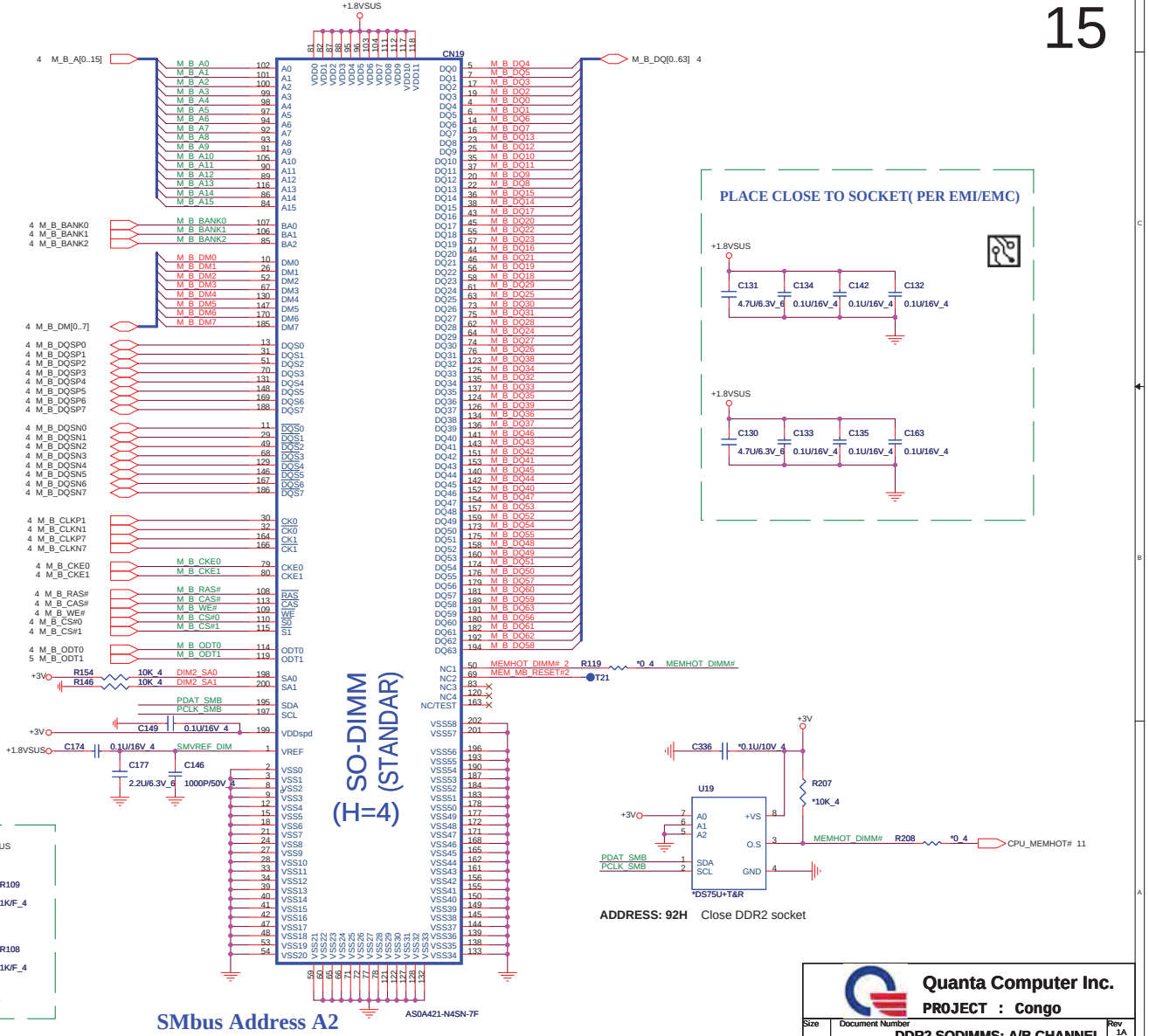
TERMINATOR DECOUPLING CAPACITOR



DDR2 TERMINATOR







ADDRESS: 92H Close DDR2 socket

DDRII

Quanta Computer Inc.		
PROJECT : Congo		
Size	Document Number: DDR2 SODIMMS: A/B CHANNEL	Rev: 1A
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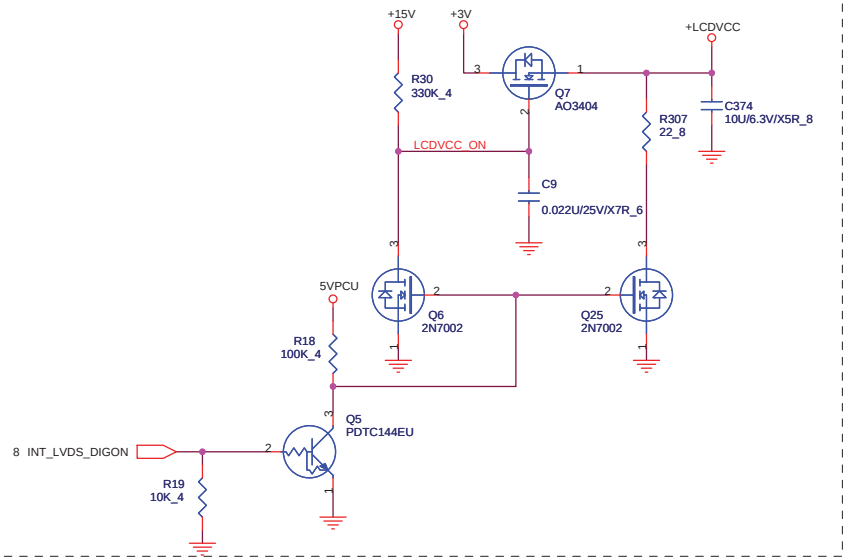
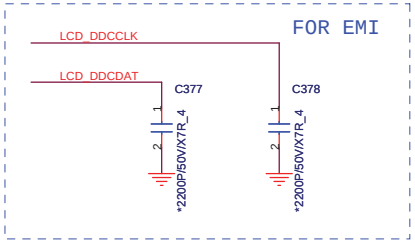
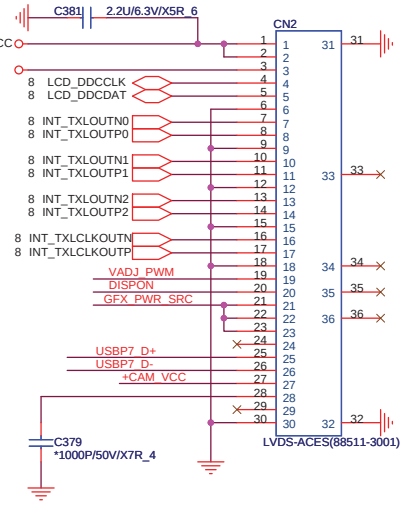
LCDVCC

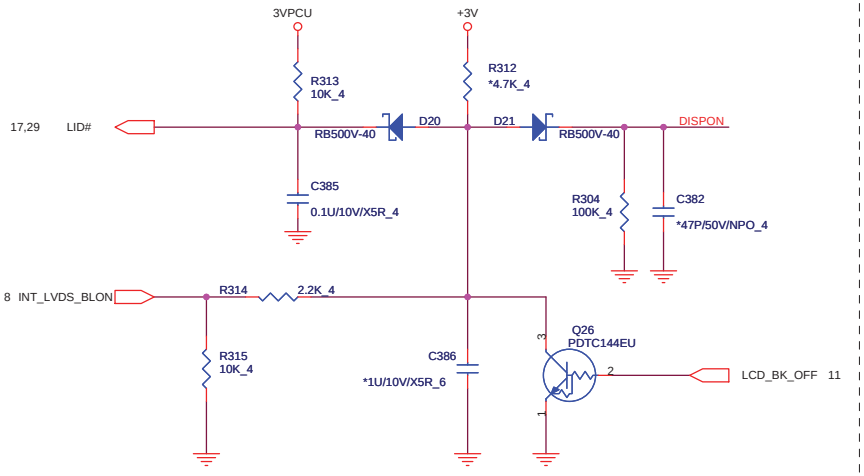


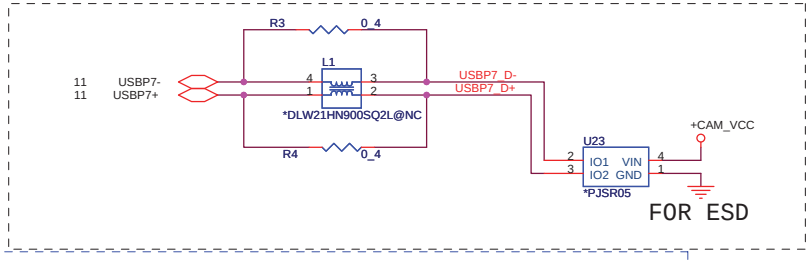
LVDS (11.6") (1024x600, 1366x768)

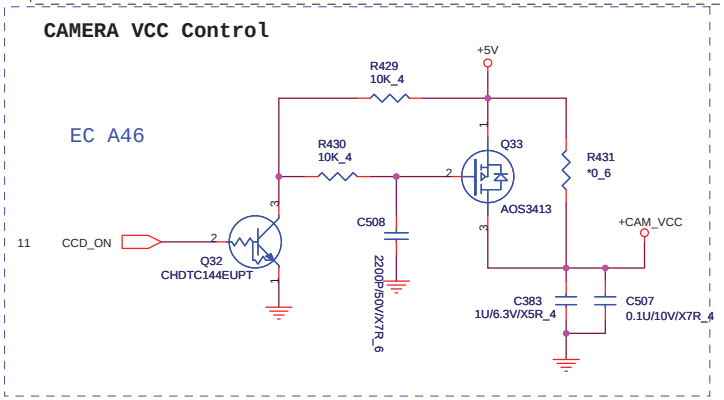


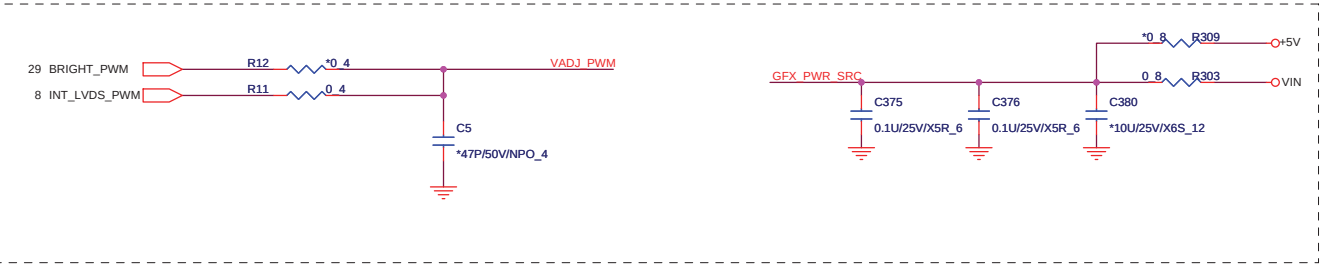


Back light





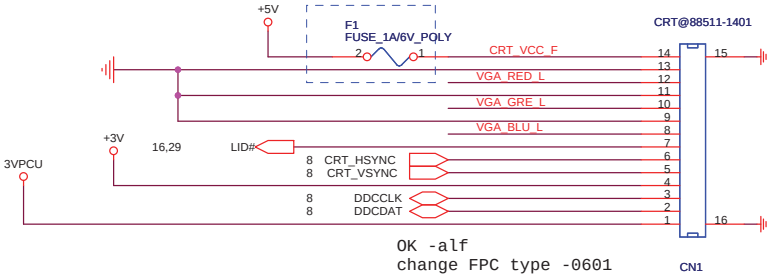




Quanta Computer Inc.
PROJECT : Congo

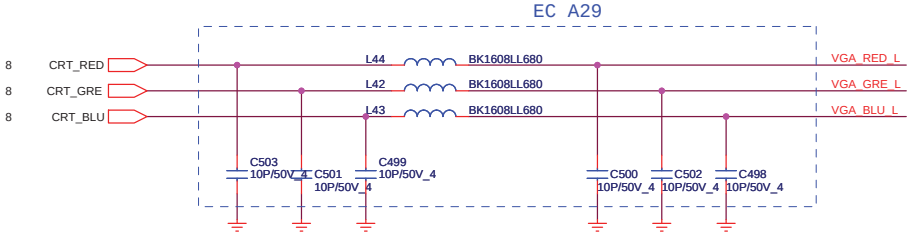
Size	Document Number	Rev
	LCD + CAMERA CONN	1A
Date: Thursday, October 22, 2009	Sheet 16 of 42	

EC A58



OK -alf
change FPC type -0601

EC A29



Quanta Computer Inc.

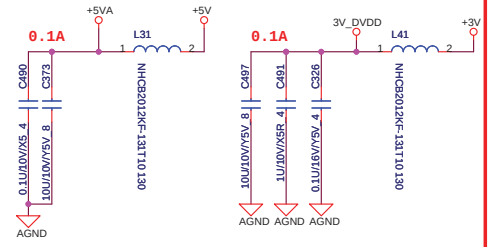
PROJECT : Congo

Size	Document Number	Rev
	CRT CONN	1A
Date: Thursday, October 22, 2009	Sheet 17 of 42	

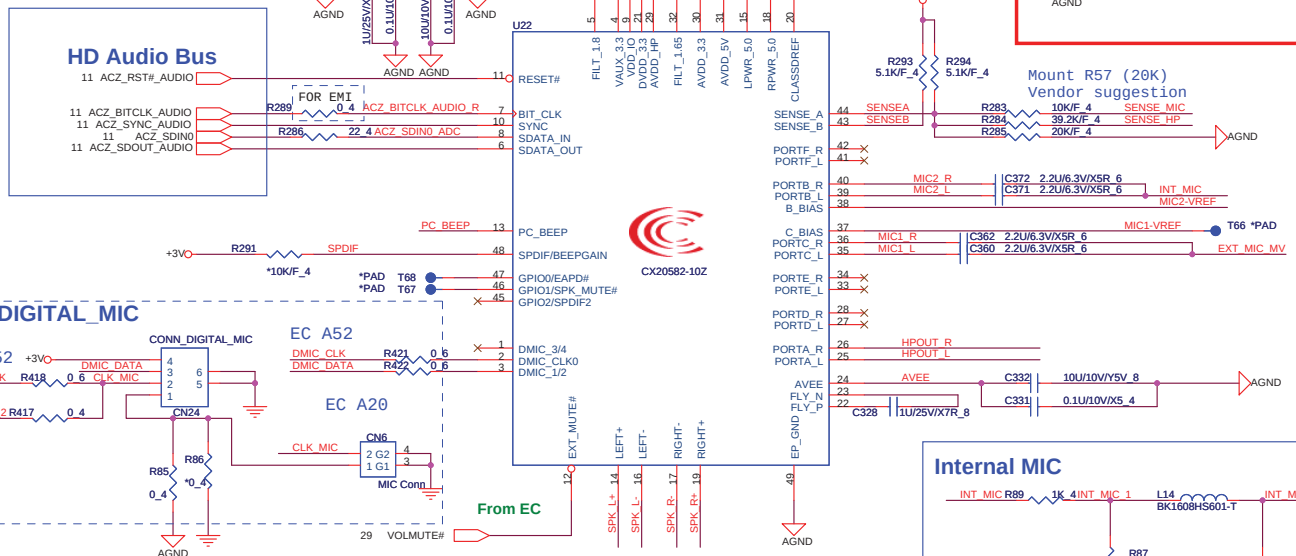
Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

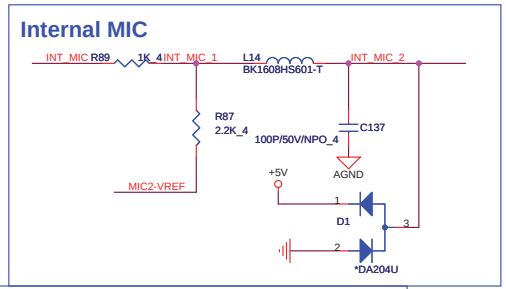


HD Audio Bus

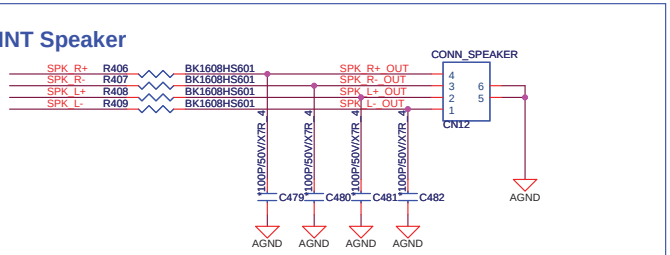


DIGITAL_MIC

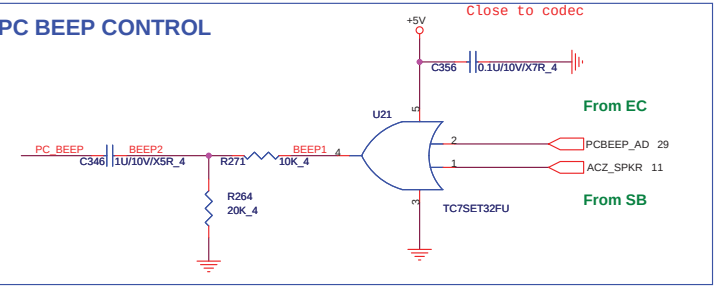
Internal MIC



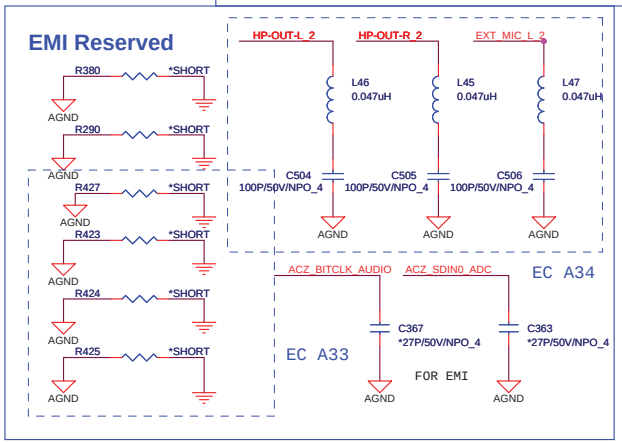
INT Speaker



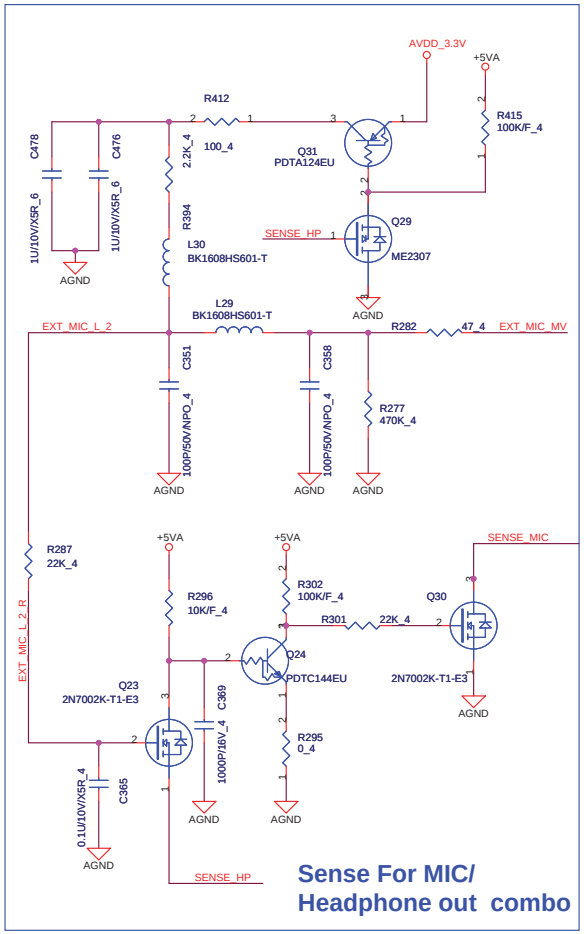
PC BEEP CONTROL



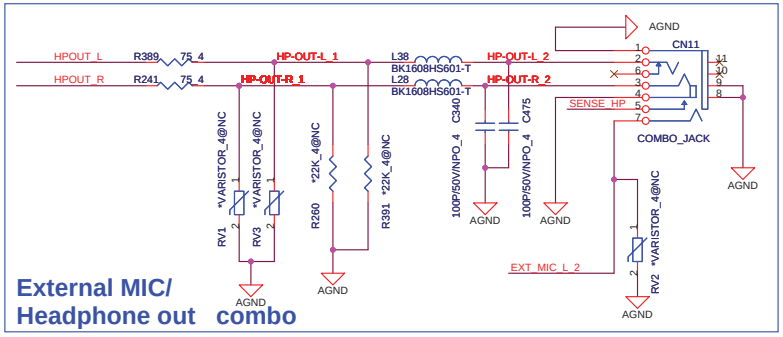
EMI Reserved



Sense For MIC/ Headphone out combo



External MIC/ Headphone out combo



Quanta Computer Inc.		
PROJECT : Congo		
Size	Document Number: AUDIO (CX20582, SPK)	Rev 1A
Date: Thursday, October 22, 2009	Sheet 18 of 42	

LANVCC

3VPCU

38 LAN_ON

Q16 AO6402

C289 0.1U/10V/X5R_4

LANVCC
Trace width>60mil,
Trace length<200mil

For RTL8102EL/8103EL, use this block.

DVDD12 — R122 *0_4@8103 CTRL12/VDD

For RTL8111DL, use this block

LANVCC — R126 0_4@8111 CTRL12/VDD

Y2 25MHZ

XTAL1 — C272 27P/50V/NPO_4

XTAL2 — C271 27P/50V/NPO_4

Tramsformer

U12 NS892405

MDI0-	12	TD4-	MX4-	13	LAN_MX0-
MDI0+	11	TD4+	MX4+	14	LAN_MX0+
	10	TCT4	MCT4	15	LAN_MCT0
MDI1-	9	TD3-	MX3-	16	LAN_MX1-
MDI1+	8	TD3+	MX3+	17	LAN_MX1+
	7	TCT3	MCT3	18	LAN_MCT1
MDI2-	6	TD2-	MX2-	19	LAN_MX2-
MDI2+	5	TD2+	MX2+	20	LAN_MX2+
	4	TCT2	MCT2	21	LAN_MCT2
MDI3-	3	TD1-	MX1-	22	LAN_MX3-
MDI3+	2	TD1+	MX1+	23	LAN_MX3+
	1	TCT1	MCT1	24	LAN_MCT3

C245 0.01U/16V/X7R_4 — R365 75/F_4 — LANCT3

C261 0.01U/16V/X7R_4 — R366 75/F_4

C290 0.01U/16V/X7R_4 — R368 75/F_4

C305 0.01U/16V/X7R_4 — R374 75/F_4

R135 1M_6 — C215 1000P/3KV/NPO_18

RJ45 Connector

U13 CM1293A-04SO: MDI0- / MDI1+ → MDI0+ / MDI1-

U14 CM1293A-04SO: MDI2- / MDI3+ → MDI2+ / MDI3-

EMI:NEAR CN5006 — C317 *0.1U/10V/X5R_4

LANVCC — R239 150_4 — LAN_OLED — LED1_LINK/EESK

CN9 RJ45: LAN_MX0+ / LAN_MX0- / LAN_MX1+ / LAN_MX2+ / LAN_MX2- / LAN_MX1- / LAN_MX3+ / LAN_MX3-

LANVCC — R240 150_4 — LAN_GLED / LED0_ACT

EMI:NEAR CN4 — C318 *0.1U/10V/X5R_4

RJ45 Connector

C70 is only for RTL8111DL.

Remove R56 and R58 for RTL8102EL/8103EL application.

R56 and R58 are used in the RTL8111DL application. Remove R58 if switching regulator is enabled. Remove R56 if external power 1.2V is used.

R158 is only required by RTL8102EL and RTL8103EL.

CTRL12/VDD LANVCC

C268 0.1U/10V/X5R_4 — C253 22U/6.3V/X5R_8@8111

R175 0_4@8111 — R174 *0_4@8103

R173 2.49K/F_4

DVDD12

LED0_ACT

LANVCC

Pin48
Trace width>60mil,
Trace length<200mil

U17 RTL8102EL/8103EL/8111DL

	1	AVDD33	DVDD12	36	LED1_LINK/EESK
MDI0+	2	MDIP0	LED1/EESK	35	LED2/EEDI
MDI0-	3	MDIN0	LED2/EEDI	34	LED3/EEDO
	4	NC/FB12	LED3/EEDO	33	EECS
MDI1+	5	MDIP1	EECS	32	GND
MDI1-	6	MDIN1	GND	31	DVDD12
	7	GND	DVDD12	30	VDD33
MDI2+	8	NC/MDIP2	VDD33	29	LANVCC
MDI2-	9	NC/MDIN2	ISOLATEB	28	ISOLATEB
	10	DVDD12/AVDD12	PERSTB	27	LAN_REST#
MDI3+	11	NC/MDIP3	LANWAKEB	26	
MDI3-	12	NC/MDIN3	CLKREQB	25	

WAKE# 23,29 — PCIE_REQ_LAN# 2

R156 *10K_4@8103 — GND

U10 *AT93C46A(3.3V): EECS / LED1_LINK/EESK / LED2/EEDI / LED3/EEDO — CS SK DI DO VCC DC ORG GND

C247 *0.1U/10V/X5R_4

DVDD12 — R125 3.6K_6 — LANVCC

+3V — R404 1K_4 — R405 15K_4 — D23 RB500V-40 — LAN_ISOLATEB 29

LAN_REST# — R247 0_4 — PLT_RST# 10,25

DVDD12 — EVDD12

ENERGY_DET 29

PCIE_TXP1 7 / PCIE_TXN1 7

PCIE_RXN1_C C345 0.1U/10V/X5R_4 — PCIE_RXN1 7

PCIE_RXP1_C C344 0.1U/10V/X5R_4 — PCIE_RXP1 7

CLK_PCIE_LANN 2

CLK_PCIE_LANP 2

Pin 23 is GPO pin for 8111DL. It is used for DSM function.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

CTRL12A — L25 4.7uH — CTRL12A_R

C265 22U/6.3V/X5R_8 — C291 0.1U/10V/X5R_4

Change L1 to 0 ohm in RTL8102EL/8103EL application.

C5 is only for RTL8111DL.

R276 0_8 — EVDD12

* C6 and C7 are for for U2 EVDD12 pin 19.

C343 1U/6.3V/X5R_4 — C348 1U/6.3V/X5R_4 — GND

Remove R1 & R2 in RTL8102EL/8103EL application.

R213 0_8

* C9 to C13 are for 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.

* C9 to C12 are for 8102EL/8103EL DVDD12 pins-- 10, 13, 30, 36.

DVDD12

C297 0.1U/10V/X5R_4 — C335 0.1U/10V/X5R_4 — C316 0.1U/10V/X5R_4 — C323 0.1U/10V/X5R_4 — C327 0.1U/10V/X5R_4

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Size	Document Number: LAN(RTL8103EL/8111DL)	Rev: 1A
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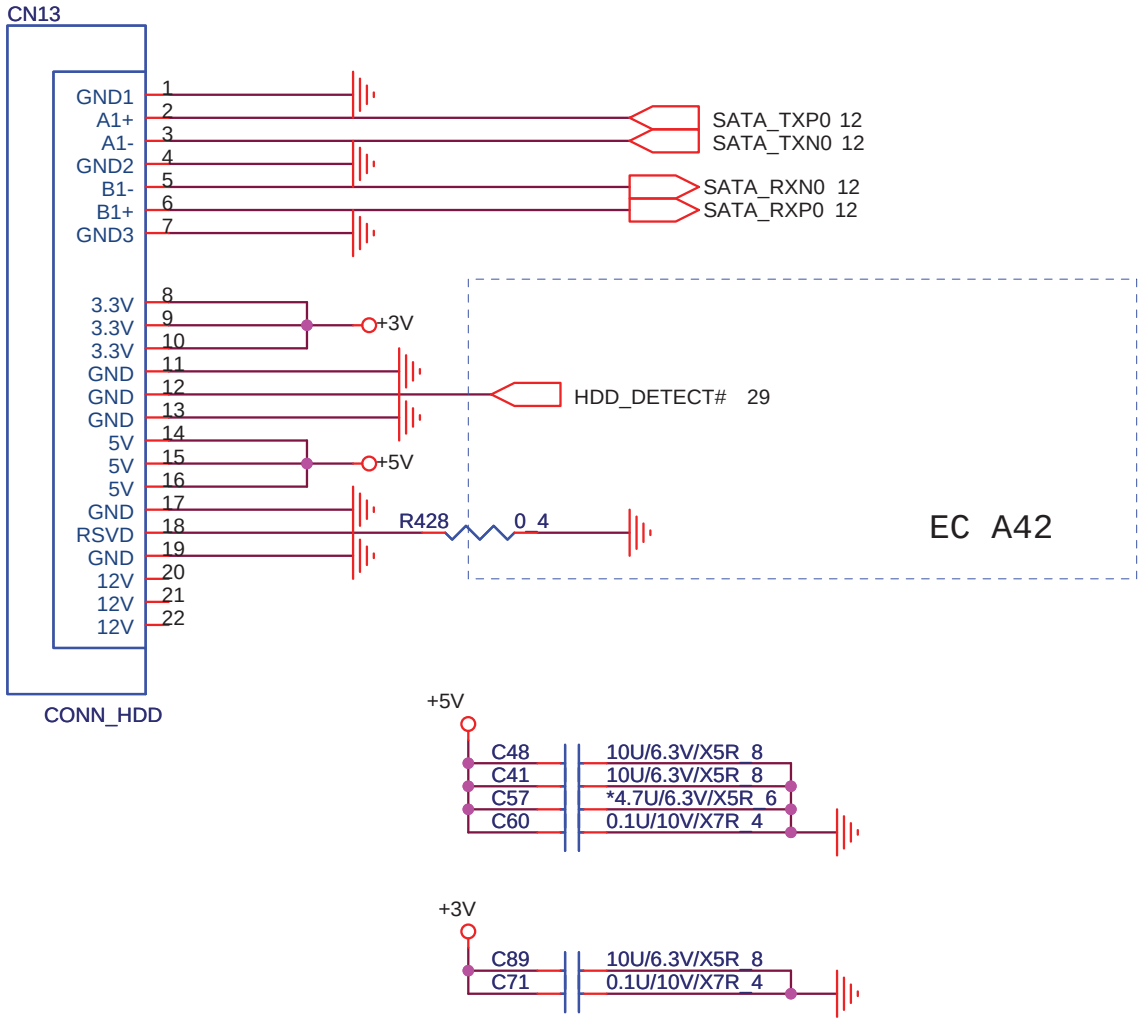
HDD

DC Current rating: 0.5 A



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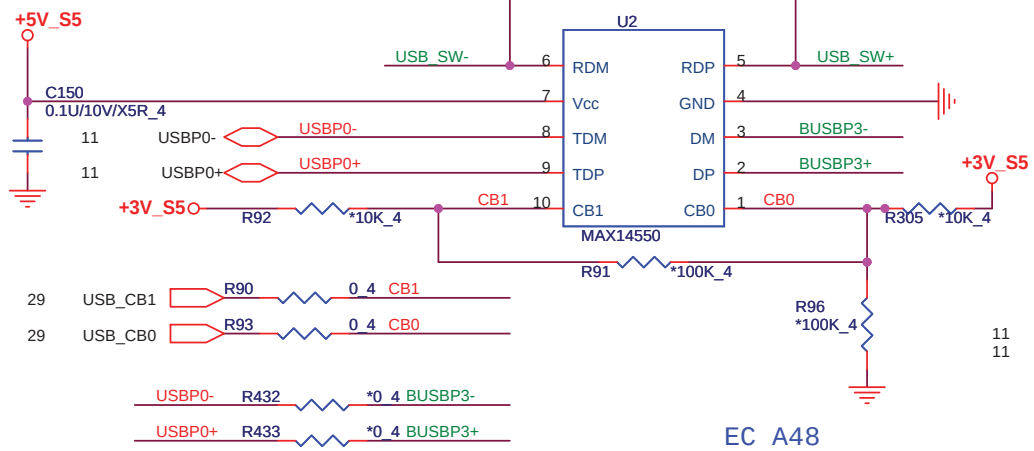
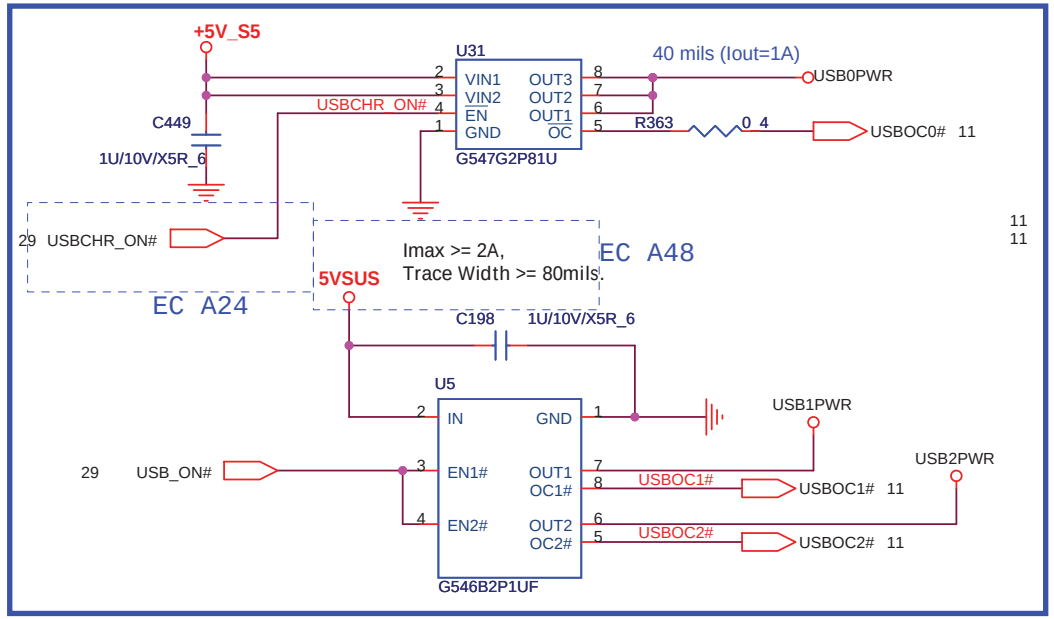
USB SLEEP CHARGE (NEW)

CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int.R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

If mount R97, R95, R94. R102 should mount 49K

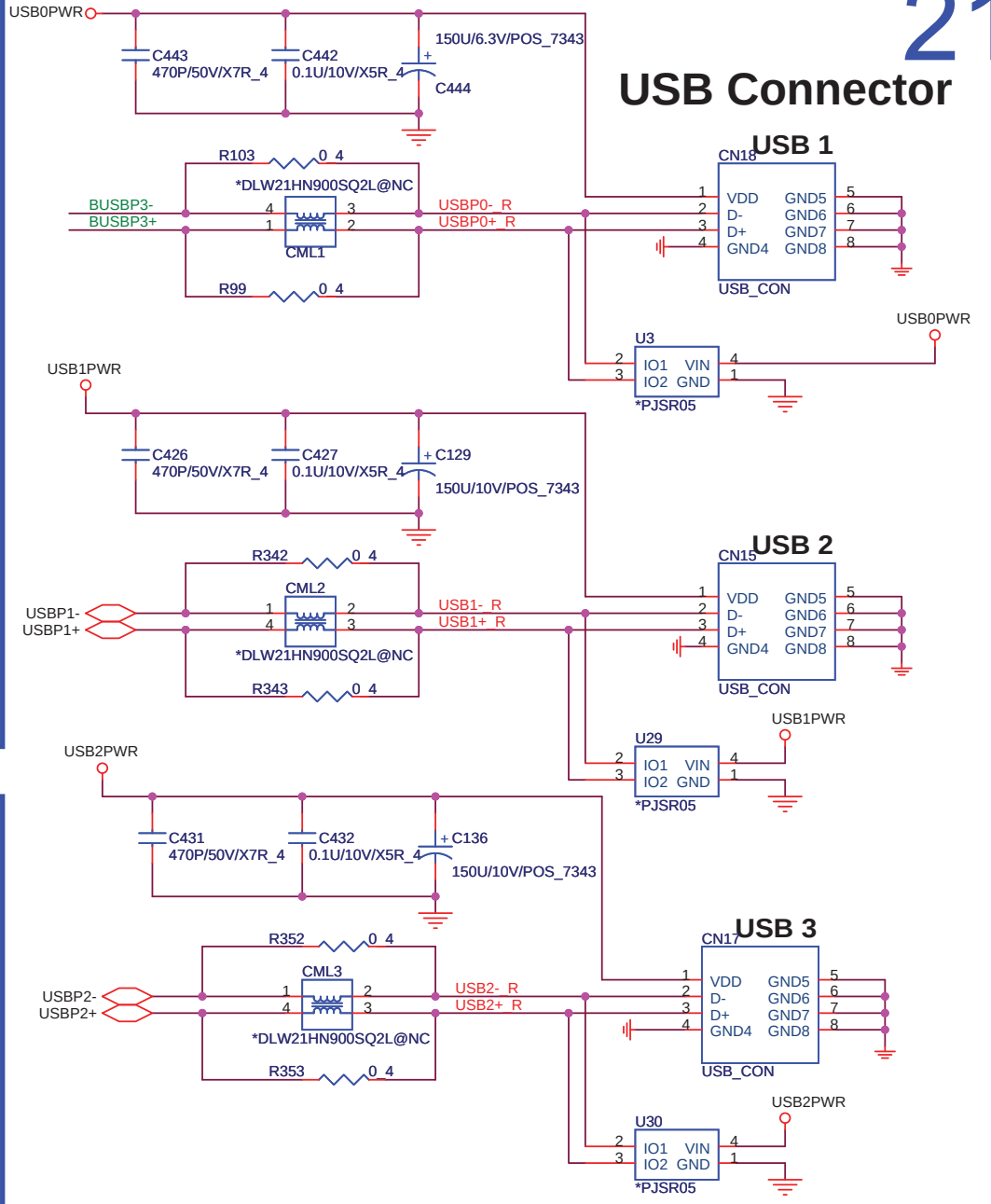
Sleep charger notice





21

USB Connector



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RTL5159

EC A57

For external 48Mhz clock input
pin13 pull high
For external 12Mhz clock input
pin13 floating

0515 EMI Changes

Note:

	SD/MMC	MS
SP0		
SP1		
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	
SP5		MS_BS
SP6		MS_D1
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9		MS_INS#
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	
SP13	SD_DAT4	
SP14		
SP15	SD_DAT3	
SP16	SD_DAT2	
SP17		
SP18		
SP19		

Card Reader Model Select

Pin 45	R273
RTS5159-GR	0 ohm (default)
RTS5158-GR	N.C

vendor suggestion:
Reserve a damping resistor for preventing noise occurred
Mika 2008/04/21

Realtek_RTS5159-GR

3 IN 1 CARD READER

3IN1_DFHD21MR012

EC A19

0505 EMI added

Add 10K to GND for +3VCARD discharge

CLOSE TO CONN

FOR EMI

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PROJECT : Congo	
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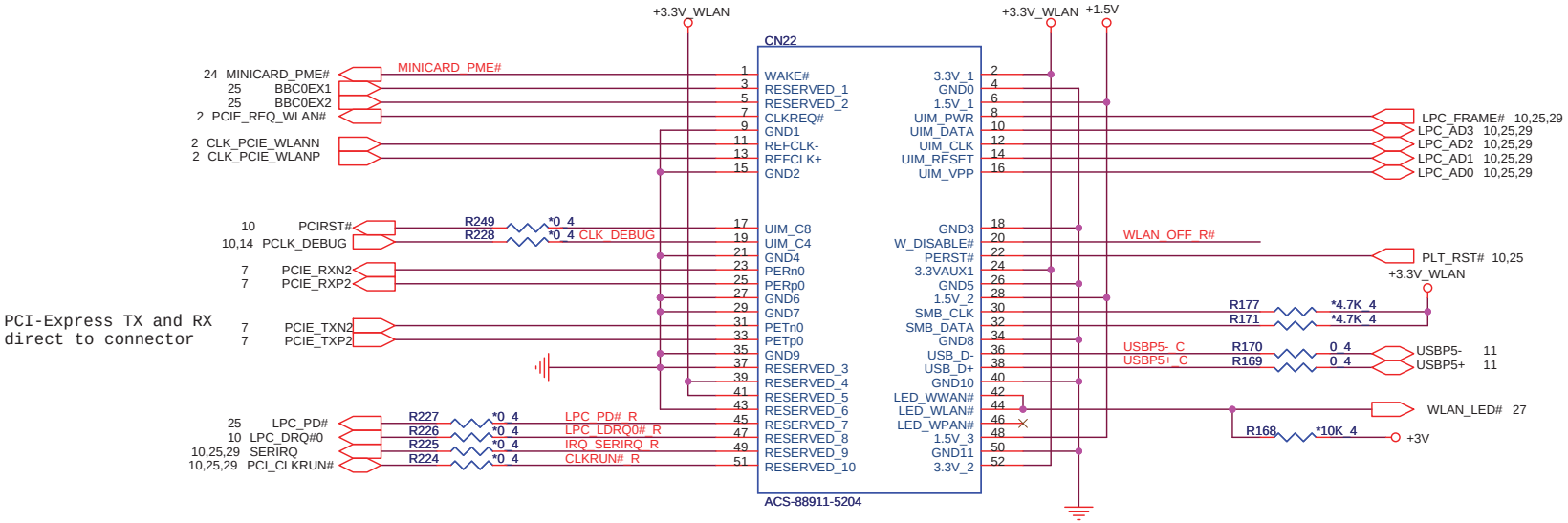
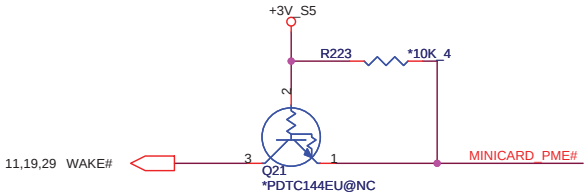
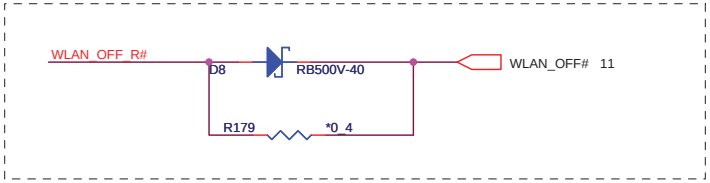
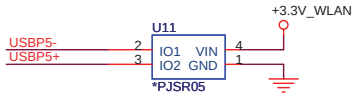
MiniCard WLAN connector

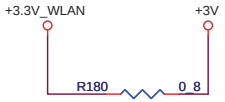


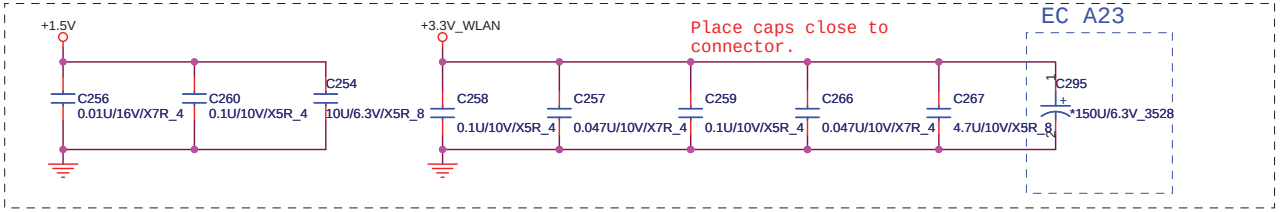
PCI-Express TX and RX direct to connector











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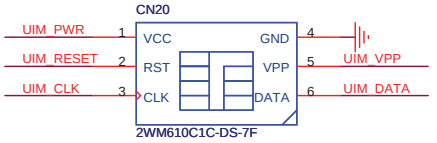
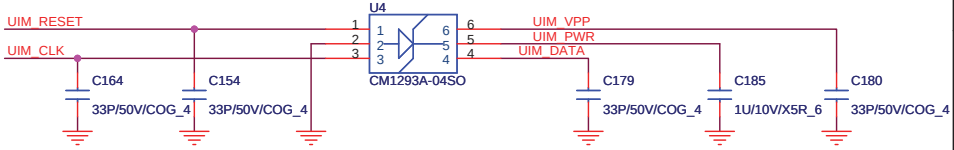
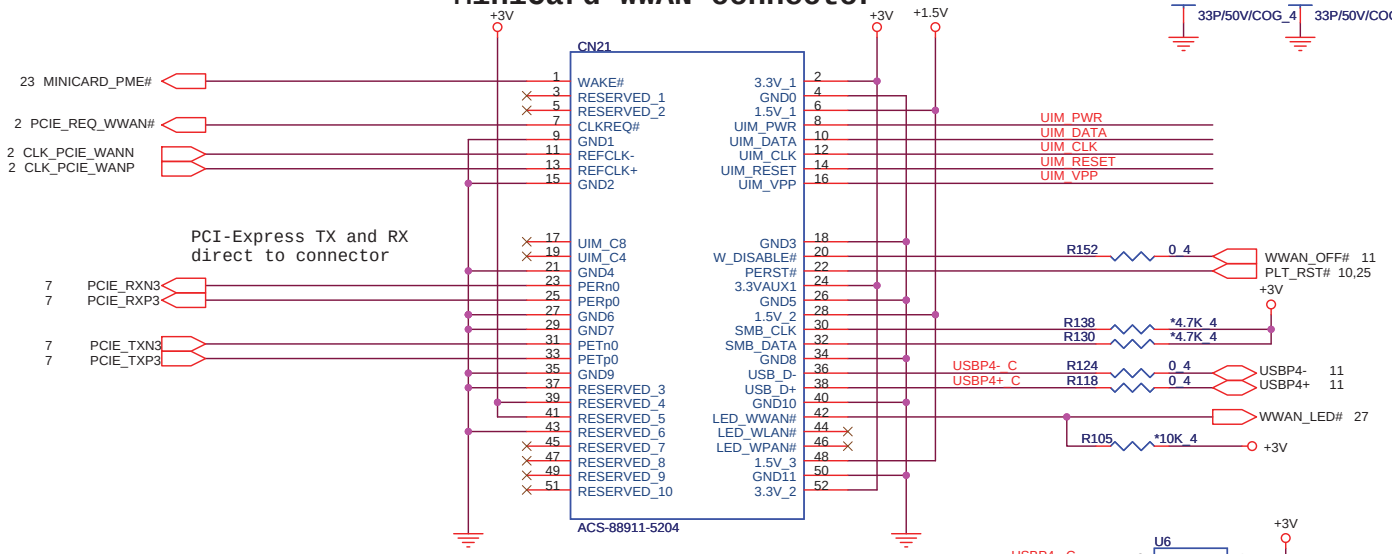
SIM Card CONN

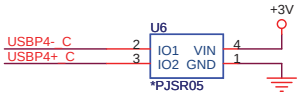


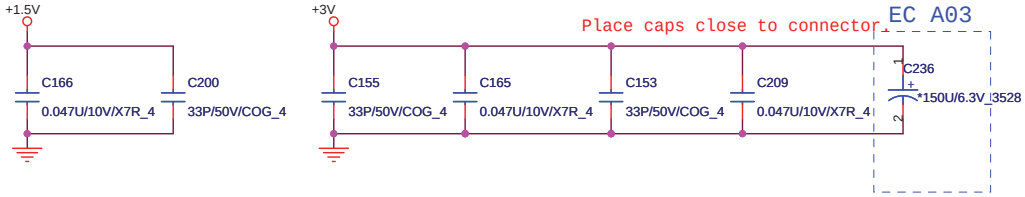
Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible



MiniCard WWAN connector







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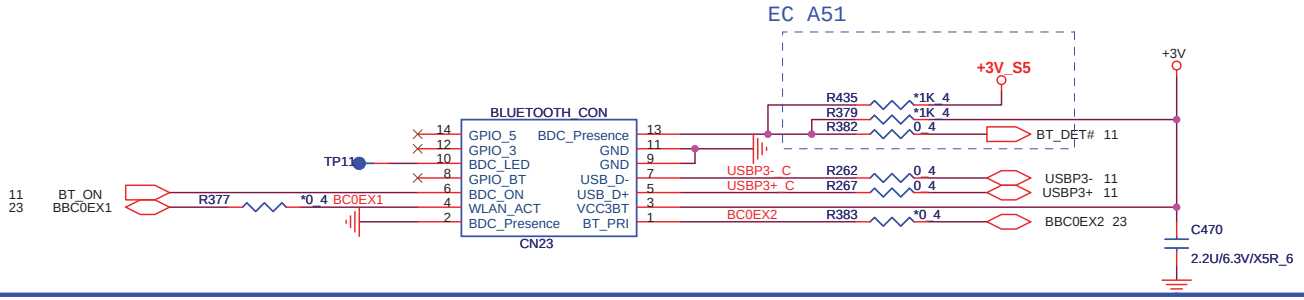
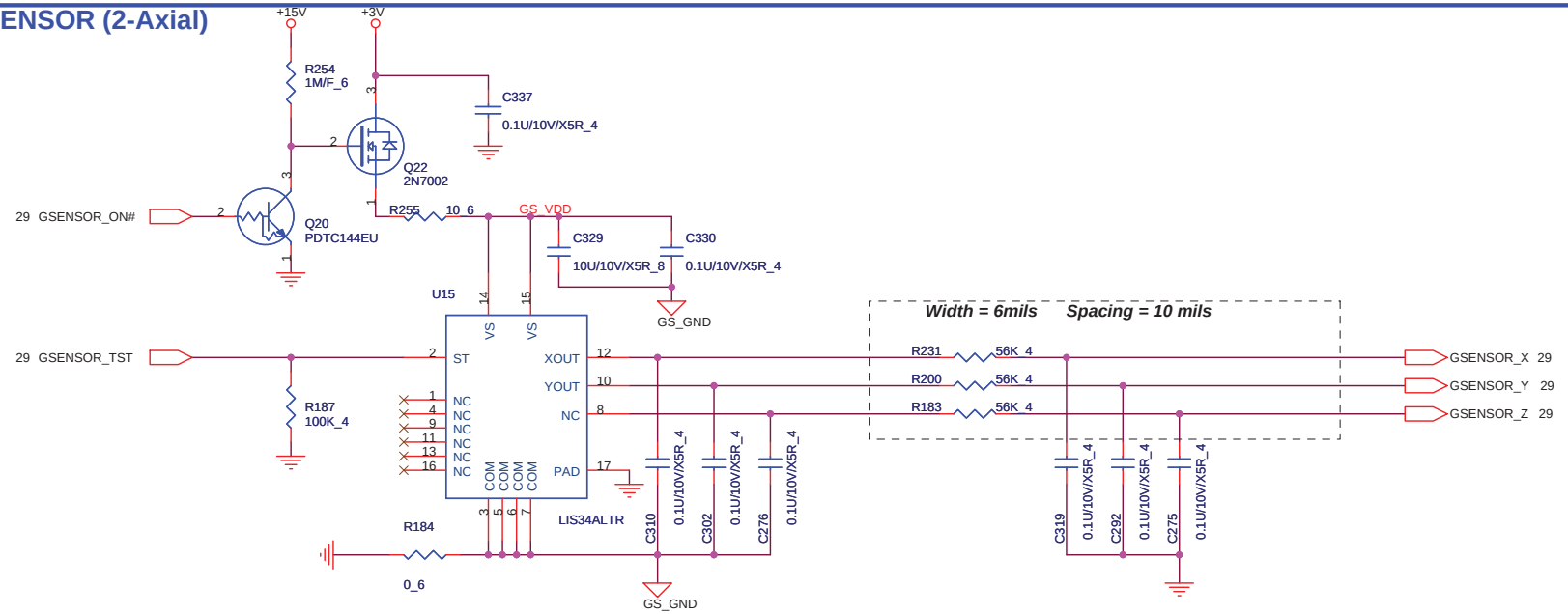
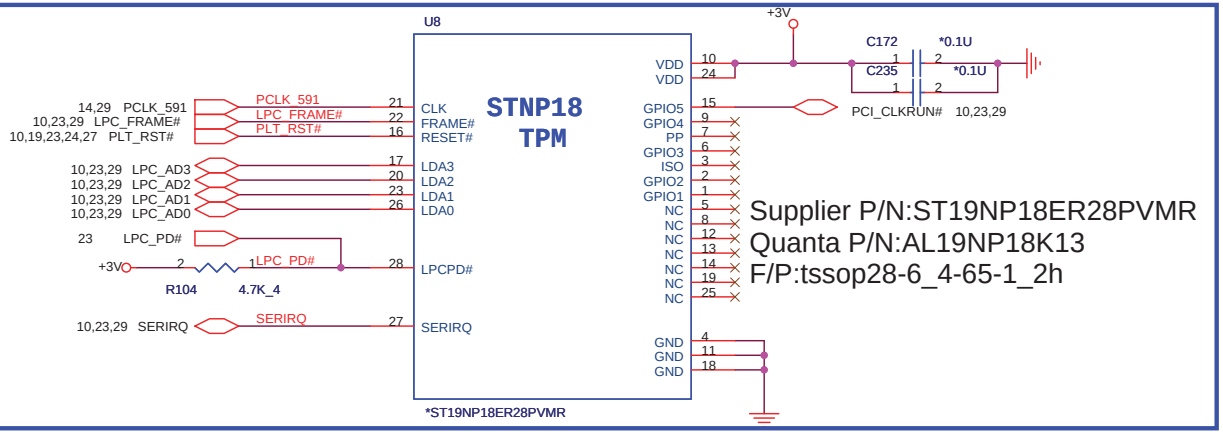
BLUETOOTH



G-SENSOR (2-Axial)



Discrete TPM



Quanta Computer Inc.
PROJECT : Congo

Size	Document Number	Rev
	BT/G-SENSOR/TPM	1A

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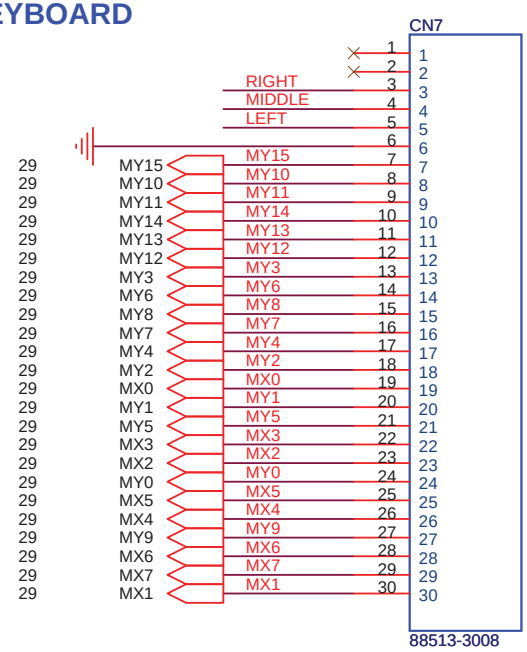
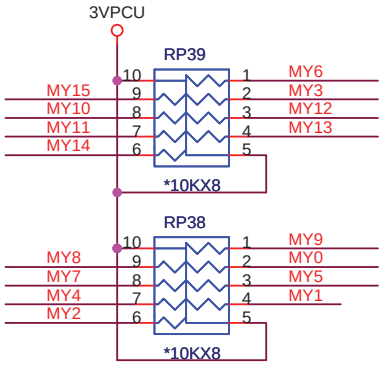
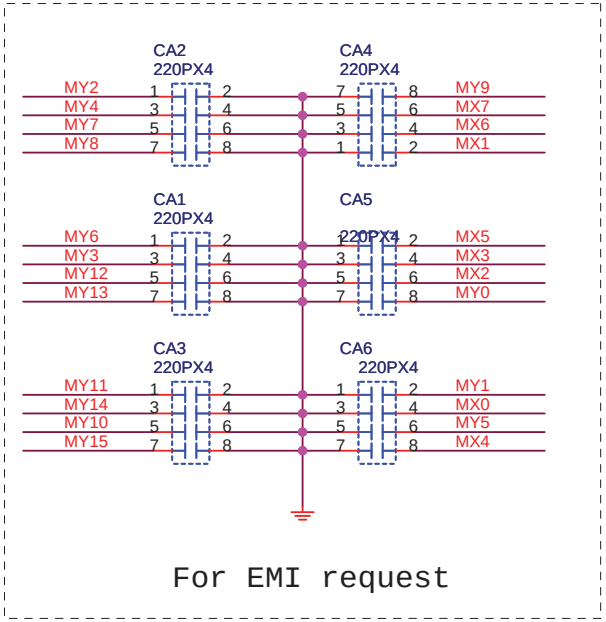
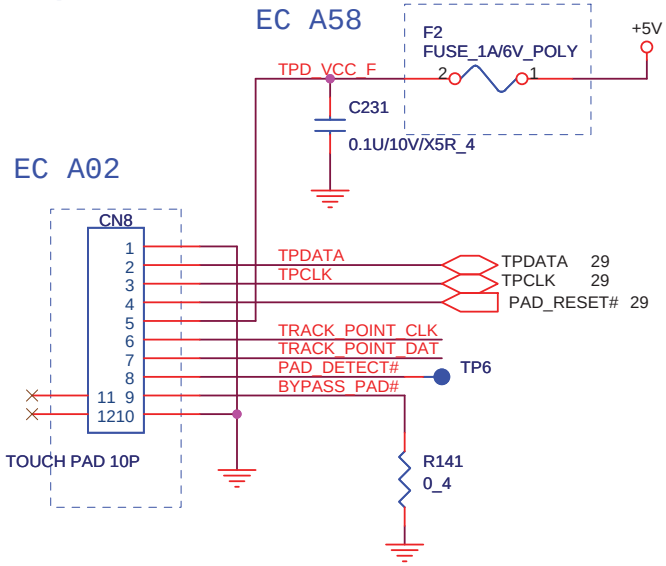
KEYBOARD

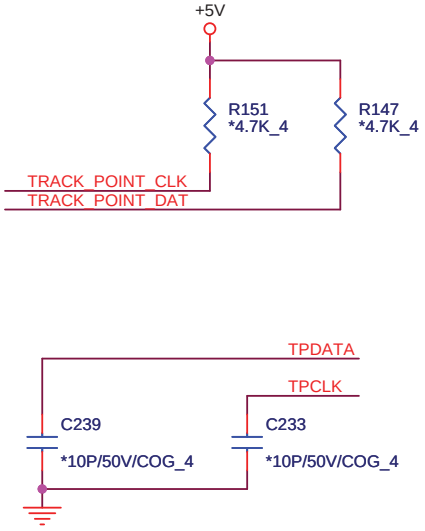




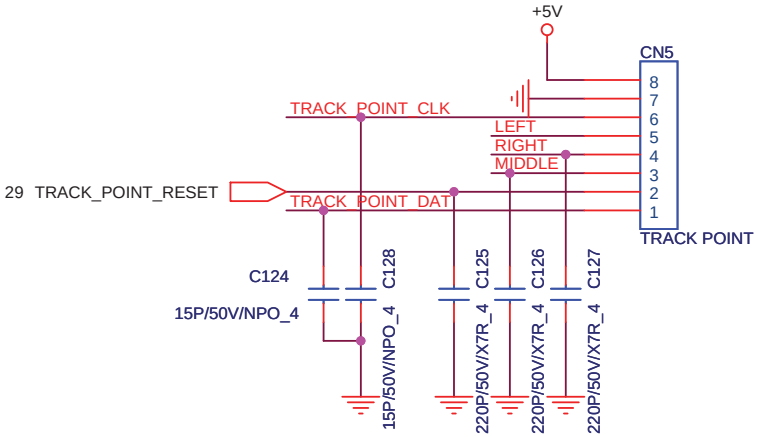


Touch pad





TRACK POINT



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PROJECT : Congo		
Size	Document Number: KB/TP	Rev: 1A
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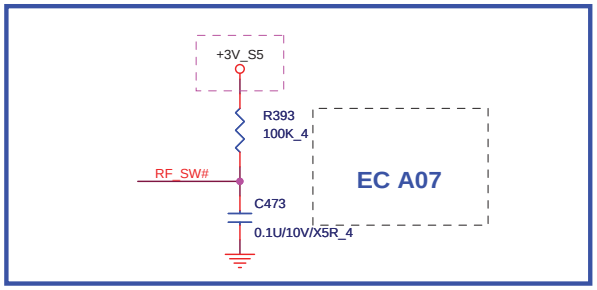

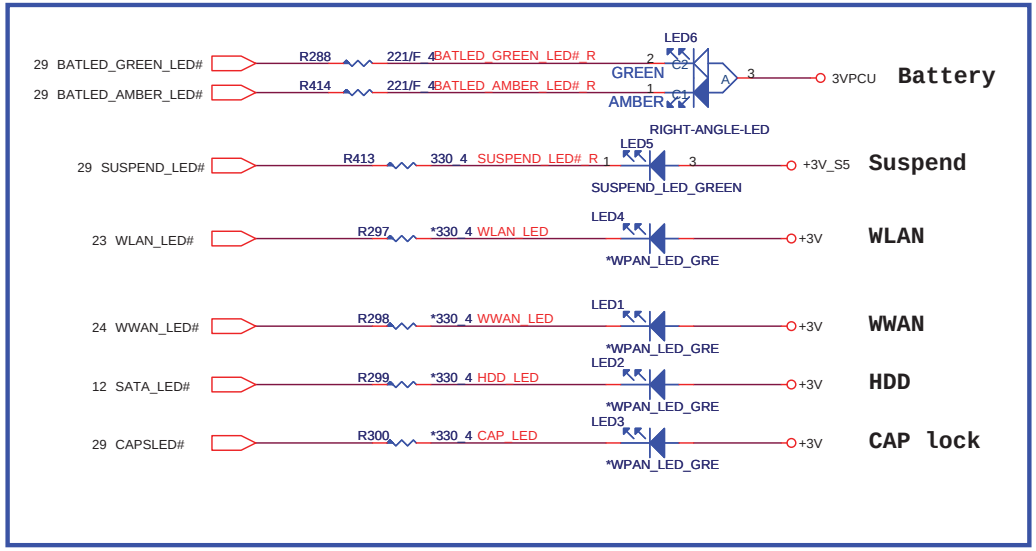

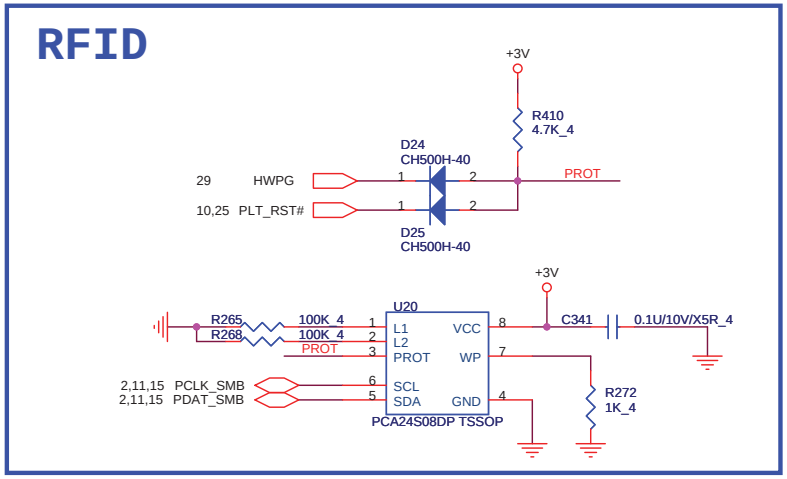

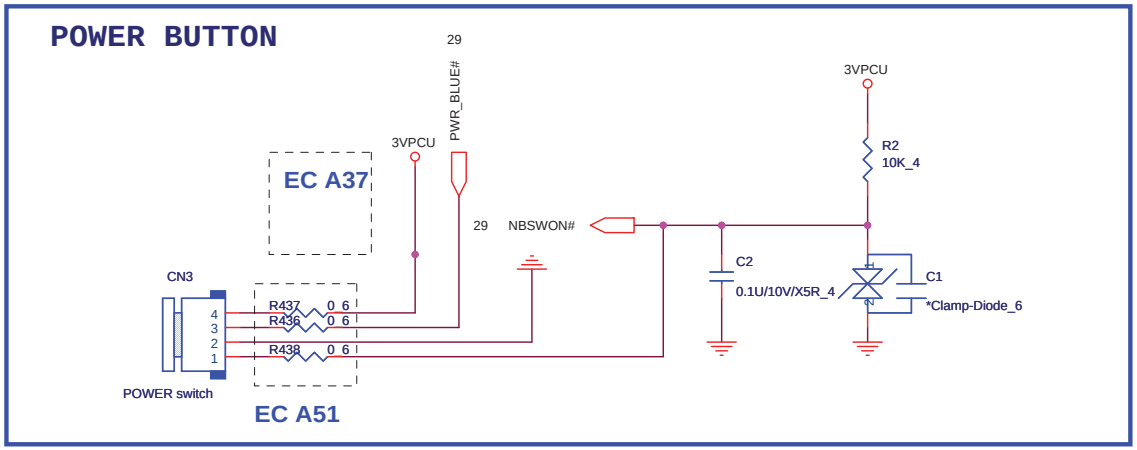

Quanta Computer Inc.		
PROJECT : Congo		
Size	Document Number: SW/LED/RFID_EEPROM	Rev: 1A
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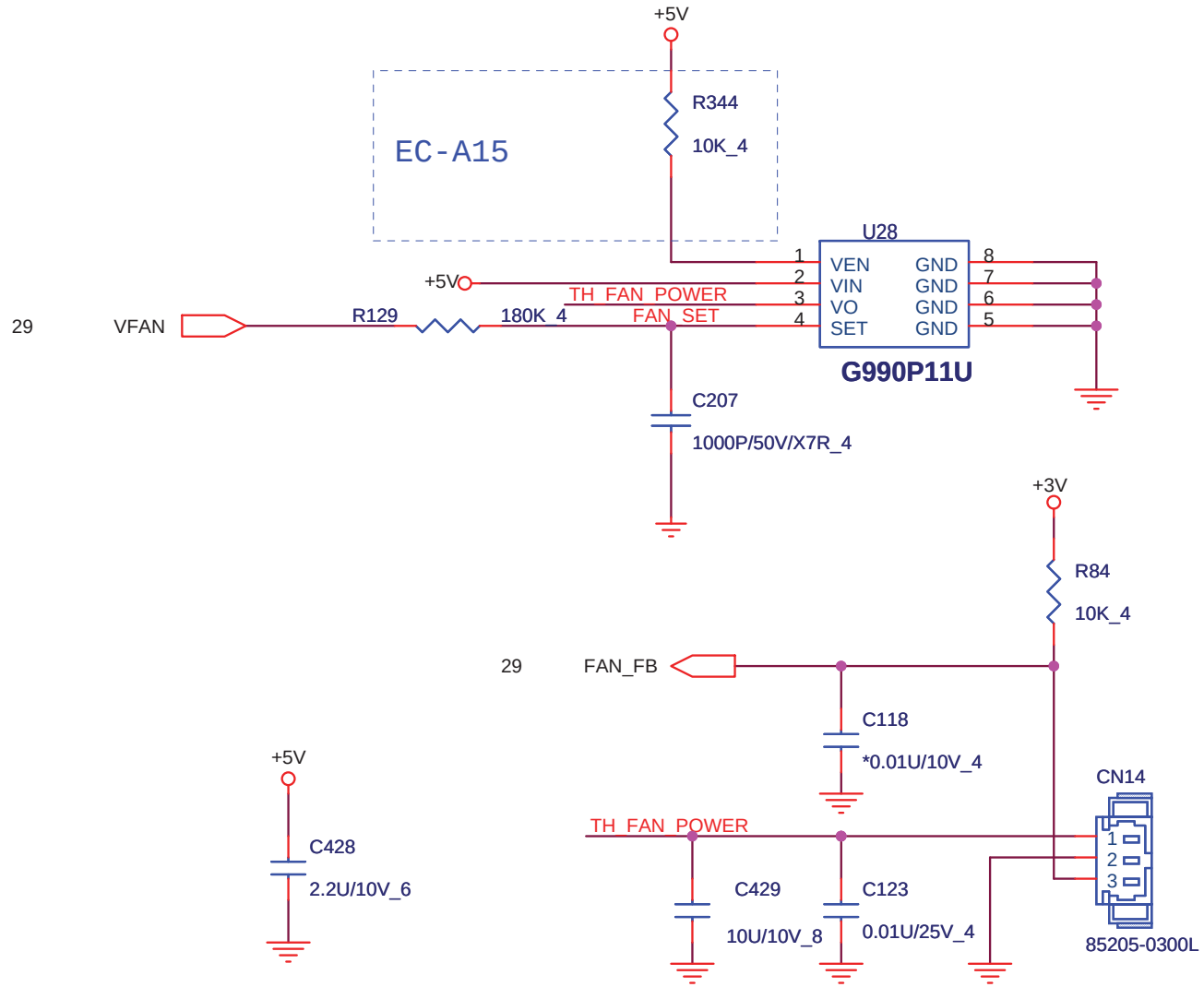
CPU FAN

FANPWR = 1.6*VSET



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PROJECT : Congo		
Size	Document Number: FAN/Thermal	Rev: 1A
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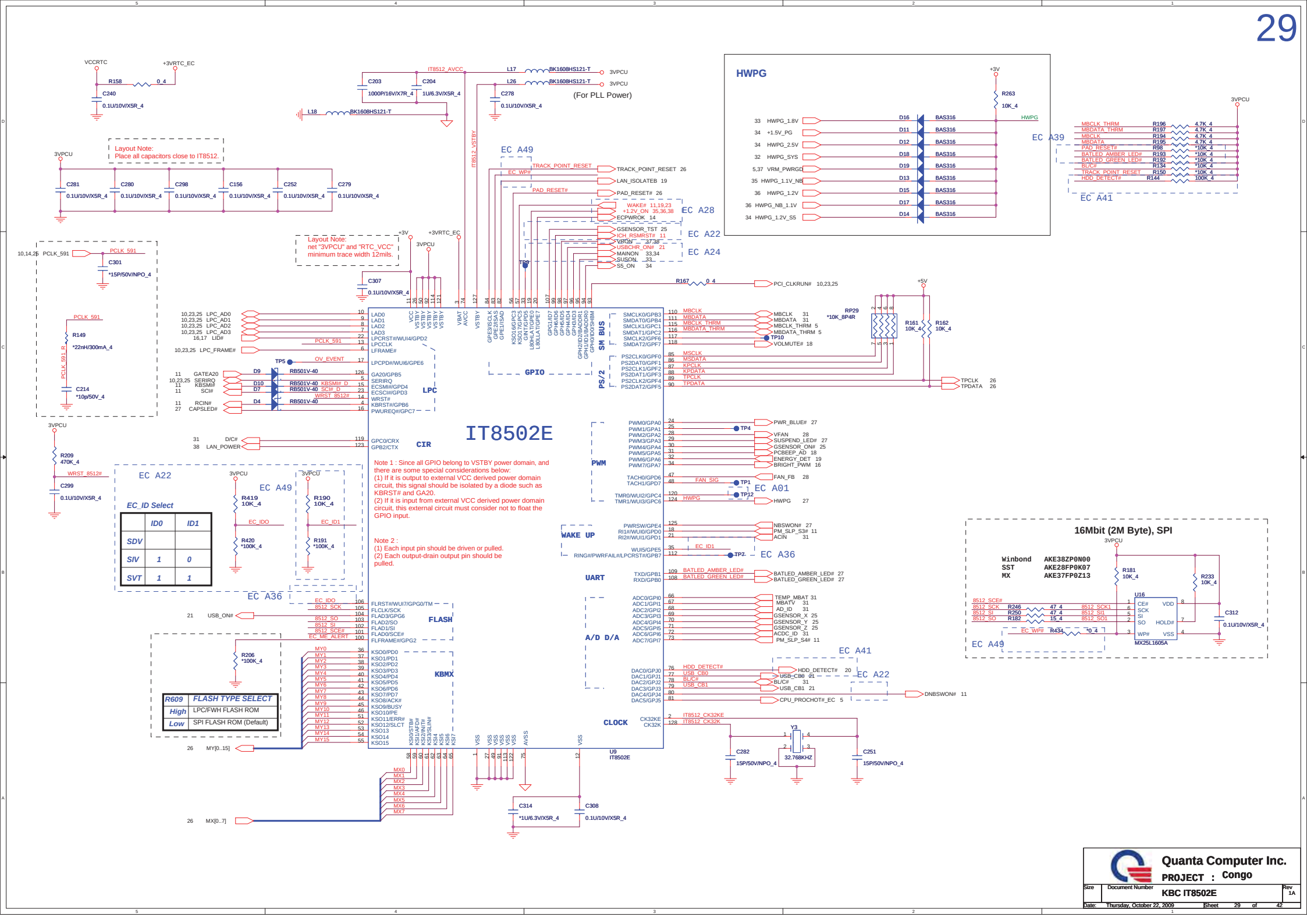
IT8502E
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
(For PLL Power)
HWPG
EC_ID Select
ID0 ID1
SDV
SIV 1 0
SVT 1 1
R609 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
16Mbit (2M Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
MX25L1605A
Quanta Computer Inc.
PROJECT : Congo
KBC IT8502E
Size
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Rev 1A
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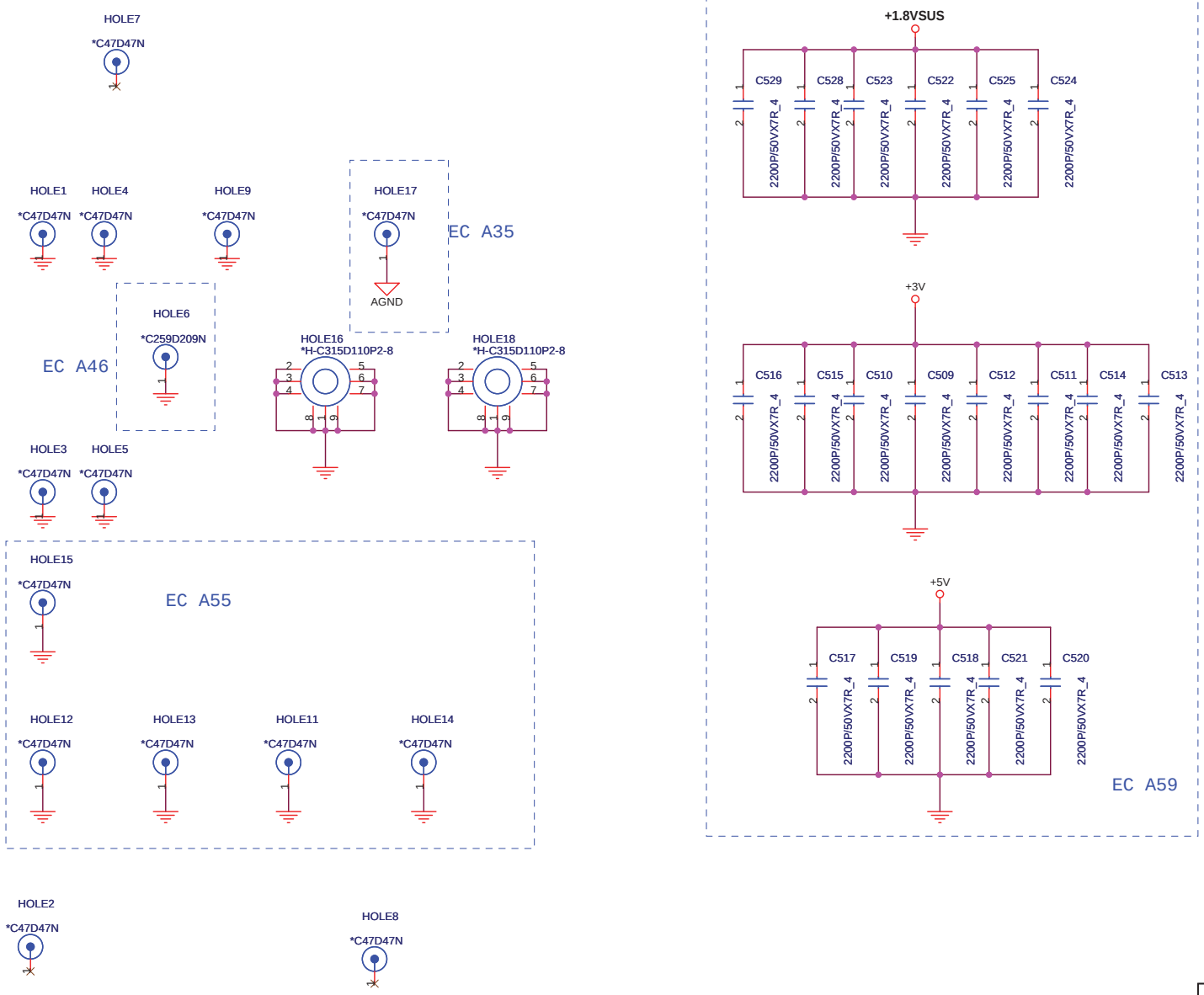

Quanta Computer Inc.		
PROJECT : Congo		
Size	Document Number	Rev
	Screw Hole/EMI	1A
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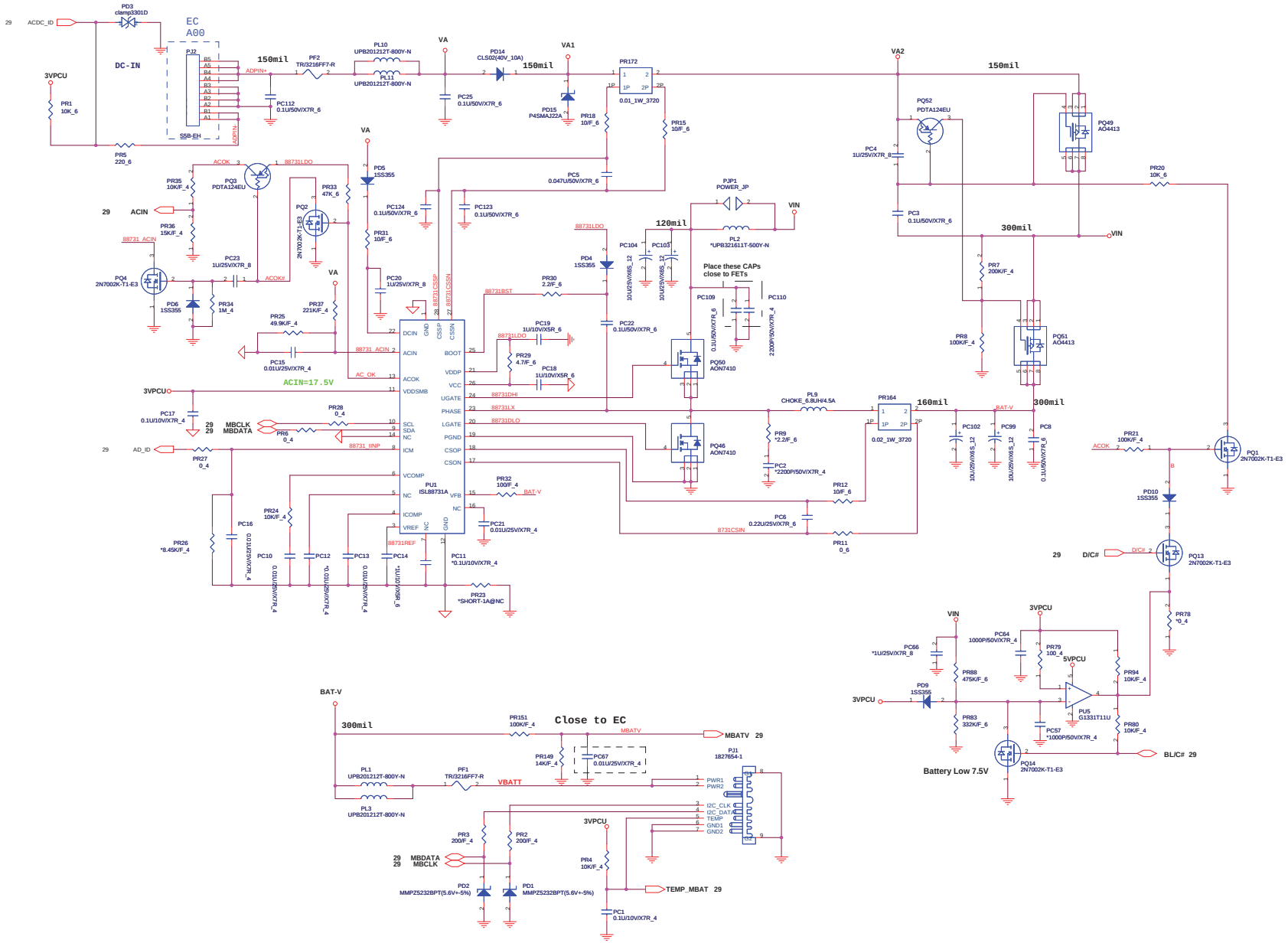
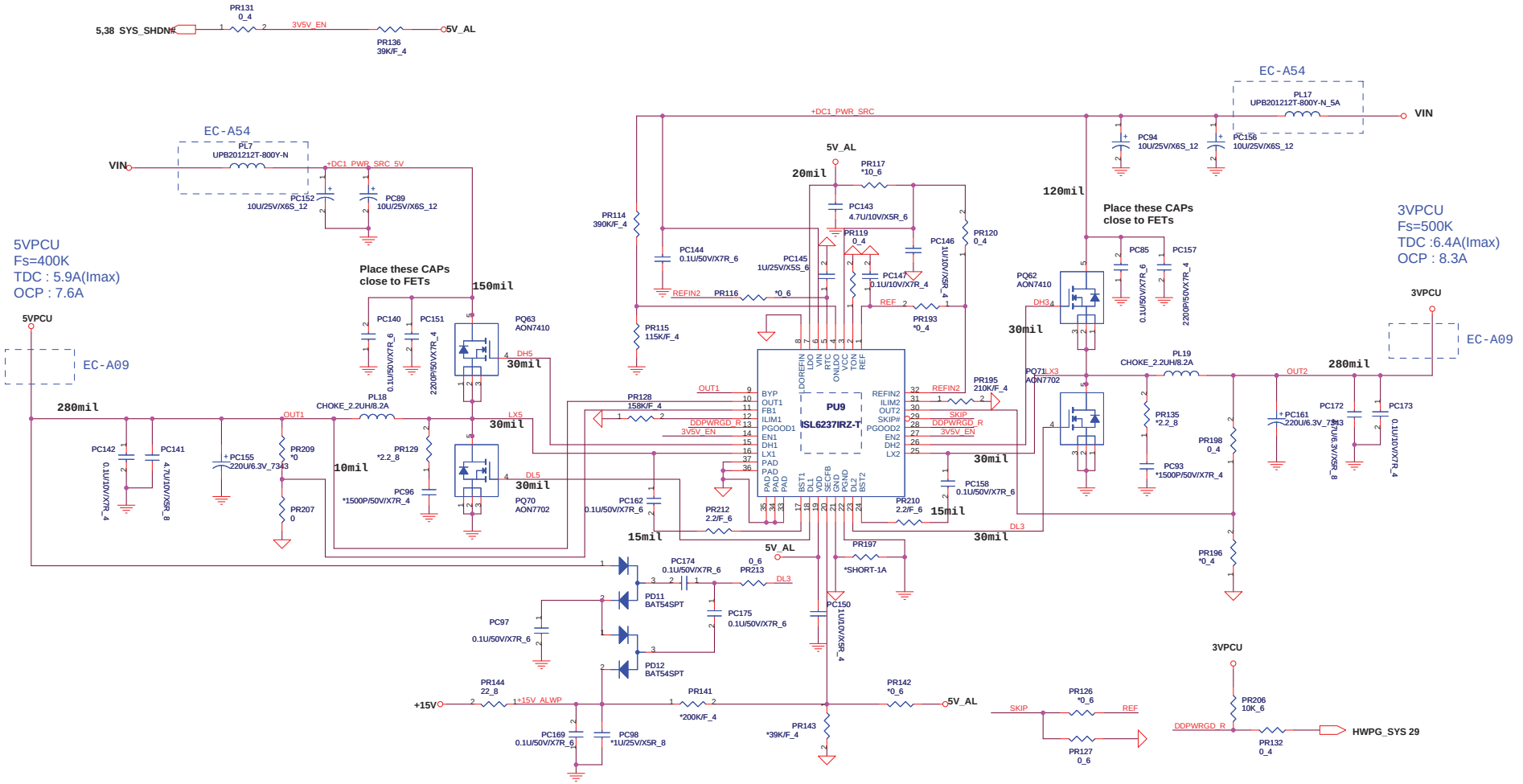

DC-IN
3VPCU
ACDC_ID
EC
A00
150mil
VA
VA1
VA2
120mil
300mil
160mil
ACIN=17.5V
Close to EC
Battery Low 7.5V
Place these CAPs close to FETs
MBATV 29
TEMP_MBAT 29
BL/C# 29
D/C# 29
MBCLK 29
MBDATA 29
ACIN 29
AD_ID 29
VIN
BAT-V
VBATT
5VPCU
ISL88731A
SSB-EH
CHOKE_6.8UH/4.5A



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PROJECT : Congo		
Size	Document Number: 3V/5V (ISL6237)	Rev: 1A
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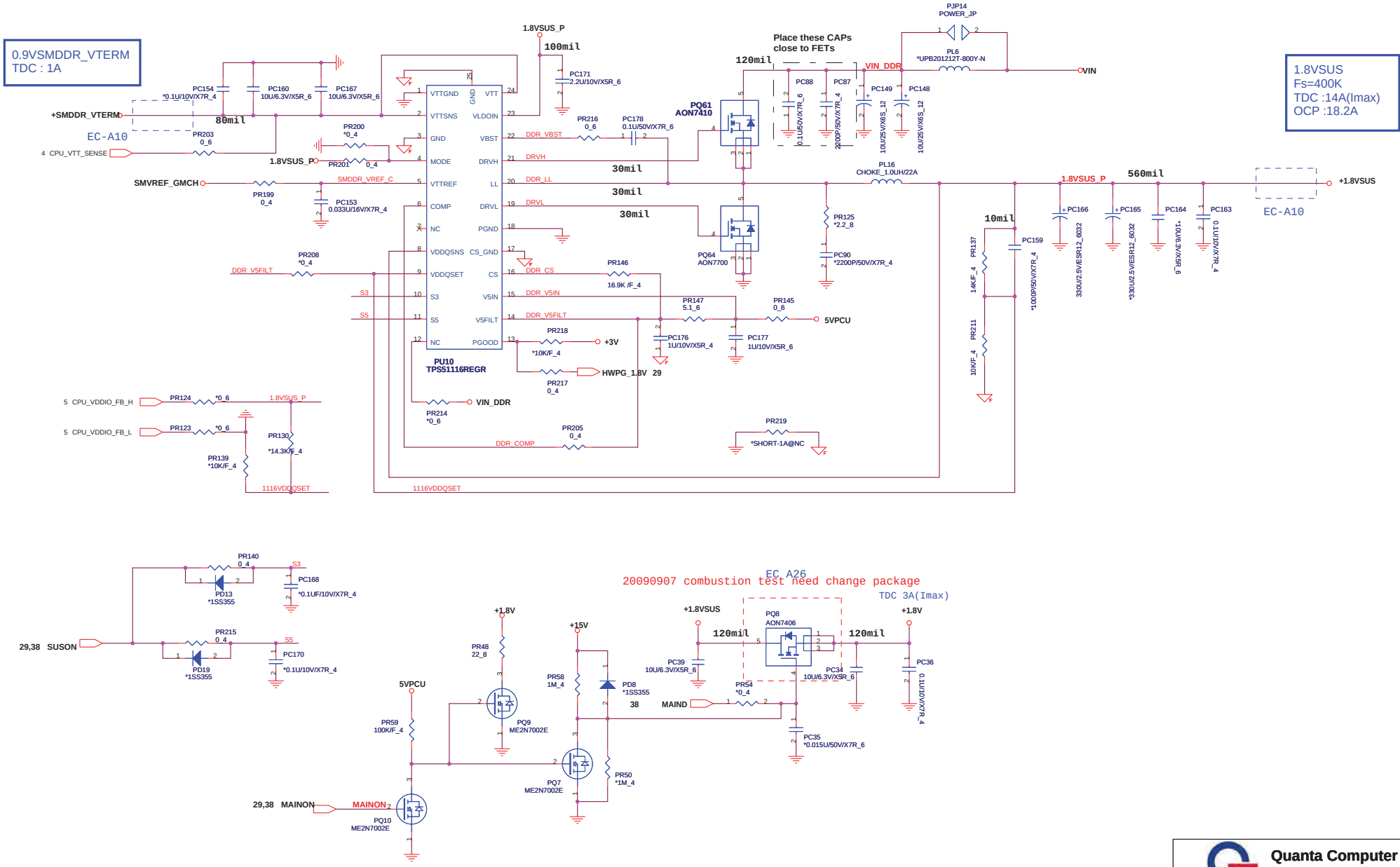

Quanta Computer Inc.			
PROJECT : Congo			
Size	Document Number		Rev
	DDR 1.8V(TPS51116)		1A
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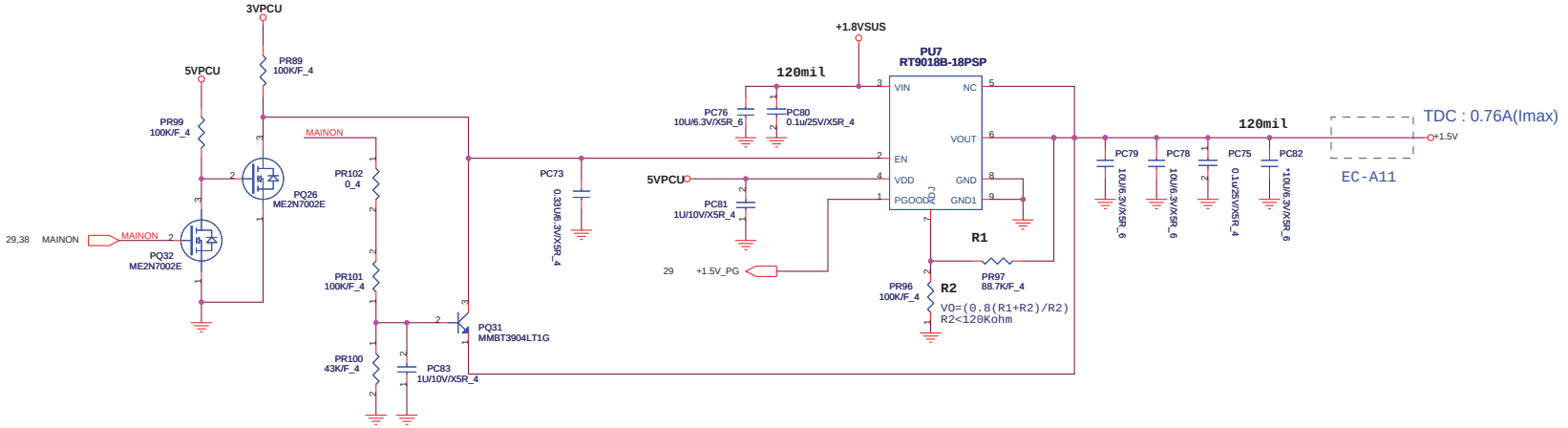

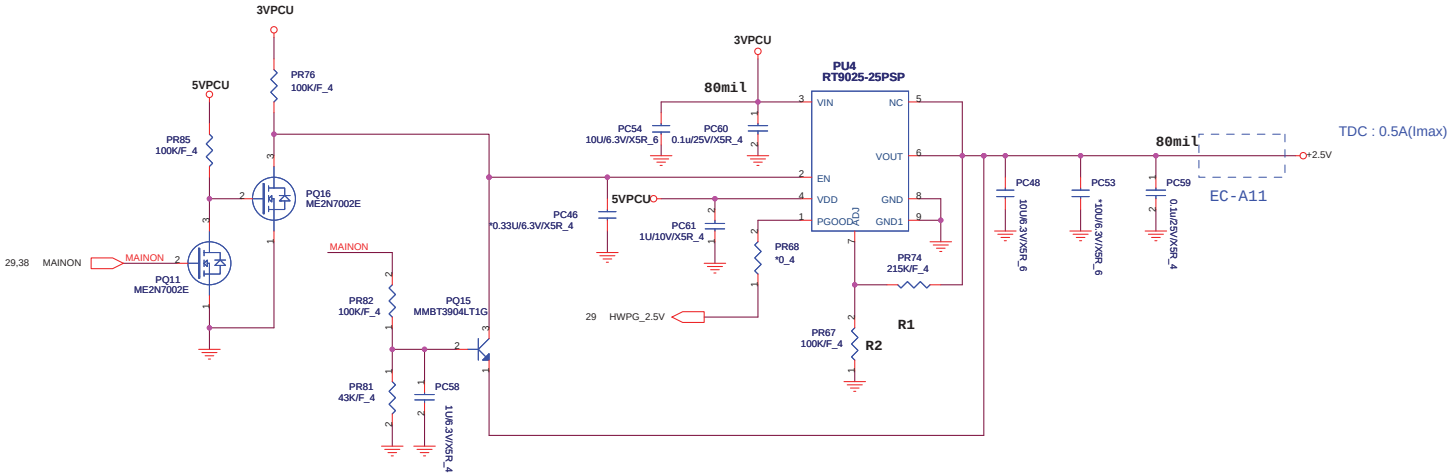

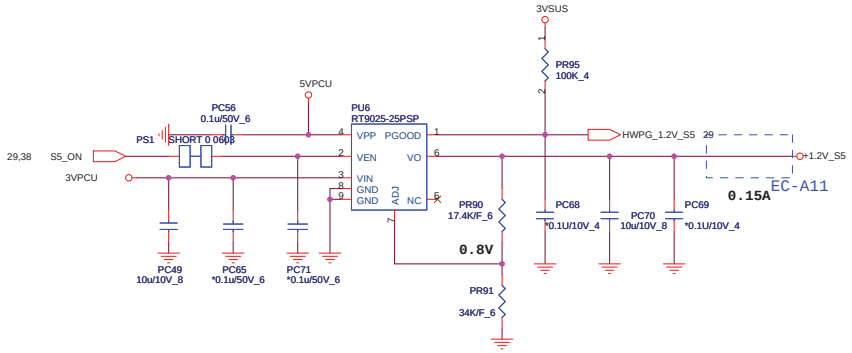

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PROJECT : Congo

Size	Document Number	Rev
	VCC1.5 / VCC2.5 (RT9025)	1A

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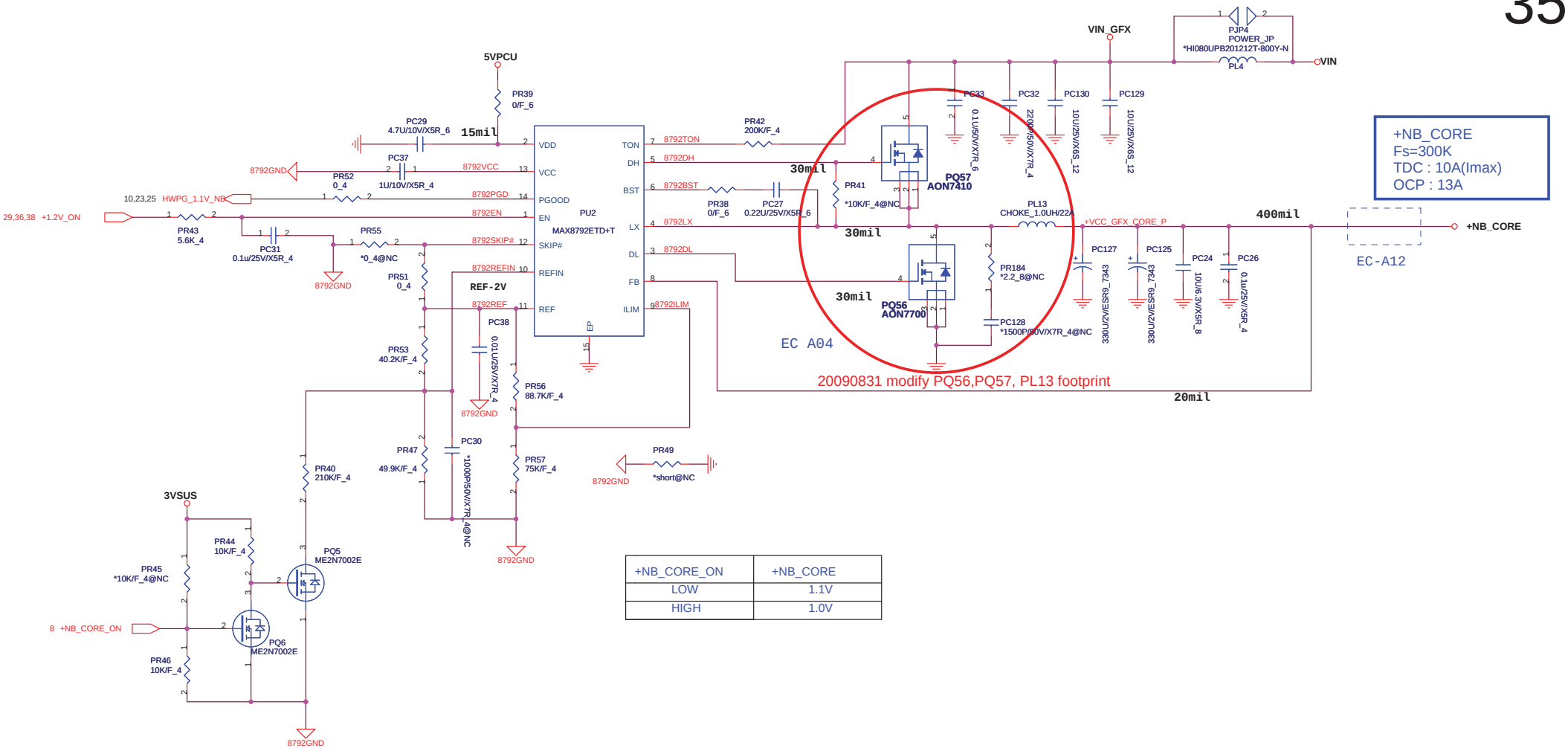

+NB_CORE_ON	+NB_CORE
LOW	1.1V
HIGH	1.0V

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PROJECT : Congo

Size	Document Number	Rev
	+NB_CORE (MAX8792)	1A
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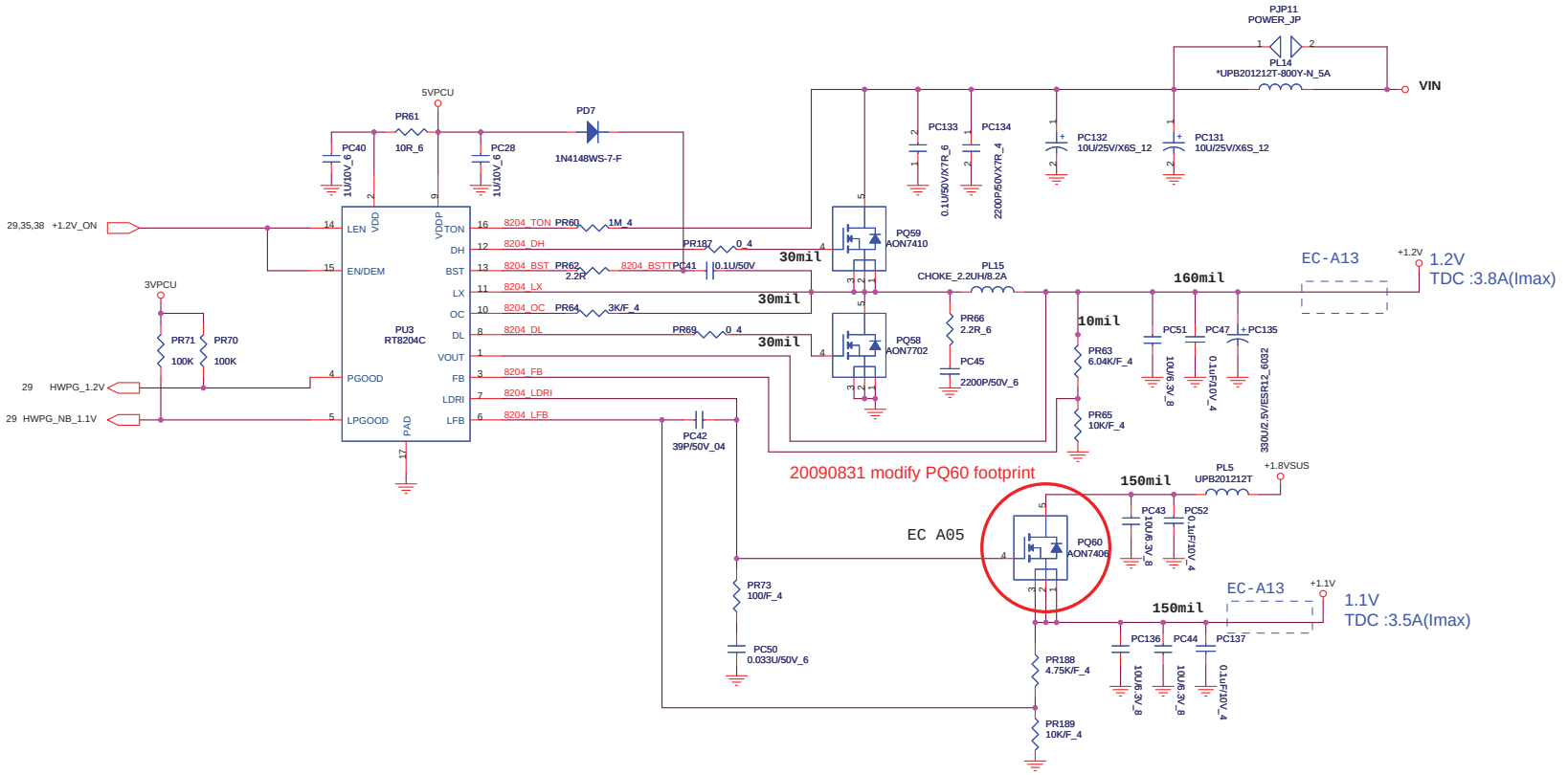

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PROJECT : Congo		
Size	Document Number: 1.2V/1.1V (RT8204)	Rev: 1A
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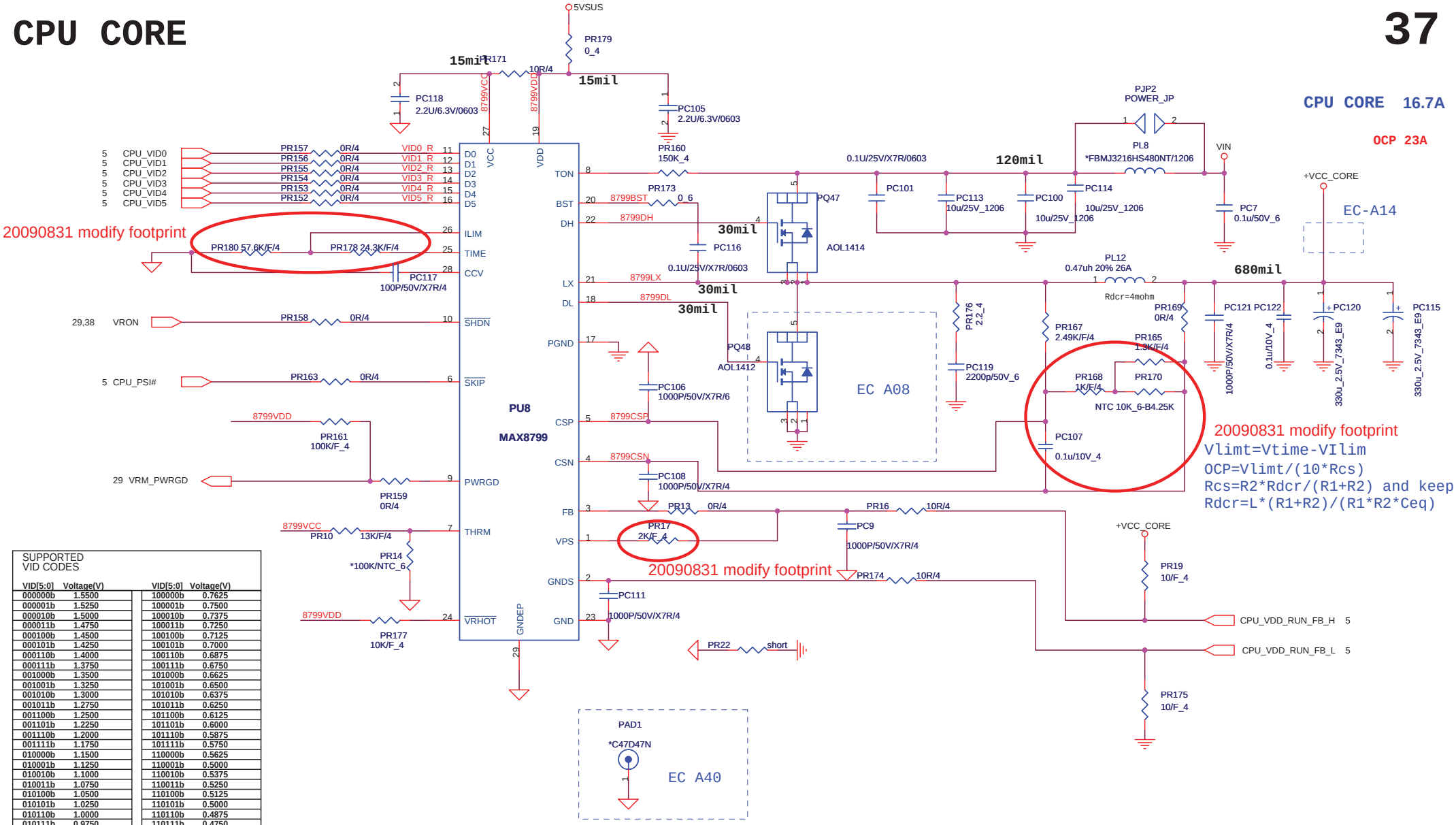
CPU CORE



SUPPORTED VID CODES

VID[5:0]	Voltage(V)	VID[5:0]	Voltage(V)
000000b	1.5500	100000b	0.7625
000001b	1.5250	100001b	0.7500
000010b	1.5000	100010b	0.7375
000011b	1.4750	100011b	0.7250
000100b	1.4500	100100b	0.7125
000101b	1.4250	100101b	0.7000
000110b	1.4000	100110b	0.6875
000111b	1.3750	100111b	0.6750
001000b	1.3500	101000b	0.6625
001001b	1.3250	101001b	0.6500
001010b	1.3000	101010b	0.6375
001011b	1.2750	101011b	0.6250
001100b	1.2500	101100b	0.6125
001101b	1.2250	101101b	0.6000
001110b	1.2000	101110b	0.5875
001111b	1.1750	101111b	0.5750
010000b	1.1500	110000b	0.5625
010001b	1.1250	110001b	0.5000
010010b	1.1000	110010b	0.5375
010011b	1.0750	110011b	0.5250
010100b	1.0500	110100b	0.5125
010101b	1.0250	110101b	0.5000
010110b	1.0000	110110b	0.4875
010111b	0.9750	110111b	0.4750
011000b	0.9500	111000b	0.4625
011001b	0.9250	111001b	0.4500
011010b	0.9000	111010b	0.4375
011011b	0.8750	111011b	
011100b	0.8500	111100b	
011101b	0.8250	111101b	
011110b	0.8000	111110b	
011111b	0.7750	111111b	0.3750

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	VCore(MAX8799)	1A

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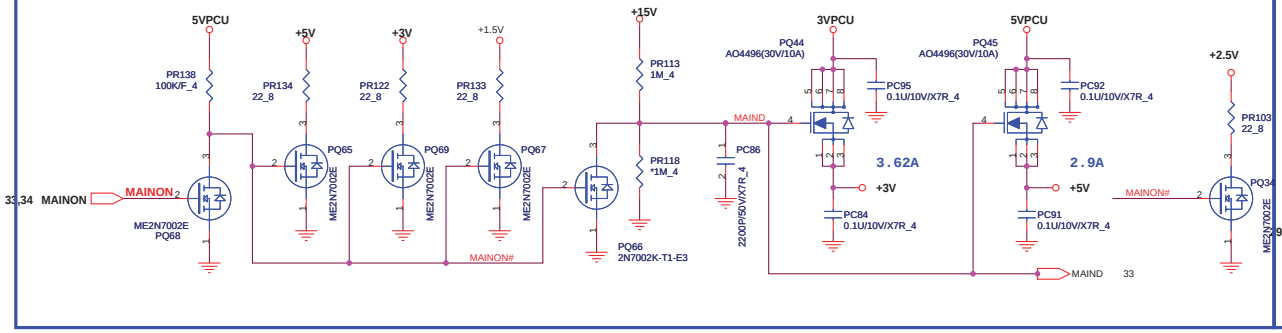
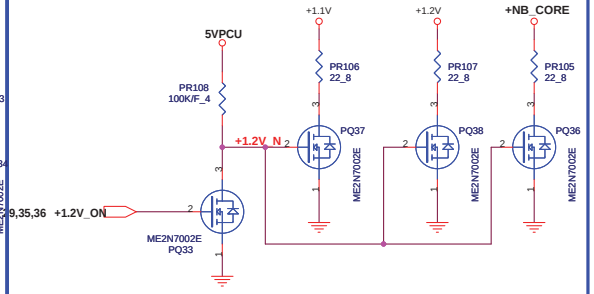
DISCHARGE

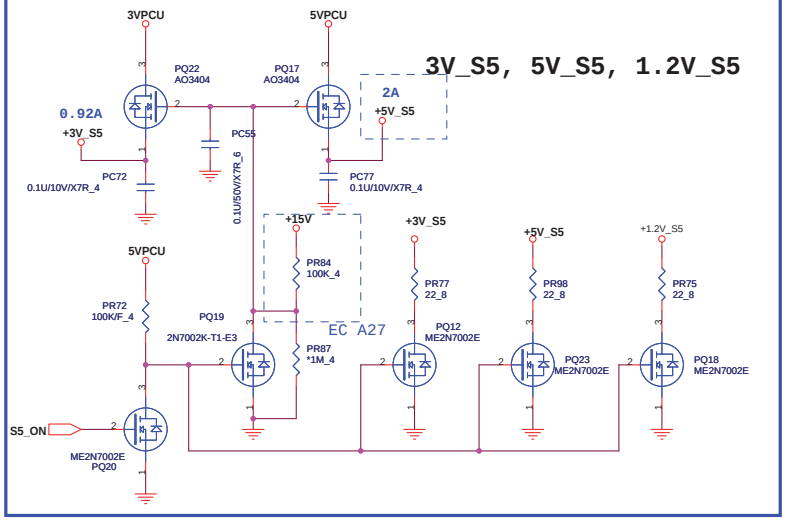
+3V, +5V,+2.5V.+1.5V



+1.1V, +1.2V,+NB_CORE

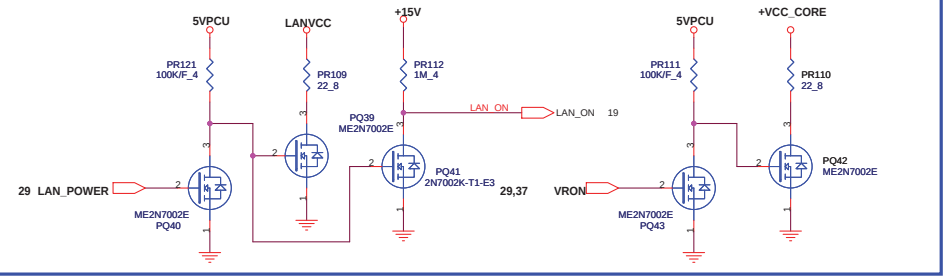


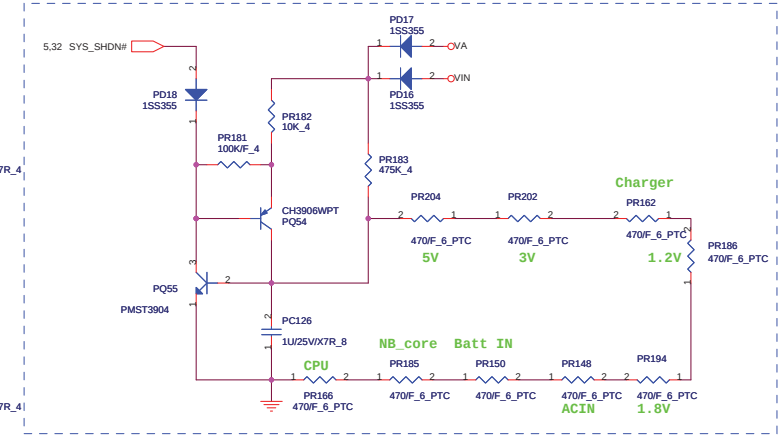
3V_S5, 5V_S5, 1.2V_S5



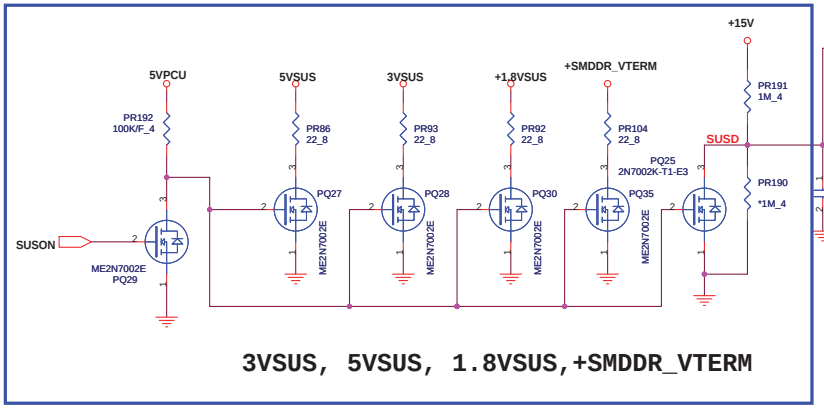
LANVCC

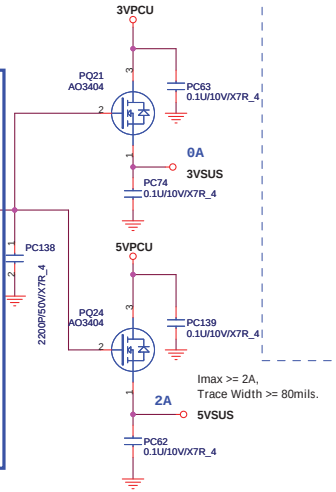
CPU_CORE





3VSUS, 5VSUS, 1.8VSUS,+SMDDR_VTERM





Imax >= 2A,
Trace Width >= 80mils.

Quanta Computer Inc.			
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Size	Document Number		Rev
	Discharge		1A
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INDEX

RS780 SM BUS

RS780 I2C (S0)	I2C and AUX Function Define
DAC_SCL DAC_SDA	CRT (+5V)
I2C_CLK I2C_DATA	LVDS (+3V)
DDC_CLK0/AUX0N DDC_DATA1/AUX0P	HDMI (+5V)
DDC_CLK1/AUX1N DDC_DATA1/AUX1P	not used

SB710 SM BUS

SB710 SMBUS	SMBUS Function Define
SMBCLK0 SMBDAT0 (+3V)	DDR / DDR THER / CLOCK GEN
SMBCLK1 SMBDAT1 (+3V_S5)	LAN IC//WI-FI
SMBCLK2 SMBDAT2 (+3V_S5)	not used

KBC(EC) SM BUS

KBC SMBUS (+3VPCU)	SMBUS Function Define
MBCLK MBDAT	BATTERY (+3VPCU)
2ND_MBCLK 2ND_MBDATA	CPU THER SENSOR(+3V) EC EEPROM (+3VPCU)
3ND_MBCLK 3ND_MBDATA	G-SENSOR(+3VS5)

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	SYSTEM INFORMATION	1A

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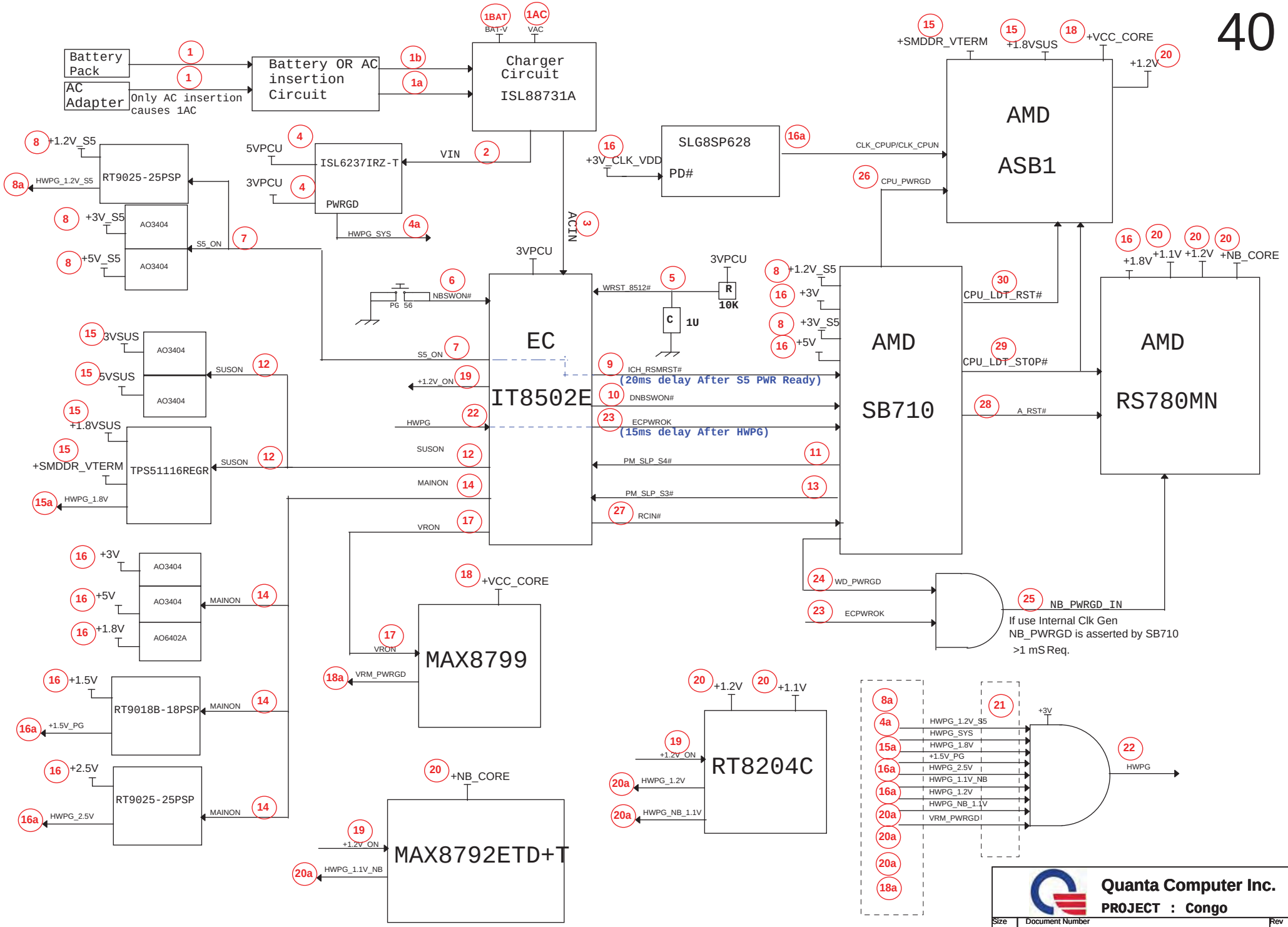

Quanta Computer Inc.

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Size	Document Number	Rev
	Power On Sequence	1A

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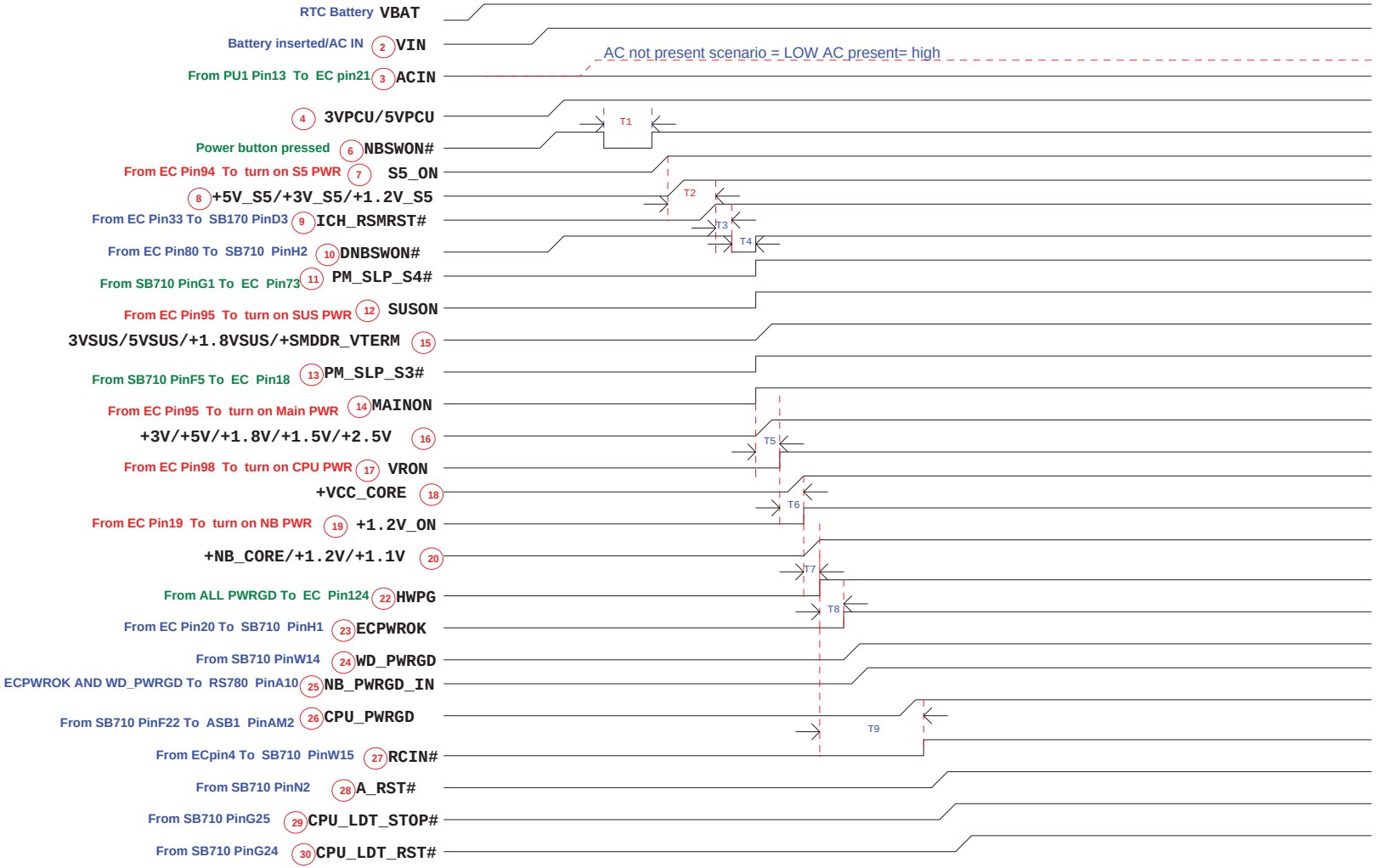

T1	>16ms
T2	20ms
T3	5ms
T4	1ms
T5	15ms
T6	5ms
T7	5ms
T8	15ms
T9	108ms

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FL3B MK-Note Congo Schematic EC Tracking Record A (for SDV --> SIV)08 /27/ 2009

EC #	Page	CMVC #	Description	Date	Part Affected
A00	31		Change PJ2 pin assignment		
A01	29,11		Change BT_ON# to Test point on EC and BT_ON controlled by SB710 pinW17 (GPIO0)		
A02	26		Change CN8 pin number (13pin-->10pin)		
A03	24		C236 change footpint size		
A04	35		Modify PQ56,PQ57, PL13 footprint		
A05	36		Modify PQ60 footprint		
A06	37		Modify PR165,PR168,PC107,PR17,PR178,PR180 footprint		
A07	27		Delete SW1		
A08	37		Delete PQ53		
A09	32		Delete PJP18,PJP15		
A10	33		Delete PJP16,PJP17		
A11	34		Delete PJP8,PJP6,PJP7		
A12	35		Delete PJP3		
A13	36		Delete PJP5,PJP12		
A14	37		Delete PJP10		
A15	28		Delete Q27 & Mount R344		
A16	05		R73 unmount & Add R416		
A17	05		Exchange Q8 pin1 and pin3 net connection , Unmount R24		
A18	11		Unmount R142,R131,R145,R111 & Mount R143,R132,R139,R110		
A19	22		Change CN10 symbol and footprint		
A20	18		Add CN24 &DIGITAL_MIC Circuit		
A21	21		Unmount R92,R91,R96 & Mount R90,R93		
A22	29		Add MB_ID circuit ,Resume_RST move to default high.(Pin.33->99) ,Delete D5		
A23	23		C295 change footpint size		
A24	29,21		Add USBCHR_ON# on EC pin97 & U31 pin4		
A25	11		Change USB5--NC,Exchange USB2 & USB4 ,USB5--USB8		
A26	33		Power combustion test need change PQ8 package		
A27	38		Change PR84 from 1M to 100K for fix 3V_S5 knee voltage		
A28	29		Add Wake# signal on EC pin57		
A29	17		Add Pi Filter near CN1 by EMI		
A30	4		Delete Q17,Q18,Q19		
A31	29		Change EC_ID0 signal from EC pin100 to EC pin35		
A32	11		Change R273 to Bead and mount C352		
A33	18		Add R423,R424,R425		
A34	18		Add L-C filter circuit near CN11		
A35	30		HOLE17 connect AGND		
A36	29		Change EC_ID0 signal from EC pin35 to EC pin106 Change EC_ID1 signal from EC pin106 to EC pin35		
A37	27		Reserve for trying LED light on PWR BD with ME		
A38	22		NC R371		
A39	29		Unmount R98		
A40	37		A short pad for EMI		
A41	29		EC Pin76 HDD_DETECT# connect to CN13 Pin12,Change R144 from 10K to 100K.		
A42	20		CN13 Pin12 connect to EC Pin76 HDD_DETECT# ,CN13 Pin18 through a 0 Ohm to GND.		
A43	10		Add D26 for CR2025 (non-chargeable RTC battery)		
A44	3-6		Modify CPU footprint for BGA ball of corner solder mask (open pad size to 14mail) at SIT-R		
A45	7-9		Modify NB footprint for BGA ball of corner solder mask (open pad size to 14mail) at SIT-R		
A46	30		Modify FP of HOLE6 to "H-C259D209P2" for ME.		
A47	16		Modify CAMVCC circuit from 3V to 5V for 5V camera module.		
A48	21		Modify values of ext. R,BOM and modify the power rail of MAX14550A & U5 & U31		
A49	29		Connect EC pin 83 to Flash WP# pin by "EC_WP#",modify BOM for ED_ID table.		
A50	25		Reserve 0 ohm for BT_DET#		
A51	27		Reserve 0603 0ohm for RF solution.		
A52	18		Reserve 0603 0ohm for RF solution.		
A53	10		Reserve charage circuit & Add diode for non-chargeable RTC battery		
A54	32		Change short PJP9 and PJP13 to add Bead (UPB201212T-800Y-N) for RF		
A55	30		Modify FP of HOLE15,HOLE14,HOLE13,HOLE12,HOLE11 for ME.		
A56	10		Change short FP of BT1 for customer request		
A57	29,21		Modify RTS5159 circuit for fix 144 Mhz NOISE		
A58	17,26		Add two 1206 fuse for CRT and Touch Pad		
A59	30		Add 2200p cap *13 for EMI		