Olympus Block Diagram

Project code: 91.4Y701.001
PCB P/N :
REVISION : 07242-SB

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3

71.09502.00W

Mobile CPU
Penryn
4, 5

G7921
07

Hyper design

HOST BUS 667/800/1066MHz@1.05V

DDR3 socket 15
DDR3 socket 16
800/1066MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13,14

UMA
PCIE*16

Extended VGA
ATI M82s
19,20,21,22,23,24

CRT 18
LCD 17
HDMI 25

X4 DMI 400MHz
C-Link0

HP/SPDIF
INT.SPKR
MIC In
INT MIC ARRAY

Codec
ALC269
(include AMP) 34
Support Dolby HT

AZALIA

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
12 USB
High Definition Audio
LPC I/F
Serial Peripheral I/F
26,27,28,29,30

PCI BUS

Ricoh
R5C833
Cardreader
32,33

1394
CONN 33

MS/MS Pro/xD/
MMC/SD
5 in 1 33

LAN
Boardcom
10 /100M
BCM5906 35

RJ45 36

PCIe x1

Mini Card *2
Kedron a/b/g/n 40

RJ11

MODEM
MDC Card 39

LPC BUS

New card 41
PCI Express

SATA
SATA

USB

MINI USB
BlueTooth 39

KBC
Winbond
WPC776 38

SPI I/F

BIOS
2M byte 51

LPC
DEBUG
CONN. 31

Power switch 29

SATA-HDD 31

SATA-CDROM 31

Touch
Pad 51

INT.
KB 51

CIR 39

22

USB
3 Port 42

CAMERA 17

PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)

TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)

TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5308 39	
3D3V_S0	2D5V_S0 (300mA)

CHARGER BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

NB DC/DC ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE

SC411 48	
DCBATOUT	1D5V_S3

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: BLOCK DIAGRAM

Size: A3 | Document Number: LT32P | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 1 of 53

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

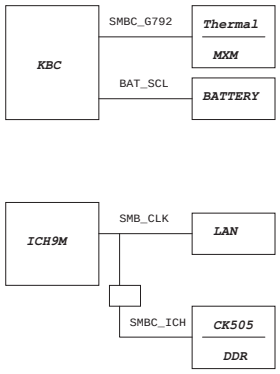
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIE is operational (Default) 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

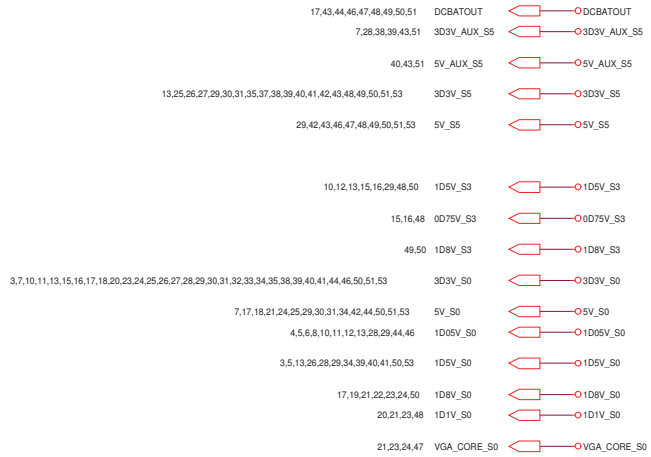
	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	Combo(ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1



BOM1

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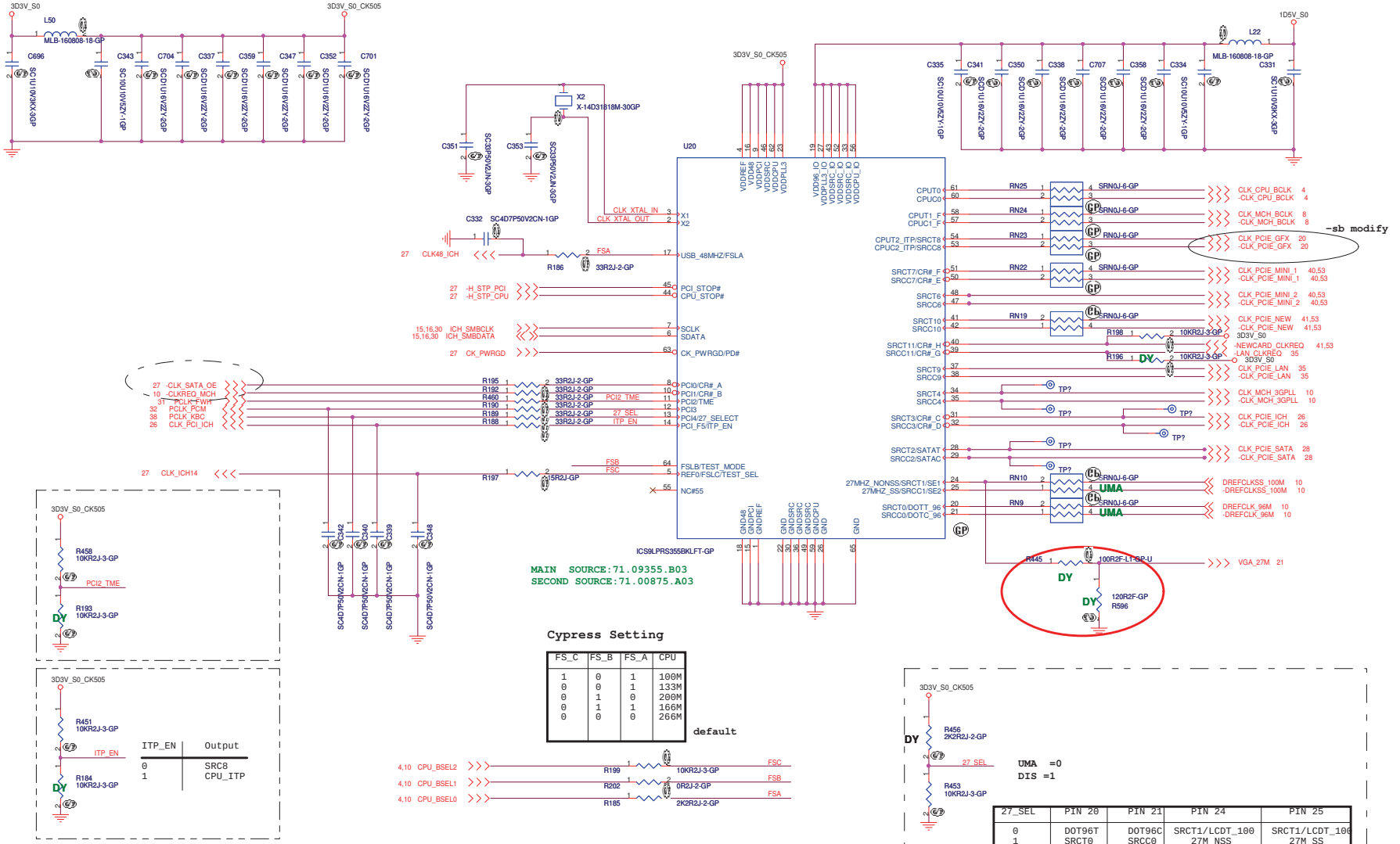
Title: Reference

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 2 of 53



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

BOM1

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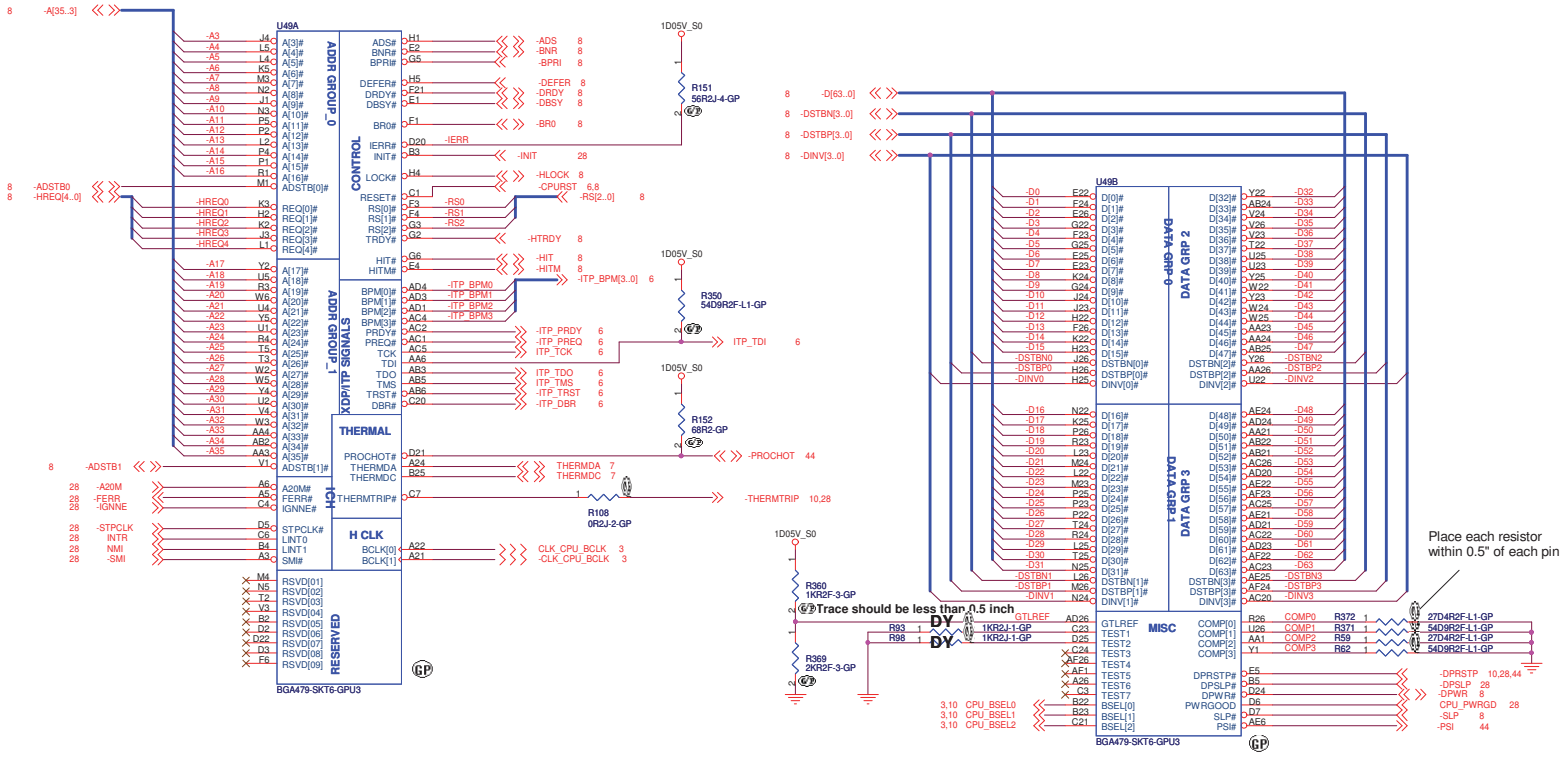
Title: *Clock Generator*

Size	Document Number	Rev
	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 3 of 53



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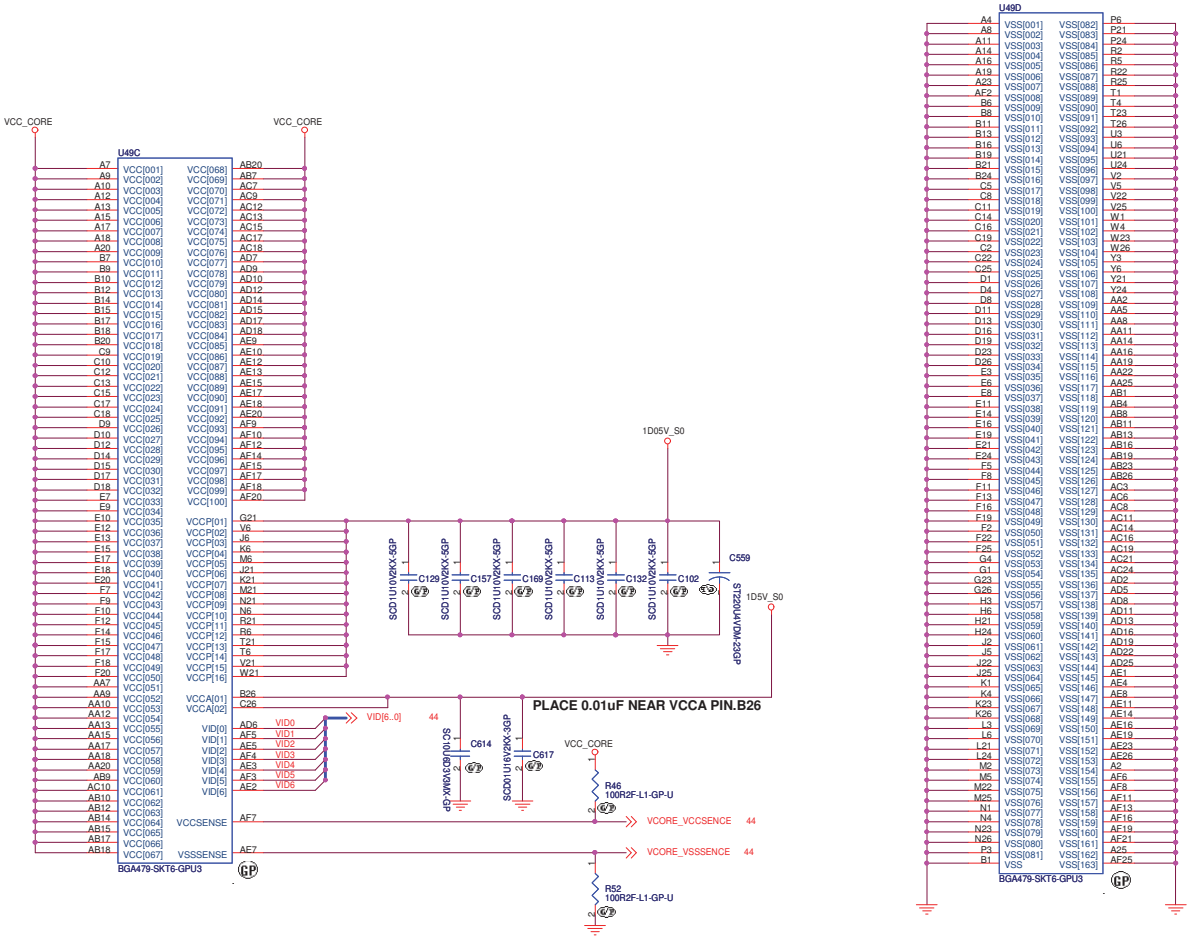
Title: **Penryn CPU(1/2)**

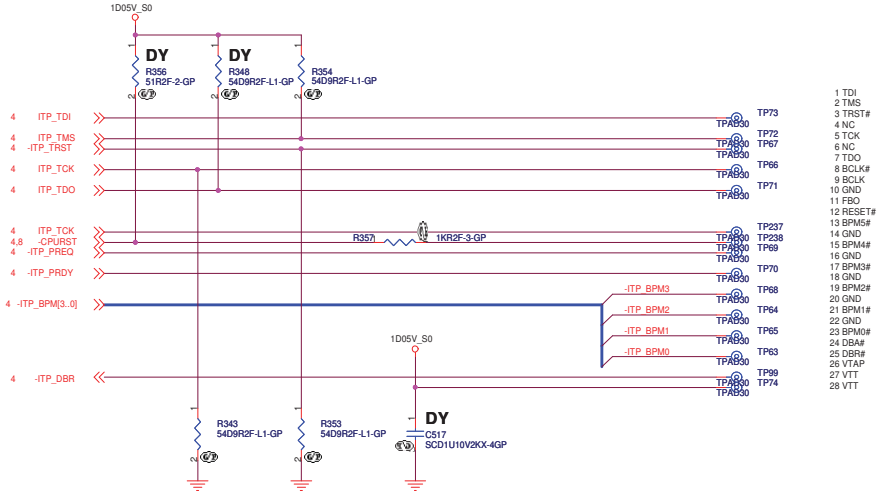
Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 4 of 53



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Penryn CPU(2/2)***	
Size C	Document Number **Olympus**	Rev SA
Date: Wednesday, December 26, 2007	Sheet 5 of 53	



(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% ASM
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

BOM1

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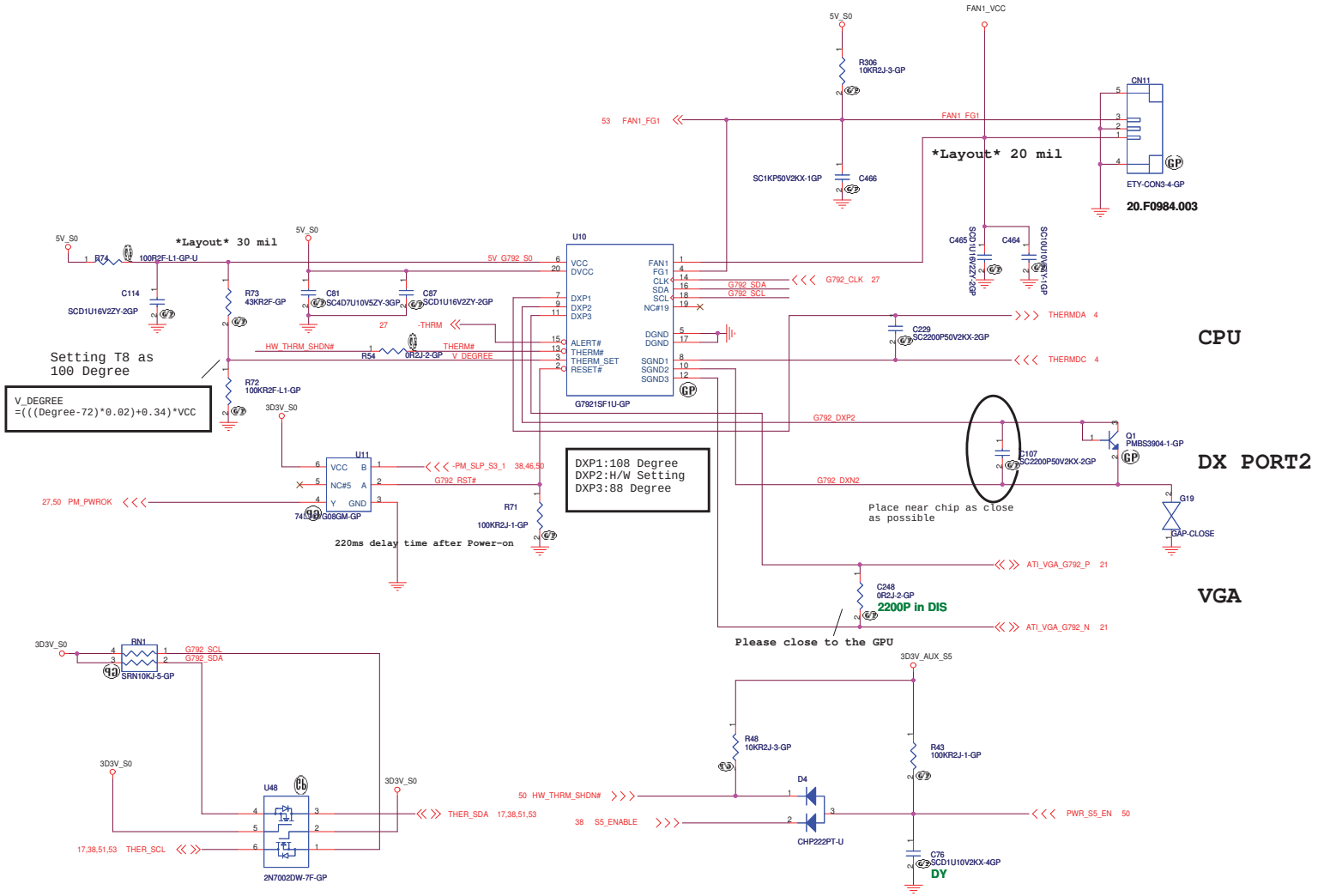
Title: **ITP CONN**

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 6 of 53



BOM1

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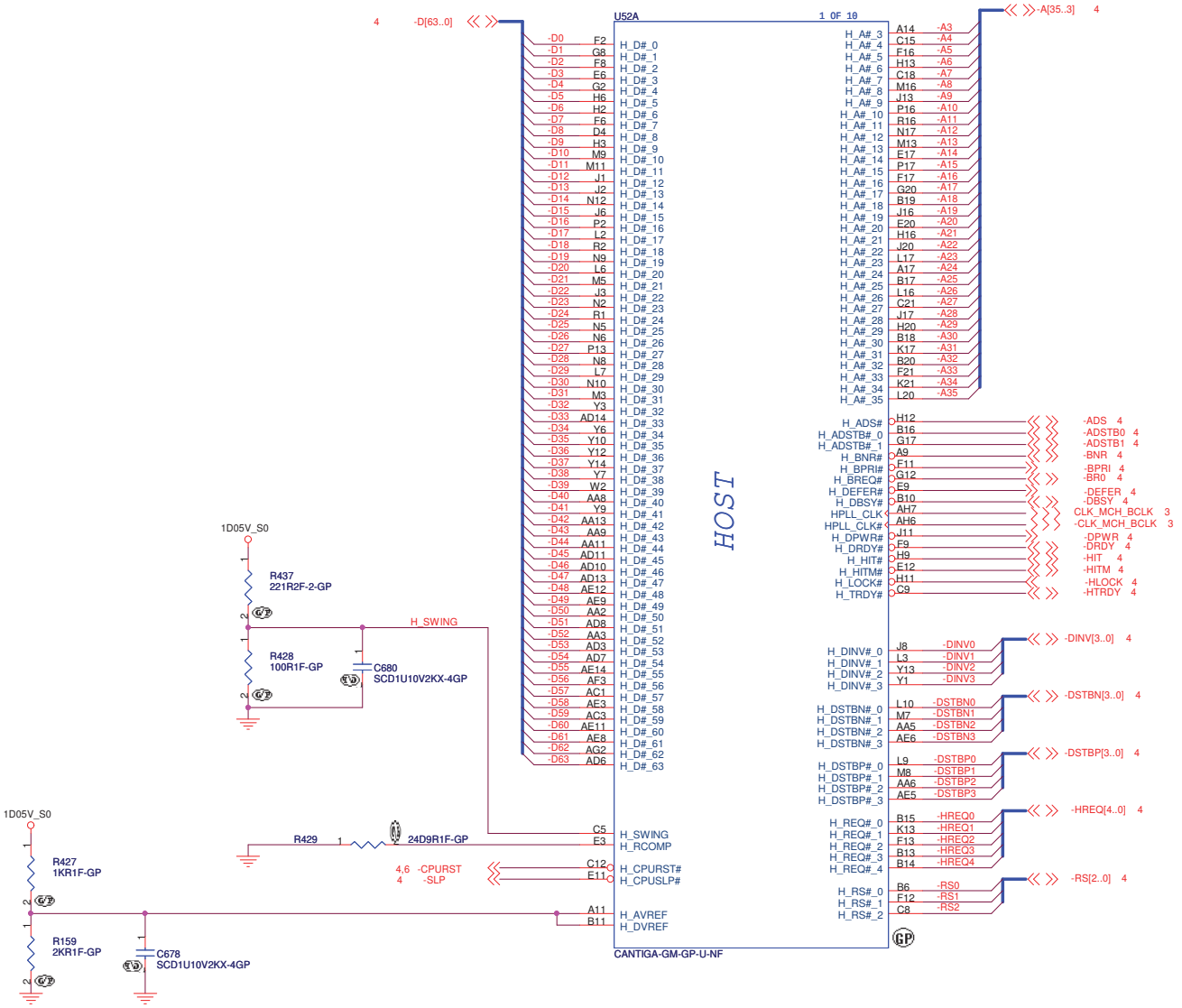
Title: ***Thermal/Fan Controllor G792***

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 7 of 53



Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

BOM1

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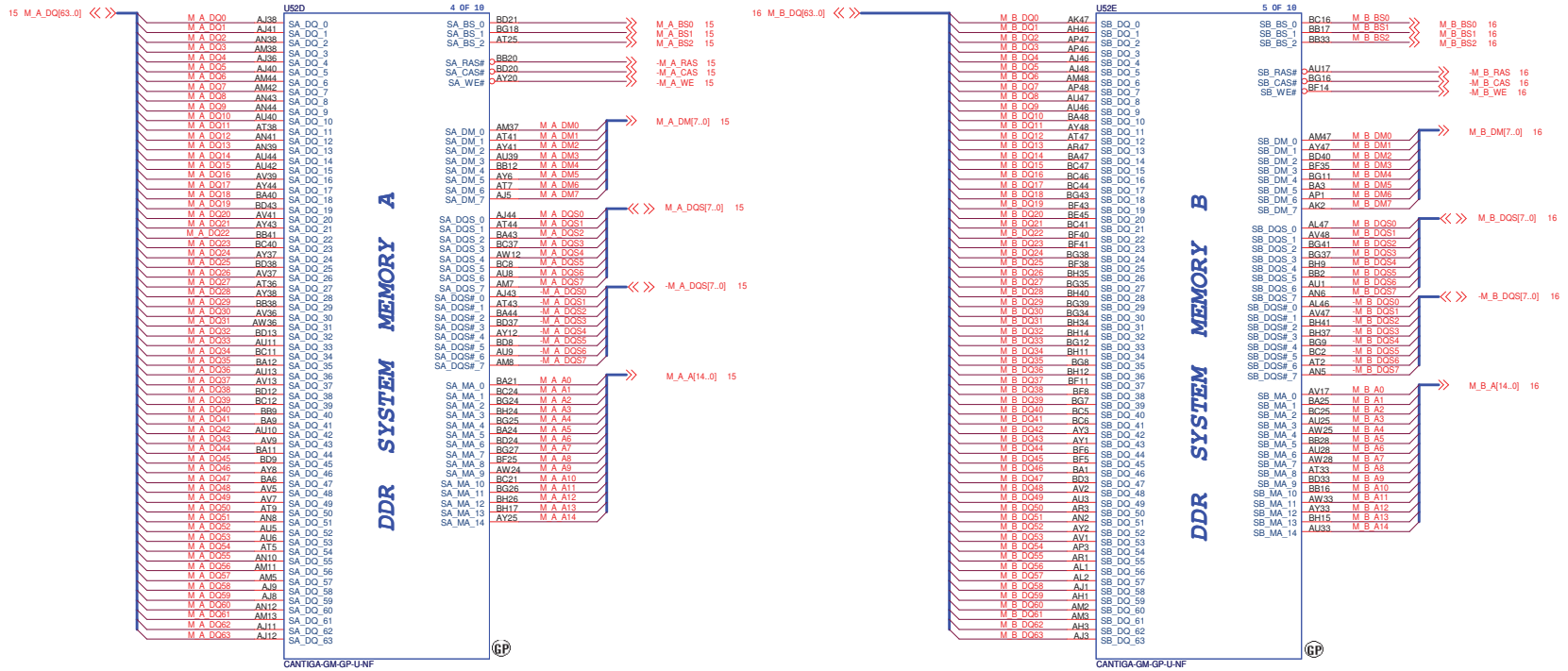
Title: **Cantiga(1/7):HOST I/F**

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 8 of 53



BOM1

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Title: ***Cantiga(2/7):DDR3***

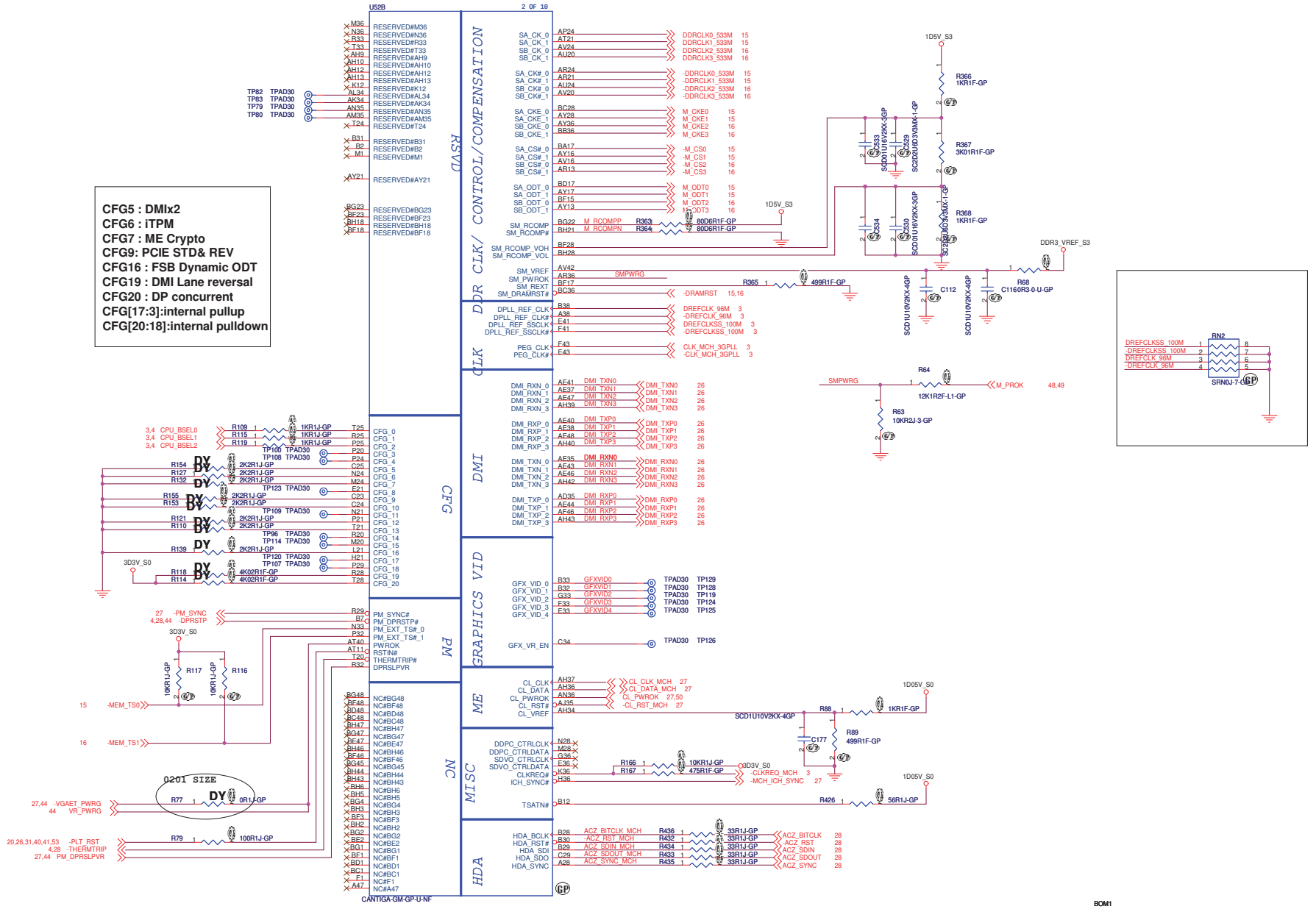
Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 9 of 53

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown



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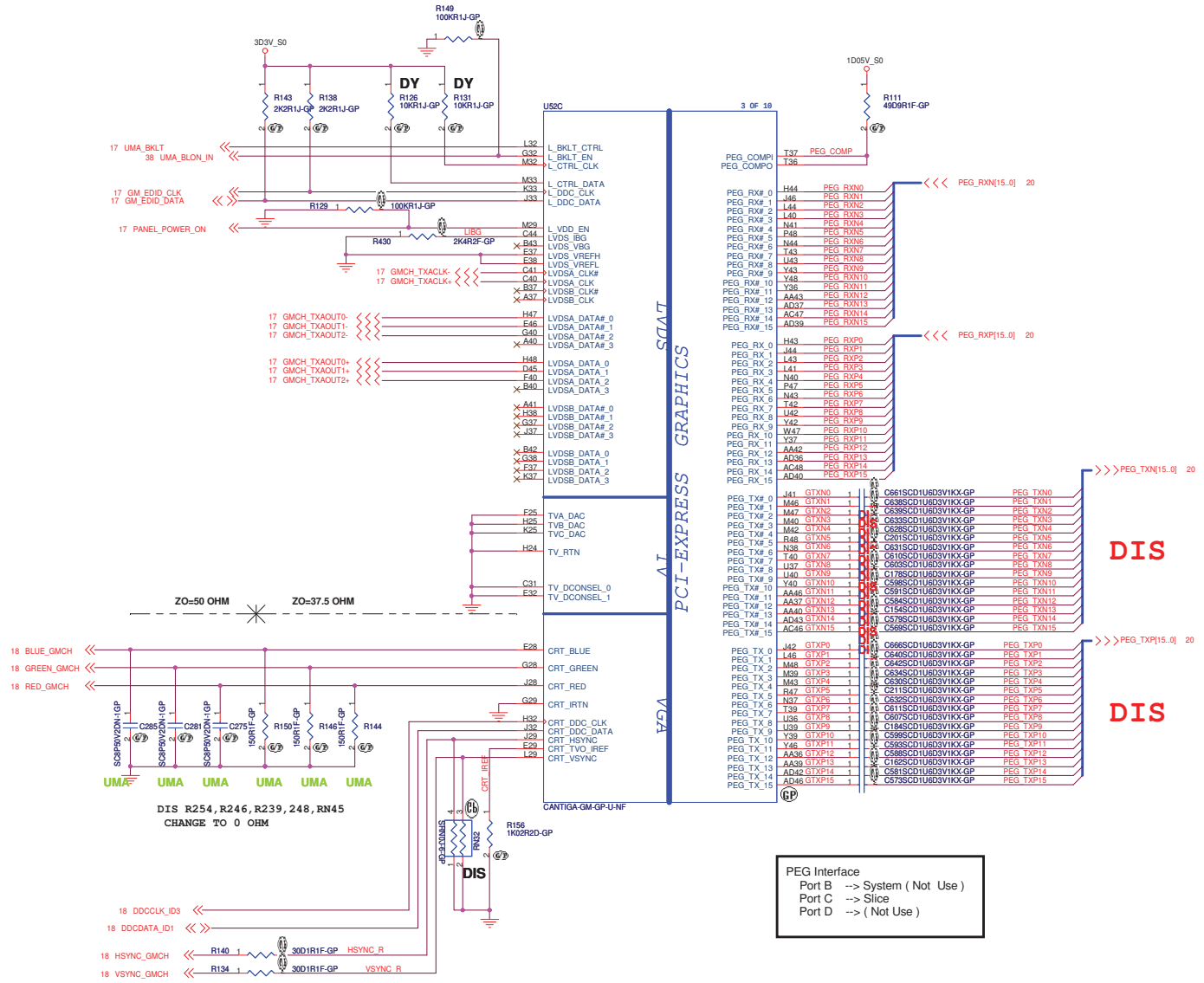
Title: **Cantiga(3/7):DMI/PM/CFG/GF**

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 10 of 53



BOM1

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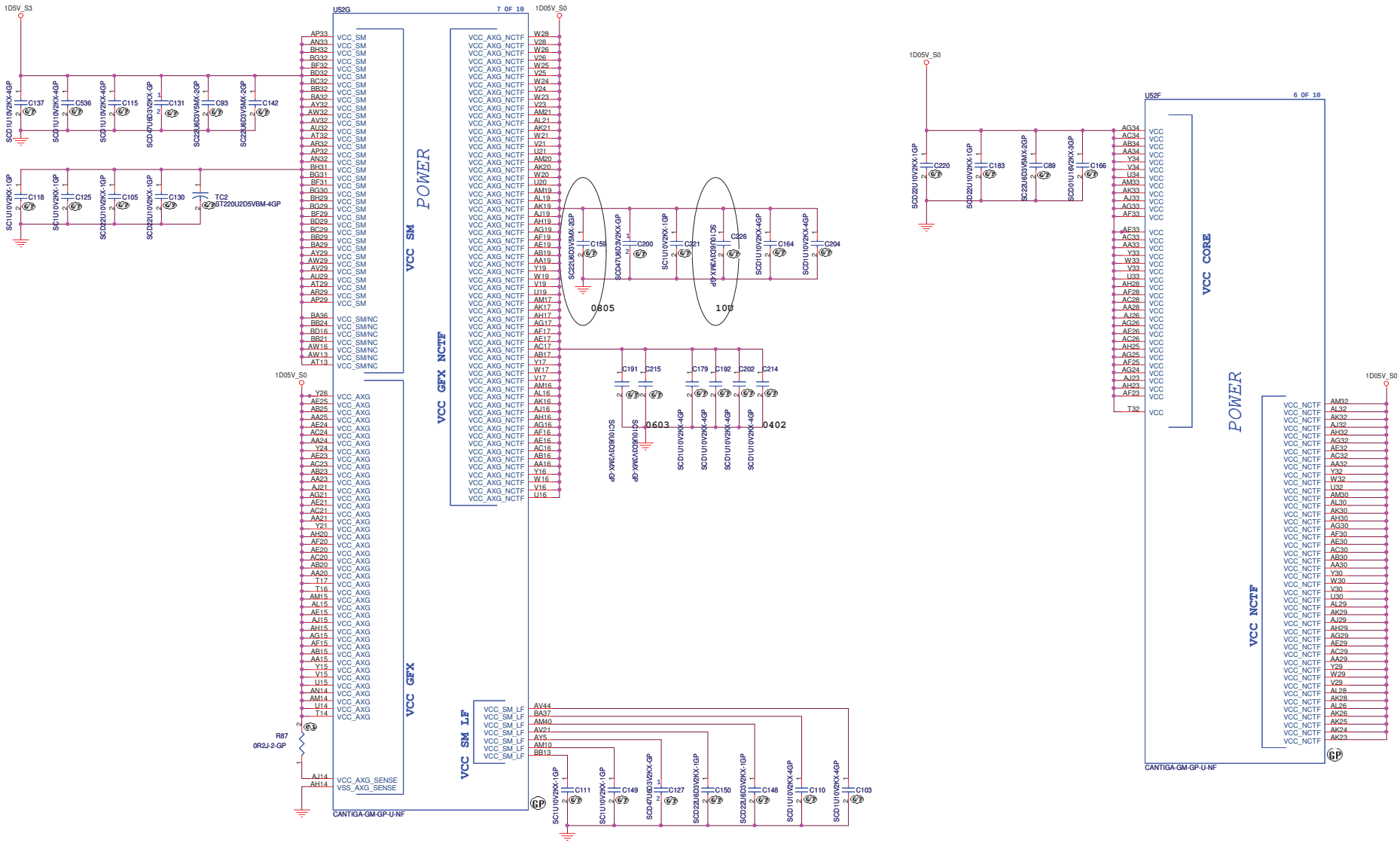
Title: ***CANTIGA(5/7)-VGA/LVDS***

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 11 of 53



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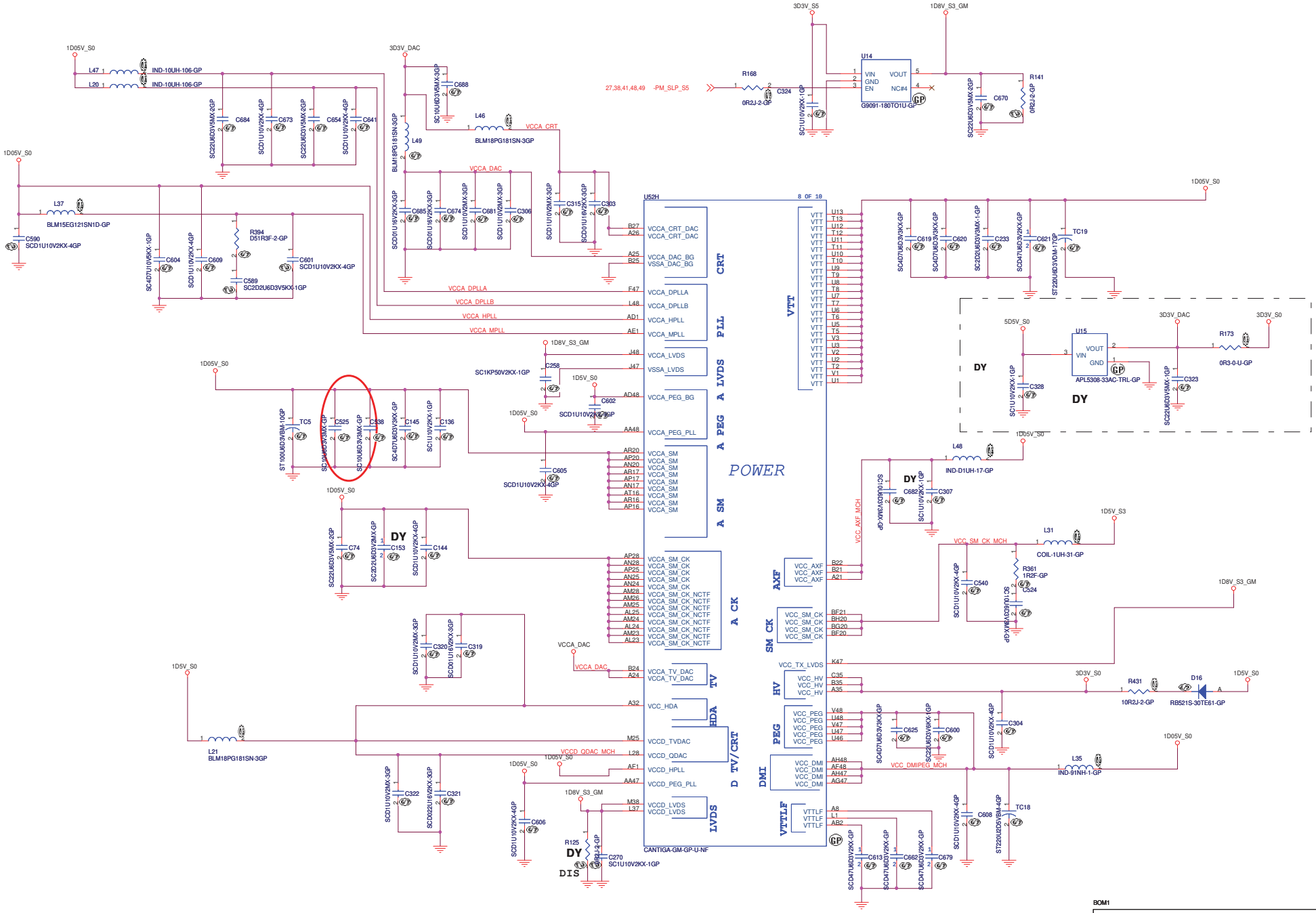
Title	***Cantiga(5/7):VCC***	
Size C	Document Number **Olympus**	Rev SB
Date: Wednesday, December 26, 2007	Sheet 12 of 53	



BOM1

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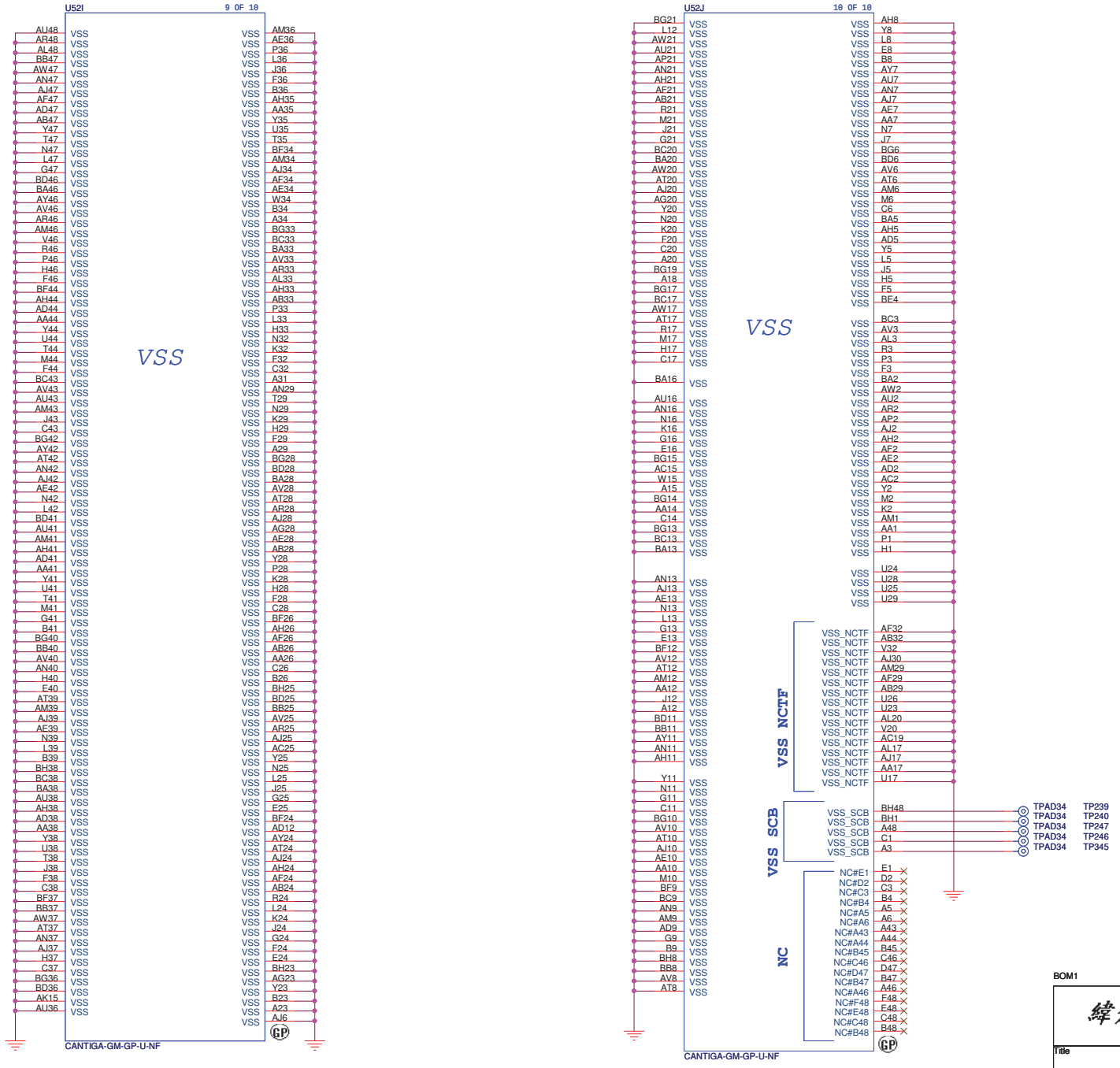
Title: ***Cantiga(6/7):VCC***

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 13 of 53



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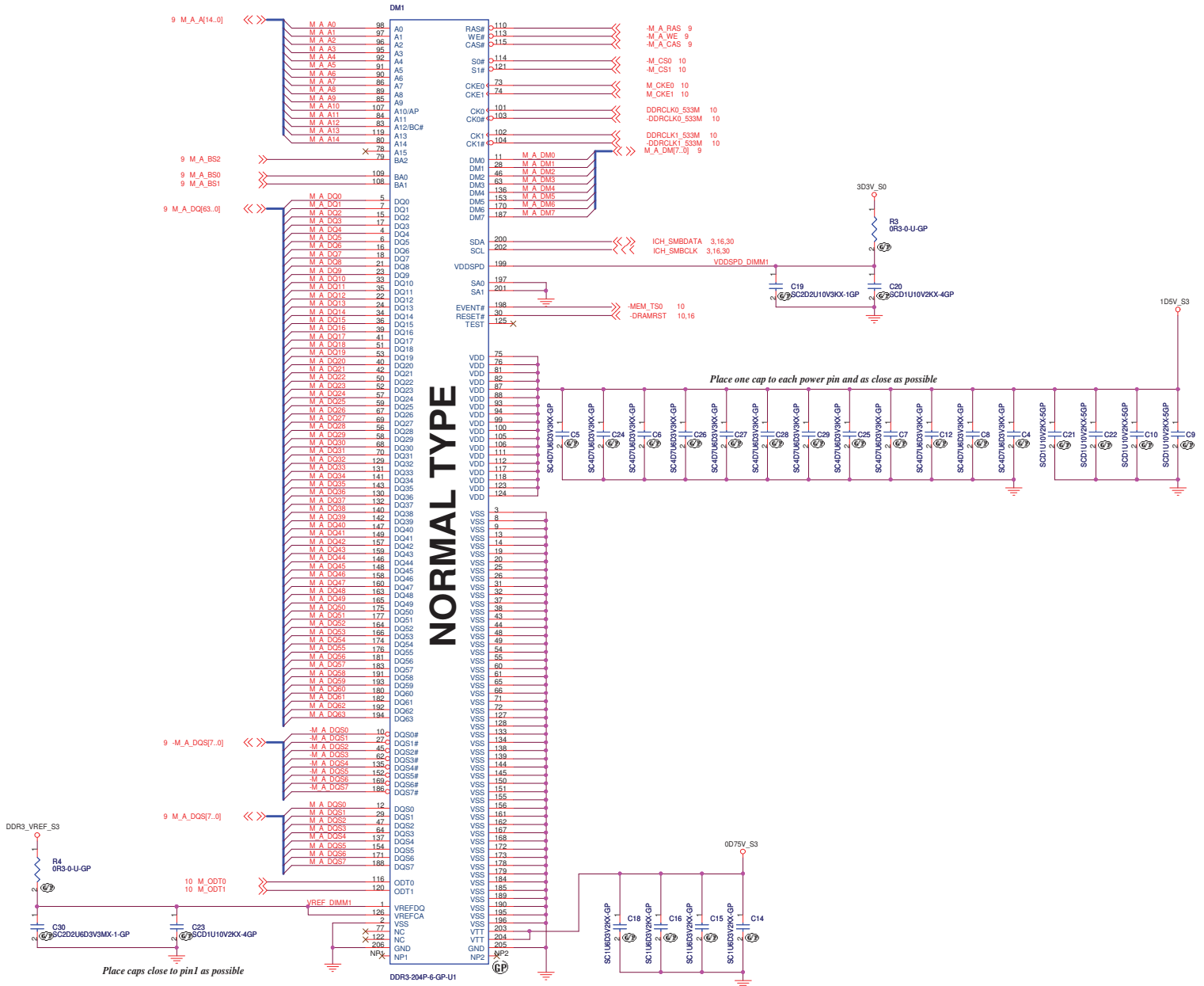
Title: ***Cantiga(8/7):GND***

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 14 of 53



62.10017.F91

H= 9.2

BOM1

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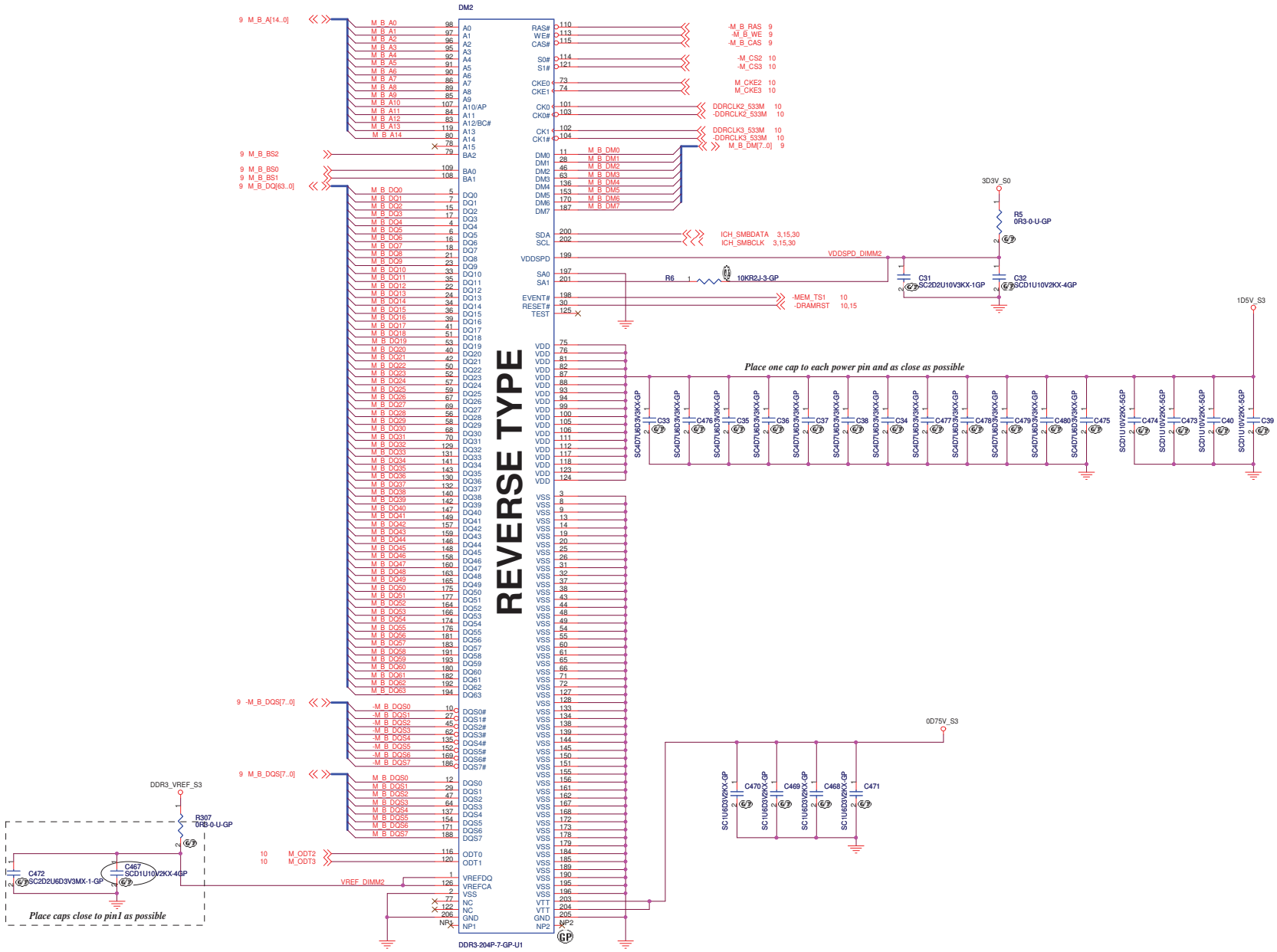
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SODIMM-A (NORMAL TYPE)

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 15 of 53



BOM1

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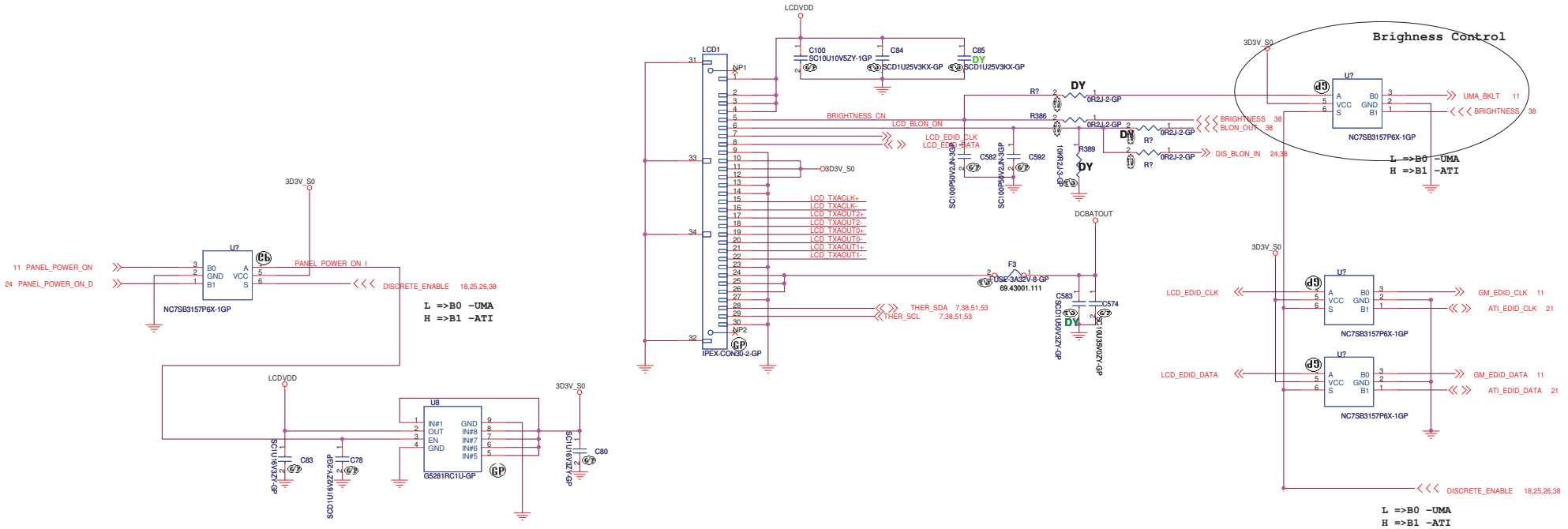
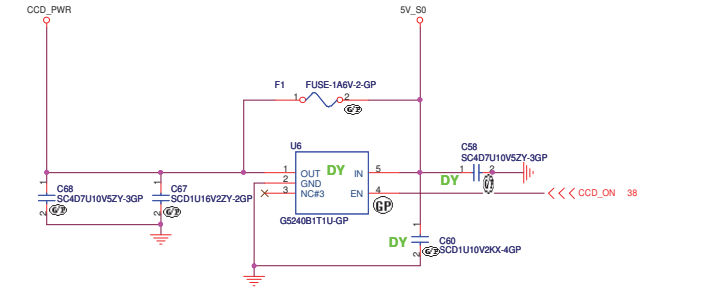
Title: **DDR3 SODIMM-B (REVERSE TYPE)**

Size	Document Number	Rev
C	Olympus	SB

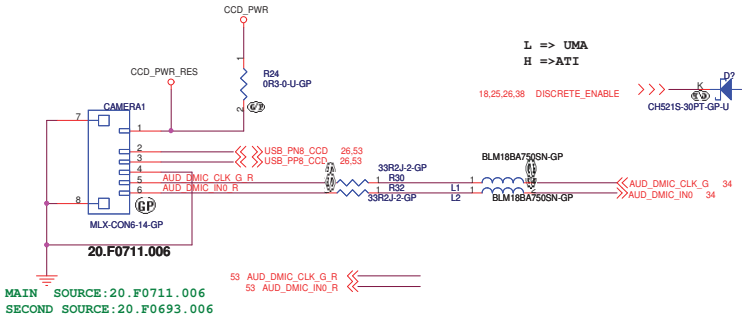
Date: Wednesday, December 26, 2007 Sheet 16 of 53

LCD/INVERTER CONN





CAMERA & DIG-MIC



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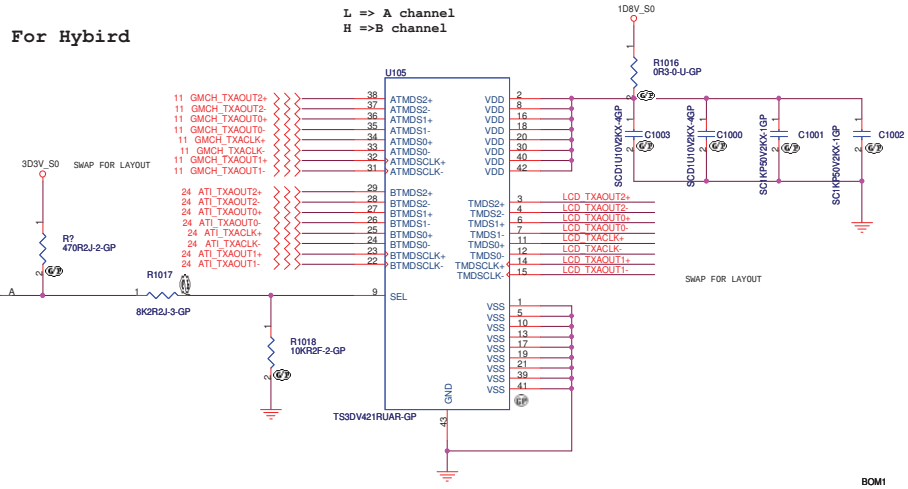
SECOND SOURCE:20.F0693.006

For Hybird



BOM1

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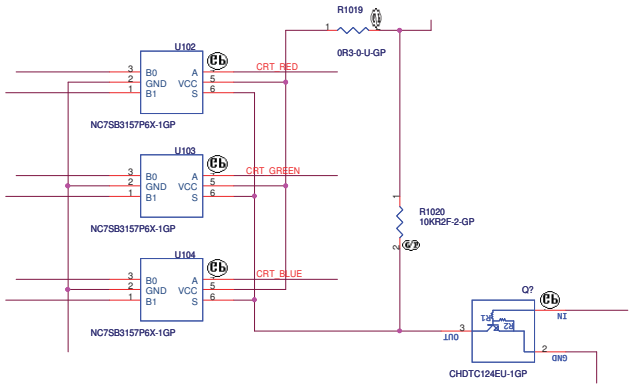
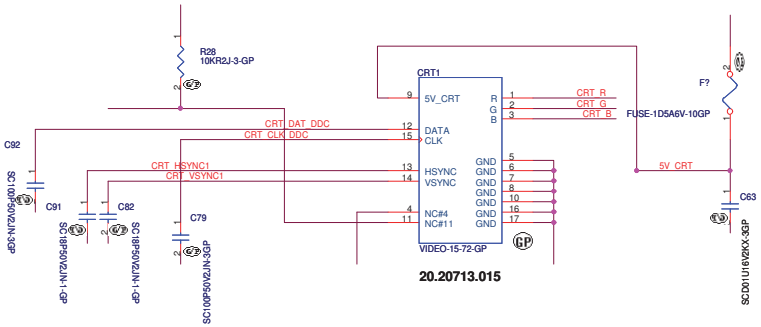
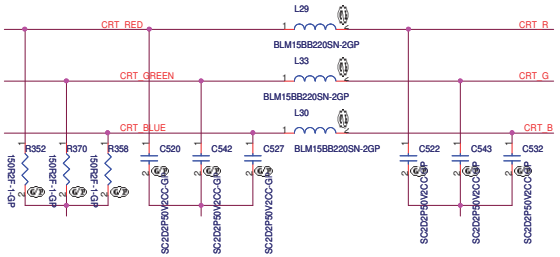
Title: LCD CONN & CAMERA & DIG-MIC

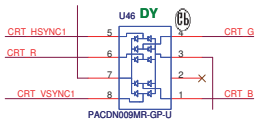
Size	Document Number	Rev
	Olympus	SB

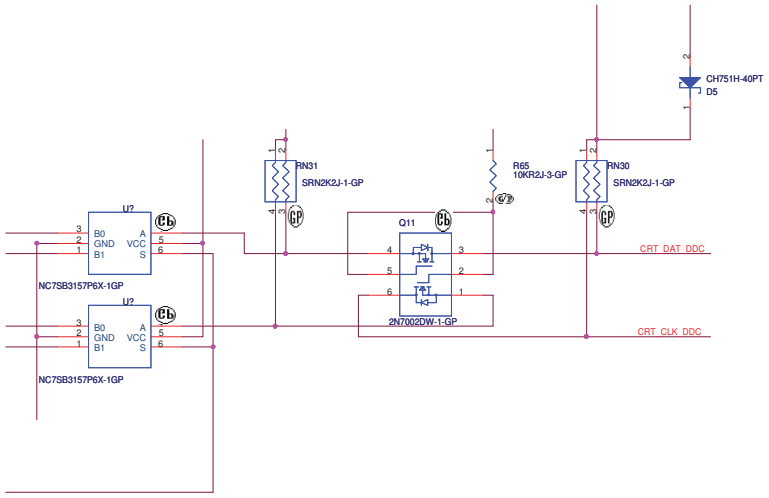
Date: Wednesday, December 26, 2007 Sheet 17 of 53

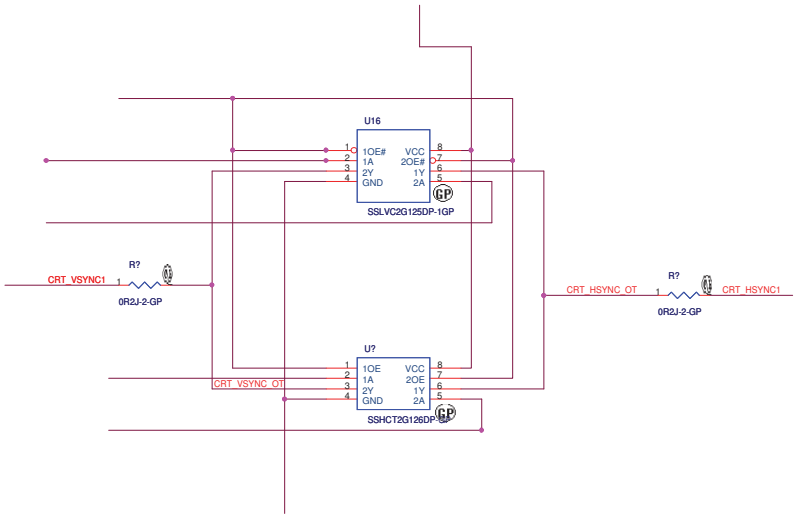












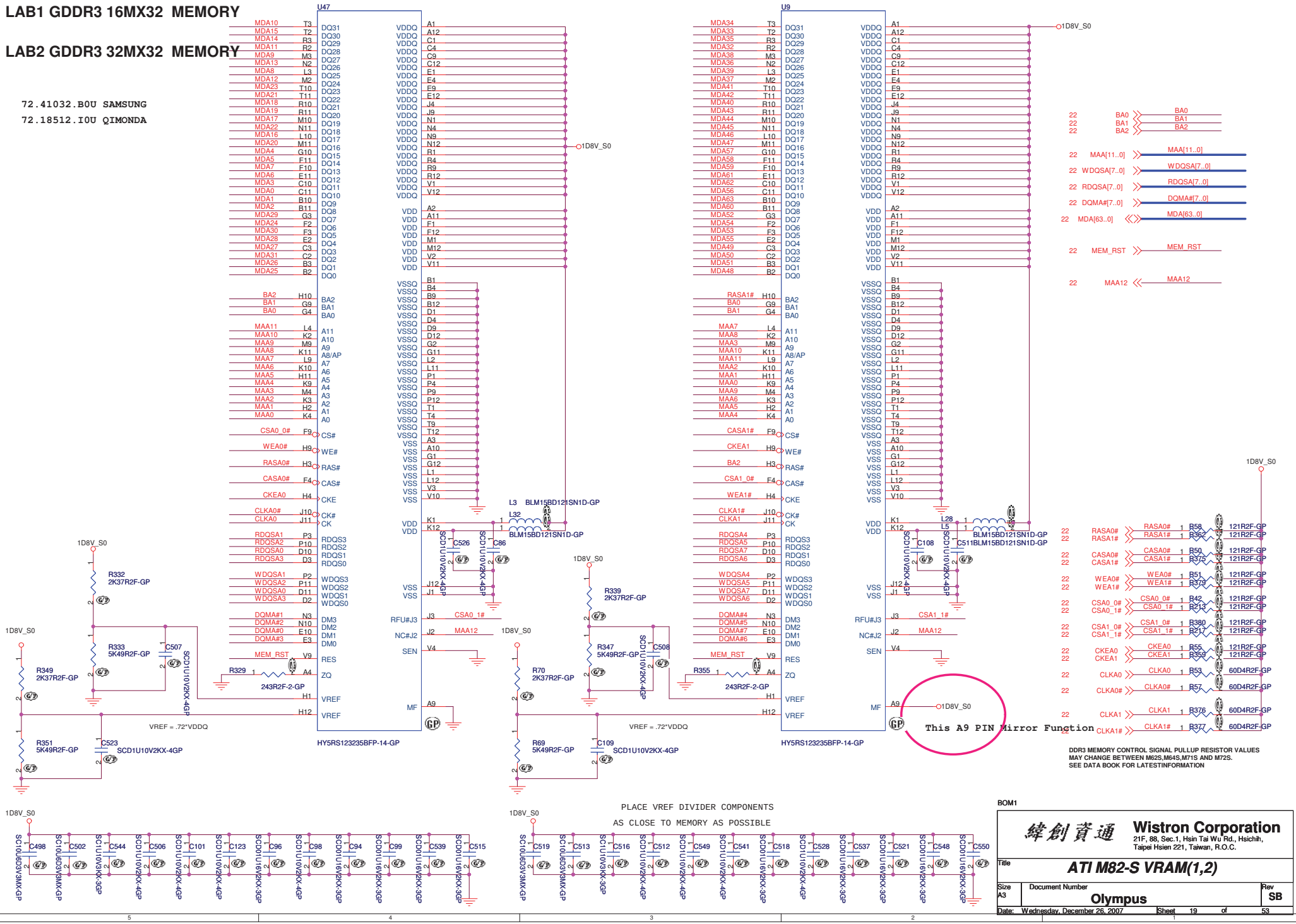
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CRT/TV Connector		
Size	Document Number: Olympus	Rev: SB
Date: Wednesday, December 26, 2007	Sheet 18 of 53	

LAB1 GDDR3 16MX32 MEMORY

LAB2 GDDR3 32MX32 MEMORY

72.41032.B0U SAMSUNG

72.18512.I0U QIMONDA



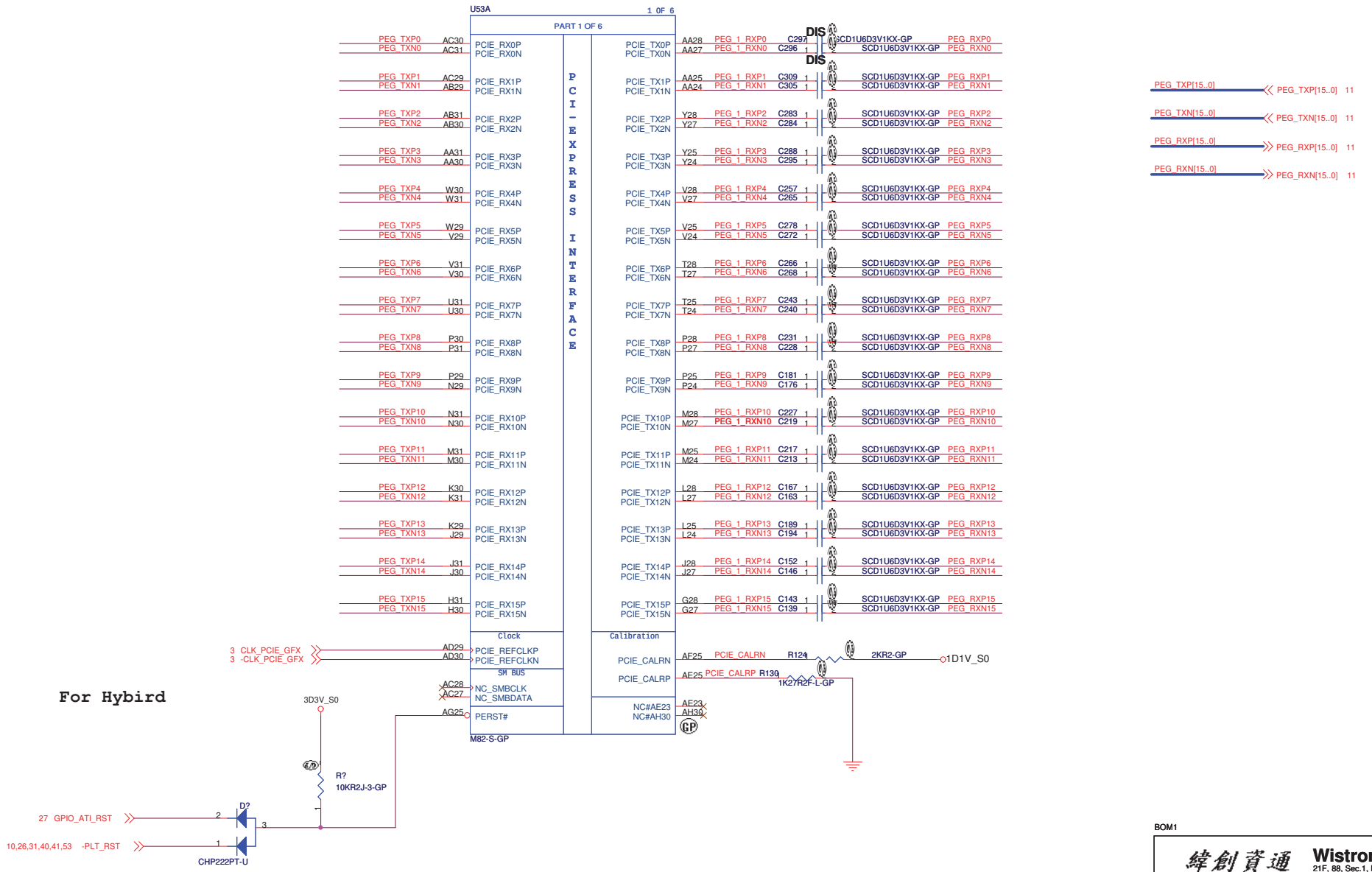
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M82-S VRAM(1,2)**

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 19 of 53



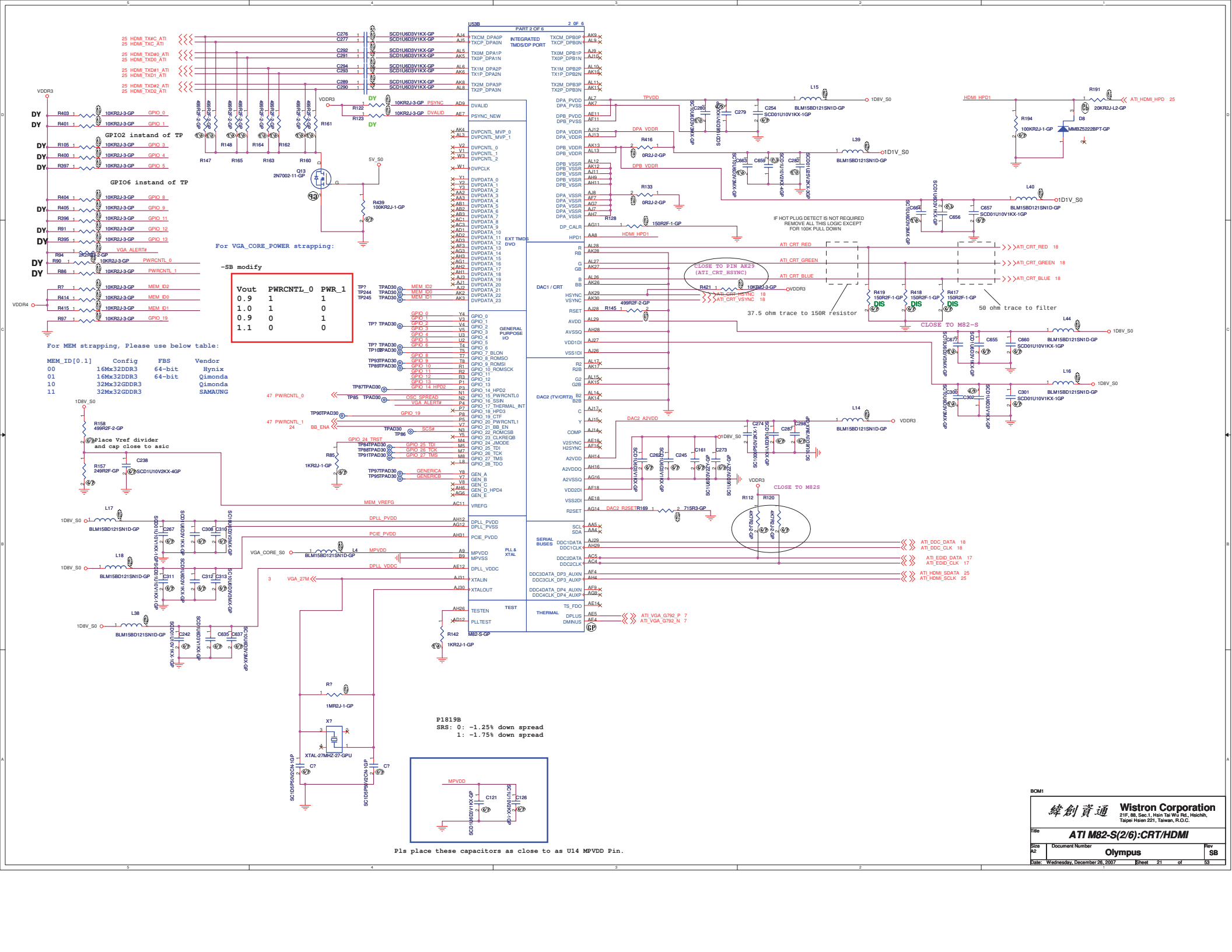
BOM1

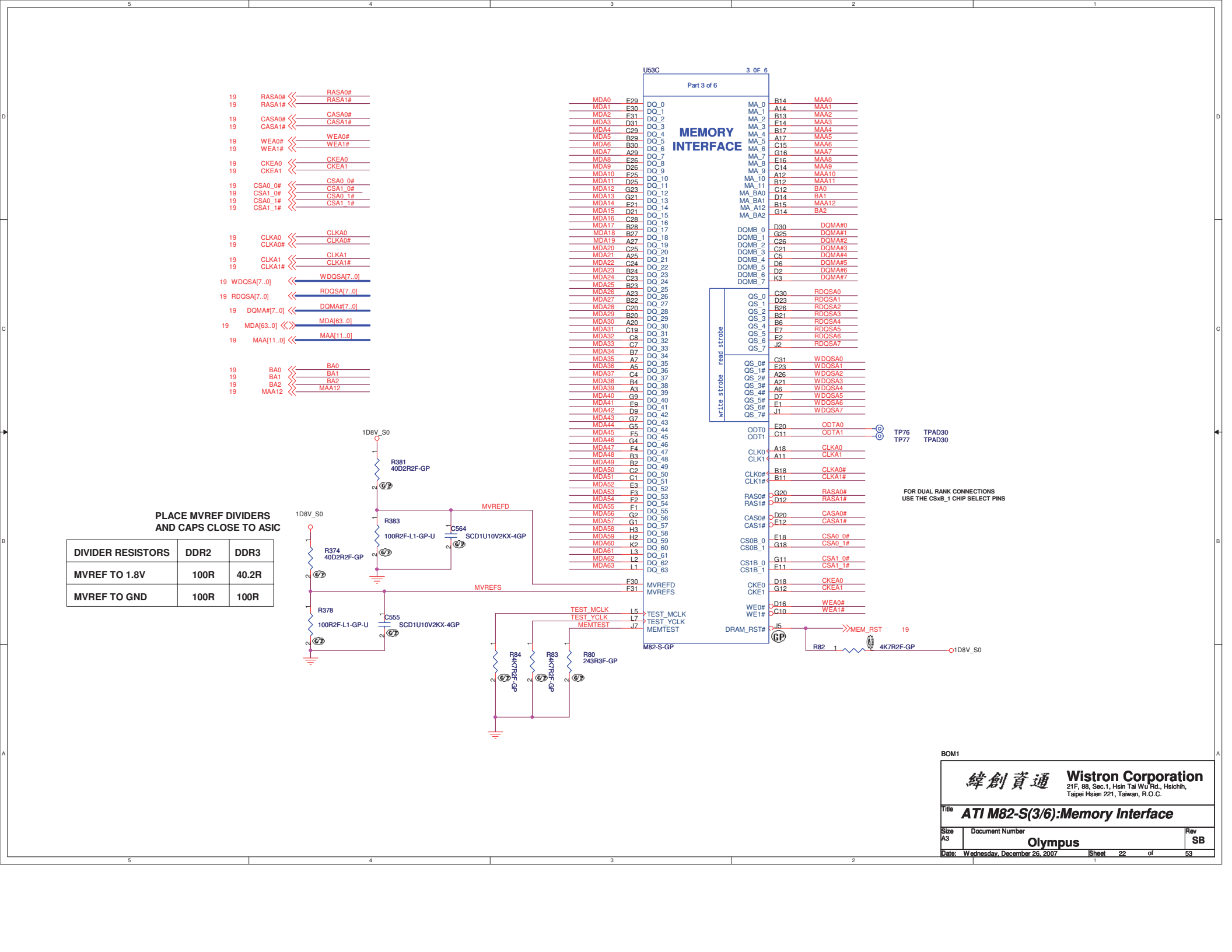
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

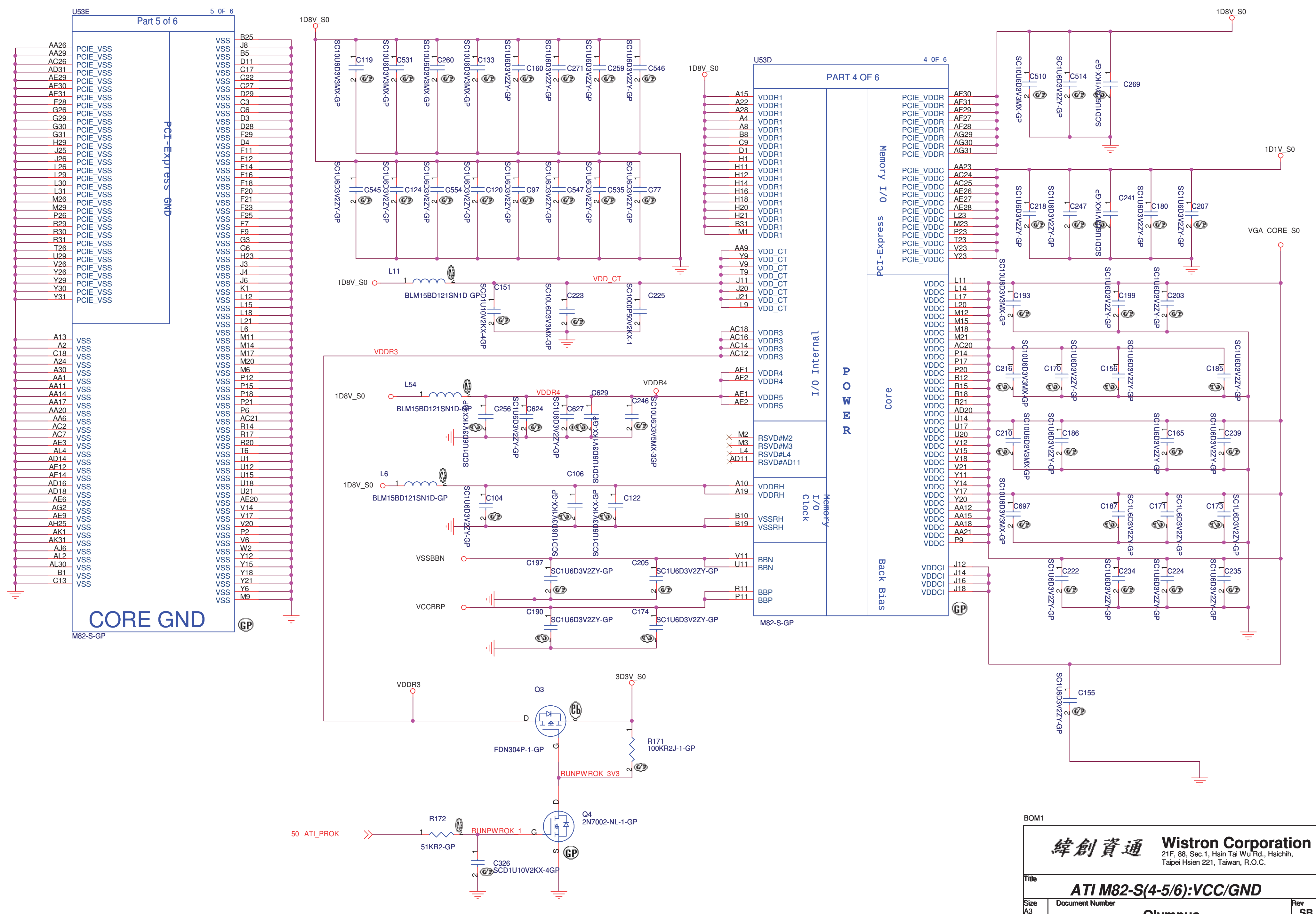
Title: ATI M82-S(1/6):PCIE Interface

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 20 of 53


GPIO2 instand of TP
GPIO6 instand of TP
For VGA_CORE_POWER strapping:
-SB modify
Vout PWRCNTL_0 PWR_1
0.9 1 1
1.0 1 0
0.9 0 1
1.1 0 0
For MEM strapping, Please use below table:
MEM_ID[0.1] Config FBS Vendor
00 16Mx32DDR3 64-bit Hynix
01 16Mx32DDR3 64-bit Qimonda
10 32Mx32GDDR3 Qimonda
11 32Mx32GDDR3 SAMAUNG
Place Vref divider and cap close to asic
P1819B
SRS: 0: -1.25% down spread
1: -1.75% down spread
Pls place these capacitors as close to as U14 MPVDD Pin.
IF HOT PLUG DETECT IS NOT REQUIRED REMOVE ALL THIS LOGIC EXCEPT FOR 100K PULL DOWN
CLOSE TO PIN AK29 (ATI_CRT_HSYNC)
37.5 ohm trace to 150R resistor
50 ohm trace to filter
CLOSE TO M82-S
CLOSE TO M82S
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI M82-S(2/6):CRT/HDMI
Olympus
SB
Wednesday, December 26, 2007
21 of 53

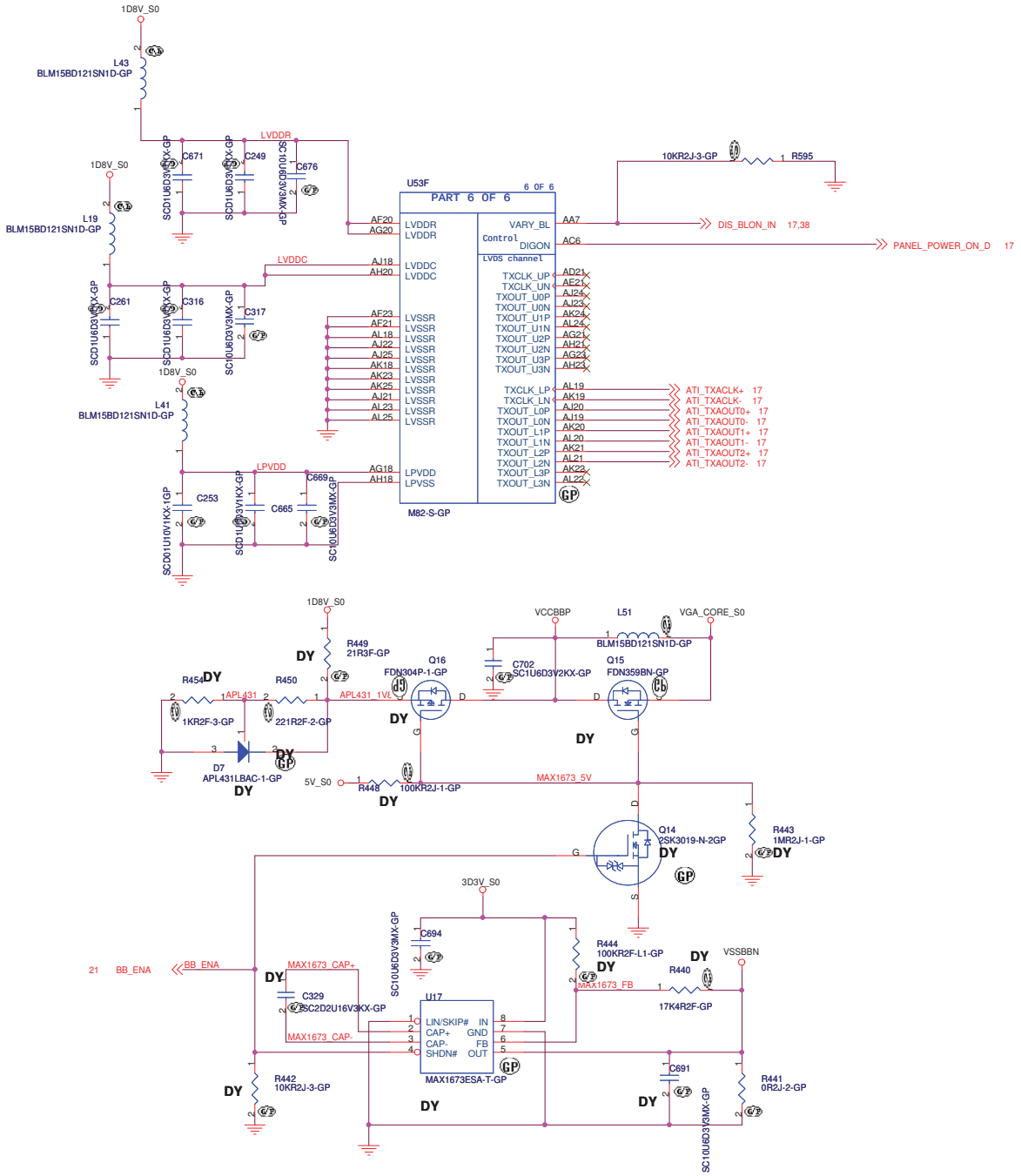

U53C
3 0F 6
Part 3 of 6
MEMORY INTERFACE
M82-S-GP
19 RASA0#
19 RASA1#
19 CASA0#
19 CASA1#
19 WEA0#
19 WEA1#
19 CKEA0
19 CKEA1
19 CSA0_0#
19 CSA1_0#
19 CSA0_1#
19 CSA1_1#
19 CLKA0
19 CLKA0#
19 CLKA1
19 CLKA1#
19 WDQSA[7..0]
19 RDQSA[7..0]
19 DQMA#[7..0]
19 MDA[63..0]
19 MAA[11..0]
19 BA0
19 BA1
19 BA2
MAA12
MDA0 E29 DQ_0
MDA1 E30 DQ_1
MDA2 E31 DQ_2
MDA3 D31 DQ_3
MDA4 C29 DQ_4
MDA5 B29 DQ_5
MDA6 B30 DQ_6
MDA7 A29 DQ_7
MDA8 E26 DQ_8
MDA9 D26 DQ_9
MDA10 E25 DQ_10
MDA11 D25 DQ_11
MDA12 G23 DQ_12
MDA13 G21 DQ_13
MDA14 E21 DQ_14
MDA15 D21 DQ_15
MDA16 C28 DQ_16
MDA17 B28 DQ_17
MDA18 B27 DQ_18
MDA19 A27 DQ_19
MDA20 C25 DQ_20
MDA21 A25 DQ_21
MDA22 C24 DQ_22
MDA23 B24 DQ_23
MDA24 C23 DQ_24
MDA25 B23 DQ_25
MDA26 A23 DQ_26
MDA27 B22 DQ_27
MDA28 C20 DQ_28
MDA29 B20 DQ_29
MDA30 A20 DQ_30
MDA31 C19 DQ_31
MDA32 C8 DQ_32
MDA33 C7 DQ_33
MDA34 B7 DQ_34
MDA35 A7 DQ_35
MDA36 A5 DQ_36
MDA37 C4 DQ_37
MDA38 B4 DQ_38
MDA39 A3 DQ_39
MDA40 G9 DQ_40
MDA41 E9 DQ_41
MDA42 D9 DQ_42
MDA43 G7 DQ_43
MDA44 G5 DQ_44
MDA45 F5 DQ_45
MDA46 G4 DQ_46
MDA47 F4 DQ_47
MDA48 B3 DQ_48
MDA49 B2 DQ_49
MDA50 C2 DQ_50
MDA51 C1 DQ_51
MDA52 E3 DQ_52
MDA53 F3 DQ_53
MDA54 F2 DQ_54
MDA55 F1 DQ_55
MDA56 G2 DQ_56
MDA57 G1 DQ_57
MDA58 H3 DQ_58
MDA59 H2 DQ_59
MDA60 K2 DQ_60
MDA61 L3 DQ_61
MDA62 L2 DQ_62
MDA63 L1 DQ_63
F30 MVREFD
F31 MVREFS
L5 TEST_MCLK
L7 TEST_YCLK
J7 MEMTEST
MA_0 B14 MAA0
MA_1 A14 MAA1
MA_2 B13 MAA2
MA_3 E14 MAA3
MA_4 B17 MAA4
MA_5 A17 MAA5
MA_6 C15 MAA6
MA_7 G16 MAA7
MA_8 E16 MAA8
MA_9 C14 MAA9
MA_10 A12 MAA10
MA_11 B12 MAA11
MA_BA0 C12 BA0
MA_BA1 D14 BA1
MA_A12 B15 MAA12
MA_BA2 G14 BA2
DQMB_0 D30 DQMA#0
DQMB_1 G25 DQMA#1
DQMB_2 C26 DQMA#2
DQMB_3 C21 DQMA#3
DQMB_4 C5 DQMA#4
DQMB_5 D6 DQMA#5
DQMB_6 D2 DQMA#6
DQMB_7 K3 DQMA#7
read strobe
QS_0 C30 RDQSA0
QS_1 D23 RDQSA1
QS_2 B26 RDQSA2
QS_3 B21 RDQSA3
QS_4 B6 RDQSA4
QS_5 E7 RDQSA5
QS_6 E2 RDQSA6
QS_7 J2 RDQSA7
write strobe
QS_0# C31 WDQSA0
QS_1# E23 WDQSA1
QS_2# A26 WDQSA2
QS_3# A21 WDQSA3
QS_4# A6 WDQSA4
QS_5# D7 WDQSA5
QS_6# E1 WDQSA6
QS_7# J1 WDQSA7
ODT0 E20 ODTA0
ODT1 C11 ODTA1
TP76 TPAD30
TP77 TPAD30
CLK0 A18 CLKA0
CLK1 A11 CLKA1
CLK0# B18 CLKA0#
CLK1# B11 CLKA1#
RAS0# G20 RASA0#
RAS1# D12 RASA1#
CAS0# D20 CASA0#
CAS1# E12 CASA1#
CS0B_0 E18 CSA0_0#
CS0B_1 G18 CSA0_1#
CS1B_0 G11 CSA1_0#
CS1B_1 E11 CSA1_1#
CKE0 D18 CKEA0
CKE1 G12 CKEA1
WE0# D16 WEA0#
WE1# C10 WEA1#
DRAM_RST# J5
MEM_RST 19
R82 1 4K7R2F-GP 1D8V_S0
FOR DUAL RANK CONNECTIONS
USE THE CSxB_1 CHIP SELECT PINS
1D8V_S0
R381 40D2R2F-GP
R383 100R2F-L1-GP-U
C564 SCD1U10V2KX-4GP
MVREFD
R374 40D2R2F-GP
MVREFS
R378 100R2F-L1-GP-U
C555 SCD1U10V2KX-4GP
TEST_MCLK
TEST_YCLK
MEMTEST
R84 4K7R2F-GP
R83 4K7R2F-GP
R80 243R3F-GP
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
DIVIDER RESISTORS | DDR2 | DDR3
MVREF TO 1.8V | 100R | 40.2R
MVREF TO GND | 100R | 100R
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M82-S(3/6):Memory Interface
Size A3
Document Number
Olympus
Rev SB
Date: Wednesday, December 26, 2007
Sheet 22 of 53



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

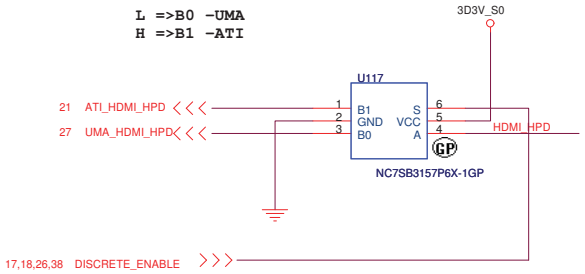
Title	ATI M82-S(4-5/6):VCC/GND		
Size A3	Document Number: Olympus		Rev SB
Date: Wednesday, December 26, 2007	Sheet 23 of 53		

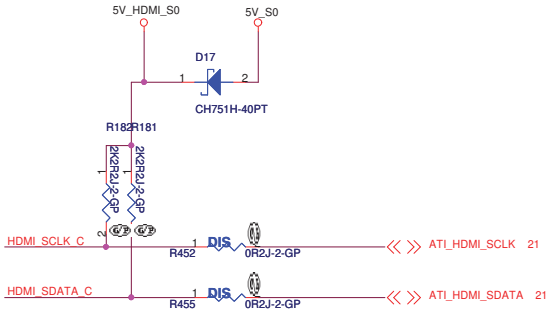


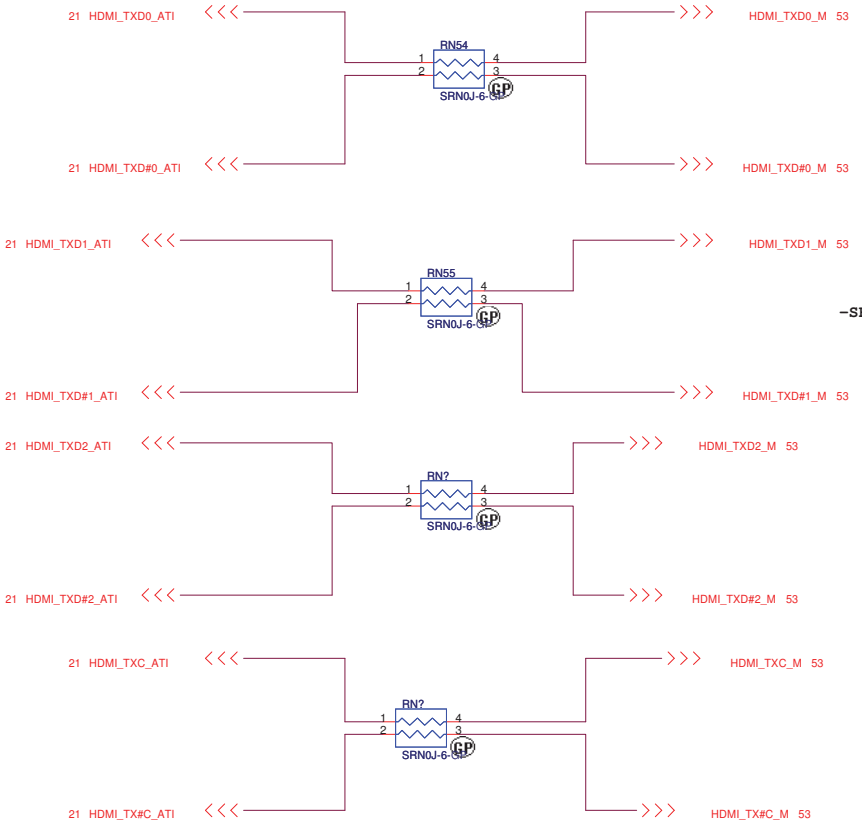
BOM1

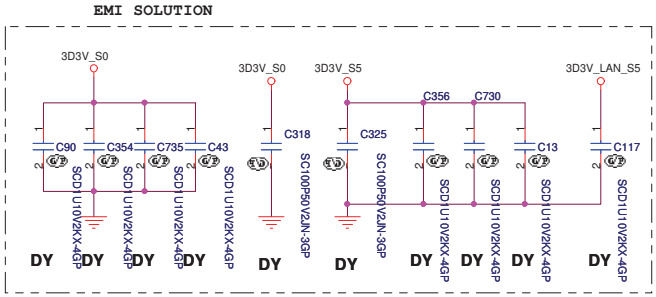
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ATI M82-S(6/6):LVDS		
Size: Custom	Document Number: Olympus	Rev: SB
Date: Wednesday, December 26, 2007	Sheet 24 of 53	

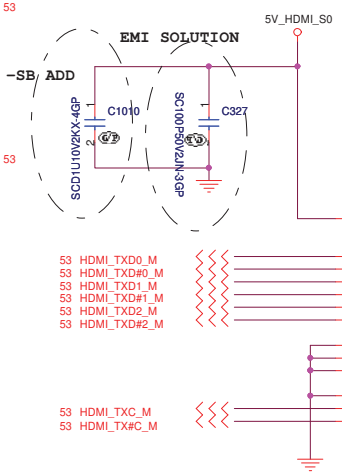
L =>B0 -UMA
H =>B1 -ATI







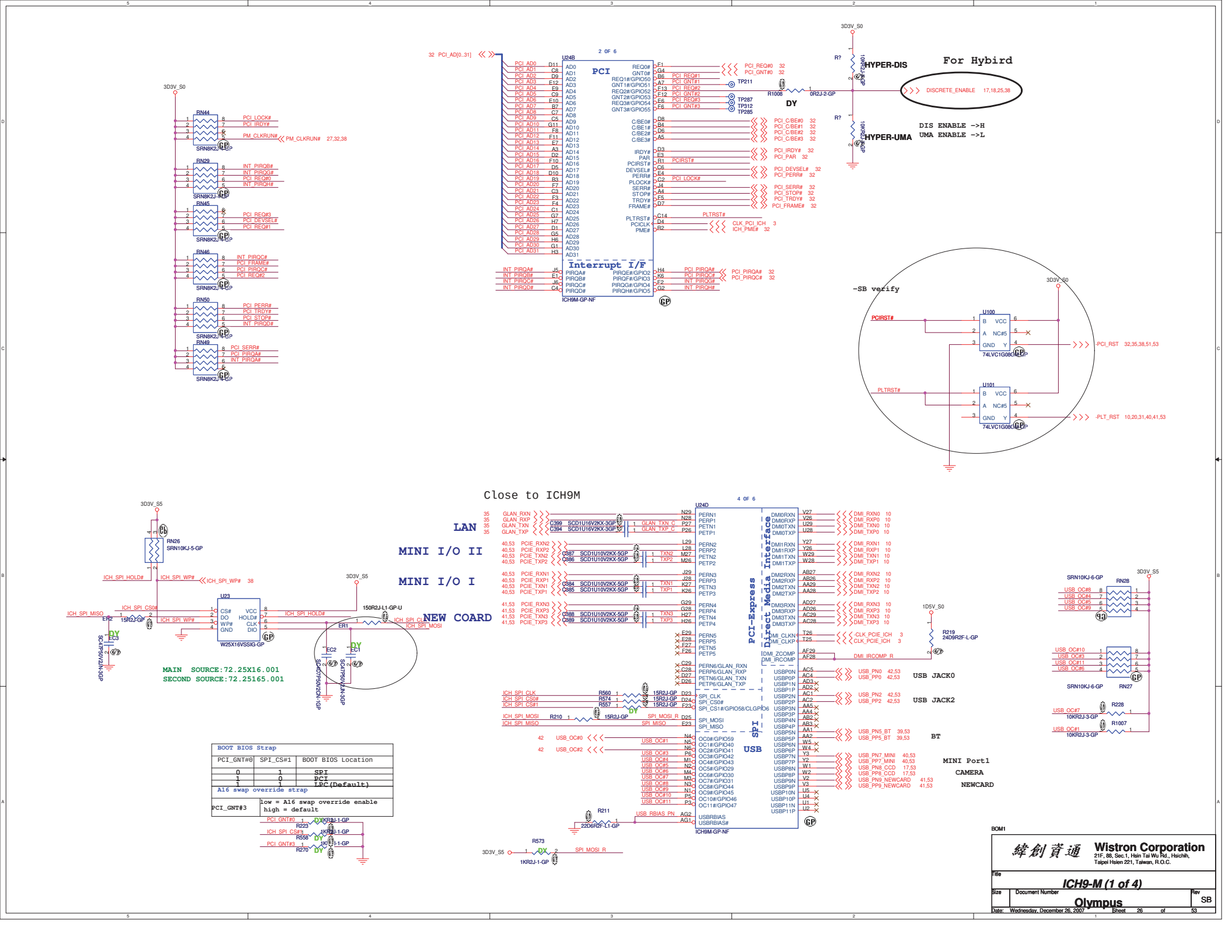




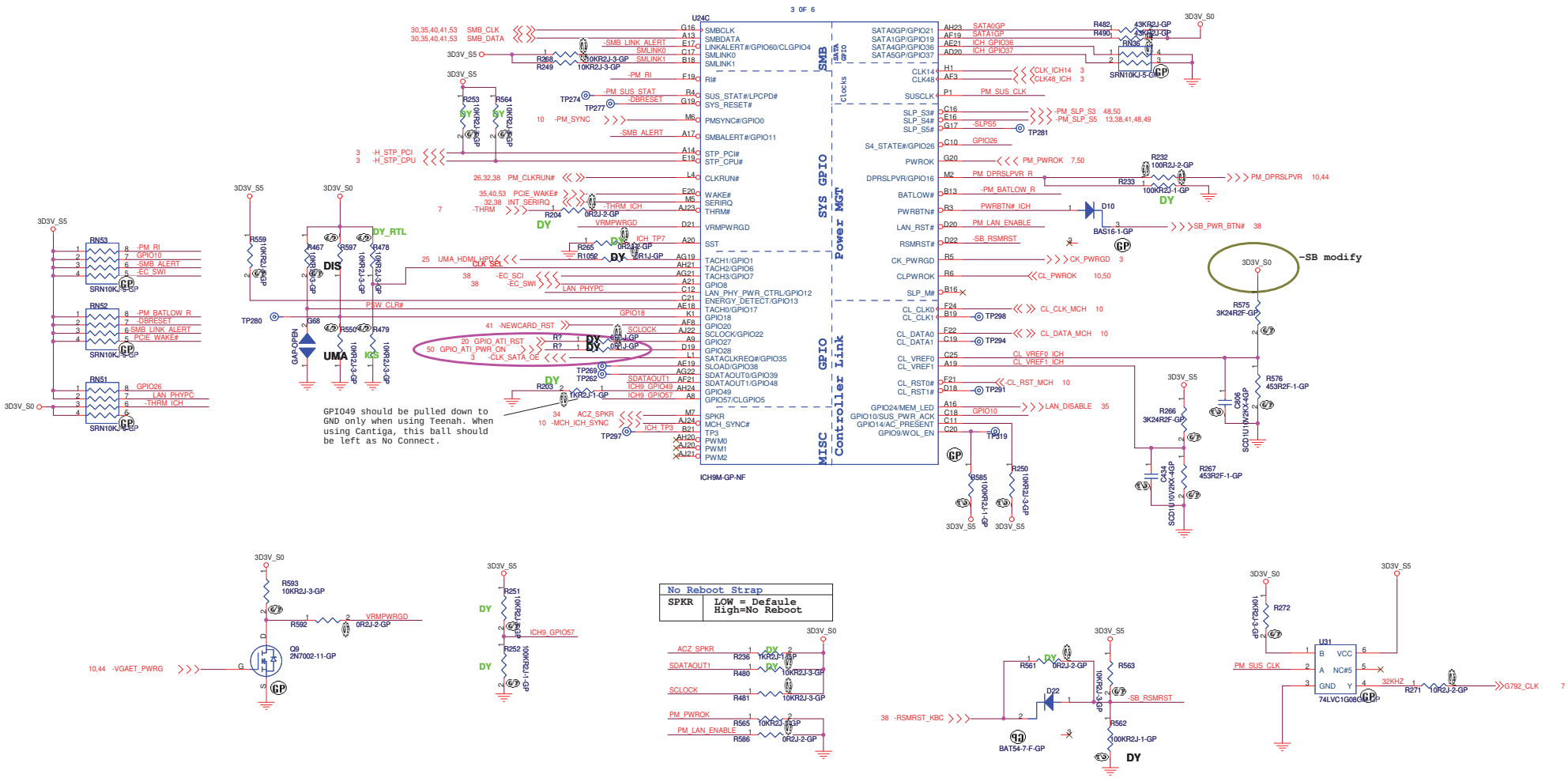
HDMI CONN

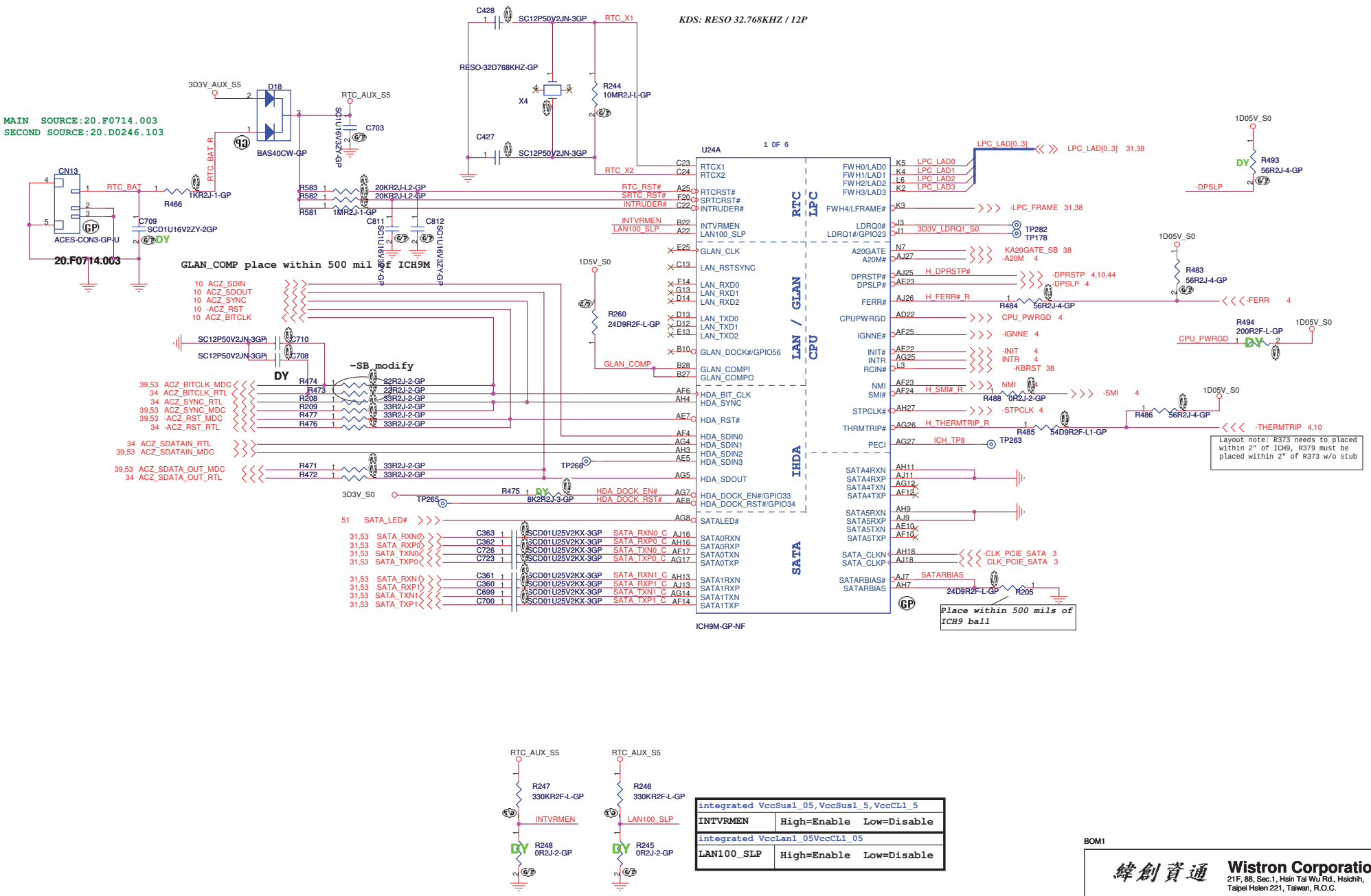
BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI CONN	
Size A3	Document Number Olympus	Rev SB
Date: Wednesday, December 26, 2007	Sheet 25 of 53	



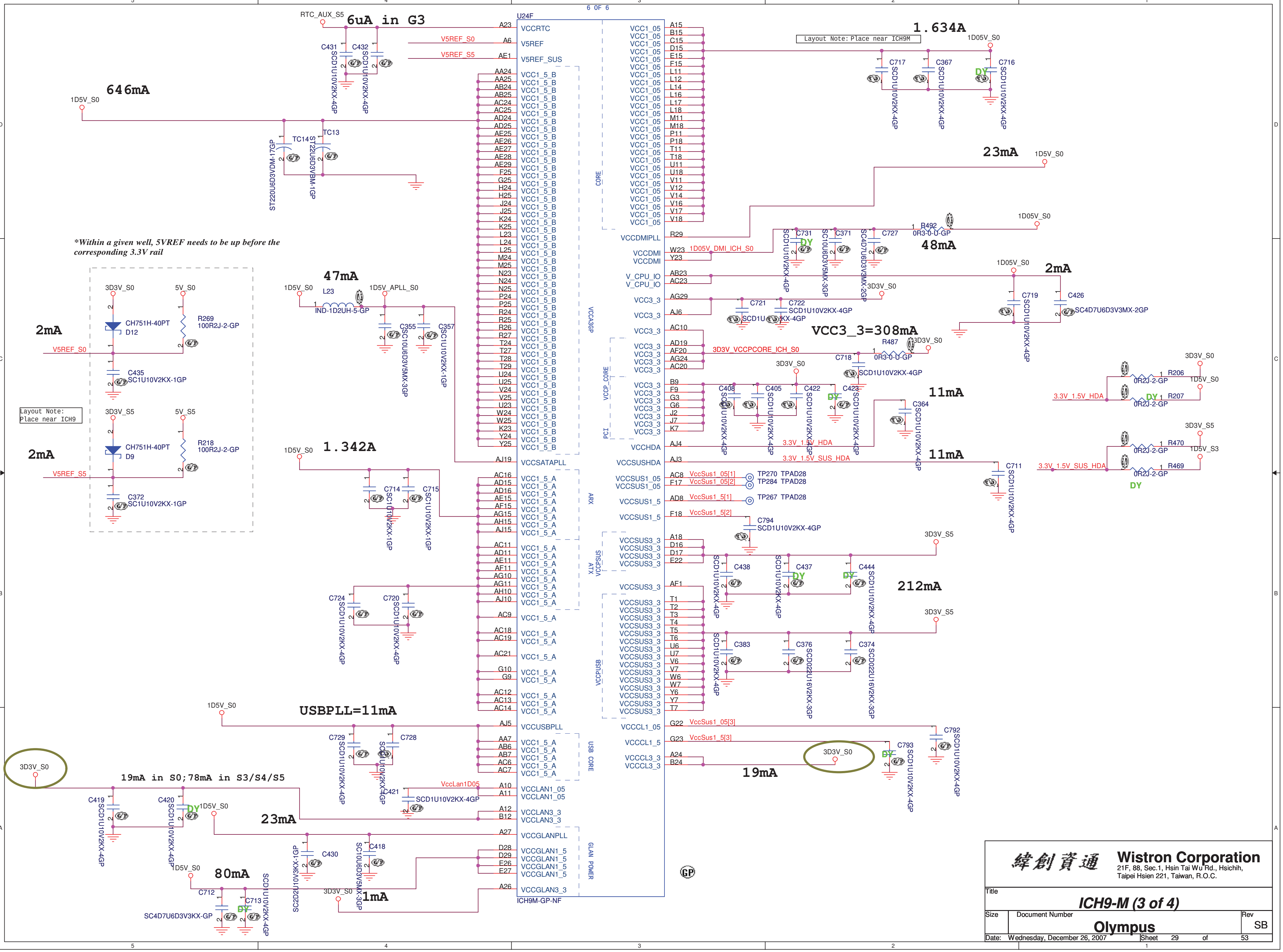
Wistron Corporation			
緯創資通	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	ICH9-M (1 of 4)		
Size	Document Number		Rev
	Olympus		SB
Date: Wednesday, December 26, 2007	Sheet 26 of 53		

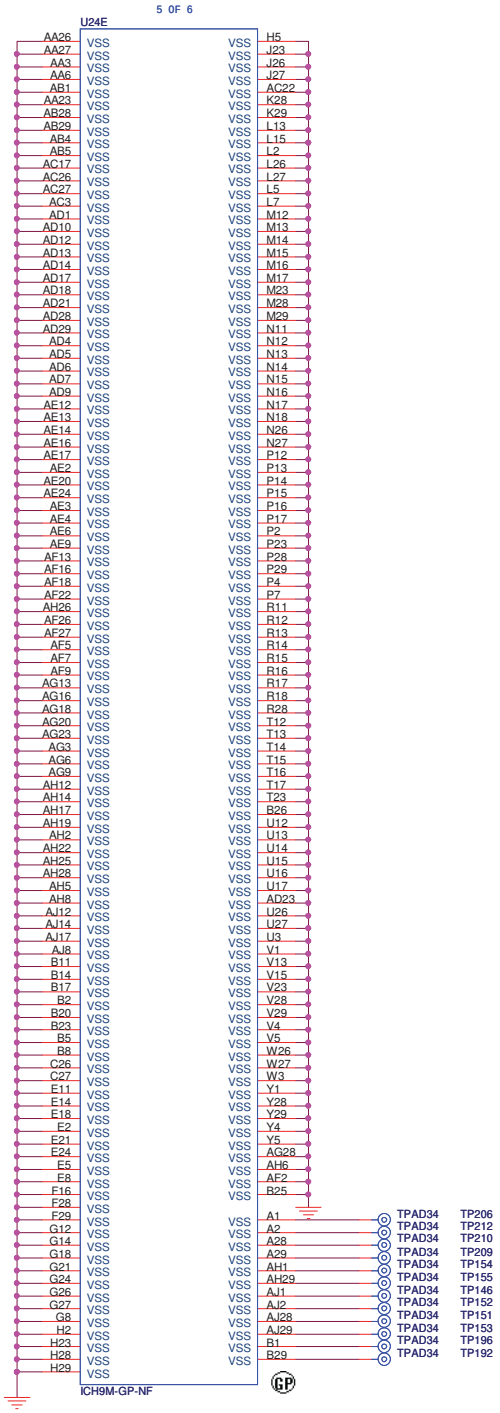

U24C
3 OF 6
ICH9M-GP-NF
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO29
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
-SB modify
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (2 of 4)
Olympus
SB
Wednesday, December 26, 2007
27
53

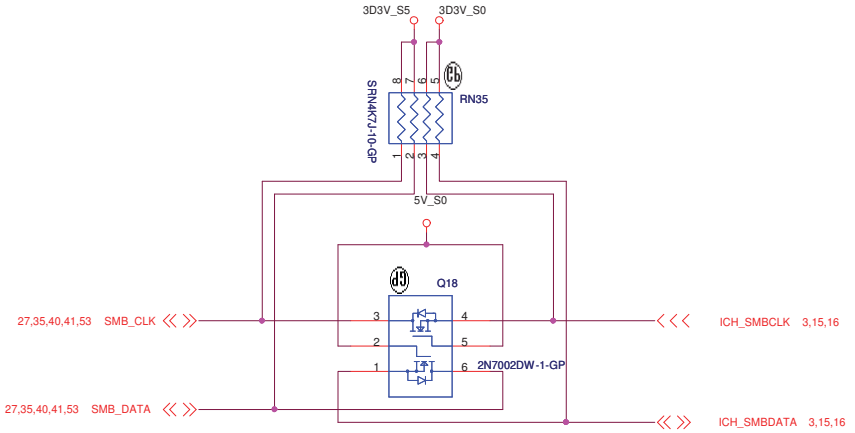


BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ICH9-M (1 of 4)*
Size / Document Number	**Olympus**
Rev	SB
Date: Wednesday, December 26, 2007	Sheet 28 of 53


6 OF 6
U24F
ICH9M-GP-NF
6uA in G3
646mA
1.634A
23mA
48mA
2mA
47mA
VCC3_3=308mA
11mA
1.342A
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
19mA
23mA
80mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9M
Layout Note: Place near ICH9
RTC_AUX_S5
1D5V_S0
1D05V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
1D5V_APLL_S0
V5REF_S0
V5REF_S5
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B
VCC1_05
VCCDMIPLL
VCCDMI
V_CPU_IO
VCC3_3
VCCSATAPLL
VCC1_5_A
VCCHDA
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCUSBPLL
VCCCL1_05
VCCCL1_5
VCCCL3_3
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
1D05V_DMI_ICH_S0
3D3V_VCCPCORE_ICH_S0
3.3V_1.5V_HDA
3.3V_1.5V_SUS_HDA
VccSus1_05[1]
VccSus1_05[2]
VccSus1_5[1]
VccSus1_5[2]
VccSus1_05[3]
VccSus1_5[3]
VccLan1D05
TP270 TPAD28
TP284 TPAD28
TP267 TPAD28
CH751H-40PT D12
CH751H-40PT D9
R269 100R2J-2-GP
R218 100R2J-2-GP
C435 SC1U10V2KX-1GP
C372 SC1U10V2KX-1GP
L23 IND-1D2UH-5-GP
R492 0R3-0-U-GP
R487 0R3-0-U-GP
R206 0R2J-2-GP
R207 0R2J-2-GP
R470 0R2J-2-GP
R469 0R2J-2-GP
DY
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)
Size
Document Number
Olympus
Rev
SB
Date: Wednesday, December 26, 2007
Sheet 29 of 53



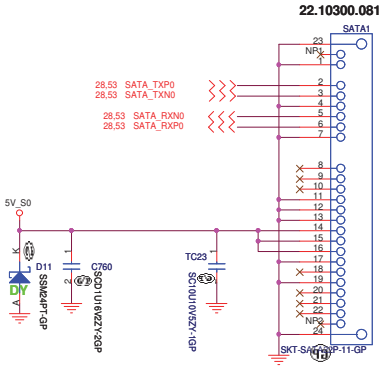


Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

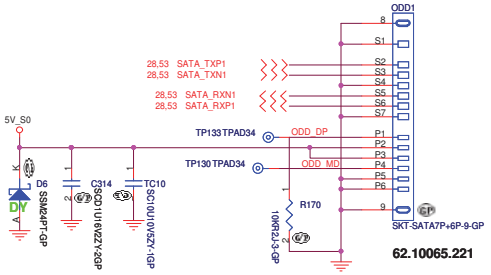
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ICH9-M (4 of 4)***	
Size	Document Number **Olympus**	Rev SB
Date: Wednesday, December 26, 2007	Sheet 30 of 53	

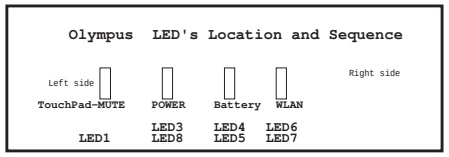
SATA HD Connector



MAIN SOURCE:22.10300.081
SECOND SOURCE:20.80919.022

ODD Connector



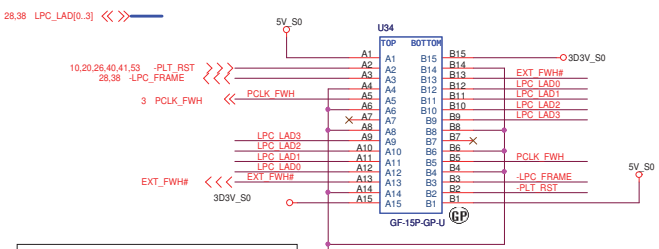


GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

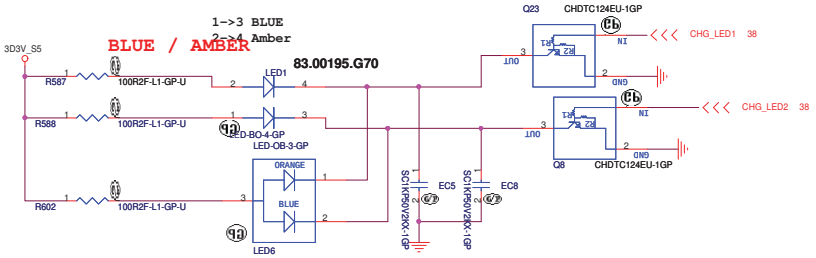
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

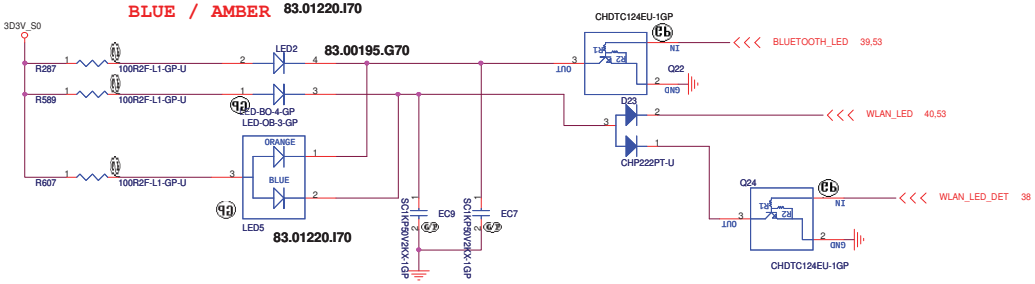
(BOTTOM VIEW)

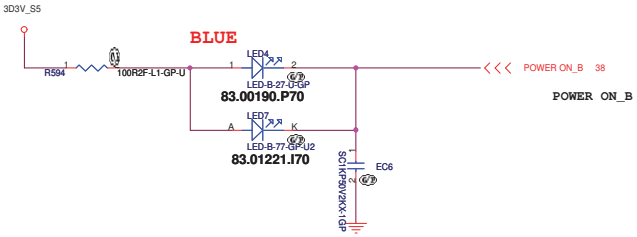


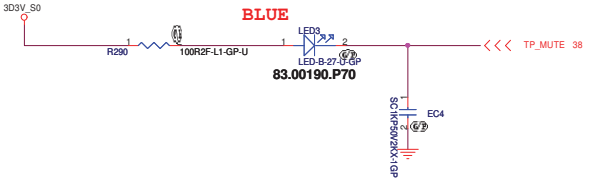
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

1->3 BLUE
2->4 Amber









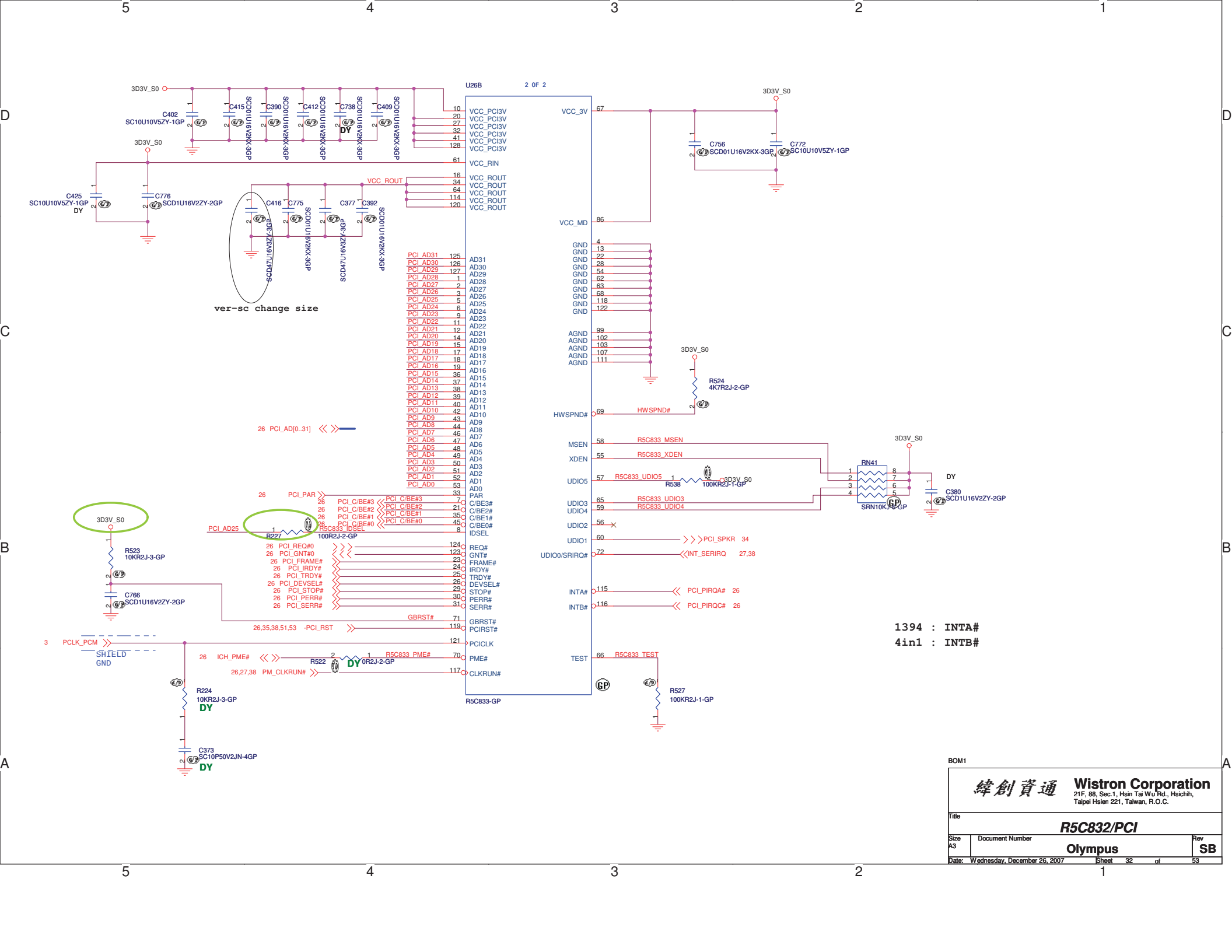
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

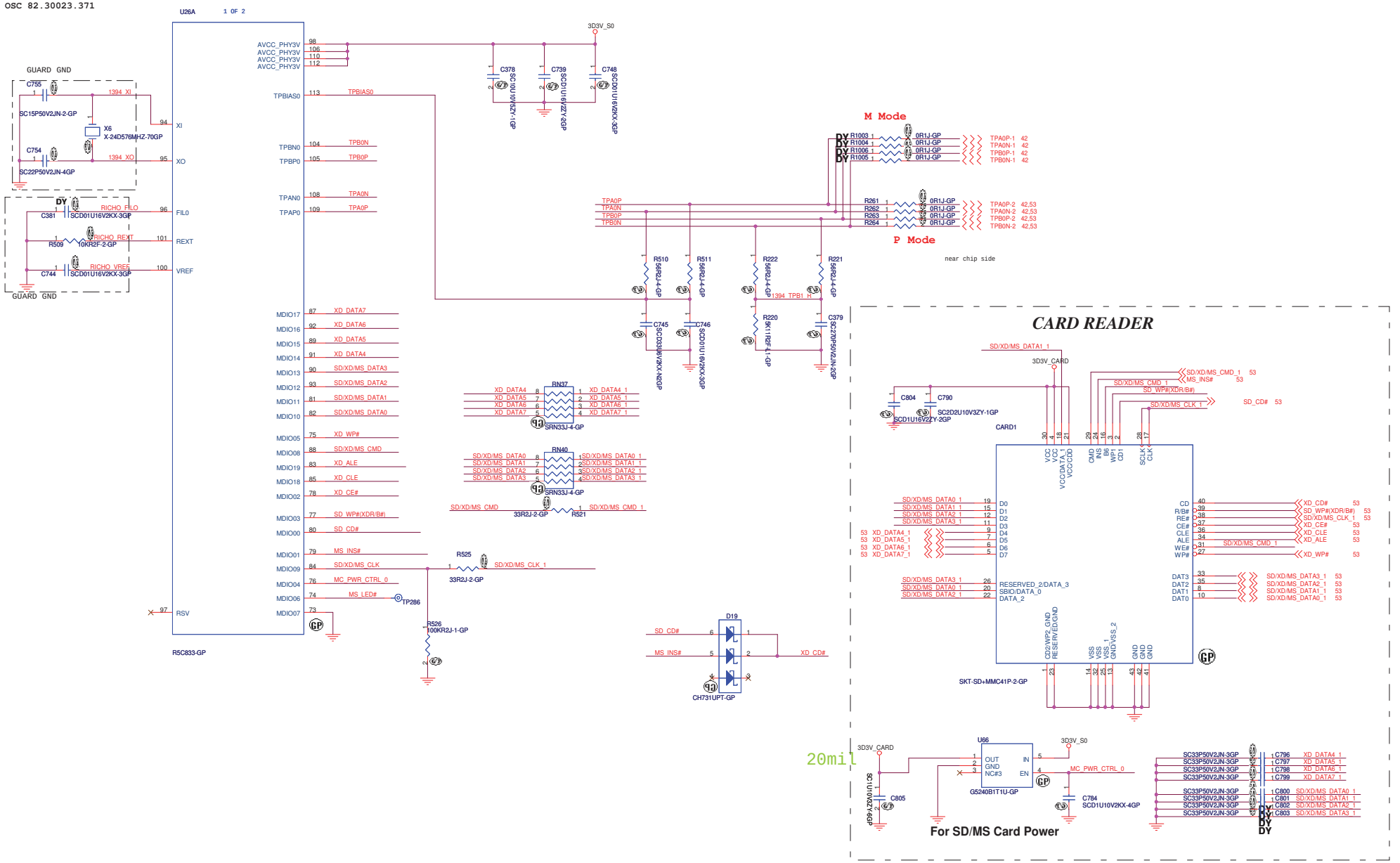
Title: HDD/CDROM/DEBUG / LEDS

Size	Document Number	Rev
	Olympus	SB

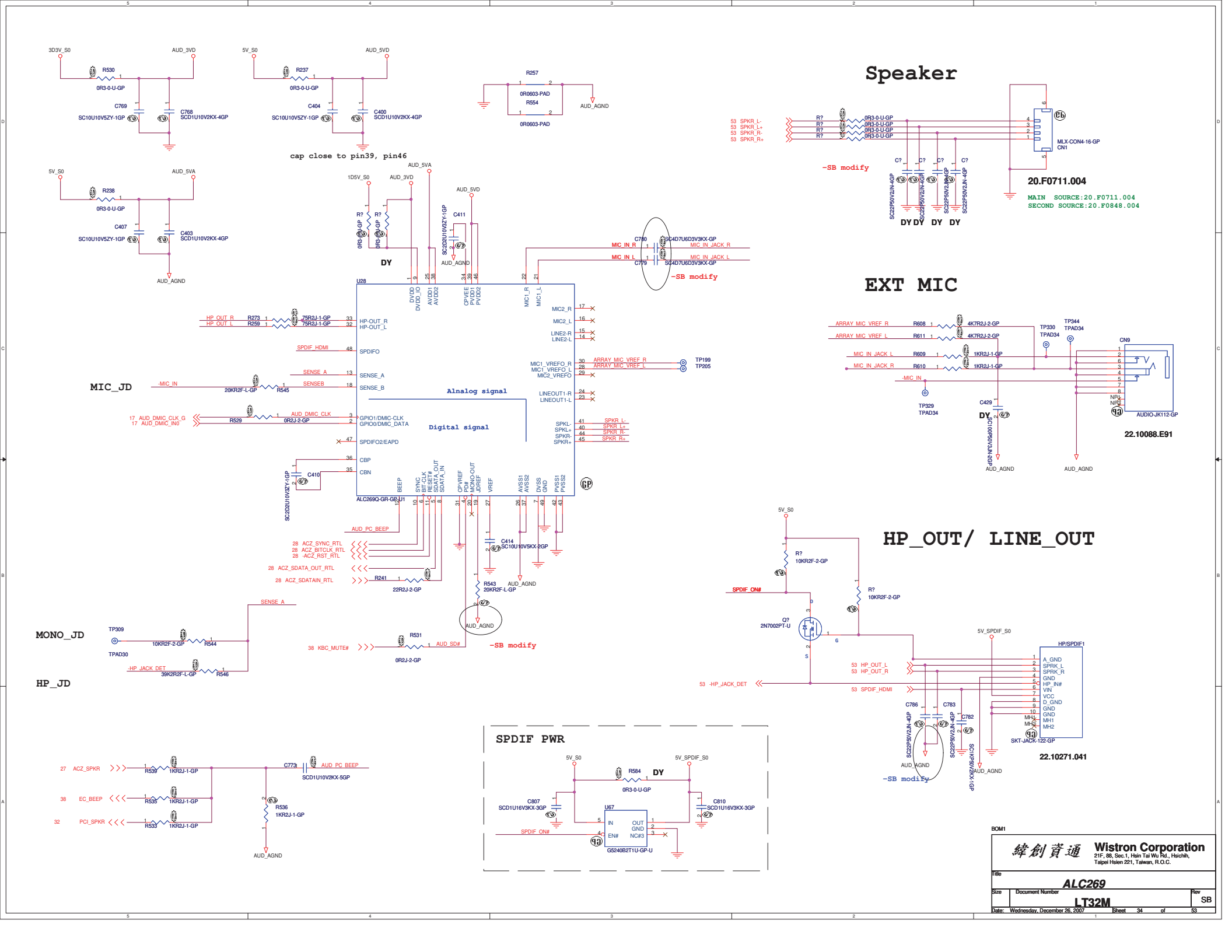
Date: Wednesday, December 26, 2007 Sheet 31 of 53

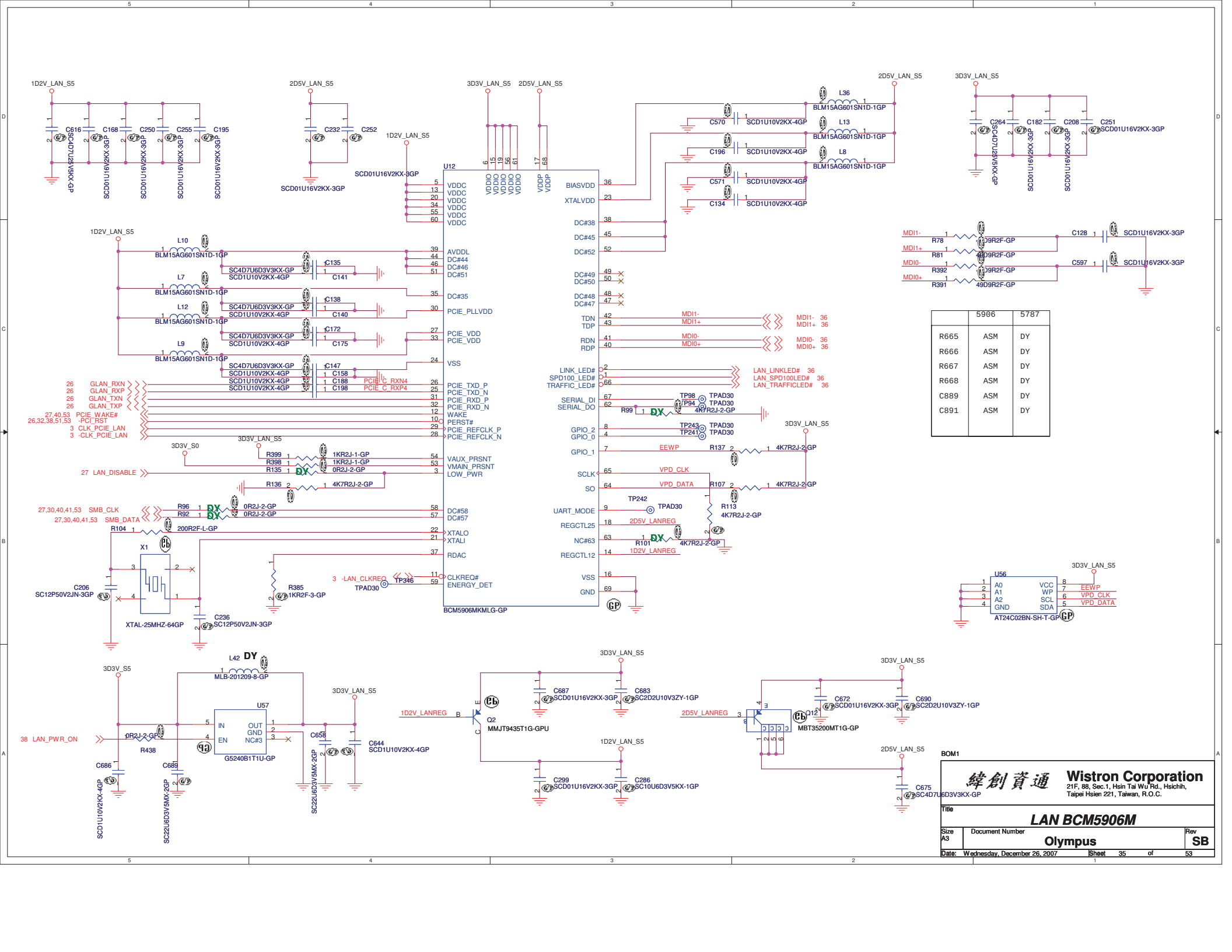

U26B
2 OF 2
R5C833-GP
ver-sc change size
1394 : INTA#
4in1 : INTB#
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
R5C832/PCI
Size
A3
Document Number
Olympus
Rev
SB
Date: Wednesday, December 26, 2007
Sheet 32 of 53

OSC 82.30023.371



BOM1			
緯創資通	Wistron Corporation		
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	R5C832/IEEE1394/SD/BT		
Size: C	Document Number: Olympus	Rev: SB	
Date: Wednesday, December 26, 2007	Sheet 33 of 53		

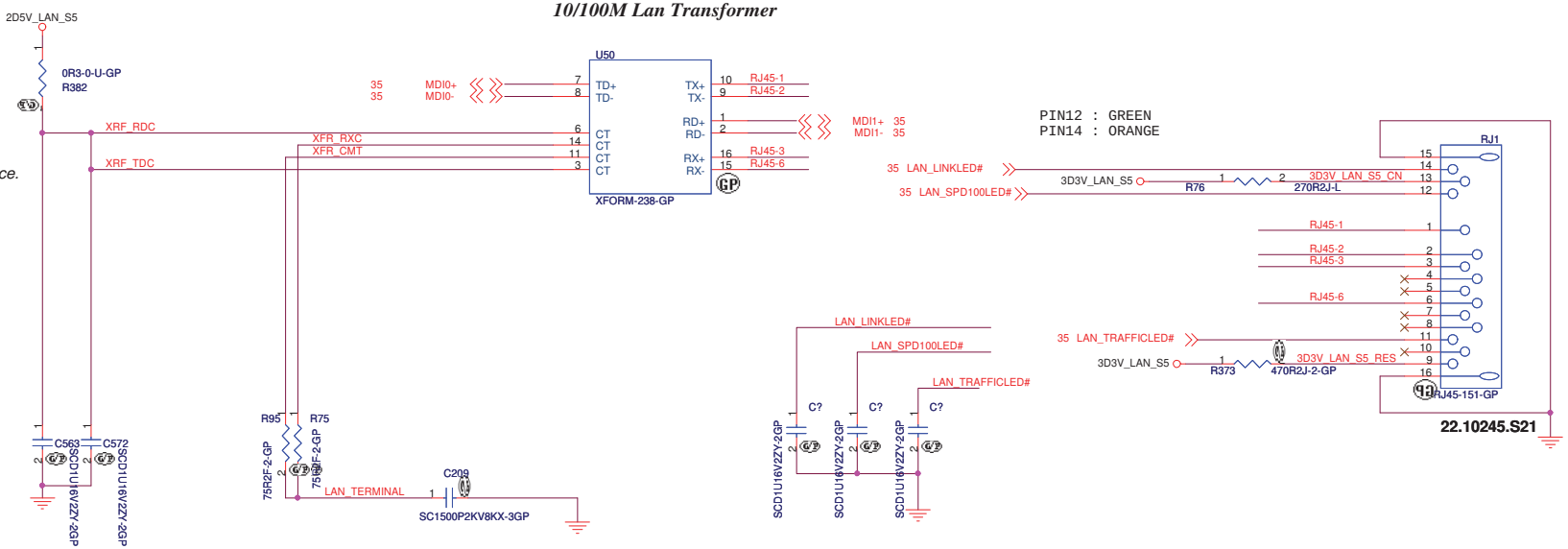

Speaker
EXT MIC
HP_OUT/ LINE_OUT
MIC_JD
HP_JD
MONO_JD
SPDIF PWR
cap close to pin39, pin46
Alnalog signal
Digital signal
-SB modify
DY
20.F0711.004
MAIN SOURCE:20.F0711.004
SECOND SOURCE:20.F0848.004
22.10088.E91
22.10271.041
ALC269Q-GR-GR-U1
G5240B2T1U-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ALC269
LT32M
Wednesday, December 26, 2007



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

10/100M Lan Transformer

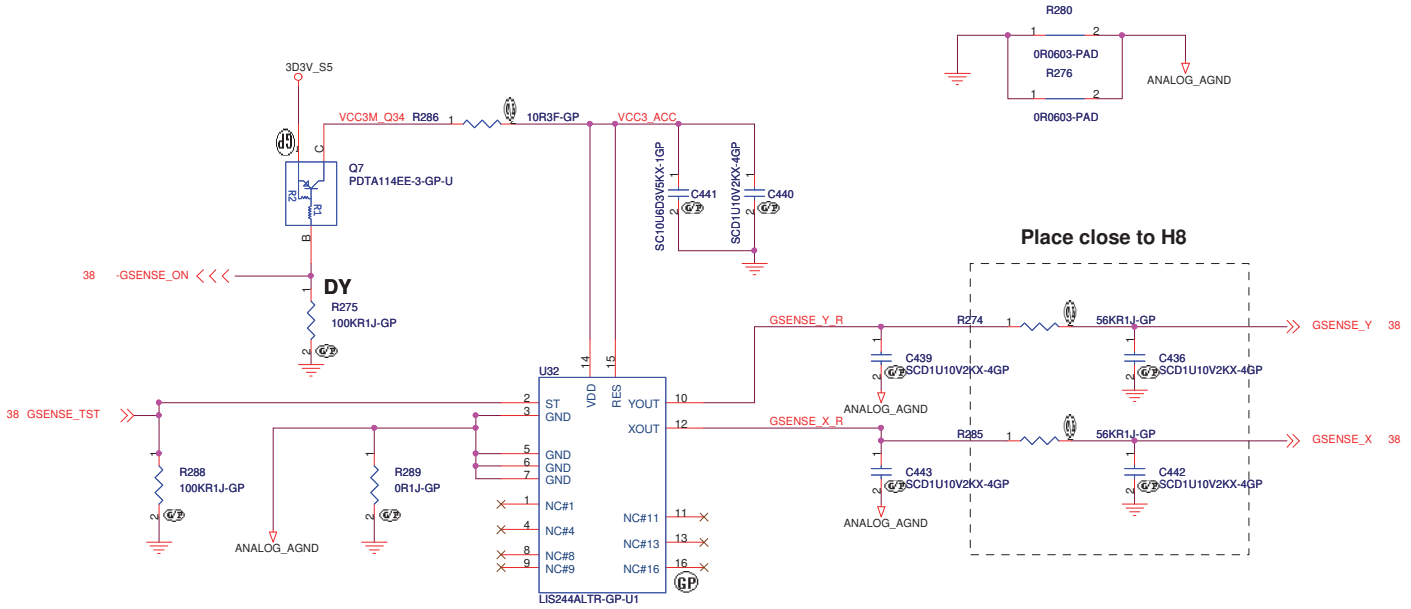
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



CLOSE TO TRANSFORMER

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LAN connector/NEW CARD/SIM***
Size: A3	Document Number: **Olympus**
Rev:	**SB**
Date: Wednesday, December 26, 2007	Sheet 36 of 53



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

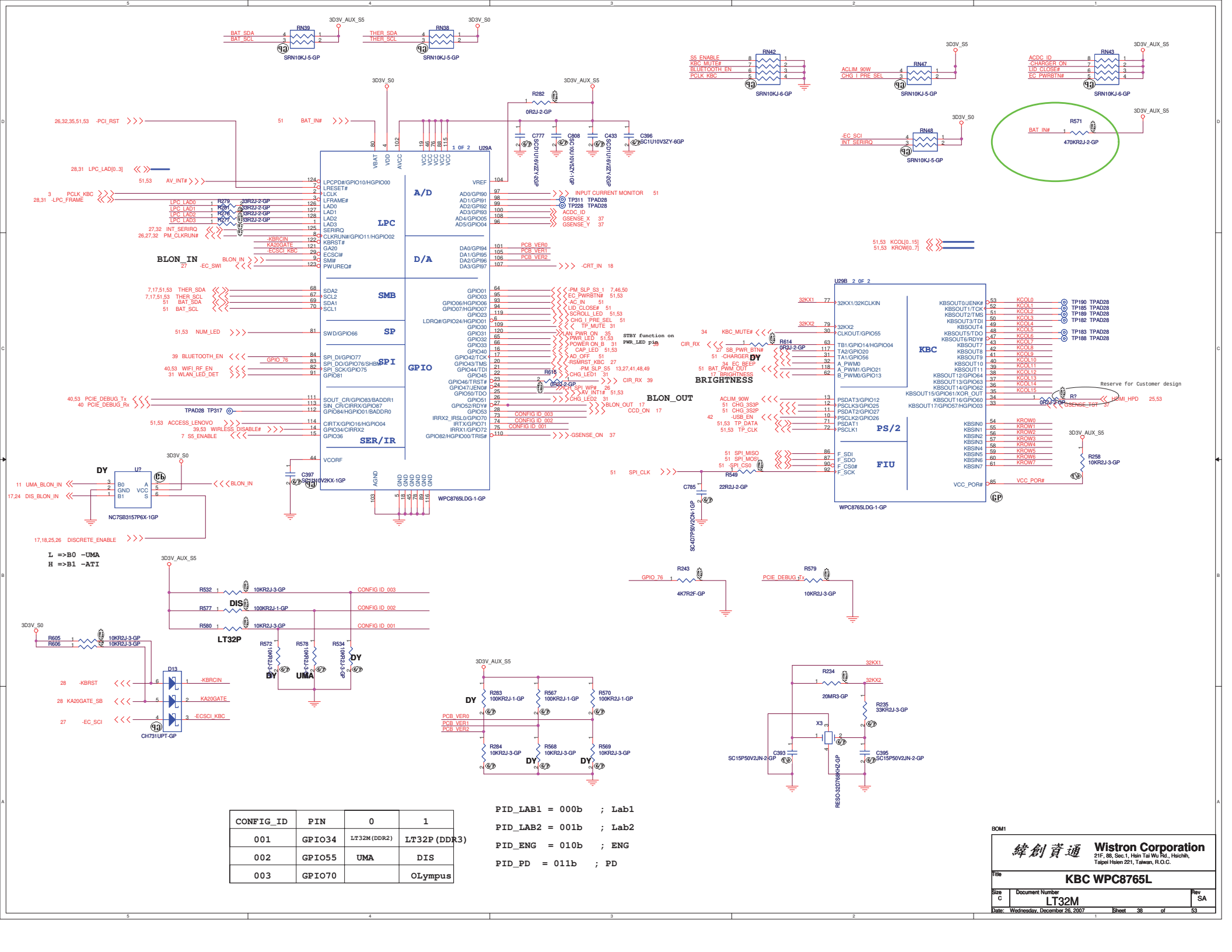
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-SENSOR**

Size: A3 | Document Number: **Olympus** | Rev: **SB**

Date: Wednesday, December 26, 2007 | Sheet 37 of 53



CONFIG_ID	PIN	0	1
001	GPIO34	LT32M(DDR2)	LT32P(DDR3)
002	GPIO55	UMA	DIS
003	GPIO70		OLympus

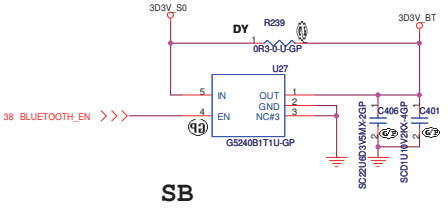
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC WPC8765L

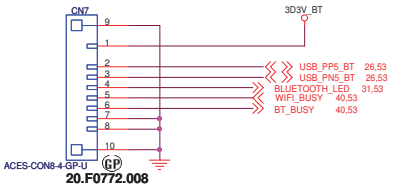
Size	Document Number	Rev
C	LT32M	SA

Date: Wednesday, December 26, 2007 Sheet 38 of 53



SB

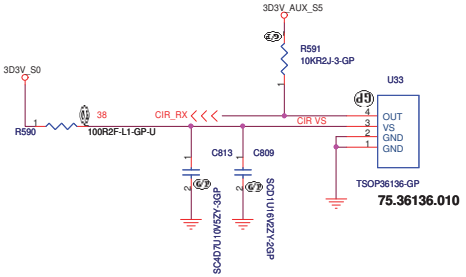
BT CONNECTOR



20.F0772.008

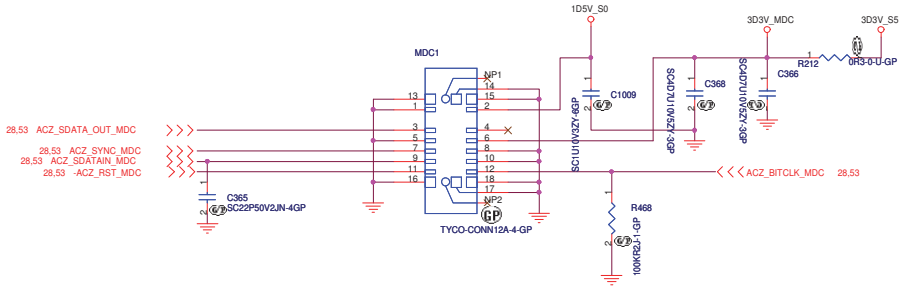
MAIN SOURCE:20.F0772.008
SECOND SOURCE:20.F0983.008

CIR



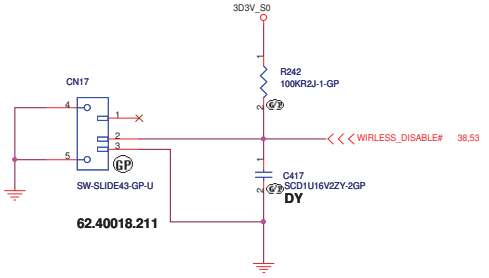
75.36136.010

MDC 1.5 CONN



MAIN SOURCE:20.F0677.012
SECOND SOURCE:20.F0676.012

WIRELESS SWITCH



62.40018.211

BOM1

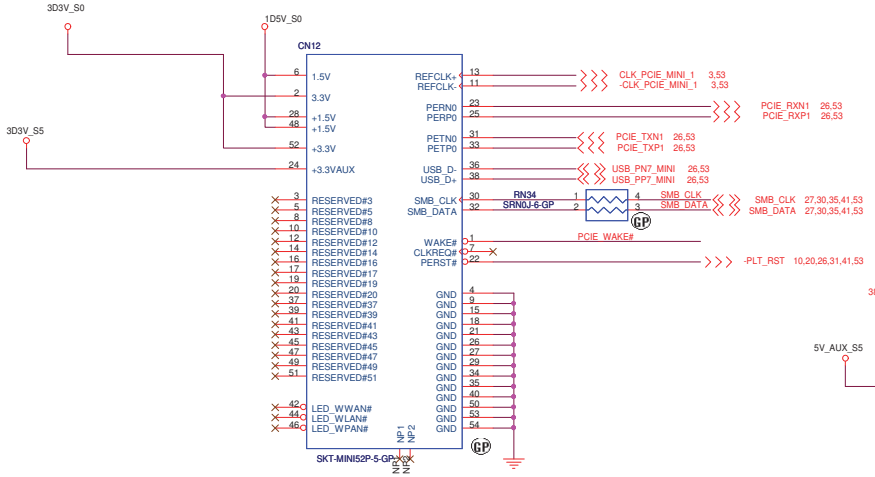
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Module_Blue Tooth/Modem/CIR	
Size	Document Number: Olympus	Rev: SB
Date: Wednesday, December 26, 2007	Sheet 39 of 53	

Mini PCI-E Connector

Only port-1 support USB

For Robson

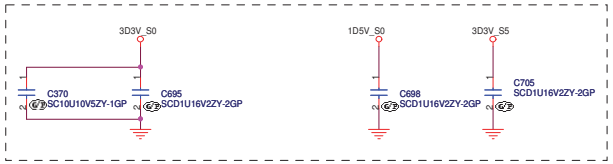
Port-1 High



20.F0832.052

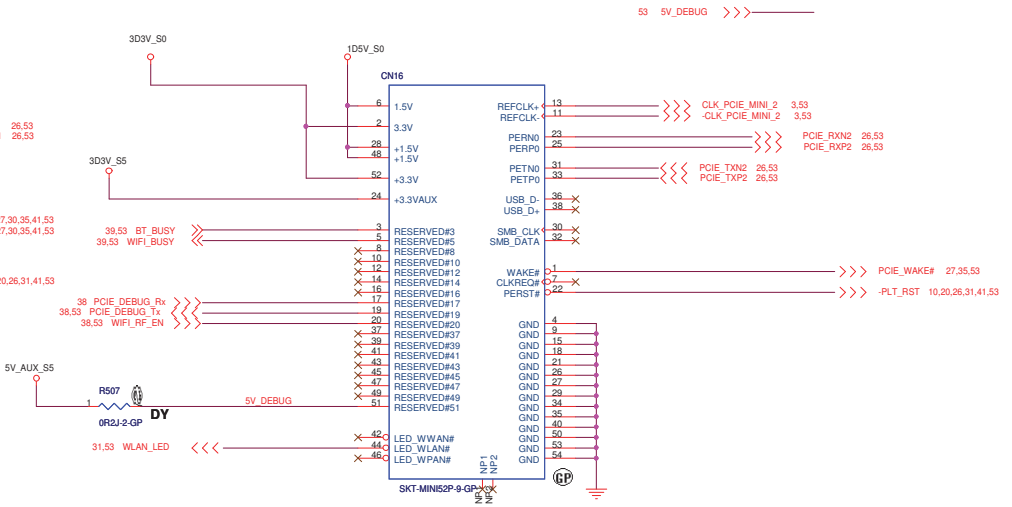
MAIN SOURCE:20.F0832.052

SECOND SOURCE:20.F1107.052



Mini PCI-E Connector

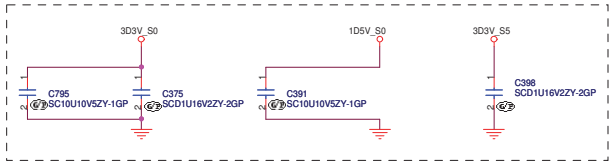
Port-2 low



62.10043.411

MAIN SOURCE:62.10043.411

SECOND SOURCE:20.F1084.052



BOM1

緯創資通 **Wistron Corporation**

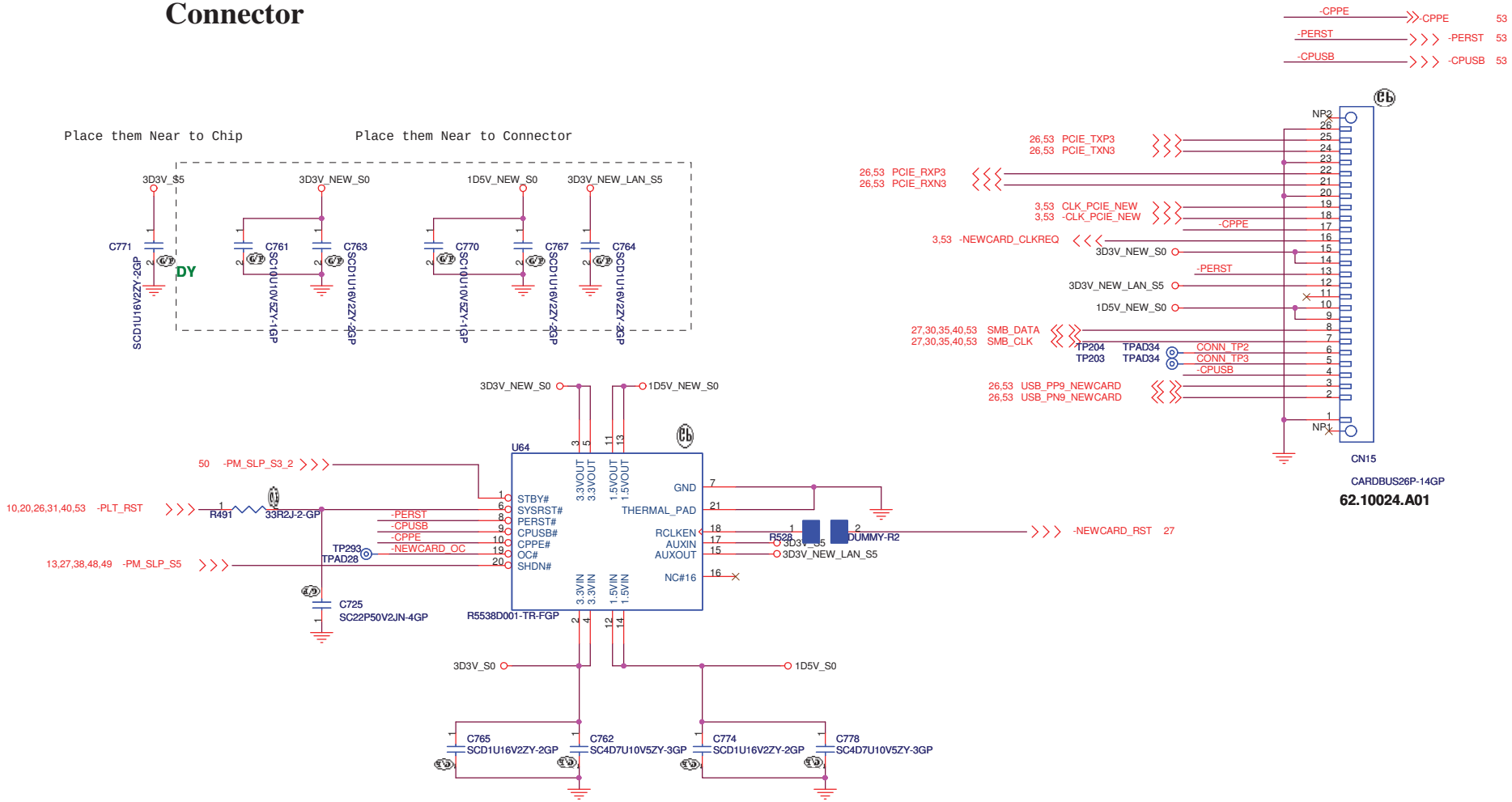
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD CONN .**

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 40 of 53

NEWCARD
Connector



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Module_NewCard

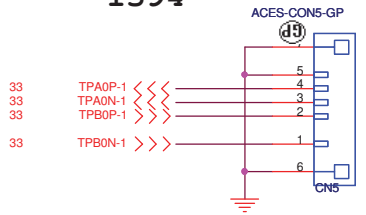
Size | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 41 of 53

*USB * 2 PORT*

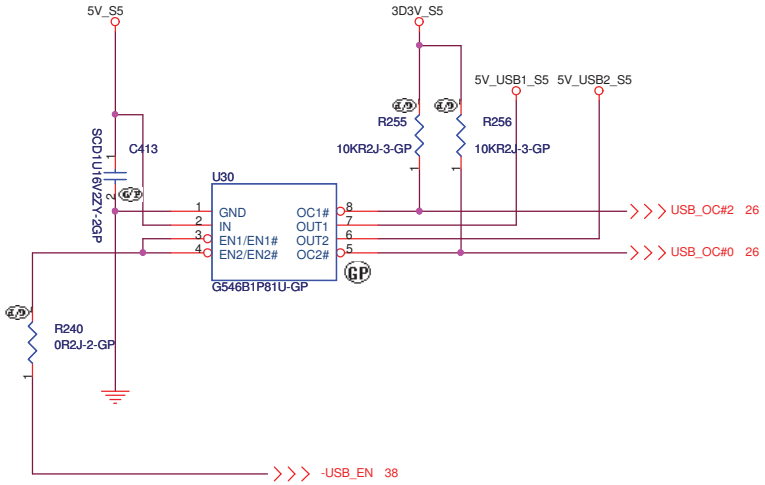
Low -End USB BOARD

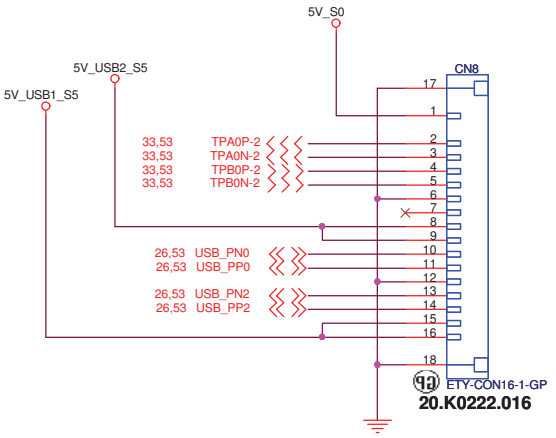
1394



MAIN SOURCE:20.k0196.005
SECOND SOURCE:20.K0212.008

USB*2 + 1394





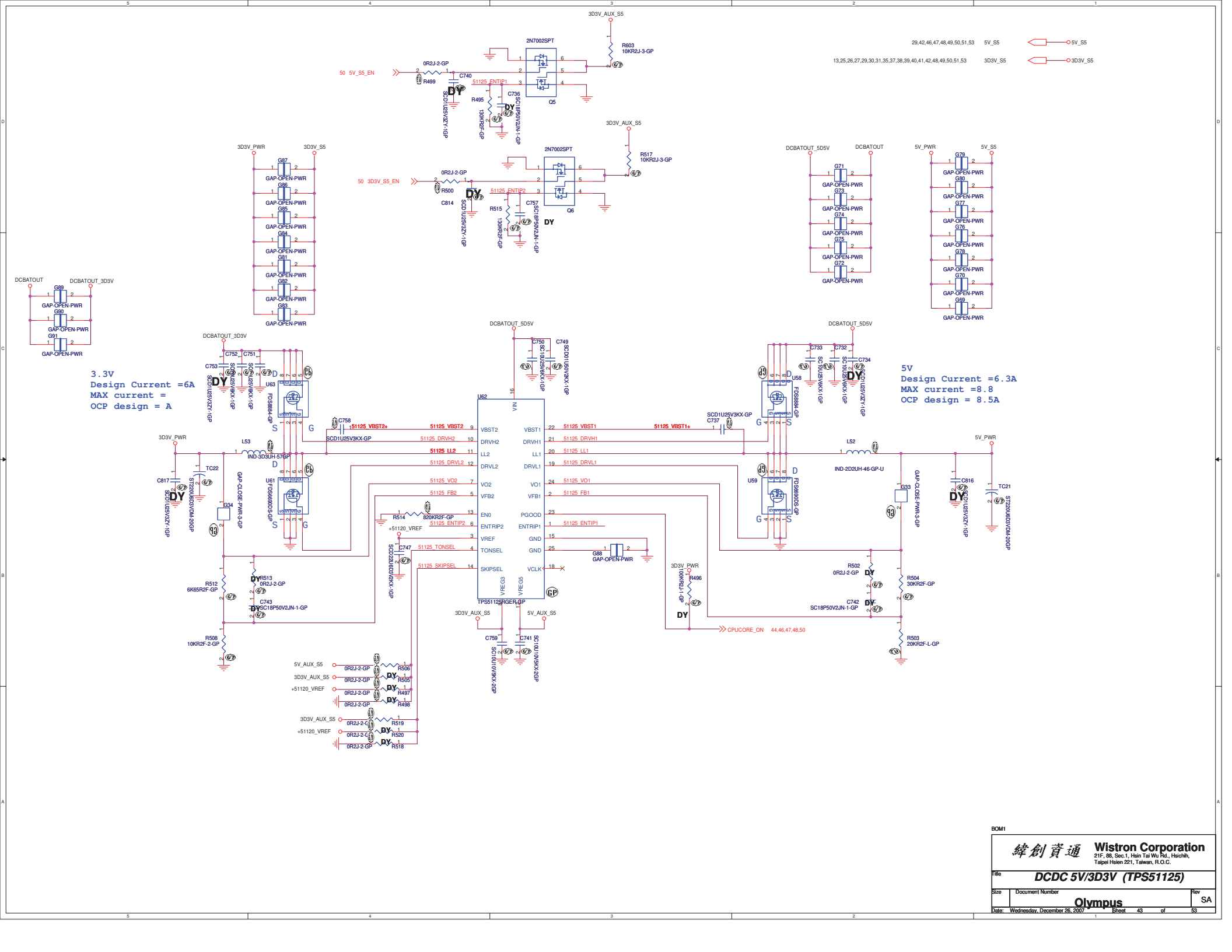
BOM1

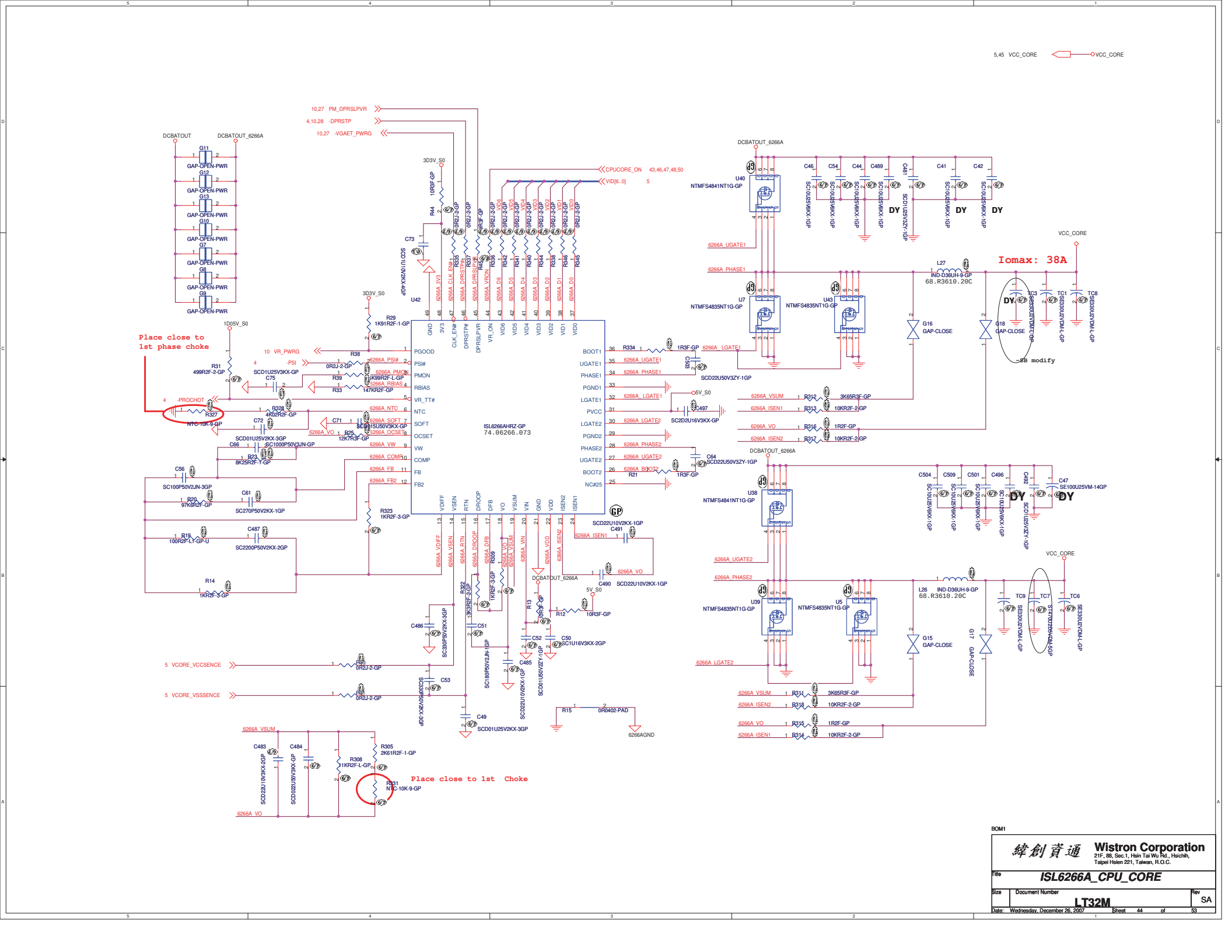
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

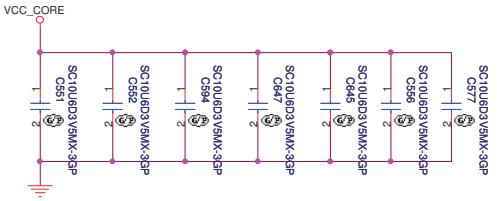
Title: ***USB I/O & 1394 CNN***

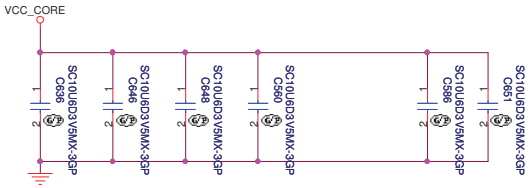
Size	Document Number	Rev
B	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 42 of 53

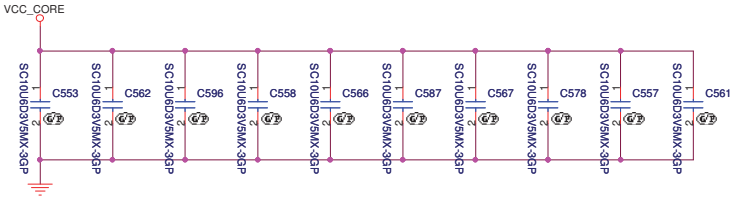

3.3V
Design Current =6A
MAX current =
OCP design = A
5V
Design Current =6.3A
MAX current =8.8
OCP design = 8.5A
U62
TPS51125RGER-GP
U61
FDS6680DS-GP
U63
FDS6894-GP
U58
FDS6894-GP
U59
FDS6680DS-GP
Q5
2N7002SPT
Q6
2N7002SPT
L53
IND-3D3UH-57GP
L52
IND-2D2UH-46-GP-U
3D3V_PWR
5V_PWR
DCBATOUT
DCBATOUT_3D3V
DCBATOUT_5D5V
3D3V_AUX_S5
5V_AUX_S5
3D3V_S5
5V_S5
+51120_VREF
CPUCORE_ON
44,46,47,48,50
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Olympus
SA
Wednesday, December 26, 2007
Sheet 43 of 53

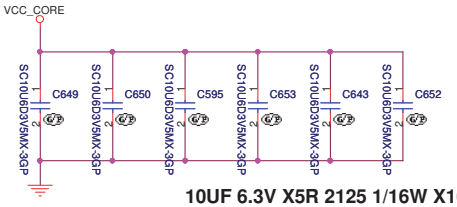

5,45 VCC_CORE
VCC_CORE
10,27 PM_DPRSLPVR
4,10,28 -DPRSTP
10,27 -VGAET_PWRG
CPUCORE_ON 43,46,47,48,50
VID[6..0] 5
DCBATOUT
DCBATOUT_6266A
3D3V_S0
1D05V_S0
5V_S0
VCC_CORE
Iomax: 38A
-SB modify
Place close to 1st phase choke
Place close to 1st Choke
ISL6266AHRZ-GP
74.06266.073
U42
U40
U38
U39
U7
U43
U5
NTMFS4841NT1G-GP
NTMFS4835NT1G-GP
L27
L26
IND-D36UH-9-GP
68.R3610.20C
G16 GAP-CLOSE
G18 GAP-CLOSE
G15 GAP-CLOSE
G17 GAP-CLOSE
6266A_UGATE1
6266A_PHASE1
6266A_LGATE1
6266A_UGATE2
6266A_PHASE2
6266A_LGATE2
6266A_VSUM
6266A_ISEN1
6266A_ISEN2
6266A_VO
6266AGND
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size
Document Number
LT32M
Rev
SA
Date: Wednesday, December 26, 2007
Sheet 44 of 53





10UF 6.3V X5R 2125 1/16W X16 PCS



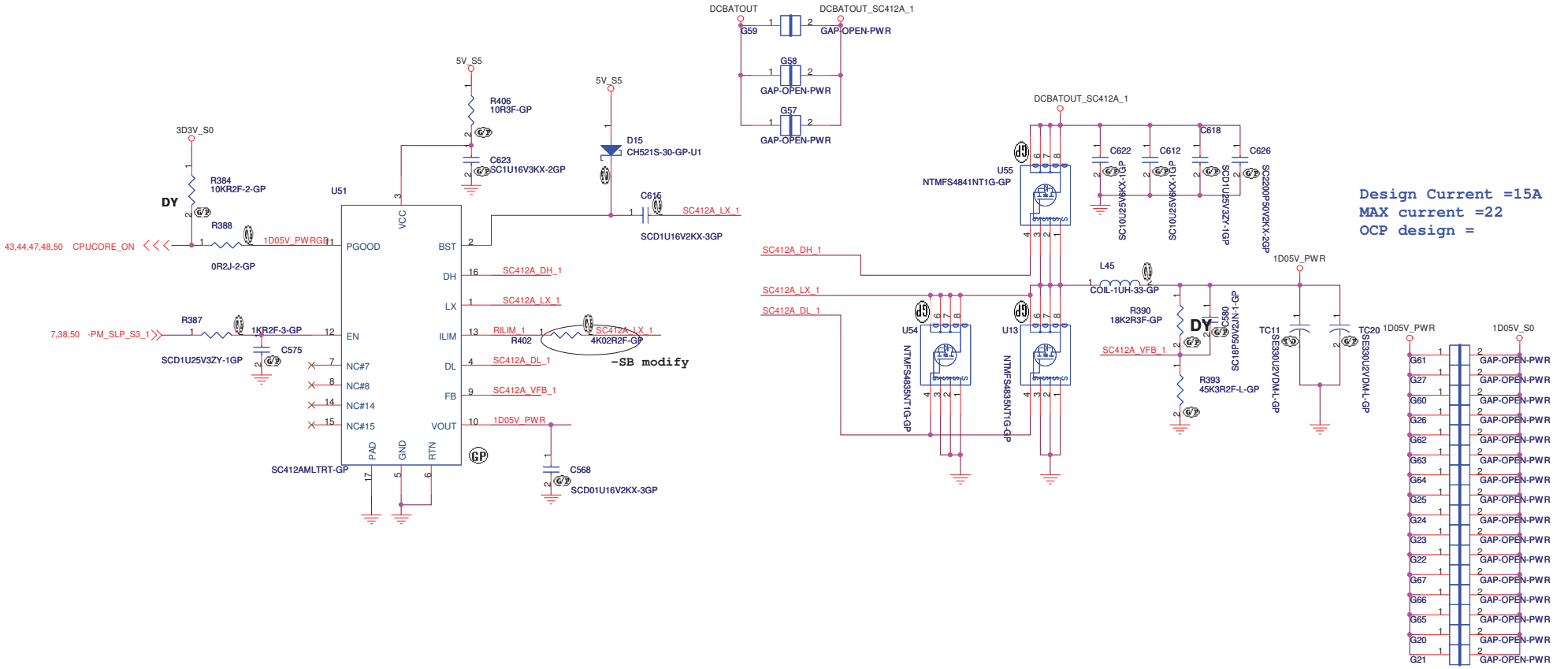


10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

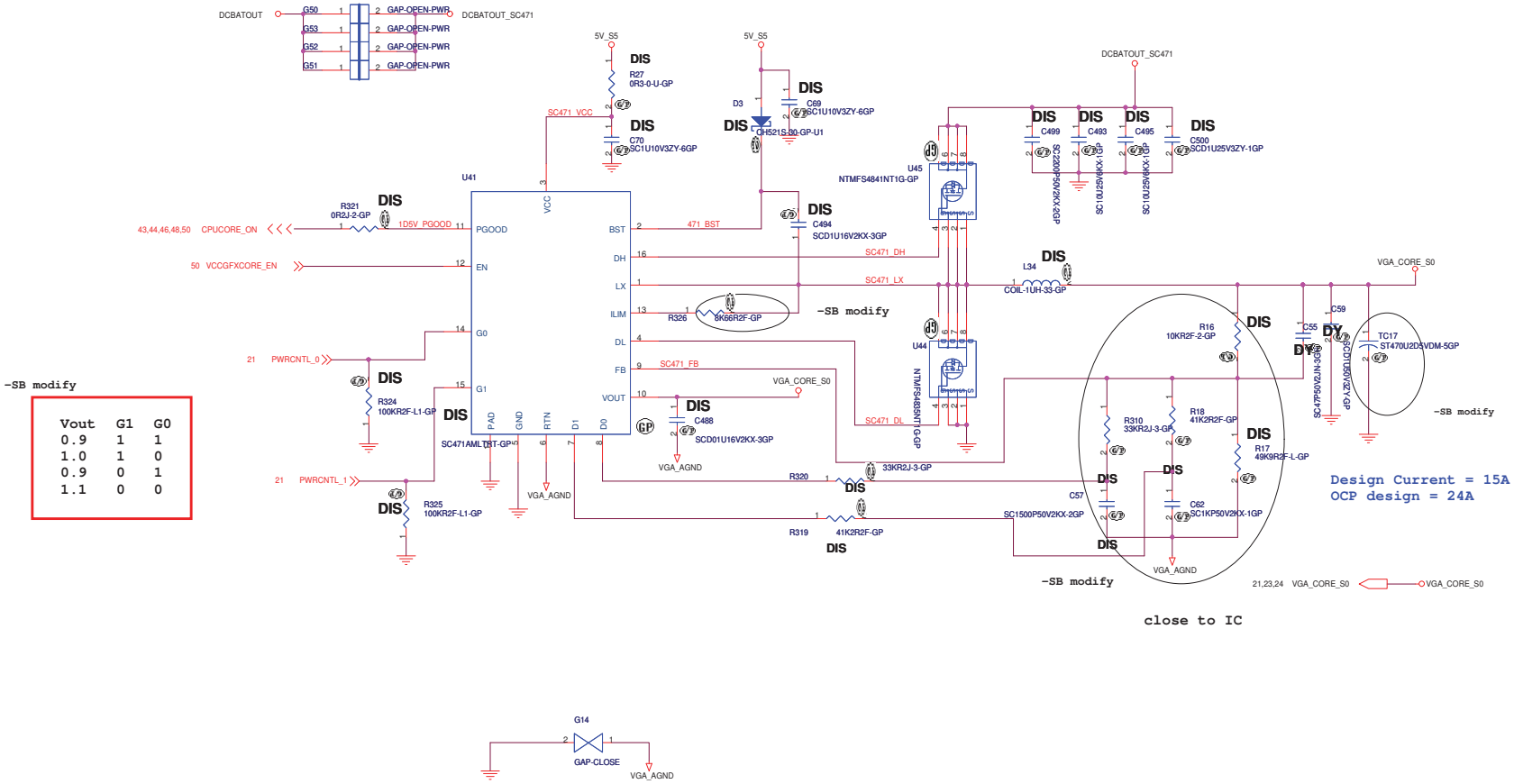
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VCCCPUCORE DECOUPLING***	
Size: Custom	Document Number: **LT32M**	Rev: **SA**
Date: Wednesday, December 26, 2007	Sheet 45 of 53	



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SC412A +1.05VM***	
Size A3	Document Number **LT32M**	Rev **SA**
Date: Wednesday, December 26, 2007	Sheet 46 of 53	



-SB modify

Vout	G1	G0
0.9	1	1
1.0	1	0
0.9	0	1
1.1	0	0

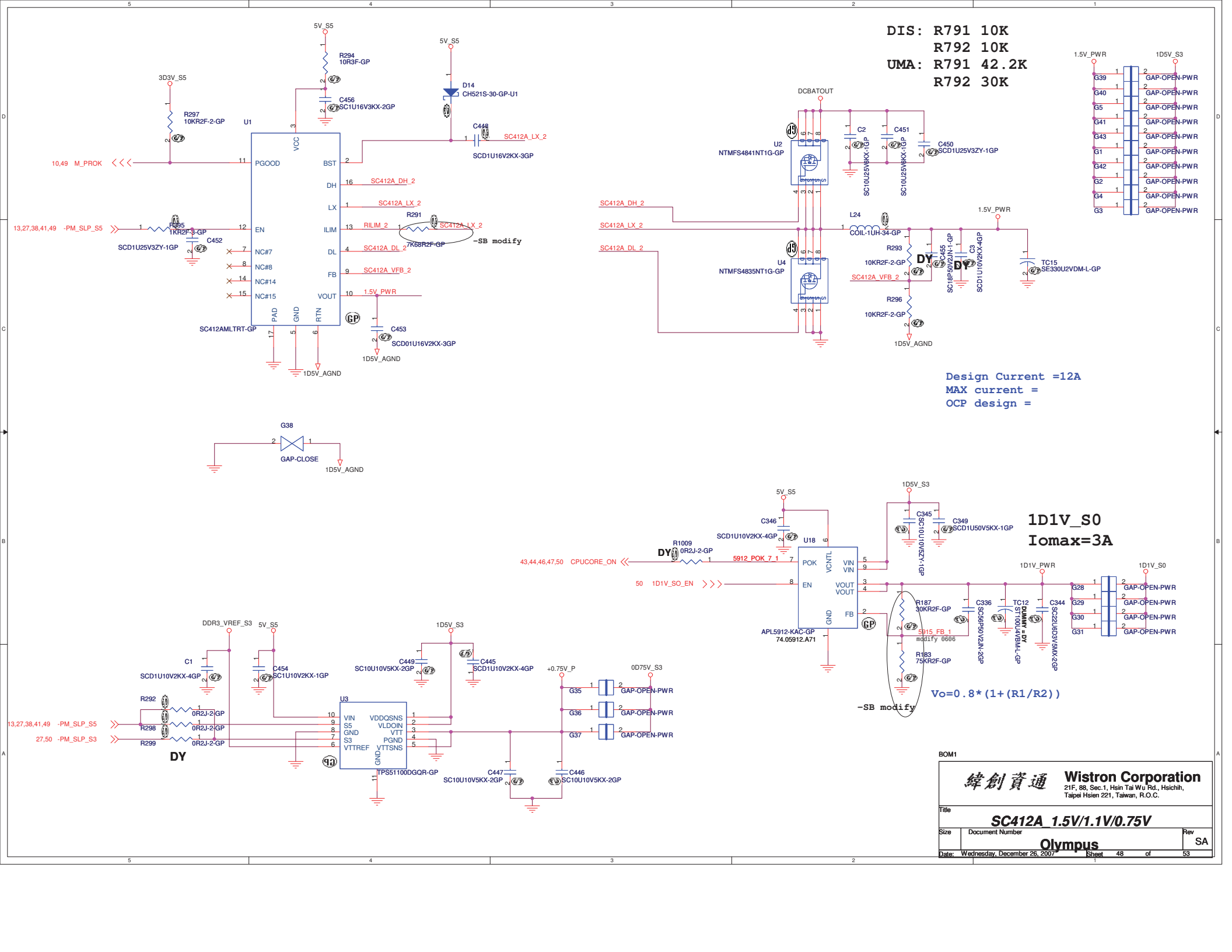
BOM1

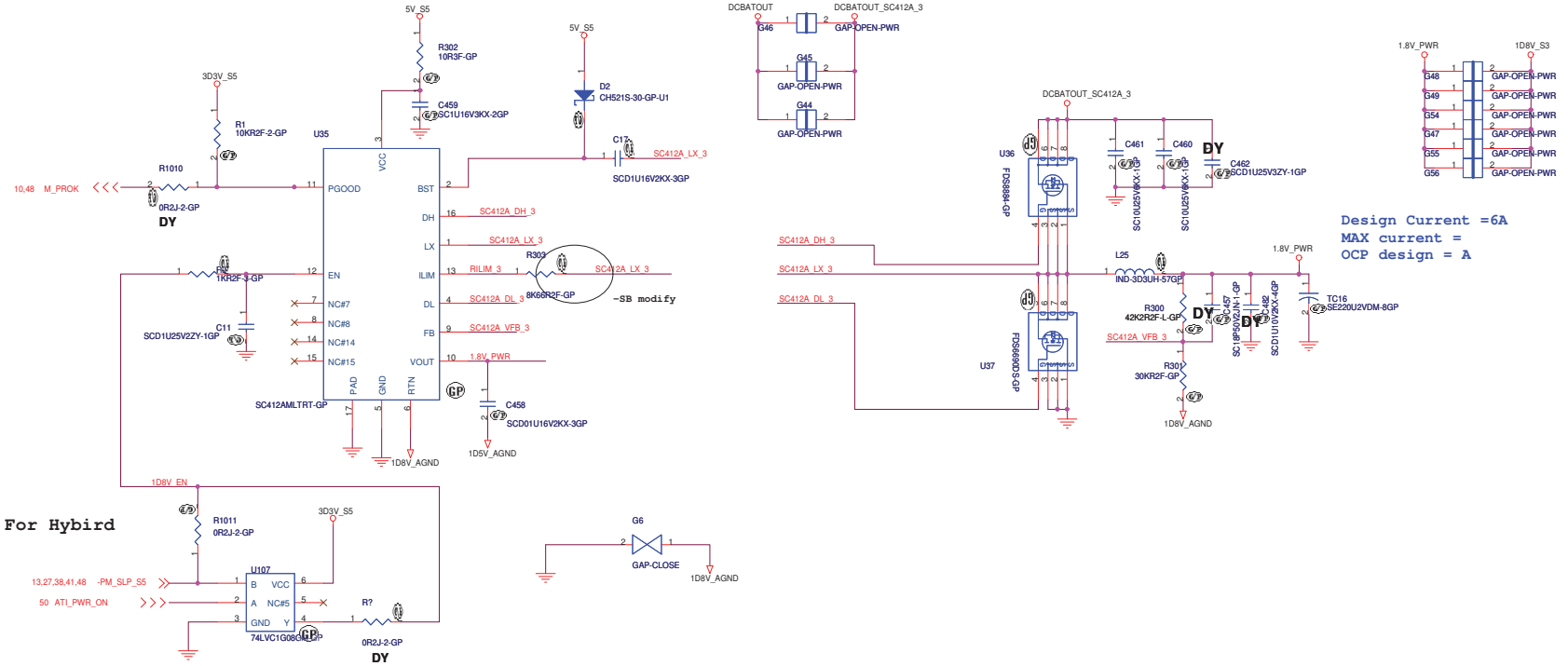
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC471A VGA CORE

Size	Document Number	Rev
C	LT32M	SA

Date: Wednesday, December 26, 2007 Sheet 47 of 53


DIS: R791 10K
R792 10K
UMA: R791 42.2K
R792 30K
Design Current =12A
MAX current =
OCP design =
1D1V_S0
Iomax=3A
Vo=0.8*(1+(R1/R2))
-SB modify
DY
U1
SC412AMLTRT-GP
U2
NTMFS4841NT1G-GP
U4
NTMFS4835NT1G-GP
U3
TPS51100DGQR-GP
U18
APL5912-KAC-GP
74.05912.A71
L24
COIL-1UH-34-GP
D14
CH521S-30-GP-U1
5V_S5
3D3V_S5
1.5V_PWR
1D5V_S3
1D5V_AGND
DCBATOUT
1D1V_PWR
1D1V_S0
DDR3_VREF_S3
0D75V_S3
+0.75V_P
GAP-OPEN-PWR
GAP-CLOSE
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SC412A_1.5V/1.1V/0.75V
Size
Document Number
Olympus
Rev
SA
Date: Wednesday, December 26, 2007
Sheet 48 of 53



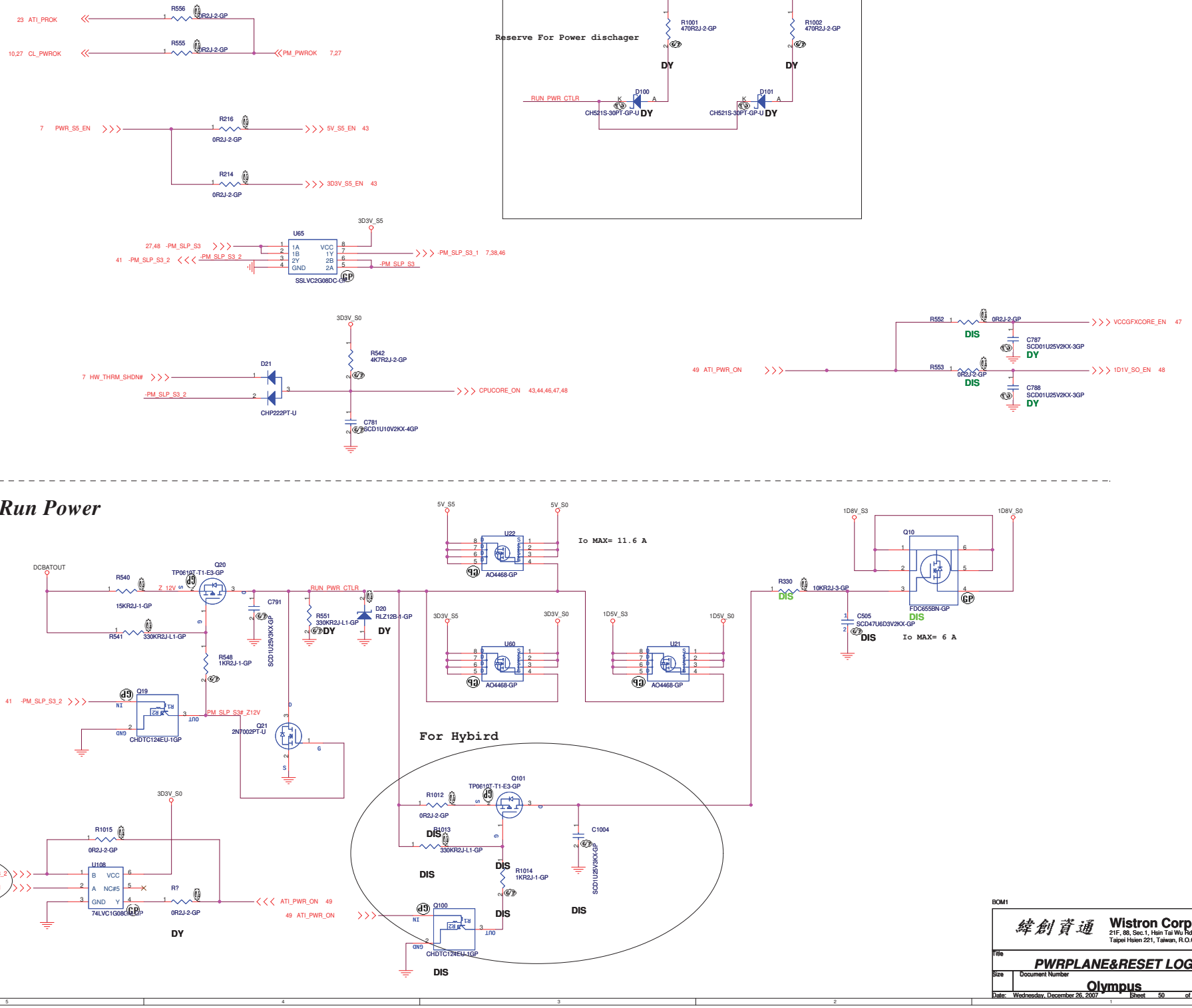
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC412A_1.8V

Size	Document Number	Rev
	LT32M	SA

Date: Wednesday, December 26, 2007 Sheet 49 of 53



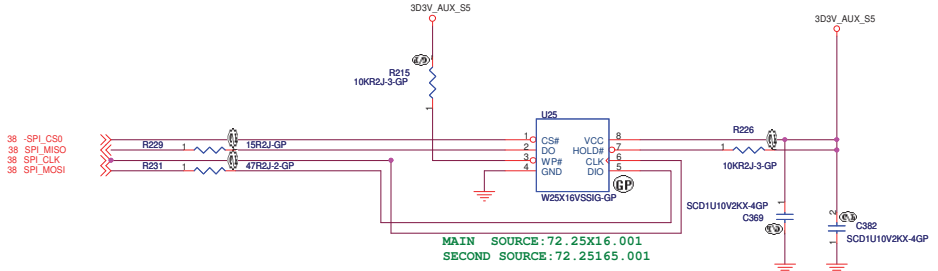
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

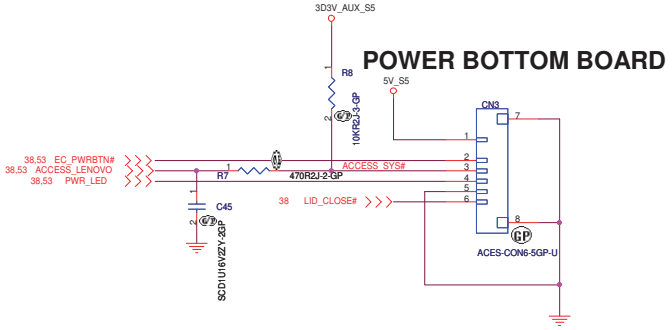
Title: PWRPLANE&RESET LOGIC

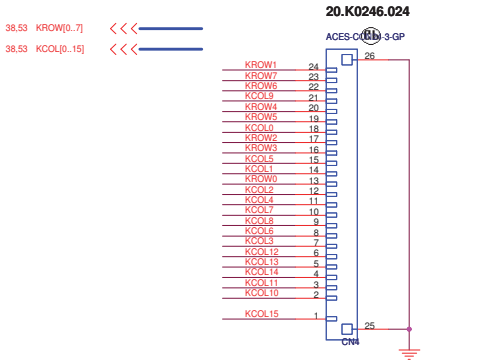
Size	Document Number	Rev
	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 50 of 53

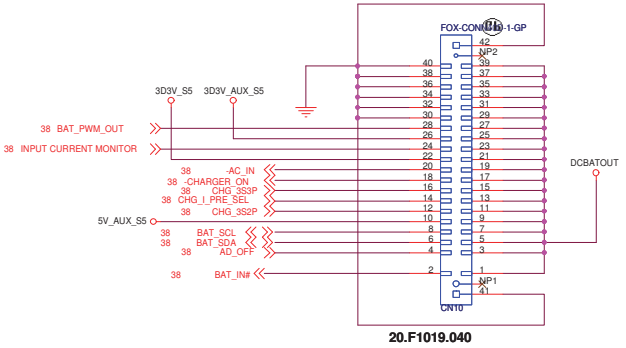


SPI FLASH





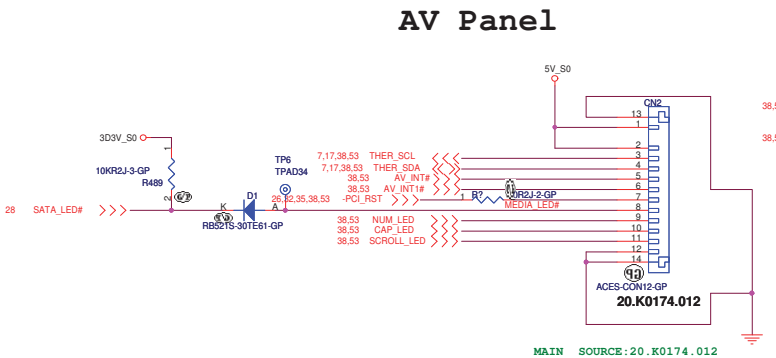
KEYBORD CONNECTOR

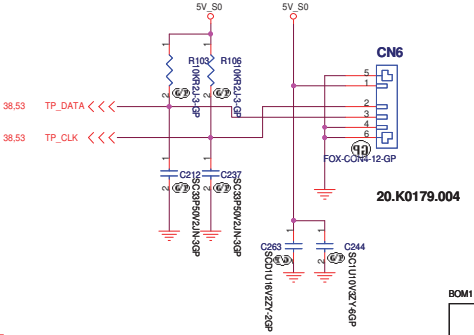


CHARGER CONNECTOR

AV Panel

TouchPad Connector





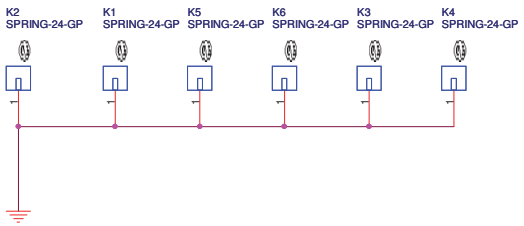
BOM1

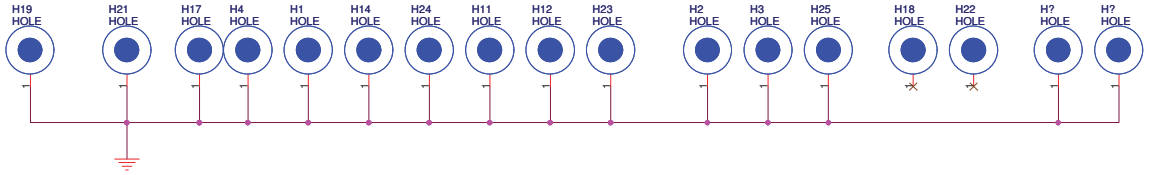
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

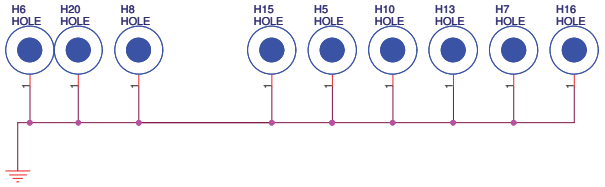
Title: KB/TP/SPI/AV/Charger

Size	Document Number	Rev
	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 51 of 53







BOM1

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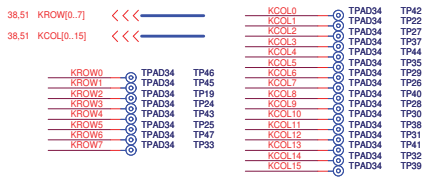
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PTH FOR SCREW HOLES***

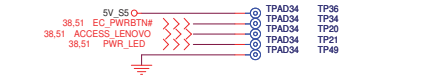
Size	Document Number	Rev
Custom	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 52 of 53

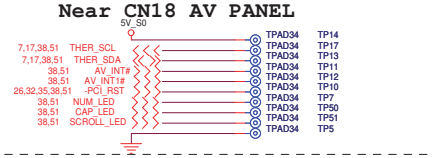
Near CN13 KB



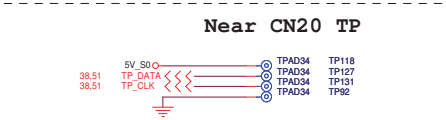
Near CN24 POWER BOOTOM BOARD



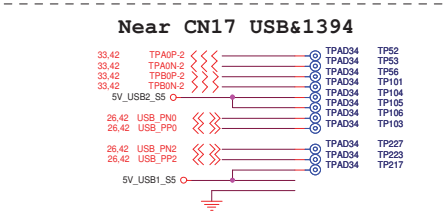
Near CN18 AV PANEL



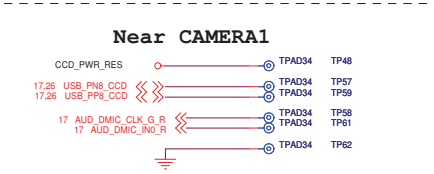
Near CN20 TP



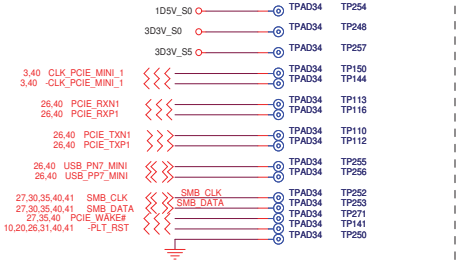
Near CN17 USB&1394



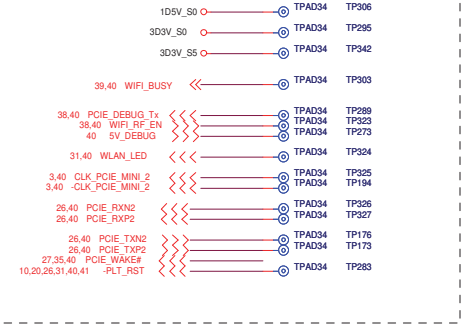
Near CAMERA1



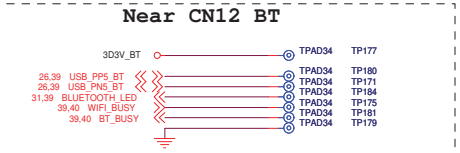
Near CN6 MINI PORT-1



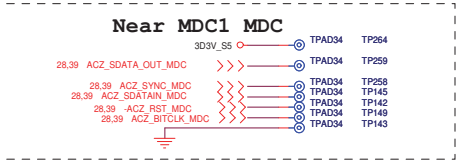
Near CN7 MINI PORT-2



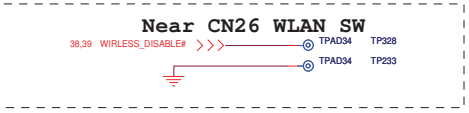
Near CN12 BT



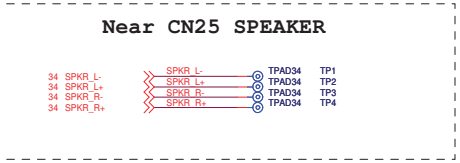
Near MDC1 MDC



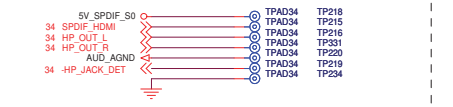
Near CN26 WLAN SW



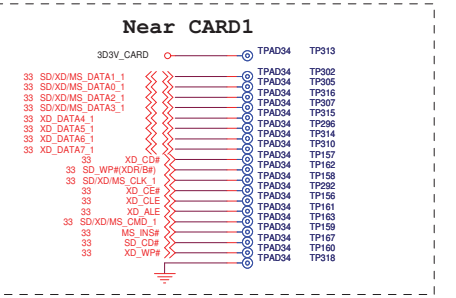
Near CN25 SPEAKER



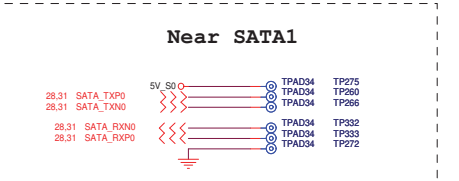
Near HP/SPDIF1



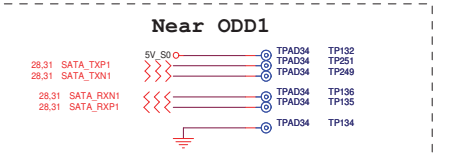
Near CARD1



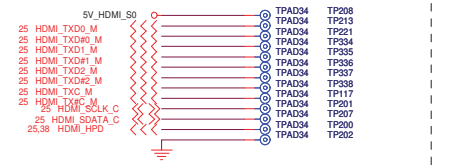
Near SATA1



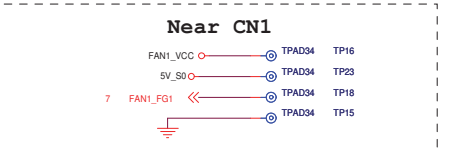
Near ODD1



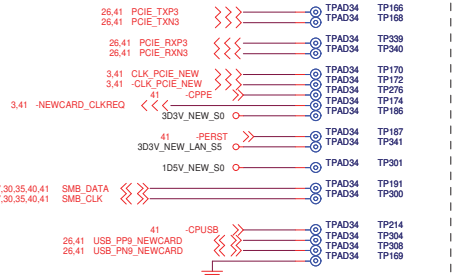
Near HDMI1



Near CN1



Near CN9 NewCard



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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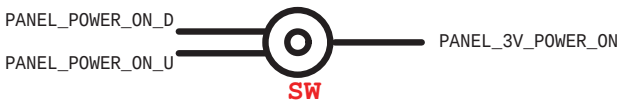
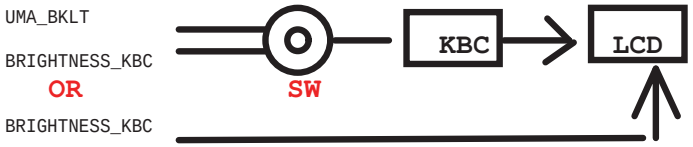
Size C	Document Number **Olympus**	Rev **SB**
Date: Wednesday, December 26, 2007	Sheet 53 of 53	

LCD

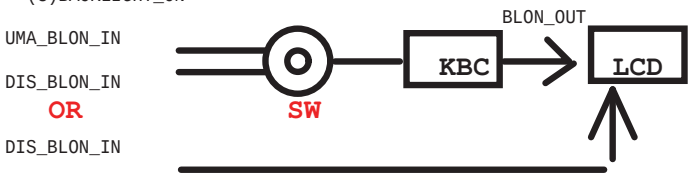
(1)PANEL_3V_ON



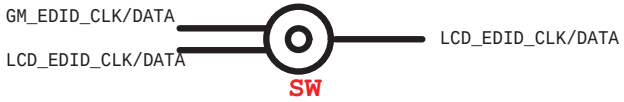
(2)BRIGHTNESS PWM



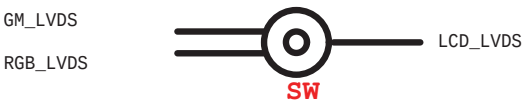
(3)BACKLIGHT_ON



(4)EDID DATA/CLK



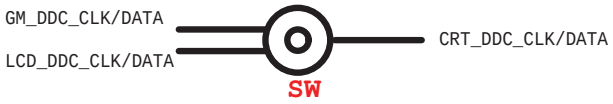
(5) LVDS signal



All the switch control by SB_GPIO52
and define
L => -UMA channel
H => -ATI channel

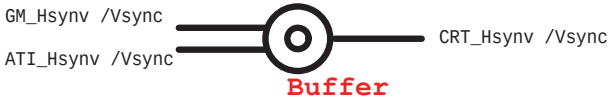
CRT

(1)DDC DATA/CLK



(2) RGB signal

(2) Hsynv & Vsync



BOM1

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Title: *TTEST_PAD*		
Size: A	Document Number: **Olympus**	Rev: **SB**
Date: Wednesday, December 26, 2007	Sheet 54 of 53	