

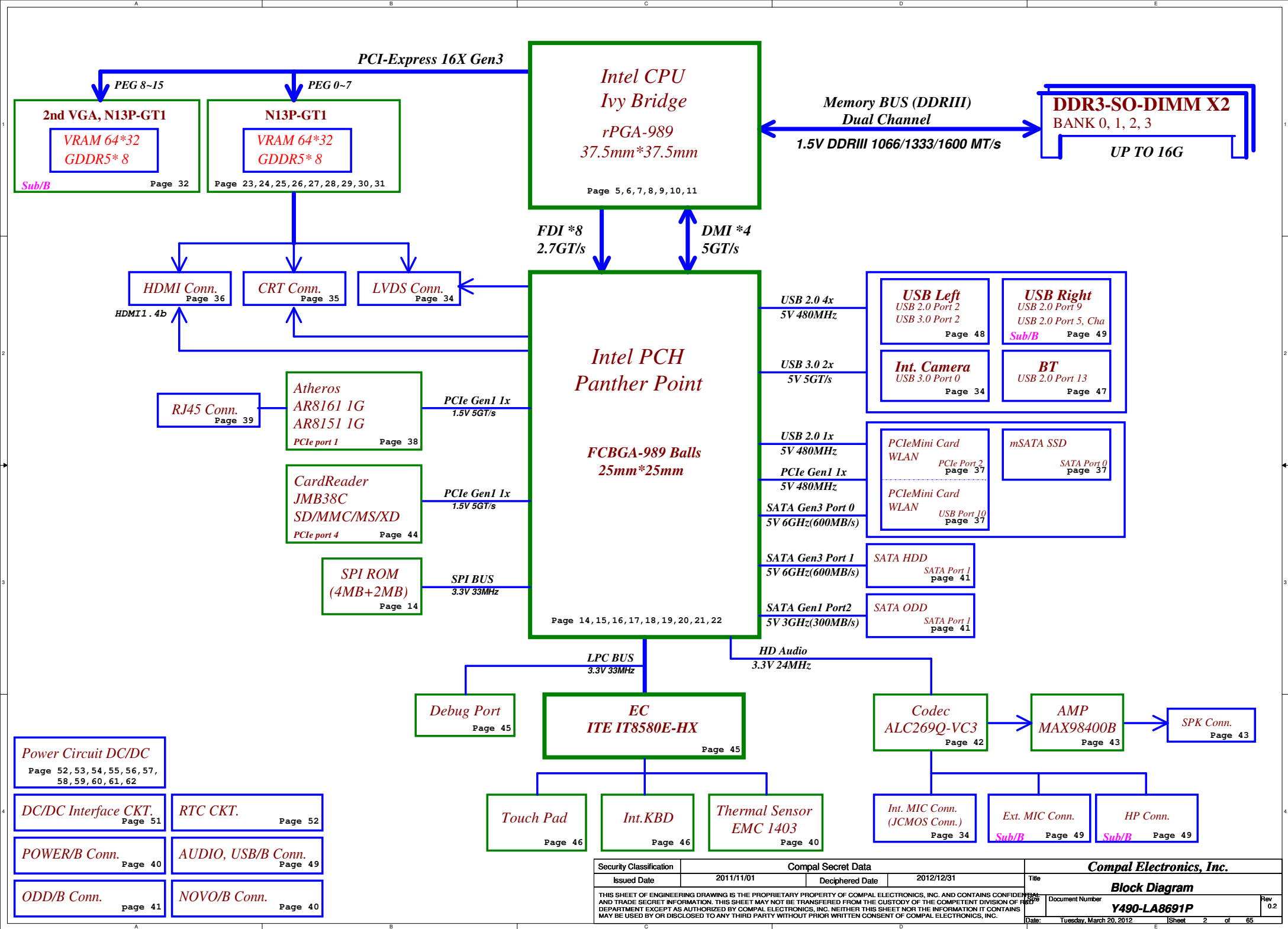
QIQY5

Whisky3.0 (Y490)

LA-8691P Rev0.2 Schematic

*Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13P GT1-A2 + 2nd VGA N13P GT1-A2
2012-02-05 Rev0.2*

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
	XHCI 1	0	Camera
		1	
		2	USB Port (Left Side)
		3	
		4	
		5	USB Port (Right Side)
		6	
		7	
	EHCI 2	8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

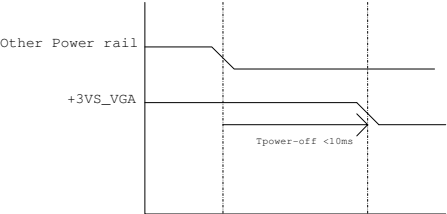
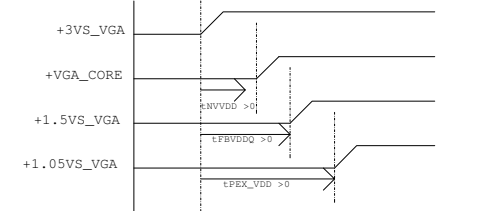


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Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

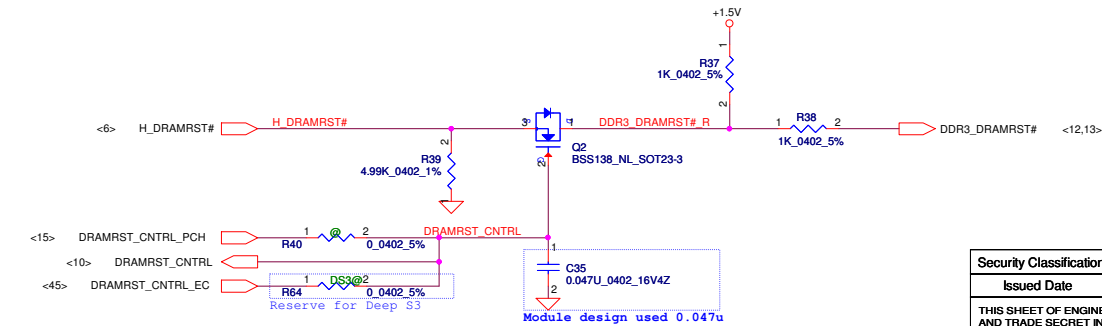
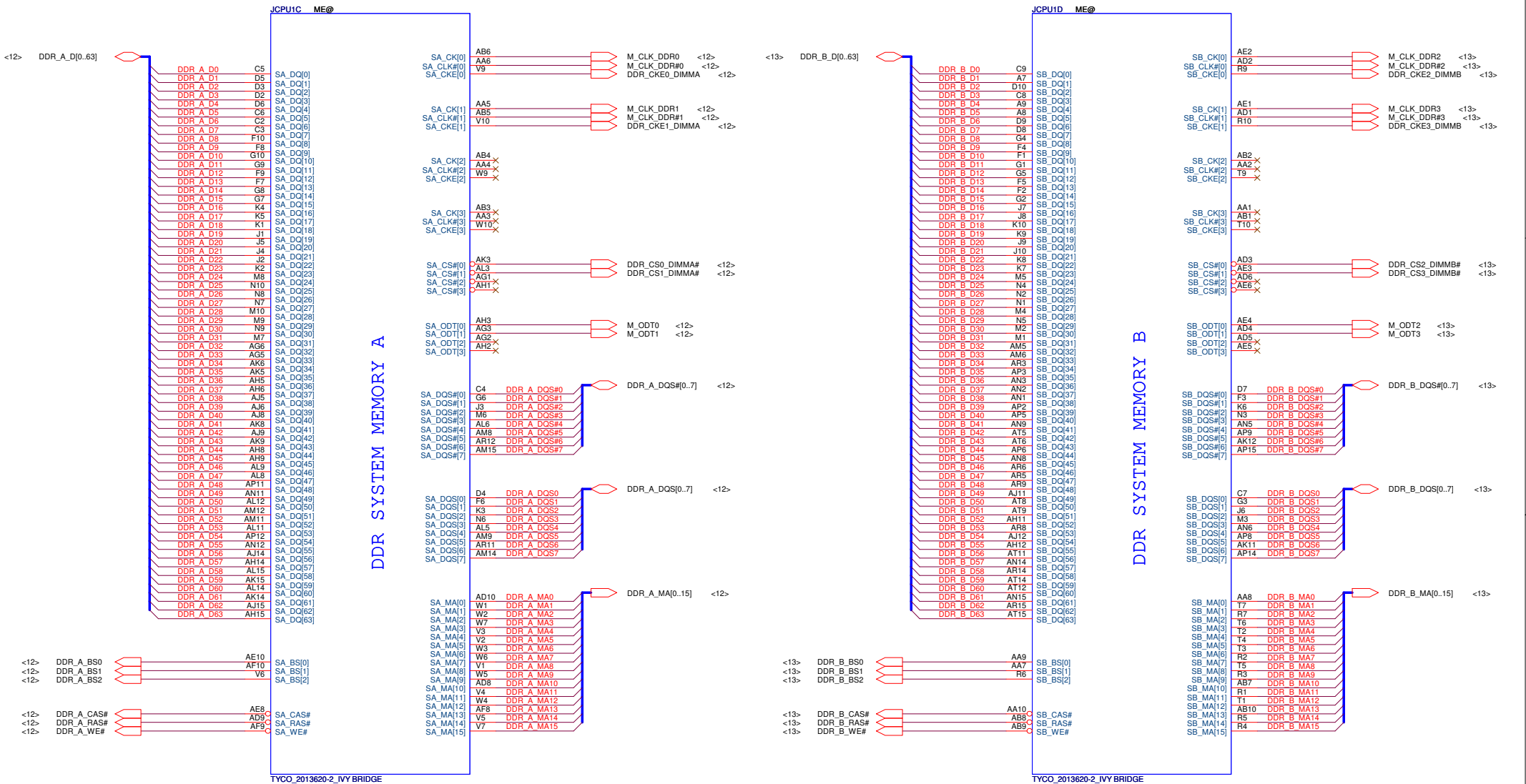
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID		setting	I2C Slave addresses ID
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
			1	0x9C

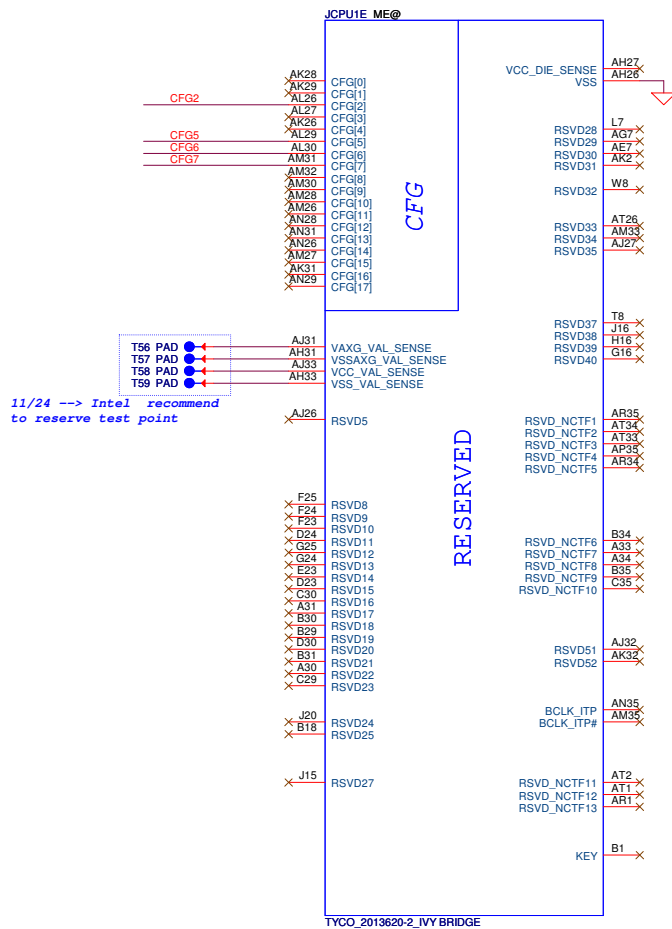
GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

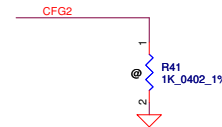
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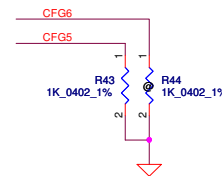


CFG Straps for Processor

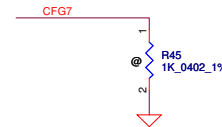


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	★ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



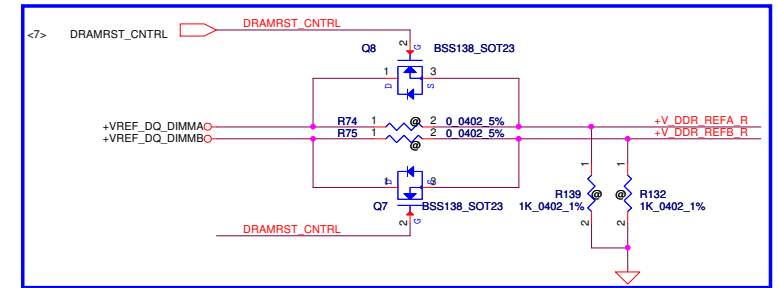
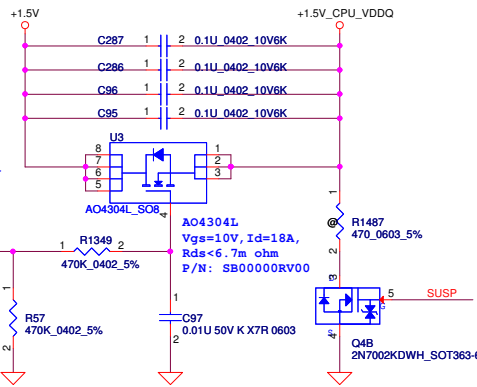
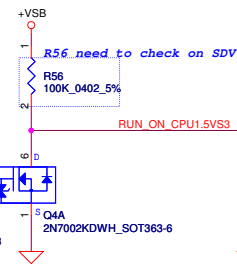
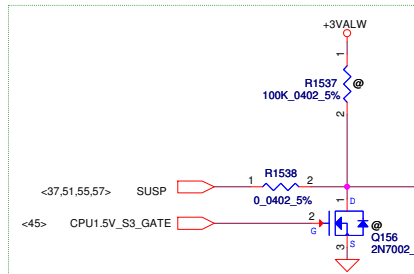
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled ★10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

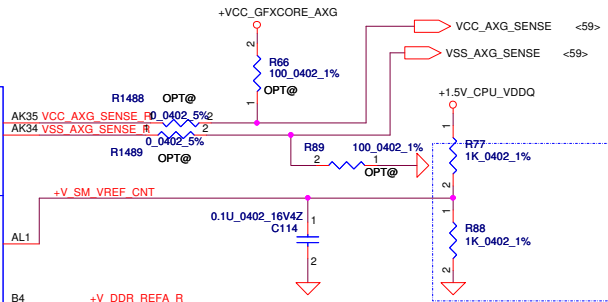
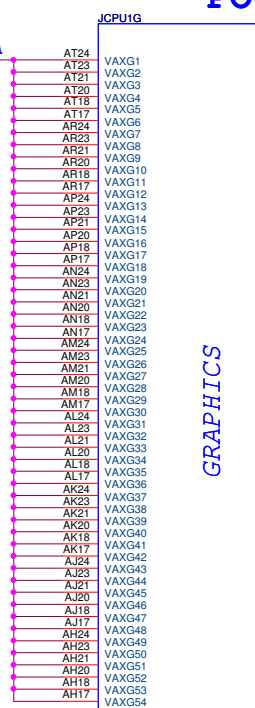
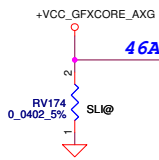
+1.5V_CPU_VDDQ

For Deep S3

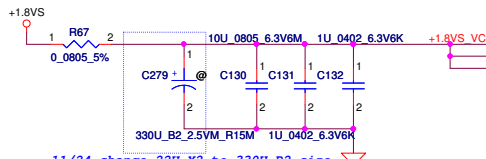
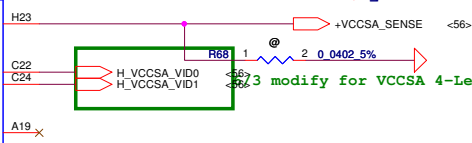
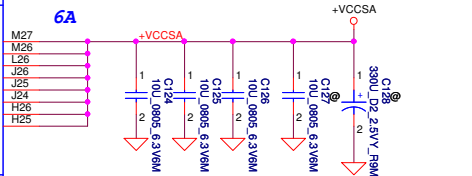
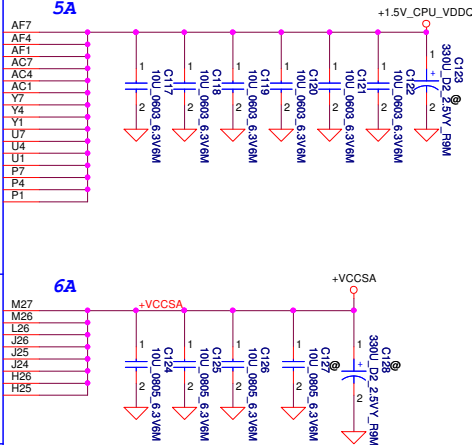


6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

POWER



Place the PU/PD resistor close to CPU within 2 inch (Reserve power side)

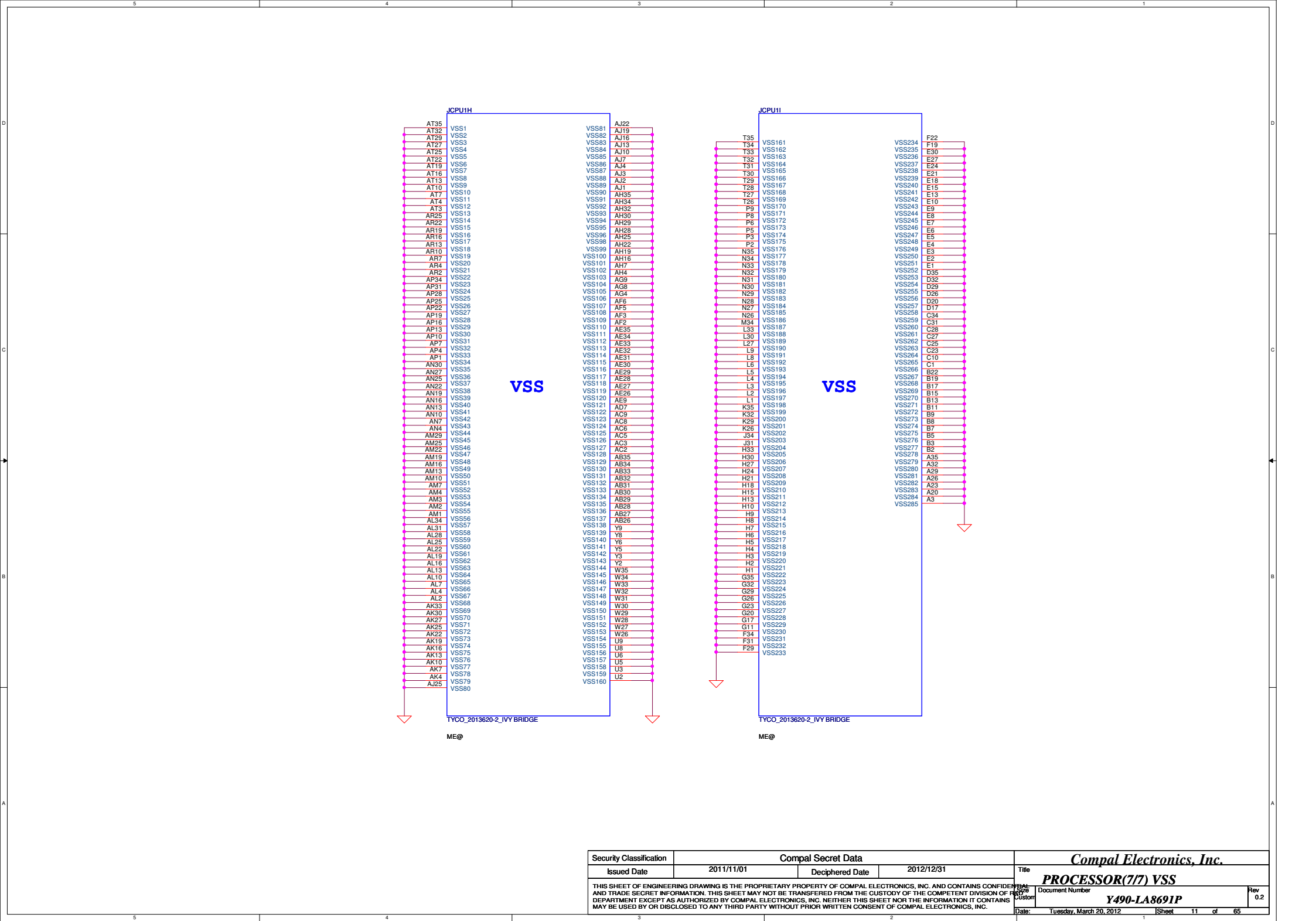


11/24 change 22U X2 to 330U B2 size

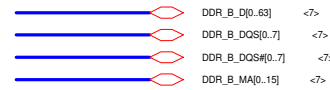
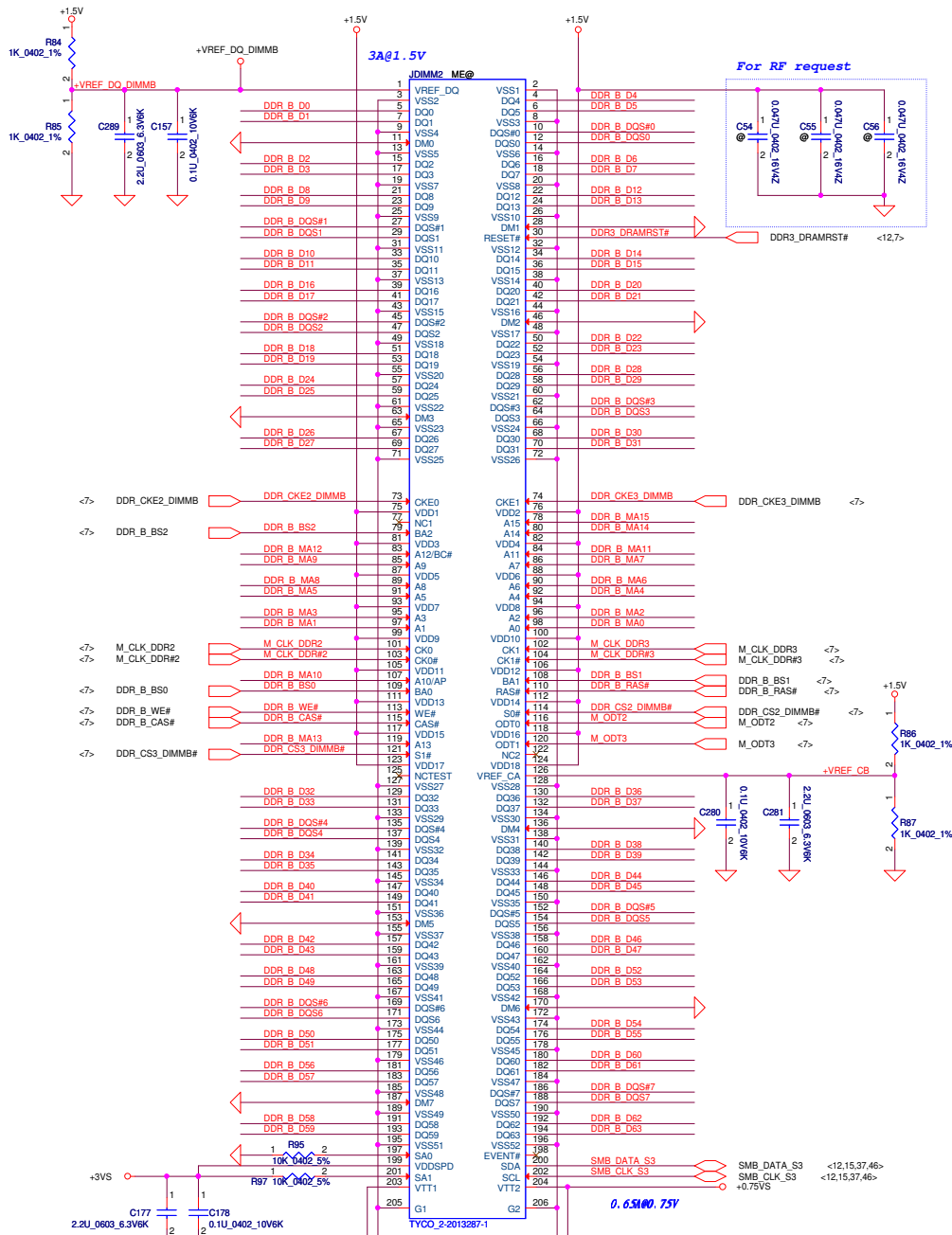
TYCO 2013620-2_VYBRIDGE

ME@

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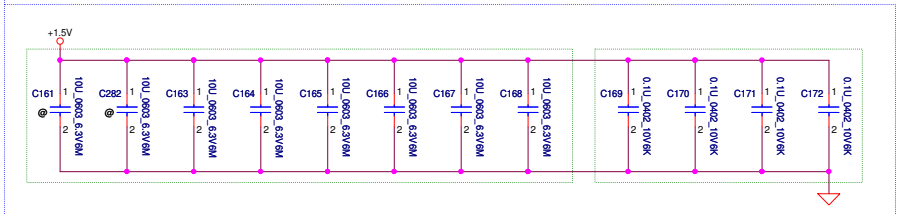


DDR3 SO-DIMM B



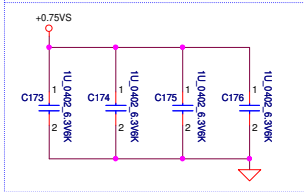
Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4



Layout Note:
Place near DIMM

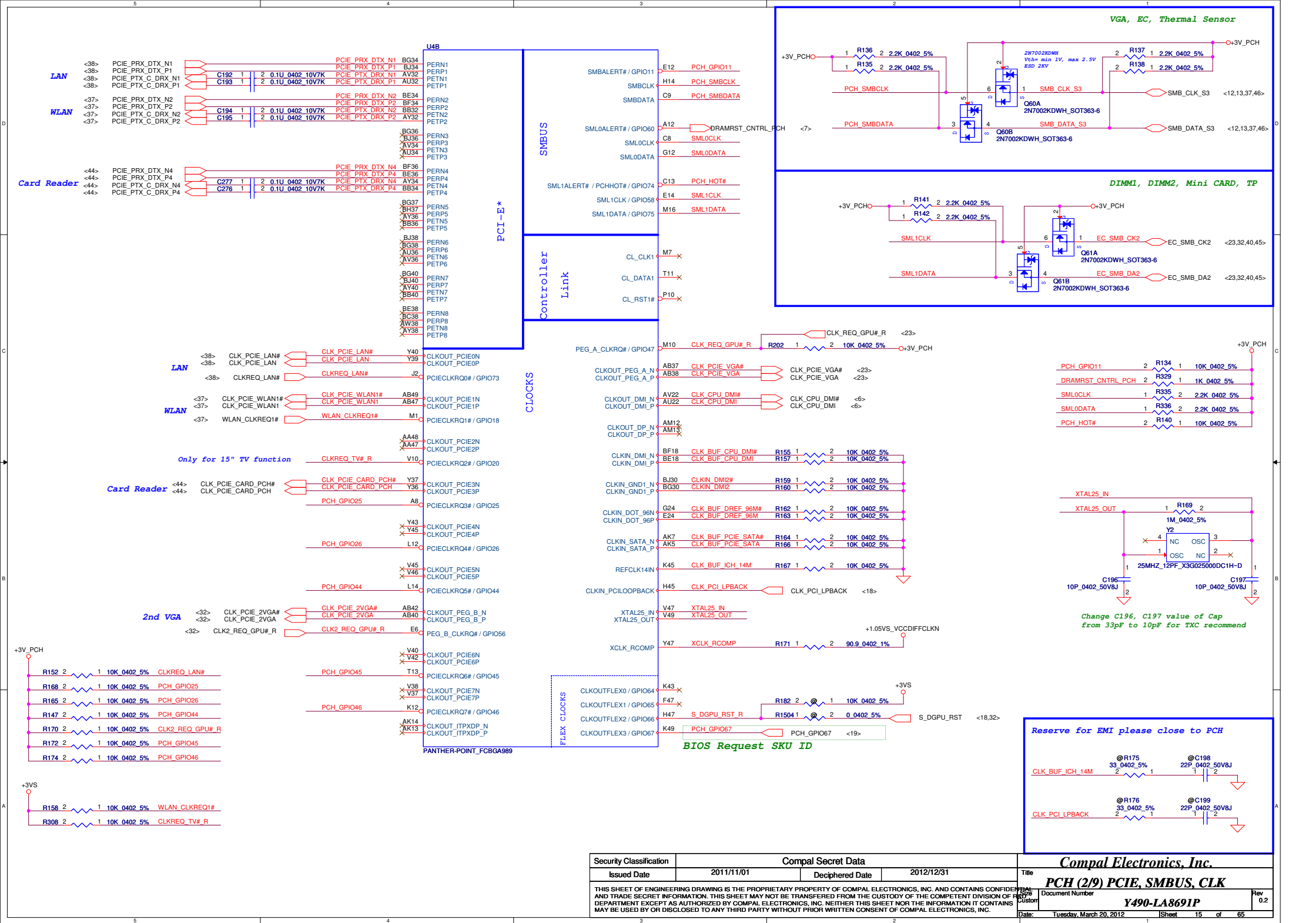
Layout Note:
Place near DIMM

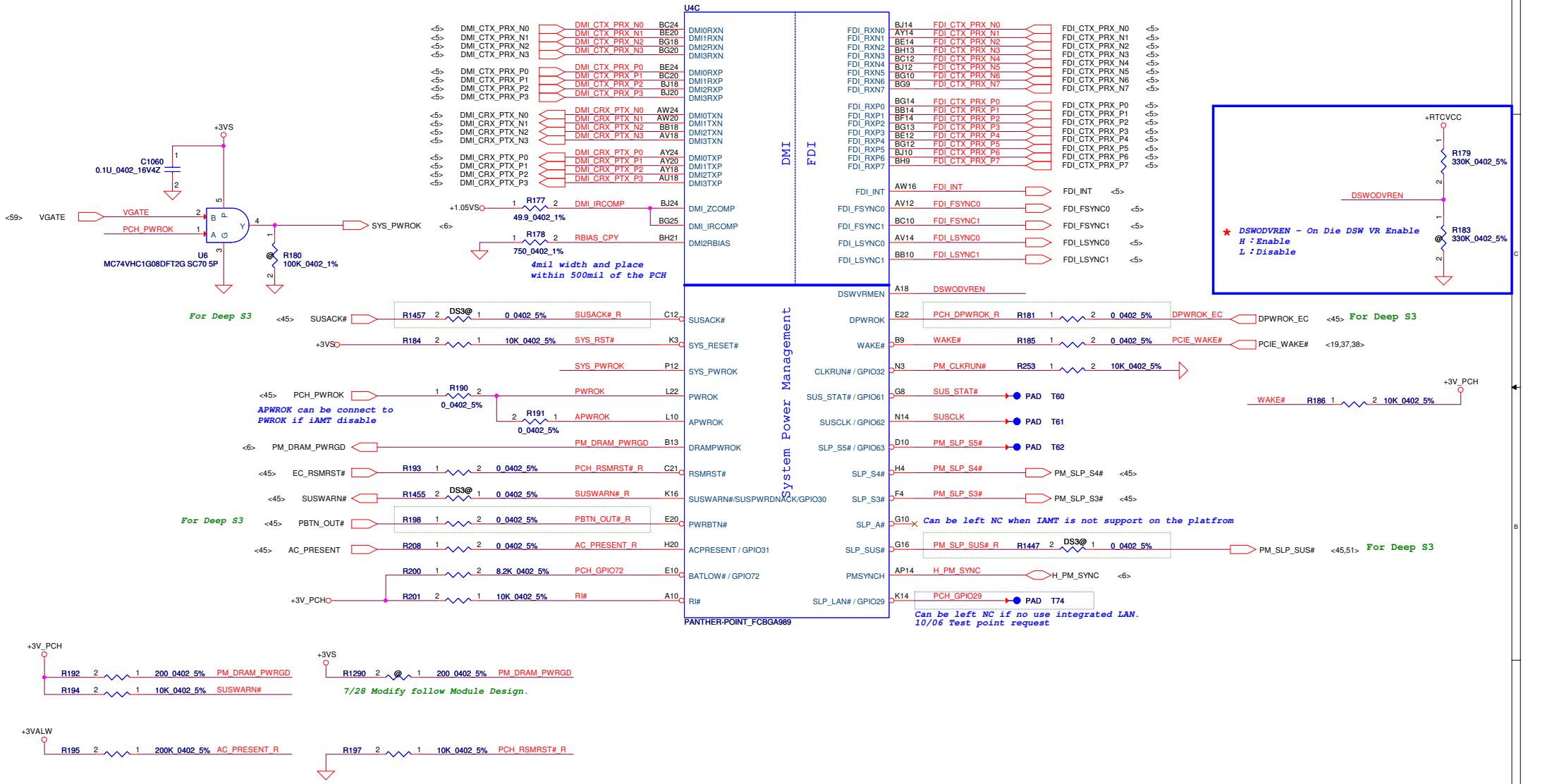


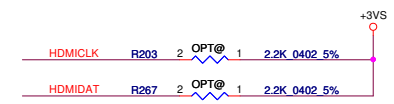
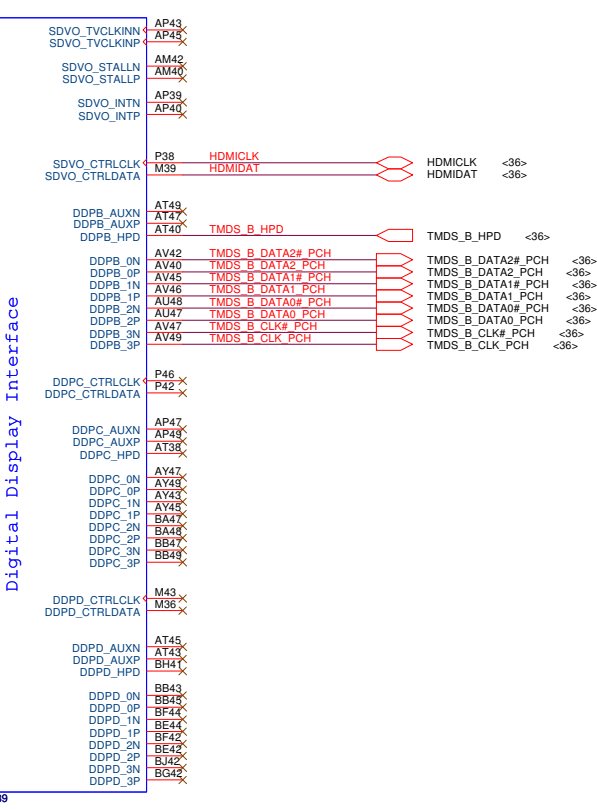
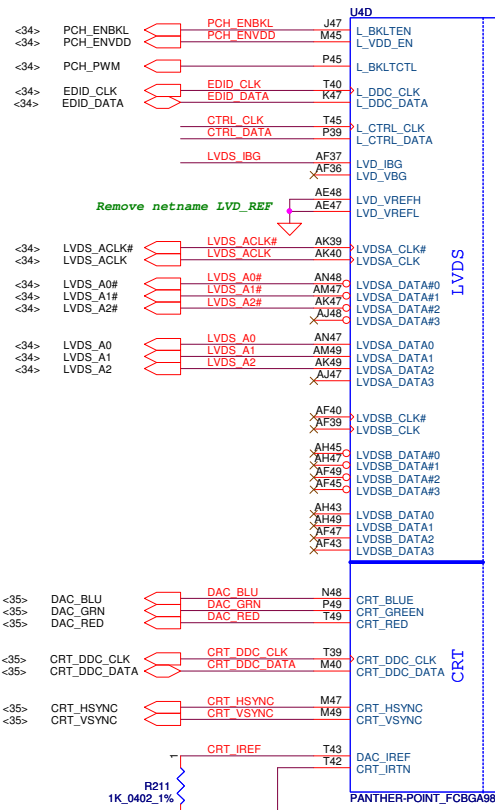
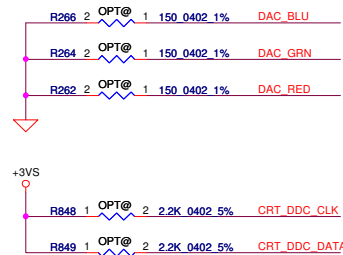
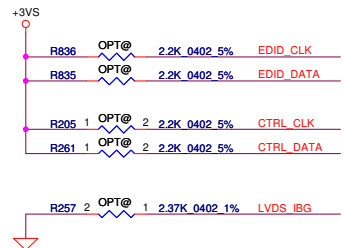
DDR_B_DM[0:7] connect to GND

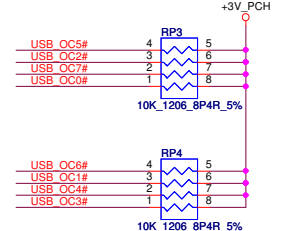
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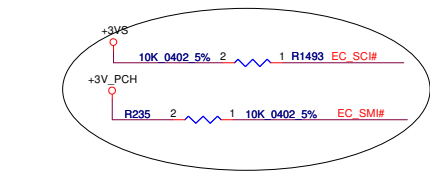






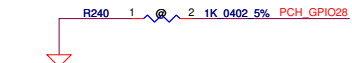


Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

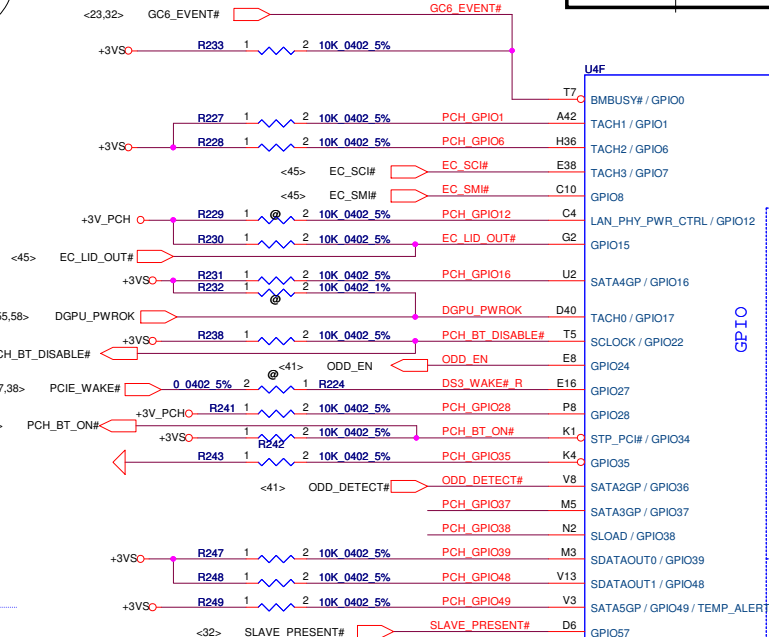
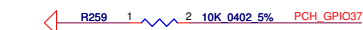
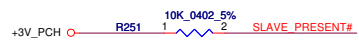
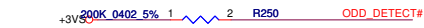
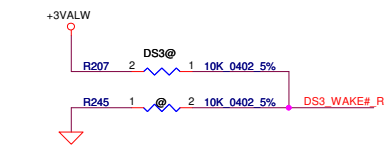


GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

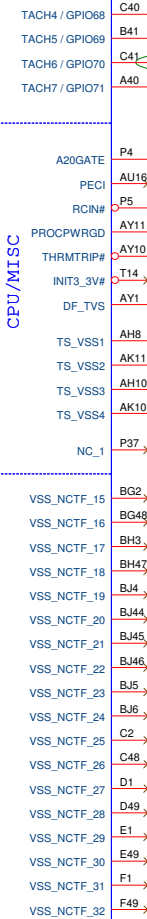


* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable



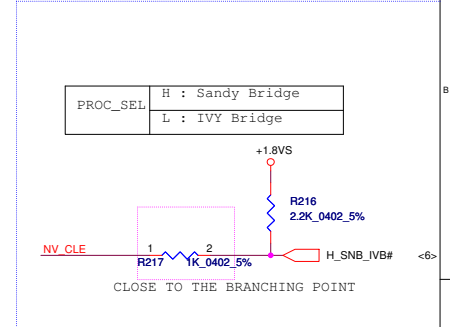
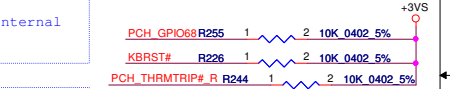
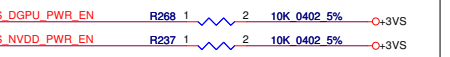
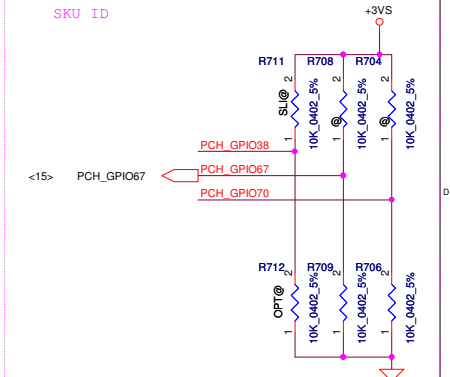
GPIO

NCTF

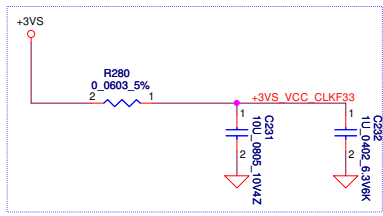


CPU/MISC

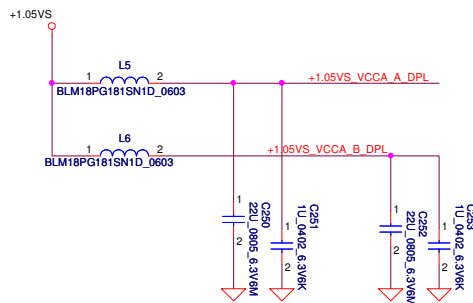
NCTF



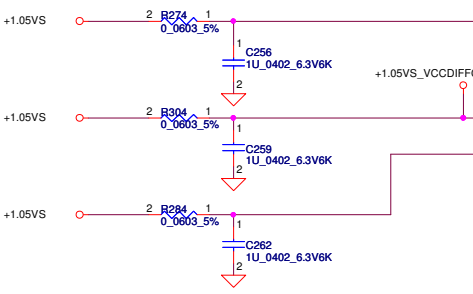
PROC_SEL	H : Sandy Bridge
	L : IVY Bridge



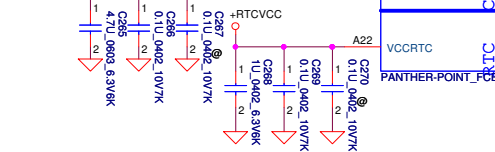
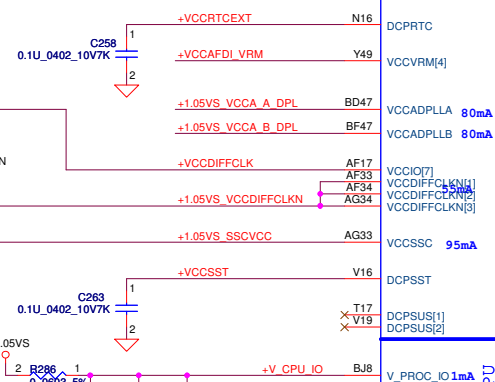
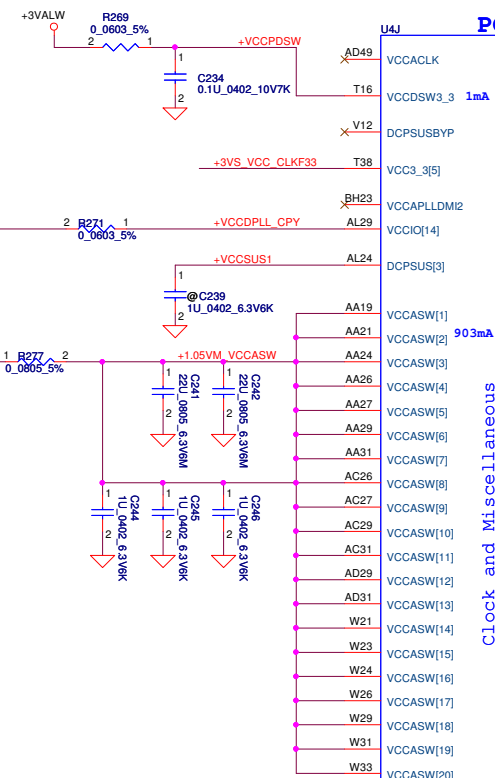
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA



Before gerber out change to 22u_0805



Have internal VRM



POWER

USB

PCI/GPIO/LPC

SATA

MISC

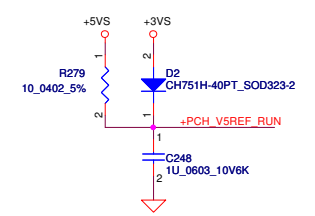
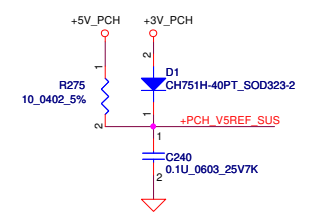
CPU

Clock and Miscellaneous

RTC

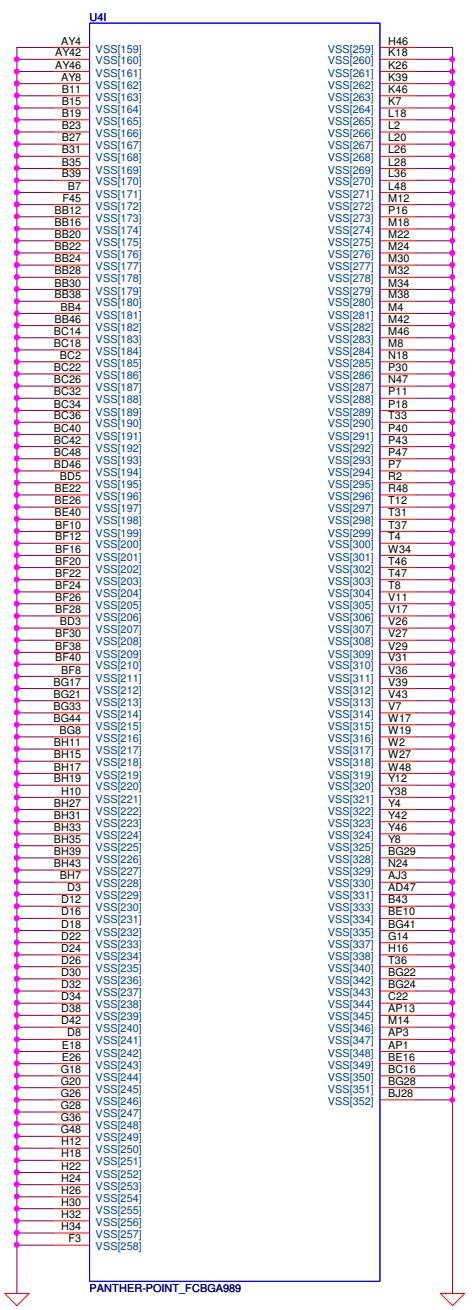
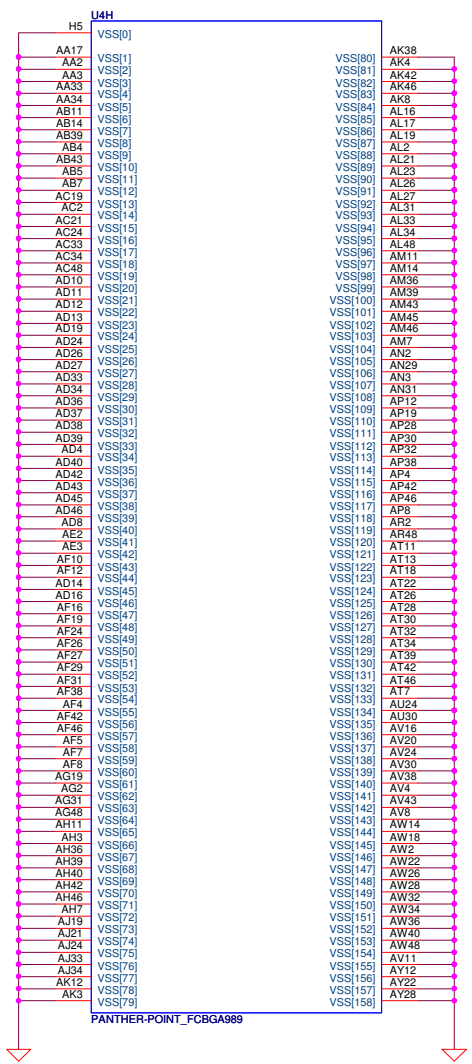
RTC

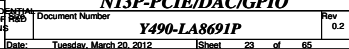
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

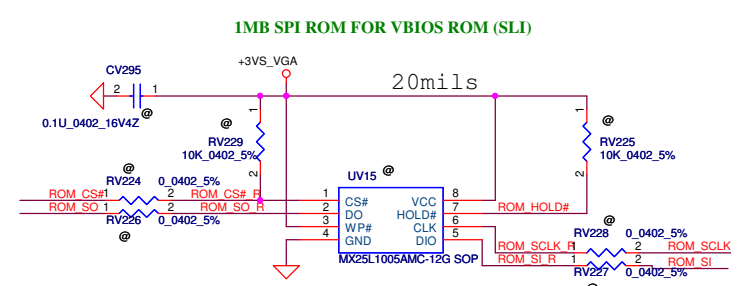


On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

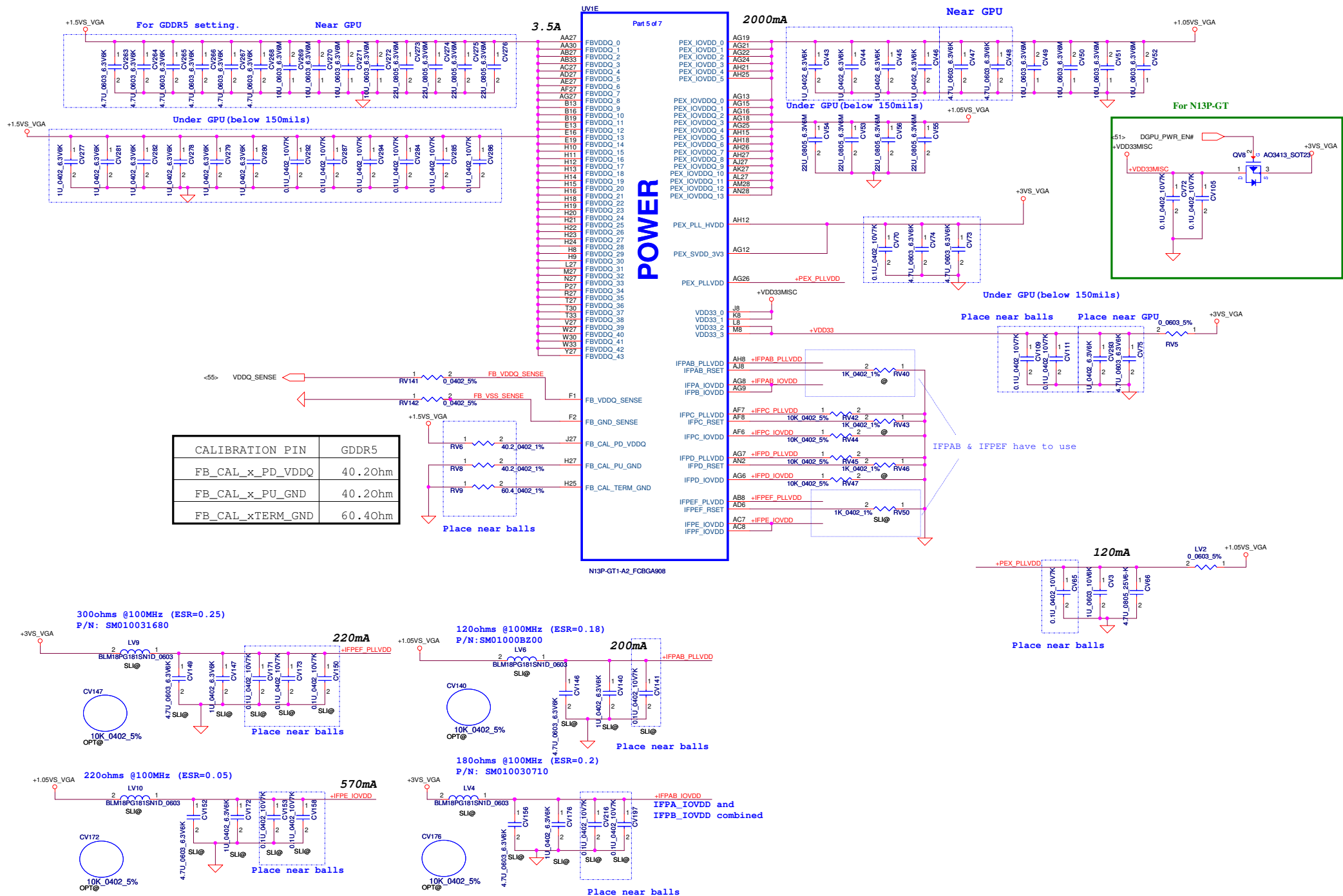
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						Document Number		Rev	
						Y490-LA8691P		0.2	
						Date: Tuesday, March 20, 2012		Sheet 21 of 65	



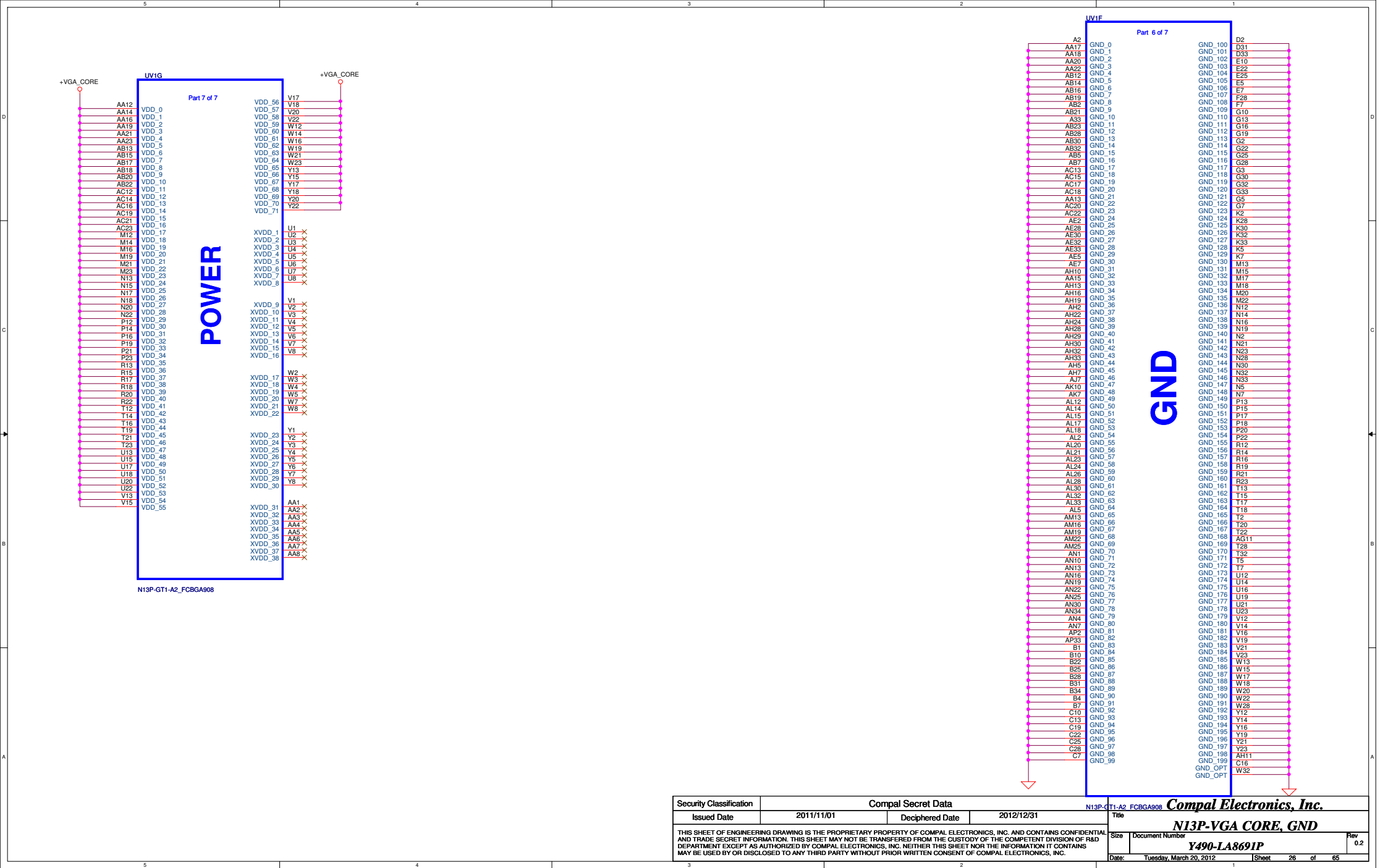


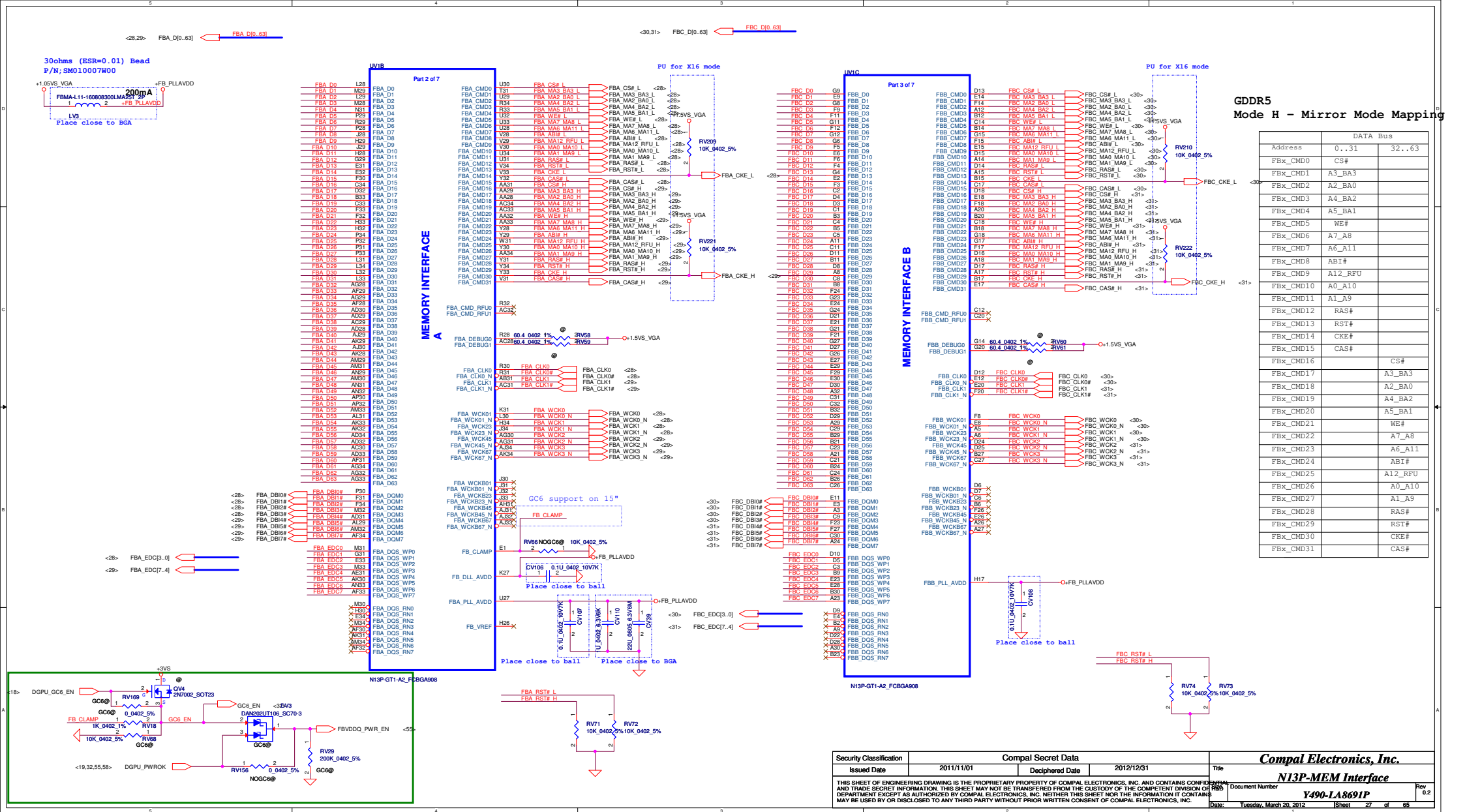


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					Rev 0.2
				Date:	Tuesday, March 20, 2012
				Sheet	24 of 65



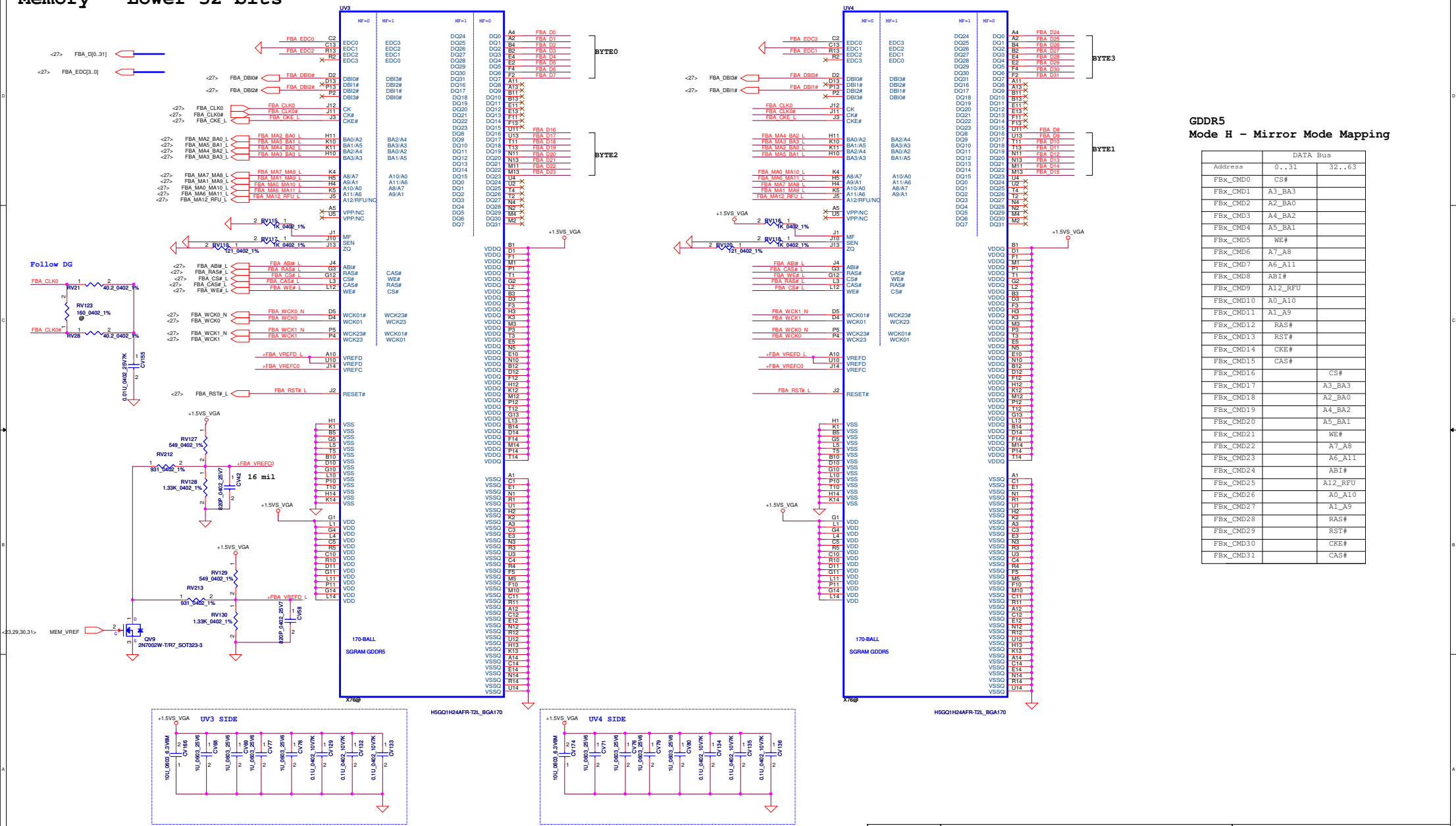
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	40.20hm
FB_CAL_xTERM_GND	60.40hm





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Date		Tuesday, March 20, 2012		Sheet 27 of 65	

Memory - Lower 32 bits

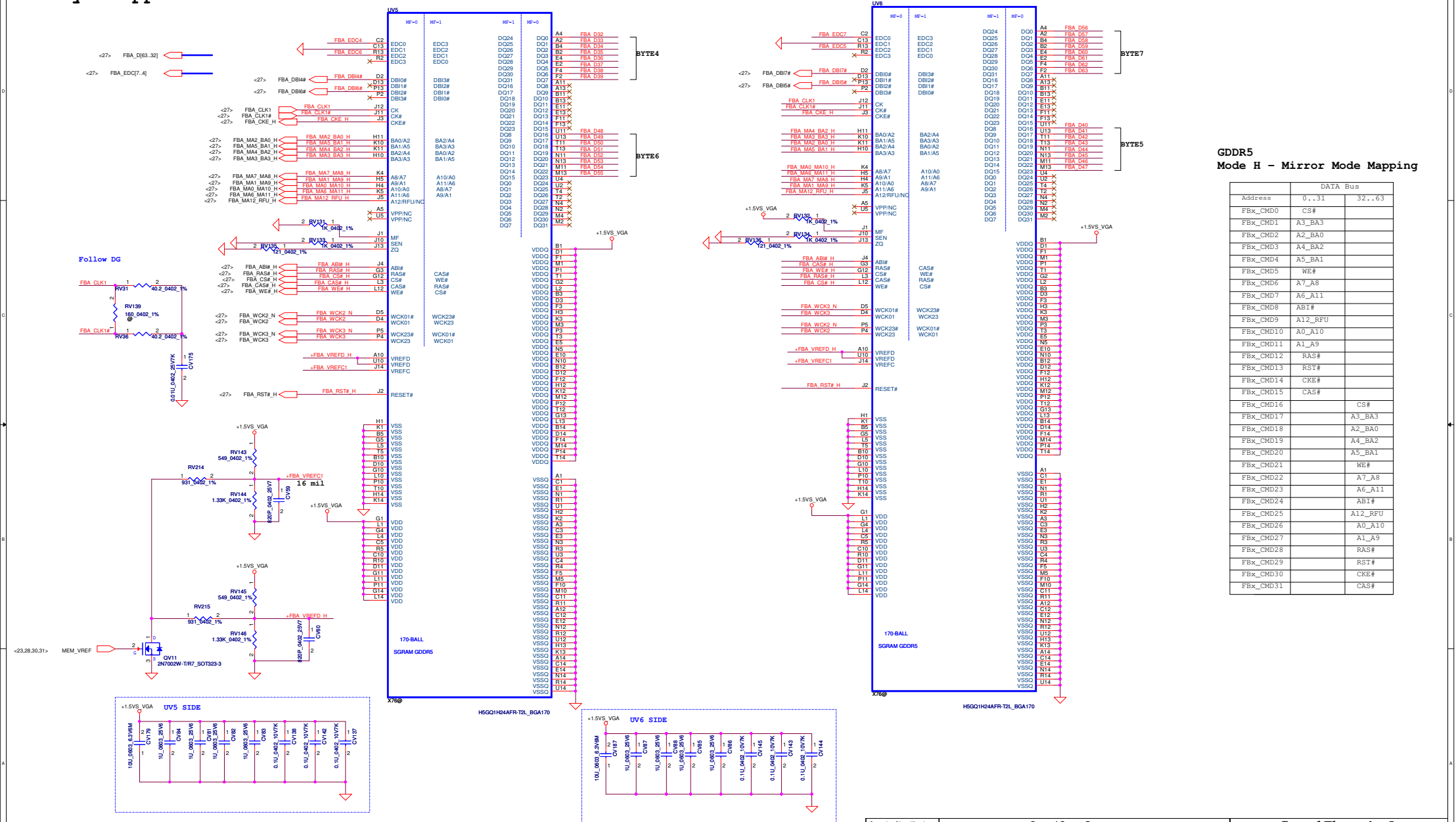


DDR5

Mode H - Mirror Mode Mapping

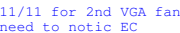
	DATA Bus	
Address	0...31	32...63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Memory – Upper 32 bits

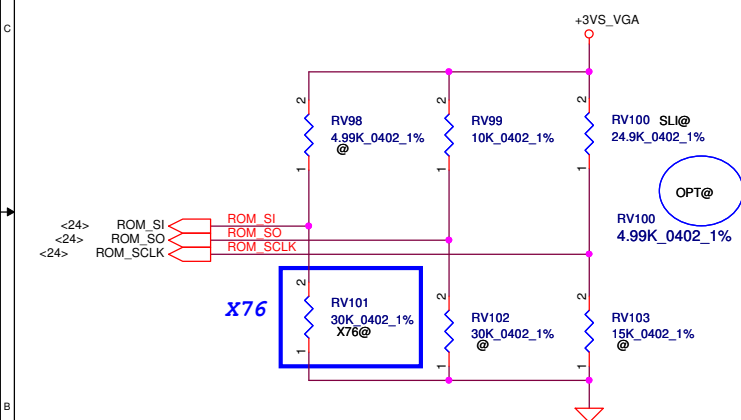
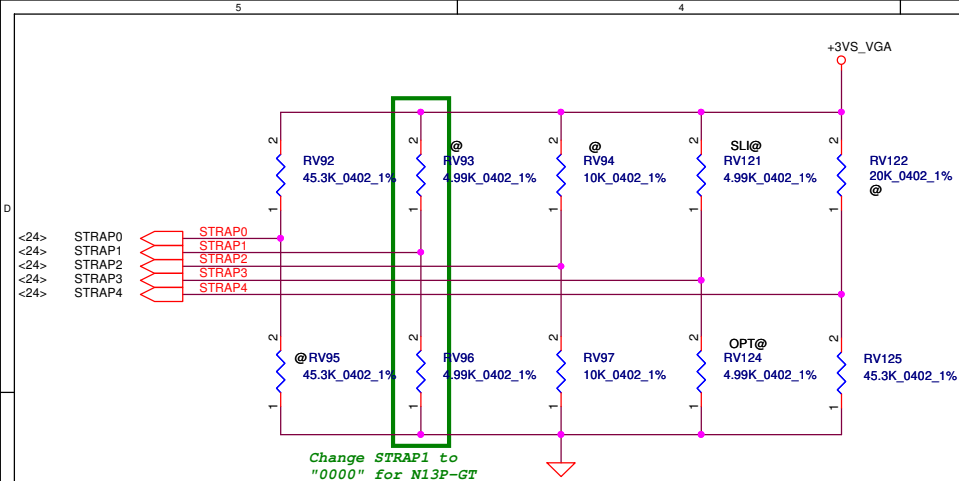


	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	ABI#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RAS#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17		A3_BA3
FbX_CMD18		A2_BA0
FbX_CMD19		A4_BA2
FbX_CMD20		A5_BA1
FbX_CMD21		WE#
FbX_CMD22		A7_A8
FbX_CMD23		A6_A11
FbX_CMD24		ABI#
FbX_CMD25		A12_RFU
FbX_CMD26		A0_A10
FbX_CMD27		A1_A9
FbX_CMD28		RAS#
FbX_CMD29		RST#
FbX_CMD30		CKE#
FbX_CMD31		CAS#

Security Classification	Compel Secret Data				
Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	<i>213P-VRAM A Upper</i> <i>Y148A18691P</i>
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				Sheet	29 of 65



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				Custom	0.2
				Document Number Y490-LA8691P	
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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

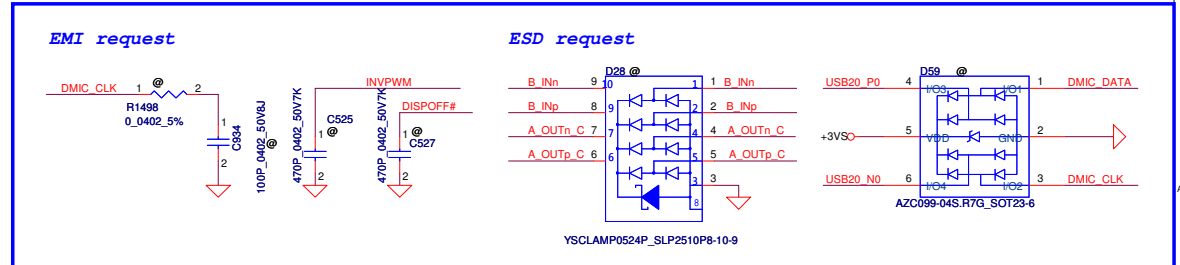
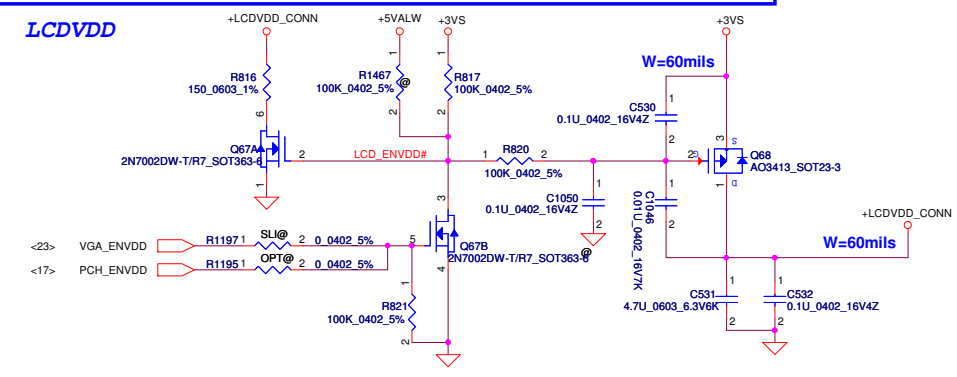
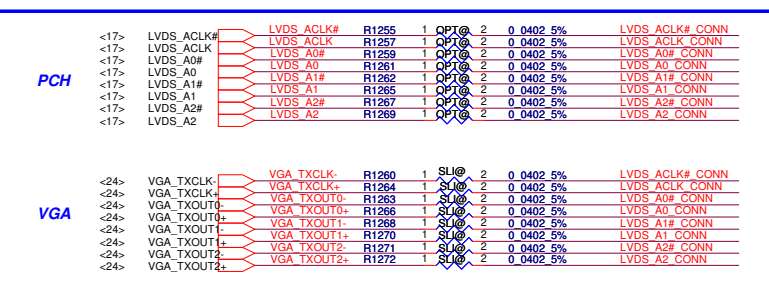
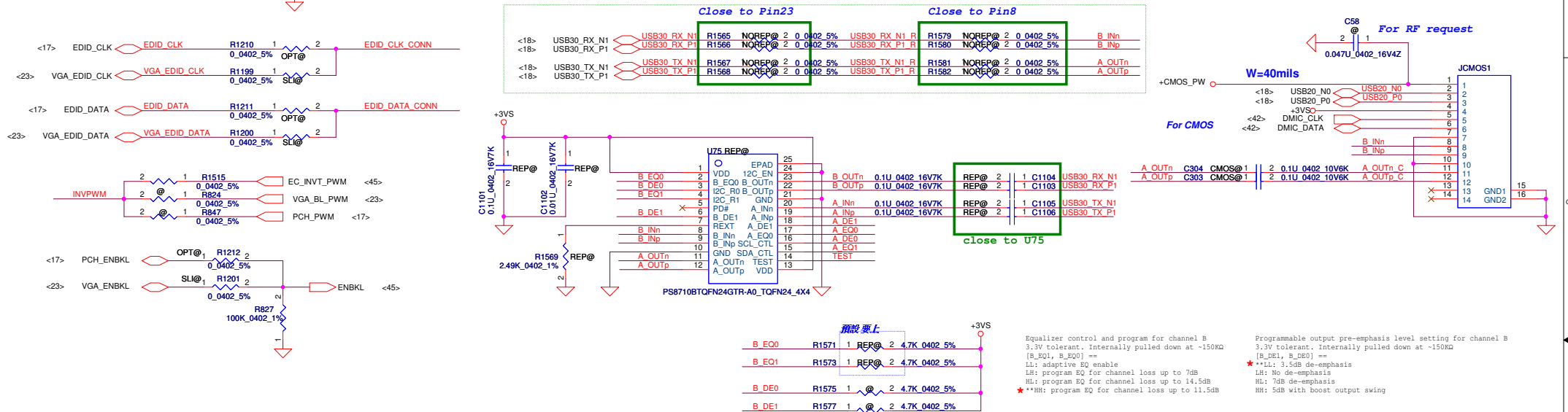
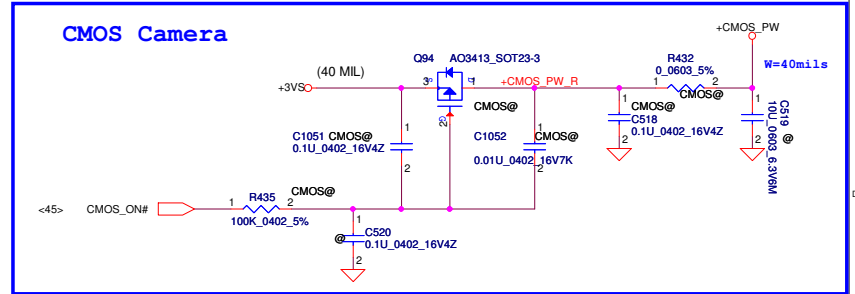
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

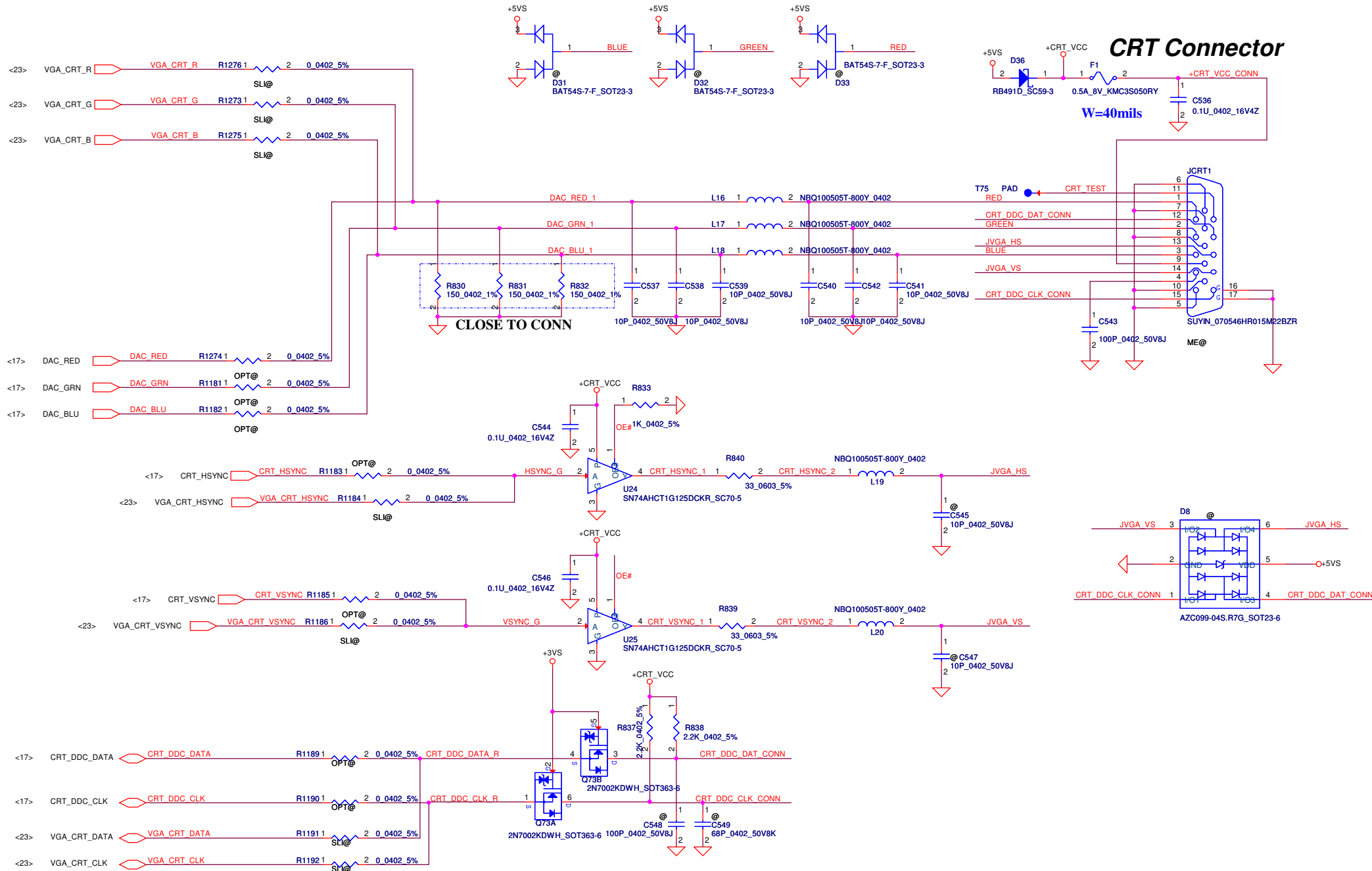
GPU		FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32		PD 30K	PU 10K	PU 25K (SLI)	PU 45K	PD 5K	PD 10K	PU 5K	PD 10K
		K4G10325FG-HC04 1G 32Mx32		PD 45K							
	Hynix	H5GQ2H24MFR-T2C 2G 64Mx32		PD 25K							
		H5GQ1H24BFR-T2C 1G 32Mx32		PD 35K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J

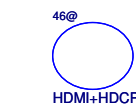
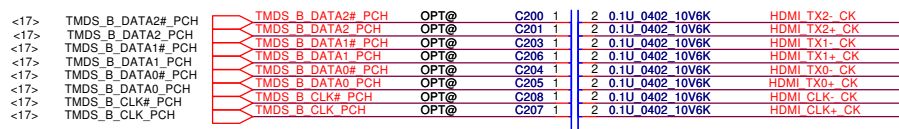
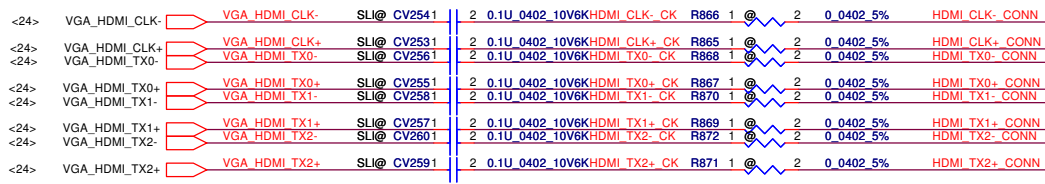
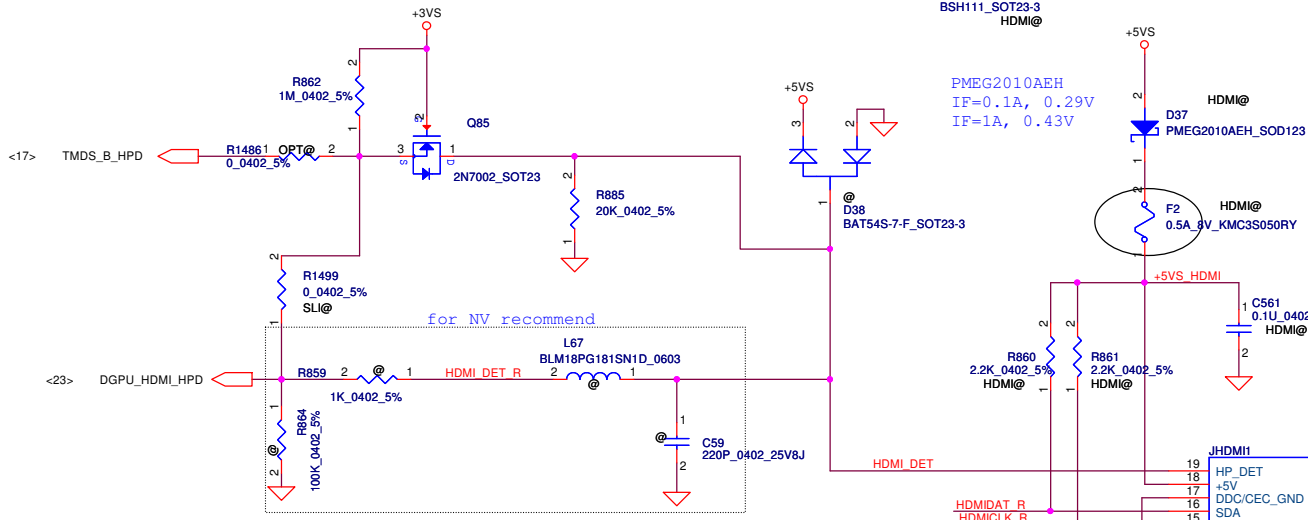
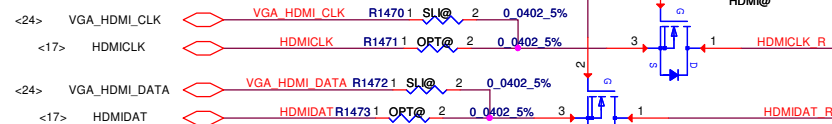
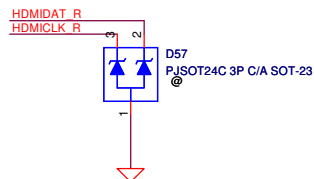
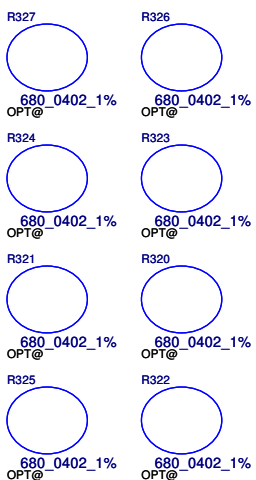
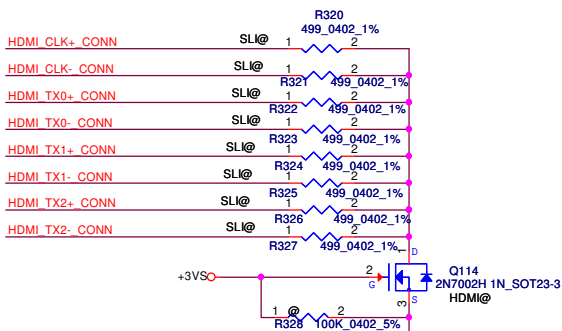
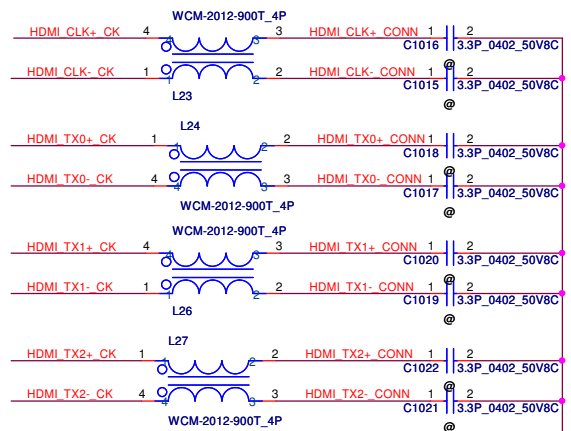
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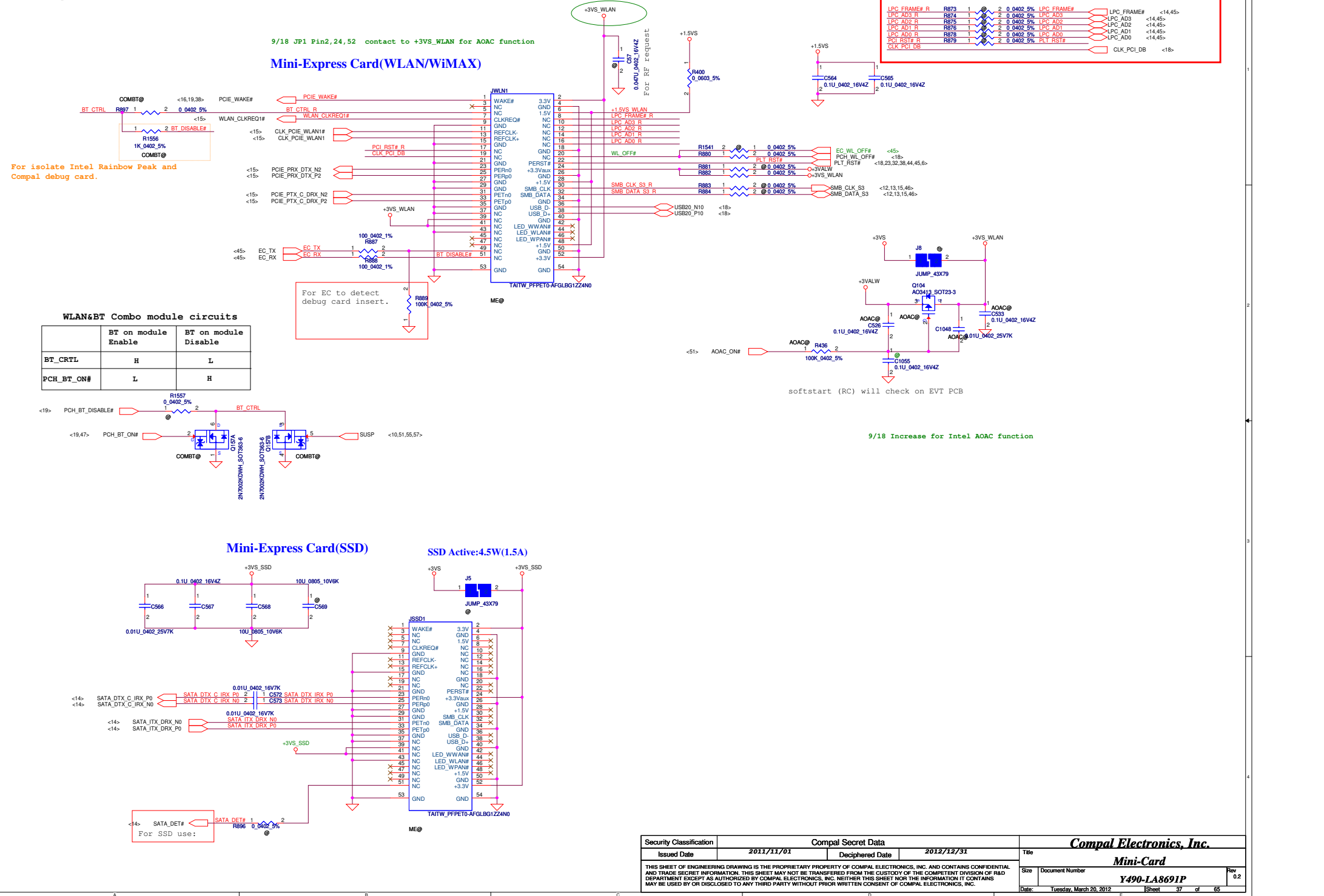


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Size	Custom	Document Number	Y490-LA8691P		Rev 0.2
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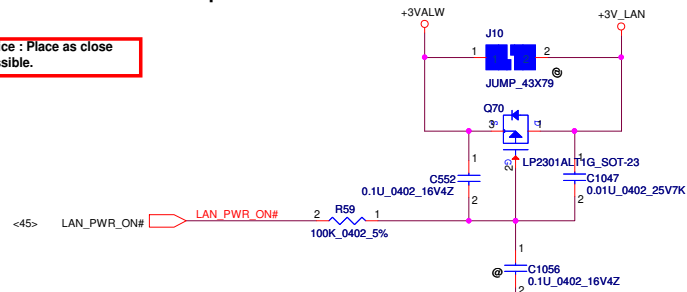
Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	
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Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

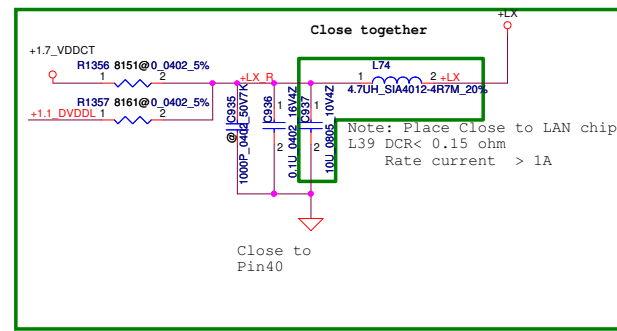
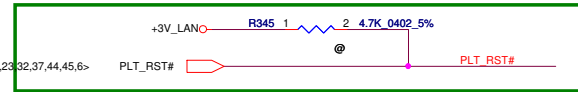


Atheros request can't disable LAN power

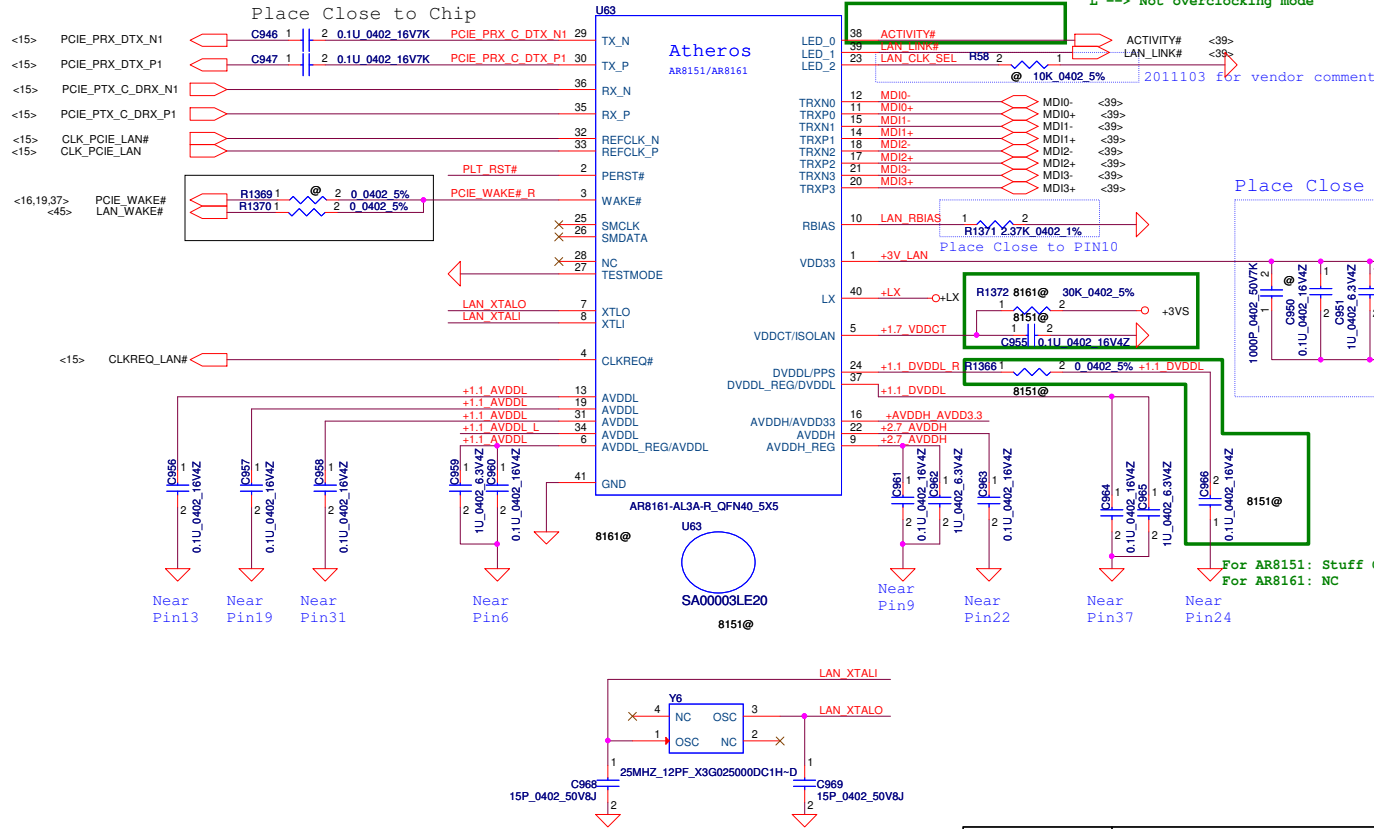
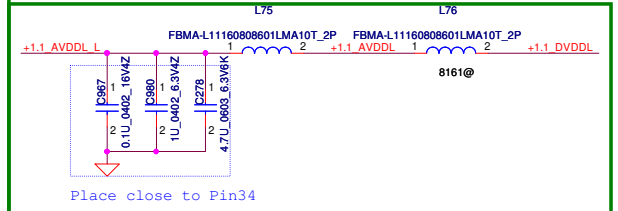
Layout Notice : Place as close chip as possible.



Vendor recommend reseve the
PU resistor close LAN chip

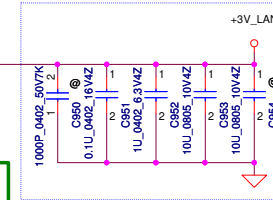


	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76

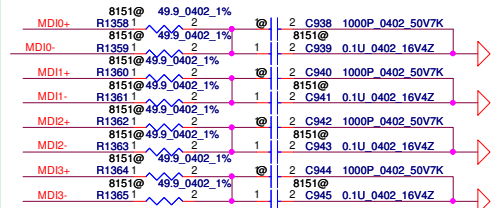


```
H --> Overclocking mode
L --> Not overclocking mode
```

Place Close to PIN1



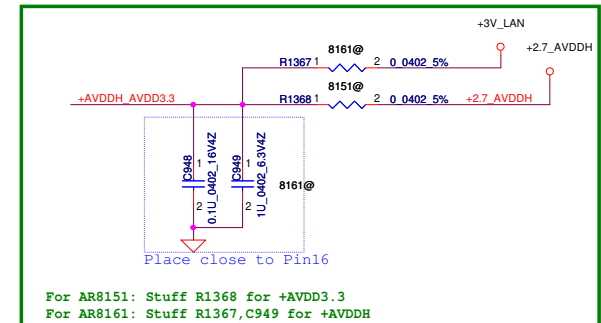
Place Close to LAN chip



Note : C938, C940, C942, 944, reserved for EMI.

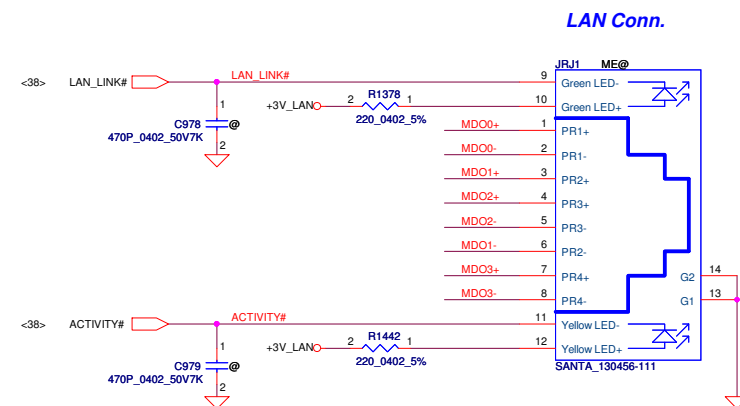
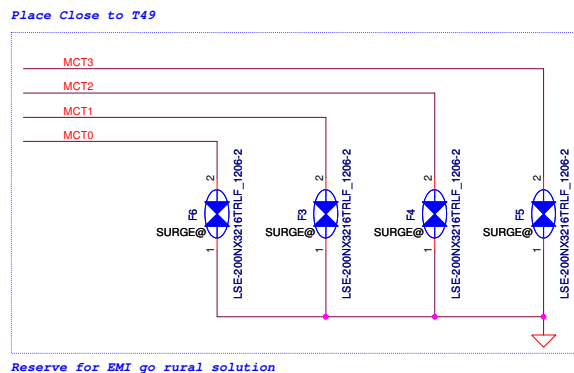
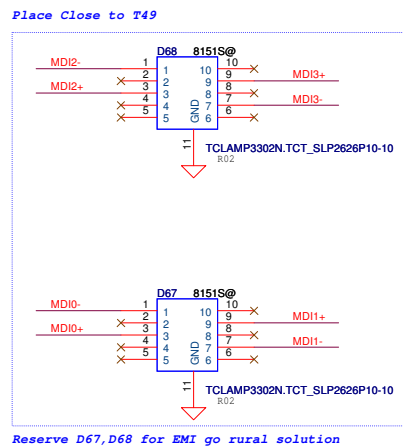
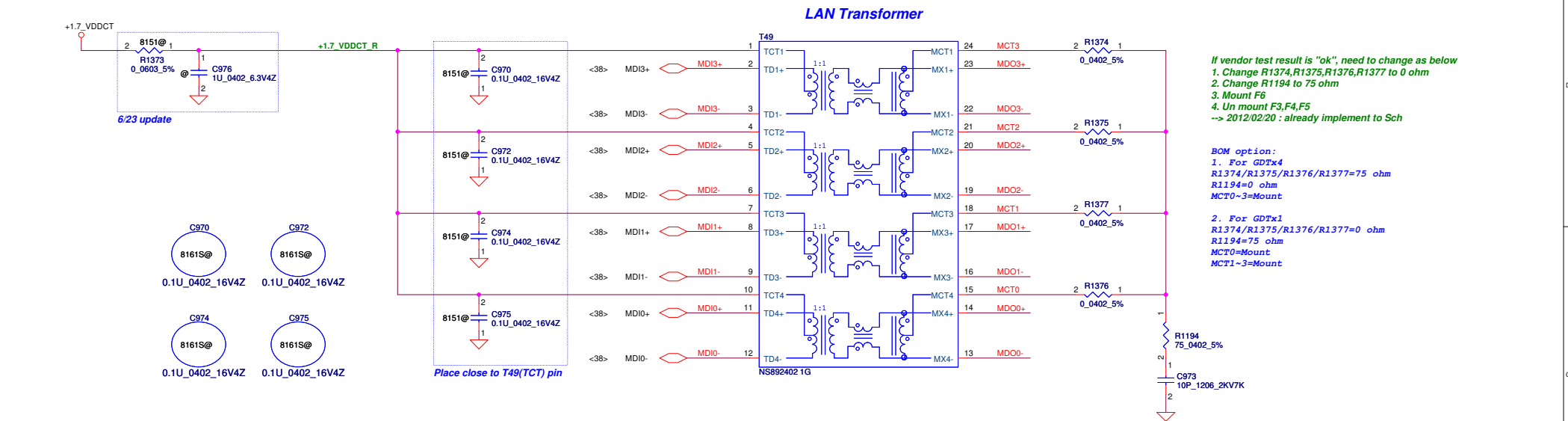
For AR8151: Stuff 49.9K and 0.1u

For AR8161: NC

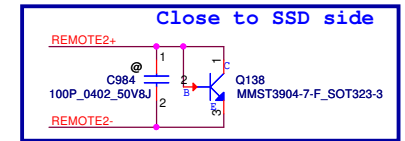
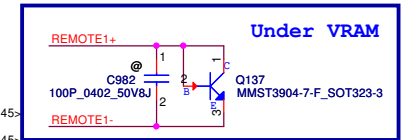
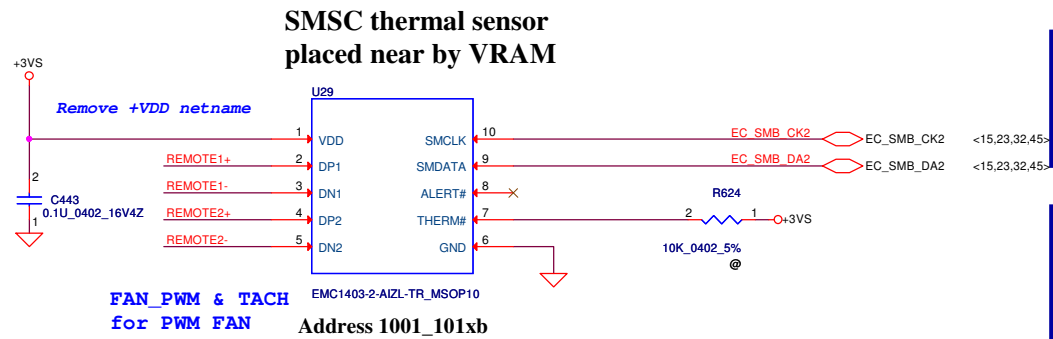
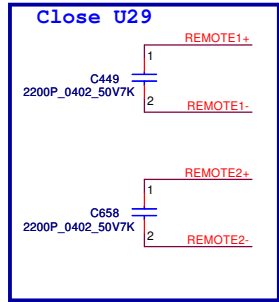


```
For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367,C949 for +AVD
```

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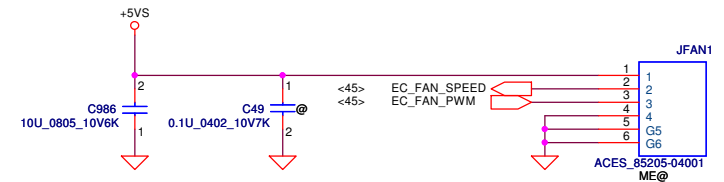
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Issued Date		2011/11/01		Deciphered Date		2012/12/31		Title			
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						Document Number		Y490-LA8691P		Rev 0.2	
						Date		Tuesday, March 20, 2012		Sheet 39 of 65	



internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

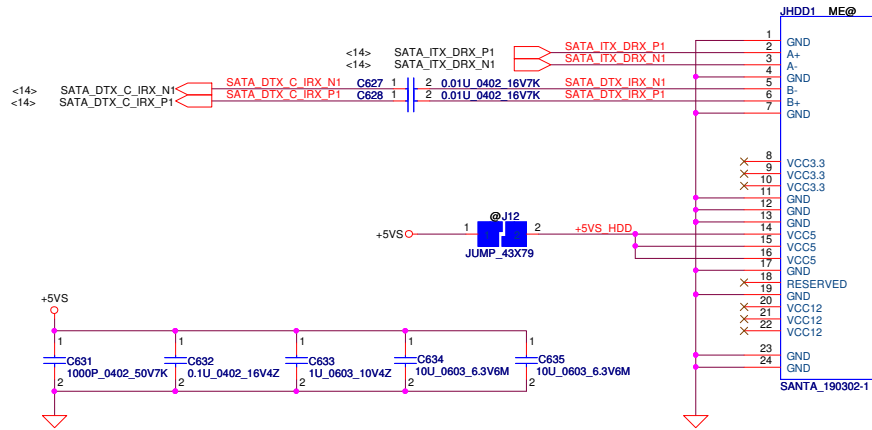
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

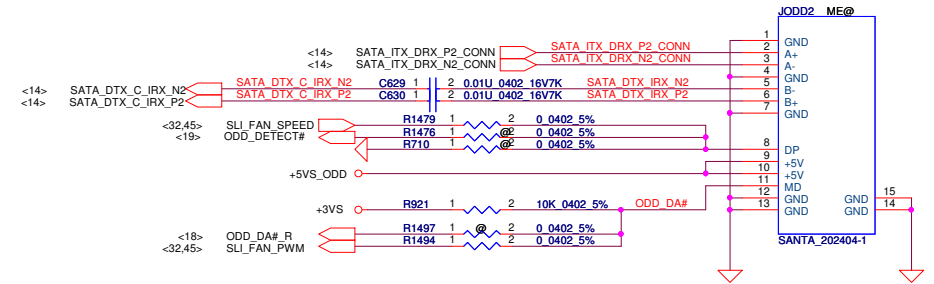


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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	
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Size	Custom	Document Number	Y490-LA8691P		Rev
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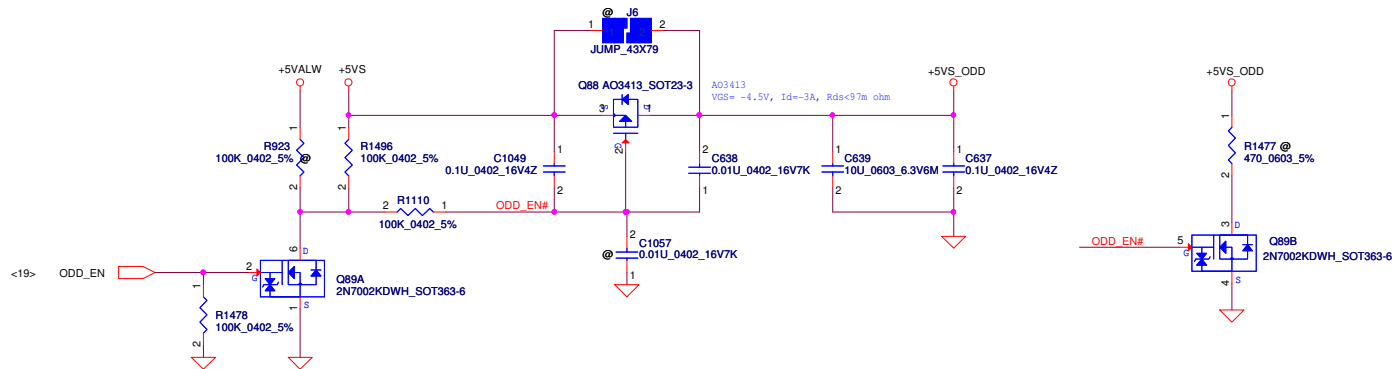
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control

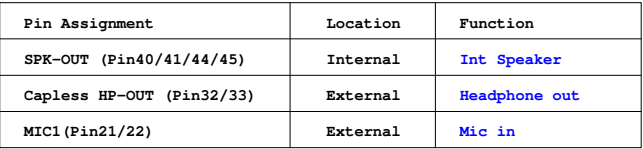


Security Classification	Compal Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2012/12/31	
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Date: Tuesday, March 20, 2012				Sheet 41 of 65

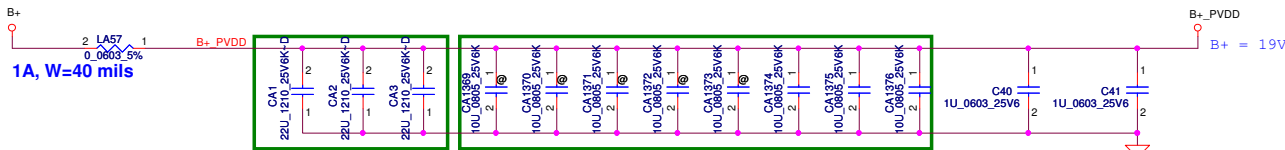
Compal Electronics, Inc.

HDD/ODD Connector

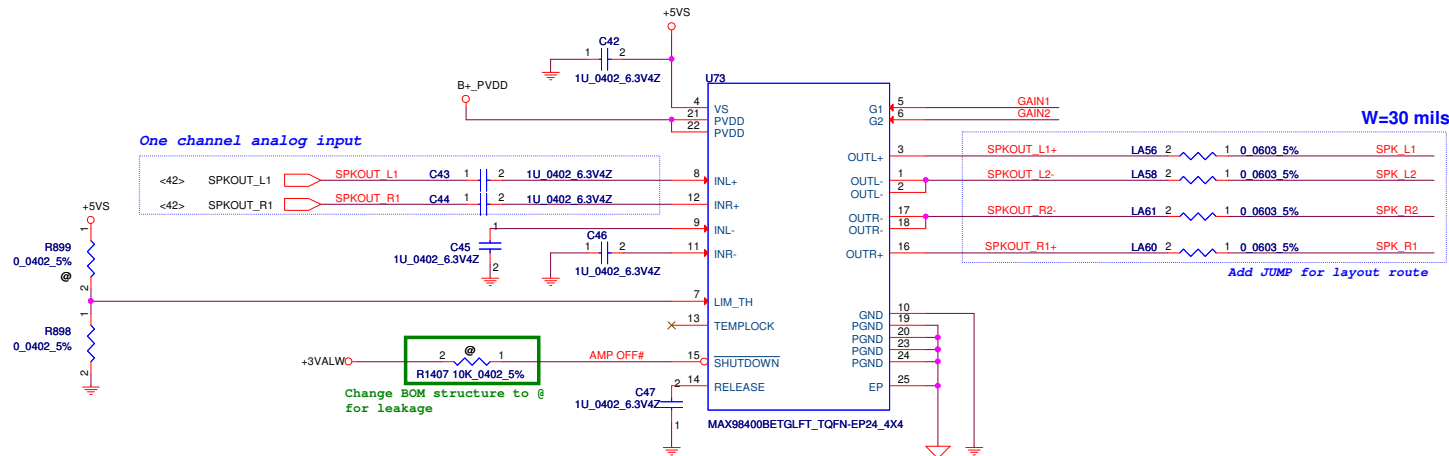
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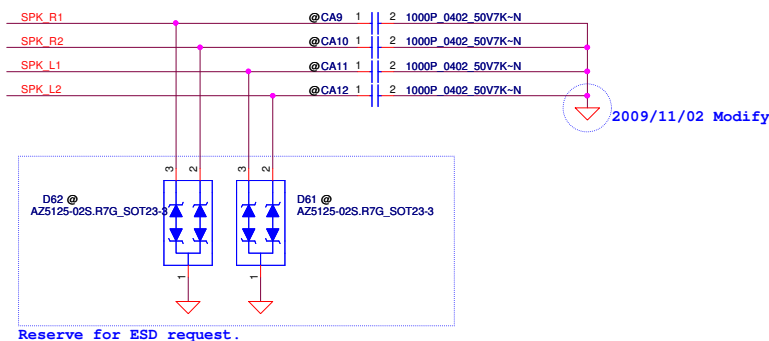
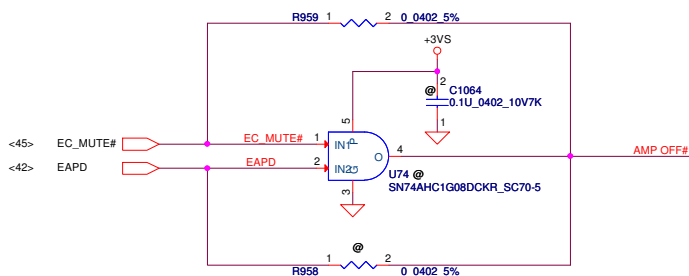
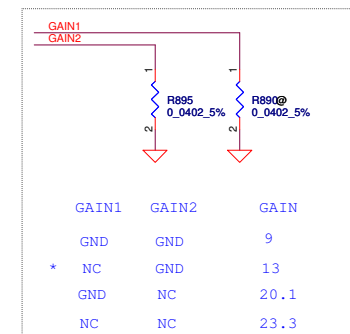
Security Classification	Compal Secret Data			Compal Electronics, Inc. HD Audio ALC269Q-VC3	
Issued Date	2011/11/01	Deciphered Date	2012/03/09	Title	
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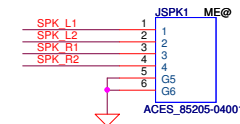
One channel analog input

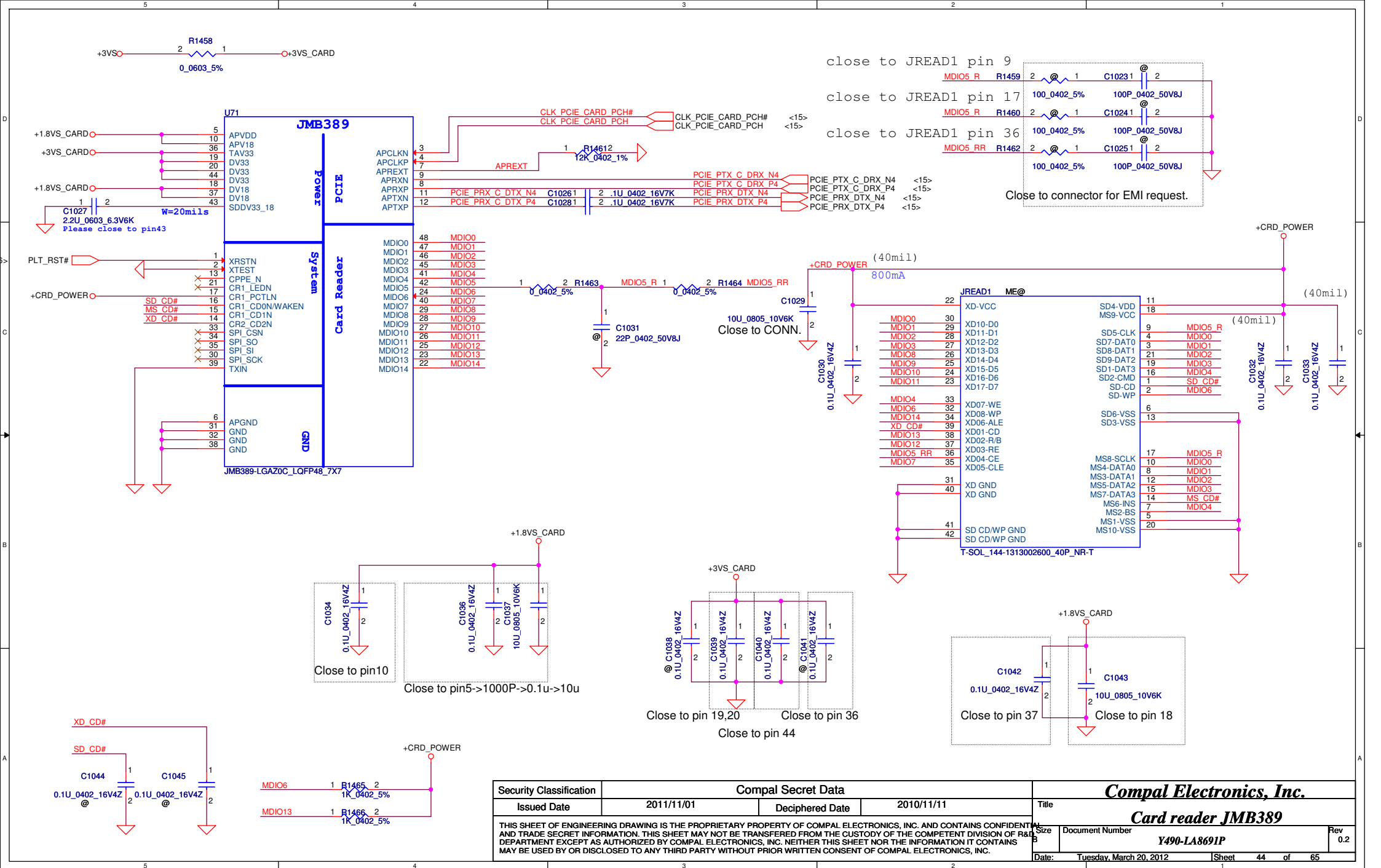


GAIN SETTING

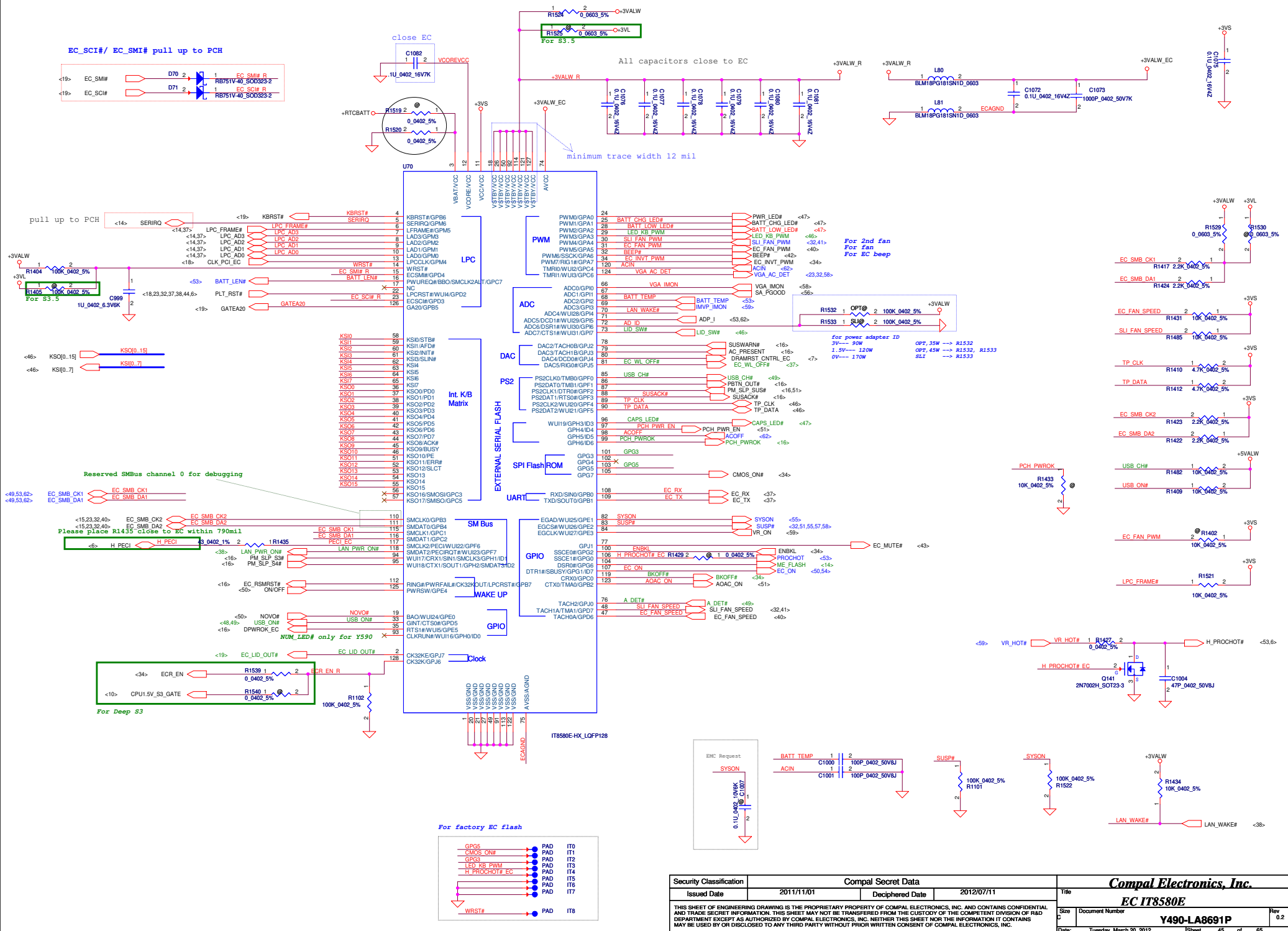


Speaker Conn.

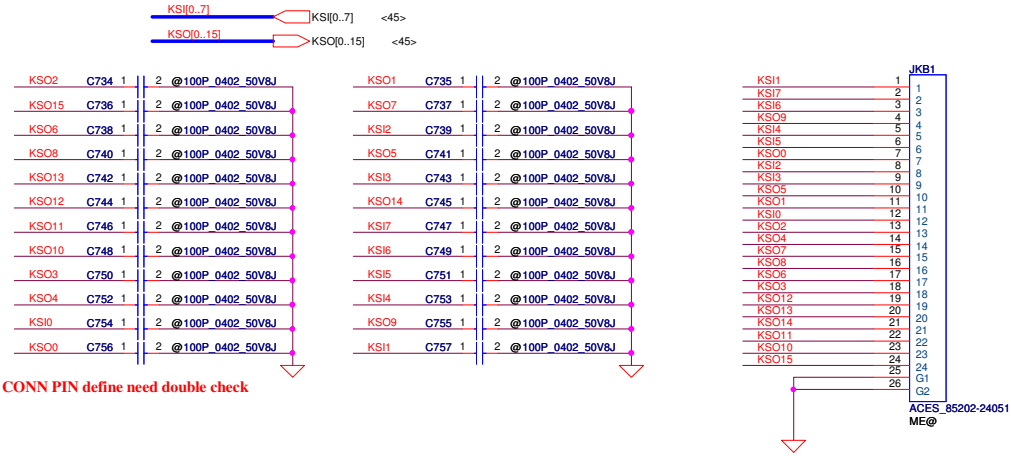




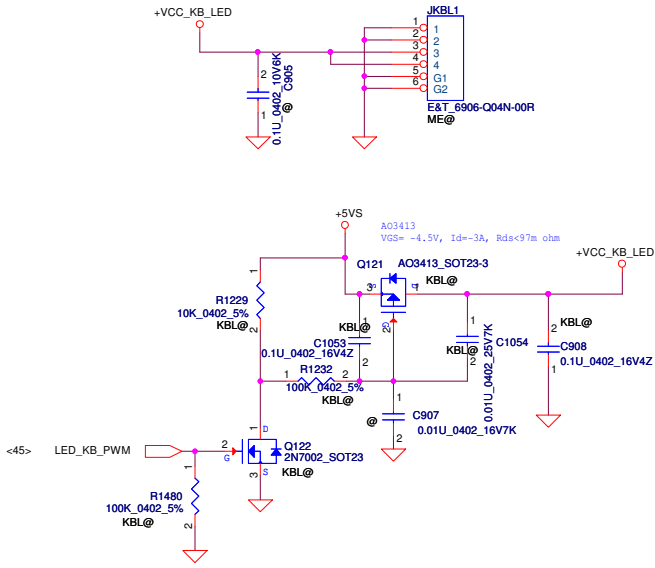
Security Classification		Compal Secret Data		Title	
Issued Date	2011/11/01	Deciphered Date	2010/11/11	Card reader JMB389	
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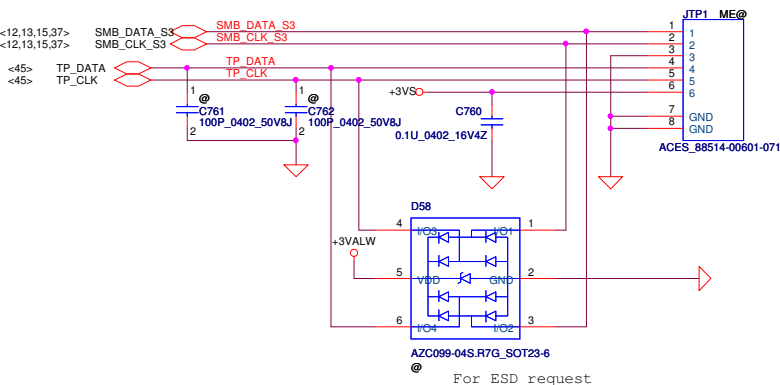
14" INT_KBD Conn.



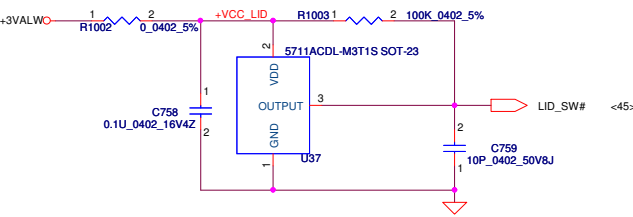
KB Lighting CONN.4pin

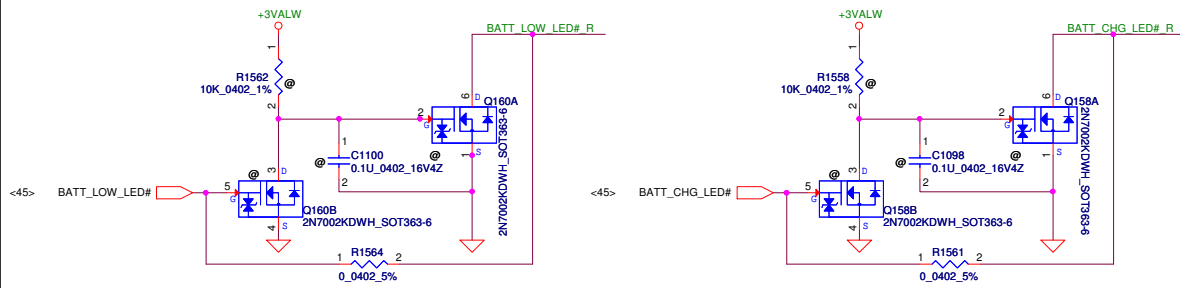


To TP/B Conn.

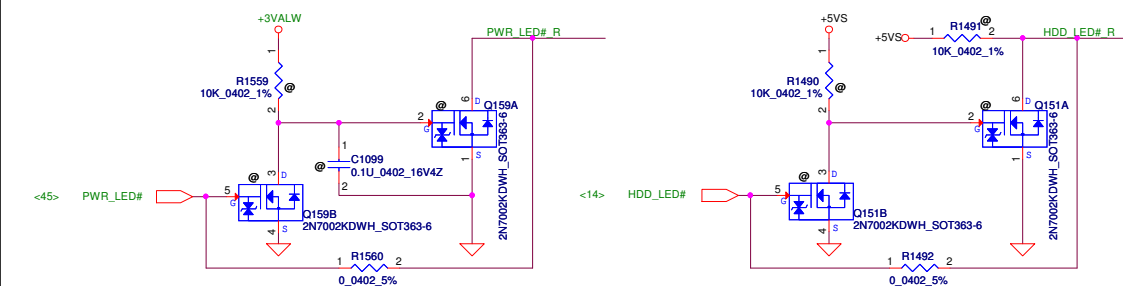
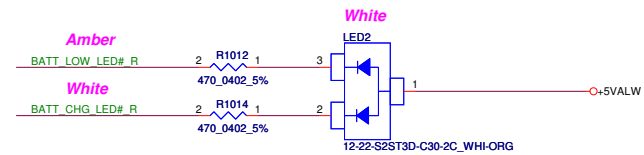


Lid Switch

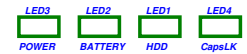
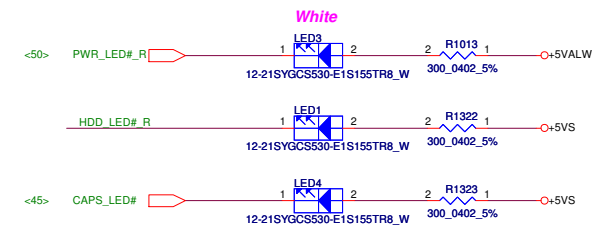




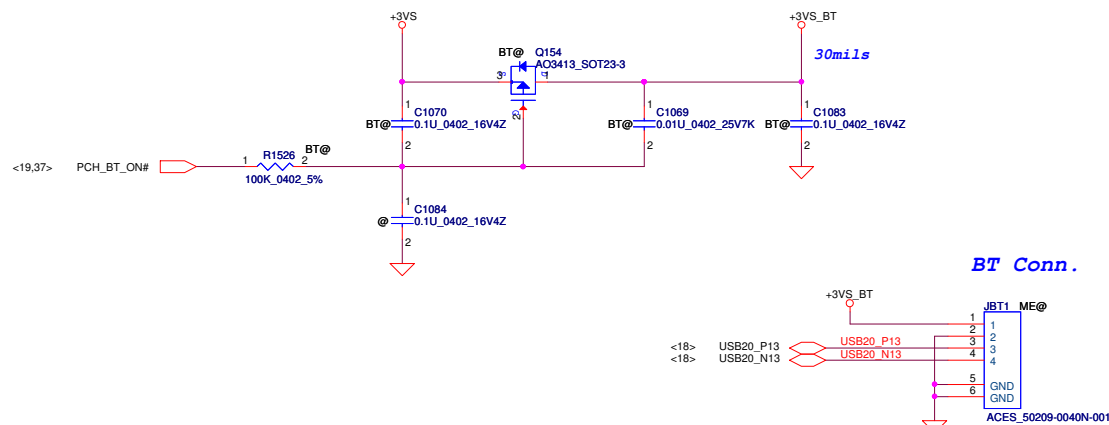
BATT CHARGE/LOW LED



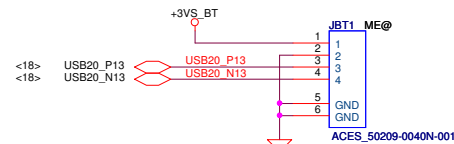
PWR LED HDD LED CapsLK LED



BlueTooth DC



BT Conn.



PCB Fedcal Mark PAD



Screw Hole

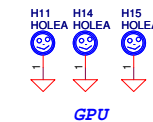
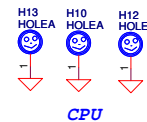
CPU and GPU: H_3P8X 6

C: H_3P8X 3

B: H_3P8X 3

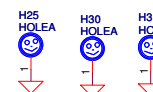
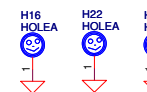
MIN PCIE: H_3P3 X 1

E: H_3P3X 1



ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

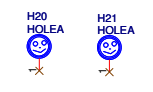
A: H_2P8X 8



E: H_3P3X 1

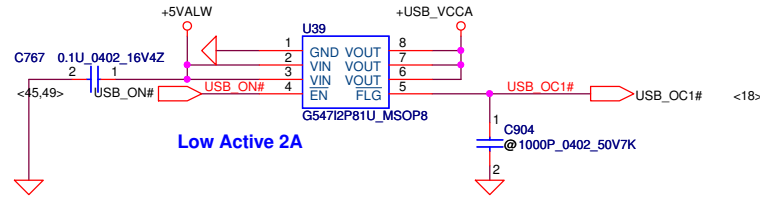
H_4P0X3P0NX 3

H_2P0X 2

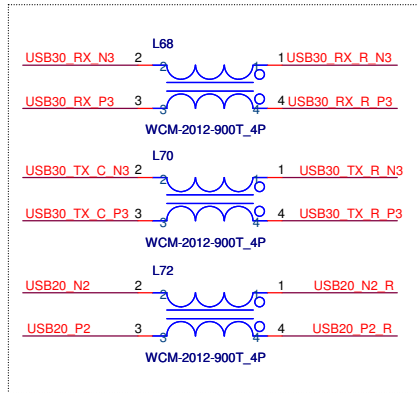


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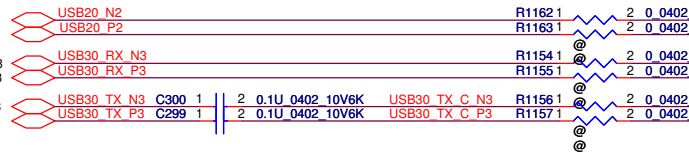
LEFT SIDE USB3.0 PORT X1



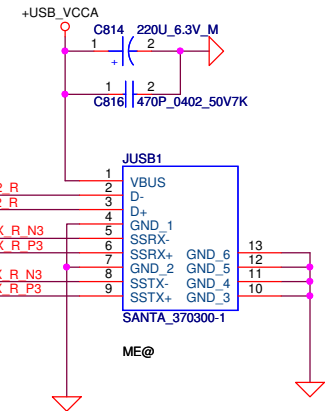
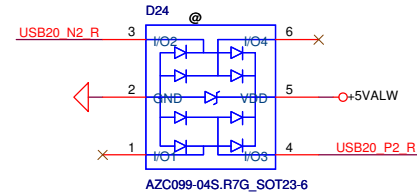
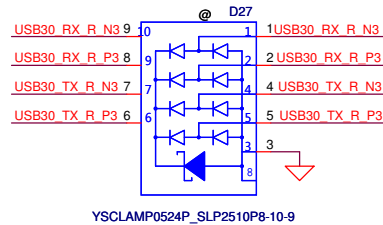
For EMI request
 USB2.0 choke --> SM070000I00
 USB3.0 Choke --> SM070001U00



<18> USB20_N2
 <18> USB20_P2
 <18> USB30_RX_N3
 <18> USB30_RX_P3
 <18> USB30_TX_N3
 <18> USB30_TX_P3



For ESD request



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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	USB3.0 ports
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Right side USB Charger Port (USB_Port5, near JMIC1)



	M1	M2	EM_EN	ACTIVE	MODE	
*	0	0	1	Dedicated	Charger	Emulation Cycle
	0	1	0	Date	Pass-through	
	0	1	0	BC1.2	DCP	
	1	0	1	BC1.2	SDP	
	1	0	1	Dedicated	Charger	Emulation Cycle
	1	1	0	Date	Pass-through	
	1	1	1	BC1.2	CDP	

SEL Pin Decode

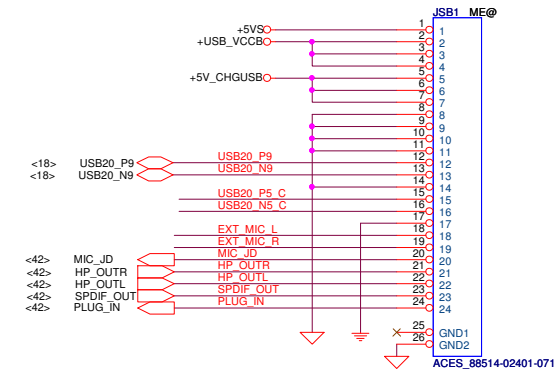
- Pull Low
- OR-500mA
- 10K-900mA
- 12K-1000mA
- 15K-1200mA
- 18K-1500mA
- 22K-1800mA
- 27K-2000mA
- ★ 33K-2500mA

```

Pull Low
0R -1010_000
* 10K-1010_000
12K-1010_000
15K-1010_000
18K-0110_000
22K-0110_000
27K-0110_000
33K-0110_000

```

AUDIO/B Conn.



need change to 無錫 material
COMPAL : SP010015W1J
Footprint : 88514-0240N-071

EXT. MIC

+MIC1_VREFO_L

Remove Diode (DA1, DA2)

RA1622
2.2K_0402_5%

RA1623
2.2K_0402_5%

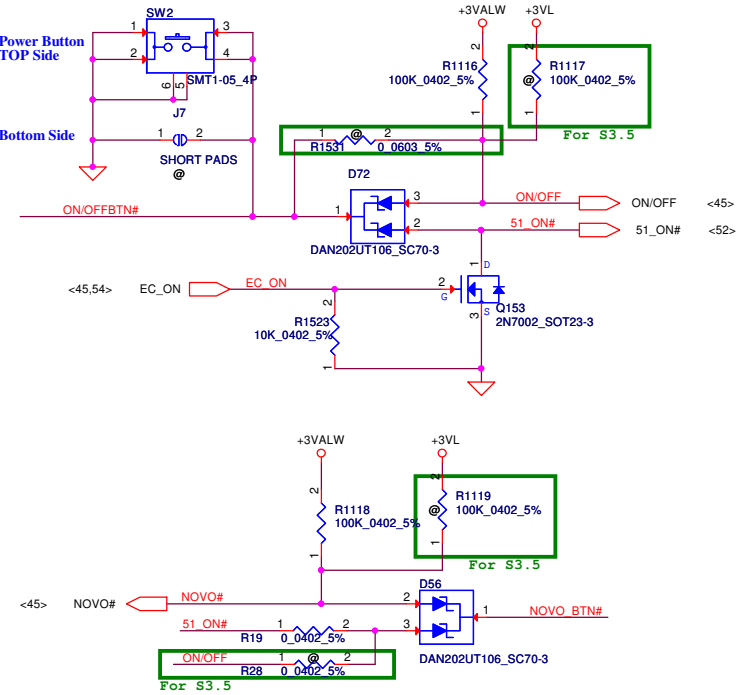
1K_0402_5%

<42> MIC2_R RA1634 2 1K_0402_5% EXT_MIC_R

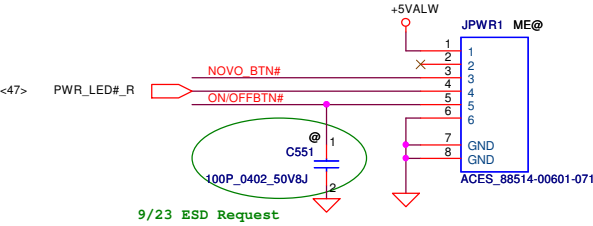
<42> MIC1_R RA1633 2 1K_0402_5% EXT_MIC_L

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Issued Date	2011/11/01	Deciphered Date	2012/12/31	Title	Audio B Conn/USB charger
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				Document Number	0.2
Date: Tuesday, March 20, 2012				Sheet	49 of 65

ON/OFF switch



Power Button/B link
to Function/B Conn. 10pin

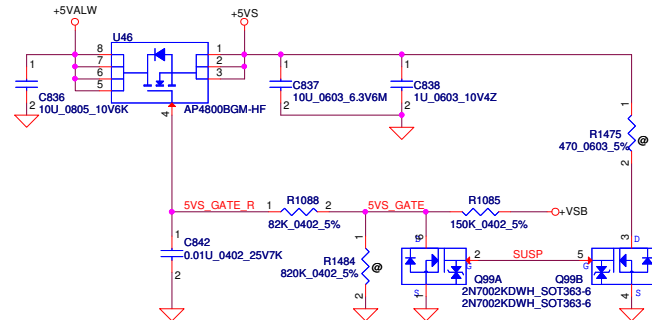


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

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Size Custom	Document Number			Y490-LA8691P	Rev 0.2
Date:	Tuesday, March 20, 2012	Sheet	50	of	65

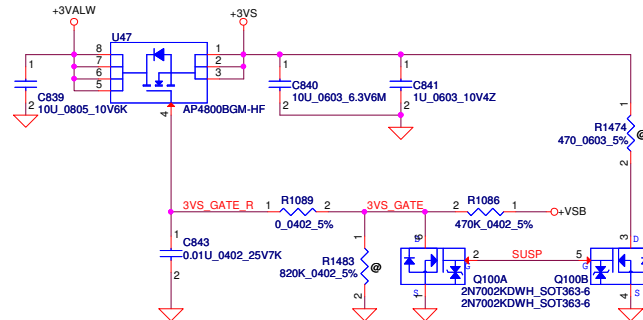
+5VALW to +5VS

AP4800BGM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V

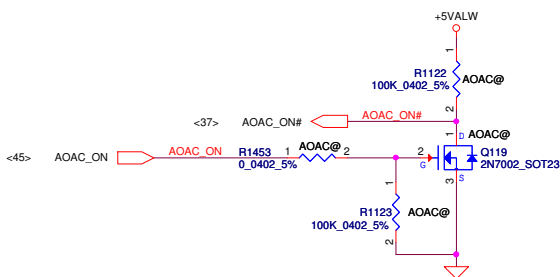
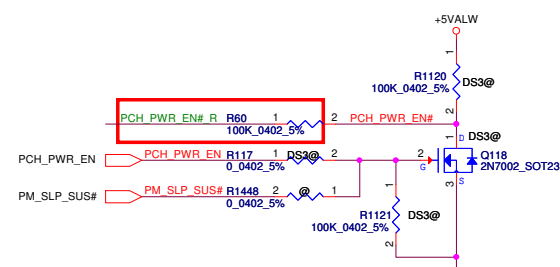
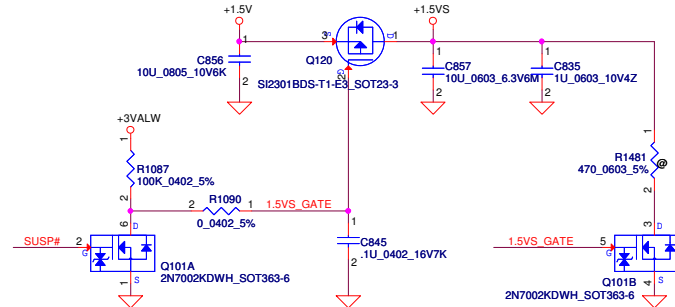
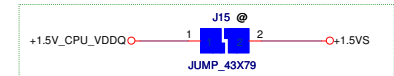


+3VALW to +3VS

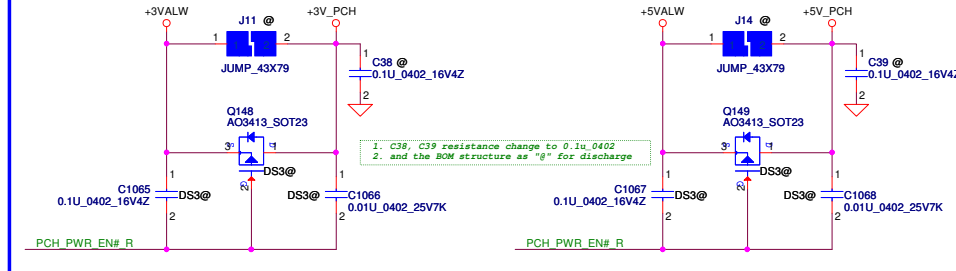
AP4800BGM
VGS=10V, ID=9A, Rds=18m ohm
VGS=-25V



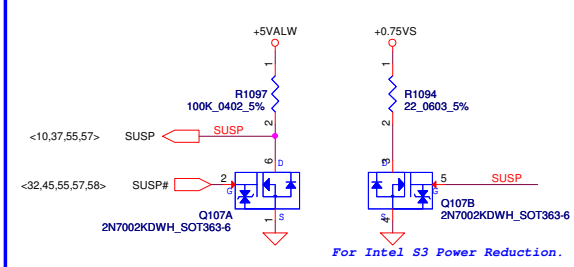
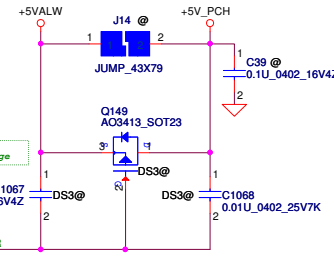
+1.5V to +1.5VS



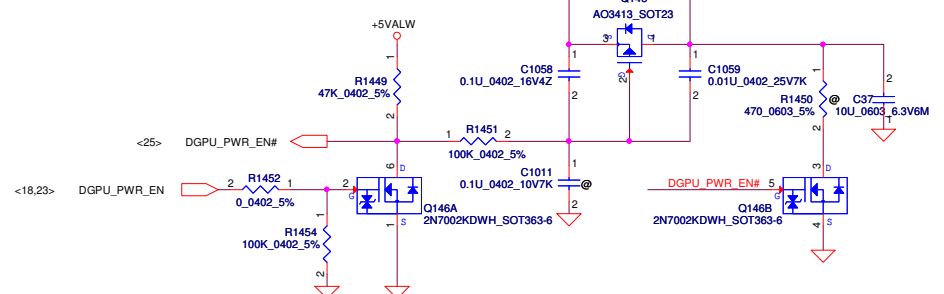
+3VALW to +3V_PCH



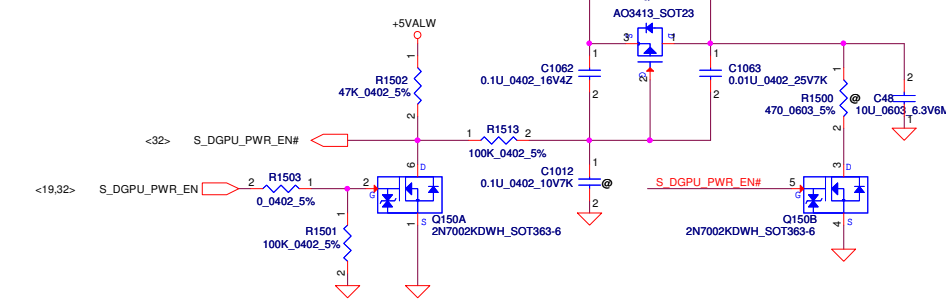
+5VALW to +5V_PCH



+3VS to +3VS_VGA

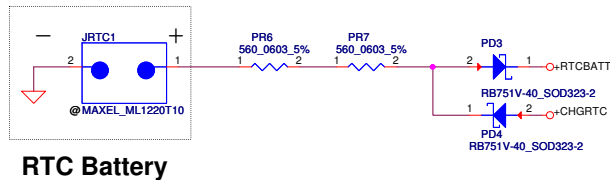
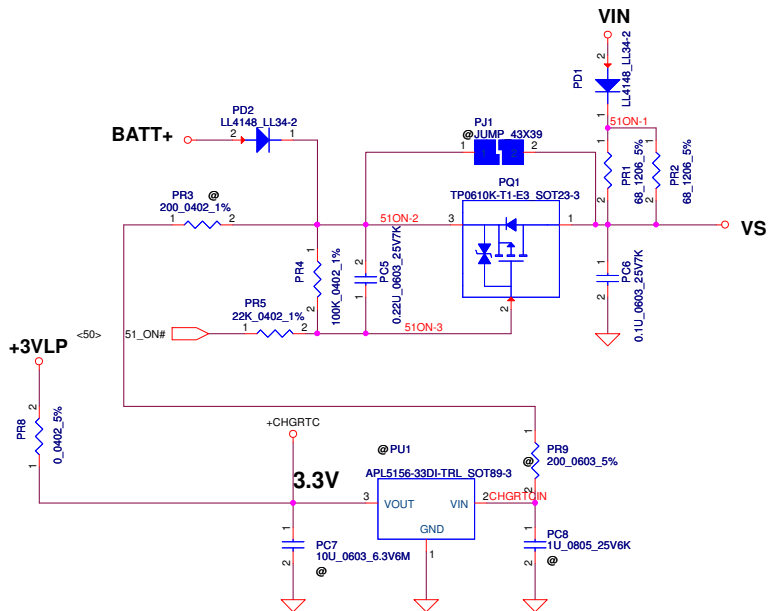
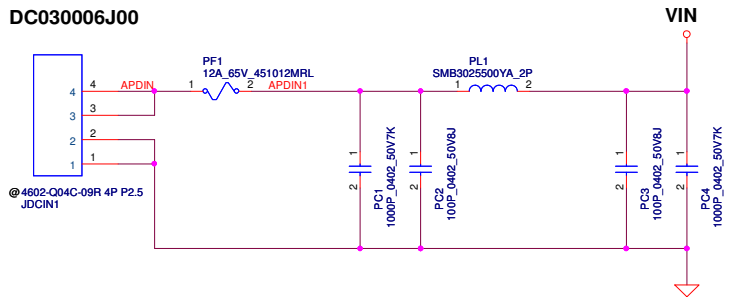


+3VS to +3VS_SLI

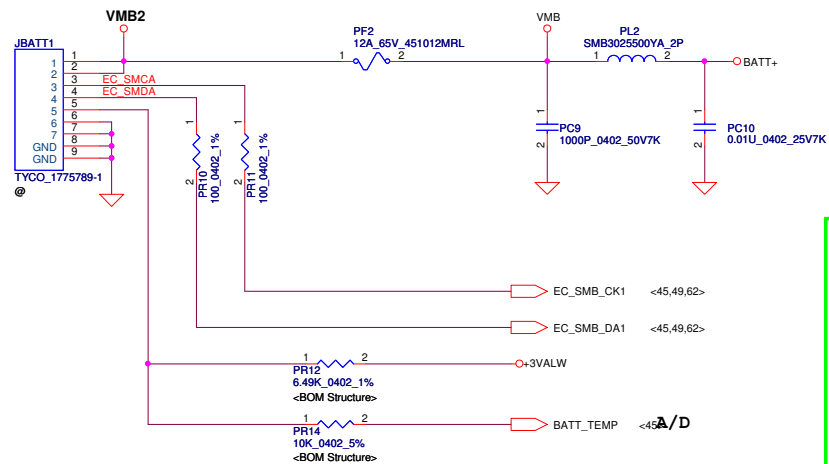


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Issued Date				2011/11/01				DC Interface			
Deciphered Date				2012/12/31				Y490-LA8691P			
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DC030006J00



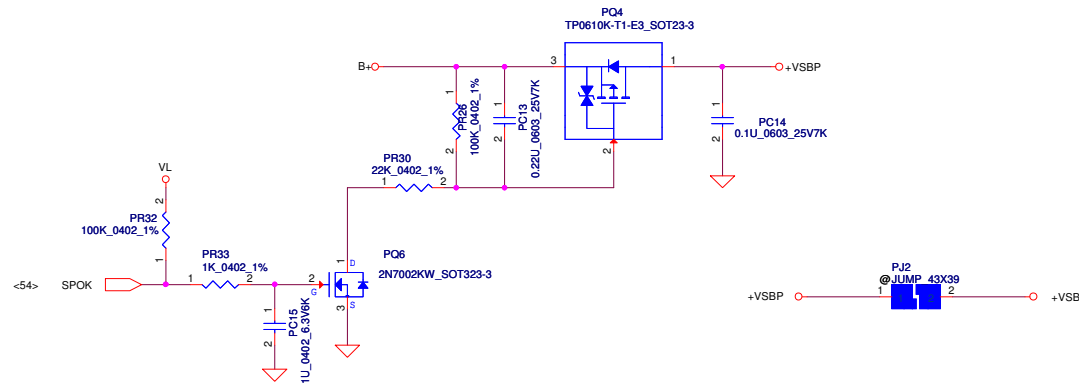
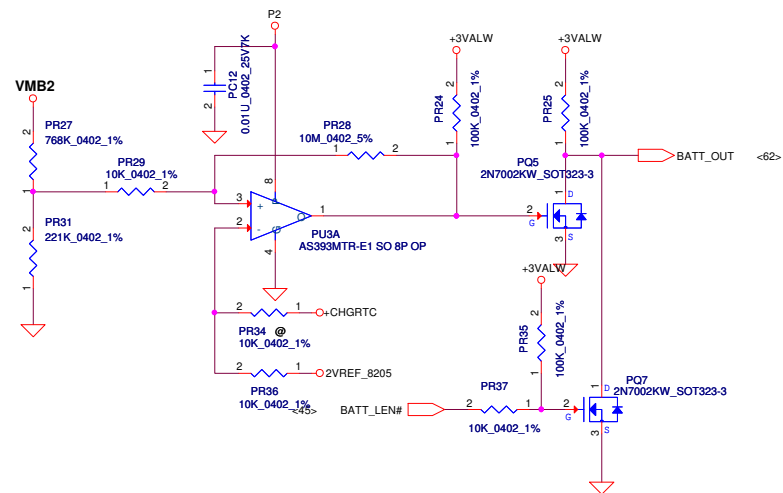
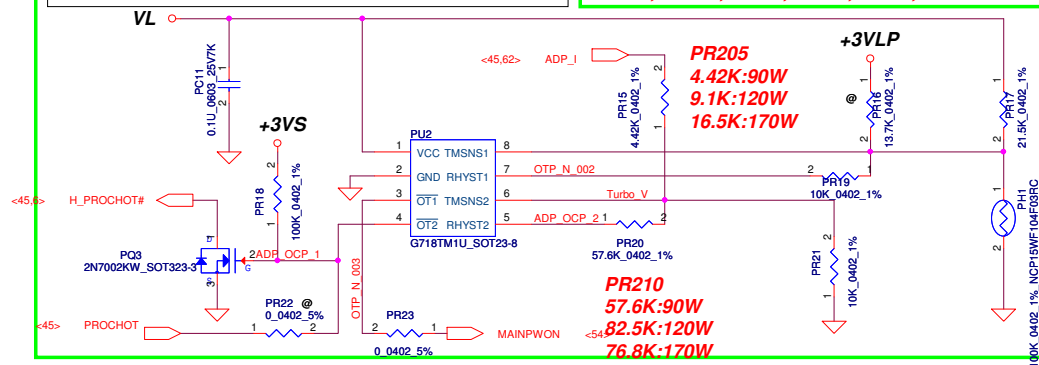
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2012/12/31	Title	Vin Detector
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PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +3 degree C

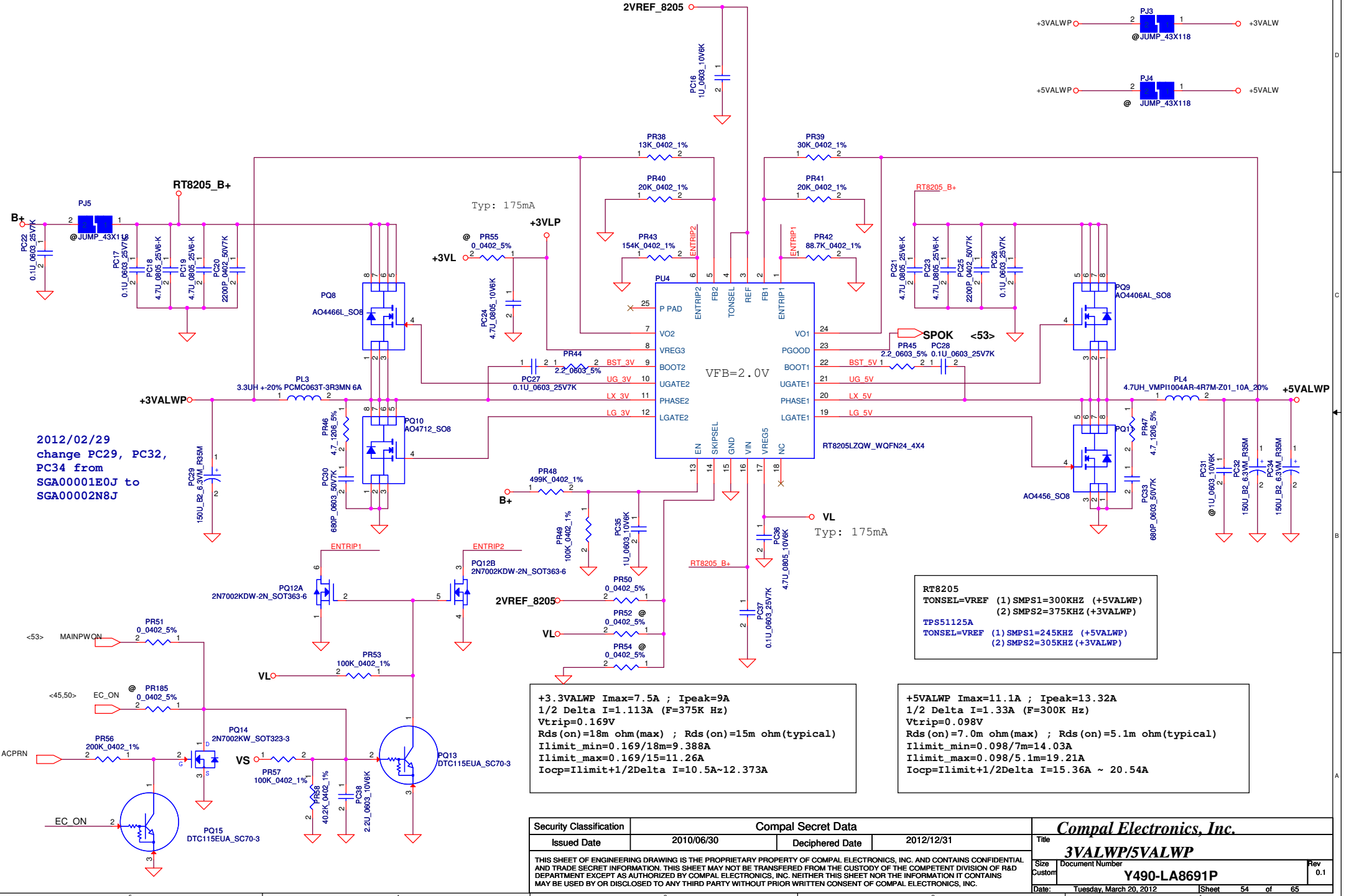
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 (Red square) --> Remove PU1 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



2012/02/29
change PC29, PC32,
PC34 from
SGA00001E0J to
SGA00002N8J

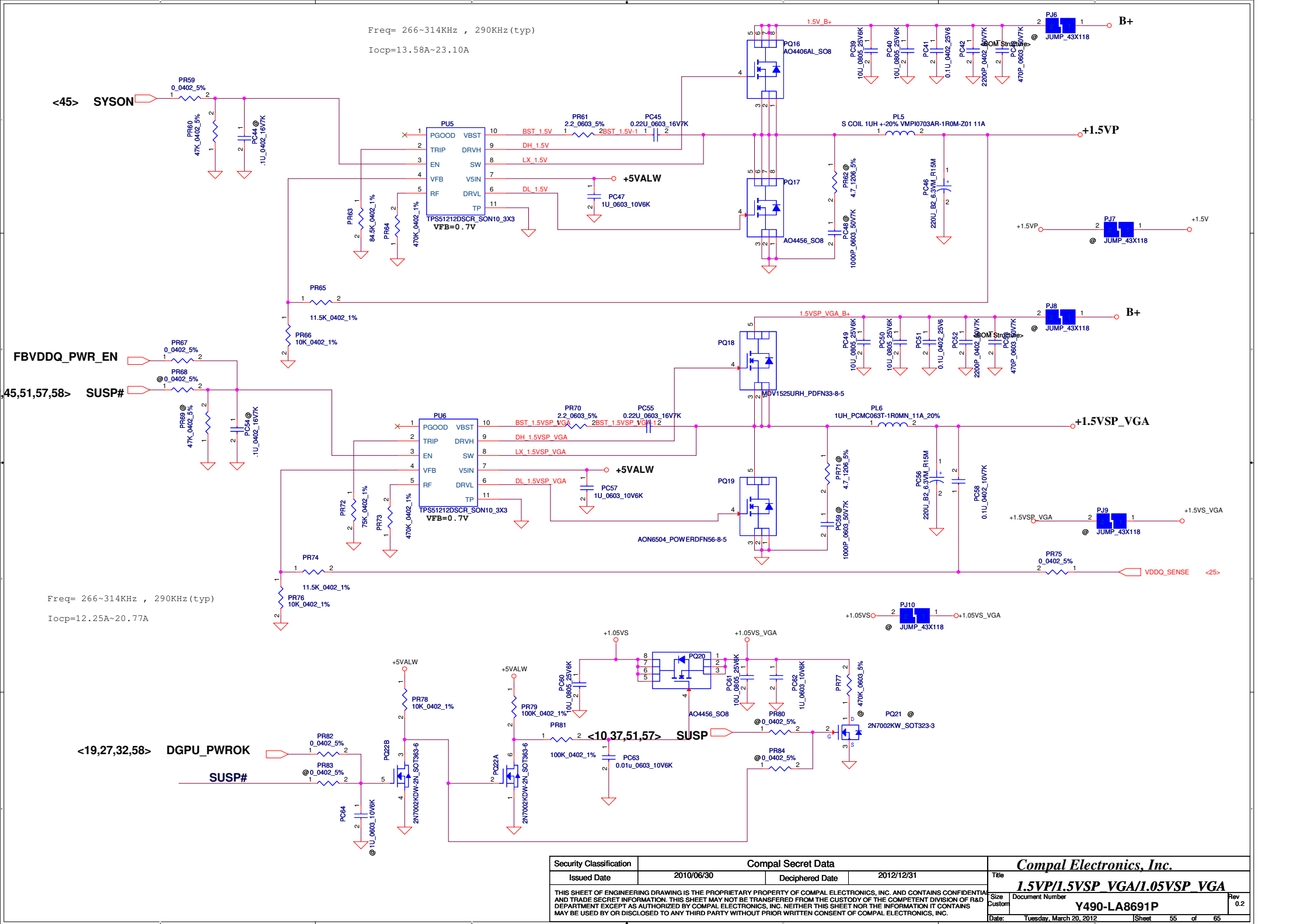
RT8205
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)
TPS51125A
TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
(2) SMPS2=305KHZ (+3VALWP)

+3.3VALWP I_{max}=7.5A ; I_{peak}=9A
1/2 Delta I=1.113A (F=375K Hz)
V_{trip}=0.169V
R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
I_{limit_min}=0.169/18m=9.388A
I_{limit_max}=0.169/15=11.26A
I_{ocp}=I_{limit}+1/2Delta I=10.5A~12.373A

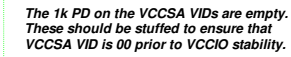
+5VALWP I_{max}=11.1A ; I_{peak}=13.32A
1/2 Delta I=1.33A (F=300K Hz)
V_{trip}=0.098V
R_{ds(on)}=7.0m ohm(max) ; R_{ds(on)}=5.1m ohm(typical)
I_{limit_min}=0.098/7m=14.03A
I_{limit_max}=0.098/5.1m=19.21A
I_{ocp}=I_{limit}+1/2Delta I=15.36A ~ 20.54A

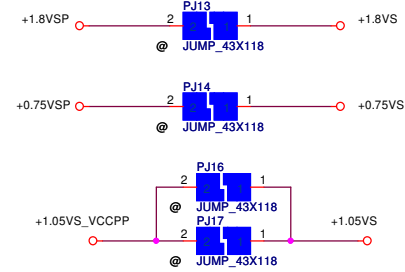
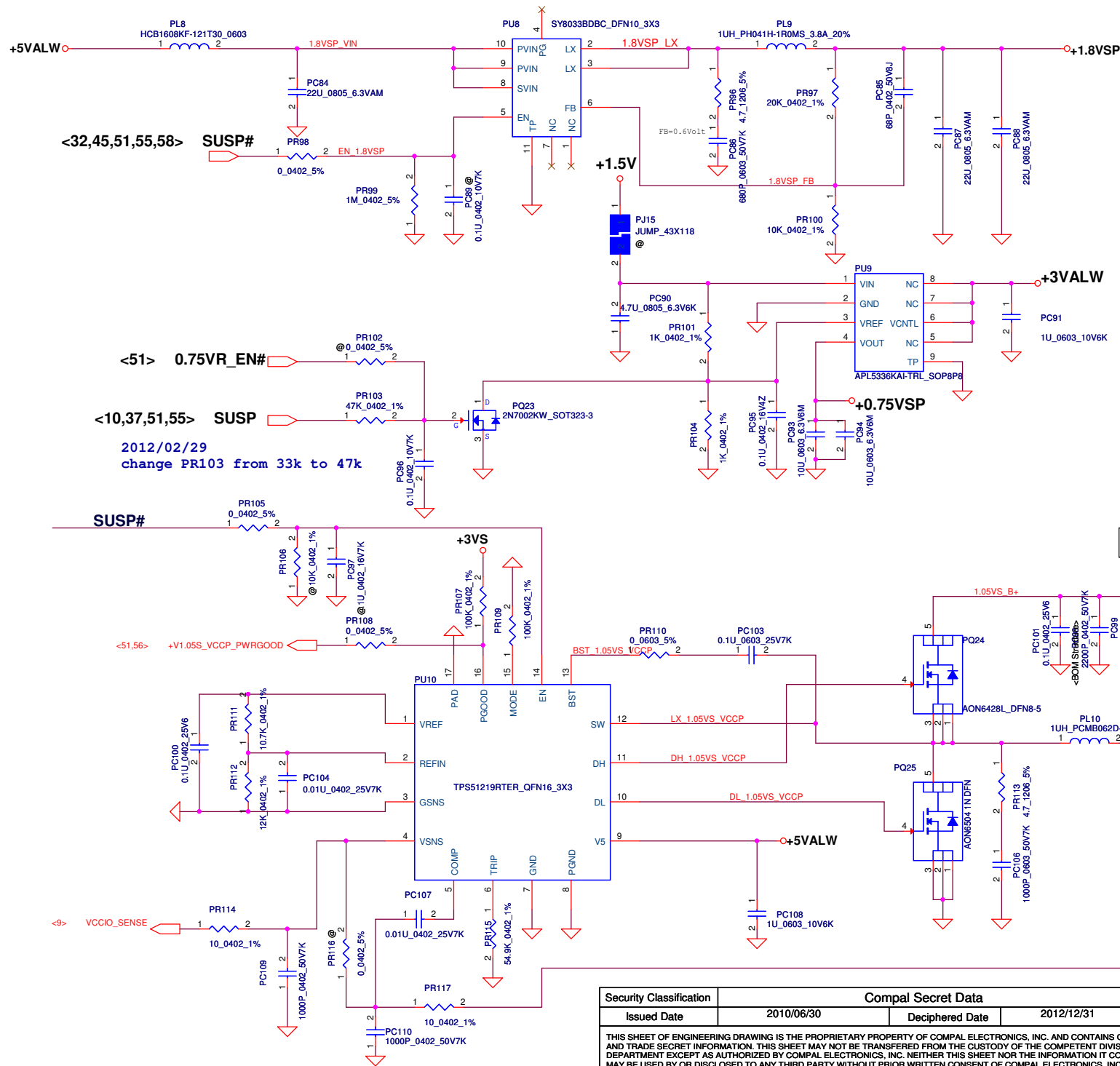
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title	3VALWP/5VALWP
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Freq= 266~314KHz , 290KHz(typ)
Iocp=13.58A~23.10A



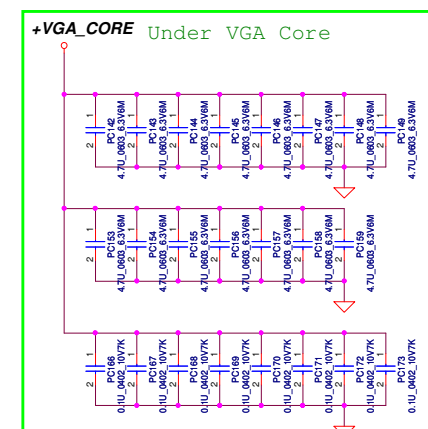
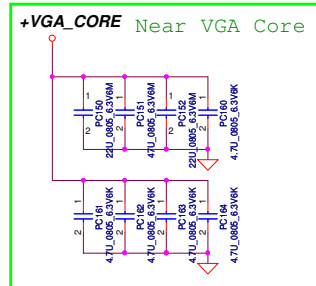
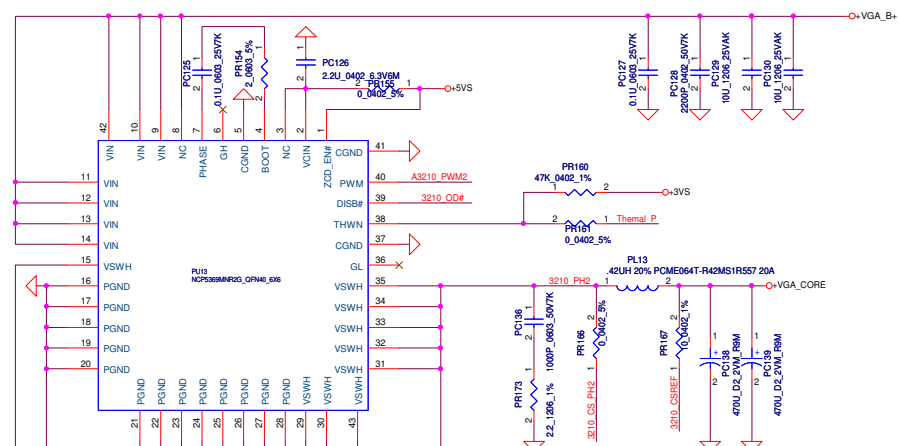
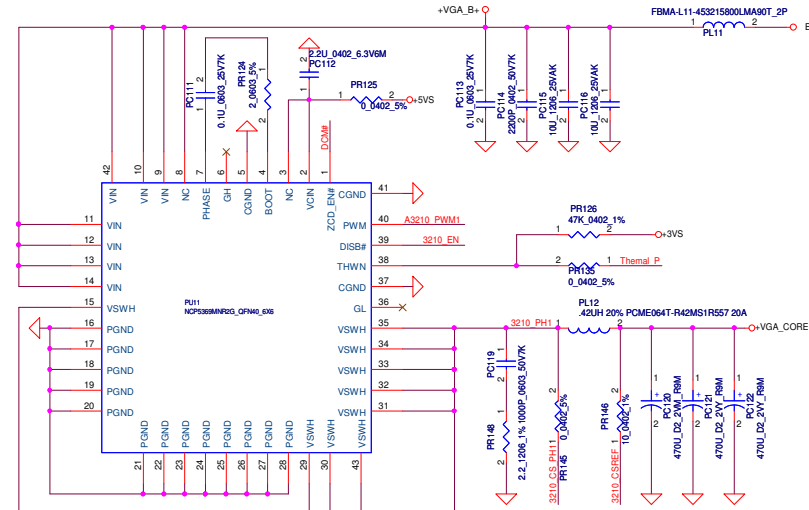
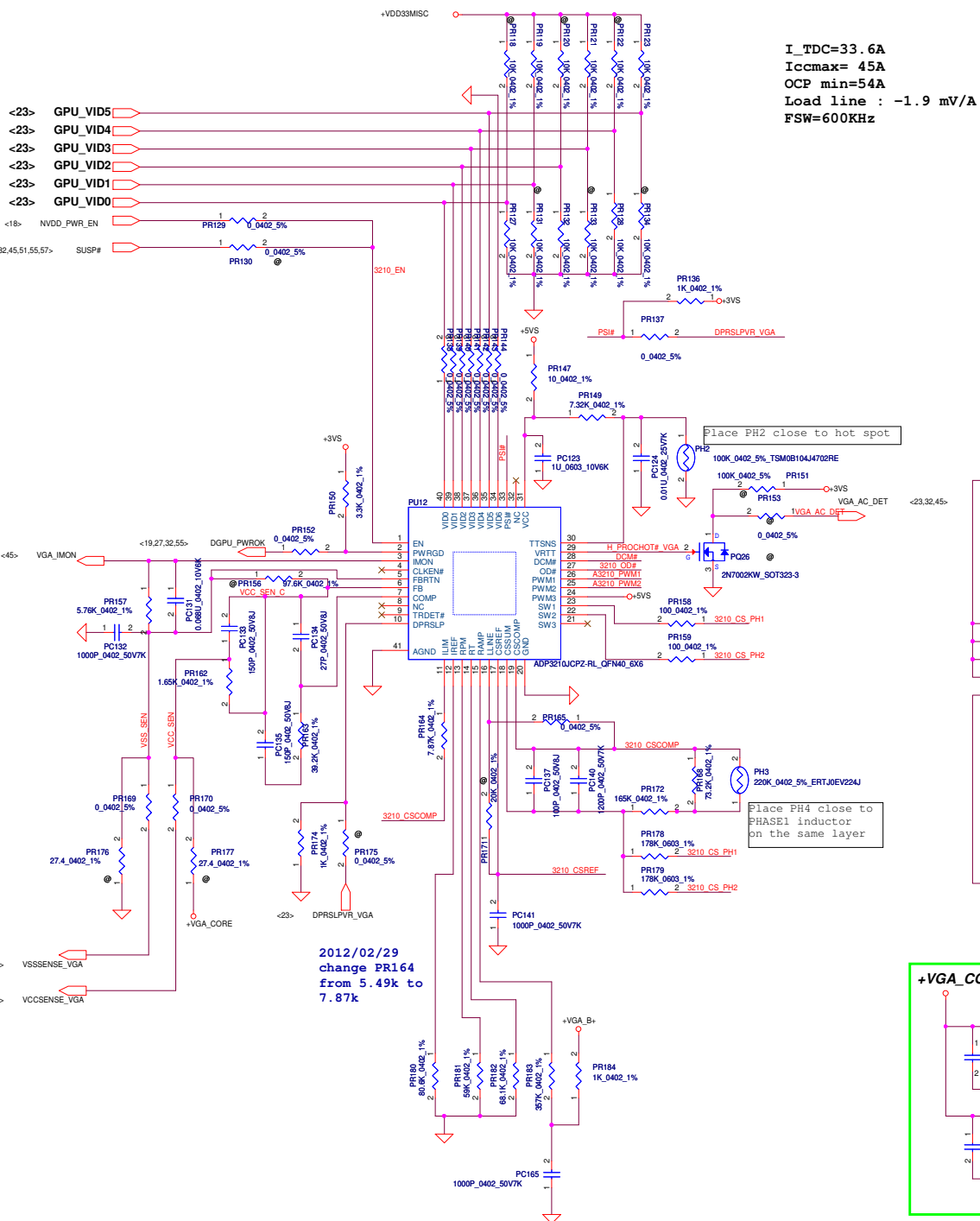
output voltage adjustable network



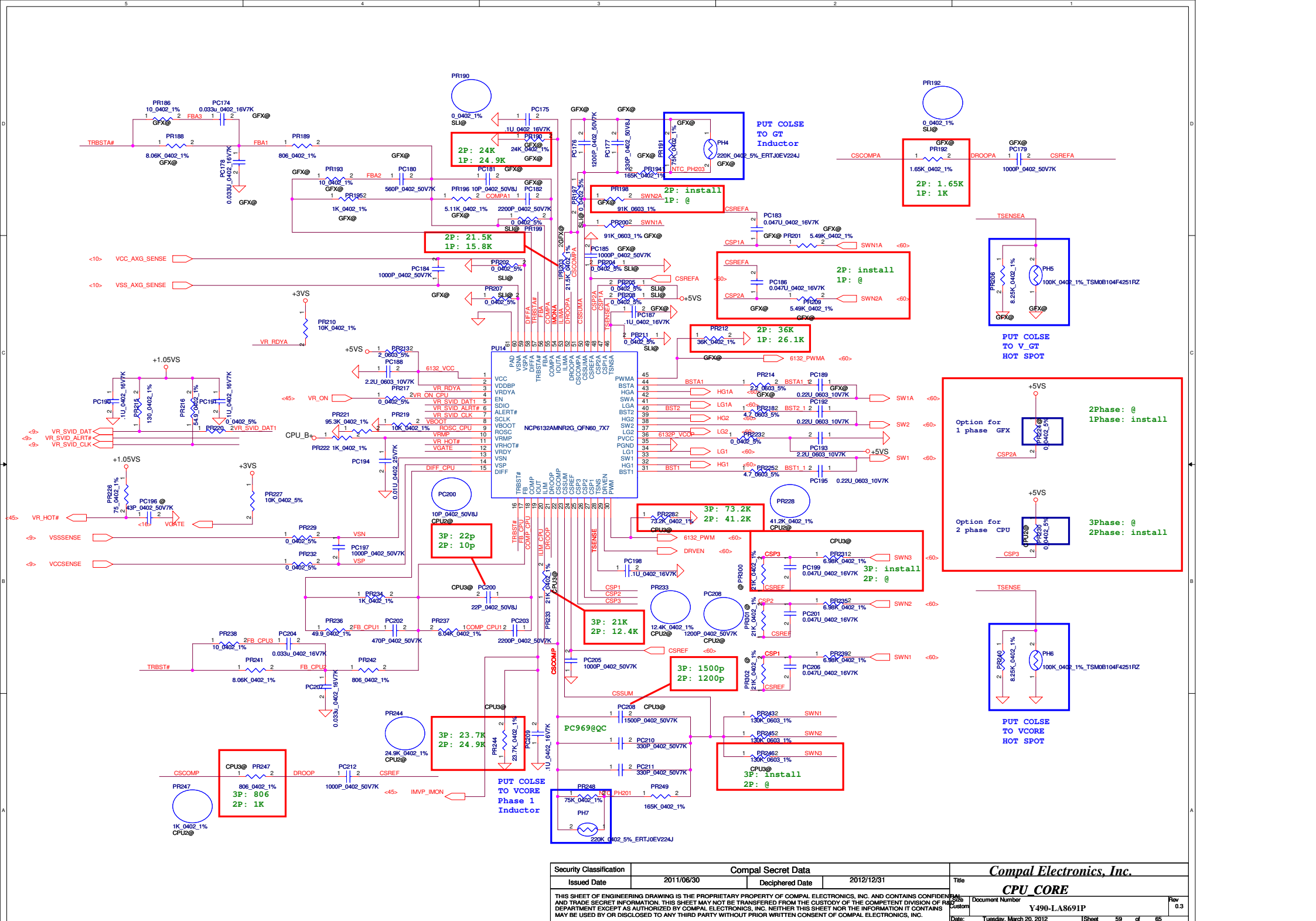


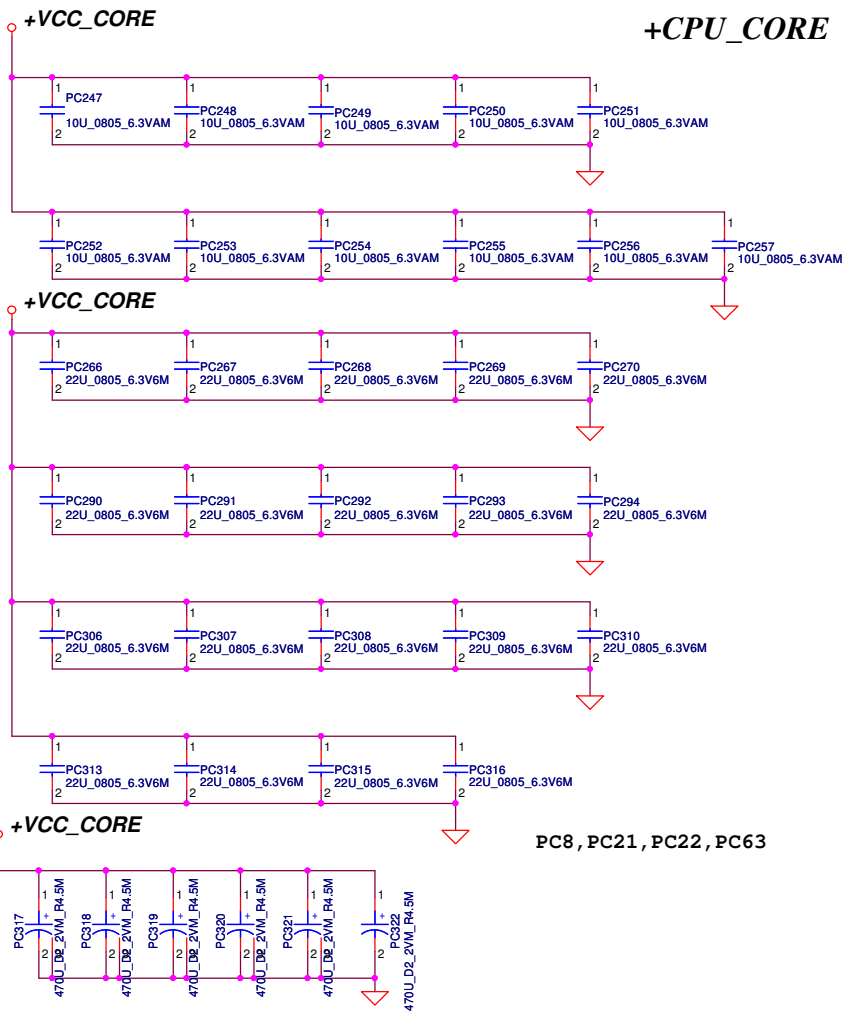
+1.05VS_VCCPP OCP (min) = 22.38A

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Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title	1.8VSP/0.75VSP/1.05VS_VCCPP
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				Date: Tuesday, March 20, 2012	Sheet 57 of 65

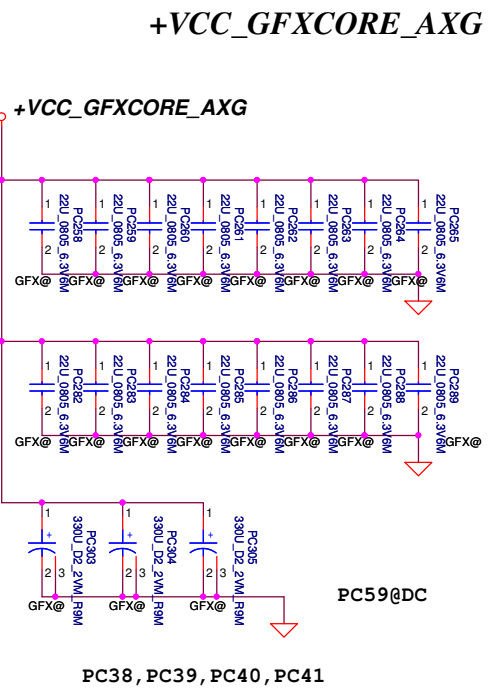


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2011/06/30		2012/12/31		VGA COREP	
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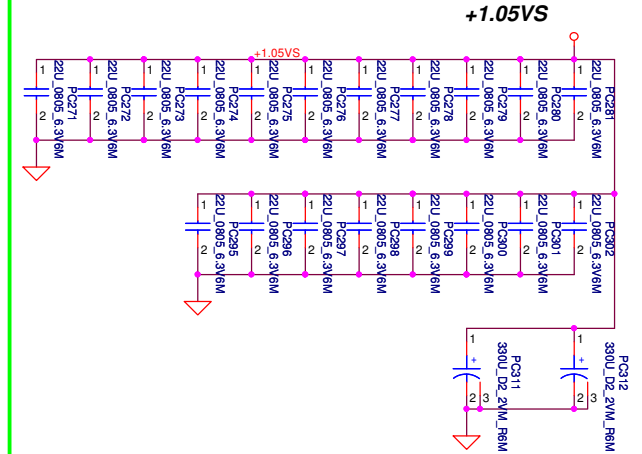


DC: PC73, PC74, PC75, PC76, PC77, PC78 (330uF/9m)
 QC: PC76, PC78 (470uF/4.5m), PC73, PC74, PC75 (330uF/9m)



Below is 458544_CRV_PDDG_0.5 Table 5-8.

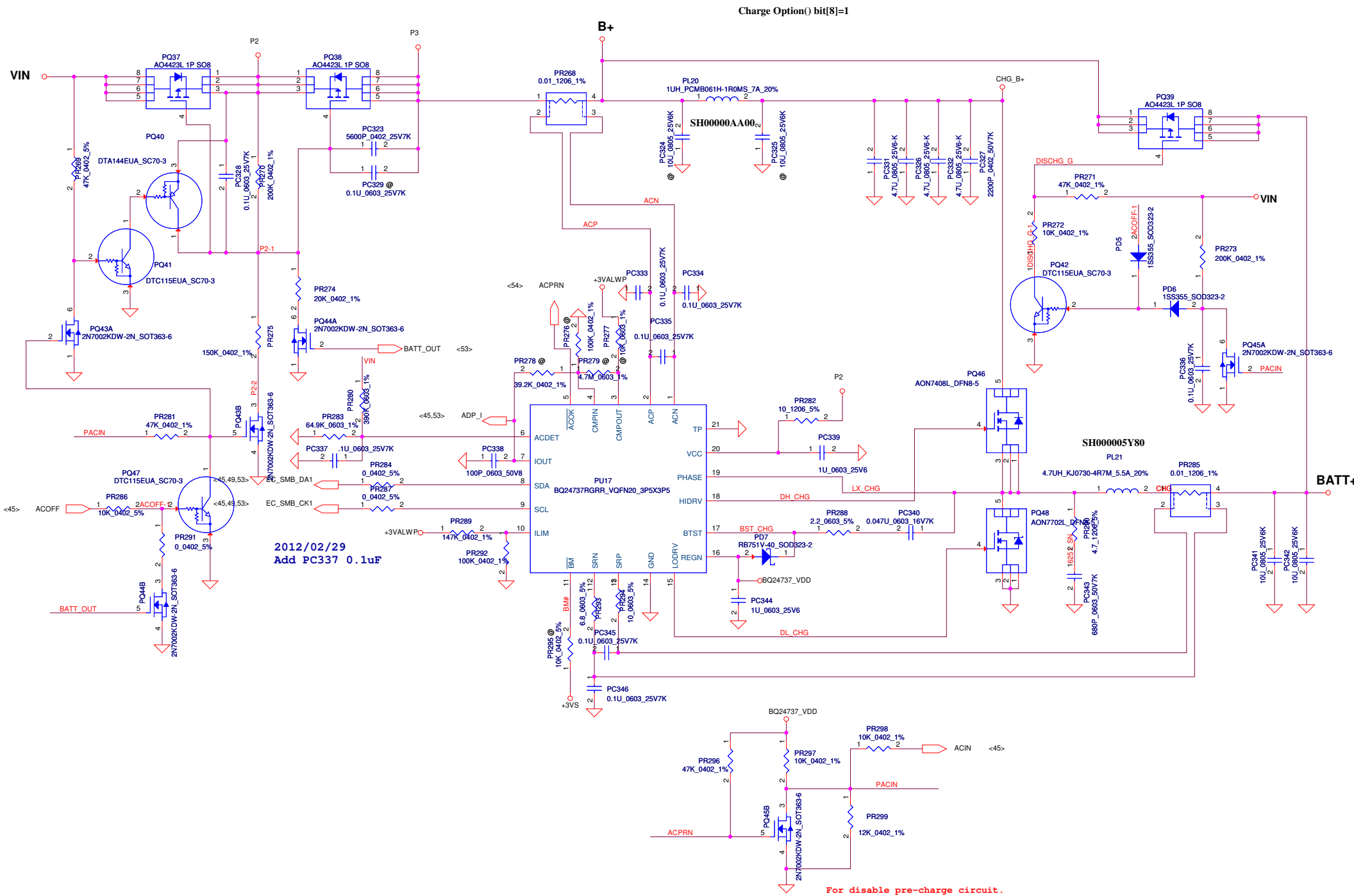
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



PC32, PC49, PC54, PC55, PC56

PC38, PC39, PC40, PC41

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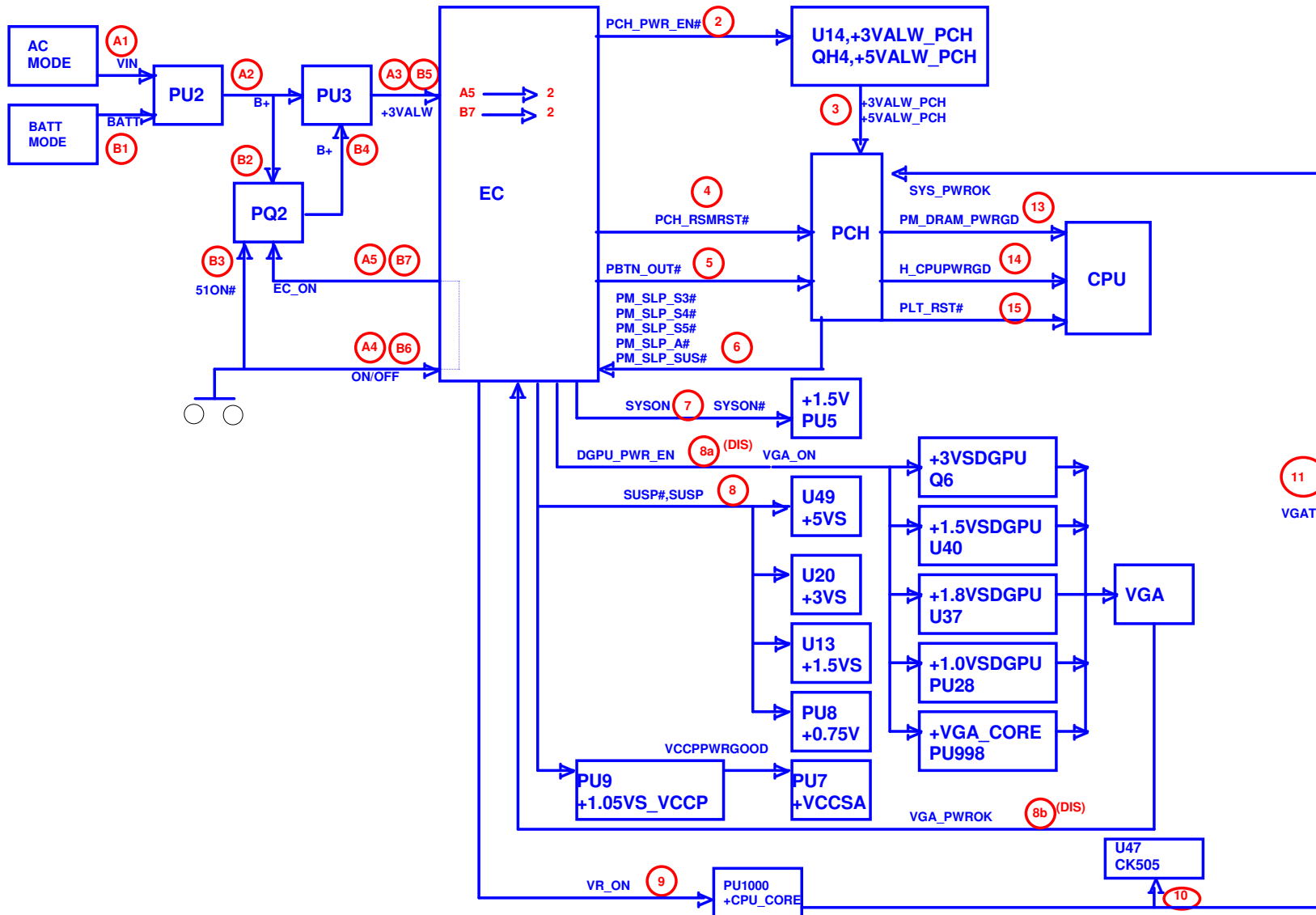


Charge Option() bit[8]=1

2012/02/29
Add PC337 0.1uF

For disable pre-charge circuit.

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Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10					
11					
12					
13					
14					
15					
16					
17					

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				Document Number	
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HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "a" to "DS3a"
				For Deep S3 Function

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/07/21		Deciphered Date	
		2012/12/31			
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				Document Number	
				Rev 0.1	
Date: Tuesday, March 20, 2012				Sheet 65 of 65	