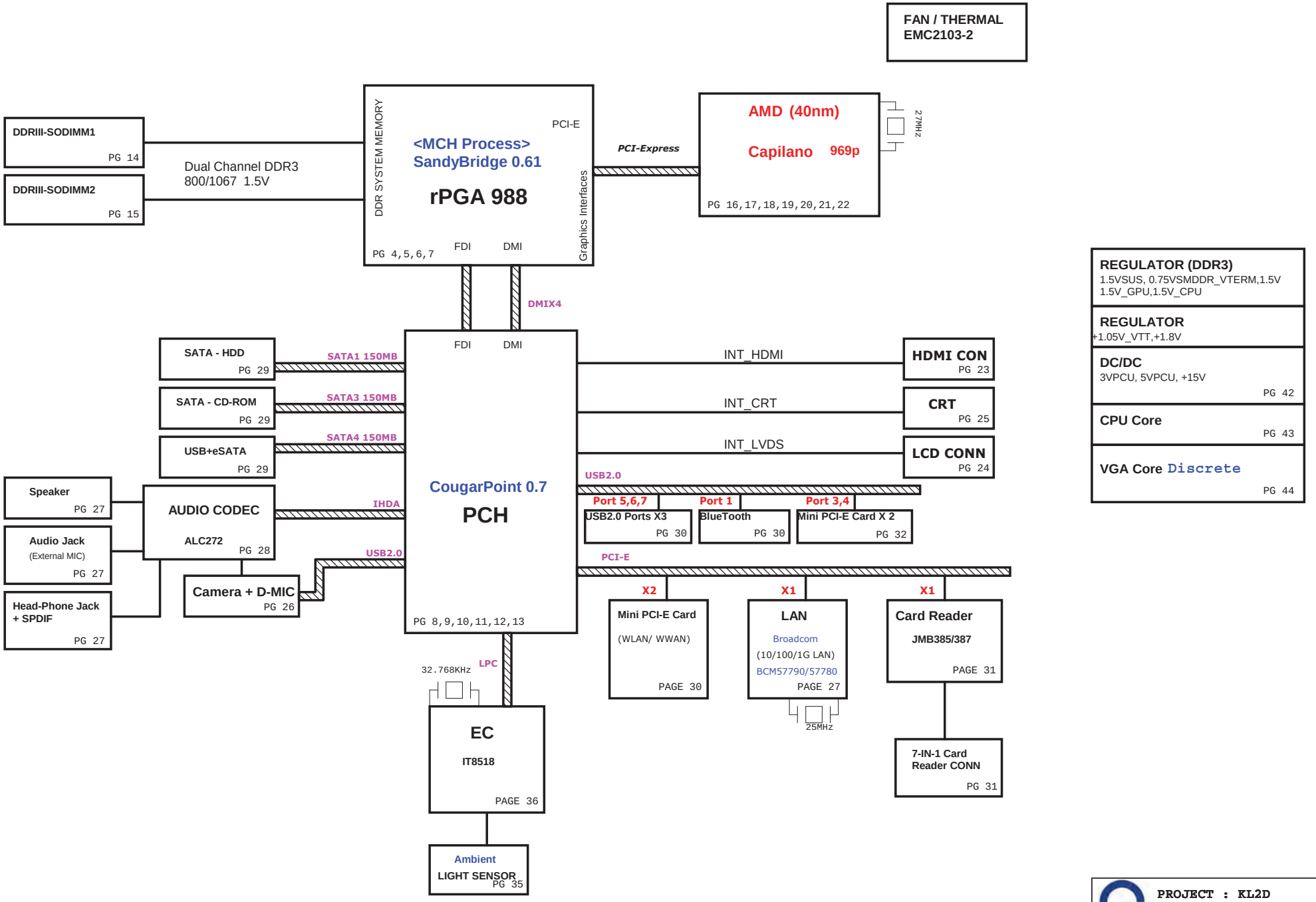

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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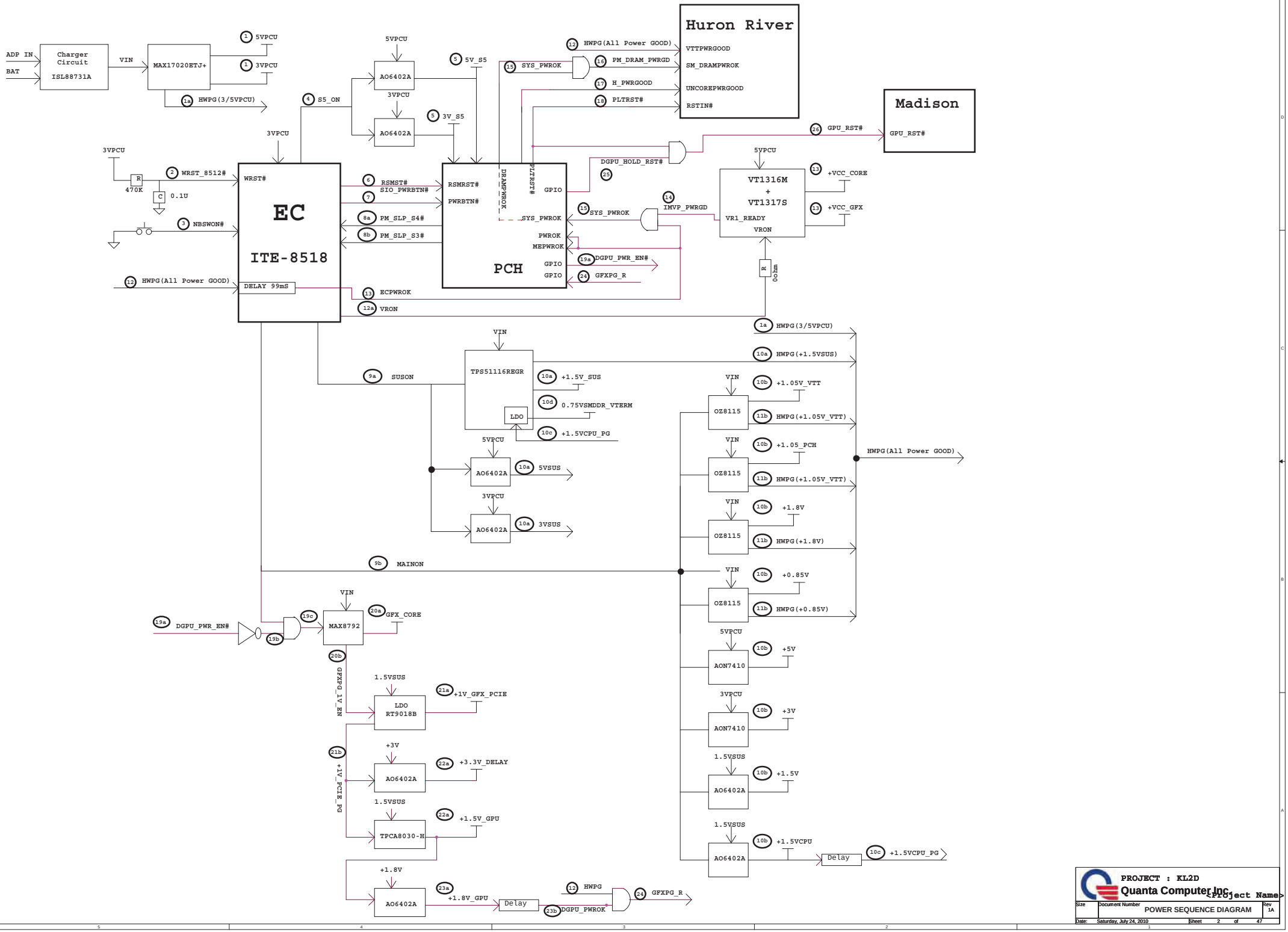
Huron River
VTTPWRGOOD
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
Madison
GPU_RST#
ADP IN
BAT
Charger Circuit
ISL88731A
VIN
MAX17020ETJ+
5VPCU
3VPCU
HWPG(3/5VPCU)
AO6402A
5V_S5
3V_S5
S5_ON
SYS_PWROK
PM_DRAM_PWRGD
H_PWRGOOD
PLTRST#
HWPG(All Power GOOD)
GPU_RST#
DGPU_HOLD_RST#
VT1316M
+
VT1317S
VR1_READY
VRON
+VCC_CORE
+VCC_GFX
IMVP_PWRGD
WRST_8512#
470K
0.1U
NBSWON#
EC
ITE-8518
WRST#
RSMST#
SIO_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
DELAY 99mS
ECPWROK
VRON
RSMRST#
PWRBTN#
DRAMPWROK
PLTRST#
GPIO
SYS_PWROK
PWROK
MEPWROK
DGPU_PWR_EN#
GFXPG_R
PCH
10ohm
TPS51116REGR
LDO
+1.5V_SUS
0.75VSMDDR_VTERM
+1.5VCPU_PG
SUSON
5VSUS
3VSUS
OZ8115
+1.05V_VTT
HWPG(+1.05V_VTT)
+1.05_PCH
+1.8V
HWPG(+1.8V)
+0.85V
HWPG(+0.85V)
HWPG(+1.5VSUS)
HWPG(All Power GOOD)
MAINON
MAX8792
GFX_CORE
DGPU_PWR_EN#
GFXPG_1V_EN
LDO
RT9018B
+1V_GFX_PCIE
+1V_PCIE_PG
+3V
+3.3V_DELAY
AO6402A
TPCA8030-H
+1.5V_GPU
+1.8V
+1.8V_GPU
Delay
DGPU_PWROK
HWPG
GFXPG_R
AON7410
+5V
+3V
+1.5V
+1.5VCPU
+1.5VCPU_PG
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Quanta Computer Inc.
<Project Name>
POWER SEQUENCE DIAGRAM
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CLK Gen(CLK)

03

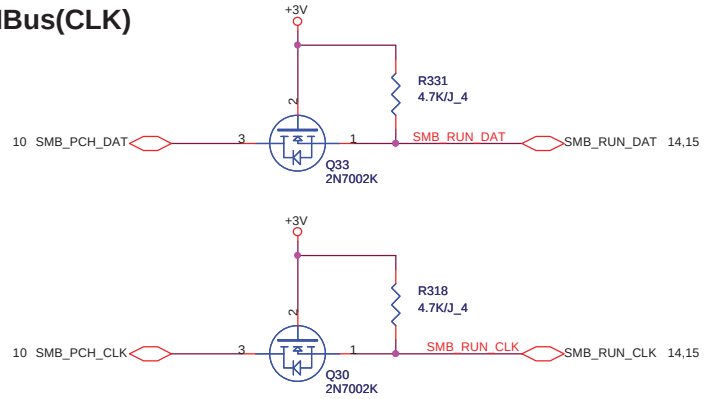
02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



PROJECT : KL2D

Quanta Computer Inc.

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	Clock Generator	1A

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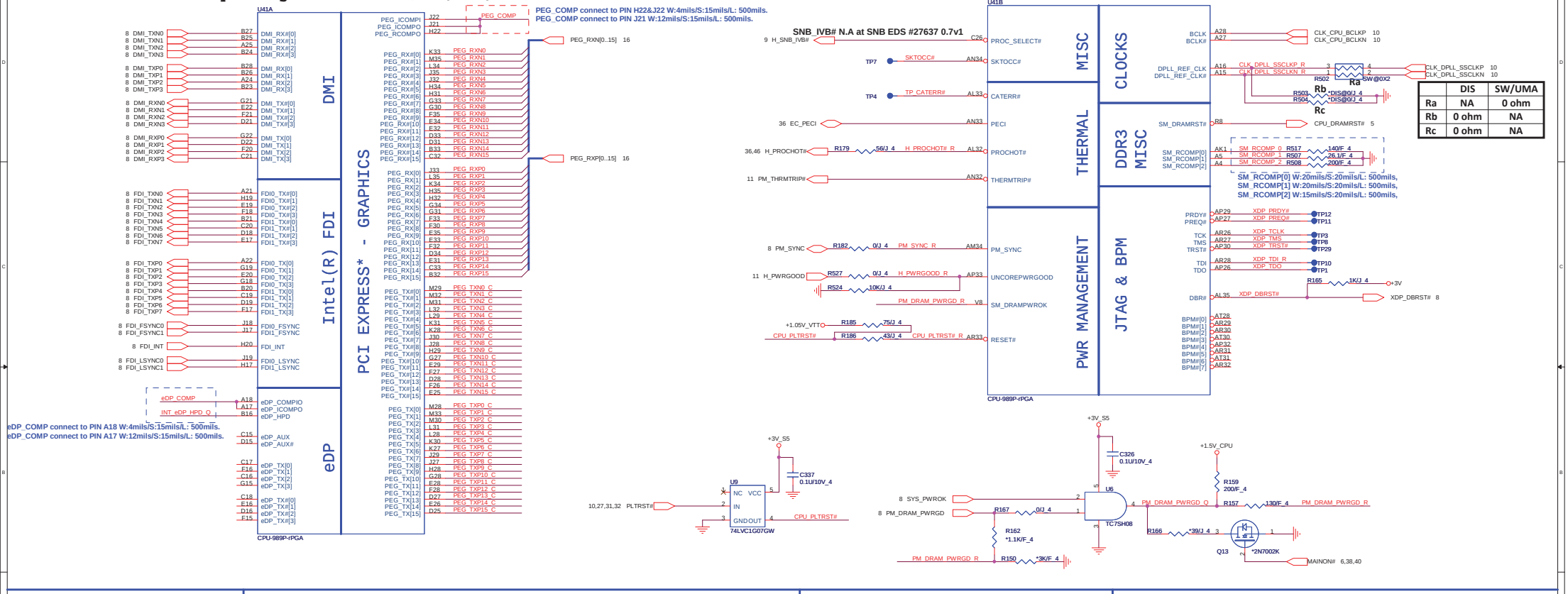
Sandy Bridge Processor (DMI,PEG,FDI)

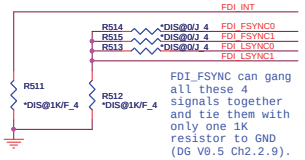
Sandy Bridge Processor (CLK,MISC,JTAG)

04

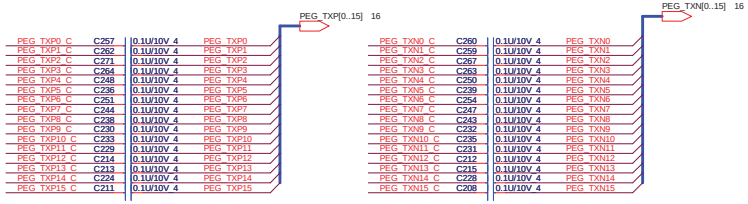


	DIS	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

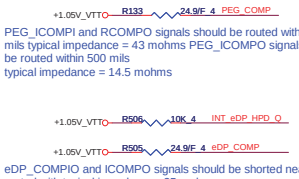
FDI Disable



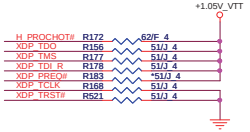
PEG x16 (UMA Non-stuff)



DP & PEG Compensation



Processor pull-up(CPU)



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Quanta Computer Inc.
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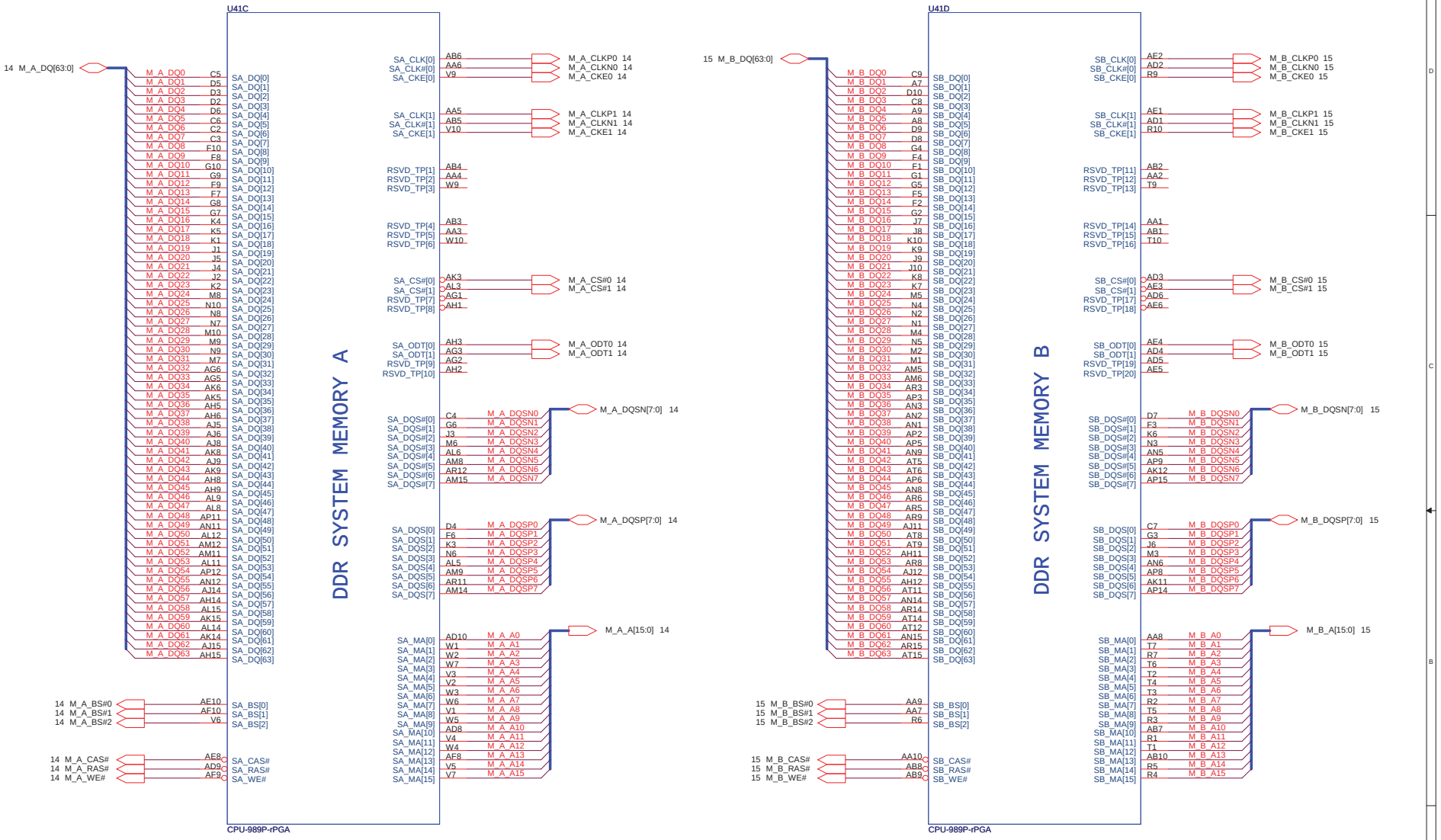
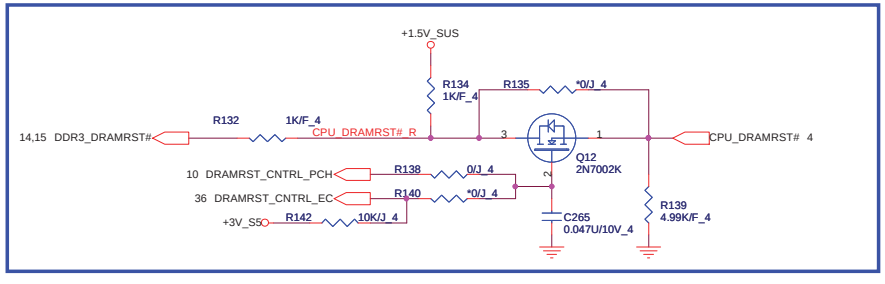
Sandy Bridge Processor (DDR3)





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Quanta Computer Inc.			
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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

22uF (Reserved)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

22uF (Reserved)

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

Reserved

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
Place PU resistor close to CPU

SVID DATA
Close to VR
Place PU resistor close to CPU

SVID ALERT

4.5A

3/26 DB add for Intel. Placement close to CPU.

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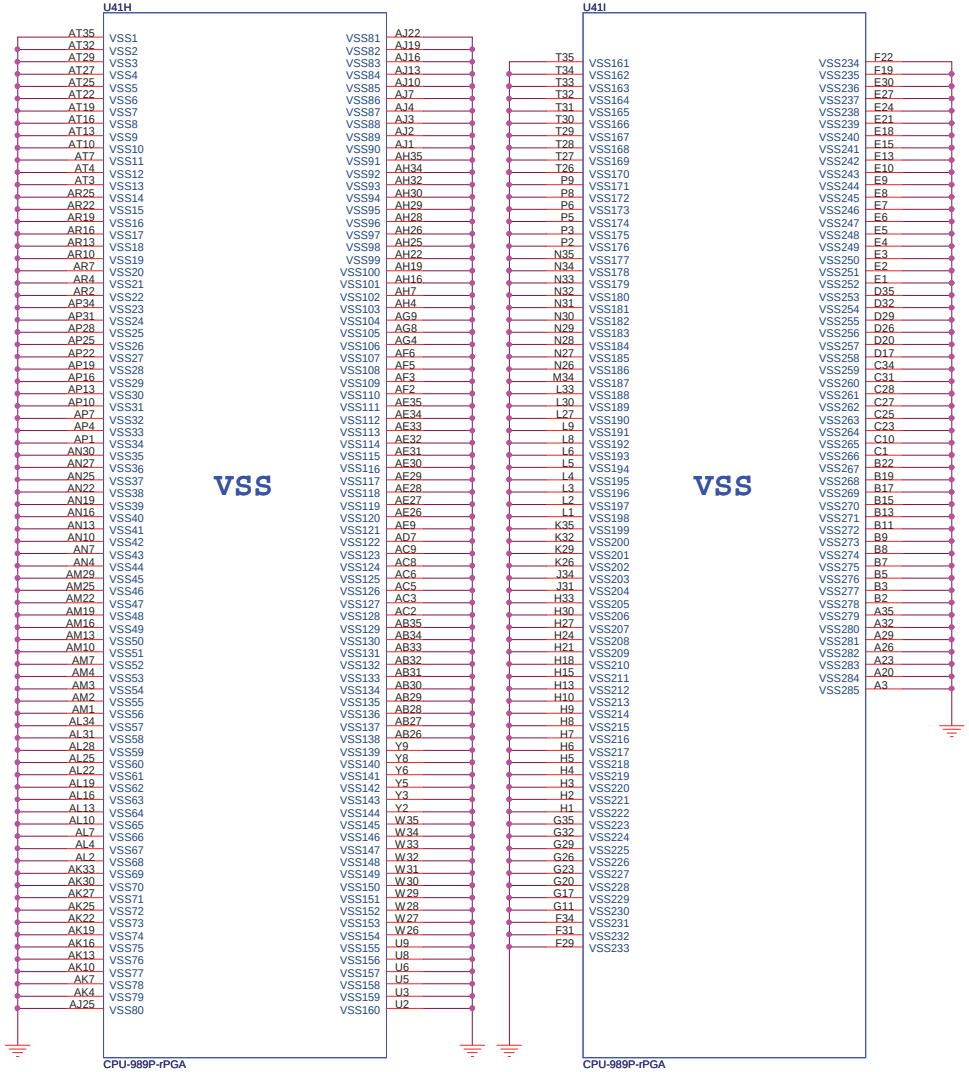
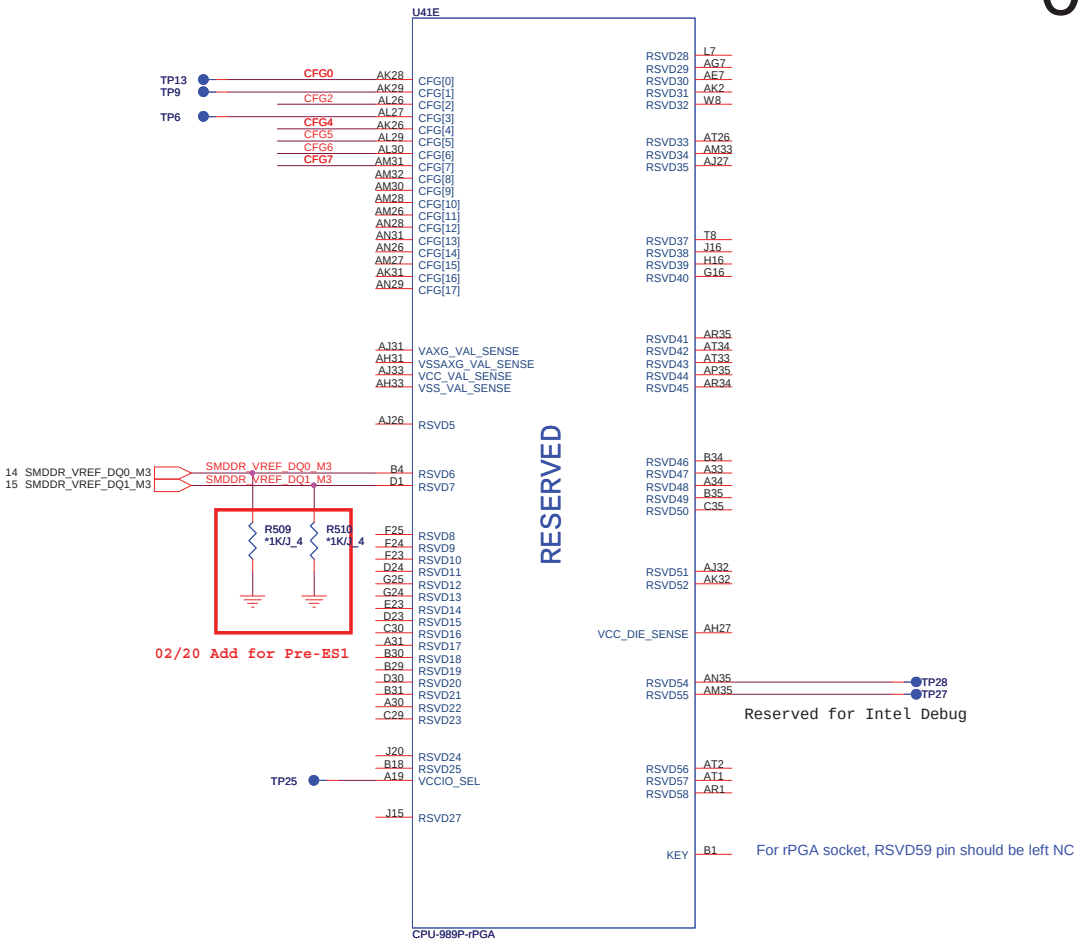
Quanta Computer Inc.
Sandy Bridge 3/4
Saturday, July 24, 2010

Sandy Bridge Processor (GND)



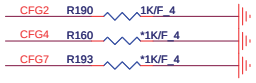
Sandy Bridge Processor (RESERVED, CFG)

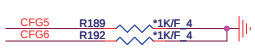


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Quanta Computer Inc.

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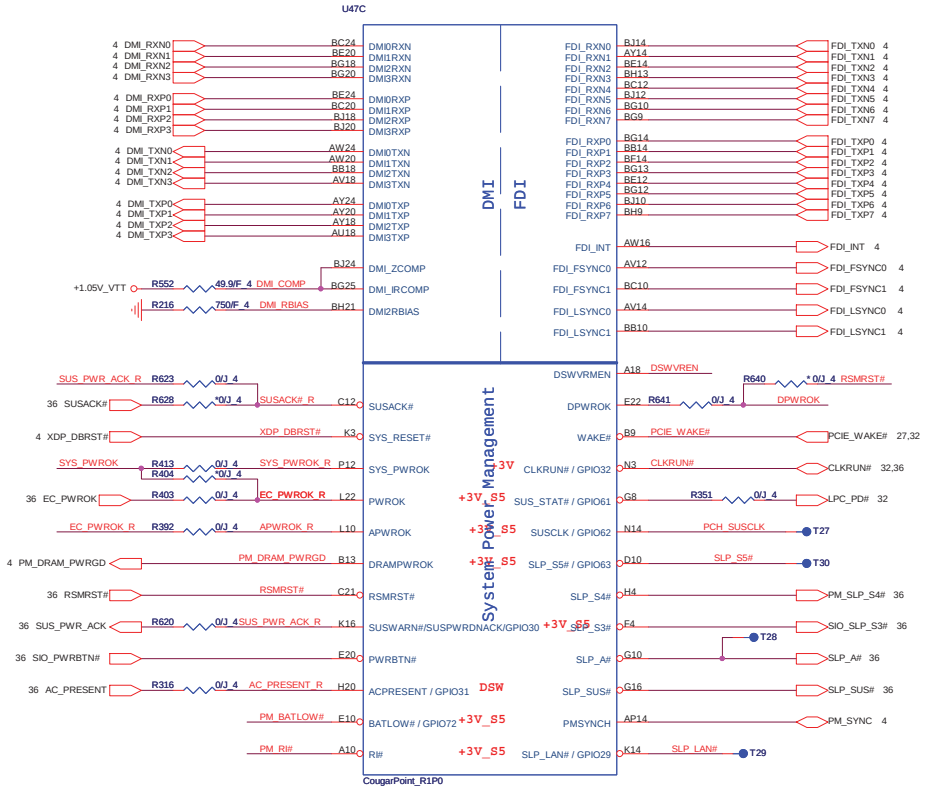
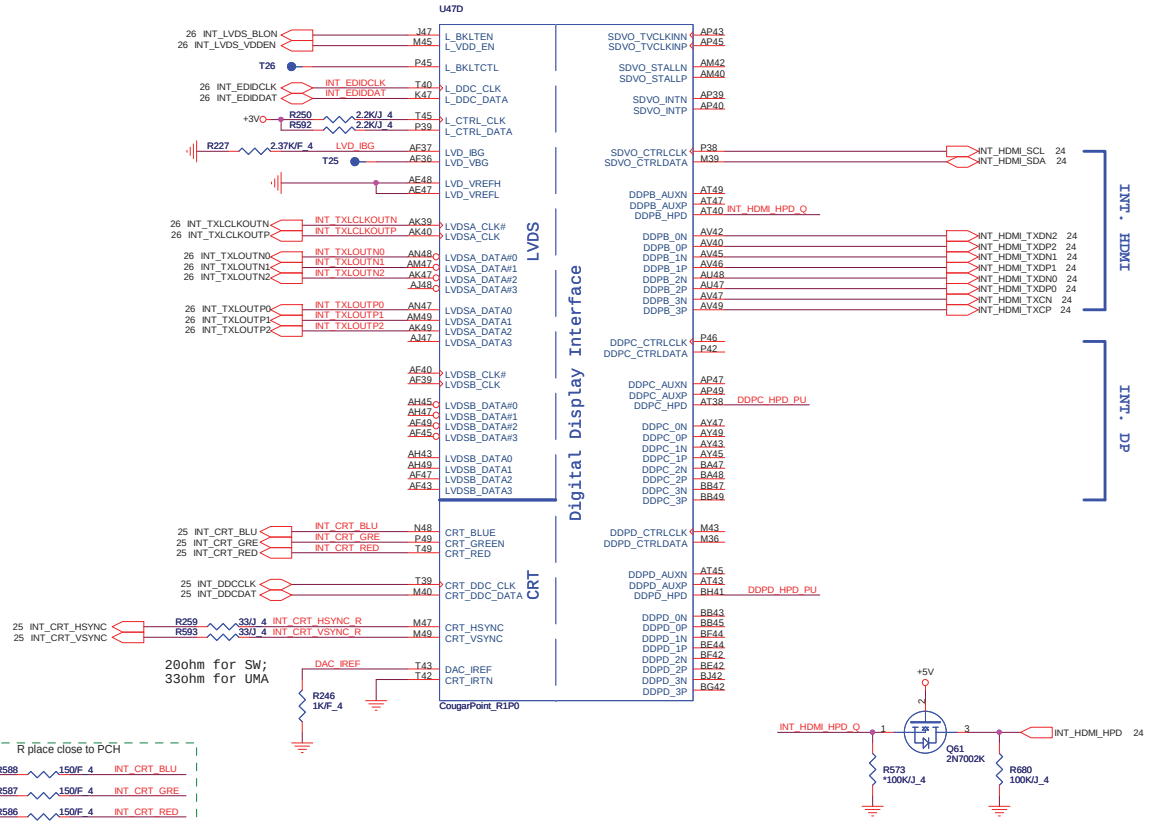
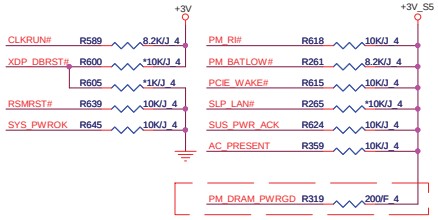
Cougar Point (DMI,FDI,PM)



Cougar Point (LVDS,DDI)

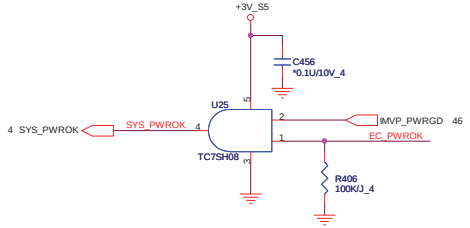


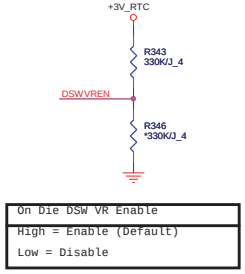
PCH Pull-high/low(CLG)



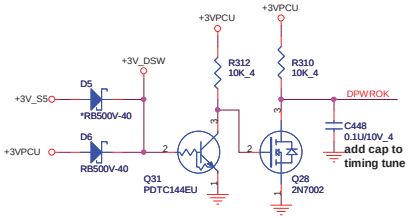
3/16 Change topology; 200ohm PU to +3V_S5

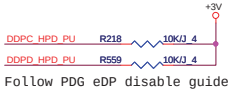
System PWR_OK(CLG)





DPWROK FOR DSW





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Quanta Computer Inc.

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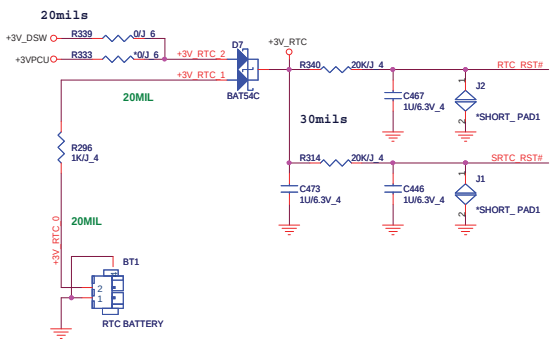
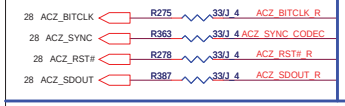
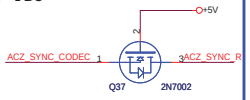
RTC Circuitry(RTC)



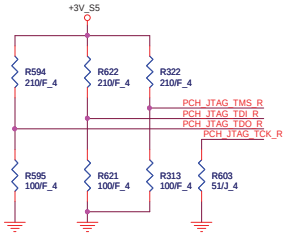
HDA Bus(CLG)



To Separate Codec Sync by PD3

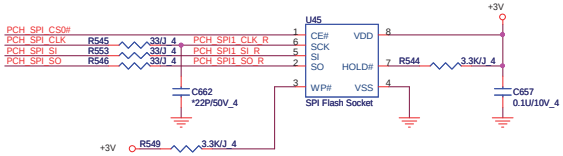


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

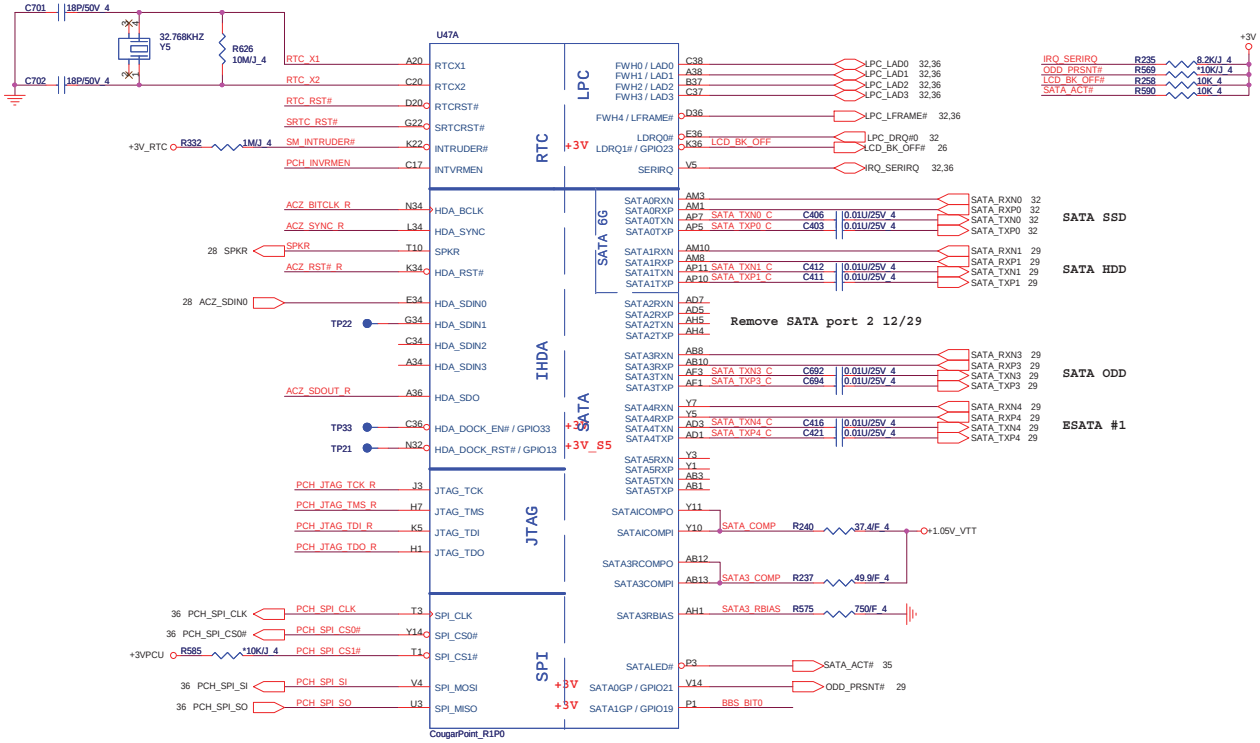
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



PCH2 (CLG)

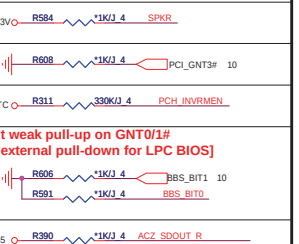
Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



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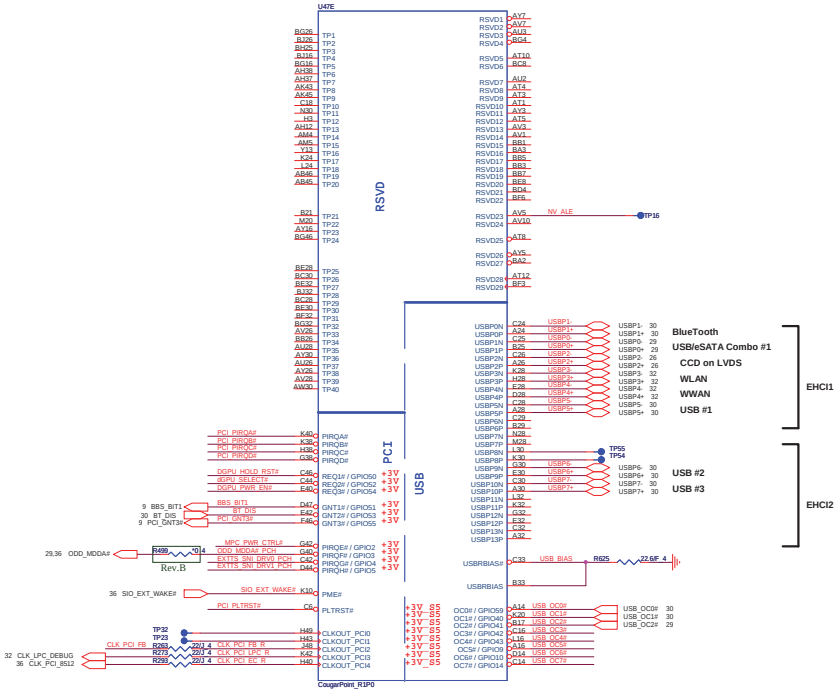
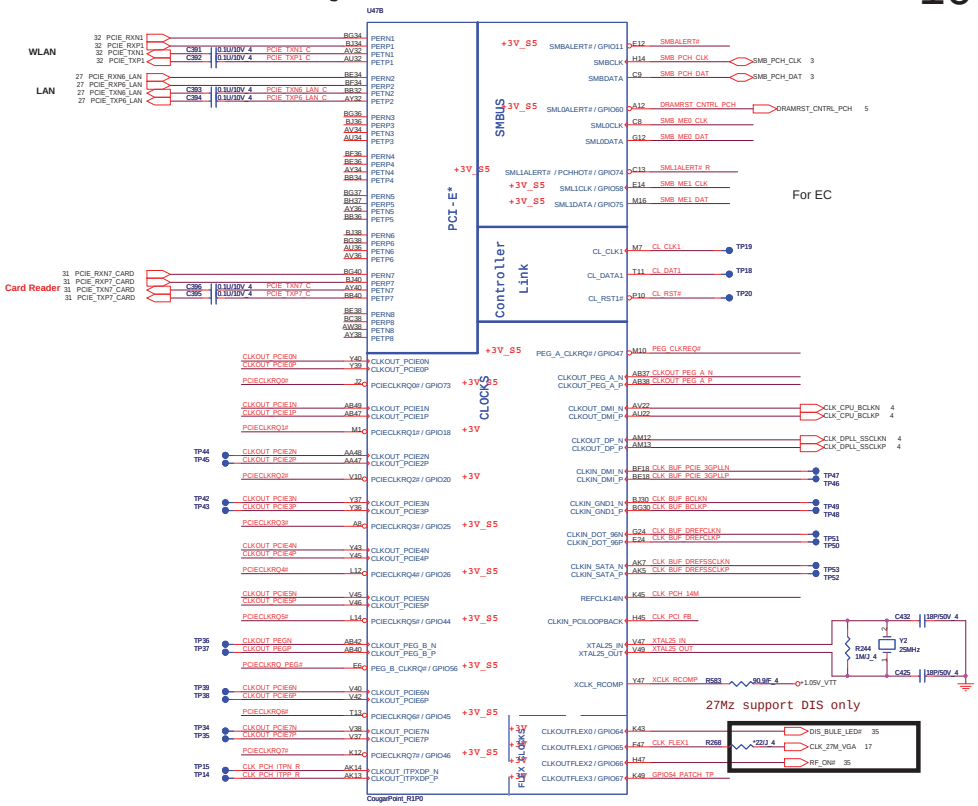
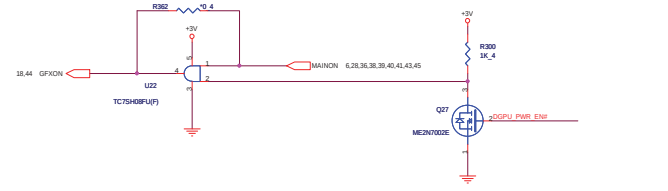
Cougar Point-M (PCI,USB,NVRAM)



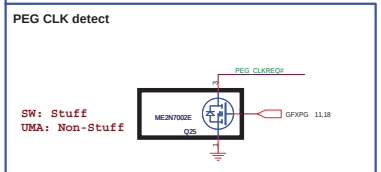
Cougar Point-M (PCI-E,SMBUS,CLK)

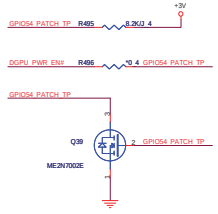


DGPU Power ON

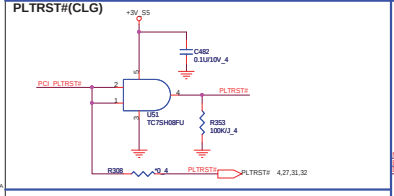


PEG CLK detect

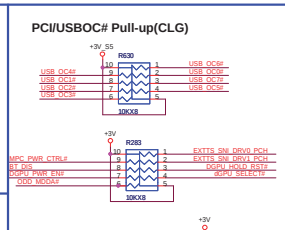




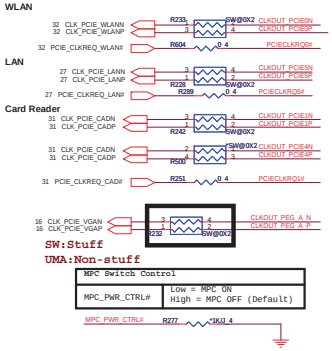
PLTRST#(CLG)



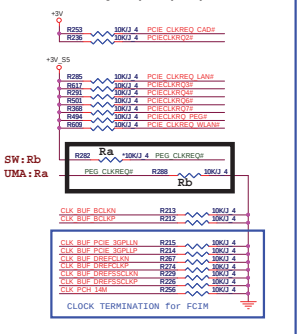
PCI/USBOC# Pull-up(CLG)



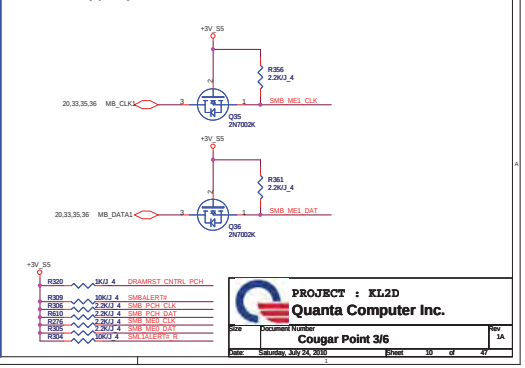
WLAN / LAN / Card Reader



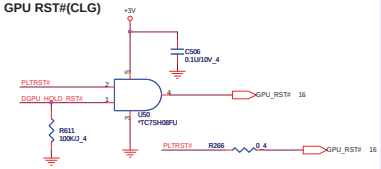
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



GPU RST#(CLG)



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Quanta Computer Inc.
Cougar Point 3/6
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Cougar Point (GPIO,VSS_NCTF,RSVD)

U47F

S_GPIO R376 100_4 — T7 BMBUSY# / GPIO0 +3V
36 EC_EXT_SMI# — EC_EXT_SMI# — A42 TACH1 / GPIO1 +3V
BOARD_ID1 — H36 TACH2 / GPIO6 +3V
36 EC_EXT_SCI# — EC_EXT_SCI# — E38 TACH3 / GPIO7 +3V
SYSTEM_ID — C10 GPIO8 +3V_S5
32 LAN_DISABLE# — LAN_DISABLE# — C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
HOST_ALERT#1_R — G2 GPIO15 +3V_S5
BOARD_ID0 — U2 SATA4GP / GPIO16 +3V
GFXPG_R — D40 TACH0 / GPIO17 +3V
BIOS_REC — T5 SCLOCK / GPIO22 +3V
32 WWAN_OFF# — R269 0/J_4 WWAN_OFF#_R — E8 GPIO24 / MEM_LED +3V_S5
GPIO27 — E16 GPIO27 DSW
9,36 PLL_ODVR_EN — R388 0/J_4 PLL_ODVR_EN_R — P8 GPIO28 +3V_S5
STP_PCI# — K1 STP_PCI# / GPIO34 +3V
30 BT_ON# — BT_ON# — K4 GPIO35 +3V
32 SDD_DA_DSS — SDD_DA_DSS — V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG — M5 SATA3GP / GPIO37 +3V
MFG_MODE — N2 SLOAD / GPIO38 +3V
DGPU_PRSNT# — M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP — V13 SDATAOUT1 / GPIO48 +3V
33,36 TEMP_ALERT# — V3 SATA5GP / GPIO49 +3V
SV_DET — D6 GPIO57 +3V_S5

GPIO

TACH4 / GPIO68 +3V — C40 — SSD_DETECT# 32
TACH5 / GPIO69 +3V — B41 R614 1.5K/F_4
TACH6 / GPIO70 +3V — C41 — SATA_ODD_PWR_EN 29
TACH7 / GPIO71 +3V — A40 BOARD_ID2

CPU/MISC

A20GATE — P4 — EC_A20GATE 36
PECI — AU16 — TP17
RCIN# — P5 EC_RCIN# — EC_RCIN# 36
PROCPWRGD — AY11 — H_PWRGOOD 4
THRMTRIP# — AY10 PCH_THRMTRIP# R220 390/J_4 — PM_THRMTRIP# 4
INIT3_3V# — T14
DF_TVS — AY1 — DF_TVS 9

TS_VSS1 — AH8
TS_VSS2 — AK11
TS_VSS3 — AH10
TS_VSS4 — AK10
NC_1 — P37

3/16 Connected to GND
DG rev0.9

NCTF

VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49
VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

CougarPoint_R1P0

R264 *0_4 +3V
GFXPG_R — U15 TC7SH08FU(F) — HWPG 36,40,41,42,43,45
GFXPG 10,18

GPIO Pull-up/Pull-down(CLG)

+3V_S5
LAN_DISABLE# R612 10K/J_4
WWAN_OFF#_R R271 10K/J_4

+3V
EC_EXT_SMI# R616 10K/J_4
EC_EXT_SCI# R294 10K/J_4
SSD_DETECT# R632 10K/J_4
STP_PCI# R599 10K/J_4
EC_A20GATE R252 10K/J_4
EC_RCIN# R302 10K/J_4
TEMP_ALERT# R577 10K/J_4
BT_ON# R255 10K/J_4
SATA_ODD_PWR_EN R292 10K/J_4

GPIO27 R321 10K/J_4
GFXPG_R R290 10K/J_4

Model	BOARD_ID2	BOARD_ID1	BOARD_ID0
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0

+3V
R582 10K/J_4 BOARD_ID0 R581 *10K/J_4
R298 *10K/J_4 BOARD_ID1 R299 10K/J_4
R295 10K/J_4 BOARD_ID2 R301 *10K/J_4
R307 10K/J_4 SYSTEM_ID R303 *10K/J_4

SV_SET_UP
High = Strong (Default)

TEST_SET_UP — R241 10K/J_4 — R243 *0/J_4 — +3V

+3V
R270 *10K/J_4 SV_DET R262 100K/J_4

	SWITCHABLE	UMA
Stuff	R8489	R8490
No Stuff	R8490	R8489

+3V
R601 *10K/J_4 DGPU_PRSNT# R602 100K/J_4

+3V_S5
HOST_ALERT#1_R R607 1K/J_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

SGPIO

+3V
S_GPIO R382 10K/J_4 — R389 *0/J_4

+3V
R260 100K/J_4 FDI_OVRVLTG R254 *1K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
SDD_DA_DSS R239 200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R245 10K/J_4 — R247 *0/J_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

+3V
MFG_MODE R597 10K/J_4 — R596 *0/J_4

PROJECT : KL2D
Quanta Computer Inc.

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	Cougar Point 4/6	1A
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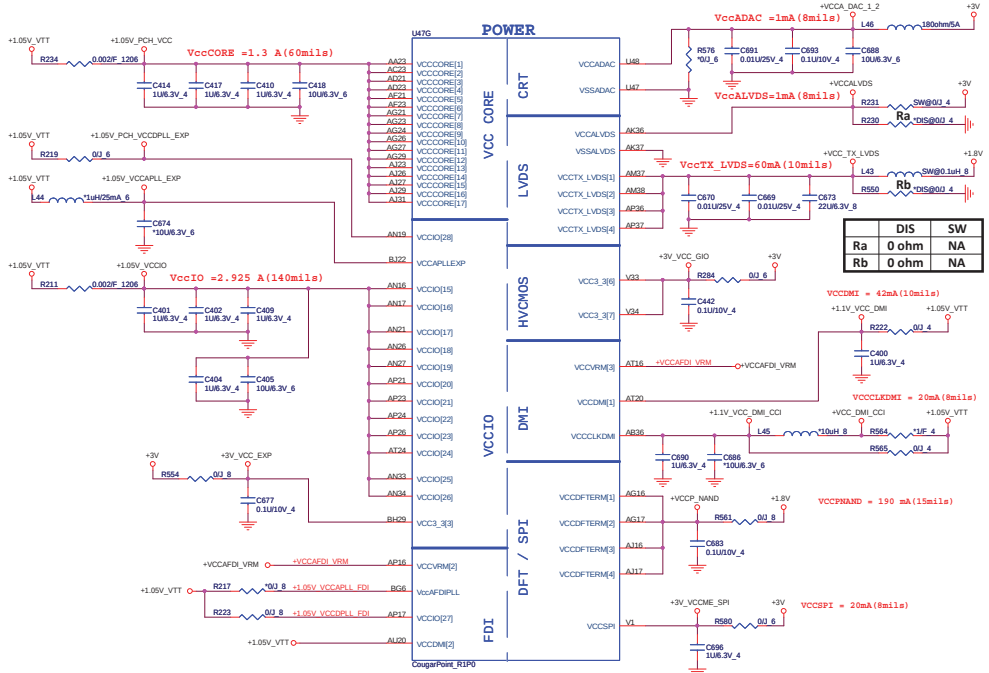
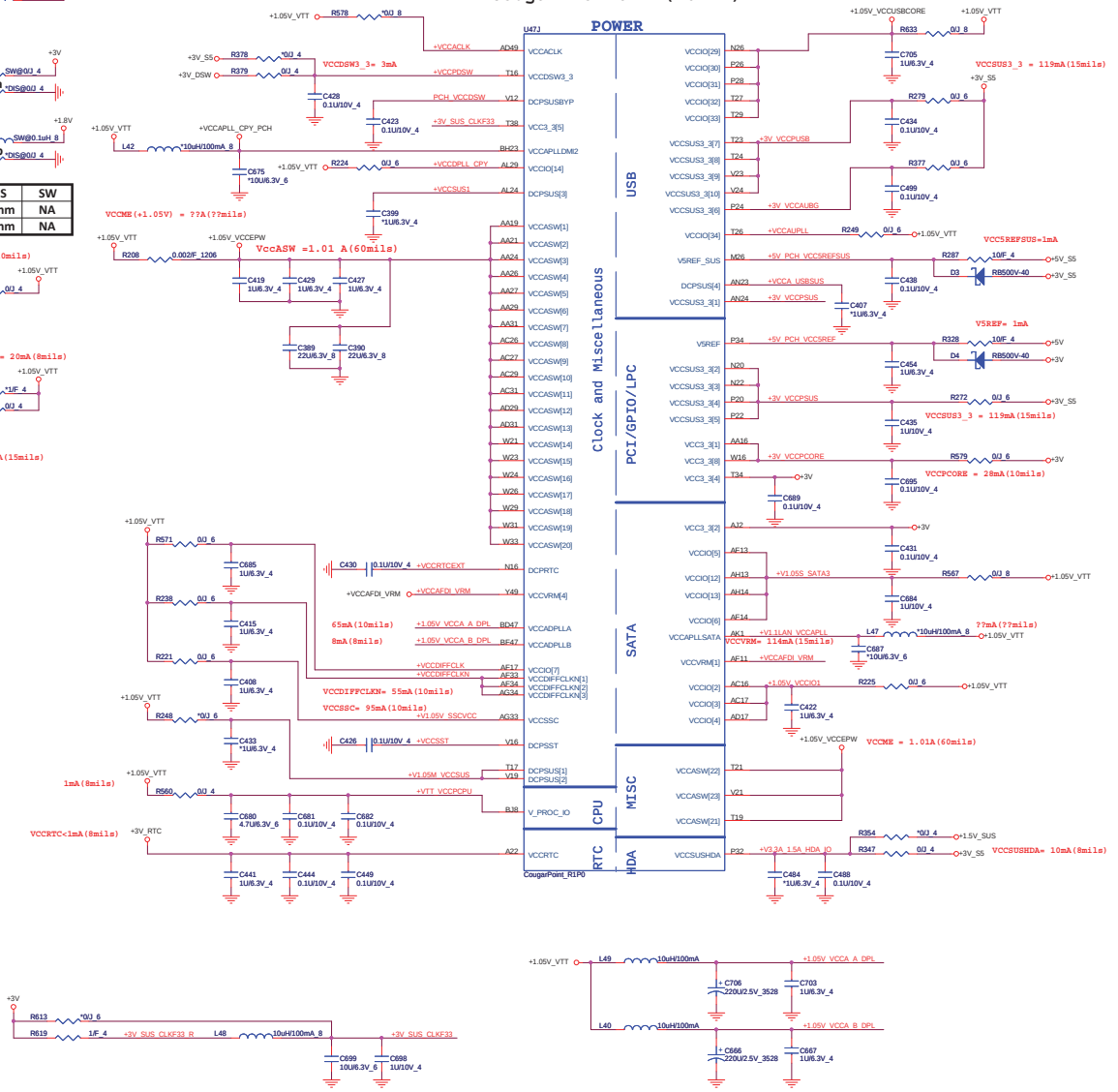
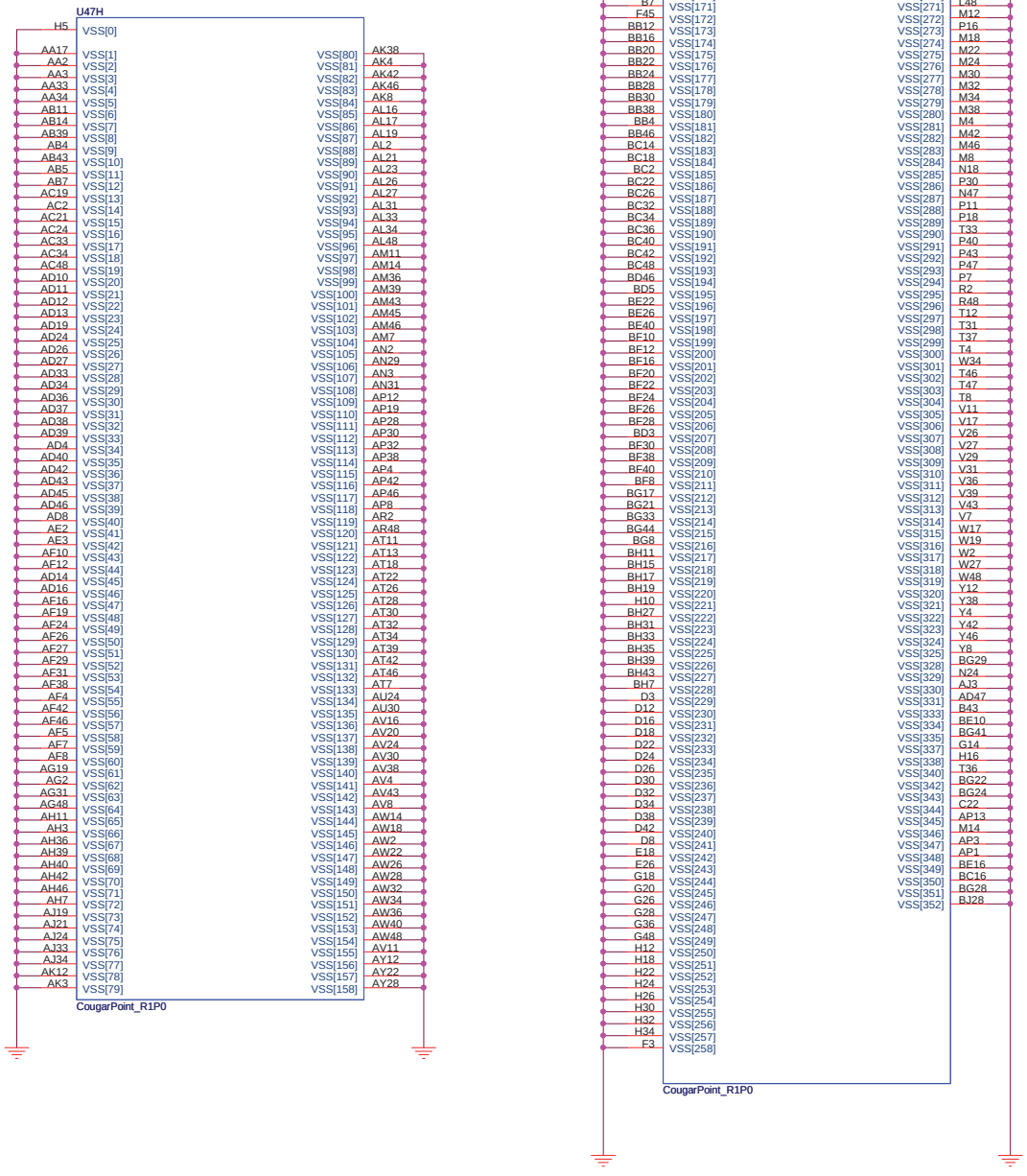
COUGAR POINT (POWER)



Cougar Point-M (POWER)



IBEX PEAK-M (GND)



PROJECT : KL2D

Quanta Computer Inc.

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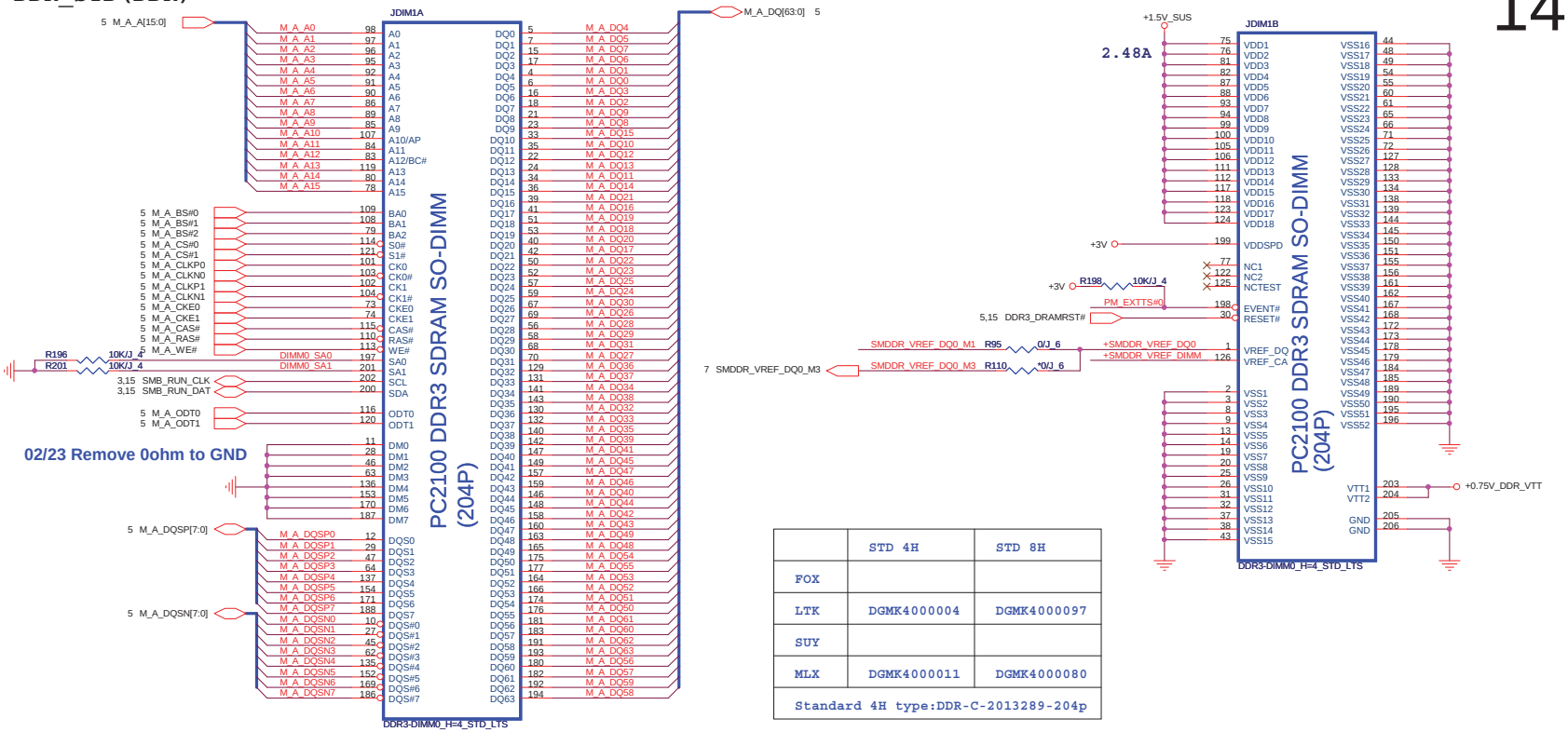
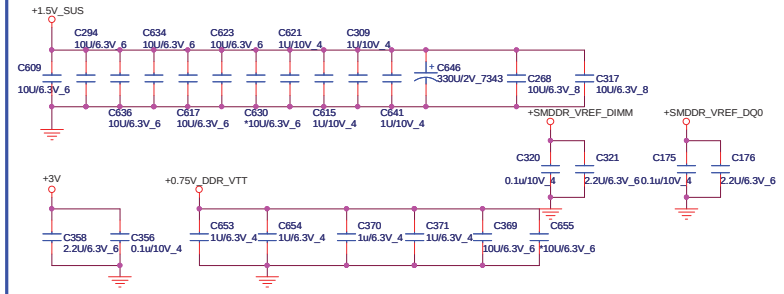
DDR_STD(DDR)

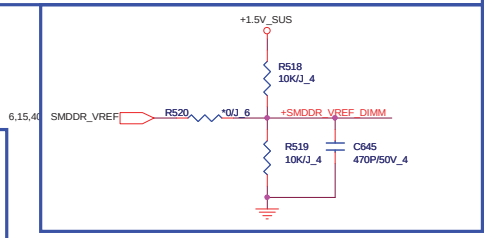


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

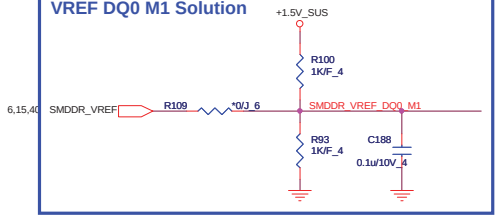
VREF DQ0 M2 Solution

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A

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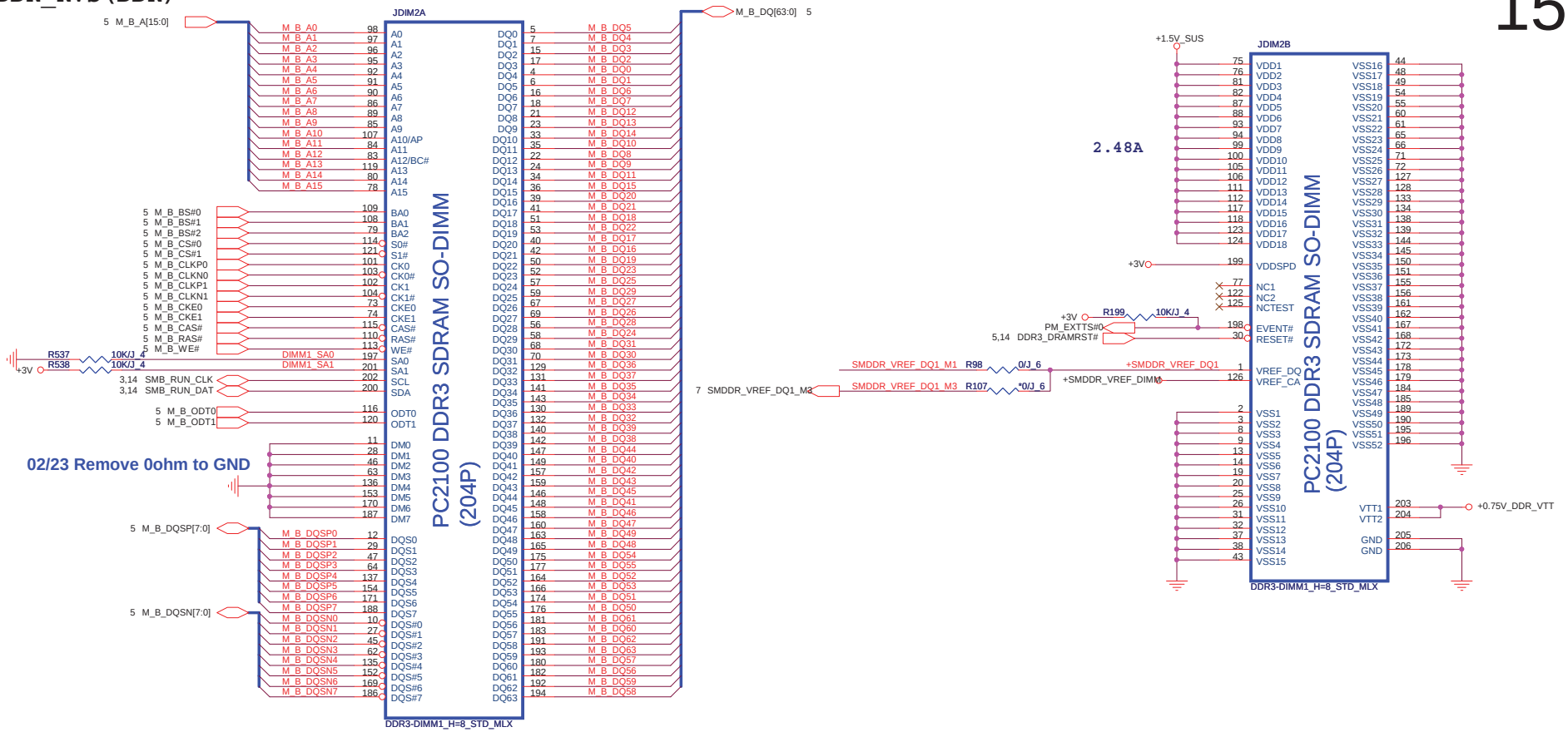
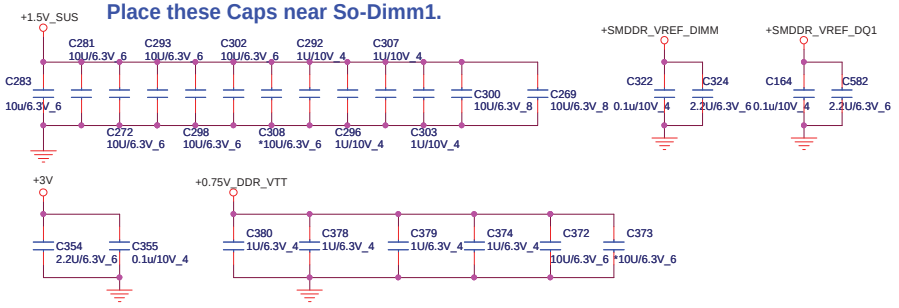
DDR_RVS(DDR)

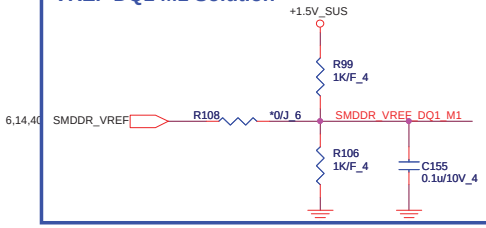


Place these Caps near So-Dimm1.



VREF DQ1 M2 Solution

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

PROJECT : KL2D

Quanta Computer Inc.

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	DDRIII SO-DIMM-1	1A

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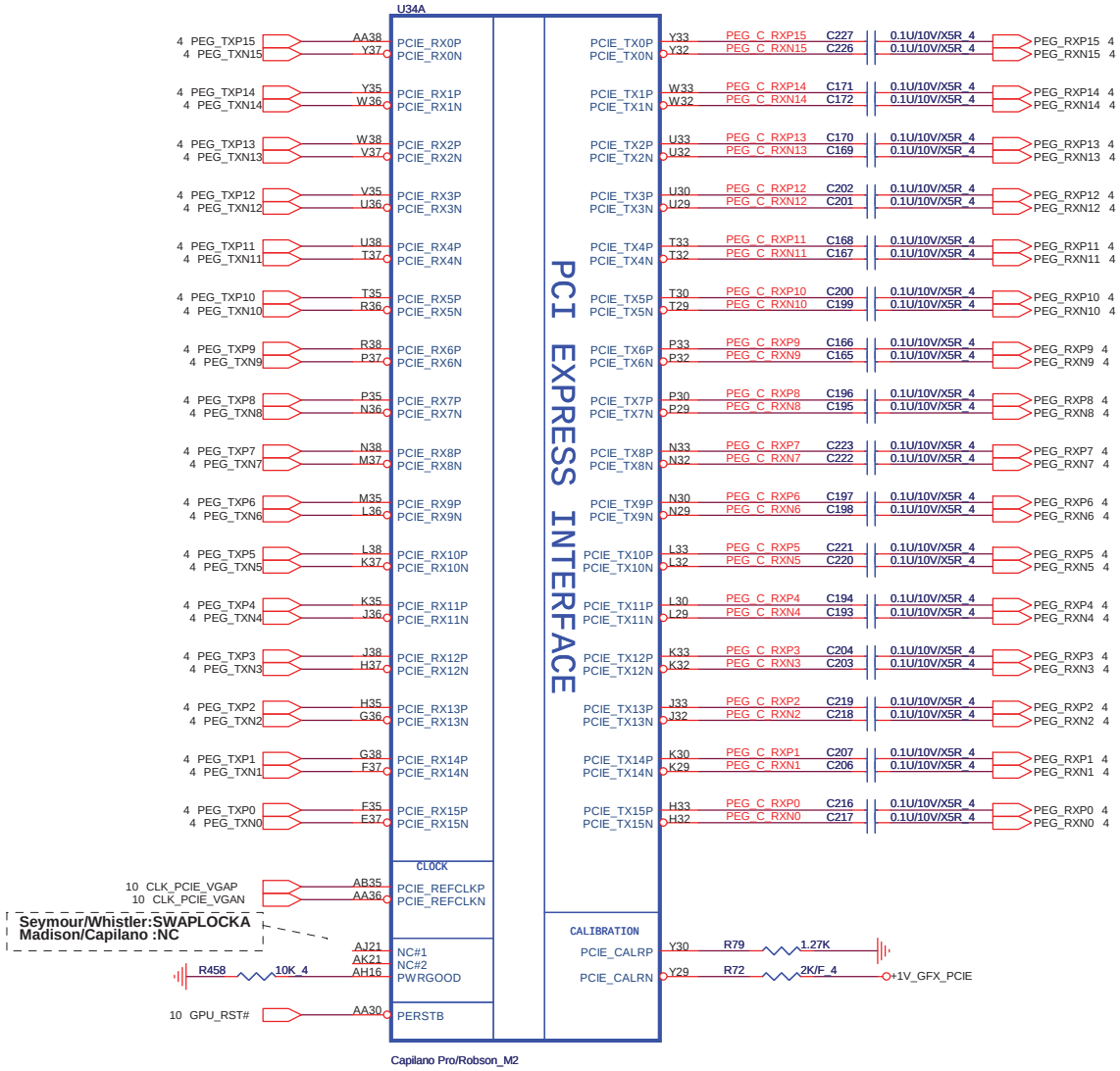

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison PCIE I/F	1A

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Memory Straps		RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
		0	0	1	0
		0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

+1.8V_GPU

R455 *10K_4 RAM_TYPE_CFG0
R454 *10K_4 RAM_TYPE_CFG1
R453 *10K_4 RAM_TYPE_CFG2
R456 *10K_4 RAM_TYPE_CFG3

VRAM TYPE

+3.3V_DELAY

R44 10K_4 RAM_CFG0
R40 *10K_4 RAM_CFG1
R33 *10K_4 RAM_CFG2

APERTURE SIZE

+3.3V_DELAY

R35 *10K_4 GFX_CORE_CNTRL0
R41 *10K_4 GFX_CORE_CNTRL1
R56 10K_4 GPIO0
R51 10K_4 GPIO1
R30 *10K_4 GPIO2
R63 *10K_4 GPIO3
R58 *10K_4 GPIO4
R47 *10K_4 GPIO5
R49 *10K_4 GPIO6
R31 *10K_4 GPIO8
R37 *10K_4 GPIO9
R43 *10K_4 GPIO10
R75 *10K_4 VGAVSYNC2
R39 10K_4 EXT_PANEL_BKEN

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

R48 1 2 TEMP_FAIL *10K_4

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

Power PWM config

Use 27Mhz Crystal for A test Danny0518

NC FOR PARK

RAM_TYPE_CFG0 AR8
RAM_TYPE_CFG1 AU8
RAM_TYPE_CFG2 AP8
RAM_TYPE_CFG3 AW8
AR3
AR1
AU1
AU3
AW3
AP6

NC FOR PARK

AW5 AU5 AR6 AW6 AU6 AT7 AV7 AN7 AV9 AT9 AR10 AW10 AU10 AP10 AV11 AT11 AR12 AW12 AU12 AP12

Accss to SCL and SDA is mandatory on BACO design for debug purposes.

+3.3V_DELAY
R70 *4.7K_4
R65 *4.7K_4

LVDS
EXT_LVDS_DDCCLK AK26
EXT_LVDS_DDCDAT AJ26

U34B

MUTI GFX

DVPCNTL_MVP_0 DVPCNTL_MVP_1 DVPCNTL_0 DVPCNTL_1 DVPCNTL_2 DVPCLK
DVPDATA_0 DVPDATA_1 DVPDATA_2 DVPDATA_3 DVPDATA_4 DVPDATA_5 DVPDATA_6 DVPDATA_7 DVPDATA_8 DVPDATA_9 DVPDATA_10 DVPDATA_11 DVPDATA_12 DVPDATA_13 DVPDATA_14 DVPDATA_15 DVPDATA_16 DVPDATA_17 DVPDATA_18 DVPDATA_19 DVPDATA_20 DVPDATA_21 DVPDATA_22 DVPDATA_23

DPA: TXCAP_DPA3P AU24, TXCAM_DPA3N AV23; TX0P_DPA2P AT25, TX0M_DPA2N AR24; TX1P_DPA1P AU26, TX1M_DPA1N AV25
DPB: TX2P_DPA0P AT27, TX2M_DPA0N AR26; TXCBP_DPB3P AR30, TXCBM_DPB3N AT29; TX3P_DPB2P AV31, TX3M_DPB2N AU30; TX4P_DPB1P AR32, TX4M_DPB1N AT31; TX5P_DPB0P AT33, TX5M_DPB0N AU32
DPC: TXCCP_DPC3P AU14, TXCCM_DPC3N AV13; TX0P_DPC2P AT15, TX0M_DPC2N AR14; TX1P_DPC1P AU16, TX1M_DPC1N AV15; TX2P_DPC0P AT17, TX2M_DPC0N AR16
DPD: TXCDP_DPD3P AU20, TXCDM_DPD3N AT19; TX3P_DPD2P AR20, TX3M_DPD2N AT21; TX4P_DPD1P AU22, TX4M_DPD1N AV21; TX5P_DPD0P AT23, TX5M_DPD0N AR22

NC FOR PARK

I2C: SCL, SDA

GENERAL PURPOSE I/O

GPIO0 AH20, GPIO1 AH18, GPIO2 AN16, GPIO3 AH23, GPIO4 AJ23, GPIO5 AH17, GPIO6 AJ17, GPIO_6 AK17, GPIO_7_BLON, GPIO8 AJ13, GPIO9 AH15, GPIO10 AJ16, RAM_CFG0 AK16, RAM_CFG1 AL16, RAM_CFG2 AM16, GPIO_13, GPIO_14_HPD2, GPIO_15_PWRCNTL_0, GPIO_16_SSIN, GPIO_17_THERMAL_INT, GPIO_18_HPD3, GPIO_19_CTF, GPIO_20_PWRCNTL_1, GPIO_21_BB_EN, GPIO_22_ROMCSB, GPIO_23_CLKREQB, JTAG_TRSTB, JTAG_TDI, JTAG_TCK, JTAG_TMS, JTAG_TDO, GENERICA, GENERICB, GENERICC, GENERICD, GENERICE_HPD4, GENERICF, GENERICG

EXT_PANEL_BKEN
44 GFX_CORE_CNTRL0
20 THERMAL_INT#
33 TEMP_FAIL
44 GFX_CORE_CNTRL1
T2 PAD AM14 GFX_CORE_CNTRL0 AM13 CLK_VGA_27M_SS_R AK14 AG30
T4 PAD AN14 TEMP_FAIL AM17 GFX_CORE_CNTRL1 AL13
T33 T5 T32 T12 T35 T34 T20 T17 T7 T6 T13 T10 T15 T11 T14 PAD AJ14 AK13 AN13 AM23 AN23 AK23 AL24 AM24 AJ19 AK19 AJ20 AK20 AJ24 AH26 AH24

GenericF/G is NC on PARK

EXT_HDMI_HPD AK24 HPD1

VREFG AH13

PLL/CLOCK: DPLL_PVDD AM32 AN32, DPLL_PVSS, DPLL_VDDC AN31, XO_IN AW34, XO_IN2 AW35, XTALIN AV33, XTALOUT AU34

DPLUS AF29, DMINUS AG29 THERMAL

TS_FDO, TSVDD AK32, TSVSS AJ32 AJ33

DAC1: R AD39 RB AD37, G AE36 GB AD35, B AF37 BB AE38, HSYNC AC36, VSYNC AC38, RSET AB34, AVDD AD34 AVSSQ AE34, VDD1DI AC33 VSS1DI AC34

EXT_CRT_R
EXT_CRT_G
EXT_CRT_B

RSET R87 499/F_4
+AVDD
+VDD1DI

DAC2: R2 AC30 R2B AC31, G2 AD30 G2B AD31, B2 AF30 B2B AF31, C AC32, Y AD32, COMP AF32, H2SYNC AD29, V2SYNC AC29 VGAVSYNC2, VDD2DI AG31 VSS2DI AG32, A2VDD AG33, A2VDDQ AD33, A2VSSQ AF33, R2SET AA29

R499 0_4 R81 0_4 C144 0.1U/10V/X7R_4 +VDD2DI
R82 0_4 +3.3V_DELAY
R89 0_4 +A2VDDQ
R2SET R73 2 1 715/F_4

NC on Seymour/Whistler

DDC/AUX: DDC1CLK AM26 DDC1DATA AN26, AUX1P AM27 AUX1N AL27, DDC2CLK AM19 DDC2DATA AL19, AUX2P AN20 AUX2N AM20, DDCCLK_AUX3P AL30 DDCDATA_AUX3N AM30, DDCCLK_AUX4P AL29 DDCDATA_AUX4N AM29, DDCCLK_AUX5P AN21 DDCDATA_AUX5N AM21, DDC6CLK AJ30 DDC6DATA AJ31, NC_DDCCLK_AUX7P AK30 NC_DDCDATA_AUX7N AK29

!!! NC when M92-M2/PARK
!!! NC when M92-M2/PARK

HDMI

CRT

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

Capilano Pro/Robson_M2

+1.8V_GPU L8 BLM15BD121SN1D 120ohm, 300mA +DPLL_PVDD (1.8V @ 120mA DPLL_PVDD)
C143 10U/6.3V/X5R_6 C142 1U/10V/X5R_4 C141 0.1U/10V/X7R_4

+1V_GFX_PCIE L7 BLM15BD121SN1D 120ohm, 300mA +DPLL_VDDC 1.0V @ 150mA DPLL_VDDC
C132 4.7U/6.3V/X5R_4 C131 1U/10V/X5R_4 C134 0.1U/10V/X7R_4

+1.8V_GPU R19 499/F_4 R15 249/F_4 C24 0.1U/10V/X7R_4 PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

CLK_VGA_27M_SS R59 *0_4 CLK_VGA_27M_SS_R R57 *10K_4

10 CLK_27M_VGA R477 100/F_4 R473 *0_4 R474 120/F_4 R476 0_4 R480 0_4 Y4 27MHZ R491 1M R475 R482 *0_4 C588 18P/50V/COG_4 C587 18P/50V/COG_4

R471 0_4 R469 0_4 XTAIN XTAOUT

20 VGA_THERMDP AF29
20 VGA_THERMDN AG29

+TSVDD (1.8V @ 20mA TSVDD)
+1.8V_GPU L13 BLM15BD121SN1D 120ohm, 300mA
C160 10U/6.3V/X5R_6 C153 1U/10V/X5R_4 C126 0.1U/10V/X7R_4

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

R488 150/F_4 R498 150/F_4 R497 150/F_4

+1.8V_GPU L14 BLM15BD121SN1D 120ohm, 300mA +AVDD (1.8V @ 70mA AVDD)
C181 10U/6.3V/X5R_6 C173 1U/10V/X5R_4 C159 0.1U/10V/X7R_4

+1.8V_GPU L18 BLM15BD121SN1D 120ohm, 300mA +VDD1DI (1.8V @ 45mA VDD1DI)
C187 10U/6.3V/X5R_6 C163 1U/10V/X5R_4 C178 0.1U/10V/X7R_4 R83 *0_4/S +VDD2DI (1.8V @ 40mA VDD2DI)

+1.8V_GPU L11 BLM15BD121SN1D 120ohm, 300mA +A2VDDQ (1.8V @ 20mA A2VDDQ)
C157 1U/10V/X5R_4 C161 0.1U/10V/X7R_4

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

18,19,43 +1.8V_GPU
18,20,24 +3.3V_DELAY
16,18,19,38,44 +1V_GFX_PCIE

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Quanta Computer Inc.
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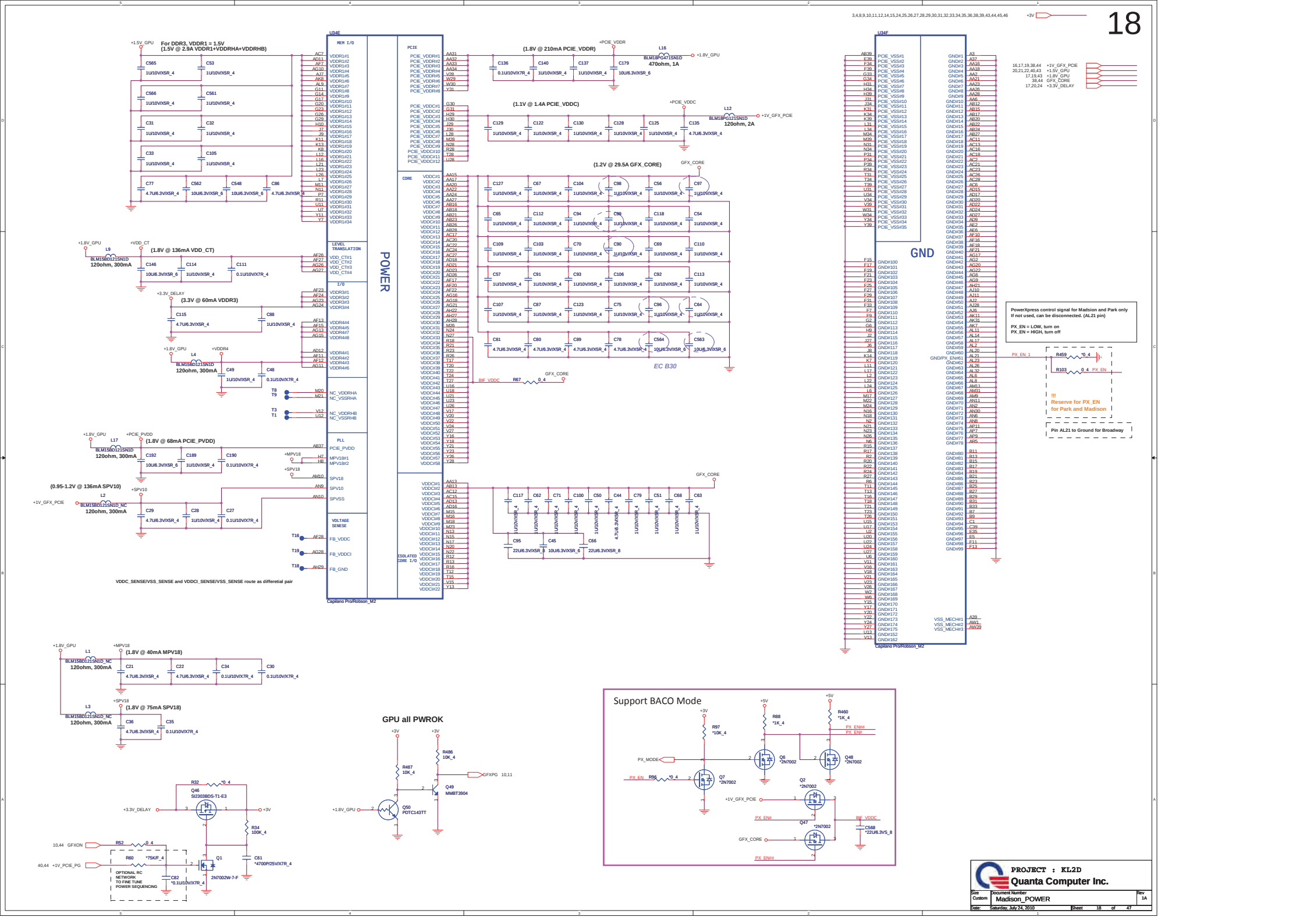
POWER
GND
U34E
U34F
Capilano Pro/Robson_M2
For DDR3, VDDR1 = 1.5V
(1.5V @ 2.9A VDDR1+VDDRHA+VDDRHB)
(1.8V @ 210mA PCIE_VDDR)
(1.1V @ 1.4A PCIE_VDDC)
(1.2V @ 29.5A GFX_CORE)
EC B30
(1.8V @ 136mA VDD_CT)
(3.3V @ 60mA VDDR3)
(1.8V @ 68mA PCIE_PVDD)
(0.95-1.2V @ 136mA SPV10)
(1.8V @ 40mA MPV18)
(1.8V @ 75mA SPV18)
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
Reserve for PX_EN
for Park and Madison
Pin AL21 to Ground for Broadway
GPU all PWROK
Support BACO Mode
OPTIONAL RC
NETWORK
TO FINE TUNE
POWER SEQUENCING
PROJECT : KL2D
Quanta Computer Inc.
Madison_POWER
Saturday, July 24, 2010
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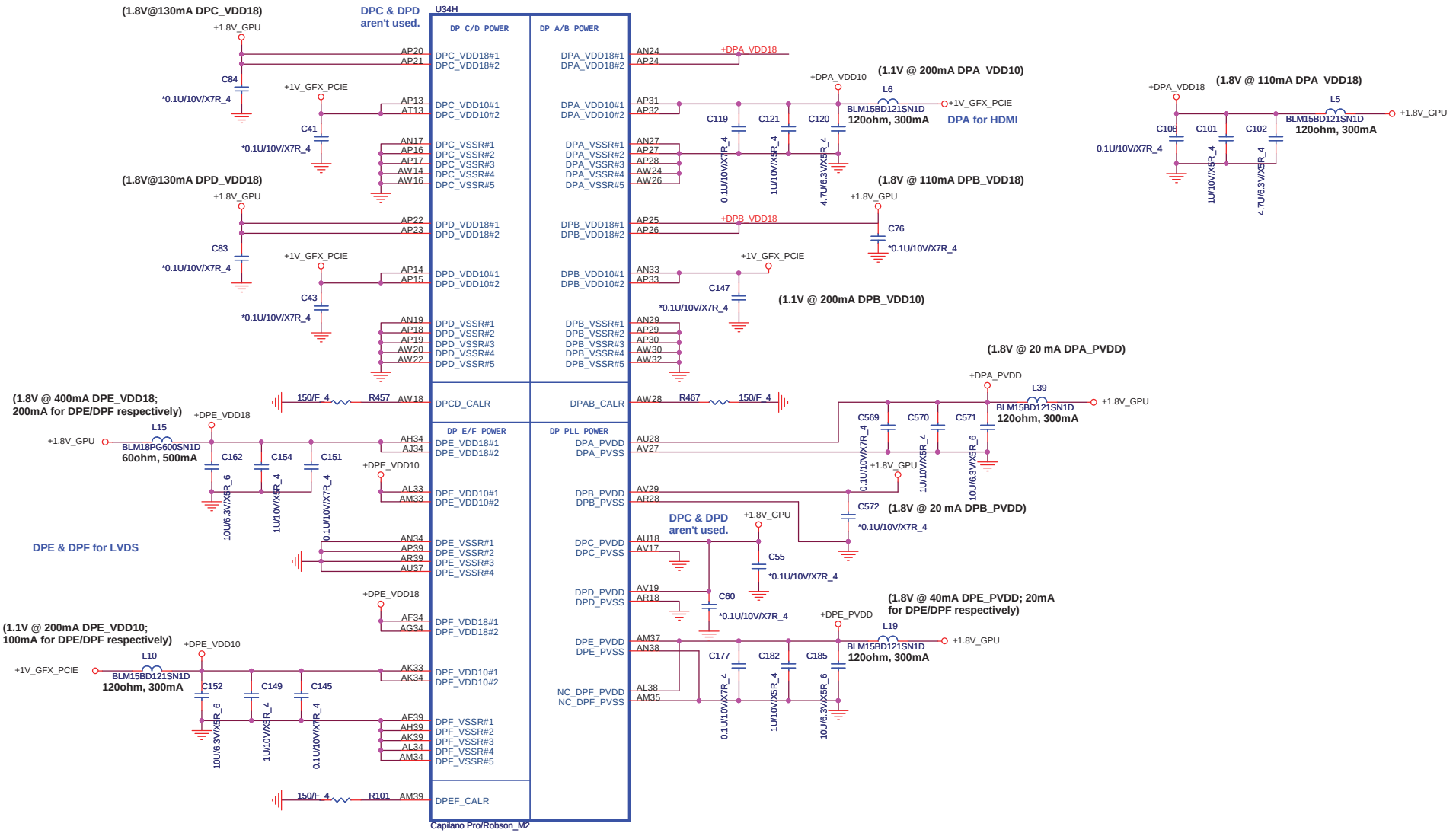
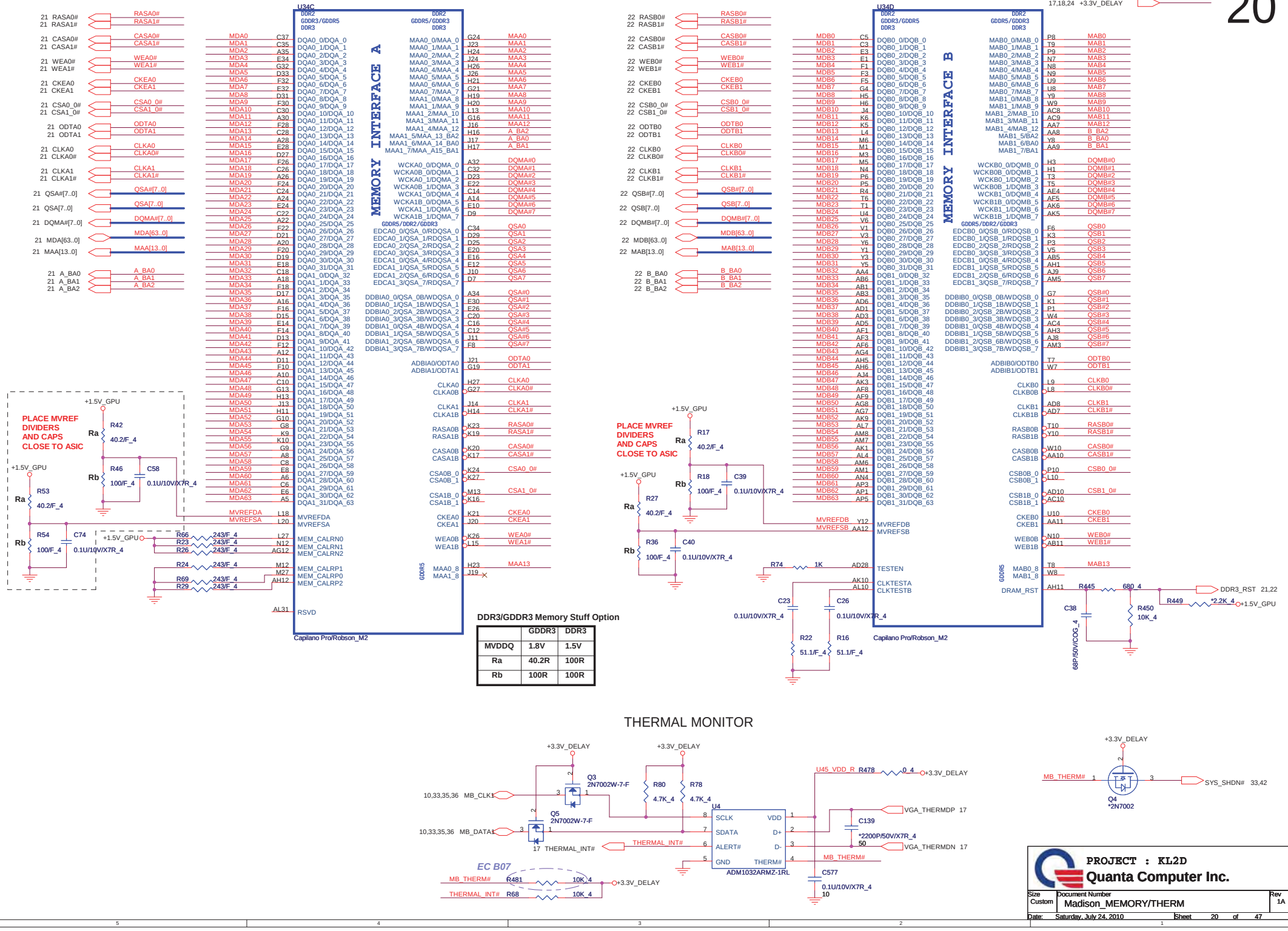
16,17,18,38,44 +1V_GFX_PCIE
17,18,43 +1.8V_GPU

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V



PROJECT :	KL2D
Quanta Computer Inc.	
Size: Custom	Document Number: Madison_DP_POWER
Rev: 1A	
Date: Saturday, July 24, 2010	Sheet 19 of 47


U34C
MEMORY INTERFACE A
DDR2
GDDR3/GDDR5
DDR3
Capilano Pro/Robson_M2
U34D
MEMORY INTERFACE B
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
+1.5V_GPU
+3.3V_GPU
DDR3/GDDR3 Memory Stuff Option
MVDDQ 1.8V 1.5V
Ra 40.2R 100R
Rb 100R 100R
THERMAL MONITOR
U4
ADM1032ARMZ-1RL
EC B07
Q3 2N7002W-7-F
Q4 *2N7002
Q5 2N7002W-7-F
PROJECT : KL2D
Quanta Computer Inc.
Size Custom
Document Number Madison_MEMORY/THERM
Rev 1A
Date: Saturday, July 24, 2010
Sheet 20 of 47

DDR3 64MX16, CH A : 512MB

18,20,22,40,43 +1.5V_GPU

U5 / U38 / U3 / U35 — K4W1G1646E-HC12 (100-BALL SDRAM DDR3)

20 CLKA0 / 20 CLKA0# / 20 CKEA0 / 20 ODTA0 / 20 CSA0_0# / 20 RASA0# / 20 CASA0# / 20 WEA0# / 20,22 DDR3_RST / R94 240/F 4

20 CLKA1 / 20 CLKA1# / 20 CKEA1 / 20 ODTA1 / 20 CSA1_0# / 20 RASA1# / 20 CASA1# / 20 WEA1# / R71 240/F 4

R490 240/F 4 / R461 240/F 4

20 MDA[63..0] / 20 MAA[13..0] / 20 QSA#[7..0] / 20 QSA[7..0] / 20 DQMA#[7..0] / 20 A_BA[2..0]

Placement has to be close to VRAM

CLKA0 R105 56 4 — C184 0.01U/16V/X7R 4

CLKA0# R102 56 4

CLKA1 R45 56 4 — C52 0.01U/16V/X7R 4

CLKA1# R50 56 4

+1.5V_GPU

R86 4.99K/F_4 — VREF_A0 — R92 4.99K/F_4 — C156 0.1U/10V/X7R_4

R84 4.99K/F_4 — VREF_A1 — R85 4.99K/F_4 — C150 0.1U/10V/X7R_4

R483 4.99K/F_4 — VREF_A2 — R485 4.99K/F_4 — C583 0.1U/10V/X7R_4

R492 4.99K/F_4 — VREF_A3 — R493 4.99K/F_4 — C591 0.1U/10V/X7R_4

R62 4.99K/F_4 — VREF_A4 — R64 4.99K/F_4 — C116 0.1U/10V/X7R_4

R61 4.99K/F_4 — VREF_A5 — R55 4.99K/F_4 — C85 0.1U/10V/X7R_4

R468 4.99K/F_4 — VREF_A6 — R464 4.99K/F_4 — C567 0.1U/10V/X7R_4

R463 4.99K/F_4 — VREF_A7 — R466 4.99K/F_4 — C573 0.1U/10V/X7R_4

Close to U4

C579 1U/6.3V/X5R_4 — C205 *1U/6.3V/X5R_4 — C596 1U/6.3V/X5R_4 — C595 *1U/6.3V/X5R_4 — C191 1U/6.3V/X5R_4

Close to U44

C608 1U/6.3V/X5R_4 — C580 *1U/6.3V/X5R_4 — C578 1U/6.3V/X5R_4 — C586 *1U/6.3V/X5R_4 — C584 1U/6.3V/X5R_4

Close to U3

C59 1U/6.3V/X5R_4 — C138 *1U/6.3V/X5R_4 — C37 1U/6.3V/X5R_4 — C42 *1U/6.3V/X5R_4 — C47 1U/6.3V/X5R_4

Close to U41

C560 1U/6.3V/X5R_4 — C581 *1U/6.3V/X5R_4 — C575 1U/6.3V/X5R_4 — C592 *1U/6.3V/X5R_4 — C574 1U/6.3V/X5R_4

Close to U4 & U44

C225 10U/6.3V/X5R_6 — C124 4.7U/6.3V/X5R_4 — C585 10U/6.3V/X5R_6 — C148 *10U/6.3V/X5R_6 — C133 4.7U/6.3V/X5R_4

Close to U3 & U41

C72 4.7U/6.3V/X5R_4 — C607 10U/6.3V/X5R_6 — C576 10U/6.3V/X5R_6 — C46 *10U/6.3V/X5R_6 — C73 4.7U/6.3V/X5R_4

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
C	Madison_DDR3_A_512M	1A

Date: Saturday, July 24, 2010 Sheet 21 of 47

DDR3 64MX16, CH B : 512MB

18,20,21,40,43 +1.5V_GPU

U29 / U1 / U2 / U30 — K4W1G1646E-HC12 — 100-BALL SDRAM DDR3

20 CLKB0 / 20 CLKB0# / 20 CKEB0 — R440 240/F 4 — 20,21 DDR3_RST

20 CLKB1 / 20 CLKB1# / 20 CKEB1 — R12 240/F 4 — 20 ODTB1 / 20 CSB1_0# / 20 RASB1# / 20 CASB1# / 20 WEB1#

R9 240/F 4 — R438 240/F 4

20 MDB[63..0] / 20 MAB[13..0] / 20 QSB#[7..0] / 20 QSB[7..0] / 20 DQMB#[7..0] / 20 B_BA[2..0]

+1.5V_GPU

R448 4.99K/F_4 — R444 4.99K/F_4 — C550 0.1U/10V/X7R_4 — VREF_B0

R435 4.99K/F_4 — R436 4.99K/F_4 — C537 0.1U/10V/X7R_4 — VREF_B1

R4 4.99K/F_4 — R5 4.99K/F_4 — C8 0.1U/10V/X7R_4 — VREF_B2

R13 4.99K/F_4 — R14 4.99K/F_4 — C20 0.1U/10V/X7R_4 — VREF_B3

R11 4.99K/F_4 — R10 4.99K/F_4 — C15 0.1U/10V/X7R_4 — VREF_B4

R6 4.99K/F_4 — R7 4.99K/F_4 — C9 0.1U/10V/X7R_4 — VREF_B5

R437 4.99K/F_4 — R434 4.99K/F_4 — C533 0.1U/10V/X7R_4 — VREF_B6

R446 4.99K/F_4 — R447 4.99K/F_4 — C551 0.1U/10V/X7R_4 — VREF_B7

Placement has to be close to VRAM

CLKB0 R2 56_4 — CLKB0# R3 56_4 — C7 0.01U/16V/X7R_4

CLKB1 R8 56_4 — CLKB1# R1 56_4 — C5 0.01U/16V/X7R_4

Close to U35

C536 1U/6.3V/X5R_4 — C528 *1U/6.3V/X5R_4 — C530 1U/6.3V/X5R_4 — C529 *1U/6.3V/X5R_4 — C549 1U/6.3V/X5R_4

Close to U1

C18 1U/6.3V/X5R_4 — C1 *1U/6.3V/X5R_4 — C6 1U/6.3V/X5R_4 — C2 *1U/6.3V/X5R_4 — C538 1U/6.3V/X5R_4

Close to U2

C535 1U/6.3V/X5R_4 — C3 *1U/6.3V/X5R_4 — C16 1U/6.3V/X5R_4 — C4 *1U/6.3V/X5R_4 — C12 1U/6.3V/X5R_4

Close to U36

C527 1U/6.3V/X5R_4 — C532 *1U/6.3V/X5R_4 — C544 1U/6.3V/X5R_4 — C531 *1U/6.3V/X5R_4 — C534 1U/6.3V/X5R_4

Close to U35 & U1

C526 10U/6.3V/X5R_6 — C555 10U/6.3V/X5R_6 — C11 10U/6.3V/X5R_6 — C17 4.7U/6.3V/X5R_4 — C19 *4.7U/6.3V/X5R_4

Close to U2 &U36

C14 4.7U/6.3V/X5R_4 — C545 10U/6.3V/X5R_6 — C525 10U/6.3V/X5R_6 — C10 *10U/6.3V/X5R_6 — C13 4.7U/6.3V/X5R_4

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
C	Madison_DDR3_B_512M	1A

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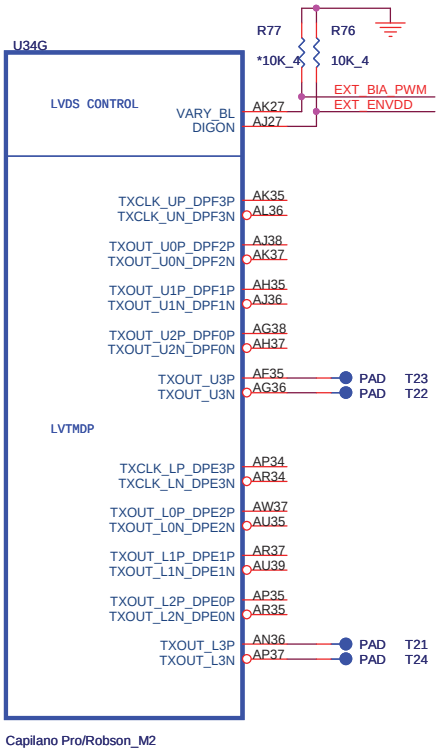
CRT SWITCH



PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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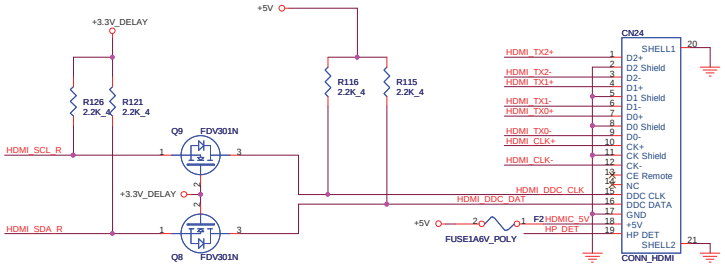
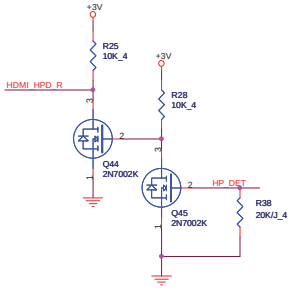
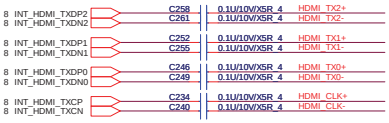
DIS/SG HDMI

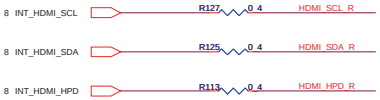


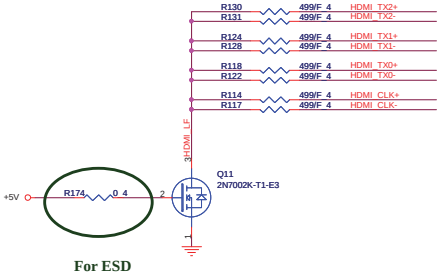
HDMI Hot-PLUG to EC and GPU



UMA Only / Muxless HDMI

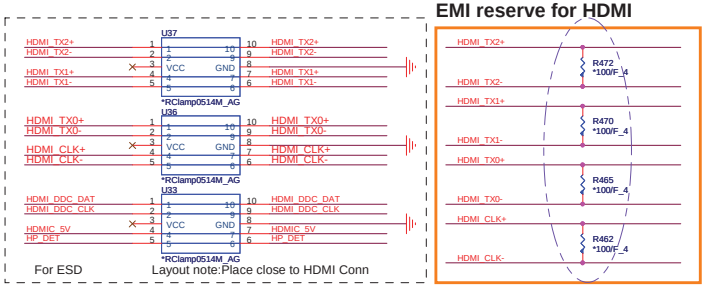






For ESD

EMI reserve for HDMI

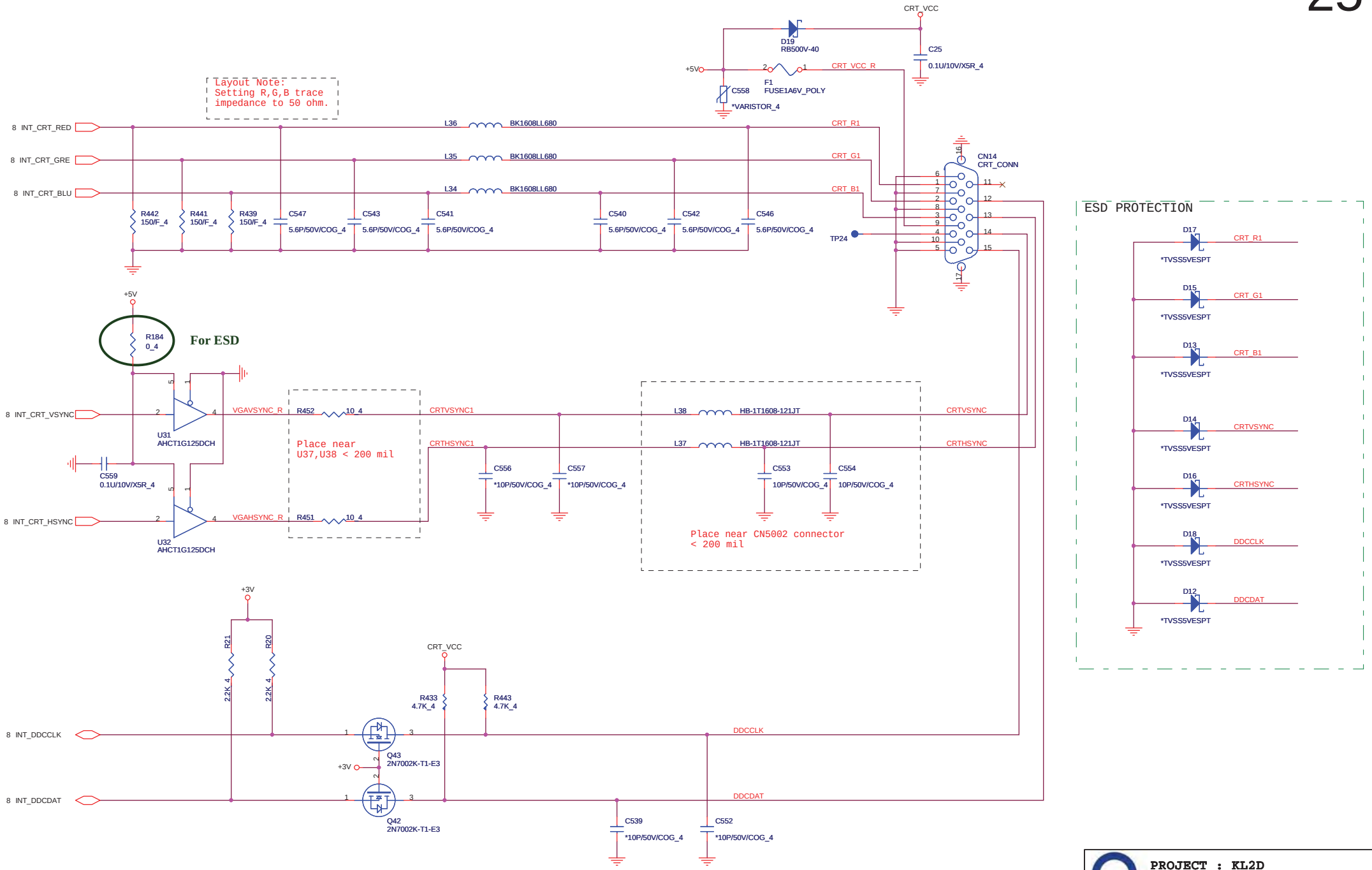


8,9,12,18,25,26,28,29,33,34,36,38,39 +5V
3,4,8,9,10,11,12,14,15,18,25,26,27,28,29,30,31,32,33,34,35,36,38,39,43,44,45,46 +3V
17,18,20 +3.3V_DELAY

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

Date: Saturday, July 24, 2010 Sheet 24 of 47



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CONN	1A
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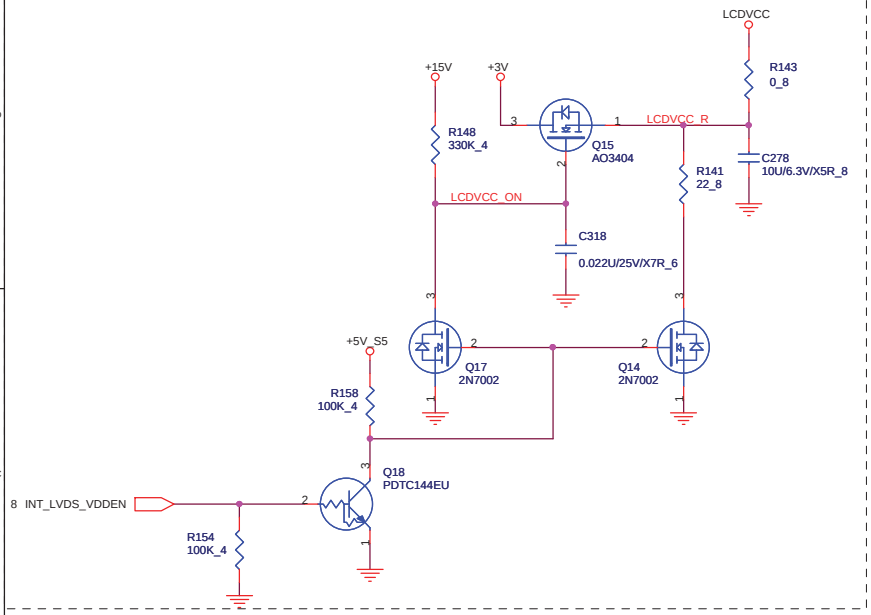
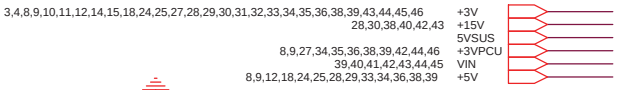
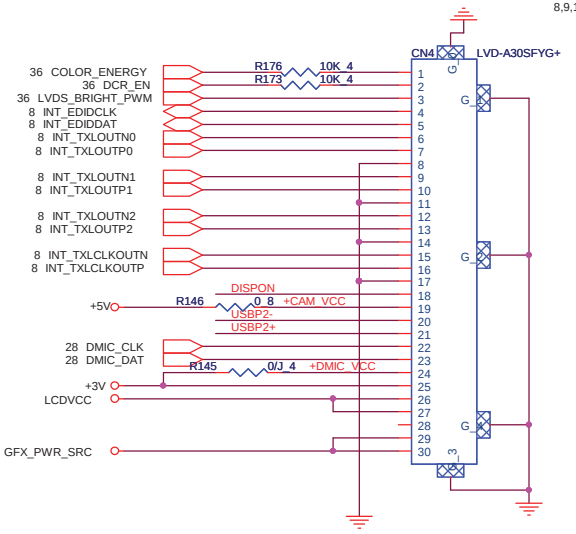
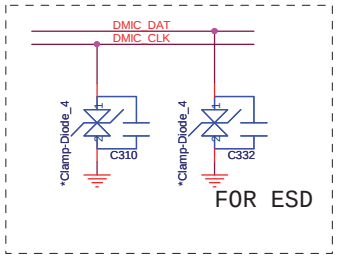
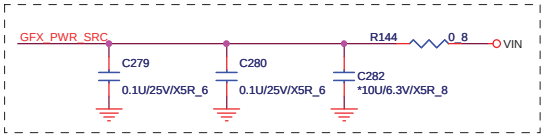
LCDVCC



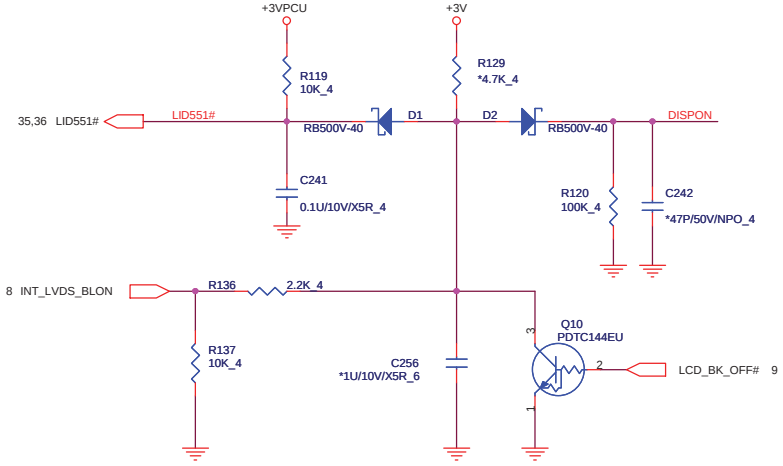


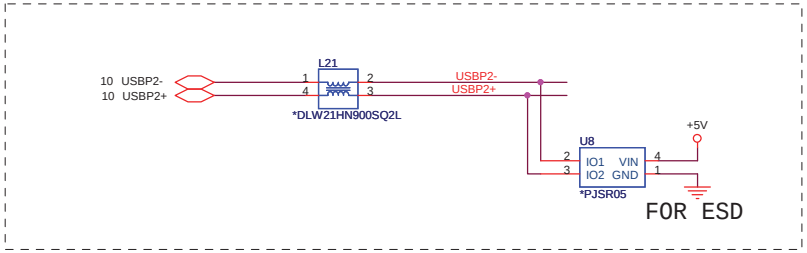






back light





PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A

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8,9,26,34,35,36,38,39,42,44,46 +3VPCU
3,4,8,9,10,11,12,14,15,18,24,25,26,28,29,30,31,32,33,34,35,36,38,39,43,44,45,46 +3V

Core Power Decoupling

VDDIO Power Decoupling

U13

BCM57780
7mm x 7mm
48-Pin QFN

Package Body

Transformer

U11 LFE9292A-R

U12 *CM1293A-04SO

U10 *CM1293A-04SO

RJ45 Connector

CN17 JM36113-N4525-7F

3.3V LANVCC

Q23 AO6402

Q57 PDTC144EU

Q24 PDTC144EU

U44 *74AHCT1G08GW

U14 M24C02-WMN6TP

3.3V Device ONLY

PROJECT : KL2D
Quanta Computer Inc.
Size: Custom
Document Number: LAN (BCM57780, RJ45)
Rev: 1A
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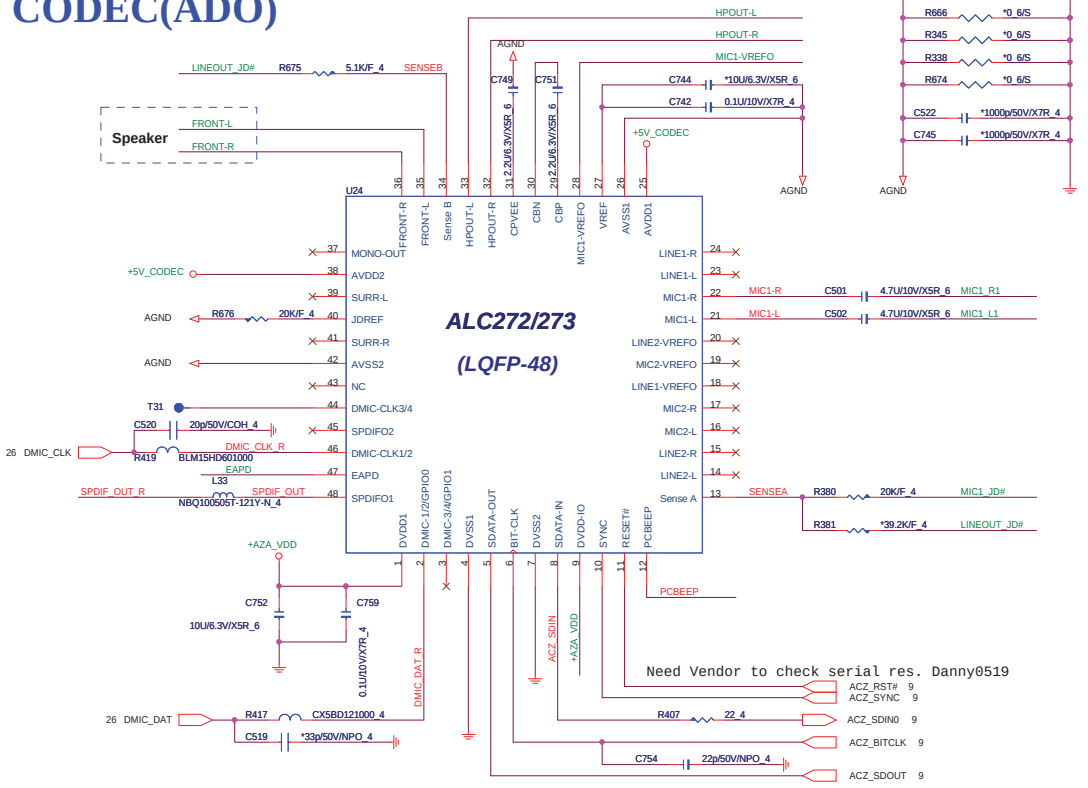
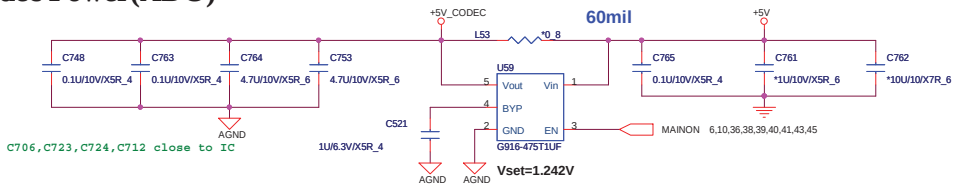
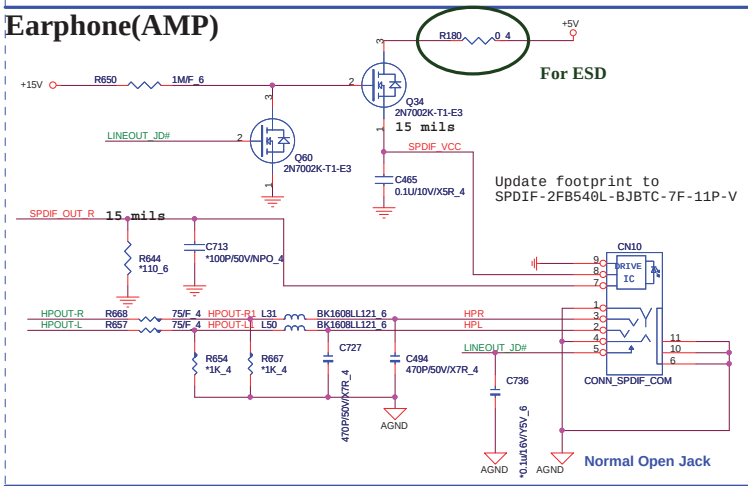
CODEC(ADO)



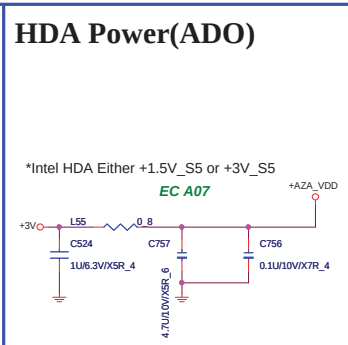
Codec Power(ADO)



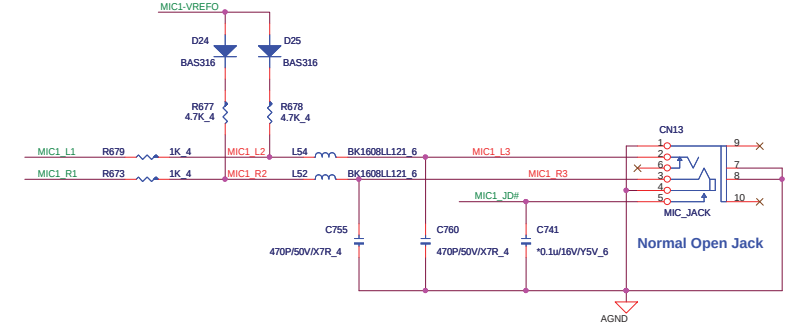
Earphone(AMP)



HDA Power(ADO)

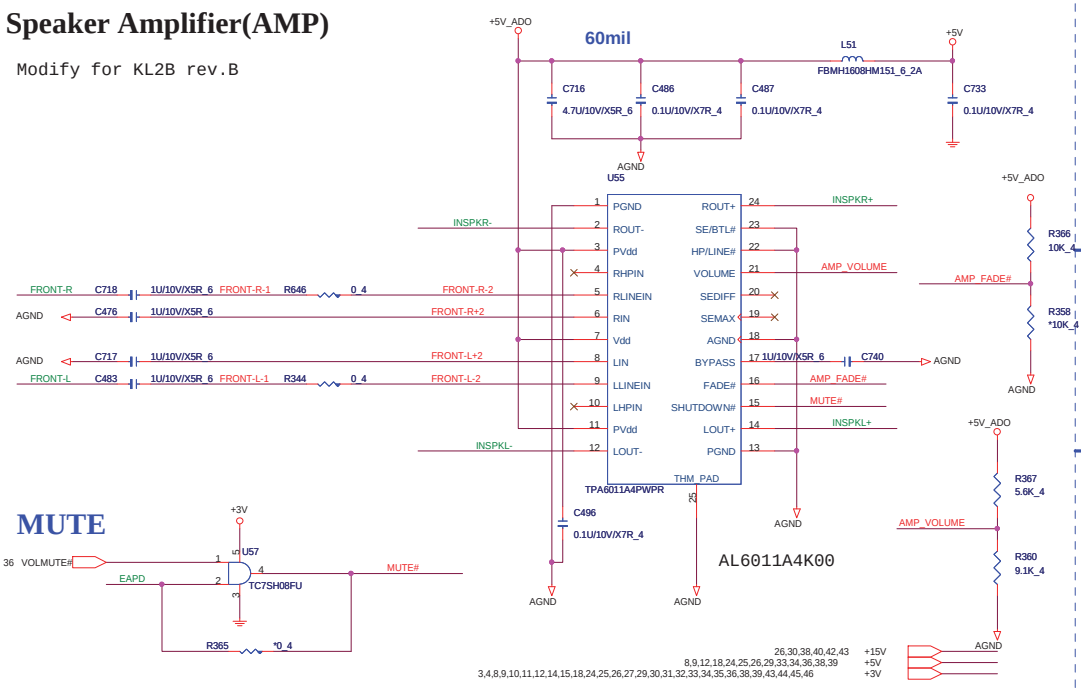


System MIC(AMP)



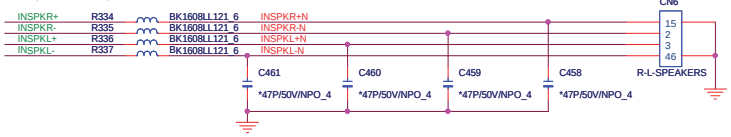
Speaker Amplifier(AMP)

Modify for KL2B rev.B

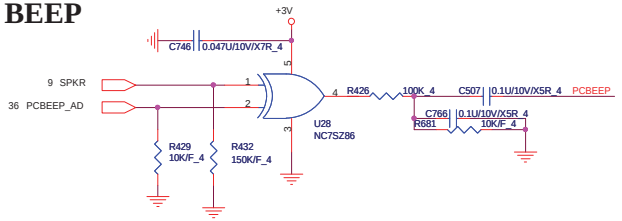


MUTE

Speaker(AMP)



PC BEEP



PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	AL272/AMP/MIC/LINE-OUT	1A

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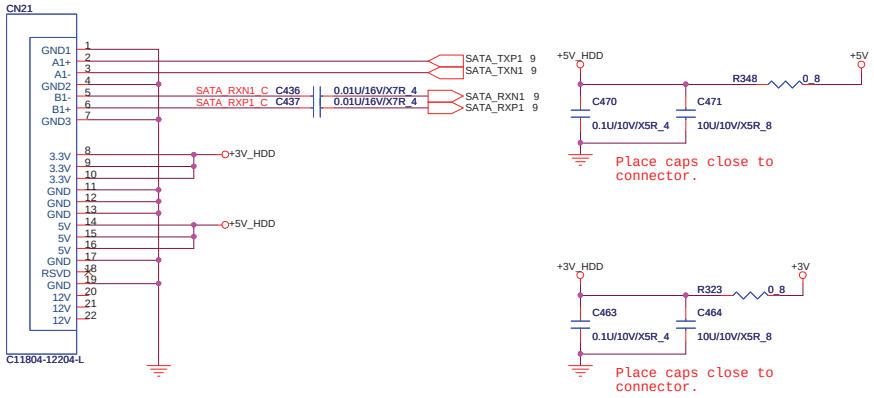
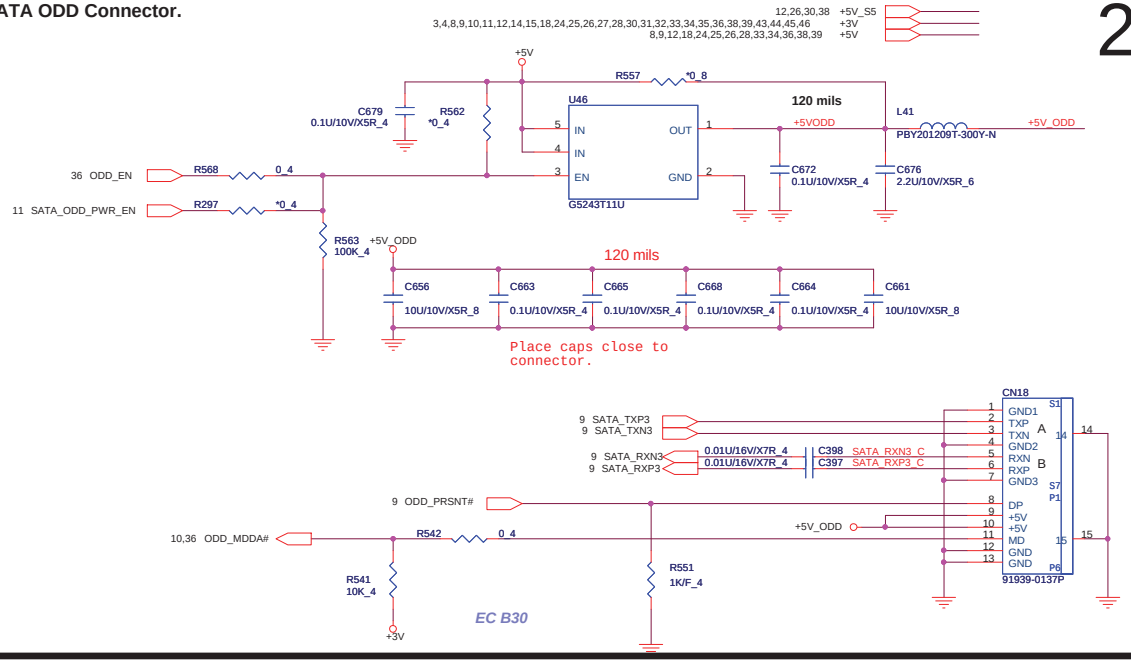
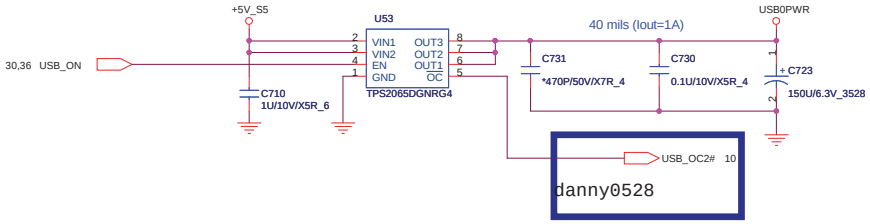
SATA HDD Connector.

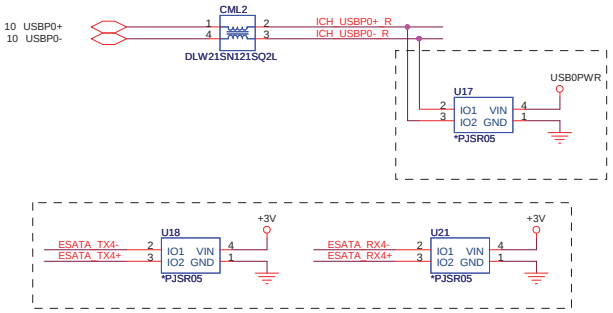


SATA ODD Connector.

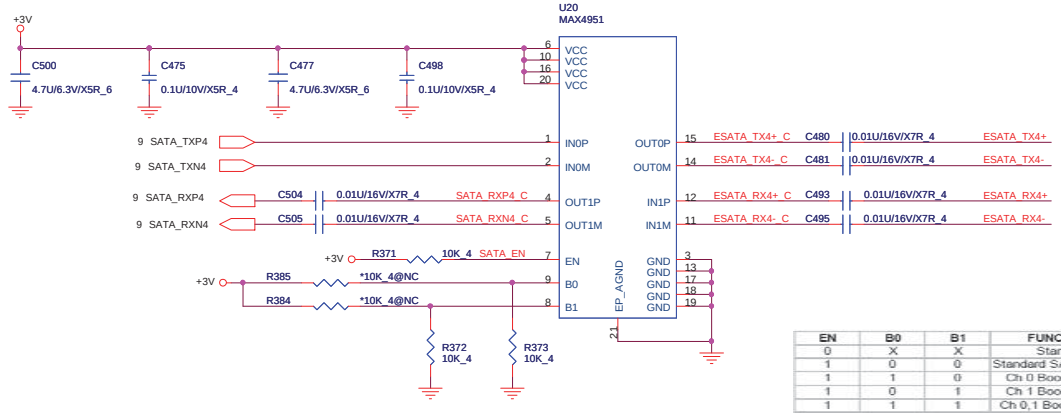


USB + E-SATA

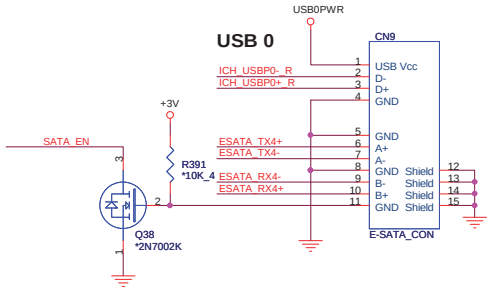




E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

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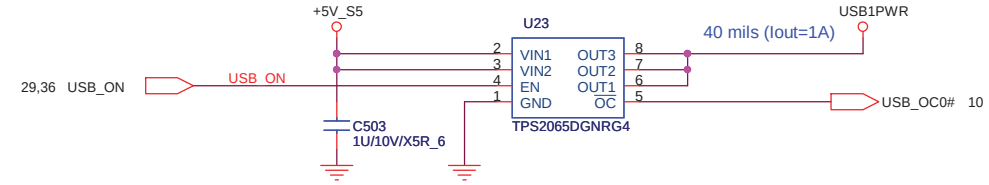
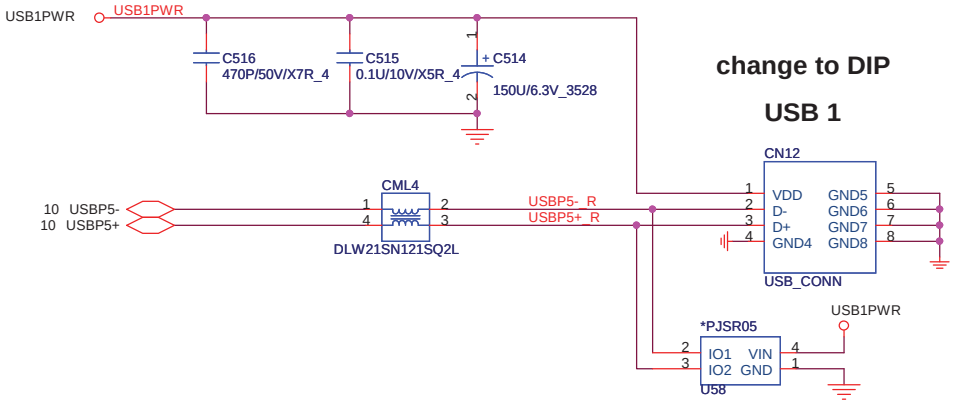
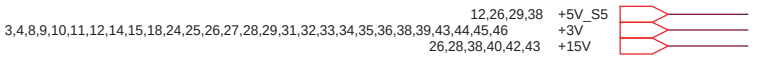
USBX3

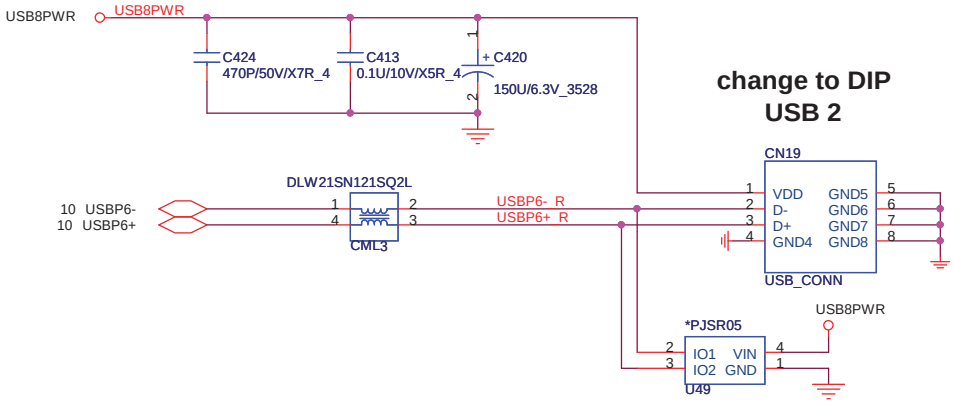


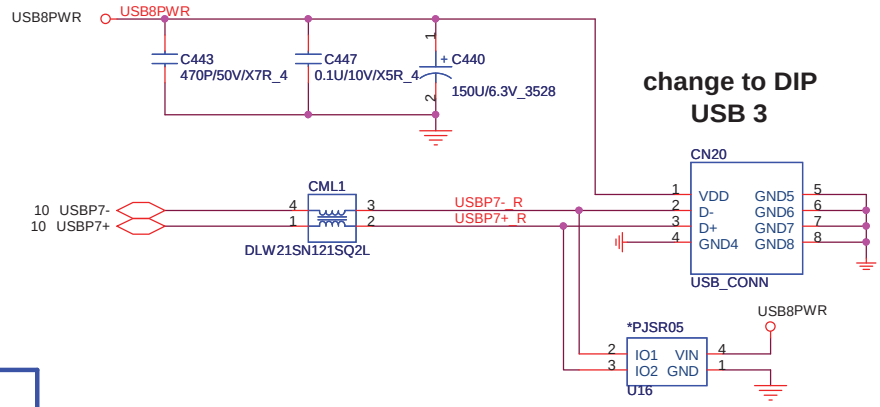


USB 1

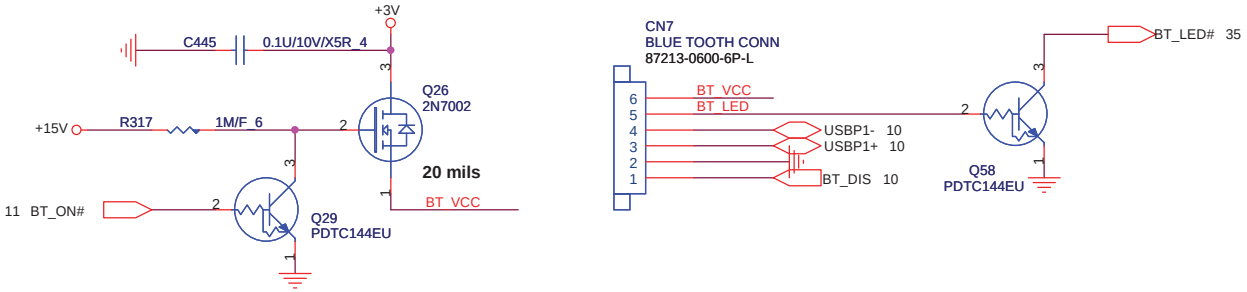


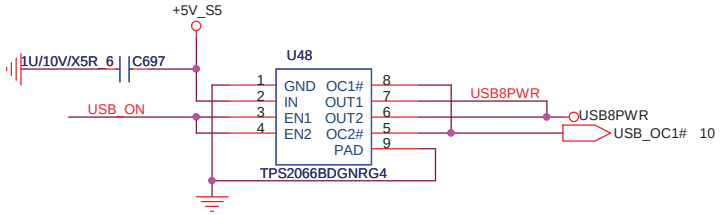
29





BLUETOOTH





PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB X3/BT	1A

Date: Saturday, July 24, 2010 Sheet 30 of 47

3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,32,33,34,35,36,38,39,43,44,45,46 +3V

7 IN 1 CARD READER

C640 & C639 close to APVDD(pin5)
(length must under 120mil) and
trace width = 30mil, after C640,
pls put one more 0.1uF for it.

+1.8V_VDD
C462 10U/6.3V/X5R_6
C468 0.1U/10V/X5R_4
C466 0.1U/10V/X5R_4
C735 0.1U/10V/X5R_4
C720 1000P/50V/X7R_4

+3V
R638 0_8
C732 10U/6.3V/X5R_6
C725 0.1U/10V/X5R_4
C715 0.1U/10V/X5R_4
C721 0.1U/10V/X5R_4
C712 0.1U/10V/X5R_4
+3V_CARD

JMB385 C Only
R662 *0_4

JMB387 A Only
R656 0_4

U54
JMB385 C
JMB387 A
JMICRON

XD_D4/MS_D4
XD_D5/MS_D5
XD_D6/MS_D6
XD_D7/MS_D7
XD_RE#
XD_R/B#
XD_ALE
PWR_CTRL
SD_MMC_CD#
MS_CD#
xD_CD#
CR_CPPE#
R636 *0_4/S
EC C01
PCIE_CLKREQ_CAD# 10

XD_CLE
XD_WP#/SD_WP/MMC_WP#
XD_CE#/MS_SCLK/SD_CLK_L
XD_WE#/MS_BS/SD_CMD
XD_D3/MS_D3/SD_D3
XD_D2/MS_D2/SD_D2
XD_D1/MS_D1/SD_D1
XD_D0/MS_D0/SD_D0

4,10,27,32 PLTRST#
PCIE_RX7+_C C709 0.1U/10V/X5R_4
PCIE_RX7-_C C708 0.1U/10V/X5R_4
PCIE_RXP7_CARD 10
PCIE_RXN7_CARD 10
10 CLK_PCIE_CADN
10 CLK_PCIE_CADP
R634 9.1K_4
PCIE_TXN7_CARD 10
PCIE_TXP7_CARD 10
Trace width = 12mil" at PREXT

CN11
R015-212-LM
VCC_XD

Memory Card Power Supply

250mA
PWR_CTRL
VCC_XD

Use 0805 type and
Trace width = 30 mil"
at MC_PWR_CTRL#,
C719 0.1U/10V/X5R_4
C455 10U/6.3V/X5R_6
C452 1U/6.3V/X5R_4

XD_CE#/MS_SCLK/SD_CLK_L R649 22_4 XD_CE#/MS_SCLK/SD_CLK
C726 20P/50V/COG_4

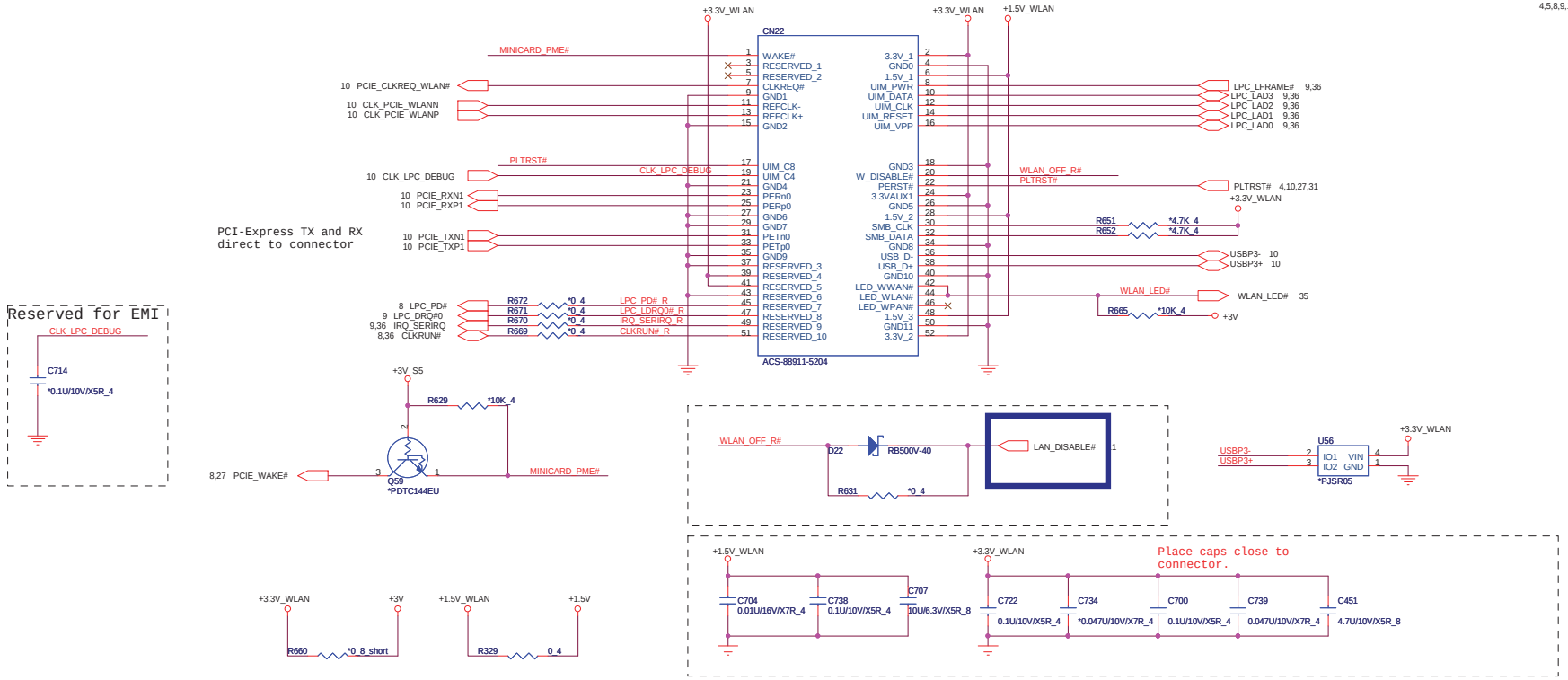
+3V_CARD
R637 4.7K_4 xD_CD#
R642 4.7K_4 MS_CD#
R643 4.7K_4 SD_MMC_CD#
R653 10K_4 XD_CLE

VCC_XD
R342 10K_4 XD_WE#/MS_BS/SD_CMD
R659 1K_4 XD_R/B#
R349 10K_4 XD_WP#/SD_WP/MMC_WP#
XD_RE# R663 200K_4
XD_ALE R655 200K_4

PROJECT : KL2D
Quanta Computer Inc.

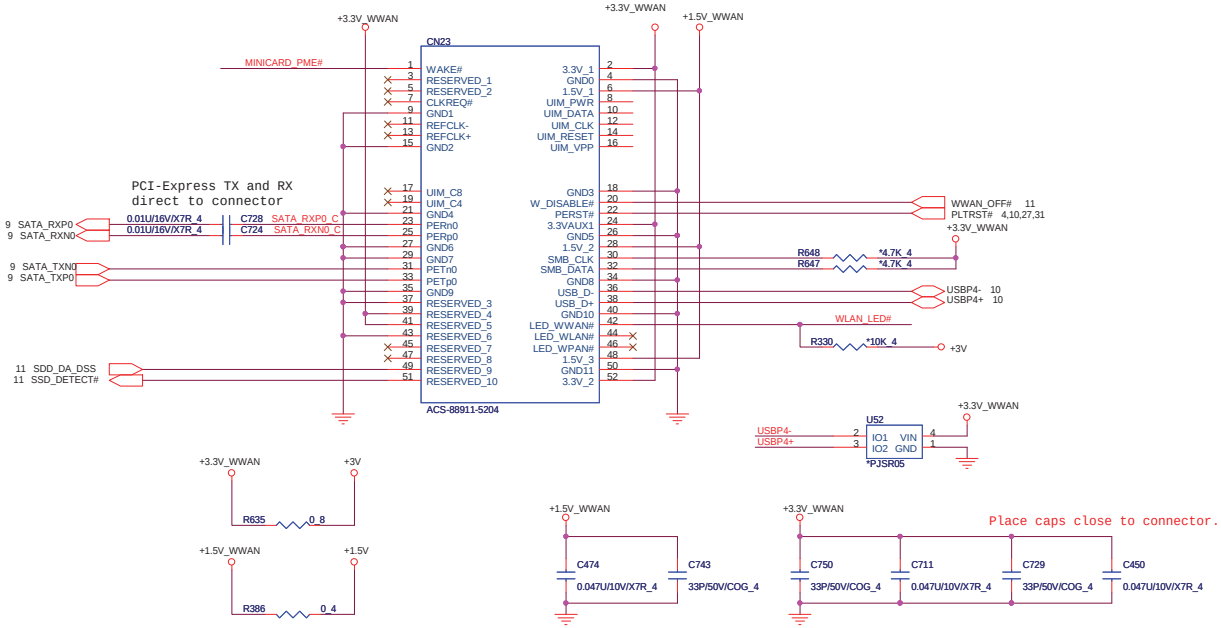
Size	Document Number	Rev
Custom	JMB385/387 Card Reader	1A
Date: Saturday, July 24, 2010	Sheet 31 of 47	

MiniCard WLA connector



MiniCard WWAN/SATA SSD connector

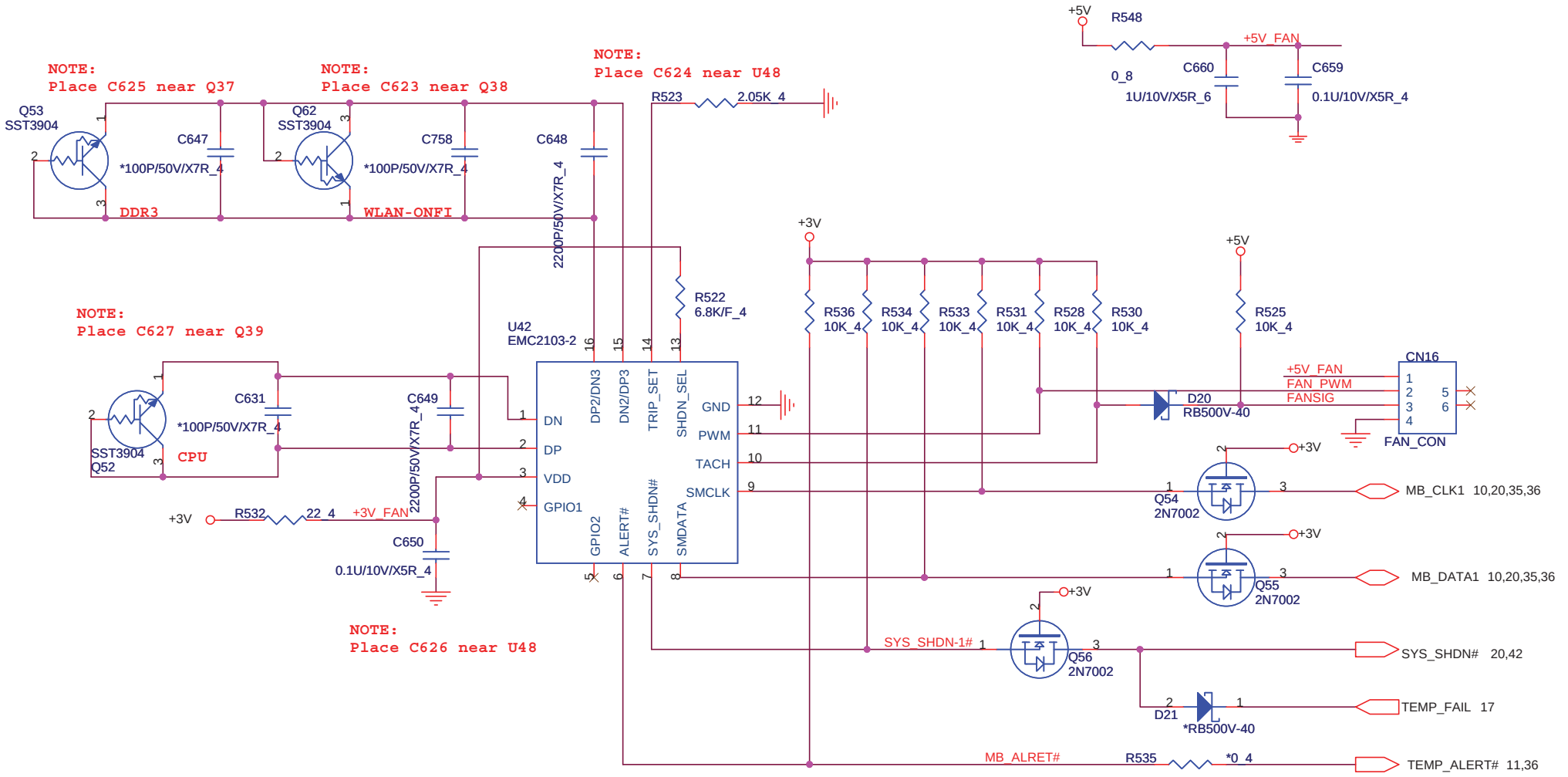
SIM Card CONN



FAN CONTROL

3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,34,35,36,38,39,43,44,45,46 +3V
8,9,12,18,24,25,26,28,29,34,36,38,39 +5V

33

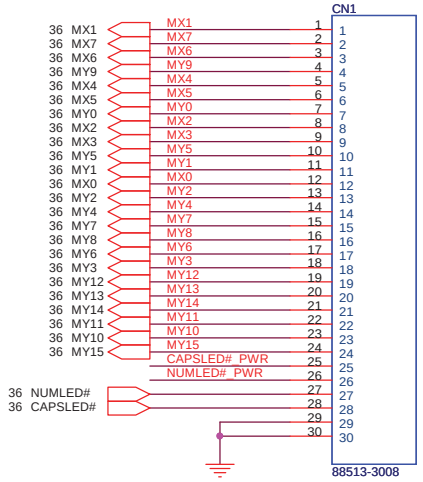


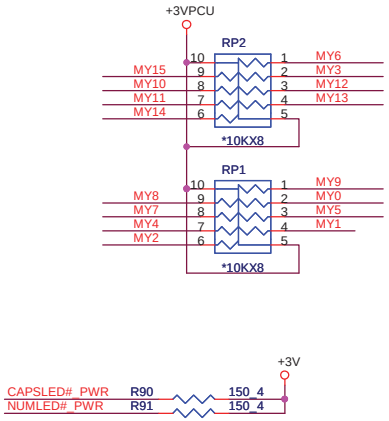
PROJECT : KL2D

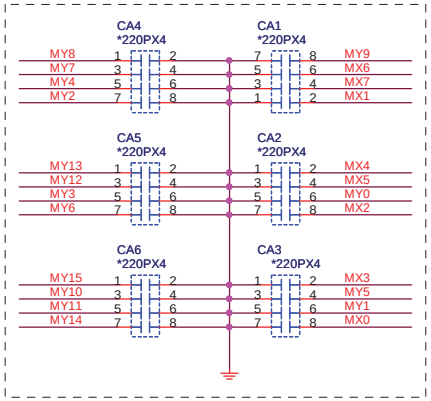
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A
Date: Saturday, July 24, 2010	Sheet 33 of 47	

KEYBOARD



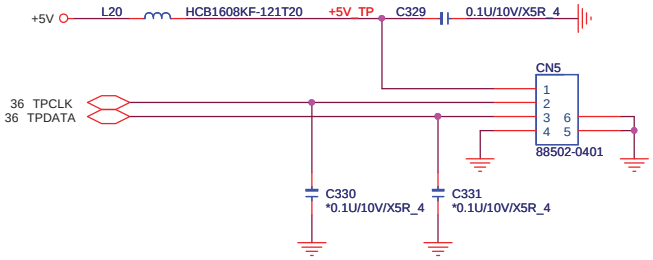




For EMI request

8,9,12,18,24,25,26,28,29,33,36,38,39 +5V
8,9,26,27,35,36,38,39,42,44,46 +3VPCU
26,28,30,38,40,42,43 +15V
3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,35,36,38,39,43,44,45,46 +3V
5VSUS

Touch pad



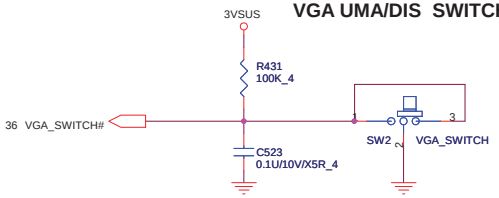
Backlight Keybaord Con.

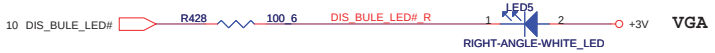
PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B, T/P	1A

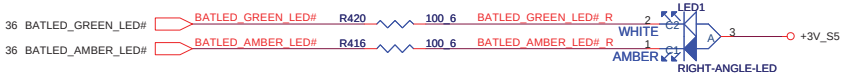
Date: Saturday, July 24, 2010 Sheet 34 of 47

VGA UMA/DIS SWITCH

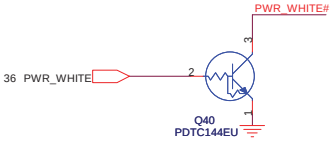


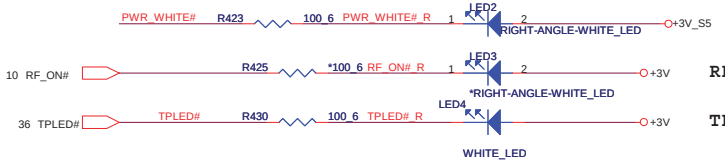


VGA



Battery



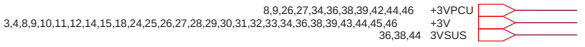


Power/suspend LED

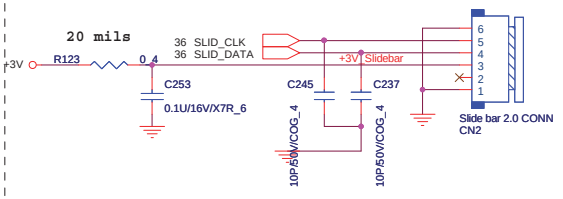
RF

TP

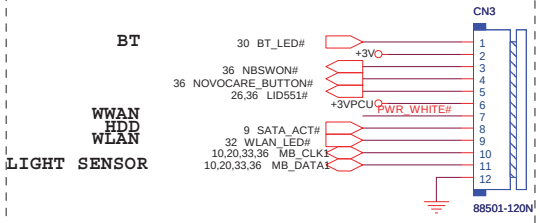
Logo LED CONN



Slide bar 2.0



POWER BOARD



5VPCU Cable for CPU Core Power

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	B TO B CON/LED	1A
Date: Saturday, July 24, 2010	Sheet 35 of 47	

IT8518 IT8519

Rev.B

RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

16Mbit (2M Byte), SPI

Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13

MX25L1605A

Borad ID

DIS =>R275
UMA=>R274

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

(For PLL Power)

LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC IT8512E	1A

Date: Saturday, July 24, 2010 Sheet 36 of 47

MiniCard WLAN

HOLE28 H-TC197D79PT
HOLE30 H-TC197D79PT

MiniCard WWAN

HOLE31 H-TC197D79PT

Hole for PCH support

HOLE24 H-TC197D59PT
HOLE27 H-TC197D59PT

HOLE32 H-TC197D79PT
HOLE33 H-TC197D79PT
HOLE34 H-TC197D79PT
HOLE35 H-TC197D79PT
HOLE36 H-TC197D79PT
HOLE37 H-TC197D79PT

Hole for CPU support

HOLE4 *H-C142D142N
HOLE8 *H-C142D142N
HOLE5 *H-C142D142N
HOLE7 *h-bc142tc221d142pt

VGA nut

HOLE20 H-TC197BC138I102D102P2
HOLE22 H-TC197BC138I102D102P2

PAD

HOLE25 *SPAD-S79
HOLE26 *SPAD-S79
HOLE21 *SPAD-S83X71
HOLE23 *SPAD-S87X73

Boundary Hole

HOLE1 *h-sd106p2-kl2
HOLE11 *H-C315I3146BO378D106P2
HOLE15 *H-C118D118N
HOLE18 *H-C315I126D106P2
HOLE19 *H-C315I126D106P2
HOLE13 *H-TC197BC256D106P2
HOLE17 *H-C315I126D106P2
HOLE16 *H-C315I126D106P2
HOLE14 *H-C118D118N
HOLE9 *H-TC197BC256D106P2
HOLE3 *H-C315I126D106P2

ESD Mask Copper

CO1 CO2 CO3 CO4 CO5 CO6 CO7 CO8 CO9 CO10 CO11 CO12
CO13 CO14 CO15 CO16 CO17 CO18 CO19 CO20 CO21 CO22

Boundary Hole

HOLE2 *H-TC197BC256D106P2
HOLE6 *O-KL2-1
HOLE12 *O-KL2-2

HDD PAD

EC QV08

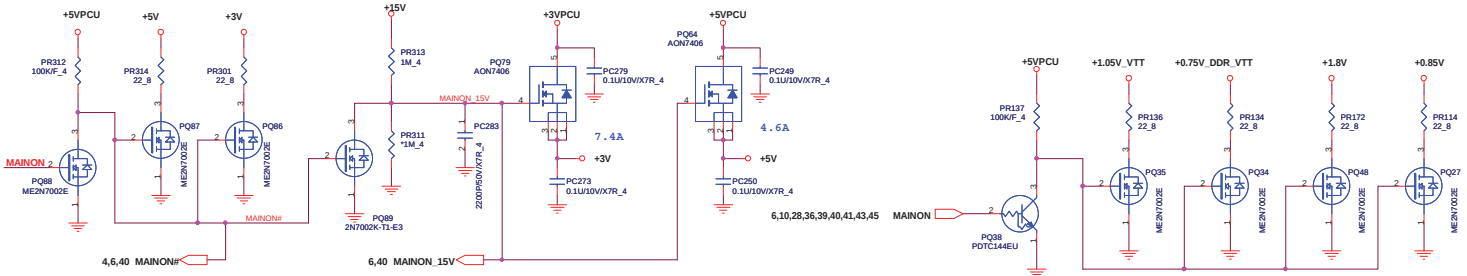
HOLE10 *H-O158X355D158X355N

PROJECT : KL2D
Quanta Computer Inc.

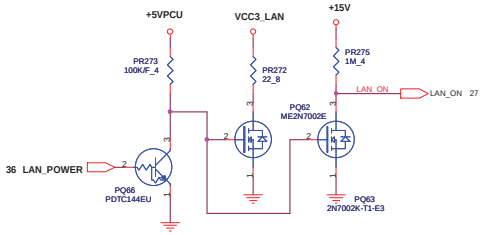
Size	Document Number	Rev
Custom	HOLD & SKEW	1A

Date: Saturday, July 24, 2010 Sheet 37 of 47

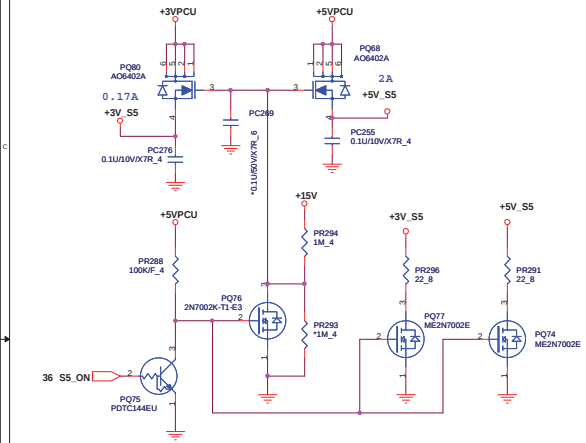
+3V, +5V

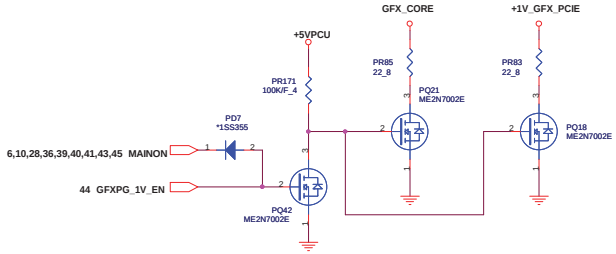


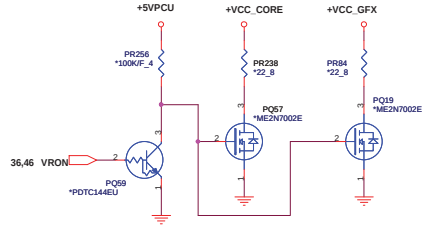
LANVCC



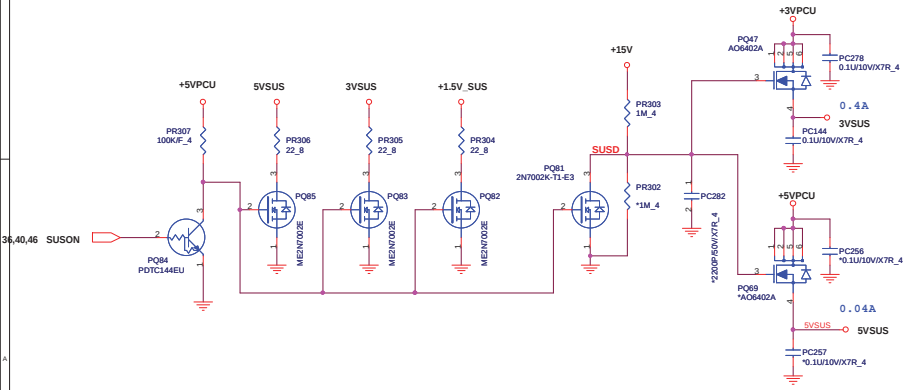
3V_S5, 5V_S5

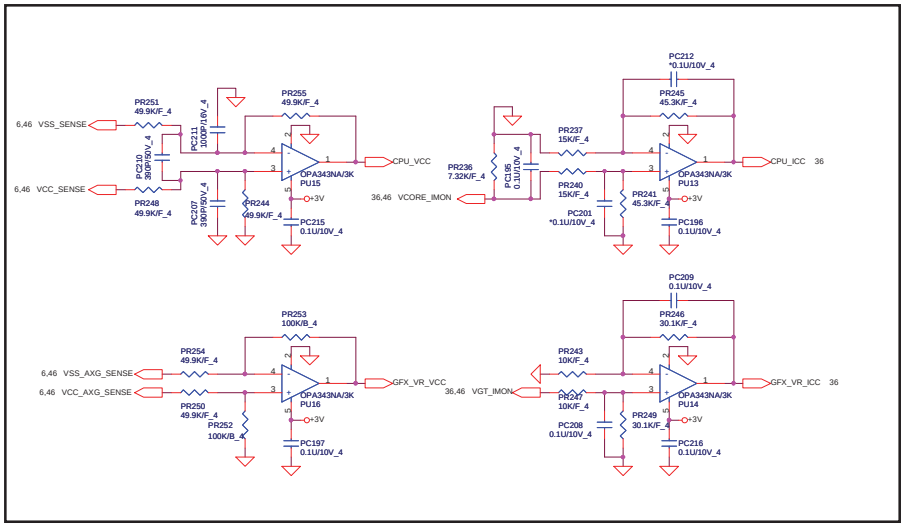






3VSUS, 5VSUS



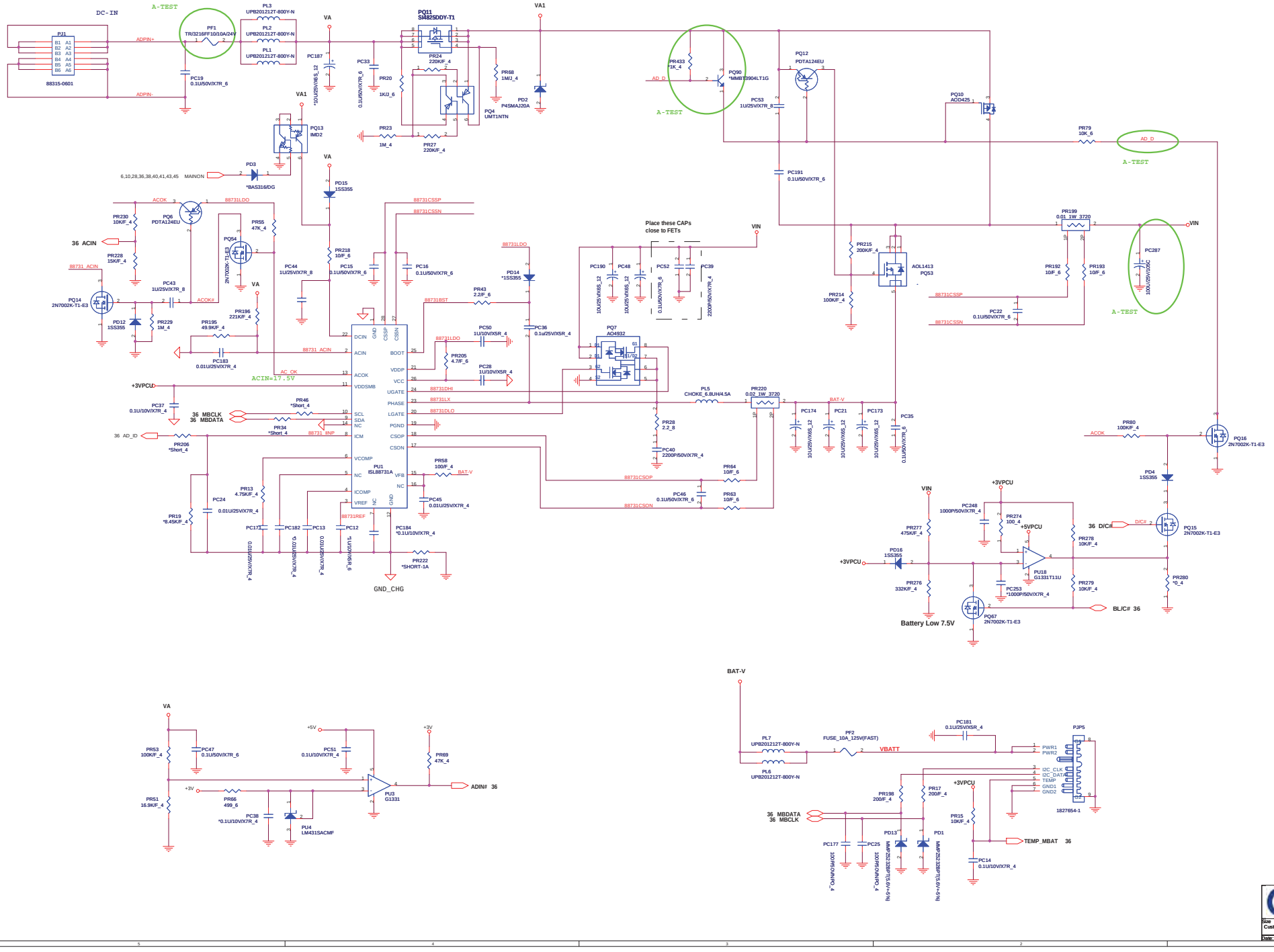


PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

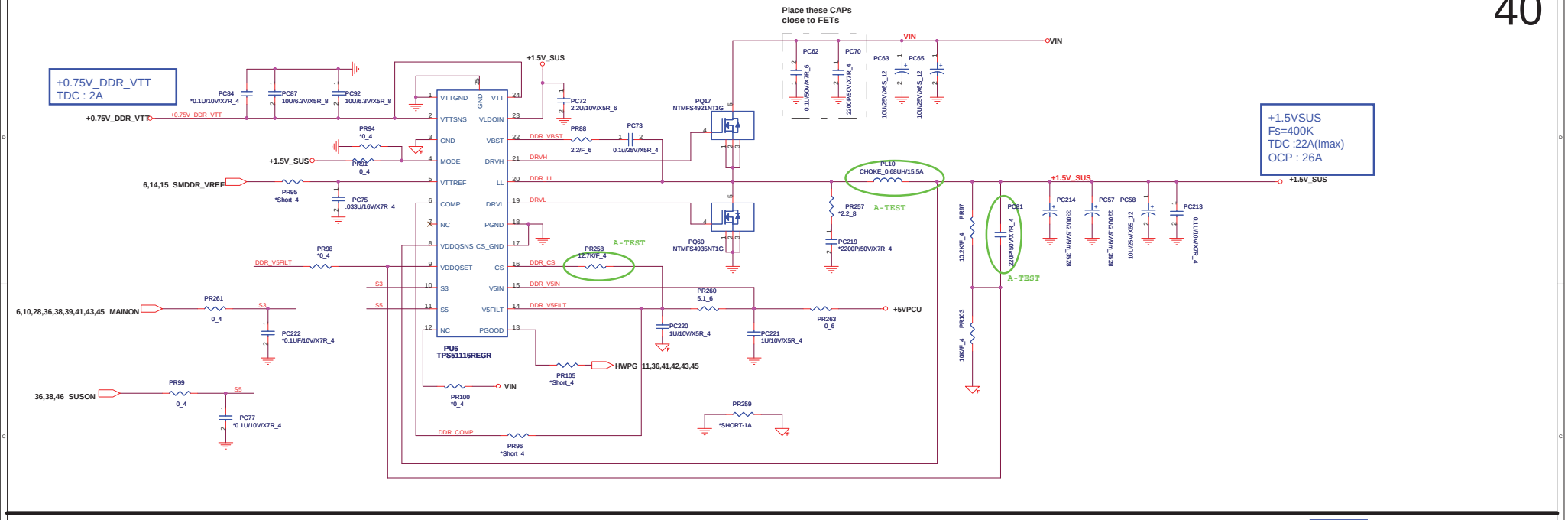
Date: Saturday, July 24, 2010 Sheet 38 of 47

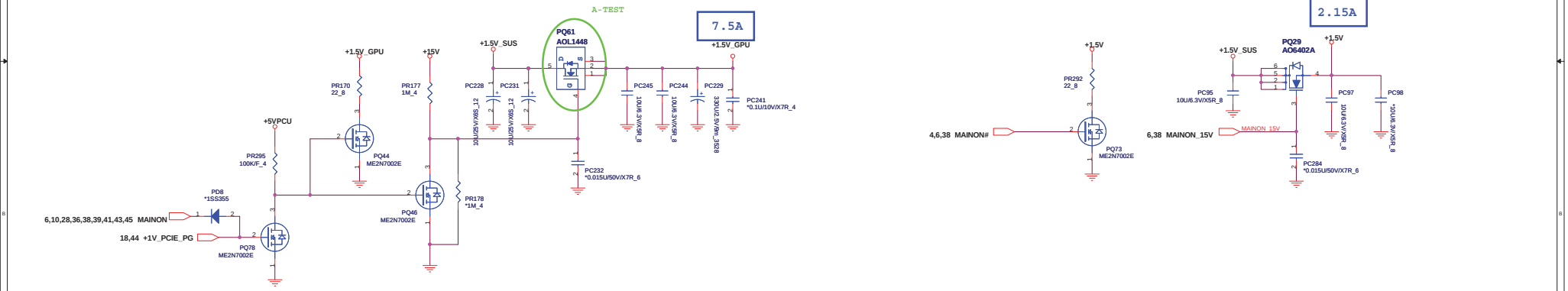


PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL88731A)	1A

Date: Saturday, July 24, 2010 Sheet 39 of 47

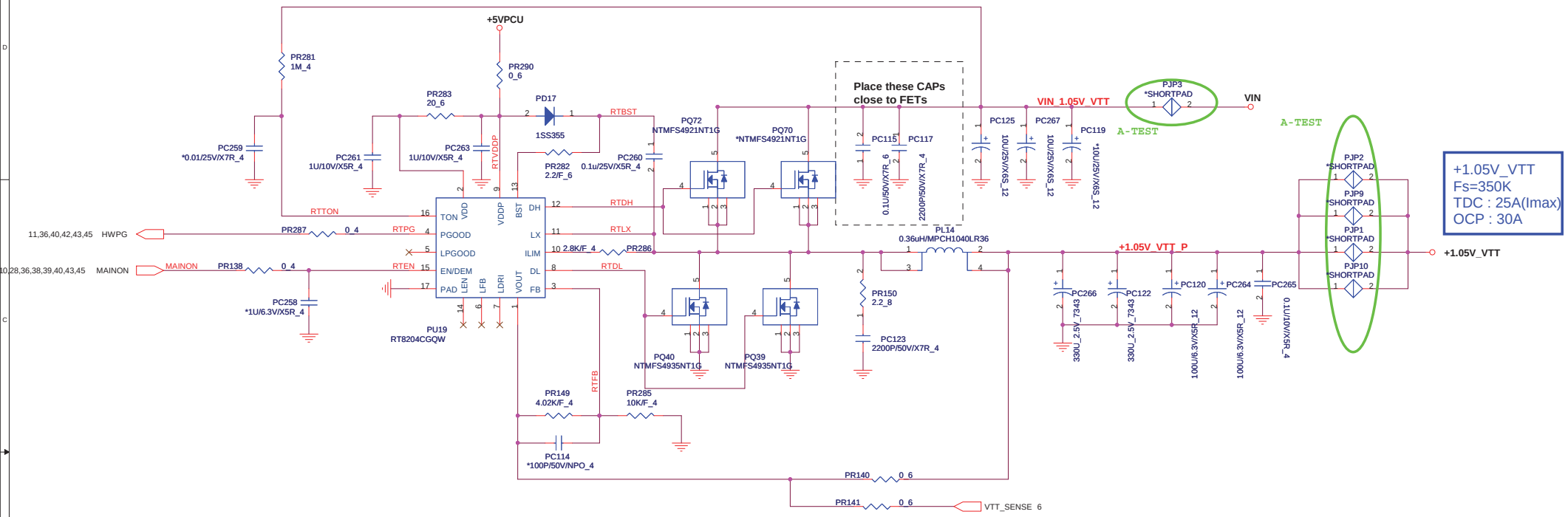




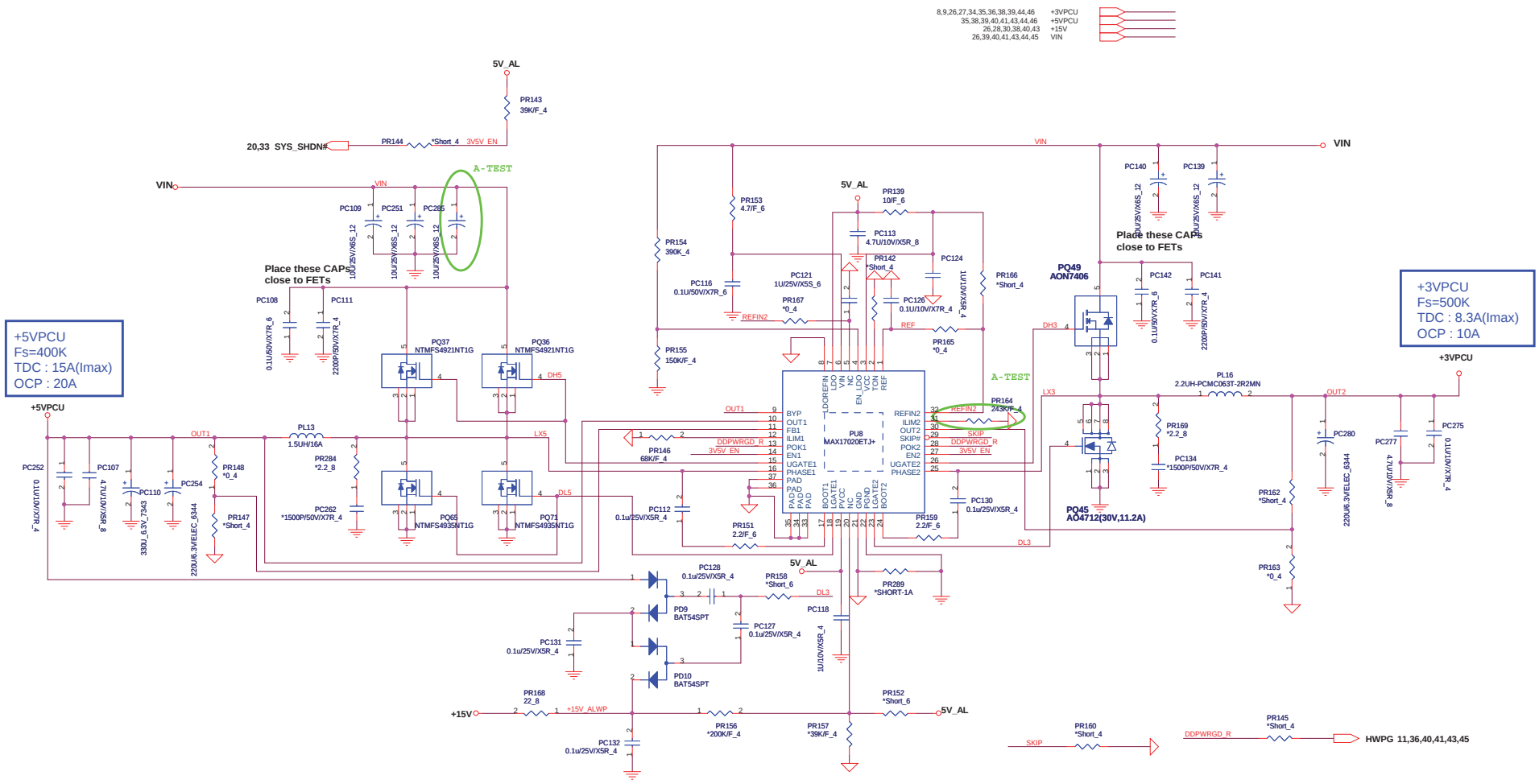
For S3 Power Saving

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V (TPS51116REGR)	1A
Date: Saturday, July 24, 2010	Sheet 40 of 47	



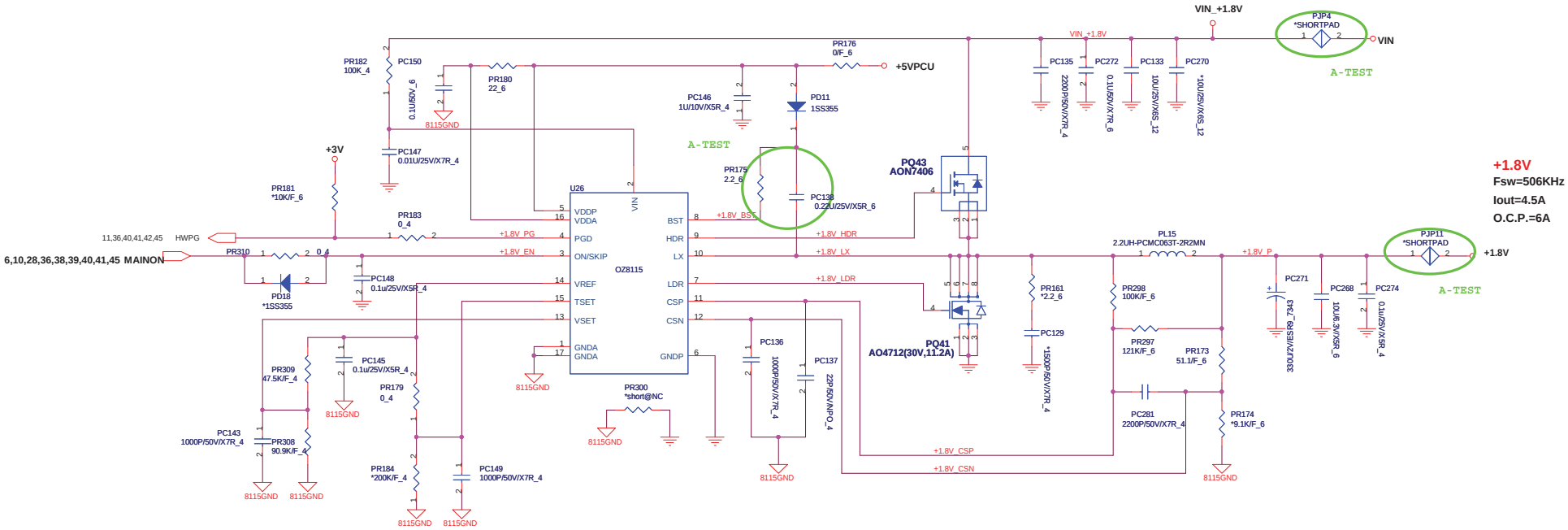
PROJECT : KL2D		
Quanta Computer Inc.		
Size: Custom	Document Number: 1.05V_VTT (RT8204)	Rev: 1A
Date: Saturday, July 24, 2010	Sheet 41 of 47	

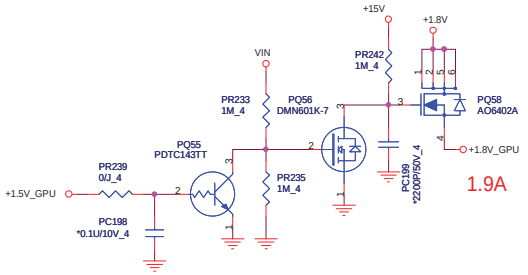


PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
C	3V/5V (MAX17020ETJ+)	1A

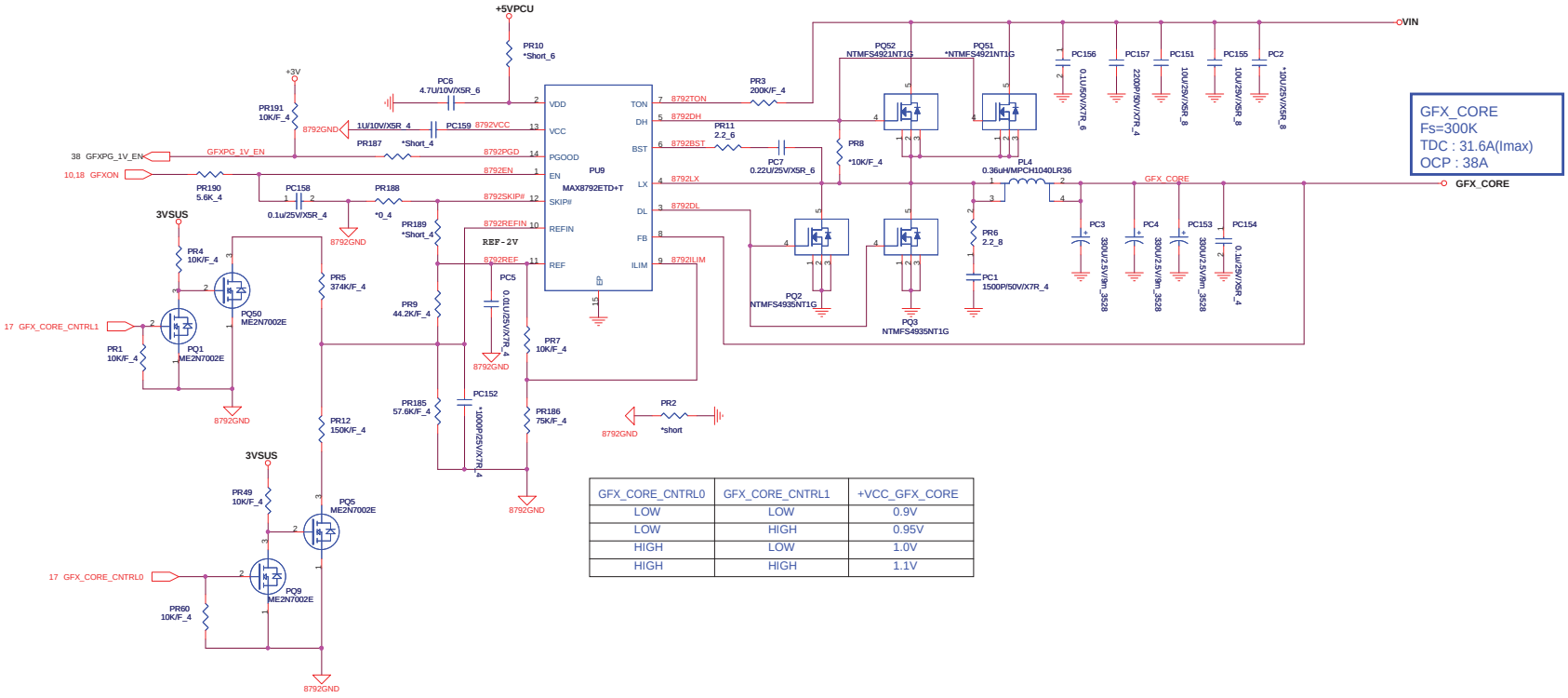
Date: Saturday, July 24, 2010 Sheet 42 of 47



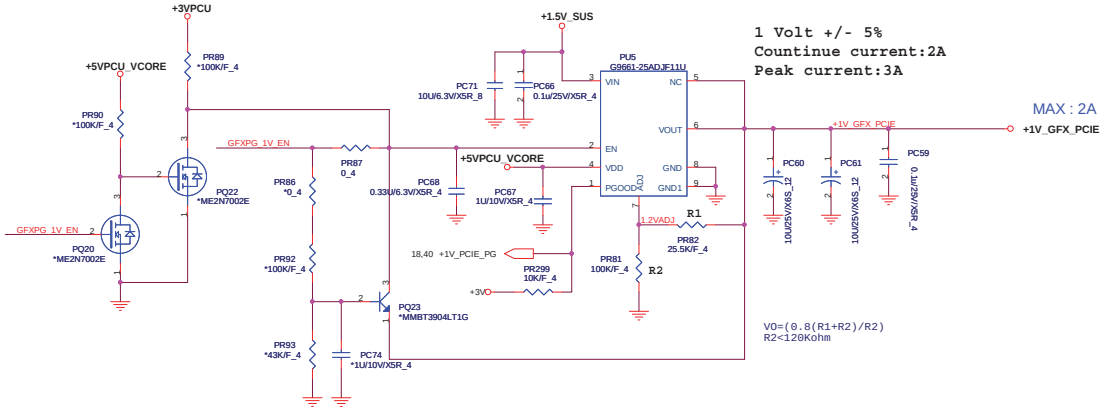


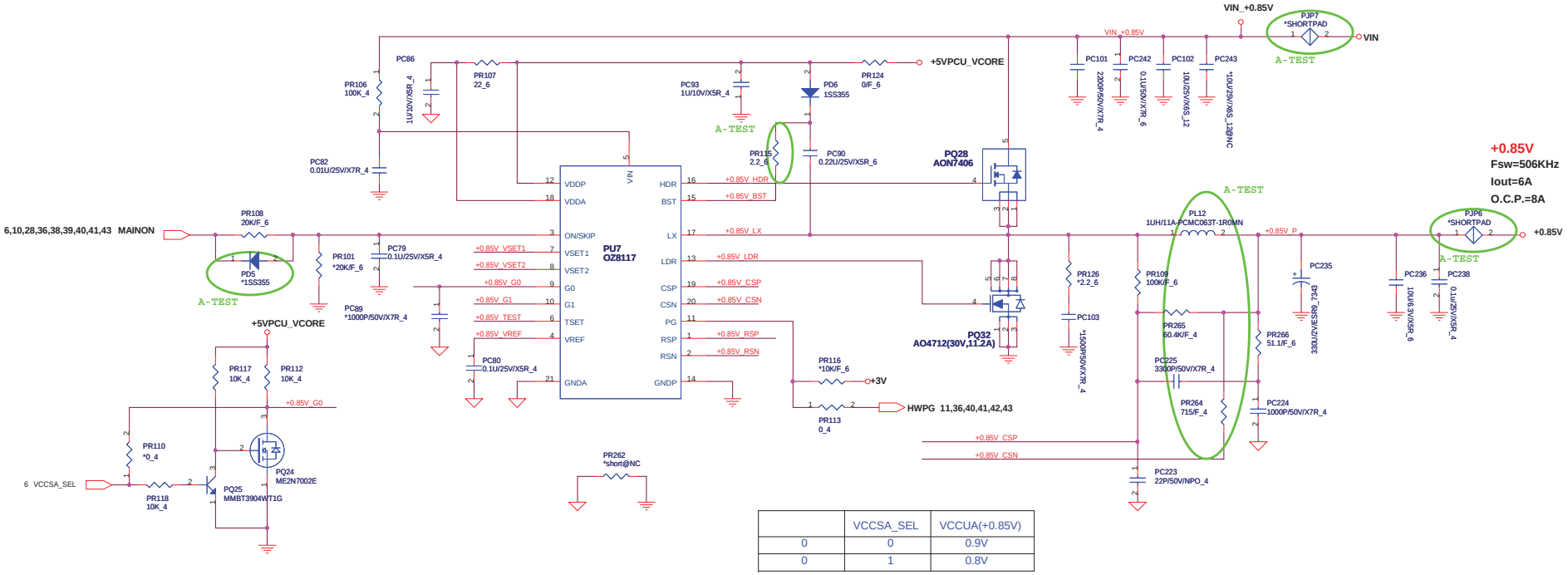
PROJECT : KL2D
Quanta Computer Inc.

Size: Custom	Document Number		Rev: A
Date: Saturday, July 24, 2010	Sheet 43 of 47		

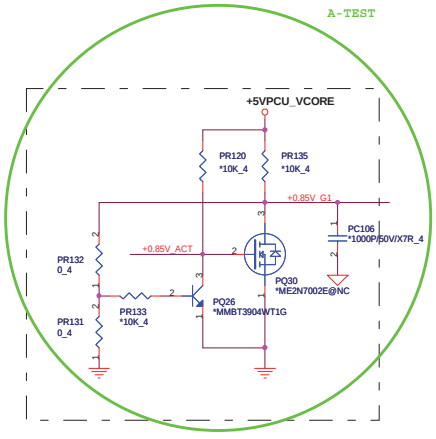


GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	0.95V
HIGH	LOW	1.0V
HIGH	HIGH	1.1V

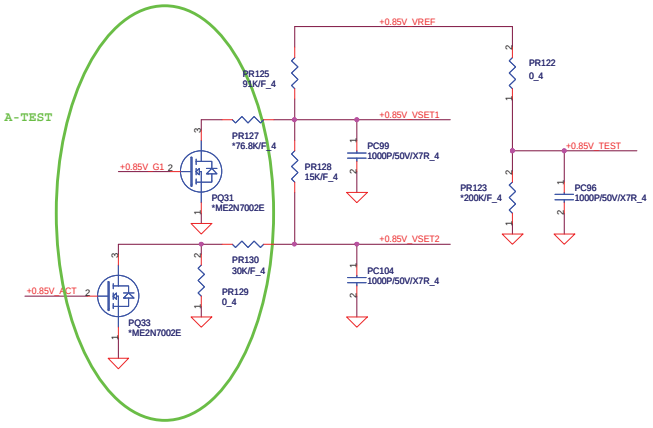


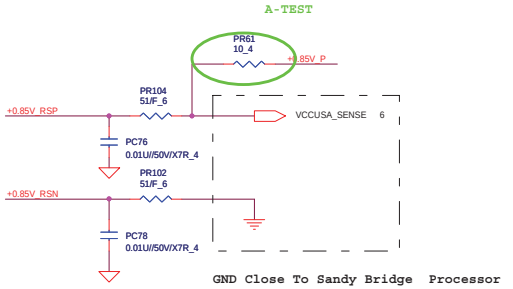


	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V



For Sandy Bridge And IV Bridge VID Select





GND Close To Sandy Bridge Processor (POWER) Side

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<Project Name>

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	+0.85V (uP6112)	1A

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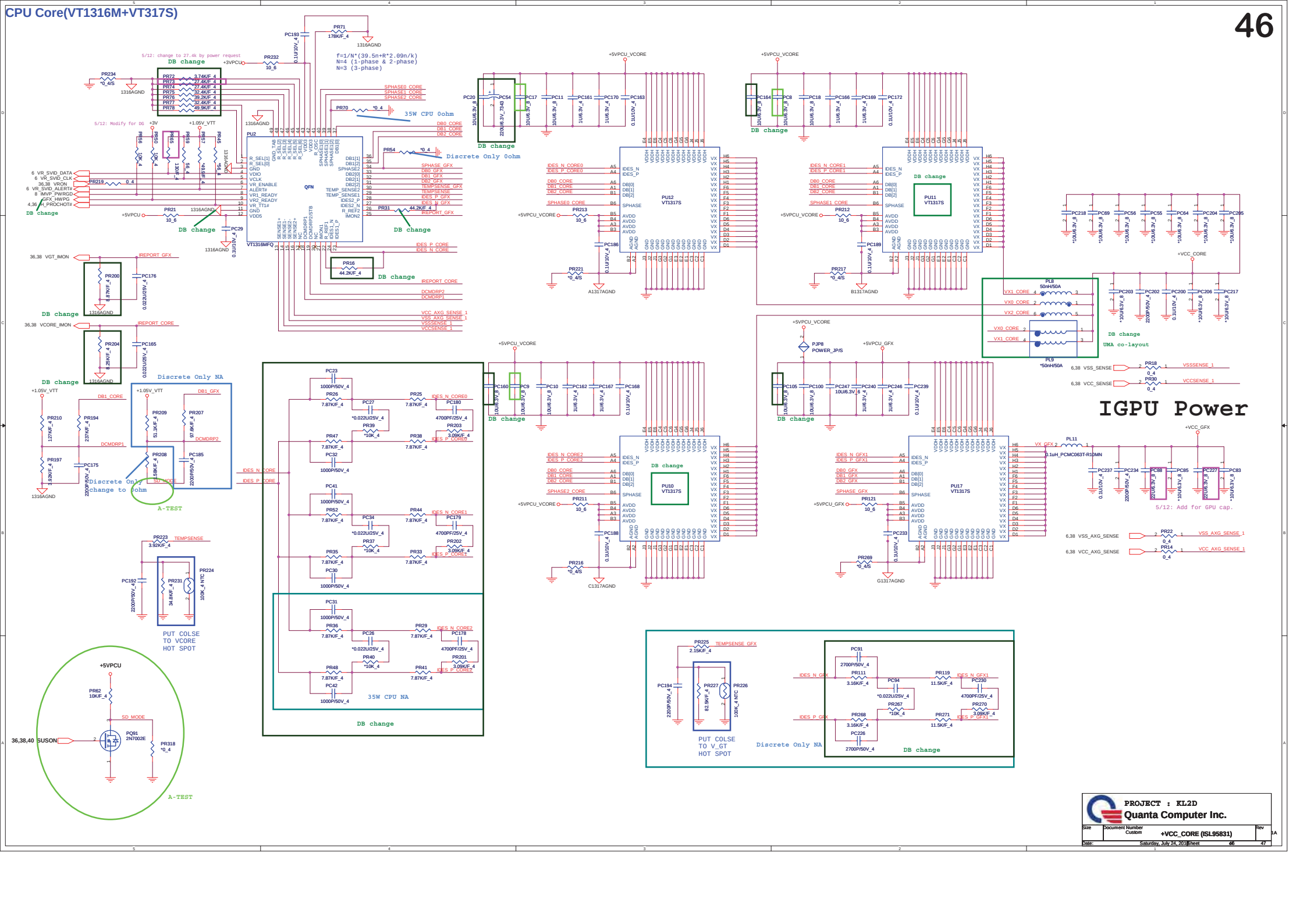
5/12: change to 27.4k by power request
DB change
f=1/N*(39.5n+R*2.09n/k)
N=4 (1-phase & 2-phase)
N=3 (3-phase)
35W CPU 0ohm
Discrete Only 0ohm
5/12: Modify for DG
DB change
Discrete Only NA
change to 0ohm
A-TEST
PUT COLSE TO VCORE HOT SPOT
35W CPU NA
PUT COLSE TO V_GT HOT SPOT
Discrete Only NA
UMA co-layout
5/12: Add for GPU cap.
IGPU Power
PROJECT : KL2D
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+VCC_CORE (ISL95831)
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EC #	Page	Description	Part Affected