Blue Moutain KIWB1/B2

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:0.1

Security Classification	Compal Secret Data		
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Compal confidential
File Name :

ZZZ1
15.6W_PCB_LA4601P

POWER BD
Power on X1
LED X1 (G)
:POWER
NOVO X1

Slide Bar LED X 10 (B)
USER-DEFINED (W)
DOLBY (W)
LED X 3
WIRELESS LED (G)
BLUETOOTH LED (G)
3G LED (G)
HDD LED (G)

RIGHT BD
VOLUME UP X1
VOLUME DOWN X1
MUTE X1
MUTE LED X1(G)

USB_Board
USB CONN X 2
TV CONN X1

POWER ON (G)
BATTERY CHARG(G/A)
WIRELESS SWITCH (G)
ON/OFF

VRAM 32*32 GDDR3*4 page20
NVidia NB9M
NVidia NB9P page16~24

PCI-E X16

Mobile Penryn
uFCPGA-478 CPU
page5,6,7

Clock Gen.
SLG8SP556VTR
ICS9LPRS387AKLFT page25

H_A#(3..35)
H_D#(0..63)
FSB
667/800/1066MHz

HDMI CONN page26

PS8101T page26

PCI-E

Intel Cantiga GMCH
PCBGA 1329
page 8,9,10,11,12,13

DDR3-800(1.5V)
DDR3-1067(1.5V)
Dual Channel

Double check ME
DDR3-SO-DIMM X2
BANK 0, 1, 2, 3 page 14,15
UP TO 8G

CRT cable page28

LVDS I/F

LVDS Connector page27

SPK amplifier page36
2Channel Speaker page37
WOOFER amplifier page37
1Channel Speaker page37

DMI
C-Line

PCI Express Mini card Slot 1 page31
PCI Express Mini card Slot 2 page31
PCI Express Mini card Slot 3 page31

6*PCI-E BUS

New Card page31

None
PCI BUS
3.3V / 33 MHz

Intel ICH9-M
mBGA-676
page27,28,29,30

AZALIA
12*USB2.0
4*SATA serial

Audio Codec
Realtek ALC272
page36

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CMOS Camera page41
BlueTooth CONN page41
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MS/MS
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LPC BUS

EC
ENE KB926D
page38

SIM Card page31

BCM5906/BCM5784M
10/100/1G LAN
page32

RJ45 CONN page33

Int.KBD page39
Touch Pad page39
BIOS page40

REPEATER page35
ESATA HDD AND USB CONN page35
SATA HDD CONN page35
SATA ODD CONN page35

HDD/ODD,SCL & T/L LED on MB
CAPS and NUM on KBD

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Title: *MB Block Diagram*

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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Title: **MB Notes List**

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VGA and DDR2 Voltage Rails (NB9M-GS)

State \ power plane			+1.8V	+3VS +VGA_CORE +1.1VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

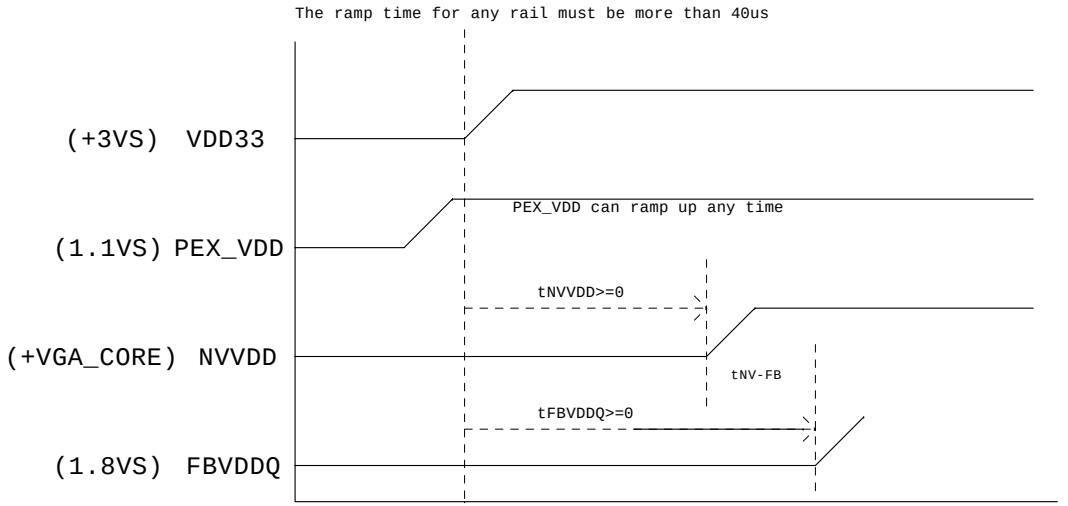
GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	Available
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2 or MEM VID
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	FAN control and/or Thermal Alert (PWM)
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP link E
GPIO16	IN	-	Dongle DVI Mode control for Primary Displayport
GPIO17	IN	-	Dongle HDMI Mode control for Primary Displayport
GPIO18	IN	-	Dongle DVI Mode control for Secondary Displayport
GPIO19	IN	-	Dongle HDMI Mode control for Secondary Displayport
GPIO20	IN	-	Hot plug detect for IFP link D
GPIO21	IN	-	Hot plug detect for IFP link E
GPIO22	IN	-	SLI swap ready signal
GPIO23	N/A	N/A	Available

VRAM POWER SQUENCE
GDDR3 FOR 4 UNIT = 5.4A

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9P-GS		NB9P-GE2	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	20.65A	16.96A	18.47A	16.06A
FB_DLLAVDD	1.1	10mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	80mA			
IFPD_IOVDD	1.1	80mA			
IFPE_IOVDD	1.1	160mA			
IFPF_IOVDD	1.1	160mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	90mA			
PLLVDD	1.1	45mA			
SP_PLLVDD	1.1	45mA			
VID_PLLVDD	1.1	45mA			
TOTAL	1.1	2.3A			
FBVDD/Q	1.8	3.37A	2.02A	3.21A	2.25A
IFPA_IOVDD	1.8	95mA			
IFPB_IOVDD	1.8	95mA			
IFPAB_PLLVDD	1.8	70mA			
IFPCD_PLLVDD	1.8	25mA			
IFPEF_PLLVDD	1.8	85mA			
TOTAL	1.8	5.76A	3.69A	5.47A	3.96A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	120mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	150mA			
TOTAL	3.3	0.51A			

POWER SQUENCE



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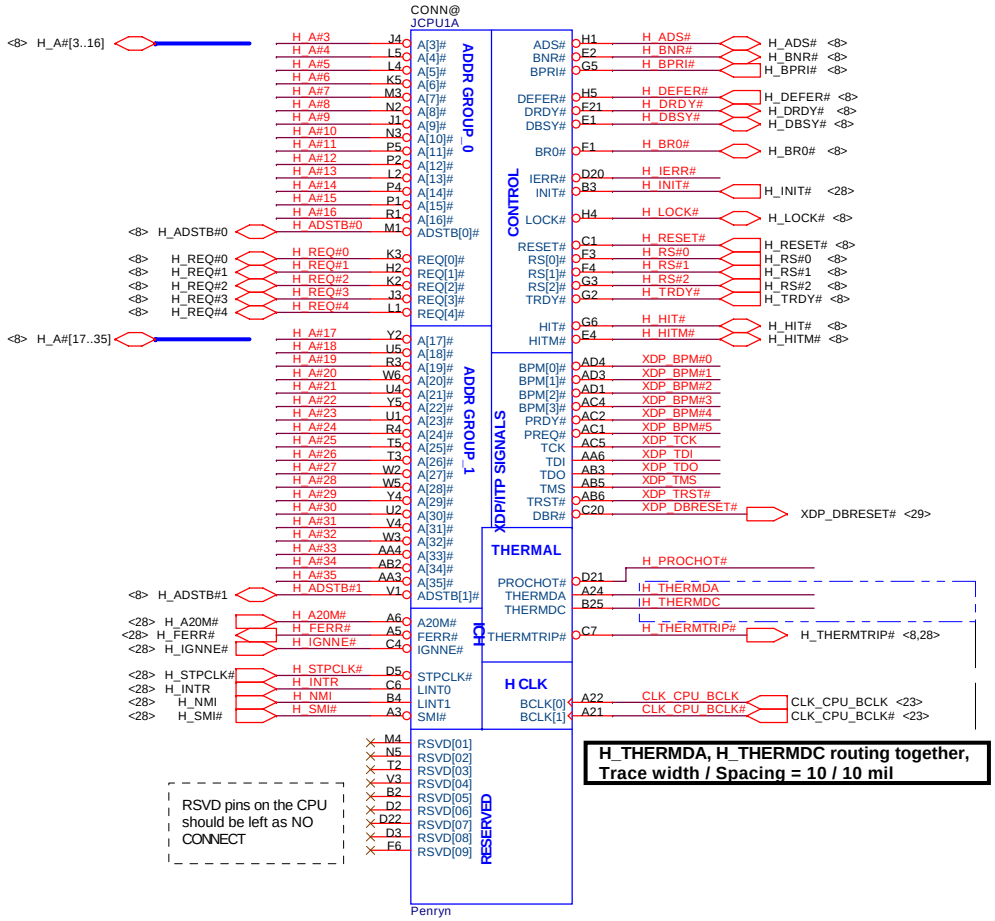
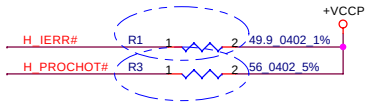
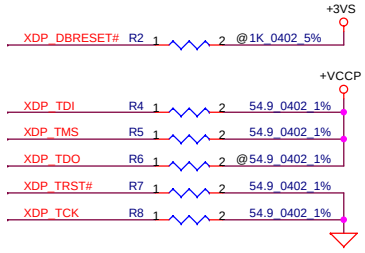


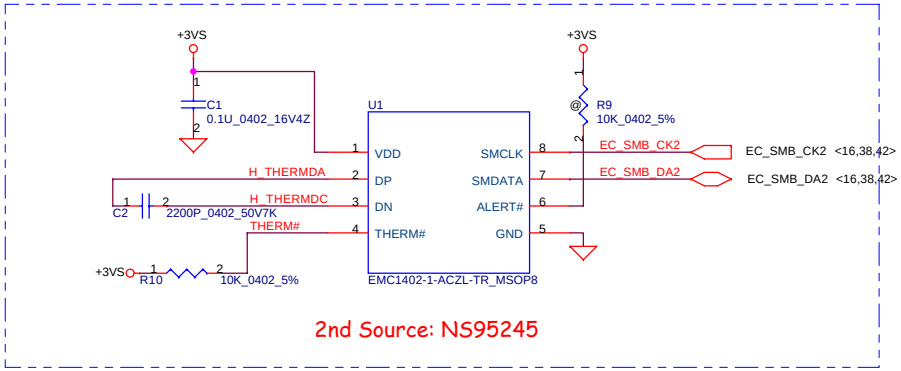
USE->56Ω,NOT USE->50Ω



USE->68Ω,NOT USE-->56Ω

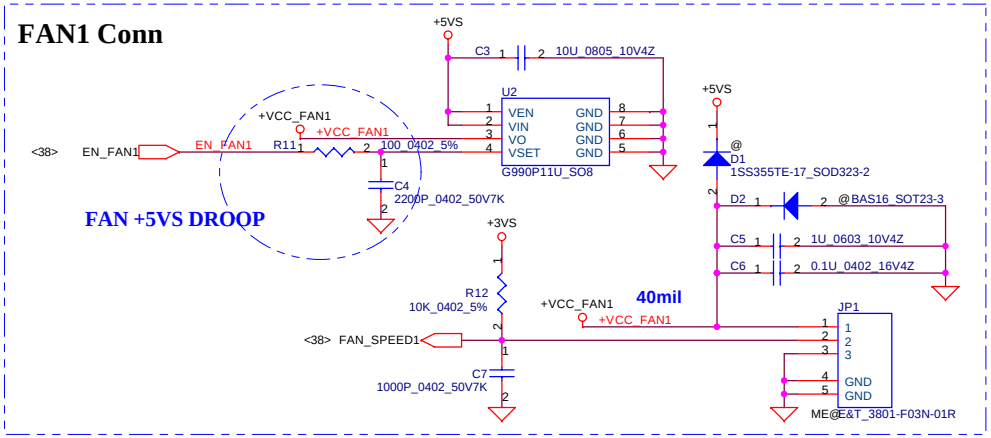
XDP Reserve





Address:100_1100

FAN1 Conn



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Title: **Penryn(1/3)**

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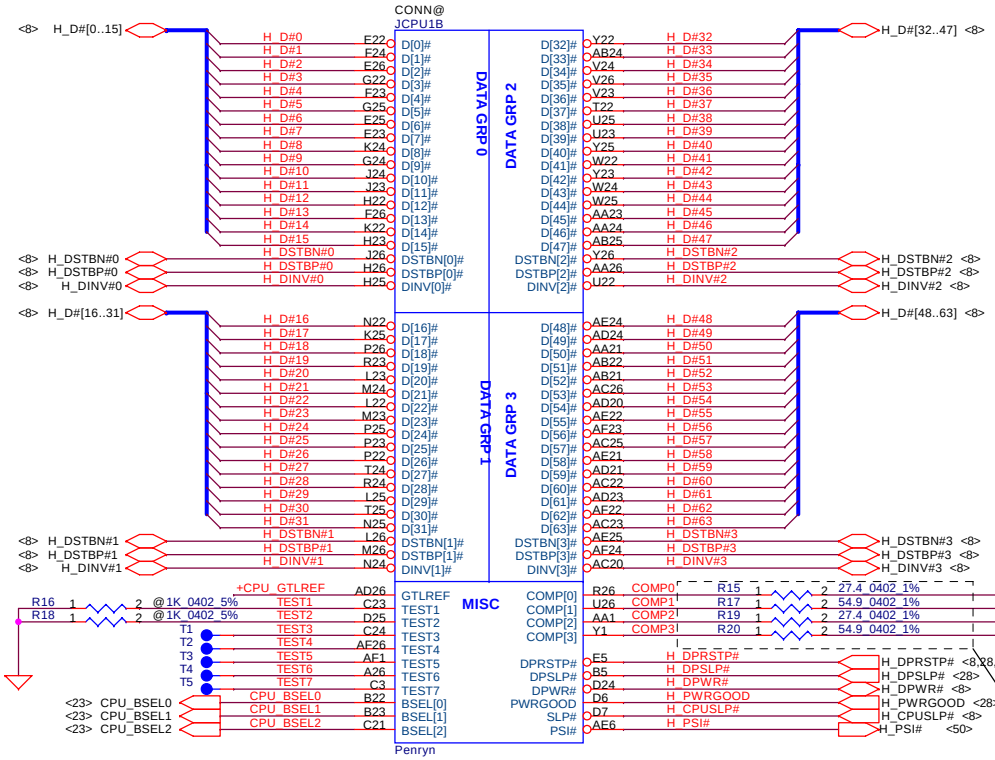
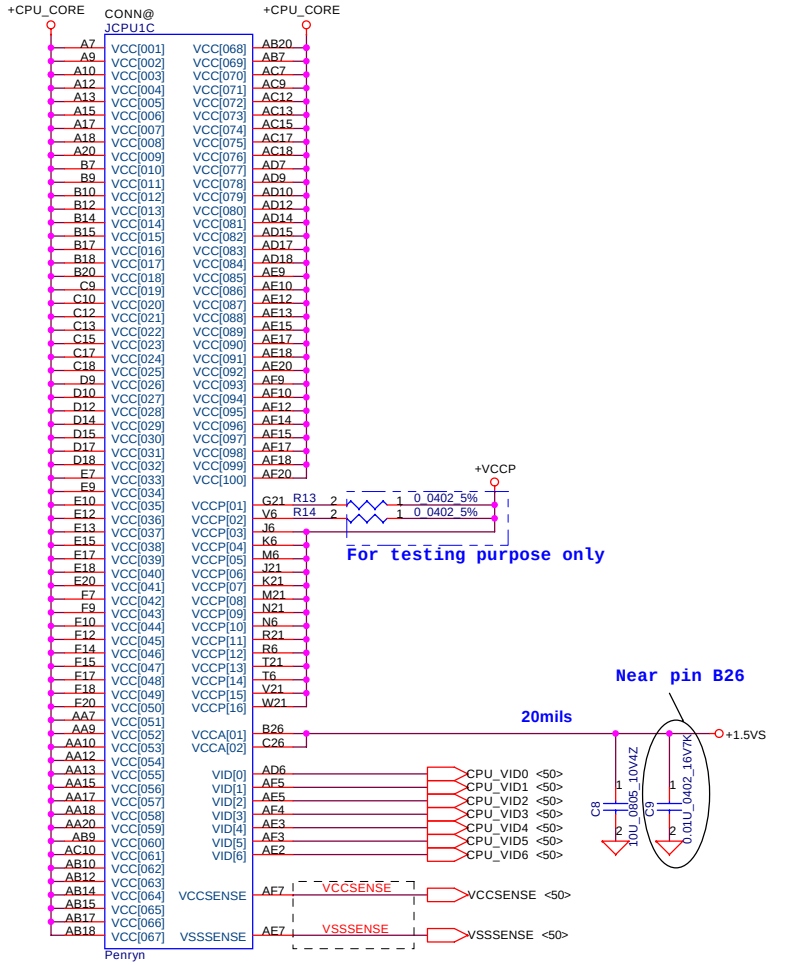
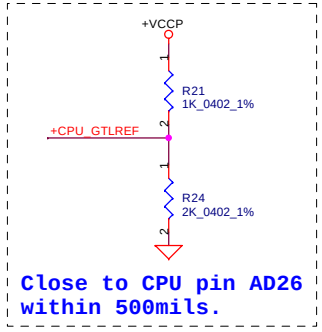




layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

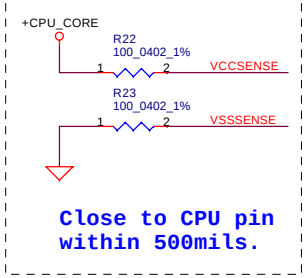


Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.
The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



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Title: **Penryn (2/3)**

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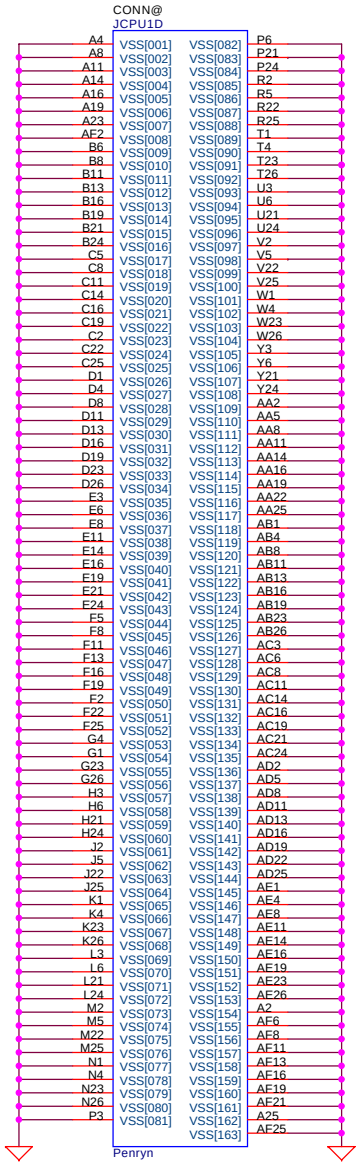
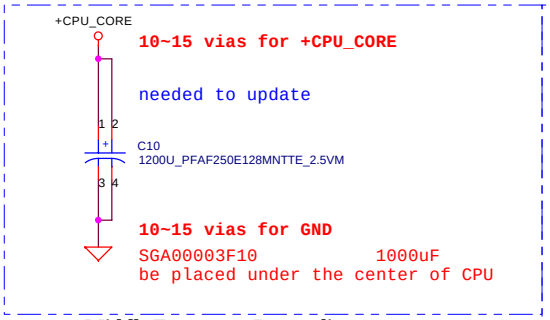
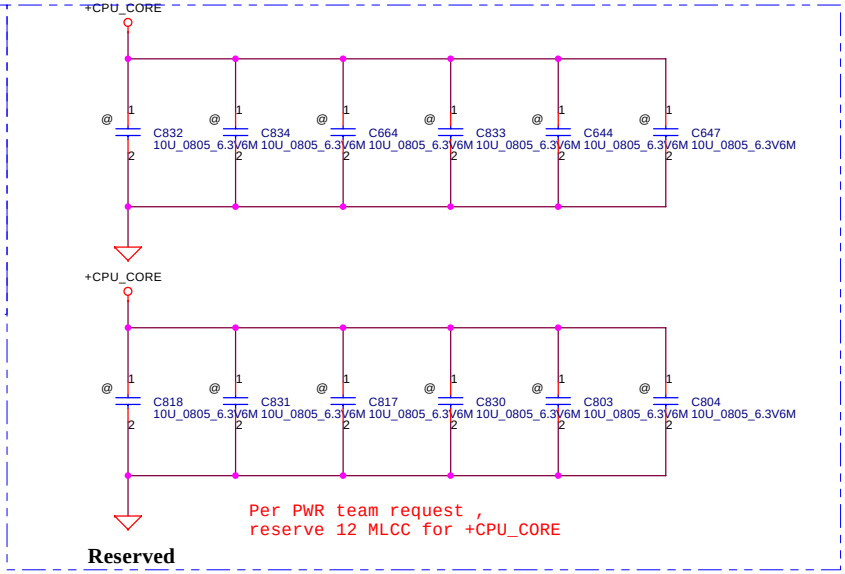
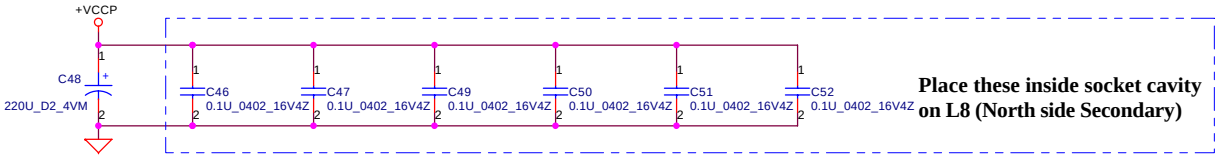




Middle Frequency Decoupling



Reserved



Place these inside socket cavity on L8 (North side Secondary)

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Title: **Penryn (3/3)**

Size	Document Number	Rev
B	KIW10/11_LA4142P	0.1

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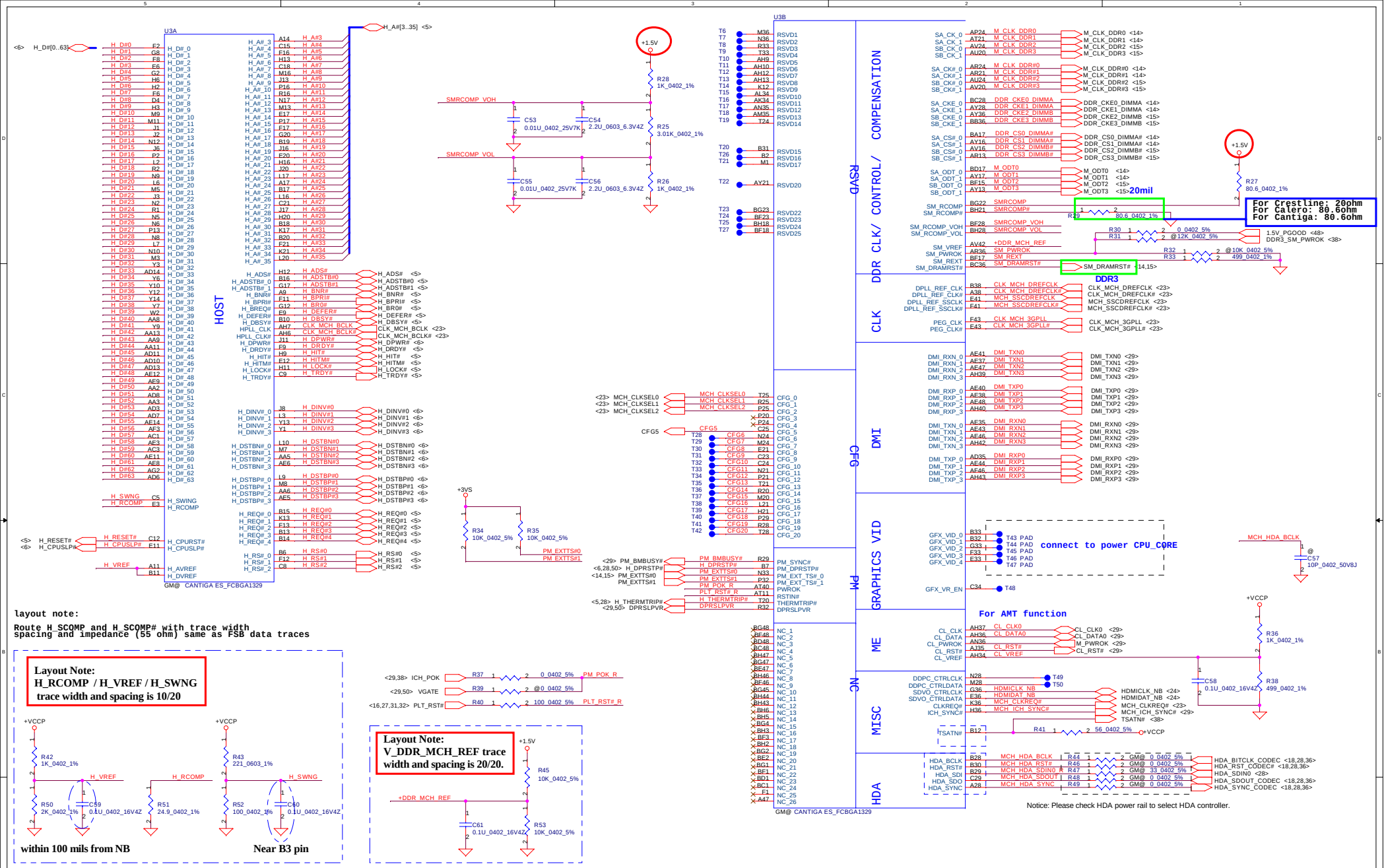

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Title	Compal Electronics, Inc.		
	Cantiga GMCH(1/6)-GTL		
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Title: **Cantiga GMCH (2/6)-DDRII**

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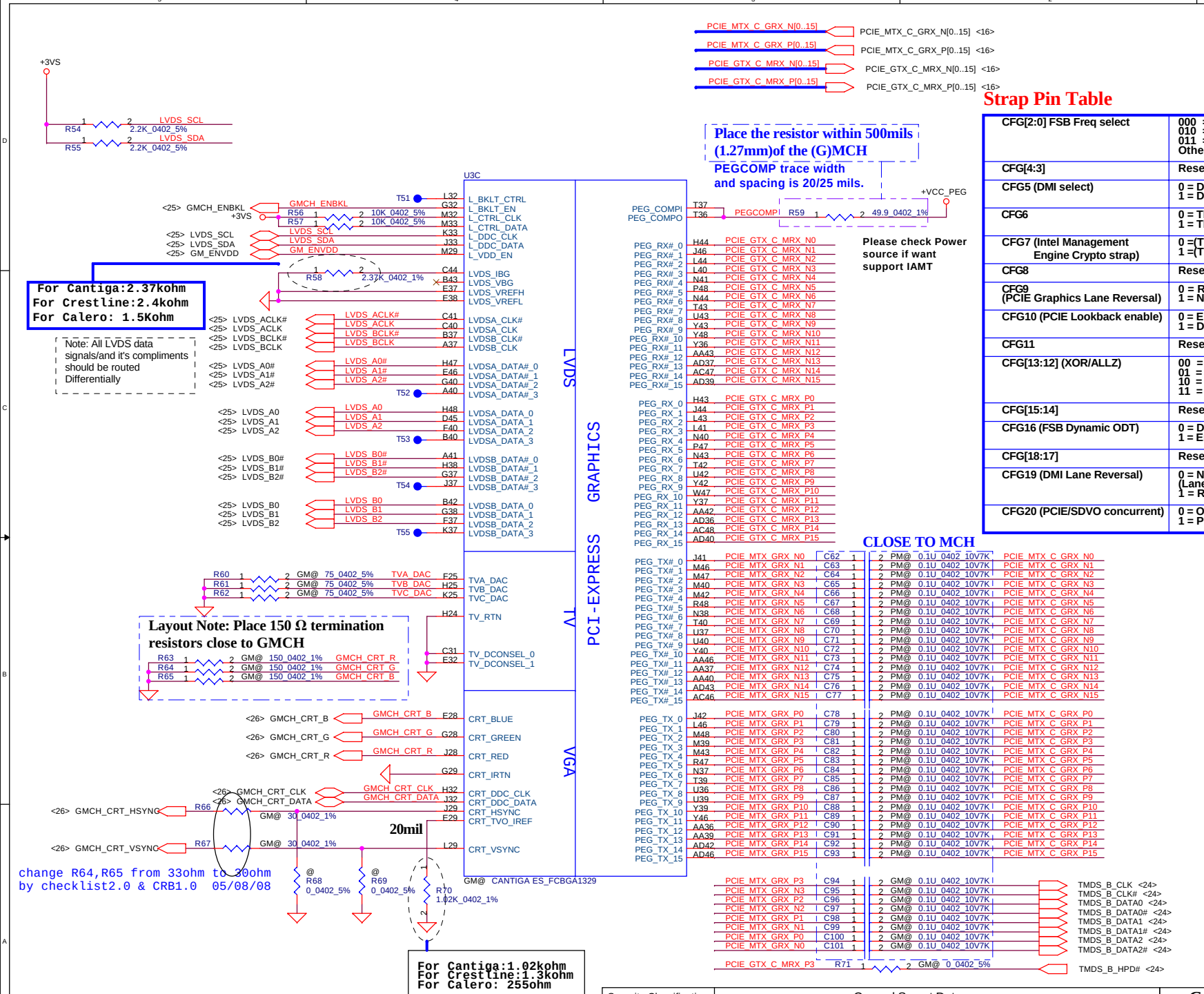

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: Cantiga(3/6)-VGA/LVDS/TV

Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

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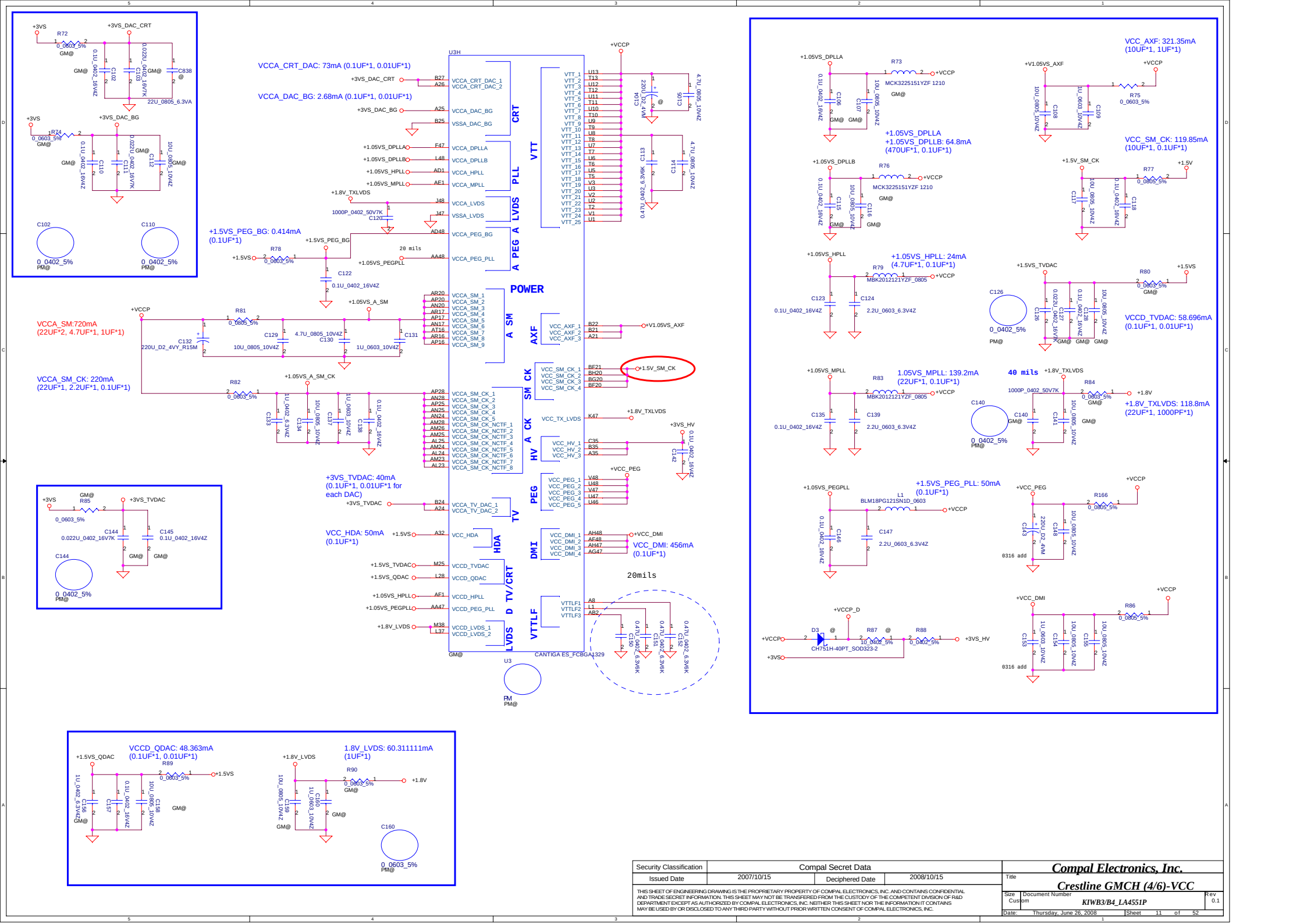
VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)
+1.5VS_PEG_BG: 0.414mA (0.1UF*1)
VCCA_SM:720mA (22UF*2, 4.7UF*1, 1UF*1)
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)
+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
VCC_HDA: 50mA (0.1UF*1)
VCC_DMI: 456mA (0.1UF*1)
20mils
VCCD_QDAC: 48.363mA (0.1UF*1, 0.01UF*1)
1.8V_LVDS: 60.311111mA (1UF*1)
VCC_AXF: 321.35mA (10UF*1, 1UF*1)
+1.05VS_DPLLA
+1.05VS_DPLLB: 64.8mA (470UF*1, 0.1UF*1)
VCC_SM_CK: 119.85mA (10UF*1, 0.1UF*1)
+1.05VS_HPLL: 24mA (4.7UF*1, 0.1UF*1)
VCCD_TVDAC: 58.696mA (0.1UF*1, 0.01UF*1)
1.05VS_MPLL: 139.2mA (22UF*1, 0.1UF*1)
40 mils
+1.8V_TXLVDS: 118.8mA (22UF*1, 1000PF*1)
+1.5VS_PEG_PLL: 50mA (0.1UF*1)
U3H
CRT
PLL
VTT
LVDS
PEG A
POWER
A SM
AXF
SM CK
A CK
HV
PEG
TV
DMI
HDA
D TV/CRT
VTTLF
LVDS
CANTIGA ES_FCBGA1329
Security Classification
Compal Secret Data
Issued Date
2007/10/15
Deciphered Date
2008/10/15
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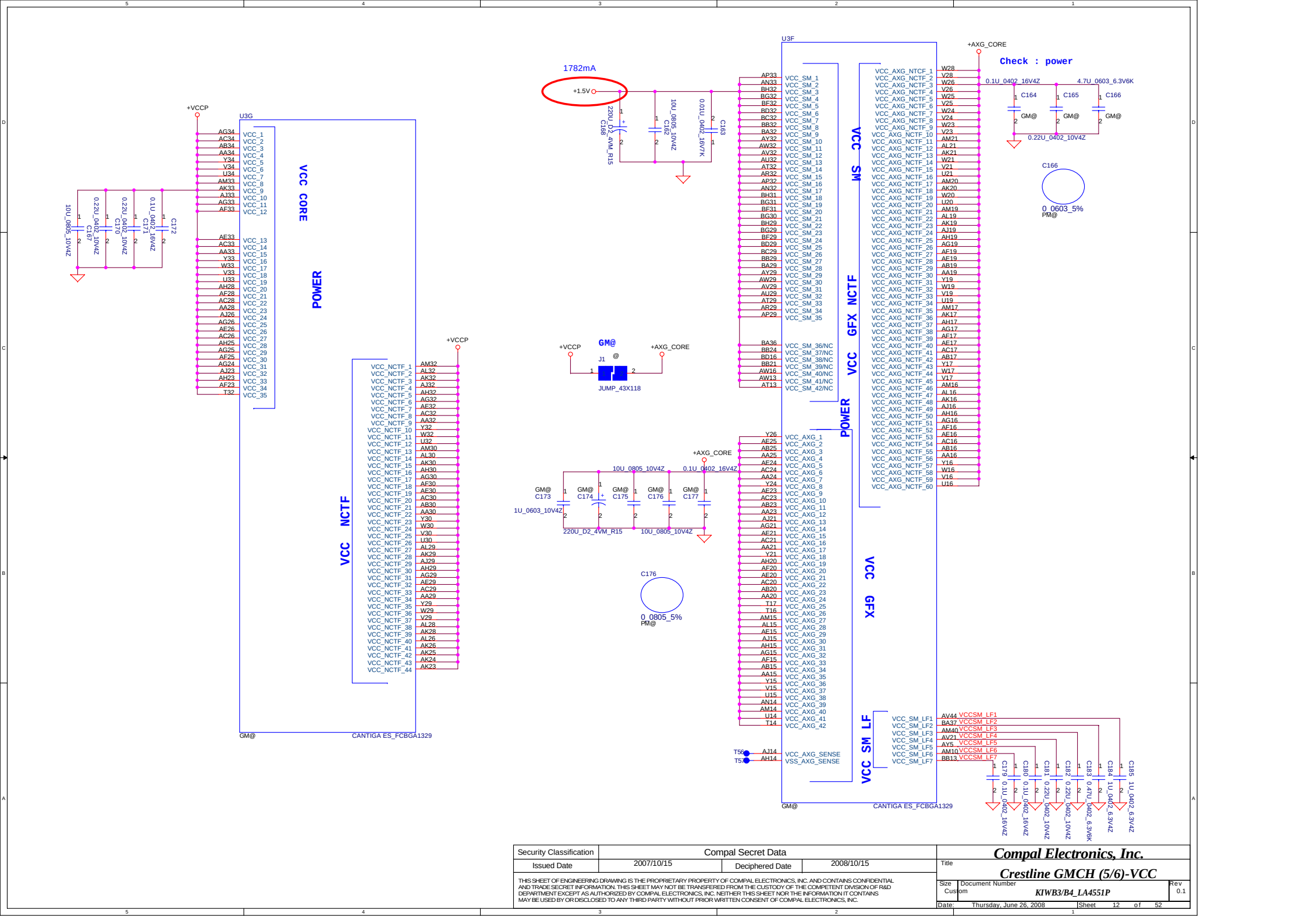
Compal Electronics, Inc.
Title
Crestline GMCH (4/6)-VCC
Size
Custom
Document Number
KIWB3/B4_LA4551P
Rev
0.1
Date:
Thursday, June 26, 2008
Sheet
11
of
52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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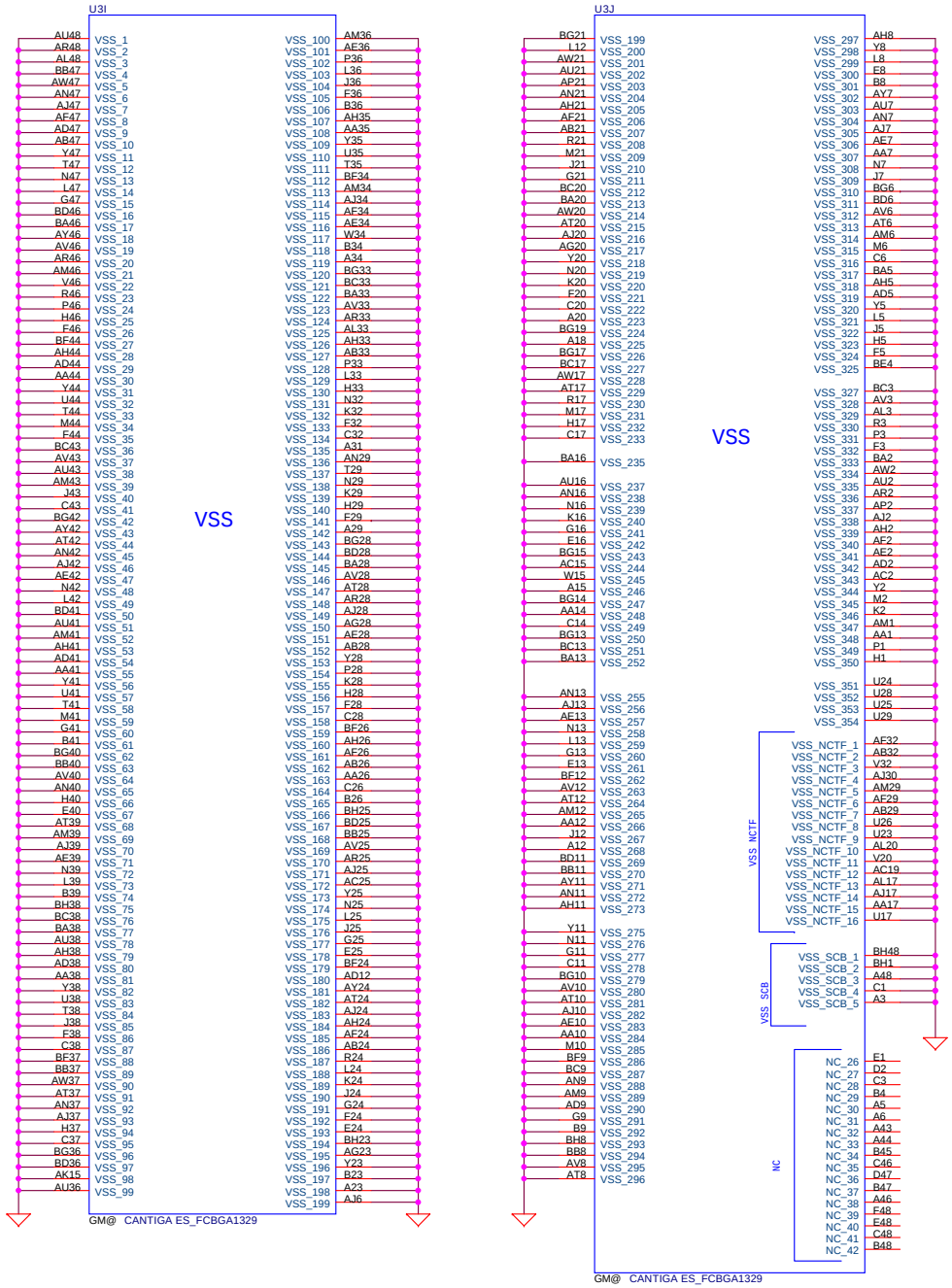
Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Thursday, June 26, 2008 | Sheet 12 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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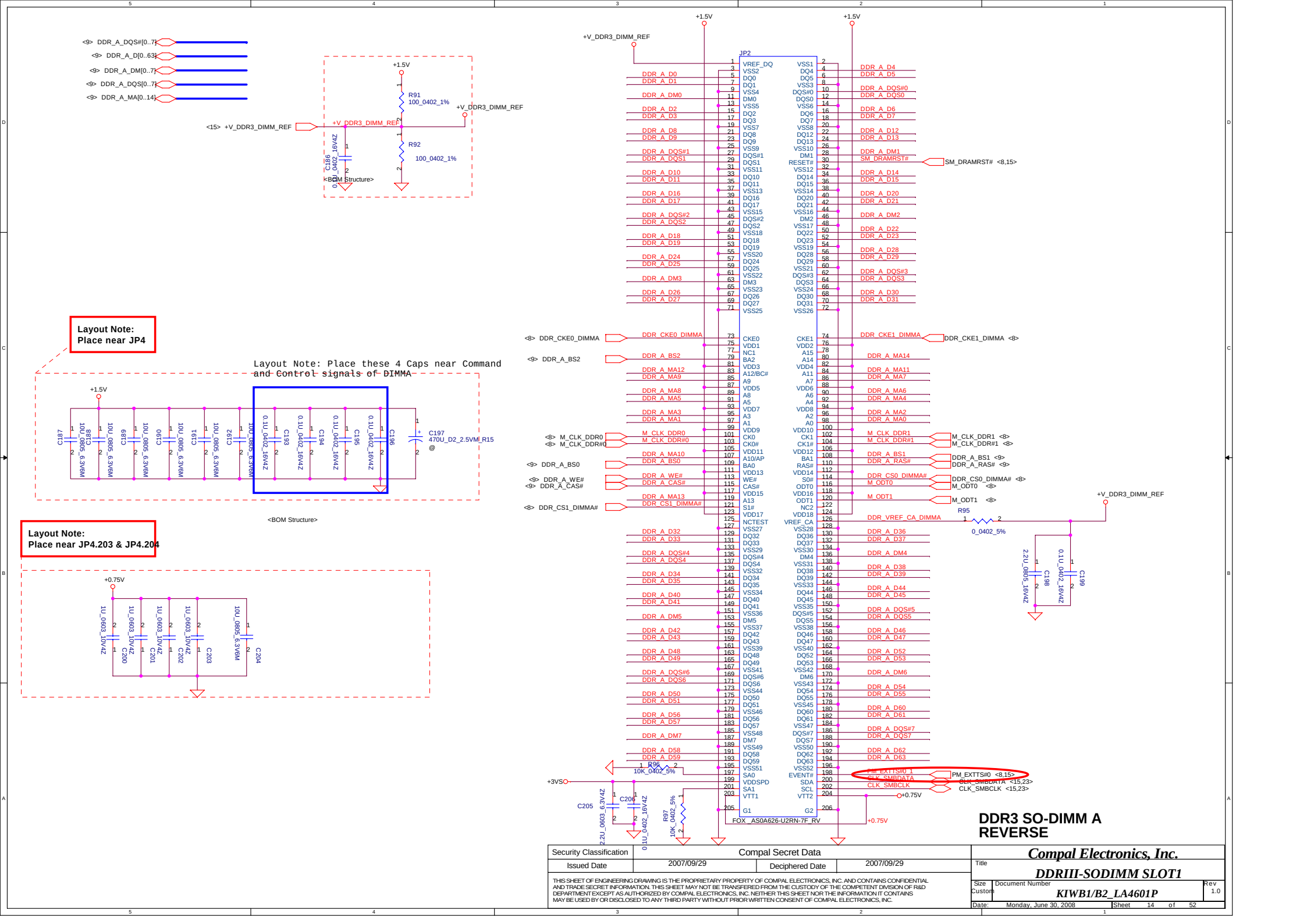
Compal Electronics, Inc.

Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
Custom	KIWB3/B4_LA4551P	0.1

Date: Thursday, June 26, 2008 Sheet 13 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

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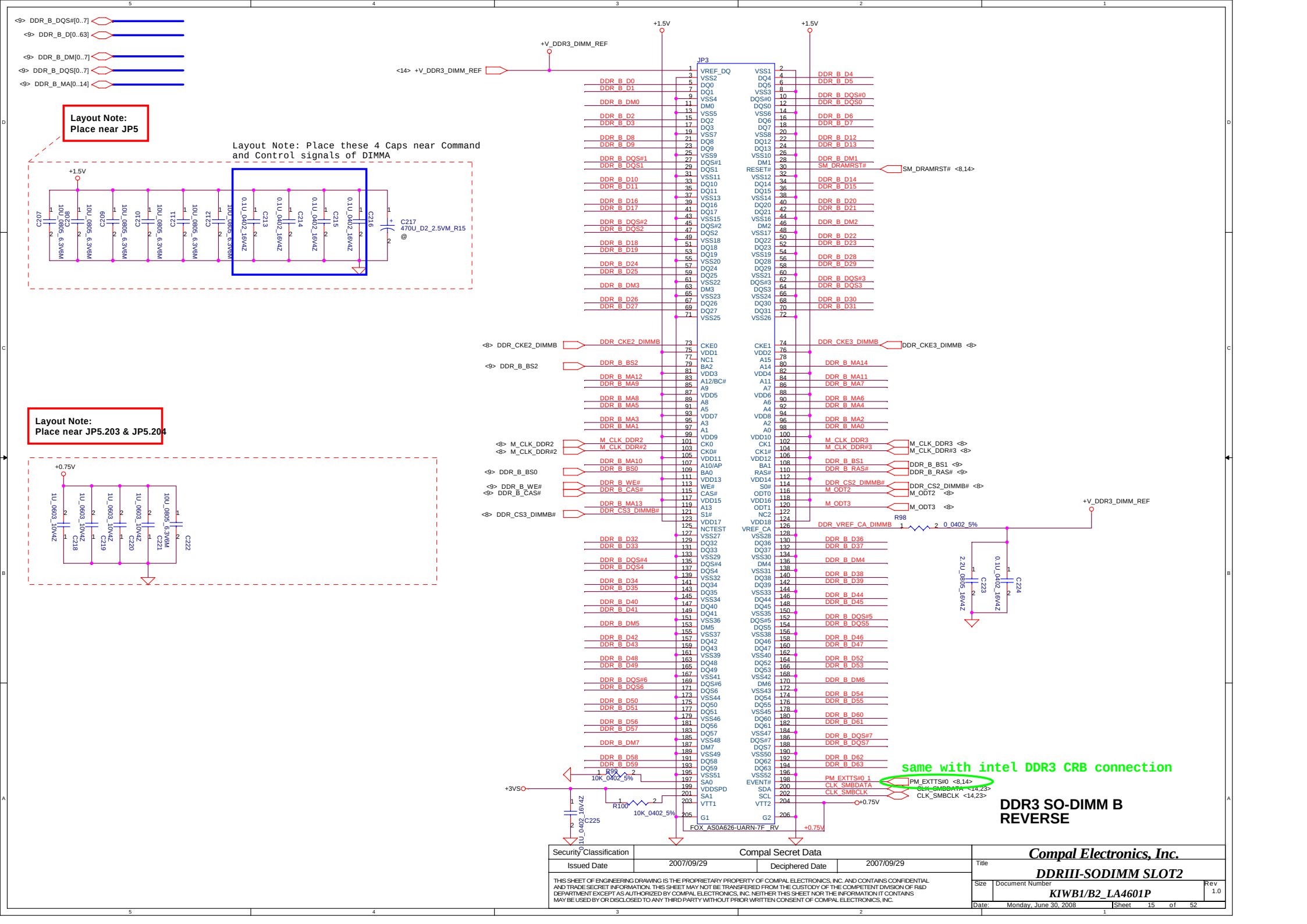
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	1.0

Date: Monday, June 30, 2008 Sheet 14 of 52


Layout Note:
Place near JP5
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
Layout Note:
Place near JP5.203 & JP5.204
JP3
FOX_AS0A626-UARN-7F_RV
same with intel DDR3 CRB connection
DDR3 SO-DIMM B
REVERSE
Compal Electronics, Inc.
DDRIII-SODIMM SLOT2
KIWB1/B2_LA4601P
Monday, June 30, 2008
Sheet 15 of 52
Security Classification
Compal Secret Data
Issued Date
2007/09/29
Deciphered Date
2007/09/29

GPIO6	GPIO5		
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10,12
1	1	1.17V	0
1	0	1.09V	8

NB9M-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
1	1	1.00V	0
0	1	0.9V	8,10,12

NB9P-GE2

for GT21x request

for GT21x request

If External Spread Spectrum not stuff then stuff resistor

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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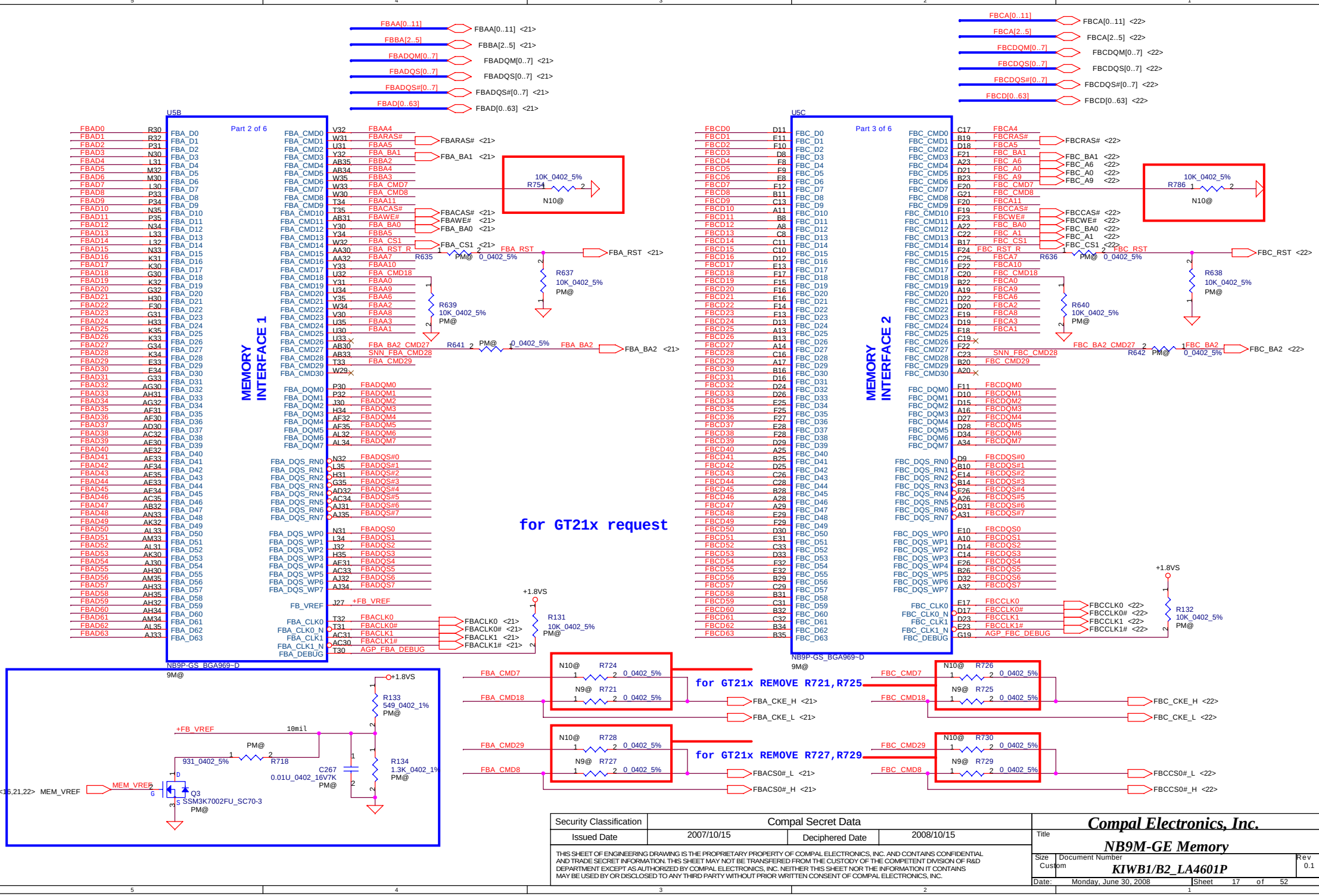
Compal Electronics,Ltd.

Title: NB9P PCIE,LVDS,GPIO,CLK

Size: Custom | Document Number: KIWB1/B2_LA4601P | Rev: 0.1

Date: Monday, June 30, 2008 | Sheet 16 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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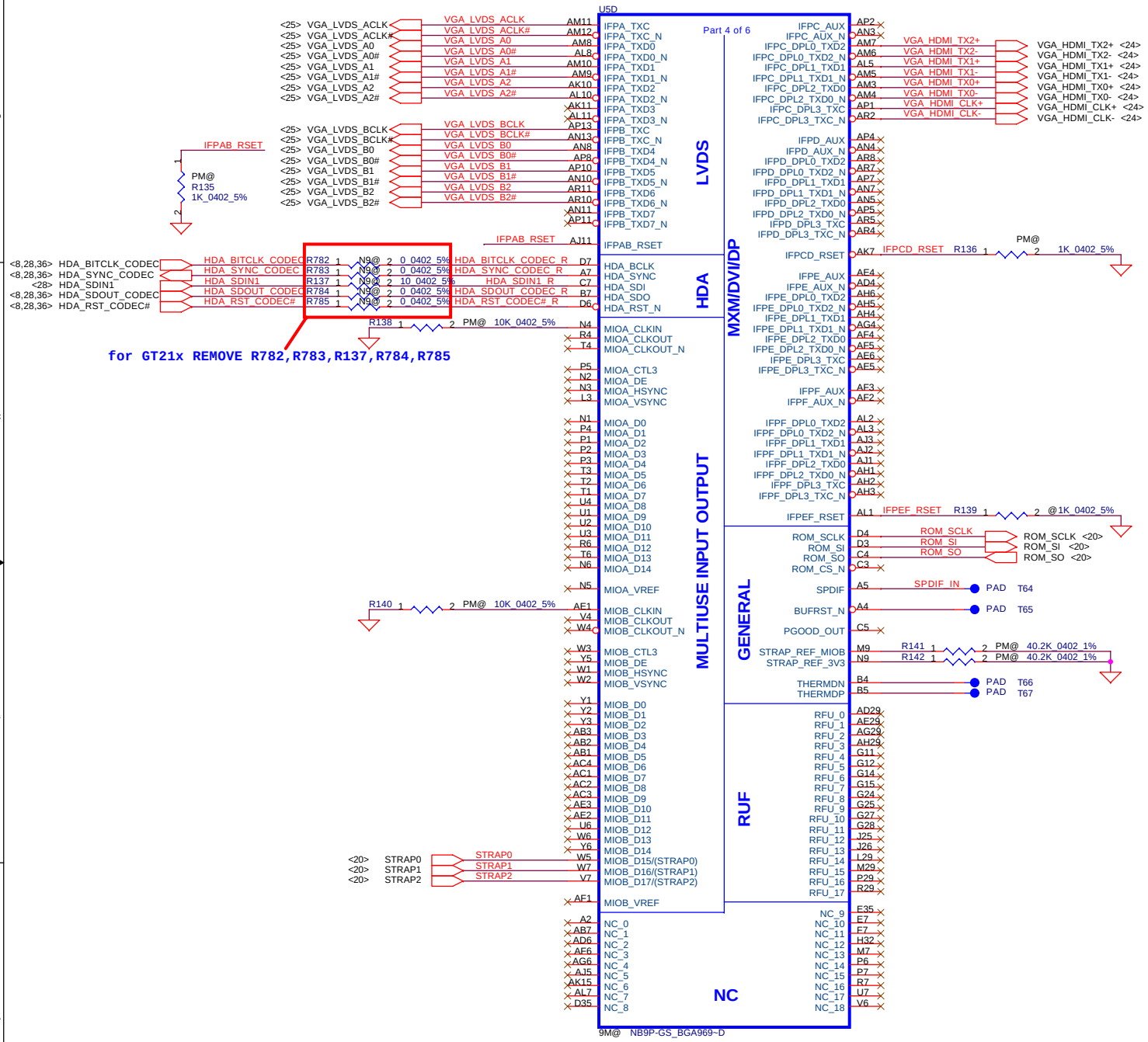
Compal Electronics, Inc.

Title: **NB9M-GE Memory**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

Date: Monday, June 30, 2008 | Sheet 17 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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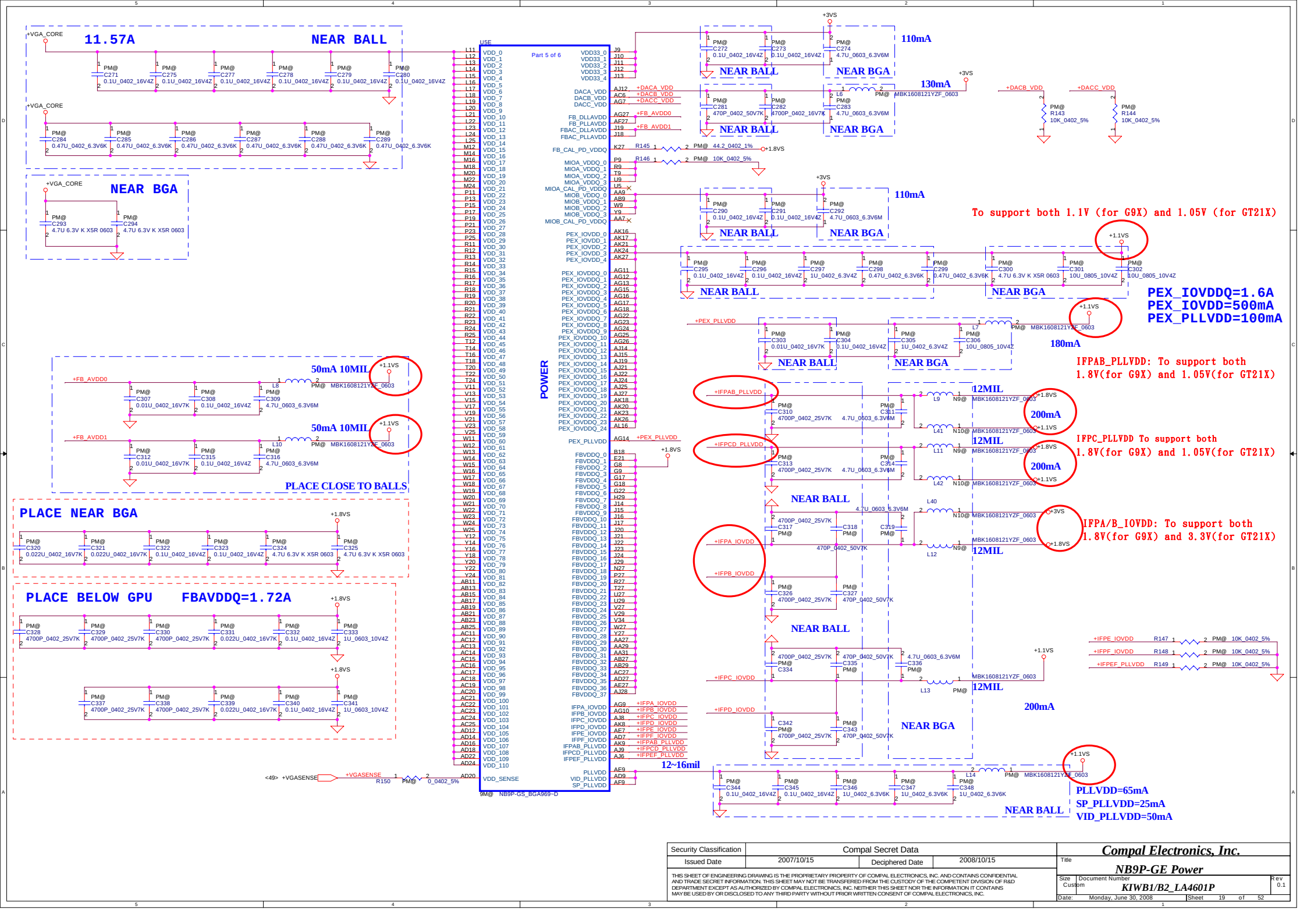
Compal Electronics, Inc.

Title: **NB9M/9P MIO,HDA,LVDS**

Size: Custom | Document Number: **KIWB1/B2_LA4601P** | Rev: 0.1

Date: Monday, June 30, 2008 | Sheet 18 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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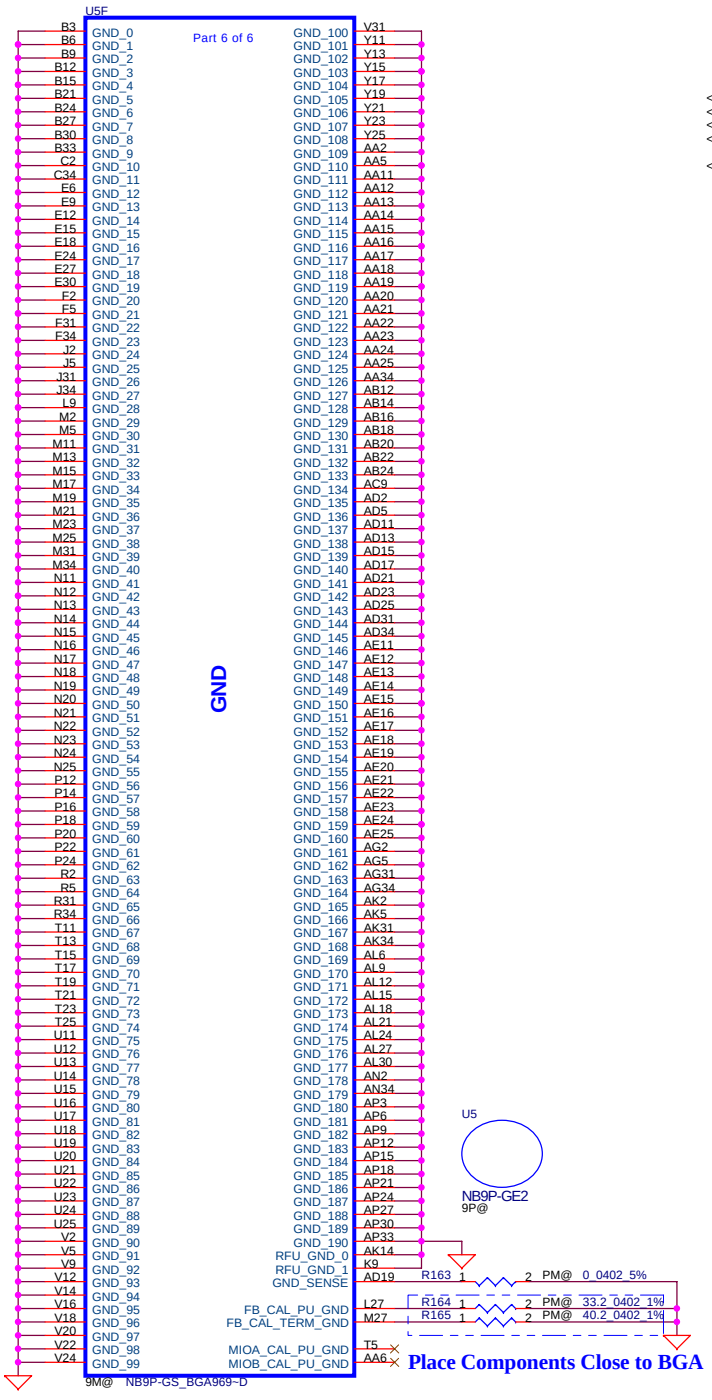
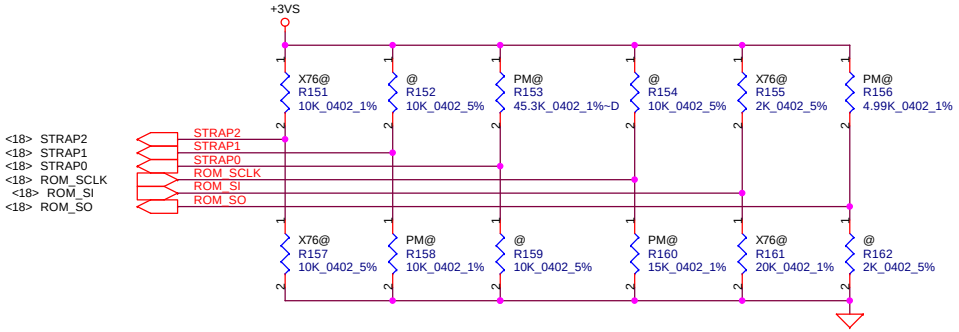
Compal Electronics, Inc.

Title: **NB9P-GE Power**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

Date: Monday, June 30, 2008 | Sheet 19 of 52





GB1 Family GPU Strap Qptions

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS 128bit	Samsung	16Mx32	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
	Hynix	16Mx32	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K
	Qimonda	16Mx32	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K

GPU	FB Memory		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9P-GE2 128bit	Samsung	16Mx32	PU 5K	PD 15K	PD 20K	PU 5K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 45K	PU 5K	PD 10K	PU 45K
	Hynix	16Mx32	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 35K	PU 5K	PD 10K	PU 45K
	Qimonda	16Mx32	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K	PU 45K
		32Mx32	PU 5K	PD 15K	PD 30K	PU 5K	PD 10K	PU 45K

Component	Manufacturer	Compal PN	Compal X76 PN
GDDR3 VRAM (16M*32)	Hynix	X	X
	Qimonda	X	X
	Samsung	X	X
GDDR3 VRAM (32M*32)	Hynix	X	X
	Qimonda	SA000024N20	
	Samsung	SA00002R600	

Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR3	33.2ohm	44.2ohm	40.2ohm
GDDR3 BY N10			

To update for NV PUN-03304-001_V06 (2008/5/20)

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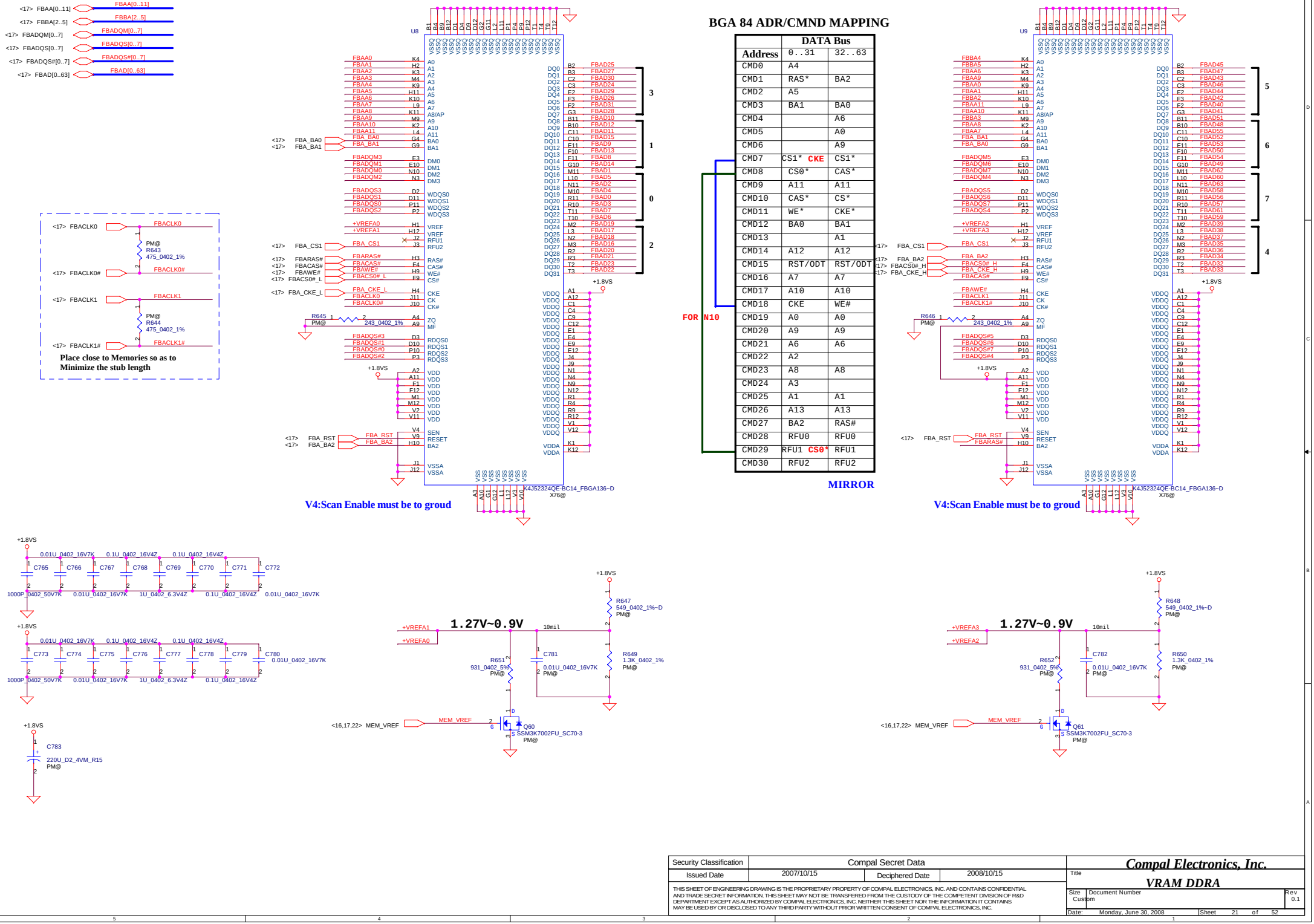
Compal Electronics,Ltd.

Title: NB9P-GE GND & STRAP

Size: Custom | Document Number: KIWB1/B2_LA4601P | Rev: 0.1

Date: Monday, June 30, 2008 | Sheet 20 of 52



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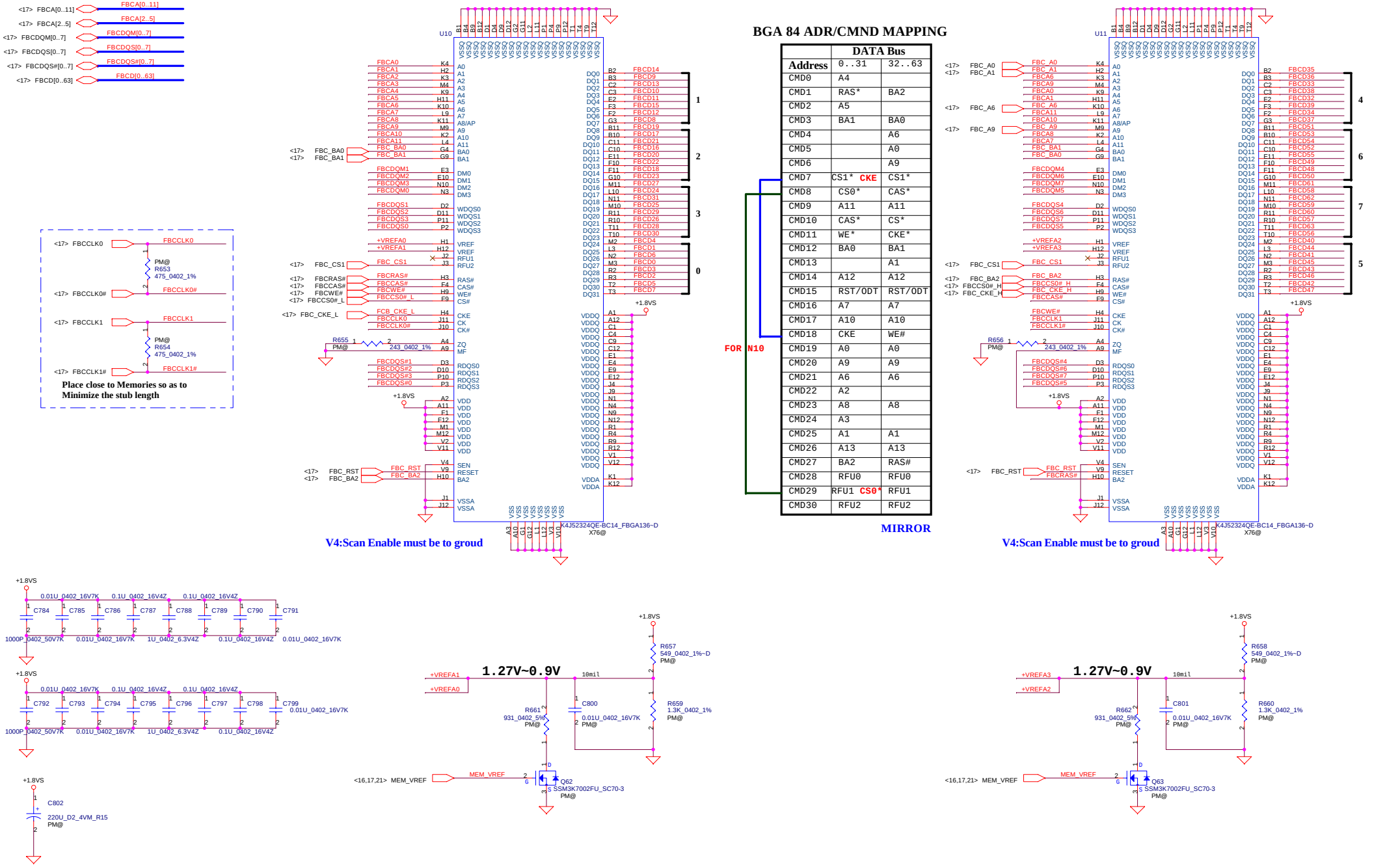
Compal Electronics, Inc.

Title: **VRAM DDRA**

Size	Document Number	Rev
Custom		0.1

Date: Monday, June 30, 2008 Sheet 21 of 52



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Compal Electronics, Inc.

Title: **VRAM DDRA**

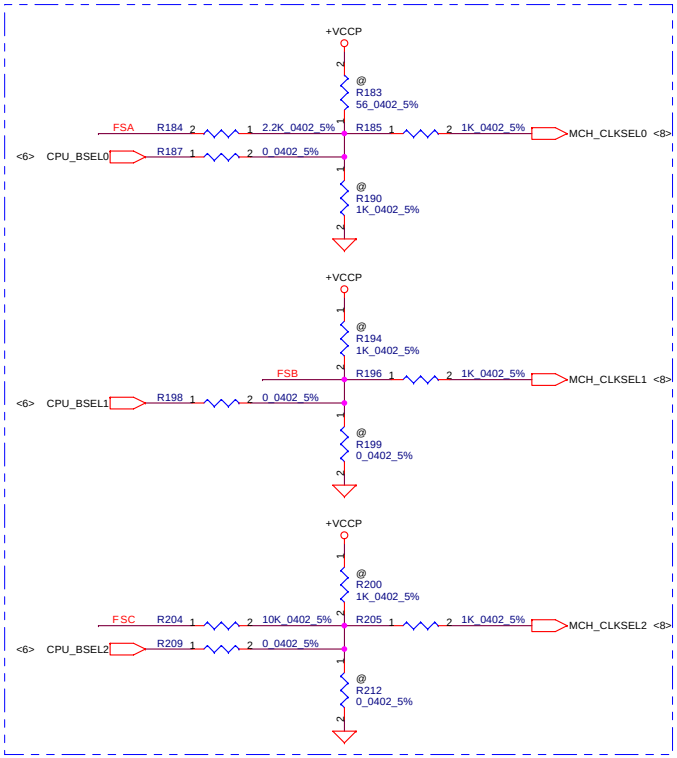
Size	Document Number	Rev
Custom		0.1

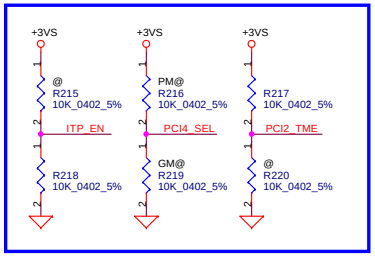
Date: Monday, June 30, 2008 Sheet 22 of 52

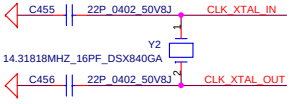
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

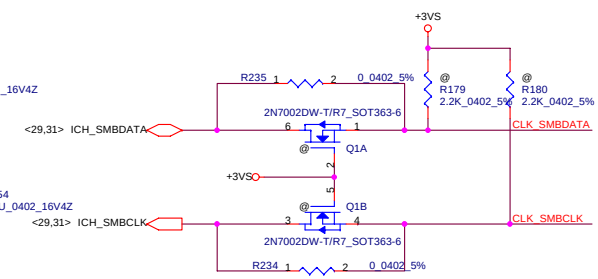
SA000020H00 (ICS : ICS9LPRS387AKLFT)





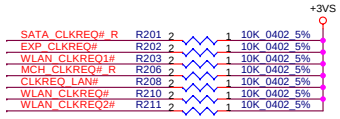


Routing the trace at least 10mil



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	PCIE_WLAN2
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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Compal Electronics,Ltd.

Title: Clock Generator CK505

Size: Custom | Document Number: KIWB3/B4_LA4551P | Rev: 0.1

Date: Monday, June 30, 2008 | Sheet 23 of 52

P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm

U17

GM@ PS8101TQFN48G_QFN48_7X7

TMDS pull down (500ohm) resistors G9x only

NEAR CONNECT

9/14 Modify for UMA used

9/14 Reserve for VGA used;check pin name

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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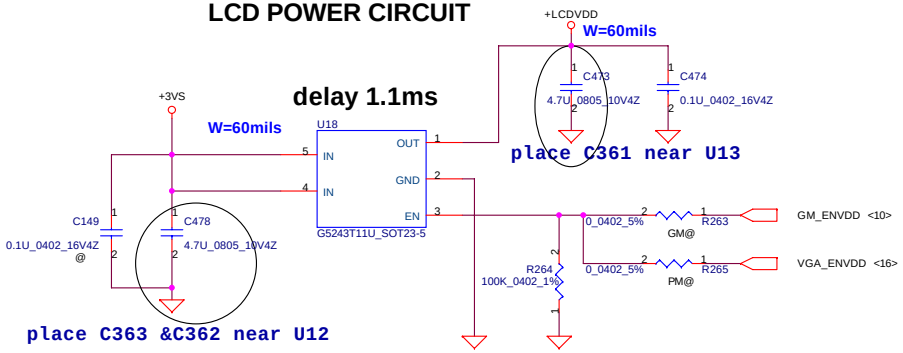
Compal Electronics,Ltd.

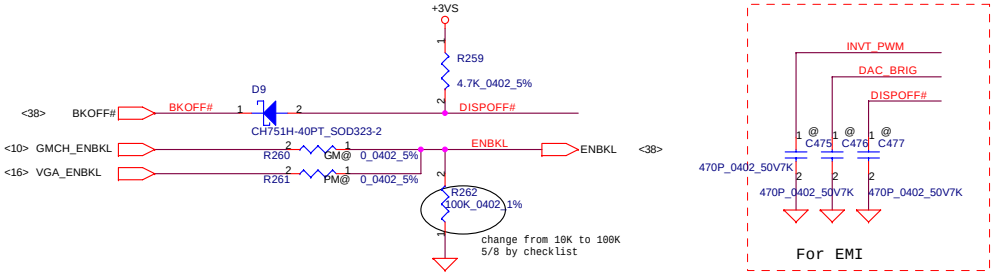
Title: Level Shiftter_PS8101T

Size: Custom | Document Number: KIWB1/B2_LA4601P | Rev: 0.1

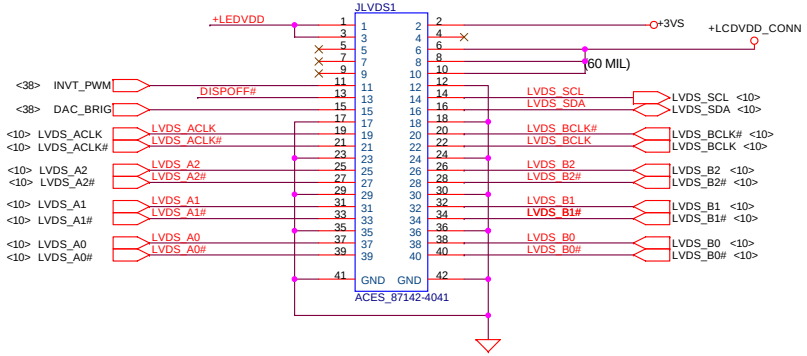
Date: Monday, June 30, 2008 | Sheet 24 of 52

LCD POWER CIRCUIT

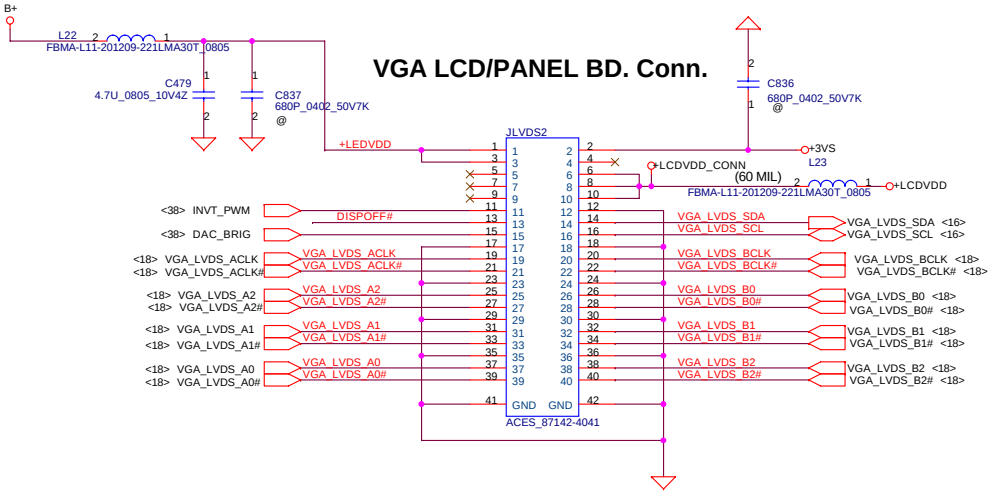




UMA LCD/PANEL BD. Conn.



VGA LCD/PANEL BD. Conn.



+LCDVDD

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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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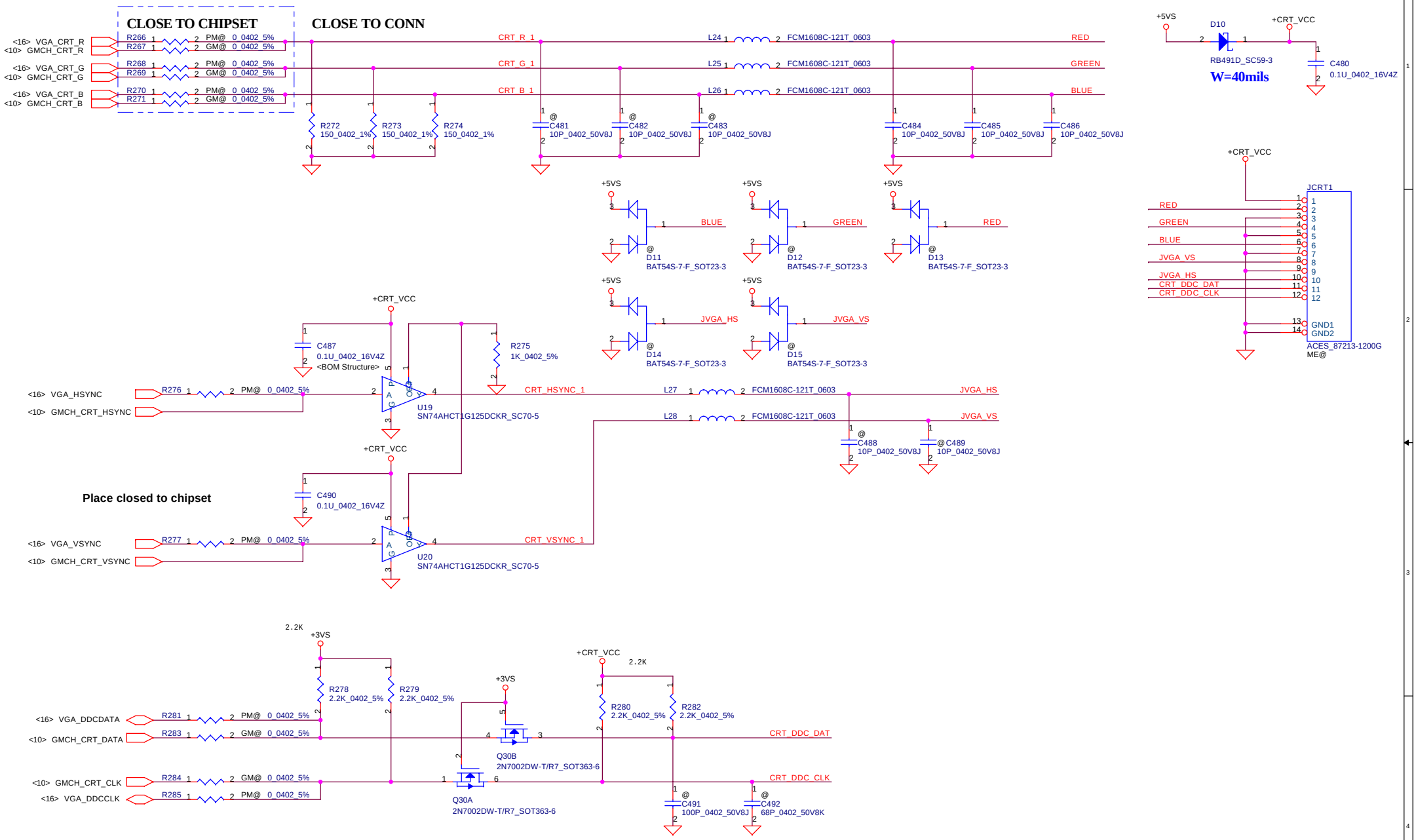
Compal Electronics, Inc.

Title: **LVDS & DVI Connector**

Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

Date: Monday, June 30, 2008 Sheet 25 of 52

CRT Connector



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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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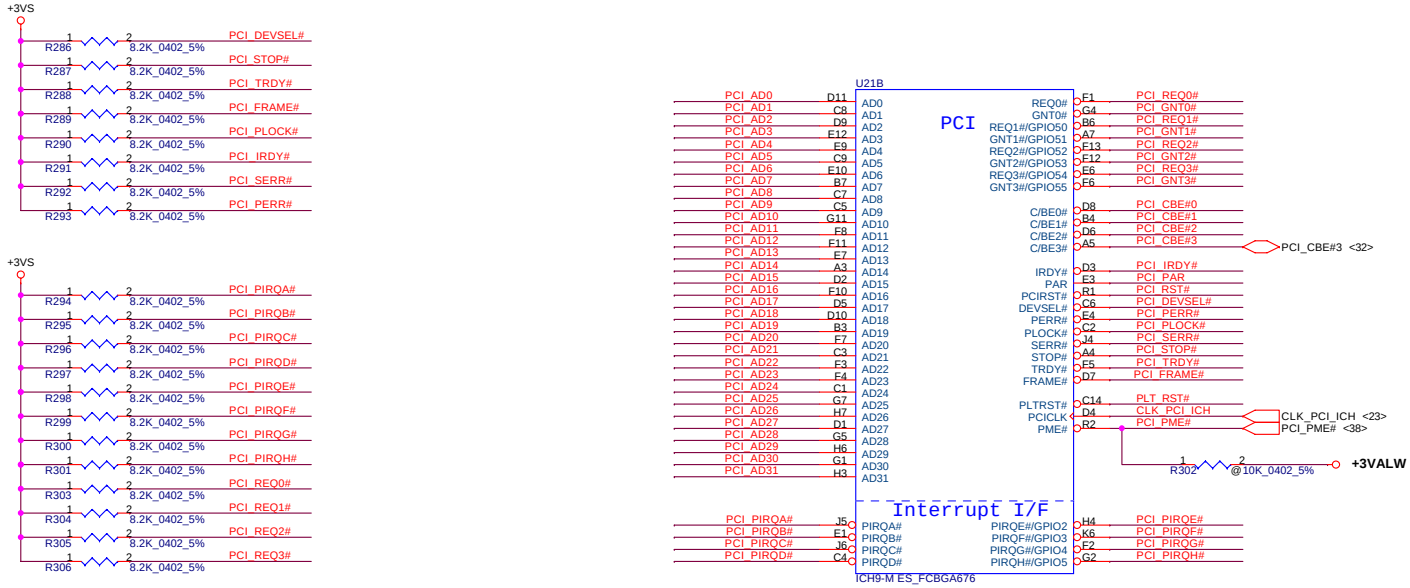
Compal Electronics, Inc.

Title: **CRT & TV-OUT Connector**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

Date: Monday, June 30, 2008 Sheet 26 of 52



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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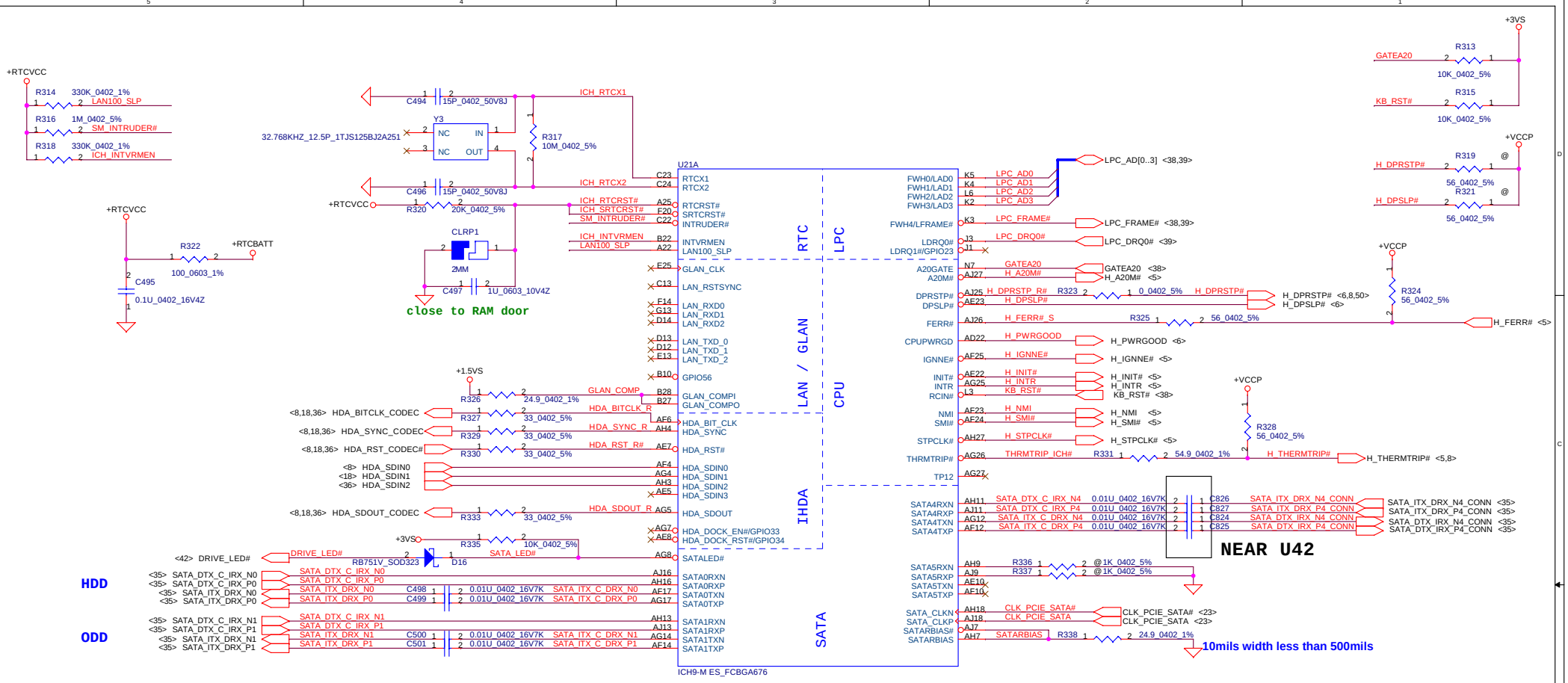
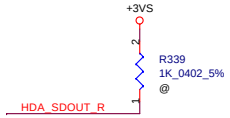
Compal Electronics, Inc.		
Title	ICH9M(1/4)-PCI	
Size	Document Number JITR1_LA-4141P	Rev 0.1
Date: Monday, June 30, 2008	Sheet 27 of 52	



Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
2	X
3	X
4	ESATA
5	X

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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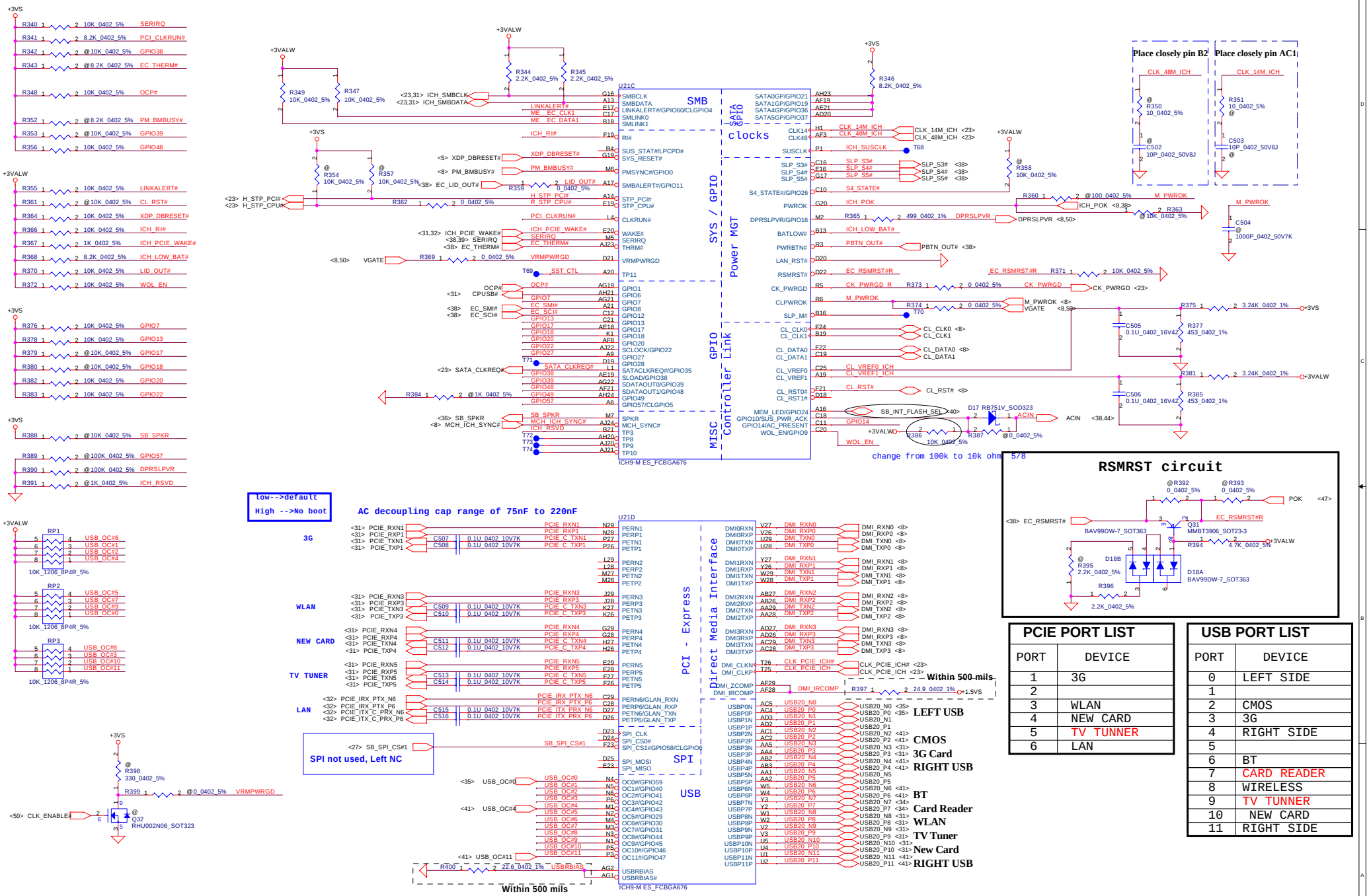
Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: JITR1_LA-4141P | Rev: 0.1

Date: Monday, June 30, 2008 | Sheet 28 of 52



PCIE PORT LIST	
PORT	DEVICE
1	3G
2	
3	WLAN
4	NEW CARD
5	TV TUNNER
6	LAN

USB PORT LIST	
PORT	DEVICE
0	LEFT SIDE
1	
2	CMOS
3	3G
4	RIGHT SIDE
5	
6	BT
7	CARD READER
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	RIGHT SIDE

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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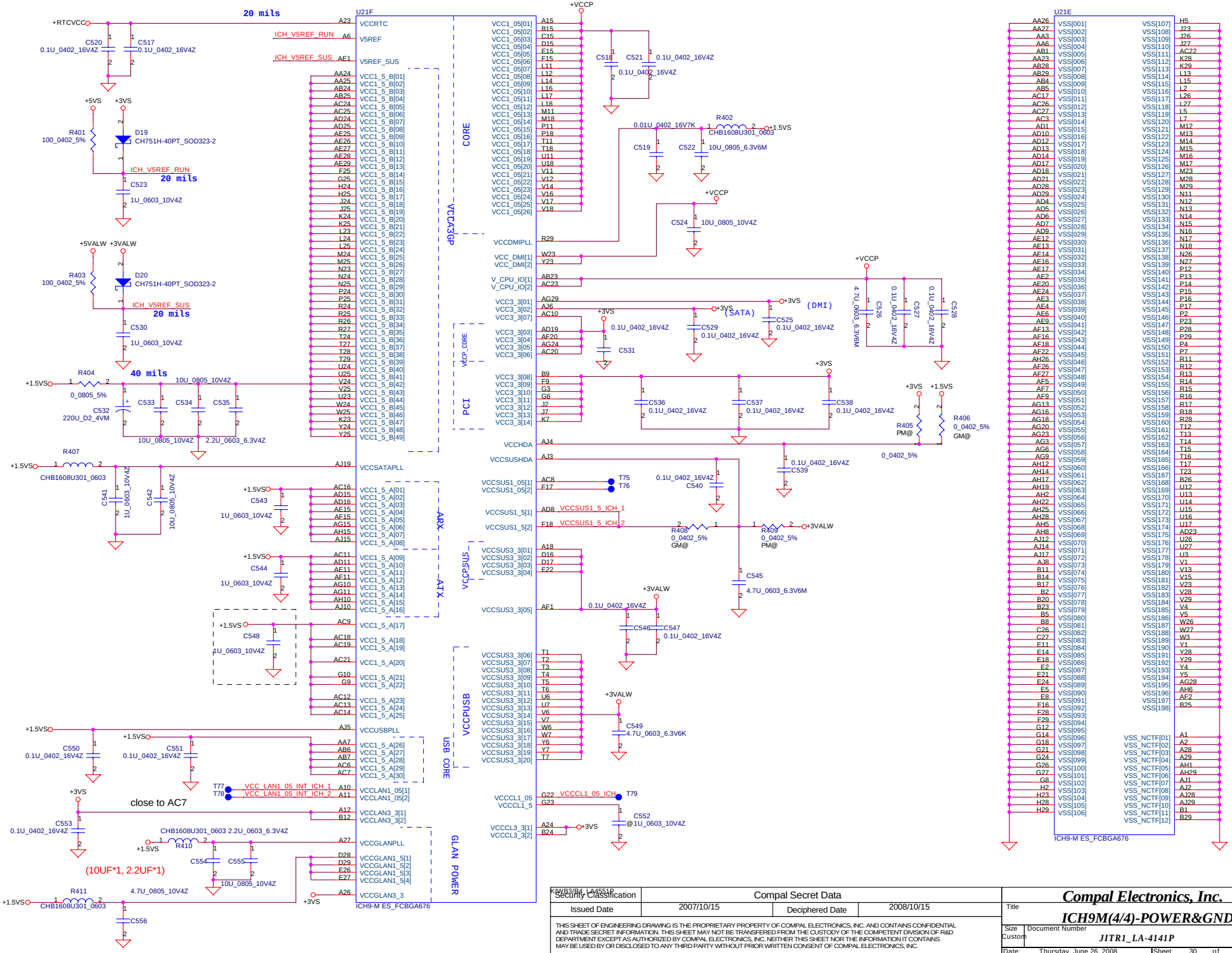
Compal Electronics, Inc.

Title: ICH9M(3/4)-USB,GPIO,PCIE

Size	Document Number	Rev
C	JITR1_LA-4141P	0.1

Date: Monday, June 30, 2008 Sheet 29 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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Compal Electronics, Inc.

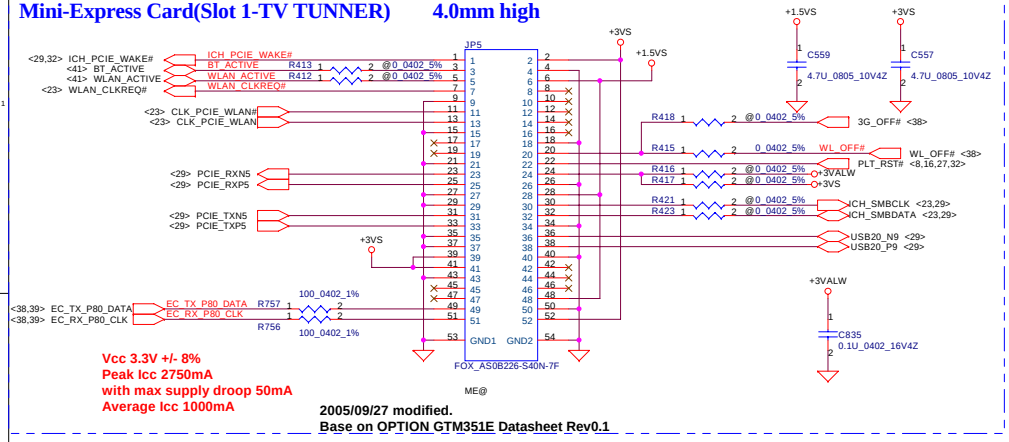
Title: **ICH9M(4/4)-POWER&GND**

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

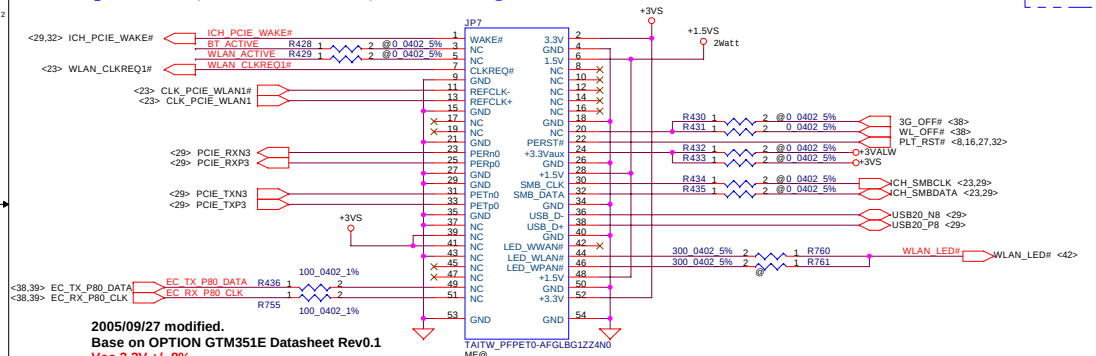
Date: Thursday, June 26, 2008 | Sheet 30 of 52

Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN

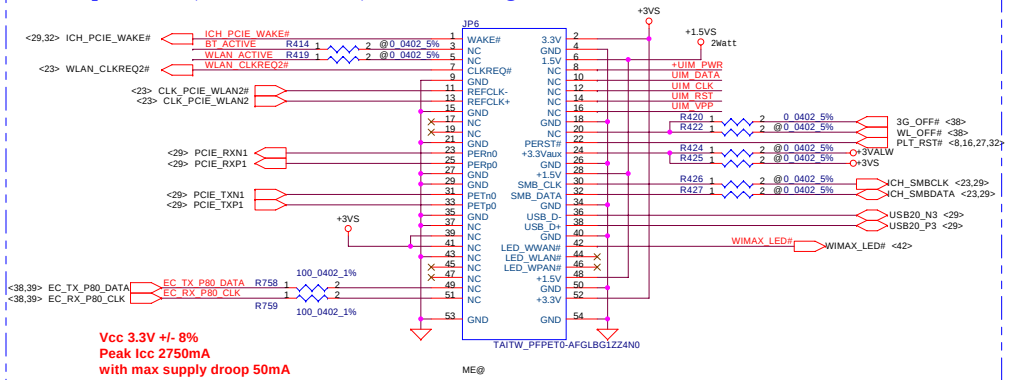
Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

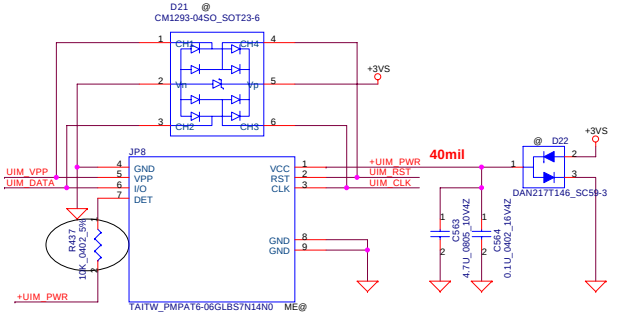


Mini-Express Card(Slot 2-WIRELESS) 5.6mm high

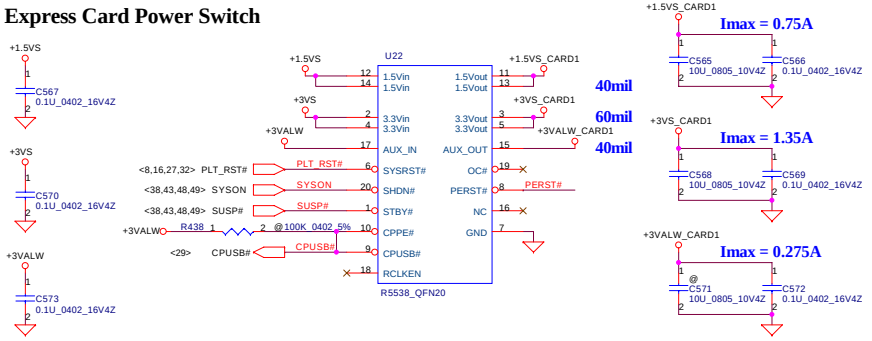


Mini-Express Card(Slot 3-WWAN 3G) 5.6mm high

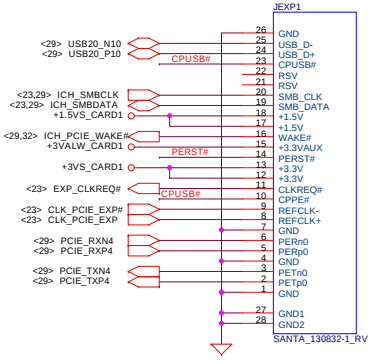




Express Card Power Switch



New Card 34mm Socket (Left/TOP)



update symbol 6/26

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Compal Electronics, Inc.

Title: Mini-Card/3G/FeliCa/BT

Size	Document Number	Rev
	JITR1_LA-4141P	0.1

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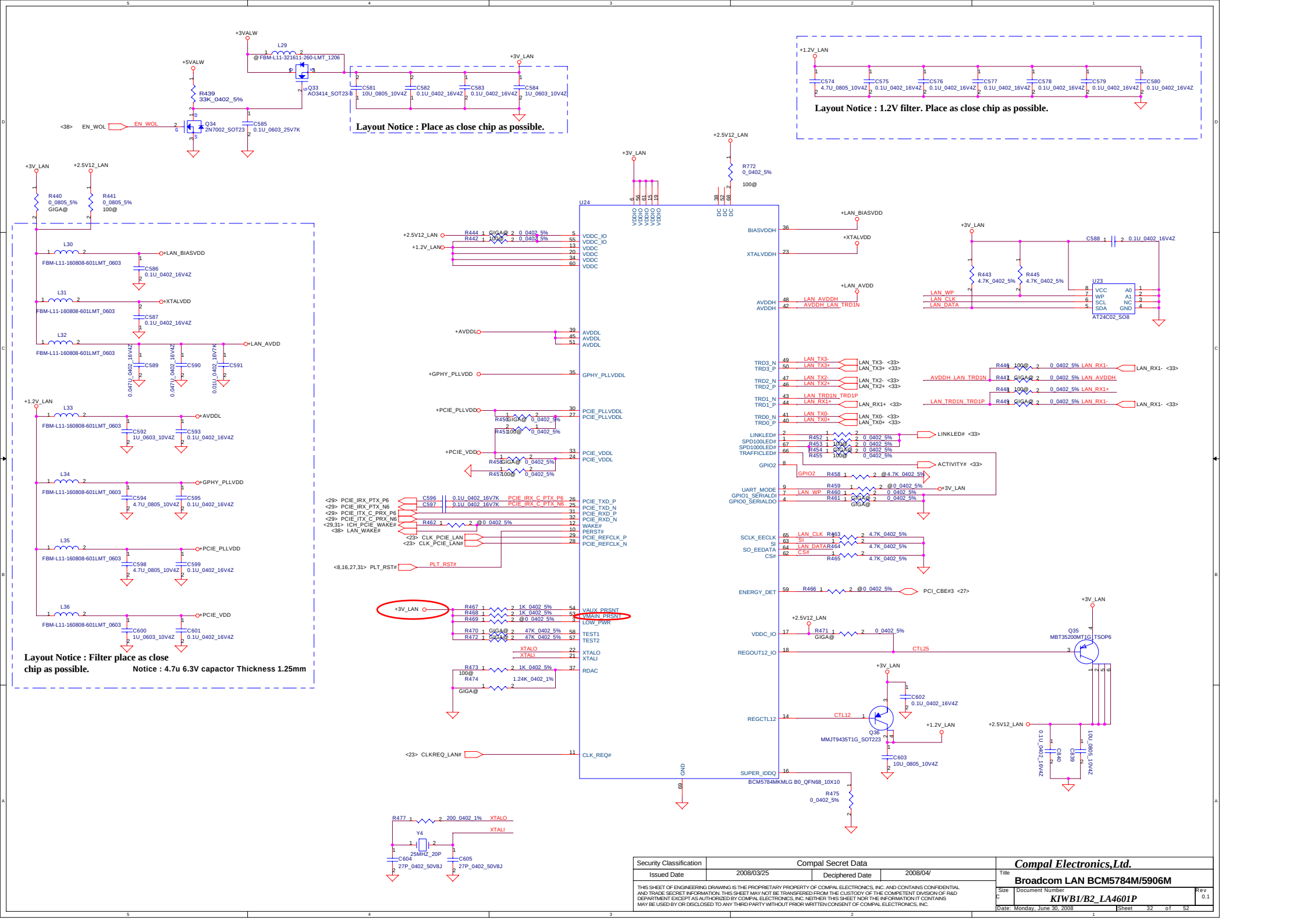

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Issued Date	2008/03/25	Deciphered Date	2008/04/

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Compal Electronics,Ltd.

Title: Broadcom LAN BCM5784M/5906M

Size	Document Number	Rev
C	KIWB1/B2_LA4601P	0.1

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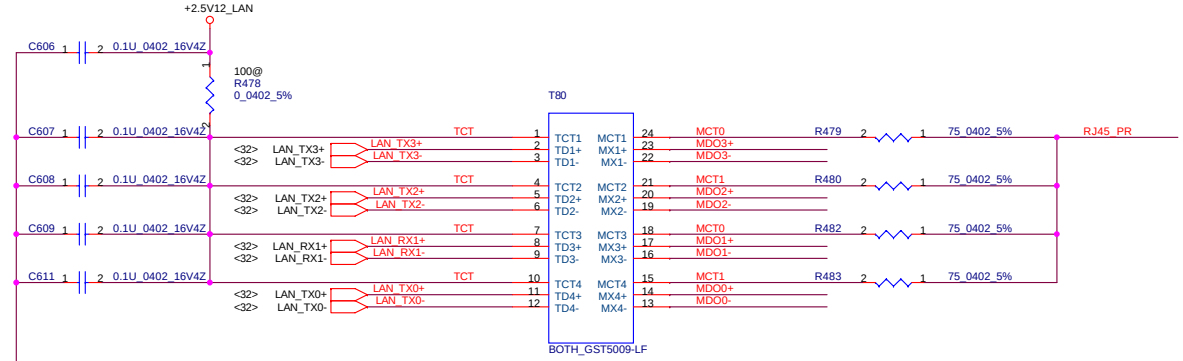
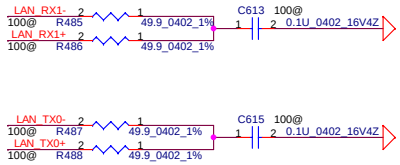
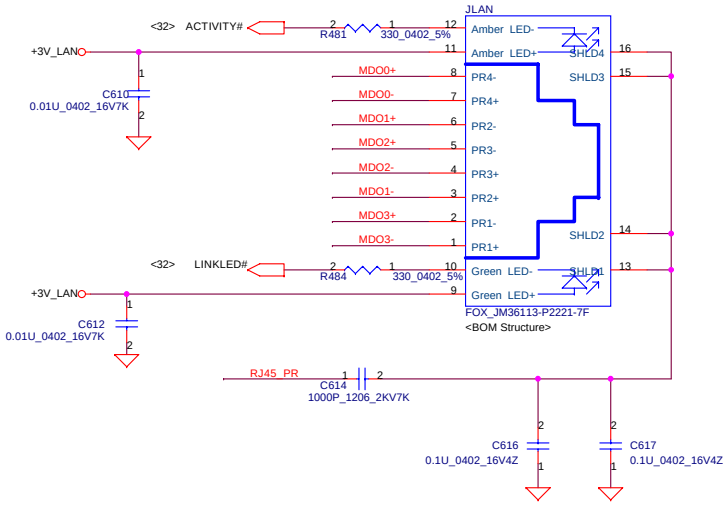


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

near LAN controller



RJ11+RJ45 CONN



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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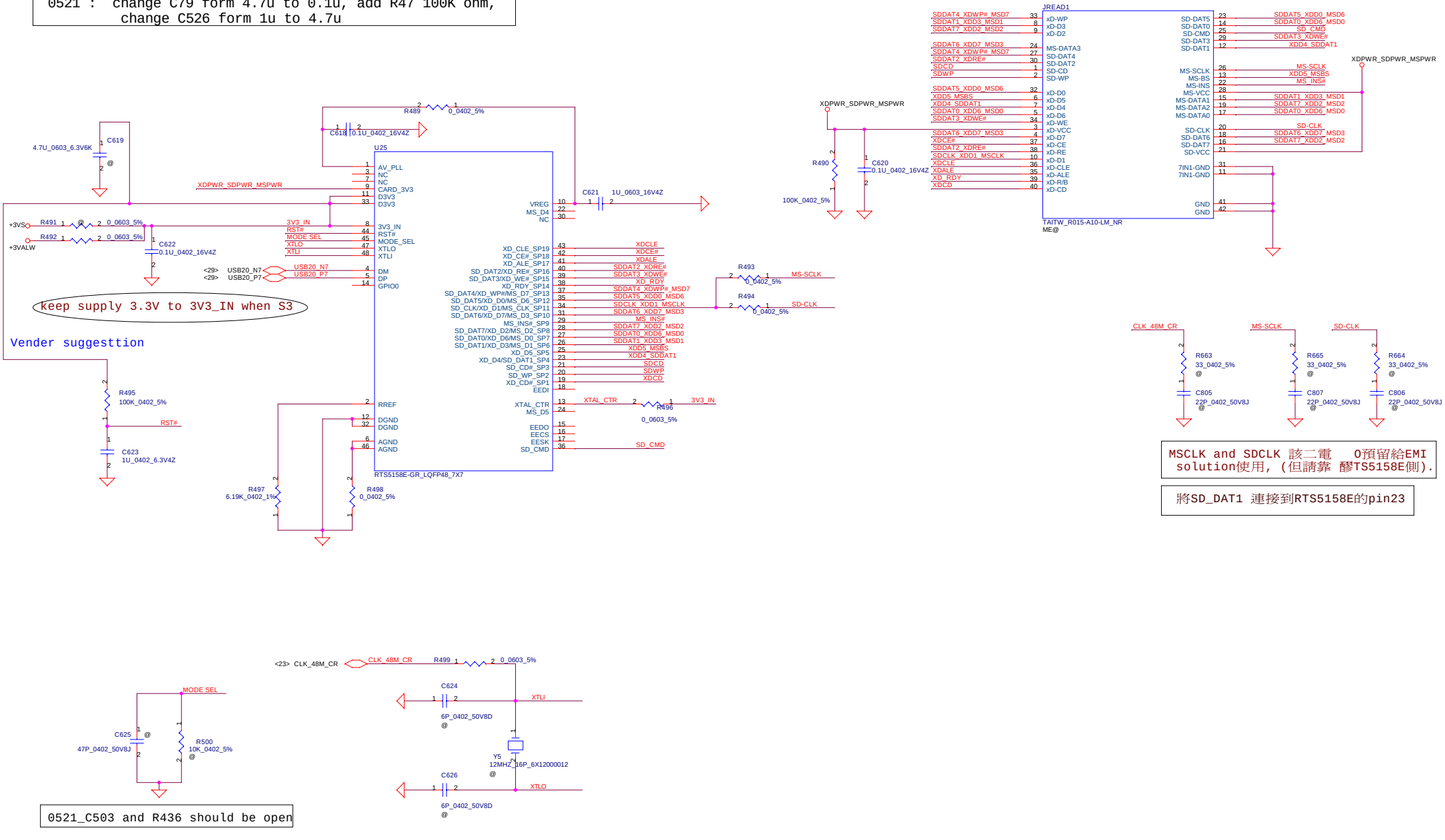
Compal Electronics, Inc.

Title: **LAN CONTROLLER**

Size	Document Number	Rev
Custom	KIWB1/B2_LA4601P	0.1

Date: Monday, June 30, 2008 Sheet 33 of 52

0513 : CARD_3V3 旁路電阻 100K change to 4.7u CAP==>預留
0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,
change C526 form 1u to 4.7u



Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

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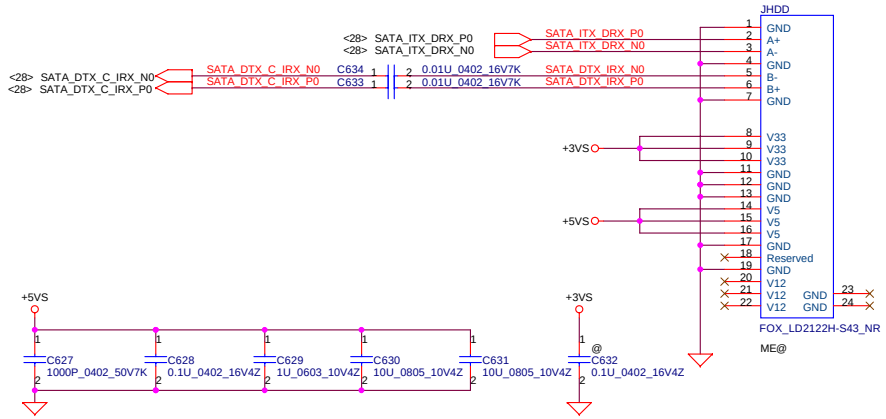
Compal Electronics, Inc.

Title: **1394+3 in 1 Card**

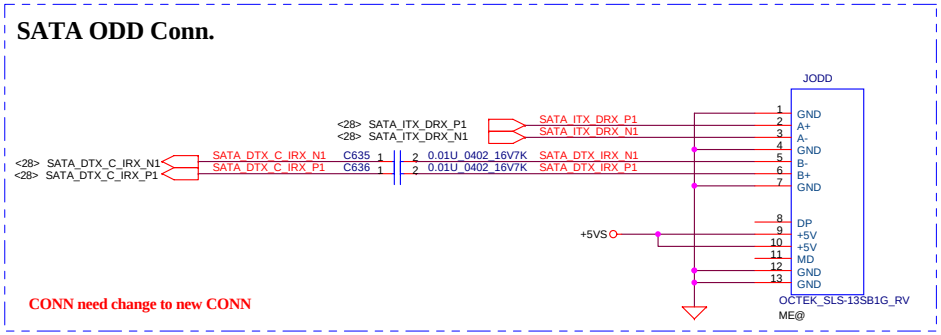
Size	Document Number	Rev
Custom	LA-3691P	1.0

Date: Monday, June 30, 2008 Sheet 34 of 52

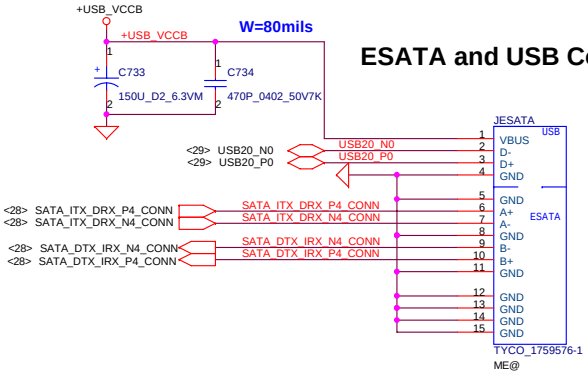
SATA HDD Conn.

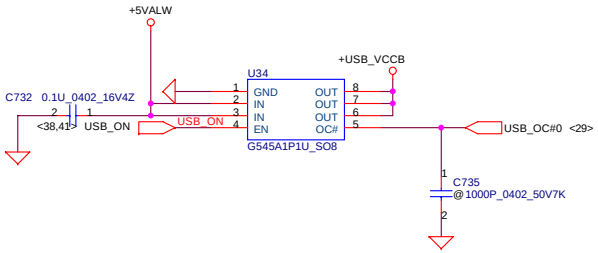


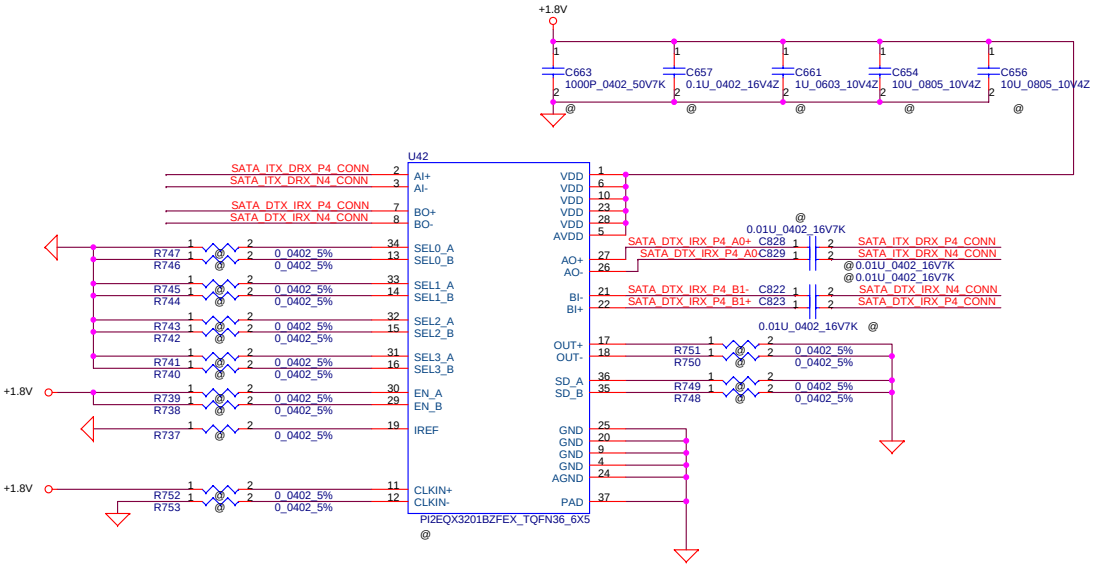
SATA ODD Conn.



ESATA and USB Conn.







OUTPUT SWING CONTROL

SEL2_[A:B]	SWING
0	1X
1	1.2X

OUTPUT DE-EMPHASIS ADJUSTMENT

SEL3_[A:B]	DE-EMPHASIS
0	9dB
1	-3.5dB

EQUALIZER SELECTION

SEL3_[A:B]	DE-EMPHASIS	COMPLIANCE CHANNEL
0	0	NO EQUALIZATION
1	1	[0:2.2.5dB]@1.6GHz
1	0	[2.5:4.5dB]@1.6GHz
1	1	[4.5:6.5dB]@1.6GHz

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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Compal Electronics, Inc.

Title: **HDD & ODD Connector**

Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

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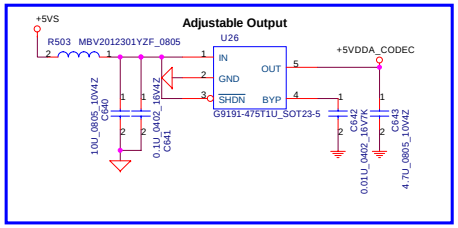
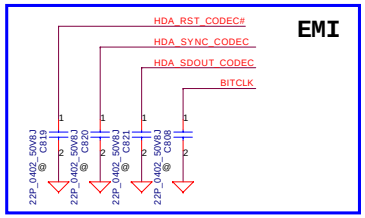
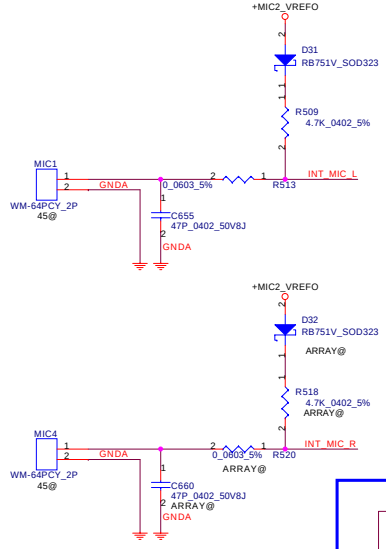
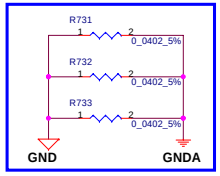
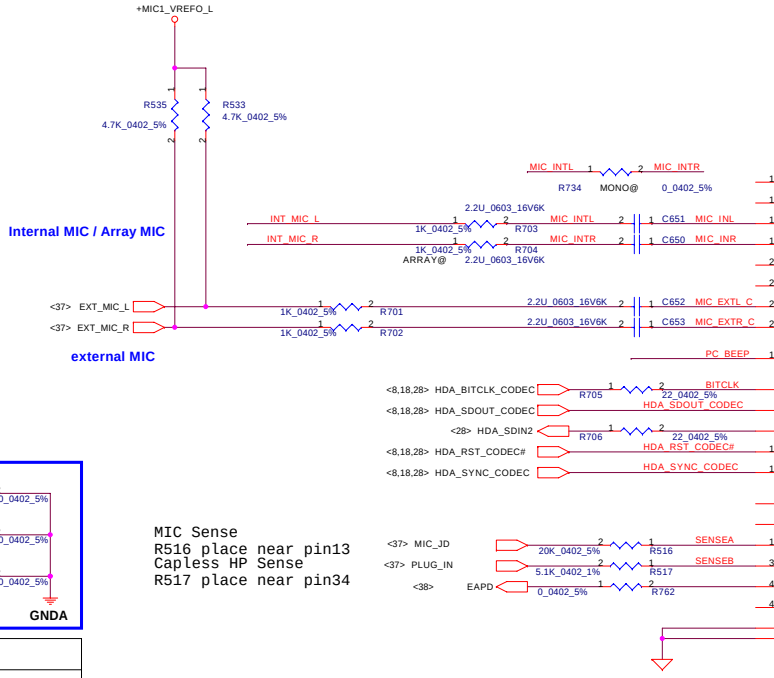


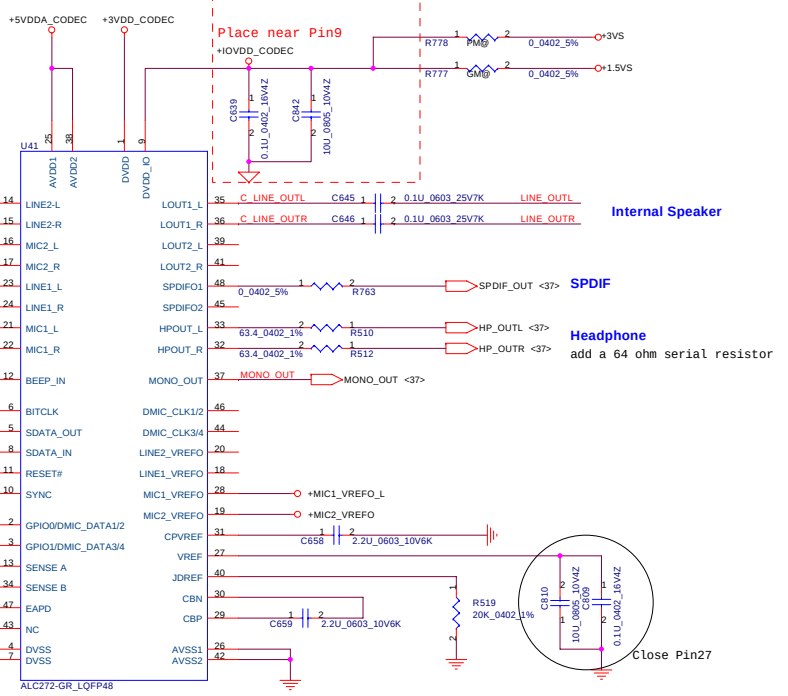




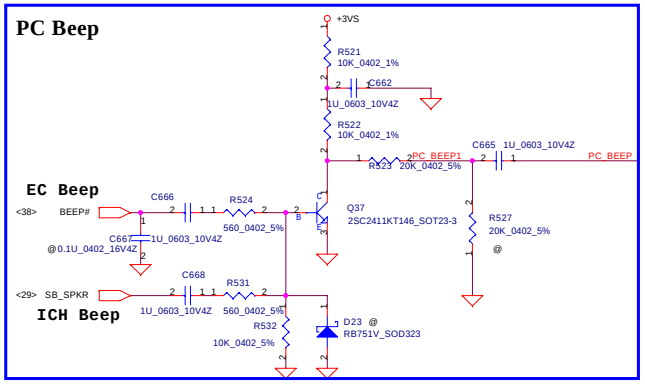


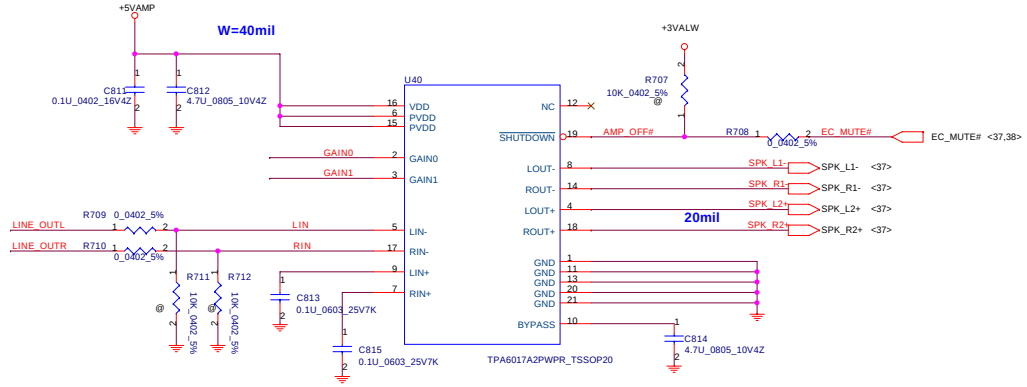


MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34

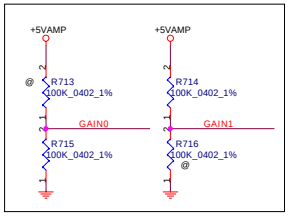


Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	Internal Subwoofer
MIC2(Pin16/17)	Internal	Internal Mic





GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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Compal Electronics,Ltd.

Title: HD Audio Codec_ALC272

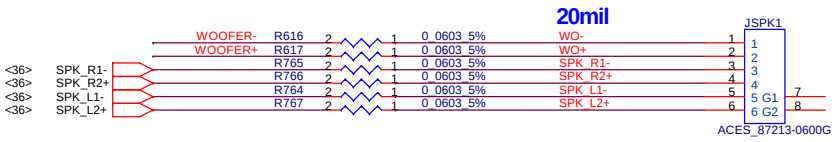
Size	Document Number	Rev
C	KIWB1/B2_LA4601P	0.1

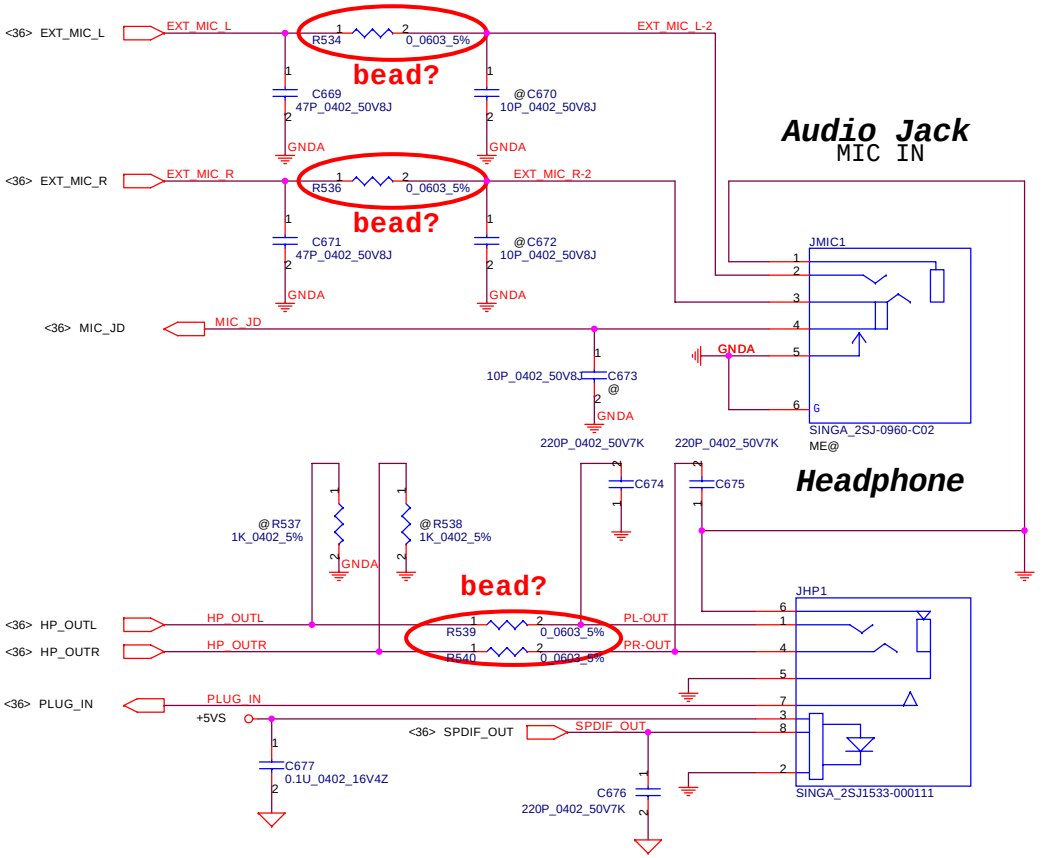
Date: Monday, June 30, 2008 Sheet 36 of 52

Audio Jack

SubWoofer Conn.

Speaker Connector

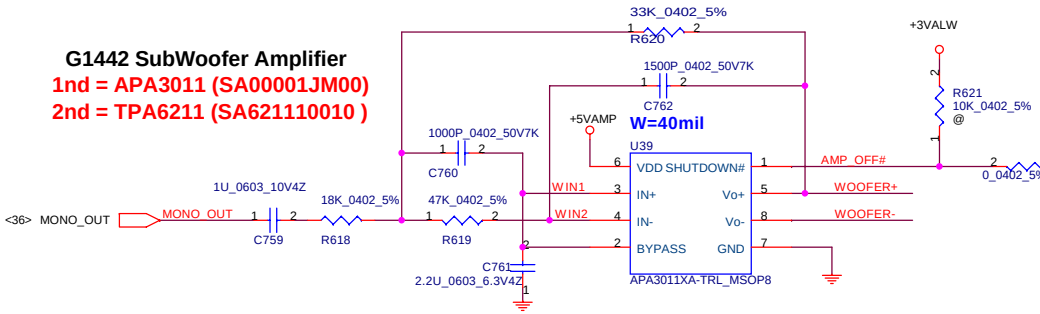




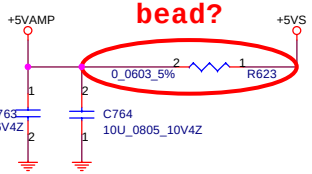
G1442 SubWoofer Amplifier

1nd = APA3011 (SA00001JM00)

2nd = TPA6211 (SA621110010)



ONLY FOR 15.6W



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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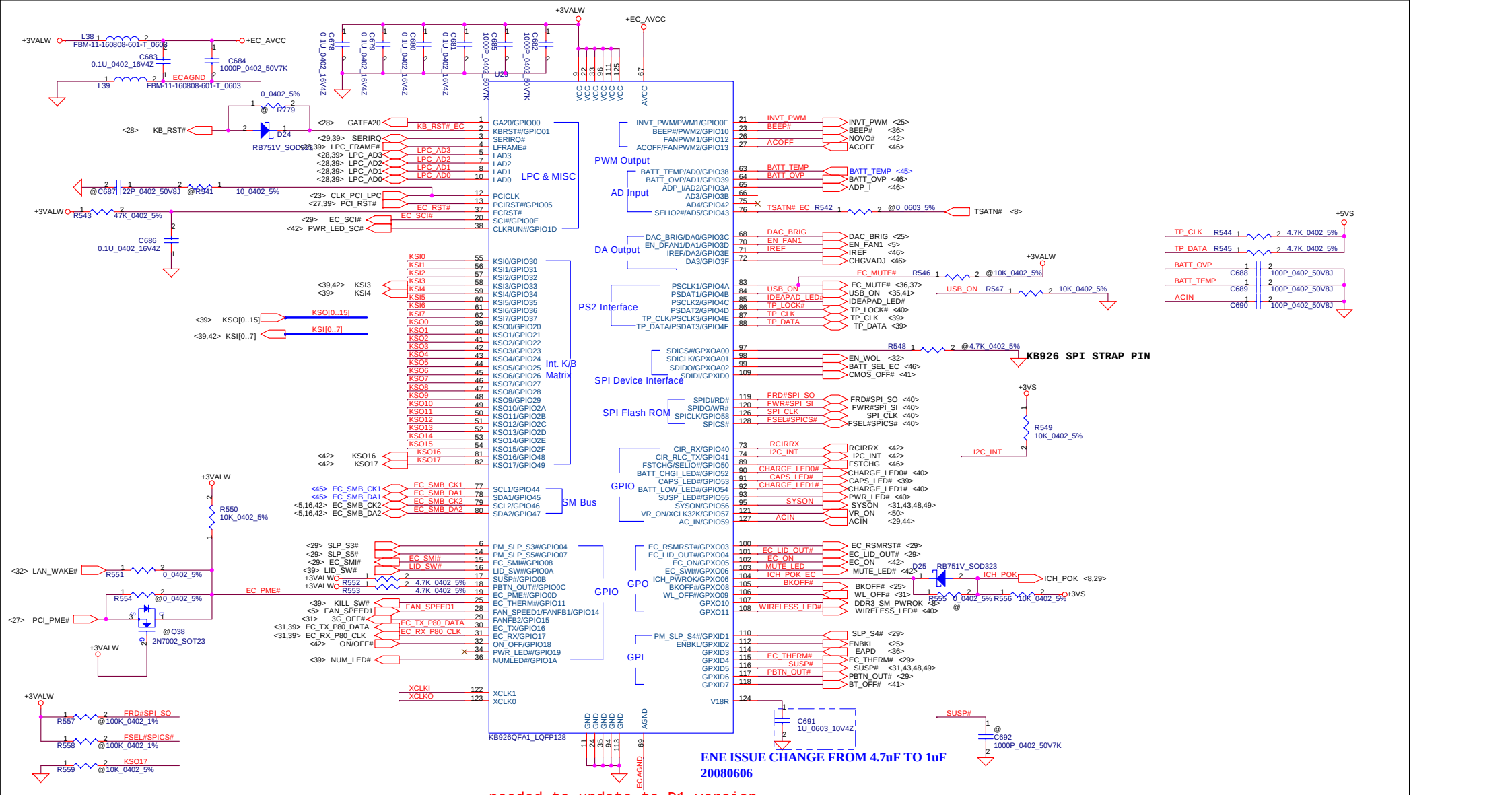
Compal Electronics,Ltd.

Title: **AMP,Audio speaker CONN**

Size: Custom | Document Number: *KIWB1/B2_LA4601P* | Rev: 0.1

Date: Monday, June 30, 2008 | Sheet 37 of 52



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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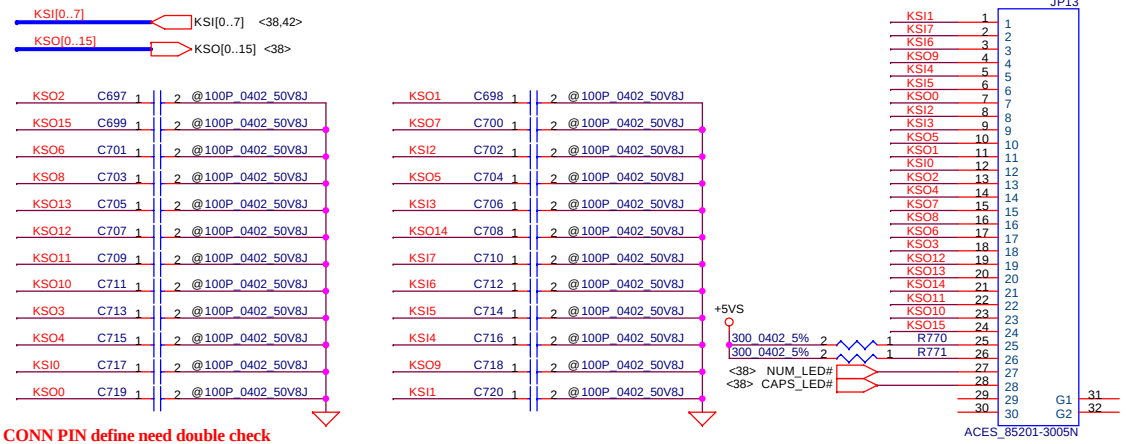
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	JITR1_LA-4141P	0.1

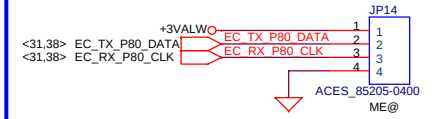
Date: Monday, June 30, 2008 | Sheet 38 of 52

INT_KBD Conn.

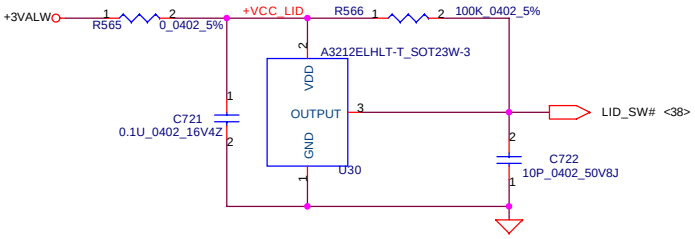


CONN PIN define need double check

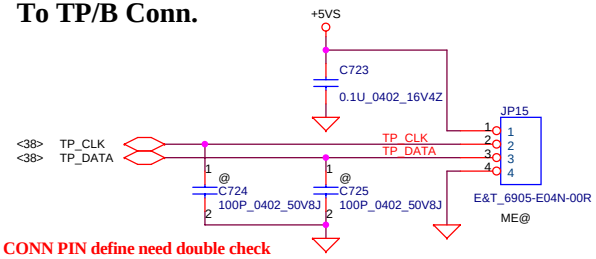
EC DEBUG PORT



Lid Switch

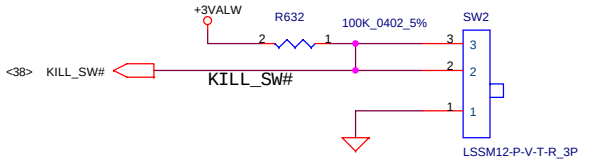


To TP/B Conn.

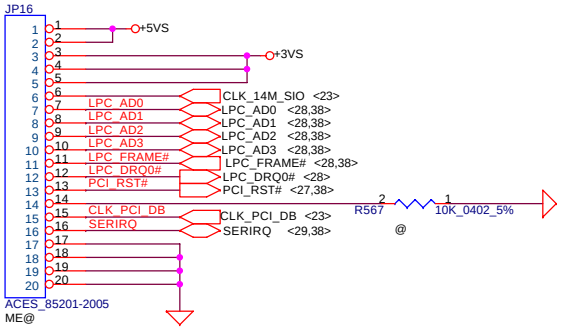


CONN PIN define need double check

Kill Switch



FOR LPC SIO DEBUG PORT



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

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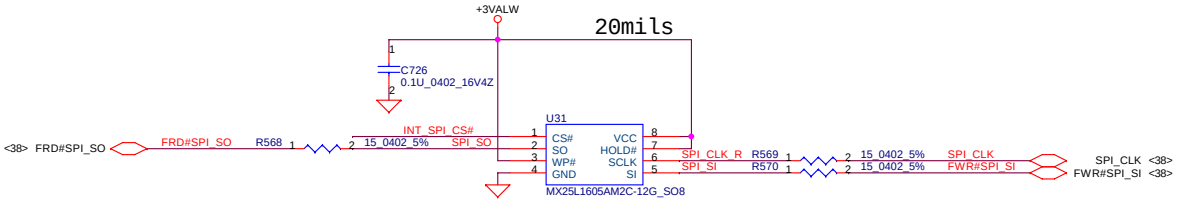
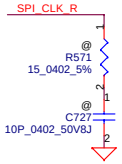
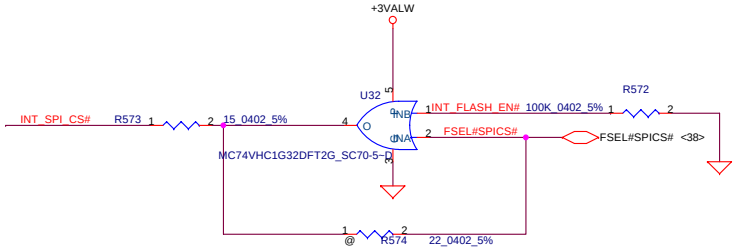
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIWB1/B2_LA4601P		Rev: 0.1
Date: Monday, June 30, 2008	Sheet 39 of 52		

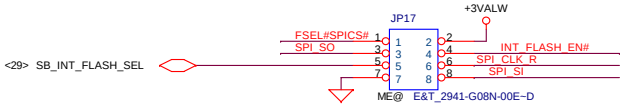
FOR EC 16M SPI ROM

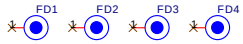




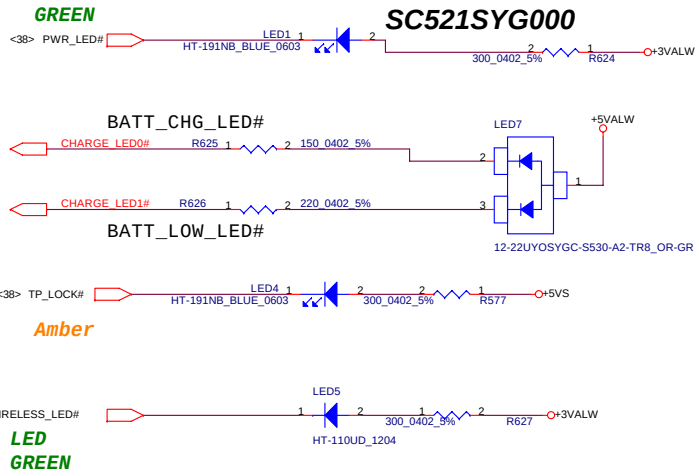
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

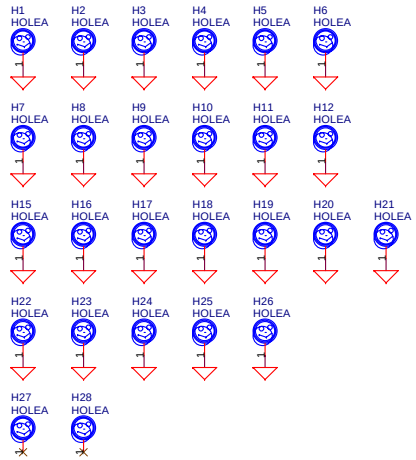






LED





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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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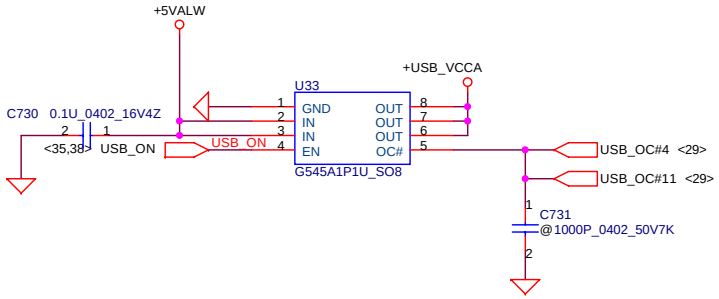
Compal Electronics, Inc.

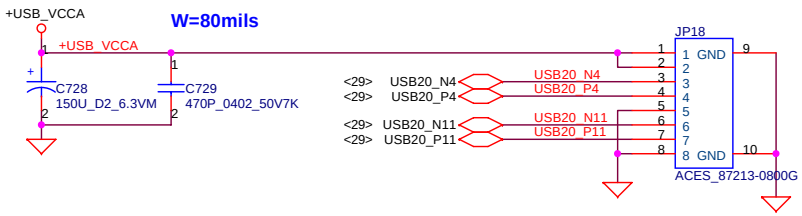
Title: **LED/EC SPI ROM**

Size	Document Number	Rev
B	KIWB1/B2_LA4601P	0.1

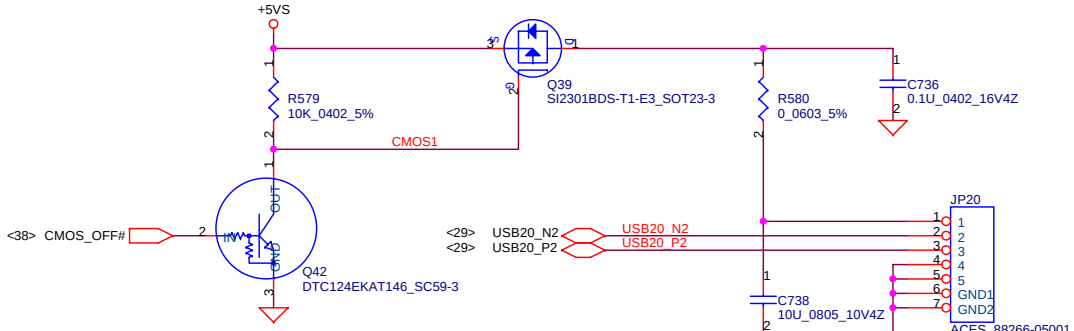
Date: Monday, June 30, 2008 Sheet 40 of 52

USB Board Conn. 10 pin

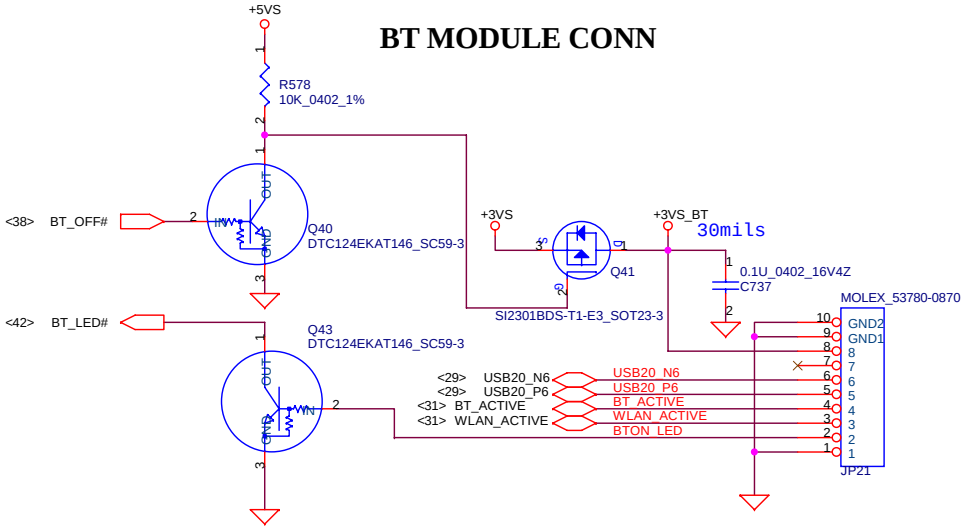




CMOS Camera Conn



BT MODULE CONN



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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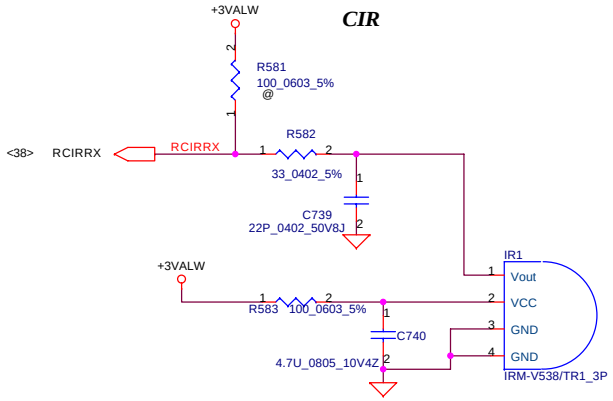
Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

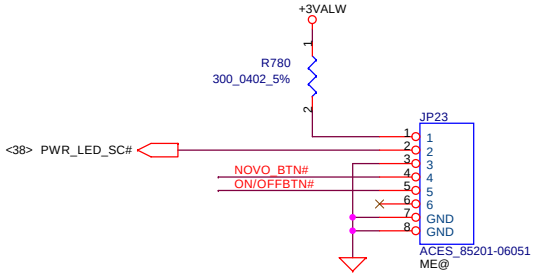
Size	Document Number	Rev
Custom	*KIWB1/B2_LA4601P*	0.1

Date: Monday, June 30, 2008 | Sheet 41 of 52

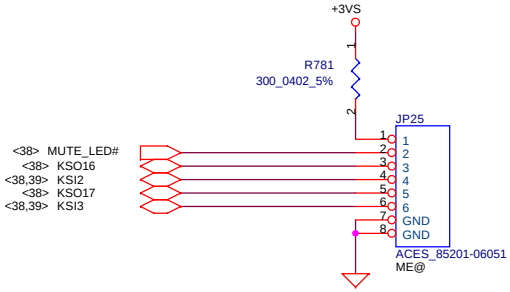
CIR



Power Bottom Board Conn. 5 pin

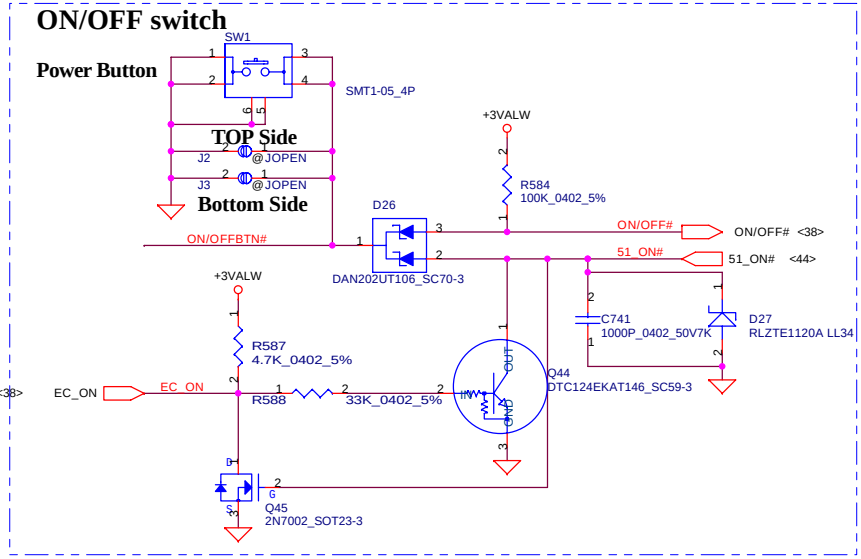


Bottom Board Conn. 6 pin

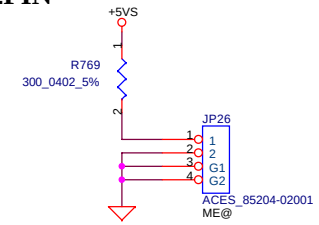


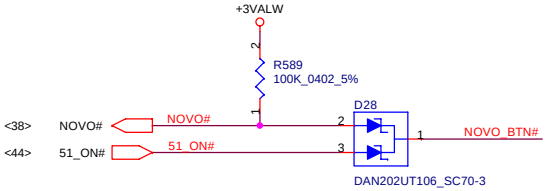
BTN FUNCTION	KEY MATRIX	
	IN	OUT
MUTE BTN	KSO17	KSI3
DOWN	KSO17	KSI2
UP	KSO16	KSI2

ON/OFF switch

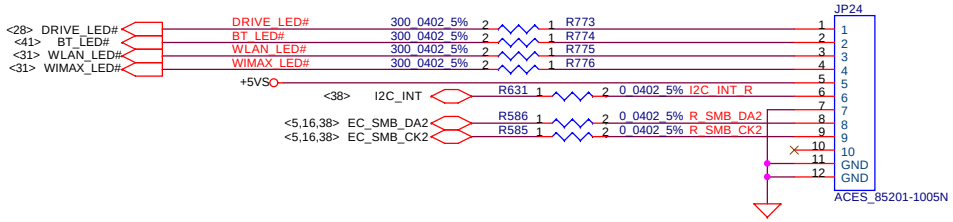


IDEAPAD BOARD 2PIN





Slide Board Conn. 12 pin



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Issued Date	2008/03/25	Deciphered Date	2008/04/

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Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

Size	Document Number	Rev
Custom	*KIWB1/B2_LA4601P*	0.1

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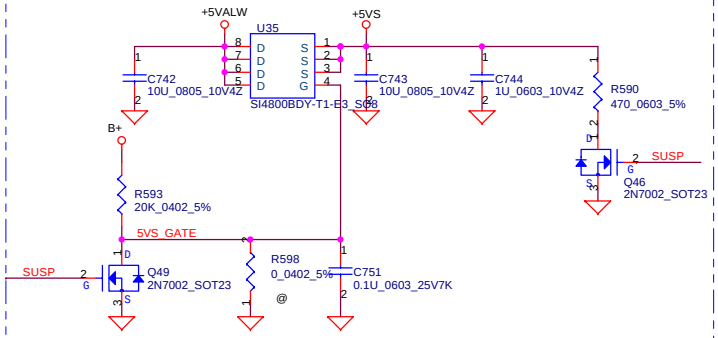
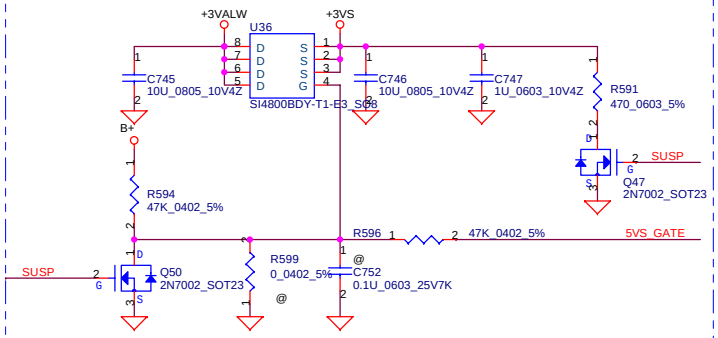
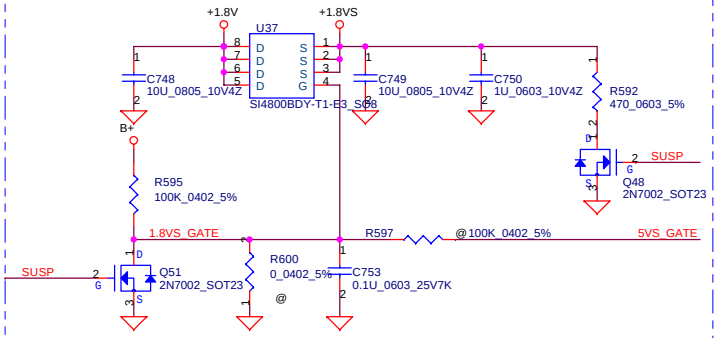
+5VALW TO +5VS



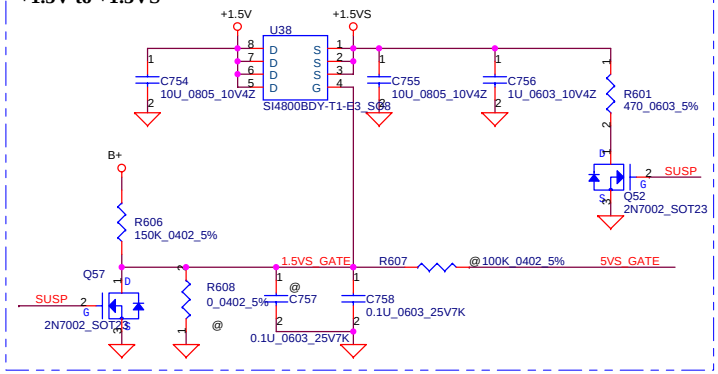
+3VALW TO +3VS

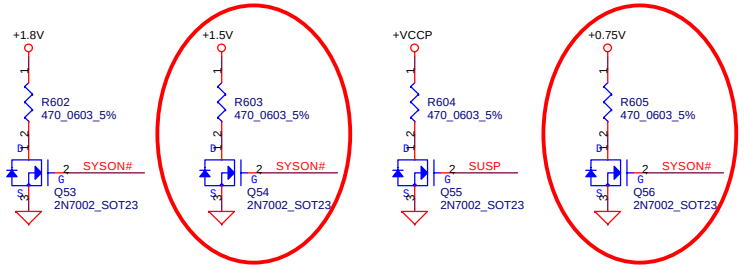


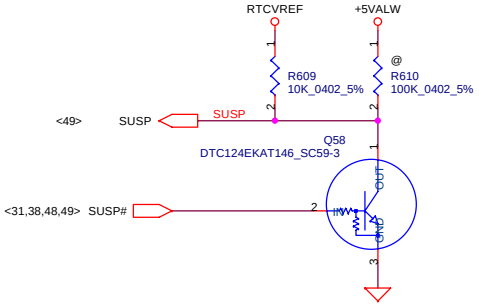
+1.8V to +1.8VS

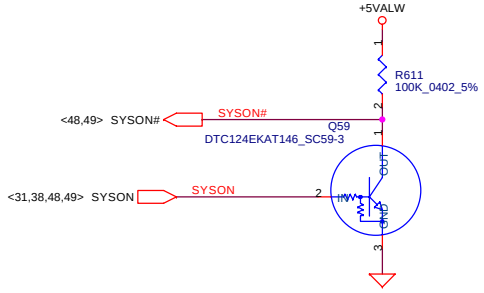


+1.5V to +1.5VS









Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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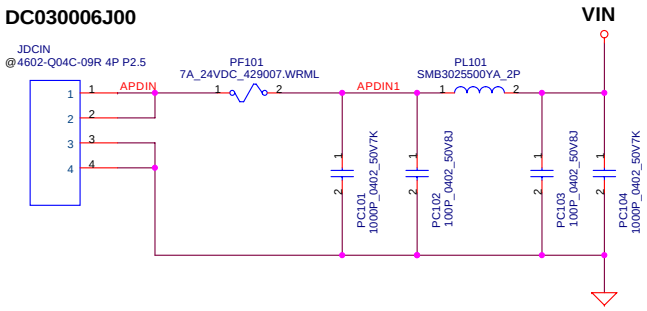
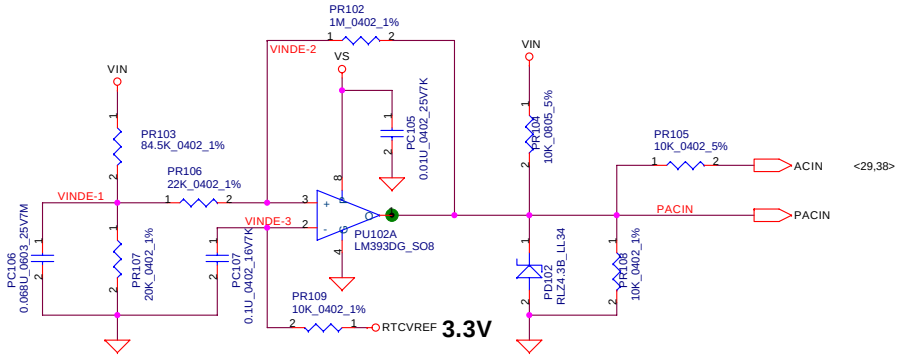
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	*KIWB1/B2_LA4601P*	0.1

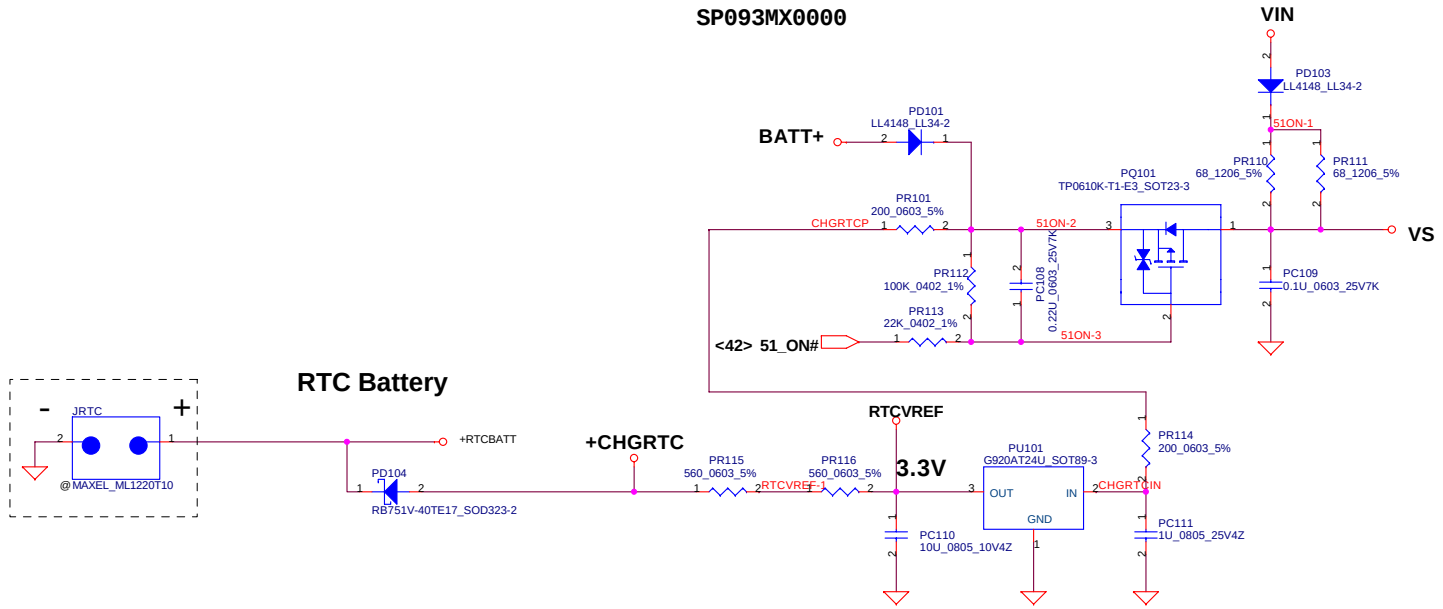
Date: Monday, June 30, 2008 Sheet 43 of 52





Vin Detector

High	**18.384**	**17.901**	**17.430**
Low	**17.728**	**17.257**	**16.976**



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Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

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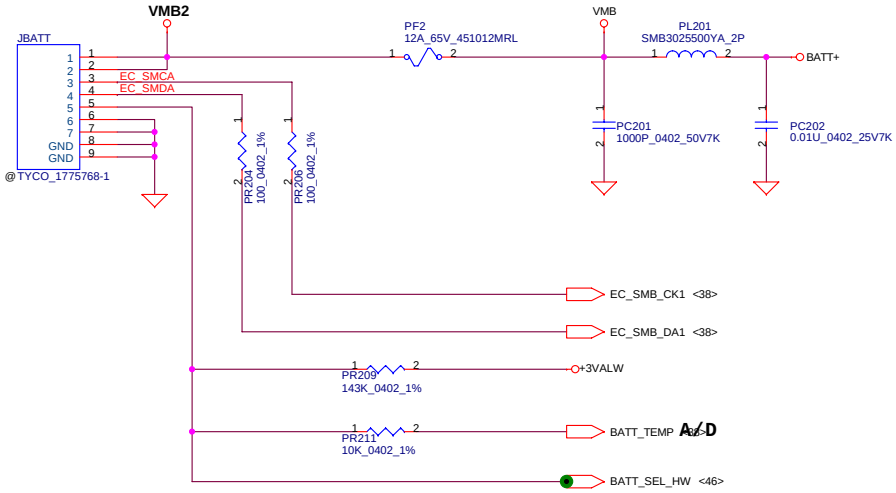
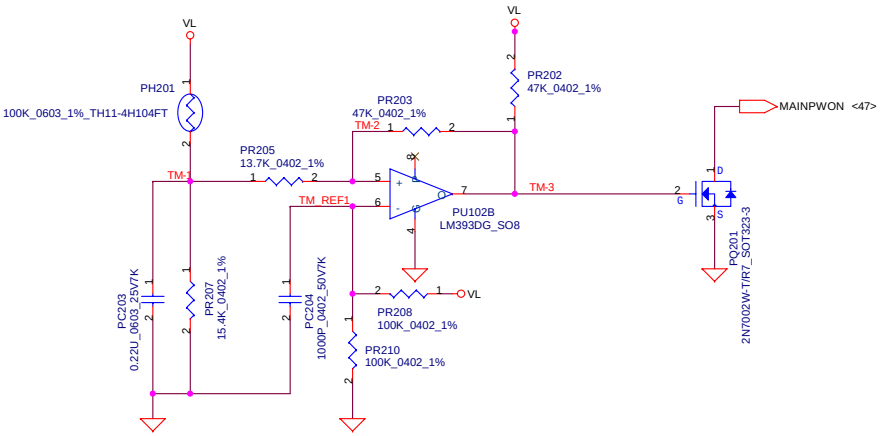
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





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Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number | Rev 0.1

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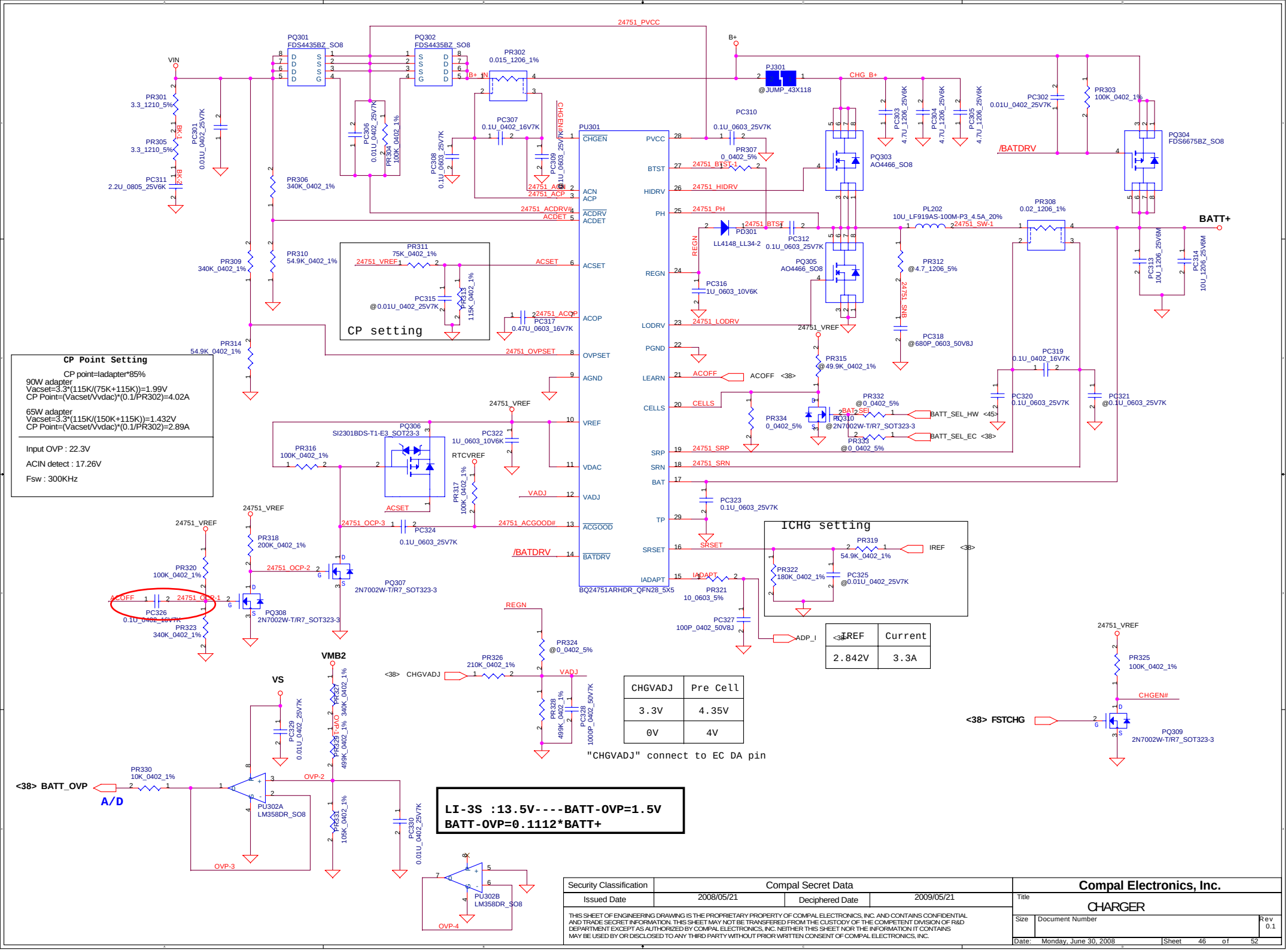

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Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: CHARGER

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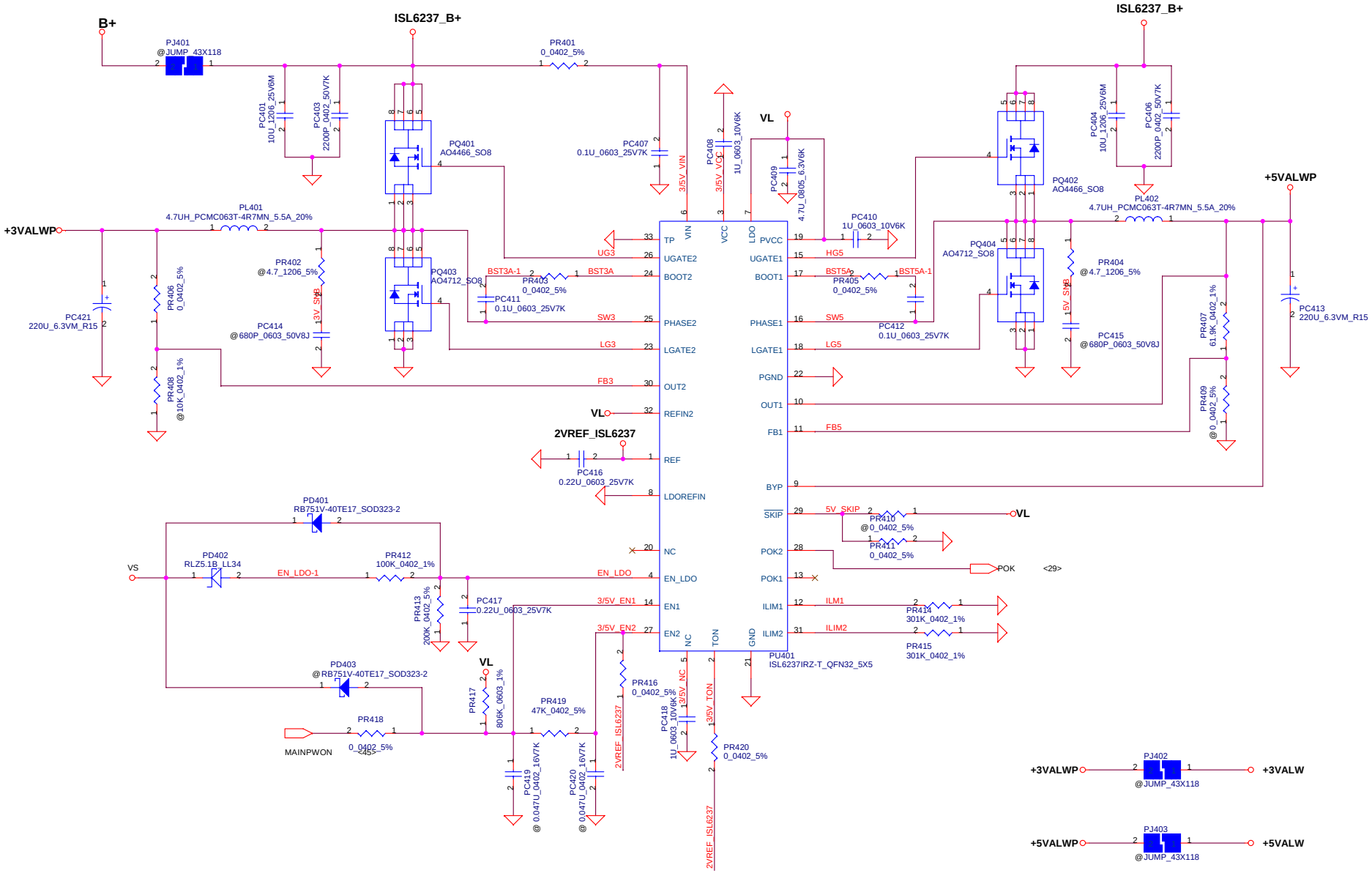
Date: Monday, June 30, 2008 | Sheet 46 of 52



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Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: **3VALW/5VALW**

Size	Document Number	Rev
Custom		0.1

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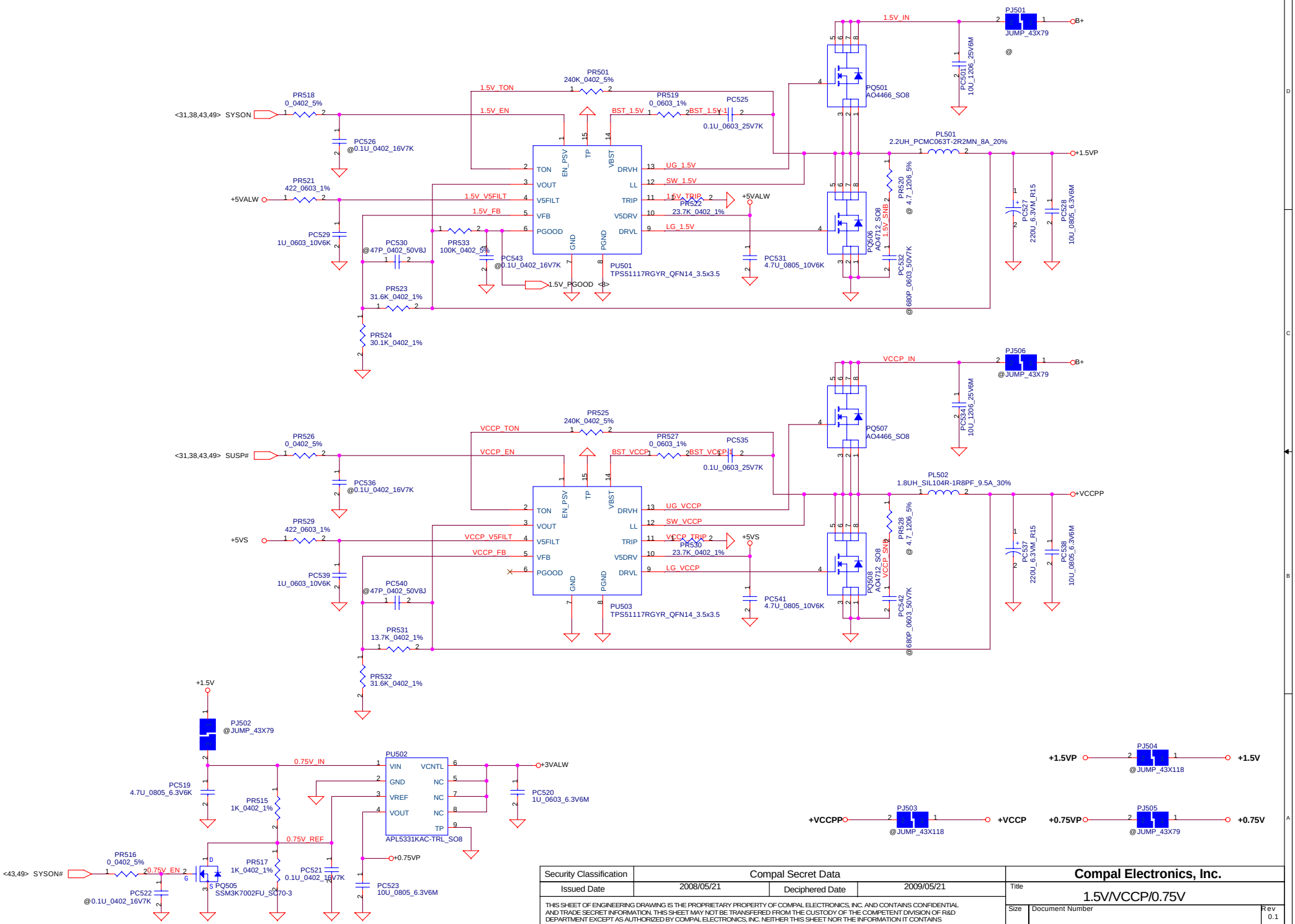

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Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: 1.5V/VCCP/0.75V

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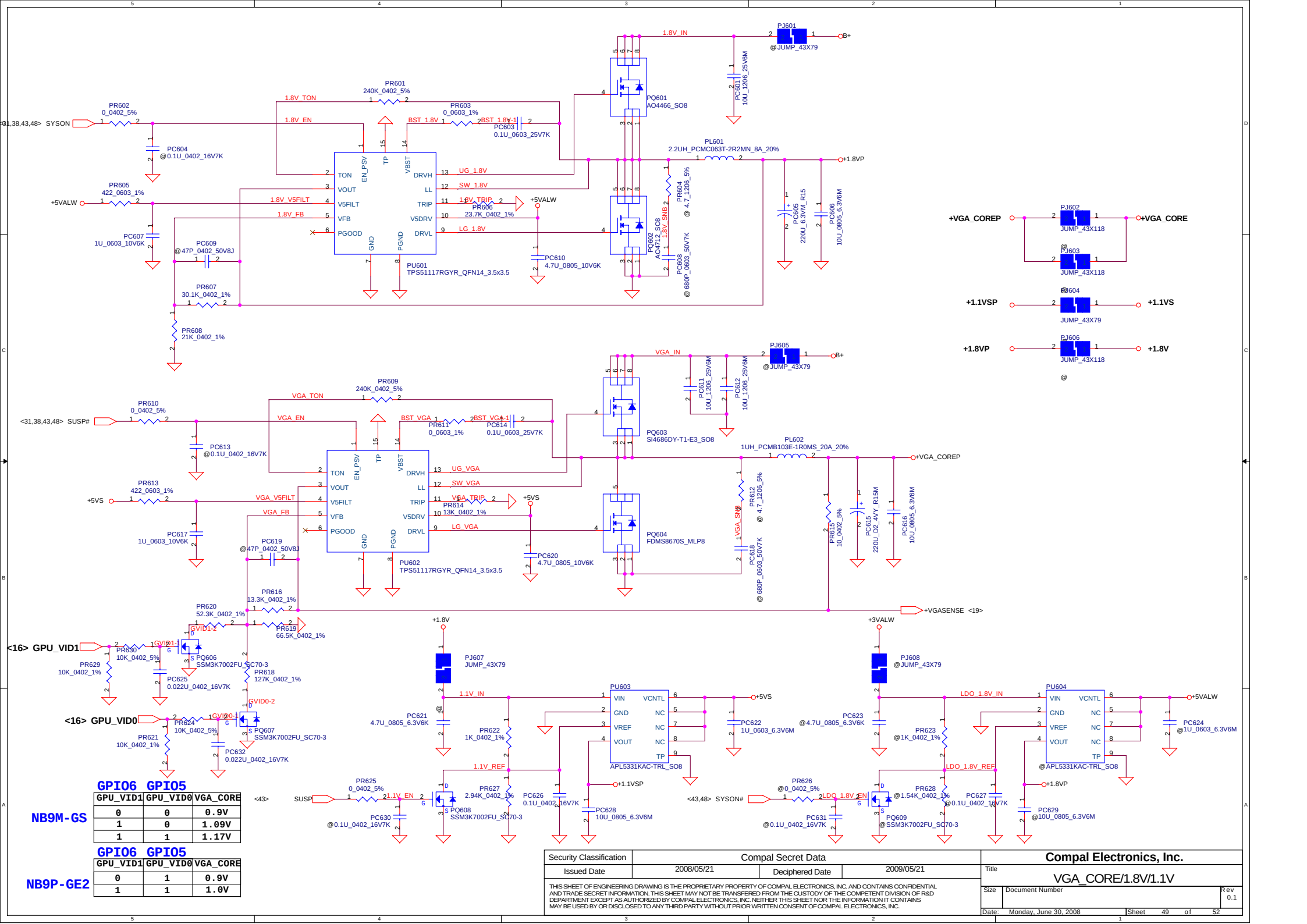

NB9M-GS

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.9V
1	0	1.09V
1	1	1.17V

NB9P-GE2

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	1	0.9V
1	1	1.0V

Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: VGA_CORE/1.8V/1.1V

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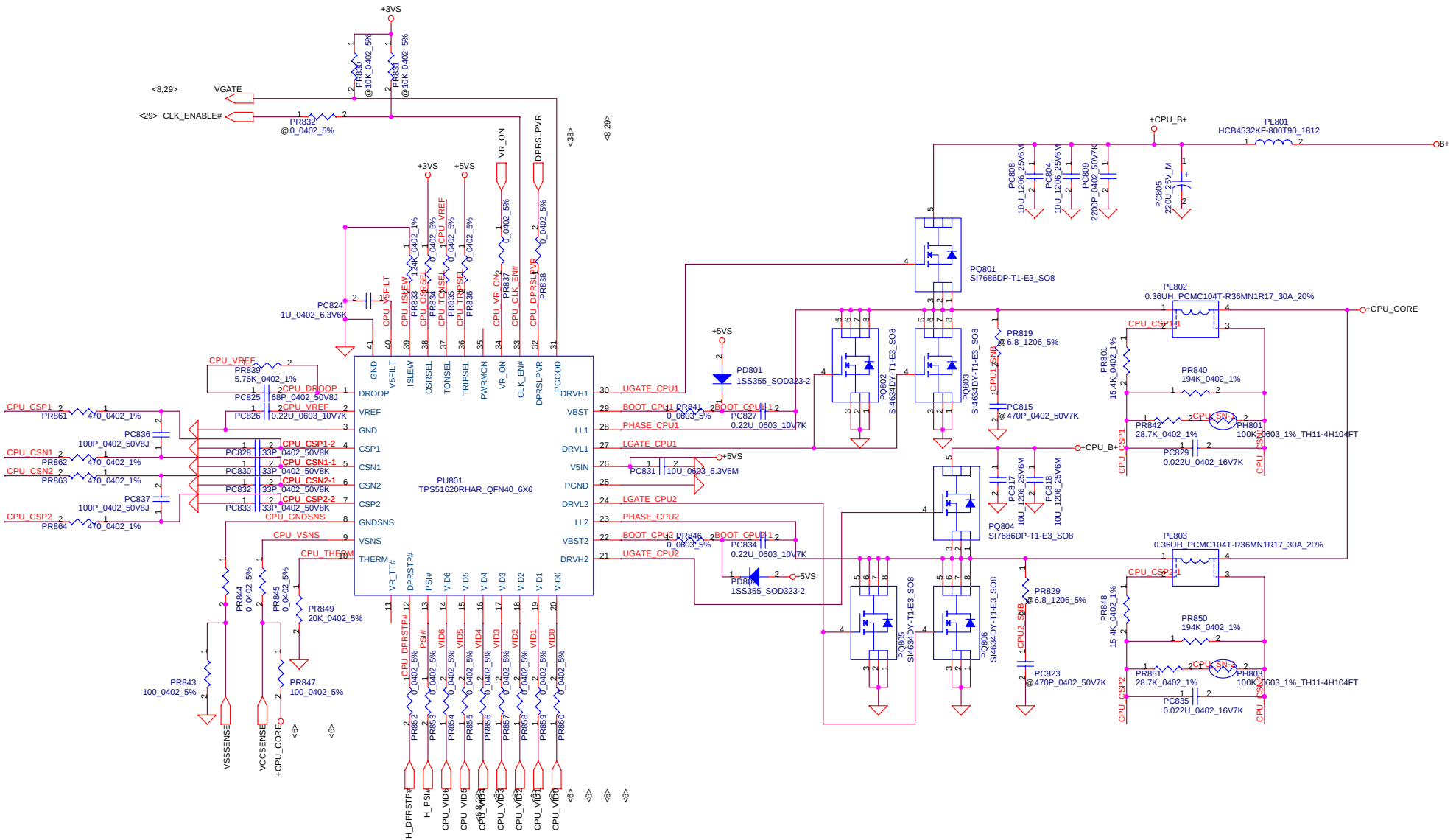

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Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: **+CPU_CORE**

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Custom		0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						20071031	EVT
2						20071115	DVT
3							
4							
5							
6							
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23							

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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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NO DATE PAGE MODIFICATION LIST PURPOSE

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Title: HW PIR		
Size: B	Document Number: KIWB3/B4_LA4551P	Rev: 0.1
Date: Thursday, June 26, 2008	Sheet 52 of 52	