LCFC Confidential

BY511/BY710 M/B Schematics Document

Intel Skylake H-Processor with DDR4 + NV N16P-GX GPU

MB NMA541

2015-07-31

REV:1.0

Security Classification	LC Future Center Secret Data		
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Title: Cover Page		
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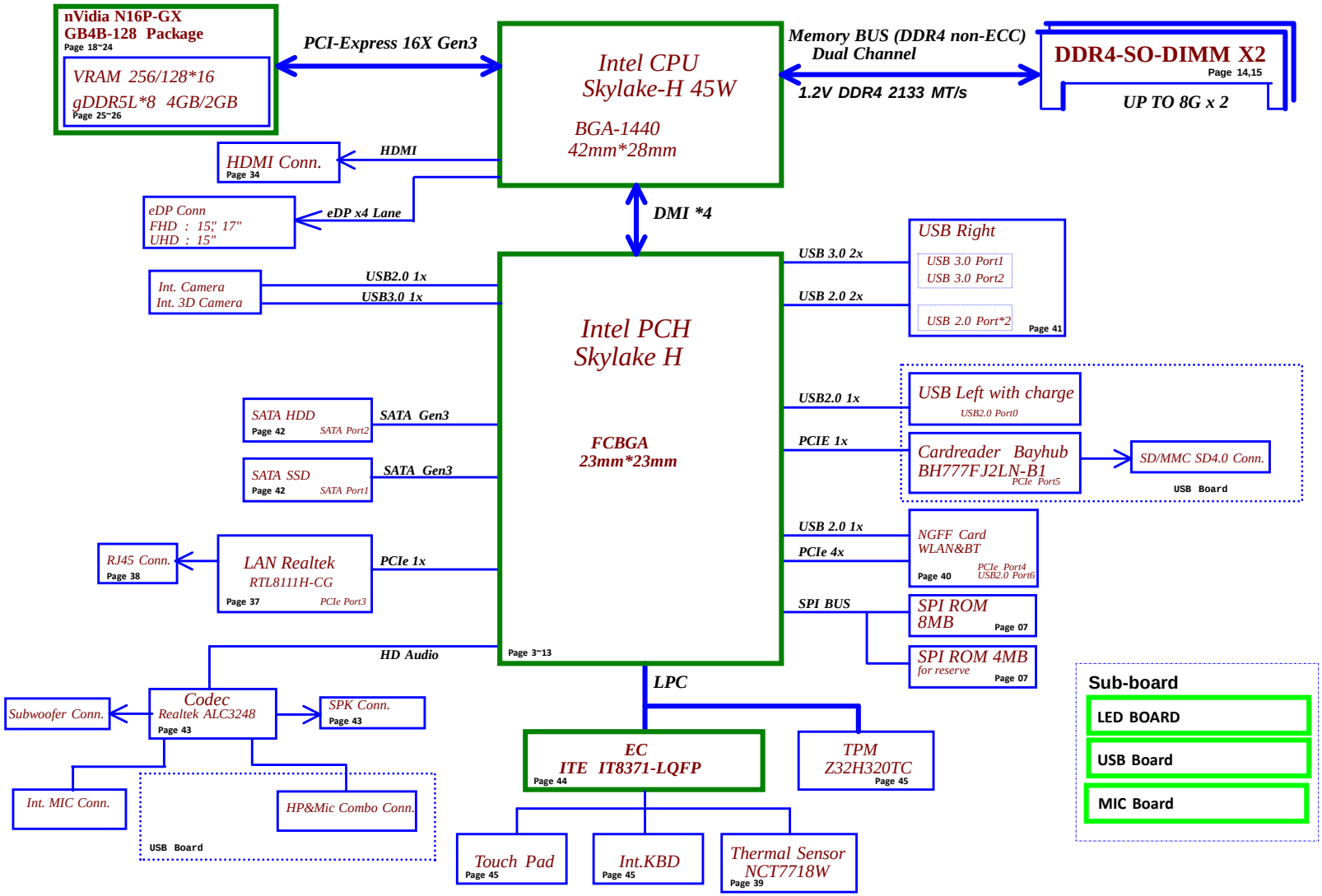

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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS +1.5VS +1.2VS +1.05VS +0.6VS CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB 2.0 Port table

Port	Function
1	RIGHT USB 2.0 (AOU)
2	LEFT USB 3.0 w/ 2.0
3	LEFT USB 3.0 w/ 2.0
4	
5	Touch Screen
6	Camera
7	
8	
9	
10	
11	Buletooth
12	
13	
14	

USB 3.0 Port table

Port	Function
1	LEFT USB 3.0 w/ 2.0
2	LEFT USB 3.0 w/ 2.0
3	
4	
5	
6	3D Camera
7	
8	

PCIE 3.0 Port table

Port	Function
1	
2	SD 4.0 Card Reader
3	WLAN
4	LAN
5	
6	
7	
8	
9	M.2 SSD 4Lanes PCIe
10	M.2 SSD 4Lanes PCIe
11	M.2 SSD 4Lanes PCIe
12	M.2 SSD 4Lanes PCIe
13	
14	
15	
16	

SATA 3.0 Port table

Port	Function
1	M.2 SSD SATA Gen3
2	HDD SATA Gen3
3	
4	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
ME@	ME part(connector, hole)
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
OPT@	For GPU part
TS@	For support touch panel sku part
TPM@	For support TPM sku part
U31@	For support USB re-driver part
3D@	For support 3D camera sku part
H4@	Hynix 256Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
S4GX4@	Samsung 256Mx16 VRAM x4pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
CD@	Cost down part
H4GX8@	Hynix 256Mx16 VRAM x8pcs sku
M4GX8@	Micron 256Mx16 VRAM x8pcs sku
S4GX8@	Samsung 256Mx16 VRAM x8pcs sku

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

Device	
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001_100xb
VGA	0x41(default)
PCH	need to update

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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Title: **Notes List**

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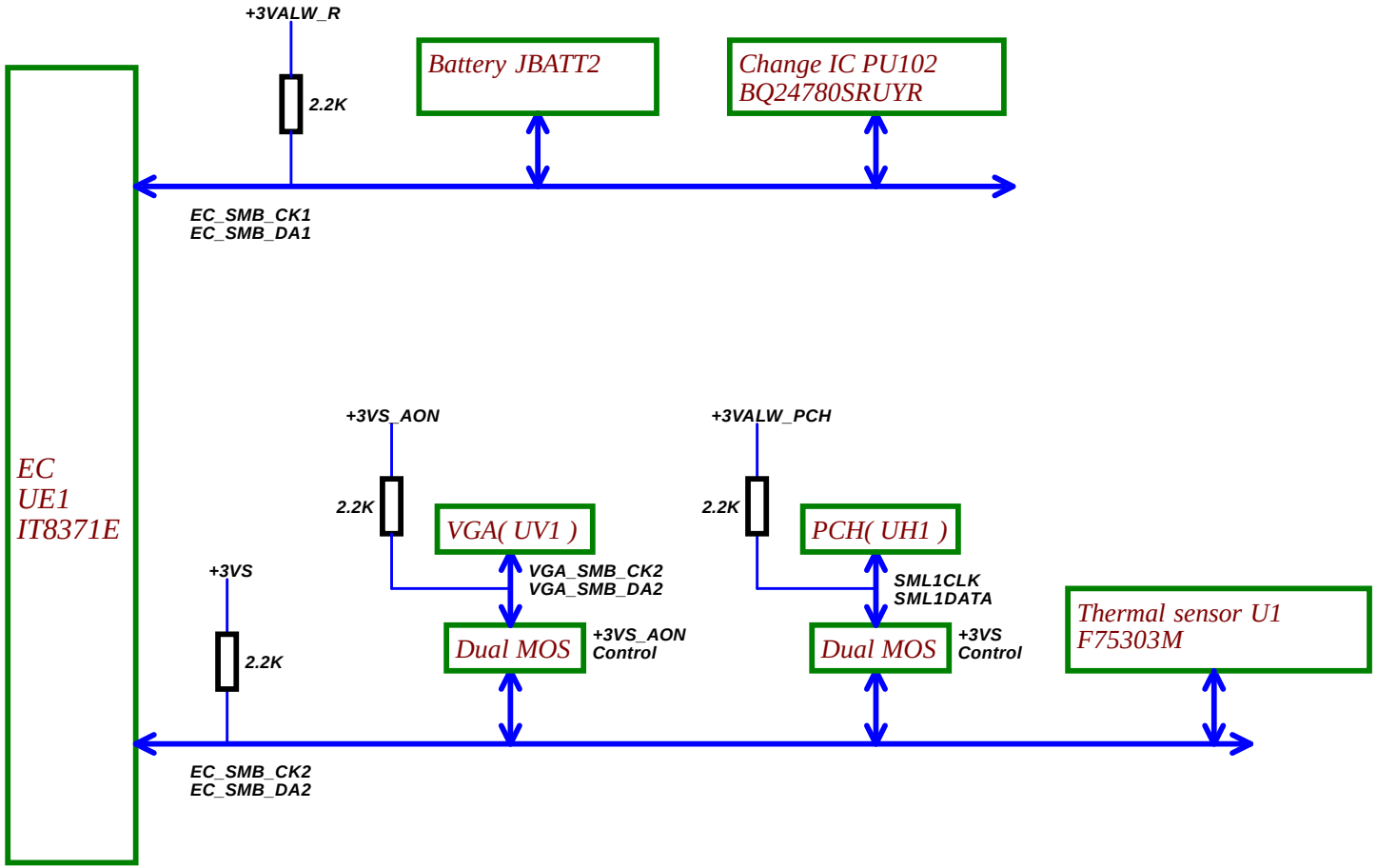

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Title: Blank4

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[24] PCIE_CRX_GTX_N[0..15]

[24] PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] [24]

PCIE_CTX_C_GRX_P[0..15] [24]

VCCIO

PEG_COMP RC1 1 2 24.9 0402 1%

CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

UC1C SKYLAKE_HALO

BGA1440

PCIE_CRX_GTX_P15	E25	PEG_RXP[0]	PEG_TXP[0]	B25	PCIE_CTX_GRX_P15	OPT@	CC32	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P15
PCIE_CRX_GTX_N15	D25	PEG_RXN[0]	PEG_TXN[0]	A25	PCIE_CTX_GRX_N15	OPT@	CC16	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N15
PCIE_CRX_GTX_P14	E24	PEG_RXP[1]	PEG_TXP[1]	B24	PCIE_CTX_GRX_P14	OPT@	CC31	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P14
PCIE_CRX_GTX_N14	F24	PEG_RXN[1]	PEG_TXN[1]	C24	PCIE_CTX_GRX_N14	OPT@	CC15	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N14
PCIE_CRX_GTX_P13	E23	PEG_RXP[2]	PEG_TXP[2]	B23	PCIE_CTX_GRX_P13	OPT@	CC30	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P13
PCIE_CRX_GTX_N13	D23	PEG_RXN[2]	PEG_TXN[2]	A23	PCIE_CTX_GRX_N13	OPT@	CC14	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N13
PCIE_CRX_GTX_P12	E22	PEG_RXP[3]	PEG_TXP[3]	B22	PCIE_CTX_GRX_P12	OPT@	CC29	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P12
PCIE_CRX_GTX_N12	F22	PEG_RXN[3]	PEG_TXN[3]	C22	PCIE_CTX_GRX_N12	OPT@	CC13	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N12
PCIE_CRX_GTX_P11	E21	PEG_RXP[4]	PEG_TXP[4]	B21	PCIE_CTX_GRX_P11	OPT@	CC28	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P11
PCIE_CRX_GTX_N11	D21	PEG_RXN[4]	PEG_TXN[4]	A21	PCIE_CTX_GRX_N11	OPT@	CC12	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N11
PCIE_CRX_GTX_P10	E20	PEG_RXP[5]	PEG_TXP[5]	B20	PCIE_CTX_GRX_P10	OPT@	CC27	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P10
PCIE_CRX_GTX_N10	F20	PEG_RXN[5]	PEG_TXN[5]	C20	PCIE_CTX_GRX_N10	OPT@	CC11	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N10
PCIE_CRX_GTX_P9	E19	PEG_RXP[6]	PEG_TXP[6]	B19	PCIE_CTX_GRX_P9	OPT@	CC26	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P9
PCIE_CRX_GTX_N9	D19	PEG_RXN[6]	PEG_TXN[6]	A19	PCIE_CTX_GRX_N9	OPT@	CC10	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N9
PCIE_CRX_GTX_P8	E18	PEG_RXP[7]	PEG_TXP[7]	B18	PCIE_CTX_GRX_P8	OPT@	CC25	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P8
PCIE_CRX_GTX_N8	F18	PEG_RXN[7]	PEG_TXN[7]	C18	PCIE_CTX_GRX_N8	OPT@	CC9	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N8
PCIE_CRX_GTX_P7	D17	PEG_RXP[8]	PEG_TXP[8]	A17	PCIE_CTX_GRX_P7	OPT@	CC24	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P7
PCIE_CRX_GTX_N7	E17	PEG_RXN[8]	PEG_TXN[8]	B17	PCIE_CTX_GRX_N7	OPT@	CC8	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N7
PCIE_CRX_GTX_P6	E16	PEG_RXP[9]	PEG_TXP[9]	C16	PCIE_CTX_GRX_P6	OPT@	CC23	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P6
PCIE_CRX_GTX_N6	E16	PEG_RXN[9]	PEG_TXN[9]	B16	PCIE_CTX_GRX_N6	OPT@	CC7	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N6
PCIE_CRX_GTX_P5	D15	PEG_RXP[10]	PEG_TXP[10]	A15	PCIE_CTX_GRX_P5	OPT@	CC22	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P5
PCIE_CRX_GTX_N5	E15	PEG_RXN[10]	PEG_TXN[10]	B15	PCIE_CTX_GRX_N5	OPT@	CC6	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N5
PCIE_CRX_GTX_P4	E14	PEG_RXP[11]	PEG_TXP[11]	C14	PCIE_CTX_GRX_P4	OPT@	CC21	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P4
PCIE_CRX_GTX_N4	E14	PEG_RXN[11]	PEG_TXN[11]	B14	PCIE_CTX_GRX_N4	OPT@	CC5	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N4
PCIE_CRX_GTX_P3	D13	PEG_RXP[12]	PEG_TXP[12]	A13	PCIE_CTX_GRX_P3	OPT@	CC20	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P3
PCIE_CRX_GTX_N3	E13	PEG_RXN[12]	PEG_TXN[12]	B13	PCIE_CTX_GRX_N3	OPT@	CC4	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N3
PCIE_CRX_GTX_P2	E12	PEG_RXP[13]	PEG_TXP[13]	C12	PCIE_CTX_GRX_P2	OPT@	CC19	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P2
PCIE_CRX_GTX_N2	E12	PEG_RXN[13]	PEG_TXN[13]	B12	PCIE_CTX_GRX_N2	OPT@	CC3	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N2
PCIE_CRX_GTX_P1	D11	PEG_RXP[14]	PEG_TXP[14]	A11	PCIE_CTX_GRX_P1	OPT@	CC18	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P1
PCIE_CRX_GTX_N1	E11	PEG_RXN[14]	PEG_TXN[14]	B11	PCIE_CTX_GRX_N1	OPT@	CC2	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N1
PCIE_CRX_GTX_P0	E10	PEG_RXP[15]	PEG_TXP[15]	C10	PCIE_CTX_GRX_P0	OPT@	CC17	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_P0
PCIE_CRX_GTX_N0	E10	PEG_RXN[15]	PEG_TXN[15]	B10	PCIE_CTX_GRX_N0	OPT@	CC1	1	2	0.22U 0402 10V6K	PCIE_CTX_C_GRX_N0

PEG_COMP G2 PEG_RCOMP

[19] DMI_CRX_PTX_P0	DMI_CRX_PTX_P0 D8	DMI_RXP[0]	DMI_TXP[0]	B8 DMI_CTX_PRX_P0	DMI_CTX_PRX_P0	[19] DMI_CTX_PRX_P0 [19]
[19] DMI_CRX_PTX_N0	DMI_CRX_PTX_N0 E8	DMI_RXN[0]	DMI_TXN[0]	A8 DMI_CTX_PRX_N0	DMI_CTX_PRX_N0	[19] DMI_CTX_PRX_N0 [19]
[19] DMI_CRX_PTX_P1	DMI_CRX_PTX_P1 E6	DMI_RXP[1]	DMI_TXP[1]	C6 DMI_CTX_PRX_P1	DMI_CTX_PRX_P1	[19] DMI_CTX_PRX_P1 [19]
[19] DMI_CRX_PTX_N1	DMI_CRX_PTX_N1 F6	DMI_RXN[1]	DMI_TXN[1]	B6 DMI_CTX_PRX_N1	DMI_CTX_PRX_N1	[19] DMI_CTX_PRX_N1 [19]
[19] DMI_CRX_PTX_P2	DMI_CRX_PTX_P2 D5	DMI_RXP[2]	DMI_TXP[2]	B5 DMI_CTX_PRX_P2	DMI_CTX_PRX_P2	[19] DMI_CTX_PRX_P2 [19]
[19] DMI_CRX_PTX_N2	DMI_CRX_PTX_N2 E5	DMI_RXN[2]	DMI_TXN[2]	A5 DMI_CTX_PRX_N2	DMI_CTX_PRX_N2	[19] DMI_CTX_PRX_N2 [19]
[19] DMI_CRX_PTX_P3	DMI_CRX_PTX_P3 J8	DMI_RXP[3]	DMI_TXP[3]	D4 DMI_CTX_PRX_P3	DMI_CTX_PRX_P3	[19] DMI_CTX_PRX_P3 [19]
[19] DMI_CRX_PTX_N3	DMI_CRX_PTX_N3 J9	DMI_RXN[3]	DMI_TXN[3]	B4 DMI_CTX_PRX_N3	DMI_CTX_PRX_N3	[19] DMI_CTX_PRX_N3 [19]

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SKYLAKE-H-CPU_BGA1440

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Title: **CPU (1/7) DMI,PEG**

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Change RC28,RC29,RC15,RC13,RC16,RC17 to R-Short

CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* — 1 = (Default) Normal Operation; No stall. — 0 = Stall.

Reserved configuration lane.	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal.	
CFG2	— 1 = Normal operation * — 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	— 1 = Disabled. * — 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	— 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* * — 11 = 1 x16 PCI Express*

PEG Training	
CFG7	* — 1 = (default) PEG Train immediately following RESET# deassertion. — 0 = PEG Wait for BIOS for training.

Need confirm with Intel if this reserved circuit can be deleted.

Reserved configuration lane.	
CFG[19:8]	N/A

20150527_Mount RC176 to enable DCI function

20150729
1. Change R10022 and R9994 to SD02810028J

Change RC22 to 0ohm jump after SDV phase

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Title: CPU (2/7) PM, XDP, CLK, CFG

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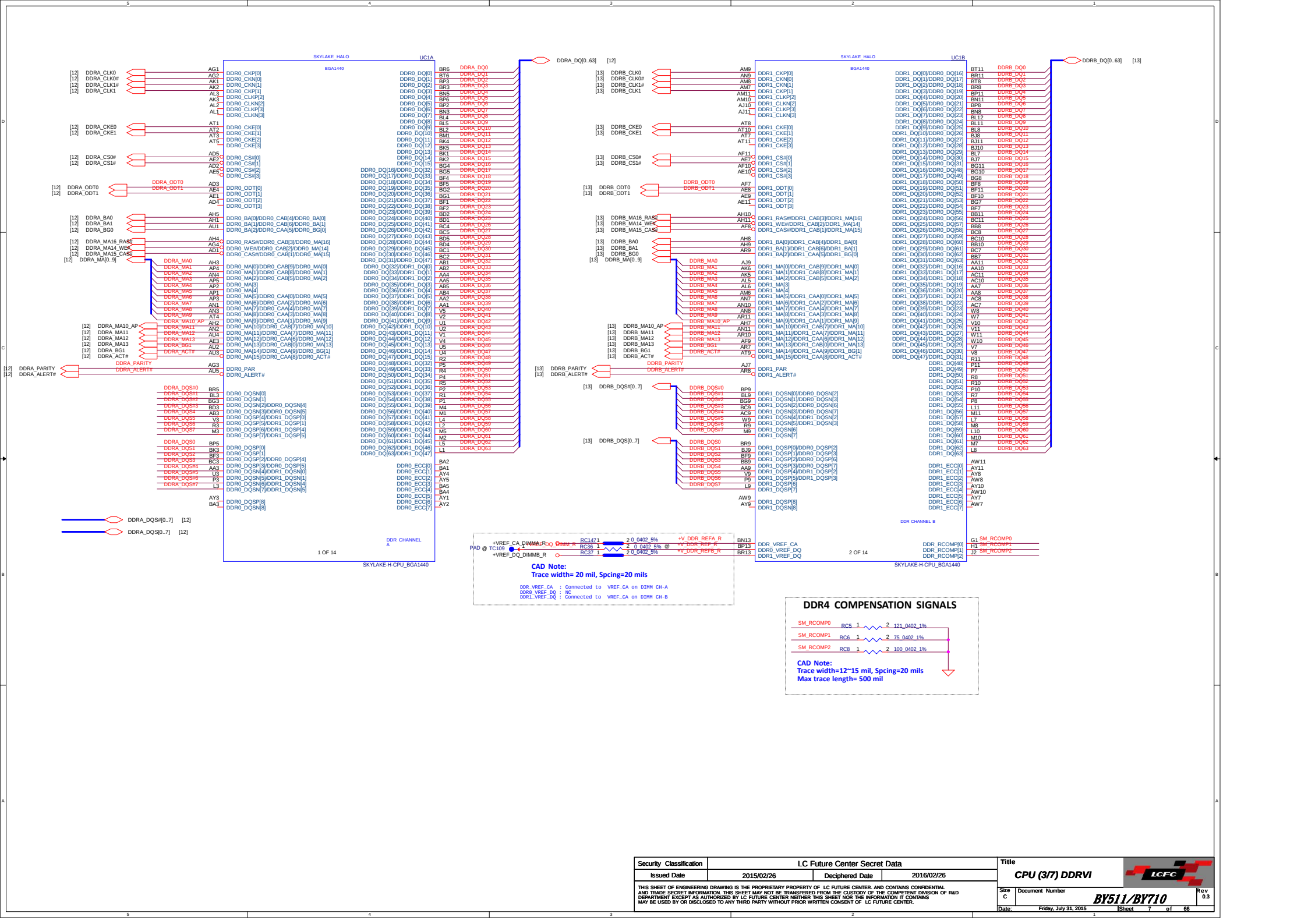

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	BY511/BY710	0.3

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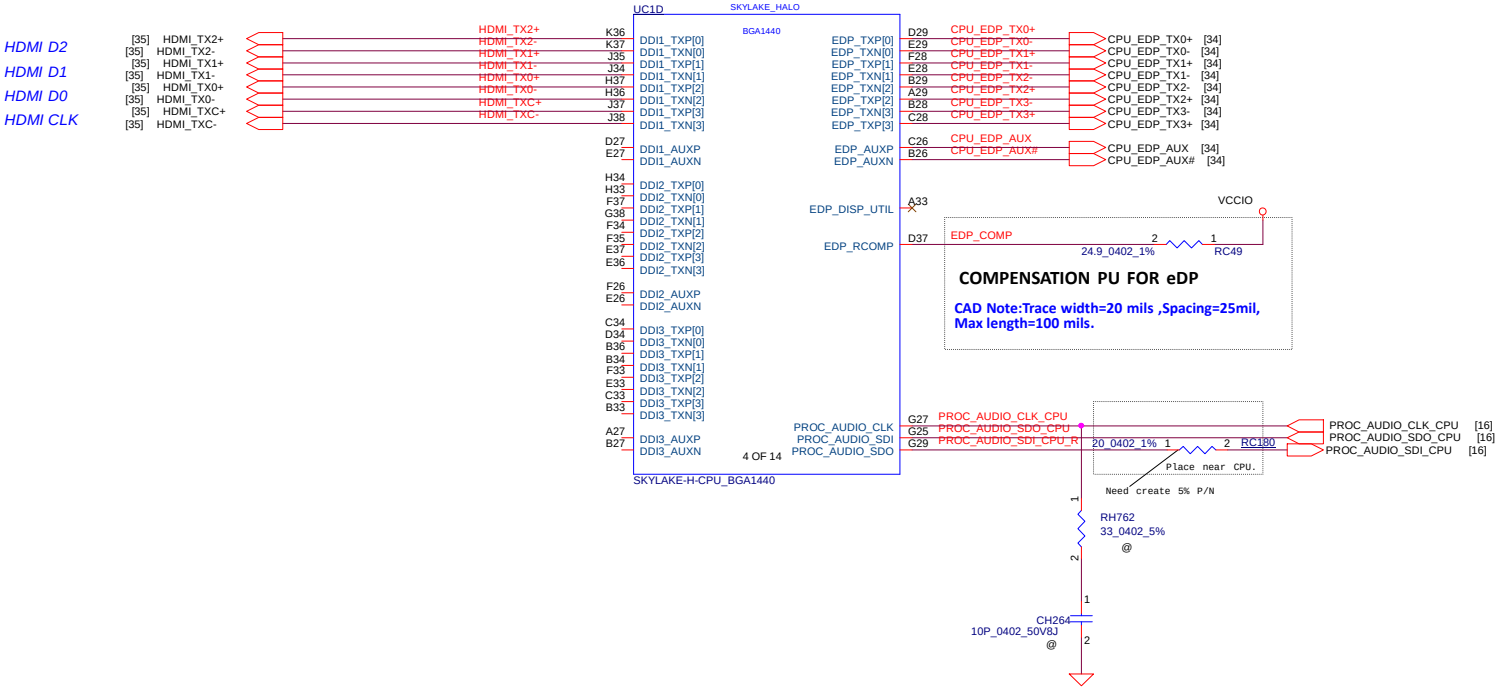

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
Custom	BY511/BY710	0.3

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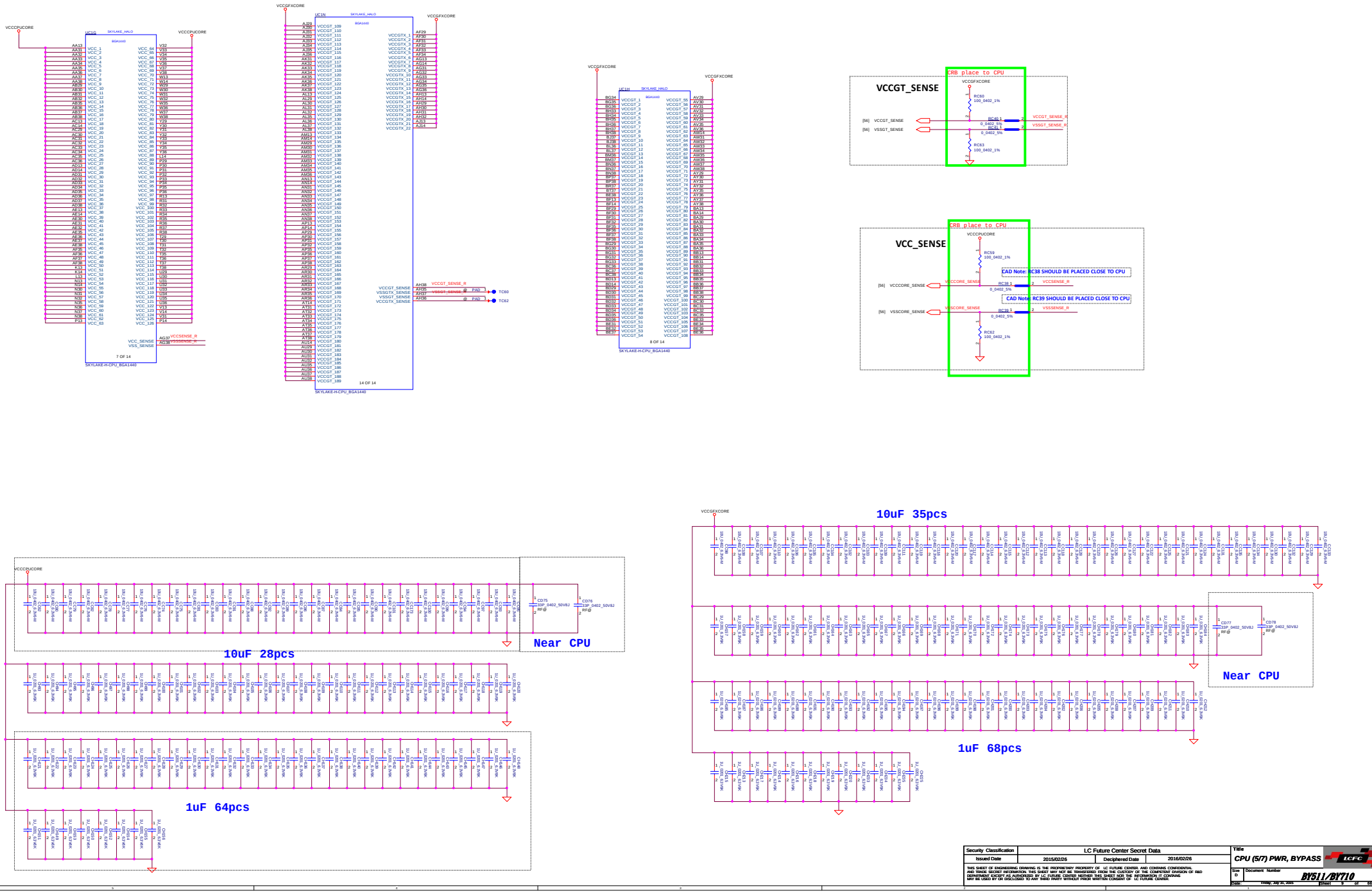

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Title	CPU (5/7) PWR, BYPASS		
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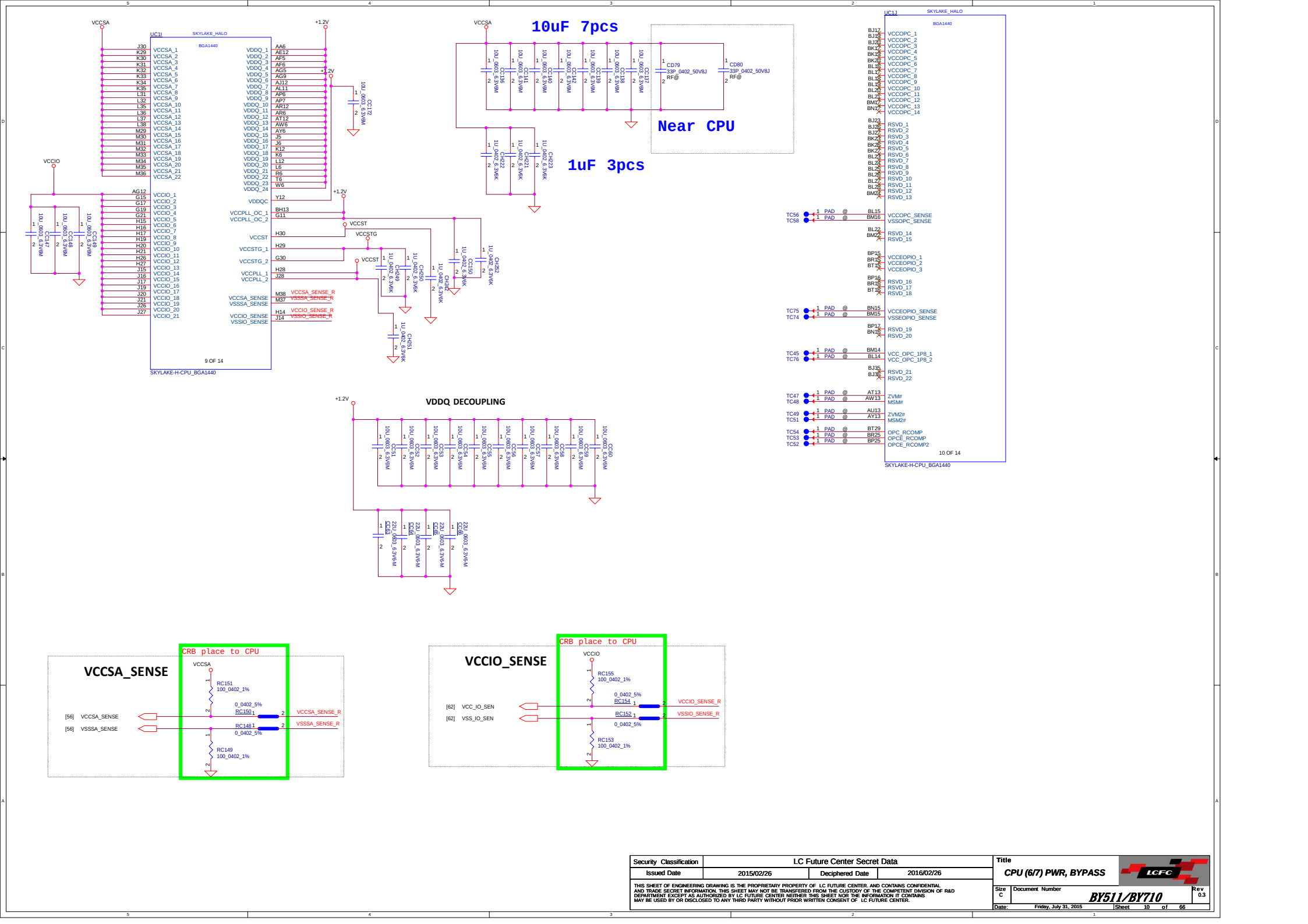

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Title: CPU (6/7) PWR, BYPASS

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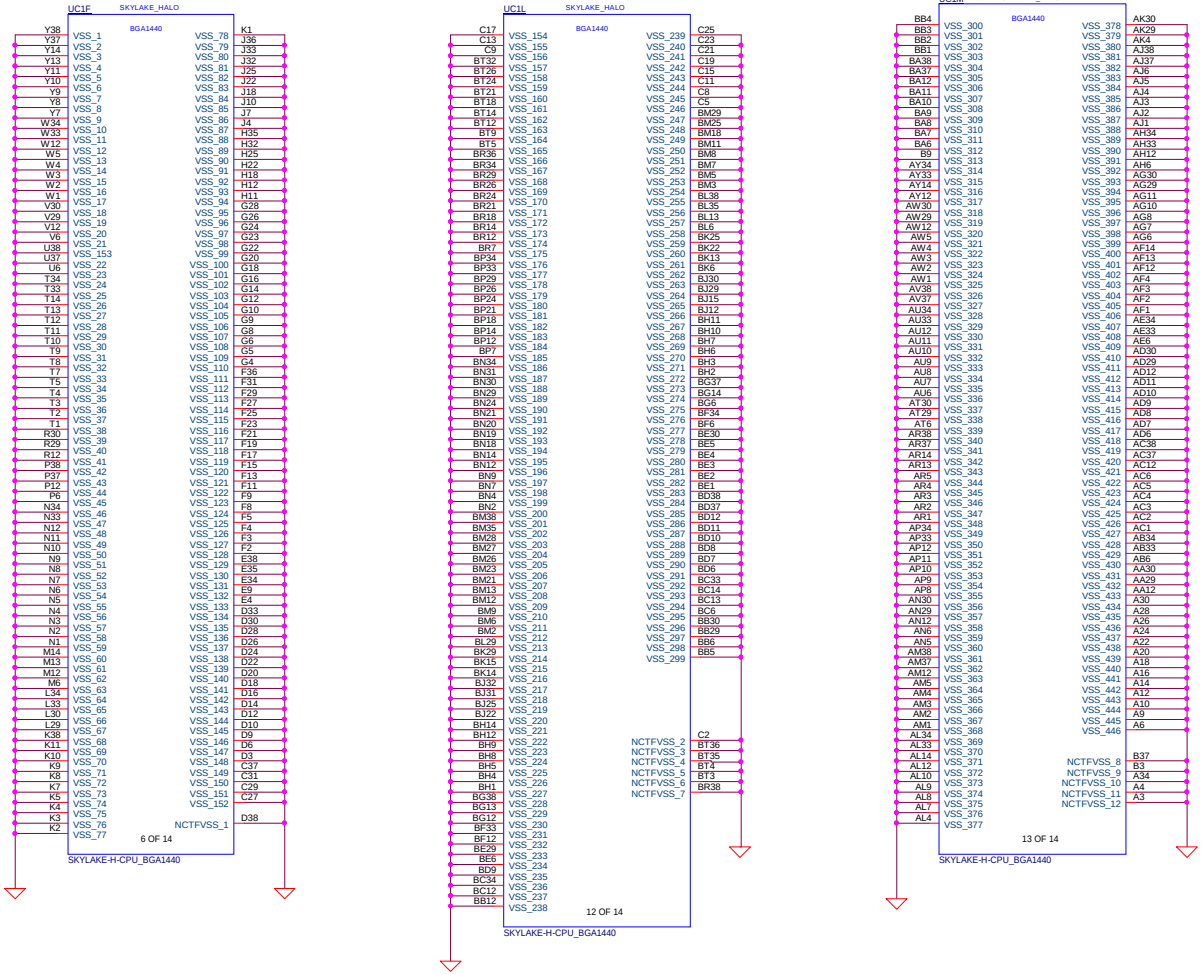

Title: **CPU (6/7) PWR, VSS**

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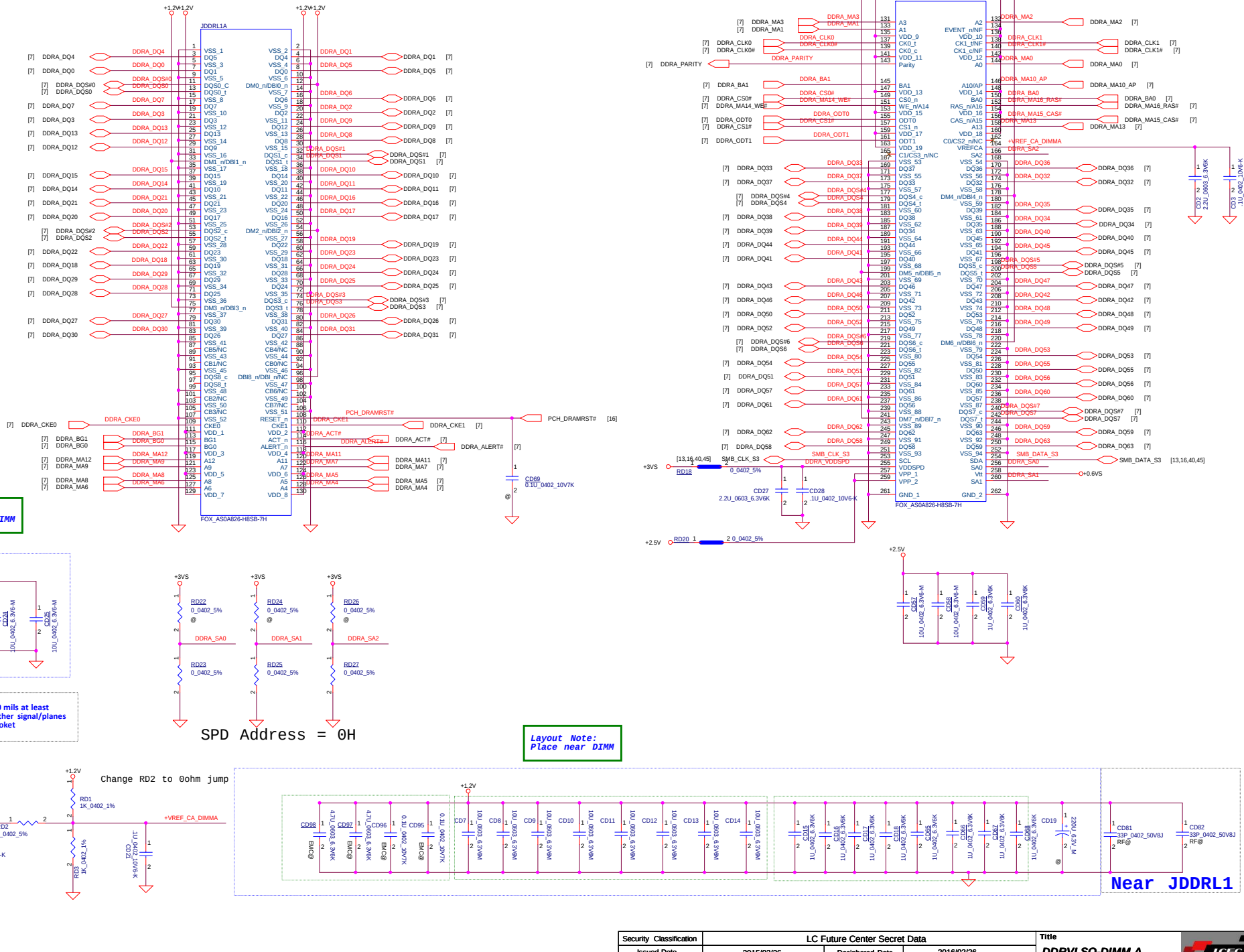
DDR4 SO-DIMM A



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	DDRVI SO-DIMM A		
Size C	Document Number	BY511/BY710	Rev 0.3
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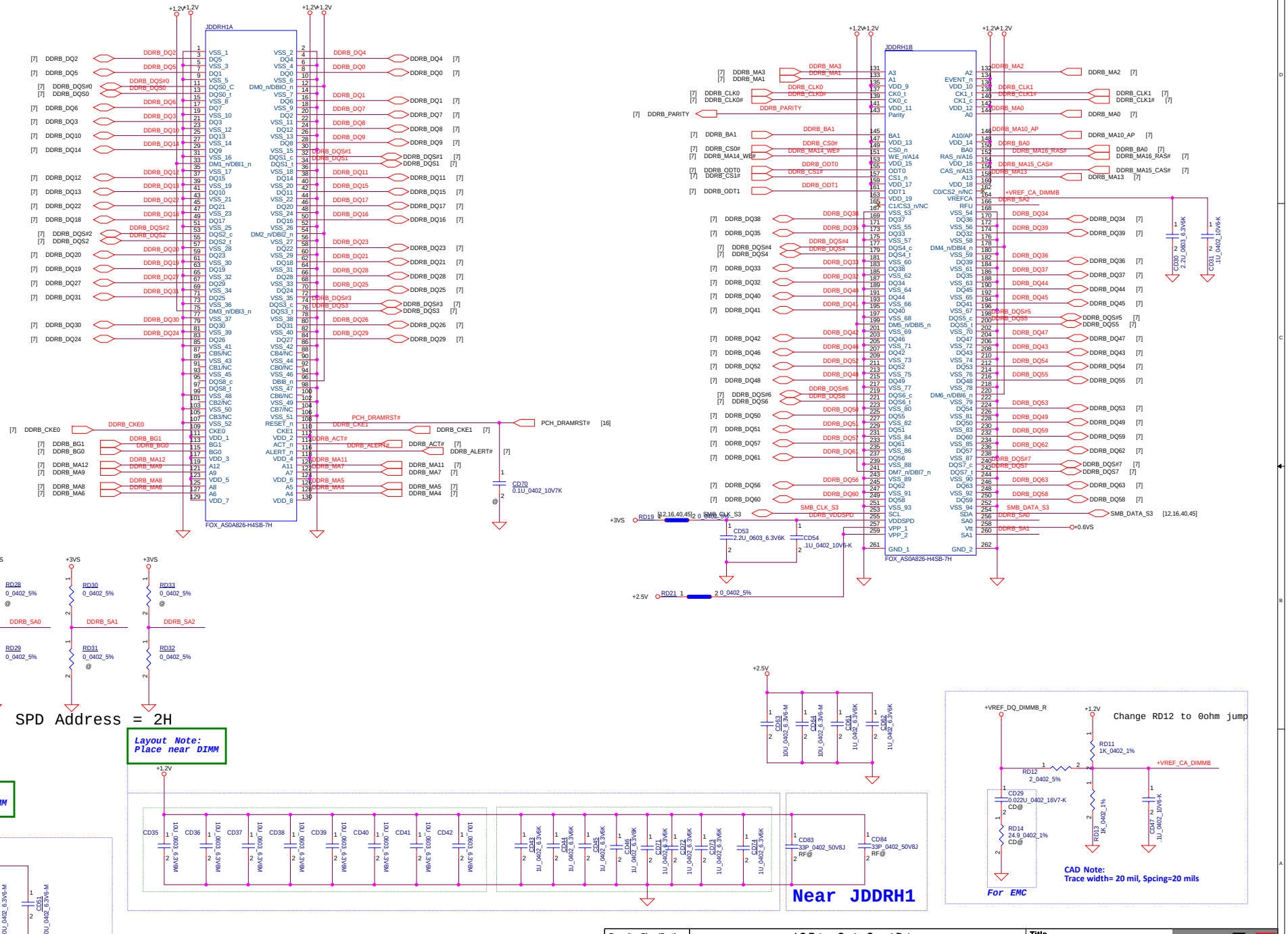
DDR4 SO-DIMM B



SPD Address = 2H

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

Near JDDRH1

Change RD12 to 0ohm jump

CAD Note:
Trace width= 20 mil, Spcing=20 mils

For EMC

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Title	DDRVI SO-DIMM B		
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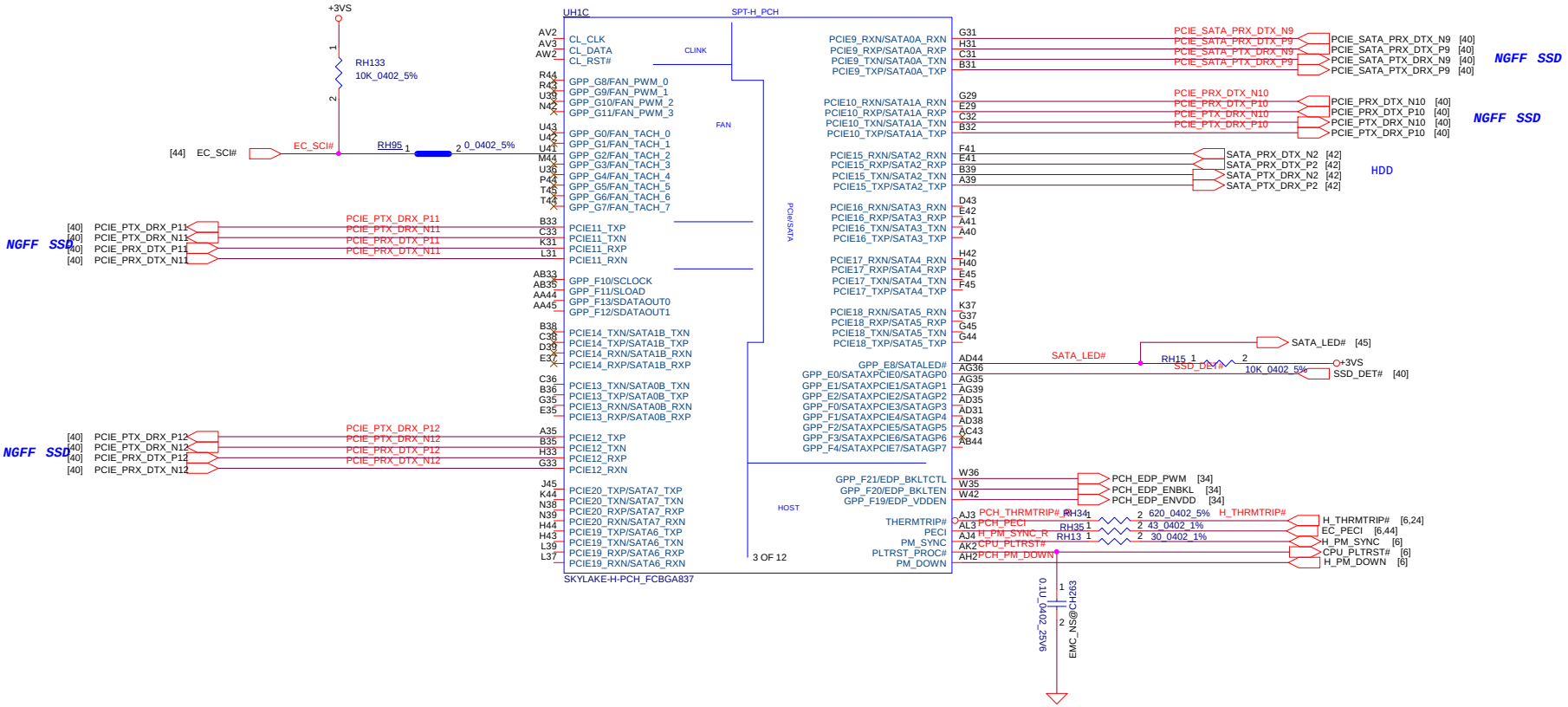


Table 1-2. PCH-H SKUs

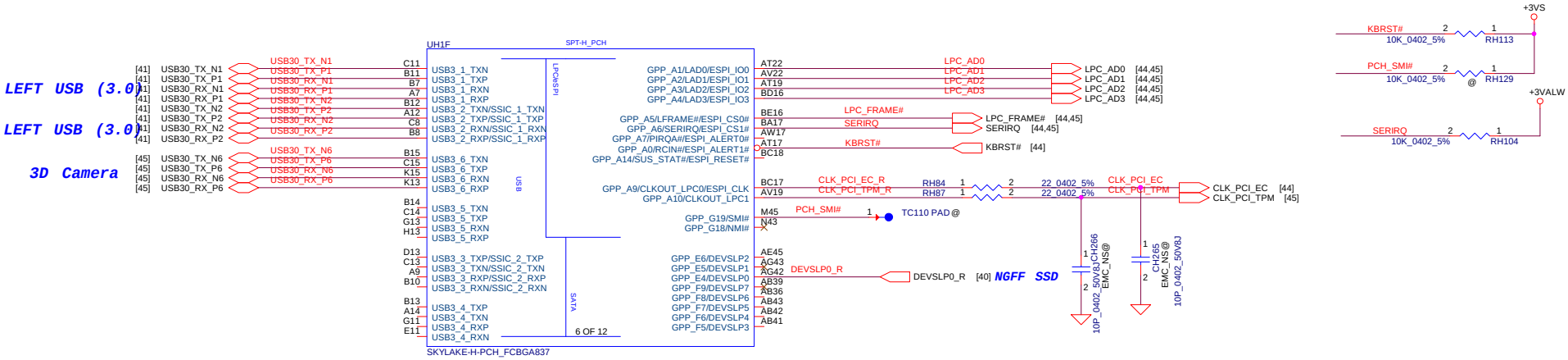
Features	H110	H170	HM170	QM170	Z170	B150	Q150	Q170
Intel® Rapid Storage Technology	AHCI Only	Full Features	Full Features	Full Features	Full Features	AHCI Only	AHCI Only	Full Features
Total USB 3.0 Ports	4	8	8	8	10	6	8	10
Total USB 2.0 Ports	10[1]	14[3]	12[2]	12[2]	14[3]	12[2]	14[3]	14[3]
Total SATA 3.0 Ports (Max 6 Gb/s)	4	6	4	4	6	6	6	6
Total PCI Express* Lanes (Gen)	6 (2.0)	16 (3.0)	16 (3.0)	16 (3.0)	20 (3.0)	8 (3.0)	10 (3.0)	20 (3.0)
Total SATA Express Capable Ports (x2)	0	2	2	2	3	1	1	3
Total Intel® RST for PCIe Storage Devices (M.2 or SATA Express)	0	2	2	2	3	0	0	3
SKL Processor dgfx bifurcation support	No	No	Yes[4]	Yes[4]	Yes[4]	No	No	Yes[4]

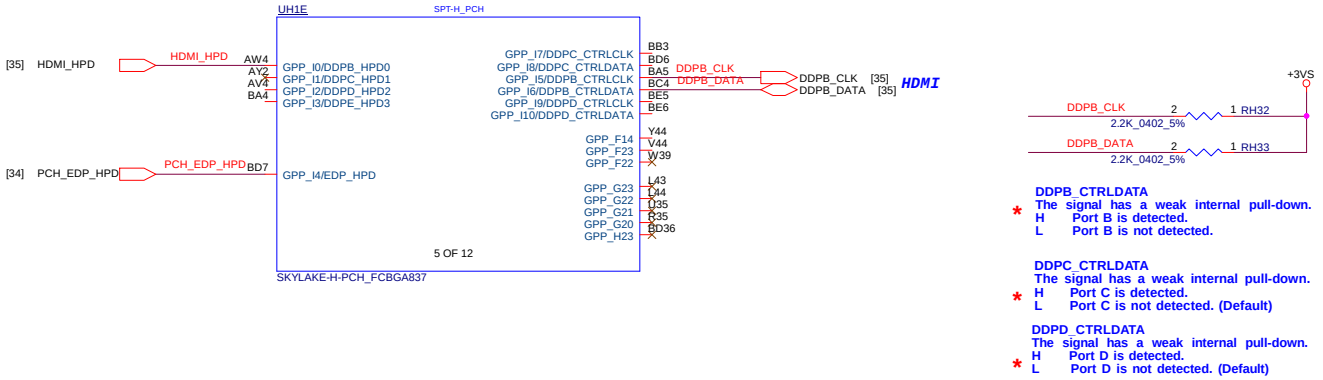
Notes:
1. USB 2.0 port numbers: 1-10
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. PCIe configuration 1x16, or 2x8 or 2x4 or 1x8 are supported.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PCH (1/9) PCIe/SATA/GPPFG**

Size	Document Number	Rev
Custom	BY511/BY710	0.3
Date: Friday, July 31, 2015	Sheet 14 of 66	

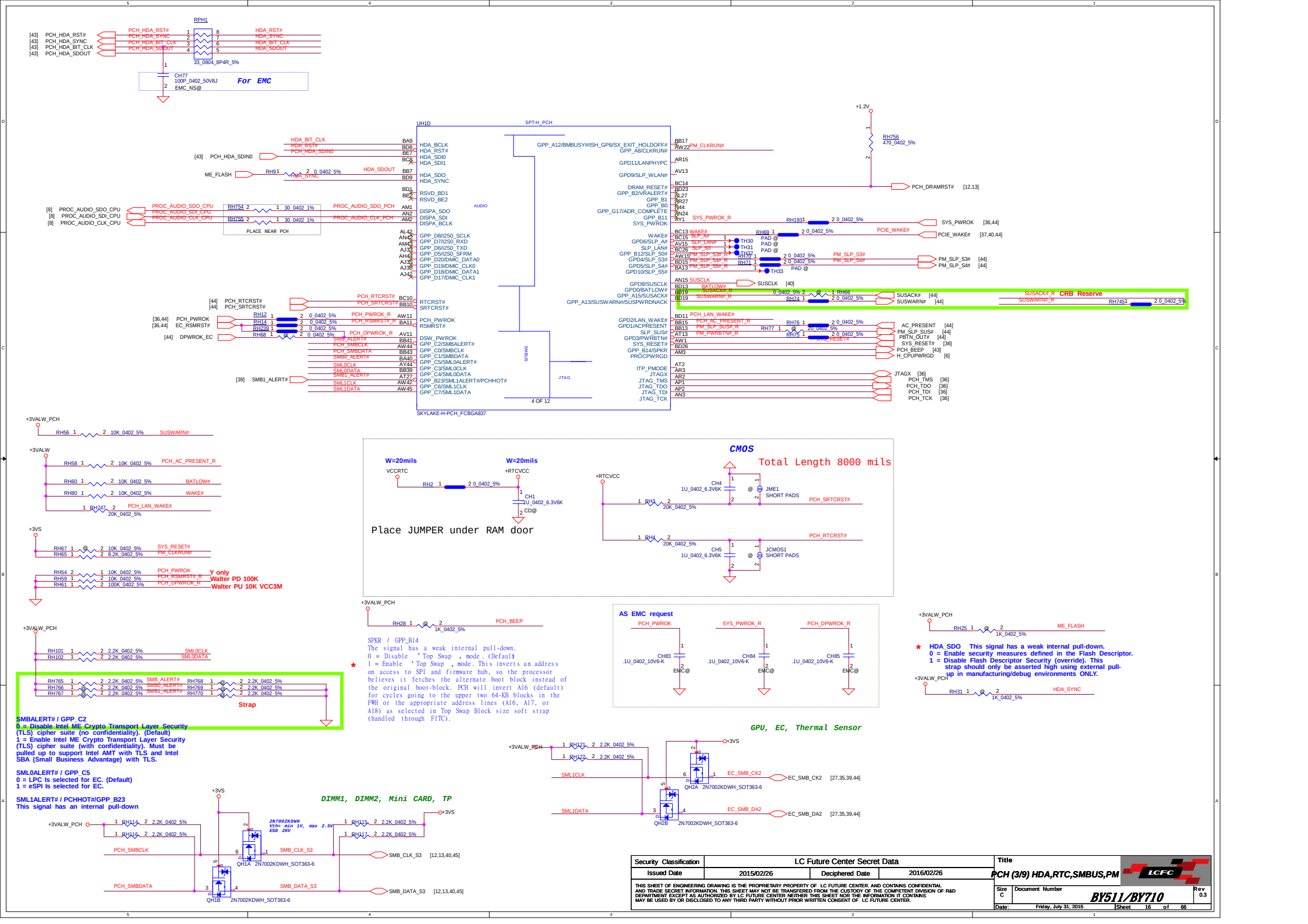




Title: PCH (2/9) USB3/GPPAEFGHI

Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 15 of 66


RPH1
33_0804_8P4R_5%
For EMC
UH1D
SPT-H_PCH
SKYLAKE-H-PCH_FCBGA837
4 OF 12
AUDIO
SMBUS
JTAG
PLACE NEAR PCH
CRB Reserve
CMOS
Total Length 8000 mils
W=20mils
W=20mils
Place JUMPER under RAM door
Y only
Walter PD 100K
Walter PU 10K VCC3M
Strap
SMBALERT# / GPP_C2
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
SML0ALERT# / GPP_C5
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
SML1ALERT# / PCHHOT#/GPP_B23
This signal has an internal pull-down
SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).
AS EMC request
HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
GPU, EC, Thermal Sensor
DIMM1, DIMM2, Mini CARD, TP
2N7002KDWH Vth= min 1V, max 2.5V ESD 2kV
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
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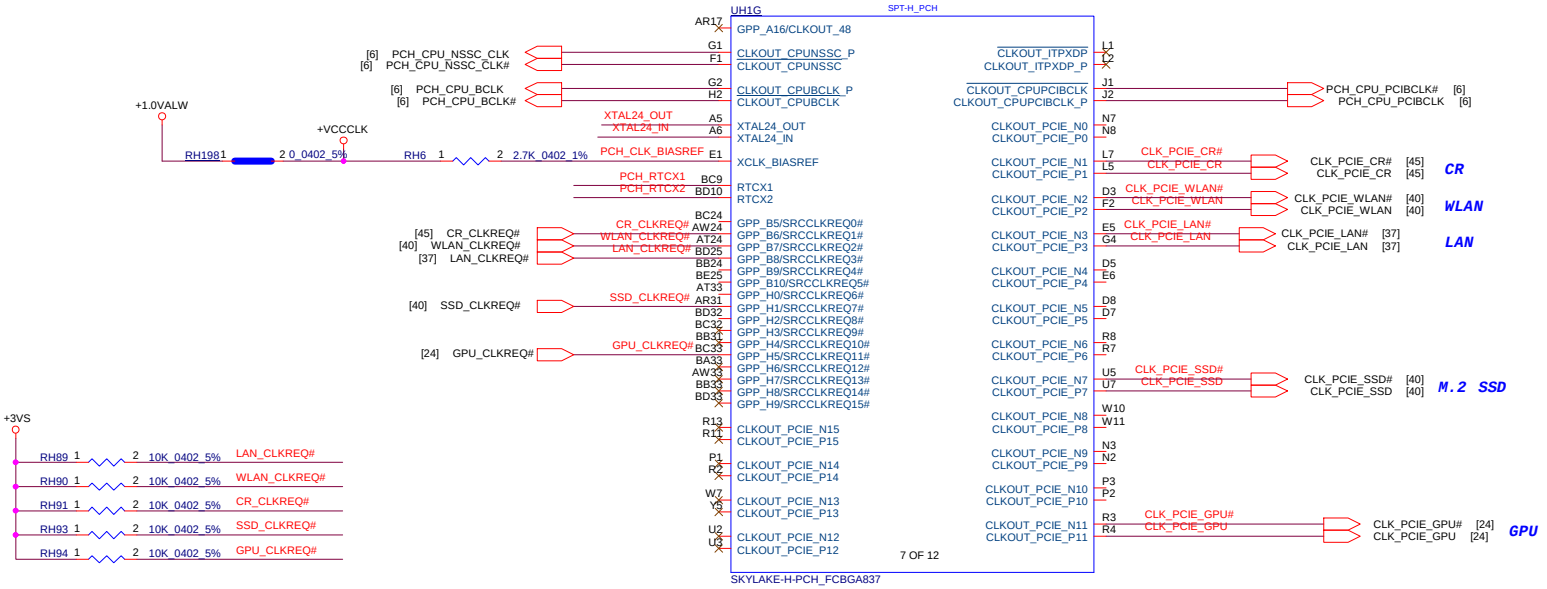
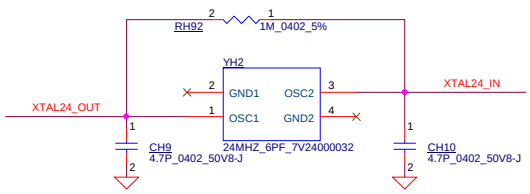
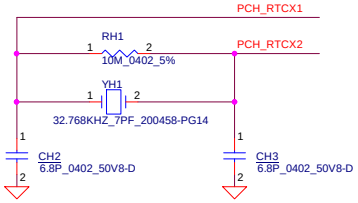
Title
PCH (3/9) HDA,RTC,SMBUS,PM
Size C
Document Number
BY511/BY710
Rev 0.3
Date: Friday, July 31, 2015
Sheet 16 of 66





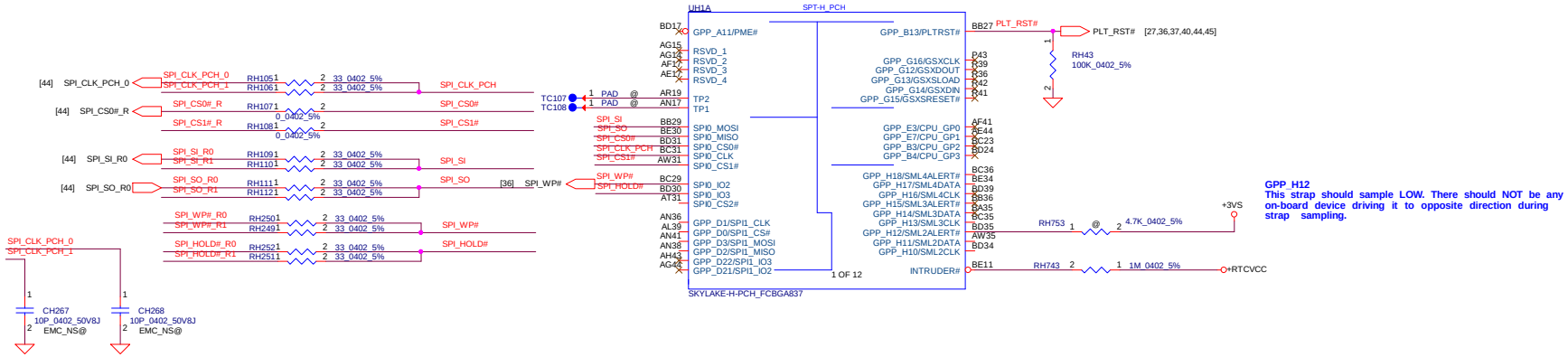


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (3/9) CLOCK,GPPBH

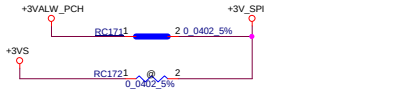
Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 17 of 66

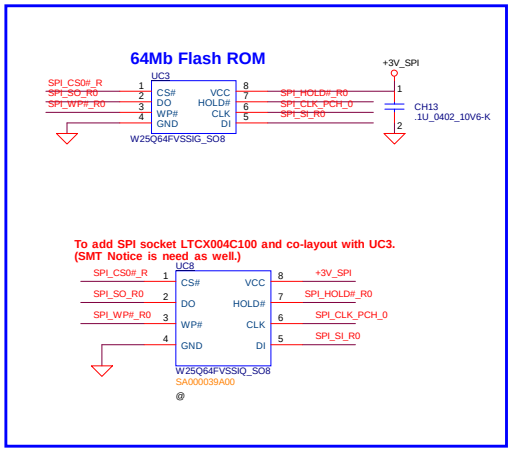


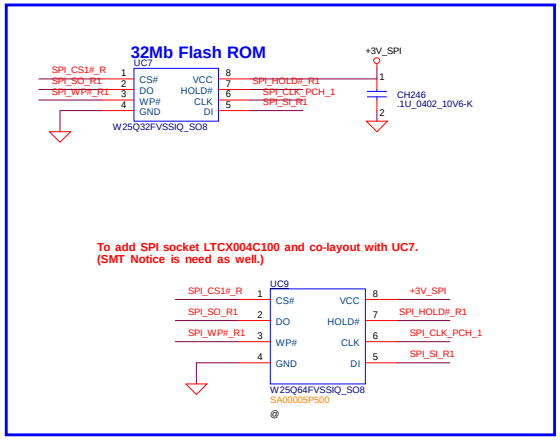
GPP_H12
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

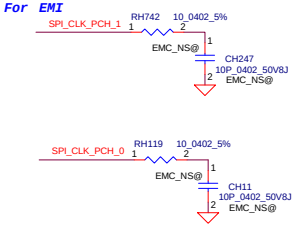
SPI0_MOSI
SPI0_MISO
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



+3V_SPI
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.





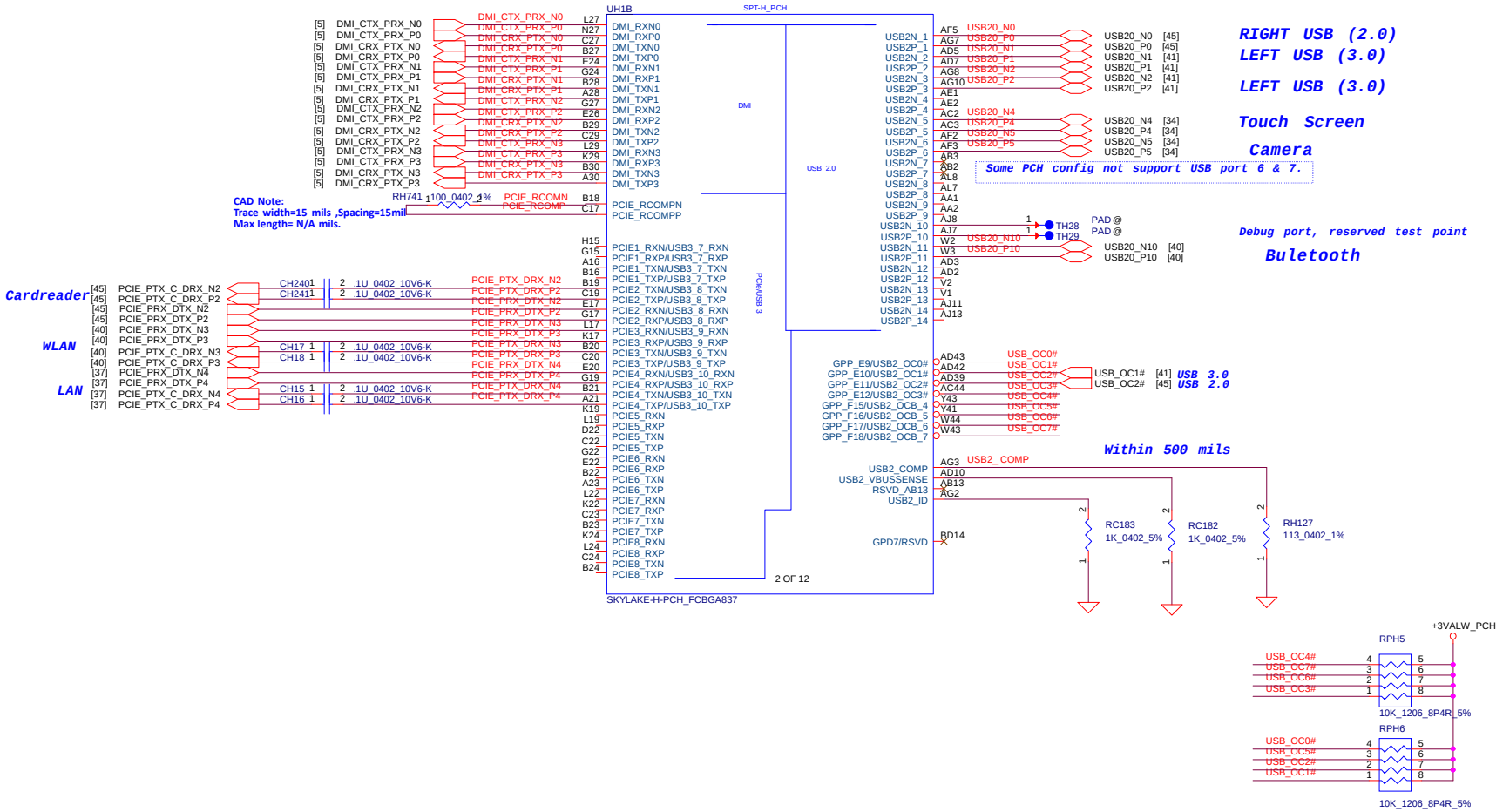


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 18 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (5/9) DMI, PCIe, USB2, GPI

Size	Document Number	Rev
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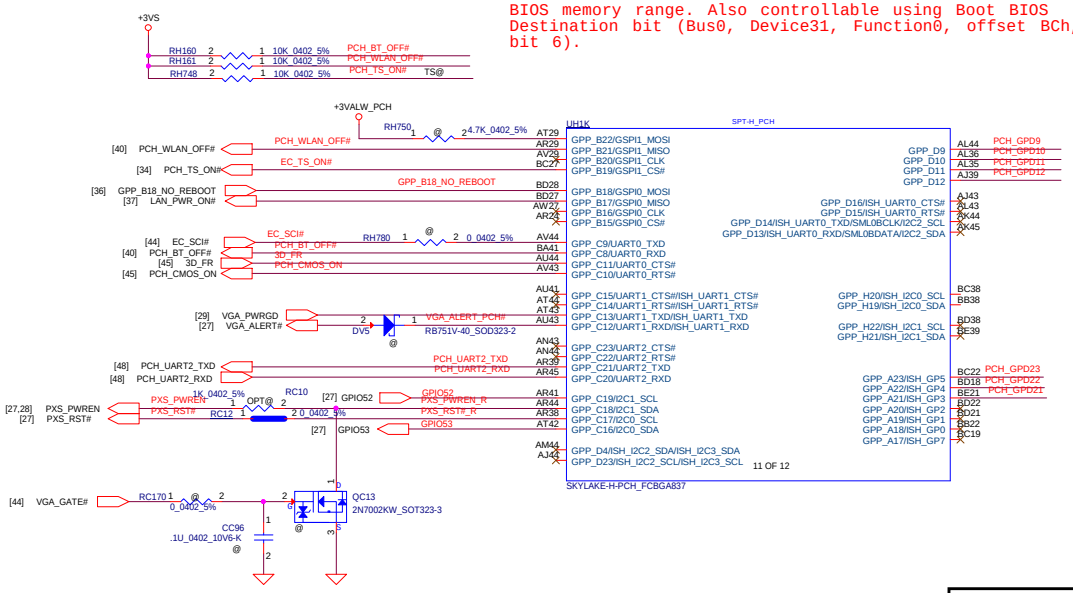
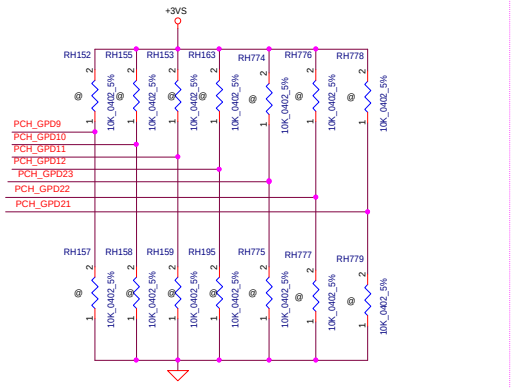
GSPI1_MOSI / GPP_B22
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).

Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC



SKU ID



Function	PCH_GPD9	PCH_GPD10	PCH_GPD11	PCH_GPD12	PCH_GPD21	PCH_GPD22	PCH_GPD23
17"	0	X	X	X	X	X	X
15"	1	X	X	X	X	X	X
non 3D Camera	X	0	X	X	X	X	X
3D Camera	X	1	X	X	X	X	X
non-touch	X	X	0	X	X	X	X
touch	X	X	1	X	X	X	X
SDV	X	X	X	X	0	0	0
SIV	X	X	X	X	0	0	1
SIT	X	X	X	X	0	1	0
SVT	X	X	X	X	0	1	1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (6/9) GPPPABCD, I2C

Size	Document Number	Rev
C	BY511/BY710	0.3

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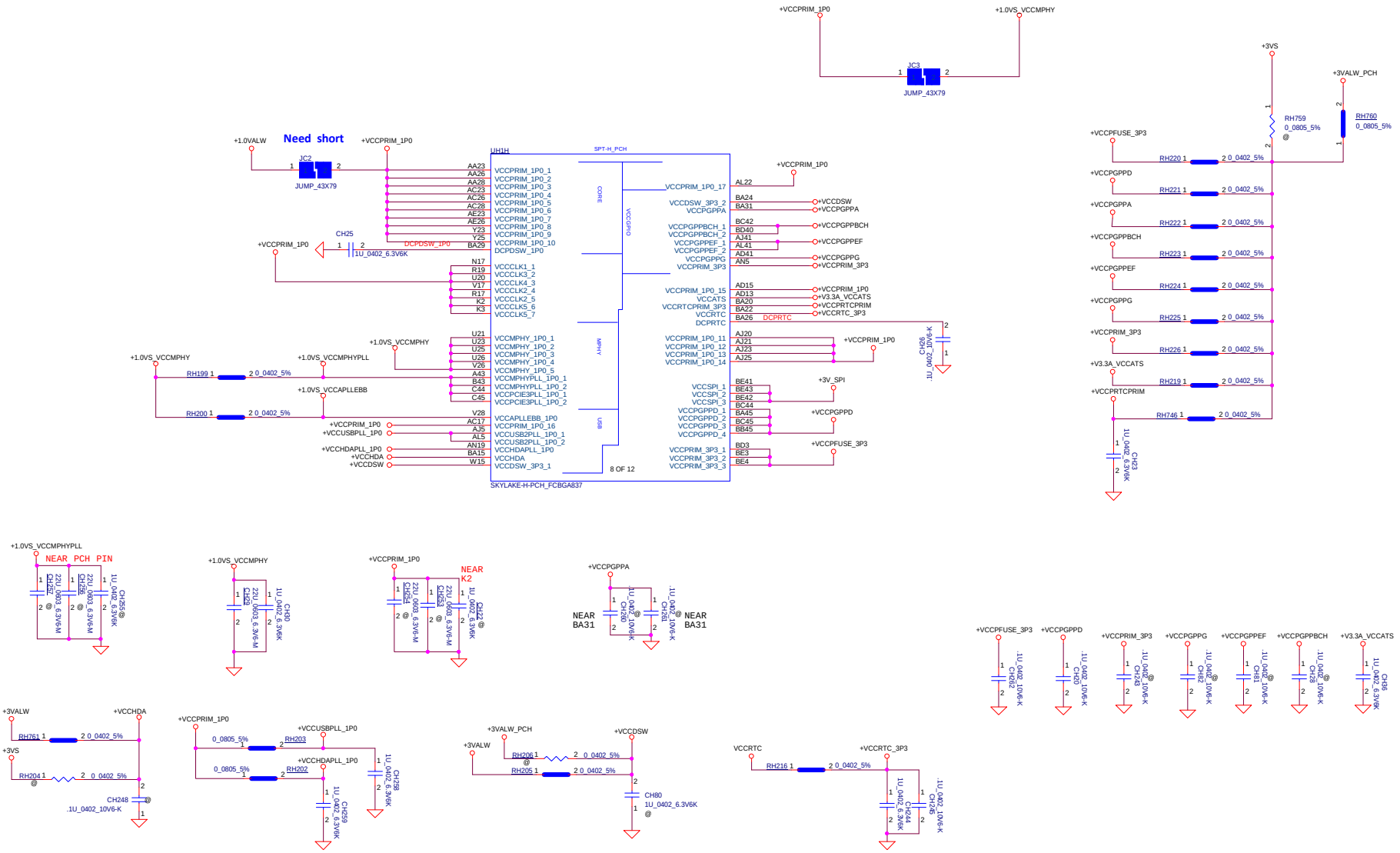
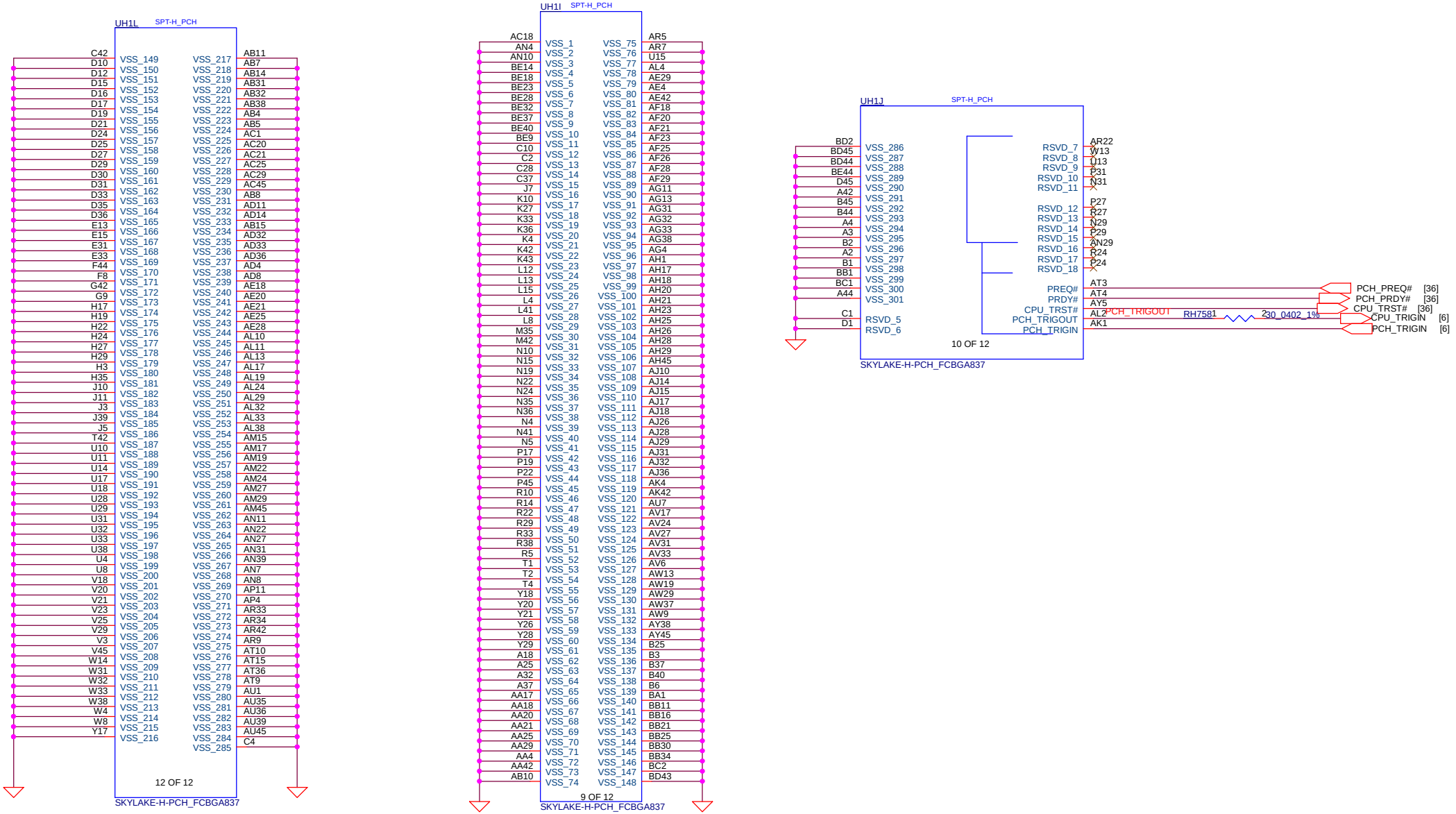


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (7/9) PWR

Size	Document Number	Rev
C	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 21 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PCH (9/9) VSS**

Size: B	Document Number: BY511/BY710	Rev: 0.3
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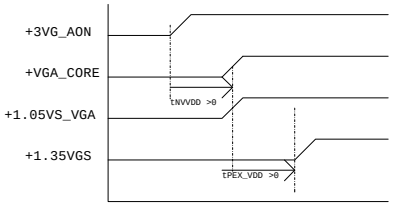
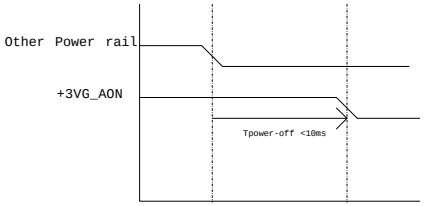
N16P-GX GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	IN	-	System side PCIe reset Monitor
GPIO9	I/O	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control (100K pull Down)
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16	IN	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT	-	GPU PCIe self-reset control
OVERT	I/O	-	Active Low Thermal Catastrophic Over Temperature

N16P-GX Power Sequence



1. all power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (DDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (A)	PCI Express (1.05V) (6) (W)		I/O and PLLVDD (1.05V) (A)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (A)	Other (3.3V) (W)
N16P-GX 128bit 2GB DDR5	50	3.27	2505	TBD	51.1	TBD	3.46	4.67	8.75	11.81	TBD	TBD		2.57	2.7	0.34	TBD

N16P-GX Multi-level Straps

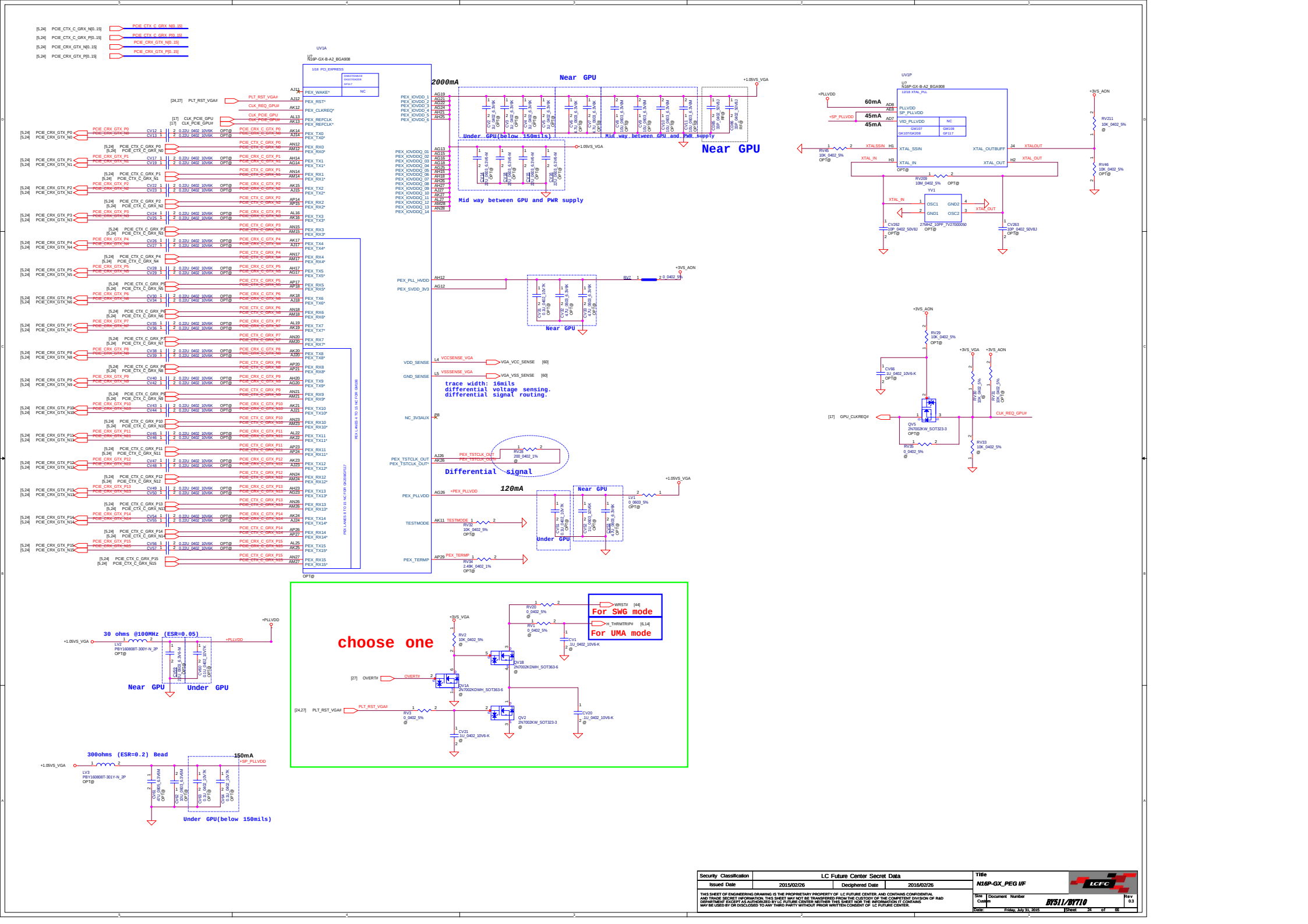
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N16P-GX Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

Title			
VGA Notes List			
Size C	Document Number BY511/BY710		Rev 0.3
Date: Friday, July 31, 2015	Sheet 23 of 66		



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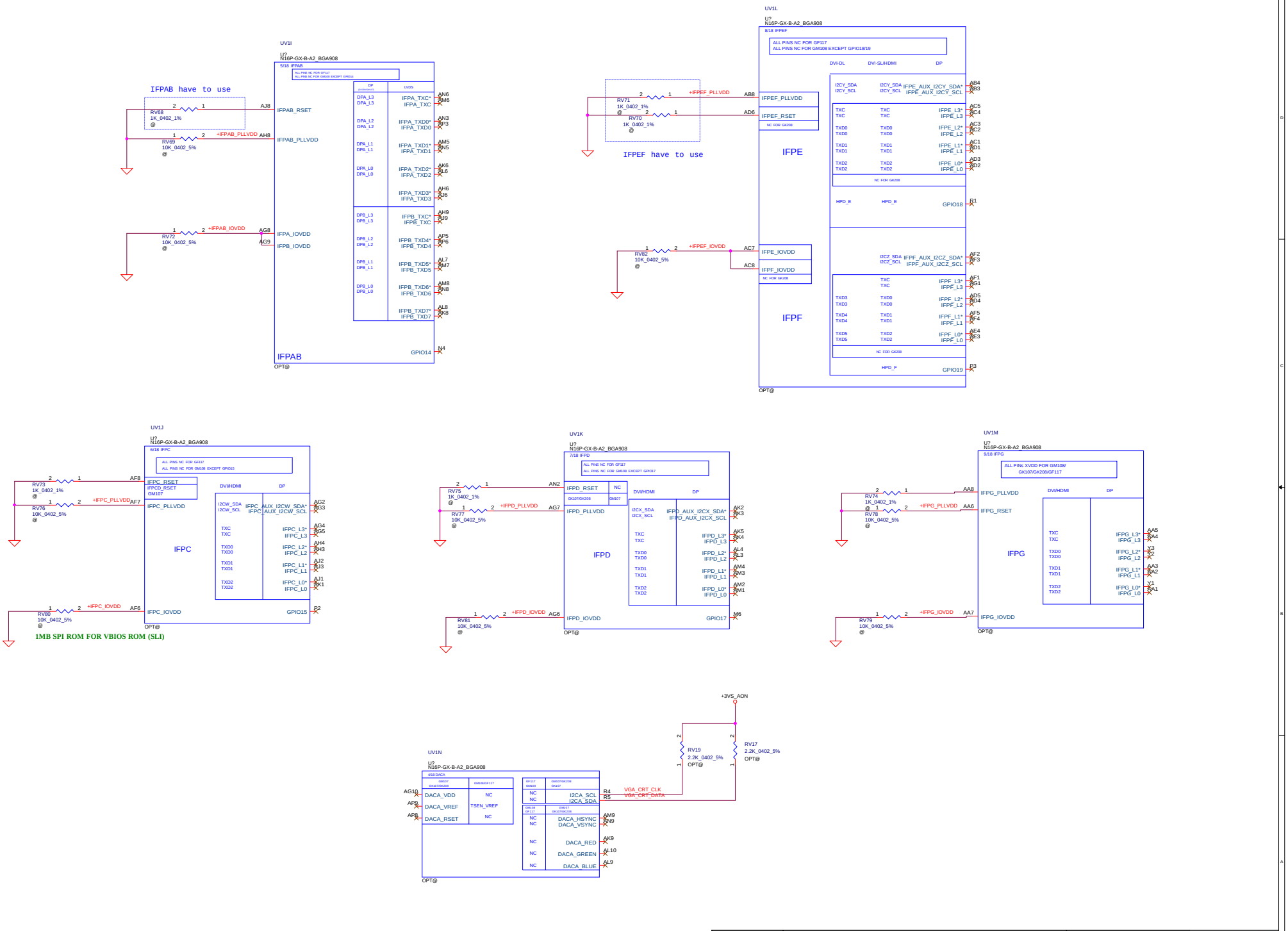
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N16P-GX_PEG I/F		
Size	Document Number		Rev
Custom	BY511/BY710		0.3
Date:	Friday, July 31, 2015	Sheet	24 of 65



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Issued Date	2015/02/26	Deciphered Date	2016/02/26

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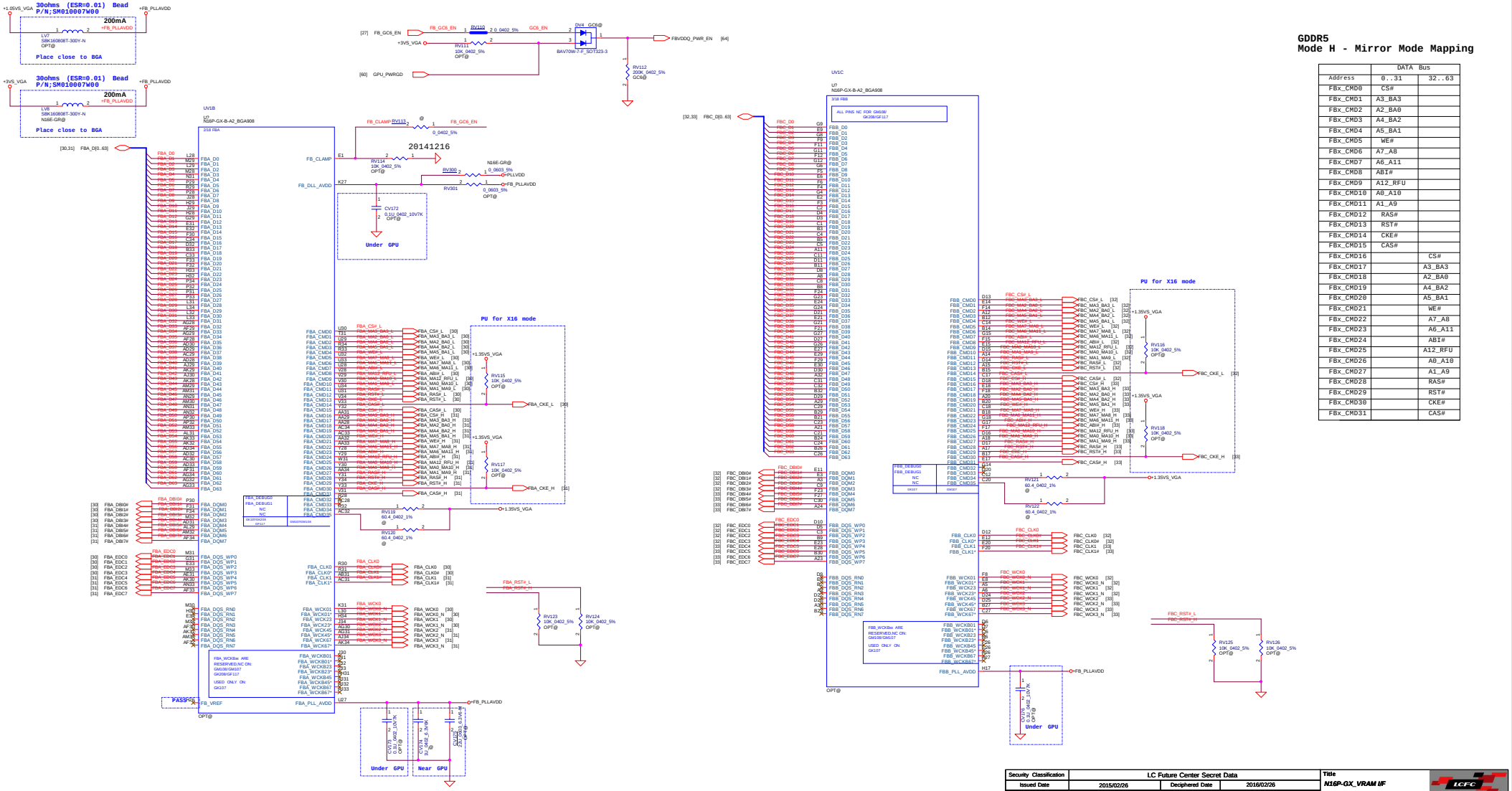
Title: N16P-GX_DIGITAL OUT I/F

Size: Custom | Document Number: BY511/BY710 | Rev: 0.3

Date: Friday, July 31, 2015 | Sheet 25 of 66

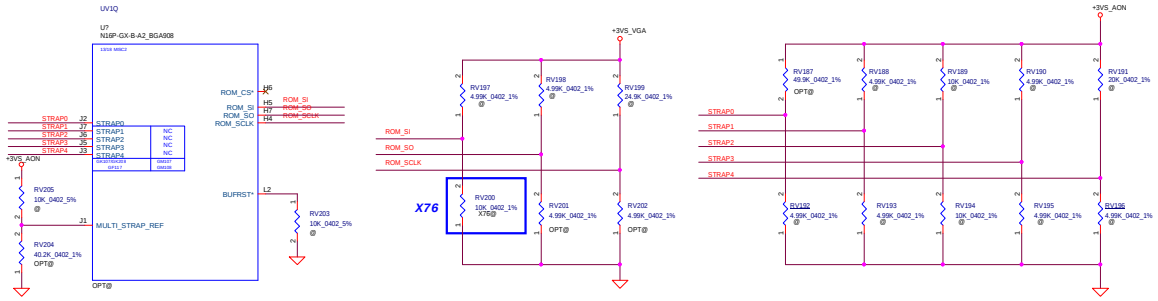


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N16P-GX_VRAM I/F		
Size	Document Number		Rev
Custom	BY511/BY710		0.3
Date:	Friday, July 31, 2015	Sheet 28 of 66	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

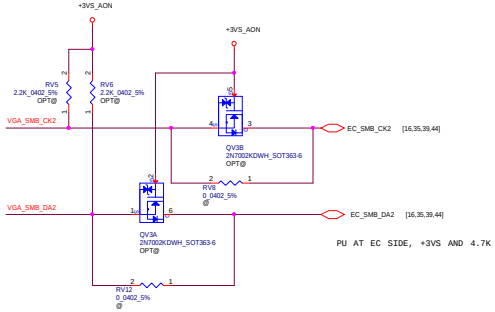
PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

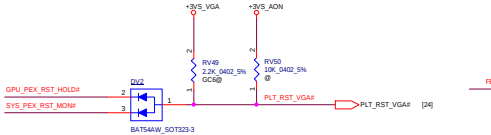
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

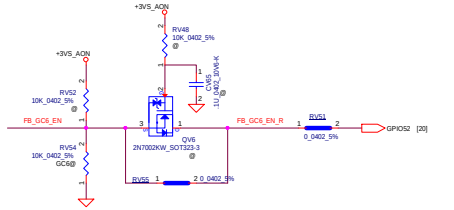
X76

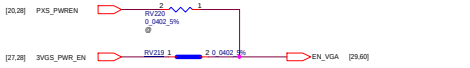
GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GX	Samsung	K4G20325FD-FC03 128X16	PD 5K	PD 5K	PD 5K	PU 50K	NC	NC	NC	NC
		K4G41325FC-HC03 256X16	PD 20K							
	Hynix	H5GC2H24BFR-T2C 128X16	PD 10K							
		H5GC4H24AJR-T2C 256X16	PD 34.8K							
	Micron	EDW2032BABG-6A-F 128X16	PD 30.1K							
		EDW4032BABG-60-F 256X16	PD 24.9K							

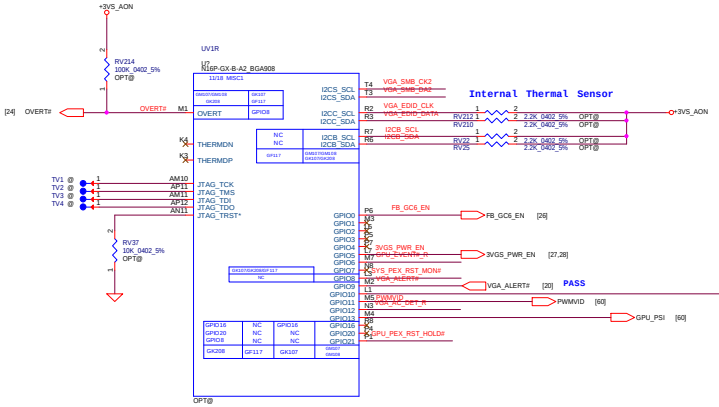


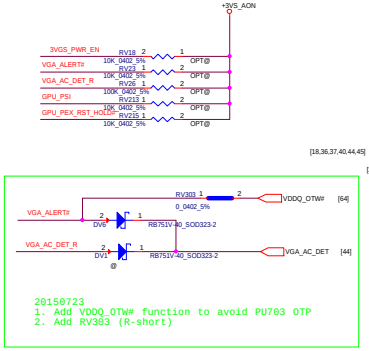
PU AT EC SIDE, +3VS AND 4.7K



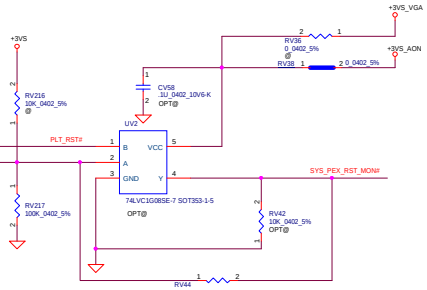






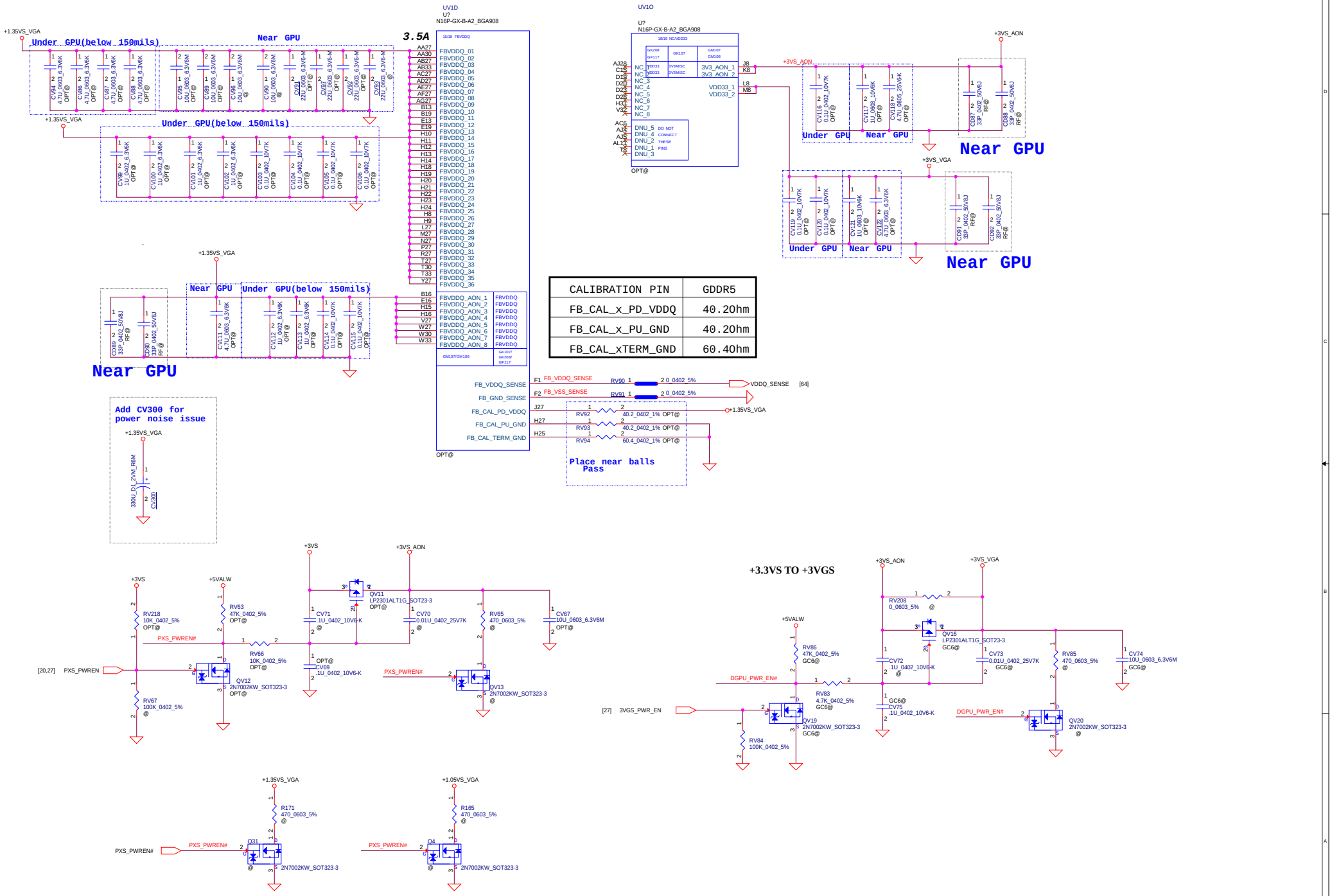


20150723
1. Add VDDQ_OTW# function to avoid PU703 OTP
2. Add RV303 (R-short)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

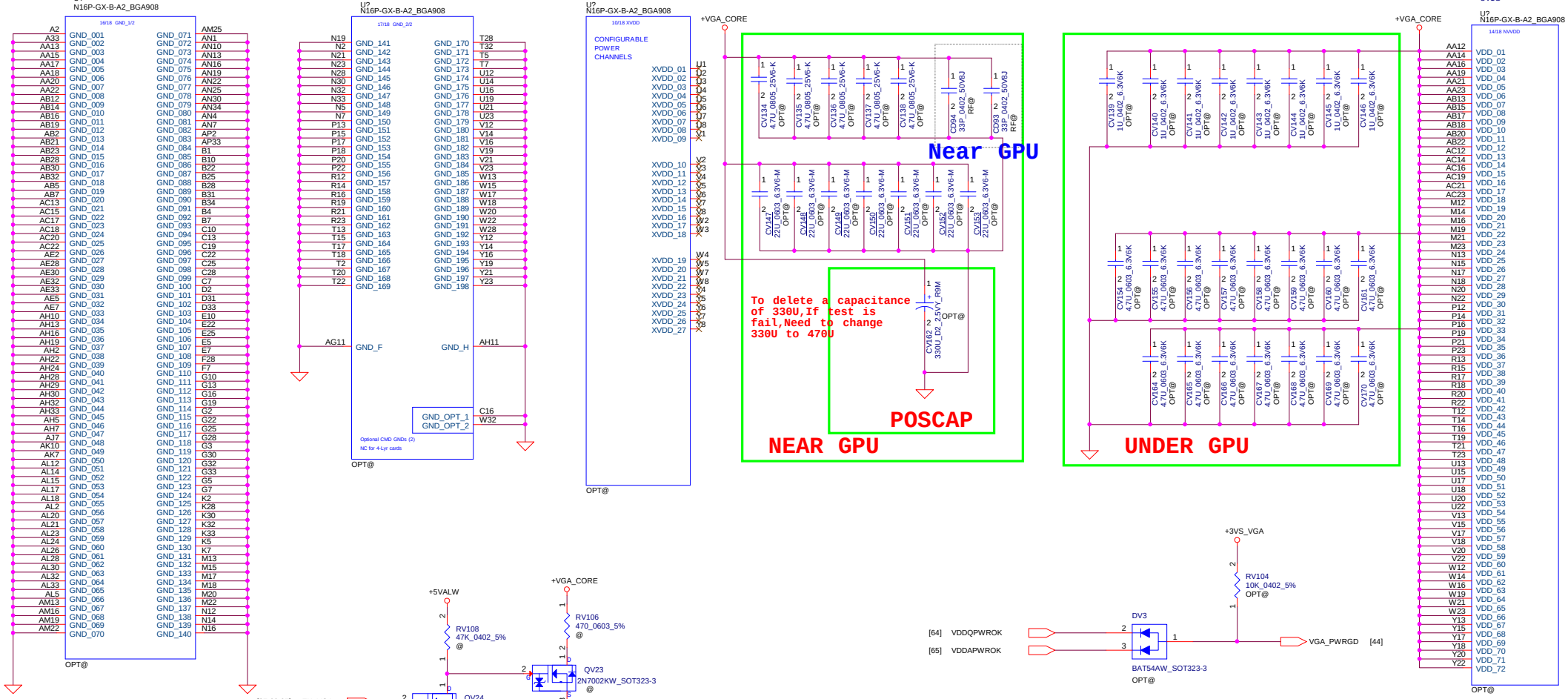
Title			
N16P-GX_PEG I/F			
Size: Custom	Document Number: BY511/BY710		Rev: 0.3
Date: Friday, July 31, 2015	Sheet 27 of 65		



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	POWER		
Size C	Document Number	BY511/BY710	Rev 0.3
Date: Friday, July 31, 2015	Sheet 28 of 66		



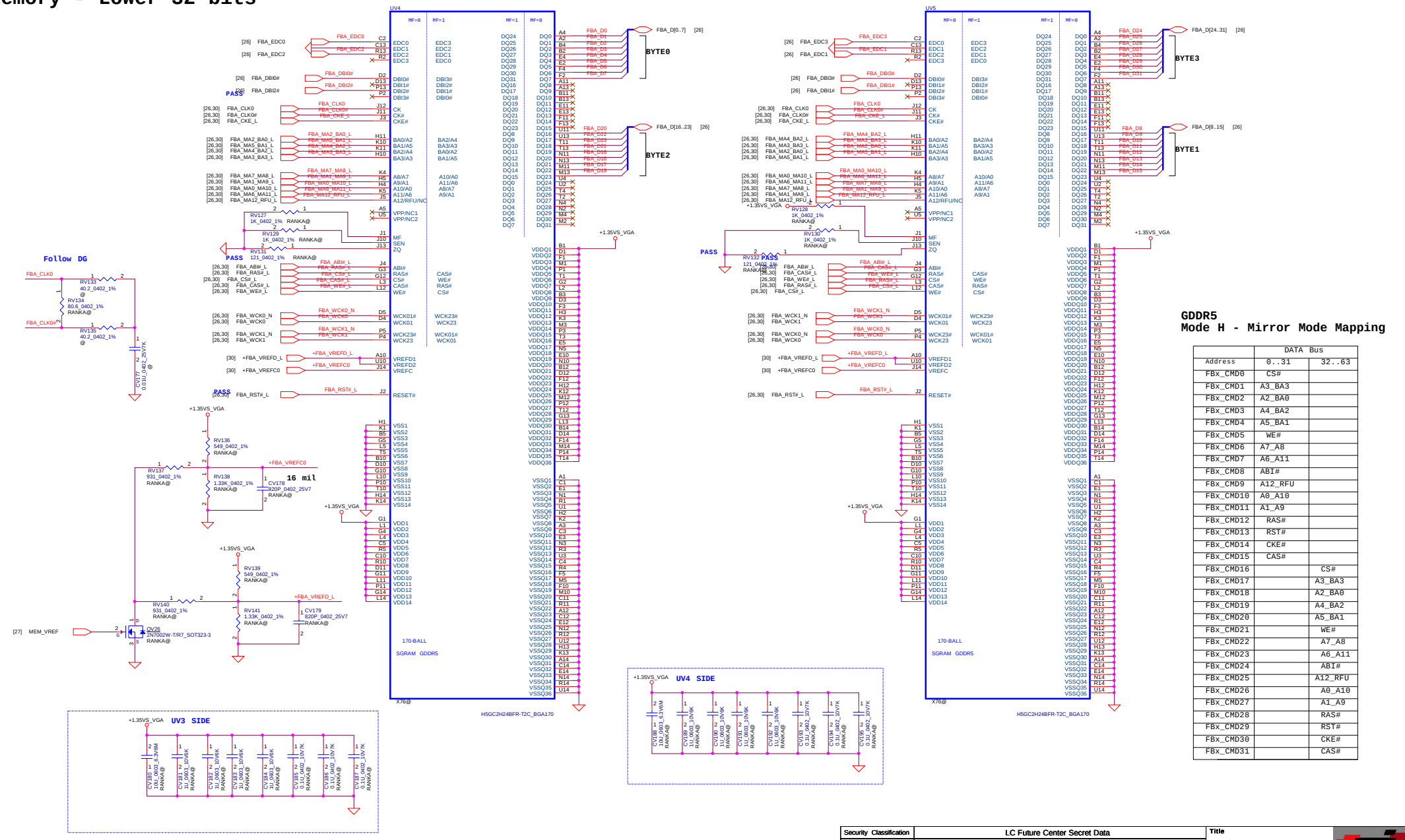
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: GND

Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 29 of 66

Memory - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

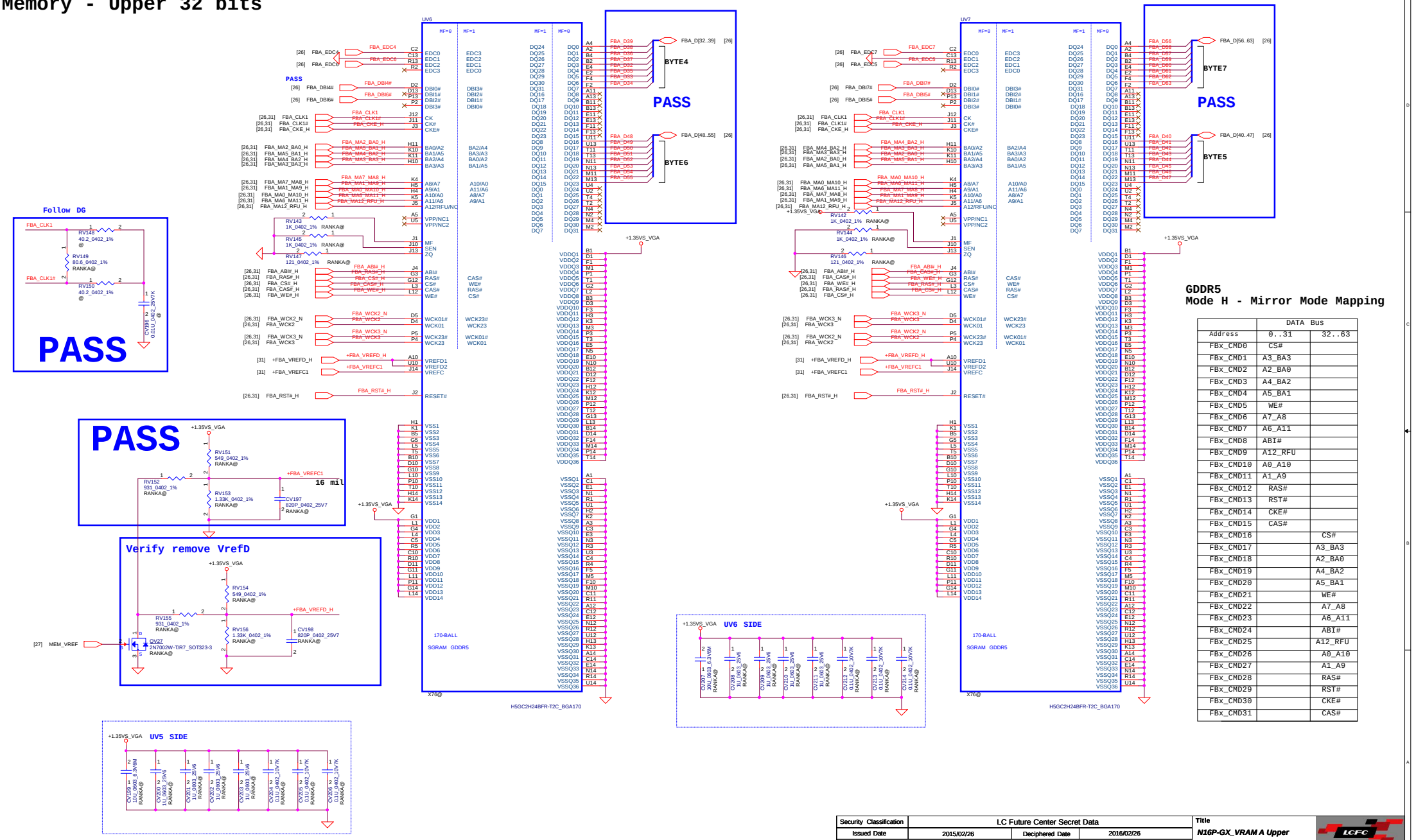
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N16P-GX_VRAM A Lower

Size: Custom | Document Number: BV511/BV710 | Rev: 0.3

Date: Friday, July 31, 2015 | Sheet 30 of 66

Memory - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

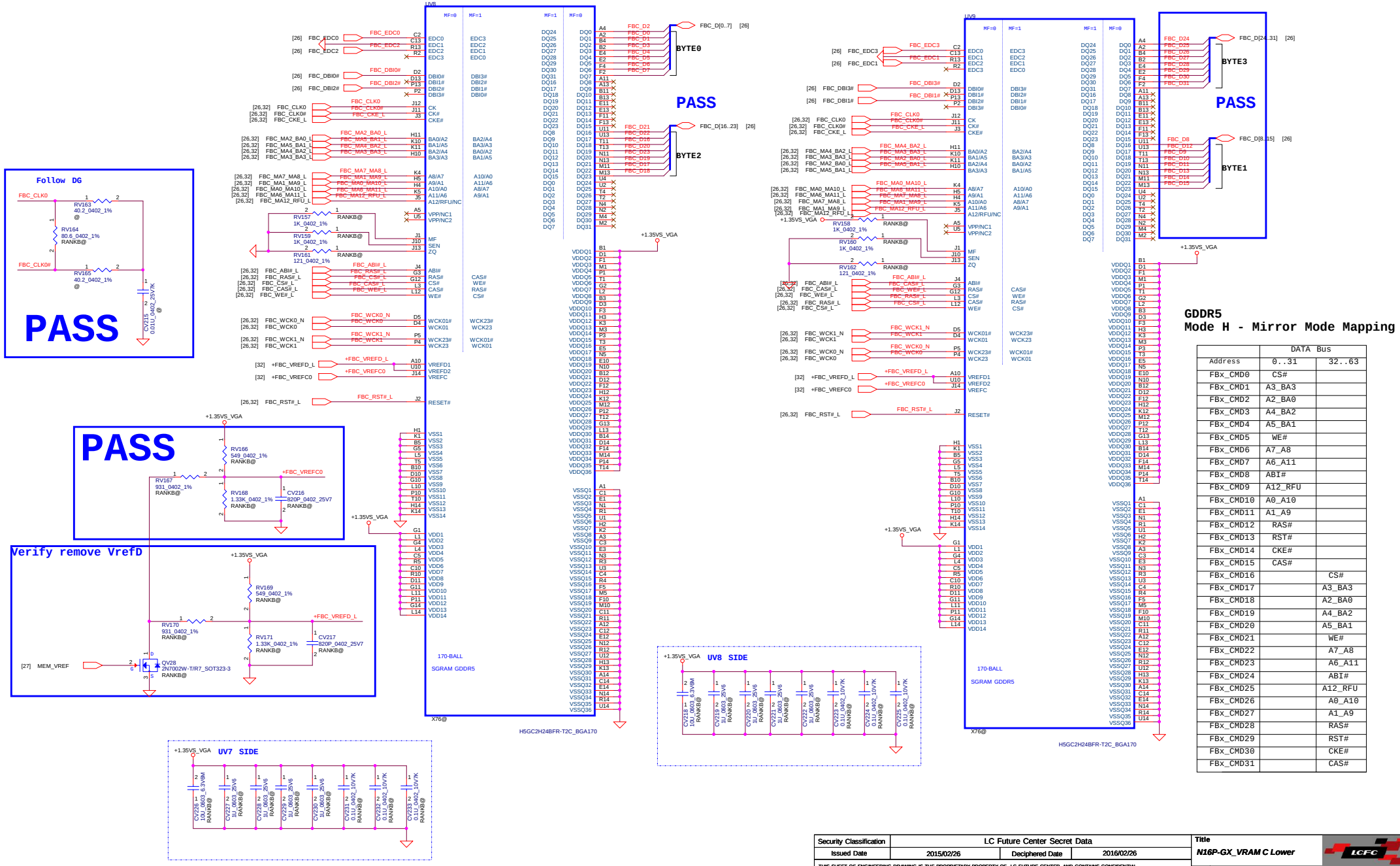
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N16P-GX_VRAM A Upper

Size: Custom | Document Number: BV511/BV710 | Rev: 0.3

Date: Friday, July 31, 2015 | Sheet 31 of 66

Memory Partition C - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

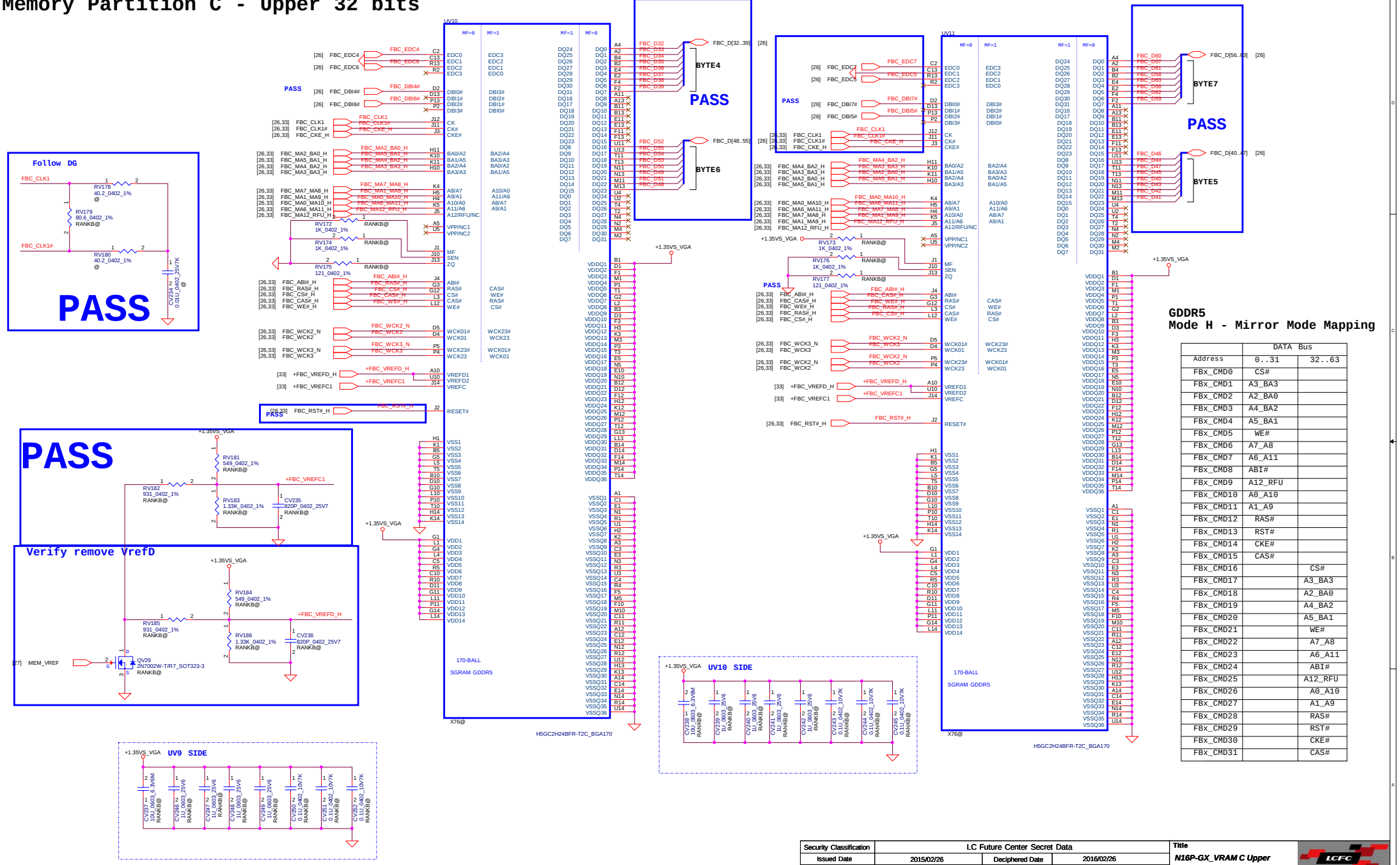
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N16P-GX_VRAM C Lower

Size: Custom | Document Number: BY511/BY710 | Rev: 0.3

Date: Friday, July 31, 2015 | Sheet 32 of 66

Memory Partition C - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

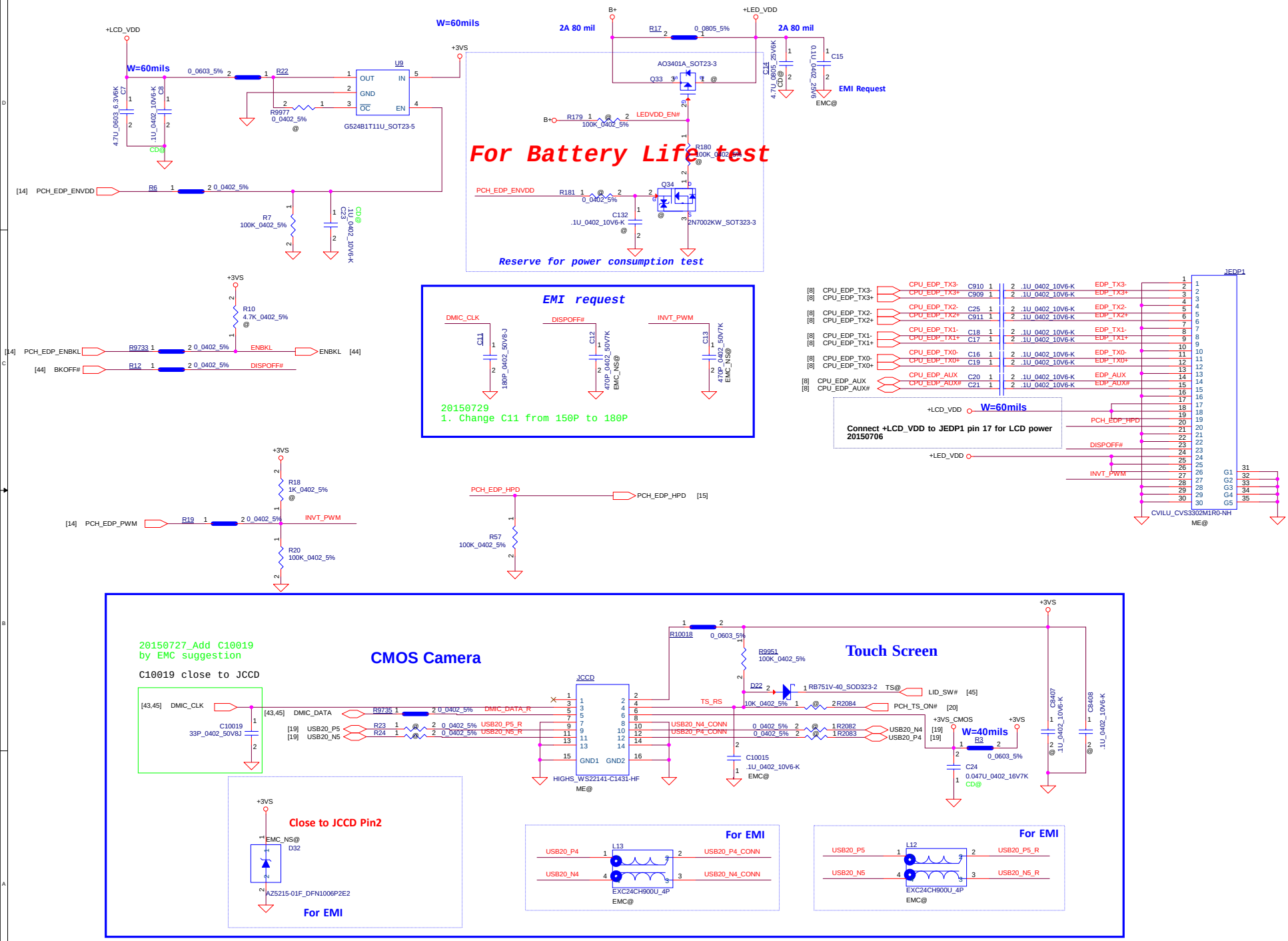
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N16P-GX_VRAM C Upper

Size: Custom | Document Number: BY511/BY710 | Rev: 0.3

Date: Friday, July 31, 2015 | Sheet 33 of 66

LCD POWER CIRCUIT

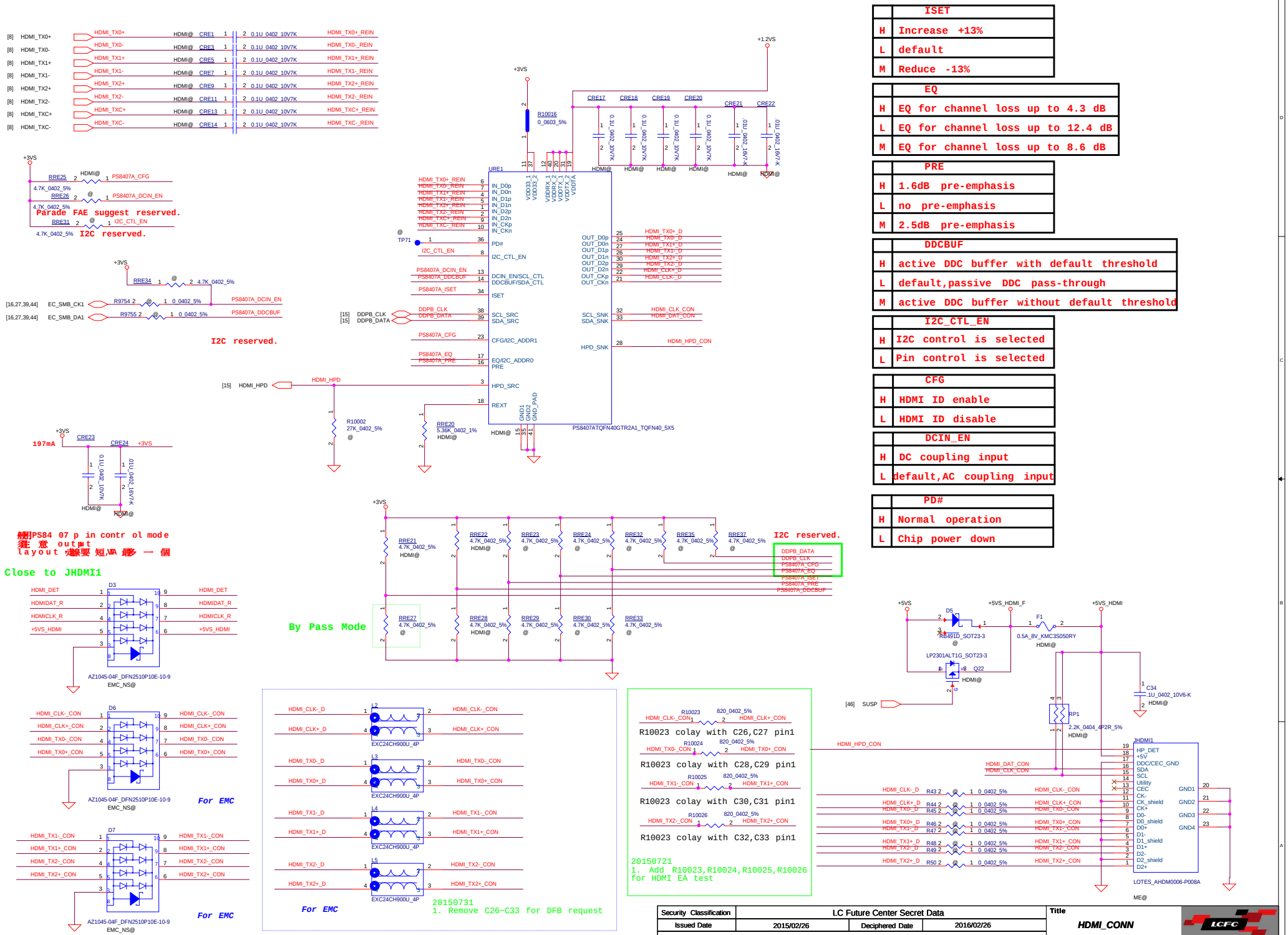


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: eDP/ CMOS/Touch screen

Size: Custom | Document Number: BY511/BY710 | Rev: 0.3

Date: Friday, July 31, 2015 | Sheet 34 of 66


ISET
H Increase +13%
L default
M Reduce -13%
EQ
H EQ for channel loss up to 4.3 dB
L EQ for channel loss up to 12.4 dB
M EQ for channel loss up to 8.6 dB
PRE
H 1.6dB pre-emphasis
L no pre-emphasis
M 2.5dB pre-emphasis
DDCBUF
H active DDC buffer with default threshold
L default,passive DDC pass-through
M active DDC buffer without default threshold
I2C_CTL_EN
H I2C control is selected
L Pin control is selected
CFG
H HDMI ID enable
L HDMI ID disable
DCIN_EN
H DC coupling input
L default,AC coupling input
PD#
H Normal operation
L Chip power down
Parade FAE suggest reserved.
I2C reserved.
I2C reserved.
I2C reserved.
197mA
Close to JHDMI1
By Pass Mode
For EMC
For EMC
R10023 colay with C26,C27 pin1
R10023 colay with C28,C29 pin1
R10023 colay with C30,C31 pin1
R10023 colay with C32,C33 pin1
20150721
1. Add R10023,R10024,R10025,R10026 for HDMI EA test
20150731
1. Remove C26~C33 for DFB request
PS8407ATQFN40GTR2A1_TQFN40_5X5
AZ1045-04F_DFN2510P10E-10-9
LOTES_AHDM0006-P008A
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
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Title
HDMI_CONN
Size C
Document Number
BY511/BY710
Rev 0.3
Date: Friday, July 31, 2015
Sheet 35 of 67

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

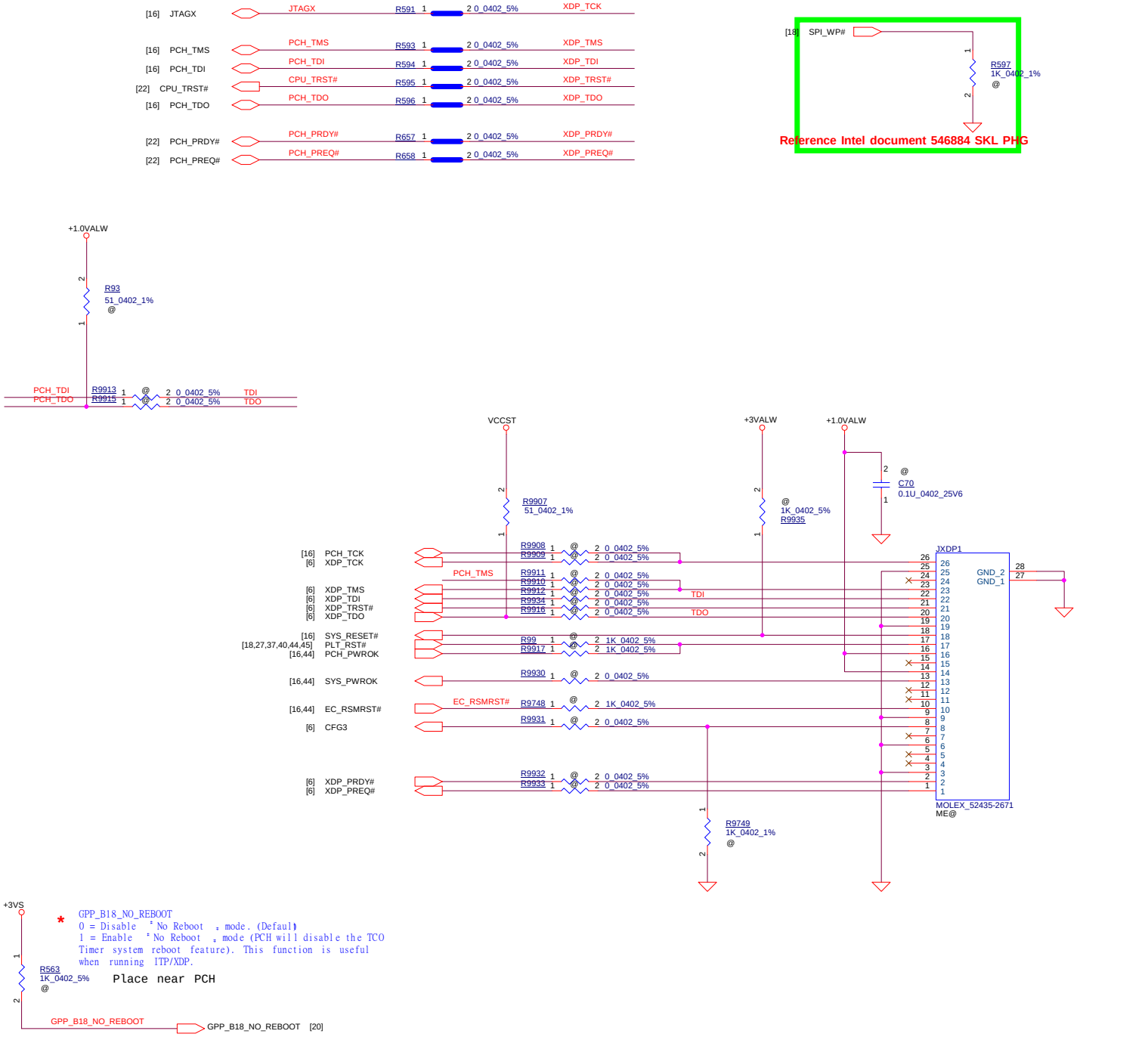
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	XDP		
Size	Document Number		Rev
Custom	BY511/BY710		0.3
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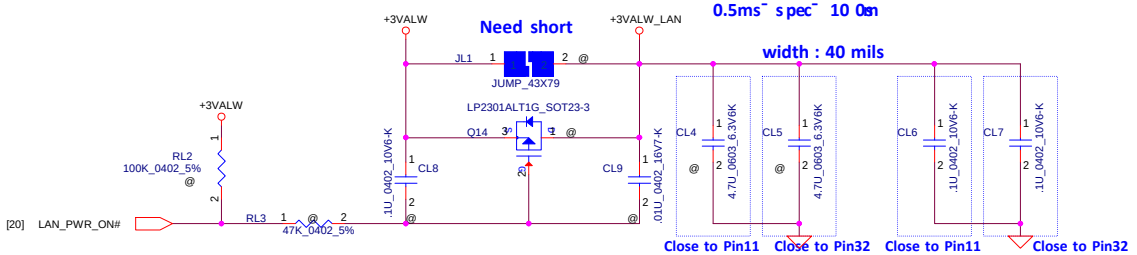
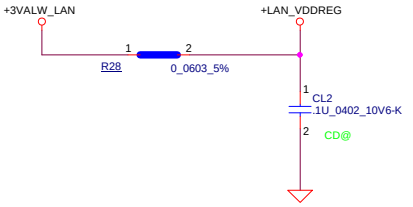
+3VALW TO +3VALW_LAN

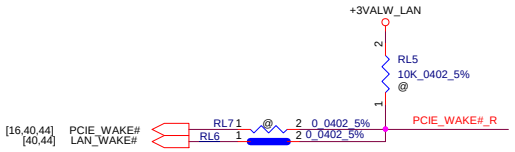
+3VALW_LAN rising time (10%~90%): 0.5ms~10ms spec

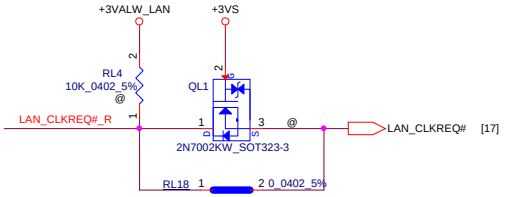
Need short

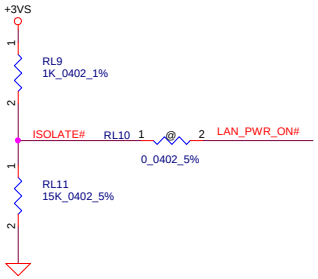
width : 40 mils

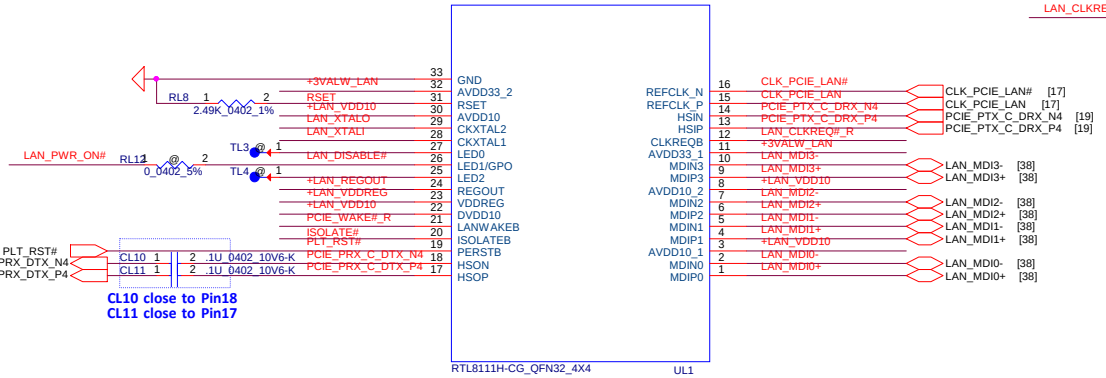


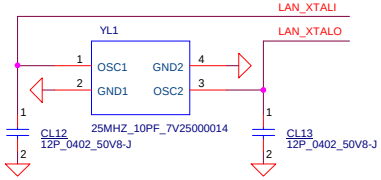


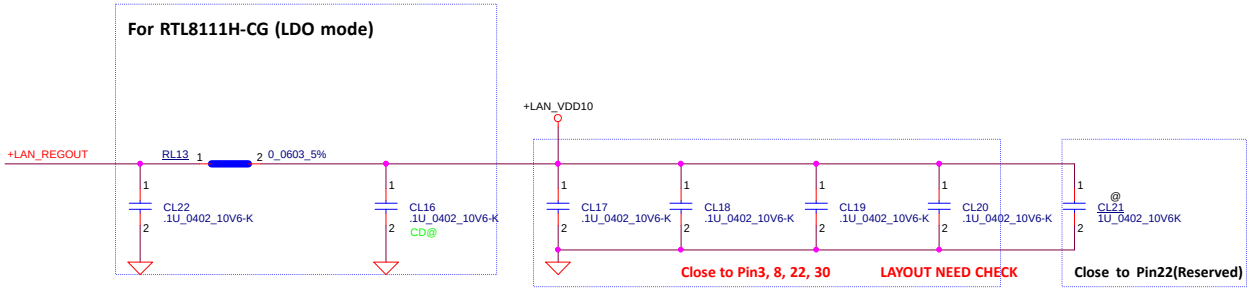












Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

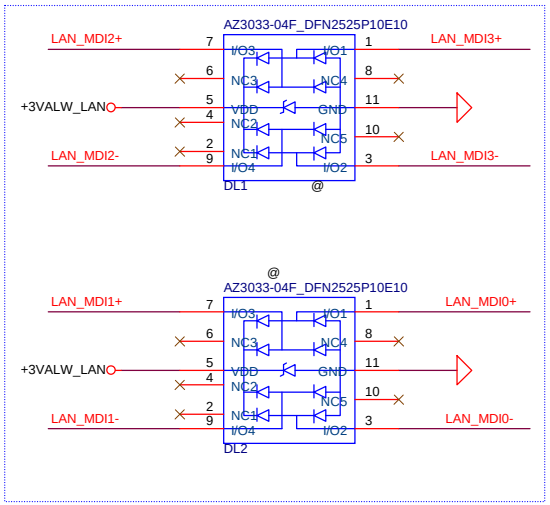
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: LAN_RTL8111GUL/RTL8106E

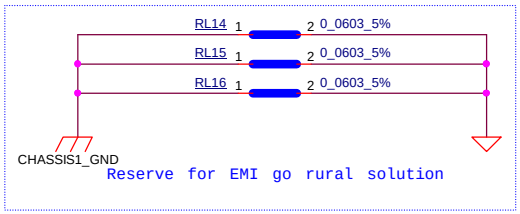
Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 37 of 67

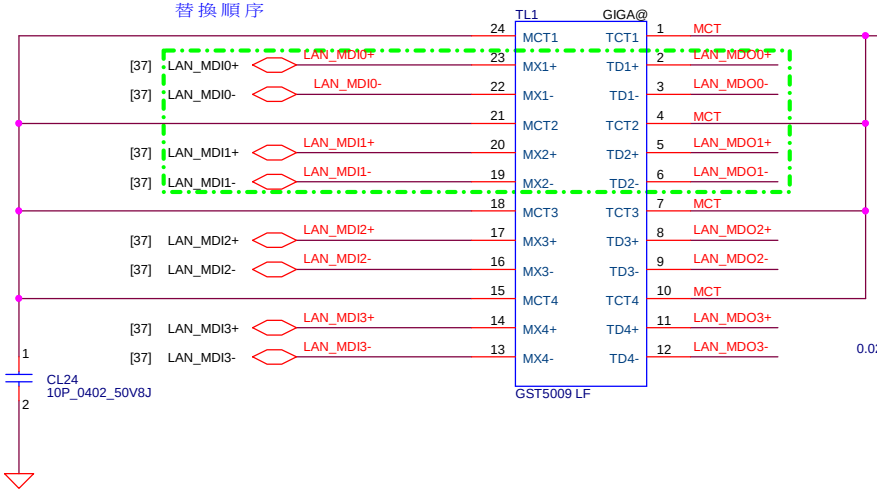
DL1/DL2
1'S PN:SC300003M00

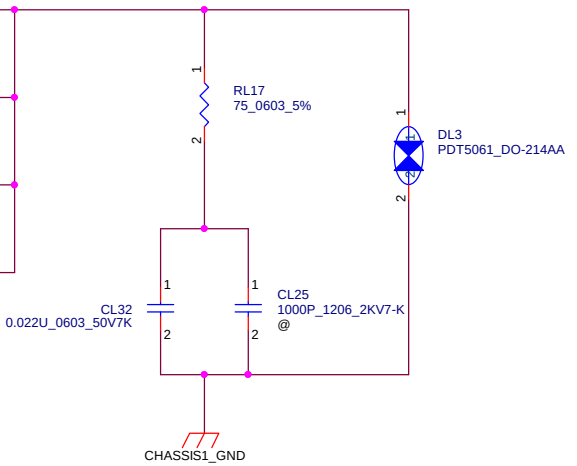


Place Close to TL1

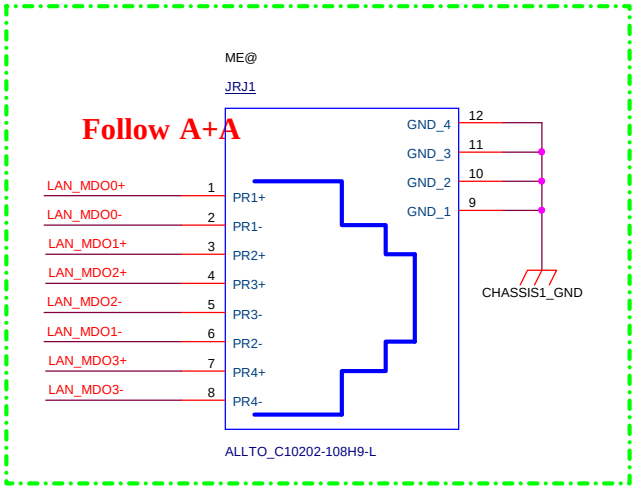


替換順序





靠JRJ 1 CONN



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

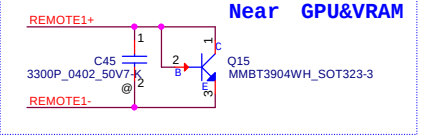
Title: LAN_Transformer

Size	Document Number	Rev
B	BY511/BY710	0.3

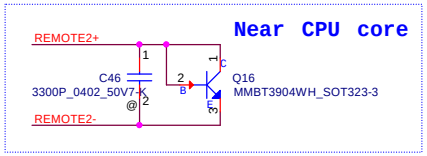
Date: Friday, July 31, 2015 Sheet 38 of 67

REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

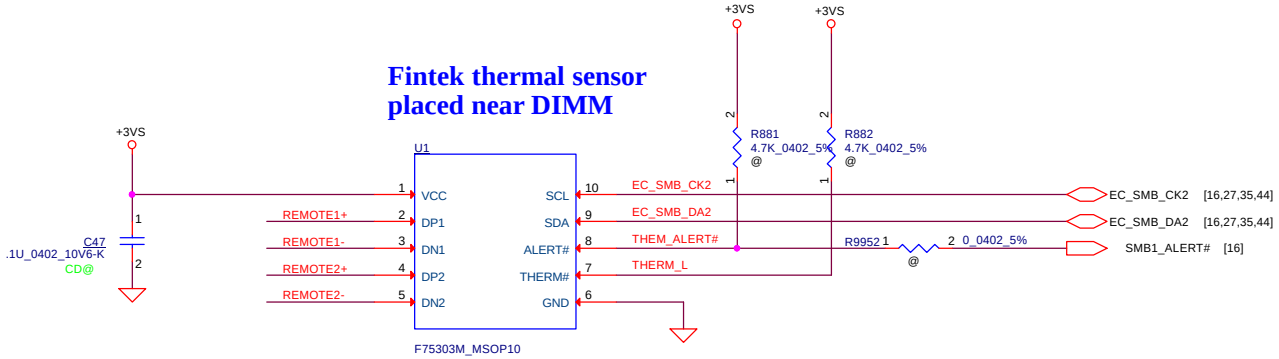
Near GPU&VRAM



Near CPU core

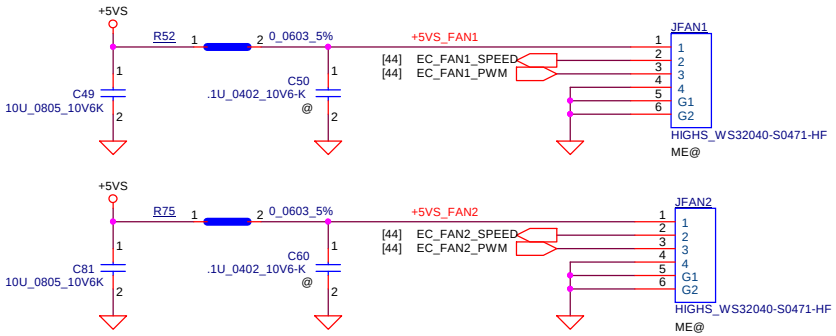


Fintek thermal sensor placed near DIMM



FAN Conn

Address 1001_101xb



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Thermal sensor/FAN CONN*

Size	Document Number	Rev
Custom	*BY511/BY710*	0.3

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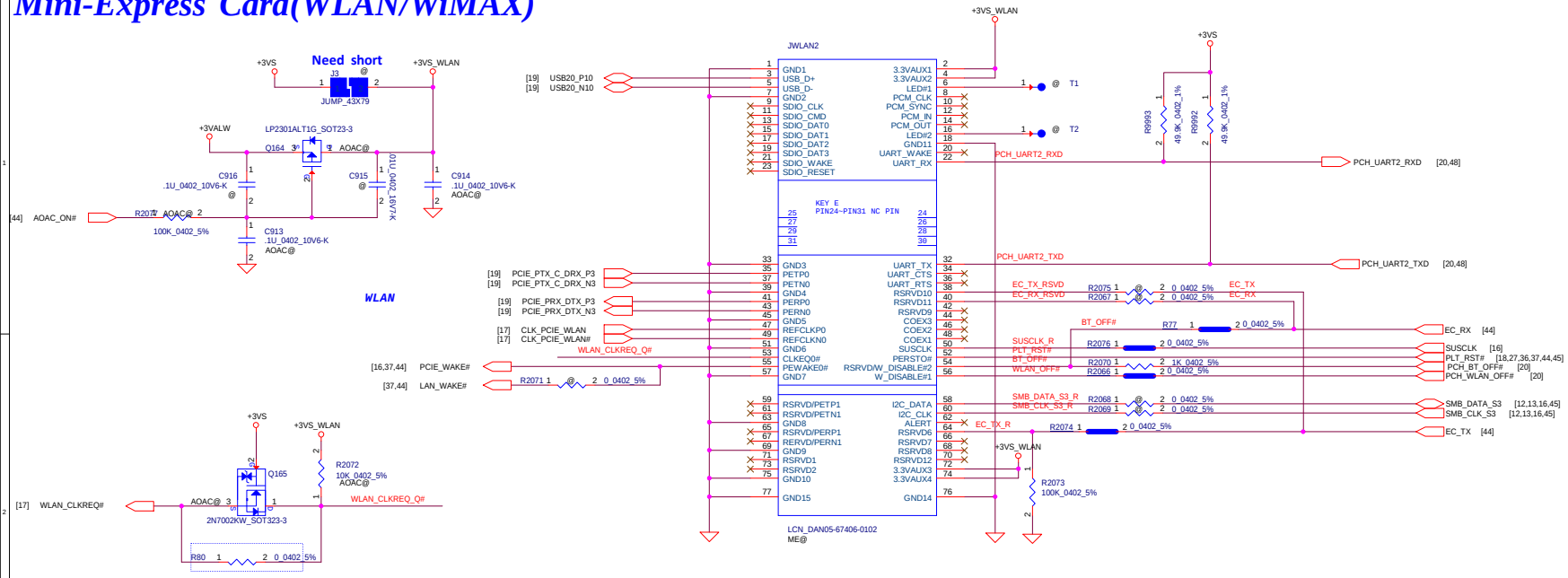
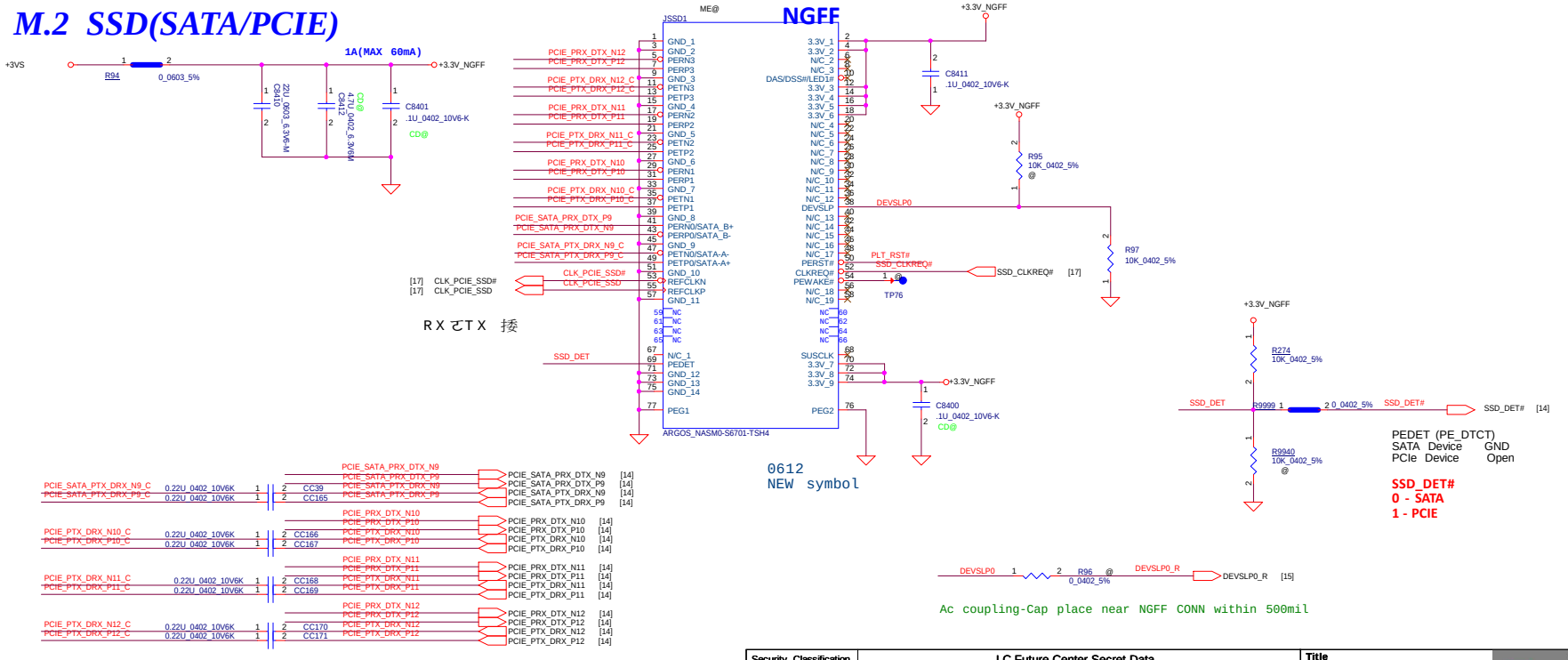
Mini-Express Card(WLAN/WiMAX)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: NGFF WLAN

Size: Custom | Document Number: BY511/BY710 | Rev: 0.3

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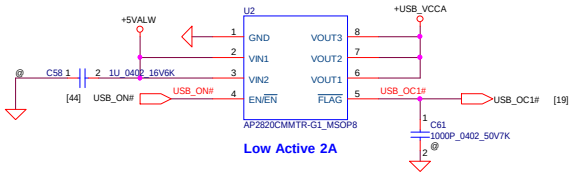
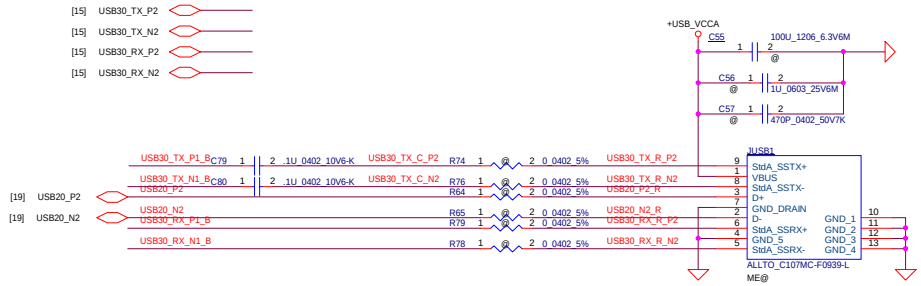
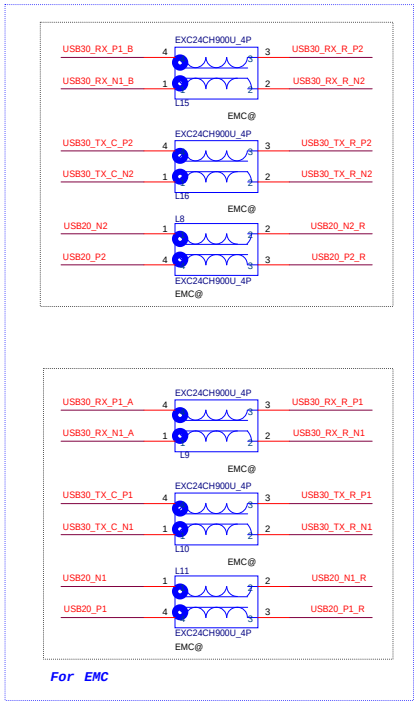
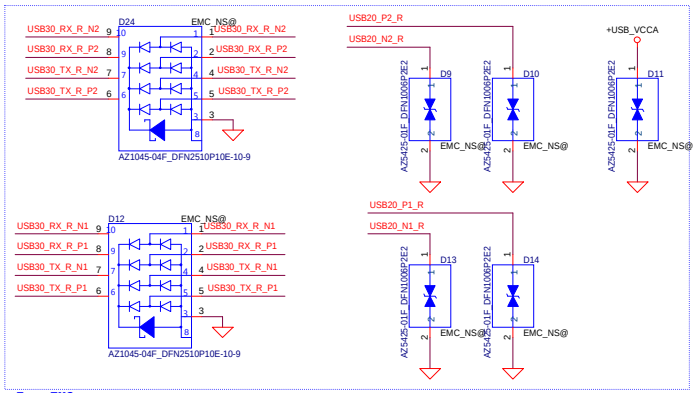
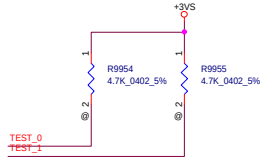
LEFT SIDE USB3.0 PORT X2

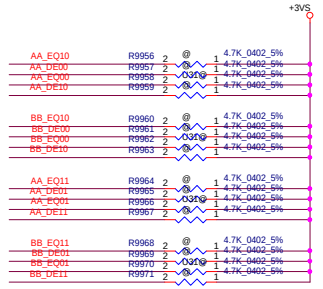


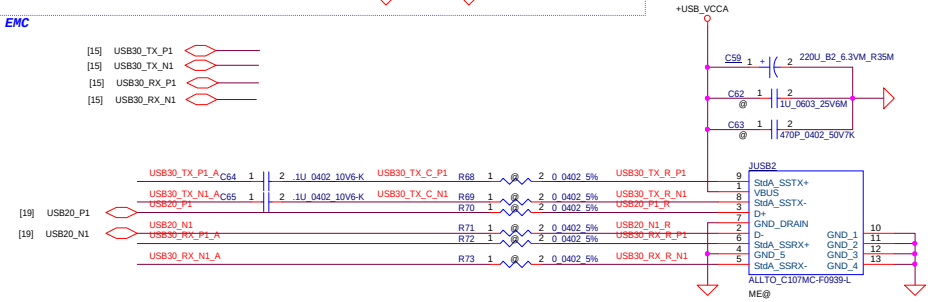




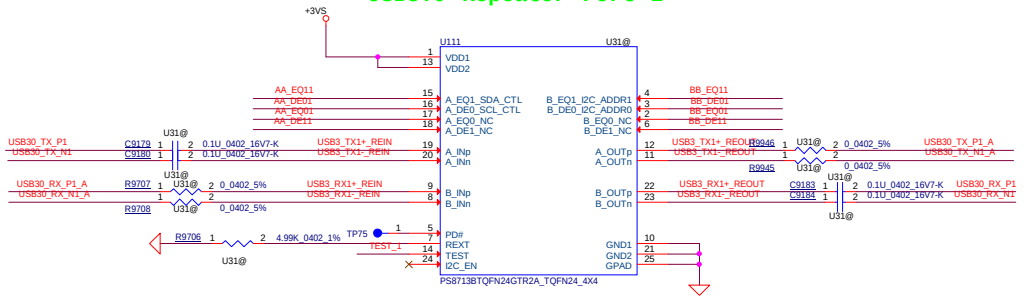




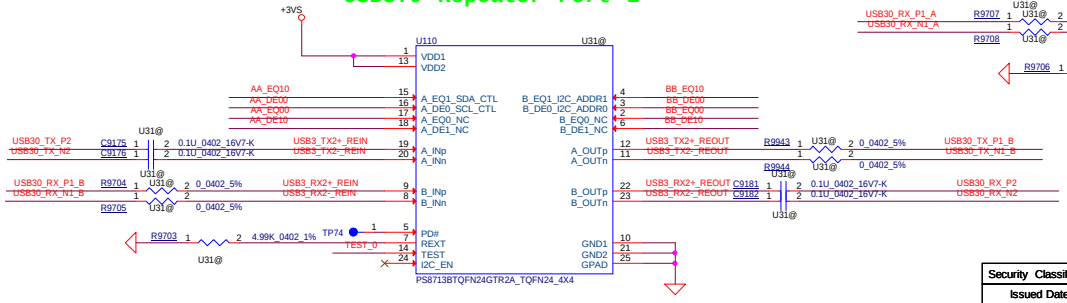




USB3.0 Repeator Port 2



USB3.0 Repeator Port 1



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: USB2.0/USB3.0 PORT (LEFT)

Size	Document Number	Rev
C	BY511/BY710	0.3

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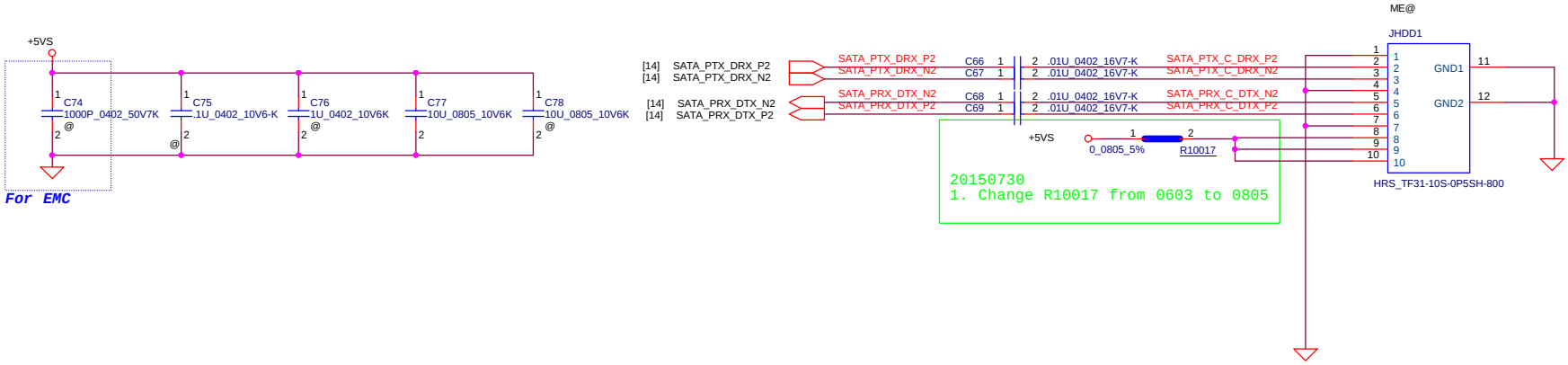
SATA HDD Conn.



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: HDD/ODD CONN

Size	Document Number	Rev
Custom	BY511/BY710	0.3

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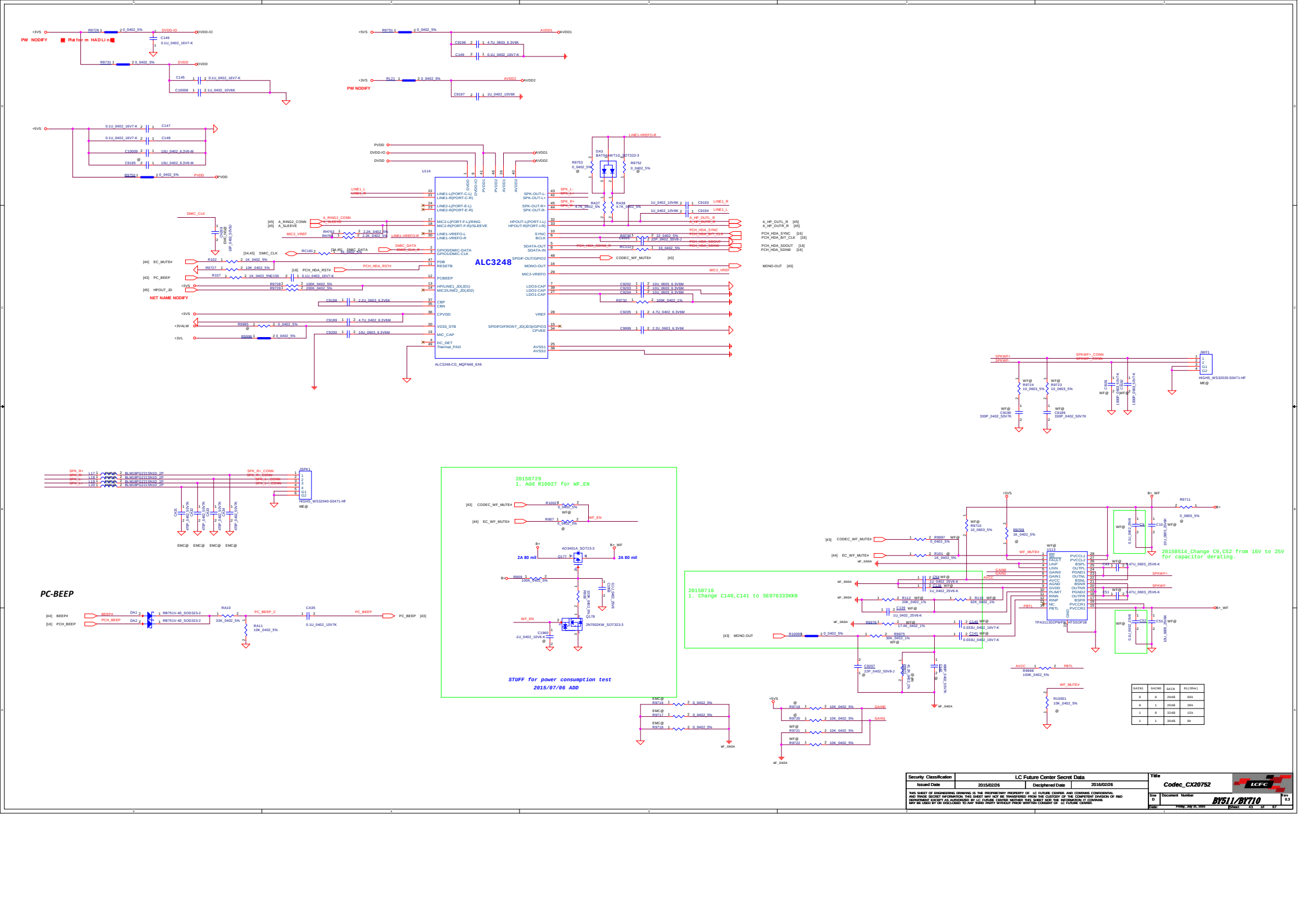
PW NODIFY
Platform HADLink
ALC3248
ALC3248-CG_MQFN48_6X6
NET NAME NODIFY
PC-BEEP
20150729
1. Add R10027 for WF_EN
STUFF for power consumption test
2015/07/06 ADD
20150716
1. Change C140,C141 to SE076333KK0
20150514_Change C9,C52 from 16V to 25V for capacitor derating.
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
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Codec_CX20752
Size
D
Document Number
BY511/BY710
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0.3
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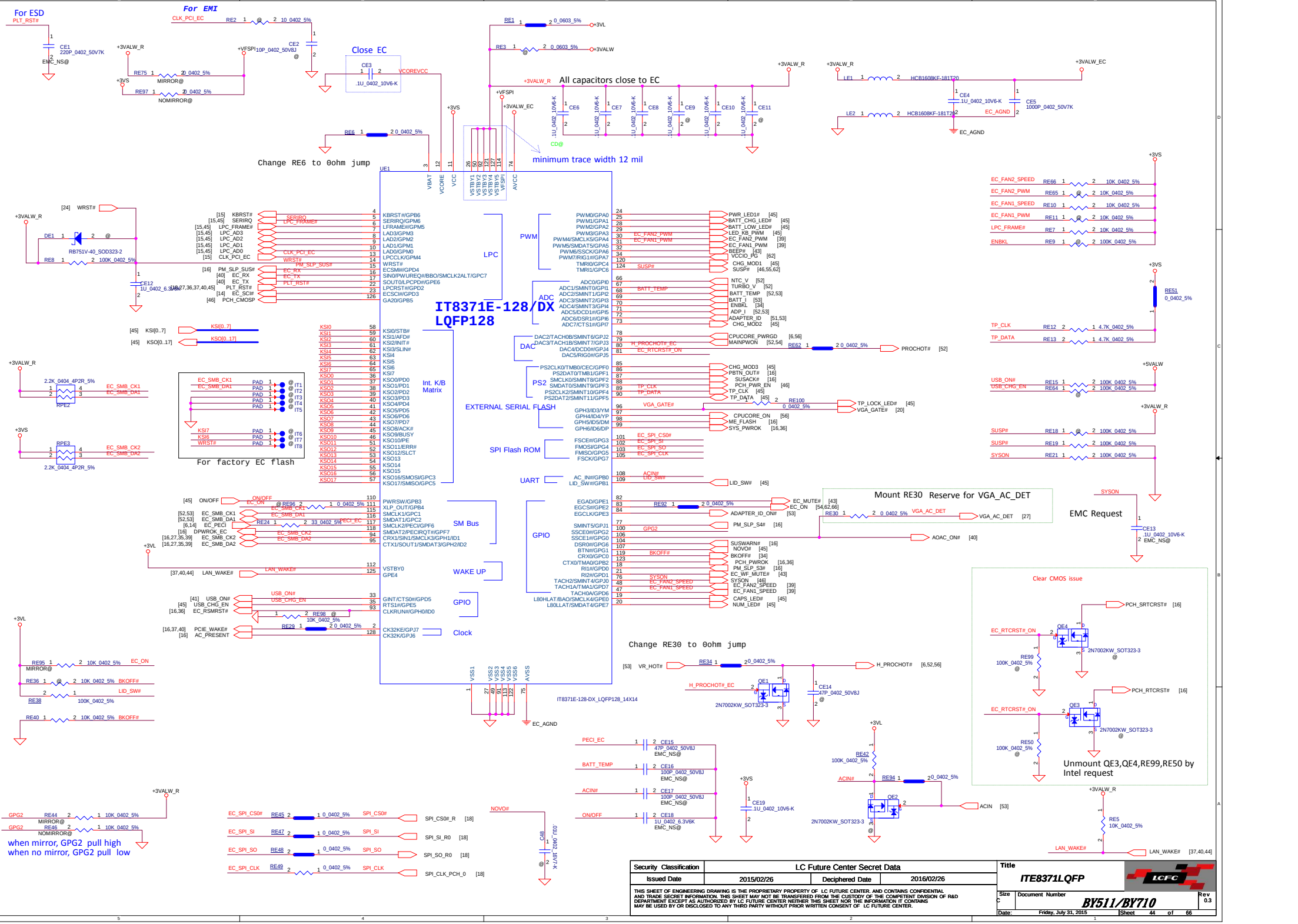
For ESD
For EMI
Close EC
All capacitors close to EC
Change RE6 to 0ohm jump
minimum trace width 12 mil
IT8371E-128/DX
LQFP128
Int. K/B Matrix
For factory EC flash
Change RE30 to 0ohm jump
Mount RE30 Reserve for VGA_AC_DET
EMC Request
Clear CMOS issue
Unmount QE3,QE4,RE99,RE50 by Intel request
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
Title
ITE8371LQFP
Document Number
BY511/BY710
Rev
0.3
Size
C
Date:
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66

ON/OFF switch

No function field

15"

17"

20150716
1. Change R142 and R9746
from 100 to 390 ohm

K/B Connector

LED

TP/B Connector

For EMC

USB charger

2.2A

Right Side USB2.0 Port X 1 (USB/B)

	pin number	6	7	8	4
	pin name	CTL1	CTL2	CTL3	ILM_SEL
Charge port Pin5 Enable H for all	S0 CDP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

SDP2 (No Discharge from/to CDP)
SDP1(Discharge from/to any charging state including CDP)

USB I/O Connector

GNDA

TPM

No function field

LID Hall Sensor

3D Camera

C10018 close to J3D

20150727_Add C10018
by EMC suggestion

For 3D CCD

From PCH

For RF solution.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: KBD/PWR/IO/LED/TP Conn.

Size: D | Document Number: BY511/BY710 | Rev: 0.3

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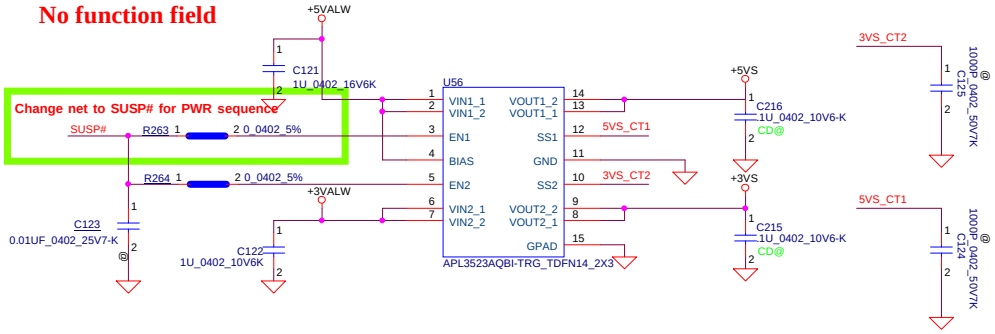
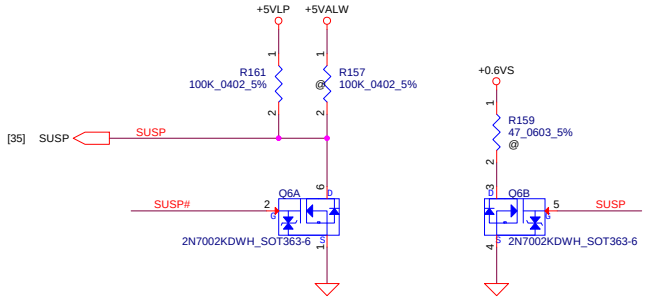
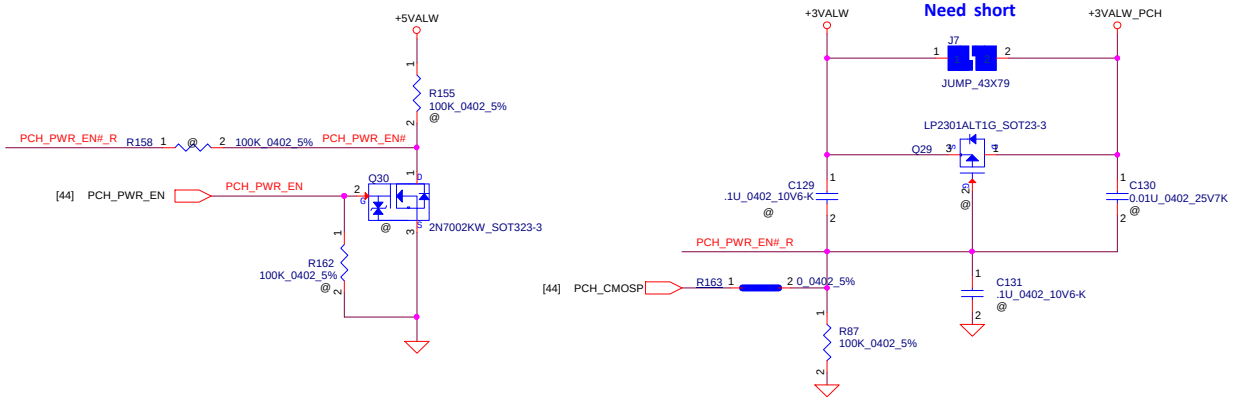
+5VALW to +5VS

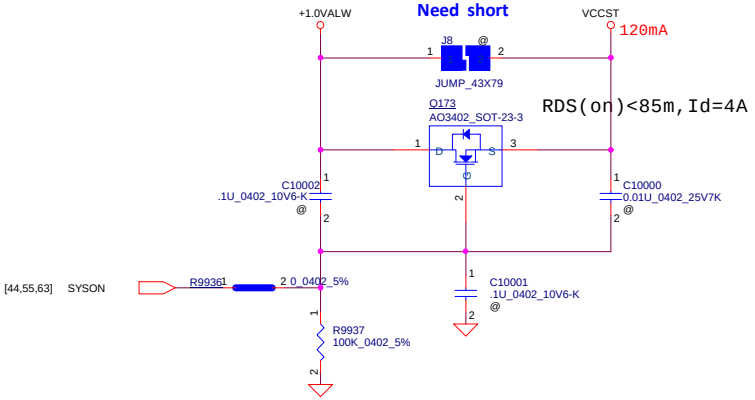
No function field

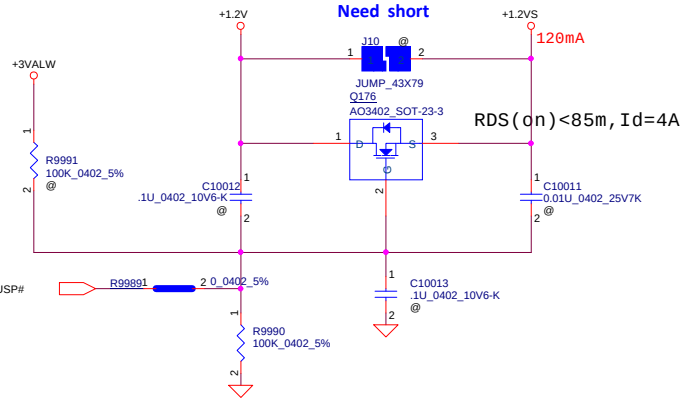


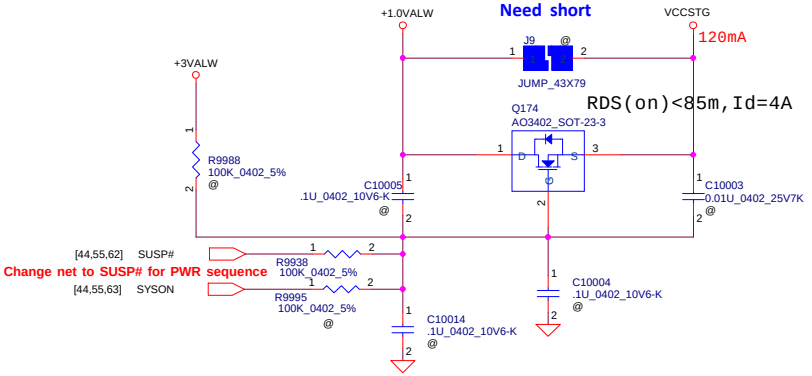


LP2301ALT1G
Rds=110mohm @
VGS=4.5V,ID=2.8A
VGS(th)=1V Max









Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	DC V TO VS INTERFACE		
Size: Custom	Document Number: BY511/BY710		Rev: 0.3
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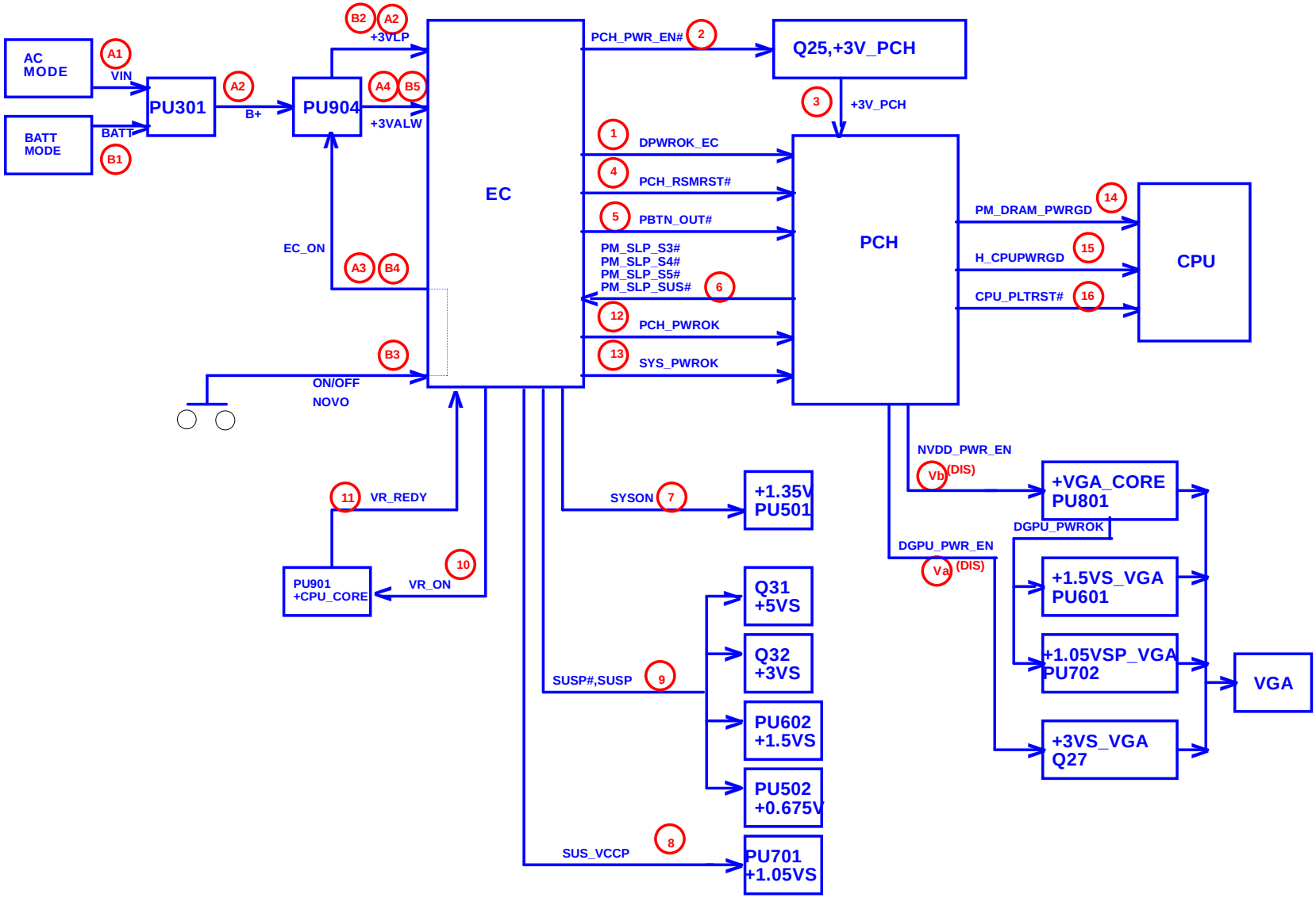

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Power sequence Block*

Size	Document Number	Rev
Custom	BY511/BY710	0.3

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

Virtual symbol

Size	Document Number	Rev
Custom	***BY511/BY710***	0.3

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H1 HOLEA — PAD_CT6P0B5P0D2P3
H2 HOLEA — PAD_CT6P0B5P0D2P3
H3 HOLEA — PAD_ShapeT9P0X11P0B5P0D2P3
H4 HOLEA — PAD_CT9P0D5P0
H5 HOLEA — PAD_CT9P0D5P0
H6 HOLEA — PAD_C6P0D6P0N
H7 HOLEA — PAD_ShapeT8p0x9p5B5P0D2P3
H8 HOLEA — PAD_CT7P0D4P0
H9 HOLEA — PAD_CT7P0D4P0

20150723_Change foot print to pad_ct5p0b6p0d3p2
by ME suggestion

H10 HOLEA — PAD_ShapeT10p5x9p0B5p0D2p3
H11 HOLEA — PAD_CT7P0D4P0
H12 HOLEA — pad_ct5p0b6p0d3p2
H13 HOLEA — PAD_C4P0D4P0N
H25 HOLEA — PAD_C4P0D4P0N

Follow layout

H14 HOLEA — CHASSIS1_GND, PAD_ShapeT10p15x7p64D4p6
H15 HOLEA — PAD_CB5P0D2P3
H16 HOLEA — PAD_CT5P0B8P0D3P3
H17 HOLEA — PAD_CT4P0B5P0D2P3
H26 HOLEA — PAD_C5P0D2P3

H18 HOLEA — PAD_CT6P0D2P6
H20 HOLEA — PAD_CT6P0D2P6

FD1 FD2 FD3 FD4 FD5 FD6

H19 HOLEA — PAD_CT9P0D5P0
H21 HOLEA — PAD_O2P9X2P3D2P9X2P3N
H22 HOLEA — PAD_O2P9X2P3D2P9X2P3N
H24 HOLEA — PAD_O2P9X2P3D2P9X2P3N

H23 HOLEA — Pad_C2p3D2p3N

SH1 ME@ — SPRING_FINGER_6.2X1.64
SH2 ME@ — SPRING_FINGER_6.2X1.64
SH3 ME@ — SPRING_FINGER_6.2X1.64
SH4 ME@ — SPRING_FINGER_6.2X1.64
SH5 ME@ — SPRING_FINGER_6.2X1.64
SH6 ME@ — SPRING_FINGER_6.2X1.64

+VGA_CORE — C135 .1U_0402_10V6-K EMC_NS@
+3VS — C136 .1U_0402_10V6-K EMC_NS@
+5VALW — C137 .1U_0402_10V6-K EMC_NS@
+3VALW — C138 .1U_0402_10V6-K EMC_NS@

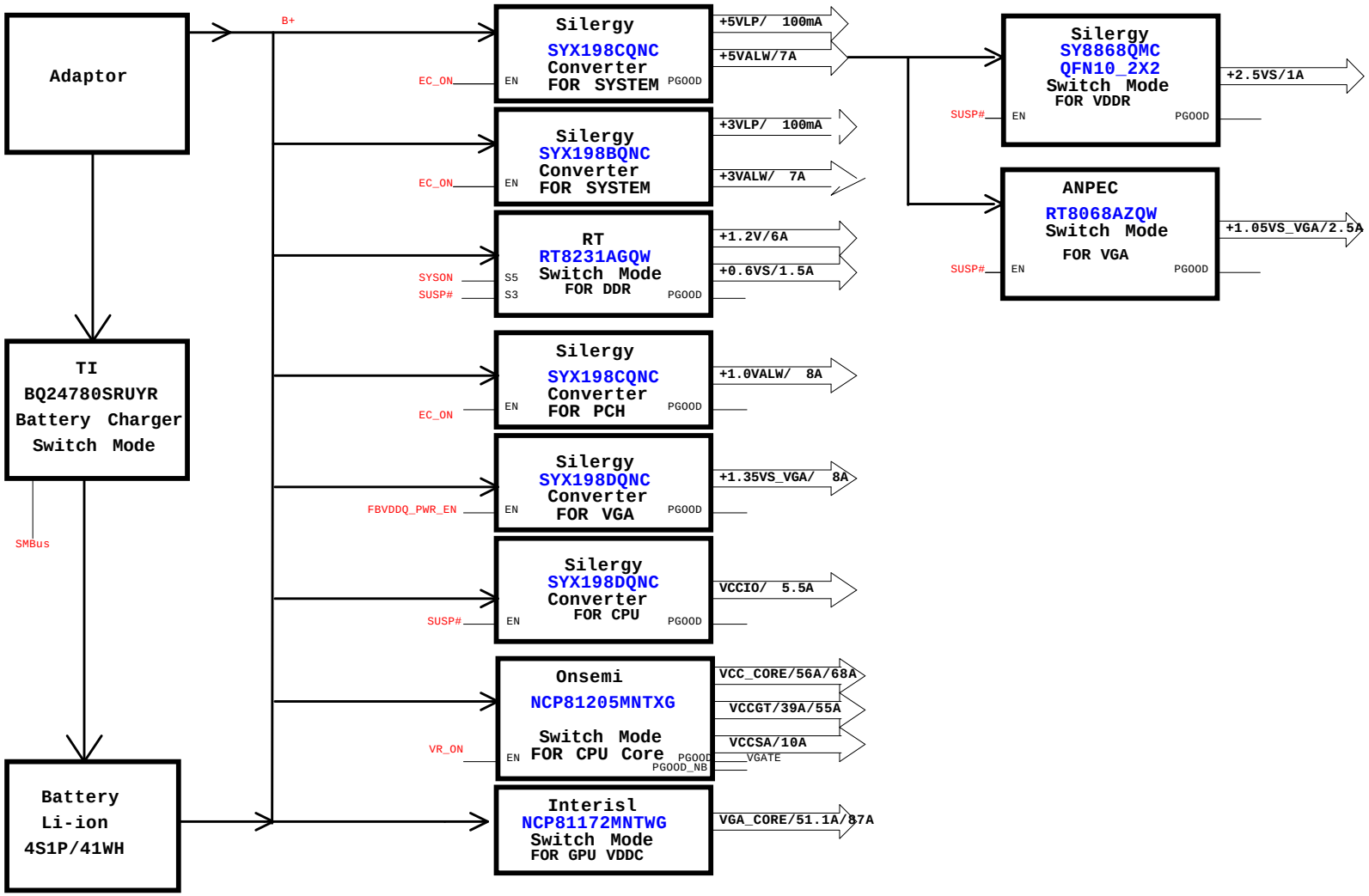
For EMC

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Hole*

Size	Document Number	Rev
B	BY511/BY710	0.3

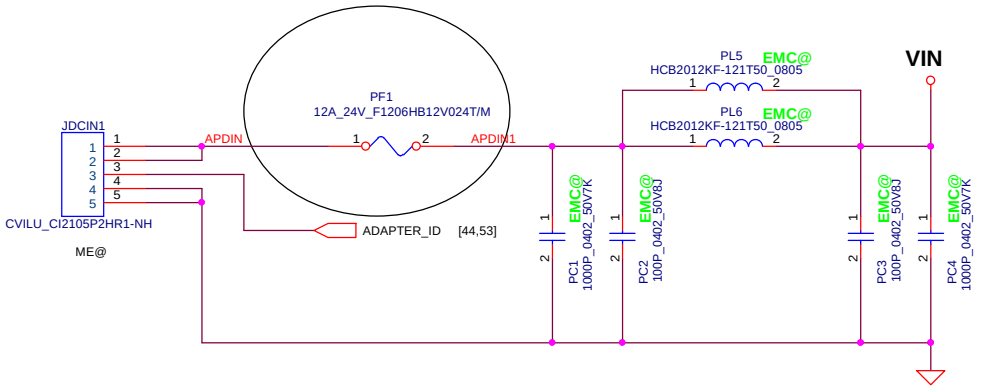
Date: Friday, July 31, 2015 Sheet 49 of 66

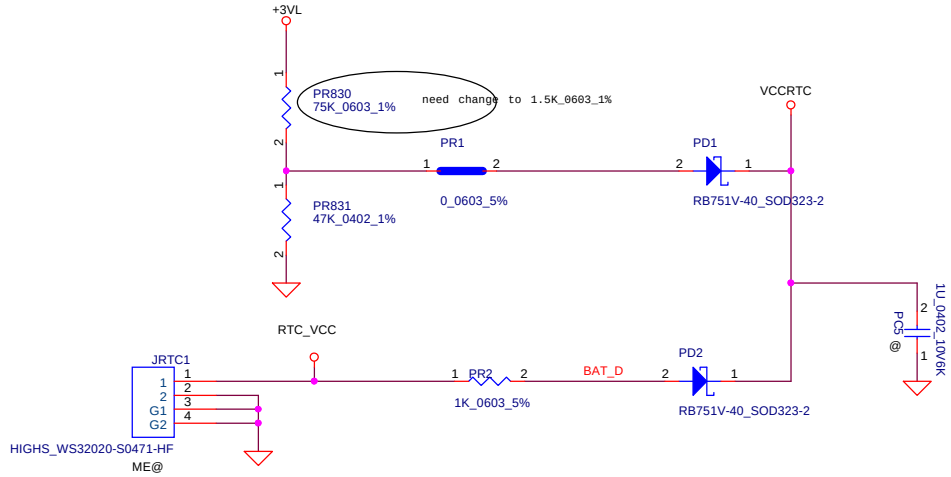


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **Power Diagram**

Size: Custom	Document Number: BY511/BY710	Rev: 0.3
Date: Friday, July 31, 2015	Sheet 50 of 66	



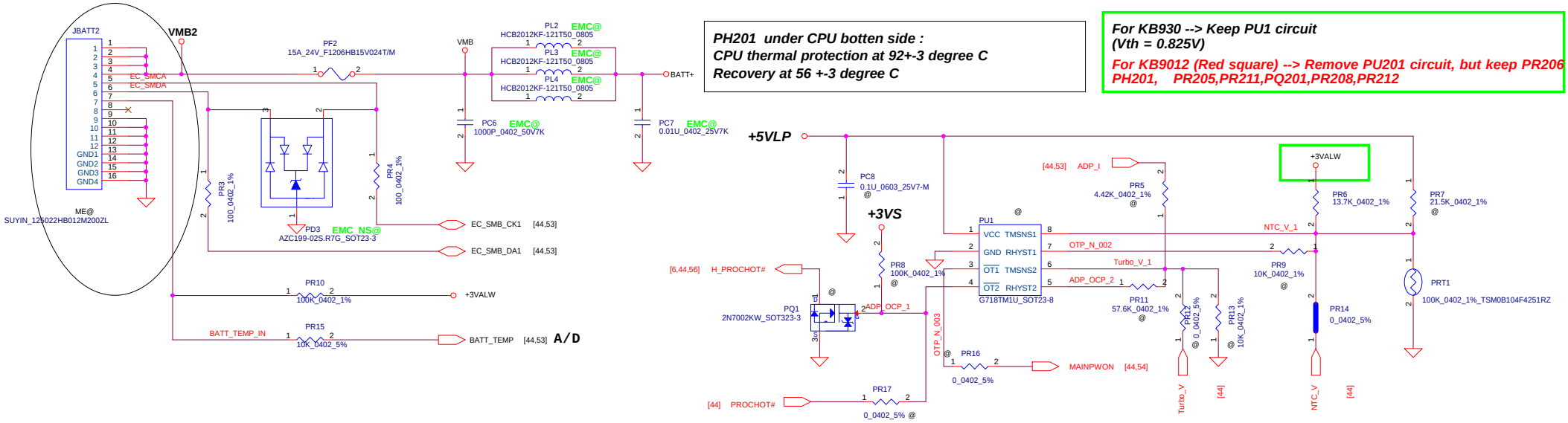


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: DCIN / RTC

Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 51 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: BATTERY CONN/OTP

Size	Document Number	Rev
Custom	BY511/BY710	0.3

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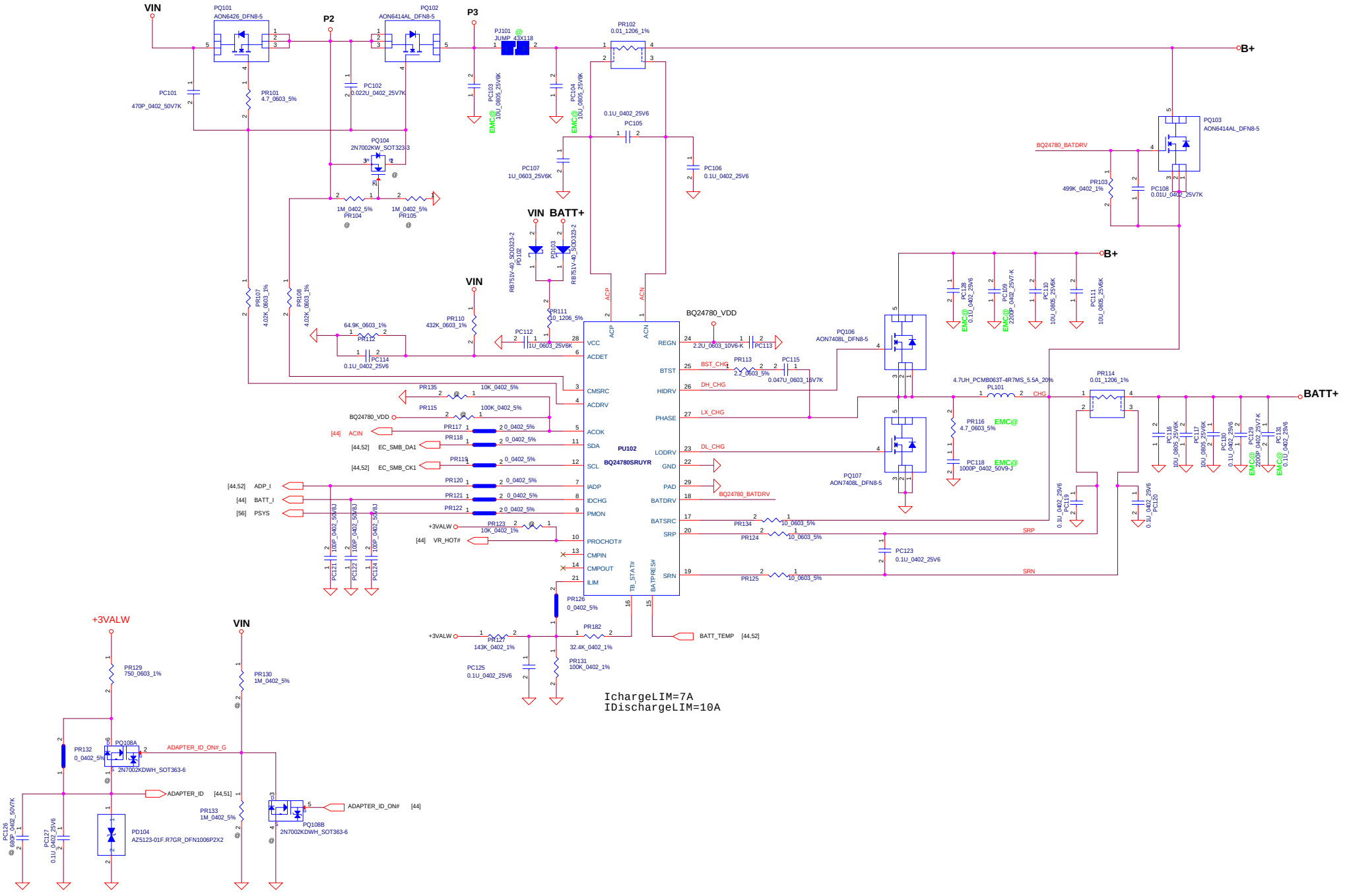
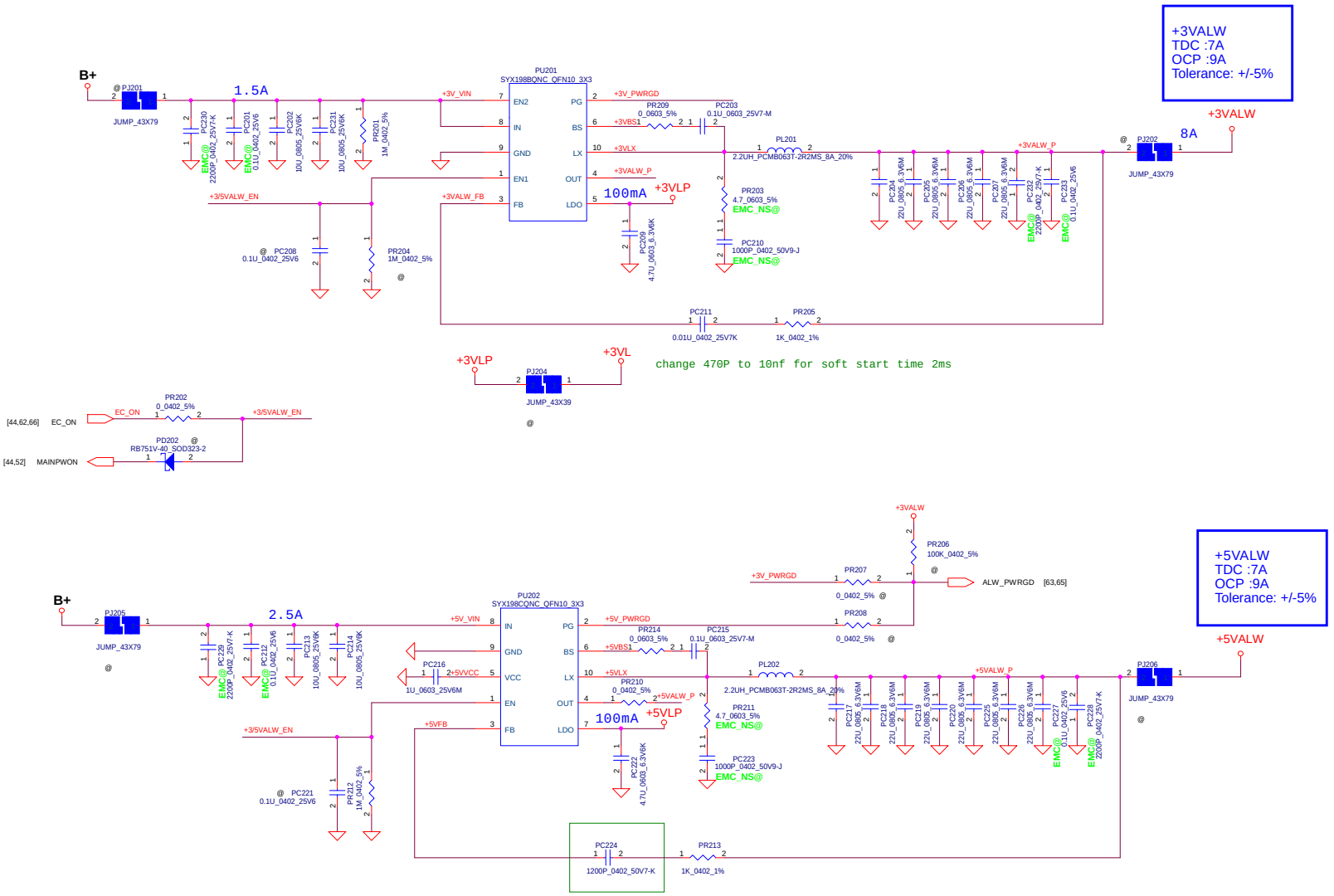


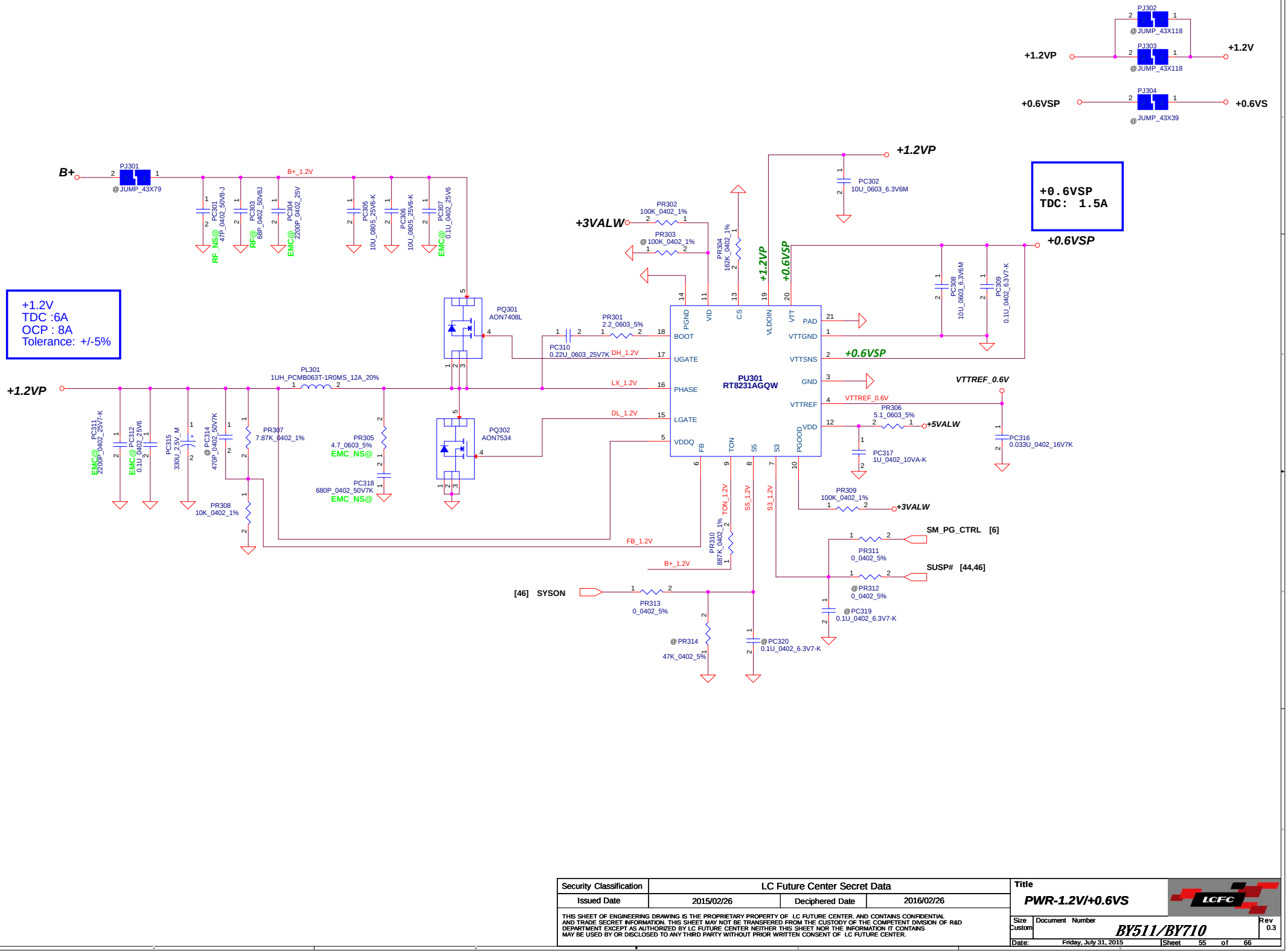
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	CHARGER		
Size	Document Number		Rev
Custom	BY511/BY710		0.3
Date:	Friday, July 31, 2015	Sheet	53 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

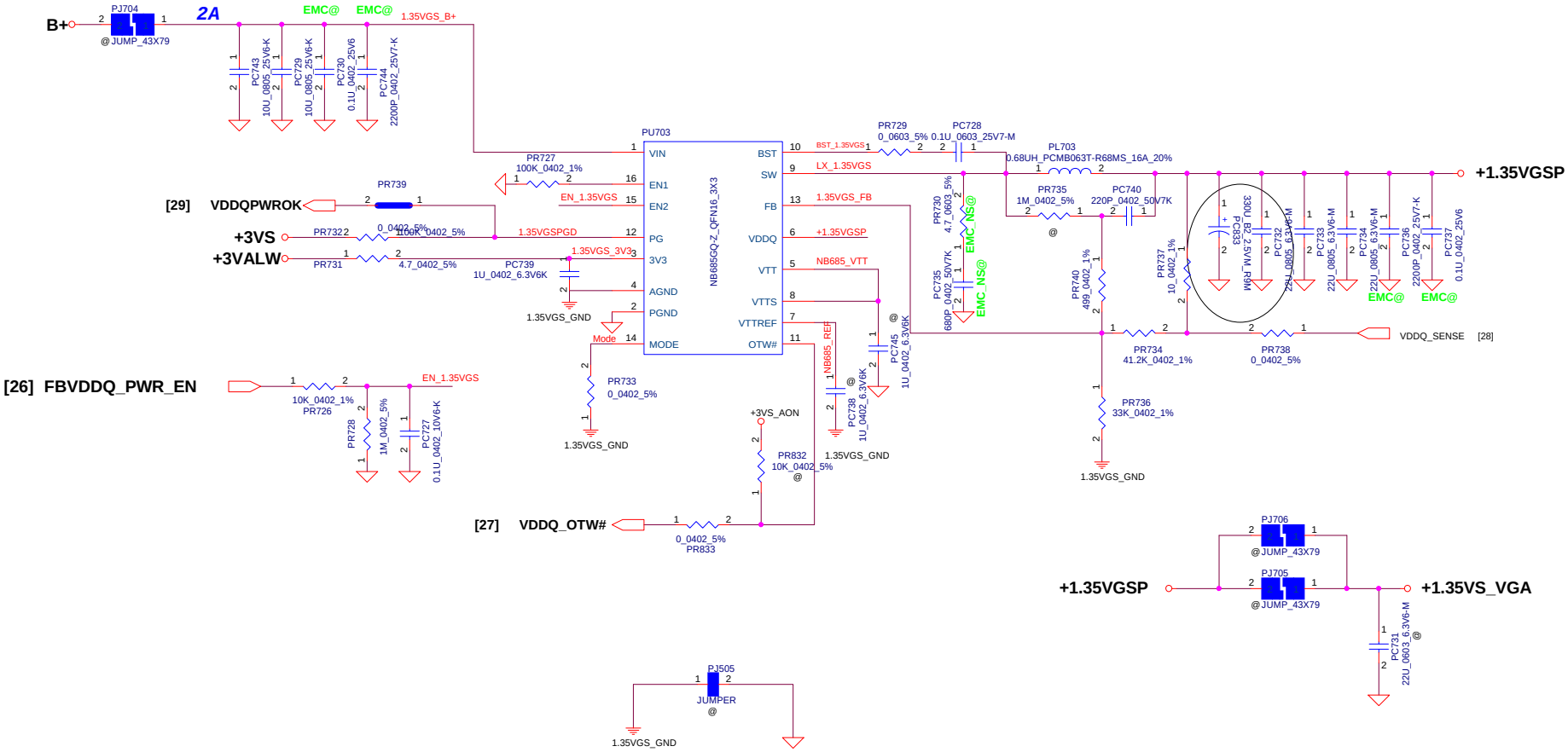
Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	BY511/BY710		0.3
Date:	Friday, July 31, 2015	Sheet	54 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PWR-1.2V/+0.6VS

Size: Custom	Document Number: BY511/BY710	Rev: 0.3
Date: Friday, July 31, 2015	Sheet 55 of 66	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *1.35VS/+0.675VS*

Size	Document Number	Rev
Custom	*BY511/BY710*	0.3

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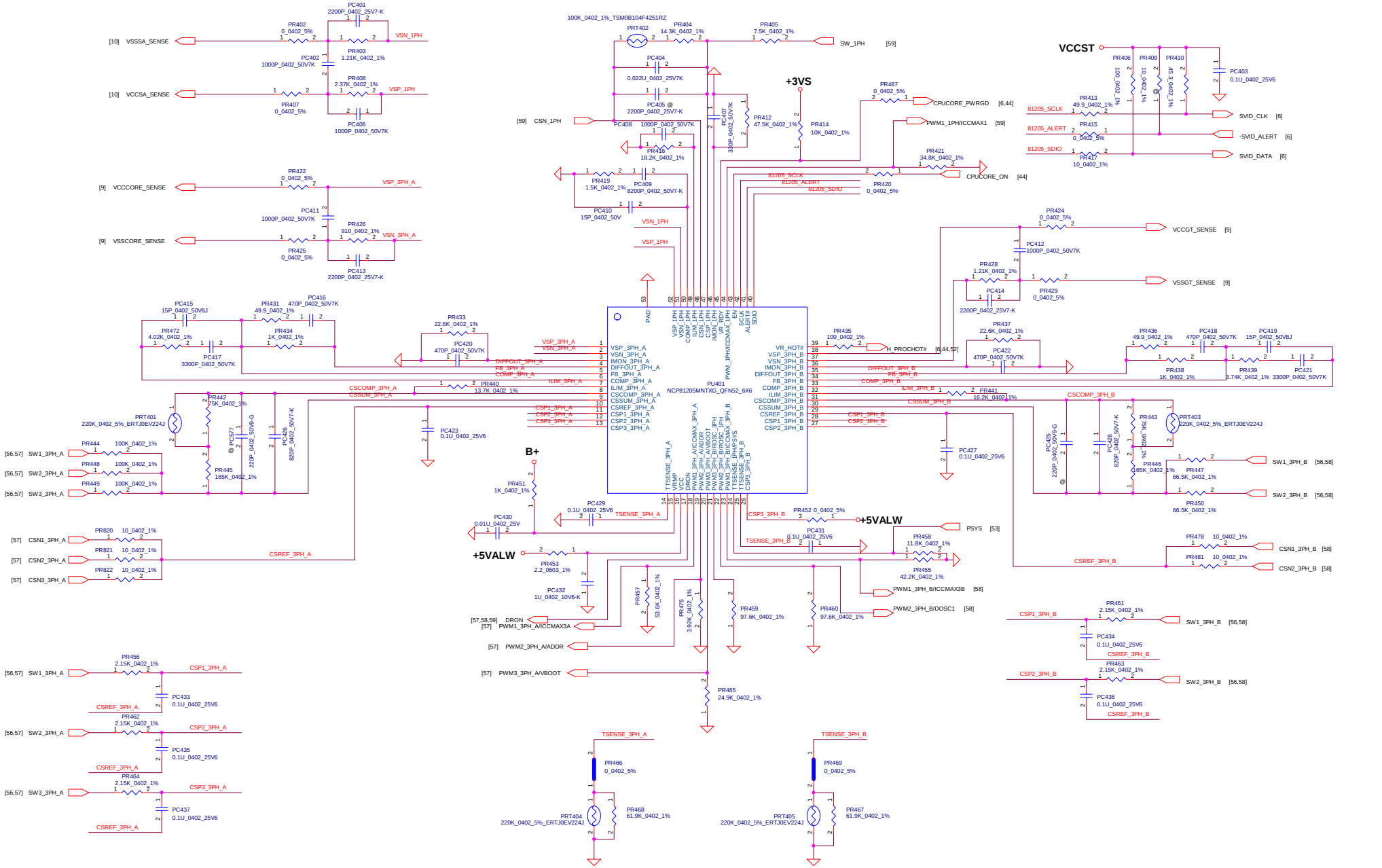

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Issued Date	2015/02/26	Deciphered Date	2016/02/26

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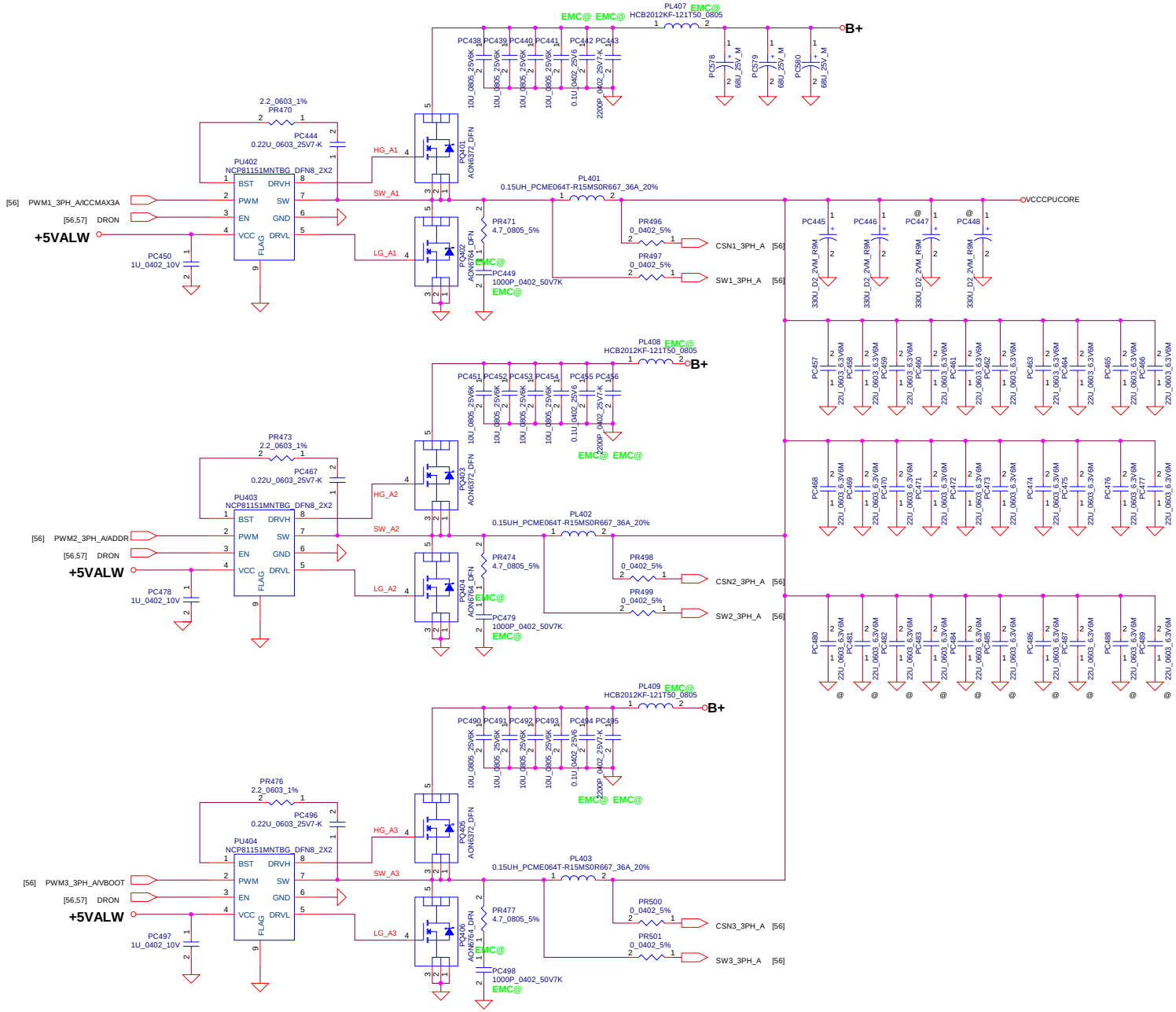
Title: DC/DC VCCCPUCORE(NCP81205)

Size	Document Number	Rev
Custom	BY511/BY710	0.3

Date: Friday, July 31, 2015 Sheet 56 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PWR-VCC_CORE**

Size	Document Number	Rev
Custom	BV511/BV710	0.3

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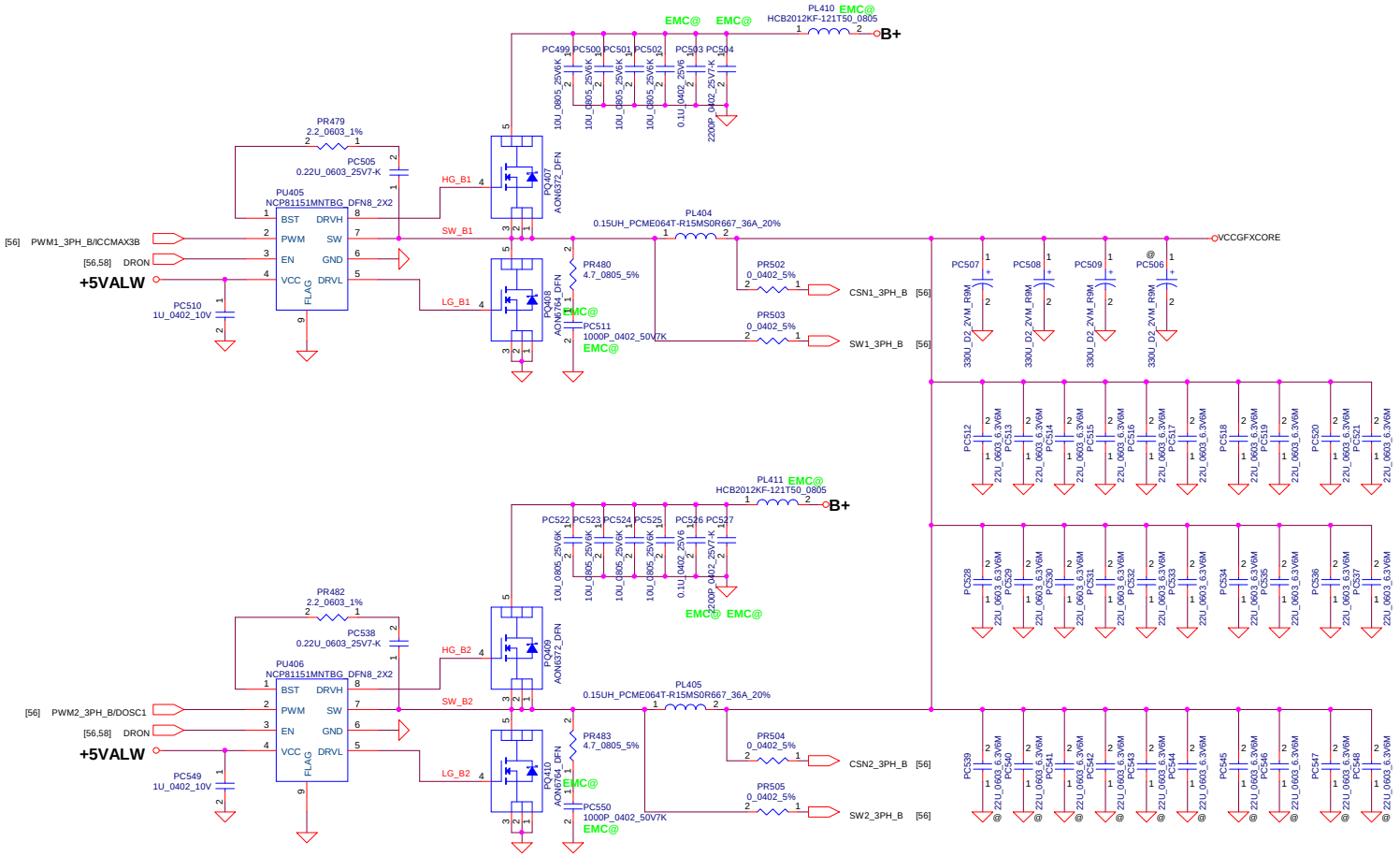

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PWR-VCCGT**

Size	Document Number	Rev
Custom	BY511/BY710	0.3

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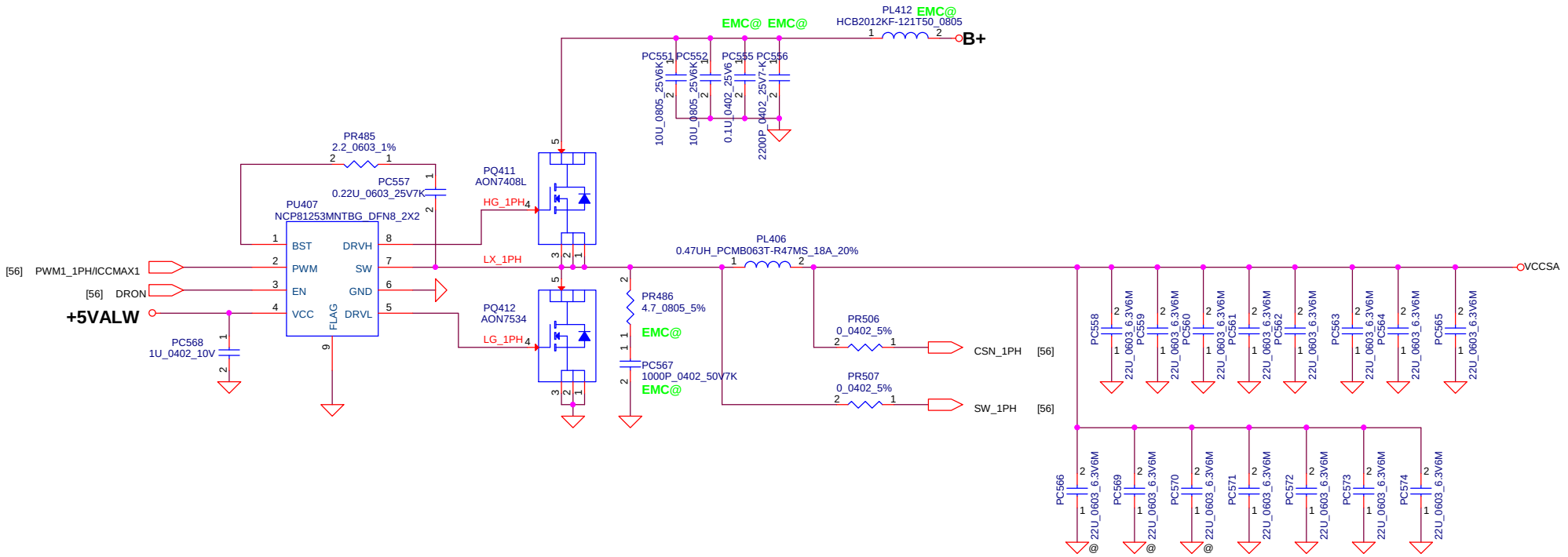

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PWR-VCCSA**

Size	Document Number	Rev
B	BY511/BY710	0.3

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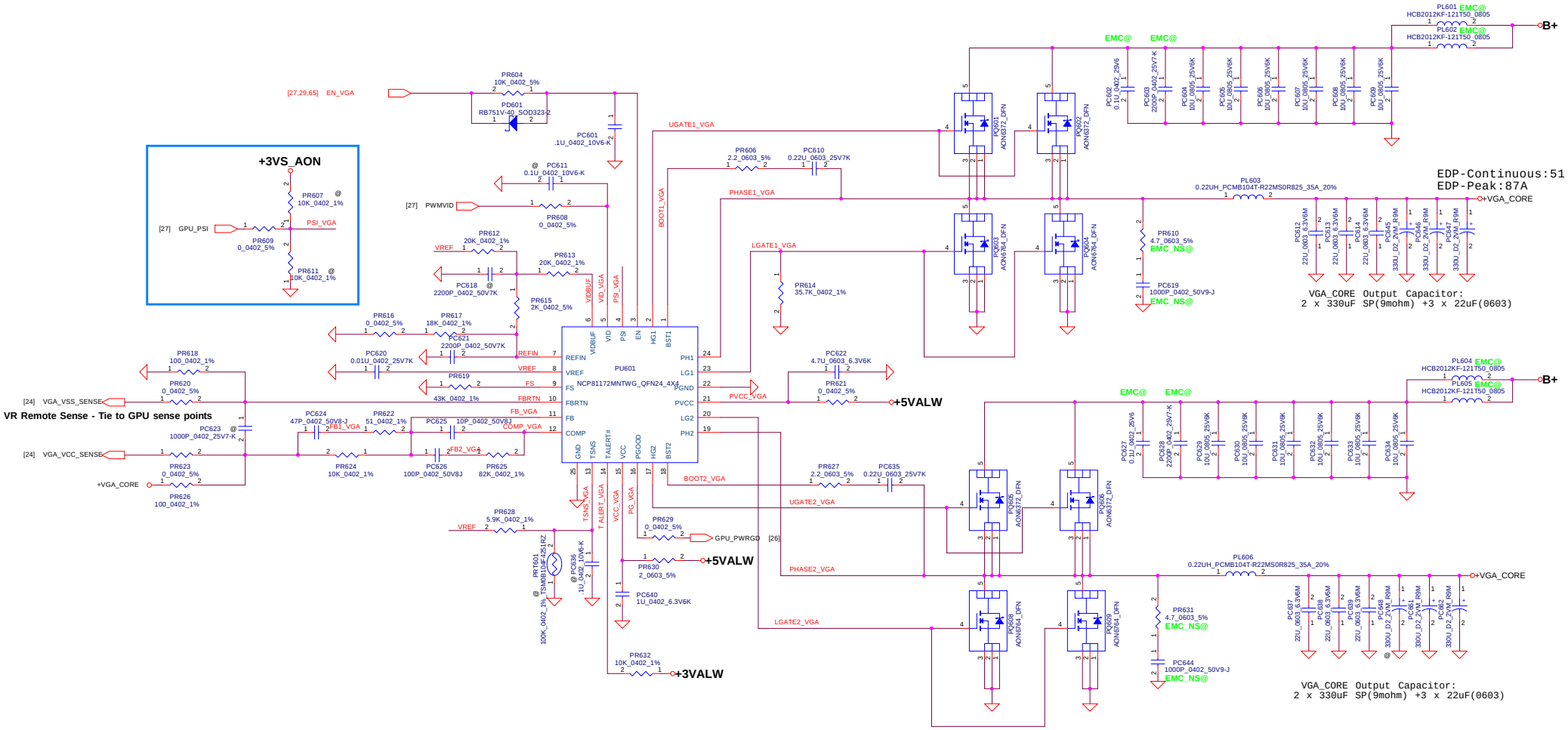

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PWR-VGA_CORE(NCP81174)		
Size	Document Number		Rev
Custom	BY511/BY710		0.3
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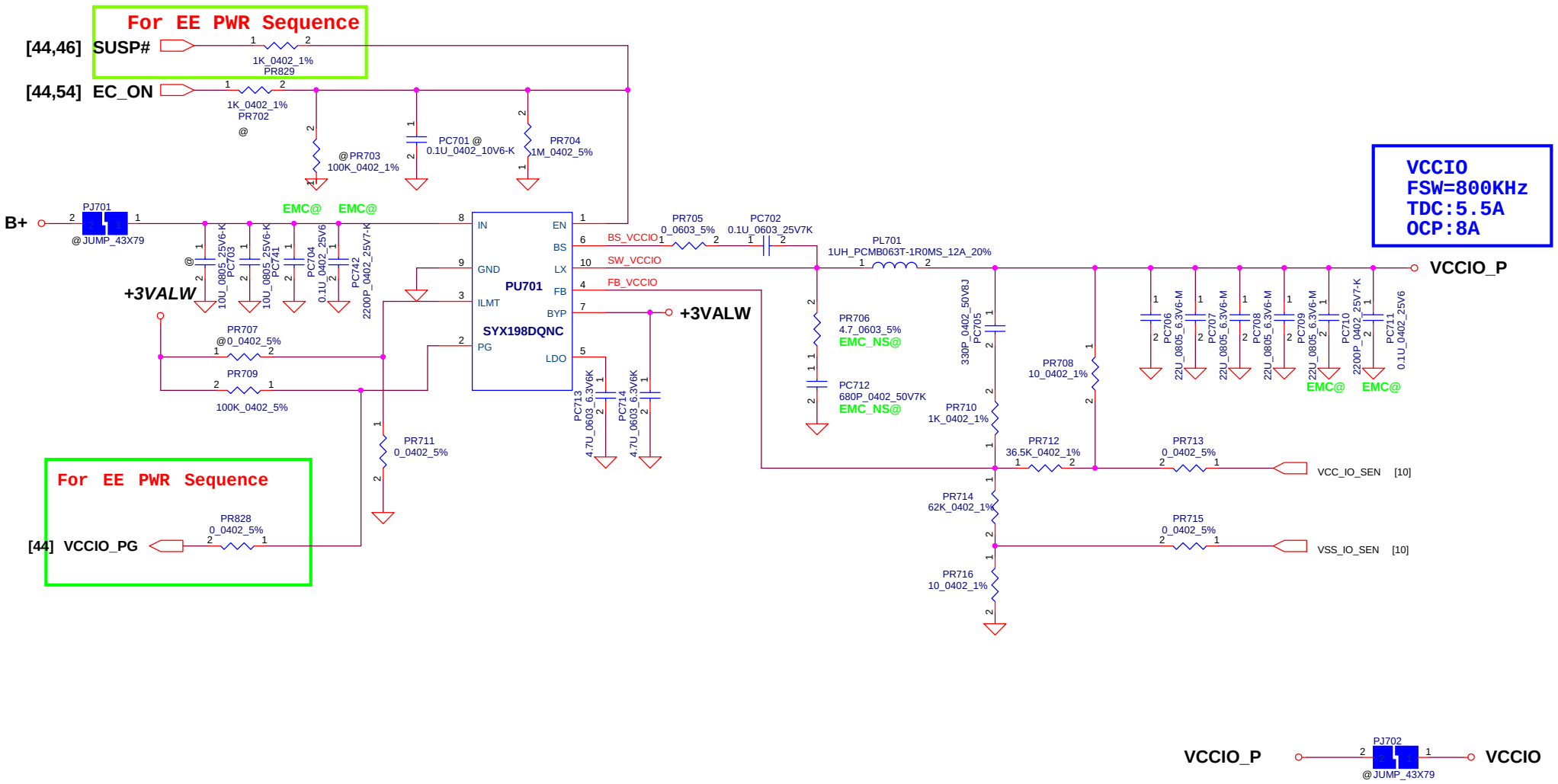
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

P61_PWR-VGA_CORE

Size	Document Number	Rev
C	***BY511/BY710***	0.3

Date: Friday, July 31, 2015 Sheet 61 of 66



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PWR-VCCIO

Size	Document Number	Rev
B	BY511/BY710	0.3

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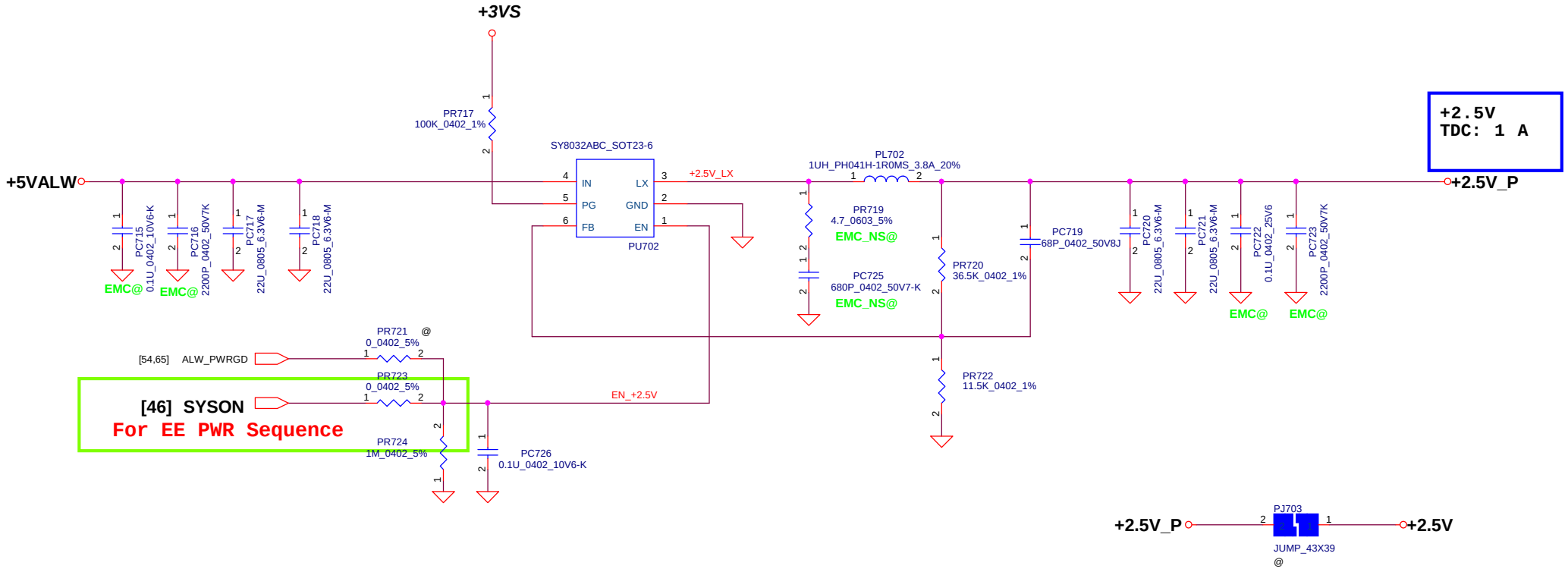

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PWR+2.5V

Size	Document Number	Rev
B	BY511/BY710	0.3

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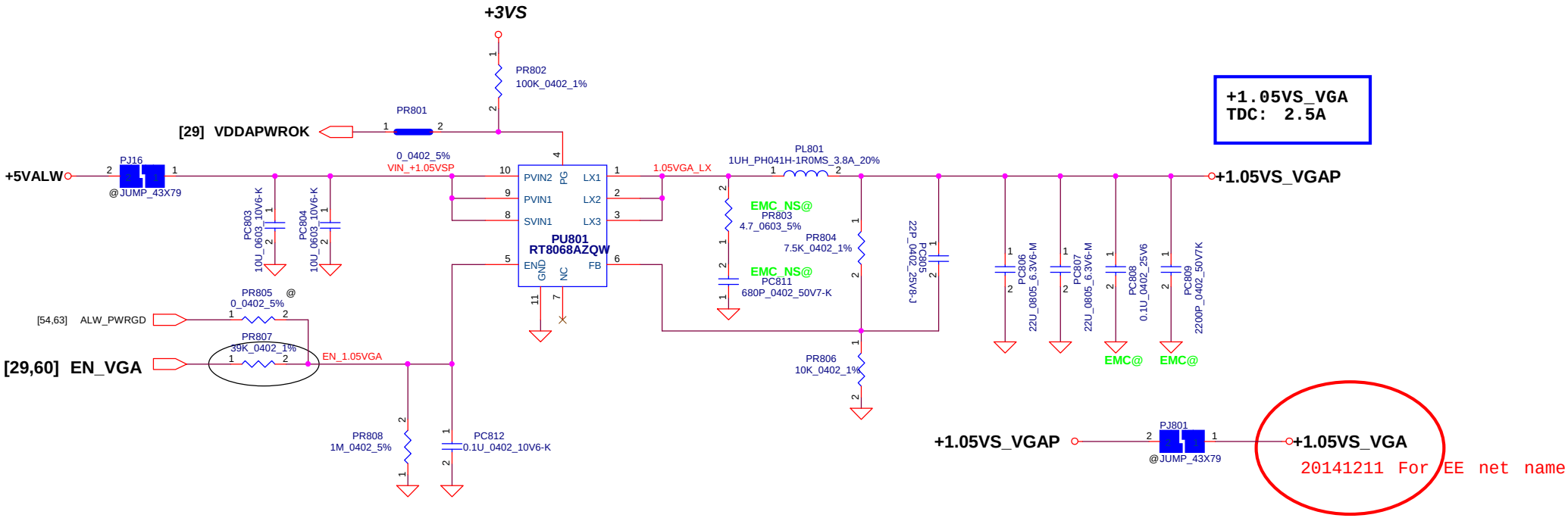

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *PWR-+1.05ALW*

Size	Document Number	Rev
B	*BY511/BY710*	0.3

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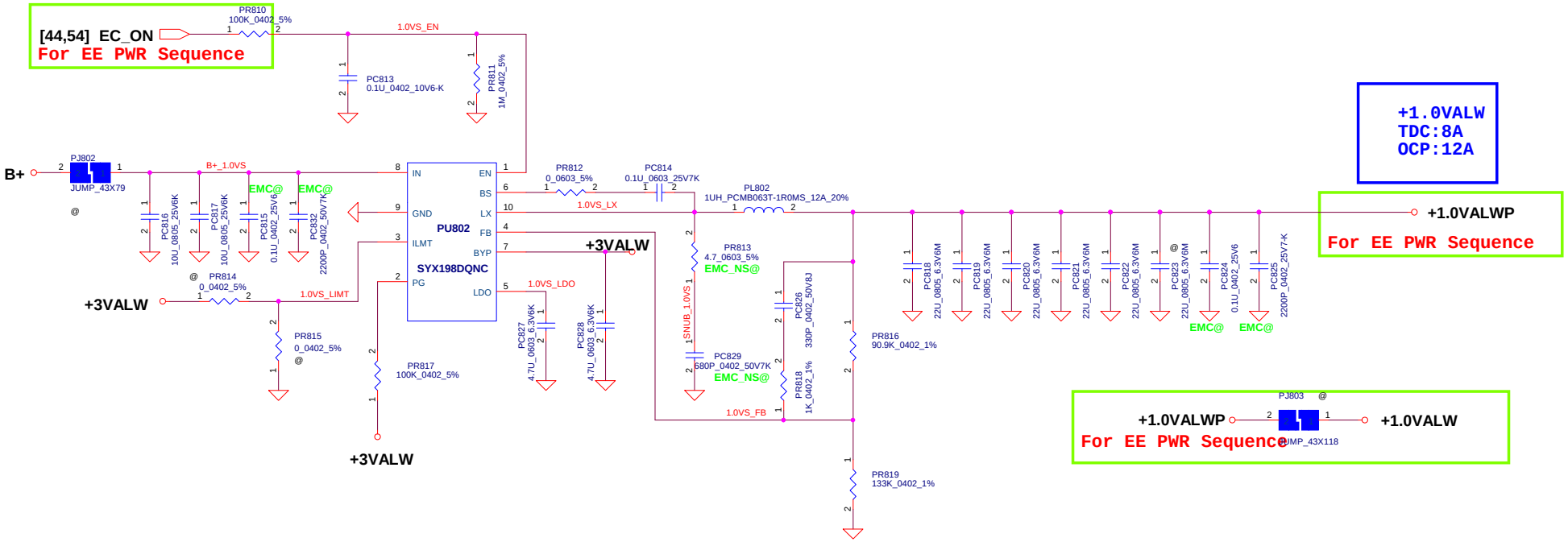

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *+1.0VS*

Size	Document Number	Rev
Custom	*BY511/BY710*	0.3

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