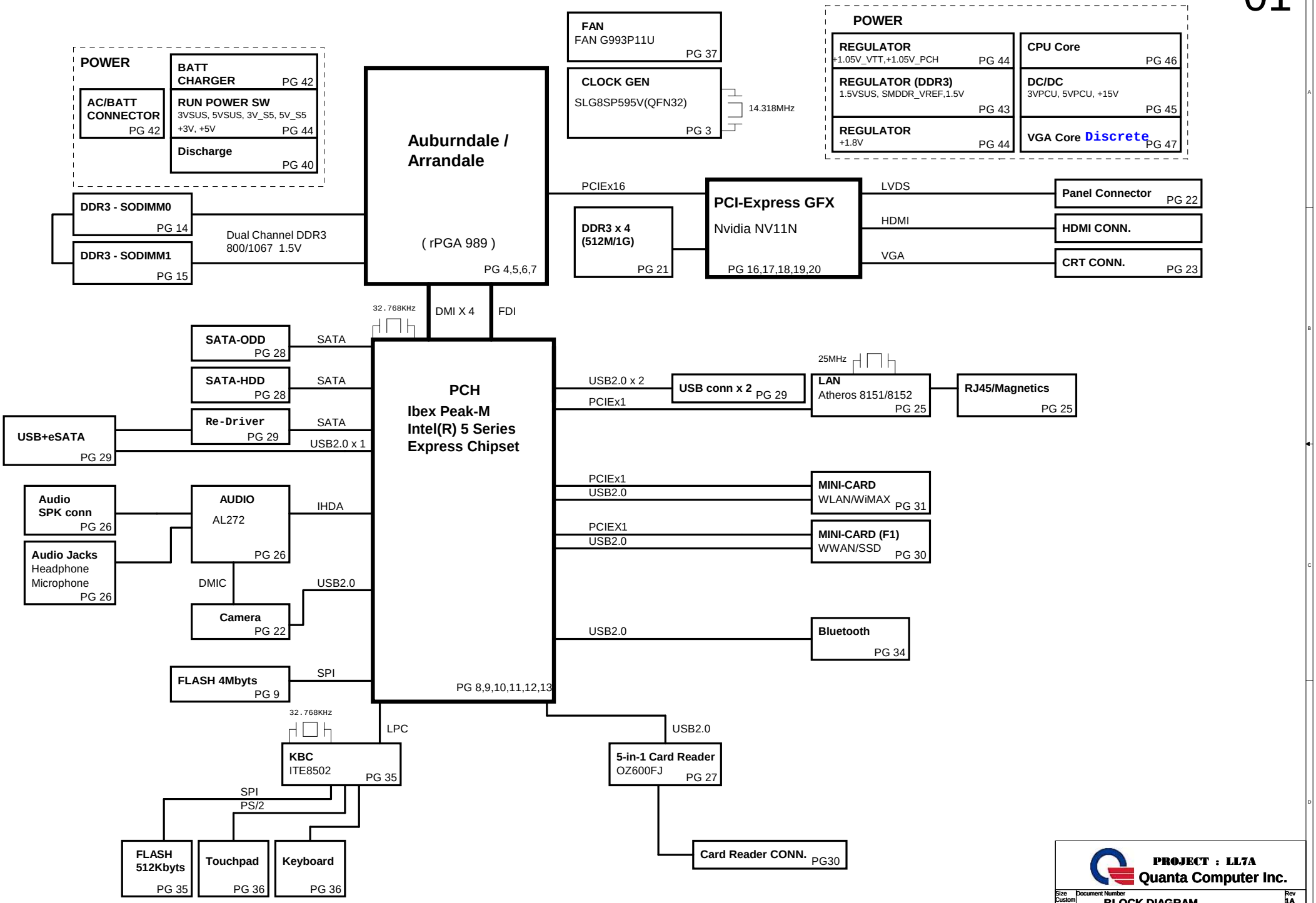

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Quanta Computer Inc.

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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	23,32,43,44,45,46,47,48,49,50	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	9,12,41	RTC		S0~S5
3VPCU	+3.3V	9,23,27,30,32,35,39,41,43,44,47	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	14,43,44,45,46,47,49,50	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	23,38,43,45,46,47	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	27,43	LAN POWER	LAN_ON	
5V_S5	+5V	12,29,30,43	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,9,10,11,12,43,52	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	23,39,43,48	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	14,15,30,34,41,43,49	SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5VSUS	+1.5V	4,6,14,15,43,45,46,49,50	SODIMM POWER	SUSON	S0~S3
0.75VSMDDR_VTERM	+0.75V	14,15,43,45	DDR3 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,18,23,24,25,26,28,35,37,41,43,44	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,8,9,10,11,12,14,15,17,23,25,26,27,28,29,30,31,32,33,34,36,37,38,39,40,41,43,44,45,46,47,48,50,52	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,12,17,18,21,22,33,43,50	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	12,18,19,20,31,32,34,45,46	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V_VTT	+1.05V	4,6,11,12,43,46,48,52	AuBurndale VTT POWER	MAIN_ON	S0
+1.05V_PCH	+1.05V	3,10,12,43,46,52	PCH CORE POWER	1.05V_RUN_ON	S0
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,43,49	VGA CORE POWER	GFXVR_EN	S0
VCC_CORE		6,43,48	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	23	LCD Power	ENVDD	S0
+5V_ODD	+5V	28	ODD Power	MAIN_ON	S0
+5V_HDD	+5V	28	HDD Power	MAIN_ON	S0
BAT-V	+10V~+17V	44	MAIN BATTERY	CHG_PBATT	S0~S5

(4,6,8,9,10,11,12,35,38,40,42) +1.05V_VTT
(27,28,37) +1.5V
(4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V

25mA
+1.05V_VTT +VDDIO_CLK
L16 HCB1608KF-181T15_6
C235 0.1U/10V/X5R_4
C229 0.1U/10V/X5R_4
C223 4.7U/6.3V/X5R_6
C231 *10U/6.3V/X5R_8S
Place each 0.1uF cap close to pin

150mA
+3V +VDDSE_CLK
L19 HCB1608KF-181T15_6
C242 4.7U/6.3V/X5R_6
C240 0.1U/10V/X5R_4
C268 0.1U/10V/X5R_4
Place each 0.1uF cap close to pin

150mA
+3V +VDDCORE_CLK
L18 *HCB1608KF-181T15_6
+1.5V
L17 HCB1608KF-181T15_6
C224 4.7U/6.3V/X5R_6
C228 0.1U/10V/X5R_4
C269 0.1U/10V/X5R_4
C230 0.1U/10V/X5R_4
Place each 0.1uF cap close to pin

Y3
XTAL_IN 1 2 XTAL_OUT
14.318MHZ
C238 33P/50V/NPO_4
C233 33P/50V/NPO_4

U7
QFN32
9LVS3197

+VDDSE_CLK → VDD_LCD, VDD_REF
+VDDCORE_CLK → C270 *0.047U/10V/X7R_4 → VDD_USB, VDD_SRC, VDD_CPU
+VDDIO_CLK → C208 *0.047U/10V/X7R_4 → VDD_CPU_IO, VDD_SRC_IO
(9,13,14) CGDAT_SMB → SDATA
(9,13,14) CGCLK_SMB → SCLK
+3V (9) CLK_ICH_14M → R129 10K_4, R137 33_4, C253 *10P/50V/C0G_4 → CPU_STOP#
CPU_SEL → REF_0/CPU_SEL
CK_PWRGD_R → CK_PWRGD/PD#_3.3
XTAL_OUT → XOUT
XTAL_IN → XIN
VSS_SATA, VSS_USB, VSS_LCD
CPU-0, CPU-0#, CPU-1, CPU-1#
DOT96T_LPR, DOT96C_LPR
SRC-1, SRC-1#
SATA, SATA#
27MHz_nonSS, 27MHz_SS
GND, VSS_REF, VSS_CPU, VSS_SRC

RP3 *4P2R-S-0: CLK_BUF_BCLK_P, CLK_BUF_BCLK_N → CLK_BUF_BCLK_P (9), CLK_BUF_BCLK_N (9)
RP6 *4P2R-S-0: CLK_BUF_DREFCLK, CLK_BUF_DREFCLK# → CLK_BUF_DREFCLK (9), CLK_BUF_DREFCLK# (9)
RP4 *4P2R-S-0: CLK_BUF_PCIE_3GPLL, CLK_BUF_PCIE_3GPLL# → CLK_BUF_PCIE_3GPLL (9), CLK_BUF_PCIE_3GPLL# (9)
RP5 *4P2R-S-0: CLK_BUF_DREFSSCLK, CLK_BUF_DREFSSCLK# → CLK_BUF_DREFSSCLK (9), CLK_BUF_DREFSSCLK# (9)
R146 EV@33_4, R145 EV@33_4: CLK_VGA_27M_NOSS, CLK_VGA_27M_SS → CLK_27M_NOSS (17), CLK_27M_SS (17)
C250 *EV@10P/50V/C0G_4, C252 *EV@10P/50V/C0G_4

Place R8044 within 0.5" of C/G

Discrete only

+3V
R138 *10K/F_4
CPU_SEL
R141 10K/F_4

	0	
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

EMI request
+3V: C227 0.1U/10V/X5R_4, C471 0.1U/10V/X5R_4, C689 0.1U/10V/X5R_4, C685 0.1U/10V/X5R_4
+1.05V_VTT: C672 0.1U/10V/X5R_4, C357 0.1U/10V/X5R_4, C377 0.1U/10V/X5R_4, C287 0.1U/10V/X5R_4, C393 0.1U/10V/X5R_4, C387 0.1U/10V/X5R_4
VIN: C236 0.1U/25V/X5R_4

+3V
R131 1K/F_4
CK_PWRGD_R
Q8 2N7002E
(40) VR_PWRGD_CLKEN#
R127 100K/F_4

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	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

JTAG MAPPING

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

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C	PROCESSER 1/4(HOST&PEG)	1A

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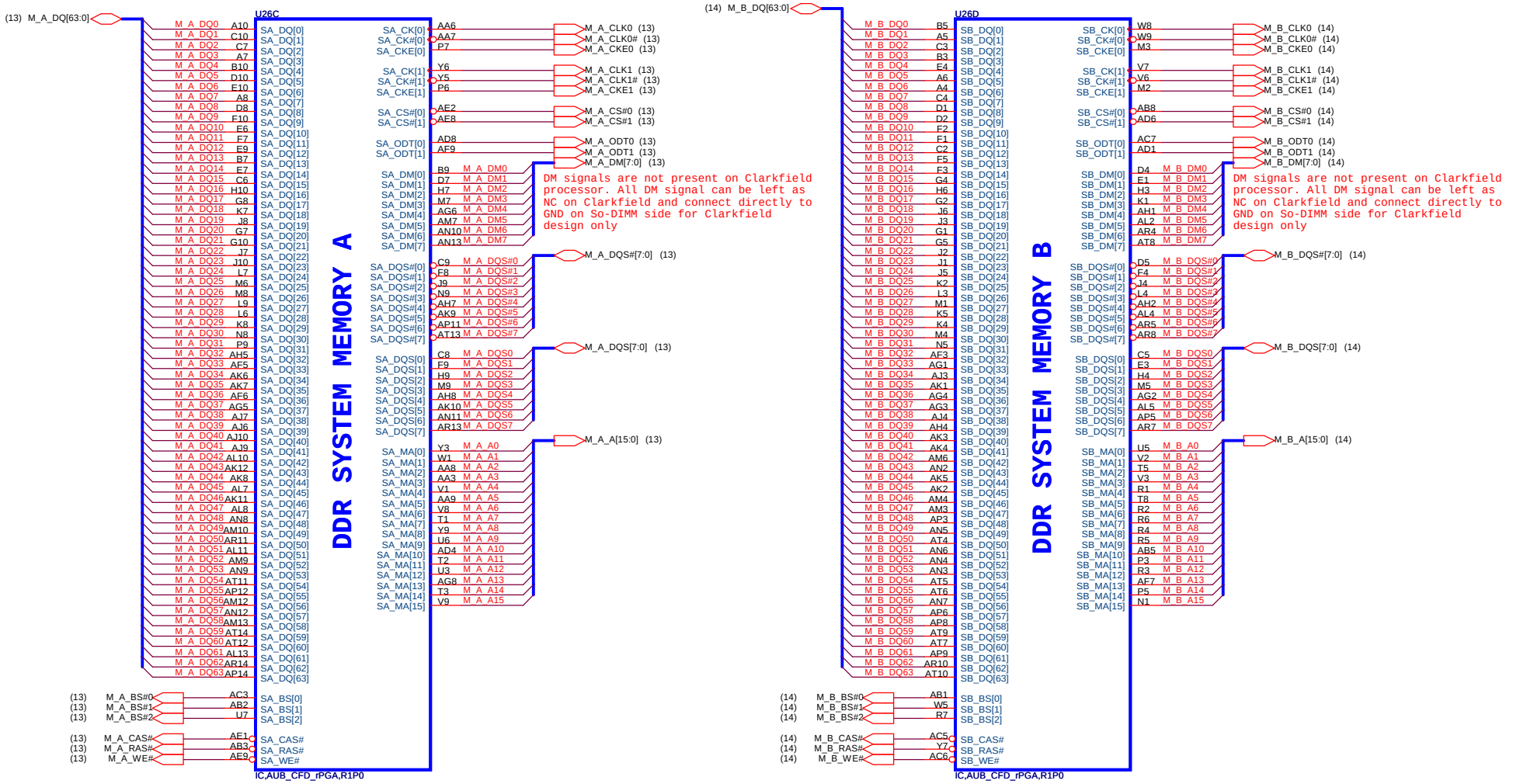
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT : LL7A

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18A

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

U26F

CPU CORE SUPPLY POWER 1.1V RAIL POWER

+VCORE

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

C183 C145 C602 C141 C187 C164 C180 C182 C600 C177 C166 C605 C601 C167 C179 C580 C188 C169 C148 C185 C186 C170 C175 C604 C173 C178 C603 C191 C165 C194 — 10U/6.3V/X5R_8; 0.1U/10V/X5R_4

*0.047U/16V/X7R_4 C189 C192 C193 — 2 — 1

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32 — +1.05V_VTT

C656 C653 C645 C660 C195 C655 C196 C657 C174 C654 — 10U/6.3V/X5R_8

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44 — +1.05V_VTT

C190 C197 — 10U/6.3V/X5R_8

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

CPU VIDS

PSI# — H_PSI#

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6] PROC_DPRSLPVR — CPU_VID0 CPU_VID1 CPU_VID2 CPU_VID3 CPU_VID4 CPU_VID5 CPU_VID6 DPRSLPVR (40)

VTT_SELECT

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

SENSE LINES

ISENSE — I_MON (40)

VTT_SENSE VSS_SENSE_VTT — VTT_SENSE (38) — T30

R460 100/F_4 — +VCORE

VCC_SENSE VSS_SENSE — VCCSENSE (40) VSSSENSE (40)

R461 100/F_4

IC,AUB_CFD_rPGA,R1P0

UMA only

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

+VGACORE_IGPU — C647 C643 C634 C637 — 10U/6.3V/X5R_8

	DIS	UMA
Ra	0 ohm	NA

Ra R474 *EV@0_8

U26G

POWER

GRAPHICS

SENSE LINES — VAXG_SENSE VSSAXG_SENSE — VCC_AXG_SENSE (42) VSS_AXG_SENSE (42)

GRAPHICS VIDs

GFX_VID[0] GFX_VID[1] GFX_VID[2] GFX_VID[3] GFX_VID[4] GFX_VID[5] GFX_VID[6] — GFXVR_VID_0 GFXVR_VID_1 GFXVR_VID_2 GFXVR_VID_3 GFXVR_VID_4 GFXVR_VID_5 GFXVR_VID_6 (42)

GFX_VR_EN — R473 Rc IV@4.7K_4

GFX_VR_EN — GFXVR_EN (35,42)

GFX_DPRSLPVR — R471 Rd IV@0_4 — GFXVR_DPRSLPVR (42)

GFX_IMON — R79 IV@0_4 — GFXVR_IMON (42)

R76 Re EV@1K/J_4

Rf

DDR3 - 1.5V RAILS

2A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

C215 C217 C218 C216 C213 C214 C212 — 1U/6.3V/X5R_4; 10U/6.3V/X5R_8

C202 *330U/2V_7343

+1.5VSUS

C220 C210 C211 C221 — 0.1U/10V/X5R_4

+1.5VSUS_L

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT0_63 VTT0_64 VTT0_65 VTT0_66 VTT0_67 VTT0_68 — +1.05V_VTT

C651 C652 C636 C639 — 10U/6.3V/X5R_8

1.8V

VCCPLL1 VCCPLL2 VCCPLL3 — +1.8V

C168 — 10U/6.3V/X5R_8
C153 — 4.7U/6.3V/X5R_6
C163 — 2.2U/6.3V/X5R_6
C157 — 1U/6.3V/X5R_4
C624 — 1U/6.3V/X5R_4

FDI PEG & DMI

VTT1_45 VTT1_46 VTT1_47 — J24 J23 H25

C181 C633 — 10U/6.3V/X5R_8 — +1.05V_VTT

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58 — K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

C661 C649 C648 C184 — 10U/6.3V/X5R_8 — +1.05V_VTT

IC,AUB_CFD_rPGA,R1P0

for S3 power reduction

+1.5VSUS

Q11 AON6718L

(35,37) MAIND — R125 *0F_2512

(13,35) MAINON_G

R120 220/F_4

Q6 2N7002E

+1.5VSUS_L

C151 C156 C144 C147 C140 C136 C117 C578 C579 C155 — *10U/6.3V/X5R_8

+VCORE

Lenovo Request

H_PSI# — R434 *0_4 — Q31 MMBT3906LT1G — R404 1K/F_4 — H_PSI#_PR (40)

(30) PSI_ON# — Q29 MMBT3904LT1G

CPU_VID0 CPU_VID1 CPU_VID2 CPU_VID3 CPU_VID4 CPU_VID5 CPU_VID6 DPRSLPVR H_PSI# — R438 R437 R451 R450 R452 R453 R439 R440 R454 R455 R457 R456 R441 R442 R459 R458 R444 R443 — 1K/J_4 *1K/J_4 — +1.05V_VTT

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

(35,42) +VGACORE_IGPU
(35,40) +VCORE
(3,4,8,9,10,11,12,35,38,40,42) +1.05V_VTT
(4,13,14,35,37,41) +1.5VSUS
(12,35,38,41) +1.8V

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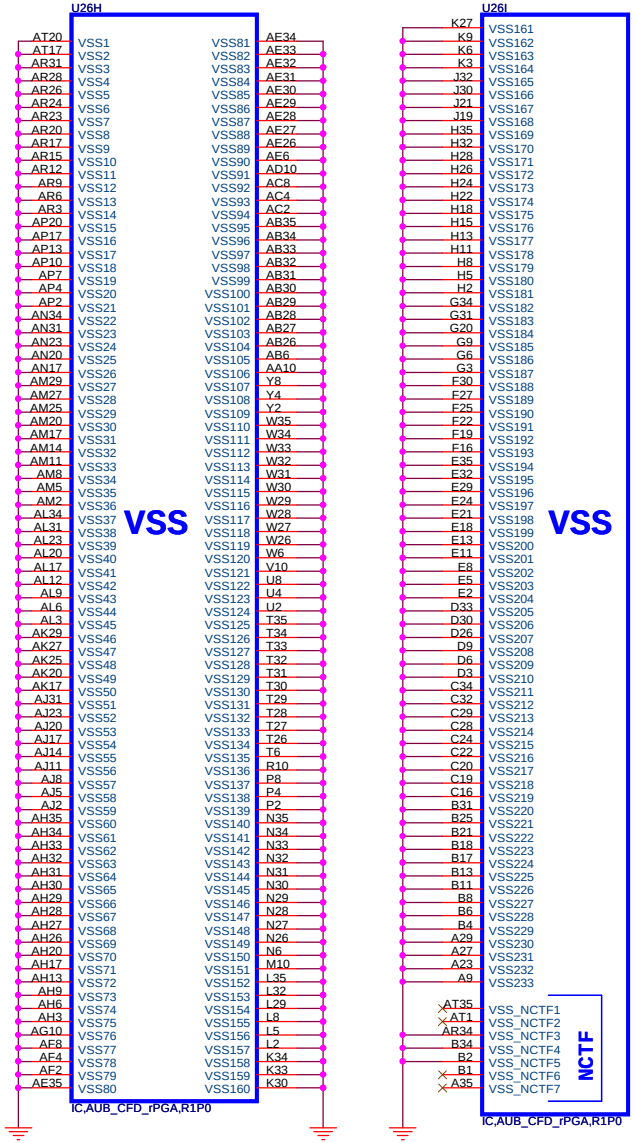
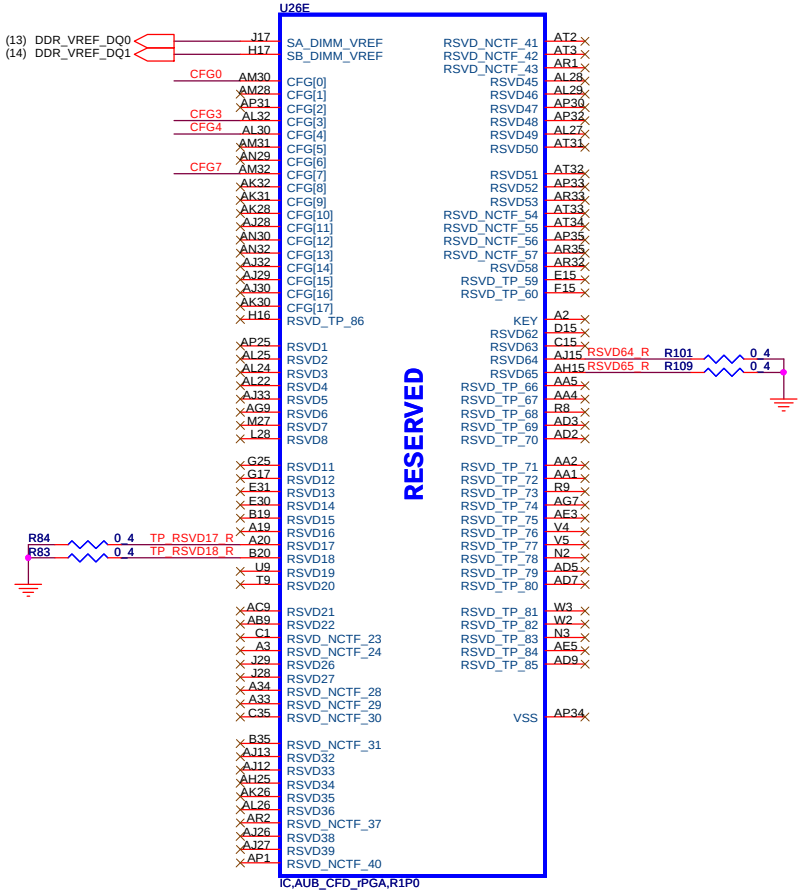
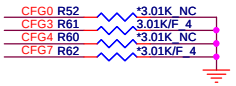
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only



CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

(20,23,29,30,32,33,35,36,38,39,41,42) +3VPCU
(3,4,6,9,10,11,12,35,38,40,42) +1.05V_VTT
(3,4,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(12,30) +RTC_CELL

08

IBEX PEAK-M (HDA,JTAG,SATA)

U34A — Ibex-M 1 OF 10

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
IHDA: HDA_BCLK A30, HDA_SYNC D29, SPKR F1, HDA_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29, HDA_DOCK_EN# / GPIO33 H32, HDA_DOCK_RST# / GPIO13 J30
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, TRST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1
LPC: FWH0 / LAD0 D33, FWH1 / LAD1 B33, FWH2 / LAD2 C32, FWH3 / LAD3 A32, FWH4 / LFRAME# C34, LDRQ0# A34, LDRQ1# / GPIO23 F34, SERIRQ AB9
SATA: SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9; SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8; SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6; SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5; SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1; SATAICOMPO AF16, SATAICOMPI AF15, SATALED# T3, SATA0GP / GPIO21 V1

Y8 32.768KHZ; C710 18P/50V/C0G_4; C707 18P/50V/C0G_4; R612 10M/J_4; RTC_X1, RTC_X2
RTC_RST#, SRTC_RST#, SM_INTRUDER#, +RTC_CELL, R619 330K/J_6 PCH_INVRMEN
ACZ_BCLK, ACZ_SYNC, (11,25) ACZ_SPKR, ACZ_RST#, (25) ACZ_SDIN0, ACZ_SDOUT, (11) PCH_GPIO33, +3VS5, R683 10K/J_4
TP38 PCH_JTAG_TCK_BUF; TP39 PCH_JTAG_TMS; TP42 PCH_JTAG_TDI; TP41 PCH_JTAG_TDO; TP40 PCH_JTAG_RST#
must add test point.
(30) SPI_CLK_R, (30) SPI_CS0#_R, TP35 SPI_CS1#, (30) SPI_SI_R, (30) SPI_SO
R682 10K/J_4 SERIRQ

SATA_RXN0_C (28), SATA_RXP0_C (28), SATA_TXN0 (28), SATA_TXP0 (28) — SSD
SATA_RXN1_C (29), SATA_RXP1_C (29), SATA_TXN1 (29), SATA_TXP1 (29) — HDD
SATA_RXN4_C (29), SATA_RXP4_C (29), SATA_TXN4 (29), SATA_TXP4 (29) — ODD
SATA_RXN5_C (26), SATA_RXP5_C (26), SATA_TXN5 (26), SATA_TXP5 (26) — E-SATA
SATA_TXN0_C 0.01U/16V/X7R_4 C336; SATA_TXP0_C C339; SATA_TXN1_C C723; SATA_TXP1_C C724; SATA_TXN4_C C373; SATA_TXP4_C C352; SATA_TXN5_C C520; SATA_TXP5_C C524
SATA_COMP R198 37.4/F_4 +1.05V_VTT; SATA_LED# (33); SATA_DET1# R29 0_4 MODEL_ID1 (11), SDD_DA_DSS (28)
LPC_DRQ#0 TP47; LCD_BK_OFF# (20); SERIRQ (30); R293 10K/J_4 +3V
(+3V) (+3V_S5) SATA0GP / GPIO21, SATA1GP / GPIO19

+1.05V_VTT: R581 *51_4 PCH_JTAG_TMS; R593 *51_4 PCH_JTAG_RST#; R587 *51_4 PCH_JTAG_TDI; R590 *51_4 PCH_JTAG_TDO; R578 *51_4 PCH_JTAG_TCK_BUF
R573 10K/J_4 SATA_LED#; R569 10K/J_4 SATA_DET1#

Ibex Peak-M_Rev1_0

UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)

U34D — Ibex-M 4 OF 10

LVDS--A: L_BKLTEN T48, L_VDD_EN T47, L_BKLTCTL Y48, L_DDC_CLK AB48, L_DDC_DATA Y45, L_CTRL_CLK AB46, L_CTRL_DATA V48, LVD_IBG AP39, LVD_VBG AP41, LVD_VREFH AT43, LVD_VREFL AT42, LVDSA_CLK# AV53, LVDSA_CLK AV51, LVDSA_DATA#0 BB47, LVDSA_DATA#1 BA52, LVDSA_DATA#2 AY48, LVDSA_DATA#3 AV47, LVDSA_DATA0 BB48, LVDSA_DATA1 BA50, LVDSA_DATA2 AY49, LVDSA_DATA3 AV48
LVDS--B: LVDSB_CLK# AP48, LVDSB_CLK AP47, LVDSB_DATA#0 AY53, LVDSB_DATA#1 AT49, LVDSB_DATA#2 AU52, LVDSB_DATA#3 AT53, LVDSB_DATA0 AY51, LVDSB_DATA1 AT48, LVDSB_DATA2 AU50, LVDSB_DATA3 AT51
CRT: CRT_BLUE AA52, CRT_GREEN AB53, CRT_RED AD53, CRT_DDC_CLK V51, CRT_DDC_DATA V53, CRT_HSYNC Y53, CRT_VSYNC Y51, DAC_IREF AD48, CRT_IRTN AB51
SDVO: SDVO_TVCLKINN BJ46, SDVO_TVCLKINP BG46, SDVO_STALLN BJ48, SDVO_STALLP BG48, SDVO_INTN BF45, SDVO_INTP BH45, SDVO_CTRLCLK T51, SDVO_CTRLDATA T53
DISPLAY PORT B: DDPB_AUXN BG44, DDPB_AUXP BJ44, DDPB_HPD AU38, DDPB_0N BD42, DDPB_0P BC42, DDPB_1N BJ42, DDPB_1P BG42, DDPB_2N BB40, DDPB_2P BA40, DDPB_3N AW38, DDPB_3P BA38
DISPLAY PORT C: DDPC_CTRLCLK Y49, DDPC_CTRLDATA AB49, DDPC_AUXN BE44, DDPC_AUXP BD44, DDPC_HPD AV40, DDPC_0N BE40, DDPC_0P BD40, DDPC_1N BF41, DDPC_1P BH41, DDPC_2N BD38, DDPC_2P BC38, DDPC_3N BB36, DDPC_3P BA36
DISPLAY PORT D: DDPD_CTRLCLK U50, DDPD_CTRLDATA U52, DDPD_AUXN BC46, DDPD_AUXP BD46, DDPD_HPD AT38, DDPD_0N BJ40, DDPD_0P BG40, DDPD_1N BJ38, DDPD_1P BG38, DDPD_2N BF37, DDPD_2P BH37, DDPD_3N BE36, DDPD_3P BD36
Digital Display Interface

(20) LVDS_BLON_IGPU, (20) DISP_ON_IGPU, (20) DPST_PWM_IGPU, (20) EDIDCLK_IGPU, (20) EDIDDATA_IGPU
10K/F_4 R184 L_CTRL_CLK; 10K/F_4 R229 L_CTRL_DATA; 2.37K/F_4 R175 LVDS_IBG; LVDS_VBG TP6
(20) LA_CLK#, (20) LA_CLK; (20) LA_DATAN0, (20) LA_DATAN1, (20) LA_DATAN2; (20) LA_DATAP0, (20) LA_DATAP1, (20) LA_DATAP2
(21) CRT_B_IGPU, (21) CRT_G_IGPU, (21) CRT_R_IGPU — 150/F_4 R571, R567, R562
(21) DDCCLK_IGPU, (21) DDCDATA_IGPU, (21) HSYNC_COM_IGPU, (21) VSYNC_COM_IGPU
R205 1K/F_4 DAC_IREF
LA_CLK C334 5.6P/50V/C0G_4; LA_CLK# C335 5.6P/50V/C0G_4

Ibex Peak-M_Rev1_0

UMA HDMI signals

DPB_CTRL_CLK R588 0_4 SDVO_CLK (22)
DPB_CTRL_DATA R583 0_4 SDVO_DATA (22)
DPB_LANE0_N C328 0.1U/10V/X5R_4 IN_D2# (22)
DPB_LANE0_P C329 0.1U/10V/X5R_4 IN_D2 (22)
DPB_LANE1_N C289 0.1U/10V/X5R_4 IN_D1# (22)
DPB_LANE1_P C284 0.1U/10V/X5R_4 IN_D1 (22)
DPB_LANE2_N C330 0.1U/10V/X5R_4 IN_D0# (22)
DPB_LANE2_P C331 0.1U/10V/X5R_4 IN_D0 (22)
DPB_LANE3_N C299 0.1U/10V/X5R_4 IN_CLK# (22)
DPB_LANE3_P C294 0.1U/10V/X5R_4 IN_CLK (22)

+3V; Q14 *IV@2N7002K; DPB_HPD_Q; HDMI_HPD_CON (22); R148 100K_4; R147 0_4

For AUDIO

(25) ACZ_RST#_AUDIO R626 33_4 ACZ_RST#
(25) ACZ_SDOUT_AUDIO R614 33_4 ACZ_SDOUT
C718 *10P/50V/C0G_4
(25) ACZ_SYNC_AUDIO R617 33_4 ACZ_SYNC
C714 *10P/50V/C0G_4
(25) BIT_CLK_AUDIO R305 33_4 ACZ_BCLK
C493 *10P/50V/C0G_4

RTC

1mA

+RTC_CELL; +3VPCU; +3VRTC_2
RB500V-40 CR4; RB500V-40 CR3
C516 1U/6.3V/X5R_4; R629 20K/F_4 RTC_RST#; C716 1U/6.3V/X5R_4 SHORT_PAD1 J1
R627 20K/F_4 SRTC_RST#; C715 1U/6.3V/X5R_4 SHORT_PAD1 J2
R628 1M_4 SM_INTRUDER#
R335 1K/F_4 +3VRTC_1; BT3 BAT_CONN

4M byte SPI ROM

+3V; R144 10K/F_4; SPI_HOLD#; C261 0.1U/10V/X5R_4
U8: VDD, CE#, SCK, SI, HOLD#, SO, VSS, WP#
W25X16A VSSIG
SPI_CS0# R162 *0/short_4 SPI_CS0#_R
SPI_CLK R143 *0/short_4 SPI_CLK_R
SPI_SI R142 *0/short_4 SPI_SI_R
SPI_SO_R R160 *0/short_4 SPI_SO
SPI_WP# R159 10K/F_4 +3V

Vendor	PN
Socket	DG008000031
WINBOND	AKE39ZP0N00
MAX	AKE39FP0N00

PROJECT : LL7A
Quanta Computer Inc.
Size: Custom | Document Number: PCH 1/5(SATA,HDA,LPC) | Rev: 1A
Date: Thursday, April 08, 2010 | Sheet 8 of 42

IBEX PEAK-M (GND)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

09

U34I

IbexPeak-M_Rev1_0

U34B

Ibex-M 2 OF 10

IbexPeak-M_Rev1_0

20100208
Change Cardreader to USB port
R303 Removed

WLAN

CARD READER

20100208
Change Cardreader to USB port

LAN

Battery SMBUS

Q46 2N7002E

Q47 2N7002E

WLAN

CARD READER

20100208
Change Cardreader to USB port
R312 removed

Q53 *EV@2N7002E

LAN

LAN SMBUS

LOGIC SMBUS

Q22 2N7002E

Q21 2N7002E

U35 *MC74VHC1G08DFT2G

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

20100208
Change Cardreader to USB port
Add 48MHz

UMA only

XTAL25_IN
XTAL25_OUT
C682 18P/50V/C0G_4
R554 1M/F_4
Y7 25MHZ
C681 18P/50V/C0G_4

DIS only

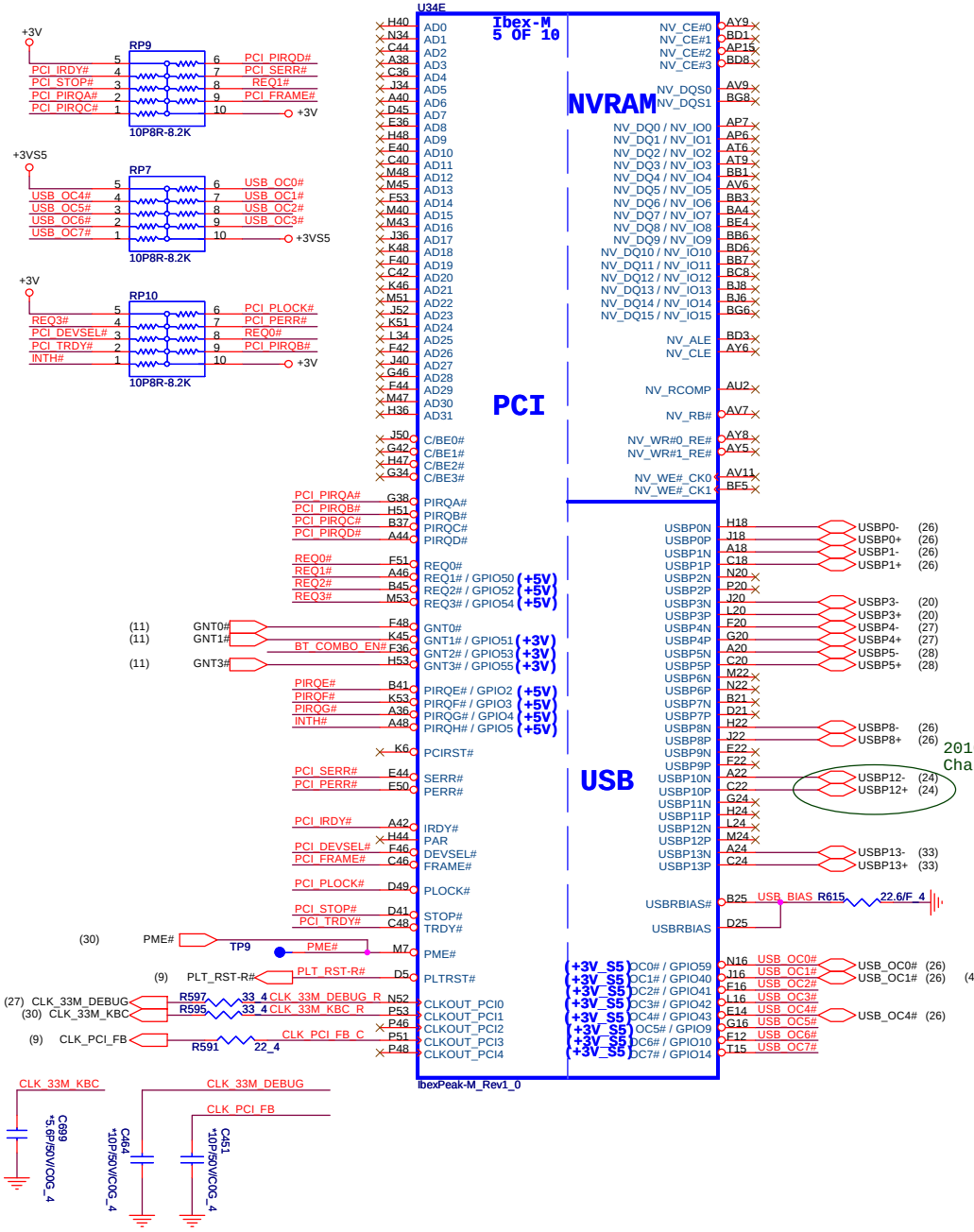
PROJECT : LL7A

Quanta Computer Inc.

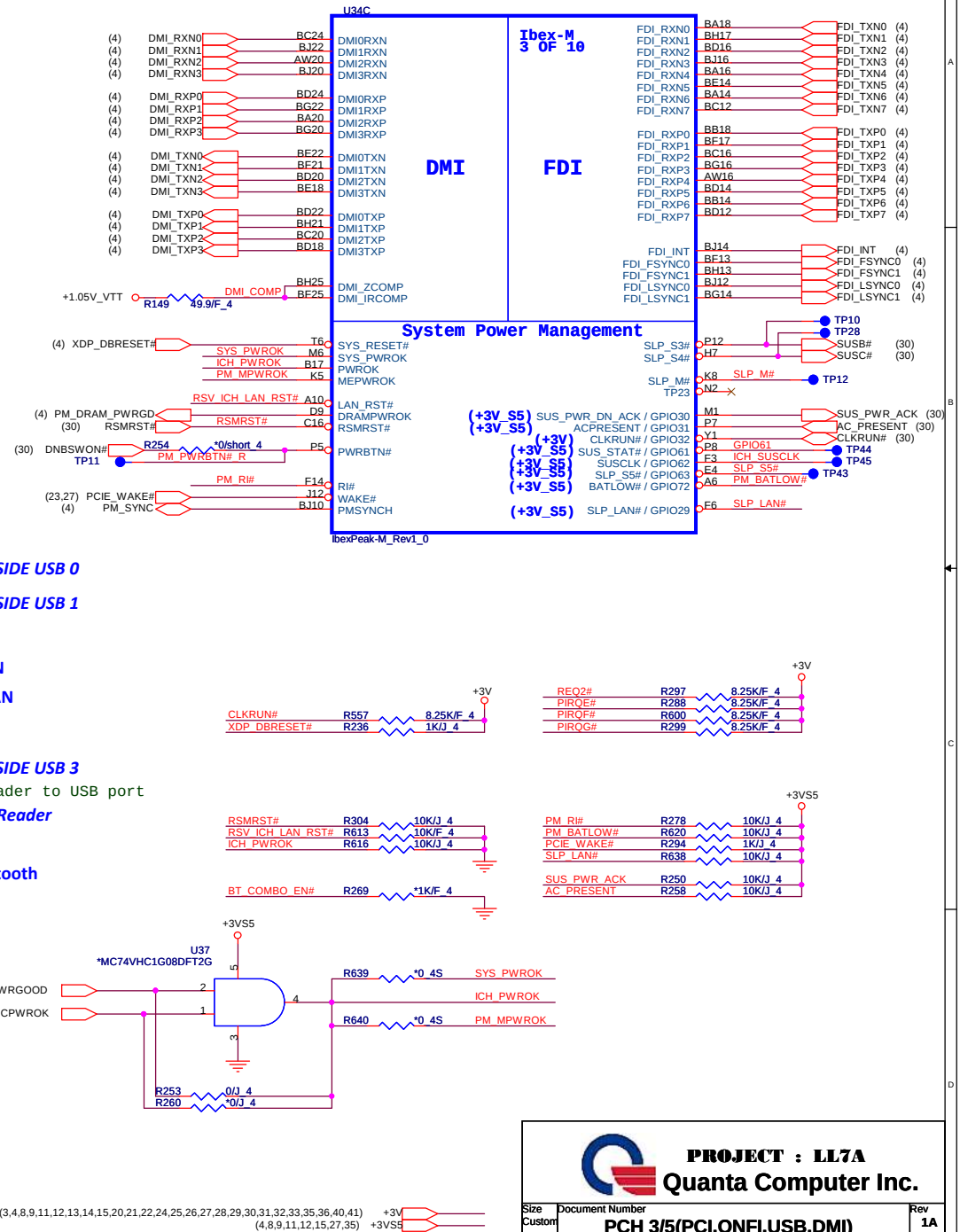
Size	Document Number	Rev
Custom	PCH 2/5(PCIE, SMBUS,CK)	1A

Date: Thursday, April 08, 2010 Sheet 9 of 42

IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)

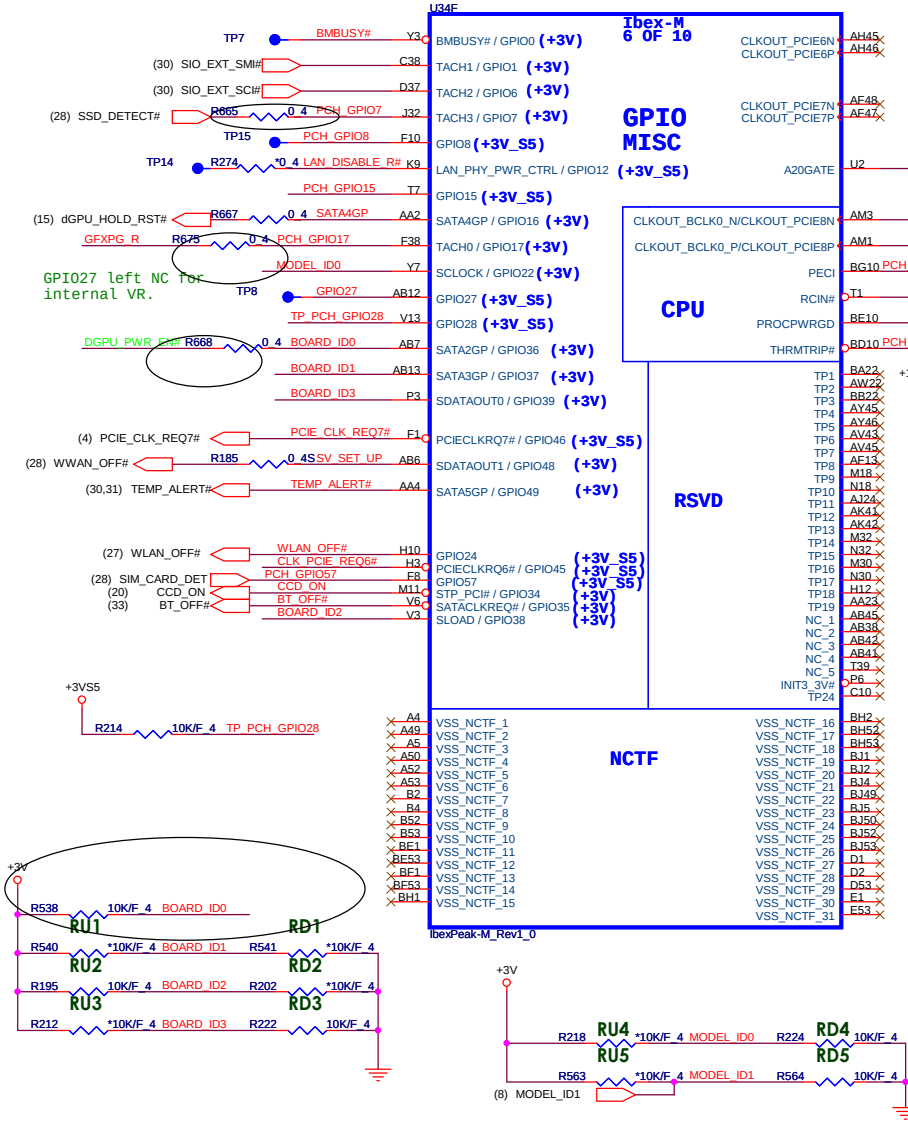


PROJECT : LL7A
Quanta Computer Inc.

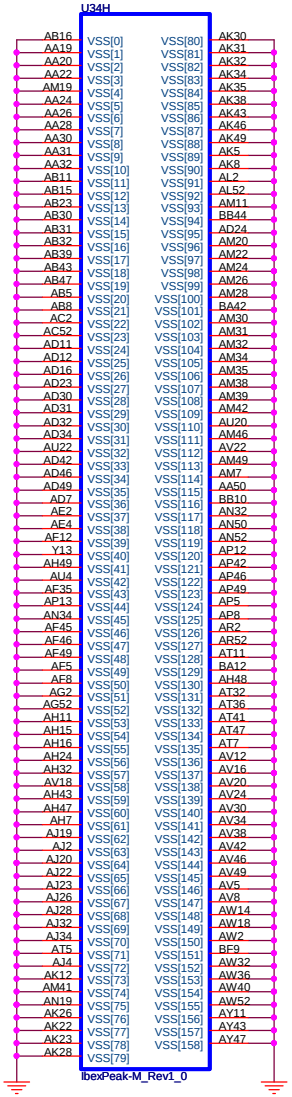
Size	Document Number	Rev
Custom	PCH 3/5(PCI,ONFI,USB,DMI)	1A

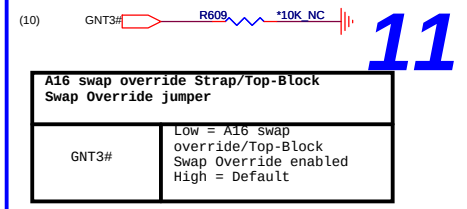
Date: Thursday, April 08, 2010 Sheet 10 of 42

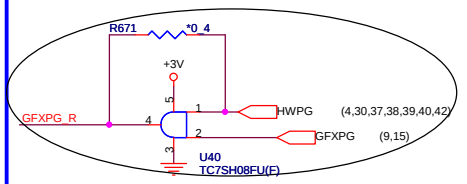
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

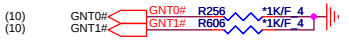


IBEX PEAK-M (GND)









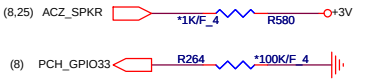
Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

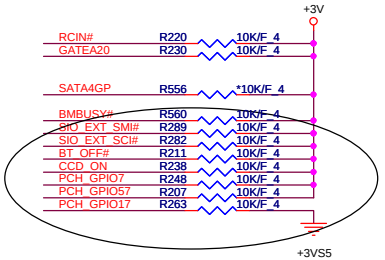
SV_SET_UP	1-X High = Strong (Default)

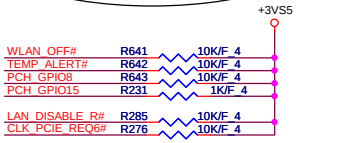
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

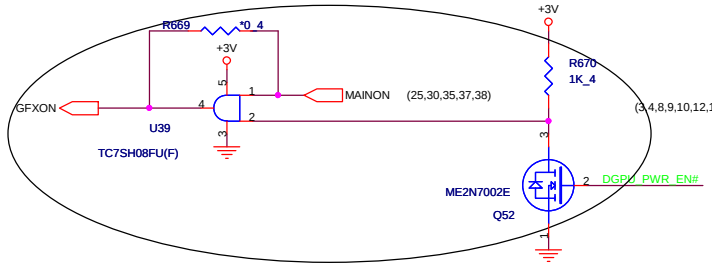
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap









Board ID For Function		ID1 GPIO37	ID2 GPIO38	ID3 GPIO39
SDV		0	0	0
SIV		0	0	0
SIT		0	1	0
SVT		1	0	0
SOVP		0	1	0

Model ID	MODEL_ID0	MODEL_ID1
Default	0	0
LL7	0	1
LL7A	1	0

(3,4,6,8,9,10,12,35,38,40,42) +1.05V_VTT
(3,4,8,9,10,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(4,8,9,10,12,15,27,35) +3VS5

PROJECT : LL7A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5(GPIO & STRAP)	1A
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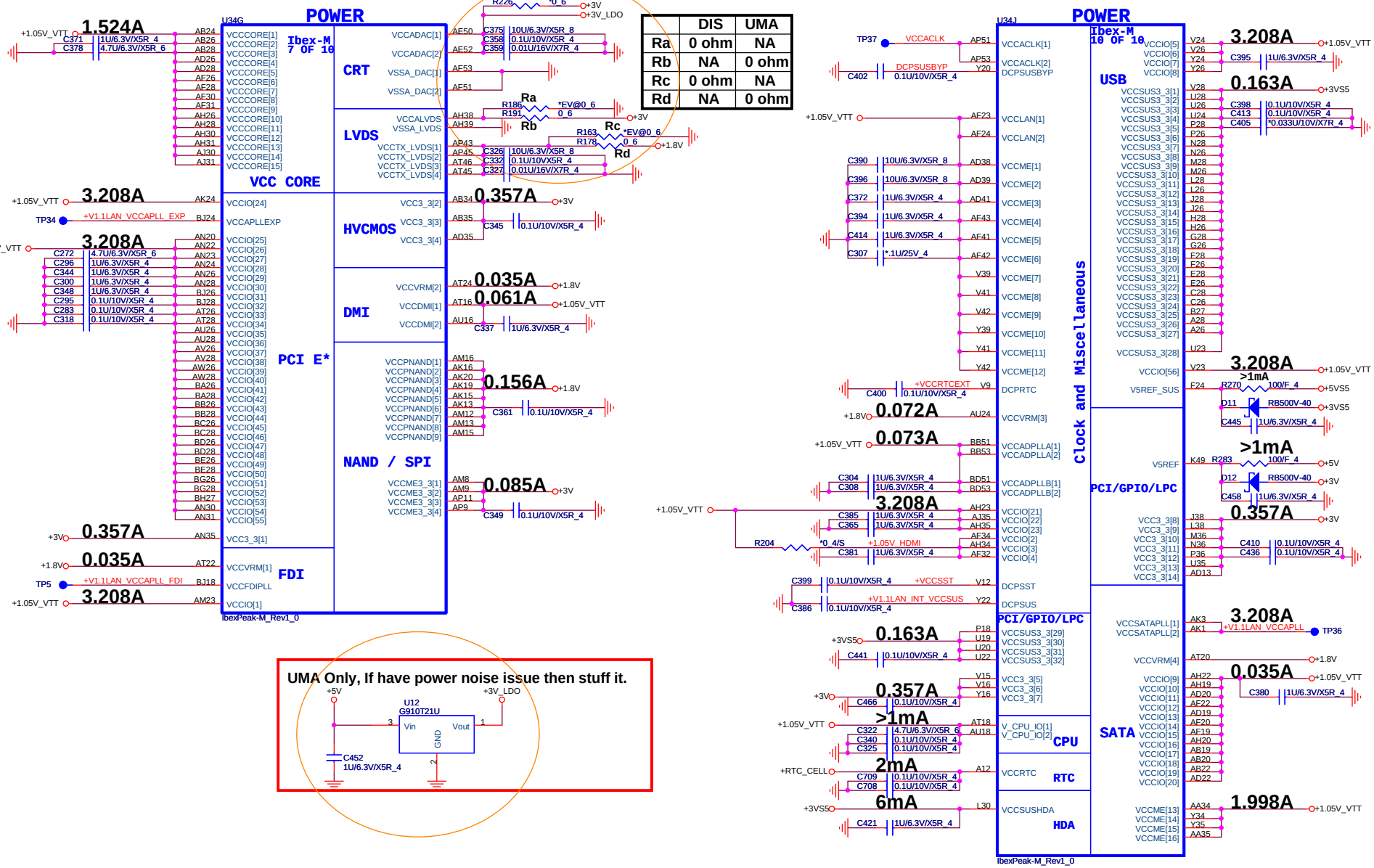

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

UMA Only, If have power noise issue then stuff it.

(3,4,6,8,9,10,11,35,38,40,42) +1.05V_VTT
(6,35,38,41) +1.8V
(3,4,8,9,10,11,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(4,8,9,10,11,15,27,35) +3VS5
(20,21,22,25,29,30,31,32,33,35,36) +5V
(26,35) +5VS5

PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5(POWER)	1A

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(4,6,14,35,37,41) +1.5VSUS
(3,4,8,9,10,11,12,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(14,35,37) +0.75V_DDR_VTT

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

JDIM4A

(5) M_A_A[15:0]

M_A_A0 98 A0
M_A_A1 97 A1
M_A_A2 96 A2
M_A_A3 95 A3
M_A_A4 92 A4
M_A_A5 91 A5
M_A_A6 90 A6
M_A_A7 86 A7
M_A_A8 89 A8
M_A_A9 85 A9
M_A_A10 107 A10/AP
M_A_A11 84 A11
M_A_A12 83 A12/BC#
M_A_A13 119 A13
M_A_A14 80 A14
M_A_A15 78 A15

(5) M_A_BS#0 109 BA0
(5) M_A_BS#1 108 BA1
(5) M_A_BS#2 79 BA2
(5) M_A_CS#0 114 S0#
(5) M_A_CS#1 121 S1#
(5) M_A_CLK0 101 CK0
(5) M_A_CLK0# 103 CK0#
(5) M_A_CLK1 102 CK1
(5) M_A_CLK1# 104 CK1#
(5) M_A_CKE0 73 CKE0
(5) M_A_CKE1 74 CKE1
(5) M_A_CAS# 115 CAS#
(5) M_A_RAS# 110 RAS#
(5) M_A_WE# 113 WE#

R565 10K/F_4 DIMM0_SA0
R566 10K/F_4 DIMM0_SA1
(3,9,14) CGCLK_SMB 202 SCL
(3,9,14) CGDAT_SMB 200 SDA

(5) M_A_ODT0 116 ODT0
(5) M_A_ODT1 120 ODT1
(5) M_A_DM[7:0]

M_A_DM0 11 DM0
M_A_DM1 28 DM1
M_A_DM2 46 DM2
M_A_DM3 63 DM3
M_A_DM4 136 DM4
M_A_DM5 153 DM5
M_A_DM6 170 DM6
M_A_DM7 187 DM7

(5) M_A_DQS[7:0]

M_A_DQS0 12 DQS0
M_A_DQS1 29 DQS1
M_A_DQS2 47 DQS2
M_A_DQS3 64 DQS3
M_A_DQS4 137 DQS4
M_A_DQS5 154 DQS5
M_A_DQS6 171 DQS6
M_A_DQS7 188 DQS7

(5) M_A_DQS#[7:0]

M_A_DQS#0 10 DQS#0
M_A_DQS#1 27 DQS#1
M_A_DQS#2 45 DQS#2
M_A_DQS#3 62 DQS#3
M_A_DQS#4 135 DQS#4
M_A_DQS#5 152 DQS#5
M_A_DQS#6 169 DQS#6
M_A_DQS#7 186 DQS#7

PC2100 DDR3 SDRAM SO-DIMM (204P)

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 15 DQ2
M_A_DQ3 17 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 16 DQ6
M_A_DQ7 18 DQ7
M_A_DQ8 21 DQ8
M_A_DQ9 23 DQ9
M_A_DQ10 33 DQ10
M_A_DQ11 35 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 24 DQ13
M_A_DQ14 34 DQ14
M_A_DQ15 36 DQ15
M_A_DQ16 39 DQ16
M_A_DQ17 41 DQ17
M_A_DQ18 51 DQ18
M_A_DQ19 53 DQ19
M_A_DQ20 40 DQ20
M_A_DQ21 42 DQ21
M_A_DQ22 50 DQ22
M_A_DQ23 52 DQ23
M_A_DQ24 57 DQ24
M_A_DQ25 59 DQ25
M_A_DQ26 67 DQ26
M_A_DQ27 69 DQ27
M_A_DQ28 56 DQ28
M_A_DQ29 58 DQ29
M_A_DQ30 68 DQ30
M_A_DQ31 70 DQ31
M_A_DQ32 129 DQ32
M_A_DQ33 131 DQ33
M_A_DQ34 141 DQ34
M_A_DQ35 143 DQ35
M_A_DQ36 130 DQ36
M_A_DQ37 132 DQ37
M_A_DQ38 140 DQ38
M_A_DQ39 142 DQ39
M_A_DQ40 147 DQ40
M_A_DQ41 149 DQ41
M_A_DQ42 157 DQ42
M_A_DQ43 159 DQ43
M_A_DQ44 146 DQ44
M_A_DQ45 148 DQ45
M_A_DQ46 158 DQ46
M_A_DQ47 160 DQ47
M_A_DQ48 163 DQ48
M_A_DQ49 165 DQ49
M_A_DQ50 175 DQ50
M_A_DQ51 177 DQ51
M_A_DQ52 164 DQ52
M_A_DQ53 166 DQ53
M_A_DQ54 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 181 DQ56
M_A_DQ57 183 DQ57
M_A_DQ58 191 DQ58
M_A_DQ59 193 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ62 192 DQ62
M_A_DQ63 194 DQ63

DDR3-DIMM0

M_A_DQ[63:0] (5)

Place these Caps near So-Dimm0.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

+1.5VSUS
C305 4.7U/6.3V/X5R_6
C312 4.7U/6.3V/X5R_6
C311 4.7U/6.3V/X5R_6
C369 4.7U/6.3V/X5R_6
C306 4.7U/6.3V/X5R_6
C370 4.7U/6.3V/X5R_6
C366 0.1U/10V/X5R_4
C303 0.1U/10V/X5R_4
C367 0.1U/10V/X5R_4
C368 0.1U/10V/X5R_4
C301 0.1U/10V/X5R_4
C313 *0.047U/10V/X7R_4
C364 *0.047U/10V/X7R_4

+0.75V_DDR_VTT
C290 1U/6.3V/X5R_4
C362 1U/6.3V/X5R_4
C350 1U/6.3V/X5R_4
C297 1U/6.3V/X5R_4
C317 *10U/6.3V/X5R_8
C388 *10U/6.3V/X5R_8
C376 4.7U/6.3V/X5R_6
C342 *0.047U/10V/X7R_4
C384 *0.047U/10V/X7R_4

SMDDR_VREF_DQ0
C351 0.1U/10V/X5R_4
C374 2.2U/6.3V/X5R_6

+3V
C360 2.2U/6.3V/X5R_6
C356 *0.1U/10V/X5R_4
C403 *0.047U/10V/X7R_4

SMDDR_VREF_DIMM
C315 0.1U/10V/X5R_4
C316 2.2U/6.3V/X5R_6
C267 *0.047U/10V/X7R_4

+1.5VSUS

JDIM4B

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V
VDDSPD 199

for S3 power reduction

NC1 77
NC2 122
NCTEST 125

(4) PM_EXTTS#0
PM_EXTTS#0
EVENT# 198
RESET# 30

(4,14) DDR3_DRAMRST#
+1.5VSUS
R153 1K/F_4

(7) DDR_VREF_DQ0
R189 *0_4
SMDDR_VREF_DQ0
SMDDR_VREF_DIMM
VREF_DQ 1
VREF_CA 126

R197 100K/F_4

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 173
VSS44 178
VSS45 179
VSS46 184
VSS47 185
VSS48 189
VSS49 190
VSS50 195
VSS51 196
VSS52

VTT1 203
VTT2 204
+0.75V_DDR_VTT

GND 205
GND 206

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

+0.75V_DDR_VTT
R217 22_4
(6,35) MAINON_G
Q16 2N7002E

for S3 power reduction

+1.5VSUS
R193 1K/F_4
SMDDR_VREF_DQ0
R192 1K/F_4
C354 0.1U/10V/X5R_4
C353 *0.047U/10V/X7R_4

C314 470P/50V/X7R_4
R156 *0_4/S
R155 *10K/F_4
SMDDR_VREF_DIMM (14)
DDR_VTTREF (37)
+1.5VSUS
R157 *10K/F_4

PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A

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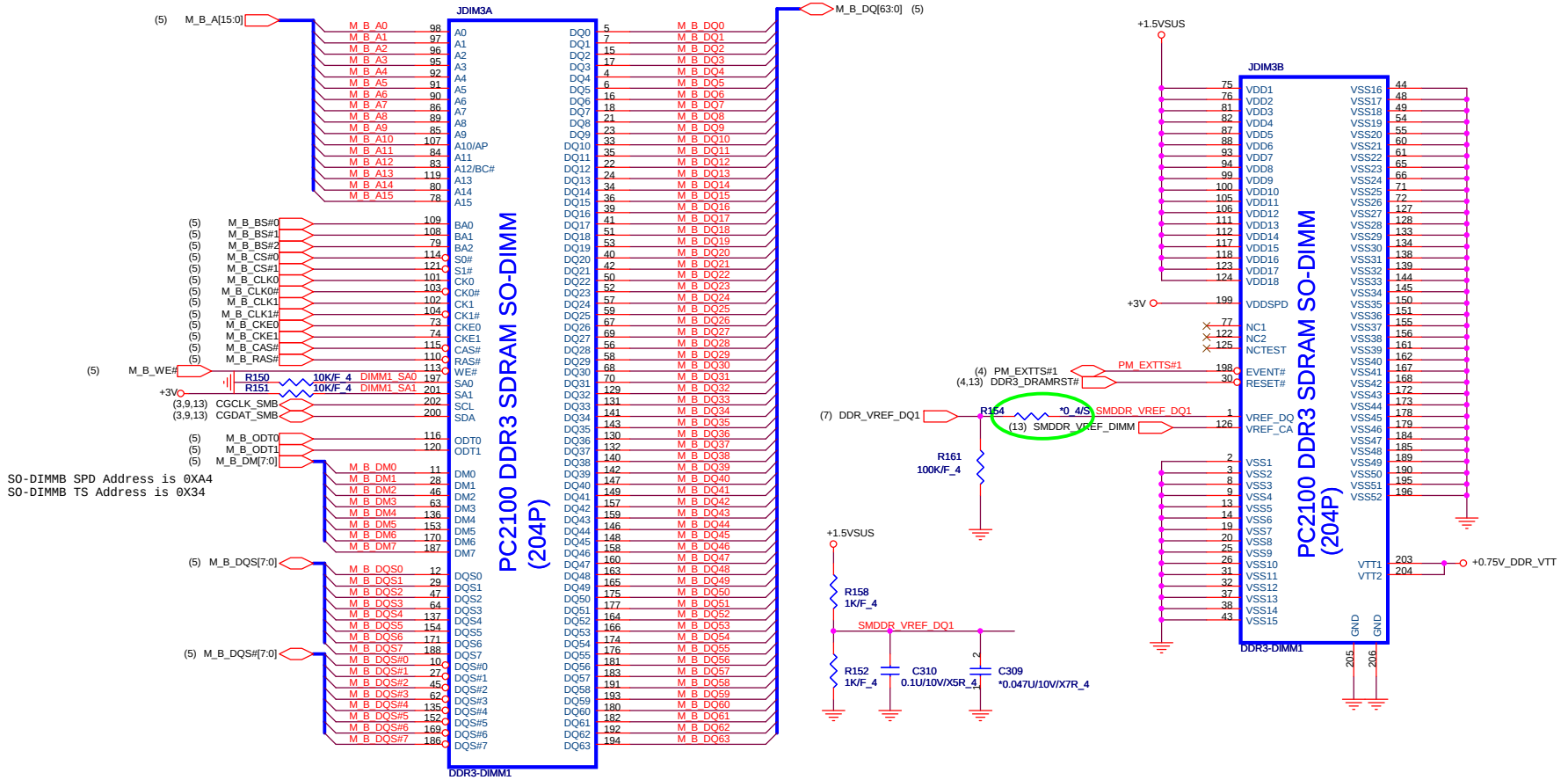
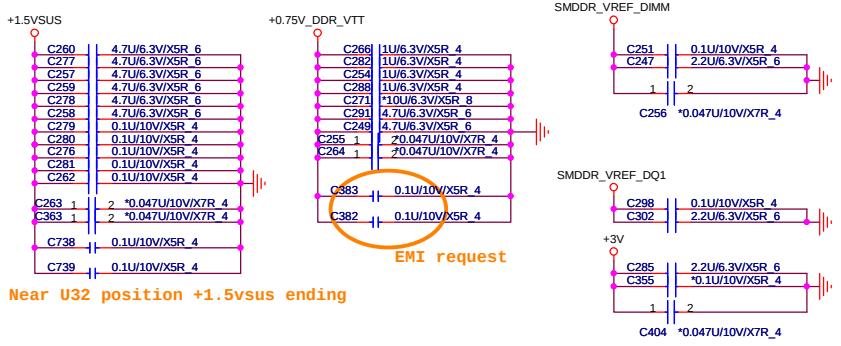
(4,6,13,35,37,41) +1.5VSUS
(3,4,8,9,10,11,12,13,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(13,35,37) +0.75V_DDR_VTT



Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



Near U32 position +1.5vsus ending

PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A
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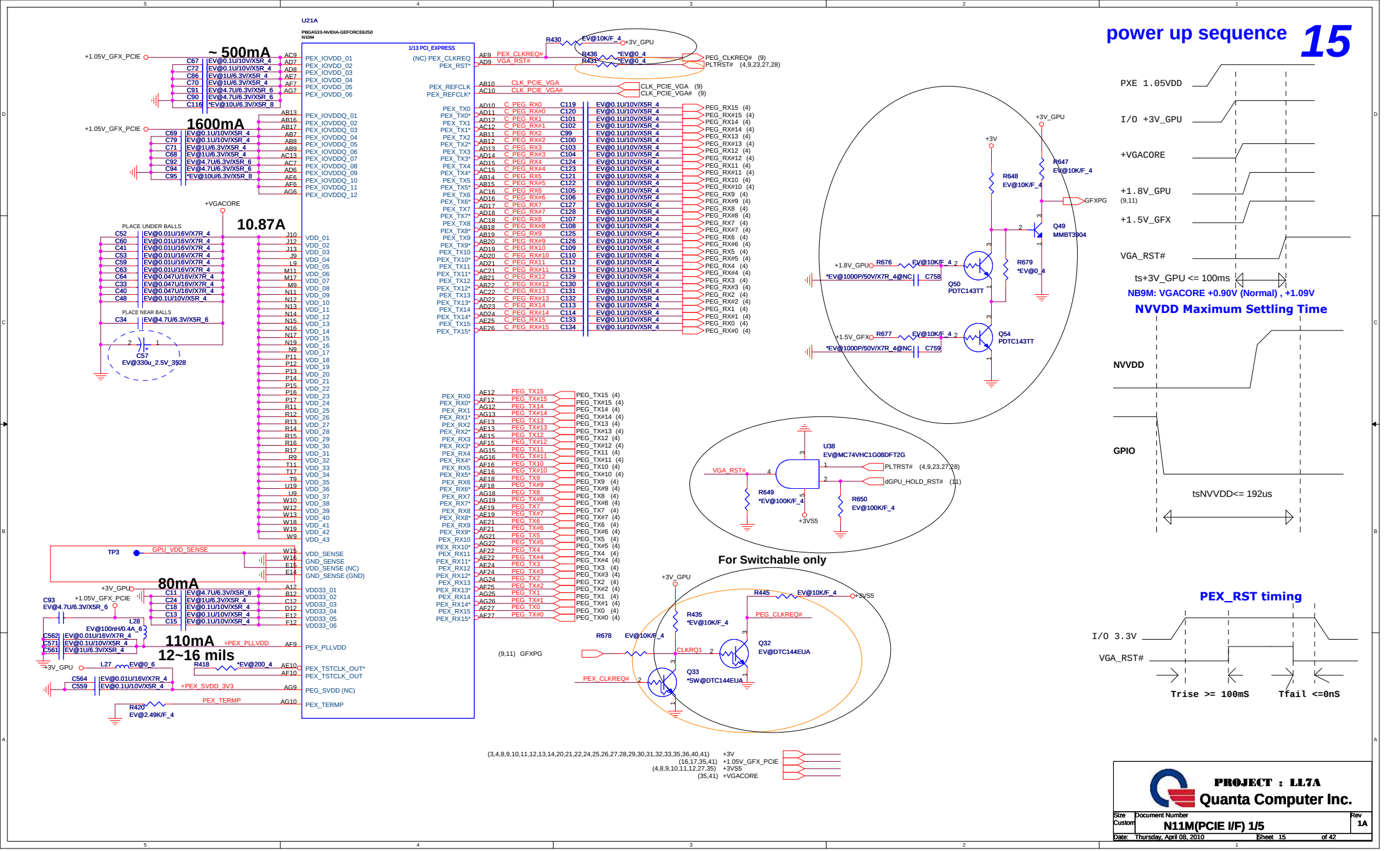

power up sequence 15
U21A
PBGA533-NVIDIA-GEFORCE6250
N10M
1/13 PCI_EXPRESS
~ 500mA
1600mA
10.87A
80mA
110mA
12~16 mils
+1.05V_GFX_PCIE
+VGACORE
PLACE UNDER BALLS
PLACE NEAR BALLS
C57
EV@330u_2.5V_3528
TP3
GPU_VDD_SENSE
+3V_GPU
+1.05V_GFX_PCIE
L28
EV@100nH/0.4A_6
+PEX_PLLVDD
+PEX_SVDD_3V3
PEX_TERMP
R420
EV@2.49K/F_4
R418
*EV@200_4
L27
EV@0_6
C93
EV@4.7U/6.3V/X5R_6
R430
EV@10K/F_4
R436
*EV@0_4
R431
*EV@0_4
PEX_CLKREQ#
VGA_RST#
PEG_CLKREQ# (9)
PLTRST# (4,9,23,27,28)
CLK_PCIE_VGA (9)
CLK_PCIE_VGA# (9)
R647
EV@10K/F_4
R648
EV@10K/F_4
GFXPG
Q49
MMBT3904
R676
EV@10K/F_4
*EV@1000P/50V/X7R_4@NC
C758
Q50
PDTC143TT
R679
*EV@0_4
R677
EV@10K/F_4
*EV@1000P/50V/X7R_4@NC
C759
Q54
PDTC143TT
U38
EV@MC74VHC1G08DFT2G
PLTRST# (4,9,23,27,28)
dGPU_HOLD_RST# (11)
R649
*EV@100K/F_4
R650
EV@100K/F_4
+3VS5
For Switchable only
R445
EV@10K/F_4
R435
*EV@10K/F_4
R678
EV@10K/F_4
CLKRQ1
Q32
EV@DTC144EUA
Q33
*SW@DTC144EUA
(9,11) GFXPG
(3,4,8,9,10,11,12,13,14,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(16,17,35,41) +1.05V_GFX_PCIE
(4,8,9,10,11,12,27,35) +3VS5
(35,41) +VGACORE
PXE 1.05VDD
I/O +3V_GPU
+VGACORE
+1.8V_GPU
(9,11)
+1.5V_GFX
VGA_RST#
ts+3V_GPU <= 100ms
NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time
NVVDD
GPIO
tsNVVDD<= 192us
PEX_RST timing
I/O 3.3V
VGA_RST#
Trise >= 100mS
Tfail <=0nS
PROJECT : LL7A
Quanta Computer Inc.
Size Custom
Document Number
N11M(PCIE I/F) 1/5
Rev 1A
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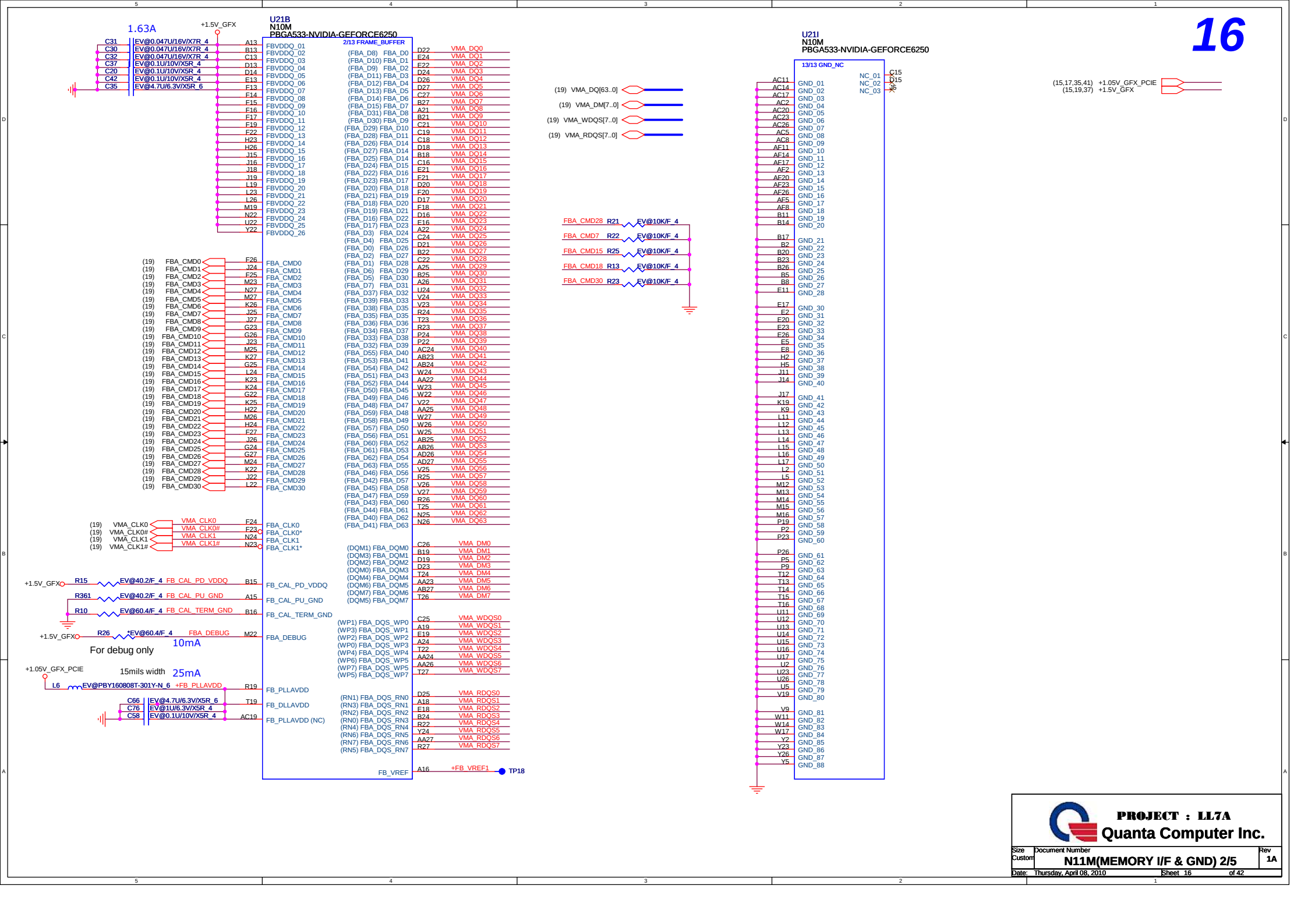
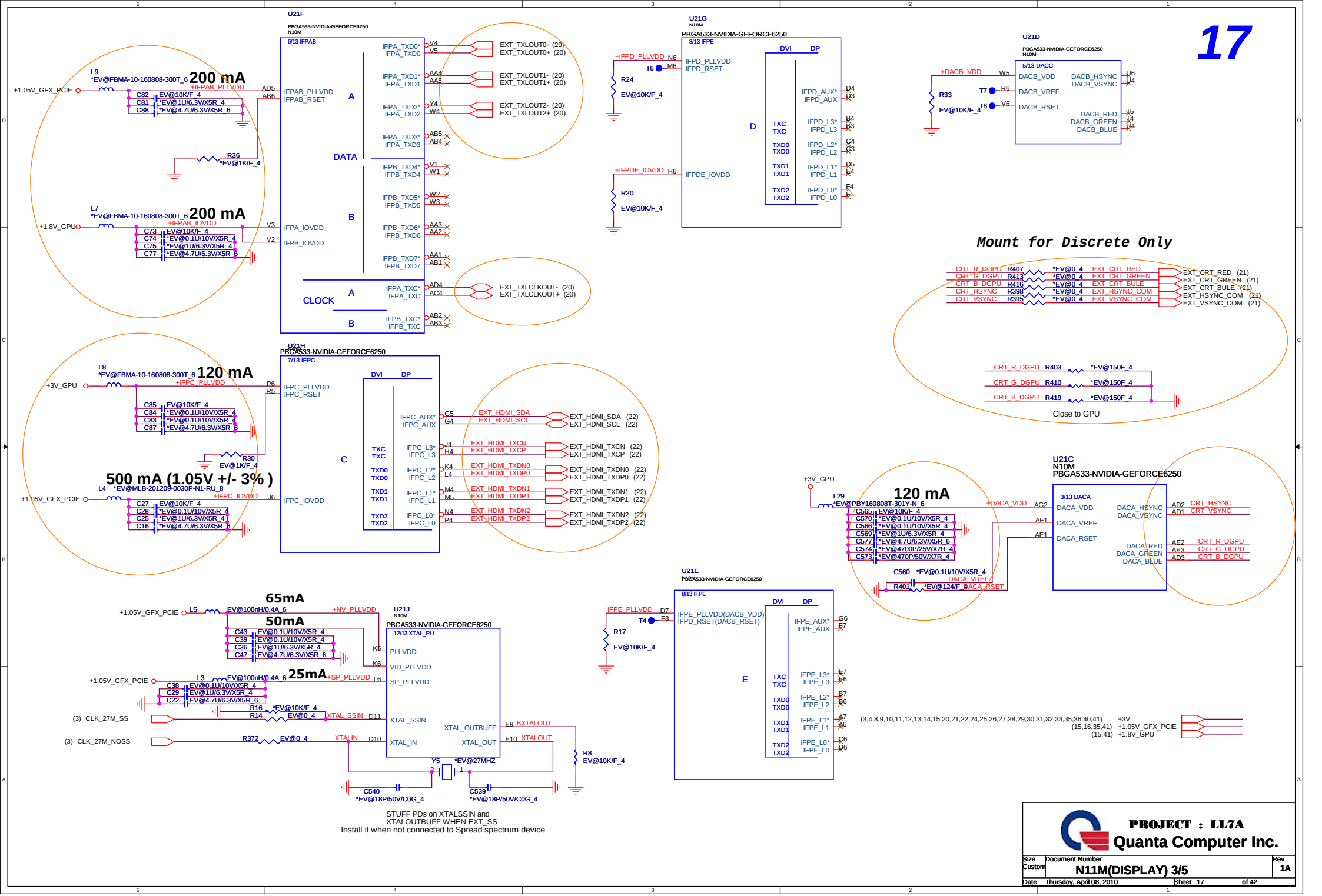


PROJECT : LL7A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11M(MEMORY I/F & GND) 2/5	1A
Date: Thursday, April 08, 2010	Sheet 16 of 42	


U21F
PBGA533-NVIDIA-GEFORCE6250
N10M
6/13 IFPAB
L9
*EV@FBMA-10-160808-300T_6
200 mA
+1.05V_GFX_PCIE
+IFPAB_PLLVDD
C82 EV@10K/F_4
C81 *EV@1U/6.3V/X5R_4
C88 *EV@4.7U/6.3V/X5R_6
R36 *EV@1K/F_4
IFPAB_PLLVDD
IFPAB_RSET
L7
*EV@FBMA-10-160808-300T_6
200 mA
+1.8V_GPU
+IFPAB_IOVDD
C73 EV@10K/F_4
C74 *EV@0.1U/10V/X5R_4
C75 *EV@1U/6.3V/X5R_4
C77 *EV@4.7U/6.3V/X5R_6
IFPA_IOVDD
IFPB_IOVDD
DATA
A
B
CLOCK
IFPA_TXD0* IFPA_TXD0
IFPA_TXD1* IFPA_TXD1
IFPA_TXD2* IFPA_TXD2
IFPA_TXD3* IFPA_TXD3
IFPB_TXD4* IFPB_TXD4
IFPB_TXD5* IFPB_TXD5
IFPB_TXD6* IFPB_TXD6
IFPB_TXD7* IFPB_TXD7
IFPA_TXC* IFPA_TXC
IFPB_TXC* IFPB_TXC
EXT_TXLOUT0- (20) EXT_TXLOUT0+ (20)
EXT_TXLOUT1- (20) EXT_TXLOUT1+ (20)
EXT_TXLOUT2- (20) EXT_TXLOUT2+ (20)
EXT_TXLCLKOUT- (20) EXT_TXLCLKOUT+ (20)
U21G
N10M
PBGA533-NVIDIA-GEFORCE6250
8/13 IFPE
+IFPD_PLLVDD
R24 EV@10K/F_4
+IFPDE_IOVDD
R20 EV@10K/F_4
IFPD_PLLVDD
IFPD_RSET
IFPDE_IOVDD
DVI
DP
D
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2
IFPD_AUX* IFPD_AUX
IFPD_L3* IFPD_L3
IFPD_L2* IFPD_L2
IFPD_L1* IFPD_L1
IFPD_L0* IFPD_L0
U21D
PBGA533-NVIDIA-GEFORCE6250
N10M
5/13 DACC
+DACB_VDD
R33 EV@10K/F_4
DACB_VDD
DACB_VREF
DACB_RSET
DACB_HSYNC
DACB_VSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
Mount for Discrete Only
CRT_R_DGPU R407 *EV@0_4 EXT_CRT_RED
CRT_G_DGPU R413 *EV@0_4 EXT_CRT_GREEN
CRT_B_DGPU R416 *EV@0_4 EXT_CRT_BULE
CRT_HSYNC R398 *EV@0_4 EXT_HSYNC_COM
CRT_VSYNC R395 *EV@0_4 EXT_VSYNC_COM
EXT_CRT_RED (21)
EXT_CRT_GREEN (21)
EXT_CRT_BULE (21)
EXT_HSYNC_COM (21)
EXT_VSYNC_COM (21)
CRT_R_DGPU R403 *EV@150F_4
CRT_G_DGPU R410 *EV@150F_4
CRT_B_DGPU R419 *EV@150F_4
Close to GPU
U21H
PBGA533-NVIDIA-GEFORCE6250
7/13 IFPC
L8
*EV@FBMA-10-160808-300T_6
120 mA
+3V_GPU
+IFPC_PLLVDD
C85 EV@10K/F_4
C84 *EV@0.1U/10V/X5R_4
C83 *EV@0.1U/10V/X5R_4
C87 *EV@4.7U/6.3V/X5R_6
R30 EV@1K/F_4
500 mA (1.05V +/- 3%)
L4 *EV@MLB-201209-0030P-N1-RU_8
+1.05V_GFX_PCIE
+IFPC_IOVDD
C27 EV@10K/F_4
C28 *EV@0.1U/10V/X5R_4
C25 *EV@1U/6.3V/X5R_4
C16 *EV@4.7U/6.3V/X5R_6
IFPC_PLLVDD
IFPC_RSET
IFPC_IOVDD
C
DVI
DP
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2
IFPC_AUX* IFPC_AUX
IFPC_L3* IFPC_L3
IFPC_L2* IFPC_L2
IFPC_L1* IFPC_L1
IFPC_L0* IFPC_L0
EXT_HDMI_SDA EXT_HDMI_SCL
EXT_HDMI_TXCN EXT_HDMI_TXCP
EXT_HDMI_TXDN0 EXT_HDMI_TXDP0
EXT_HDMI_TXDN1 EXT_HDMI_TXDP1
EXT_HDMI_TXDN2 EXT_HDMI_TXDP2
EXT_HDMI_SDA (22)
EXT_HDMI_SCL (22)
EXT_HDMI_TXCN (22)
EXT_HDMI_TXCP (22)
EXT_HDMI_TXDN0 (22)
EXT_HDMI_TXDP0 (22)
EXT_HDMI_TXDN1 (22)
EXT_HDMI_TXDP1 (22)
EXT_HDMI_TXDN2 (22)
EXT_HDMI_TXDP2 (22)
+3V_GPU
L29
*EV@PBY1608087-301Y-N_6
120 mA
+DACA_VDD
C565 EV@10K/F_4
C570 *EV@0.1U/10V/X5R_4
C566 *EV@0.1U/10V/X5R_4
C569 *EV@1U/6.3V/X5R_4
C577 *EV@4.7U/6.3V/X5R_6
C574 *EV@4700P/25V/X7R_4
C573 *EV@470P/50V/X7R_4
C560 *EV@0.1U/10V/X5R_4
DACA_VREF
R401 *EV@124/F_0
DACA_RSET
U21C
N10M
PBGA533-NVIDIA-GEFORCE6250
3/13 DACA
DACA_VDD
DACA_VREF
DACA_RSET
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
CRT_HSYNC
CRT_VSYNC
CRT_R_DGPU
CRT_G_DGPU
CRT_B_DGPU
65mA
+1.05V_GFX_PCIE
L5
EV@100nH/0.4A_6
+NV_PLLVDD
50mA
C43 EV@0.1U/10V/X5R_4
C39 EV@0.1U/10V/X5R_4
C36 EV@1U/6.3V/X5R_4
C47 EV@4.7U/6.3V/X5R_6
+1.05V_GFX_PCIE
L3
EV@100nH/0.4A_6
25mA
+SP_PLLVDD
C38 EV@0.1U/10V/X5R_4
C29 EV@1U/6.3V/X5R_4
C22 EV@4.7U/6.3V/X5R_6
R16 *EV@10K/F_4
R14 EV@0_4
(3) CLK_27M_SS
XTAL_SSIN
(3) CLK_27M_NOSS
R372 EV@0_4
XTALIN
U21J
N10M
PBGA533-NVIDIA-GEFORCE6250
12/13 XTAL_PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
BXTALOUT
XTALOUT
Y5 *EV@27MHZ
C540 *EV@18P/50V/C0G_4
C539 *EV@18P/50V/C0G_4
R8 EV@10K/F_4
STUFF PDs on XTALSSIN and
XTALOUTBUFF WHEN EXT_SS
Install it when not connected to Spread Spectrum device
U21E
PBGA533-NVIDIA-GEFORCE6250
8/13 IFPE
IFPE_PLLVDD
R17 EV@10K/F_4
IFPE_PLLVDD(DACB_VDD)
IFPD_RSET(DACB_RSET)
DVI
DP
E
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2
IFPE_AUX* IFPE_AUX
IFPE_L3* IFPE_L3
IFPE_L2* IFPE_L2
IFPE_L1* IFPE_L1
IFPE_L0* IFPE_L0
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(15,16,35,41) +1.05V_GFX_PCIE
(15,41) +1.8V_GPU
PROJECT : LL7A
Quanta Computer Inc.
Size Custom
Document Number N11M(DISPLAY) 3/5
Rev 1A
Date: Thursday, April 08, 2010
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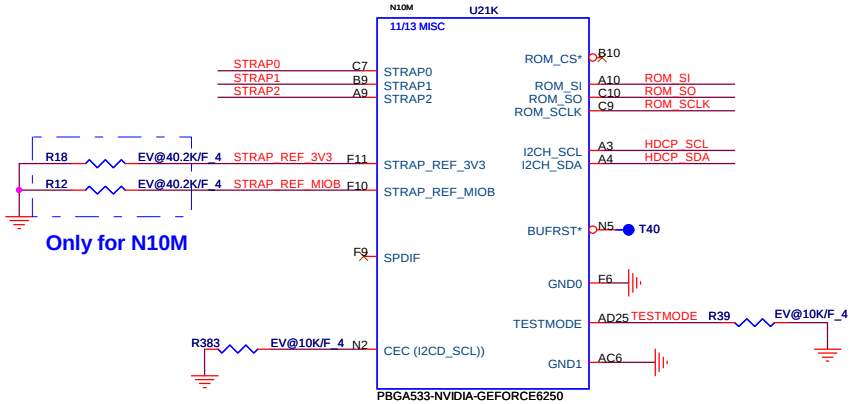
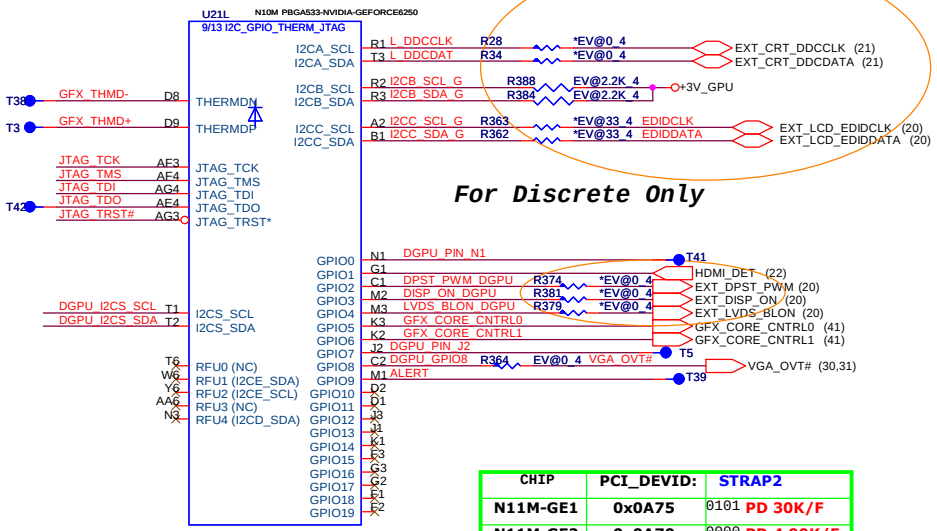
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V



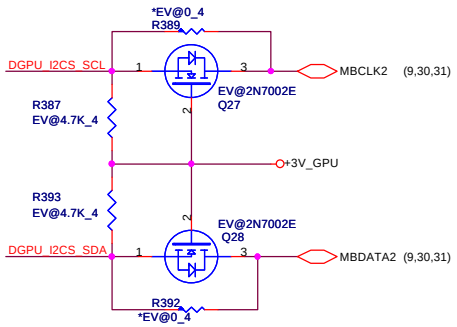


For Discrete Only

CHIP	PCI_DEVID:	STRAP2
N11M-GE1	0x0A75	0101 PD 30K/F
N11M-GE2	0x0A70	0000 PD 4.99K/F

VRAM Type	RAMCFG[0..3]	ROM_SI
Hynix AKD5LZGTW05	0x0A75	0010 PD15K/F
Samsung AKD5LGGT507	0x0A70	0011 PD 20K/F
Hynix AKD5MGGTW00	0x0A75	0110 PD 34.8K/F
Samsung AKD5MGGT501	0x0A70	0111 PD 45.3K/F

GPU Type	STRAP0	STRAP1	ROM_SO	ROM_SCLK
N11M-GE1	PU 45.3K/F	PU 34.8K/F	PD10K/F	PU15K/F
N11M-GE2	PU 45.3K/F	PU 34.8K/F	PD10K/F	PU15K/F

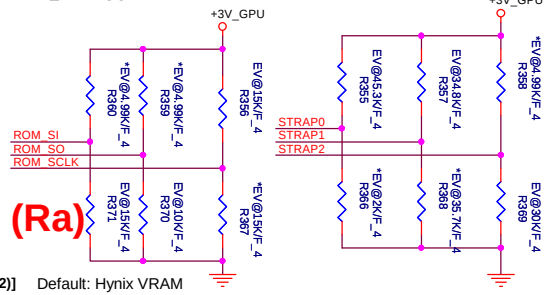


SEE Datasheet for details on N10P Straps!

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

PCI_DEVID[4]/SUBVENDOR



4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30K/F_4: CS33002FB13 [RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4: CS33482FB22 [RES CHIP 34.8K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

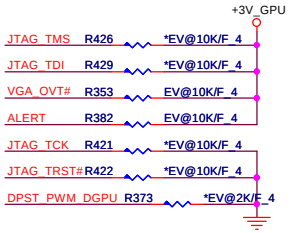
Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

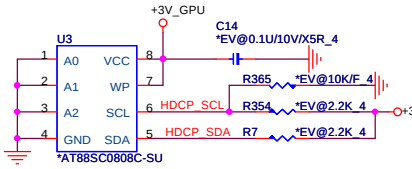
VRAM Configuration Table

(Ra)

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
	0001				
AKD5LZGTW05	0010	DDR3 64Mx16x4, 128bit, 512MB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K/F
AKD5LGGT507	0011	DDR3 64Mx16x4, 128bit, 512MB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K/F
	0101		Reserved		
	0110				
AKD5MGGTW00	0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix	H5TQ2G63BFR-12C	PD 34.8K/F
AKD5MGGT501	0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung	K4W2G1646B-HC12	PD 45.3K/F



HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

PROJECT : Z360
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11M(GPIO & STRAPS) 4/5	1A
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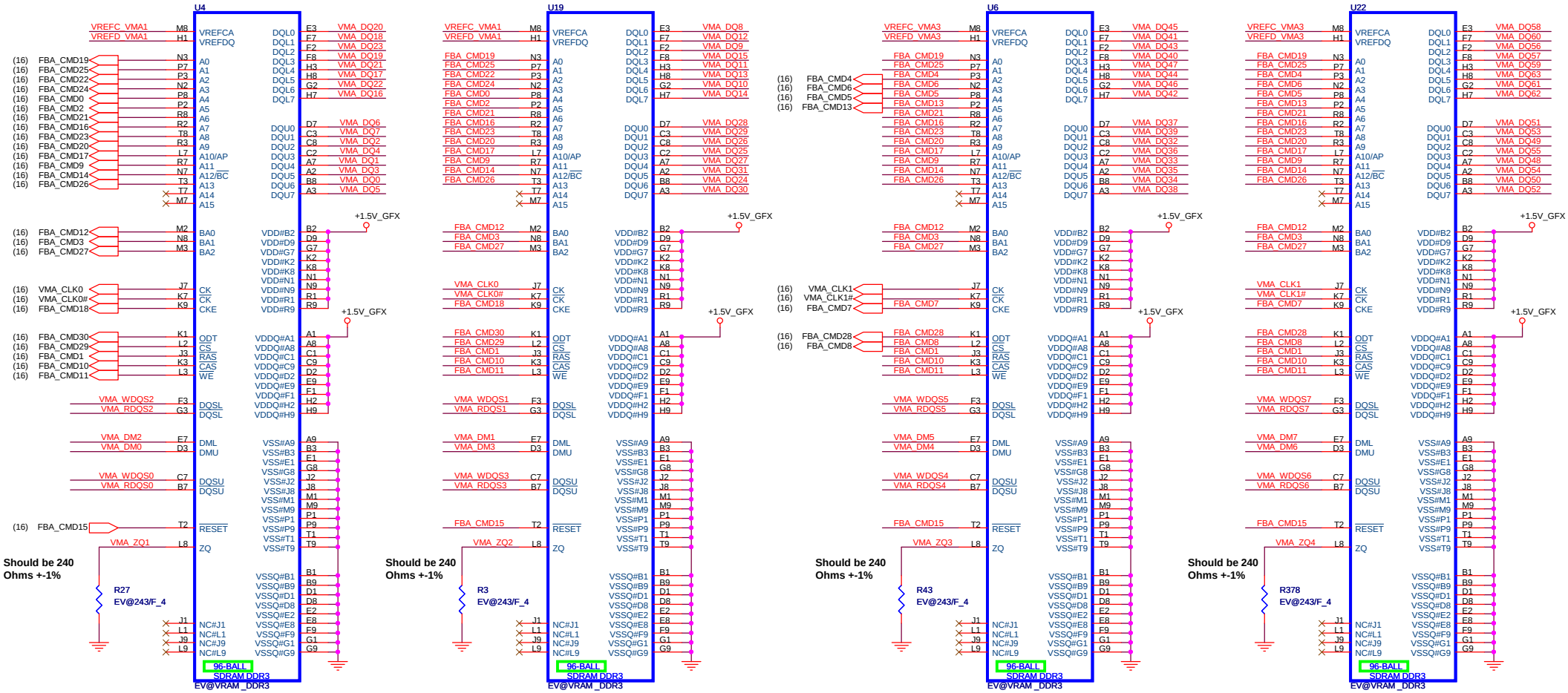
CHANNEL A: 256MB/512MB DDR3

(16) VMA_DQ[63..0]
(16) VMA_DM[7..0]
(16) VMA_WDQS[7..0]
(16) VMA_RDQS[7..0]



C6 C546 C556 C50 EV@1U/6.3V/X5R_4

C54 C7 C548 C49 C8 C5 EV@4.7U/6.3V/X5R_6 / EV@0.1U/10V/X5R_4

C45 C537 C555 C538 C542 C89 C543 C551 EV@0.1U/10V/X5R_4

C535 C536 C80 C51 C541 C550 C44 C544 EV@0.1U/10V/X5R_4

C46 C4 C115 C3 EV@0.1U/10V/X5R_4

PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11M (DDR3) 5/5	1A
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(3,4,8,9,10,11,12,13,14,15,21,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V
(29,35,37,39,41) +15V
(35,40,41) 5VSUS
(8,23,29,30,32,33,35,36,38,39,41,42) +3VPCU
(3,36,37,38,39,40,41,42) VIN
(12,21,22,25,29,30,31,32,33,35,36) +5V

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near PCH, then place these series Resistors near PCH

OPTION SIGNAL FROM PCH FOR UMA VGA

(8) LA_CLK — RN8 — 0_4P2R — TXLCLKOUT+
(8) LA_CLK# — TXLCLKOUT-
(8) LA_DATAP0 — RN14 — 0_4P2R — TXLOUT0+
(8) LA_DATAN0 — TXLOUT0-
(8) LA_DATAP1 — RN12 — 0_4P2R — TXLOUT1+
(8) LA_DATAN1 — TXLOUT1-
(8) LA_DATAP2 — RN10 — 0_4P2R — TXLOUT2+
(8) LA_DATAN2 — TXLOUT2-
(8) EDIDCLK_IGPU — RN17 — 0_4P2R — LCD_EDIDCLK
(8) EDIDDATA_IGPU — LCD_EDIDDATA
(8) LVDS_BLON_IGPU — R32 0_4 — LVDS_BLON
(8) DISP_ON_IGPU — R468 0_4 — LCD_DISP_ON
(8) DPST_PWM_IGPU — R432 0_4 — DPST_PWM

OPTION SIGNAL FROM N11M-GE2 to VGA

(17) EXT_TXLCLKOUT+ — RN9 — *EV@0_4P2R — TXLCLKOUT+
(17) EXT_TXLCLKOUT- — TXLCLKOUT-
(17) EXT_TXLOUT0+ — RN15 — *EV@0_4P2R — TXLOUT0+
(17) EXT_TXLOUT0- — TXLOUT0-
(17) EXT_TXLOUT1+ — RN13 — *EV@0_4P2R — TXLOUT1+
(17) EXT_TXLOUT1- — TXLOUT1-
(17) EXT_TXLOUT2+ — RN11 — *EV@0_4P2R — TXLOUT2+
(17) EXT_TXLOUT2- — TXLOUT2-
(18) EXT_LCD_EDIDCLK — RN18 — *EV@0_4P2R — LCD_EDIDCLK
(18) EXT_LCD_EDIDDATA — LCD_EDIDDATA
(18) EXT_LVDS_BLON — R31 *EV@0_4 — LVDS_BLON
(18) EXT_DISP_ON — R462 *EV@0_4 — LCD_DISP_ON
(18) EXT_DPST_PWM — R433 *EV@0_4 — DPST_PWM

+15V, +3V, LCDVCC
R469 330K_4
Q4 AO3404
LCDVCC_R — R70 0_8
C158 10U/6.3V/X5R_8
LCDVCC_ON
C622 0.022U/25V/X7R_6
R71 22_8
5VSUS
R470 100K_4
Q36 2N7002
Q37 2N7002
Q35 PDTC144EU
LCD_DISP_ON
R466 100K_4
LCDVCC
R50 2.2K_4
R51 2.2K_4
LCD_EDIDCLK
LCD_EDIDDATA

back light

+3VPCU, +3V
R19 10K_4
R424 *4.7K_4
(30,32) LID551#
D3 RB500V-40
D13 RB500V-40
DISPON
C78 0.1U/10V/X5R_4
R428 100K_4
C576 *47P/50V/NPO_4
LVDS_BLON — R35 *0_4_short — R38 2.2K_4
R37 10K_4
C563 *1U/10V/X5R_6
Q3 PDTC144EU
LCD_BK_OFF#

+VIN_BLIGHT
C98 0.1U/25V/X5R_6
C97 0.1U/25V/X5R_6
C137 *10U/25V/X6S_12
R45 0_8 — VIN
DPST_PWM — R427 0_4S — VADJ_PWM
(30) BRIGHT_PWM — R425 *0_4
C567 *47P/50V/NPO_4

CN7 CONN_LCD
C568 *47P/50V/NPO_4
(25) DMIC_DAT
(25) DMIC_CLK — R423 0_4 — DMIC_CLK_L
+CAM_VCC
USBP3-
USBP3+
+VIN_BLIGHT
DISPON
VADJ_PWM
TXLCLKOUT+
TXLCLKOUT-
TXLOUT2+
TXLOUT2-
TXLOUT1+
TXLOUT1-
TXLOUT0+
TXLOUT0-
LCD_EDIDDATA
LCD_EDIDCLK
+3V
LCDVCC
C1501U/10V/X5R_4
C1540.1U/10V/X5R_4

20100208
REMOVE "*"
(10) USBP3-
(10) USBP3+
L26 DLW21HN900SQ2L
USBP3-
USBP3+

CAMERA VCC Control

+5V, +3V, +CAM_VCC
C620 *1U/6.3V/X5R_4
R449 *0_4
(11) CCD_ON — R448 *0_4
U24 *AT5231H-3.3KER
VIN, VOUT, SHDN, GND, SET
R463 0_8
R447 *215K/F_4
R446 *100K/F_4
C599 4.7U/6.3V/X5R_6

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Quanta Computer Inc.

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Custom	LCD CONN	1A
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(12,20,22,25,29,30,31,32,33,35,36) +5V
(3,4,8,9,10,11,12,13,14,15,20,22,24,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V

CRT_VCC
D14 RB500V-40
C572 0.1U/10V/X5R_4
+5V
F3 FUSE1A6V_POLY
CRT_VCC_R
RV11 *VARISTOR_4

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

CRT_R L14 BLM18BA470SN1_6 CRT_R1
CRT_G L13 BLM18BA470SN1_6 CRT_G1
CRT_B L11 BLM18BA470SN1_6 CRT_B1

R72 150/F_4
R69 150/F_4
R48 150/F_4
C162 5.6P/50V/COG_4
C159 5.6P/50V/COG_4
C142 5.6P/50V/COG_4
C143 5.6P/50V/COG_4
C180 5.6P/50V/COG_4
C161 5.6P/50V/COG_4

CN13 CRT
TP4

ESD PROTECTION
D10 *TVSS5VESPT CRT_R1
D9 *TVSS5VESPT CRT_G1
D6 *TVSS5VESPT CRT_B1
D5 *TVSS5VESPT CRTVSYNC
D7 *TVSS5VESPT CRTHSYNC
D4 *TVSS5VESPT DDCCLK3
D8 *TVSS5VESPT DDCDAT3

+5V
C575 0.1U/10V/X5R_4
VSYNC_COM
U23 AHCT1G125DCH
VGAVSYNC_R
R44 10_4
CRTVSYNC1
L10 HB-1T1608-121JT_6 CRTVSYNC

+5V
C621 0.1U/10V/X5R_4
HSYNC_COM
U25 AHCT1G125DCH
VGAHSYNC_R
R49 10_4
CRTHSYNC1
L12 HB-1T1608-121JT_6 CRTHSYNC

Place near U5001,U5002 < 200 mil

C146 *10P/50V/C0G_4
C118 *10P/50V/C0G_4
C149 10P/50V/C0G_4
C135 10P/50V/C0G_4

Place near CN5002 connector < 200 mil

+3V
R464 10K_4
R409 10K_4
CRT_VCC
R58 2.2K_4
R41 2.2K_4

CRT_DDCCLK
Q30 2N7002E
DDCCLK2 R40 *0_6_short DDCCLK3

+3V
CRT_DDCDATA
Q34 2N7002E
DDCDAT2 R65 *0_6_short DDCDAT3

C152 *10P/50V/C0G_4
C96 *10P/50V/C0G_4

FOR UMA

(8) CRT_R_IGPU	R405	0_4	CRT_R
(8) CRT_G_IGPU	R411	0_4	CRT_G
(8) CRT_B_IGPU	R414	0_4	CRT_B
(8) HSYNC_COM_IGPU	R400	0_4	HSYNC_COM
(8) VSYNC_COM_IGPU	R396	0_4	VSYNC_COM
(8) DDCCLK_IGPU	R385	0_4	CRT_DDCCLK
(8) DDCDATA_IGPU	R390	0_4	CRT_DDCDATA

FOR DISCRETE

(17) EXT_CRT_RED	R406	*EV@0_4	CRT_R
(17) EXT_CRT_GREEN	R412	*EV@0_4	CRT_G
(17) EXT_CRT_BULE	R415	*EV@0_4	CRT_B
(17) EXT_HSYNC_COM	R397	*EV@0_4	HSYNC_COM
(17) EXT_VSYNC_COM	R394	*EV@0_4	VSYNC_COM
(18) EXT_CRT_DDCCLK	R386	*EV@0_4	CRT_DDCCLK
(18) EXT_CRT_DDCDATA	R391	*EV@0_4	CRT_DDCDATA

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Custom	CRT CONN	1A
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For UMA HDMI function

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Signals		PDT	CHR	PIM
PC1	Ra	NC	NC	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	4.7K	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

Signals		PDT		
EMI0	Rh	NC	NC	NC
EMI1	Ri	NC	NC	NC
ASQ0	Rj	4.7K	NC	NC
ASQ1	Rk	499	1.2K	4.7K

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318002
Vendor:PIM P/N:ALP411LS004

Signals	PS8171	
PIN 3	LEVEL	EQ
PC0/PEQ	HIGH	7db
	MID	※ 2db
	LOW	4db

Signals	PS8171	
PIN 4	LEVEL	EQ
PC1/PIO	HIGH	1.2db
	MID	2db
	LOW	※ 0db

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

PS8171

FOR UMA ONLY
FROM LEVEL SHIFTER

PLACE CLOSE HDMI CONN

FOR DISCRETE

FOR DISCRETE ONLY

DFHD19MR017

DISCRETE HDMI I2C SELECT
Close to HDMI Connector

FOR DISCRETE ONLY

0212 Update footprint.
UMA use +3V for the detect pin
Dis use +3V_VGA for the detect pin

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Quanta Computer Inc.

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Custom	HDMI CONN	3A
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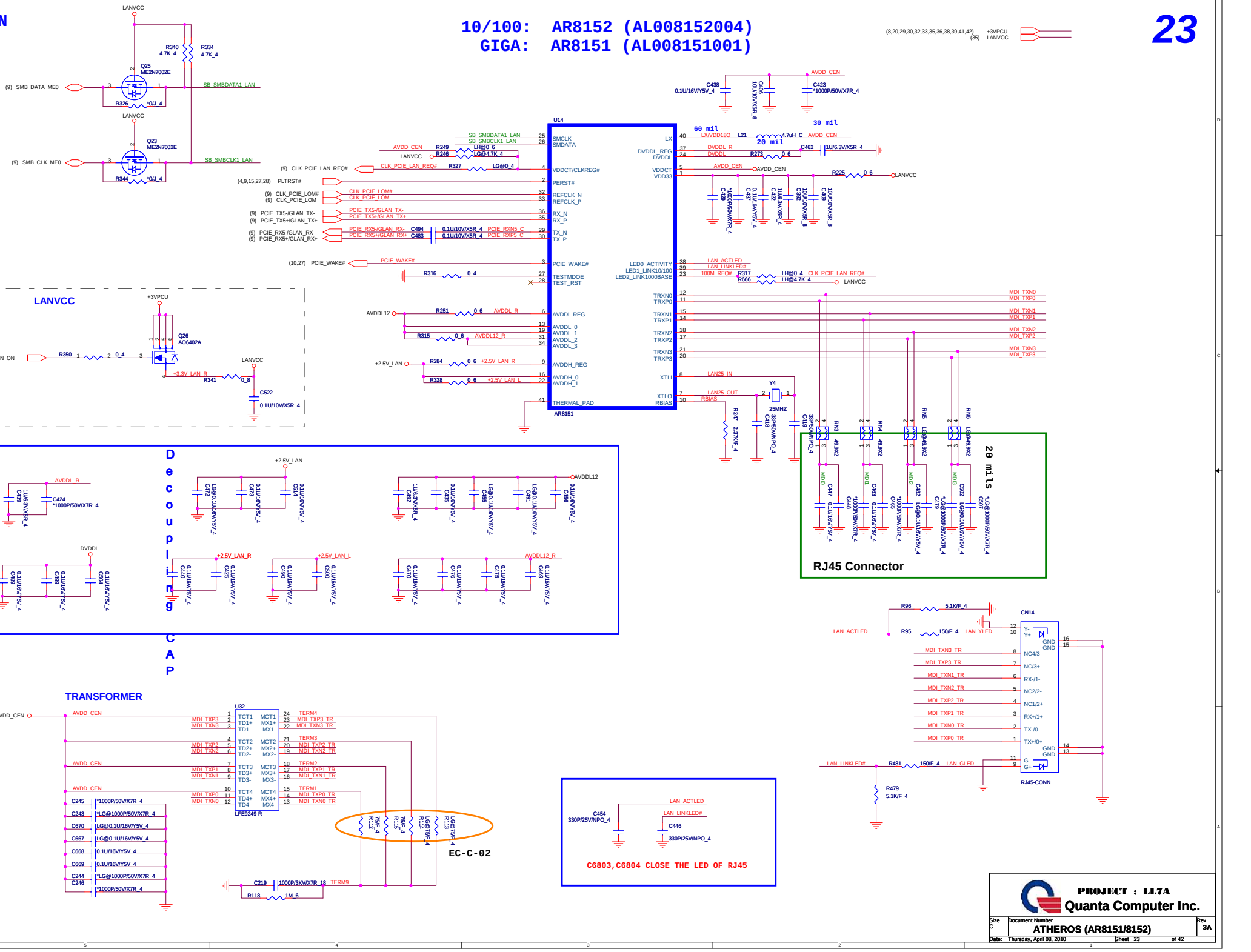
LAN

10/100: AR8152 (AL008152004)
GIGA: AR8151 (AL008151001)

(8,20,29,30,32,33,35,36,38,39,41,42) +3VPCU
(35) LANVCC



PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
C	ATHEROS (AR8151/8152)	3A

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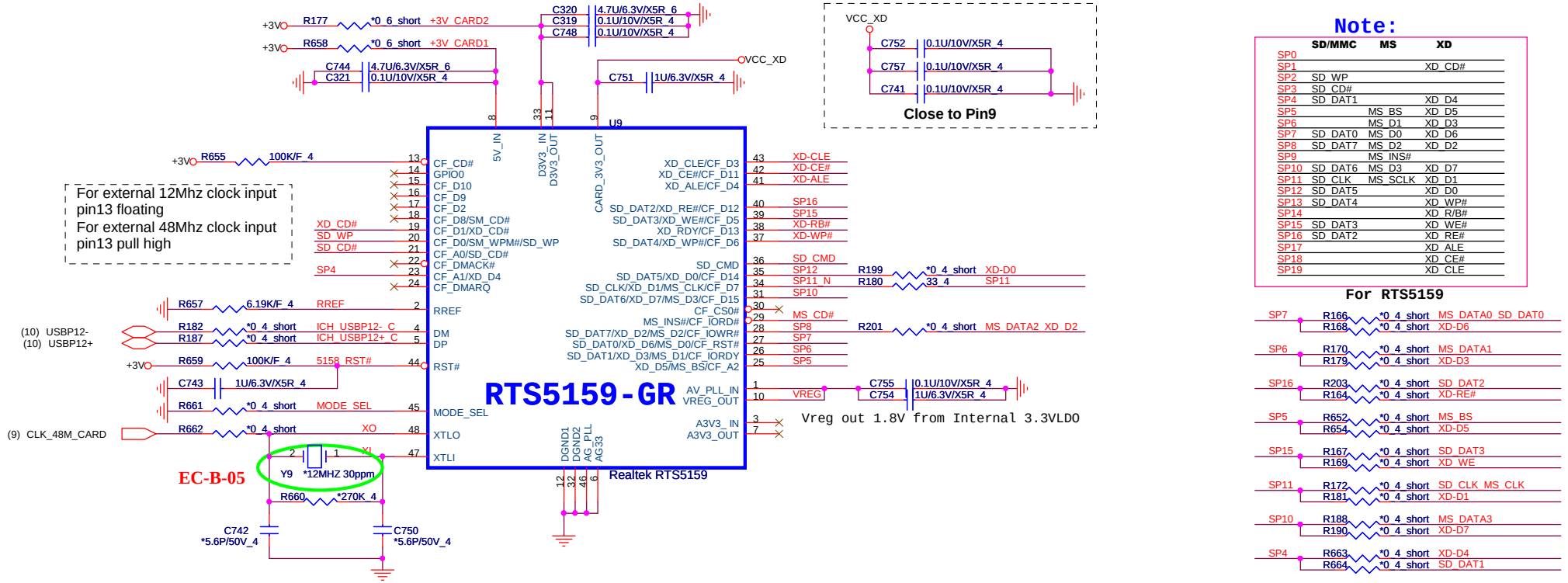
(3,4,8,9,10,11,12,13,14,15,20,21,22,25,26,27,28,29,30,31,32,33,35,36,40,41) +3V



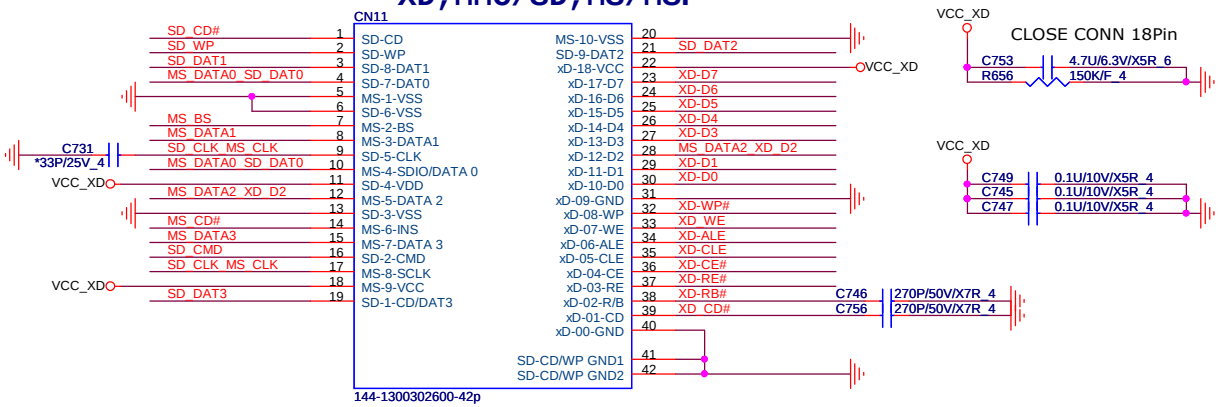
Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

For RTS5159

SP7	R166	*0_4_short	MS_DATA0_SD_DAT0
	R168	*0_4_short	XD-D6
SP6	R170	*0_4_short	MS_DATA1
	R179	*0_4_short	XD-D3
SP16	R203	*0_4_short	SD_DAT2
	R164	*0_4_short	XD-RE#
SP5	R652	*0_4_short	MS_BS
	R654	*0_4_short	XD-D5
SP15	R167	*0_4_short	SD_DAT3
	R169	*0_4_short	XD_WE
SP11	R172	*0_4_short	SD_CLK_MS_CLK
	R181	*0_4_short	XD-D1
SP10	R188	*0_4_short	MS_DATA3
	R190	*0_4_short	XD-D7
SP4	R663	*0_4_short	XD-D4
	R664	*0_4_short	SD_DAT1

5 IN1 CARD READER
XD,MMC/SD,MS/MSP



PROJECT : LL7A

Quanta Computer Inc.

Size	Document Number	Rev
B	CARD READER (Realtek RTS5159)	3A

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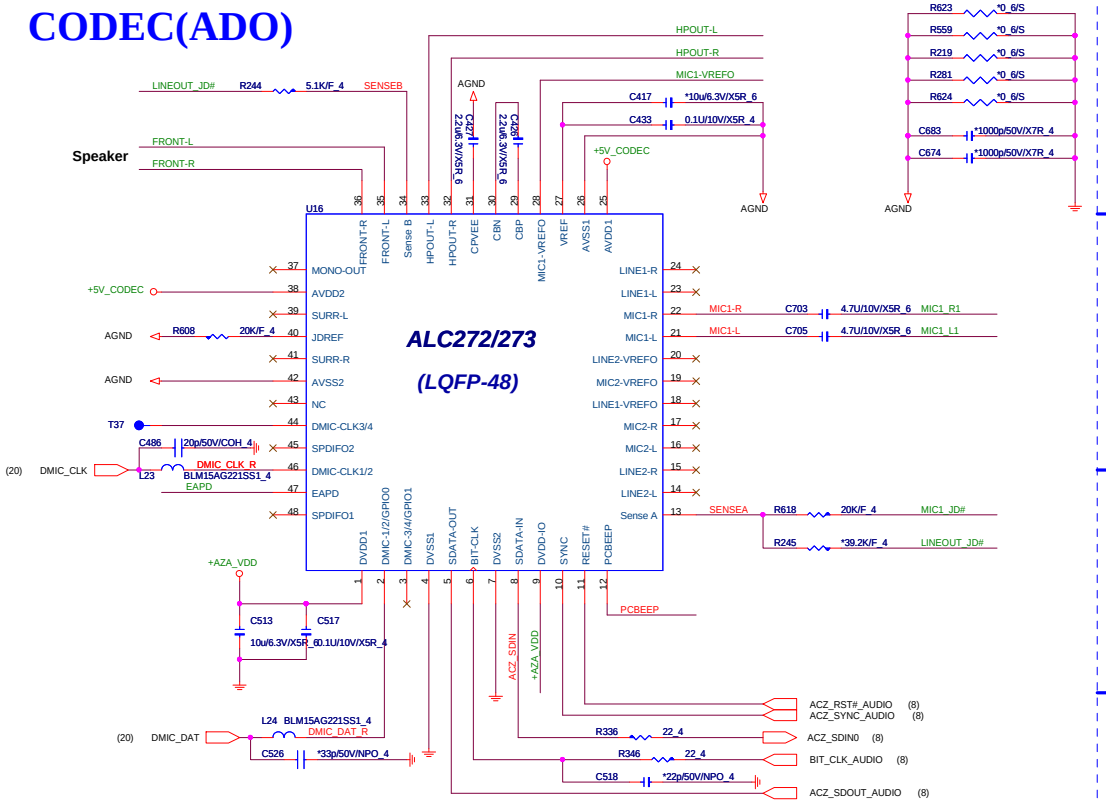
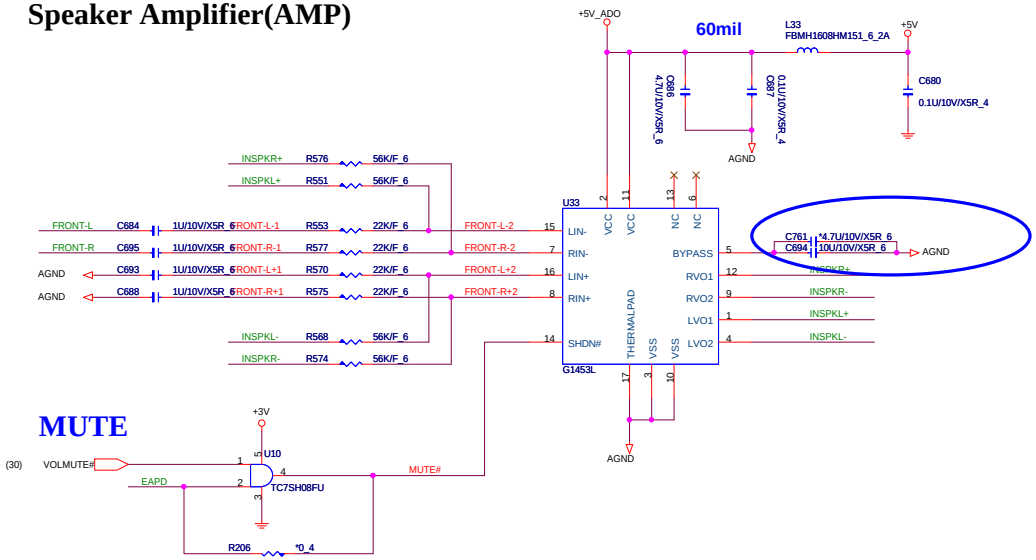
CODEC(ADO)

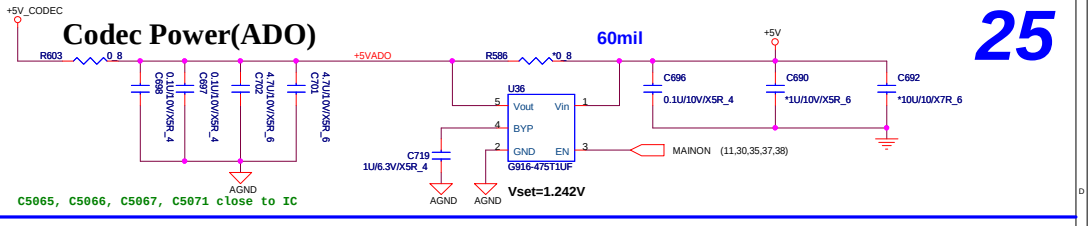


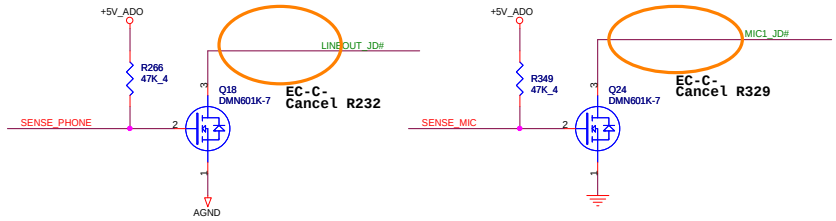
Speaker Amplifier(AMP)



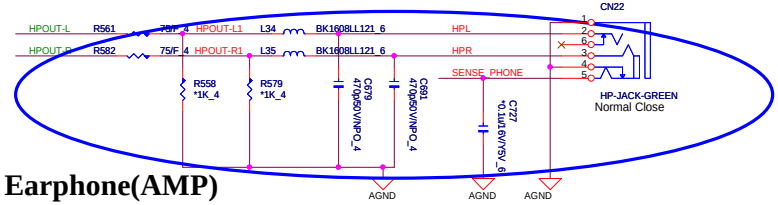
MUTE

Codec Power(ADO)

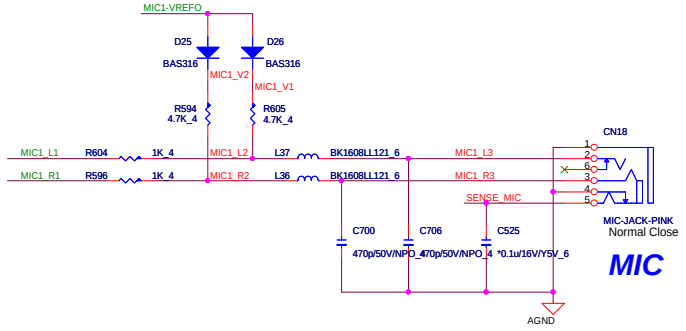




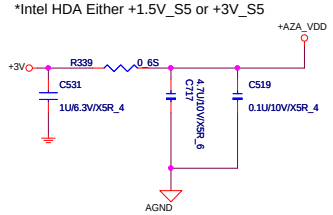
Earphone(AMP)



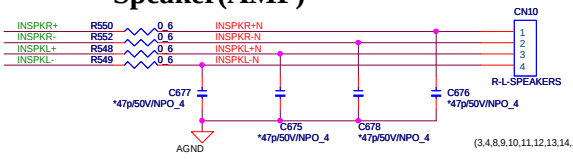
System MIC(AMP)



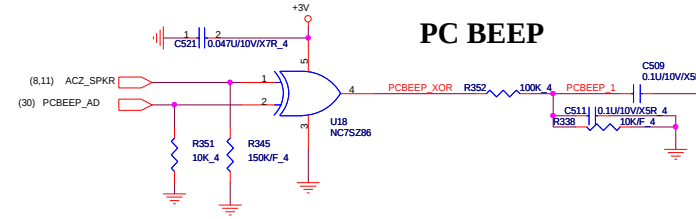
HDA Power(ADO)



Speaker(AMP)



PC BEEP



PROJECT : LL7A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	AL272/AMP/MIC/HP/SPK	3A
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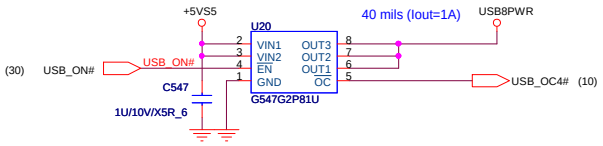
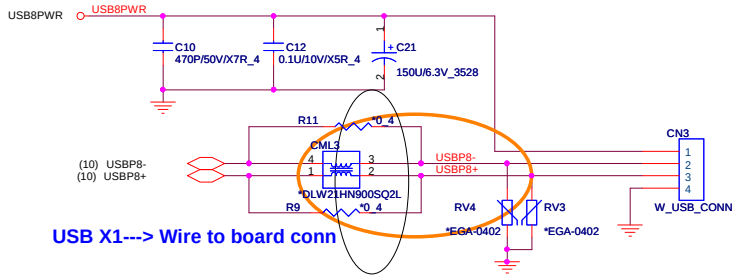
USB 3

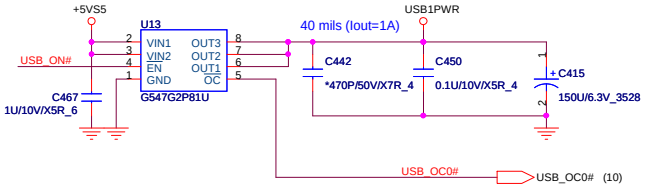


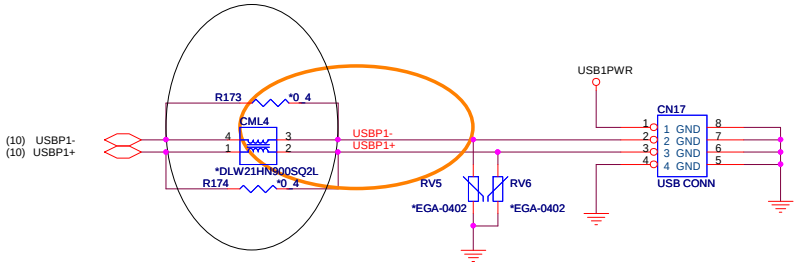


USB X1---> Wire to board conn

(12,35) +5VS5
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,27,28,29,30,31,32,33,35,36,40,41) +3V

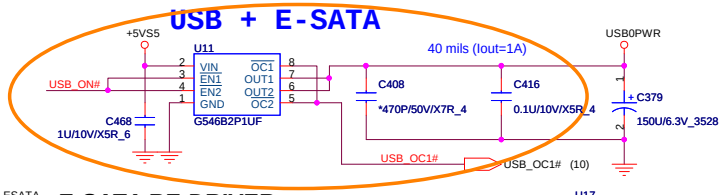
USB 2

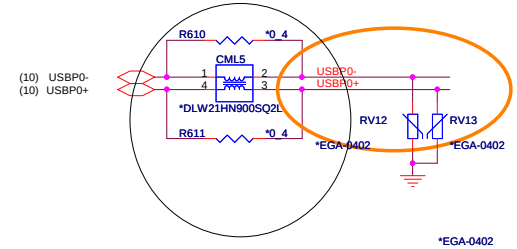


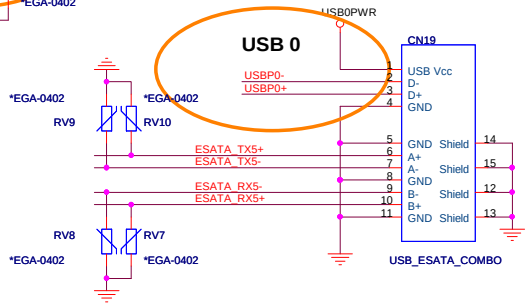


USB 1

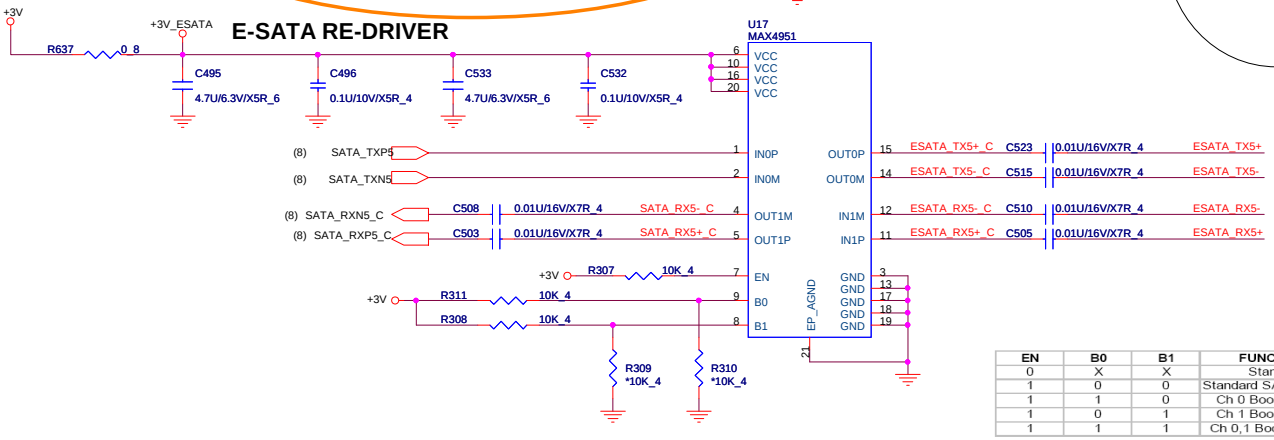
USB + E-SATA







E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USBX2/USB+ESATA	3A
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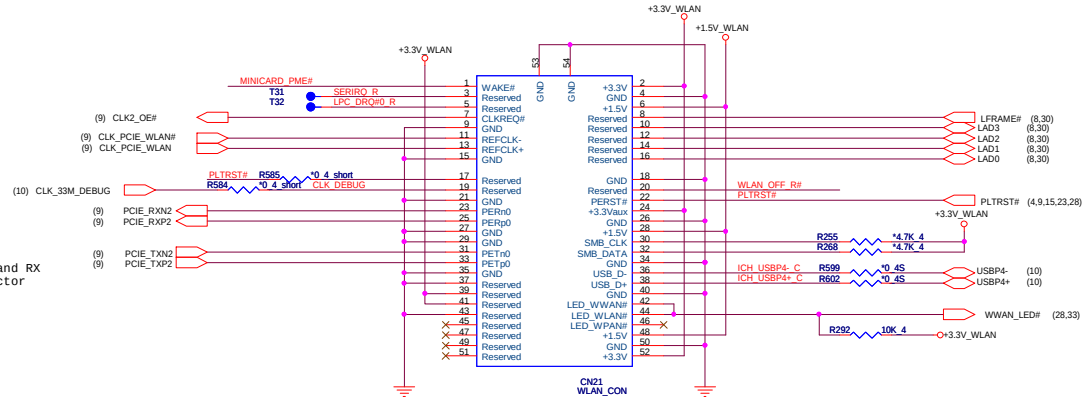
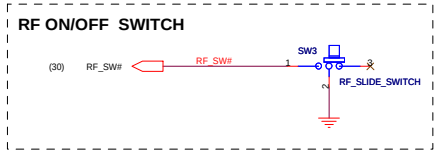
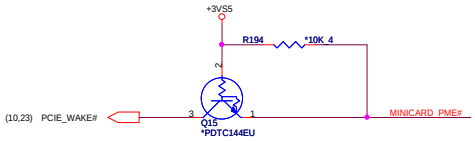
MiniCard WLAN/WiMAX connector

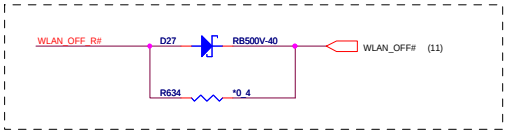
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,28,29,30,31,32,33,35,36,40,41) +3V
(3,28,37) +1.5V
(4,8,9,10,11,12,15,35) +3VS5

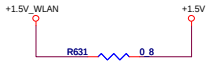
PCI-Express TX and RX direct to connector

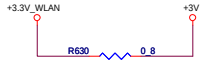


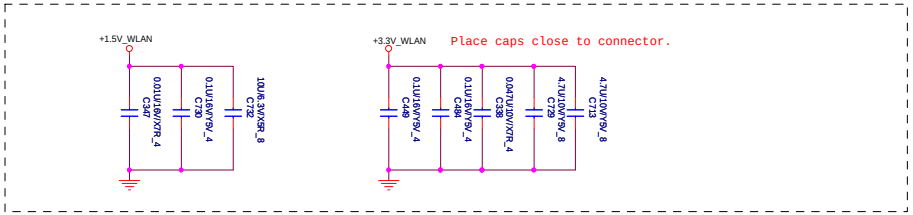












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Quanta Computer Inc.

Size	Document Number	Rev
C	MINI-CARD (WLAN)	1A

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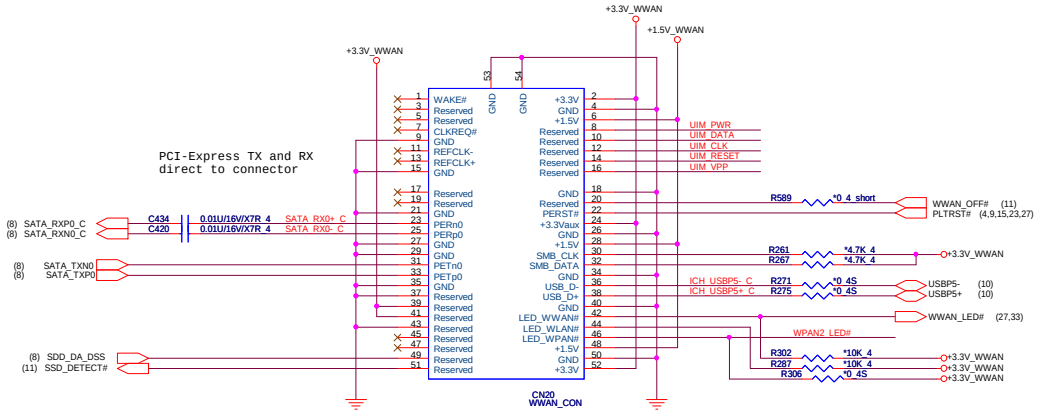
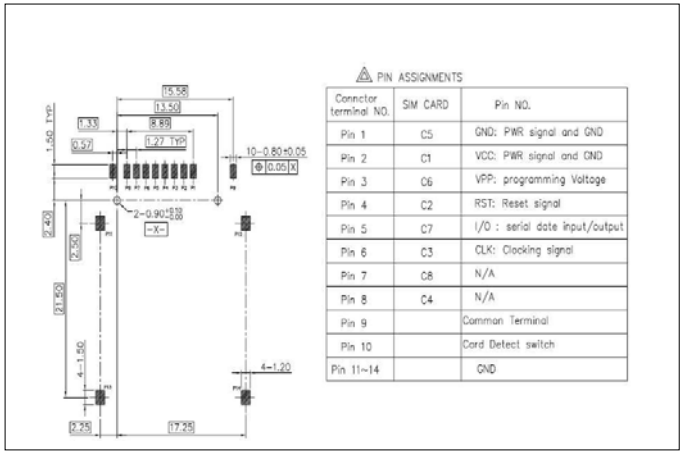
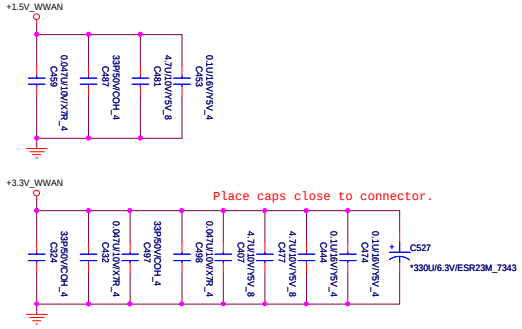
MiniCard WWAN connector



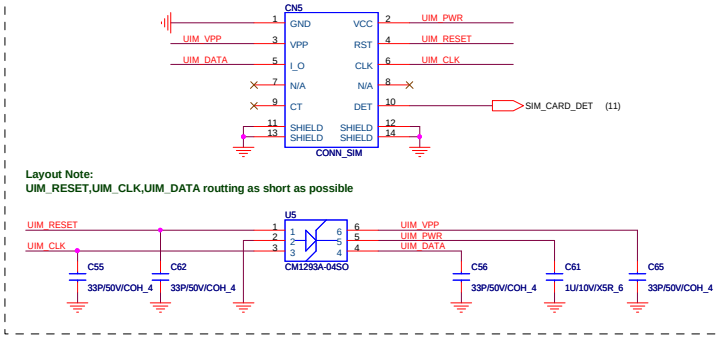


PIN ASSIGNMENTS

Connctor terminal NO.	SIM CARD	Pin NO.
Pin 1	C5	GND: PWR signal and GND
Pin 2	C1	VCC: PWR signal and GND
Pin 3	C6	VPP: programming Voltage
Pin 4	C2	RST: Reset signal
Pin 5	C7	I/O : serial date input/output
Pin 6	C3	CLK: Clocking signal
Pin 7	C8	N/A
Pin 8	C4	N/A
Pin 9		Common Terminal
Pin 10		Card Detect switch
Pin 11~14		GND



SIM Card CONN



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Quanta Computer Inc.

Size	Document Number	Rev
C	MINI-CARD (WWAN/SSD)	1A

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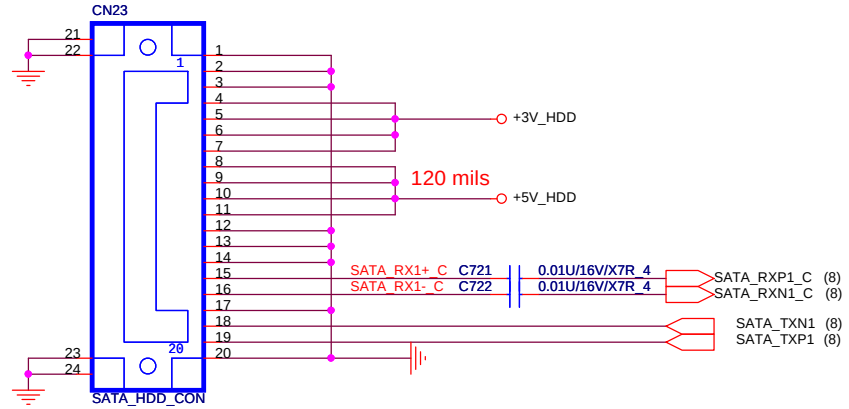
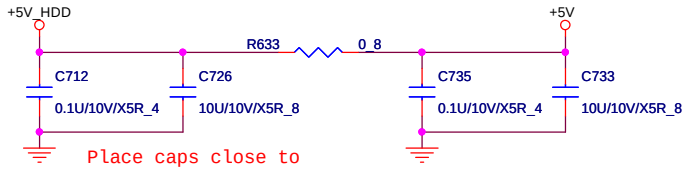
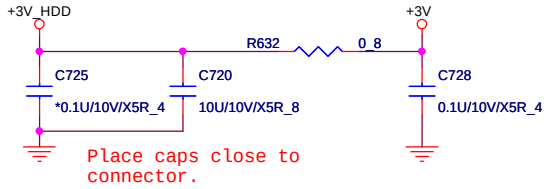
SATA-HDD CONNECTOR

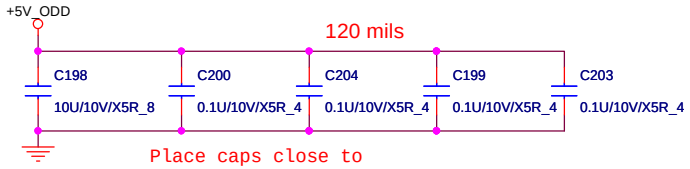


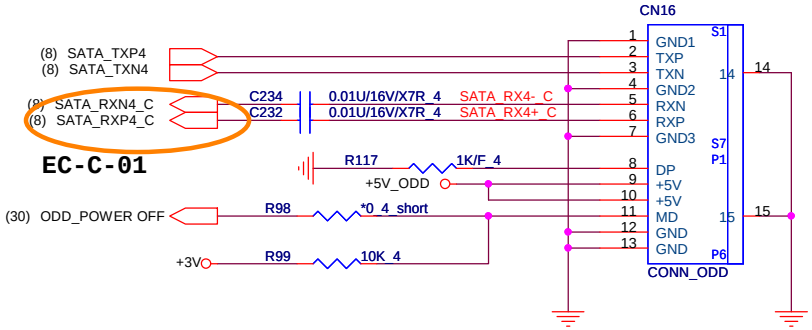
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,30,31,32,33,35,36,40,41) +3V
(12,20,21,22,25,30,31,32,33,35,36) +5V
(20,35,37,39,41) +15V
(35,36,37,38,39,41,42) 5VPCU
(8,20,23,30,32,33,35,36,38,39,41,42) +3VPCU



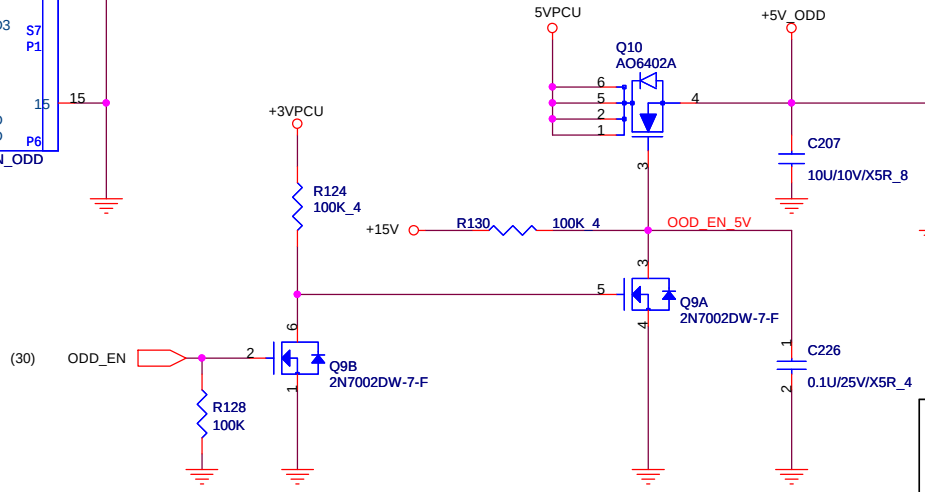


SATA CD-ROM





20100208 Del R110, +5V



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Quanta Computer Inc.

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Custom	HDD/ODD	3A
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(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,31,32,33,35,36,40,41) +3V
(8,20,23,29,32,33,35,36,38,39,41,42) +3VPCU
(8,12) +RTC_CELL
(12,20,21,22,25,29,31,32,33,35,36) +5V

IT8502E

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

(For PLL Power)

DIS =>R164
UMA=>R163

R298	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

1Mbit (512K Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

W25X16AVSSIG

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Custom	KBC IT8502E	1A

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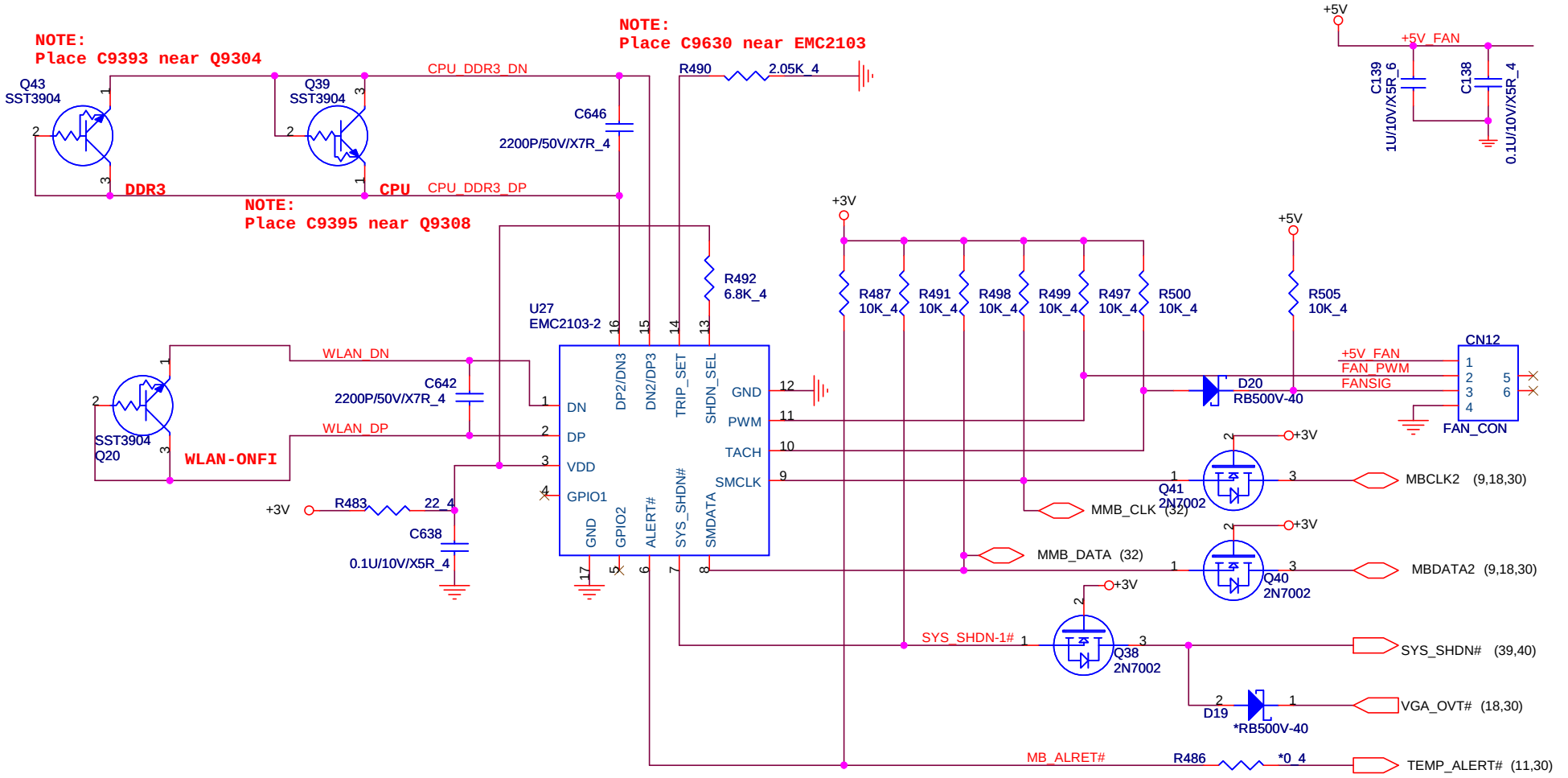
FAN CONTROL

(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,32,33,35,36,40,41) +3V
(12,20,21,22,25,29,30,32,33,35,36) +5V

31



PROJECT : LL7A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN / THERMAL	1A
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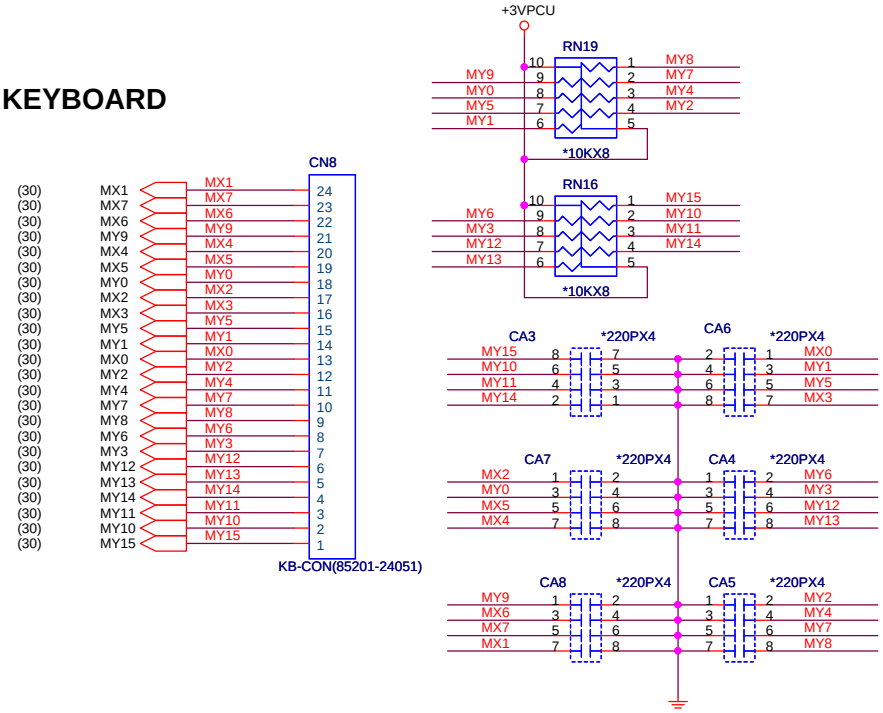
KEYBOARD

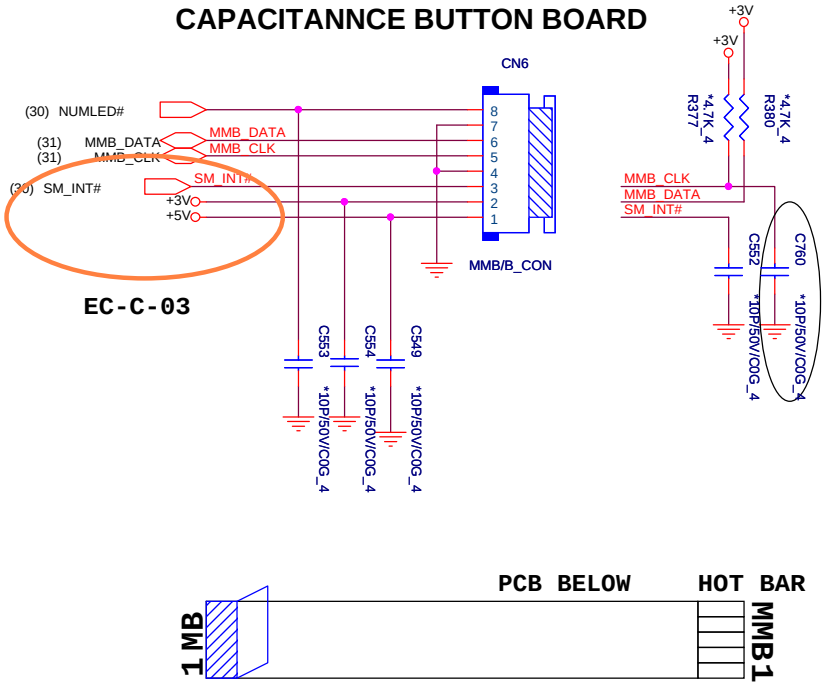


For EMI request

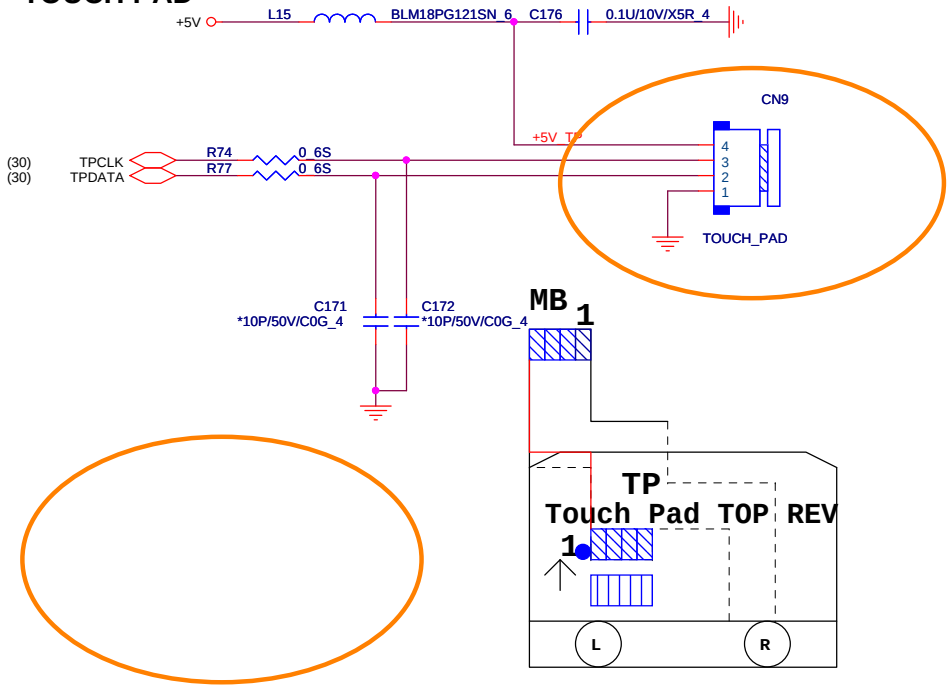
CAPACITANNCE BUTTON BOARD

(8,20,23,29,30,33,35,36,38,39,41,42) +3VPCU
(12,20,21,22,25,29,30,31,33,35,36) +5V
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,33,35,36,40,41) +3V

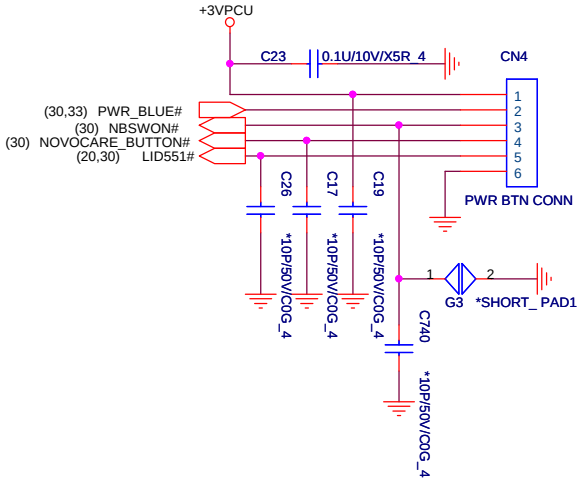
32

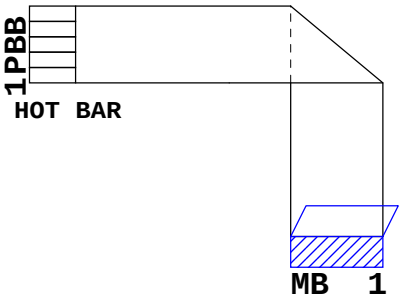


TOUCH PAD



POWER BUTTON BOARD





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Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/TP/PW-B/CTS	3A

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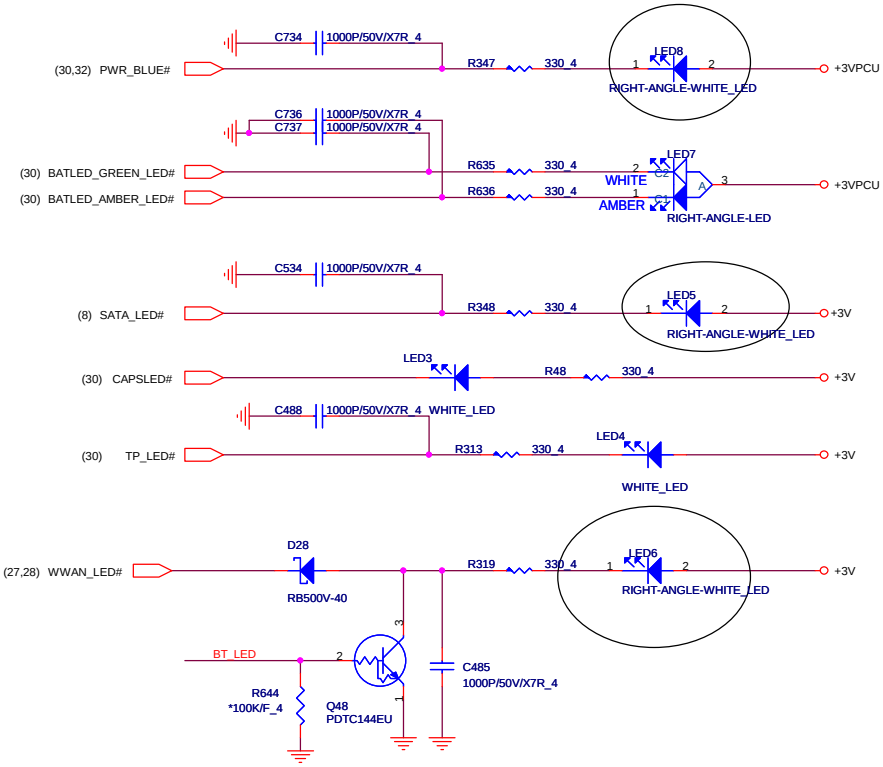
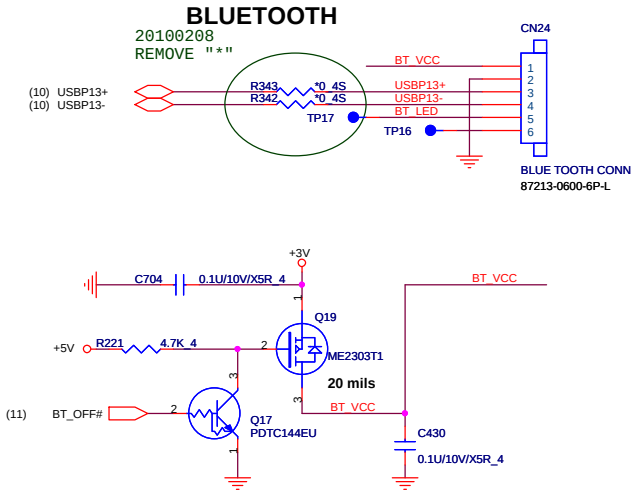
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,35,36,40,41) +3V
(12,20,21,22,25,29,30,31,32,35,36) +5V
(8,20,23,29,30,32,35,36,38,39,41,42) +3VPCU

LED



BLUETOOTH



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Quanta Computer Inc.

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Custom	LED/BT	1A

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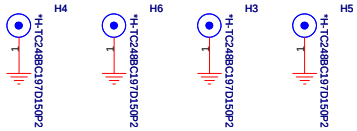
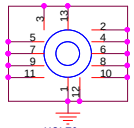
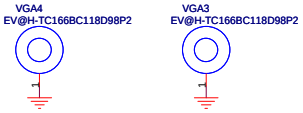
CPU BKT



CRT HOLE

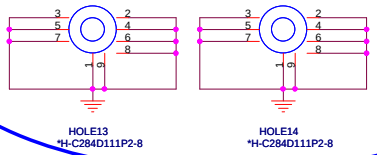


GPU NUT

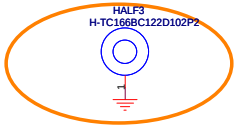


ODD HOLE

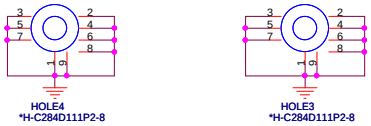
KEYBOARD HOLE



WLAN nut

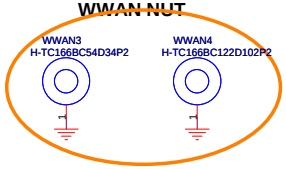


BATTERY HOLE

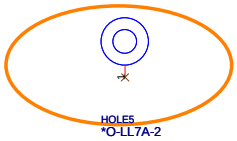


WLAN CABLE HOLE

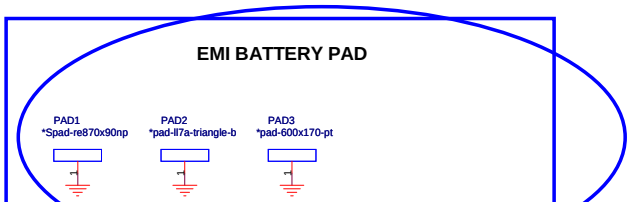
WWAN NUT



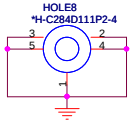
WLAN CABLE HOLE



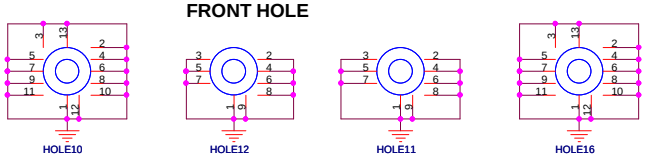
EMI BATTERY PAD



DDR 3 HOLE



FRONT HOLE



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Quanta Computer Inc.

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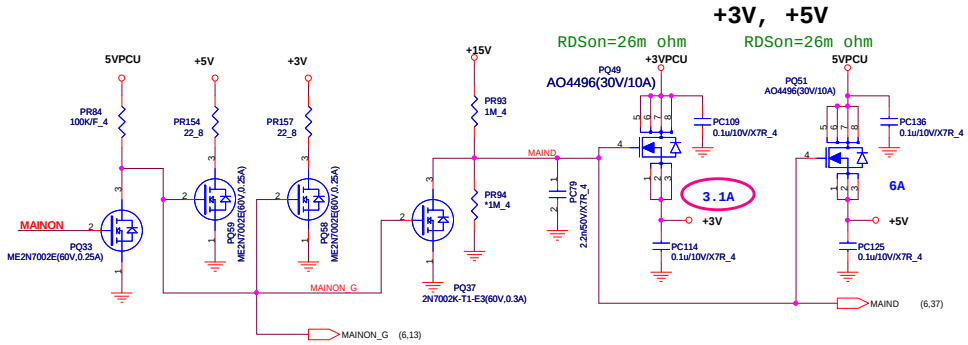
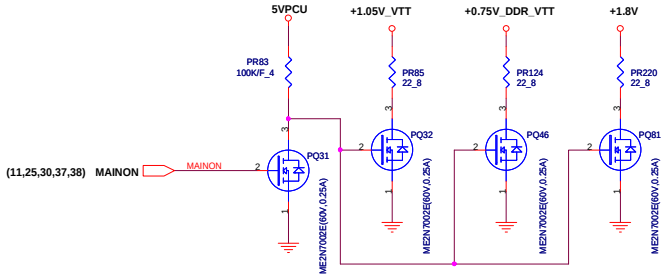
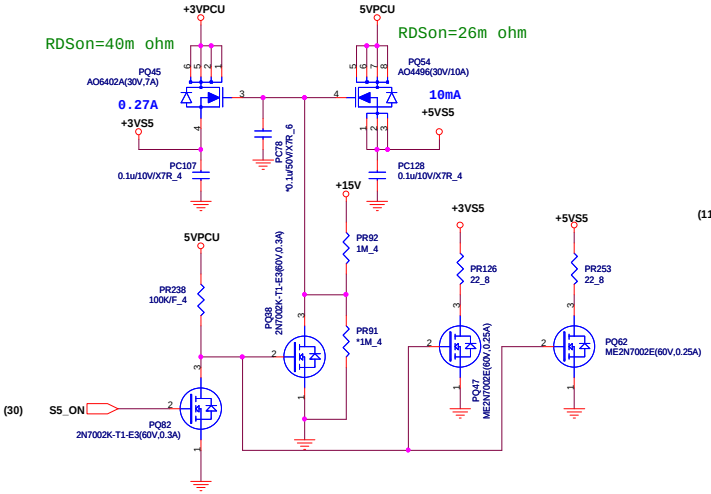
DISCHARGE

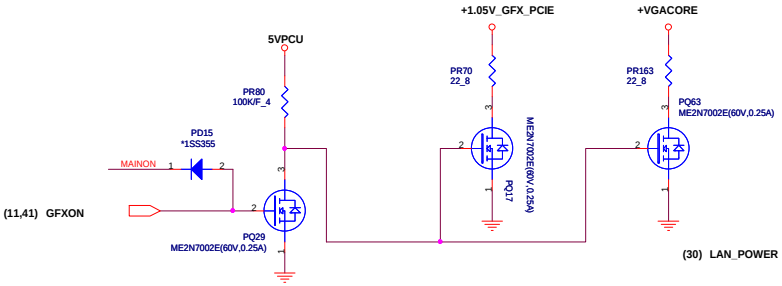
+3V, +5V



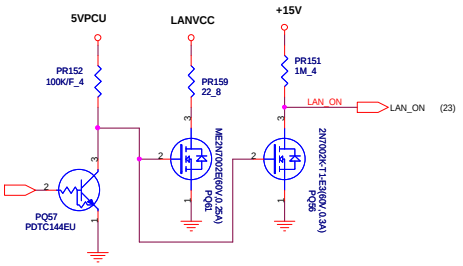


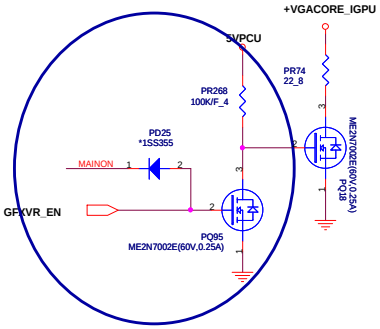
3V_S5, 5V_S5



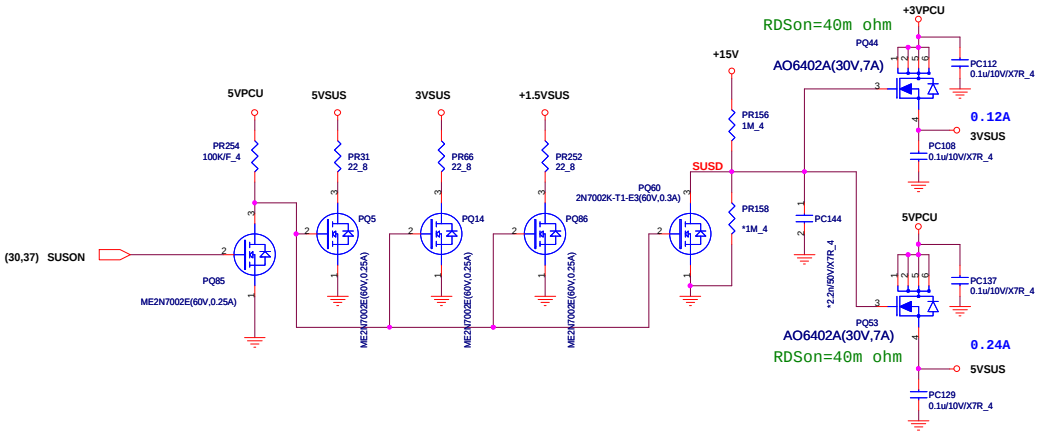


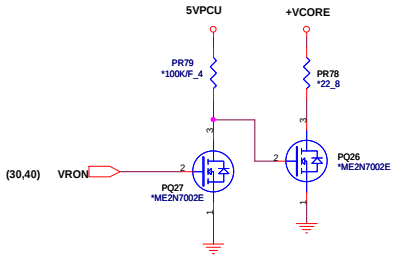
LANVCC





3VSUS, 5VSUS





(20,29,37,39,41) +15V
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,36,40,41) +3V
(12,20,21,22,25,29,30,31,32,33,36) +5V
(6,12,38,41) +1.8V
(3,4,6,8,9,10,11,12,38,40,42) +1.05V_VTT
(13,14,37) +0.75V_DDR_VTT
(29,36,37,38,39,41,42) 5VPCU
(8,20,23,29,30,32,33,36,38,39,41,42) +3VPCU
(23) LANVCC
(15,41) +VGACORE
(15,16,17,41) +1.05V_GFX_PCIE
(6,42) +VGACORE_IGPU
(4,8,9,10,11,12,15,27) +3VS5
(12,26) +5VS5
(20,40,41) 5VSUS
(30,41) 3VSUS
(4,6,13,14,37,41) +1.5VSUS
(6,40) +vCORE

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Quanta Computer Inc.

Size	Document Number	Rev
C	DISCHARGE	1A

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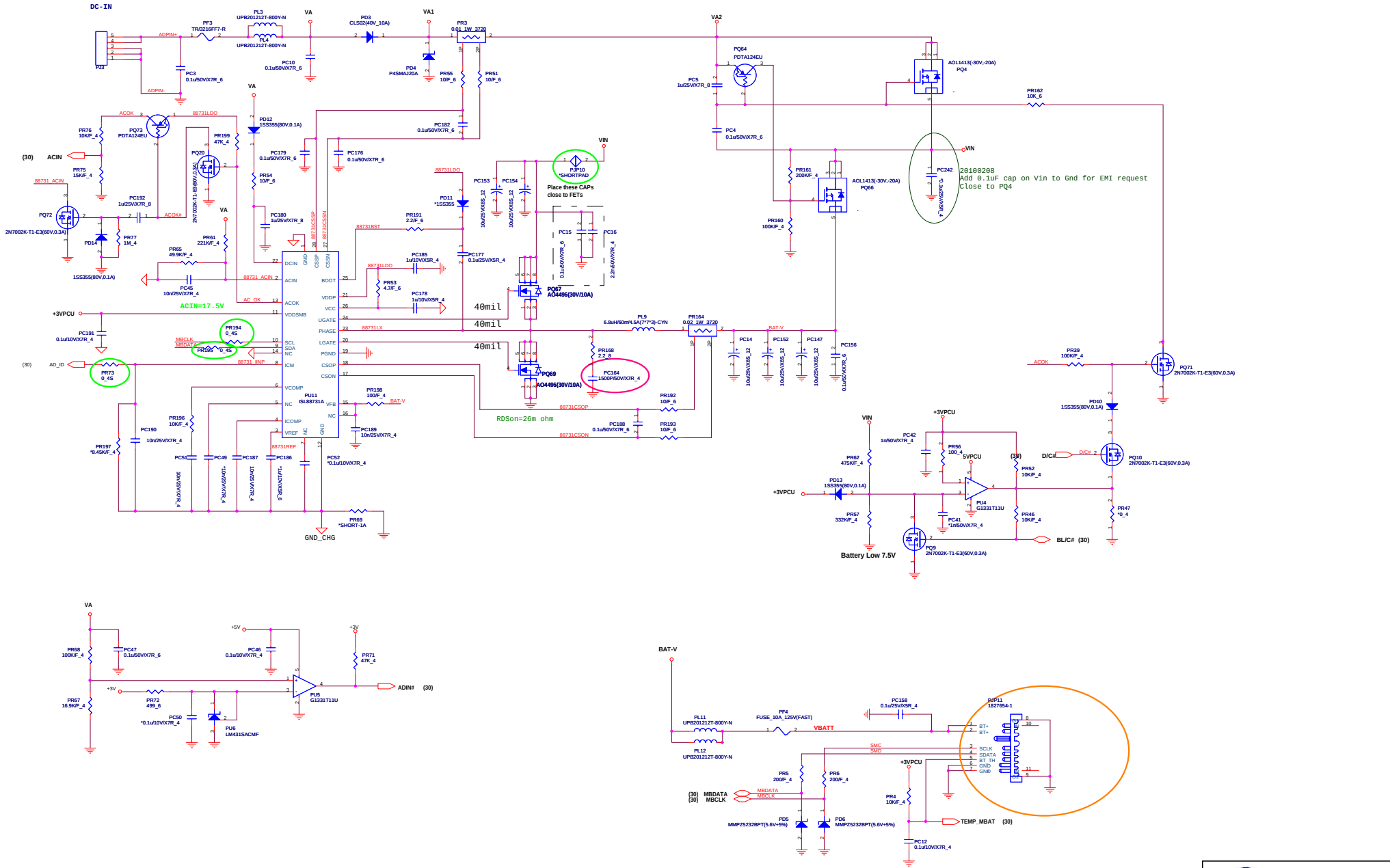
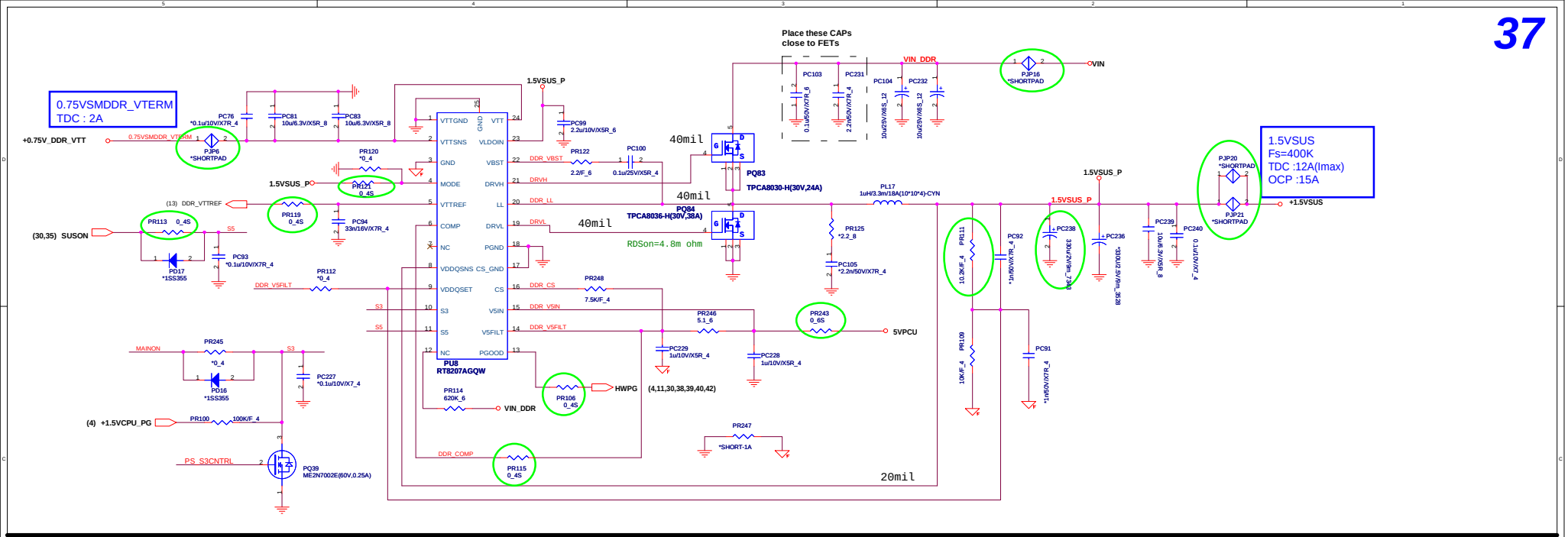
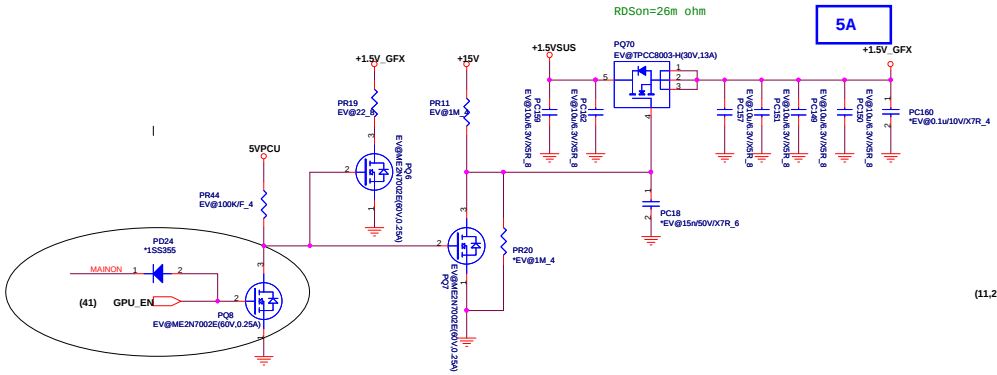
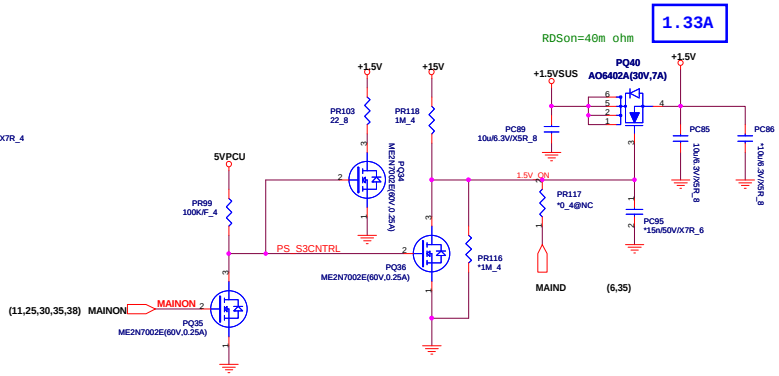
(3,20,37,38,39,40,41,42) VIN
(8,20,23,29,30,32,33,35,38,39,41,42) +3VPCU
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,40,41) +3V
(12,20,21,22,25,29,30,31,32,33,35) +5V









(3,20,36,38,39,40,41,42) VIN
(4,6,13,14,35,41) +1.5VSUS
(29,35,36,38,39,41,42) 5VPCU
(13,14,35) +0.75V_DDR_VTT
(3,27,28) +1.5V
(20,29,35,39,41) +15V
(15,16,19) +1.5V_GFX

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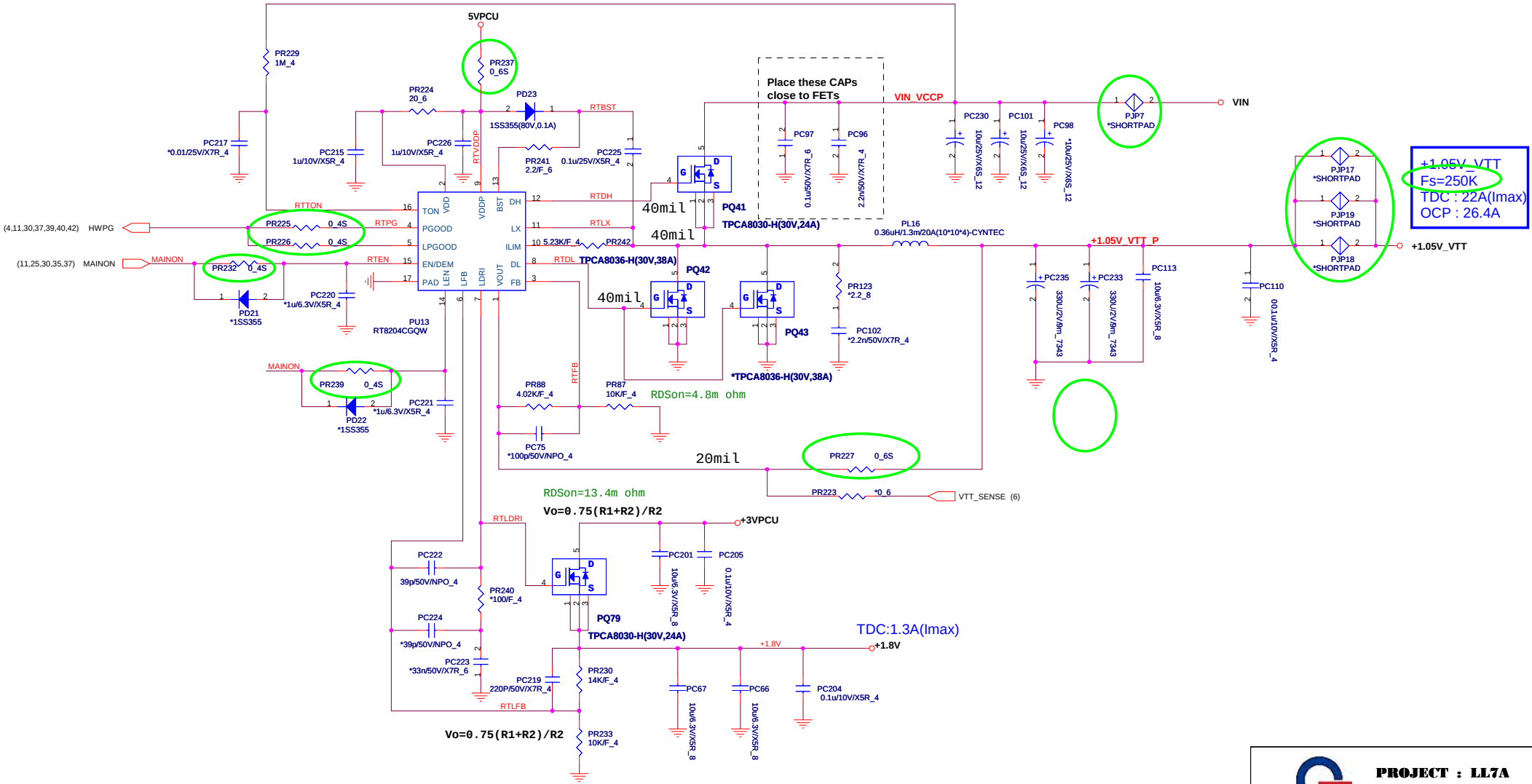
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207AGQW)	1A

Date: Thursday, April 08, 2010 Sheet 37 of 42

(3,20,36,37,39,40,41,42) VIN
(3,4,6,8,9,10,11,12,35,40,42) +1.05V_VTT
(6,12,35,41) +1.8V
(8,20,23,29,30,32,33,35,36,39,41,42) +3VPCU
(29,35,36,37,39,41,42) 5VPCU



PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V_VTT (RT8204C)	1A

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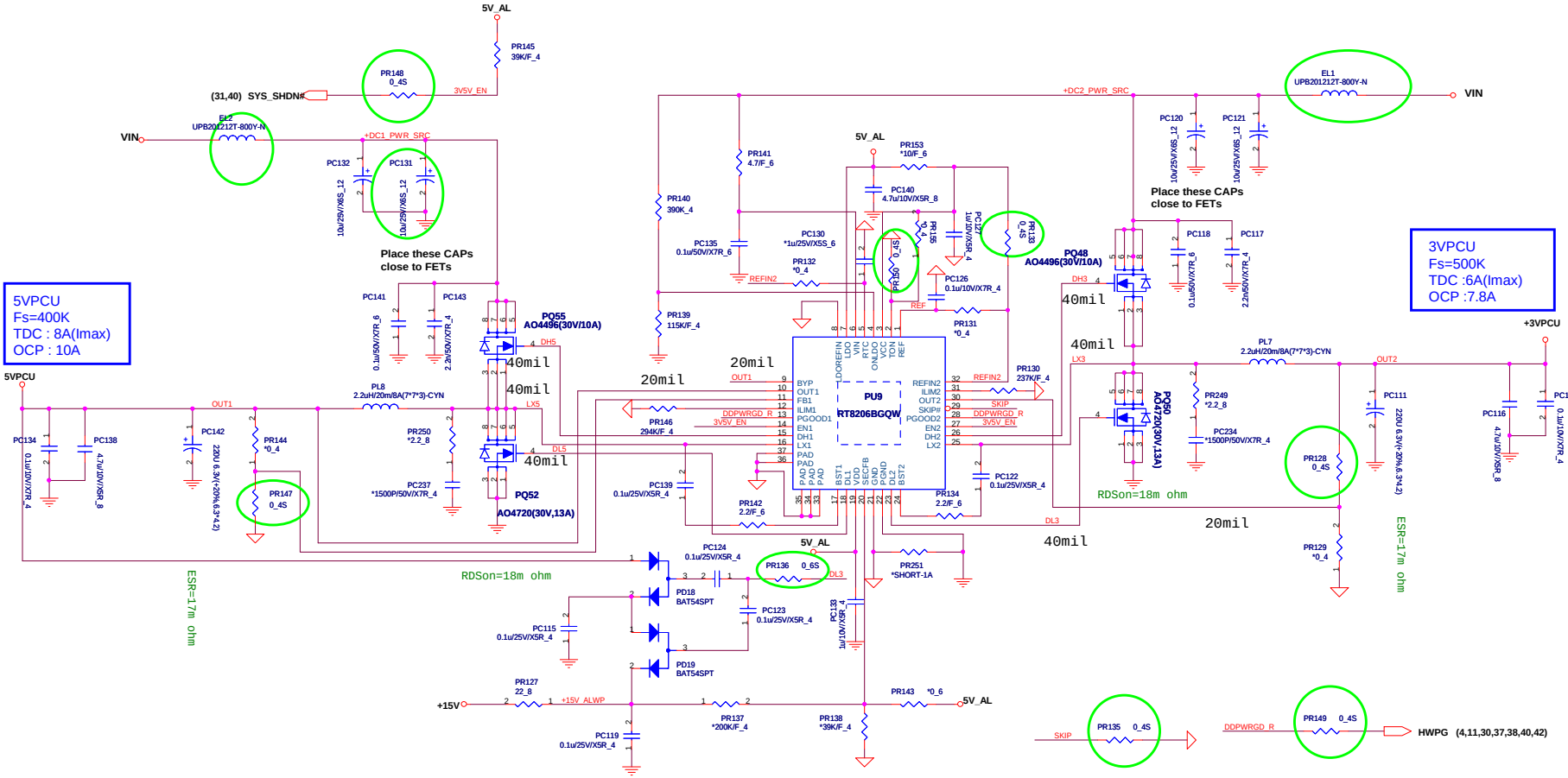
(3,20,36,37,38,40,41,42) VIN
(8,20,23,29,30,32,33,35,36,38,41,42) +3VPCU
(29,35,36,37,38,41,42) 5VPCU
(6,12,35,38,41) +1.8V
(3,4,6,8,9,10,11,12,35,38,40,42) +1.05V_VTT



PROJECT : LL7A
Quanta Computer Inc.

Size	Document Number	Rev
C	3V/5V (RT8206BGQW)	1A
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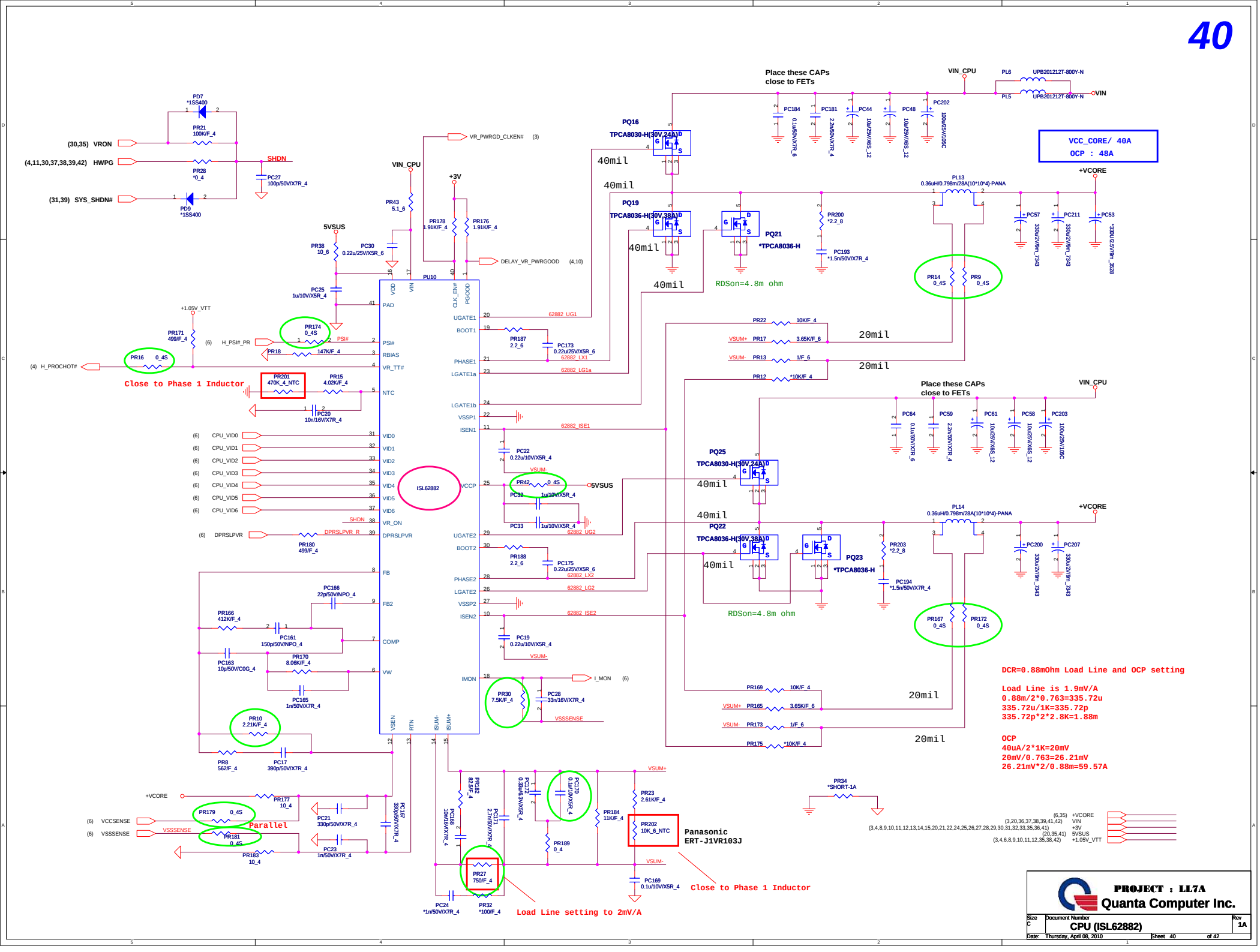

Place these CAPs close to FETs
VIN_CPU
PL6 UPB201212T-800Y-N
PL5 UPB201212T-800Y-N
VIN
PC184 0.1u/50V/X7R_6
PC181 2.2n/50V/X7R_4
PC44 10u/25V/X6S_12
PC48 10u/25V/X6S_12
PC202 100u/25V/105C
VCC_CORE/ 40A
OCP : 48A
PQ16 TPCA8030-H(30V,24A)
PQ19 TPCA8036-H(30V,38A)
PQ21 *TPCA8036-H
PQ25 TPCA8030-H(30V,24A)
PQ22 TPCA8036-H(30V,38A)
PQ23 *TPCA8036-H
40mil
20mil
RDSon=4.8m ohm
PL13 0.36uH/0.798m/28A(10*10*4)-PANA
PL14 0.36uH/0.798m/28A(10*10*4)-PANA
+VCORE
PC57 330u/2V/9m_7343
PC211 330u/2V/9m_7343
PC53 *330U/2.5V/9m_3528
PR14 0_4S
PR9 0_4S
PR200 *2.2_8
PC193 *1.5n/50V/X7R_4
PR22 10K/F_4
PR17 3.65K/F_6
PR13 1/F_6
PR12 *10K/F_4
PC64 0.1u/50V/X7R_6
PC59 2.2n/50V/X7R_4
PC61 10u/25V/X6S_12
PC58 10u/25V/X6S_12
PC203 100u/25V/105C
PC200 330u/2V/9m_7343
PC207 330u/2V/9m_7343
PR203 *2.2_8
PC194 *1.5n/50V/X7R_4
PR167 0_4S
PR172 0_4S
PR169 10K/F_4
PR165 3.65K/F_6
PR173 1/F_6
PR175 *10K/F_4
PD7 *1SS400
PR21 100K/F_4
(30,35) VRON
(4,11,30,37,38,39,42) HWPG
PR28 *0_4
SHDN
PC27 100p/50V/X7R_4
(31,39) SYS_SHDN#
PD9 *1SS400
VR_PWRGD_CLKEN# (3)
VIN_CPU
+3V
PR43 5.1_6
PR178 1.91K/F_4
PR176 1.91K/F_4
DELAY_VR_PWRGOOD (4,10)
5VSUS
PR38 10_6
PC30 0.22u/25V/X5R_6
PC25 1u/10V/X5R_4
PU10
ISL62882
VDD
VIN
CLK_EN#
PGOOD
PAD
PSI#
RBIAS
VR_TT#
NTC
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSLPVR
FB
FB2
COMP
VW
VSEN
RTN
ISUM-
ISUM+
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
+1.05V_VTT
PR171 499/F_4
(6) H_PSI#_PR
PR174 0_4S
PR18 147K/F_4
(4) H_PROCHOT#
PR16 0_4S
Close to Phase 1 Inductor
PR201 470K_4_NTC
PR15 4.02K/F_4
PC20 10n/16V/X7R_4
(6) CPU_VID0
(6) CPU_VID1
(6) CPU_VID2
(6) CPU_VID3
(6) CPU_VID4
(6) CPU_VID5
(6) CPU_VID6
(6) DPRSLPVR
PR180 499/F_4
PC166 22p/50V/NPO_4
PR166 412K/F_4
PC161 150p/50V/NPO_4
PC163 10p/50V/C0G_4
PR170 8.06K/F_4
PC165 1n/50V/X7R_4
PR10 2.21K/F_4
PR8 562/F_4
PC17 390p/50V/X7R_4
62882_UG1
PR187 2.2_6
PC173 0.22u/25V/X5R_6
62882_LX1
62882_LG1a
62882_ISE1
PC22 0.22u/10V/X5R_4
VSUM-
PR42 0_4S
5VSUS
PC32 1u/10V/X5R_4
PC33 1u/10V/X5R_4
62882_UG2
PR188 2.2_6
PC175 0.22u/25V/X5R_6
62882_LX2
62882_LG2
62882_ISE2
PC19 0.22u/10V/X5R_4
I_MON (6)
PR30 7.5K/F_4
PC28 33n/16V/X7R_4
VSSSENSE
+VCORE
PR177 10_4
PR179 0_4S
(6) VCCSENSE
(6) VSSSENSE
Parallel
PR181 0_4S
PR183 10_4
PC21 330p/50V/X7R_4
PC23 1n/50V/X7R_4
PC167 330p/50V/X7R_4
PR182 82.5/F_4
PC168 10n/16V/X7R_4
PC171 2.7n/50V/X7R_4
PC172 0.33u/6.3V/X5R_4
PC170 0.1u/10V/X5R_4
PR184 11K/F_4
PR189 0_4
PR23 2.61K/F_4
PR202 10K_6_NTC
Panasonic ERT-J1VR103J
PR27 750/F_4
PC24 *1n/50V/X7R_4
PR32 *100/F_4
Load Line setting to 2mV/A
PC169 0.1u/10V/X5R_4
Close to Phase 1 Inductor
PR34 *SHORT-1A
(6,35) +VCORE
(3,20,36,37,38,39,41,42) VIN
(3,4,8,9,10,11,12,13,14,15,20,21,22,24,25,26,27,28,29,30,31,32,33,35,36,41) +3V
(20,35,41) 5VSUS
(3,4,6,8,9,10,11,12,35,38,42) +1.05V_VTT
DCR=0.88mOhm Load Line and OCP setting
Load Line is 1.9mV/A
0.88m/2*0.763=335.72u
335.72u/1K=335.72p
335.72p*2*2.8K=1.88m
OCP
40uA/2*1K=20mV
20mV/0.763=26.21mV
26.21mV*2/0.88m=59.57A
PROJECT : LL7A
Quanta Computer Inc.
Size C
Document Number CPU (ISL62882)
Rev 1A
Date: Thursday, April 08, 2010
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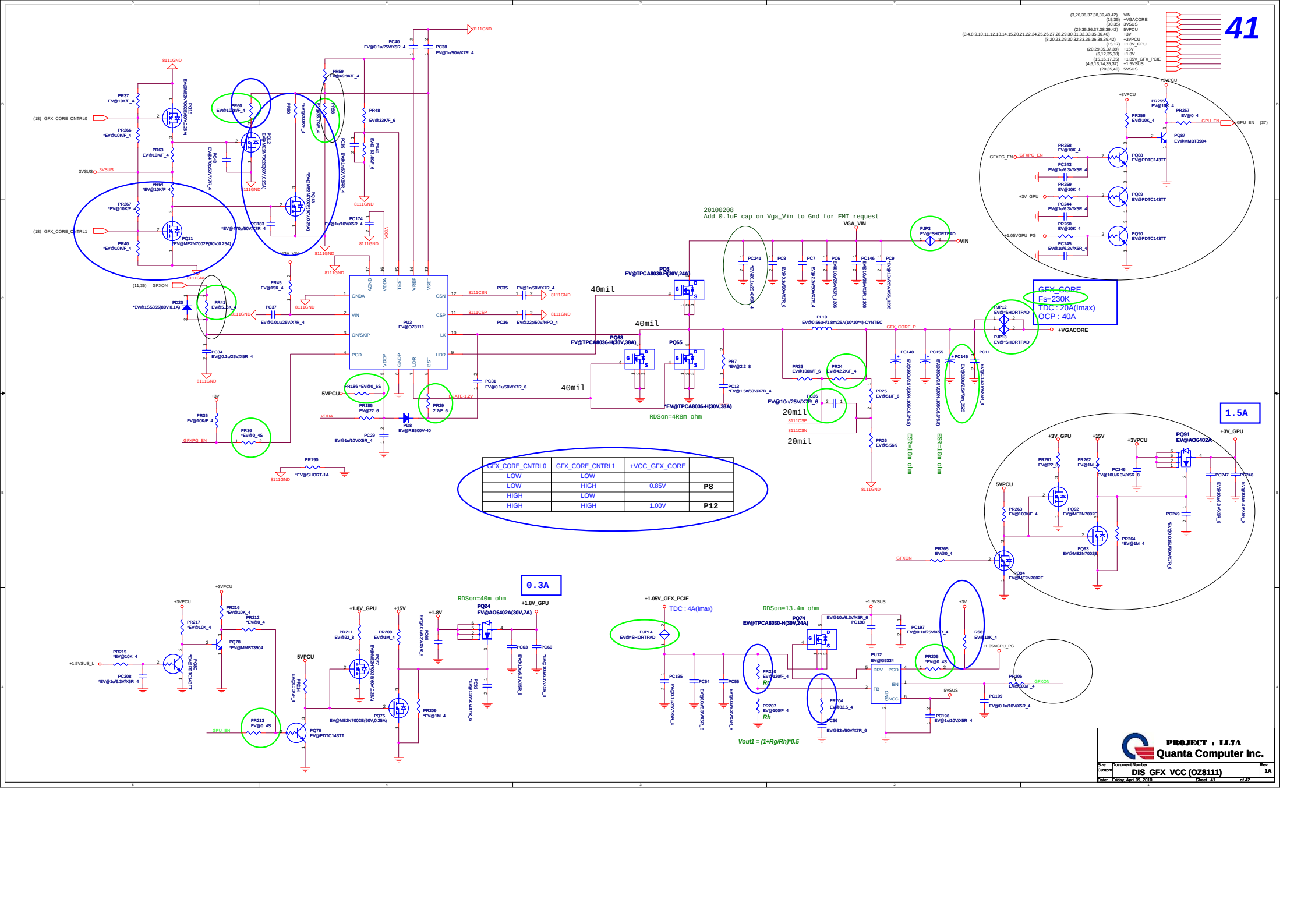
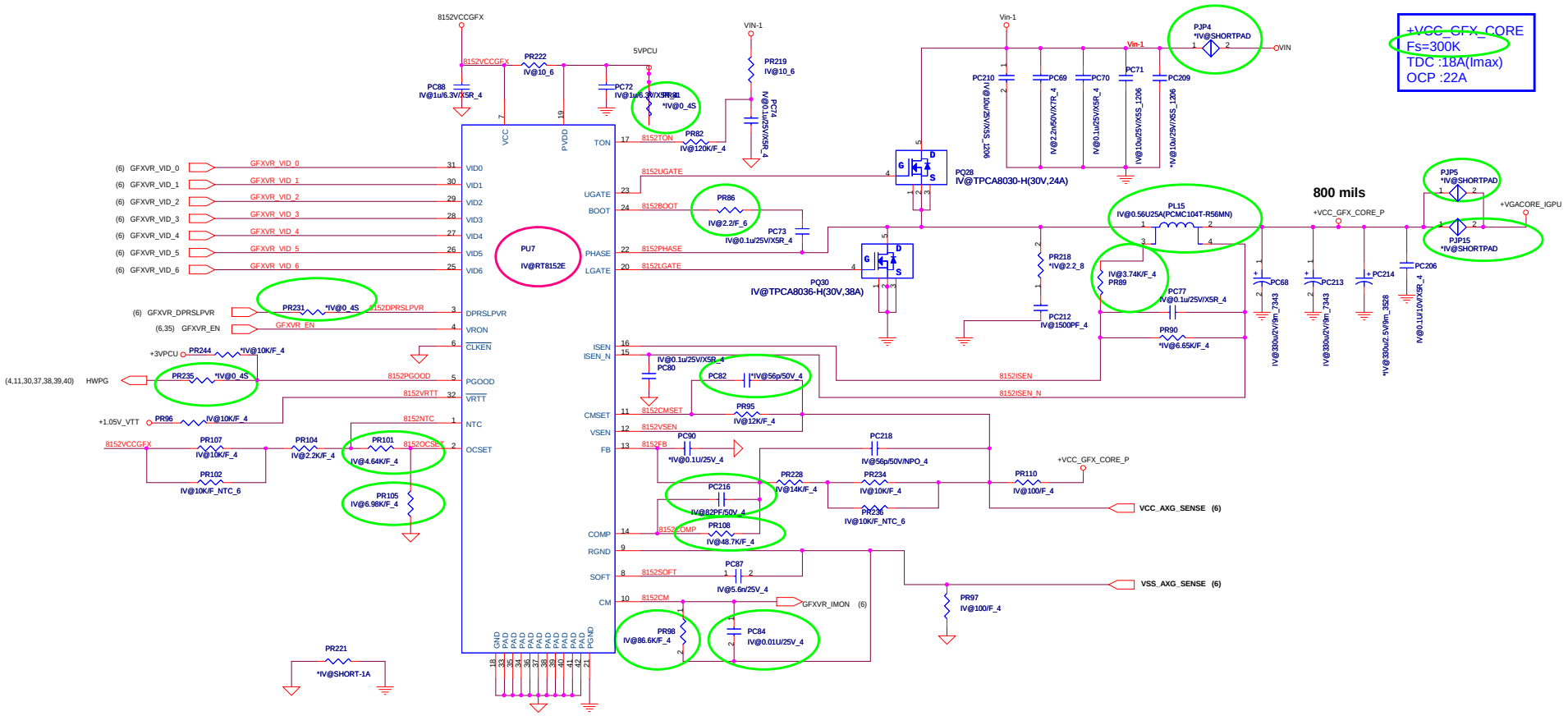


GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE	
LOW	LOW		
LOW	HIGH	0.85V	P8
HIGH	LOW		
HIGH	HIGH	1.00V	P12



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Quanta Computer Inc.			
Size: C	Document Number: GFX_VCC (RT8152C)		Rev: 1A
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