KL6A Intel Huron River Platform with Discrete GFX

01

FAN / THERMAL
EMC2103-2

DDRIII-SODIMM1
PG 13

DDRIII-SODIMM2
PG 14

Dual Channel DDR3
1333/1600 1.5V

DDR SYSTEM MEMORY

<MCH Process>
SandyBridge 0.61

rPGA 988

PCI-E

PG 3,4,5,6

FDI DMI

Graphics Interfaces

PCI-Express

Nvidia
N12P-GE
N12P-GV1 973p
N12P-GV

PG 15,16,17,18,19,20,21

27MHz

DMIX4

REGULATOR (DDR3)
1.5VSUS, 0.75VSMDDR_VTERM,1.5V
1.5V_GPU,1.5V_CPU

REGULATOR
+1.05V_VTT,+1.8V

DC/DC
3VPCU, 5VPCU, +15V
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CPU Core
PG 43

VGA Core Discrete
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PG 27
SATA1 150MB

SATA - CD-ROM
PG 27
SATA3 150MB

USB+eSATA
PG 27
SATA4 150MB

FDI DMI

CougarPoint 0.7
PCH

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HDMI CON
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INT_CRT
CRT
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ALC269
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IHDA

A-MIC
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PCI-E

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(WLAN)
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X1
LAN
Realtek
(10/100/1G LAN)
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RTL8105E
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25MHz

32.768KHz

LPC

EC
IT8518
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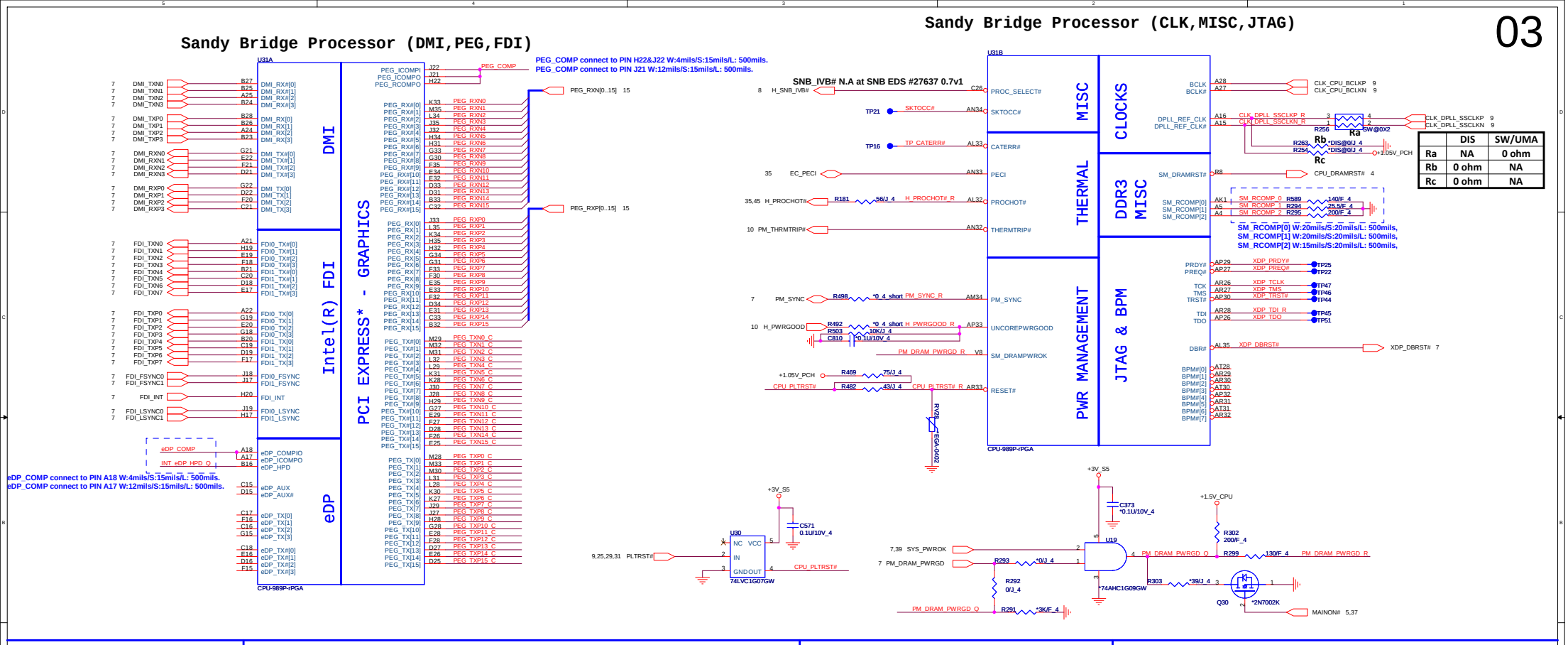
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,30,31,32,33,34,35	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	11,12,38	RTC		S0~S5
3VPCU	+3.3V	11,15,18,25,26,28,30,31,34,36	ITE8052 POWER	3V5V_EN	S0~S5
5VPCU	+5V	11,30,31,32,33,34,36	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,30,32,34	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	18,30	LAN POWER	LAN_ON	
5V_S5	+5V	12,20,30	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	8,11,12,21,22,30	Sys Management,PCH Resume Well,Intel HD Audio,USB,WLAN WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	26,30,35,36	SLP_S4# CTRLD POWER	SUSON	S0~S3
+VCC_GFX_CORE	+0.9V~+1.2V	6,36	VGA CORE POWER	MAIN_ON	S0
0.9VSMDDR_VTERM	+0.75V	5,14,32	DDR2 SODIMM REFERENCE POWER	MAIN_ON	S0
+5V	+5V	12,15,16,17,19,25,27,28,30	SLP_S3# CTRLD POWER	MAIN_ON	S0
+3V	+3.3V	3,4,6,9,10,11,12,14,15,16,17,18,19,21,22,23,24,26,28,30,32,33,34,35	SLP_S3# CTRLD POWER	MAIN_ON	S0
+1.8V	+1.8V	6,21,32	LVDS,NVM POWER	MAIN_ON	S0
+1.5V	+1.5V	6,8,12,17,22,23,36	Mini PCIe,Express Card POWER	MAIN_ON	S0
+1.05V	+1.05V	3,4,6,9,12,30,33	PCH CORE POWER	MAIN_ON	S0
VCC_CORE		6,30,35	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	L_VDD_EN	S0
BAT-V	+10V~+17V	31	MAIN BATTERY	CHG_PBATT	S0~S5

Sandy Bridge Processor (DMI,PEG,FDI)

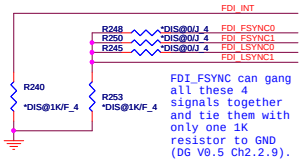
Sandy Bridge Processor (CLK,MISC,JTAG)

03

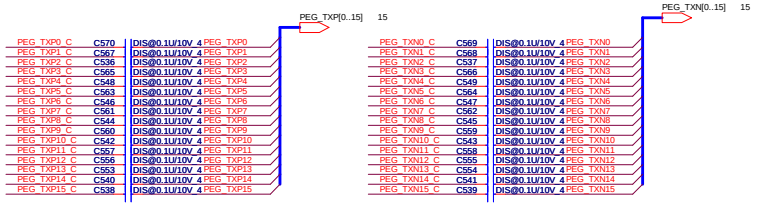


	DIS	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

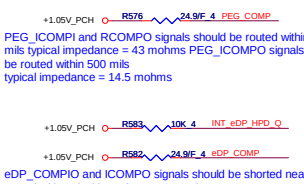
FDI Disable



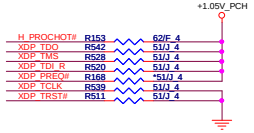
PEG x16 (UMA Non-stuff)



DP & PEG Compensation



Processor pull-up(CPU)



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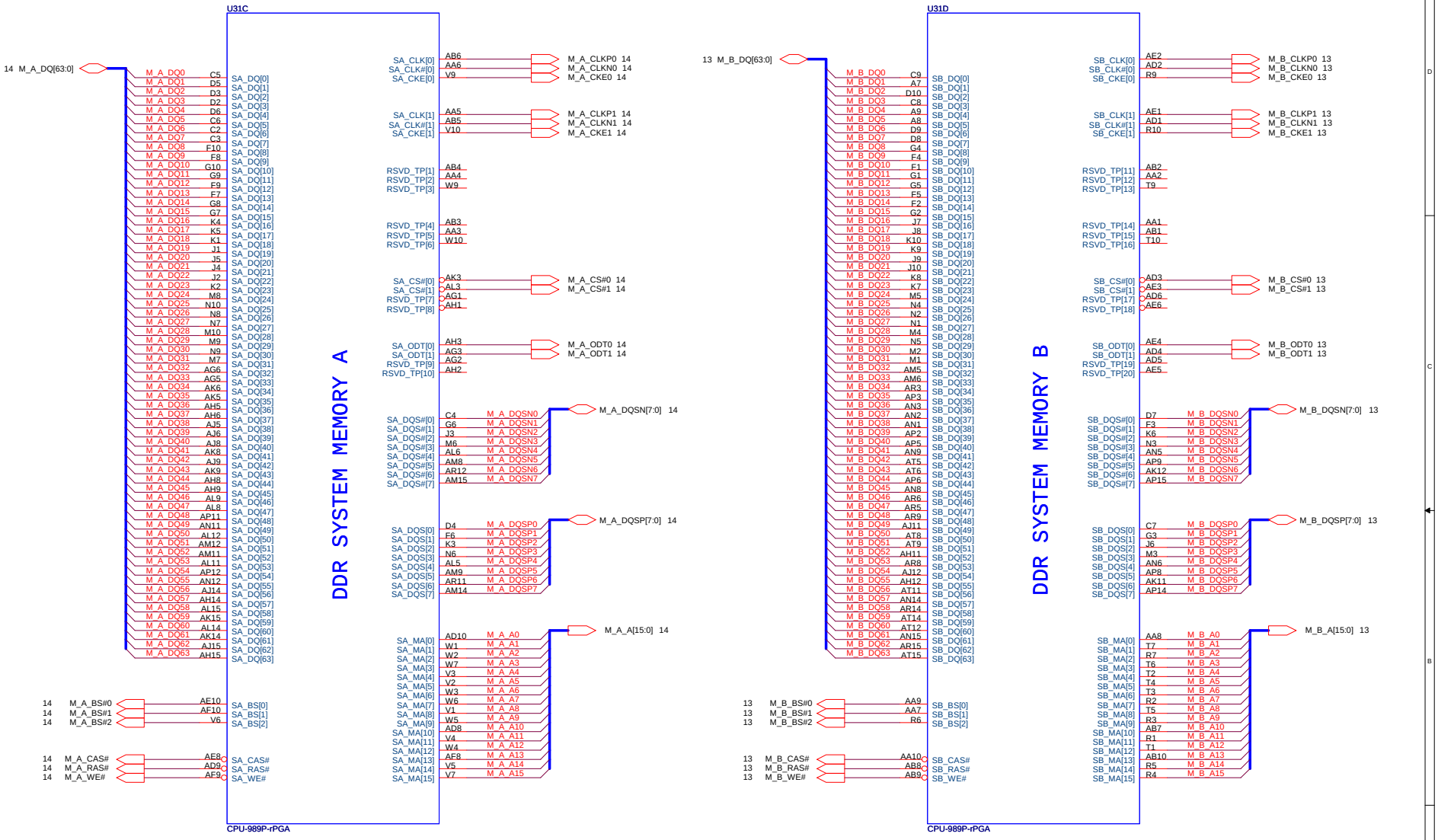
Sandy Bridge Processor (DDR3)



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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

22uF (Reserved)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

22uF (Reserved)

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

Reserved

Ra	DIS	SW
Ra	0 ohm	NA

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
R169 54.9/F_4
Place PU resistor close to CPU
R171 130/F_4

SVID DATA
Close to VR
R161 130/F_4
Place PU resistor close to CPU
R160 75/J_4

SVID ALERT

4.5A
Q31 AO4496
Q92 DMN601K-7
3/26 DB add for Intel. Placement close to CPU.

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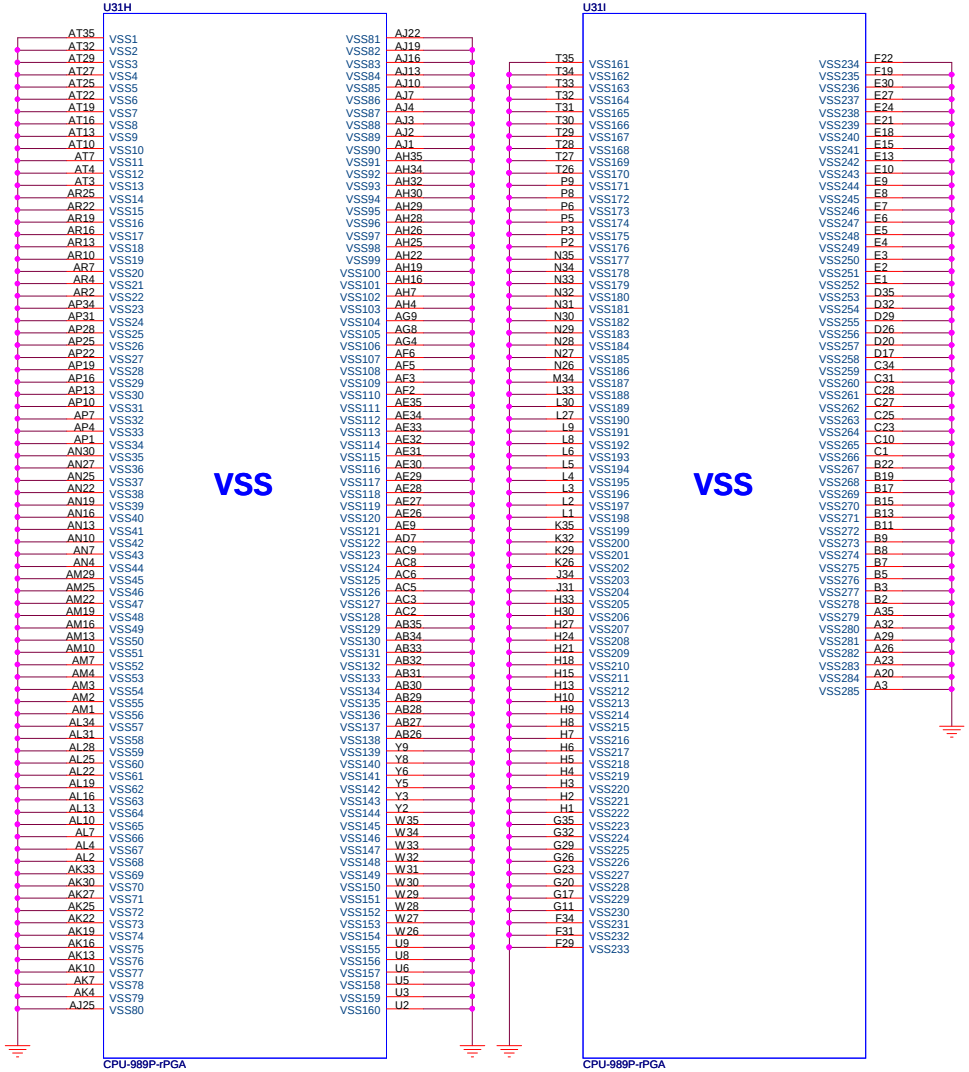
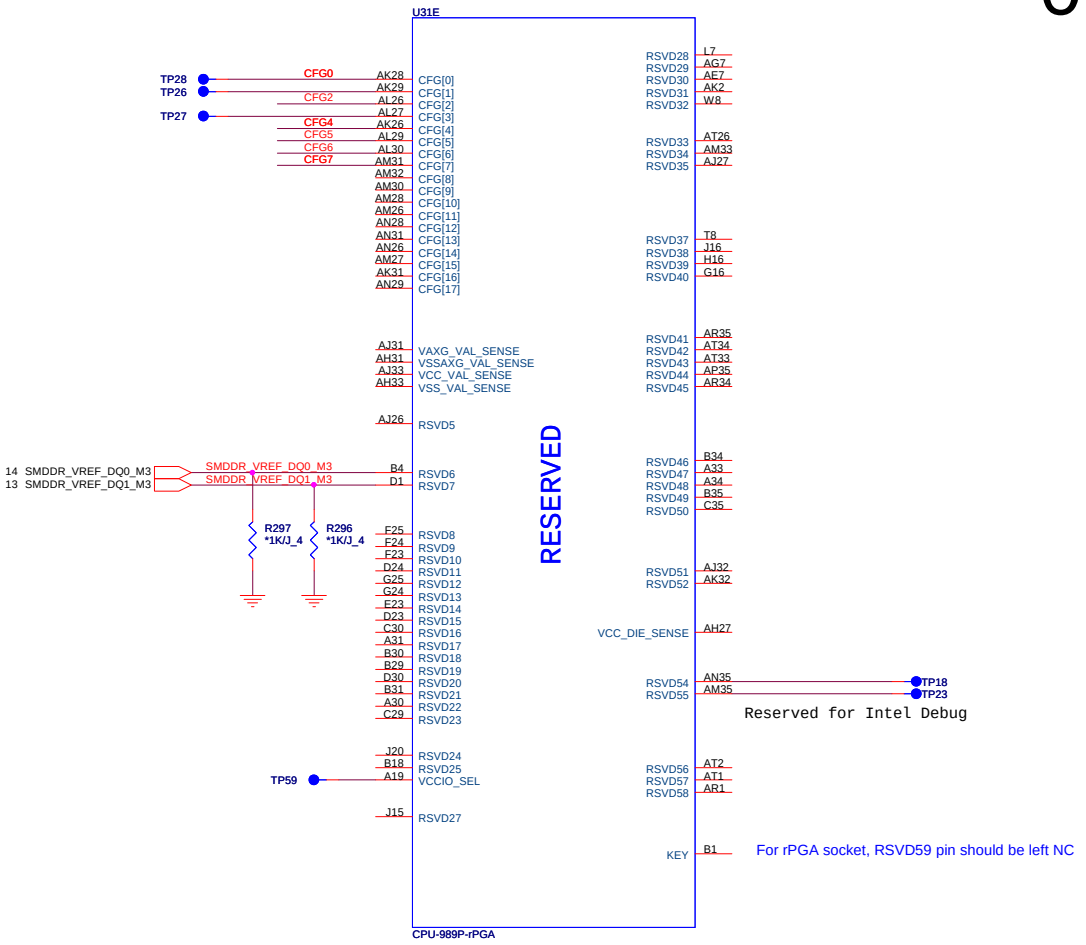
Sandy Bridge Processor (GND)



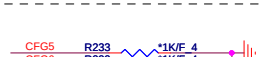
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

For rPGA socket, RSVD59 pin should be left NC

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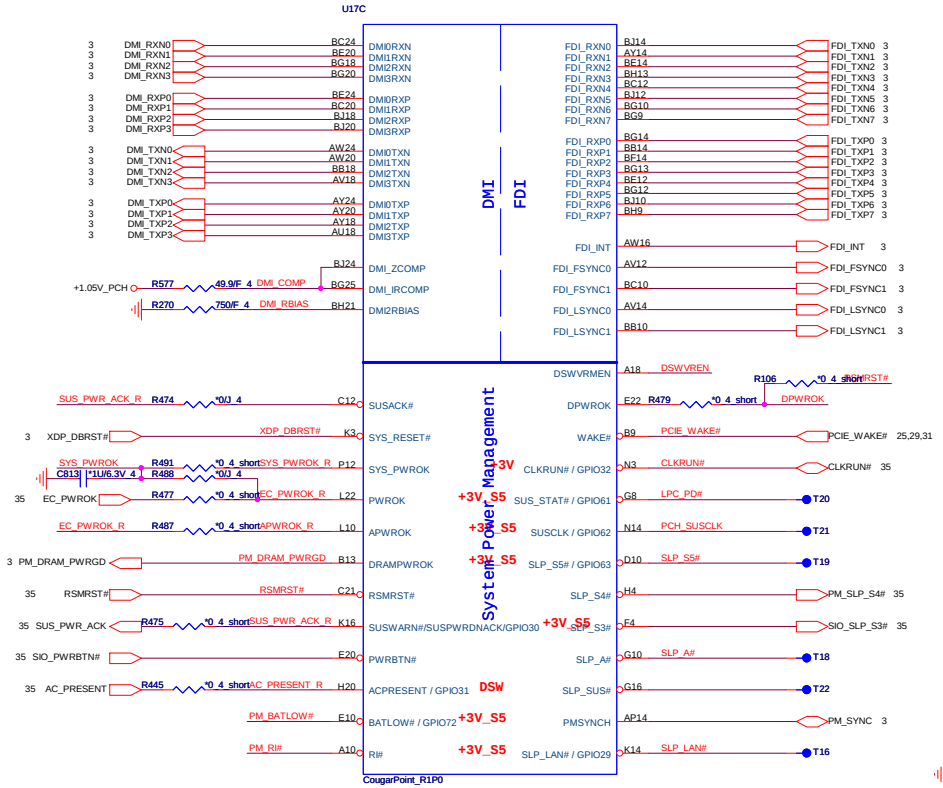
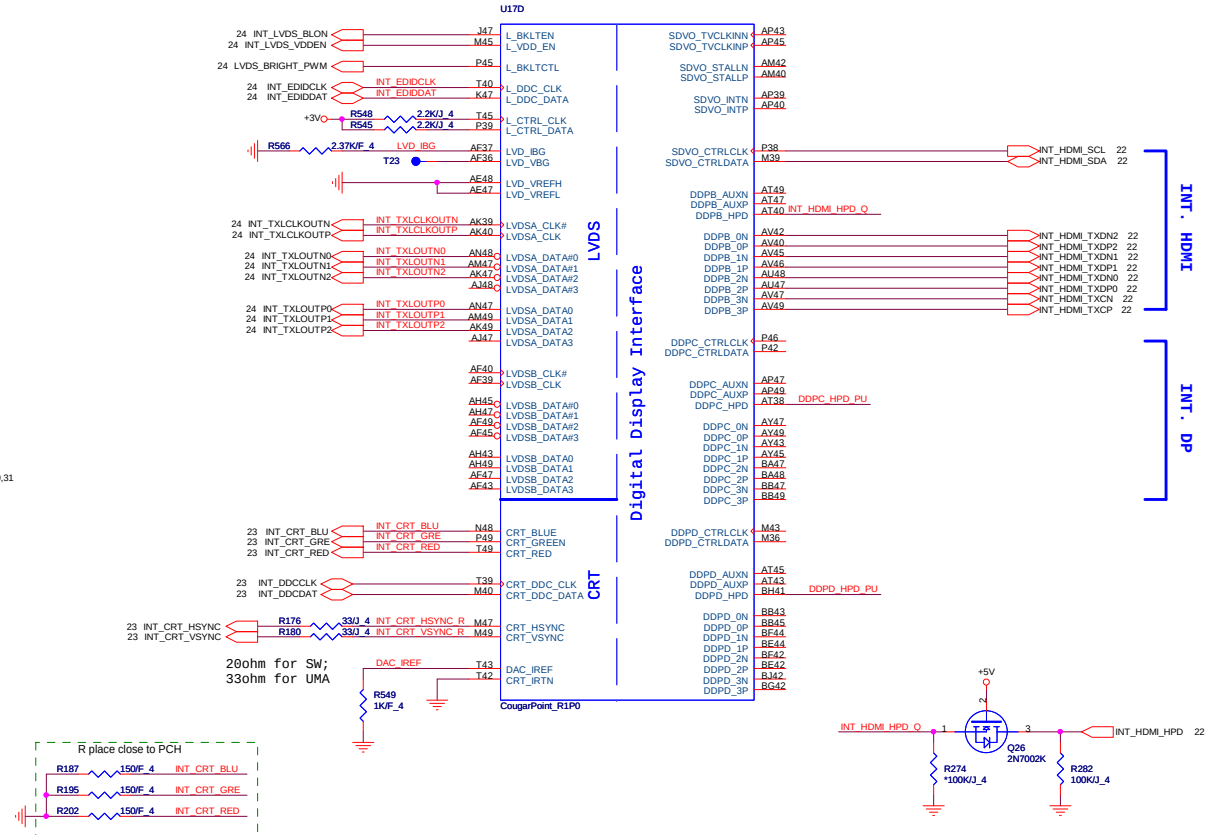
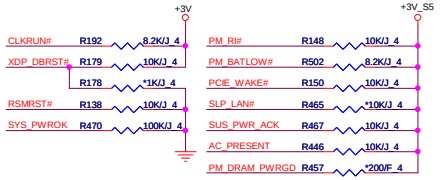
Cougar Point (DMI,FDI,PM)



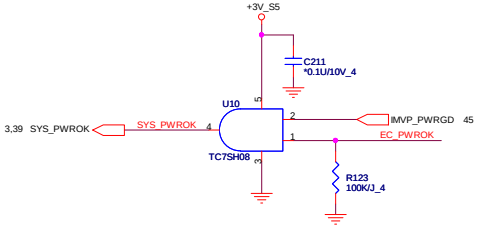
Cougar Point (LVDS,DDI)

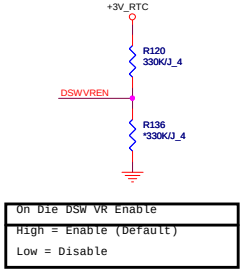


PCH Pull-high/low(CLG)

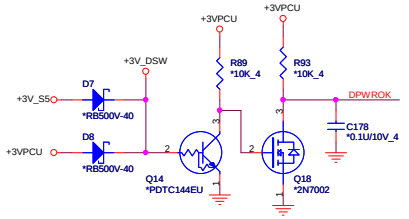


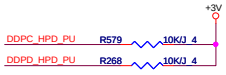
System PWR_OK(CLG)





DPWROK FOR DSW





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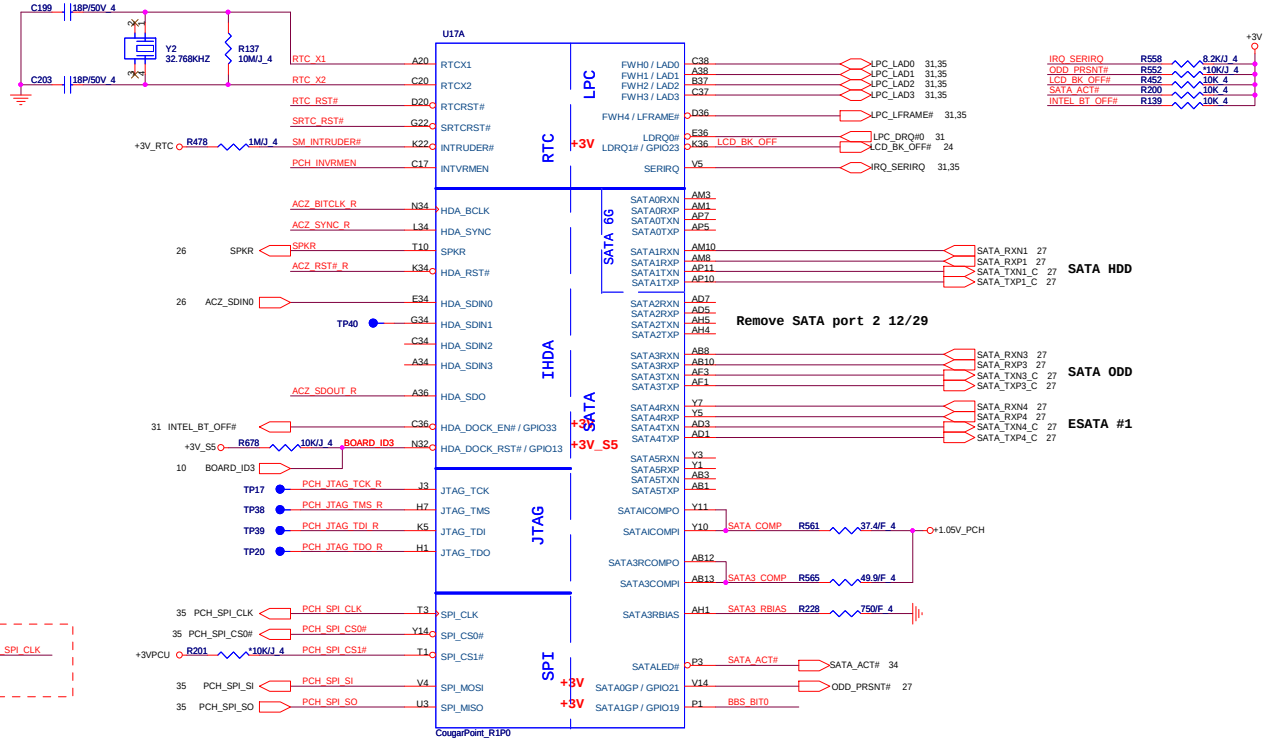
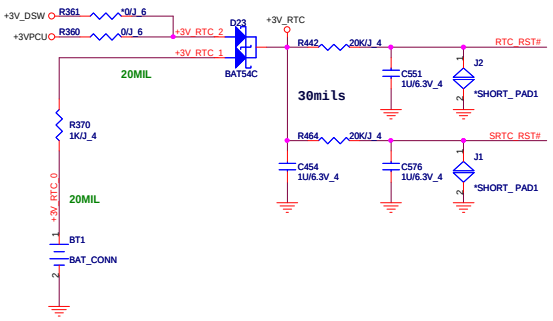
PCH2(CLG)

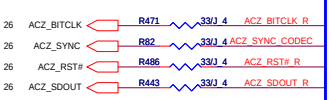
Cougar Point (HDA,JTAG,SATA)



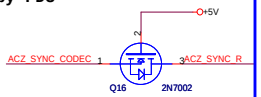
RTC Circuitry(RTC)



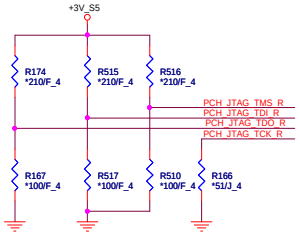
HDA Bus(CLG)



To Separate Codec Sync by PD3



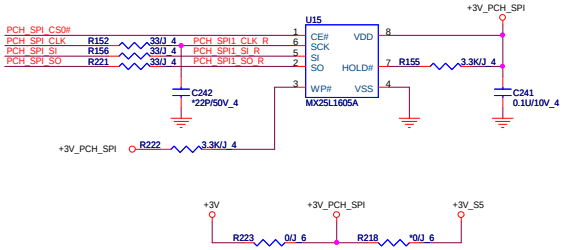
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

32Mbit (4M Byte), SPI

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



*10P/50V/COG_4 SC807 PCH_SPI_CLK

RF request

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R557 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R521 *1K/J_4 PCI_GNT3# 9
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R121 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI *; 0 0 LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R504 *1K/J_4 BBS_BIT1 9 R193 *1K/J_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R463 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R265 2.2K/J_4 +1.8V R266 4.7K/J_4 DF_TVS 10 H_SNB_IVB# 3
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R522 *1K/J_4 PLL_ODVR_EN 10
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R81 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R146 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

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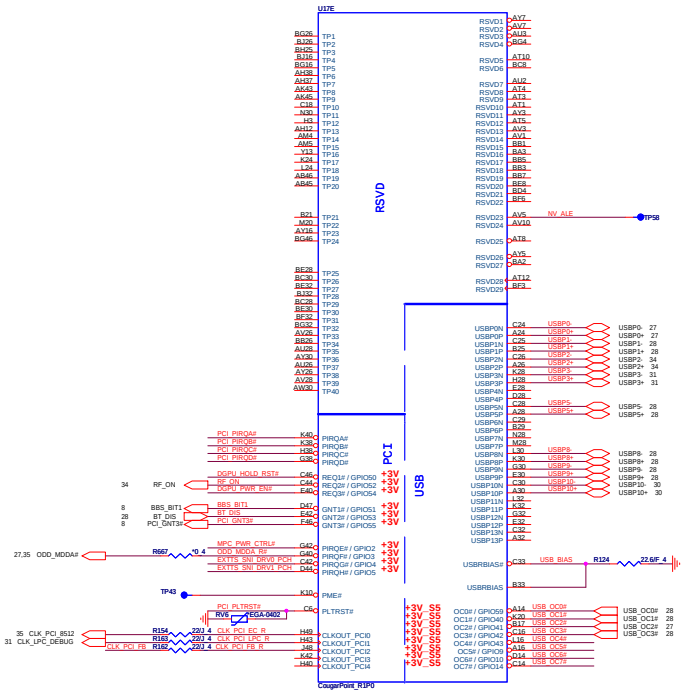
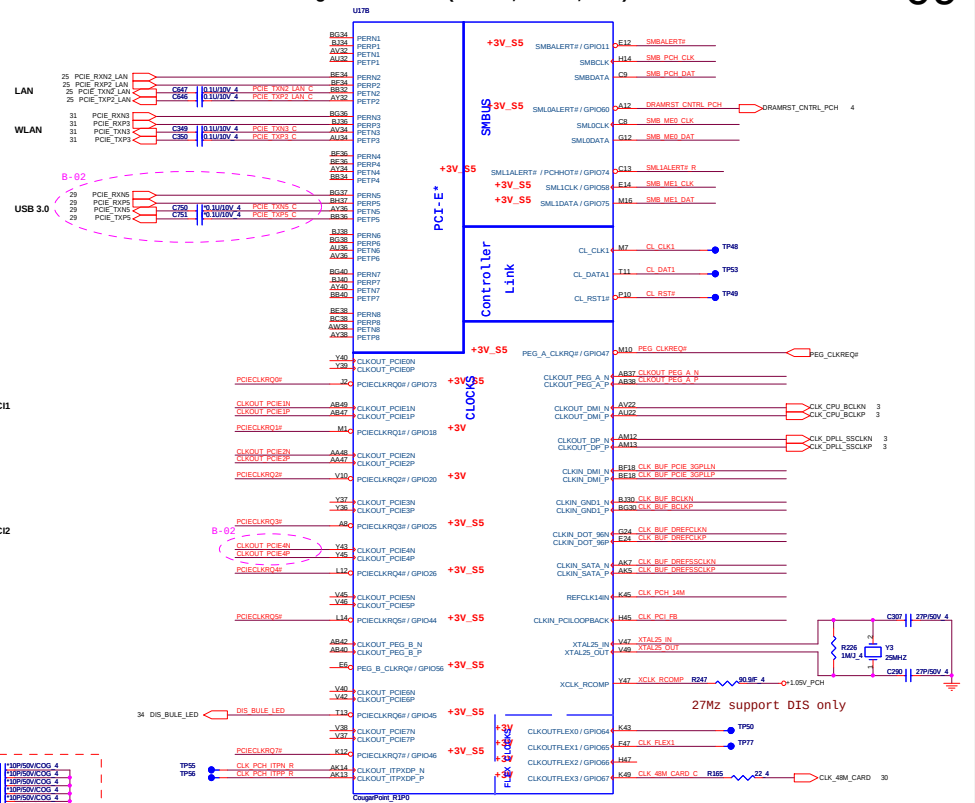
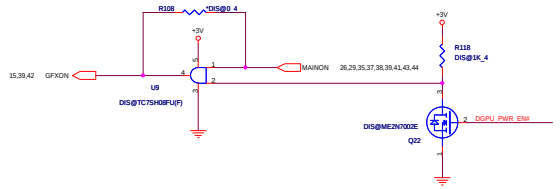
Cougar Point-M (PCI,USB,NVRAM)



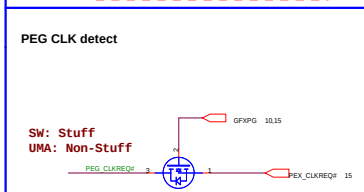
Cougar Point-M (PCI-E,SMBUS,CLK)



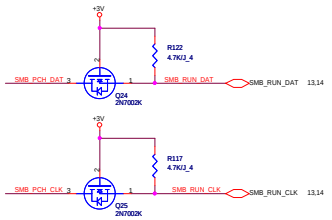
DGPU Power ON



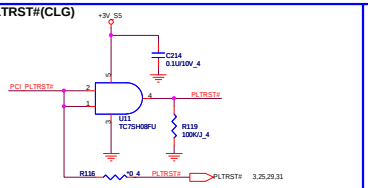
PEG CLK detect



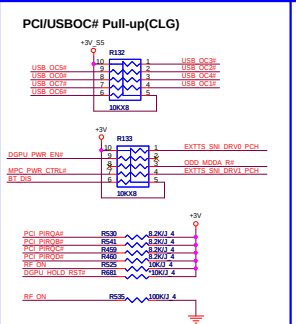
SMBus(CLK)



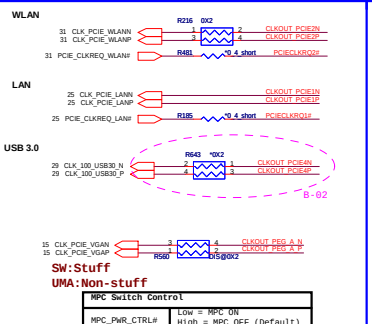
PLTRST#(CLG)



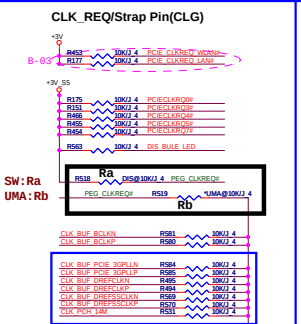
PCI/USBOC# Pull-up(CLG)



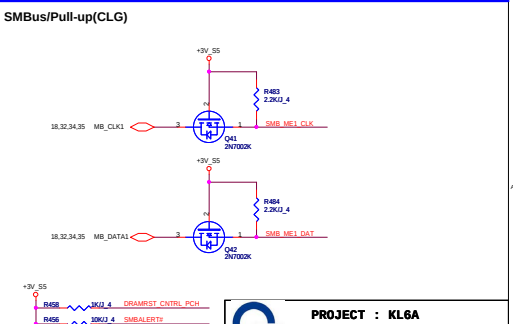
WLAN / LAN / USB 3.0



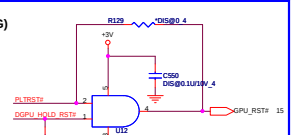
CLK_REQ/Strap Pin(CLG)



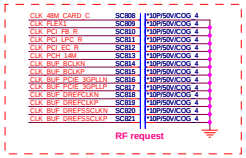
SMBus/Pull-up(CLG)



GPU RST#(CLG)



RF request



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Cougar Point (GPIO,VSS_NCTF,RSVD)

U17F

GPIO

S_GPIO R546 100_4	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40 CPU_ID
29,35 EC_EXT_SMI#	A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41 R126 1.5K/F_4
BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41 COLOR_ENGINE_DET
35 EC_EXT_SCI#	E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40 BOARD_ID2
TP76 ICC_EN#	C10	GPIO8	+3V_S5			
31 LAN_DISABLE#	C4	LAN_PHY_PWR_CTRL / GPIO12		+3V_S5		
HOST_ALERT#1_R	G2	GPIO15	+3V_S5			
BOARD_ID0	U2	SATA4GP / GPIO16	+3V			
GFXPG_R	D40	TACH0 / GPIO17	+3V			
BIOS_REC	T5	SCLOCK / GPIO22	+3V			
USB30_ID	E8	GPIO24 / MEM_LED	+3V_S5			
GPIO27	E16	GPIO27	DSW			
8 PLL_ODVR_EN	P8	GPIO28	+3V_S5			
SYSTEM_ID	K1	STP_PCI# / GPIO34	+3V			
28 BT_ON#	K4	GPIO35	+3V			
TP54 DMI_OVRVLTG	V8	SATA2GP / GPIO36	+3V			
FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V			
MFG_MODE	N2	SLOAD / GPIO38	+3V			
DGPU_PRSNT#	M3	SDATAOUT0 / GPIO39	+3V			
TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V			
32,35 TEMP_ALERT#	V3	SATA5GP / GPIO49	+3V			
SV_DET	D6	GPIO57	+3V_S5			

CPU/MISC

A20GATE	P4	EC_A20GATE 35	
PECI	AU16	TP57	
RCIN#	P5	EC_RCIN#	EC_RCIN# 35
PROCPWRGD	AY11		H_PWRGOOD 3
THRMTRIP#	AY10	PCH_THRMTRIP# R578 390/J_4	PM_THRMTRIP# 3
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS 8
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

R114 *DIS@0_4 +3V

GFXPG_R → GFXPG_R 4 → U8 (1 → HWPG 35,39,40,41,43,44,45; 2 → GFXPG 9,15; 5 → +3V)

DIS@TC7SH08FU(F)

SGPIO

S_GPIO R551 10K/J_4 R550 *0/J_4 +3V

GPIO Pull-up/Pull-down(CLG)

+3V_S5

LAN_DISABLE#	R164	10K/J_4

+3V

COLOR_ENGINE_DET	R644	10K_4
EC_EXT_SMI#	R127	10K/J_4
EC_EXT_SCI#	R461	10K/J_4
EC_A20GATE	R543	10K/J_4
EC_RCIN#	R556	10K/J_4
TEMP_ALERT#	R211	10K/J_4
BT_ON#	R507	10K/J_4
GPIO27	R490	10K/J_4
GFXPG_R	R113	DIS@10K/J_4

Board ID

B-04

Board ID For Function	SYSTEM_ID GPIO34	ID2 GPIO71	ID3 GPIO13	ID1 GPIO6	ID0 GPIO16	CPU_ID GPIO68
SDV	1	1	0	0	0	1
SIV	1	1	0	0	1	1
SIT	1	1	0	1	0	1
SVT	1	1	0	1	1	1
SOVP	1	1	1	0	0	1

Board ID use below GPIO:
BOARD_ID0
BOARD_ID1
BOARD_ID3

ID2: 0-->6 layer
1-->8 layer

System ID: 0-->KL5
1-->KL6

CPU_ID: 0-->35W
1-->45W

+3V

R675	*10K/J_4	CPU_ID	R676	10K/J_4	
R207	10K/J_4	BOARD_ID0	R199	*10K/J_4	
R462	*10K/J_4	BOARD_ID1	R444	10K/J_4	
R140	10K/J_4	BOARD_ID2	R125	*10K/J_4	
R147	*10K/J_4	SYSTEM_ID	R142	10K/J_4	

+3V_S5

R682	10K/J_4	BOARD_ID3	R683	*10K/J_4	BOARD_ID3 8

SV_SET_UP
High = Strong (Default)

TEST_SET_UP R559 10K/J_4 R555 *0/J_4 +3V

USB30_ID	GPIO24
USB3.0	0
Non-USB3.0	1

+3V_S5 R679 *10K/J_4 USB30_ID R680 10K/J_4

+3V R509 *10K/J_4 SV_DET R501 100K/J_4

HOST_ALERT#1_R R508 1K/J_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

+3V R533 *10K/J_4 DGPU_PRSNT# R532 DIS@100K/J_4

R526 100K/J_4 FDI_OVRVLTG R527 *1K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R668 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R547 10K/J_4 R554 *0/J_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

MFG_MODE R184 10K/J_4 R194 *0/J_4 +3V

PROJECT : KL6A

Quanta Computer Inc.

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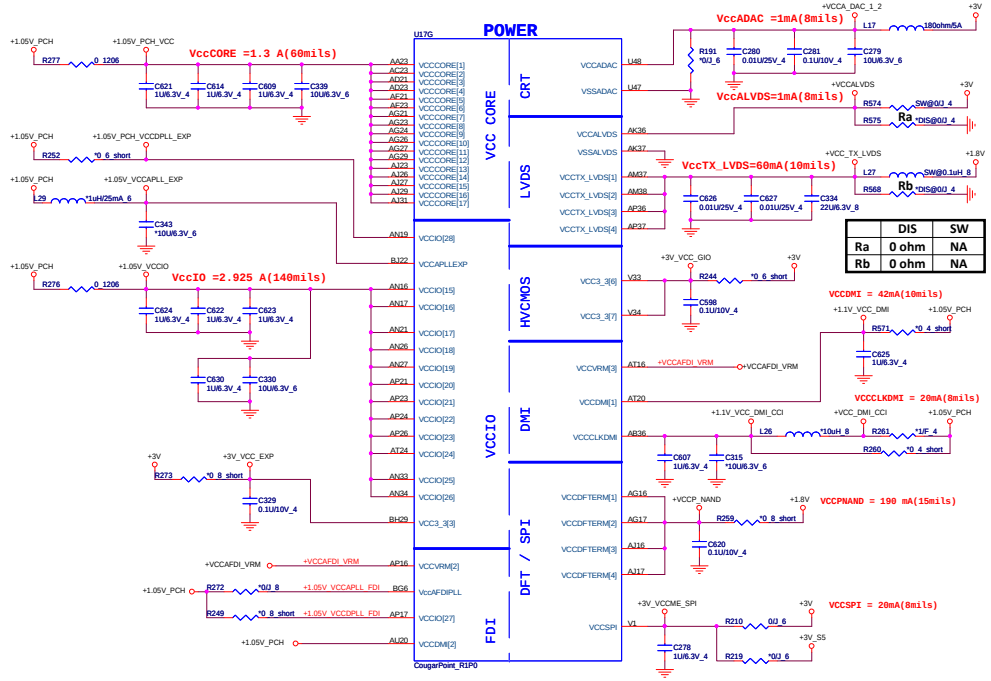
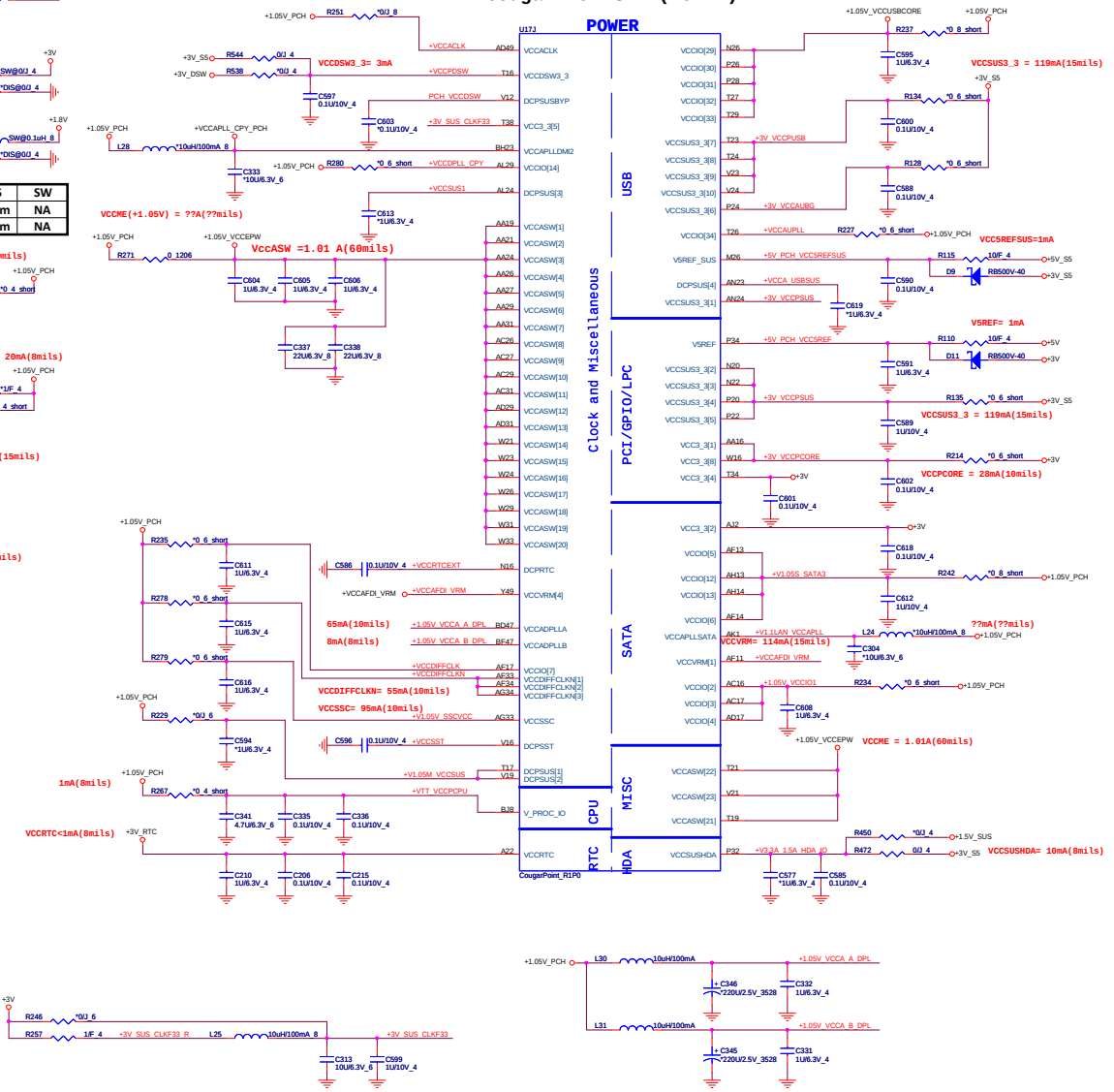
	Cougar Point 4/6	1A
Date: Friday, October 29, 2010	Sheet 10 of 47	

COUGAR POINT (POWER)



Cougar Point-M (POWER)



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 5/6	1A

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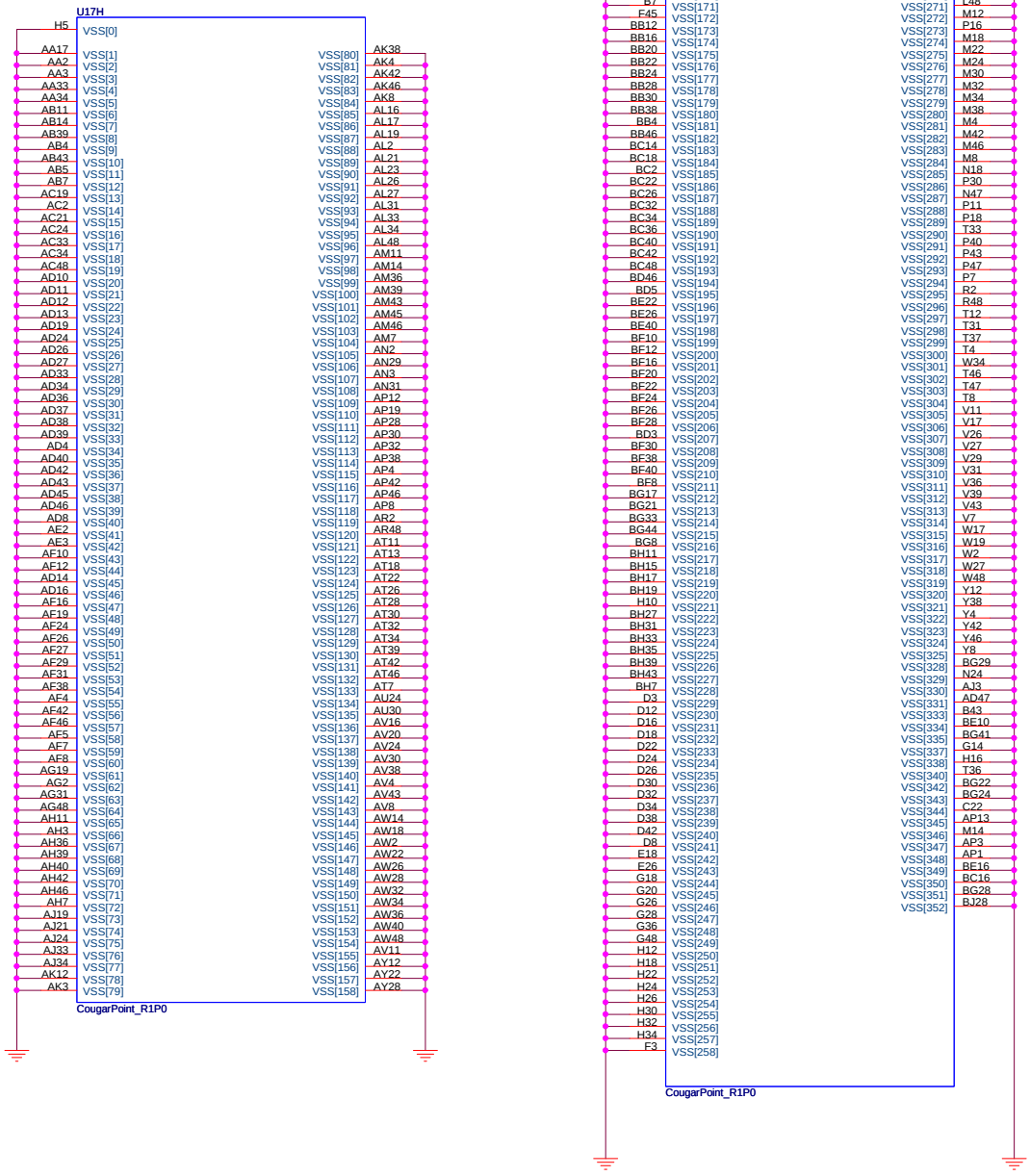
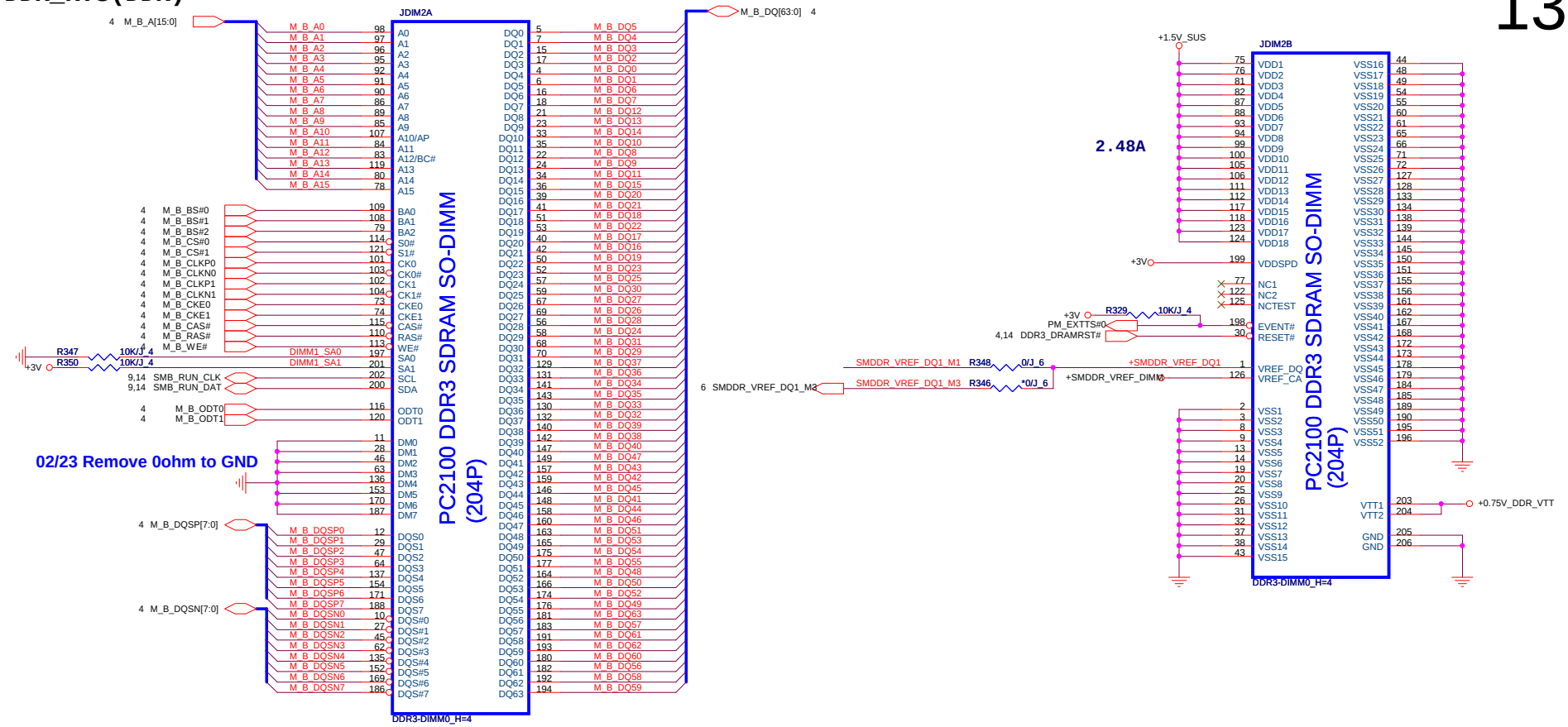
IBEX PEAK-M (GND)

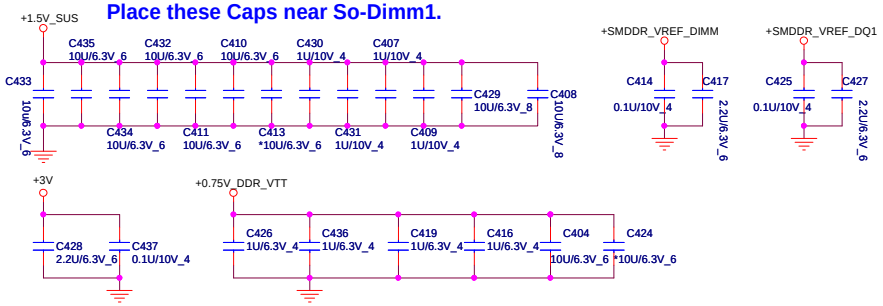


PROJECT : KL6A		
Quanta Computer Inc.		
Size	Document Number: Cougar Point 6/6	Rev: 1A
Date: Friday, October 29, 2010	Sheet 12 of 47	

DDR_RVS(DDR)

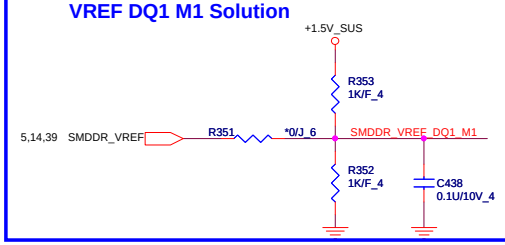


Place these Caps near So-Dimm1.



VREF DQ1 M2 Solution

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A

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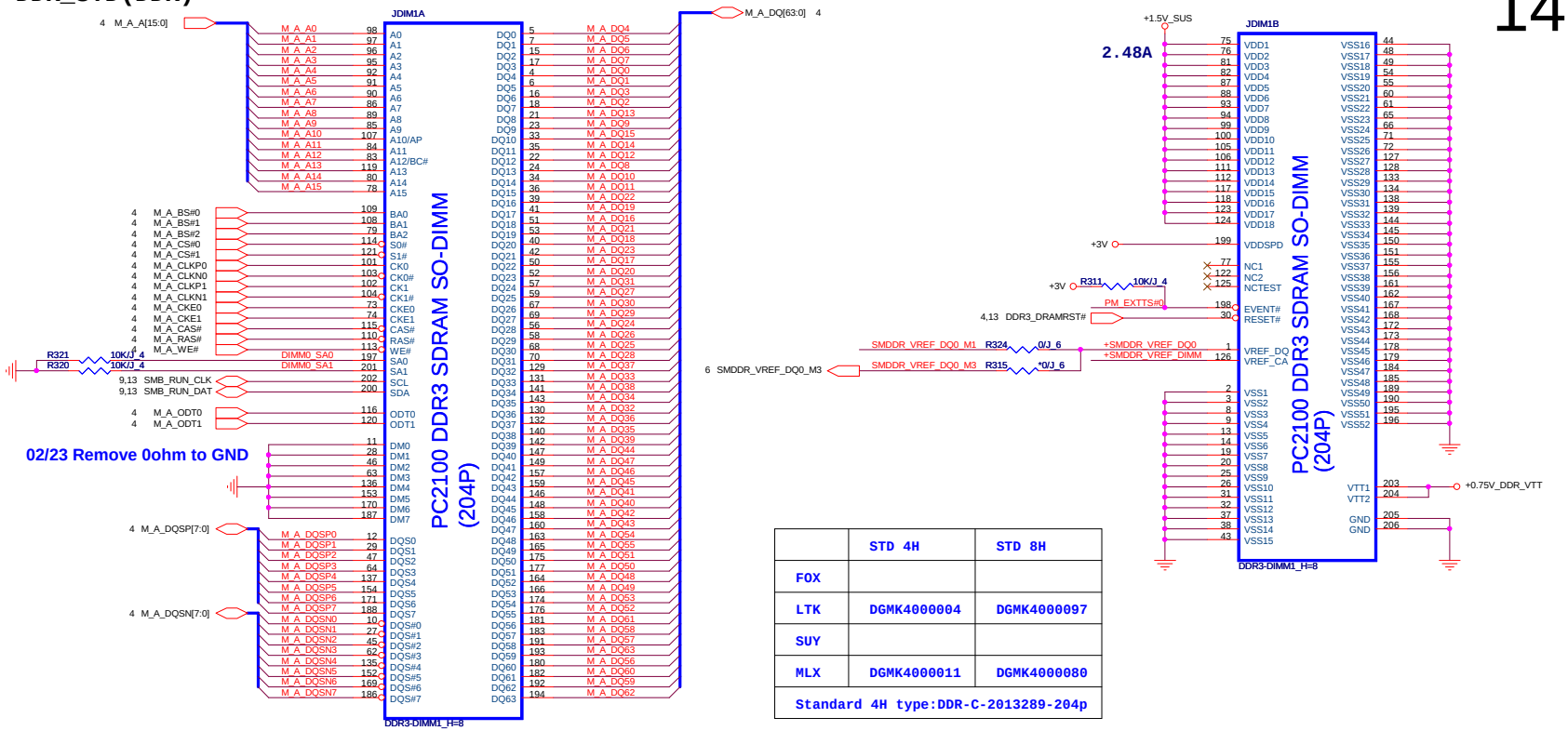
DDR_STD(DDR)

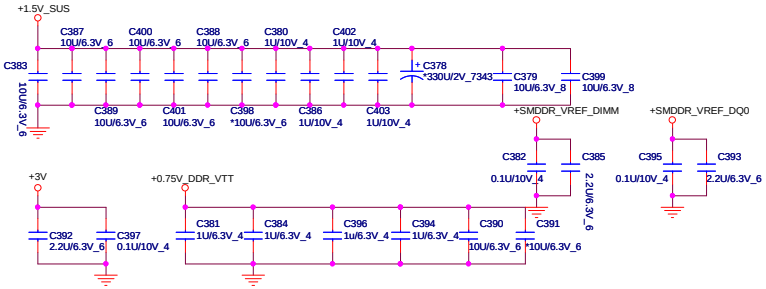


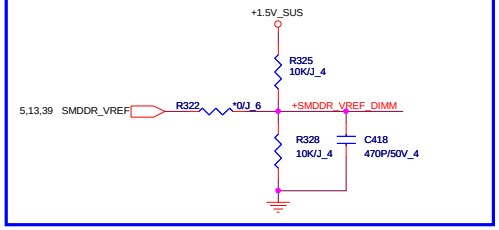
02/23 Remove 0ohm to GND

	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

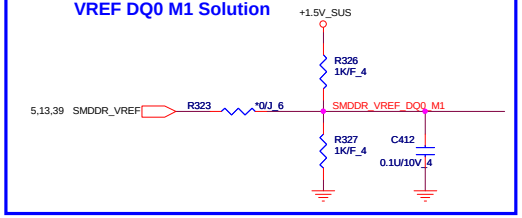
VREF DQ0 M2 Solution

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

0.5A

+1.05V_GFX_PCIE

C171 0.1U/10V_4
C167 0.1U/10V_4
C172 1U/6.3V_4
C173 1U/6.3V_4
C216 4.7U/6.3V_6
C201 10U/6.3V_8
C213 22U/6.3V_8

1.6A

+1.05V_GFX_PCIE

C169 0.1U/10V_4
C154 0.1U/10V_4
C155 1U/6.3V_4
C156 1U/6.3V_4
C166 4.7U/6.3V_6
C195 10U/6.3V_8
C212 22U/6.3V_8

CAP CLOSE TO BGA

+3V_GPU

C107 4.7U/6.3V_6
C93 1U/6.3V_4
C82 0.1U/10V_4
C86 0.1U/10V_4
C97 0.1U/10V_4

GFX_CORE

12~16 mils width for 110mA

+1.05V_GFX_PCIE

L15 BLM18PG121SN
C196 0.1U/10V_4
C187 1U/6.3V_4
C200 4.7U/6.3V_6
+PEX_PLLVDD

12~16 mils width

+3V_GPU

L1 0/J_6 +PEX_SVDD_3V3
C64 1U/6.3V_4
C153 0.1U/10V_4
C76 4.7U/6.3V_6

R60 *10K/J_4 PGOOD

R420 *40.2K/F_4 MULTI_STRAP_REF2_GND

U28A
fcbga973-nvidia-n12p-ge
COMMON

PEX_IOVDD_1 AK16
PEX_IOVDD_2 AK17
PEX_IOVDD_3 AK21
PEX_IOVDD_4 AK24
PEX_IOVDD_5 AK27

PEX_IOVDDQ_1 AG11
PEX_IOVDDQ_2 AG12
PEX_IOVDDQ_3 AG13
PEX_IOVDDQ_4 AG15
PEX_IOVDDQ_5 AG16
PEX_IOVDDQ_6 AG17
PEX_IOVDDQ_7 AG18
PEX_IOVDDQ_8 AG22
PEX_IOVDDQ_9 AG23
PEX_IOVDDQ_10 AG24
PEX_IOVDDQ_11 AG25
PEX_IOVDDQ_12 AG26
PEX_IOVDDQ_13 AJ14
PEX_IOVDDQ_14 AJ15
PEX_IOVDDQ_15 AJ19
PEX_IOVDDQ_16 AJ21
PEX_IOVDDQ_17 AJ22
PEX_IOVDDQ_18 AJ24
PEX_IOVDDQ_19 AJ25
PEX_IOVDDQ_20 AJ27
PEX_IOVDDQ_21 AK18
PEX_IOVDDQ_22 AK20
PEX_IOVDDQ_23 AK23
PEX_IOVDDQ_24 AK26
PEX_IOVDDQ_25 AL16

VDD33_1 J10
VDD33_2 J11
VDD33_3 J12
VDD33_4 J13
VDD33_5 J9

VDD_SENSE AD20
NC_9/ VDD_SENSE D35
NC_16/ VDD_SENSE P7

GND_SENSE AD19
NC_10/ GND_SENSE E35
NC_17/ GND_SENSE R7

PEX_PLLVDD AG14

PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3 AG19
NC_12/ PEX_SVDD_3V3 F7

PEX_CAL_PU_GND/ NC AG20
NC_1 A2
NC_2 AB7
NC_3 AD6
NC_4 AF6
NC_5 AG6
NC_6 AJ5
NC_7 AK15
NC_8 AL7
NC_11 E7
NC_13 H32
NC_14 M7
NC_15 P6
NC_18 U7
NC_19 V6

PCI EXPRESS

PEX_RX0 AP17
PEX_RX0* AN17
PEX_RX1 AN19
PEX_RX1* AP19
PEX_RX2 AR19
PEX_RX2* AR20
PEX_RX3 AP20
PEX_RX3* AN20
PEX_RX4 AN22
PEX_RX4* AP22
PEX_RX5 AR22
PEX_RX5* AR23
PEX_RX6 AP23
PEX_RX6* AN23
PEX_RX7 AN25
PEX_RX7* AP25
PEX_RX8 AR25
PEX_RX8* AR26
PEX_RX9 AP26
PEX_RX9* AN26
PEX_RX10 AN28
PEX_RX10* AP28
PEX_RX11 AR28
PEX_RX11* AR29
PEX_RX12 AP29
PEX_RX12* AN29
PEX_RX13 AN31
PEX_RX13* AP31
PEX_RX14 AR31
PEX_RX14* AR32
PEX_RX15 AP32
PEX_RX15* AP34

PEG_TXP15 3
PEG_TXN15 3
PEG_TXP14 3
PEG_TXN14 3
PEG_TXP13 3
PEG_TXN13 3
PEG_TXP12 3
PEG_TXN12 3
PEG_TXP11 3
PEG_TXN11 3
PEG_TXP10 3
PEG_TXN10 3
PEG_TXP9 3
PEG_TXN9 3
PEG_TXP8 3
PEG_TXN8 3
PEG_TXP7 3
PEG_TXN7 3
PEG_TXP6 3
PEG_TXN6 3
PEG_TXP5 3
PEG_TXN5 3
PEG_TXP4 3
PEG_TXN4 3
PEG_TXP3 3
PEG_TXN3 3
PEG_TXP2 3
PEG_TXN2 3
PEG_TXP1 3
PEG_TXN1 3
PEG_TXP0 3
PEG_TXN0 3

PEX_TX0 AL17 PEG_RXP15_C C260 0.1U/10V_4
PEX_TX0* AM17 PEG_RXN15_C C259 0.1U/10V_4
PEX_TX1 AM18 PEG_RXP14_C C231 0.1U/10V_4
PEX_TX1* AM19 PEG_RXN14_C C232 0.1U/10V_4
PEX_TX2 AL19 PEG_RXP13_C C258 0.1U/10V_4
PEX_TX2* AK19 PEG_RXN13_C C257 0.1U/10V_4
PEX_TX3 AL20 PEG_RXP12_C C230 0.1U/10V_4
PEX_TX3* AM20 PEG_RXN12_C C229 0.1U/10V_4
PEX_TX4 AM21 PEG_RXP11_C C255 0.1U/10V_4
PEX_TX4* AM22 PEG_RXN11_C C256 0.1U/10V_4
PEX_TX5 AL22 PEG_RXP10_C C228 0.1U/10V_4
PEX_TX5* AK22 PEG_RXN10_C C227 0.1U/10V_4
PEX_TX6 AL23 PEG_RXP9_C C254 0.1U/10V_4
PEX_TX6* AM23 PEG_RXN9_C C253 0.1U/10V_4
PEX_TX7 AM24 PEG_RXP8_C C226 0.1U/10V_4
PEX_TX7* AM25 PEG_RXN8_C C225 0.1U/10V_4
PEX_TX8 AL25 PEG_RXP7_C C252 0.1U/10V_4
PEX_TX8* AK25 PEG_RXN7_C C251 0.1U/10V_4
PEX_TX9 AL26 PEG_RXP6_C C224 0.1U/10V_4
PEX_TX9* AM26 PEG_RXN6_C C223 0.1U/10V_4
PEX_TX10 AM27 PEG_RXP5_C C250 0.1U/10V_4
PEX_TX10* AM28 PEG_RXN5_C C249 0.1U/10V_4
PEX_TX11 AL28 PEG_RXP4_C C222 0.1U/10V_4
PEX_TX11* AK28 PEG_RXN4_C C221 0.1U/10V_4
PEX_TX12 AK29 PEG_RXP3_C C219 0.1U/10V_4
PEX_TX12* AL29 PEG_RXN3_C C220 0.1U/10V_4
PEX_TX13 AM29 PEG_RXP2_C C248 0.1U/10V_4
PEX_TX13* AM30 PEG_RXN2_C C247 0.1U/10V_4
PEX_TX14 AM31 PEG_RXP1_C C218 0.1U/10V_4
PEX_TX14* AM32 PEG_RXN1_C C217 0.1U/10V_4
PEX_TX15 AN32 PEG_RXP0_C C245 0.1U/10V_4
PEX_TX15* AP32 PEG_RXN0_C C246 0.1U/10V_4

PEG_RXP15 3
PEG_RXN15 3
PEG_RXP14 3
PEG_RXN14 3
PEG_RXP13 3
PEG_RXN13 3
PEG_RXP12 3
PEG_RXN12 3
PEG_RXP11 3
PEG_RXN11 3
PEG_RXP10 3
PEG_RXN10 3
PEG_RXP9 3
PEG_RXN9 3
PEG_RXP8 3
PEG_RXN8 3
PEG_RXP7 3
PEG_RXN7 3
PEG_RXP6 3
PEG_RXN6 3
PEG_RXP5 3
PEG_RXN5 3
PEG_RXP4 3
PEG_RXN4 3
PEG_RXP3 3
PEG_RXN3 3
PEG_RXP2 3
PEG_RXN2 3
PEG_RXP1 3
PEG_RXN1 3
PEG_RXP0 3
PEG_RXN0 3

PEX_REFCLK AR16
PEX_REFCLK* AR17

CLK_PCIE_VGAP 9
CLK_PCIE_VGAN 9

PEX_TSTCLK_OUT AJ17
PEX_TSTCLK_OUT* AJ18
PEX_TSTCLK R90 *200/J_4

PEX_RST* AM16 VGA_RST# R435 *0_4_short GPU_RST#
GPU_RST# 9

R441 1 2 100K/J_4

PEX_CLKREQ* AR13 R468 10K/J_4 +3V_GPU
PEX_CLKREQ# 9

PEX_TERMP AG21 PEX_TERMP R79 2.49K/F_4

TESTMODE AP35 TESTMODE R141 10K/J_4

+3V_GPU
+3V
R104 EV@10K/F_4
R85 EV@10K/F_4
GFXPG 9,10
Q19 MMBT3904

+1.8V_GPU R101 EV@10K/F_4
*EV@1000P/50V/X7R_4@NC C197
R80 *EV@0_4
Q17 PDTC143TT

+1.5V_GPU R72 EV@10K/F_4
*EV@1000P/50V/X7R_4@NC C147
Q12 PDTC143TT

For power-down sequency

+3V_GPU +1.5V_GPU +3V_GPU GFX_CORE
D6 RB500V-40
D5 RB500V-40

The following voltage constraints must be satisfied at all times including power down after VDD33 has ramped up:

- NVVDD <= VDD33+0.5 V
- FBVDDQ <= VDD33+0.5 V

9,39,42 GFXON

R107 0/J_4
C179 *1U/6.3V_4

+1.05V_GFX_PCIE +3V
R102 *100K/F_4
R109 *390/F_4
R112 *8.2K_4
+3V_GPU_EN
+3V_GPU_EN 44
Q21 *MMBT3904
Q20 *ME2N7002E

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(PCIe)	1A
Date: Friday, October 29, 2010	Sheet 15 of 47	

U28B
fcbga973-nvidia-n12p-ge
COMMON

MEMORY I/F A

U28C
fcbga973-nvidia-n12p-ge
COMMON

MEMORY I/F C

POP For Debug only

3/18 Change to 60.4ohm

PLACE NEAR BALLS

PLACE UNDER BALLS

PBY201209T-331Y-N

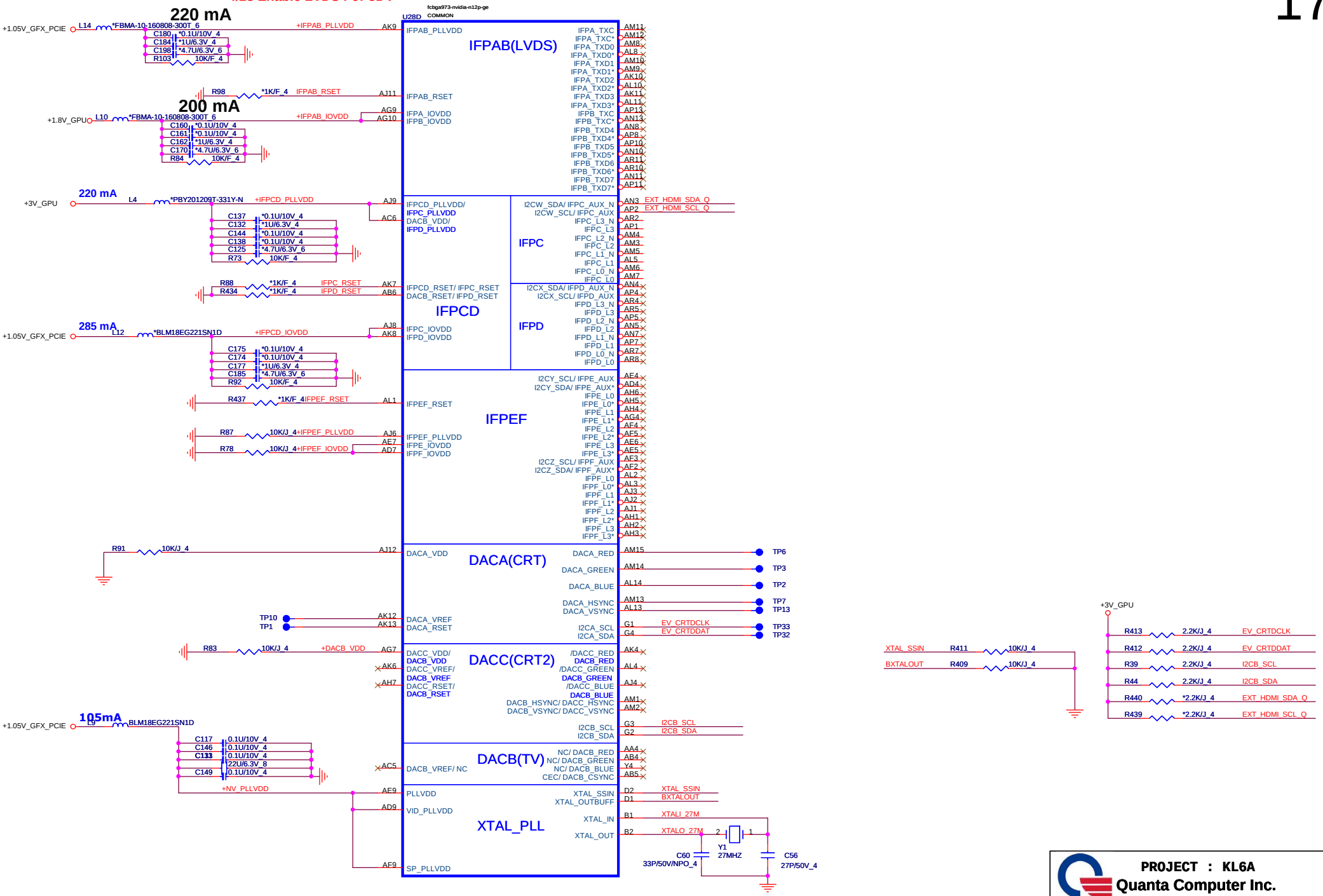
15mils width

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(MEM IF)	1A

Date: Friday, October 29, 2010 Sheet 16 of 47

4/28 Enable LVDS For 3DV



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(Display)	1A

Date: Friday, October 29, 2010 Sheet 17 of 47

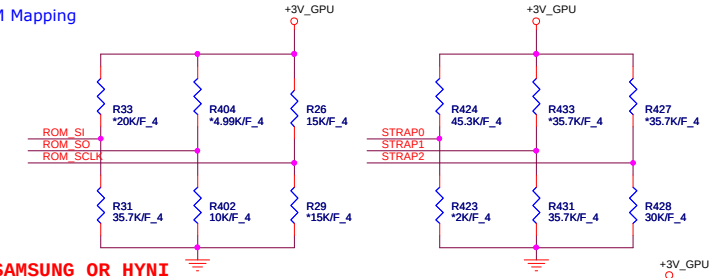
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 2GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW06	H5TQ2G63BFR-12C
0x7(0111)	800MHz 2GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT507	K4W2G1646B-HC12
0x6(0110)	900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

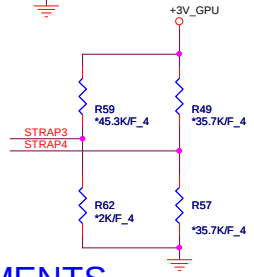
ROM_SI Strap Bit for RAM Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

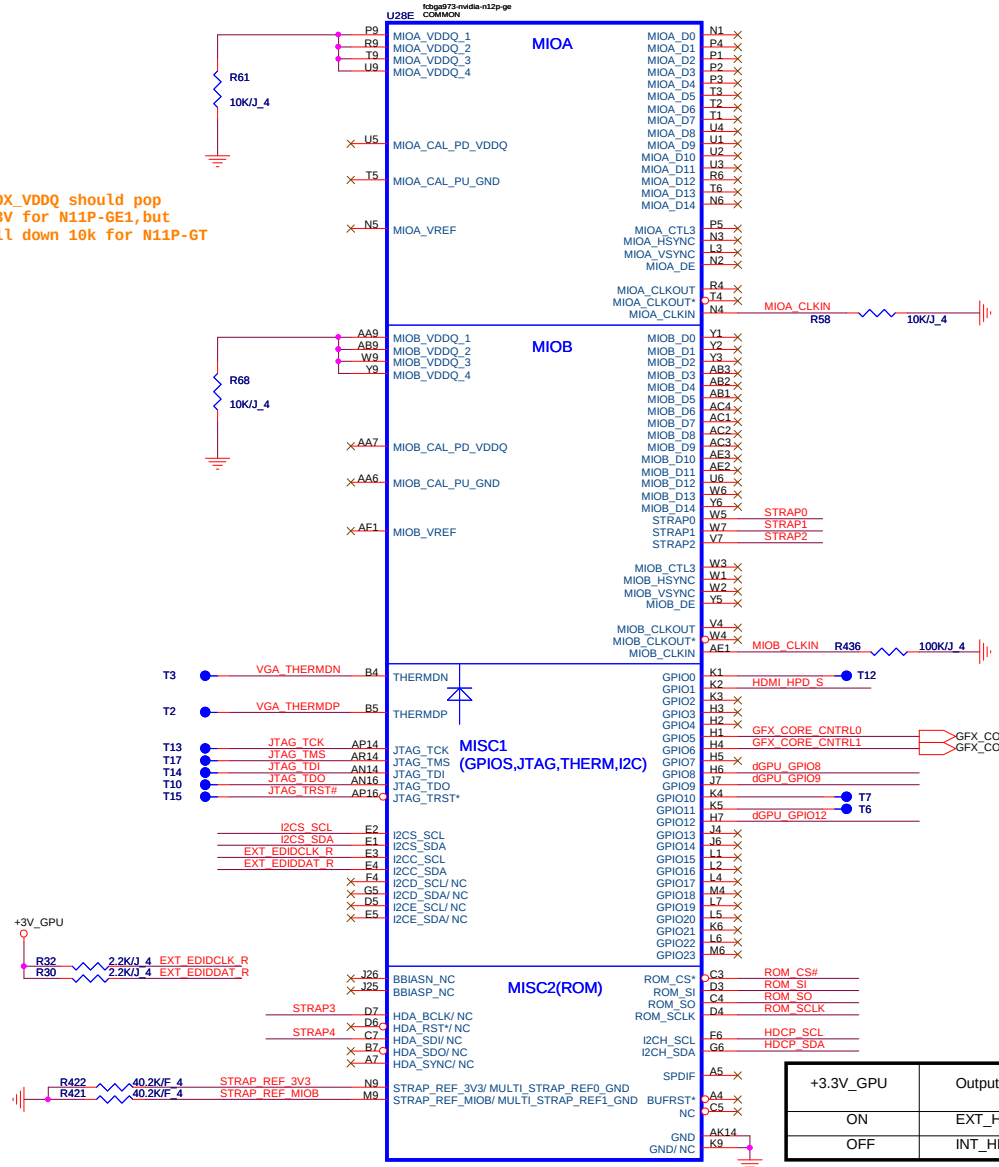


SAMSUNG OR HYNI

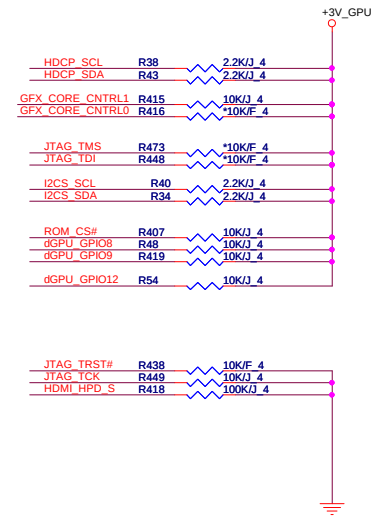
N12P-GE ROM_SO 10K pull low
Strap2 30K pull low
N12P-GV1 ROM_SO 10K pull low
Strap2 45K pull low
N12P-GV ROM_SO 10K pull high
Strap2 45K pull high
Strap3 5K pull low
Strap4 20K pull low

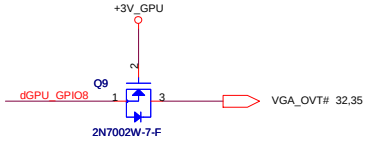


MIOX_VDDQ should pop 3.3V for N11P-GE1,but pull down 10k for N11P-GT



+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

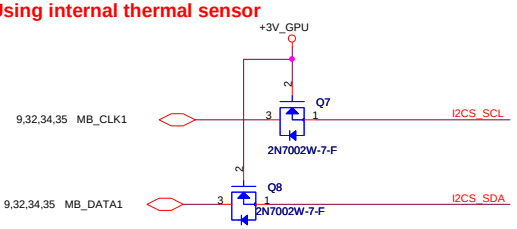




GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

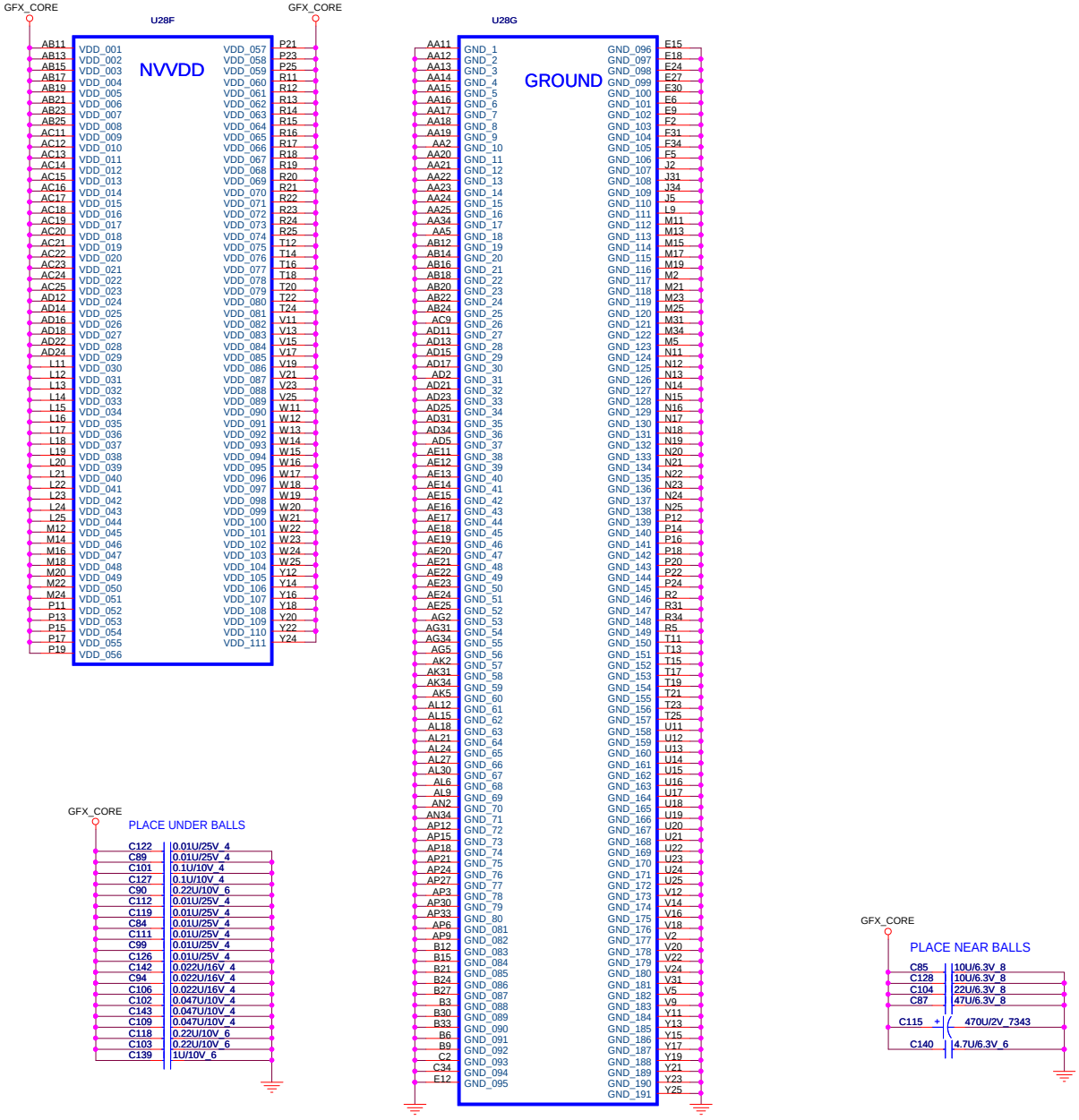
Using internal thermal sensor



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(GPIO/STRAP)	1A

Date: Friday, October 29, 2010 Sheet 18 of 47



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-N12P GB2-128(POWER)	1A

Date: Friday, October 29, 2010 Sheet 19 of 47

16 VMA_DQ[63..0]
16 VMA_DM[7..0]
16 VMA_WDQS[7..0]
16 VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

U4 / U27 / U7 / U29 — 96-BALL SDRAM DDR3 K4W1G1646E-HC11

Should be 240 Ohms +-1%

R67 240/F_4 (U4) · R410 240/F_4 (U27) · R97 240/F_4 (U7) · R430 240/F_4 (U29)

+1.5V_GPU

Placement has to be close to VRAM

R417 1.33K/F_4 · R414 1.33K/F_4 · C518 0.01U/25V_4 · VREFC_VMA1

R52 1.33K/F_4 · R45 1.33K/F_4 · C70 0.01U/25V_4 · VREFD_VMA1

C123 *10U/6.3V_6

R77 1.33K/F_4 · R86 1.33K/F_4 · C159 0.01U/25V_4 · VREFC_VMA3

R425 1.33K/F_4 · R426 1.33K/F_4 · C529 0.01U/25V_4 · VREFD_VMA3

R405 162/F_4 · VMA_CLKP0 · VMA_CLKN0

R95 162/F_4 · VMA_CLKP1 · VMA_CLKN1

C528 C65 C168 C145 C531 C186 C7 C15 C234 C235 C133 C535 — 1U/6.3V_4 / 0.1U/10V_4

C572 C526 C527 C533 C532 C71 C523 C524 C574 C573 C236 C194 — 1U/6.3V_4 / 0.1U/10V_4

C32 C48 C52 C55 C507 C100 C525 C59 C88 C58 C114 C176 — 1U/6.3V_4 / 0.1U/10V_4

C510 C520 C513 C514 C72 C4 C5 C515 C519 C522 C183 C516 — 1U/6.3V_4 / 0.1U/10V_4

PROJECT	KL6A
Quanta Computer Inc.	
Size	
Document Number	VGA-N12P GB2-128(VRAM-1)
Rev	1A
Date:	Friday, October 29, 2010
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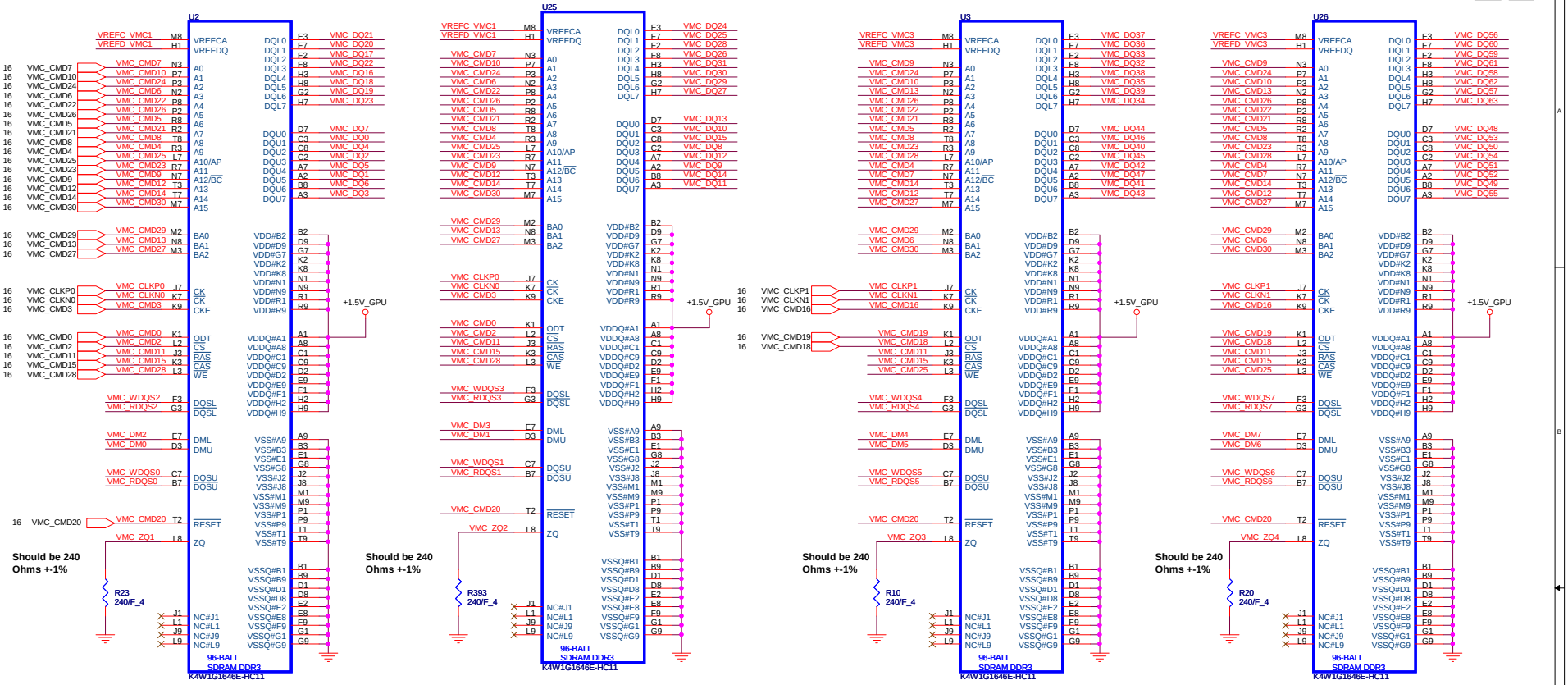
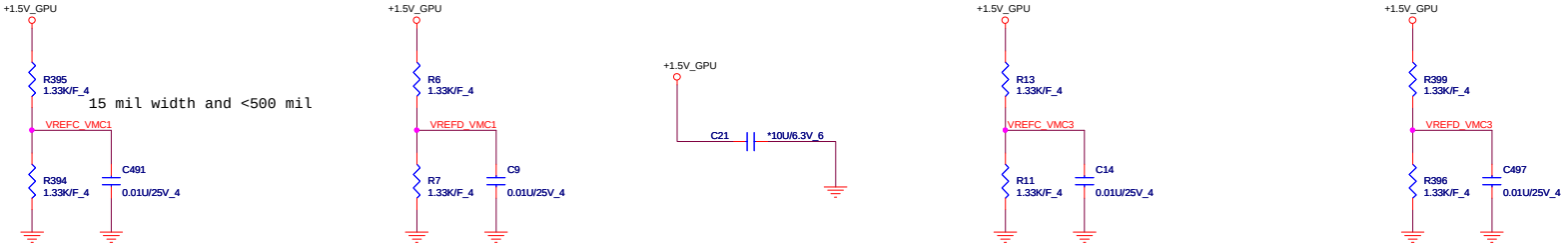
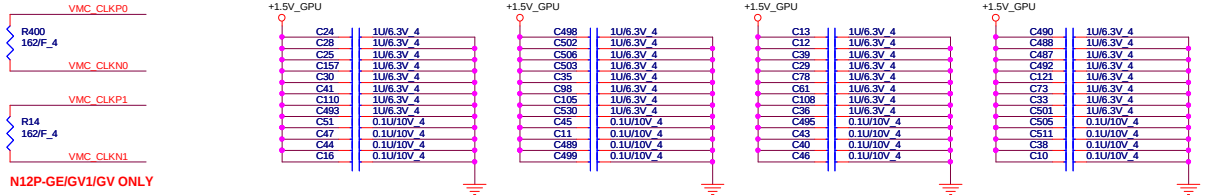
CHANNEL B: 512MB/1024MB DDR3

16 VMC_DQ[63..0]
16 VMC_DM[7..0]
16 VMC_WDQS[7..0]
16 VMC_RDQS[7..0]

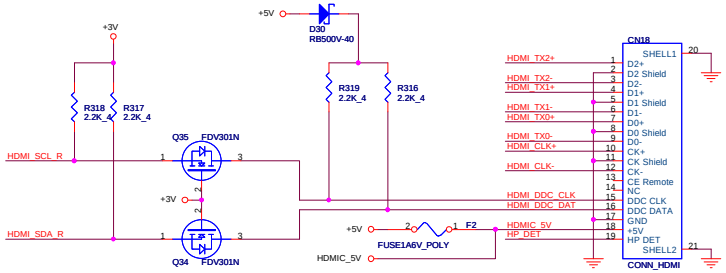




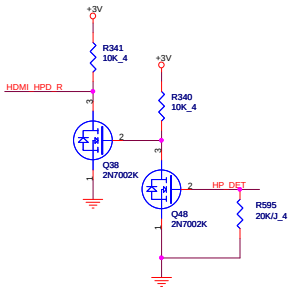
Placement has to be close to VRAM

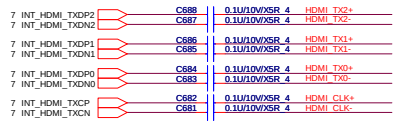


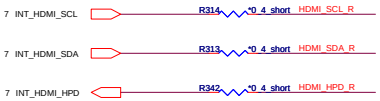
PROJECT : KL6A		
Quanta Computer Inc.		
Size	Document Number: VGA-N12P GB2-128(VRAM-2)	Rev: 1A
Date: Friday, October 29, 2010	Sheet 21 of 47	

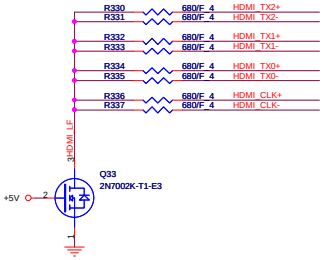


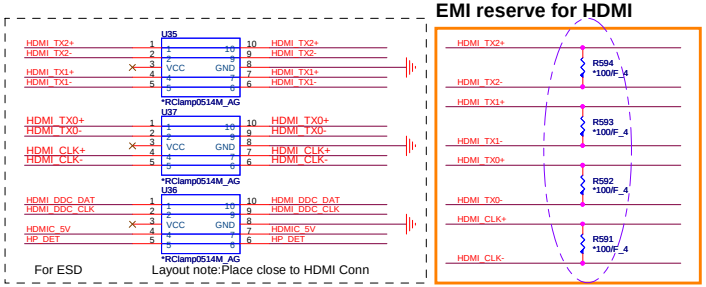
HDMI Hot-PLUG to EC and GPU











7,8,11,23,26,27,32,33,34,35,36,37,38,45 +5V
7,8,9,10,11,13,14,15,23,24,25,26,27,28,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V

PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

Date: Friday, October 29, 2010 Sheet 22 of 47

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

7 INT_CRT_RED
7 INT_CRT_GRE
7 INT_CRT_BLU
L23 BLM18BA470SN1
L22 BLM18BA470SN1
L21 BLM18BA470SN1
CRT_R1
CRT_G1
CRT_B1
R230 150/F_4
R225 150/F_4
R215 150/F_4
C305 5.6P/50V/COG_4
C291 5.6P/50V/COG_4
C285 5.6P/50V/COG_4
C284 5.6P/50V/COG_4
C292 5.6P/50V/COG_4
C306 5.6P/50V/COG_4
TP19
CRT_VCC
D26 RB500V-40
C617 0.1U/10V/X5R_4
+5V
F1 FUSE1A6V_POLY
C274 *VARISTOR_4
CRT_VCC_R
CN14 CRT_CONN

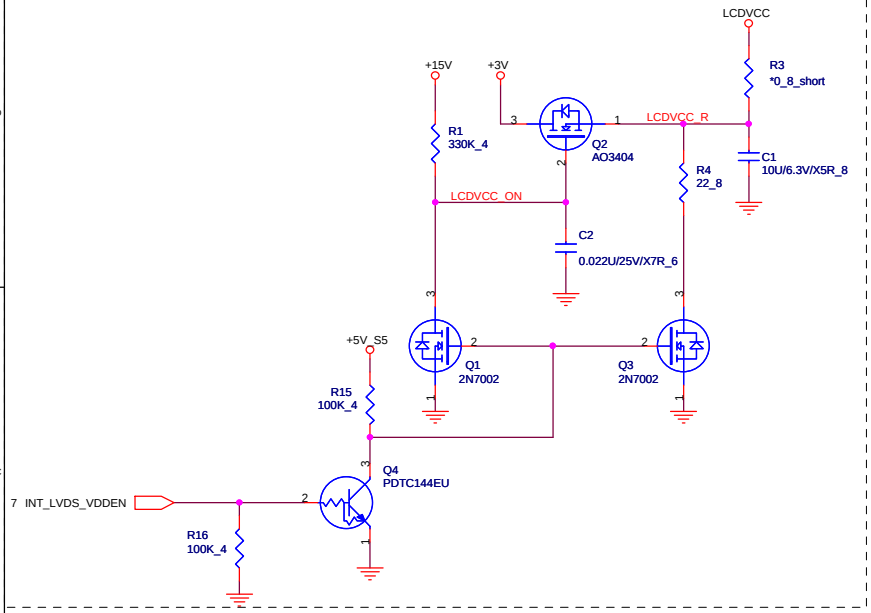
ESD PROTECTION
D21 *TVSS5VESPT CRT_R1
D20 *TVSS5VESPT CRT_G1
D18 *TVSS5VESPT CRT_B1
D15 *TVSS5VESPT CRTVSYNC
D16 *TVSS5VESPT CRTHSYNC
D25 *TVSS5VESPT DDCCLK
D27 *TVSS5VESPT DDCDAT

+5V
7 INT_CRT_VSYNC
U14 AHCT1G125DCH
VGAVSYNC_R
R188 10_4
CRTVSYNC1
C286 0.1U/10V/X5R_4
7 INT_CRT_HSYNC
U16 AHCT1G125DCH
VGAHSYNC_R
R203 10_4
CRTHSYNC1
Place near U37,U38 < 200 mil
C275 *10P/50V/COG_4
C265 *10P/50V/COG_4
L16 HB-1T1608-121JT
L20 HB-1T1608-121JT
CRTVSYNC
CRTHSYNC
C277 10P/50V/COG_4
C264 10P/50V/COG_4
Place near CN5002 connector < 200 mil

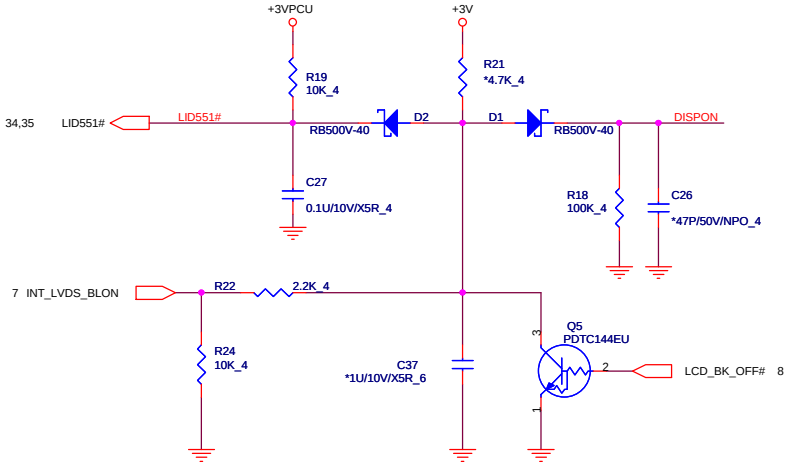
+3V
R567 2.2K_4
R553 2.2K_4
CRT_VCC
R564 4.7K_4
R540 4.7K_4
7 INT_DDCCLK
7 INT_DDCDAT
Q43 2N7002K-T1-E3
Q44 2N7002K-T1-E3
DDCCLK
DDCDAT
C610 *10P/50V/COG_4
C587 *10P/50V/COG_4

PROJECT : KL6A
Quanta Computer Inc.
Size: Custom
Document Number: CRT CONN
Rev: 1A
Date: Friday, October 29, 2010
Sheet 23 of 47

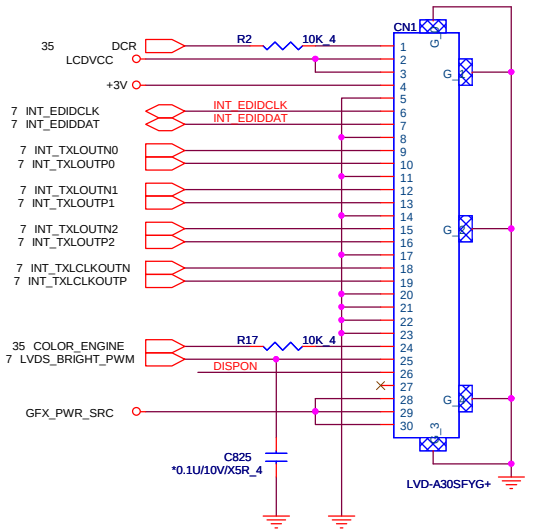
LCDVCC

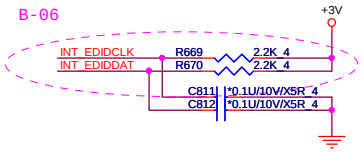


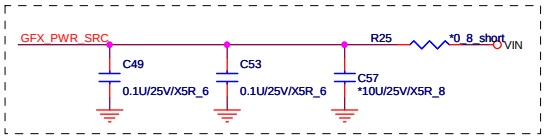
back light



7,8,9,10,11,13,14,15,22,23,25,26,27,28,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V
27,28,29,37,39,40,41,44 +15V
7,8,25,27,33,34,35,37,38,40,41 +3VPCU
36,38,39,40,42,43,44,45 VIN





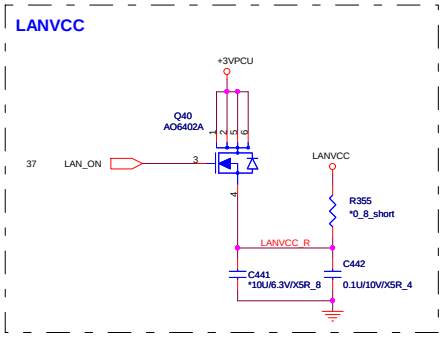


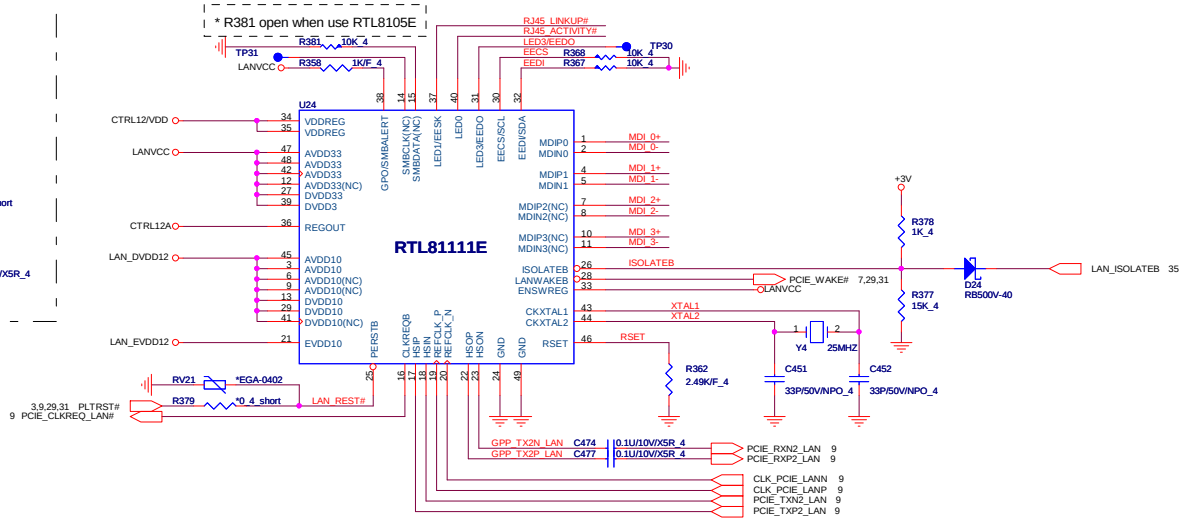
PROJECT : KL6A
Quanta Computer Inc.

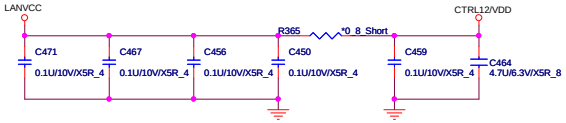
Size	Document Number	Rev
Custom	LCD CONN	1A

Date: Friday, October 29, 2010 Sheet 24 of 47

LANVCC



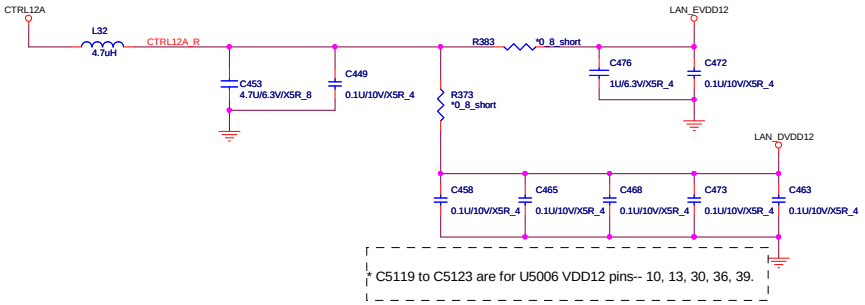




* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.

Place C5113 ,C5094 closed to U5006 pins44,45.

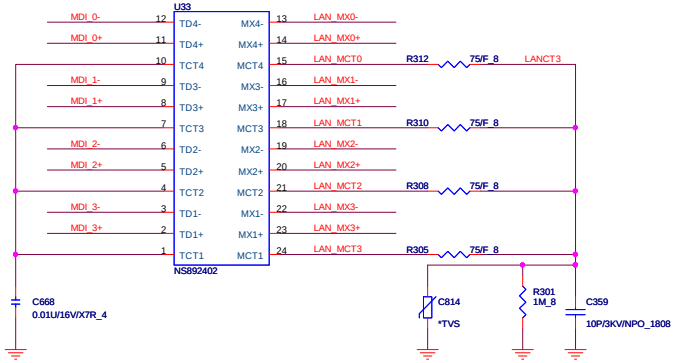
* C476 and C472 are for U24 LAN_EVDD12 pin 21.



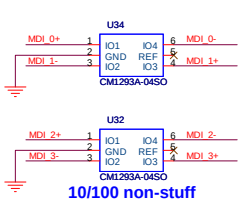
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

Layout:All termination signal should have 20 mil trace

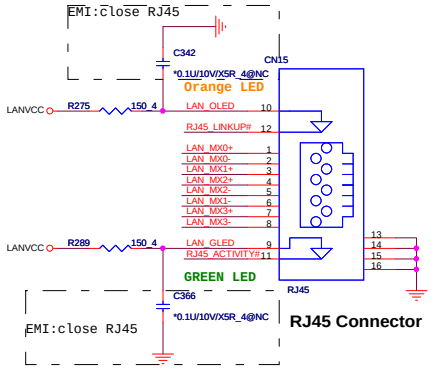
Tramsformer



RJ45 Connector



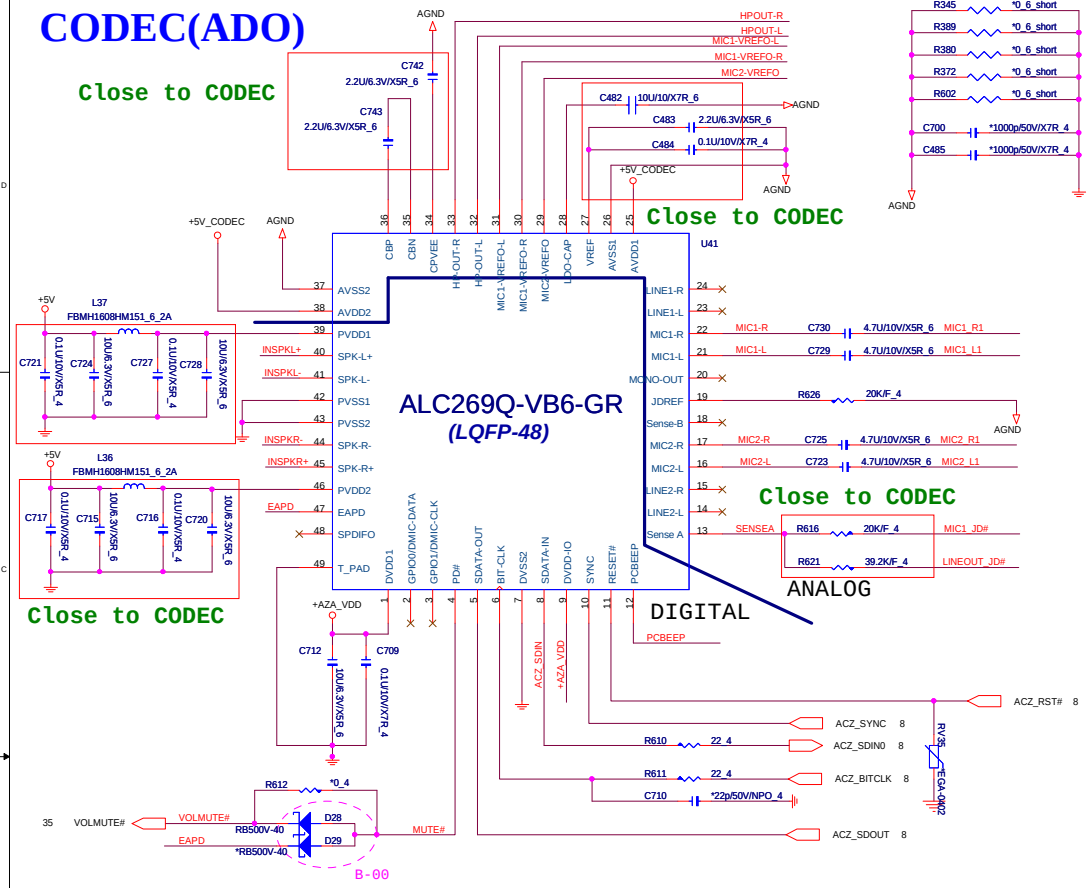
10/100 non-stuff



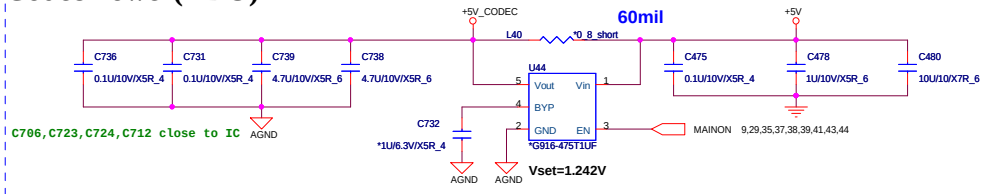
RJ45 Connector

PROJECT : KL6A			
Quanta Computer Inc.			
Size: Custom	Document Number: RTL8111EL-VB		Rev: 1A
Date: Friday, October 29, 2010	Sheet 25 of 47		

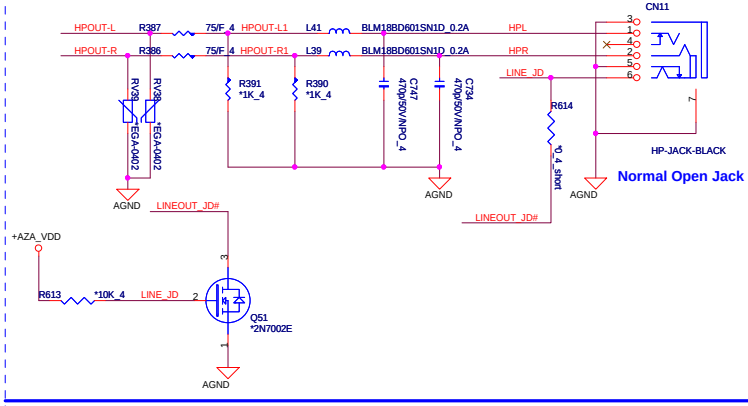
CODEC(ADO)



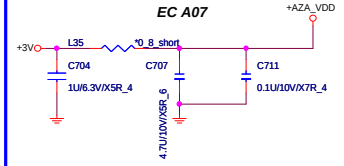
Codec Power(ADO)



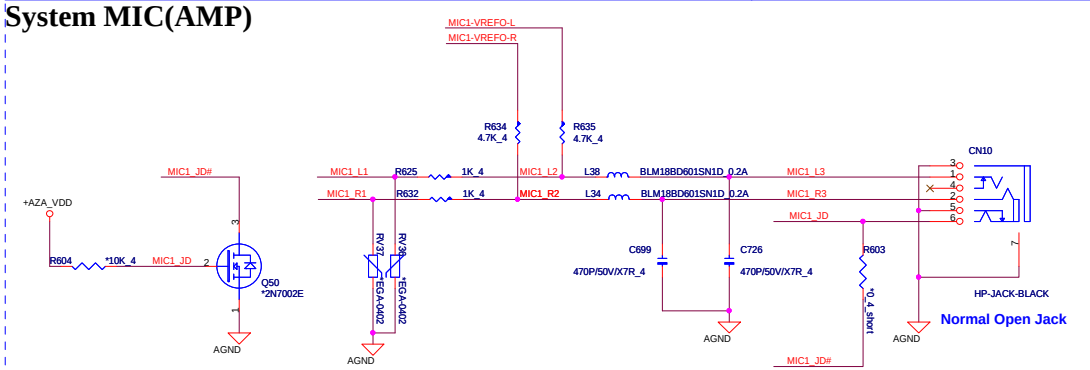
Earphone(AMP)



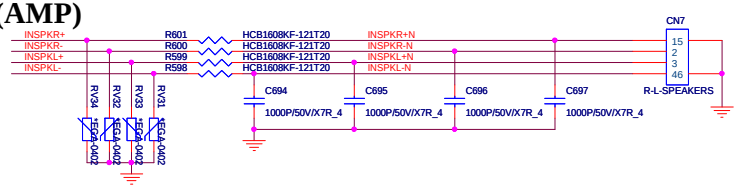
HDA Power(ADO)



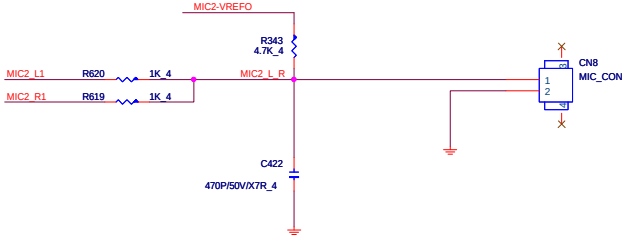
System MIC(AMP)



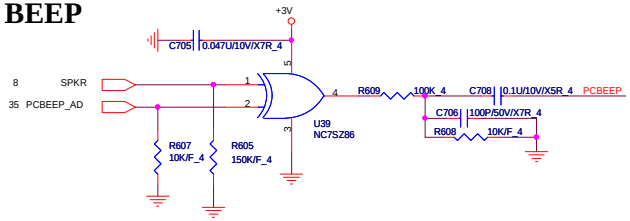
Speaker(AMP)



INTERNAL MIC



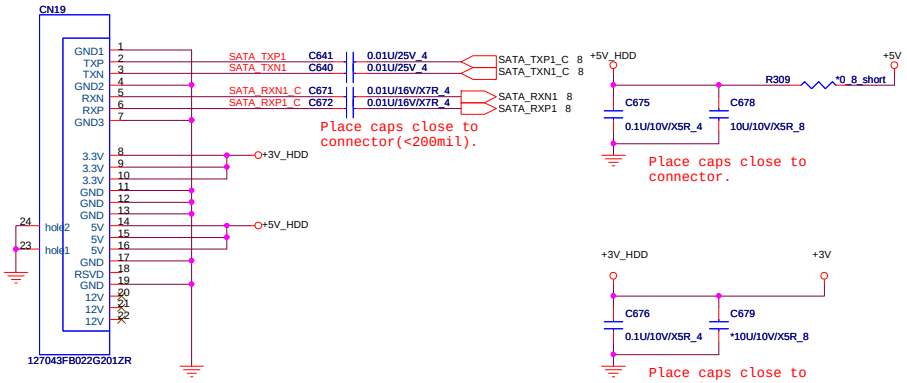
PC BEEP



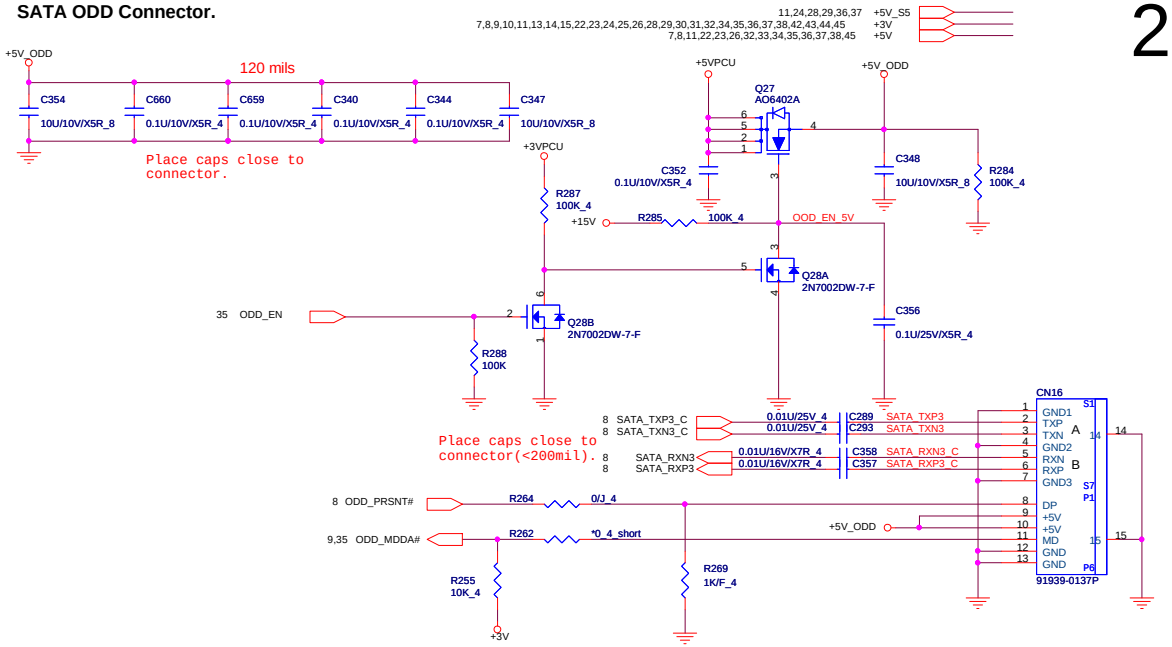
PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC269/MIC/Line out	1A
Date: Friday, October 29, 2010	Sheet 26 of 47	

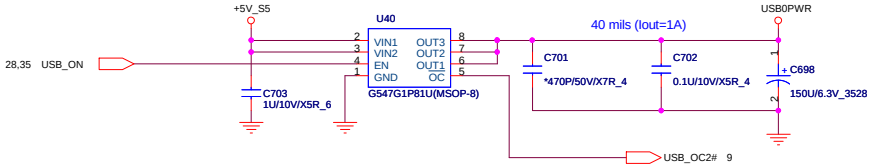
SATA HDD Connector.

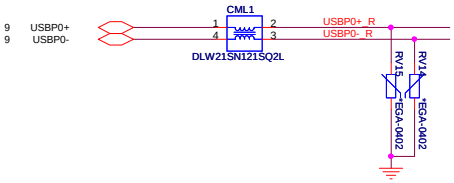


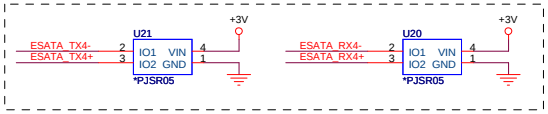
SATA ODD Connector.



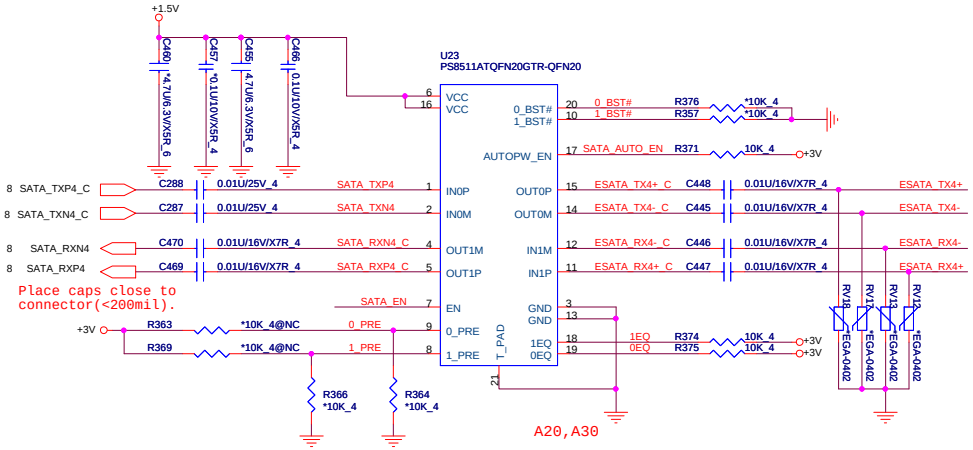
USB + E-SATA







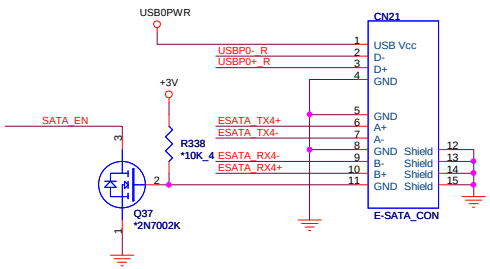
E-SATA RE-DRIVER



All straps of PS8511A have int. PL 150Kohm.

EN	AUTO_EN	0/1EQ	0/1EQ	0/1_BST#	0/1_BST#	0/1_PRE	0/1_PRE	Function
0	X	X	X	X	X	X	X	Standby
1	0	X	X	X	X	X	X	disable auto power saving
1	1	X	X	X	X	X	X	enable auto power saving
1	X	0	X	X	X	X	X	Short and medium length
1	X	X	1	X	X	X	X	Long length
1	X	X	X	0	X	X	X	Output :800~1200 mVpp
1	X	X	X	X	1	X	X	Output :400~700 mVpp
1	X	X	X	X	X	0	X	Pre-emphasis disabled
1	X	X	X	X	X	X	1	Pre-emphasis enabled

USB 0



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A

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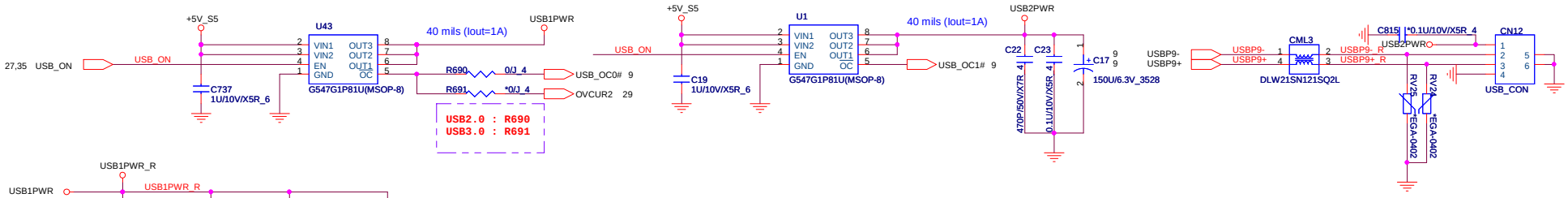
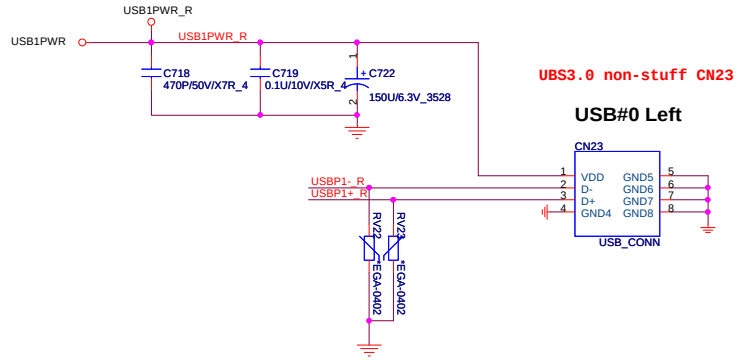
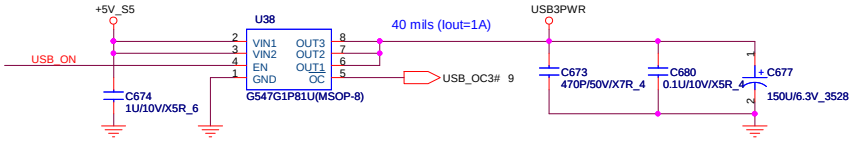
11,24,27,29,36,37 +5V_S5
7,8,9,10,11,13,14,15,22,23,24,25,26,27,29,30,31,32,34,35,36,37,38,42,43,44,45 +3V
24,27,29,37,39,40,41,44 +15V

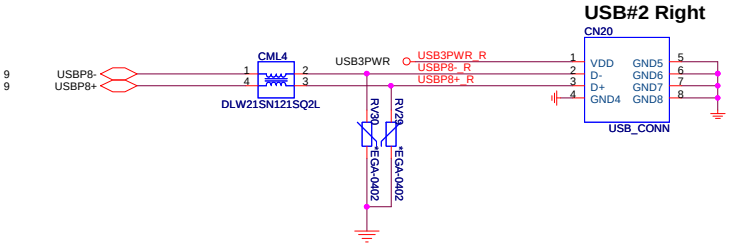
USB2.0*3

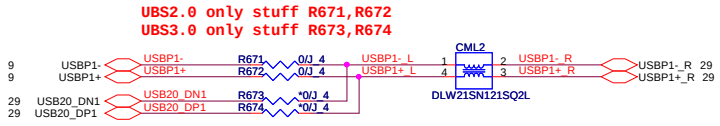
USB#1 Daughter board



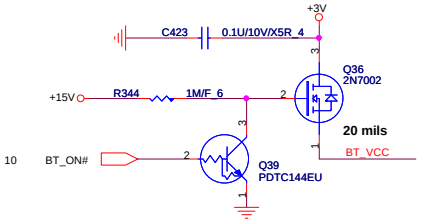


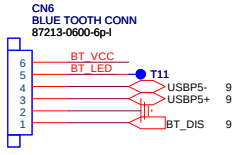






BLUETOOTH





PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
	BT/USBX3	1A

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REAR USB PORT X1

SPI Flash ROM

P3V3_USB30

R648 10K/F_4

U45 MX25L512MC-12G

SPICS# SPISCLK SPISI SPISO

CE# SCK SI SO WP# VDD HOLD# VSS

Copy From ZN7

R649 10K/F_4 R650 10K/F_4 SMDAT SMCLK

+3.3VAUX

OVCUR1 R651 10K_4

OVCUR2 R652 10K_4

OVCUR3 R653 10K_4

OVCUR4 R655 10K_4

USB3.0 PORT1

CN24

USB1PWR_R

28 USBP1-_R

28 USBP1+_R

USB30_RX1- USB30_RX1+

U3TXDN1 0.1U/16V_4 C754 USB30_TX1-

U3TXDP1 0.1U/16V_4 C752 USB30_TX1+

C754, C752 close to CN24

VBUS D- D+ GND SSRX- SSRX+ GND SSTX- SSTX+

USB3.0 CONN

SUY USB3.0: DFHS09FR063

Q55 2N7002E

PLTRST#

10,35 EC_EXT_SMI#

USB30_SMI#

+3.3VAUX

R677 *10K/F_4 R646 *10K/F_4 R647 10K/F_4

PCIE_WAKE#

USB30_SMI#

JTAGCK

7,25,31 PCIE_WAKE#

OVCUR2 28

TESTEN R656 4.7K_4

SSREXT R657 6.04K/F_4

PEXREXT R654 3.01K/F_4

TP61 TP62 TP63 TP64 TP65 TP66

0.1U/16V_4 C806

U47

VL800 / VL801 QFN88

VL800 4PORT

VL801 2PORT

Near PCIEx Slot

For debug only.
Don't connect to system SMBus

VDD SSTX1+ SSTX1- VCCA10SSRX1 SSRX1+ SSRX1- VCCA33SS1 USBHP1+ USBHP1- VCCA33SS1 SSTX2+ SSTX2- VCCA10SSRX2 SSRX2+ SSRX2- VCCA33SS2 USBHP2+ USBHP2- VCCA33SS2 VCCA10SSM SSXI SSXO

VSUSS33 USBHPE2# USBHPE3# USBHPE4# SPISO SPISI SPISCLK SPICS# VDD VCCA33PEXTX PEXTX0- PEXTX0+ VCCA33PEXM PEXRX0- PEXRX0+ VCCA33PEXRX PEXCLK- PEXCLK+ VCCA33REG12 PEXREXT VCCA33REG25 VDD

PWREN2 PWREN3 PWREN4 TP67 TP68 TP69

PCIE_RXN5_C PCIE_RXP5_C C755 0.1U/16V_4 C753 0.1U/16V_4

PCIE_RXN5 9 PCIE_RXP5 9

PCIE_TXN5 9 PCIE_TXP5 9

CLK_100_USB30_N 9 CLK_100_USB30_P 9

PLTRST_PCIE_N_USB 0_4 R660 PLTRST# 3,9,25,31

Remove power for VL801

ESD

U46 *RClamp0544.TBT msop10-4_9-5

USB30_RX1- USB30_RX1+ USB30_TX1- USB30_TX1+ USB1PWR

X'tal 25MHz

27P/50V_4 C756 R662 *0_6 short SSXI

Y7 25MHz/20pF/30ppm

27P/50V_4 C757 SSXO

BG625000486

XTL-5_3X3_2-3_8-1_2H

Crystal foot print must be reserved in case 25MHz clock from clock generator is not stable enough.

Power circuit (+1.05_SUS) For USB3.0

+5V_S5 C758 1U/6.3V_4 U48 G9661-25ADJF11U

9,26,35,37,38,39,41,43,44 MAINON R663 *10K/F_6

35,37,39 SUSON R664 10K/F_6

+1.5V_SUS

VPP PGOOD VEN VO VIN GND GND ADJ NC

0.6A P1V05_SUS

R1 R665 10K/F_6

0.8V

R2 R666 33K/F_6

C767 C768 C769 C770

Vout =0.8(1+R1/R2)

For USB3.0

Remove SUSD turn on switch (From PCU to SUS)
(Used +3V_S5 power plane)

For +3V_SUS (Power for wake up)

From M/B +3V_SUS L42 BLM18PG300SN1D +3.3VAUX

C759 4.7uF/6.3V_6 C760 0.1U/16V_4 C761 4.7uF/6.3V_6 C762 0.1U/16V_4

For +3V_RUN

From M/B +3V L43 BLM18PG300SN1D P3V3_USB30

C763 4.7uF/6.3V_6 C764 0.1U/16V_4 C765 4.7uF/6.3V_6 C766 0.1U/16V_4

For +1.05_SUS (Power for wake up)

P1V05_SUS From M/B L44 BLM18PG300SN1D P/N:CX11P300000

1.0V L45 BLM18PG300SN1D L46 BLM18PG300SN1D 1.0VE 1.0VL

C771 4.7uF/6.3V_6 C772 0.1U/16V_4 C773 C774 4.7uF/6.3V_6 C775 0.1U/16V_4 C776 4.7uF/6.3V_6

Power sequence for Host.

+3.3VSUS +3.3V Reset +1.0V

+3.3VAUX C777 C778 C779 C780 C781 C782 C783 C784 C785 C786

1.0VL C787 C788 C789 C790 C791 C792

P3V3_USB30 C793 C794 C795 C796 C797

+3.3VAUX C798 C799 C800

1.0VE C801 C802 C803 C804 C805

All 0.1U/16V_4

PLTRST_PCIE_N_USB circuit

P3V3_USB30 R692 100K/F_4 Q58 ME2303T1 C822 1U/6.3V_4 COREPWRDN

+15V / +3V_S5 / +3V_SUS

+15V R693 1M_4 Q59 AO6402A +3V_S5

C823 *0.1U/50V/X7R_6 +3V_SUS C824 0.1U/10V/X7R_4

37 SUSON# Q60 2N7002K

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Quanta Computer Inc.

Size	Document Number	Rev
C	USB3.0 *1	1A

Date: Friday, October 29, 2010 Sheet 29 of 47

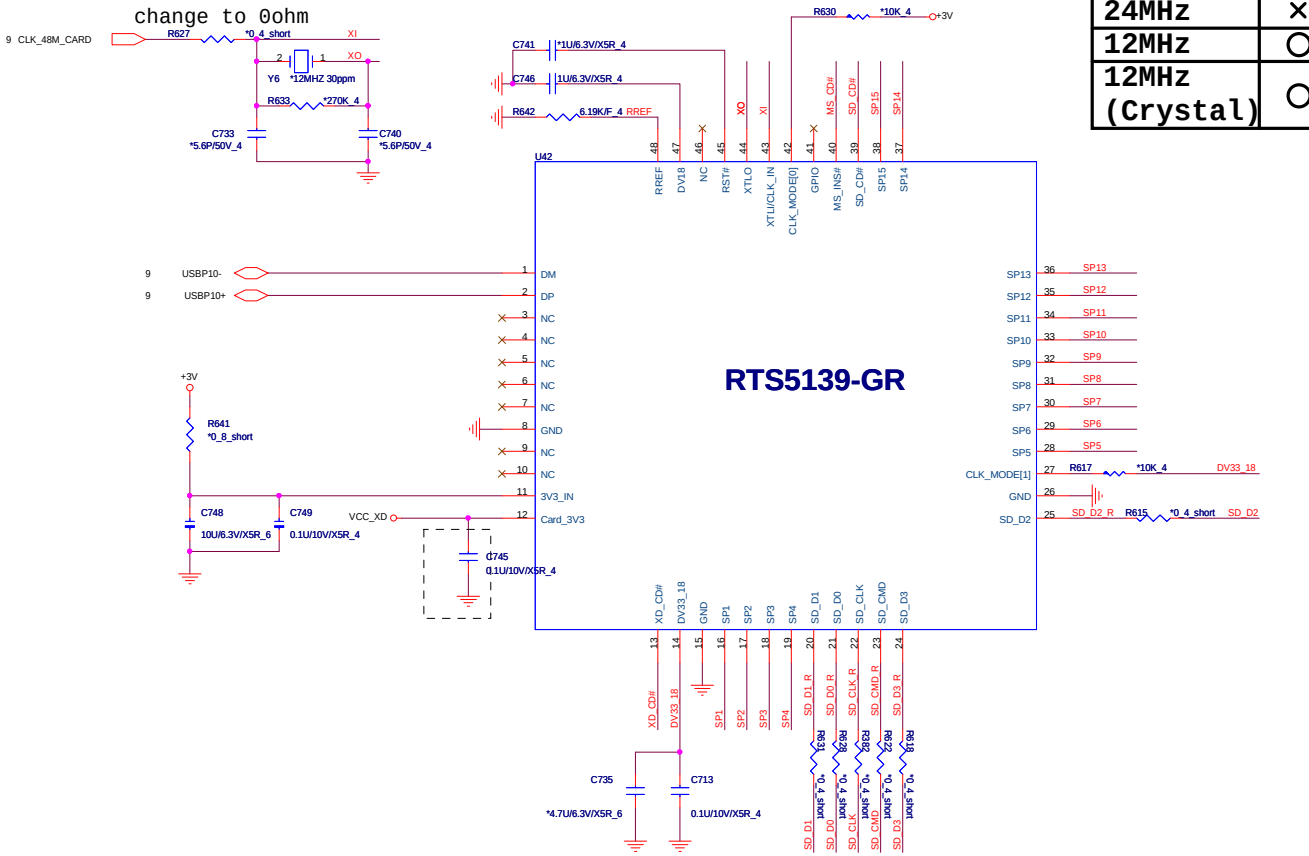
Clock Mode strap	R9287	R9307
48MHz	×	×
24MHz	×	○
12MHz	○	×
12MHz (Crystal)	○	○

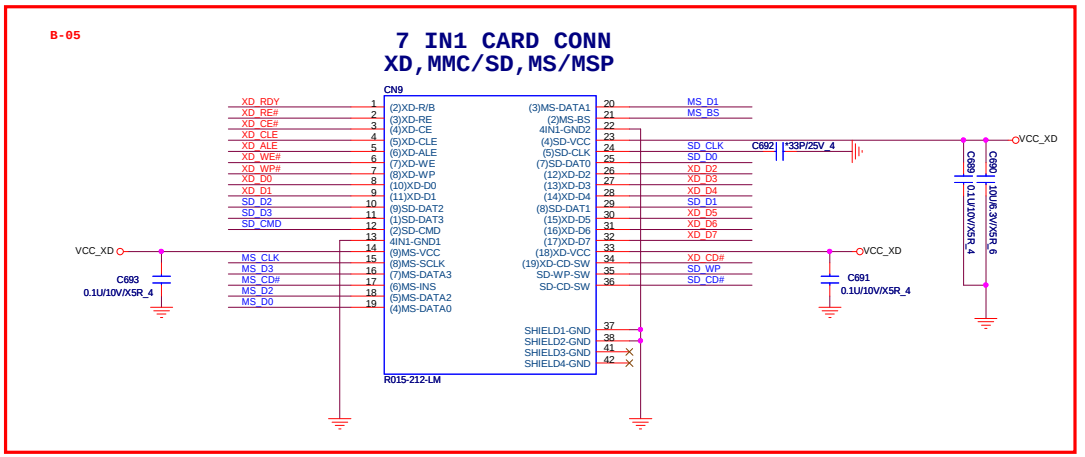
Note:

SD/MMC	MS	XD
SP1 SD_D7		XD_RDY
SP2 SD_D6		XD_RE#
SP3 SD_D5		XD_CE#
SP4 SD_D4		XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15 SD_WP		XD_D7

For RTS5139

SD,MS 4bit only





PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader (RTS5159)	1A

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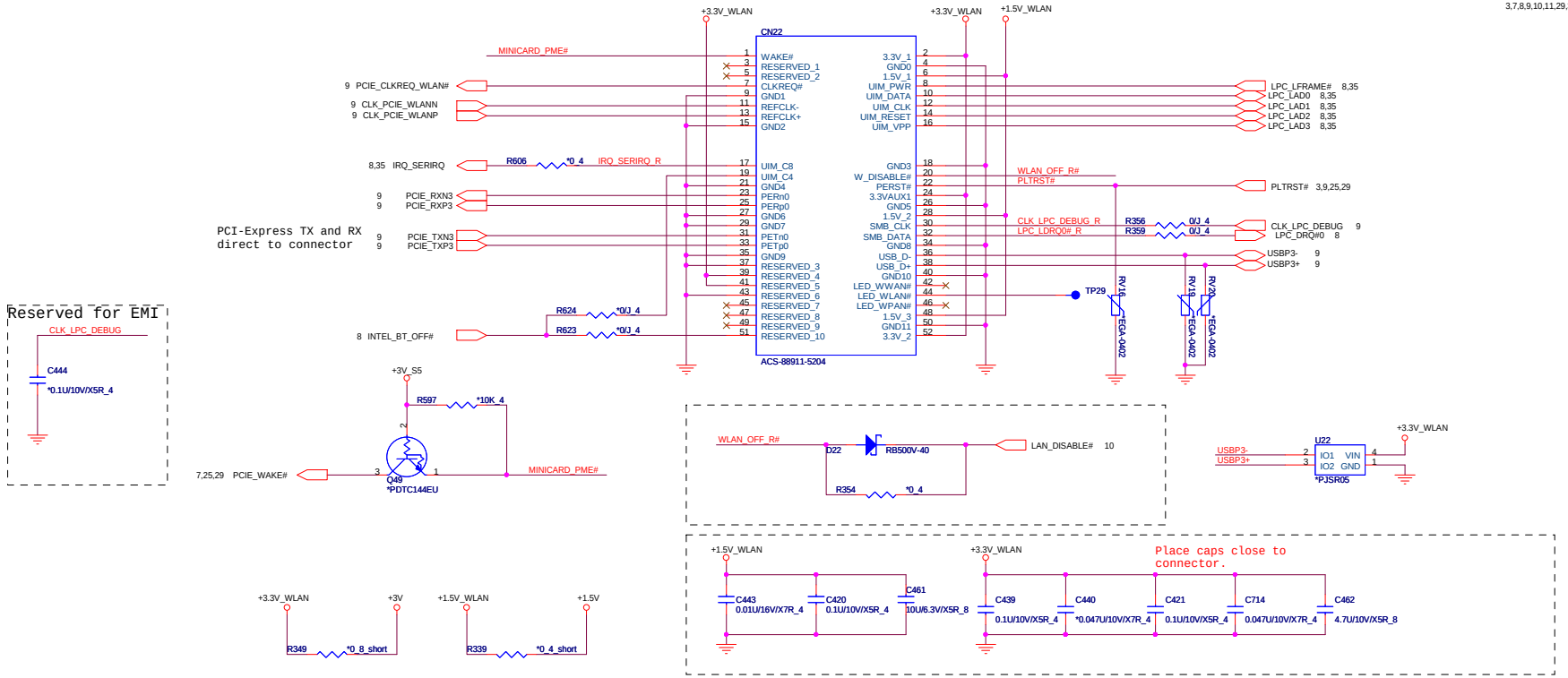
MiniCard WLAN connector

7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,32,34,35,36,37,38,42,43,44,45 +3V
11,27,37 +1.5V
3,7,8,9,10,11,29,34,37 +3V_S5



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-Card WLAN	1A

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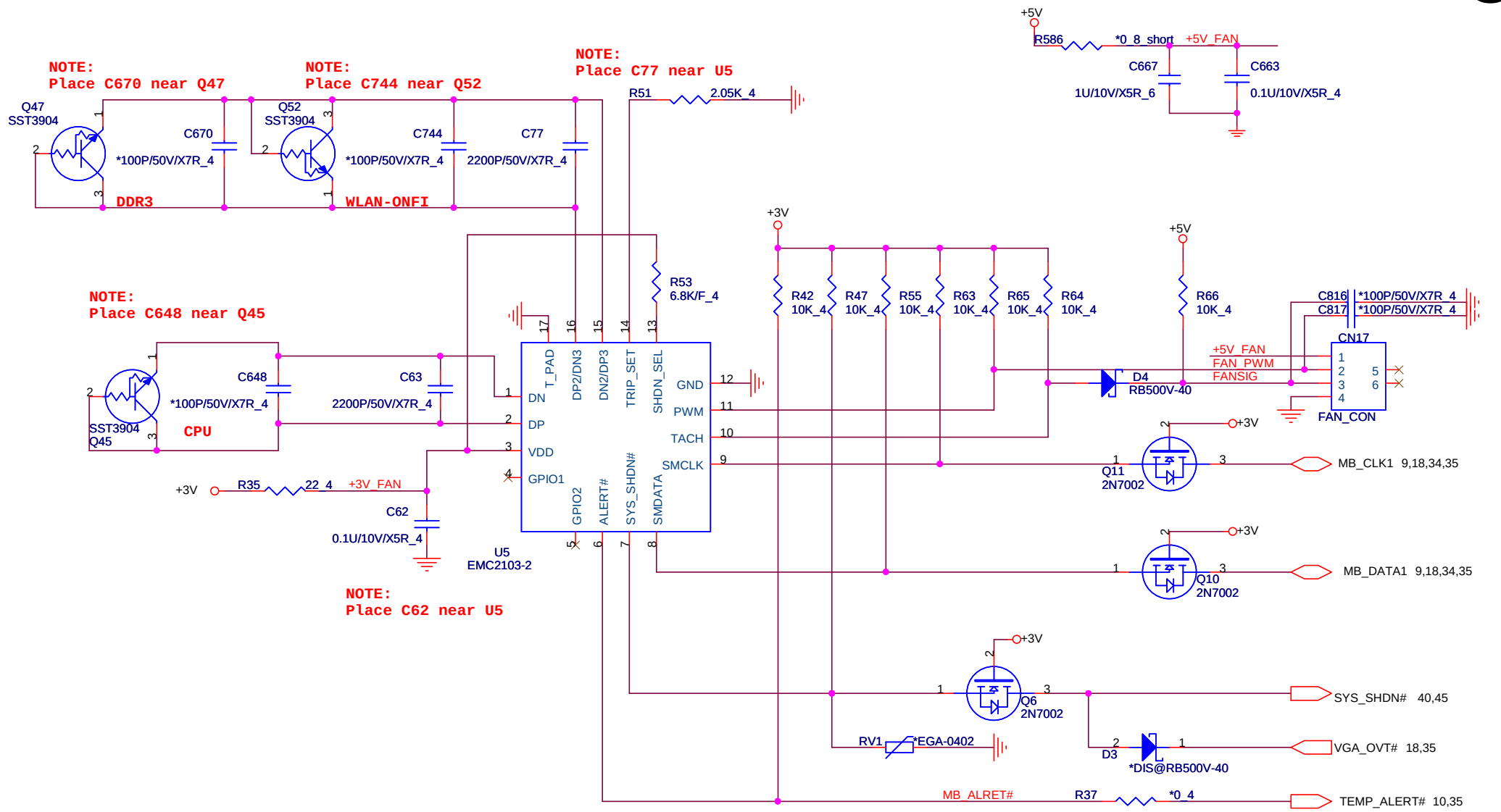
FAN CONTROL

7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,31,34,35,36,37,38,42,43,44,45 +3V
7,8,11,22,23,26,27,33,34,35,36,37,38,45 +5V

32



PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A

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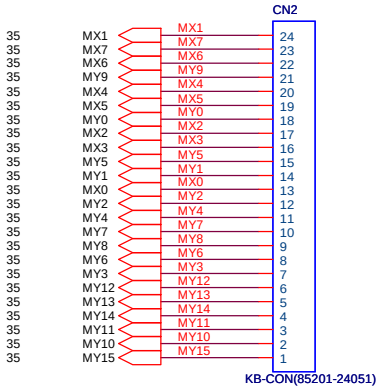
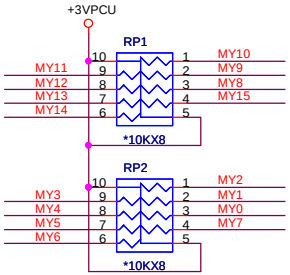
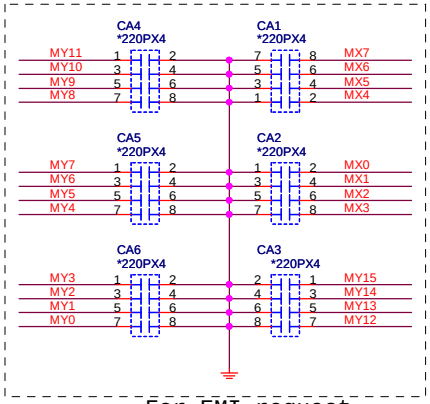
KEYBOARD

7,8,11,22,23,26,27,32,34,35,36,37,38,45 +5V
7,8,24,25,27,34,35,37,38,40,41 +3VPCU

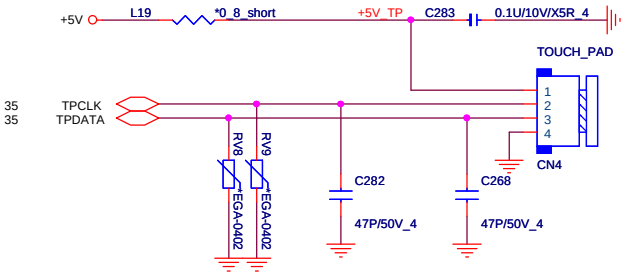






For EMI request

Touch pad



PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B, T/P	1A

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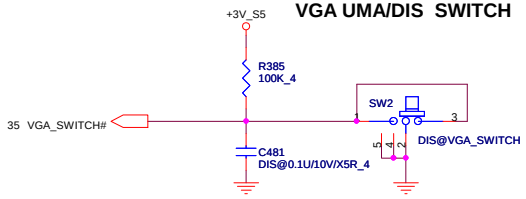
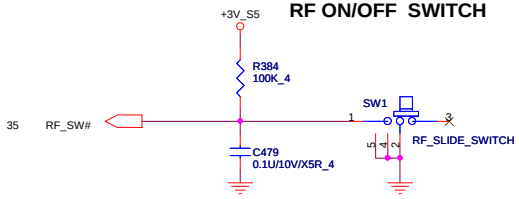
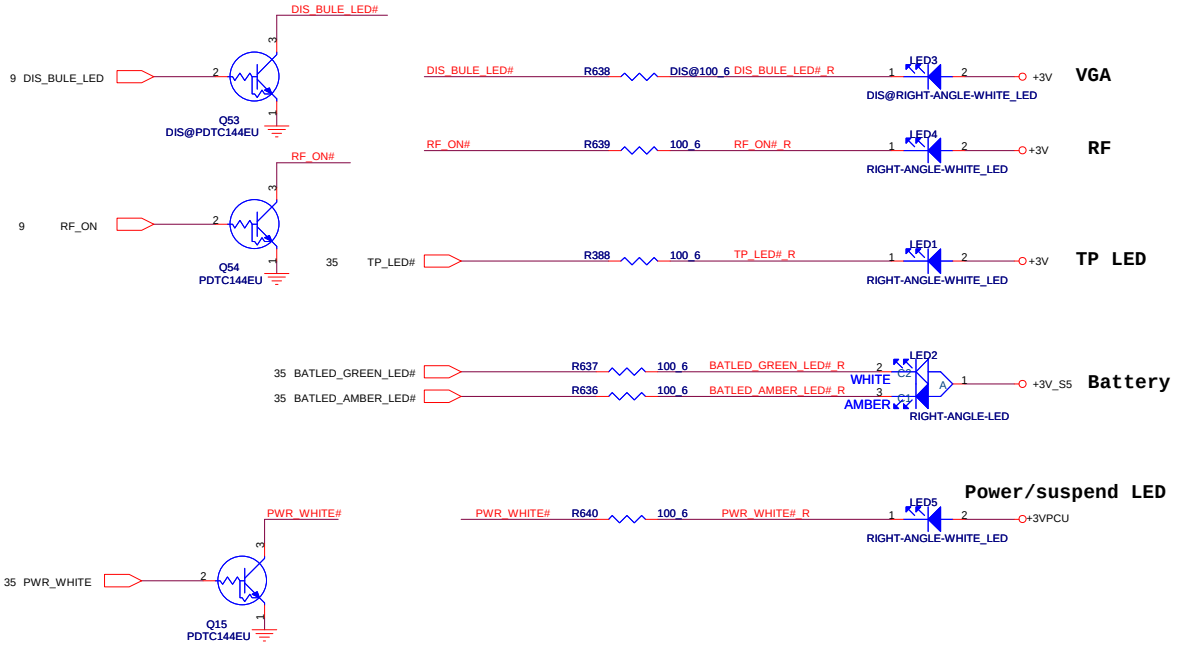
3,7,8,9,10,11,29,31,37 +3V_S5
7,8,9,10,11,13,14,15,22,23,24,25,26,27,28,29,30,31,32,35,36,37,38,42,43,44,45 +3V

VGA UMA/DIS SWITCH

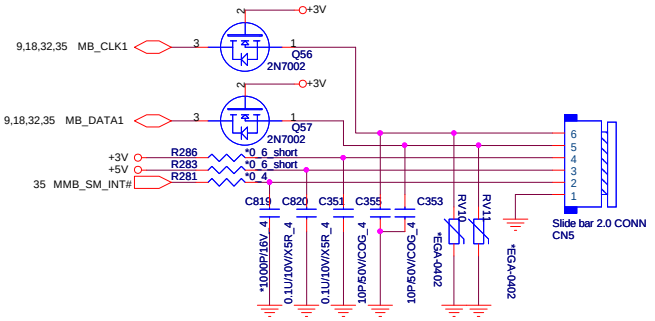


RF ON/OFF SWITCH

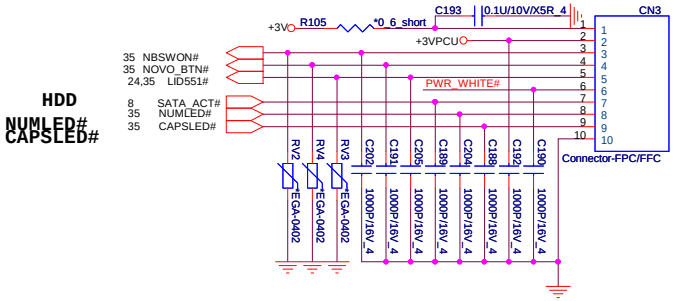




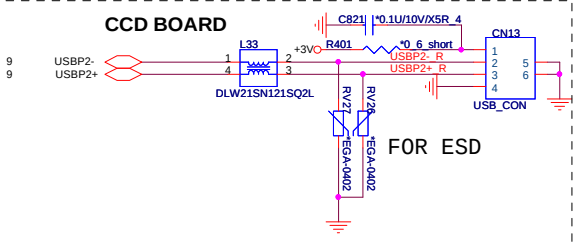
CAPACITANNCE BUTTON BOARD



POWER BOARD



CCD BOARD



PROJECT : KL6A		
Quanta Computer Inc.		
Size: Custom	Document Number: B TO B CON/LED	Rev: 1A
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IT8518 IT8519

Board ID

+3VPCU
R76 DIS@10K_4
BOARD_ID
R75 *10K_4

DIS =>R76
UMA=>R75

Power Switch / Novo Button

+3VPCU R208 10K_4 — NBSWON# — C276 0.1U/10V/X5R_4
+3.3V_EC R100 10K_4 — NOVO_BTN# — C182 0.1U/10V/X5R_4

4Mbit (512K Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

+3VPCU R217 10K_4 — R224 10K_4
U18 W25X40BVSSIG: CE# SCK SI SO WP# VDD HOLD# VSS
8512_SCE# 8512_SCK R213 47_4 8512_SCK1
8512_SI R204 47_4 8512_SI1
8512_SO R220 15_4 8512_SO1
C294 0.1U/10V/X5R_4

Clock

CK32KE CK32K — IT8512_CK32KE — IT8512_CK32K
Y5 *32.768KHZ
R534 0/J_4
C592 *18P/50V/COG_4
C593 *18P/50V/COG_4
C575 *1U/6.3V/X5R_4
C552 0.1U/10V/X5R_4

Power Rails

IT8512_AVCC: L11 BK1608HS121-T, L18 BK1608HS121-T, L13 BK1608HS121-T, C209 1000P/16V/X7R_4, C207 1U/6.3V/X5R_4, C271 0.1U/10V/X5R_4 (For PLL Power)
IT8512_VSTBY: C181, C584, C208, C272, C269, C270 0.1U/10V/X5R_4
U13 IT8518 0.1U/10V/X5R_4, C244
D14 *DIS@RB500V-40

LPC

LAD0/GPM0(X) LAD1/GPM1(X) LAD2/GPM2(X) LAD3/GPM3(X) LPCRST#/WUI4/GPD2(Up) LPCCLK/GPM4(X) LFRAME#/GPM5(X) LPCPD#/WUI6/GPE6(Dn) GA20/GPB5(X) SERIRQ/GPM6(X) ECSMI#/GPD4(Up) ECSCI#/GPD3(Up) WRST# KBRST#/GPB6(X) PWUREQ#/BBO/SMCLK2ALT/GPC7(Up)

SM BUS / PS/2

SMCLK0/GPB3(X) SMDAT0/GPB4(X) SMCLK1/GPC1(X) SMDAT1/GPC2(X) SMCLK2/WUI22/GPF6(Up) SMDAT2/WUI23/GPF7(Up)
PS2CLK0/TMB0/GPF0(Up) PS2DAT0/TMB1/GPF1(Up) PS2CLK2/WUI20/GPF4(Up) PS2DAT2/WUI21/GPF5(Up)

GPIO

EGCLK/WUI27/GPE2(Dn) EGAD/WUI26/GPE1(Dn) EGCS#/WUI25/GPE0(Dn) L80HLATIBAO/WUI24/GPE0(Dn) L80LLATIWUI7/GPE7(Up) HMOSI/GPH6/ID6(Dn) HMISO/GPH5/ID5(Dn) HSCK/GPH4/ID4(Dn) HSCE#/WUI19/GPH3/ID3(Dn) CLKRUN#/WUI16/GPH0/ID0(Dn)

CIR

CRX0/GPC0(Dn) CTX0/TMA0/GPB2(Dn)

PWM

PWM0/GPA0(Up) PWM1/GPA1(Up) PWM2/GPA2(Up) PWM3/GPA3(Up) PWM4/GPA4(Up) PWM5/GPA5(Up)
TACH0A/GPD6(Dn) TACH1A/TMA1/GPD7(Dn)
TMR0/WUI2/GPC4(Dn) TMR1/WUI3/GPC6(Dn)

UART port

DAC4/DCD0#/GPJ4(X) DSR0#/GPG6(X) GINT/CTS0#/GPD5(Up) PS2DAT1/RTS0#/GPF3(Up) DAC5/RIG0#/GPJ5(X) PS2CLK1/DTR0#/GPF2(Up) TXD/SOUT0/GPB1(Up) RXD/SIN0/GPB0(Up)

WAKE UP

ADC5/DCD1#/WUI29/GPI5(X) ADC6/DSR1#/WUI30/GPI6(X) ADC7/CTS1#/WUI31/GPI7(X) RTS1#/WUI5/GPE5(Dn) PWM7/RIG1#/GPA7(Up) DTR1#/SBUSY/GPG1/ID7(Dn) CTX1/WUI18/SOUT1/GPH2/SMDAT3/ID2(Dn) CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1(Dn)
PWRSW/GPE4(Up) RI1#/WUI0/GPD0(Up) RI2#/WUI1/GPD1(Up)
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7(Dn)

External Serial Flash

FSCK FSCE# FMOSI FMIO

SPI Enable

KSO16/SMOSI/GPC3(Dn) KSO17/SMISO/GPC5(Dn) PWM6/SSCK/GPA6(Up)
SSCE0#/GPG2(X) SSCE1#/GPG0(X)

KBMX

KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
MY[0..15] MX[0..7]

A/D D/A

ADC0/GPI0(X) ADC1/GPI1(X) ADC2/GPI2(X) ADC3/GPI3(X) ADC4/WUI28/GPI4(X)
TACH2/GPJ0(X) GPJ1(X) DAC2/TACH0B/GPJ2(X) DAC3/TACH1B/GPJ3(X)

Misc

H_PROCHOT#_Q R71 *0_4_short → H_PROCHOT# 3,45
H_PROCHOT#_EC R111 100K/J_4 — Q13 2N7002E
GFX_PWRGD R572 *DIS@0_4 HWPG R506 10K_4
HMOSI HMISO HSCK HSCE# R197–R513 *0_4 → PCH_SPI_SI/SO/CLK/CS0# 8
MB_CLK1 R485 4.7K_4; MB_DATA1 R493 4.7K_4; MBCLK R205 2.2K_4; MBDATA R209 2.2K_4; BATLED_AMBER_LED# R196 *10K_4; BATLED_GREEN_LED# R198 *10K_4; TEMP_BBAT R96 10K_4; BL/C# R130 *10K_4; BAYSWAP# R99 10K_4
CLK_PCI_8512 → R497 33_4
EMI suggestion: Add a 15p bypass CAP on CLK_PCI_8512
Layout Note: Place all capacitors close to IT8512.
Layout Note: net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Screw for ME

WLAN

HOLE18 H-TC217BC142D102P2

HOLE19 H-TC217BC75I75D35P2

SMT NUT H=4/7mm

VGA

HOLE16 DIS@H-TC5_5BC4I3D3P2

HOLE17 DIS@H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

CPU BKT

HOLE9 *C142D102N

HOLE15 AGND *HG-TC276BC315D106P2

HOLE13 *HG-TC276BC315D106P2

HOLE12 *HG-TC276BC315D106P2

HOLE11 *HG-TC276BC315D106P2

HOLE14 *HG-TC276BC315D106P2

HOLE8 *HG-TC276BC315D106P2

HOLE5 *HG-TC276BC315D106P2

HOLE6 *HG-TC276BC315D106P2

HOLE4 *H-TC276BC315D106P2

HOLE3 *H-TC276BC315D106P2

HOLE2 *H-TC276BC315D106P2

HOLE10 *H-BS236X150D59PB

HOLE7 *H-BC197D59PB

HOLE20 *Spad-re1010x45np

HOLE21 *Spad-re1010x45np

HOLE22 *spad-kl6-1np

HOLE23 *spad-kl6-2np

HOLE24 *spad-re160x774np

HOLE25 *spad-re225x460np

EMI suggestion

VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	VIN	+5V	+VCC_GFX	+VCC_GFX
C367	C54	C31	C415	C296	C20	C406	C405	C50	C807	C808	C809
*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	*0.1U/25V/X5R_4	*0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/25V/X5R_4	0.1U/25V/X5R_4	2200P/50V/X7R_4

B-08

+5V_S5	+3V	+3V	+1.05V_PCH	+1.05V_PCH	+1.5V_SUS	GFX_CORE	VIN
SC822 *0.1U/25V/X5R_4	SC823 *0.1U/25V/X5R_4			SC824 *0.1U/25V/X5R_4		SC825 *0.1U/25V/X5R_4	
SC826 *0.1U/25V/X5R_4	SC827 *0.1U/25V/X5R_4			SC828 *0.1U/25V/X5R_4		SC829 *0.1U/25V/X5R_4	
SC830 *0.1U/25V/X5R_4	SC831 *0.1U/25V/X5R_4						
SC832 *0.1U/25V/X5R_4	SC833 *0.1U/25V/X5R_4						
SC869 *0.1U/25V/X5R_4	SC870 *0.1U/25V/X5R_4						

VIN	+3V
SC834 *0.1U/25V/X5R_4	
SC838 *0.1U/25V/X5R_4	
SC841 *0.1U/25V/X5R_4	
SC844 *0.1U/25V/X5R_4	
SC847 *0.1U/25V/X5R_4	
SC850 *0.1U/25V/X5R_4	

+VCC_CORE	VIN
SC835 *0.1U/25V/X5R_4	
SC837 *0.1U/25V/X5R_4	

VIN	+1.5V_SUS	+3V
SC839 0.1U/25V/X5R_4	SC840 *0.1U/25V/X5R_4	
SC842 0.1U/25V/X5R_4	SC843 *0.1U/25V/X5R_4	
SC845 0.1U/25V/X5R_4	SC846 *0.1U/25V/X5R_4	
SC848 0.1U/25V/X5R_4	SC849 *0.1U/25V/X5R_4	
SC851 0.1U/25V/X5R_4	SC852 *0.1U/25V/X5R_4	
SC855 *0.1U/25V/X5R_4	SC856 *0.1U/25V/X5R_4	
SC857 0.1U/25V/X5R_4	SC858 *0.1U/25V/X5R_4	
SC859 *0.1U/25V/X5R_4	SC860 *0.1U/25V/X5R_4	
SC861 0.1U/25V/X5R_4	SC862 *0.1U/25V/X5R_4	
SC863 0.1U/25V/X5R_4	SC864 *0.1U/25V/X5R_4	
	SC867 *0.1U/25V/X5R_4	

+5V	+5V_S5
SC865 *0.1U/25V/X5R_4	
SC868 *0.1U/25V/X5R_4	

+5V_S5	+1.5V_SUS
SC854 *0.1U/25V/X5R_4	

VIN	+5V
SC866 *0.1U/25V/X5R_4	

HDMIC_5V
SC876 *0.1U/25V/X5R_4

SC872	*0.1U/25V/X5R_4
SC873	*0.1U/25V/X5R_4
SC874	*0.1U/25V/X5R_4
SC875	*0.1U/25V/X5R_4

ESD suggestion

PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLD & SKEW	1A

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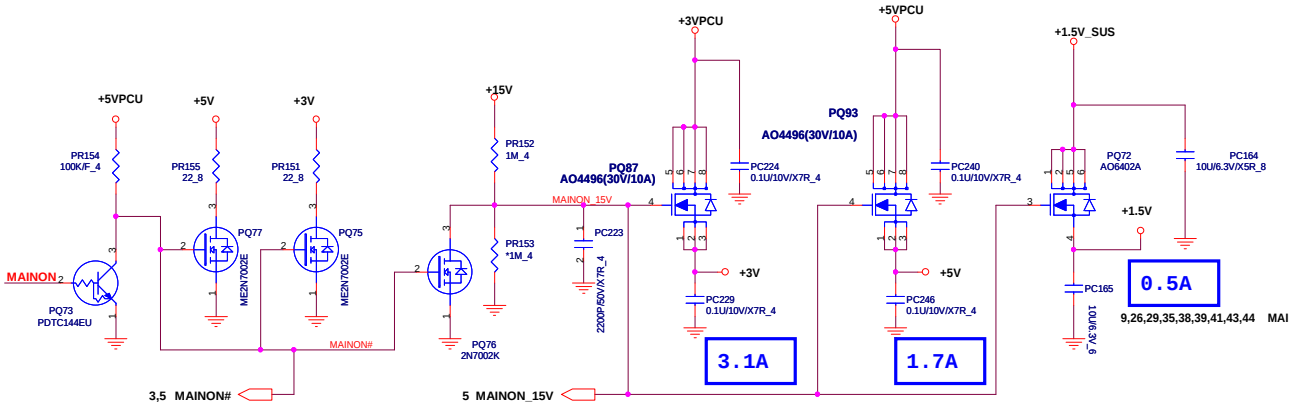
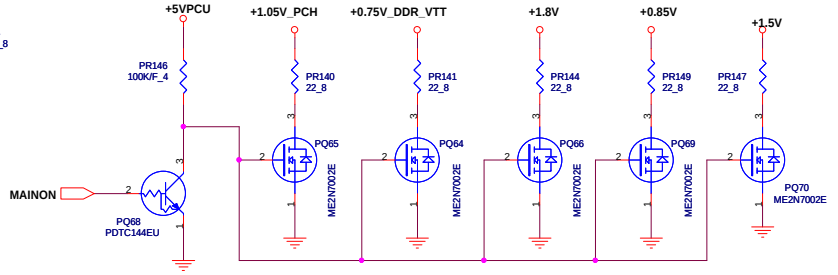
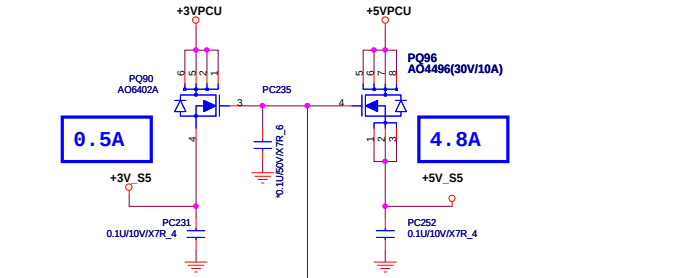
DISCHARGE

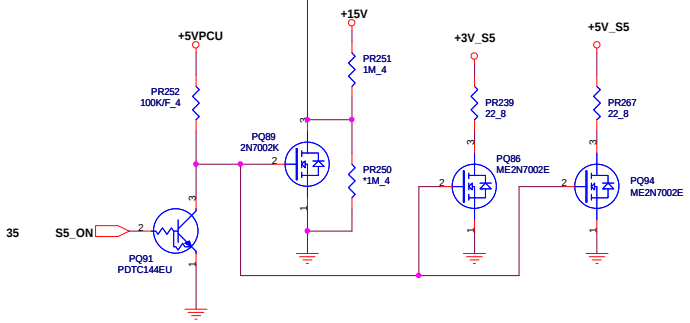
+3V, +5V,+1.5V

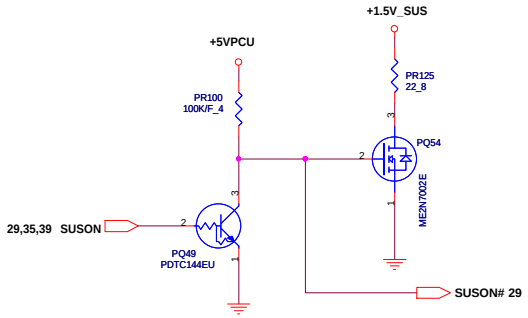




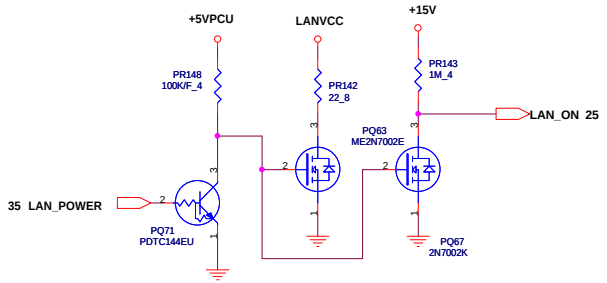
3V_S5, 5V_S5

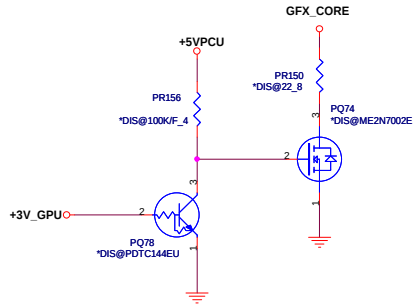






LANVCC





PROJECT : KL6A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

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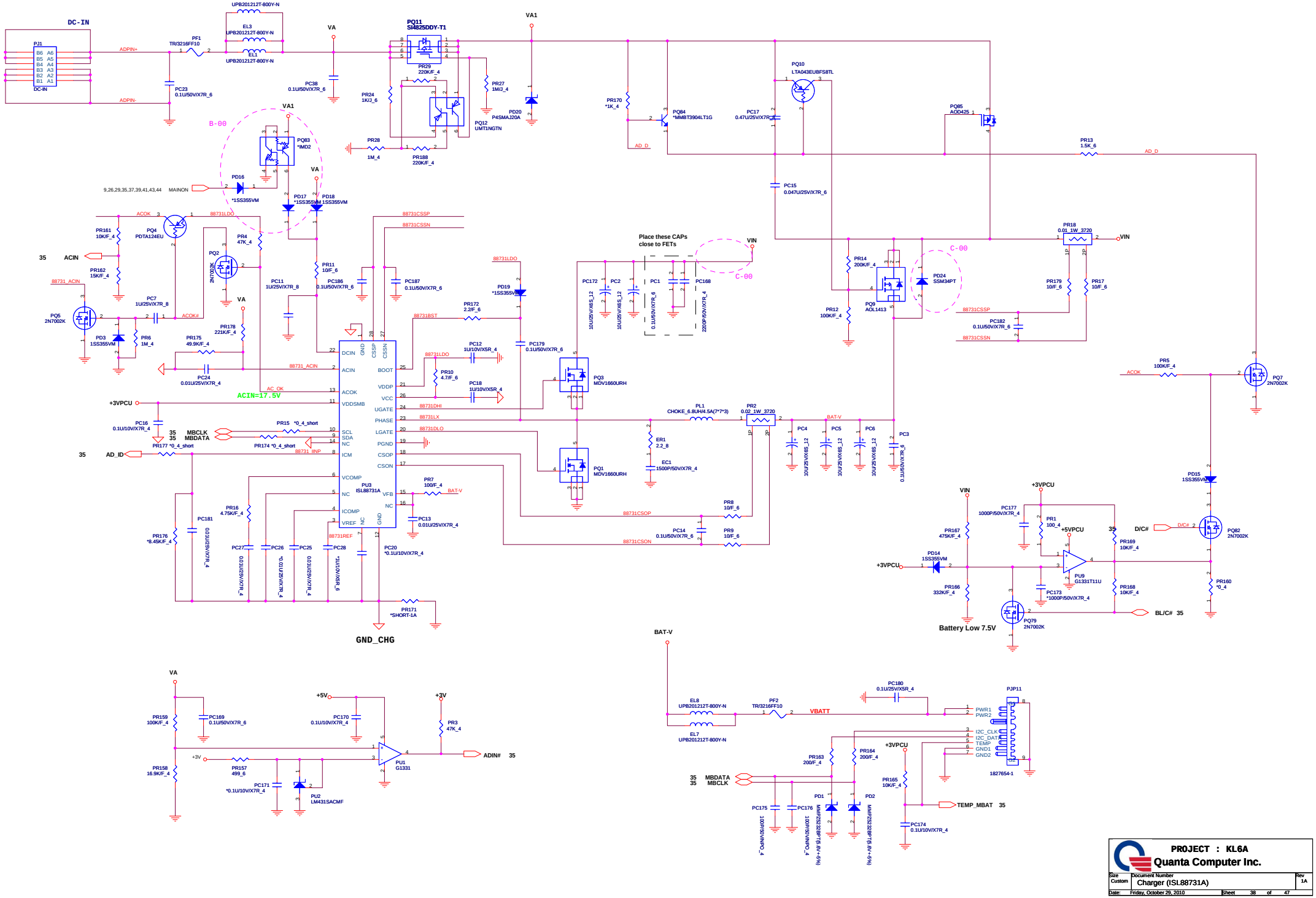
DC-IN
PJ1
DC-IN
ADPIN+
ADPIN-
PF1
TR/3216FF10
EL2
UPB201212T-800Y-N
EL3
UPB201212T-800Y-N
EL1
UPB201212T-800Y-N
PC23
0.1U/50V/X7R_6
PC38
0.1U/50V/X7R_6
VA
VA1
PQ11
SI4825DDY-T1
PR29
220K/F_4
PR24
1K/J_6
PR28
1M_4
PR188
220K/F_4
PR27
1M/J_4
PD20
P4SMAJ20A
PQ12
UMT1NGTN
PR170
*1K_4
PQ84
*MMBT3904LT1G
PQ10
LTA043EUBFS8TL
PC17
0.47U/25V/X7R_6
PQ85
AOD425
PR13
1.5K_6
AD_D
PC15
0.047U/25V/X7R_6
B-00
PQ83
*IMD2
PD16
*1SS355VM
PD17
*1SS355VM
PD18
1SS355VM
9,26,29,35,37,39,41,43,44
MAINON
ACOK
PR161
10K/F_4
PQ4
PDTA124EU
88731LDO
PR4
47K_4
PQ2
2N7002K
35
ACIN
PR162
15K/F_4
88731_ACIN
PQ5
2N7002K
PD3
1SS355VM
PR6
1M_4
PC7
1U/25V/X7R_8
ACOK#
PR178
221K/F_4
PR175
49.9K/F_4
PC24
0.01U/25V/X7R_4
PC11
1U/25V/X7R_8
PR11
10/F_6
PC186
0.1U/50V/X7R_6
88731CSSP
88731CSSN
PC187
0.1U/50V/X7R_6
PR172
2.2/F_6
88731BST
PD19
*1SS355VM
PC179
0.1U/50V/X7R_6
Place these CAPs
close to FETs
VIN
C-00
PC172
PC2
PC1
PC168
10U/25V/X6S_12
10U/25V/X6S_12
0.1U/50V/X7R_6
220P/50V/X7R_4
PR14
200K/F_4
PQ9
AOL1413
PD24
SSM34PT
PR12
100K/F_4
PR18
0.01_1W_3720
PR179
10/F_6
PR17
10/F_6
PC182
0.1U/50V/X7R_6
PR5
100K/F_4
PQ7
2N7002K
PC12
1U/10V/X5R_4
PR10
4.7/F_6
PC18
1U/10V/X5R_4
+3VPCU
PC16
0.1U/10V/X7R_4
35
MBCLK
35
MBDATA
PR15
*0_4_short
PR177 *0_4_short
PR174 *0_4_short
88731_IINP
35
AD_ID
ACIN=17.5V
AC_OK
88731DHI
88731LX
88731DLO
PQ3
MDV1660URH
PQ1
MDV1660URH
PL1
CHOKE_6.8UH/4.5A(7*7*3)
ER1
2.2_8
EC1
1500P/50V/X7R_4
PR2
0.02_1W_3720
BAT-V
PC4
PC5
PC6
PC3
10U/25V/X6S_12
10U/25V/X6S_12
10U/25V/X6S_12
0.1U/50V/X7R_6
PU3
ISL88731A
DCIN
ACIN
ACOK
VDDSMB
SCL
SDA
NC
ICM
VCOMP
NC
ICOMP
VREF
GND
CSSP
CSSN
BOOT
VDDP
VCC
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VFB
NC
GND
PR7
100/F_4
PC13
0.01U/25V/X7R_4
PR8
10/F_6
PR9
10/F_6
88731CSOP
88731CSON
PC14
0.1U/50V/X7R_6
PR16
4.75K/F_4
PR176
*8.45K/F_4
PC181
0.01U/25V/X7R_4
PC27
0.01U/25V/X7R_4
PC26
*0.01U/25V/X7R_4
PC25
0.01U/25V/X7R_4
PC28
*1U/10V/X5R_6
PC20
*0.1U/10V/X7R_4
88731REF
PR171
*SHORT-1A
GND_CHG
VIN
PC177
1000P/50V/X7R_4
PR167
475K/F_4
PD14
1SS355VM
PR166
332K/F_4
+3VPCU
PR1
100_4
+5VPCU
PU9
G1331T11U
PC173
*1000P/50V/X7R_4
35
D/C#
PR169
10K/F_4
PR168
10K/F_4
PD15
1SS355VM
PQ82
2N7002K
PR160
*0_4
BL/C# 35
PQ79
2N7002K
Battery Low 7.5V
VA
PR159
100K/F_4
PC169
0.1U/50V/X7R_6
PR158
16.9K/F_4
+3V
PR157
499_6
PC171
*0.1U/10V/X7R_4
+5V
PC170
0.1U/10V/X7R_4
PR3
47K_4
PU1
G1331
ADIN#
35
PU2
LM431SACMF
BAT-V
EL8
UPB201212T-800Y-N
EL7
UPB201212T-800Y-N
PF2
TR/3216FF10
VBATT
PC180
0.1U/25V/X5R_4
PJP11
PWR1
PWR2
I2C_CLK
I2C_DAT
TEMP
GND1
GND2
1827654-1
PR163
200/F_4
PR164
200/F_4
+3VPCU
PR165
10K/F_4
35
MBDATA
35
MBCLK
PC175
PC176
PD1
PD2
MMBZ5232BW-TG (6V~+5%)
MMBZ5232BW-TG (6V~+5%)
TEMP_MBAT
35
PC174
0.1U/10V/X7R_4
PROJECT : KL6A
Quanta Computer Inc.
Size
Custom
Document Number
Charger (ISL88731A)
Rev
1A
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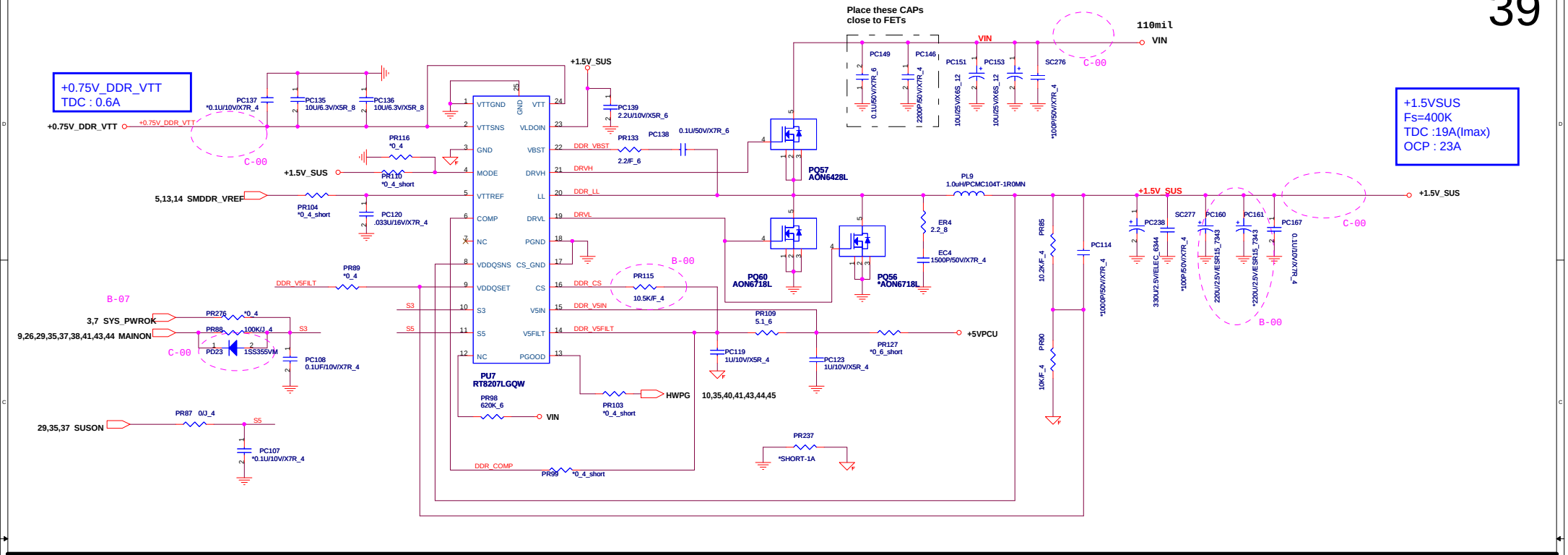
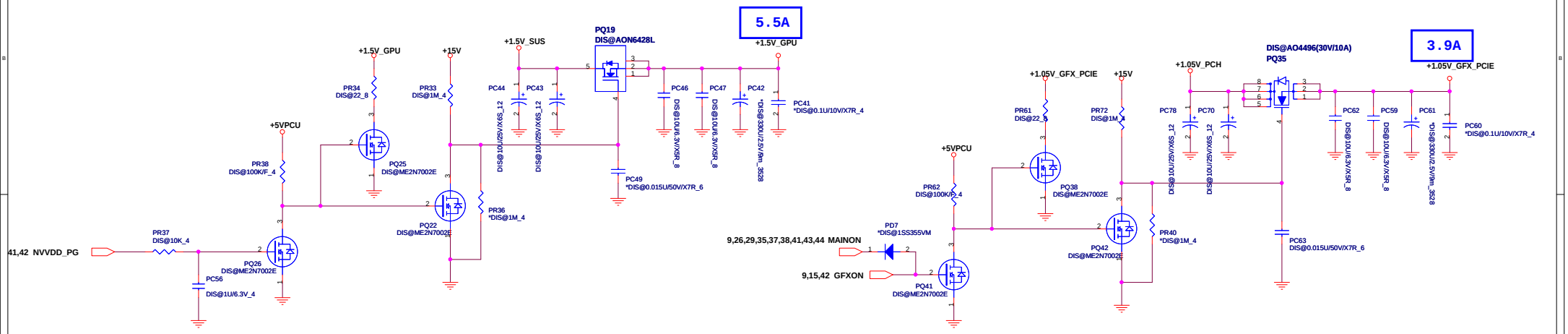
47





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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V(RT8207LGQW)	1A
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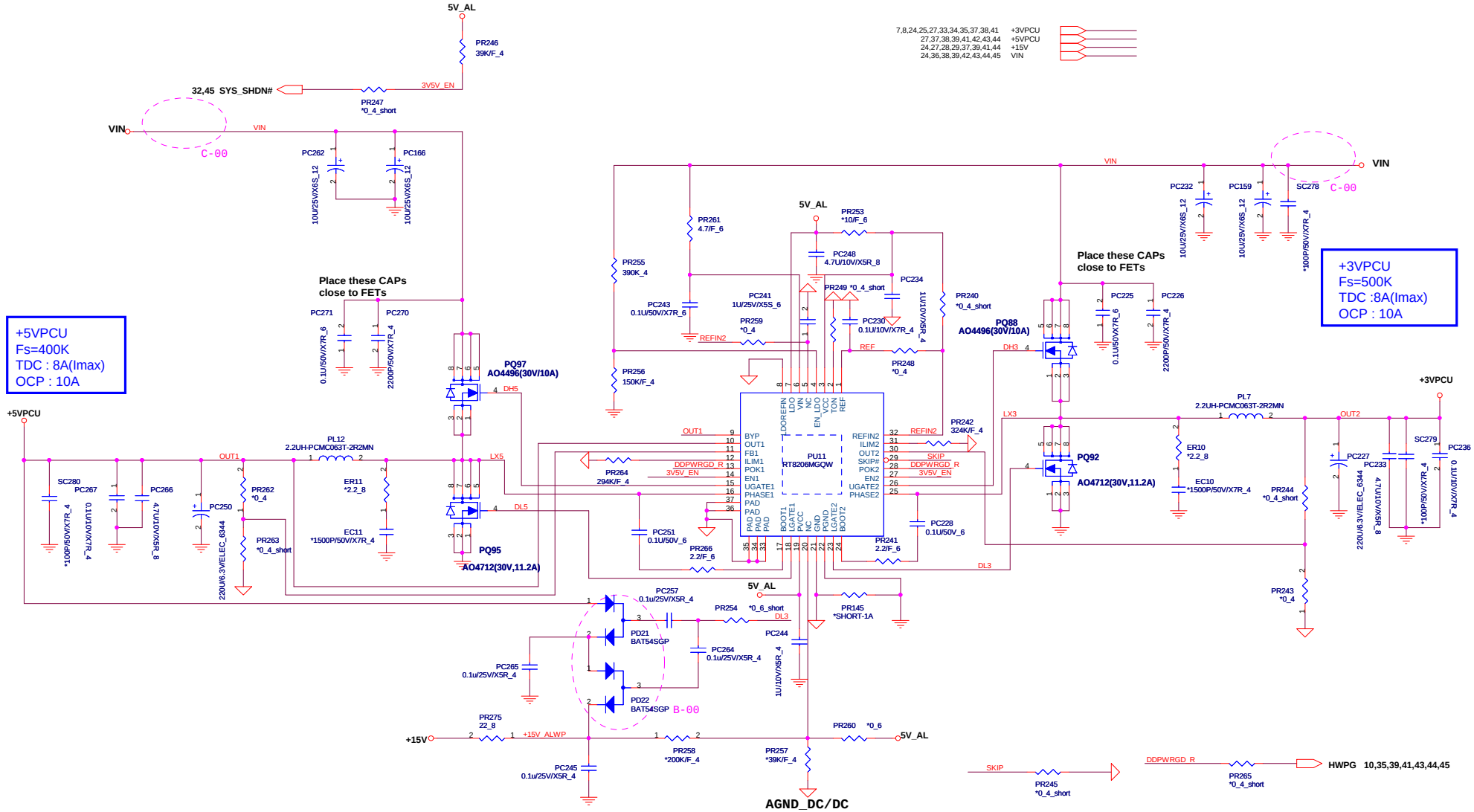

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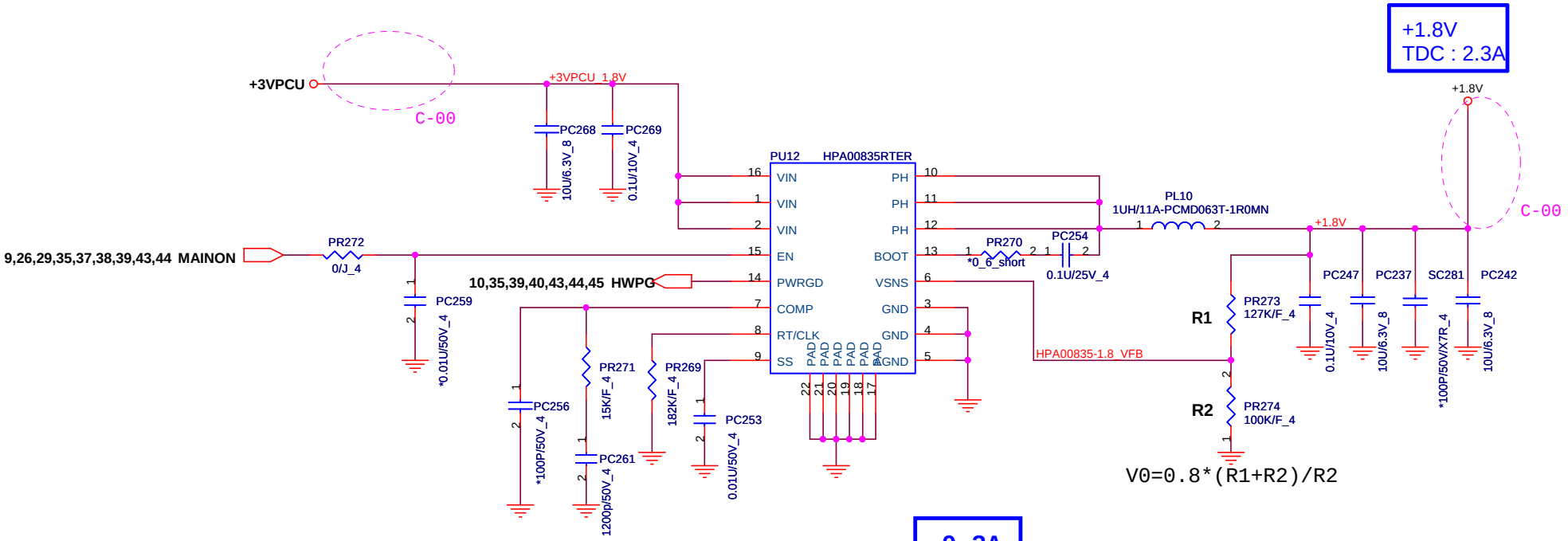
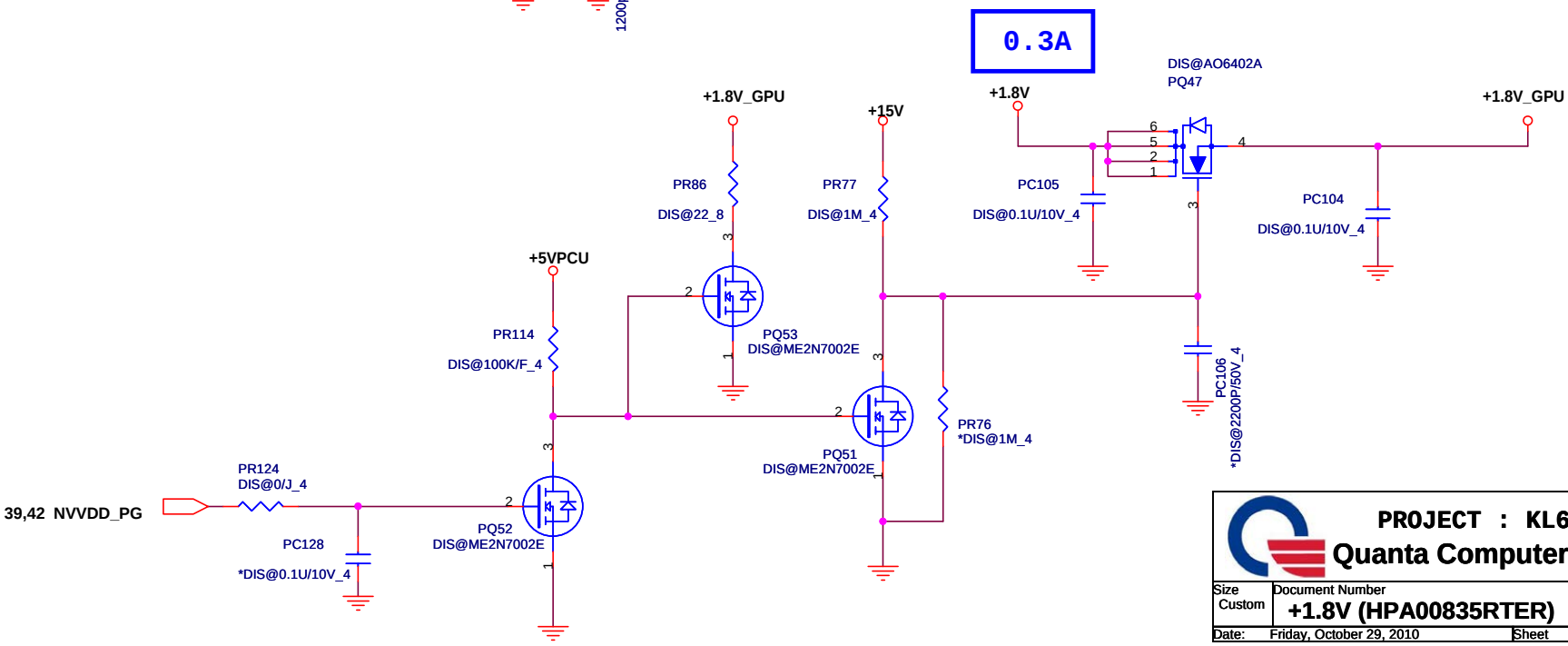
Quanta Computer Inc.	
Size: Custom	Document Number: 3V/5V (RT8206MGQW)
Rev: 1A	
Date: Friday, October 29, 2010	Sheet 40 of 47

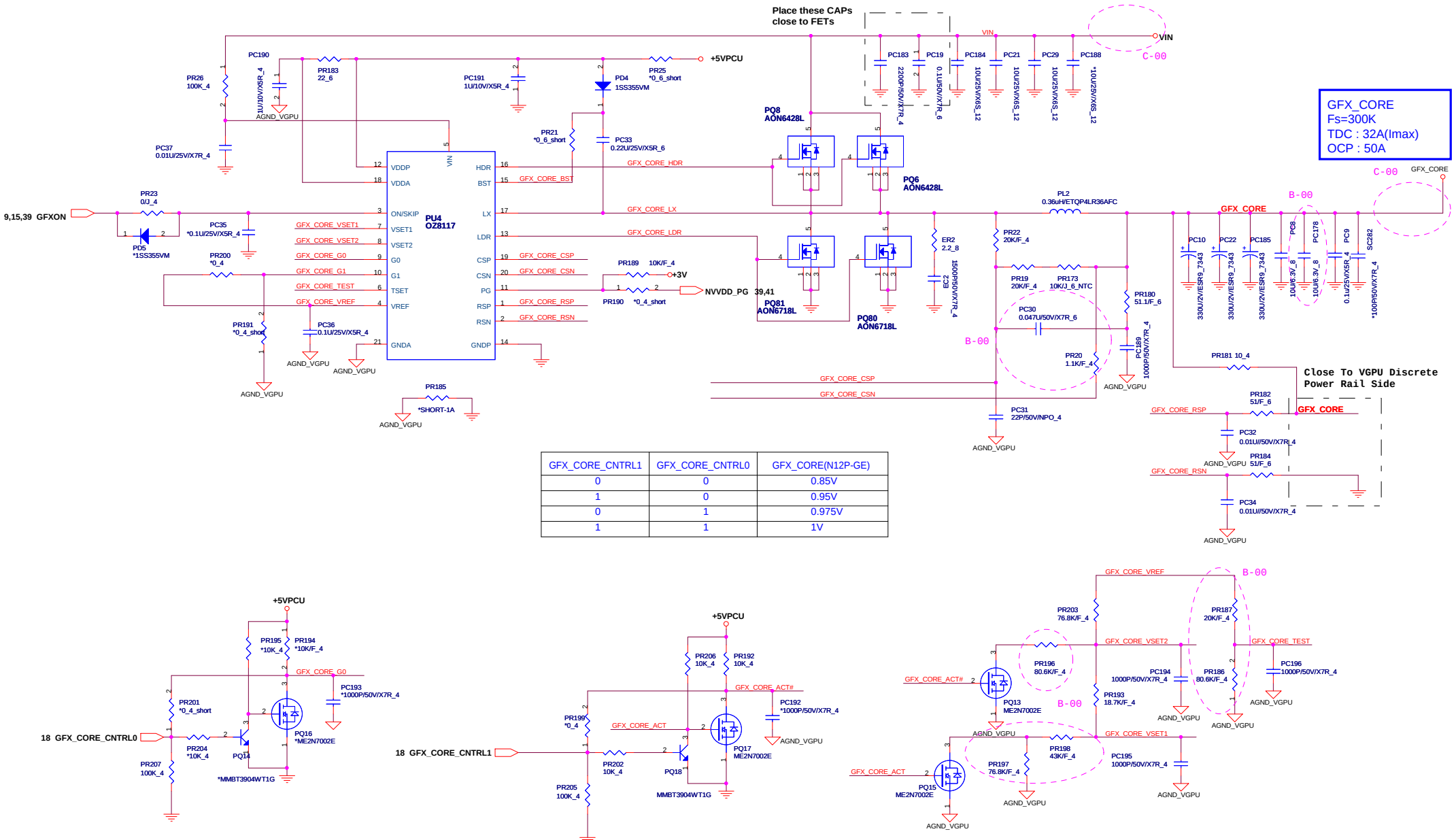




PROJECT : KL6A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.8V (HPA00835RTER)	1A
Date: Friday, October 29, 2010	Sheet 41 of 47	



GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	GFX_CORE(N12P-GE)
0	0	0.85V
1	0	0.95V
0	1	0.975V
1	1	1V

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Quanta Computer Inc.

Size	Document Number	Rev
	+VGPU_CORE (OZ8117)	1A

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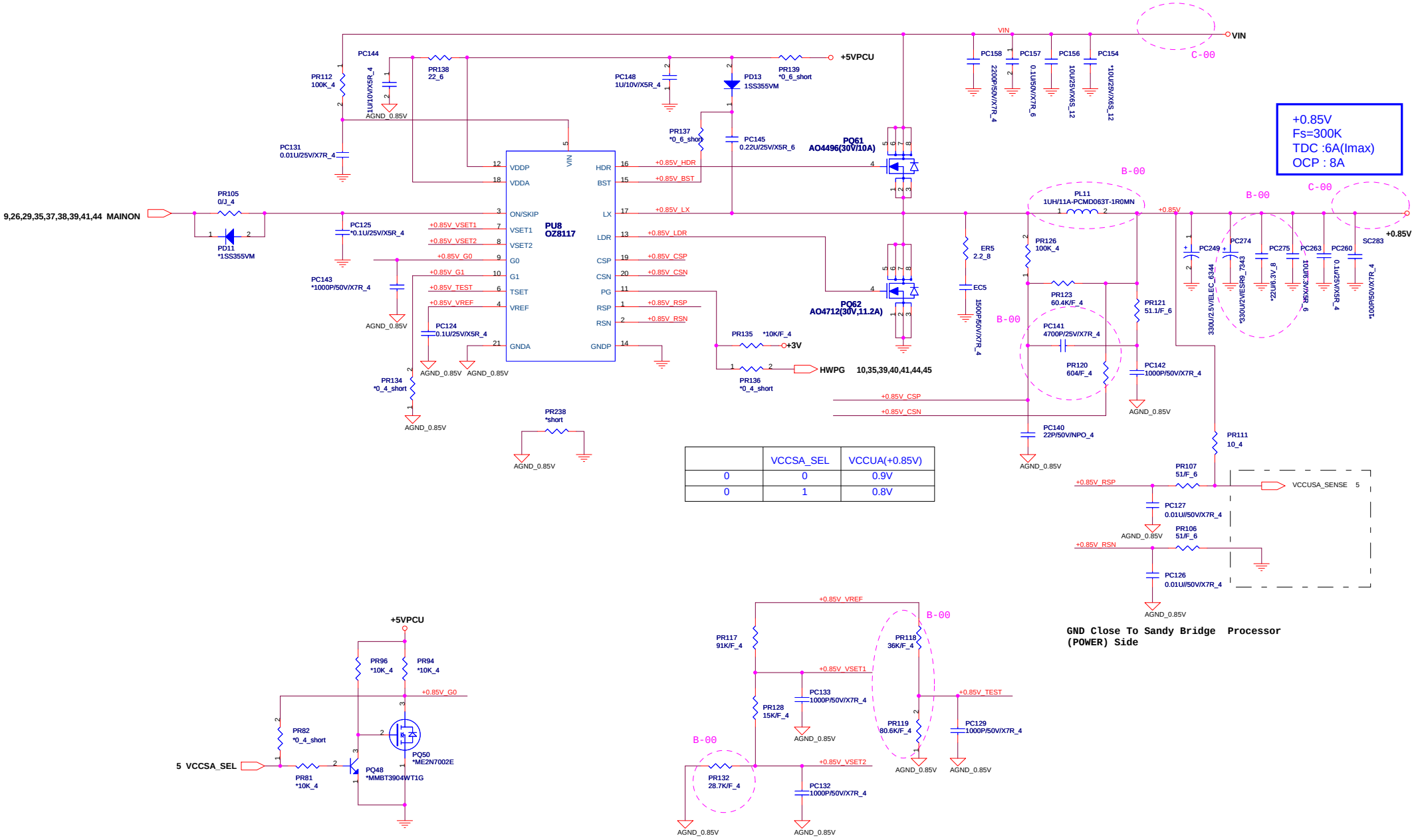

	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V

GND Close To Sandy Bridge Processor (POWER) Side

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Quanta Computer Inc.		
Size	Document Number: +0.85V (OZ8117)	Rev 1A
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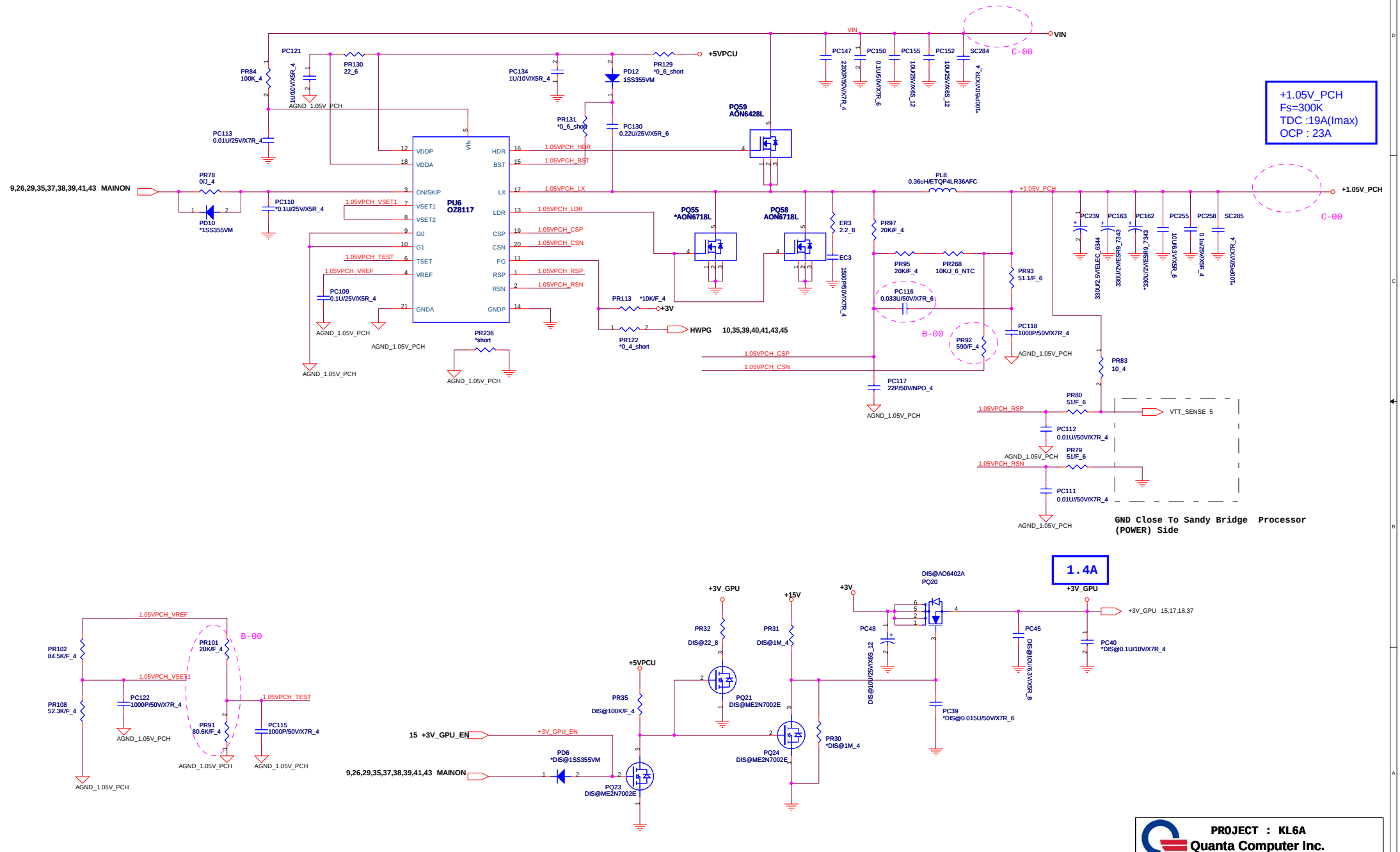
+1.05V_PCH
Fs=300K
TDC :19A(Imax)
OCP : 23A
PU6
OZ8117
PQ59
AON6428L
PQ55
*AON6718L
PQ58
AON6718L
PL8
0.36uH/ETQP4LR36AFC
VIN
+5VPCU
+1.05V_PCH
+3V
+3V_GPU
+15V
9,26,29,35,37,38,39,41,43 MAINON
HWPG 10,35,39,40,41,43,45
15 +3V_GPU_EN
1.4A
B-00
C-00
GND Close To Sandy Bridge Processor (POWER) Side
PROJECT : KL6A
Quanta Computer Inc.
+1.05_PCH (OZ8115)
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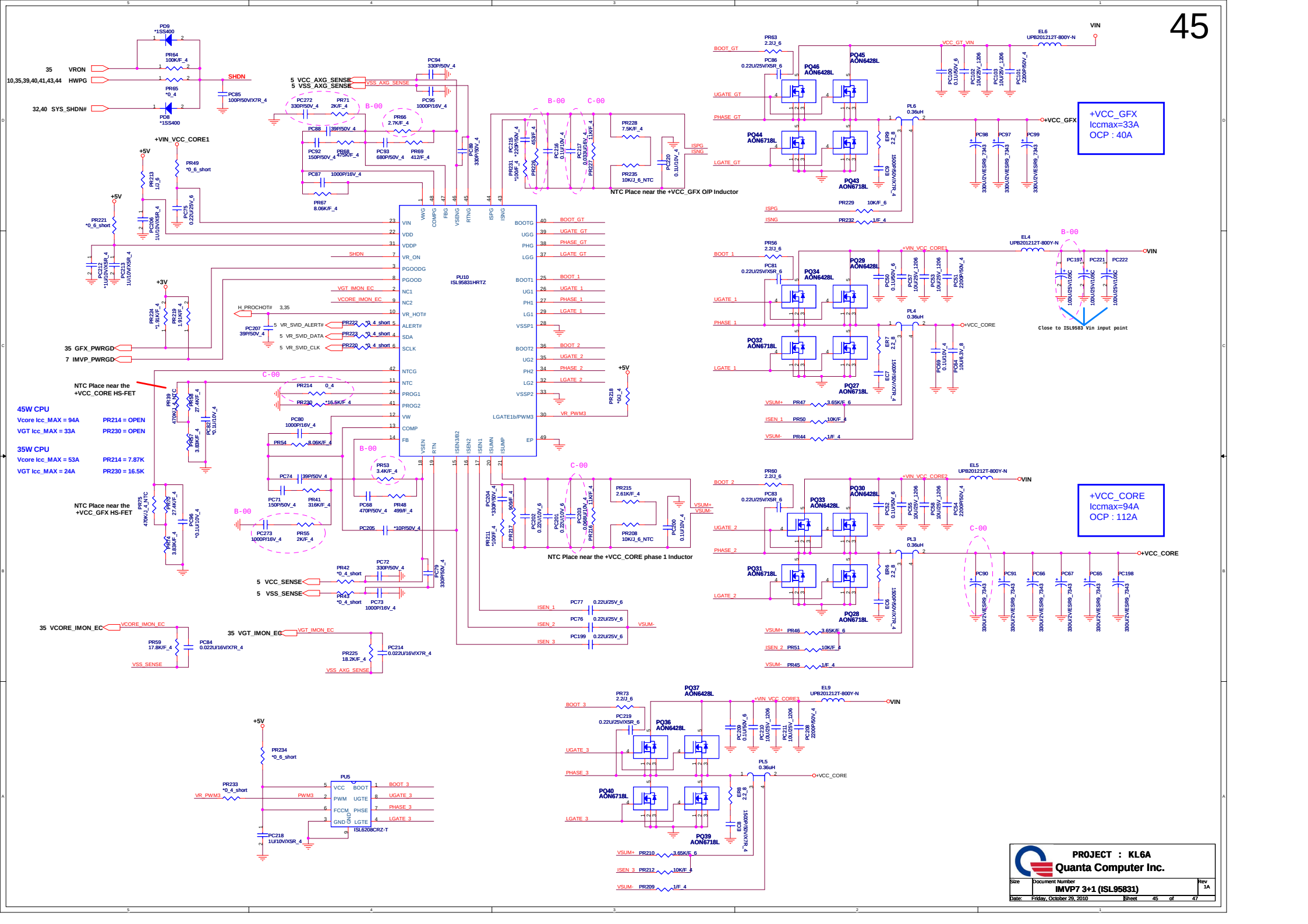
PU10
ISL95831HRTZ
VIN
VDD
VDDP
VR_ON
PGOODG
PGOOD
NC1
NC2
VR_HOT#
ALERT#
SDA
SCLK
NTCG
NTC
PROG1
PROG2
VW
COMP
FB
BOOTG
UGG
PHG
LGG
BOOT1
UG1
PH1
LG1
VSSP1
BOOT2
UG2
PH2
LG2
VSSP2
LGATE1b/PWM3
EP
VSEN
RTN
ISEN3/B2
ISEN2
ISEN1
ISUMN
ISUMP
VW
VSEN
RTN
ISPG
ISNG
COMP
FBG
VSENG
RTNG
SHDN
VGT_IMON_EC
VCORE_IMON_EC
H_PROCHOT#
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
VR_PWM3
BOOT_GT
UGATE_GT
PHASE_GT
LGATE_GT
BOOT_1
UGATE_1
PHASE_1
LGATE_1
BOOT_2
UGATE_2
PHASE_2
LGATE_2
BOOT_3
UGATE_3
PHASE_3
LGATE_3
VSUM+
VSUM-
ISEN_1
ISEN_2
ISEN_3
+VCC_GFX
Iccmax=33A
OCP : 40A
+VCC_CORE
Iccmax=94A
OCP : 112A
NTC Place near the +VCC_GFX O/P Inductor
NTC Place near the +VCC_CORE phase 1 Inductor
NTC Place near the +VCC_CORE HS-FET
NTC Place near the +VCC_GFX HS-FET
Close to ISL9583 Vin input point
45W CPU
Vcore Icc_MAX = 94A
VGT Icc_MAX = 33A
PR214 = OPEN
PR230 = OPEN
35W CPU
Vcore Icc_MAX = 53A
VGT Icc_MAX = 24A
PR214 = 7.87K
PR230 = 16.5K
PU5
ISL6208CRZ-T
PROJECT : KL6A
Quanta Computer Inc.
IMVP7 3+1 (ISL95831)
Friday, October 29, 2010
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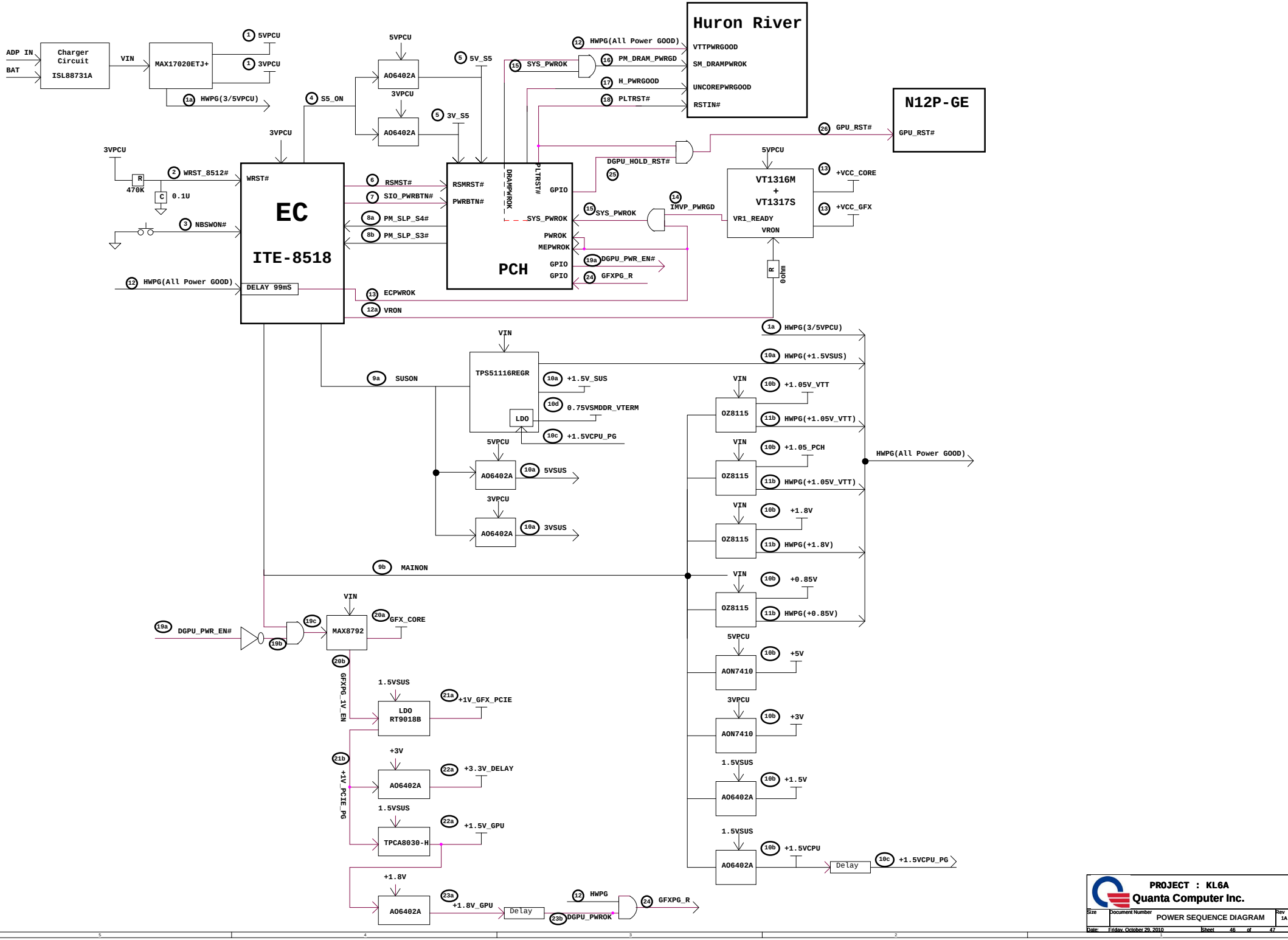
Huron River
VTTPWRGOOD
SM_DRAMPWROK
UNCOREPWRGOOD
RSTIN#
N12P-GE
GPU_RST#
ADP IN
BAT
Charger Circuit
ISL88731A
VIN
MAX17020ETJ+
5VPCU
3VPCU
HWPG(3/5VPCU)
S5_ON
AO6402A
5V_S5
3V_S5
HWPG(All Power GOOD)
SYS_PWROK
PM_DRAM_PWRGD
H_PWRGOOD
PLTRST#
GPU_RST#
DGPU_HOLD_RST#
R 470K
C 0.1U
WRST_8512#
NBSWON#
EC
ITE-8518
WRST#
DELAY 99mS
RSMST#
SIO_PWRBTN#
PM_SLP_S4#
PM_SLP_S3#
ECPWROK
VRON
RSMRST#
PWRBTN#
DRAMPWROK
PLTRST#
GPIO
SYS_PWROK
PWROK
MEPWROK
DGPU_PWR_EN#
GFXPG_R
PCH
IMVP_PWRGD
VT1316M + VT1317S
VR1_READY
VRON
+VCC_CORE
+VCC_GFX
R 0ohm
TPS51116REGR
LDO
SUSON
+1.5V_SUS
0.75VSMDDR_VTERM
+1.5VCPU_PG
5VSUS
3VSUS
OZ8115
+1.05V_VTT
+1.05_PCH
+1.8V
+0.85V
MAINON
MAX8792
GFX_CORE
DGPU_PWR_EN#
LDO RT9018B
+1V_GFX_PCIE
+3.3V_DELAY
TPCA8030-H
+1.5V_GPU
+1.8V_GPU
Delay
DGPU_PWROK
AON7410
+5V
+3V
+1.5V
+1.5VCPU
+1.5VCPU_PG
PROJECT : KL6A
Quanta Computer Inc.
POWER SEQUENCE DIAGRAM
Size
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KL6A / Z470 Huron River Schematic EC Tracking Record A (for SIV --> SIT,C)October 18, 2010

EC #	Page	CMVC #	Description	Date	Part Affected
C-00	1~46		Remove 0ohm resistor	1018	
C-01	9		Remov 27MHz from PCH	1018	
C-02	28,32, 34,36		Add capacitor for ESD/EMI suggestion	1018	

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Size	Document Number	Rev
Custom	EC Tracking Record A	1A

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