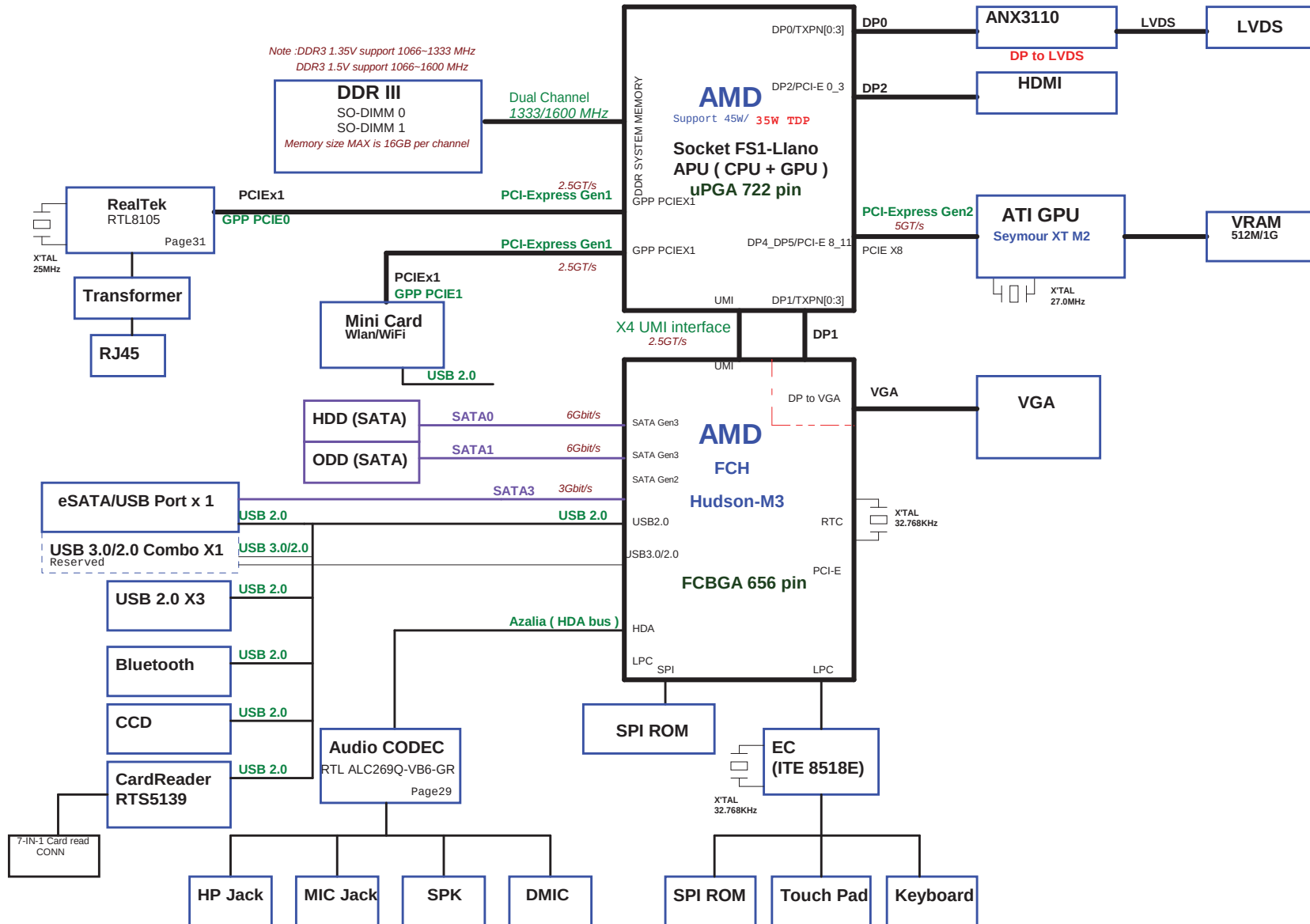


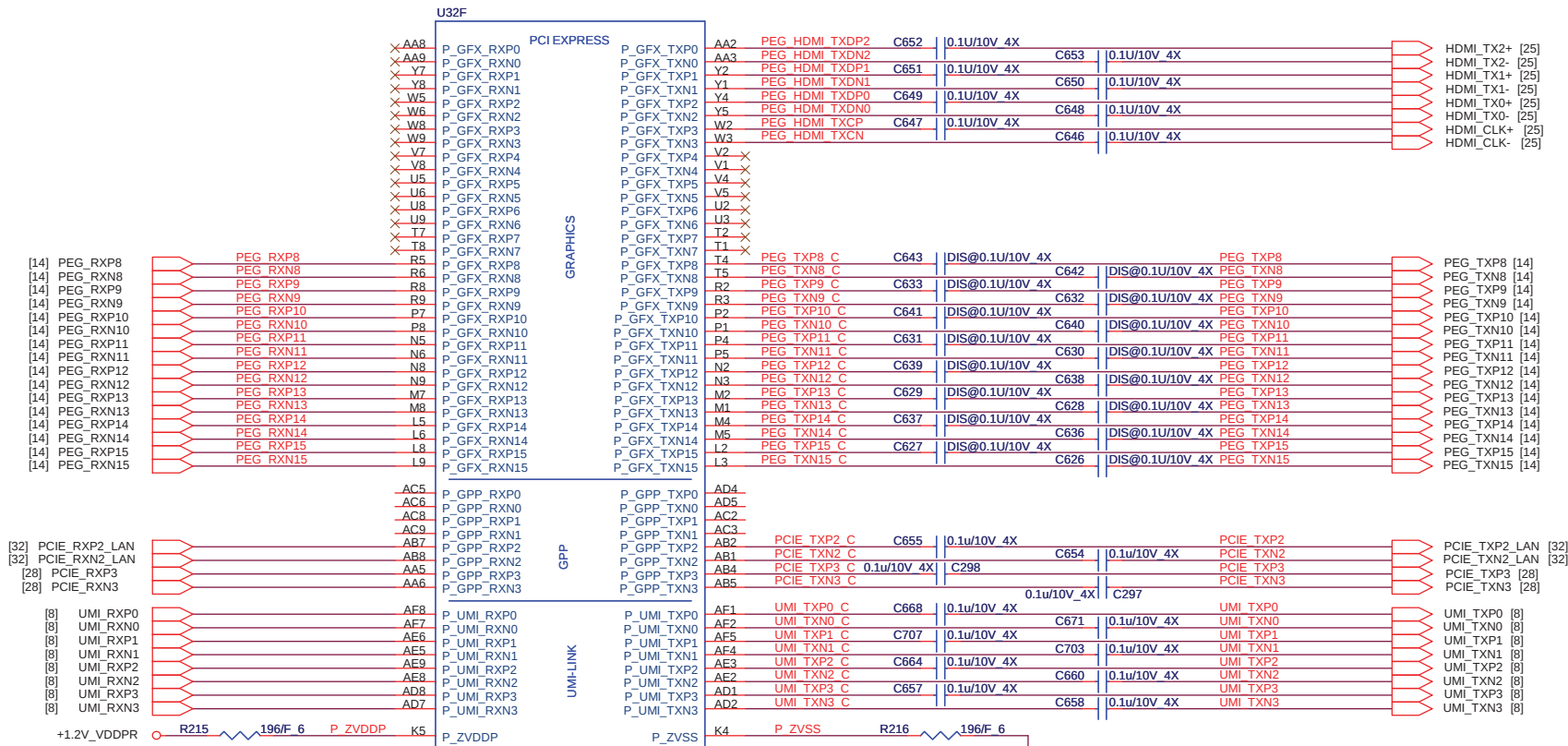
FAN /THERMAL
EMC2103-2
Page32

BLOCK DIAGRAM

Note :DP means Display Port Interface



Discharge	Page37
Charge	Page38
DDR3/0.75V (RT8207)	Page39
3V/5V (RT8206)	Page40
1.1V/+1.0V_GPU	Page41
+1.2V_VDDPR/+2.5	Page42
VDDI/VDDNB_CORE	Page43
GFX_CORE (OZ8117)	Page44
+1.8V_GPU (HFA00835RTER)	Page45

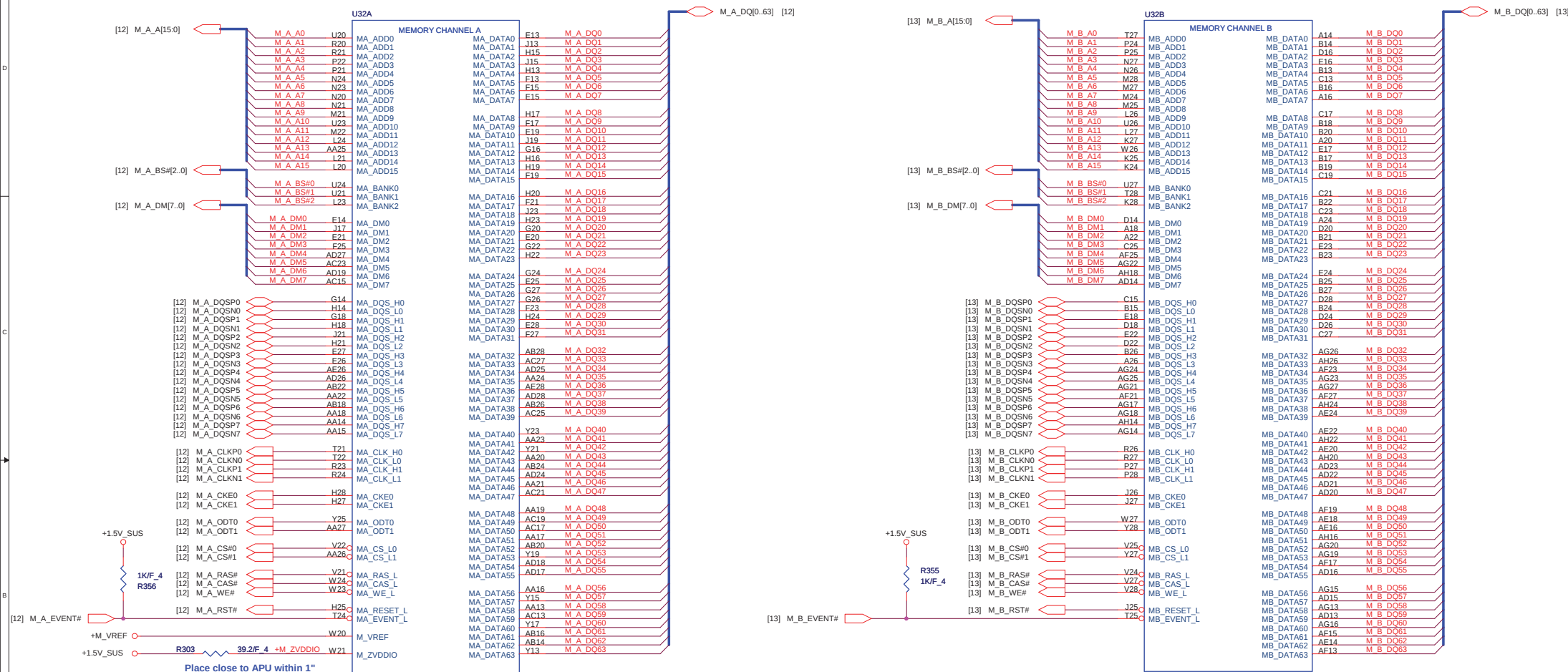


HDMI

P_GFX_TXP/N[3:0]
correspond to DisplayPort 2.

LAN
WLAN

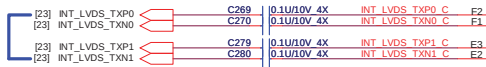
Liano APU



Liano APU

Liano APU

DP0 to LVDS

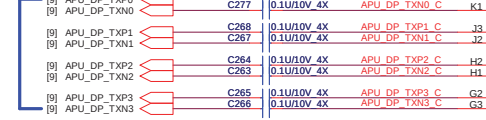


LVDS

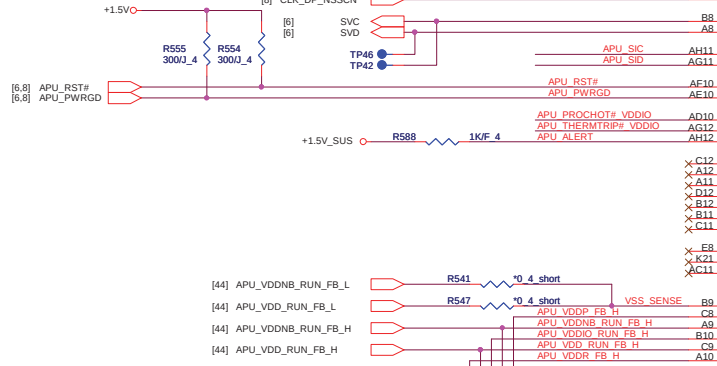
VGA

HDMI

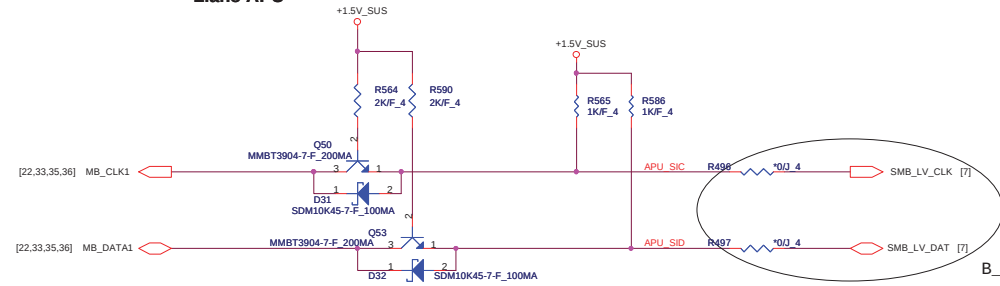
DP1 to Hudson-M3 VGA output



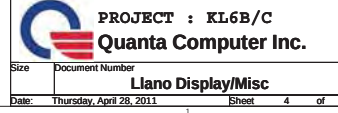
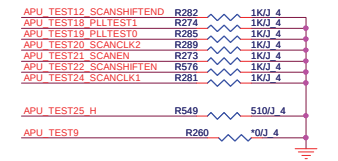
Note: CLK_APU_HCLKP/N is 100MHz SSC



Llano APU

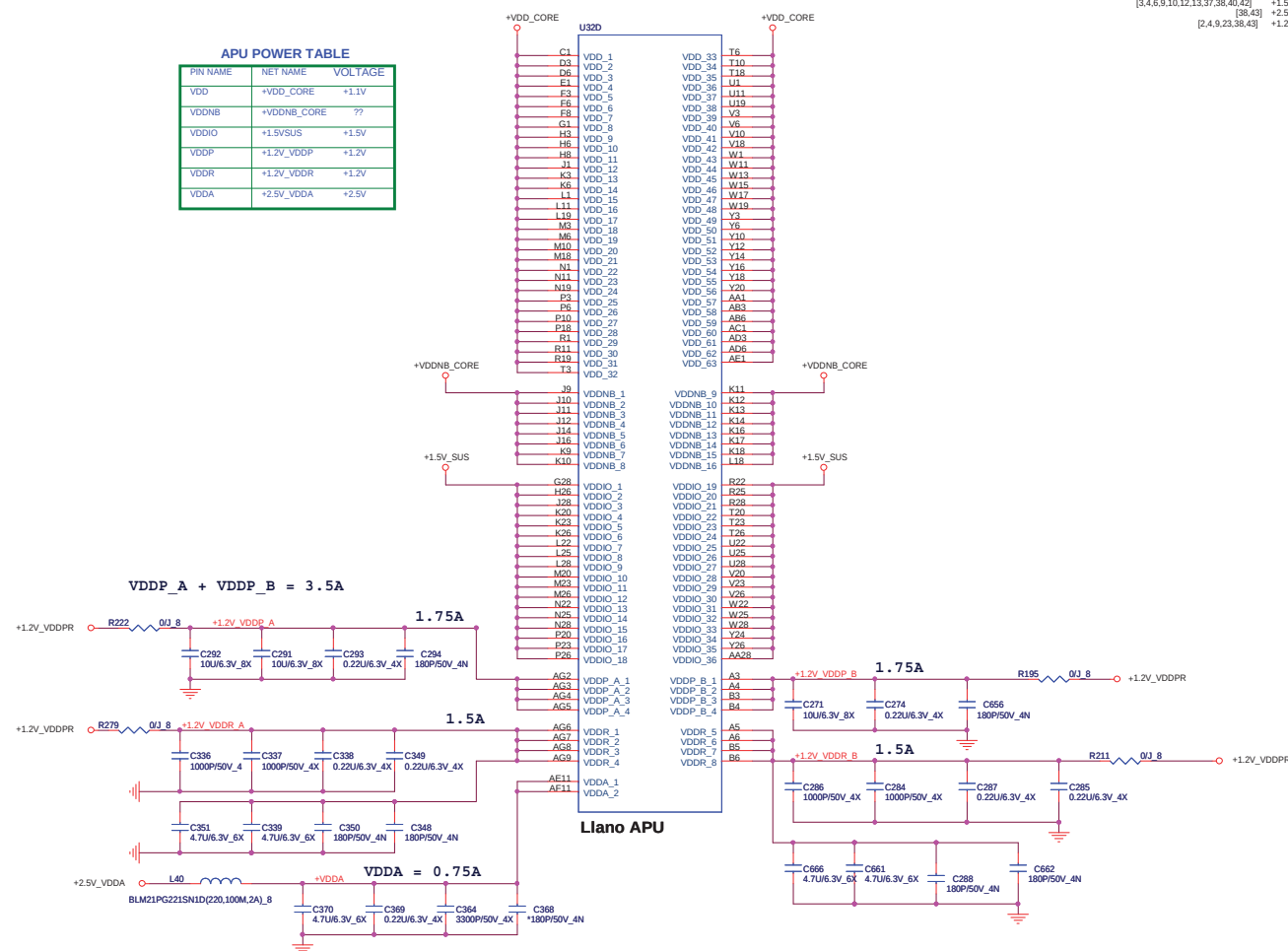


B_EC_05



APU POWER TABLE

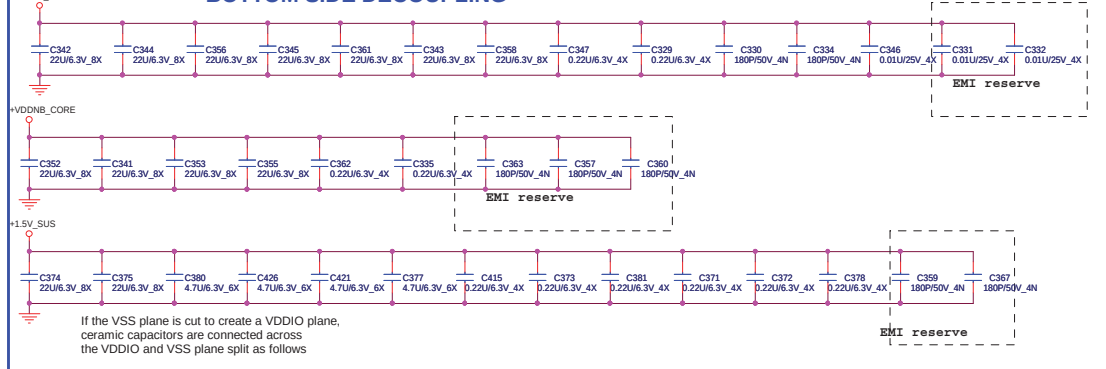
PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



U32E		
A7	VSS 1	VSS 75
A13	VSS 2	VSS 76
A15	VSS 3	VSS 77
A17	VSS 4	VSS 78
A19	VSS 5	VSS 79
A21	VSS 6	VSS 80
A23	VSS 7	VSS 81
A25	VSS 8	VSS 82
B7	VSS 9	VSS 83
C4	VSS 10	VSS 84
C10	VSS 11	VSS 85
C14	VSS 12	VSS 86
C16	VSS 13	VSS 87
C18	VSS 14	VSS 88
C20	VSS 15	VSS 89
C22	VSS 16	VSS 90
C24	VSS 17	VSS 91
C26	VSS 18	VSS 92
C28	VSS 19	VSS 93
C30	VSS 20	VSS 94
D15	VSS 21	VSS 95
D19	VSS 22	VSS 96
D21	VSS 23	VSS 97
D25	VSS 24	VSS 98
D27	VSS 25	VSS 99
E4	VSS 26	VSS 100
E10	VSS 27	VSS 101
E12	VSS 28	VSS 102
F9	VSS 29	VSS 103
F10	VSS 30	VSS 104
F11	VSS 31	VSS 105
F14	VSS 32	VSS 106
F16	VSS 33	VSS 107
F18	VSS 34	VSS 108
F20	VSS 35	VSS 109
F22	VSS 36	VSS 110
F24	VSS 37	VSS 111
F26	VSS 38	VSS 112
F28	VSS 39	VSS 113
F30	VSS 40	VSS 114
G4	VSS 41	VSS 115
G8	VSS 42	VSS 116
G13	VSS 43	VSS 117
G15	VSS 44	VSS 118
G17	VSS 45	VSS 119
G19	VSS 46	VSS 120
G21	VSS 47	VSS 121
G23	VSS 48	VSS 122
G25	VSS 49	VSS 123
J4	VSS 50	VSS 124
J18	VSS 51	VSS 125
J20	VSS 52	VSS 126
J22	VSS 53	VSS 127
J24	VSS 54	VSS 128
K19	VSS 55	VSS 129
L4	VSS 56	VSS 130
L7	VSS 57	VSS 131
L10	VSS 58	VSS 132
M0	VSS 59	VSS 133
M11	VSS 60	VSS 134
M19	VSS 61	VSS 135
N4	VSS 62	VSS 136
N7	VSS 63	VSS 137
N10	VSS 64	VSS 138
N18	VSS 65	VSS 139
N19	VSS 66	VSS 140
P11	VSS 67	VSS 141
P19	VSS 68	VSS 142
R4	VSS 69	VSS 143
R7	VSS 70	VSS 144
R10	VSS 71	VSS 145
R18	VSS 72	VSS 146
T9	VSS 73	VSS 147
	VSS 74	VSS 148
		VSS 149

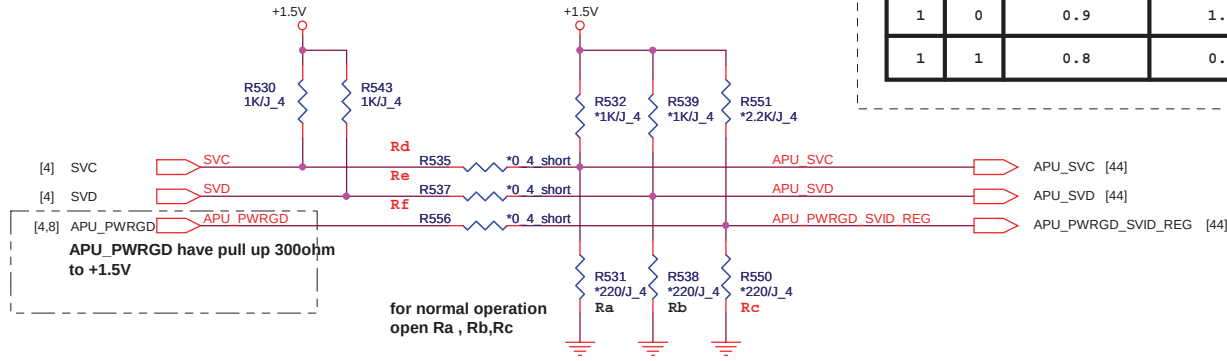
Liano APU

BOTTOM SIDE DECOUPLING

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

VID Override Circuit

Note:
To override VID, Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



BOOT VOLTAGE

SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

[4,8,9,23,25,28,29,42] +1.5V
[3,4,5,9,10,12,13,37,38,40,42] +1.5V_SUS



06

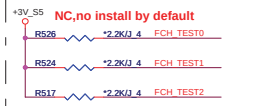
HDT+ Connector

Debug only

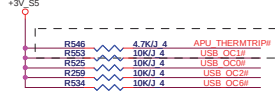
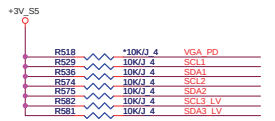
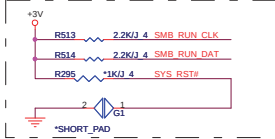


PROJECT : KL6B/C
Quanta Computer Inc.

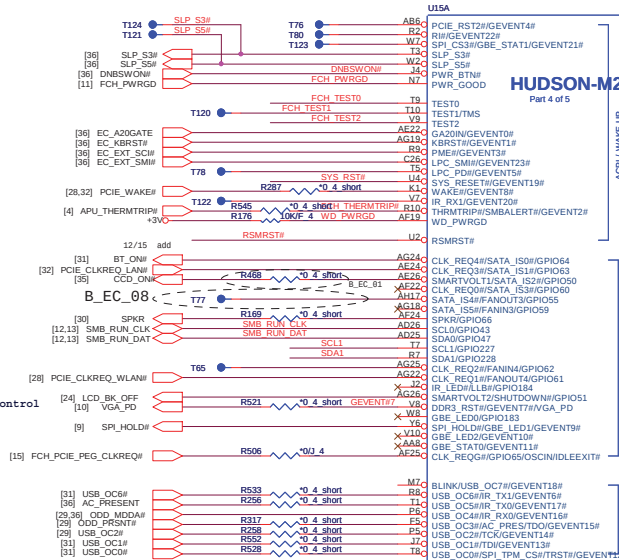
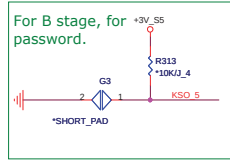
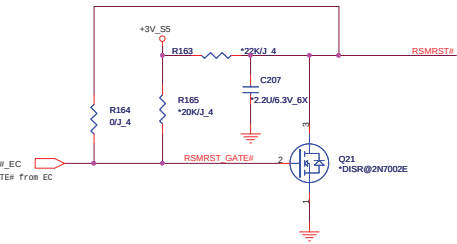
Size	Document Number	Rev 1A
Date:	Thursday, April 28, 2011	Sheet 6 of 49



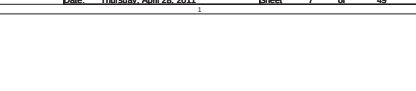
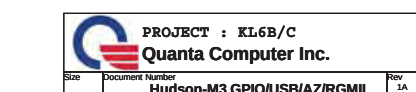
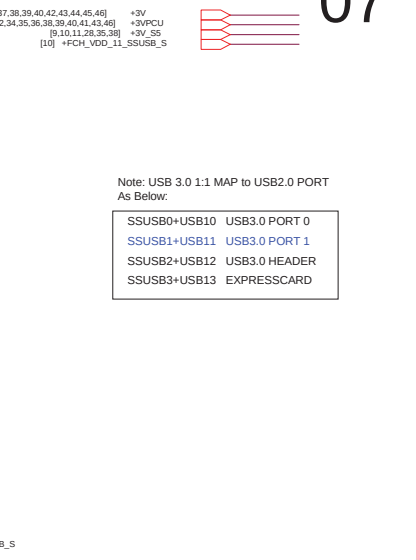
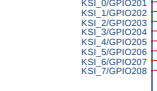
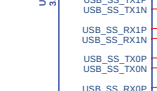
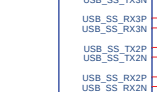
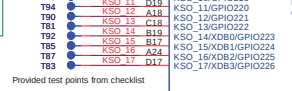
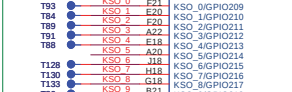
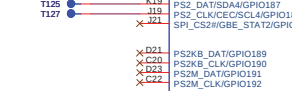
remove pull hi
(chip internal
have pull hi)



Note: LLB#, WAKE# and PWR_BTN need pull up to 3.3V_55+ only if 55+ mode is supported



HD audio
interface is
+3V_95 voltage



Note: USB 3.0 1:1 MAP to USB2.0 PORT
As Below:

SSUSB0+USB10 USB3.0 PORT 0
SSUSB1+USB11 USB3.0 PORT 1
SSUSB2+USB12 USB3.0 HEADER
SSUSB3+USB13 EXPRESSCARD

EC_A_10

Blue Tooth

WLAN

CCD

ESATA

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

USB 3.0 x1

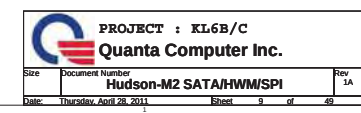
USB 3.0 x1

USB 3.0 x1

PROJECT : KL6B/C
Quanta Computer Inc.

Size Document Number
Hudson-M3 GPIO/USB/AZ/RGMII

Date: Thursday, April 28, 2011 Sheet 7 of 49



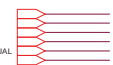


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

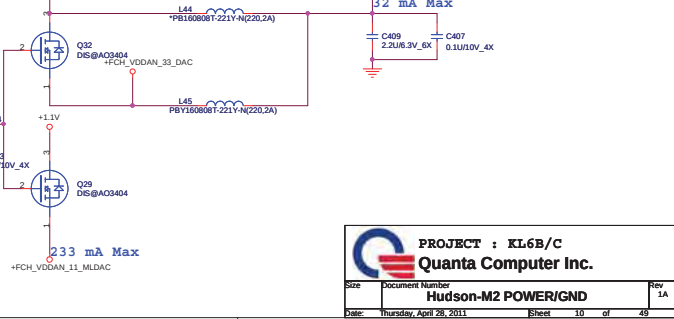
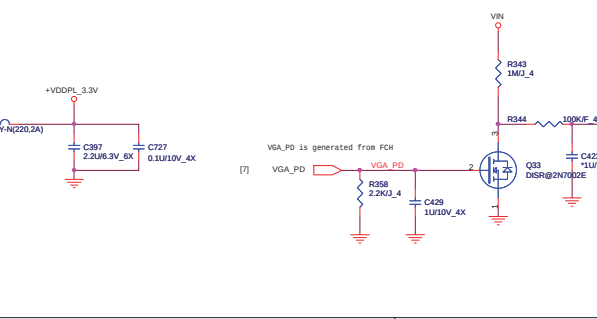
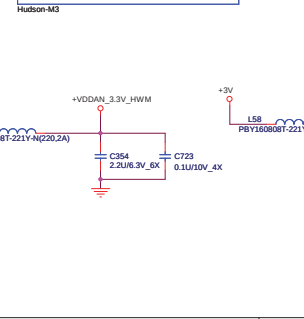
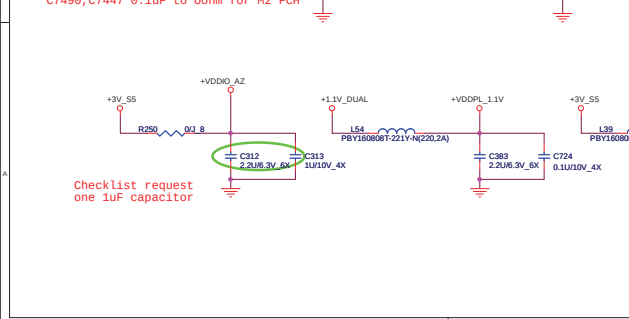
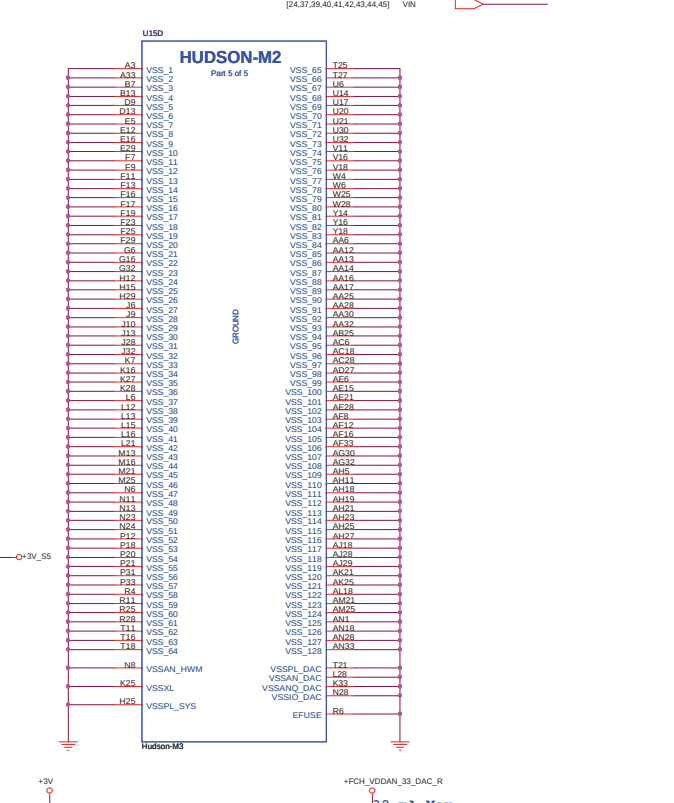
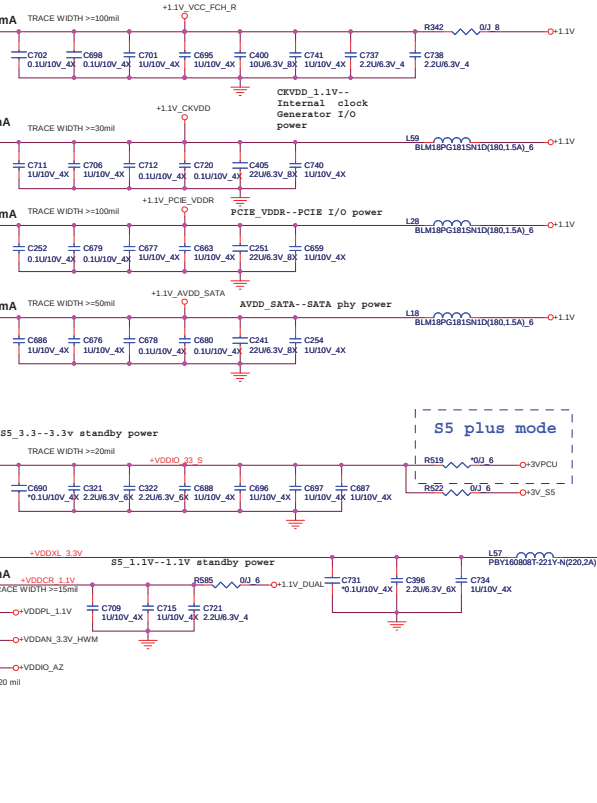
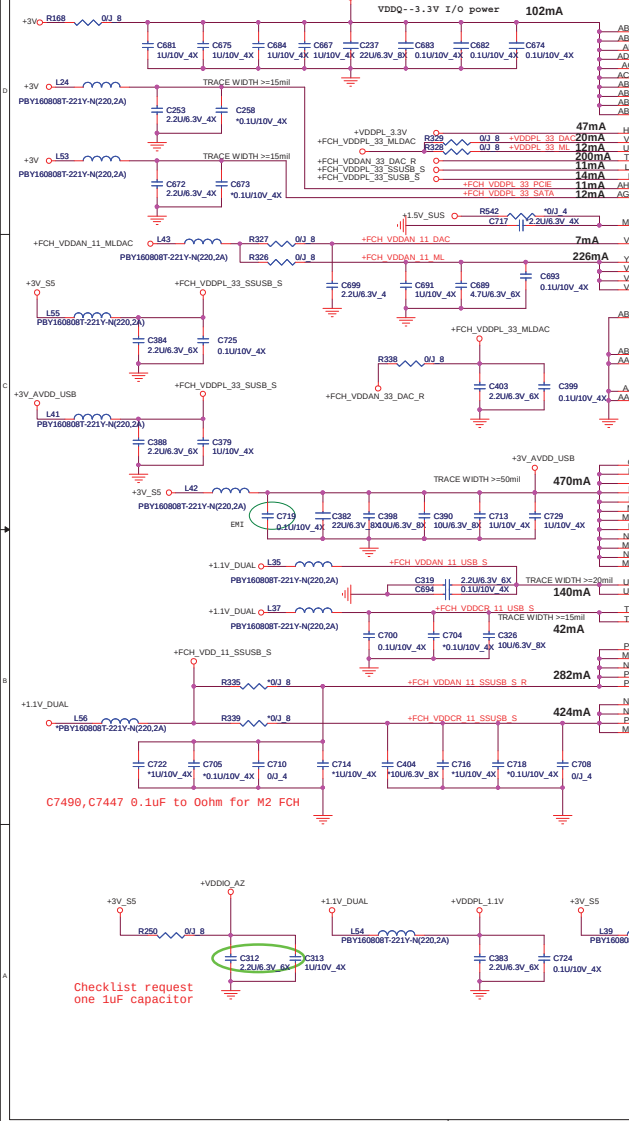
VDD-- S/B CORSE power

[4,6,7,8,9,11,12,13,19,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46]
[4,8,24,29,32,34,35,36,38,39,40,41,43,44]
[7,9,11,28,35,38]
[24,37,39,40,41,42,43,44,45]

+3V
+1.1V
+3VPCU
+3V_S5
+1.1V_DUAL
VH



10



C7490,C7447 0.1uF to 0ohm for M2 FCH

Checklist request one 1uF capacitor

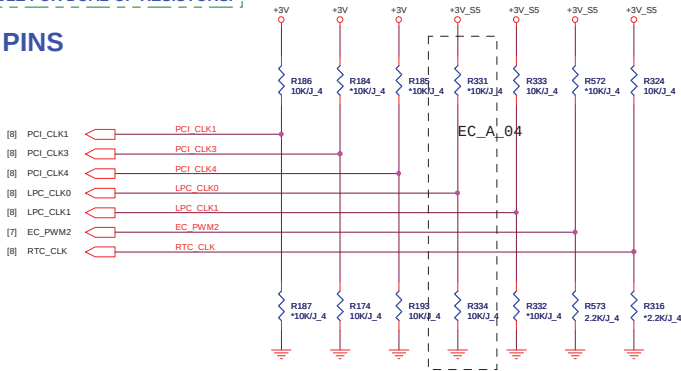
VGA_PD is generated from FCH

233 mA Max

PROJECT : KL6B/C
Quanta Computer Inc.
Size Document Number Hudson-M2 POWER/GND Rev 1A
Date: Thursday, April 28, 2011 Sheet 10 of 49

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

STRAPS PINS

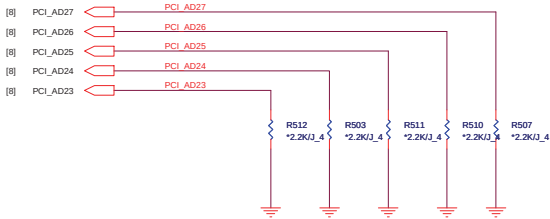


REQUIRED STRAPS

	*****	PCI_CLK1	*****	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
	PULL HIGH	ALLOW PCIE Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	*****	FORCE PCIE Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

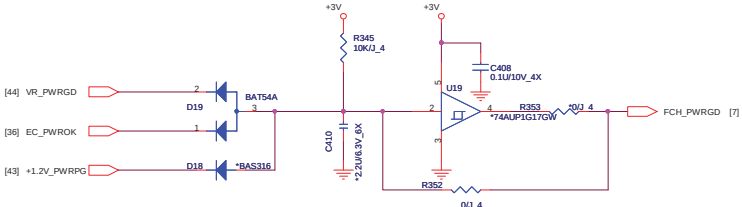
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

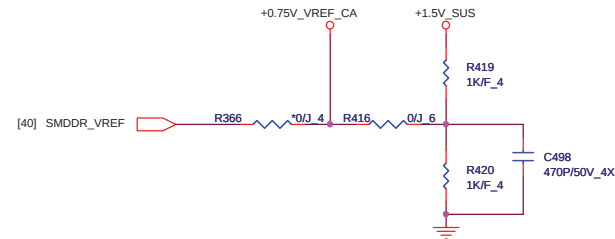


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

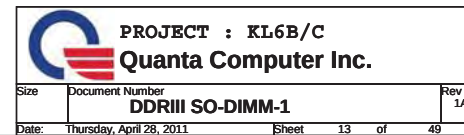
[4,6,7,8,9,10,12,13,19,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46] +3V [7,9,10,28,35,38] +3V_S5



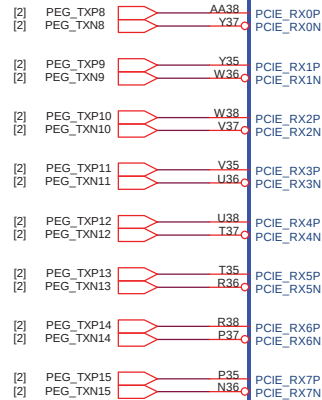
FCH PWRGD CKT



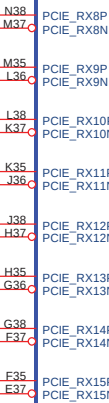
13



5GT/s bit rate

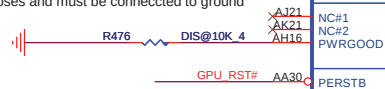


U30A



CLK_PCIE_VGAP
CLK_PCIE_VGAN

For M97 only Madison and Park the PWRGOOD ball is for test purposes and must be connected to ground



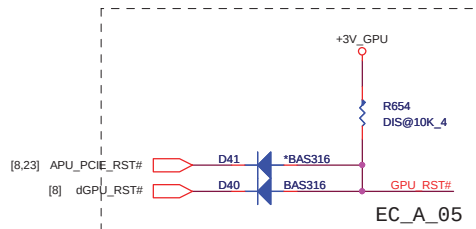
DIS@Seymour_M2

PCI EXPRESS INTERFACE

CALIBRATION



[15,17,18,38,40] +1V_GPU



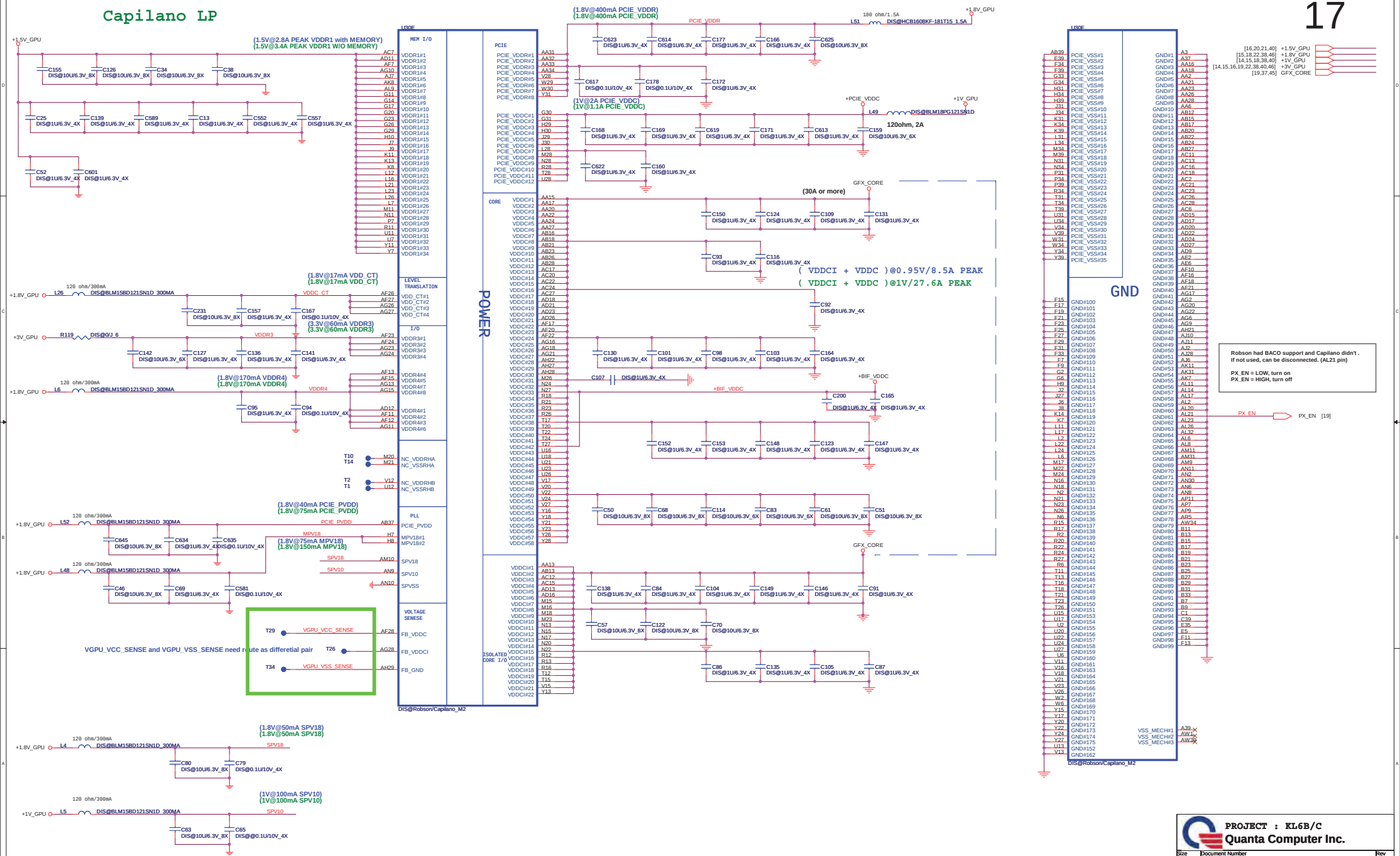


16



Robson PRO
Capilano LP

17

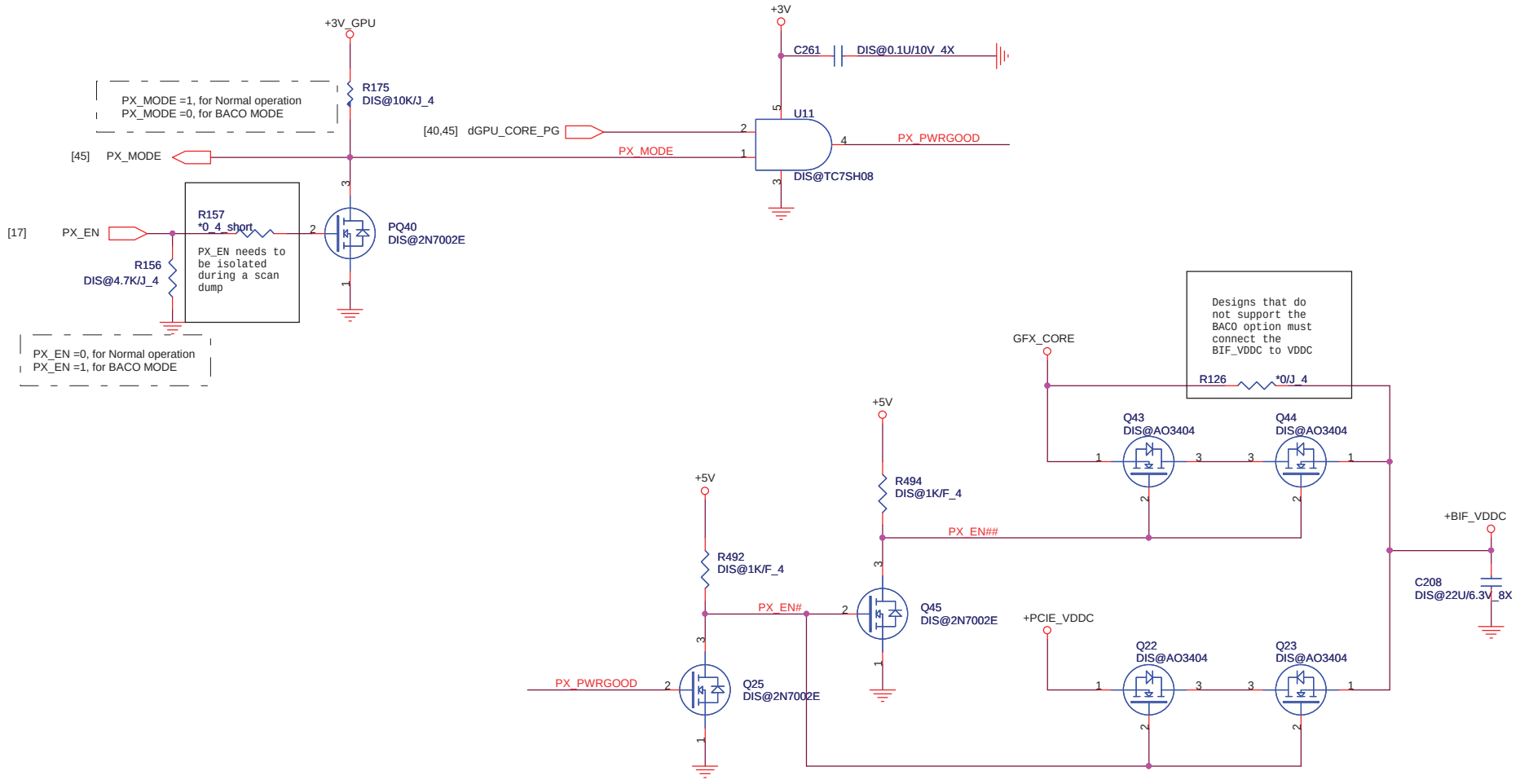




[4,6,7,8,9,10,11,12,13,23,24,25,26,27,28,29,30,31,32,33,35,36,37,38,39,40,42,43,44,45,46]
 [9,23,25,26,29,30,33,34,35,36,37,38,39,44]
 [14,15,16,17,22,38,40,46]
 [17,37,45]

+3V
 +5V
 +PCIE_VDDC
 +3V_GPU
 GFX_CORE

19



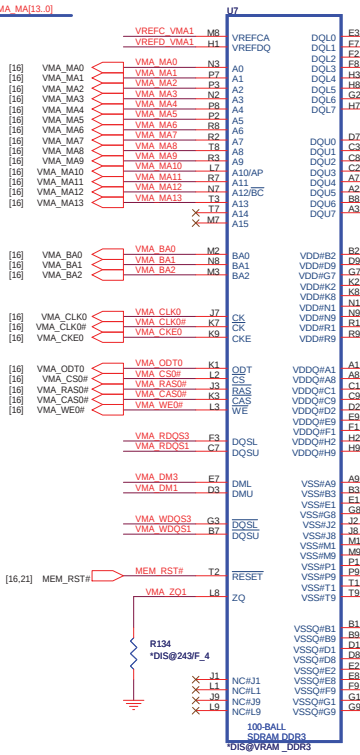
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

20

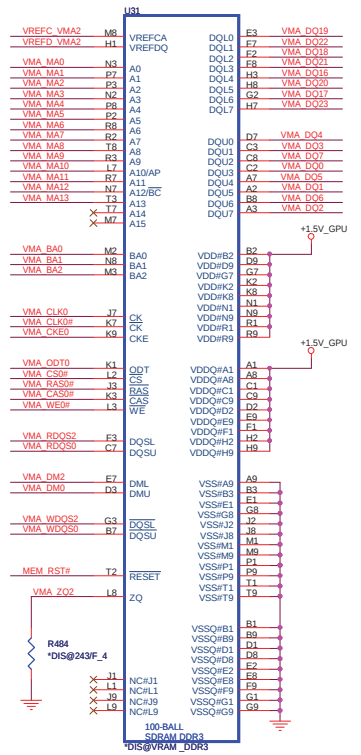
[16] VMA_DQ[63..0] VMA_DM[7..0] VMA_RDQS[7..0] VMA_WDQS[7..0] VMA_MA[13..0]

QSA[7..0] QSA[7..0]

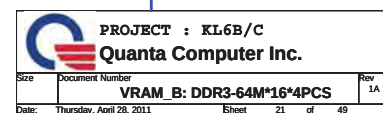
[16,17,21,40] +1.5V_GPU

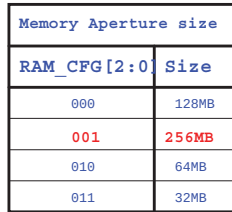


TOP Left



21





ROM Table		
HSYNC	VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

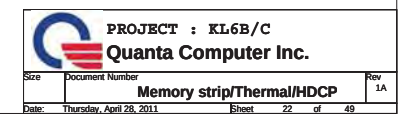
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

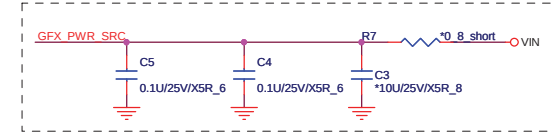
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONXY M2SP10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	1	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1]	HSYNC	AUD[1:0] 00: NO AUDIO FUNCTION.		
AUD[0]	VSYNC	01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

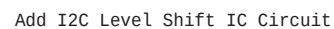


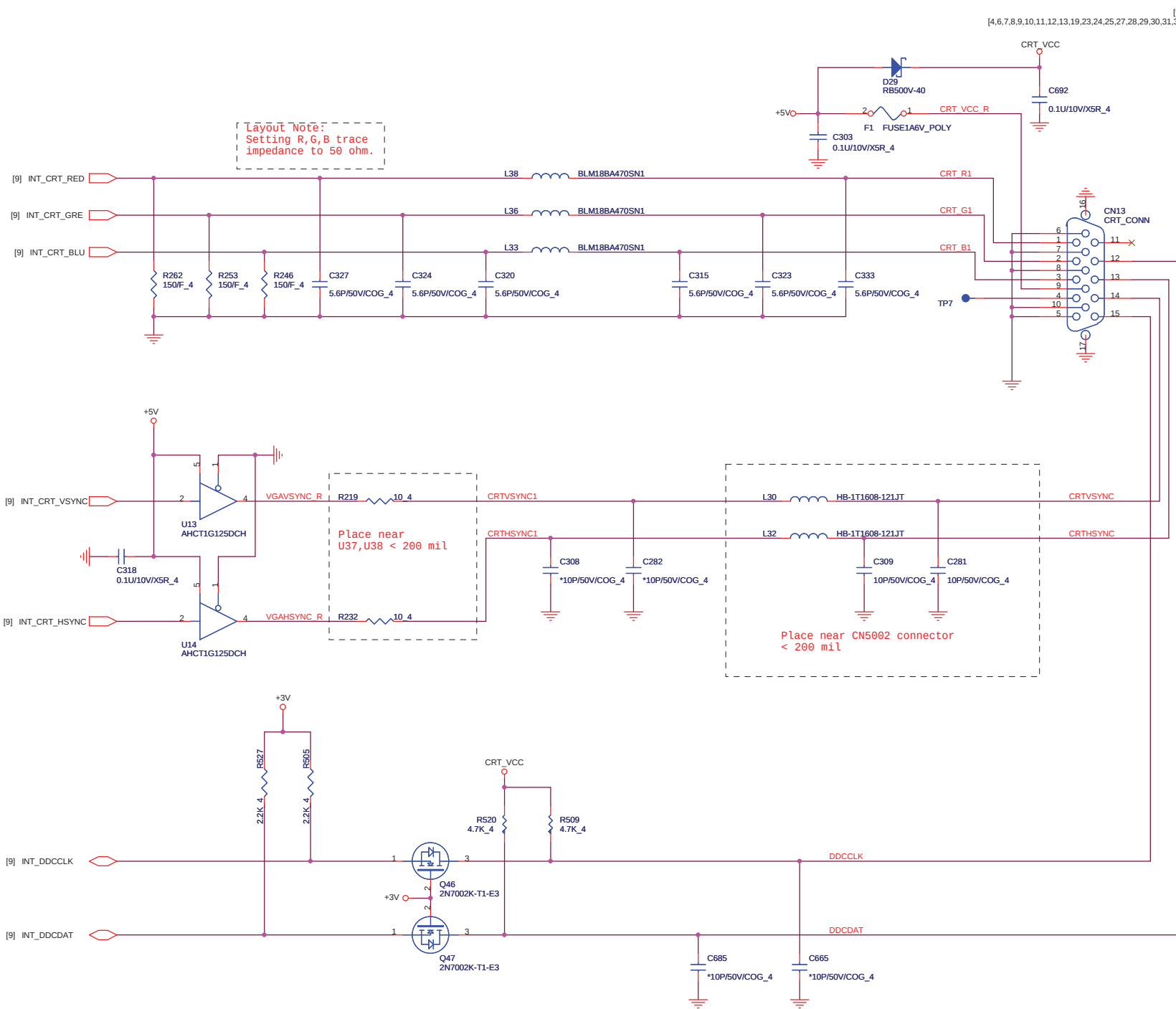
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63DFR -11C	AKD5LZWWT02 (64M*16-1Gb)	512MB	0	0	1	0	0	1
	H5TQ2G63BFR -11C	AKD5MGWTW00 (128M*16-1Gb)	1GB	0	0	0	0	0	1
Samsung	K4W1G1646G -BC11	AKD5EGGT500 (64M*16-1Gb)	512MB	0	0	1	1	0	1
	K4W2G1646C -HC11	AKD5MGWT500 (128M*16-1Gb)	1GB	0	0	0	1	0	1

+1.8V_GPU

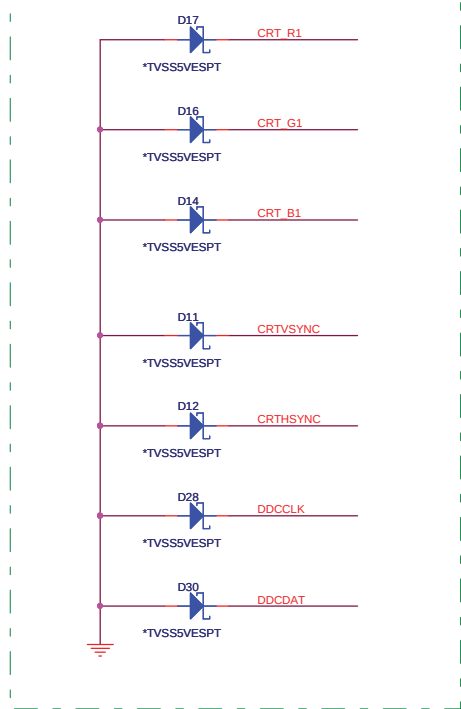


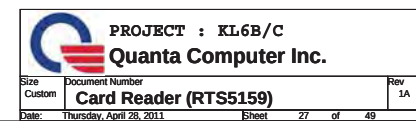




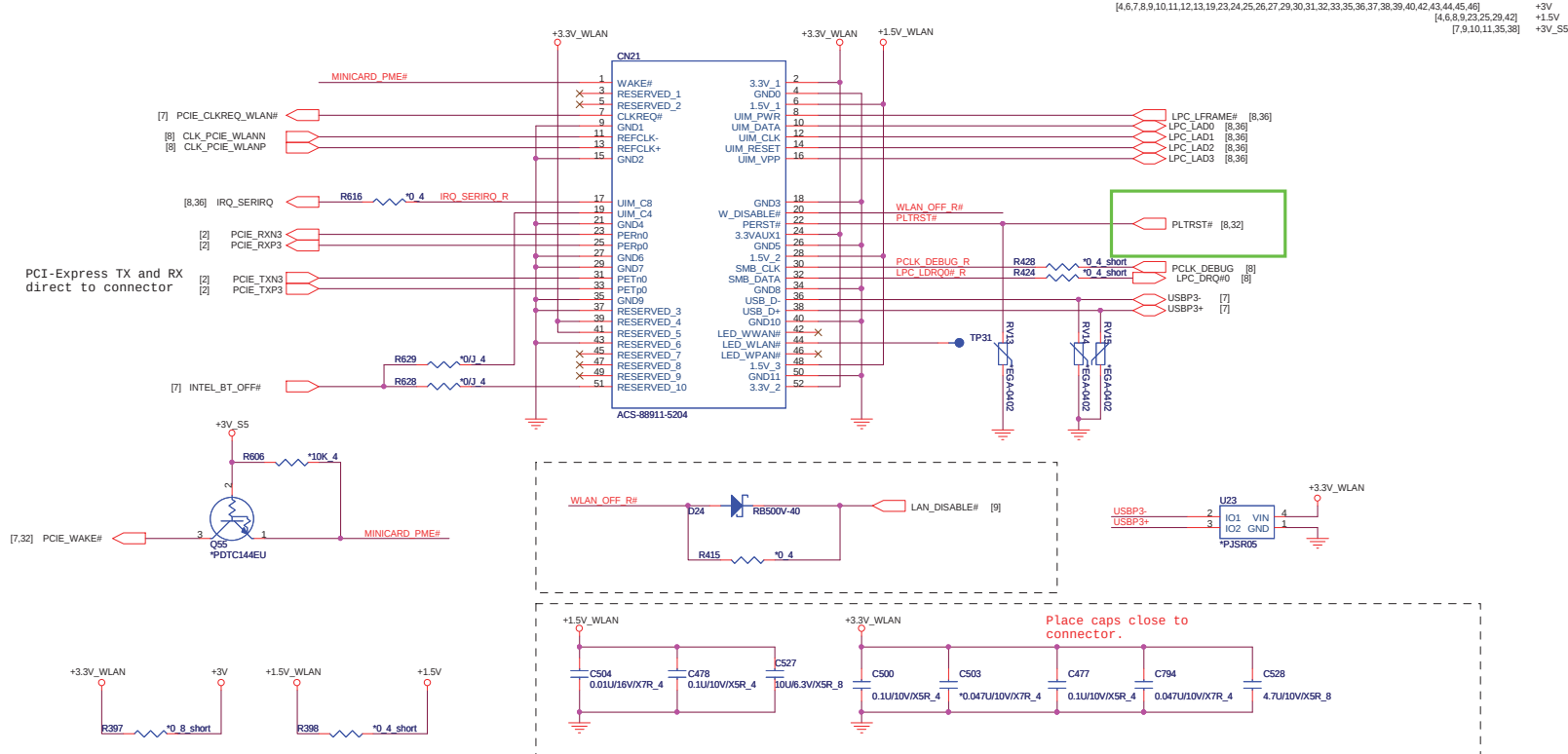
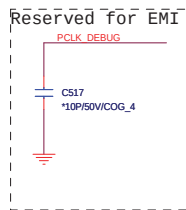


ESD PROTECTION

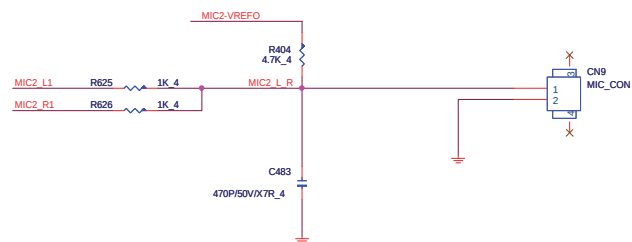




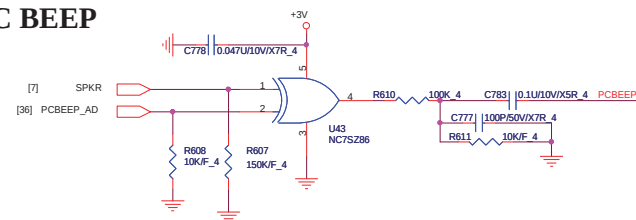
MiniCard WLAN connector



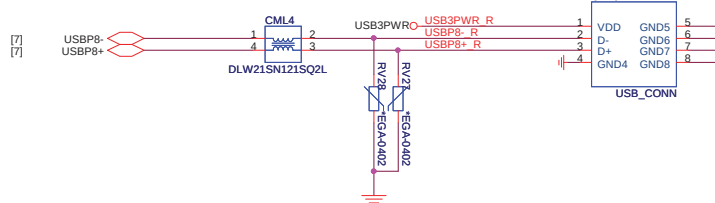
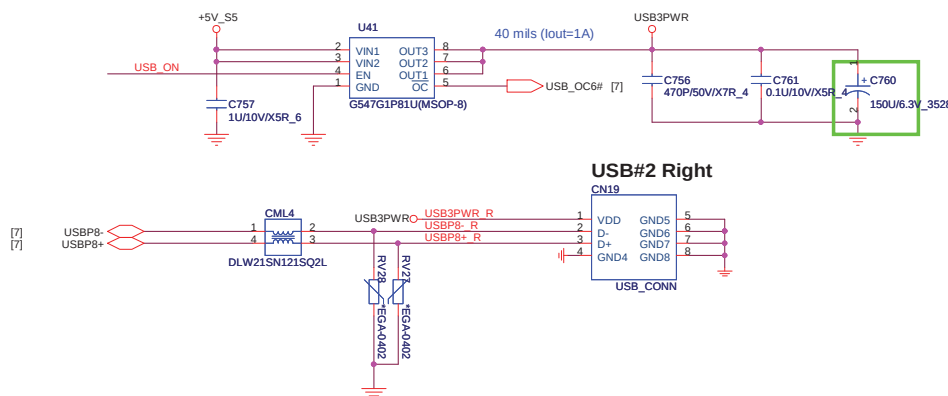
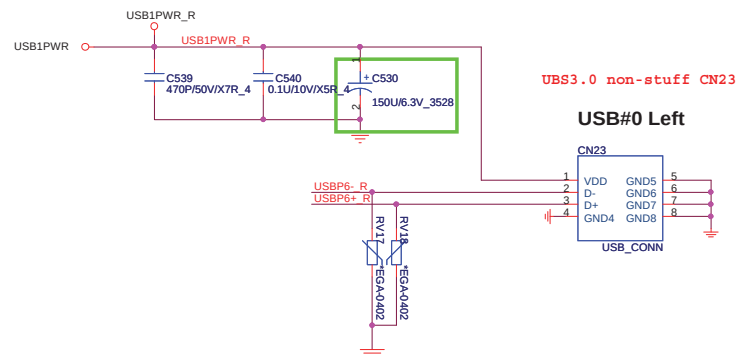
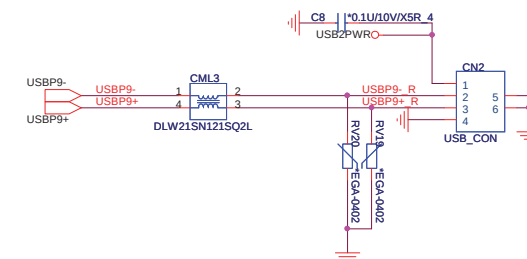
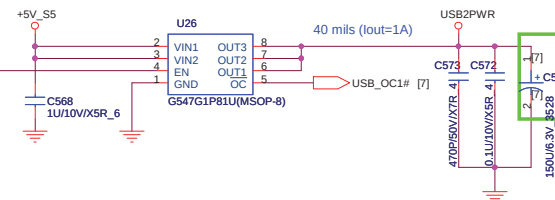
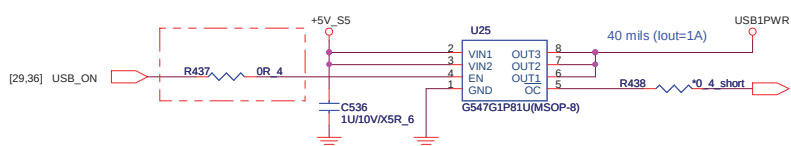
Close to CODEC



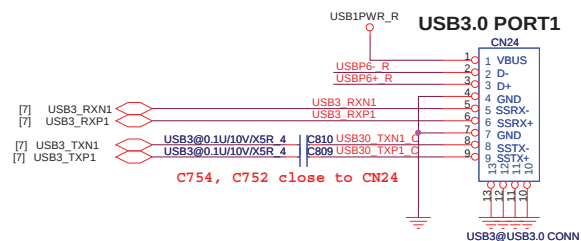
Earphone(AMP)



USB#1 Daughter board

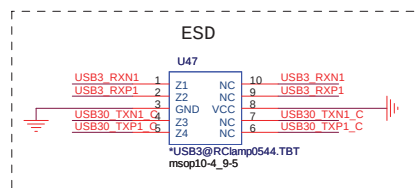
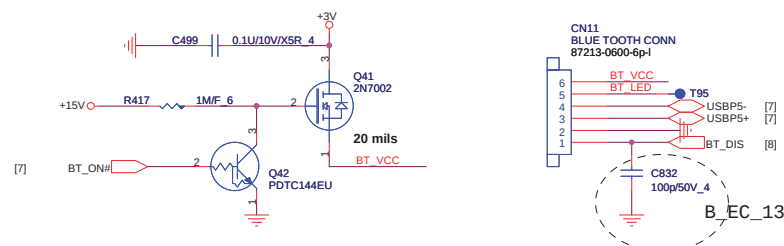


REAR USB PORT X1



SUY USB3.0: DFHS09FR063

BLUETOOTH



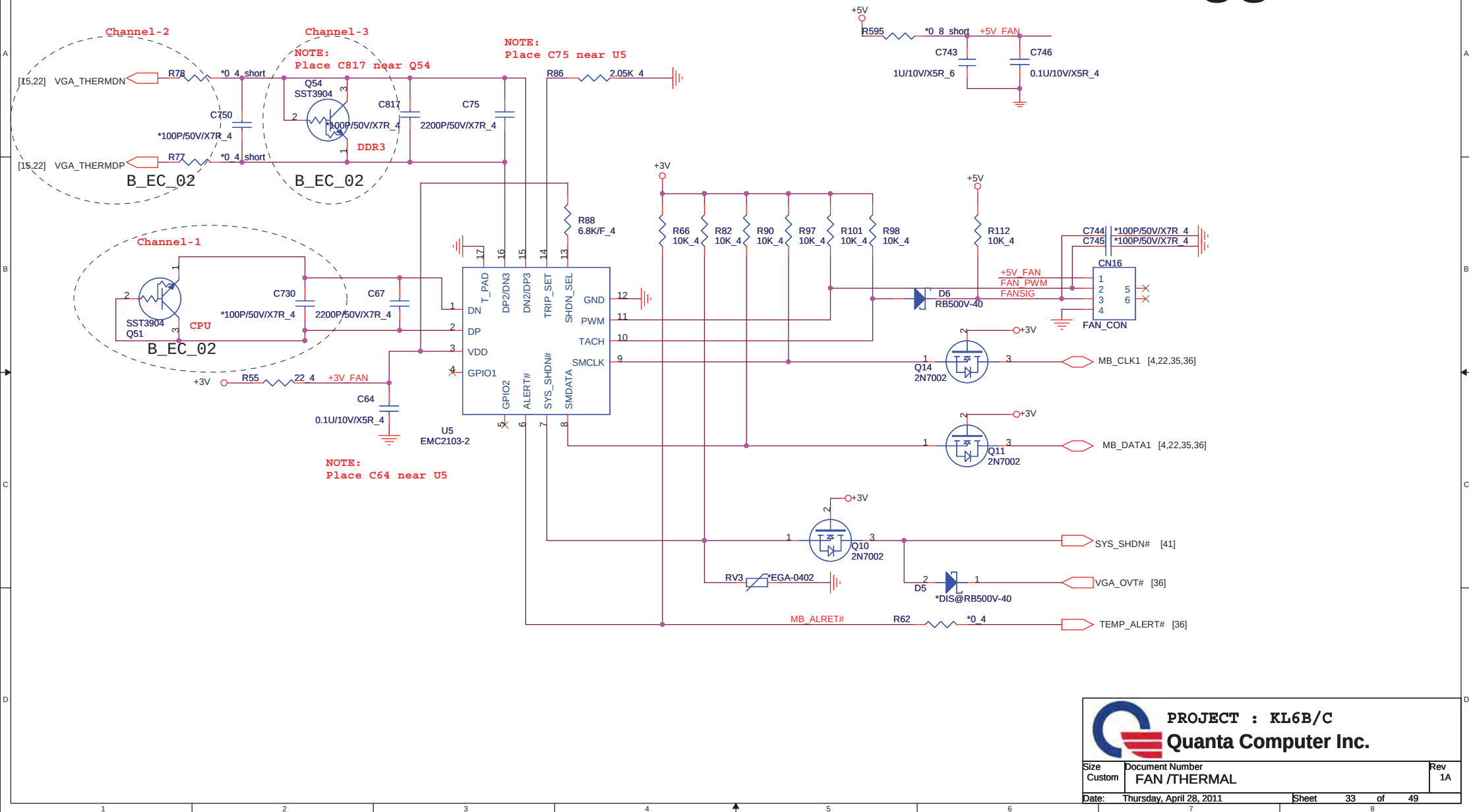
FAN CONTROL

[4,6,7,8,9,10,11,12,13,19,23,24,25,26,27,28,29,30,31,32,35,36,37,38,39,40,42,43,44,45,46]
[9,19,23,25,26,29,30,34,35,36,37,38,39,44]

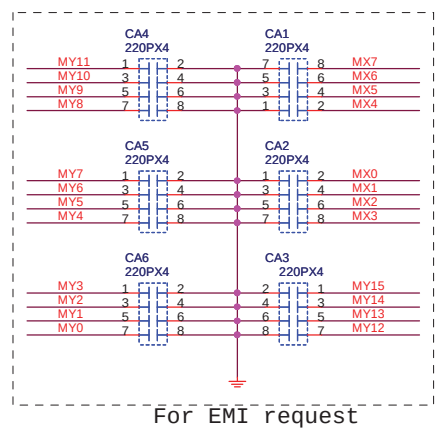
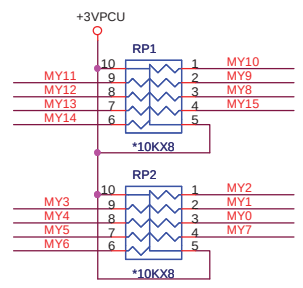
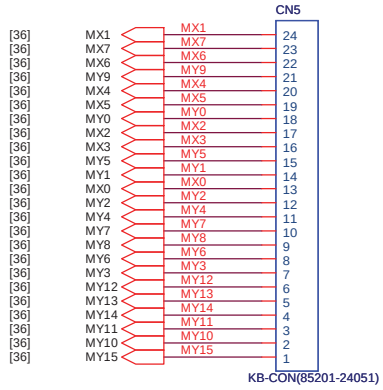
+3V
+5V



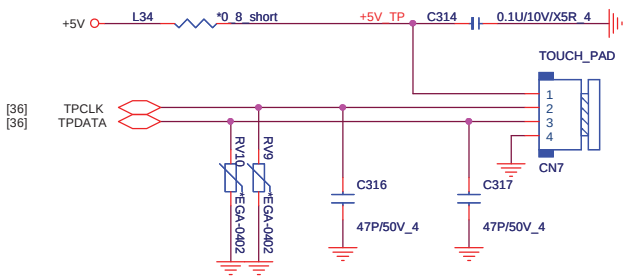
33

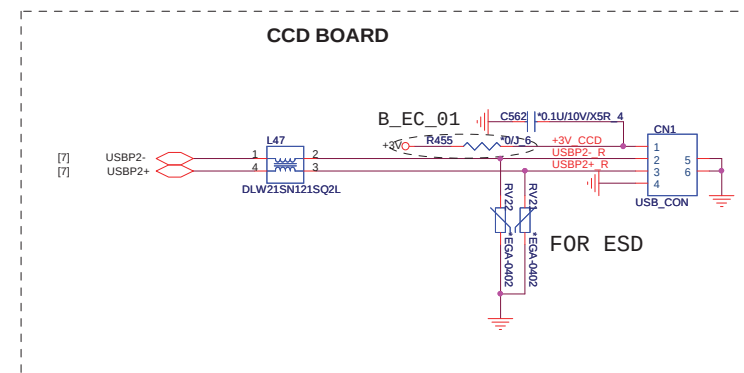
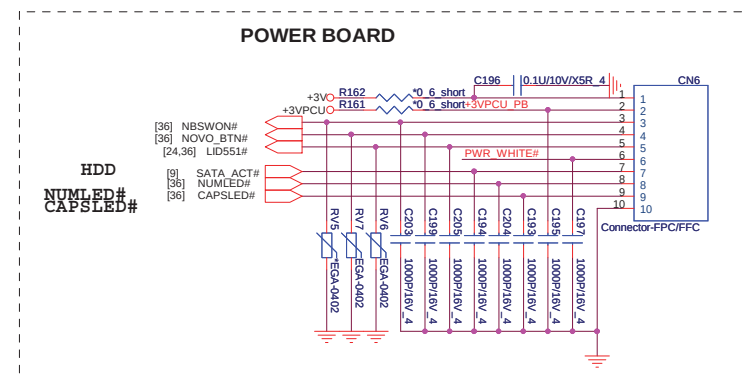
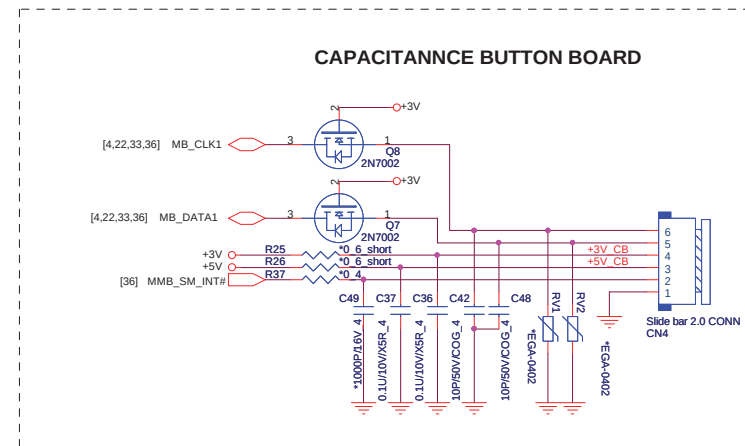
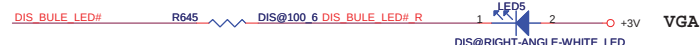
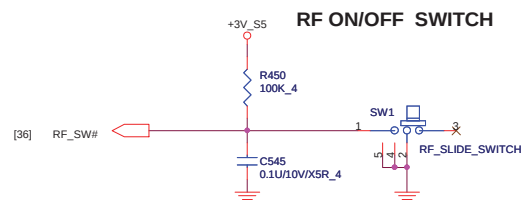


KEYBOARD



Touch pad



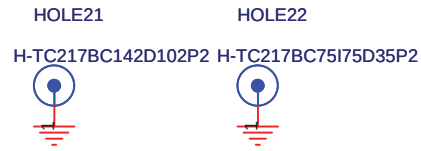


Screw for ME

CPU BKT

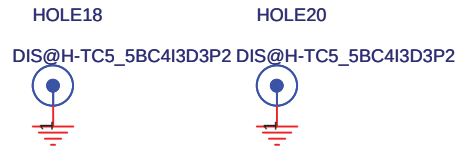
37

WLAN

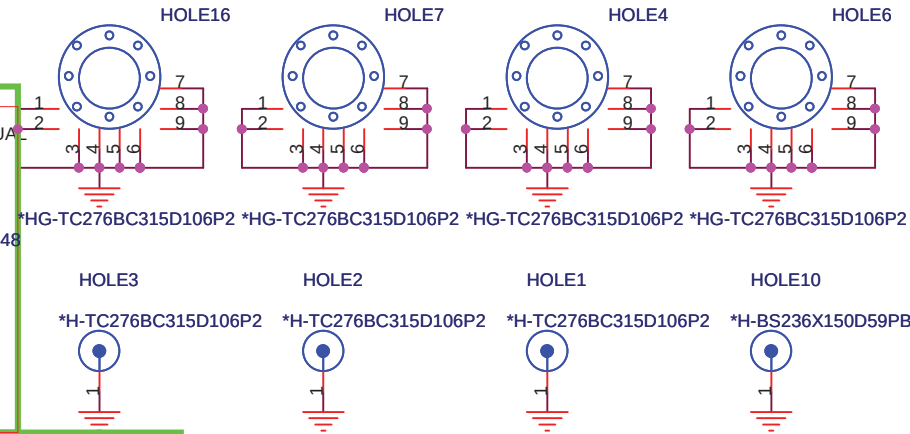
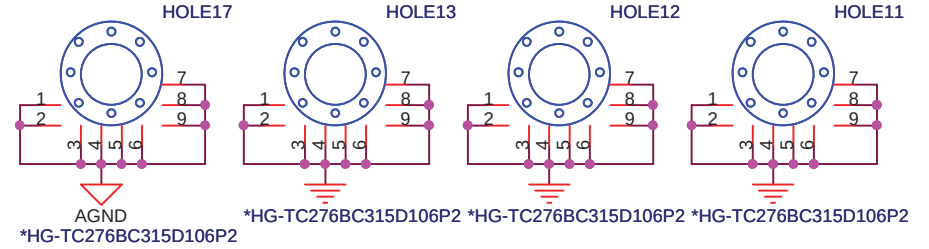
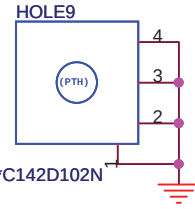


SMT NUT H=4/7mm

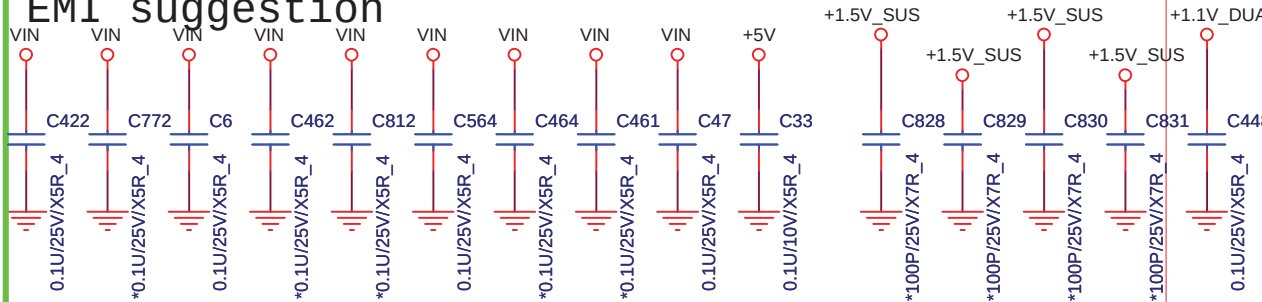
VGA



SMT NUT H=4/7mm



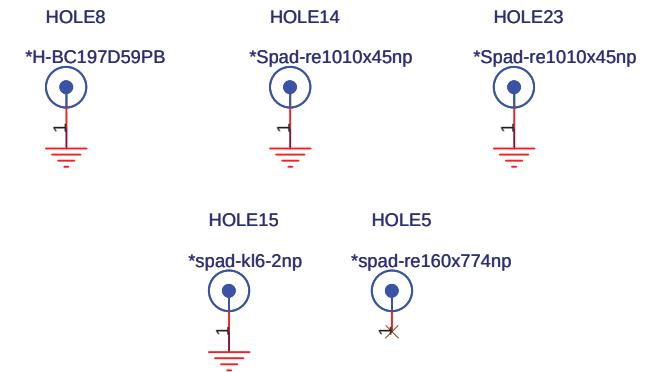
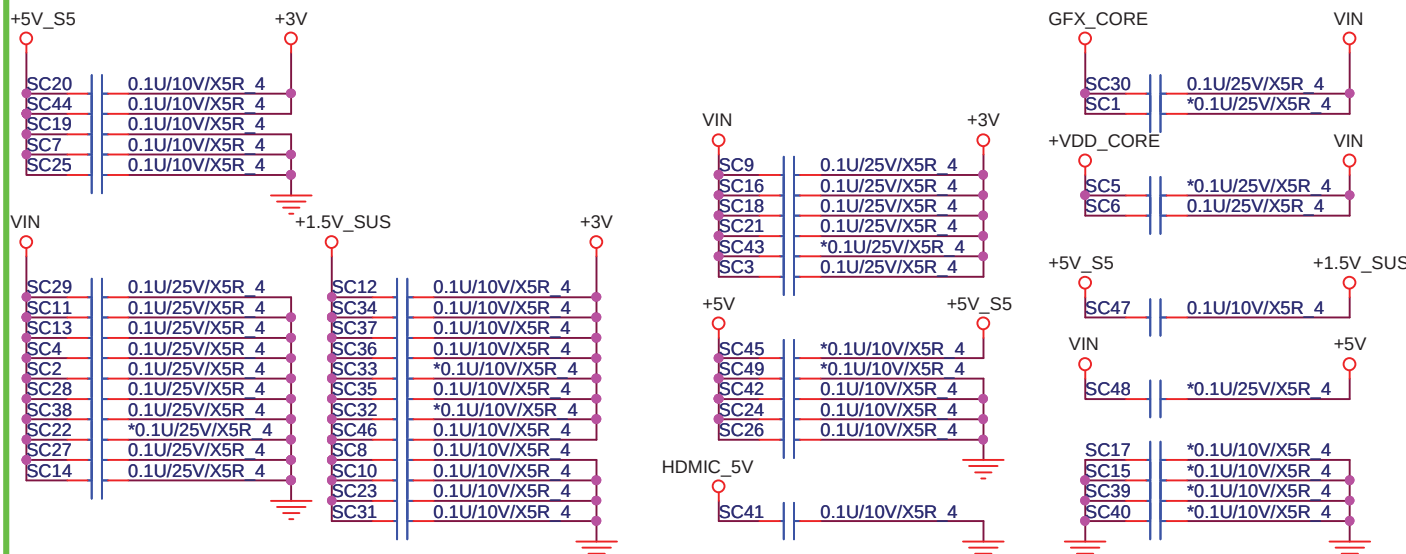
EMI suggestion



B-08

4/22 change

ESD suggestion

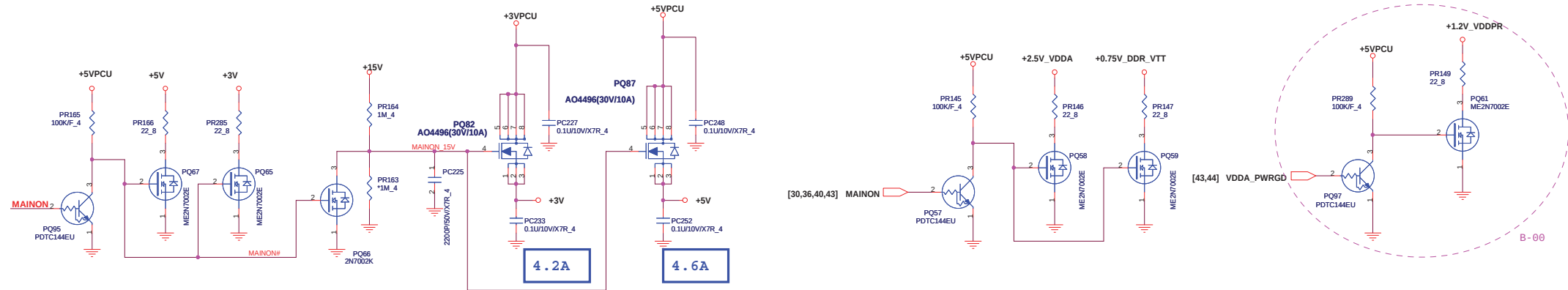


PROJECT : KL6B/C
Quanta Computer Inc.

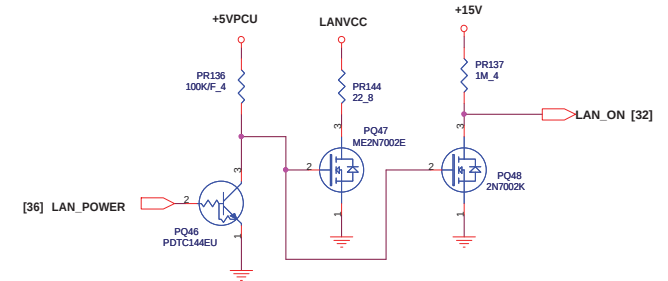
Size Custom	Document Number HOLD & SKEW	Rev 1A
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DISCHARGE

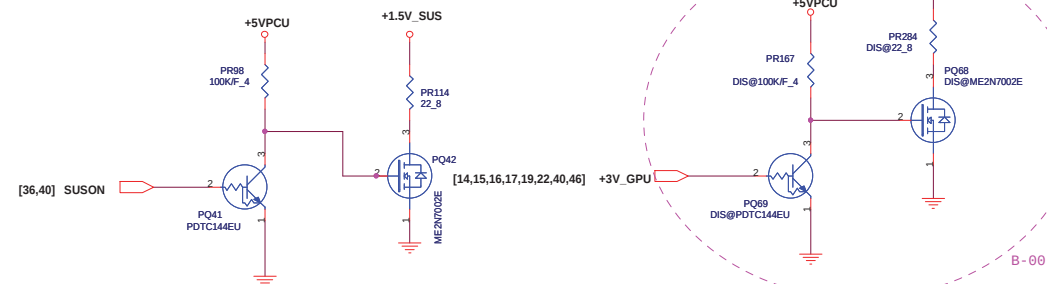
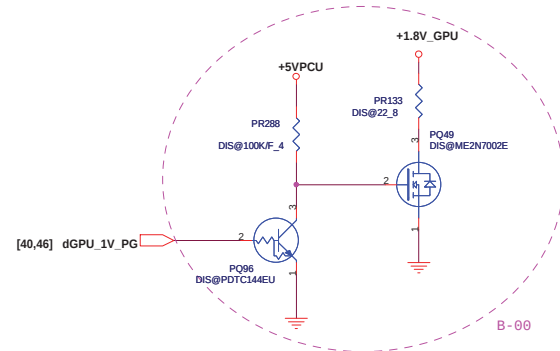
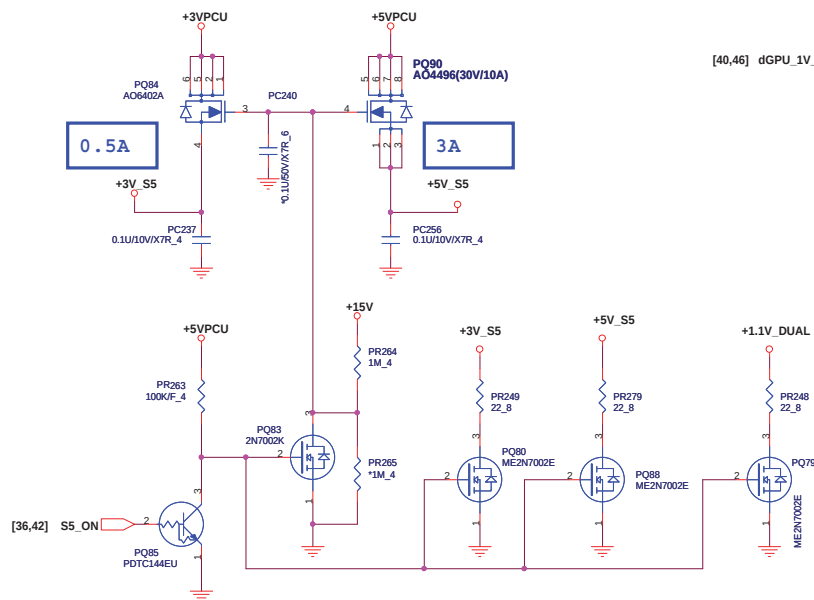
+3V, +5V, +1.5V



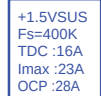
LANVCC



3V_S5, 5V_S5

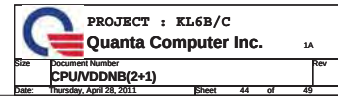


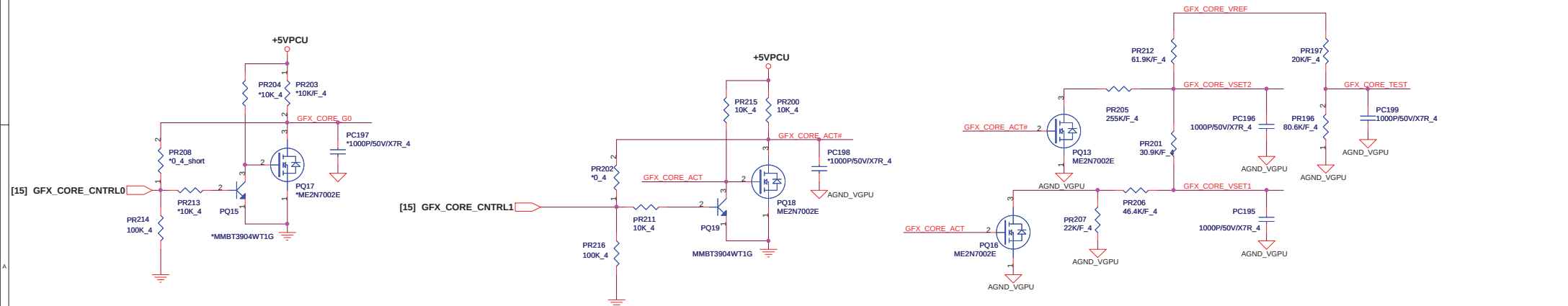
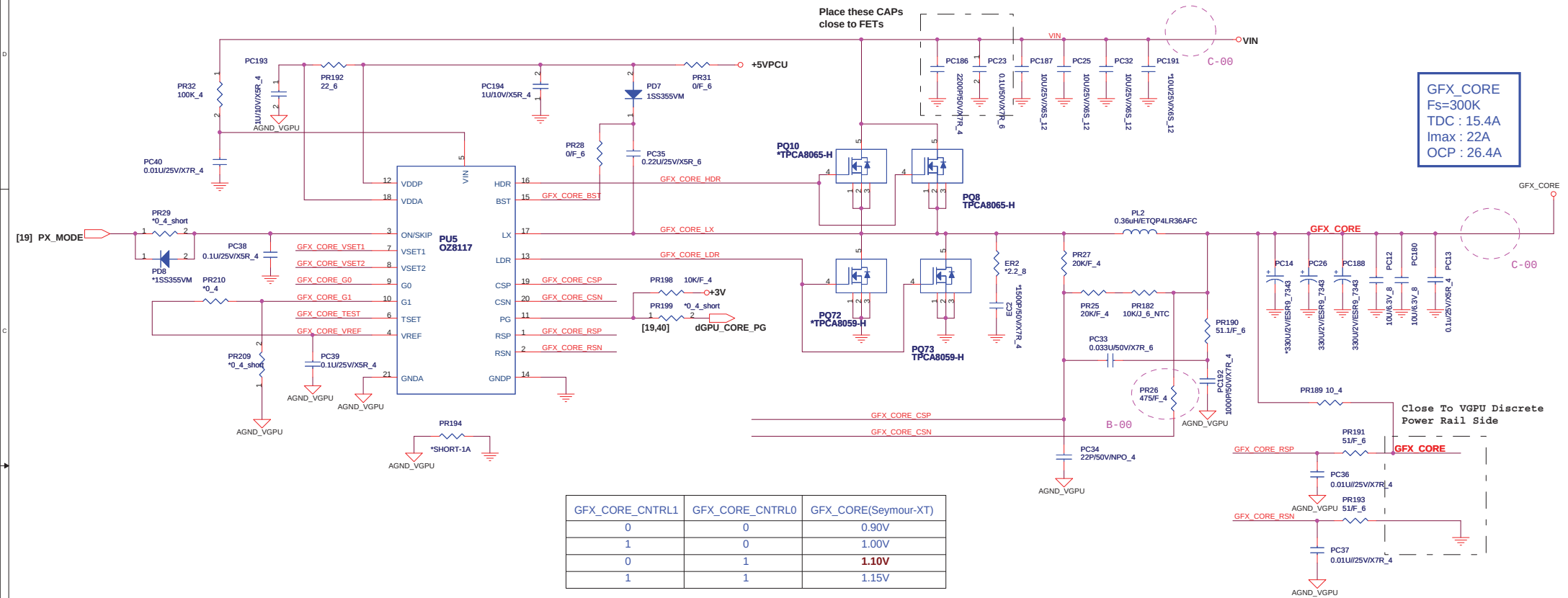


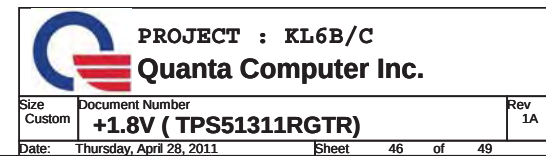




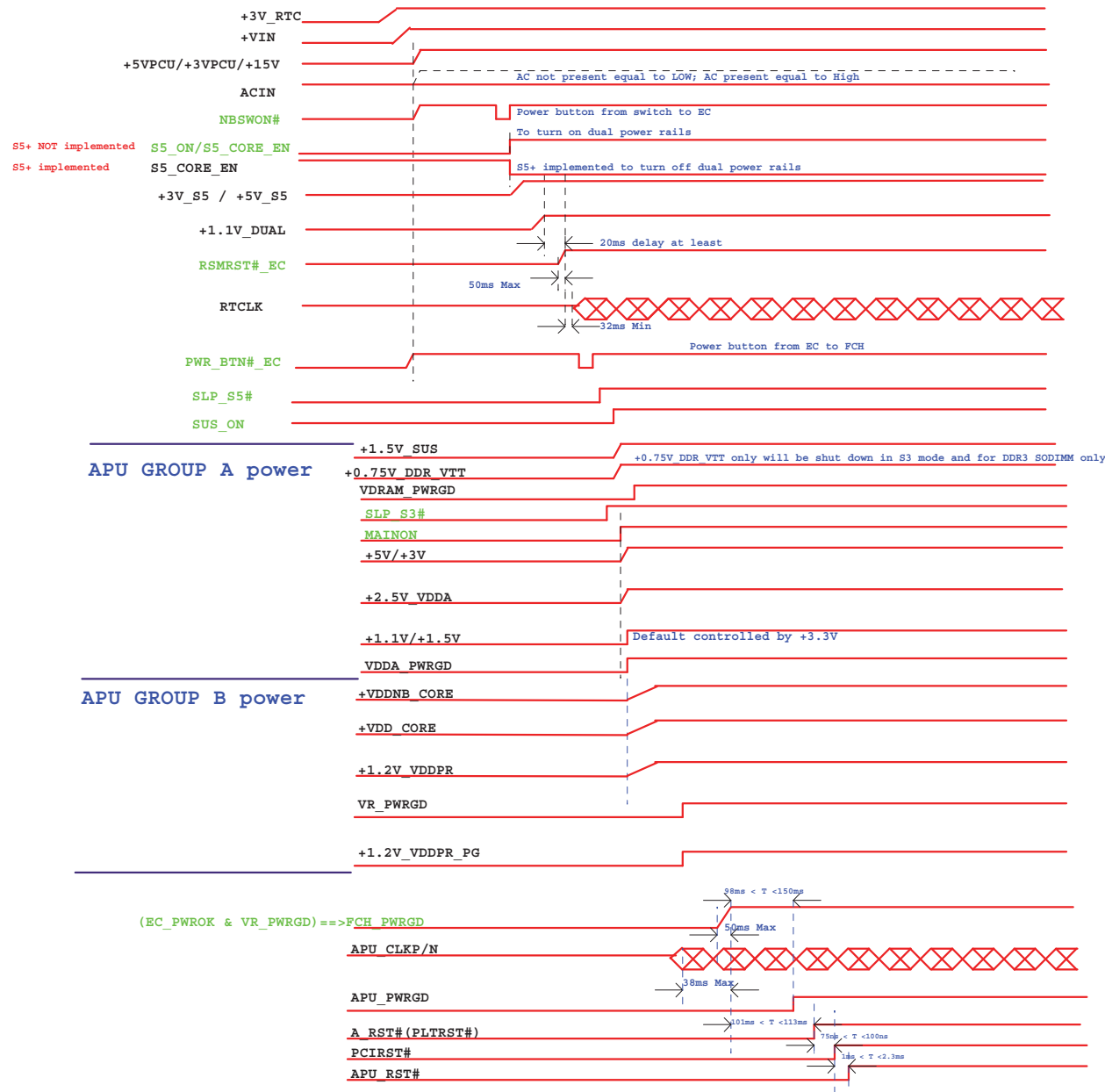








Z475 Power On Sequence: S5 > S0



APU Power on sequence required:

Llano APU:

1.Group A (+1.5V_SUS, +2.5V_VDDA) ramp before Group B
(+VDD_CORE, +VDDNB_CORE, +1.2V_VDDPR)

HUDSON-M2/M3:

1.+3V_S5 ramp before +1.1V_DUAL
2.+3V ramp before +1.1V
3.+3V_RTC must ramp at least 5 secs before the +3V_S5

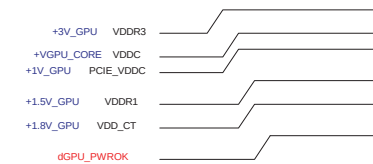
Robson-Pro M2/Capilano-LP M2 package Power-on sequence

All power rails reach nominal within 20ms

1=> +3V_GPU
2=> +VGPU_CORE/+1V_GPU
3=> +VGPU_CORE_PWRGD to enable +1.5V_GPU
4=> +1V_GPU_PWRGD to enable +1.8V_GPU

NOTE

1.EC (EC_PWR_EN) or FCH (PE_GPIO1) to turn on +3V_GPU
2.+3V_GPU ready to enable +VGPU_CORE/+1V_GPU
(+1V_GPU will ramp up before +VGPU_CORE)
3.+VGPU_CORE_PWRGD to enable +1.5V_GPU
3.+1V_GPU_PWRGD to enable +1.8V_GPU



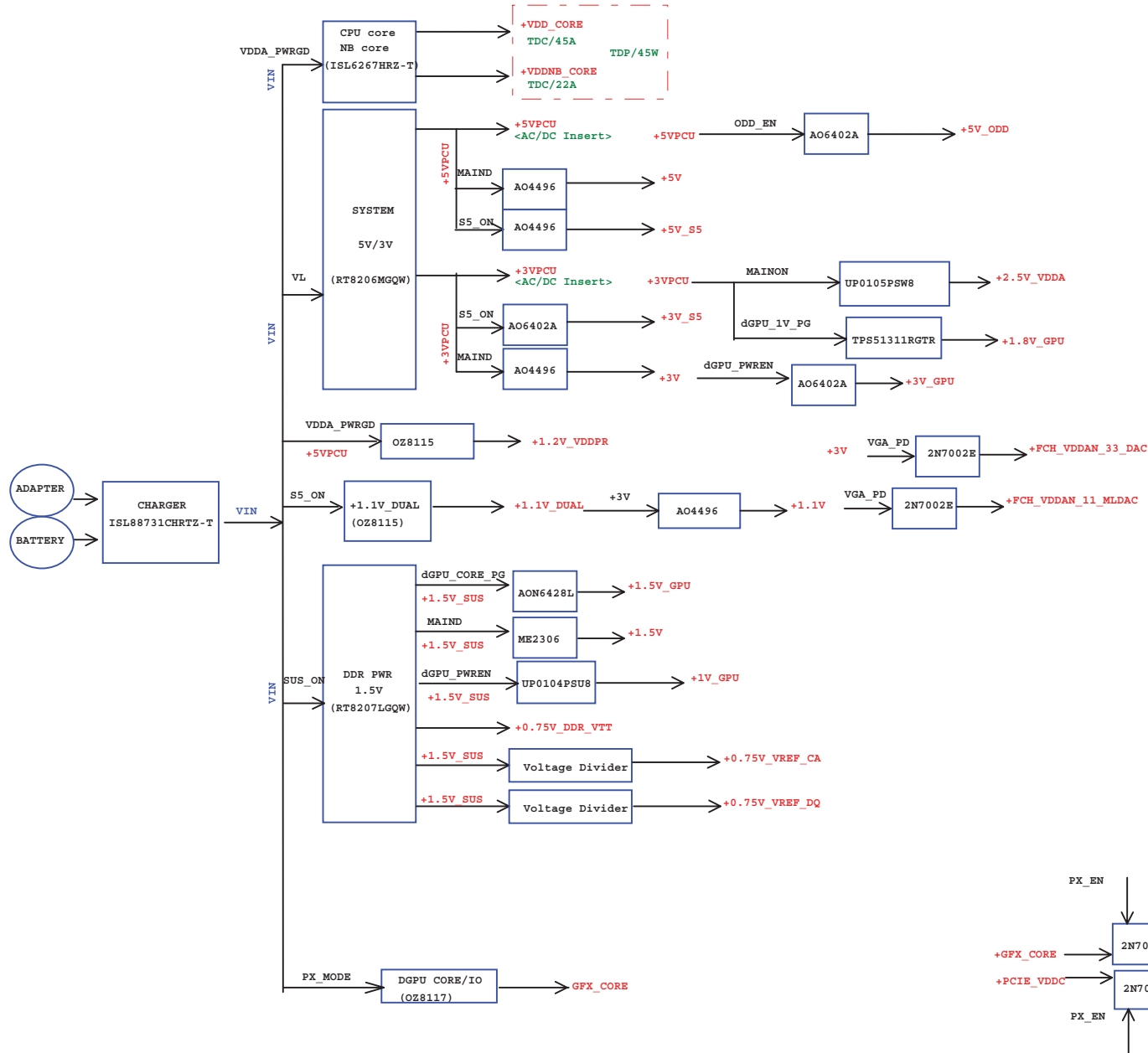
TRAVIS_L ANX3110 power sequence

1.+3V must lead +1.2V_TRAVIS

NOTE: EC output TRAVIS_EN# after receive
+1.2V_VDDPR_PG

2.+1.2V_TRAVIS must lead TRAVIS_RST#

NOTE: FCH must output PCIE_RST# TRAVIS or
APU_PCIE_RST# after +1.2V_TRAVIS ready



KL6C / Z475 Schematic EE EC Tracking list

EC #	Page	CMVC #	Description	Date	Part Affected
A-01	4		Add level shifter design for LVDS PWM signal	0208	
A-02	4		Sys_pwrok pull high from 10K to 100K	0208	
A-03	9		Design issue need to swap SPI SI/SO signal	0208	
A-04	11		Disable Strap pin (EC disable) for CRT no function issue	0208	
A-05	14		DGPU reset change design to be controlled by GPIO only	0208	
A-06	16		Disable DGPU JTAG DEBUG MODE	0208	
A-07	23		Remove Travis IC power switch schematic for cost down	0208	
A-08	23		Design issue need to swap LVDS EDID signal	0208	
A-09	35		Change Resistor value to adjust the brightness of LED	0208	
A-10	7		Change USB port for USB2.0 & CardReader to USB.(Disable Hub3)	0208	
A-11	25		Change PU resistor value from 100ohm to 100kohm	0208	
A-12	36		Change EC pin to default PL to avoid PWR LED light one time as DC-IN	0208	
A-13	25		I2C level shift IC change to stuff.	0211	
A-14	22		no need to enable HDMI audio function in DGPU	0216	
A-15	7		Add Thermal trip PU resistor	0216	
A-16	18		Remove bead & cap for cost down	0218	
A-17	35		Add R188 ODD_MDDA# to connect to EC	0224	
A-18	35		Remove VGA SW2(ATI can't support HW switch)	0224	
A-19	22		Remove VGA External thermal IC	0224	
SIV					
B-01	35		Add CCD P_SW on/off (Add C578, Q62, R467, Q63, R468 ; Del R455)	0306	
B-02	33		Connect to VGA Therm_Die use Channel 1.Del Q58(WLAN) for CPU used. Add: R78, R77 ; Del: Q58	0306	
B-03	9		Change U17 VDD to +3V_S5	0306	
B-04	9		ADD SPI_HOLD# GPIO control, reserve R469	0306	
B-05	4		ADD SM_LV_CLK & SM_LV_DAT to connect FCH; Reserve R496 & R497	0306	
B-06	9		AUXCAL change to power rail for VGA Power Down Feature	0306	
B-07	22		ADD MOSFET for VGA SMBUS; ADD Q19, Q20, R158, R159	0306	
B-08	23		Del R8 ,R177,R99, R41,R42,R43 for remove LVDS reserve schematic	0307	
B-09	25		Delete R389,R401,D20,D21,D22,D23,Q36,Q37 cost reduce fail	0316	
B-10	25		Add R657,R658,R659,R660,R661,R662,R663,R664,C826,C827,U49	0316	
			2nd source verify	0316	
B-11			EMI solution	0316	
			POP R602,R601,R598,R597 120ohm	0316	
			POP CML3,CML4,CML2,CML1,L47	0316	
			Remove R464,R456,R599,R600,R451,R453,R412,R413,R465,R466 0ohm	0316	
			POP C408,C422,C749	0316	
			POP C391,C392	0316	
			Reserve C828,C829,C830,C831	0316	
B-12	06		POP R655,R656 Remove U18,R337,R330 Internal notice update	0317	
			Change Q61 PN:BA05L060000 Internal notice update	0317	
			Remove C207	0317	
B-13	34		CN5 Modify footprint to 85208-24071-24p-l	0317	
B-13	31		Add C832 for EMI solution	0318	
B-14			Change C515 & C516 to 27pF to fine tune timing	0321	
			Change C387 & C386 to 27pF to fine tune timing	0321	
			Change C188 & C184 to 27pF to fine tune timing	0321	
			Change C365 & C366 to 27pF to fine tune timing	0321	
SVT					
C-01	04		Change R541,R547 to *0_4_short	0418	
	06		Change R535,R537,R545 to *0_4_short	0418	
			Delete U18, R655, R656, R337, R330; J1, R587, R336, R323, R305, R580, R577	0418	
	07		Change R468,R287,R545,R169, R521,R533,R256,R317,R258,R552,R528 to *0_4_short	0418	
	08		Change R200,R183 to *0_4_short; Change R427 to *0_6_short	0418	



Document Number
EC Track

Thursday, April 28, 2011 Sheet 49 of 49

1

Date: Thursday, April 28, 2011 Sheet 49 of 49

KL6C / Z475 Schematic EE EC Tracking list					
EC #	Page	CMVC #	Description	Date	Part Affected
C-01	09		Change R263,R254,R247 to *0_4_short	0418	
	19		Change R157 to *0_4_short	0418	
	23		Change R83,R50,R46,R91 to *0_4_short; change R650 to *0_8_short	0418	
	24		Change R2 to *0_4_short; Change R7,R28 to *0_8_short	0418	
	25		Change R660,R661,R662,R663 to *0_4_short	0418	
			Delete U42,R603,R605, R381,R382,R384,R386,R399,R400; C375, C377,C448,C449,C459	0418	
	28		Change R398,R424,R428 to *0_4_short	0418	
			Change R397 to *0_8_short	0418	
	29		Change CML1 footprint to "choke-wcm2012-4p"	0418	
			Delete R412,R413; Change R365,R3698,R604 to *0_8_short	0418	
	31		Change R438 to *0_4_short	0418	
			Change CML2,CML3,CML4 footprint to "choke-wcm2012-4p"	0418	
			Delete R451,R453,R599,R600,R456,R464	0418	
	32		Change R444 to *0_4_short; Change R418,R421,R435,R449 to *0_8_short	0418	
	33		Change R77,R78 to *0_4_short; Change R595 to *0_8_short	0418	
	34		Change L34 to *0_8_short	0418	
	35		Change L47 footprint to "choke-wcm2012-4p"	0418	
			Delete R465,R466; Change R161,R162 to *0_6_short	0418	
	36		Change R111,R142,R188,R203 to *0_4_short	0418	
	27		Change R646 to *0_8_short	0418	
	12		Change R394 to *0_6_short	0418	
C-02	31		change U47 Pin8 design	0422	
	37		Add C448 (0.1u CAP) for EMI solution	0422	
C-03	4		delete APU debug funciton, R570, R579,R583,R584,R596	0425	
	34		Mount CA1,CA2,CA3,CA4,CA5,CA6 for EMI solution	0426	
	35		Change Q62 PN to BAM34040001	0426	
	10		Change Q29,Q32 PN to BAM34040001	0426	
C-04	25		Change value of R601,R602,R597,R598 to 140 ohm for HDMI issue	0428	
			Change value of R383,R385,R387,R388,R391,R392,R395,R402 to 560 ohm for HDMI issue	0428	