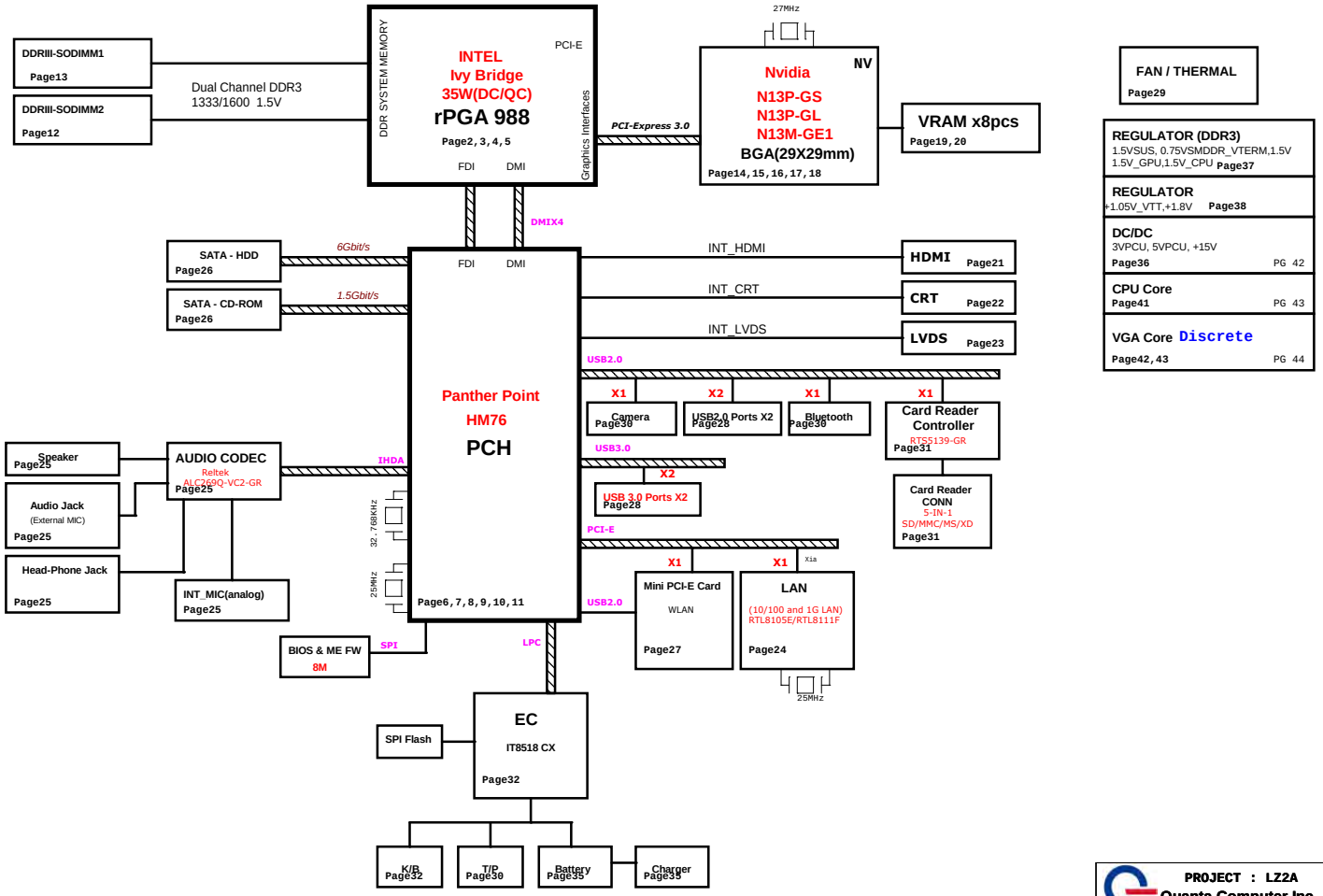
LZ3/LZ3A (Z580) Intel Chief River Platform (Optimus) Block Diagram



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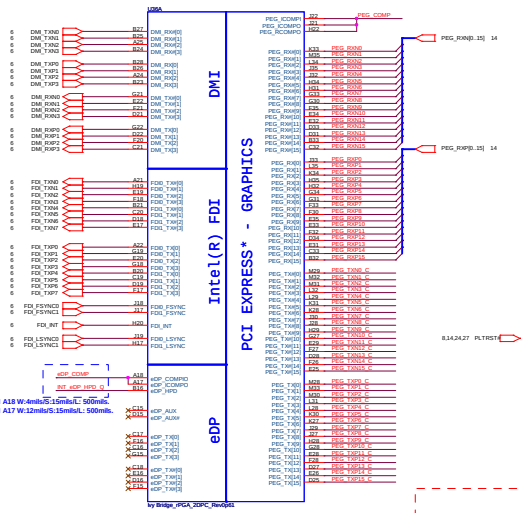
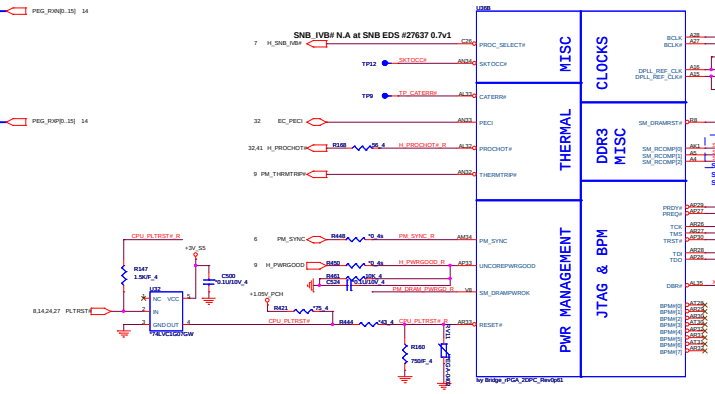
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

Ivy Bridge Processor (DMI,PEG,FDI)



eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

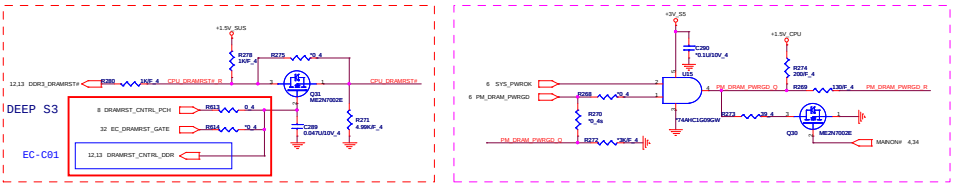
Ivy Bridge Processor (CLK,MISC,JTAG)



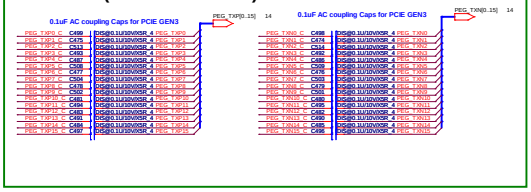
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils.
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils.
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils.

FOR DEEP S3

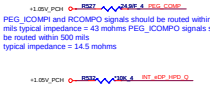
EC-C01



PEG x16 (UMA Non-stuff)



DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)

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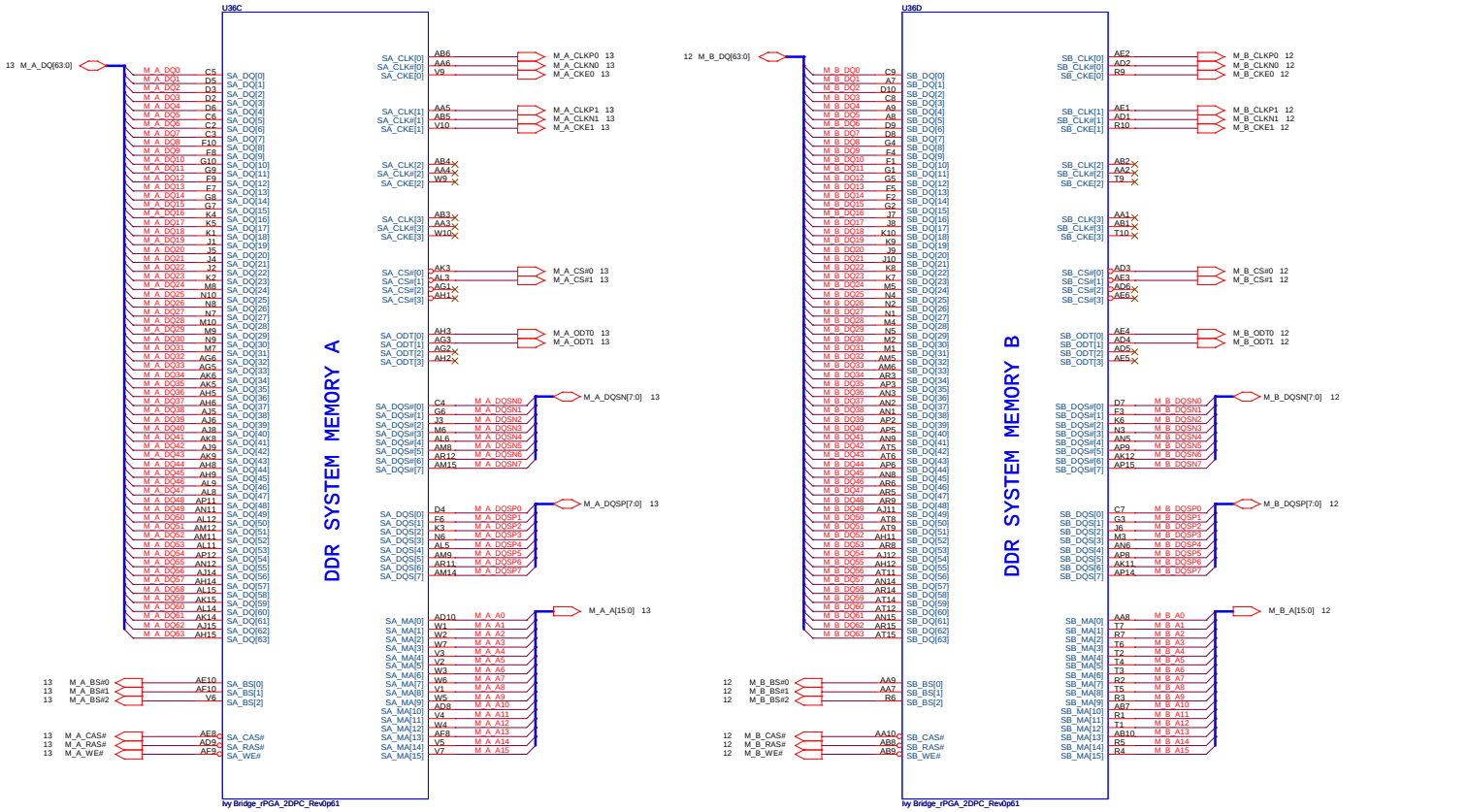
Ivy Bridge Processor (DDR3)



PROJECT : LZ2A

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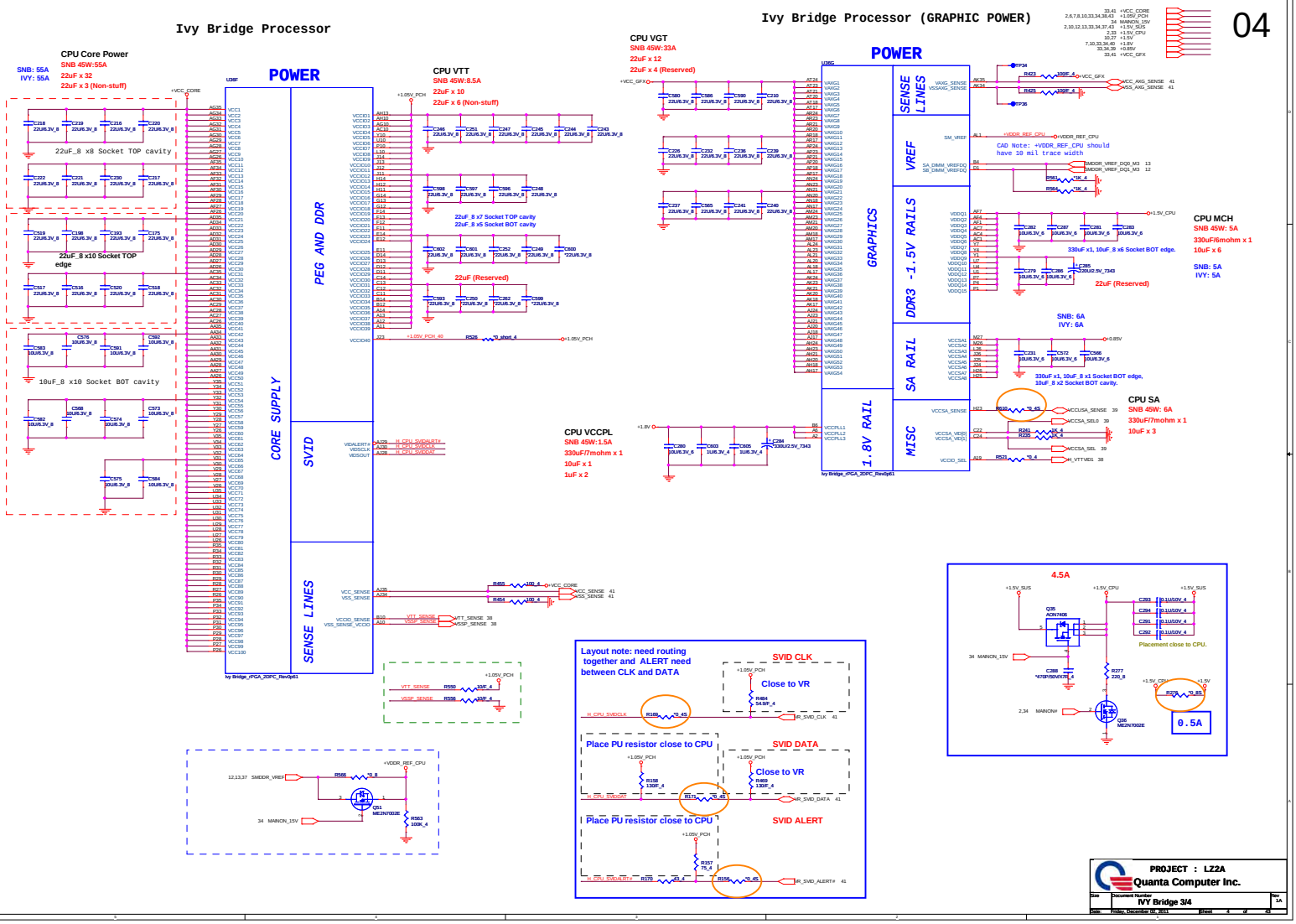
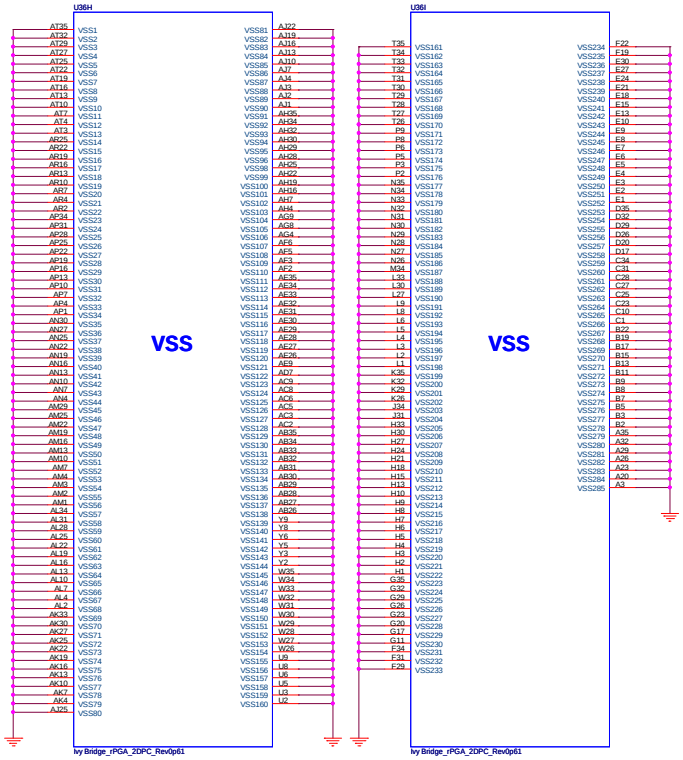
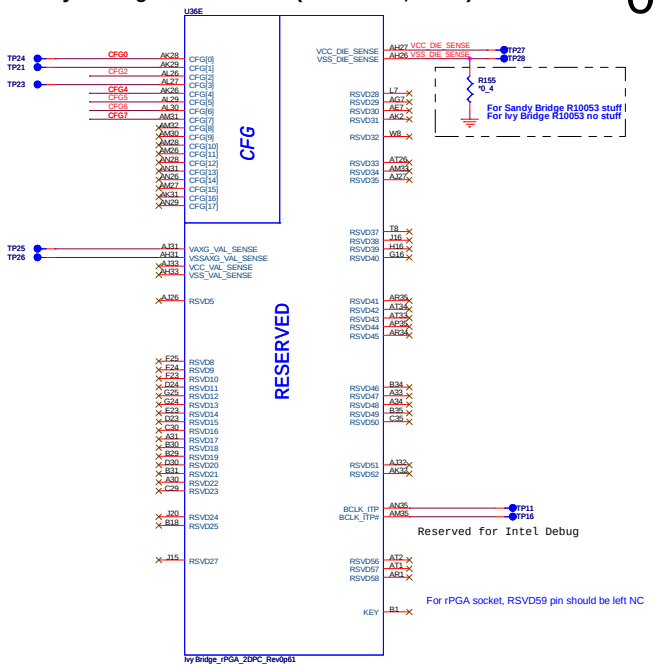

CPU Core Power
SNB: 55A
IVY: 55A
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)
POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket TOP edge
10uF_8 x10 Socket BOT cavity
CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF (Reserved)
CPU VCCPL
SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2
CPU VGT
SNB 45W:33A
22uF x 12
22uF x 4 (Reserved)
GRAPHICS
SENSE LINES
VREF
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
330uF x1, 10uF_8 x6 Socket BOT edge.
22uF (Reserved)
CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6
SNB: 5A
IVY: 5A
SNB: 6A
IVY: 6A
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.
CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3
Layout note: need routing together and ALERT need between CLK and DATA
SVID CLK
Close to VR
SVID DATA
Close to VR
Place PU resistor close to CPU
SVID ALERT
Place PU resistor close to CPU
4.5A
Placement close to CPU.
0.5A

Ivy Bridge Processor (GND)



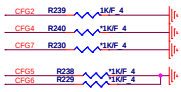
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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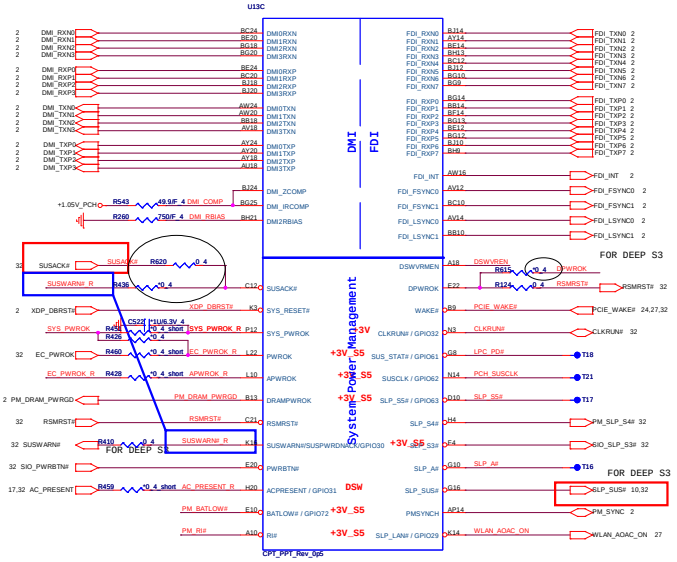
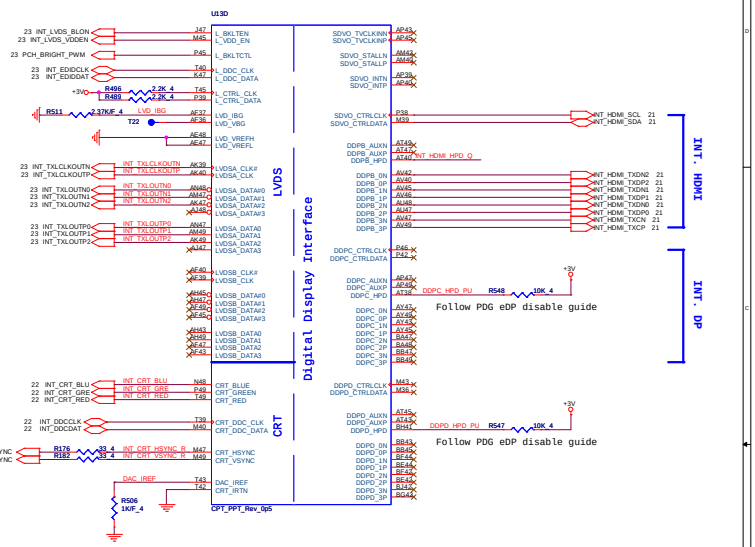
2,4,7,8,10,33,34,38,43 +1.05V_PCH
7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
2,7,8,9,10,27,31,34 +3V_S5
7,10,32 +3V_RTC

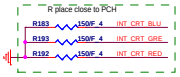
Cougar Point/Panther Point (DMI,FDI,PM)

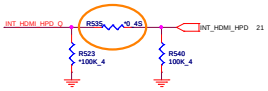


Cougar Point/Panther Point (LVDS,DDI)

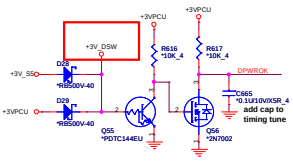


R place close to PCH

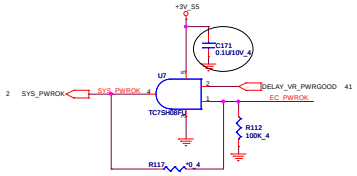


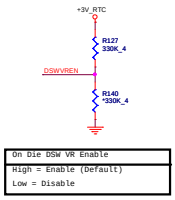


DPWROK FOR DSW (DEEP S3)



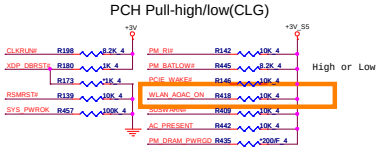
System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PCH Pull-high/low(CLG)



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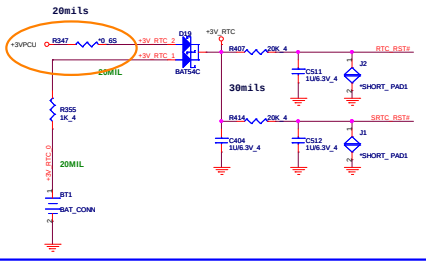
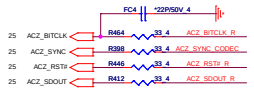
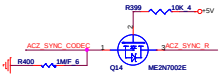
RTC Circuitry(RTC)



HDA Bus(CLG)

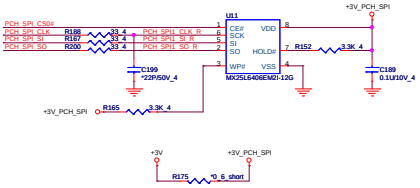




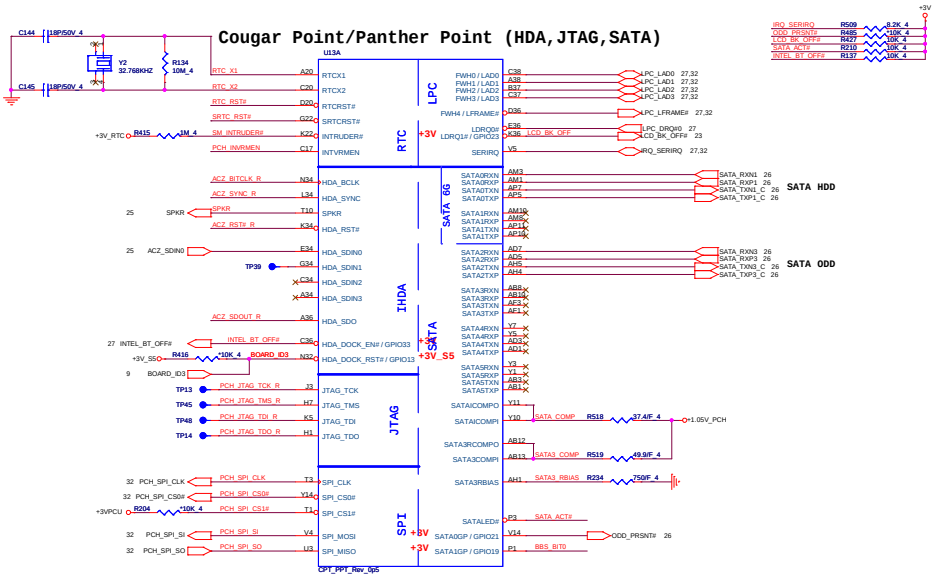
PCH Dual SPI (CLG)

32Mbit (8M Byte), SPI

AKE3EFP0N04: W25Q64CVSSIG
AKE3EFN0Q00: EN25Q64-104HIP
AKE3NFP0Z00: MX25L6406EM2I-12G
Socket: D6008000031



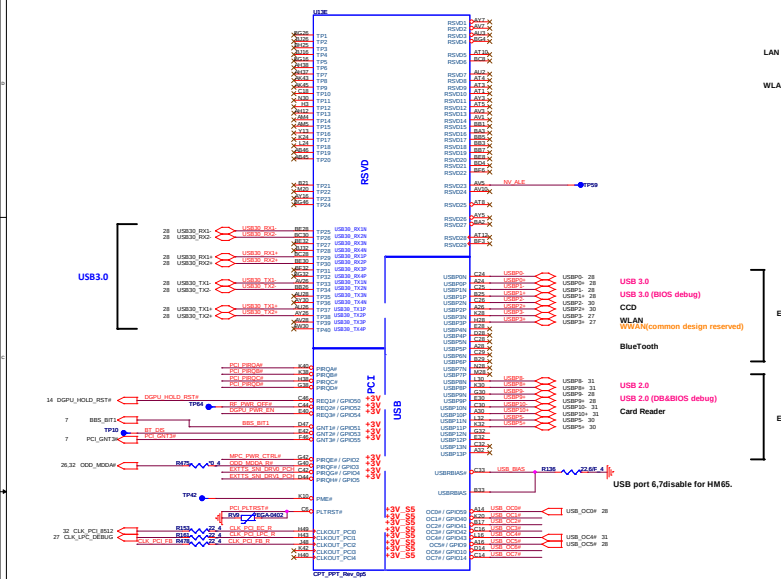
PCH2(CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

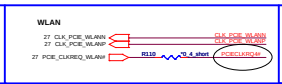
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



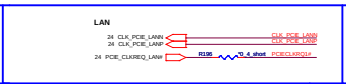
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

DGPU Power ON

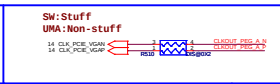
WLAN



LAN



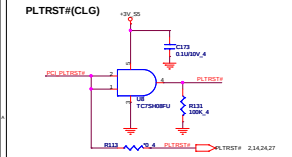
SW:Stuff UMA:Non-stuff



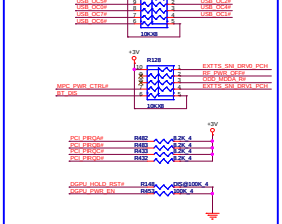
MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

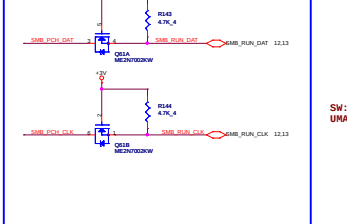
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)

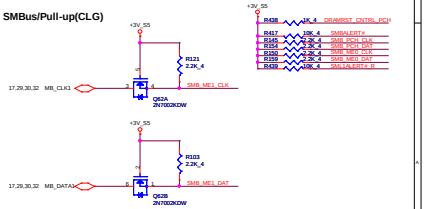


SMBus(CLK)



CLK_REQ/Strap Pin(CLG)

SMBus/Pull-up(CLG)



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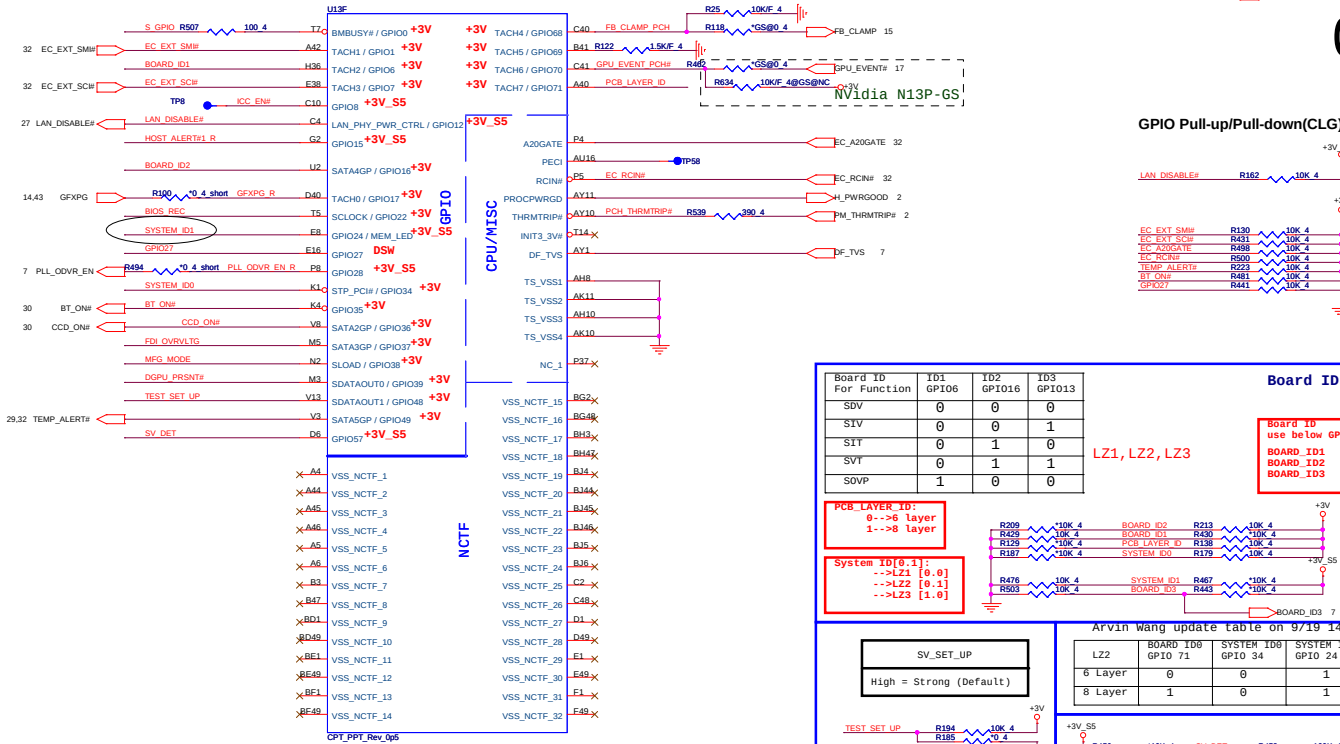
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

09



GPIO Pull-up/Pull-down(CLG)

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT	0	1	1
SOVP	1	0	0

Board ID

LZ1,LZ2,LZ3

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

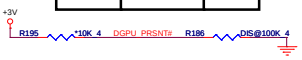
System ID[0.1]:
-->LZ1 [0.0]
-->LZ2 [0.1]
-->LZ3 [1.0]

Arvin Wang update table on 9/19 14:12

LZ2	BOARD ID0 GPIO 71	SYSTEM ID0 GPIO 34	SYSTEM ID1 GPIO 24
6 Layer	0	0	1
8 Layer	1	0	1

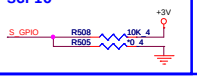
SV_SET_UP
High = Strong (Default)

	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532

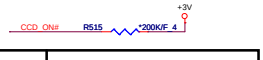


Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

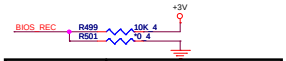
SGPIO



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

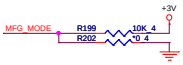


DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST



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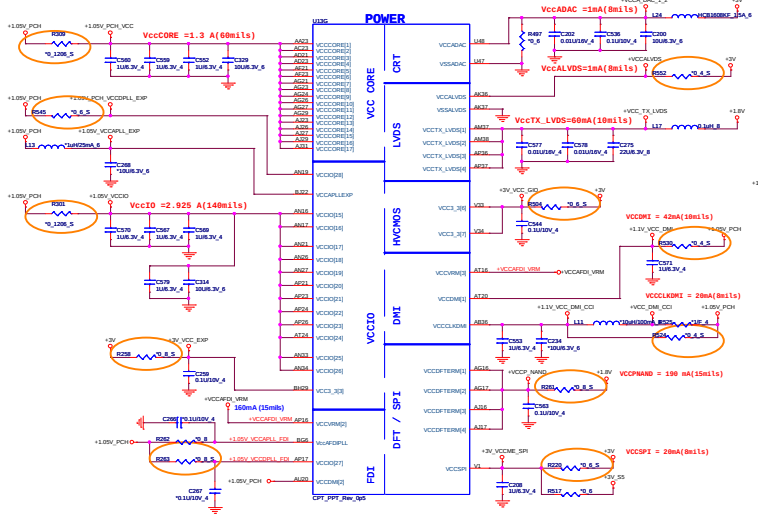
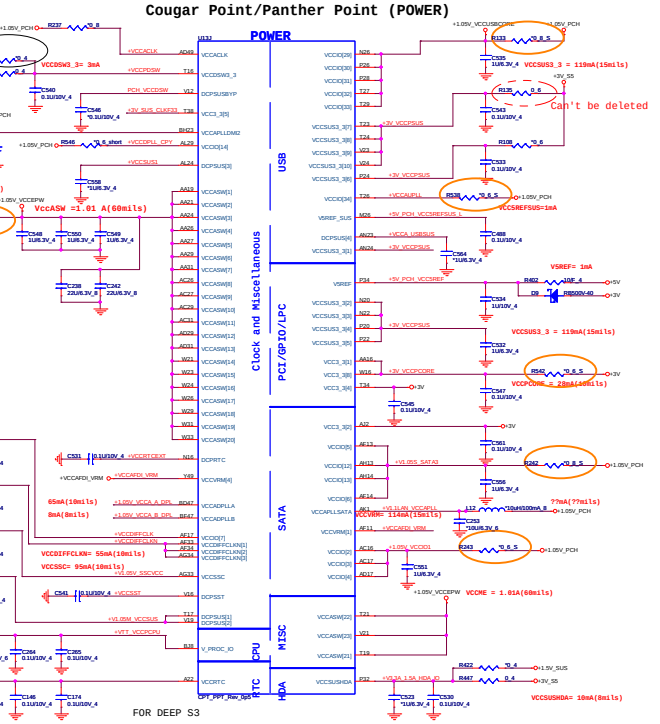
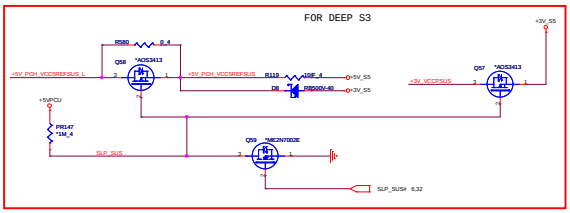
Cougar Point/Panther Point (POWER)







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Quanta Computer Inc.			
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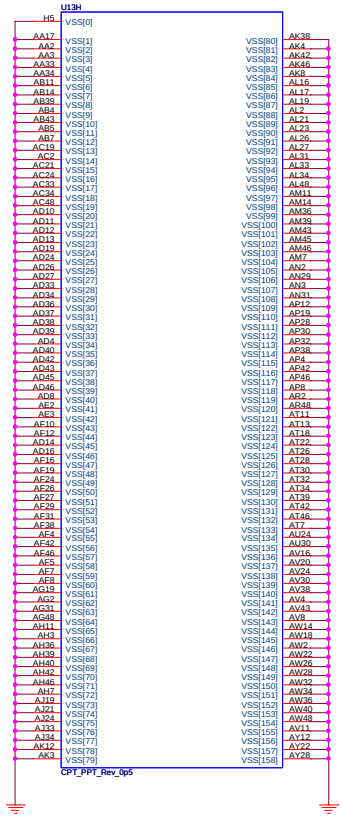
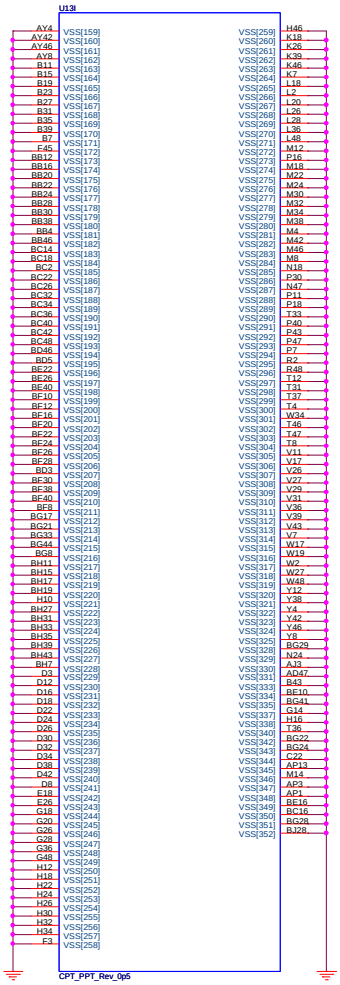
Cougar Point/Panther Point (GND)





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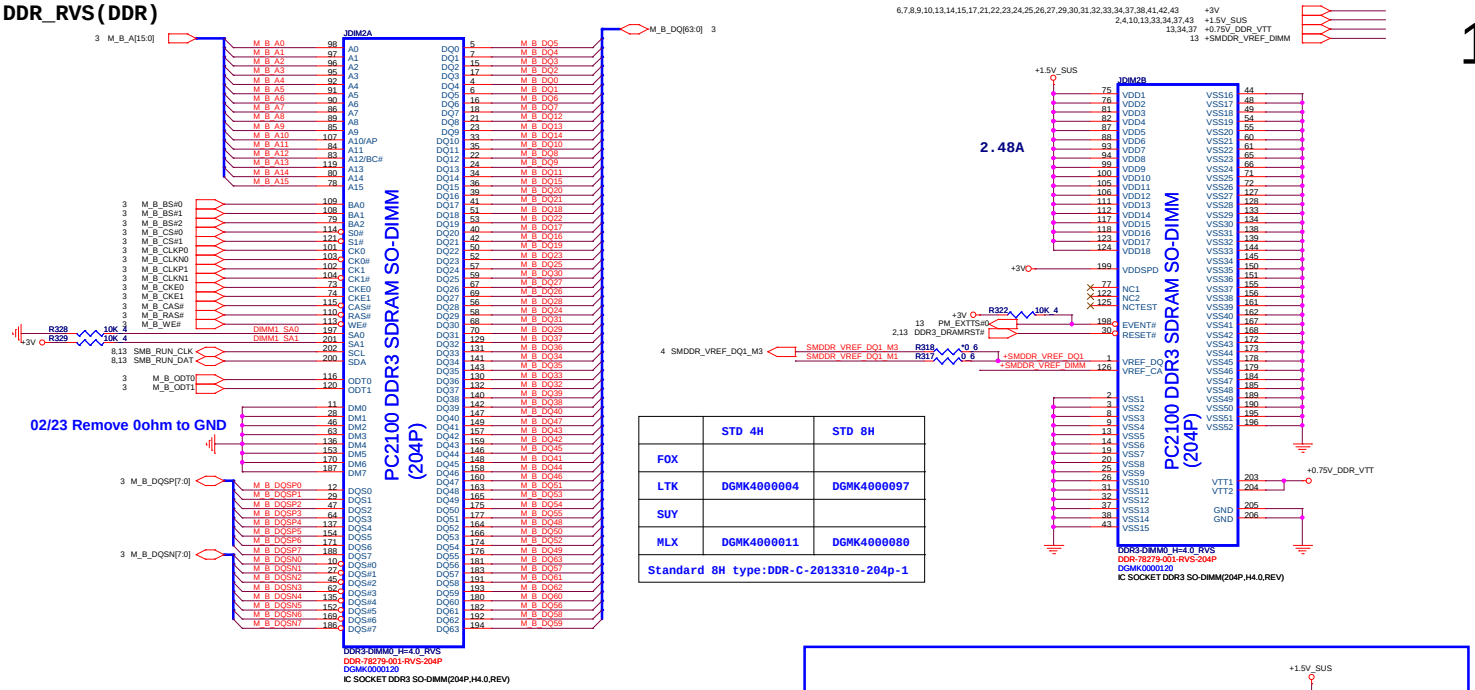
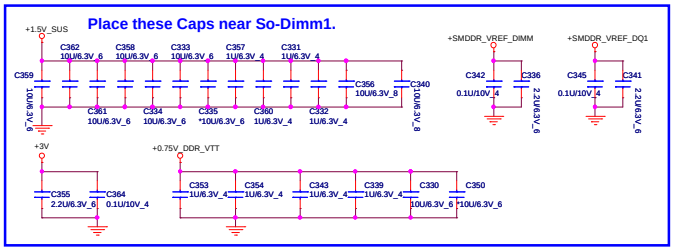
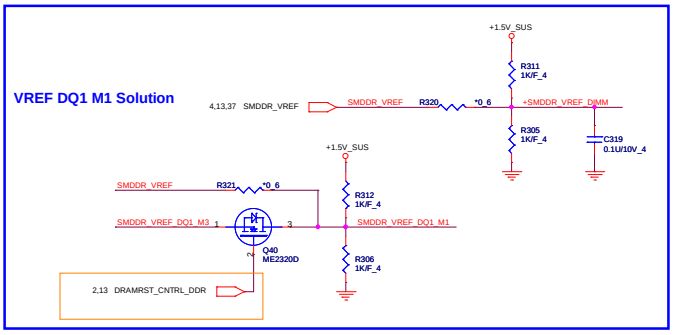
DDR_RVS(DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1





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Quanta Computer Inc.	
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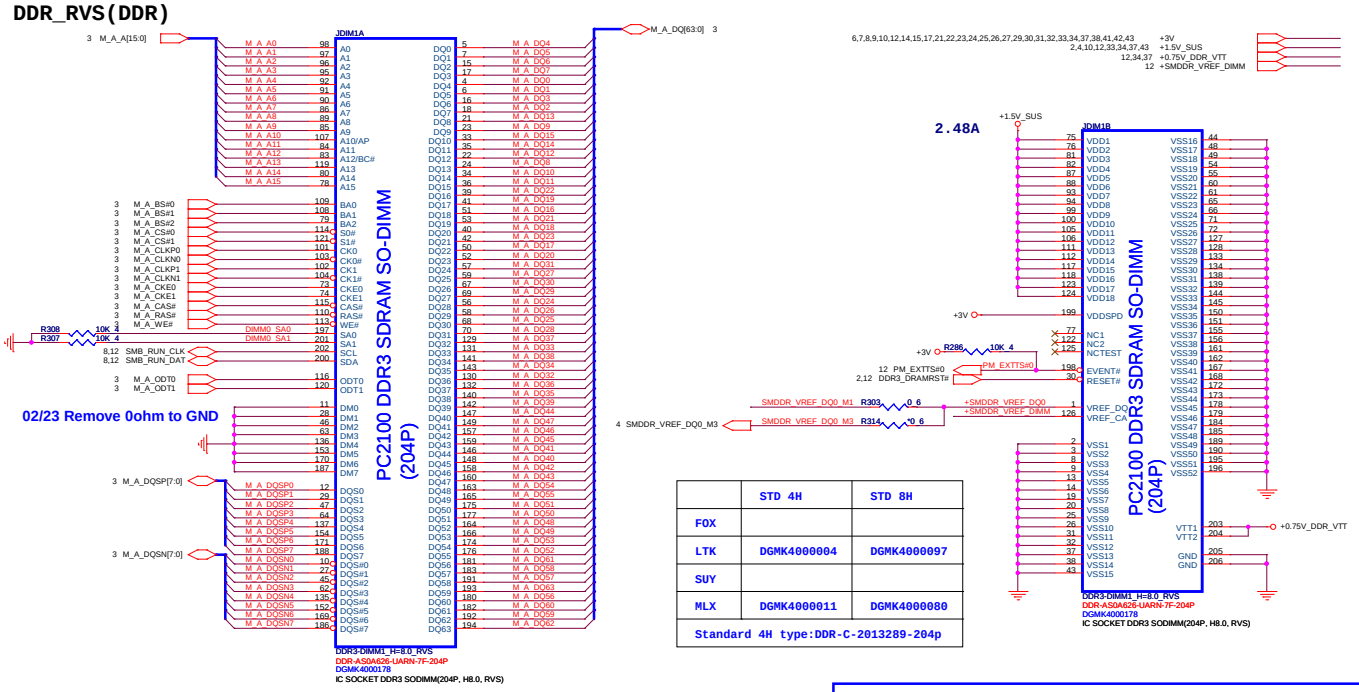
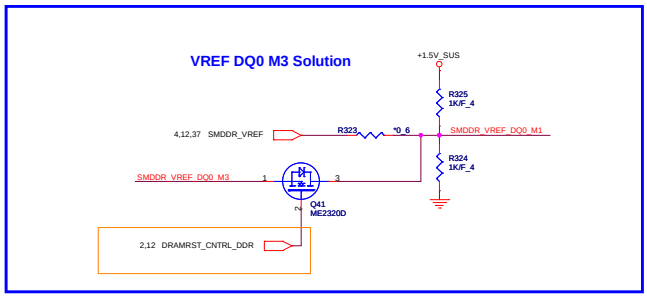
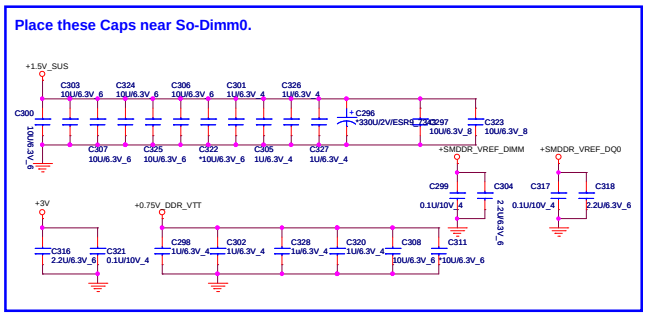
DDR_RVS(DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR-C-2013289-204p





PROJECT : LZ2A

Quanta Computer Inc.

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	DDRIII SO-DIMM-1	1A

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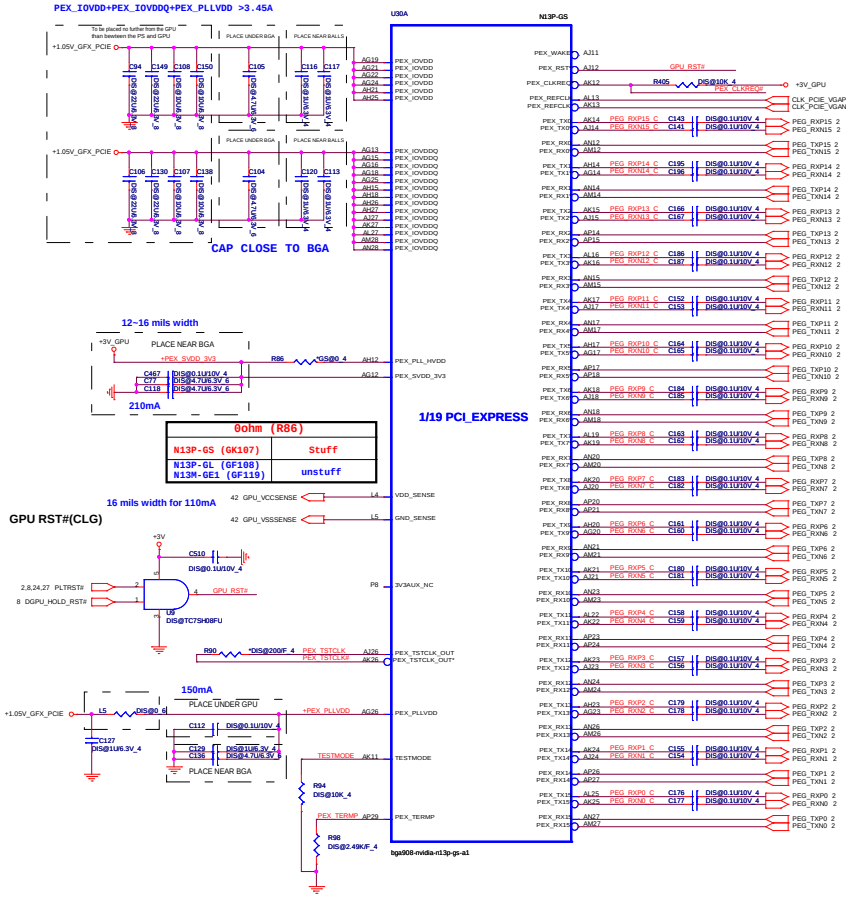
15,16,33,43 +1.05V_GFX_PCIE
17,18,43 +3V_GPU
15,19,20,33,43 +1.5V_GPU
6,7,8,9,10,12,13,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
18,33,42 GFX_CORE

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A



0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tPEX_VDD > 0
- tIFPx_IOVDD ≥ 0
- tIFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

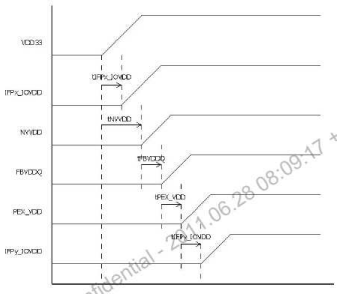


Figure 17. Recommended Power On Sequencing Order

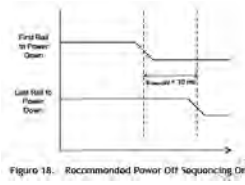
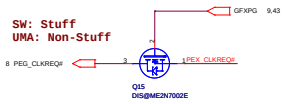


Figure 18. Recommended Power Off Sequencing Order

For power-down sequency

PEG CLK detect



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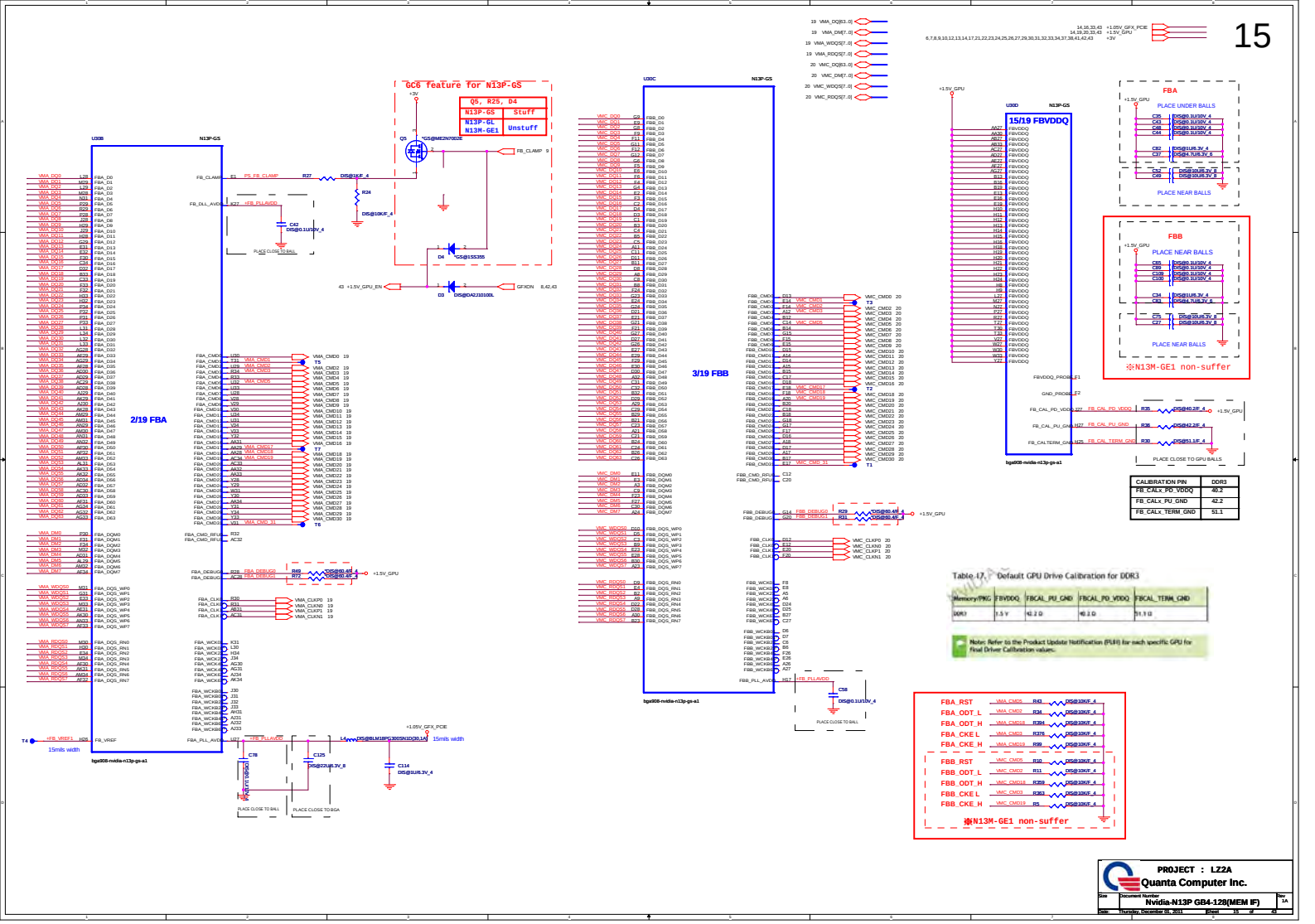

Table 17 Default GPU Drive Calibration for DDR3

Memory/PNG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3	1.5 V	42.2 Ω	40.2 Ω	51.1 Ω

Note: Refer to the Product Update Notification (PUN) for each specific GPU for final Driver Calibration values.

CALIBRATION PIN	DDR3
FB_CAL_PD_VDDQ	40.2
FB_CAL_PU_GND	42.2
FB_CALX_TERM_GND	51.1

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Quanta Computer Inc.
Nvidia-N13P GB4-128(MEM IF)
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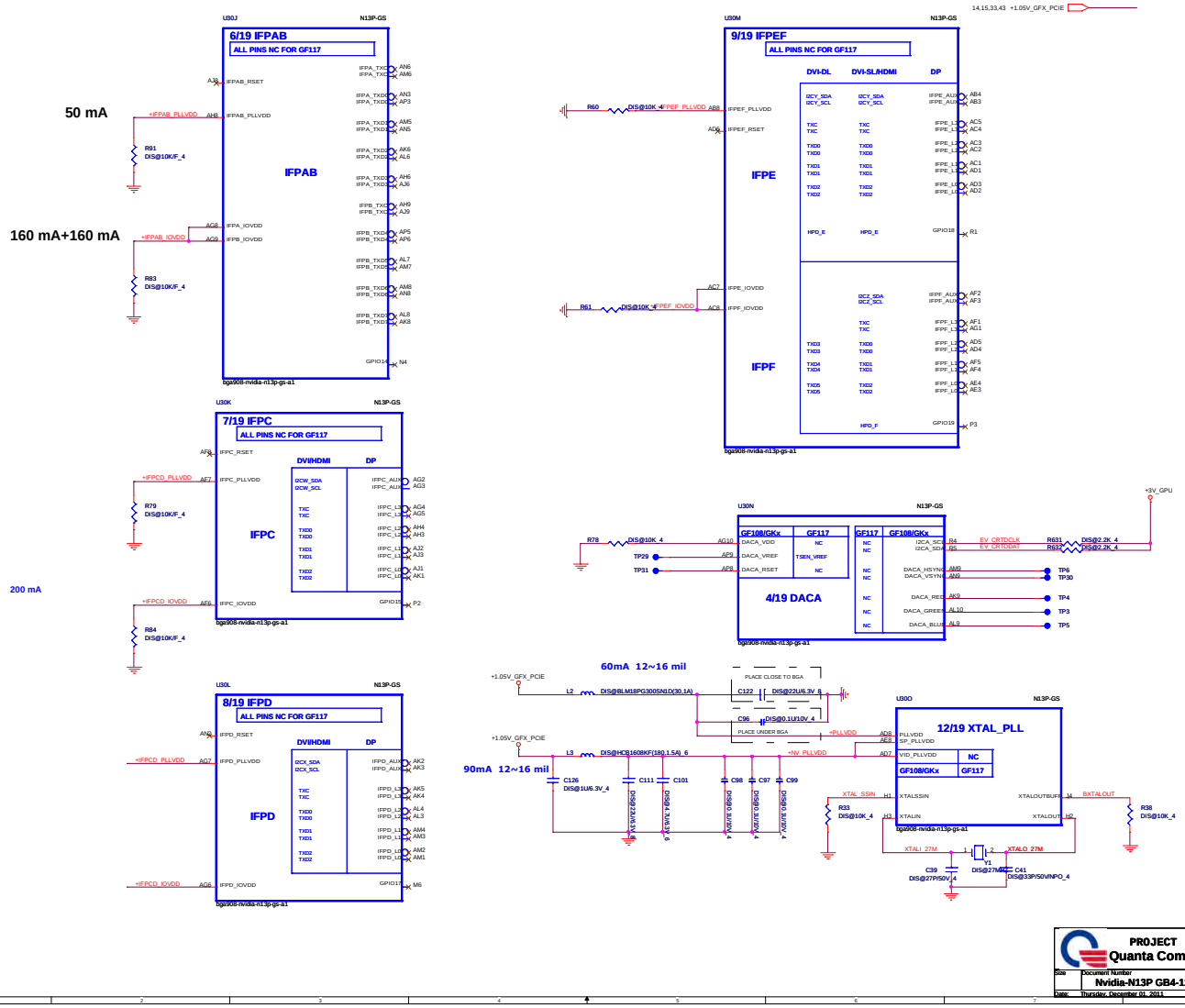

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Quanta Computer Inc.

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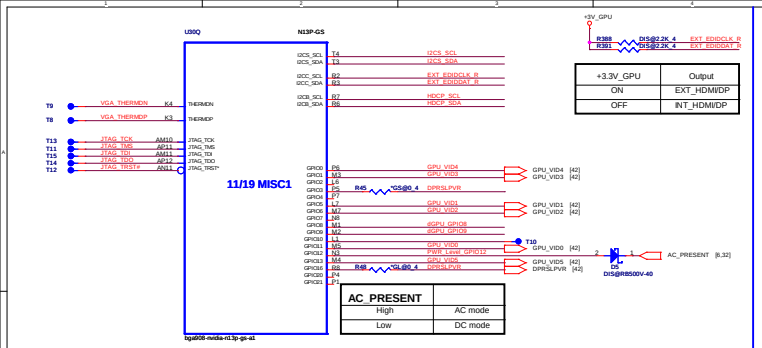
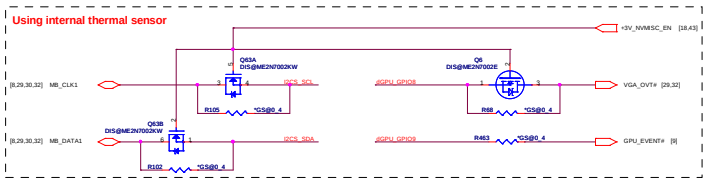


+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP

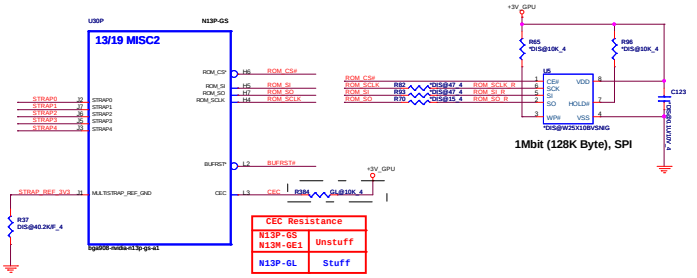
AC_PRESENT	
High	AC mode
Low	DC mode



	Q5,Q63, R81,R104	R68,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor



CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PES/-GL/-MS1 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/-GS/-LP and N14P-Q1/-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-MS1.

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_6 BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24993FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402)]
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1% (0402)

VRAM Configuration Table

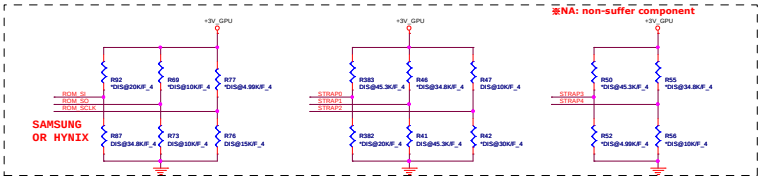
※ROM_SI Strap Bit for RAM Mapping

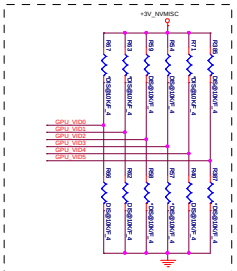
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

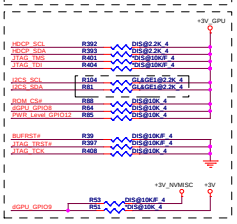
GPU Model Strap Table

GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD





NVVDD Table	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)



GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	O	GPU Core VID VID4
GPIO1	GPU_VID1	O	GPU Core VID VID1
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC or FSI	O	Panel Power Enable or Panel Shedding
GPIO4	LCD_BLEN	O	Panel Backlight Enable
GPIO5	GPU_VID1	O	GPU Core VID VID1
GPIO6	GPU_VID2	O	GPU Core VID VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VID VID0
GPIO12	PWR_LEVEL	I	AC power direct or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VID VID5
GPIO14	HPD_A#	I	Hot Plug Detect for PIPE
GPIO15	HPD_C	I	Hot Plug Detect for PIPE
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for SPD
GPIO18	HPD_E	I	Hot Plug Detect for PIPE
GPIO19	HPD_F	I	Hot Plug Detect for PIPE
GPIO20	Reserved		
GPIO21	Reserved		

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Quanta Computer Inc.
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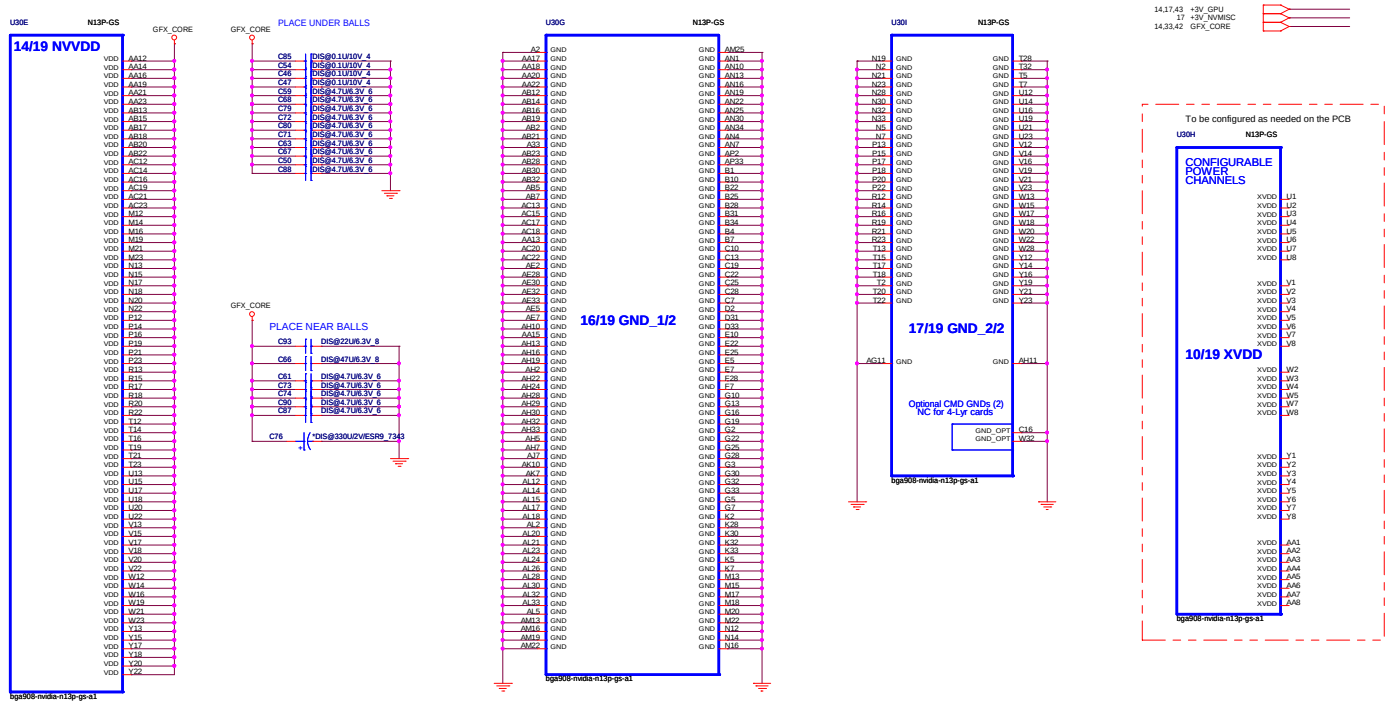

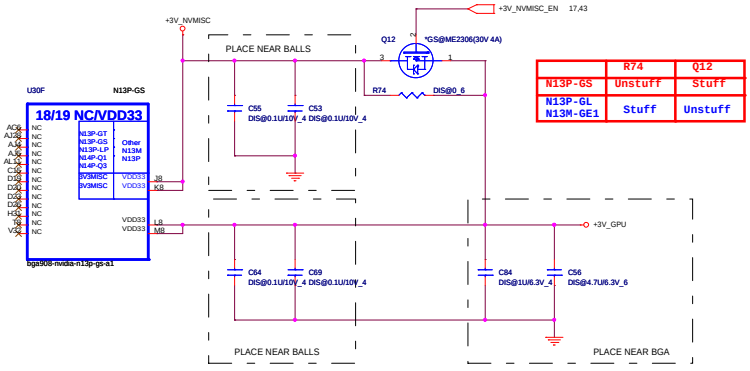

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

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	Nvidia-N13P GB4-128(POWER)	1A
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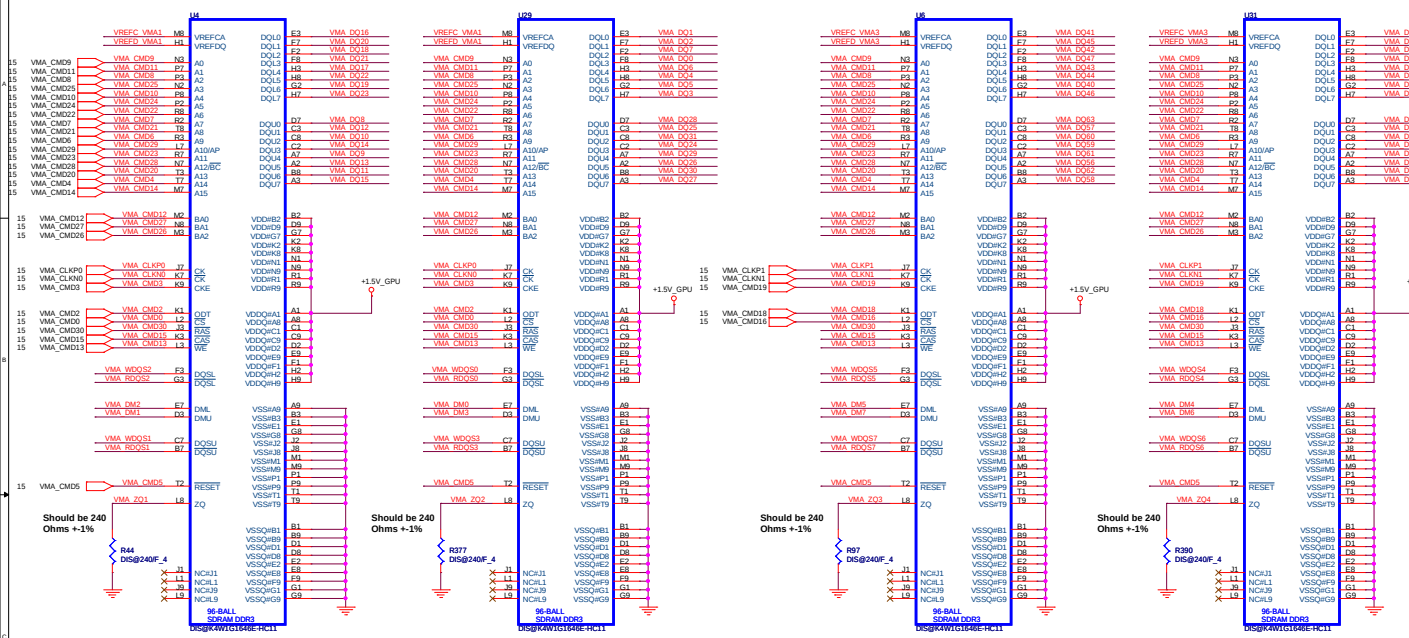
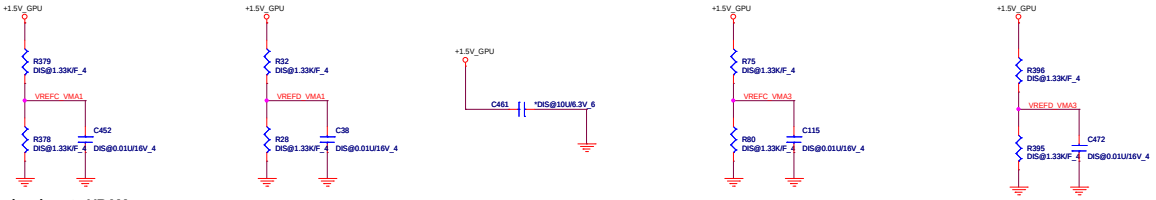
CHANNEL A: 512MB/1024MB DDR3

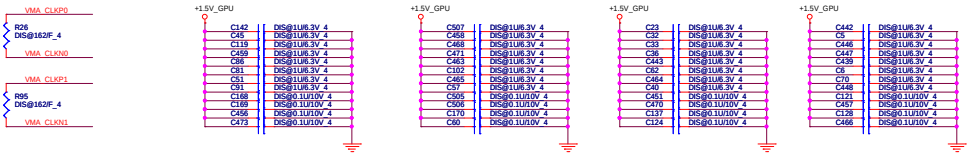
15 VMA_DQ[63..0]
15 VMA_DM[7..0]
15 VMA_WDQS[7..0]
15 VMA_RDQS[7..0]

14,15,20,33,43 +1.5V_GPU





Placement has to be close to VRAM



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	Nvidia-N13P GB4-128(VRAM-1)		1A
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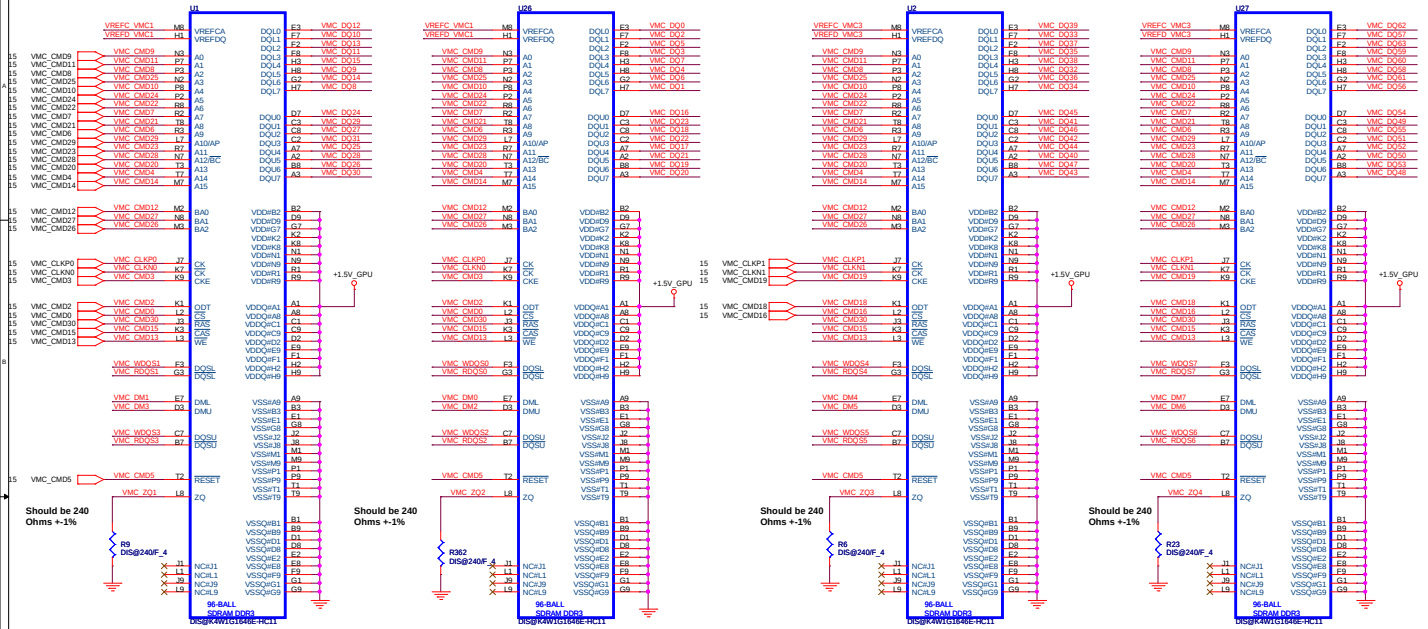
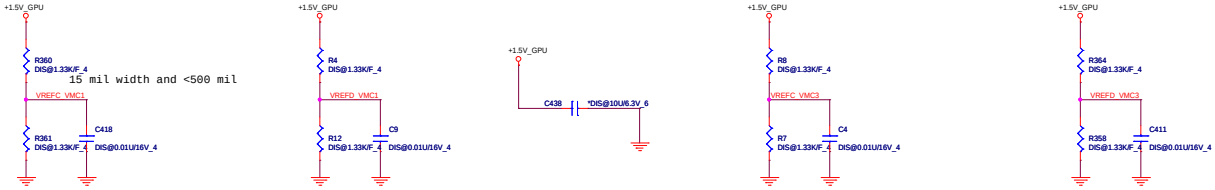
CHANNEL B: 512MB/1024MB DDR3

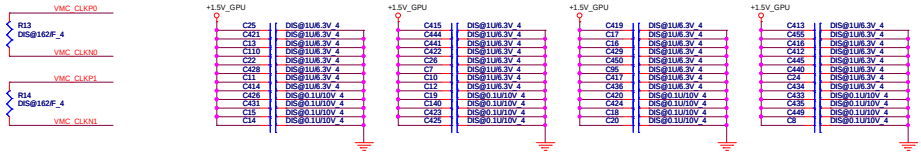
15 VMC_DQ[63..0]
15 VMC_DM[7..0]
15 VMC_WDQS[7..0]
15 VMC_RDQS[7..0]

14,15,19,33,43 +1.5V_GPU





Placement has to be close to VRAM



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6,7,8,9,10,12,13,14,15,17,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
7,10,22,25,26,29,30,33,34 +5V

Change to KL6/BC HDMI CONN

6 INT_HDMI_TXDP2 — C620 0.1U/10V_4 — HDMI_TX2+
6 INT_HDMI_TXDN2 — C619 0.1U/10V_4 — HDMI_TX2-
6 INT_HDMI_TXDP1 — C618 0.1U/10V_4 — HDMI_TX1+
6 INT_HDMI_TXDN1 — C617 0.1U/10V_4 — HDMI_TX1-
6 INT_HDMI_TXDP0 — C616 0.1U/10V_4 — HDMI_TX0+
6 INT_HDMI_TXDN0 — C615 0.1U/10V_4 — HDMI_TX0-
6 INT_HDMI_TXCP — C613 0.1U/10V_4 — HDMI_CLK+
6 INT_HDMI_TXCN — C611 0.1U/10V_4 — HDMI_CLK-

6 INT_HDMI_SCL — INT_HDMI_SCL
6 INT_HDMI_SDA — INT_HDMI_SDA
6 INT_HDMI_HPD — INT_HDMI_HPD

+3V — R551 10K_4 — INT_HDMI_HPD
+3V — R553 10K_4 — HP_DET
Q69A ME2N7002DKW-G
Q69B ME2N7002DKW-G
R549 20K_4

+3V — R316 2.2K_4, R297 2.2K_4 — INT_HDMI_SCL, INT_HDMI_SDA
Q43 DMN5L06K-7
Q39 DMN5L06K-7
+5V — R313 2.2K_4, R568 2.2K_4
+5V — FUSE_1.1A_6V_POLY — F2 — HDMIC_5V
HP_DET
C668 *68p/50V_4
C669 *68p/50V_4
C667 0.1U/10V_4

HDMI Hot-PLUG to EC and GPU

CN16 CONN_HDMI

HDMI_TX2+	1	D2+	SHELL1 20
	2	D2 Shield	SHELL2 21
HDMI_TX2-	3	D2-	
HDMI_TX1+	4	D1+	
	5	D1 Shield	
HDMI_TX1-	6	D1-	
HDMI_TX0+	7	D0+	
	8	D0 Shield	
HDMI_TX0-	9	D0-	
HDMI_CLK+	10	CK+	
	11	CK Shield	
HDMI_CLK-	12	CK-	
	13	CE Remote	
	14	NC	
HDMI_DDC_CLK	15	DDC CLK	
HDMI_DDC_DAT	16	DDC DATA	
	17	GND	
HDMIC_5V	18	+5V	
HP_DET	19	HP DET	SHELL3 22 SHELL4 23

R315 590/F_4 — HDMI_TX2+
R310 590/F_4 — HDMI_TX2-
R304 590/F_4 — HDMI_TX1+
R302 590/F_4 — HDMI_TX1-
R300 590/F_4 — HDMI_TX0+
R298 590/F_4 — HDMI_TX0-
R294 590/F_4 — HDMI_CLK+
R291 590/F_4 — HDMI_CLK-
SC51 0.1U/10V_4
3 HDMI_F
Q42 2N7002K
+5V — 2

For ESD

U39 *CM1225

HDMI_TX2+	6	NC	CH4 5 HDMI_TX2+
HDMI_TX2-	7	NC	CH3 4 HDMI_TX2-
	8	GND	GND 3
HDMI_TX1+	9	NC	CH2 2 HDMI_TX1+
HDMI_TX1-	10	NC	CH1 1 HDMI_TX1-

U38 *CM1225

HDMI_TX0+	6	NC	CH4 5 HDMI_TX0+
HDMI_TX0-	7	NC	CH3 4 HDMI_TX0-
	8	GND	GND 3
HDMI_CLK+	9	NC	CH2 2 HDMI_CLK+
HDMI_CLK-	10	NC	CH1 1 HDMI_CLK-

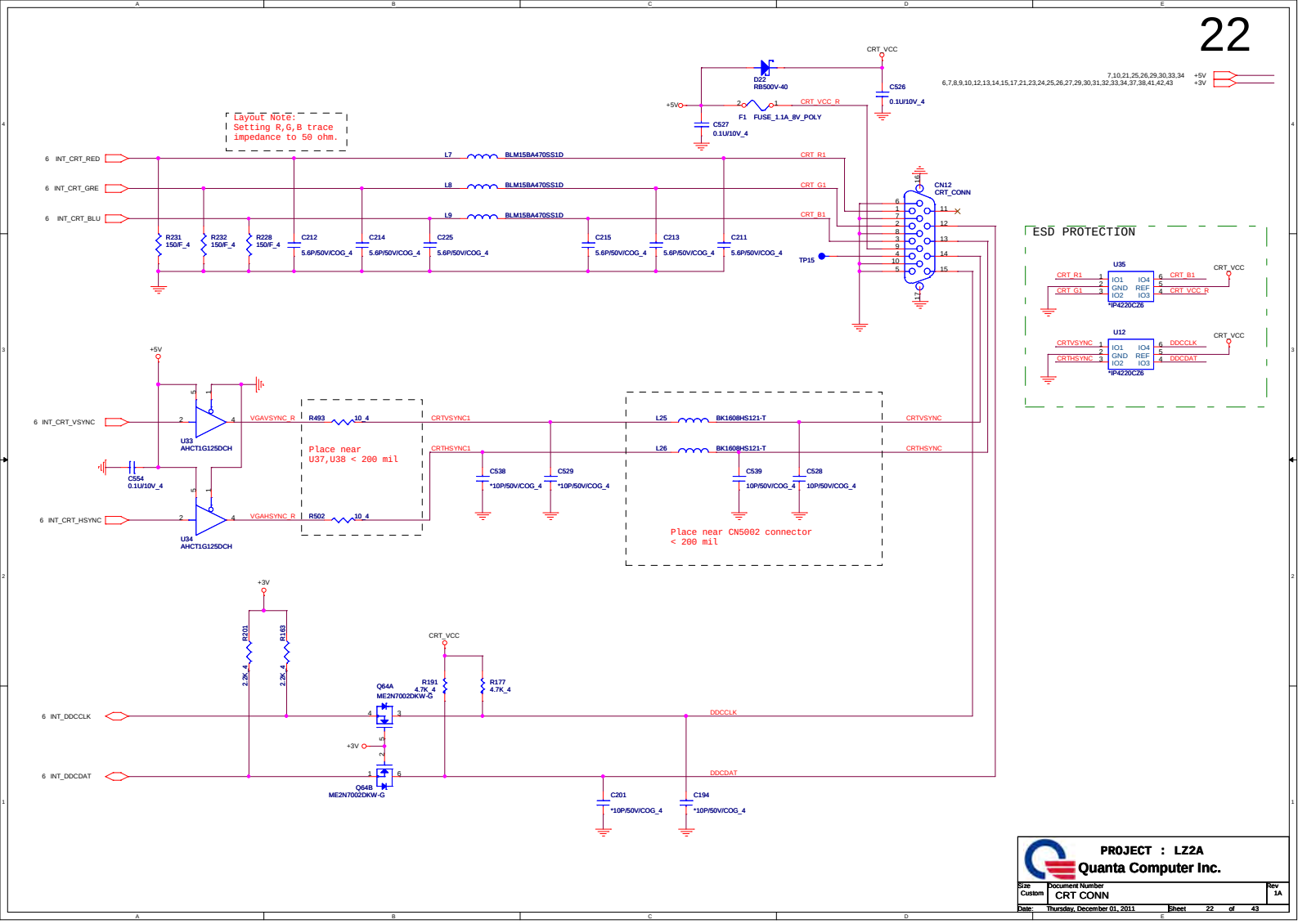
U37 *CM1225

HDMI_DDC_DAT	6	NC	CH4 5 HDMI_DDC_DAT
HDMI_DDC_CLK	7	NC	CH3 4 HDMI_DDC_CLK
	8	GND	GND 3
HDMIC_5V	9	NC	CH2 2 HDMIC_5V
HP_DET	10	NC	CH1 1 HP_DET

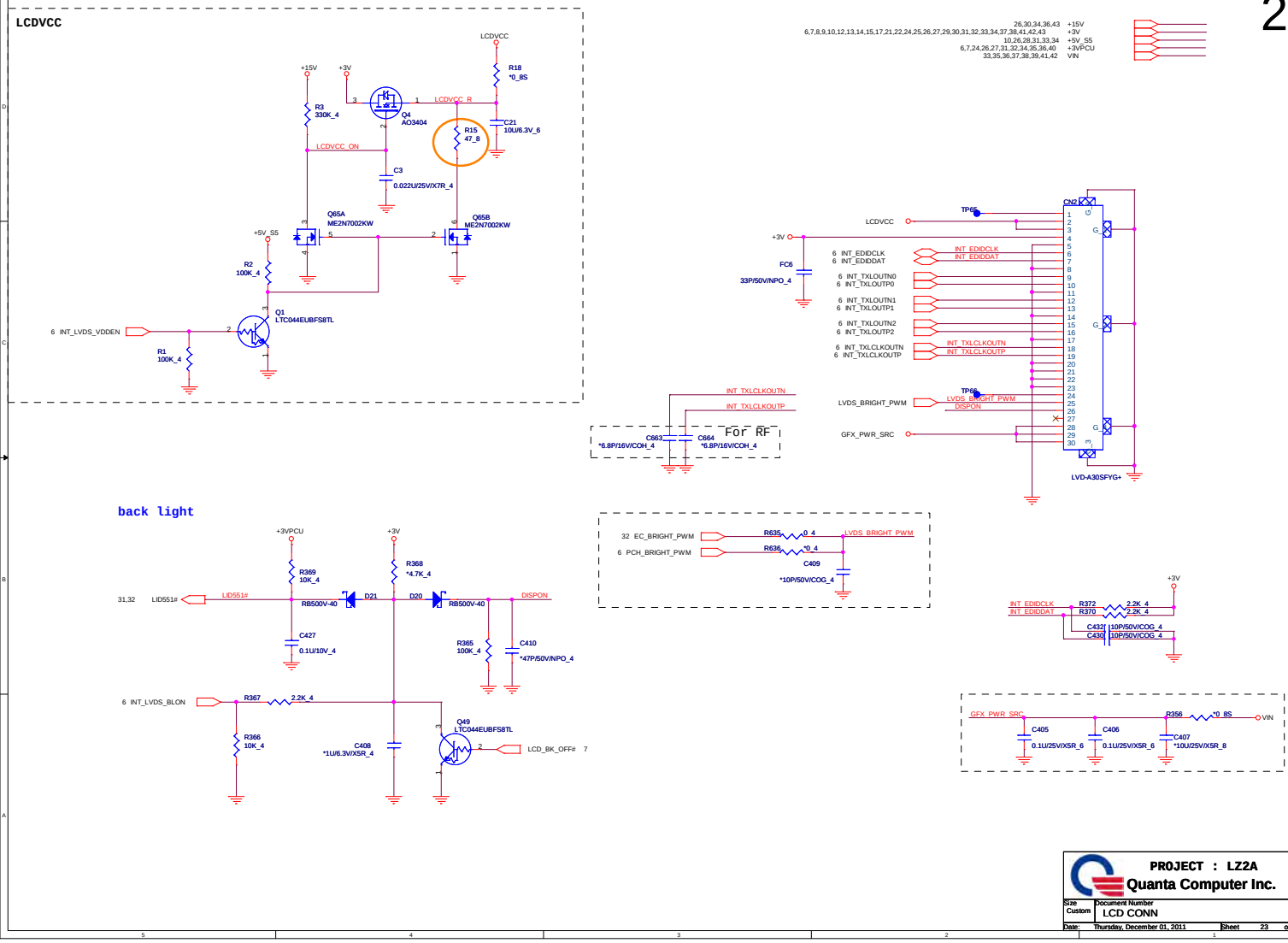
EMI reserve for HDMI

HDMI_TX2+ — R574 140/F_4 — HDMI_TX2-
HDMI_TX1+ — R573 140/F_4 — HDMI_TX1-
HDMI_TX0+ — R572 140/F_4 — HDMI_TX0-
HDMI_CLK+ — R569 140/F_4 — HDMI_CLK-

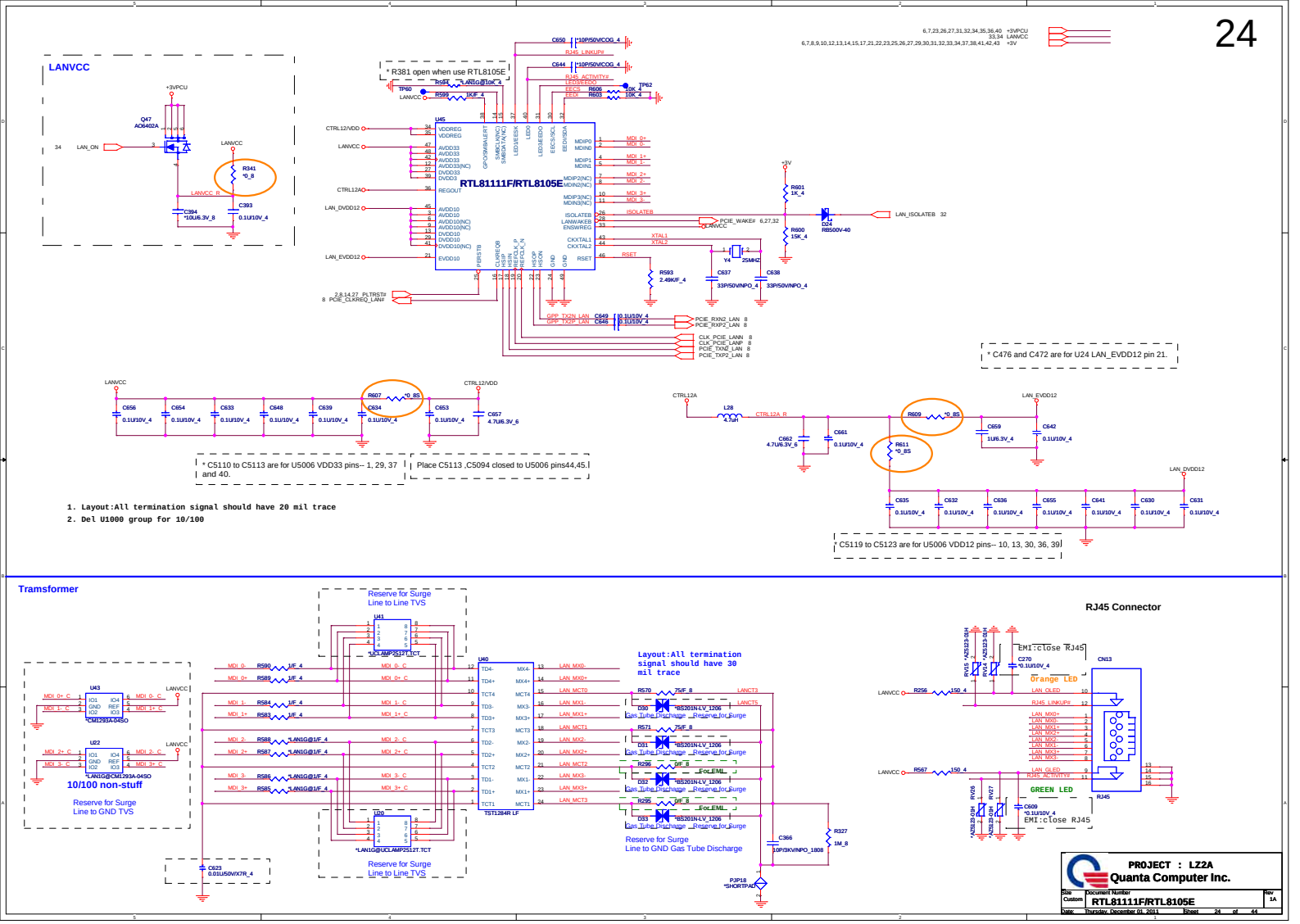
PROJECT : LZ2A
Quanta Computer Inc.
Size: Custom | Document Number: Madison_LVDS/HDMI/CRT switchable | Rev: 1A
Date: Thursday, December 01, 2011 | Sheet 21 of 43



PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: CRT CONN	Rev: 1A
Date: Thursday, December 01, 2011	Sheet 22 of 43	



PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: LCD CONN		Rev: 1A
Date: Thursday, December 01, 2011	Sheet 23 of 43		

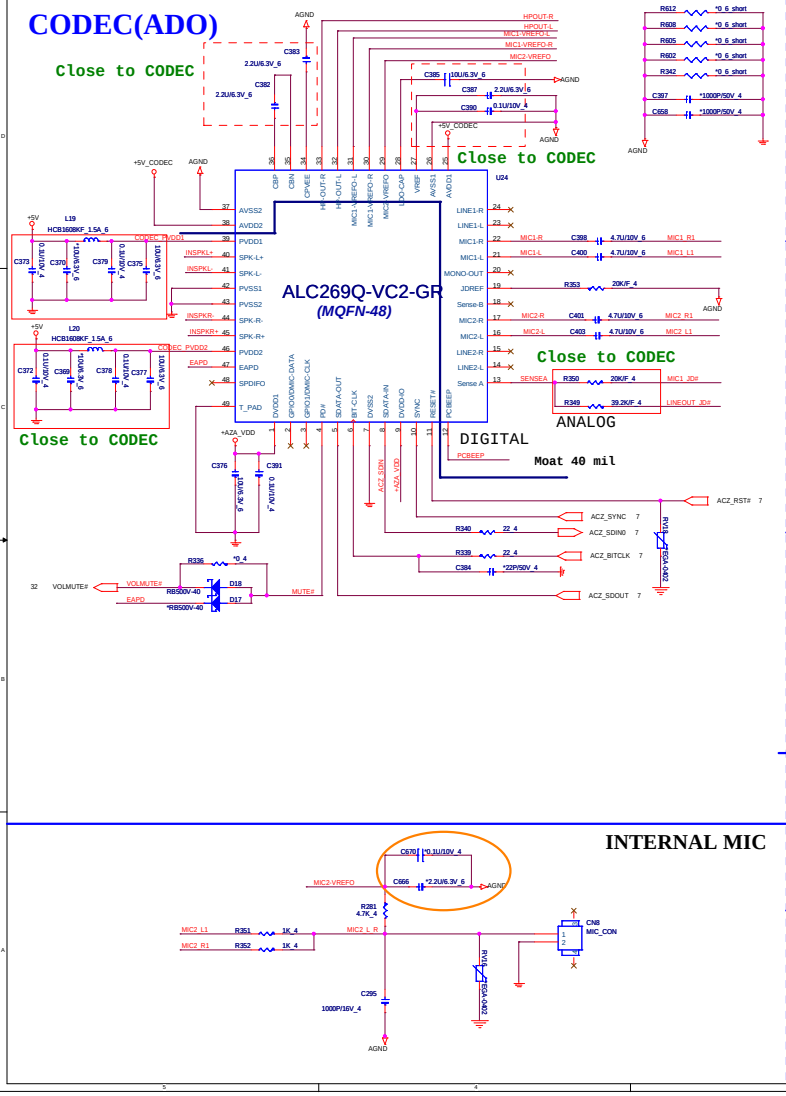


PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL81111F/RTL8105E	1A

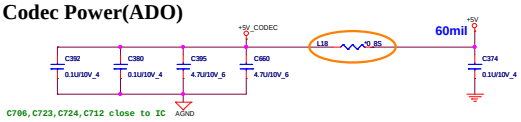
Date: Thursday, December 01, 2011 Sheet 24 of 44

CODEC(ADO)

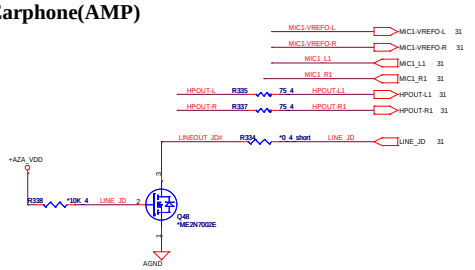


INTERNAL MIC

Codec Power(ADO)

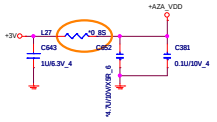


Earphone(AMP)

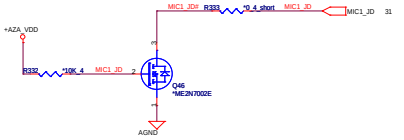


HDA Power(ADO)

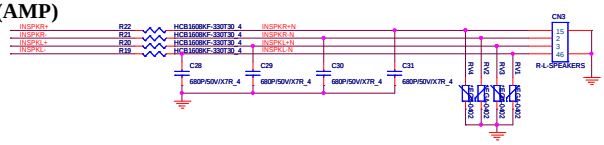
*Intel HDA Either +1.5V_S5 or +3V_S5



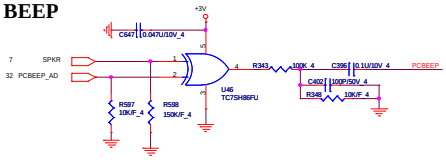
System MIC(AMP)



Speaker(AMP)

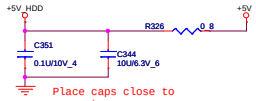


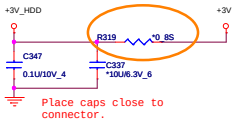
PC BEEP

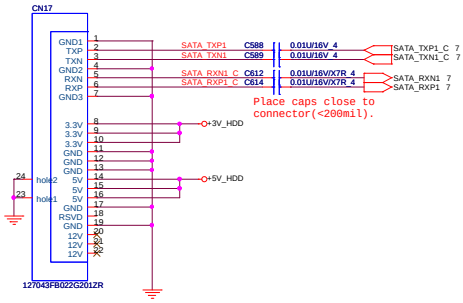


PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: ALC269/MIC/Line out	Rev: 3A
Date: Monday, December 05, 2011	Sheet 25 of 43	

SATA HDD Connector.

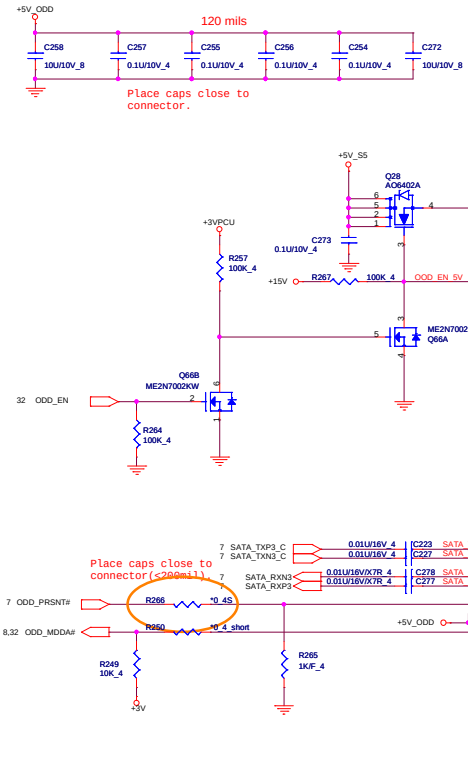






SATA ODD Connector.

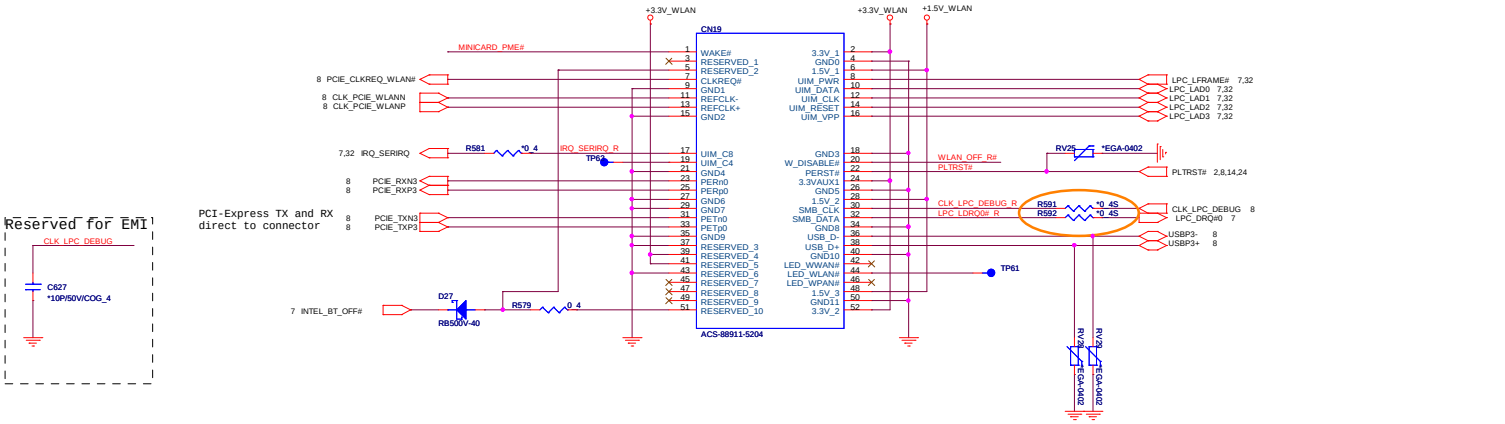
7,10,21,22,25,29,30,33,34 +5V
6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43 +3V
10,34,35,36,37,38,39,40,41,42,43 +5VPCU
6,7,23,24,27,31,32,34,35,36,40 +3VPCU

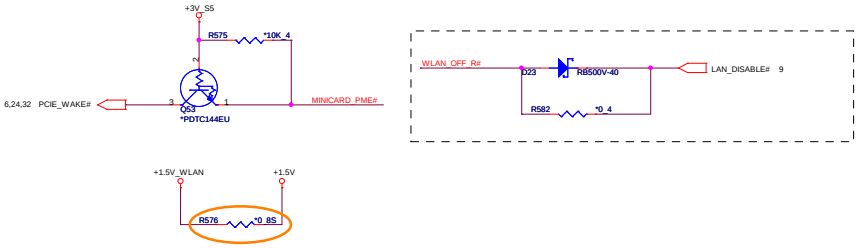


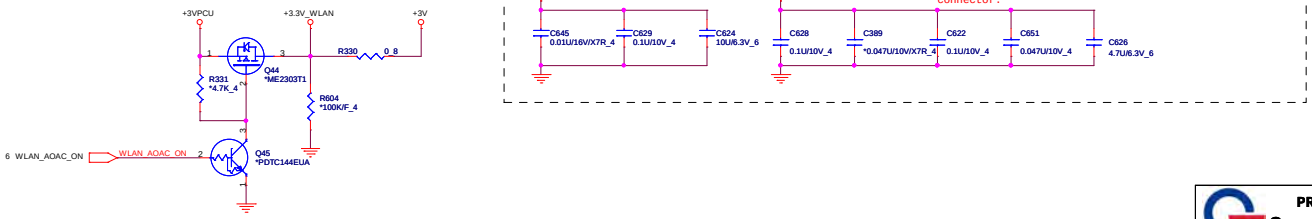
PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: SATA HDD/CD-ROM		Rev: 1A
Date: Thursday, December 01, 2011		Sheet 26 of 43	

MiniCard WLAN connector

2,6,7,8,9,10,31,34 +3V_S5
4,10 +1.5V
6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,29,30,31,32,33,34,37,38,41,42,43 +3V



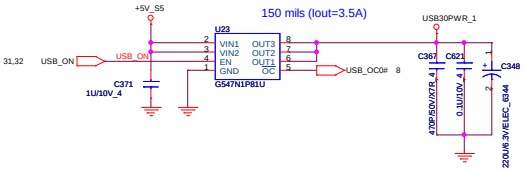


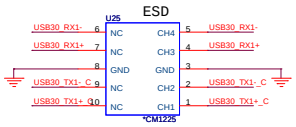


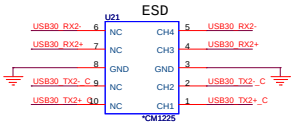
PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: USB2.0*2/WLAN/BT	Rev: 1A
Date: Thursday, December 01, 2011	Sheet 27 of 43	

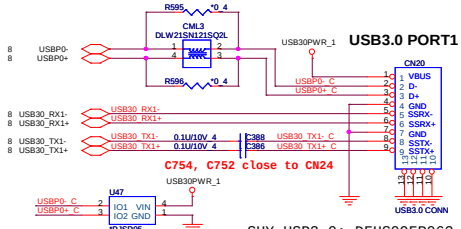
10,23,26,31,33,34 +5V_S5

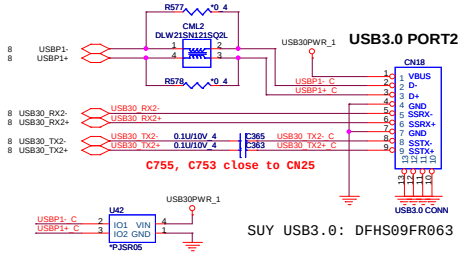
USB3.0*2



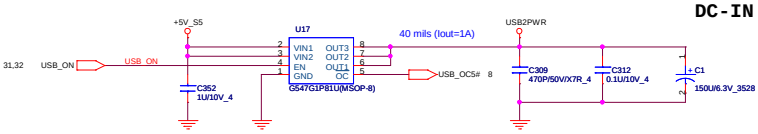


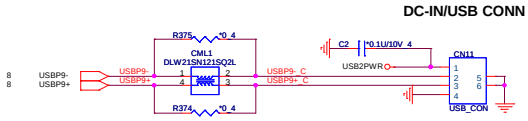


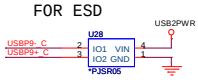




USB2.0*1

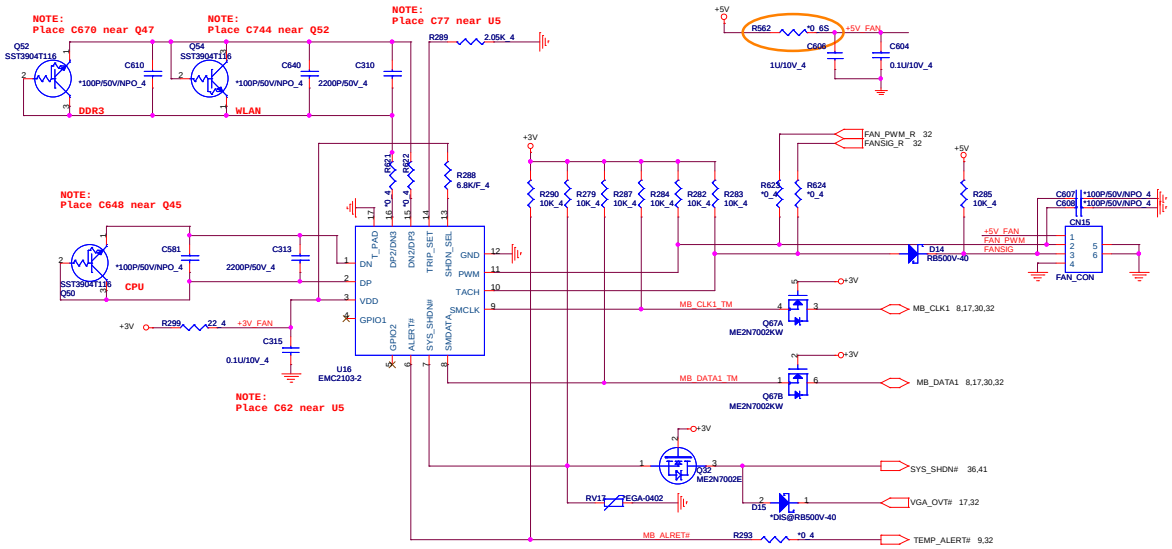






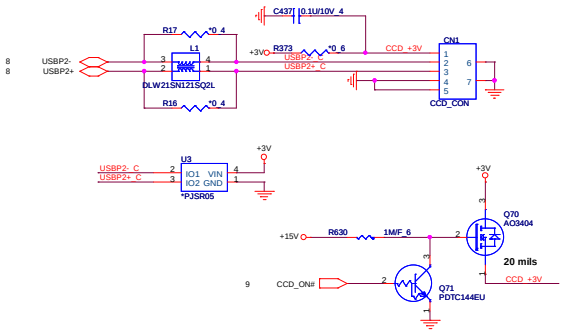
PROJECT : LZ2A Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 *1	Rev: 1A
Date: Thursday, December 01, 2011	Sheet 28 of 43	

FAN CONTROL



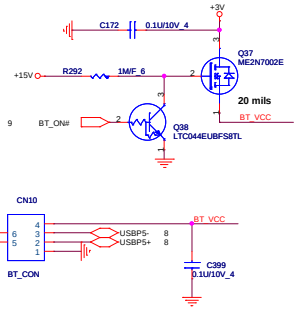
PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: FAN /THERMAL	Rev: 1A
Date: Thursday, December 01, 2011	Sheet 29 of 43	

CCD BOARD

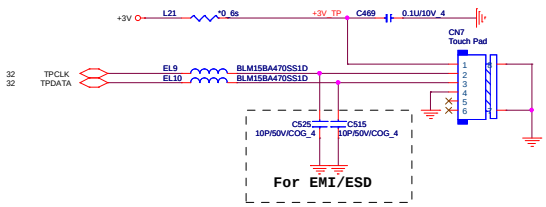


6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,31,32,33,34,37,38,41,42,43 +3V
7,10,21,22,25,26,29,33,34 +5V
23,26,34,36,43 +15V

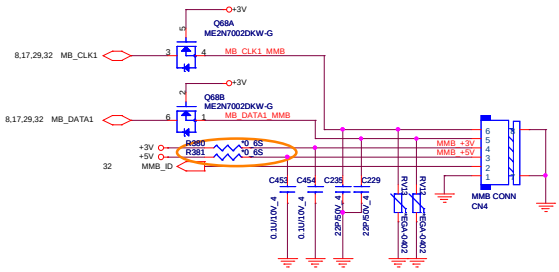
BLUETOOTH



Touch pad



MMB

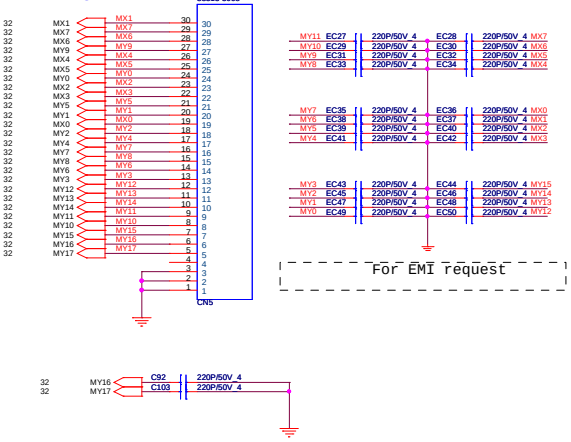


PROJECT : LZ2A
Quanta Computer Inc.

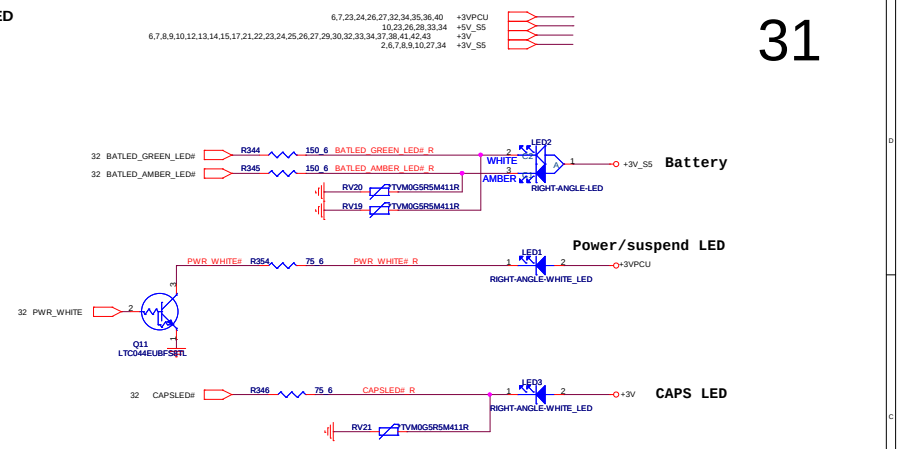
Size	Document Number	Rev
Custom	CCD/TP/BT/MMB	1A

Date: Thursday, December 01, 2011 Sheet 30 of 43

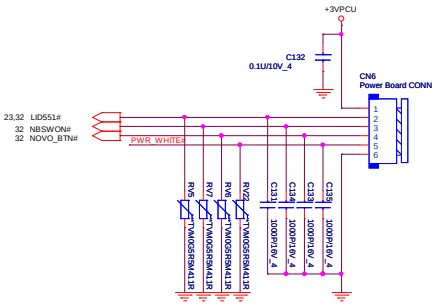
KEYBOARD



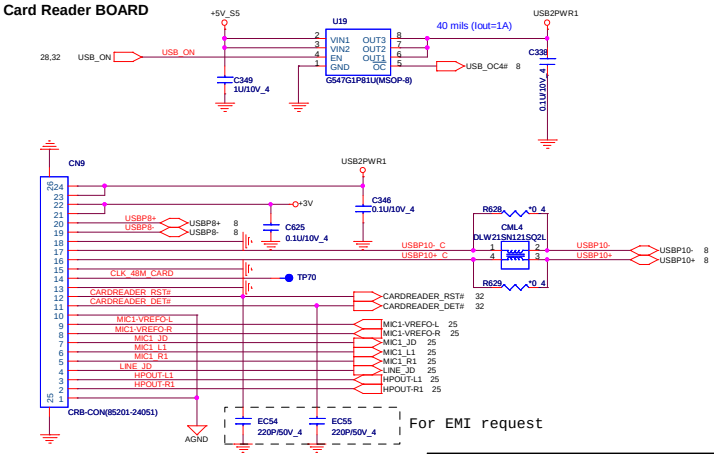
LED



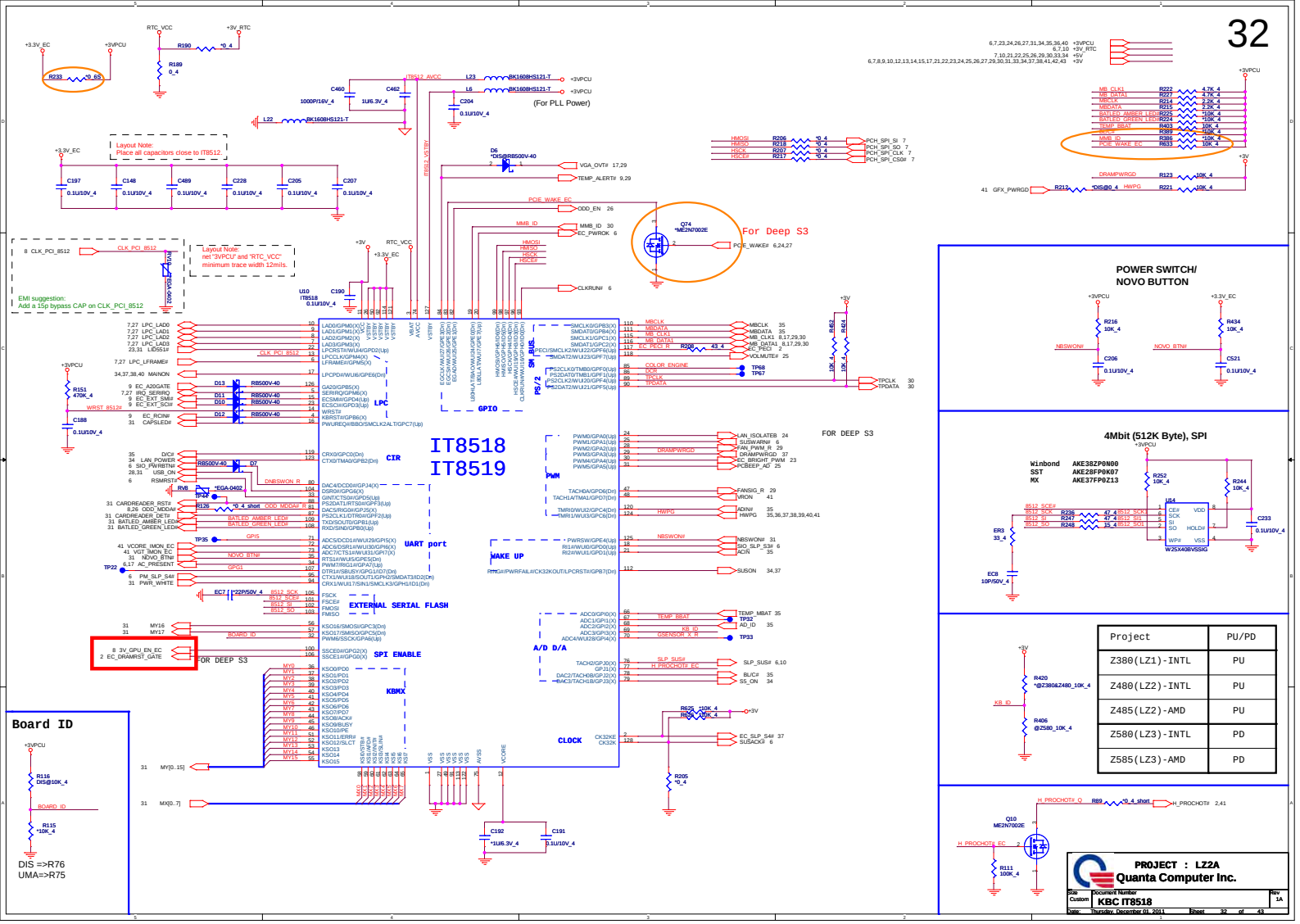
POWER BOARD



Card Reader BOARD



PROJECT : LZ2A		
Quanta Computer Inc.		
Size: Custom	Document Number: KB/PB/LED/CRB	Rev: 1A
Date: Friday, December 02, 2011	Sheet 31 of 43	



POWER SWITCH/ NOVO BUTTON

4Mbit (512K Byte), SPI

Winbond	AKE38ZP0N00
SST	AKE28FP0K07
MX	AKE37FP0Z13

Board ID

DIS =>R76
UMA=>R75

Project	PU/PD
Z380(LZ1)-INTL	PU
Z480(LZ2)-INTL	PU
Z485(LZ2)-AMD	PU
Z580(LZ3)-INTL	PD
Z585(LZ3)-AMD	PD

PROJECT : LZ2A			
Quanta Computer Inc.			
Size: Custom	Document Number: KBC IT8518		Rev: 1A
Date: Thursday, December 01, 2011	Sheet: 32	of: 43	

Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2
SMT NUT H=4/7mm

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE15 *HG-TIC248BC256D106P2
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2

HOLE4 *H-C86D86N
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N

CPU BKT

HOLE7 *C142D102N
HOLE5 *H-O316X276ID91P2
HOLE3 *H-TC217BC256D118P2
HOLE2 *H-O316X276ID91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

For ESD

+0.85V SC23 SC24 *0.1U/10V_4
+1.8V
+1.05V_GFX_PCIE SC31 SC32 *0.1U/10V_4
+1.05V_PCH
+1.5V_SUS SC29 SC28 *0.1U/10V_4
+1.5V_CPU
+1.5V_SUS SC40 SC39 0.1U/25V_4
VIN
+3V SC33 SC30 0.1U/10V_4
+5V
+VCC_CORE SC9 SC46 0.1U/25V_4
VIN
+1.05V_GFX_PCIE SC4 *0.1U/10V_4
GFX_CORE

+0.85V SC11 SC13 SC12 *0.1U/10V_4
+1.5V_CPU SC27 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+VCC_GFX SC15 SC18 *0.1U/10V_4
+5V SC38 SC25 SC37 0.1U/10V_4

+VCC_GFX SC17 SC16 SC14 *0.1U/10V_4
+1.05V_PCH SC20 SC19 SC21 *0.1U/10V_4
+1.05V_PCH SC49 SC22 SC50 SC47 SC48 *0.1U/10V_4
+1.05V_GFX_PCIE SC6 SC5 *0.1U/10V_4

+VCC_CORE SC8 SC10 *0.1U/10V_4
+1.5V_GPU SC2 SC43 SC3 *0.1U/10V_4
+1.5V_GPU SC7 SC45 *0.1U/10V_4
+1.5V_GPU SC44 SC1 *0.1U/10V_4
+1.5V_SUS SC35 SC34 SC36 *0.1U/10V_4

For EMI

VIN EC6 EC20 EC12 EC25 EC1 EC18 EC2 EC21 EC5 EC3 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS FC2 3.9p/16V/NP0_4
+1.5V_SUS FC1 3.9p/16V/NP0_4
+1.5V_WLAN FC5 47P/50V/NP0_4
+3.3V_WLAN FC3 47P/50V/NP0_4
+5V EC51 EC52 0.1U/10V_4 *0.1U/10V_4

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Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A

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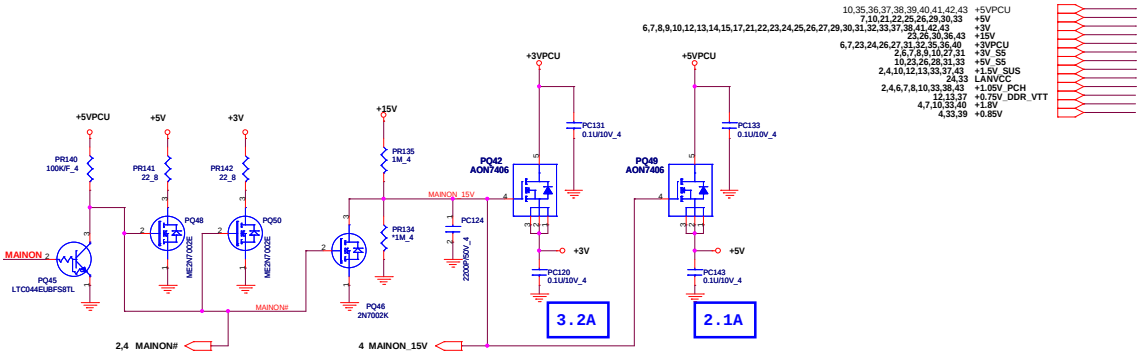
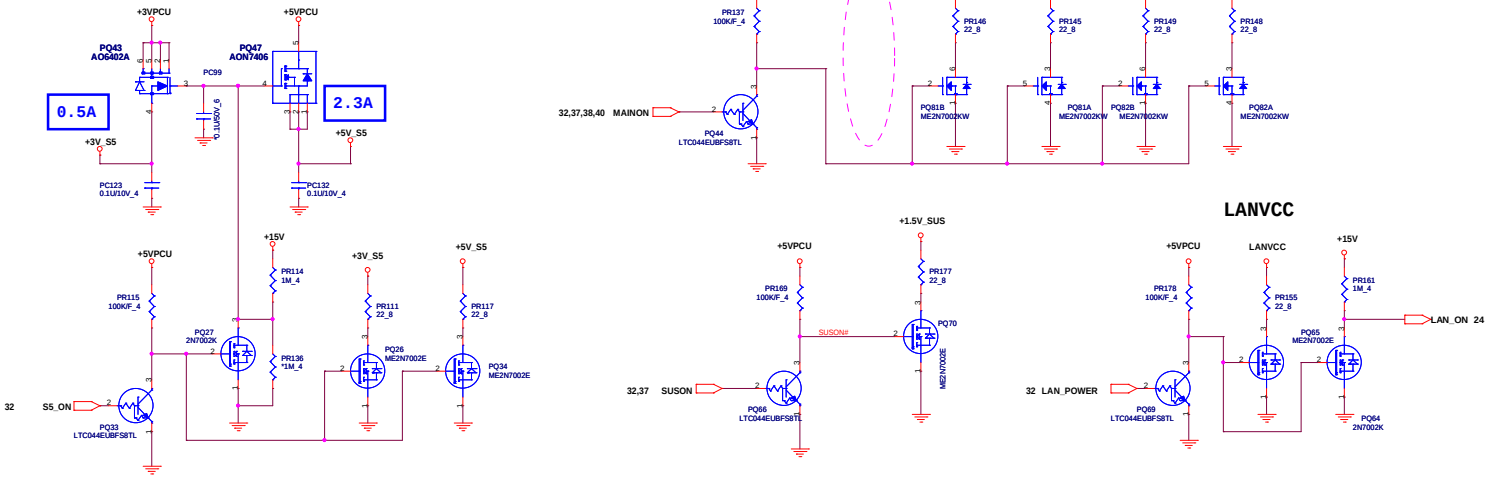
DISCHARGE

+3V, +5V



3V_S5, 5V_S5



LANVCC

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Quanta Computer Inc.

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	Discharge	
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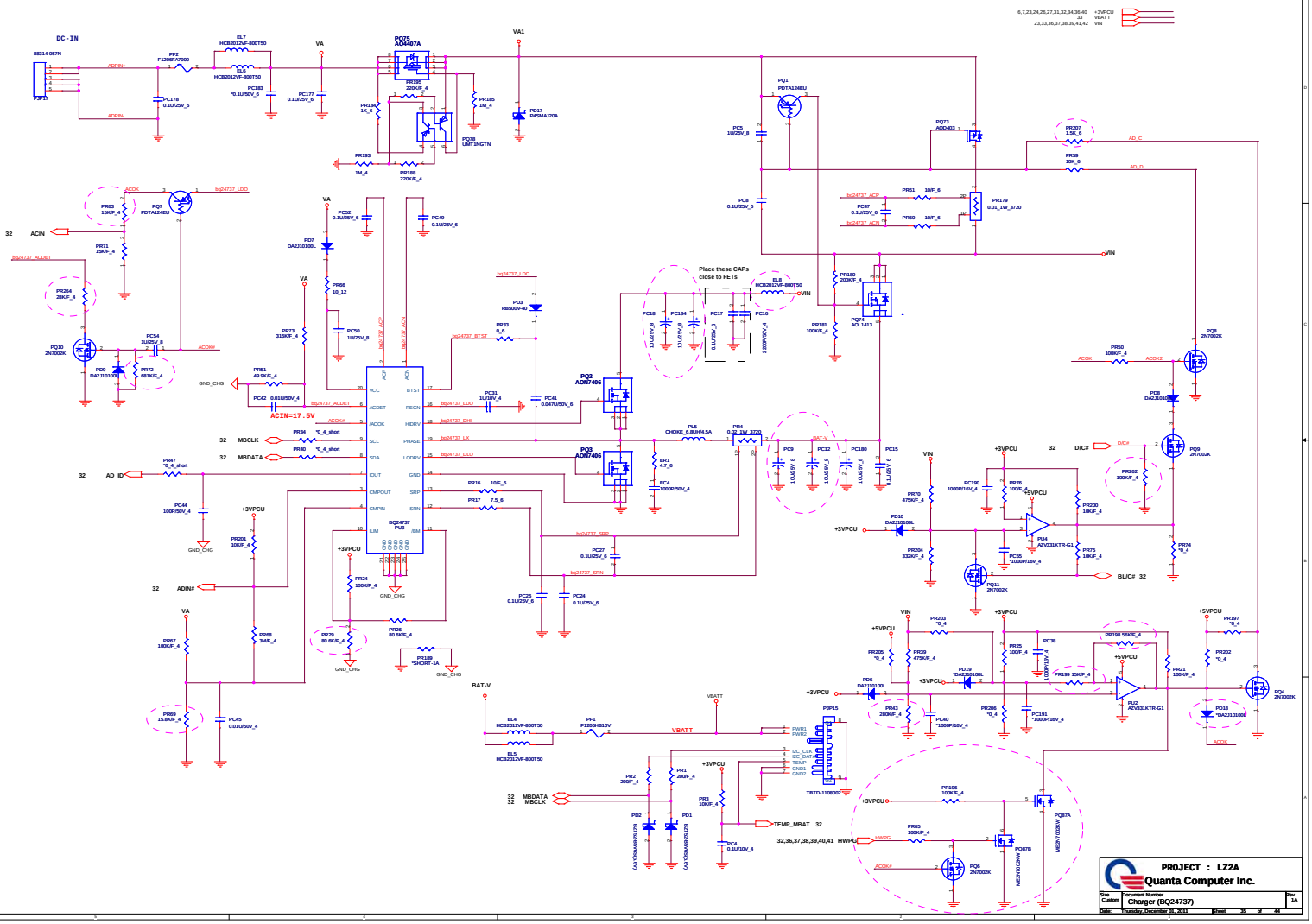
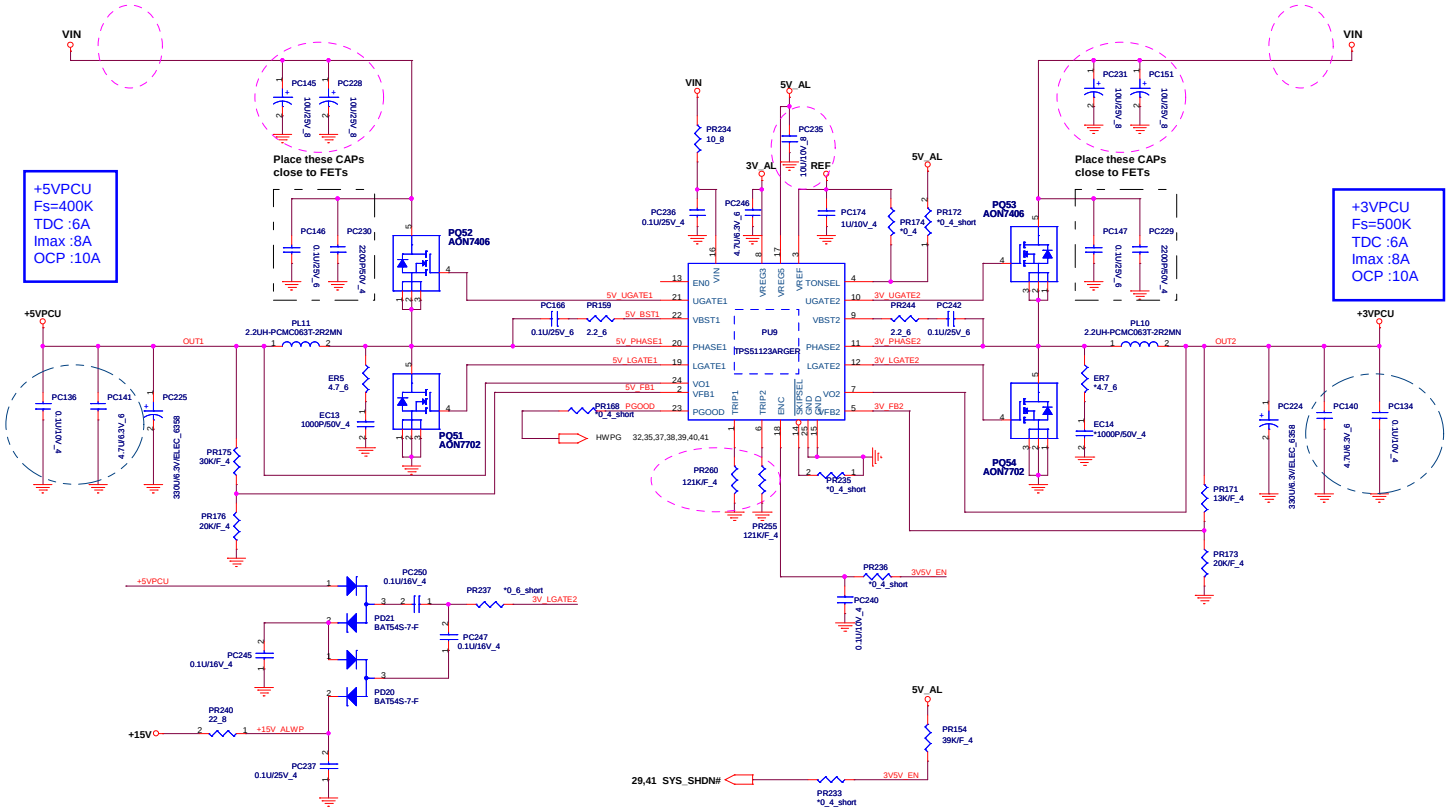

DC-IN
Place these CAPs close to FETs
ACIN=17.5V
PROJECT : LZ2A
Quanta Computer Inc.
Charger (BQ24737)
Thursday, December 08, 2011

23,33,35,37,38,39,41,42 VIN
5V_AL
3V_AL
REF
10,34,35,37,38,39,40,41,42,43 +5VPCU
23,26,30,34,43 +15V
6,7,23,24,26,27,31,32,34,35,40 +3VPCU



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Quanta Computer Inc.			
Size	Document Number		Rev
	3V/5V (TPS51123ARGER)		
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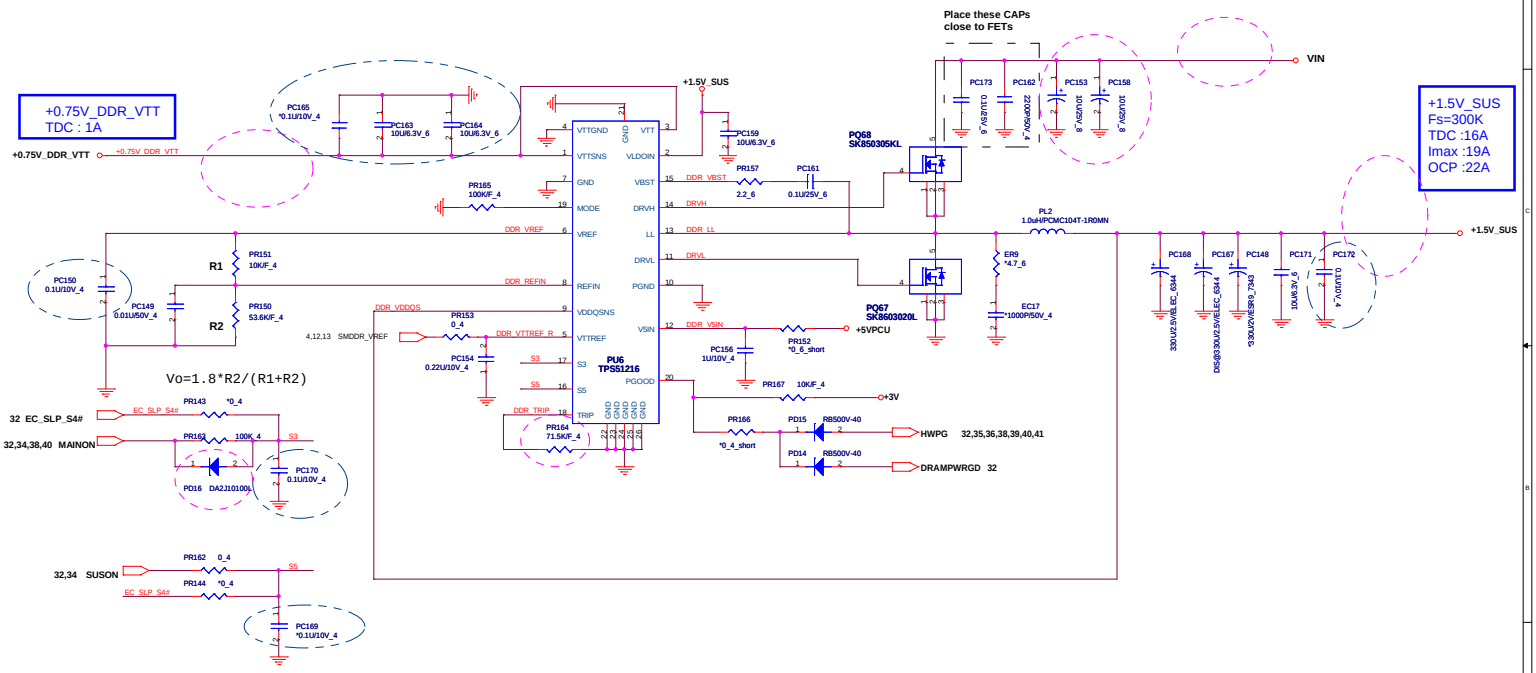
12,13,34 +0.75V_DDR_VTT
23,33,35,36,38,39,41,42 VIN
2,4,10,12,13,33,34,43 +1.5V_SUS



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Quanta Computer Inc.			
Size	Document Number		Rev
	DDR3/0.75V (TPS51216)		
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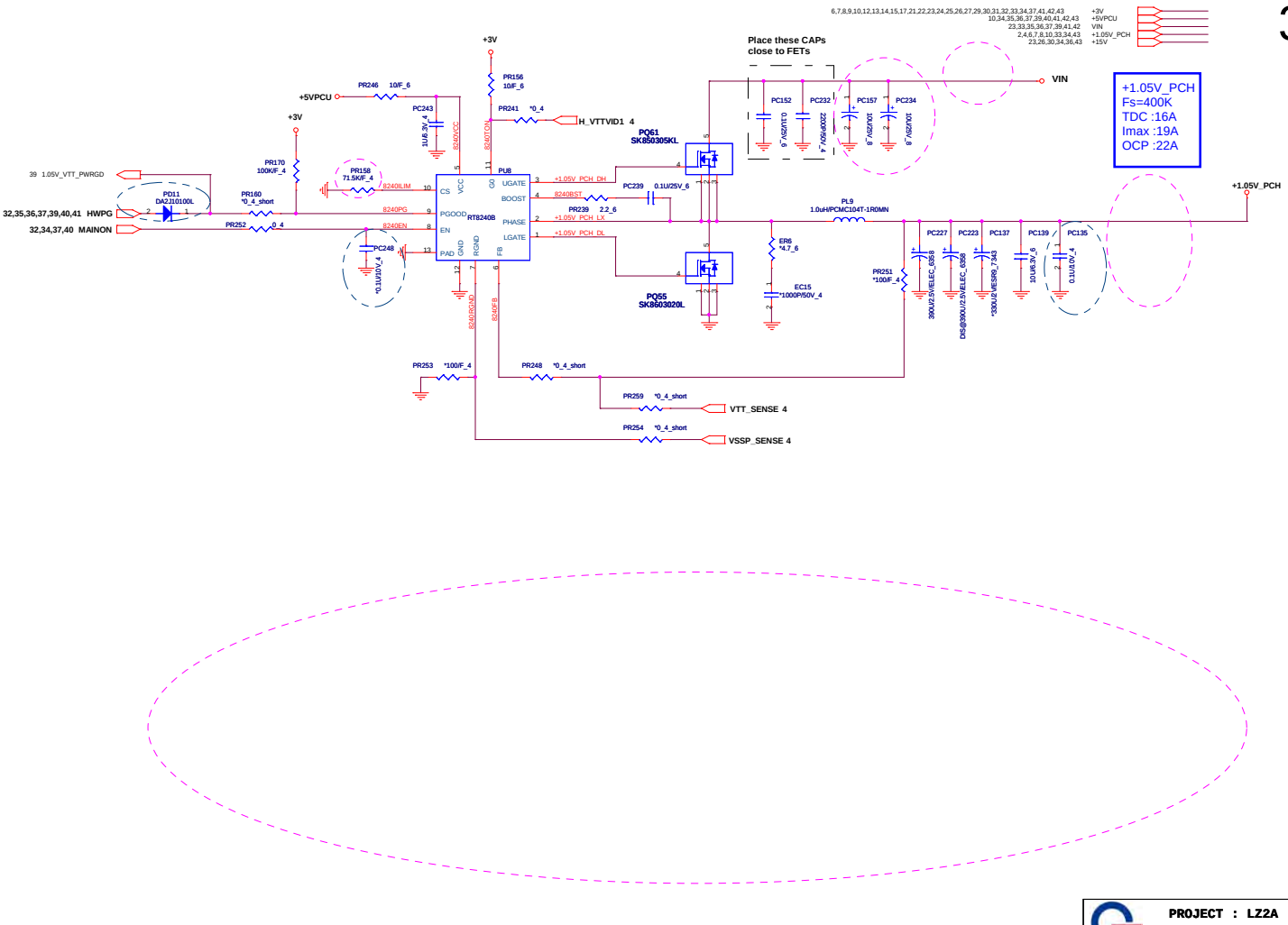

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Quanta Computer Inc.		
Size	Document Number: +1.05V_PCH	Rev
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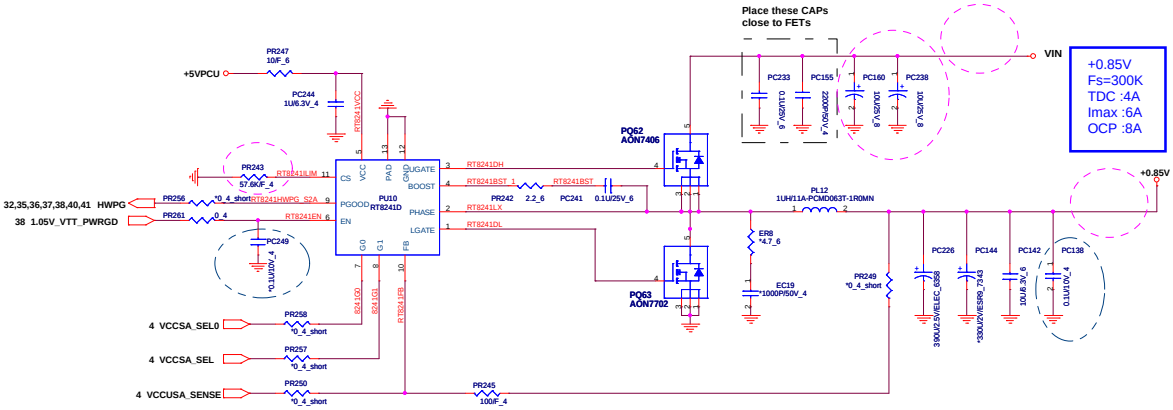
10,34,35,36,37,38,40,41,42,43 +5VPCU
23,33,35,36,37,38,41,42 VIN
4,33,34 +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

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Quanta Computer Inc.

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	VCCSA (RT8241A)	
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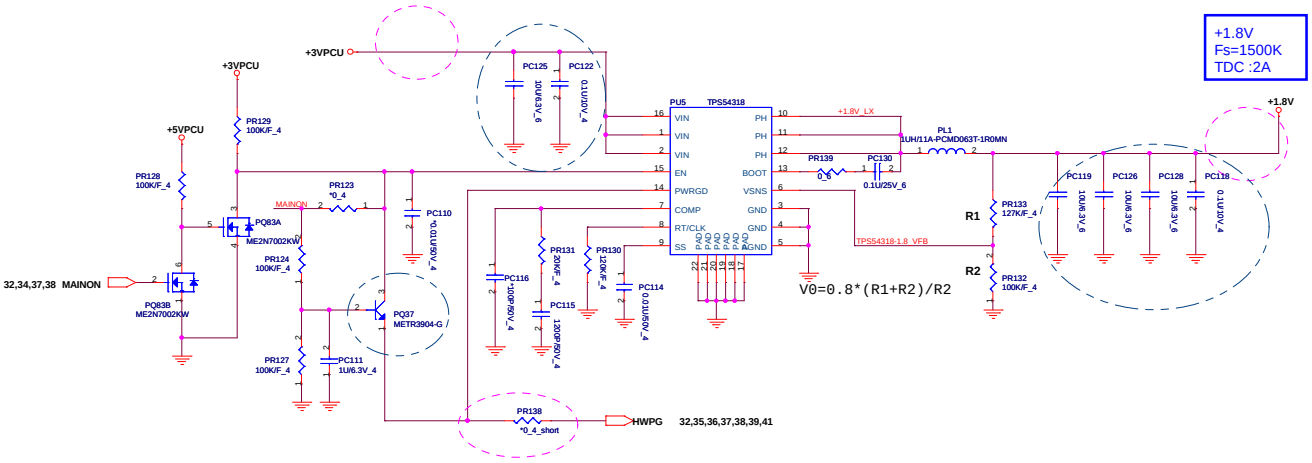
10,34,35,36,37,38,39,41,42,43 +5VPCU
6,7,23,24,26,27,31,32,34,35,36 +3VPCU
4,7,10,33,34 +1.8V



PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
	1.8V (TPS54318)	
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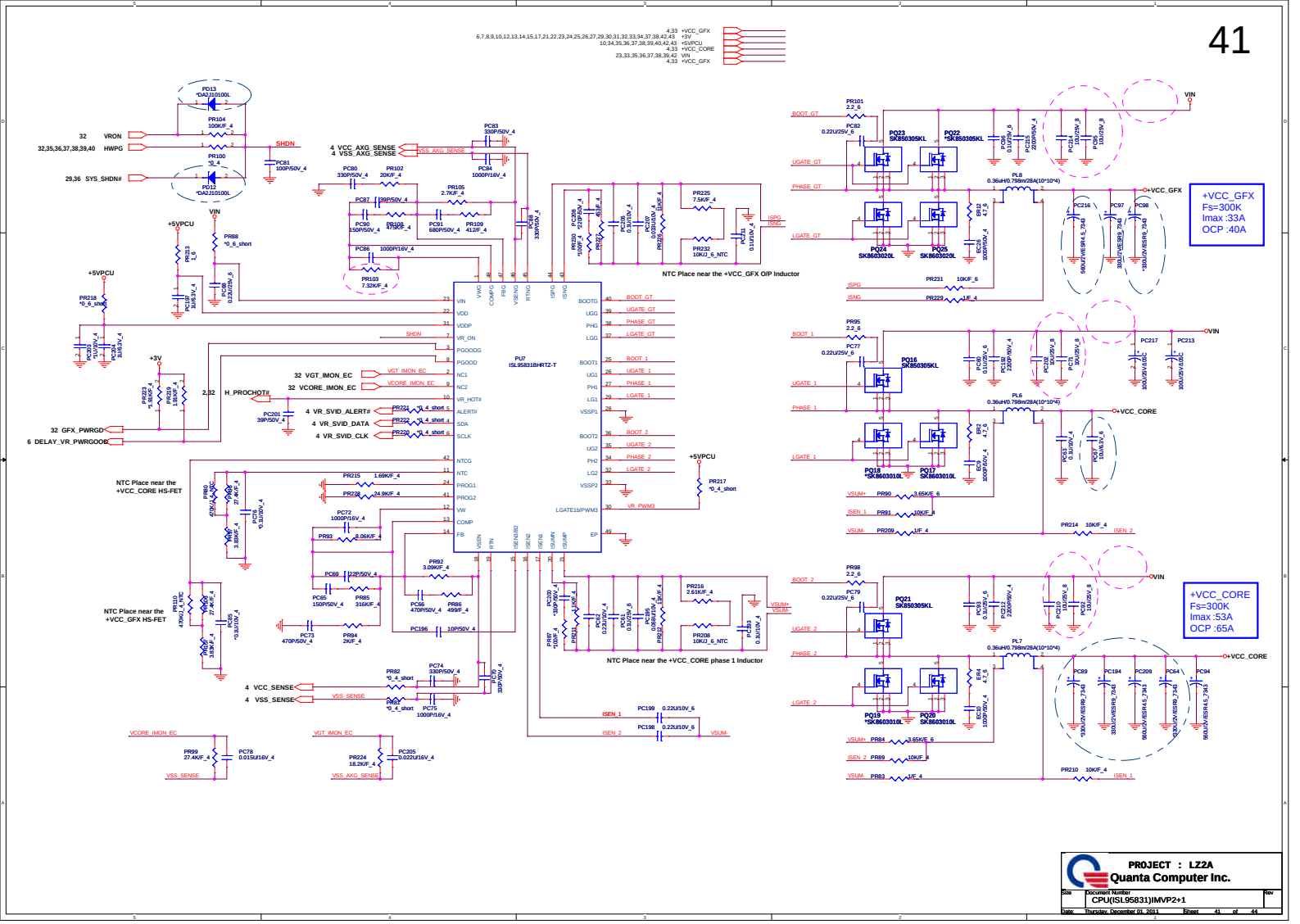

PROJECT :	LZ2A
Quanta Computer Inc.	
Size	Document Number: CPU(ISL95831)IMVP2+1 — Rev
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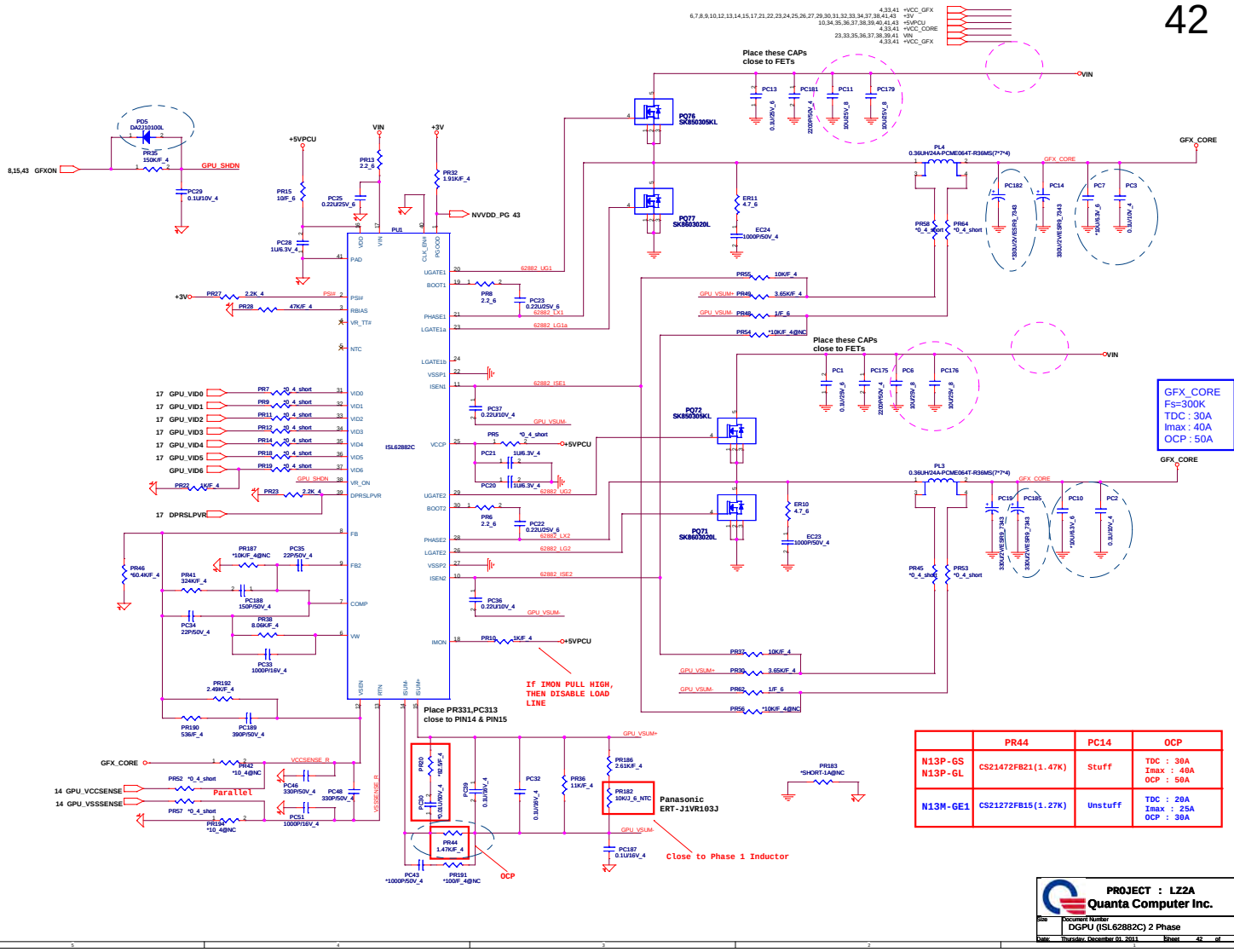
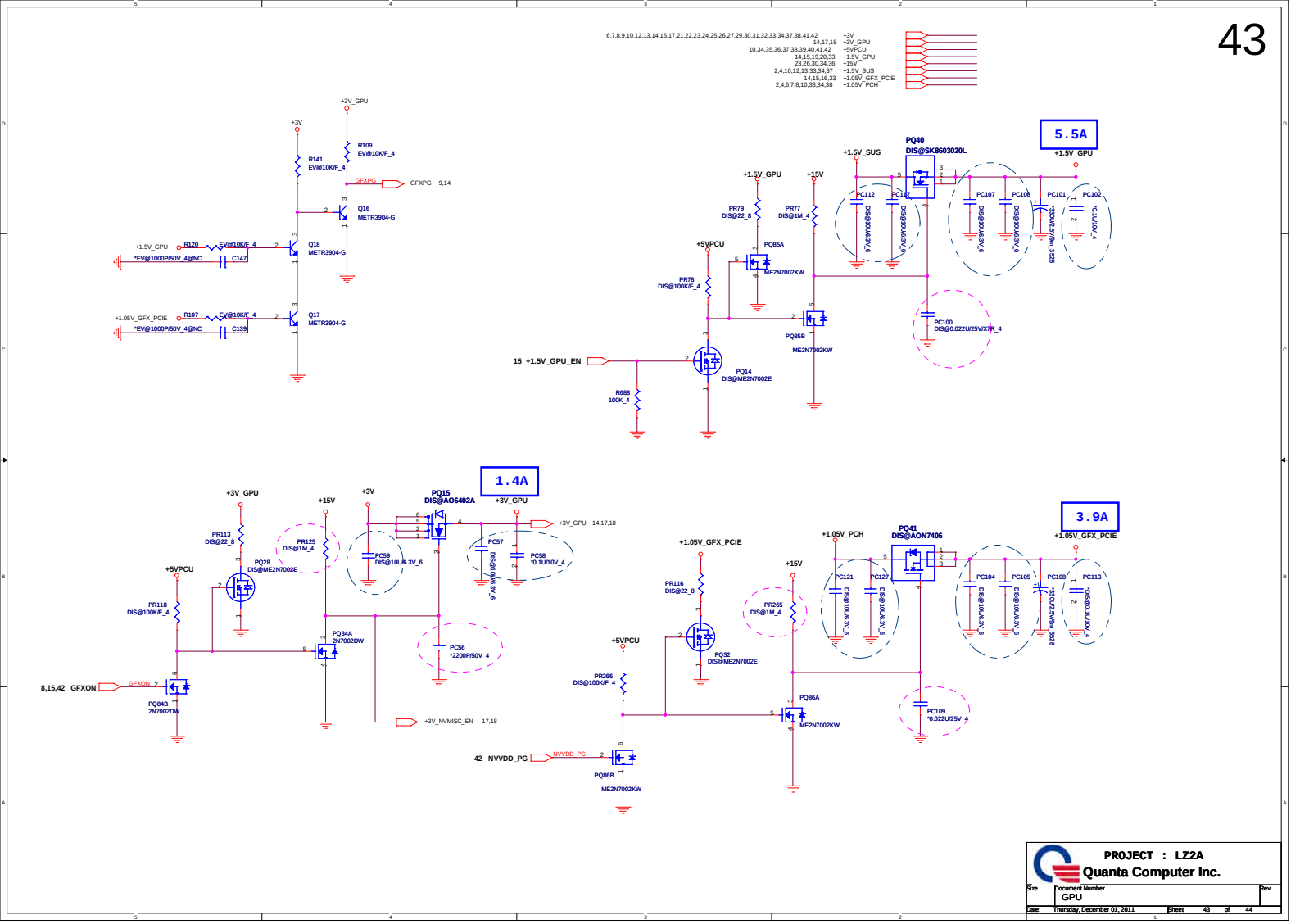


	PR44	PC14	OCP
N13P-GS N13P-GL	CS21472FB21(1.47K)	Stuff	TDC : 30A Imax : 40A OCP : 50A
N13M-GE1	CS21272FB15(1.27K)	Unstuff	TDC : 20A Imax : 25A OCP : 30A



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Quanta Computer Inc.

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	GPU	
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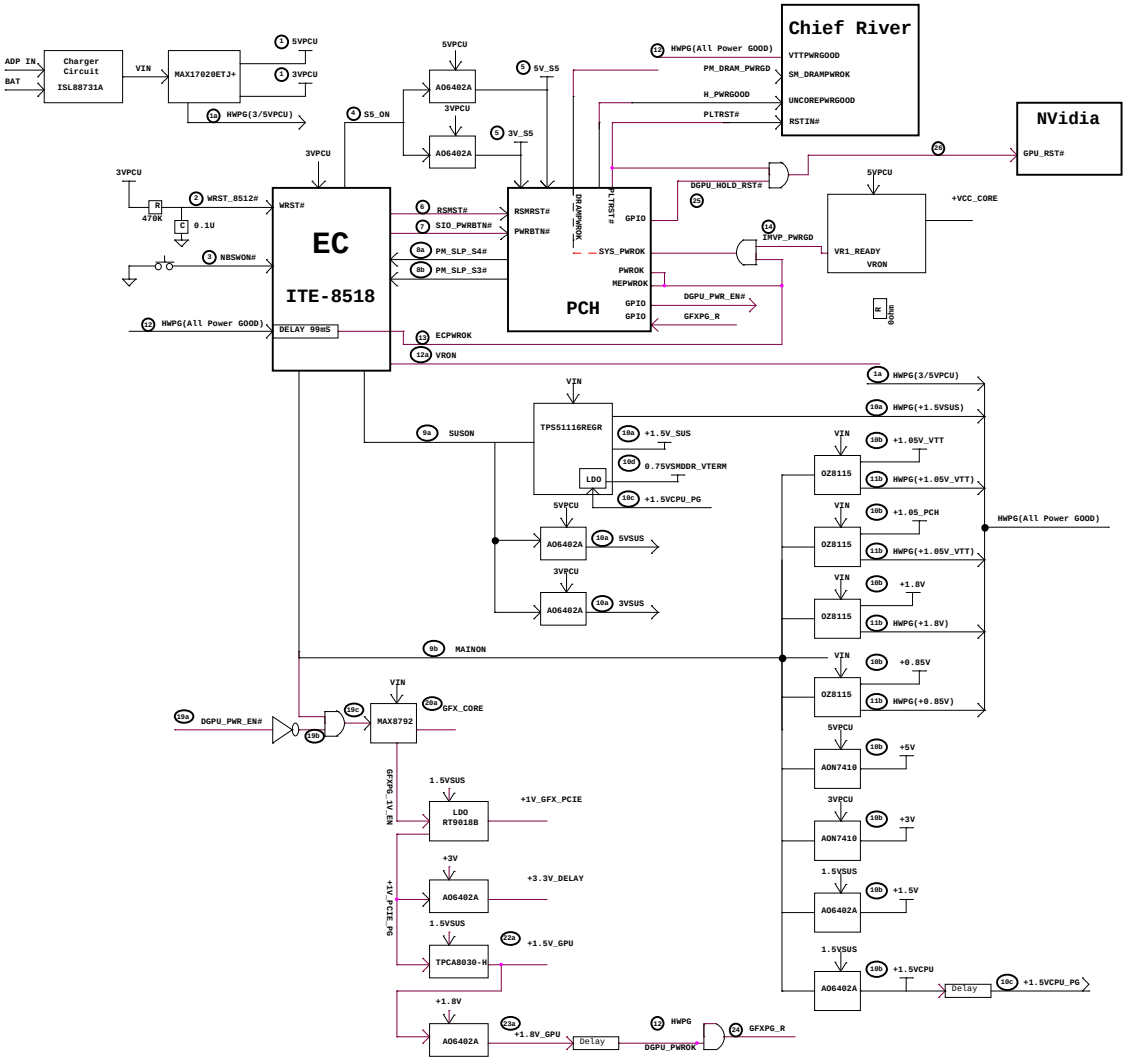

PROJECT LZ1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power Sequence Diagram	1B

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