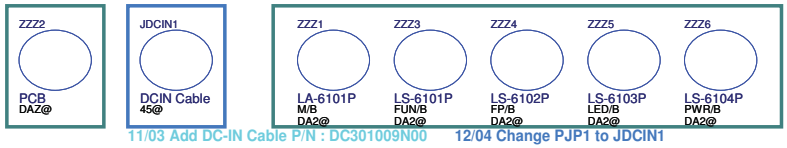

11/03 Add DC-IN Cable P/N : DC301009N00 12/04 Change PJP1 to JDCIN1

11/18 Change PCB P/N from DA60000G300 to DA60000G200

02/26 Change LA-6101P P/N from DA60000G200 to DA60000G210

02/26 Add DAZ P/N and other small board P/N

02/26 Change DAZ P/N from DAZ0D9001001 to DAZ0D900101

Compal Confidential

NAU00 LA-6101P Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

SV M/B

2010-03-09

Rev : 1.0

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Title: Cover Page

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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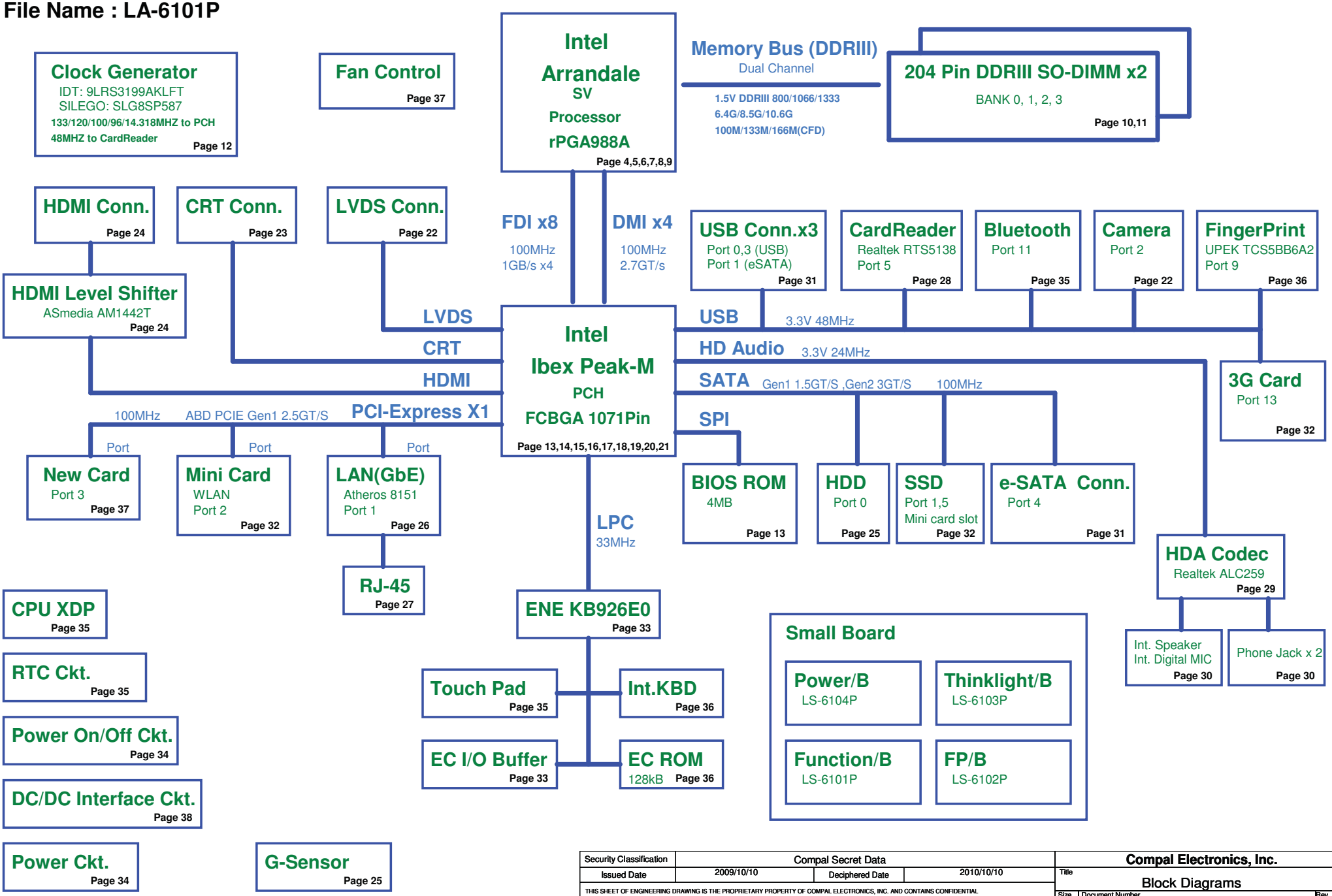
Compal Confidential

Model Name : NAU00
File Name : LA-6101P



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Compal Electronics, Inc.

Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

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Title: Notes List

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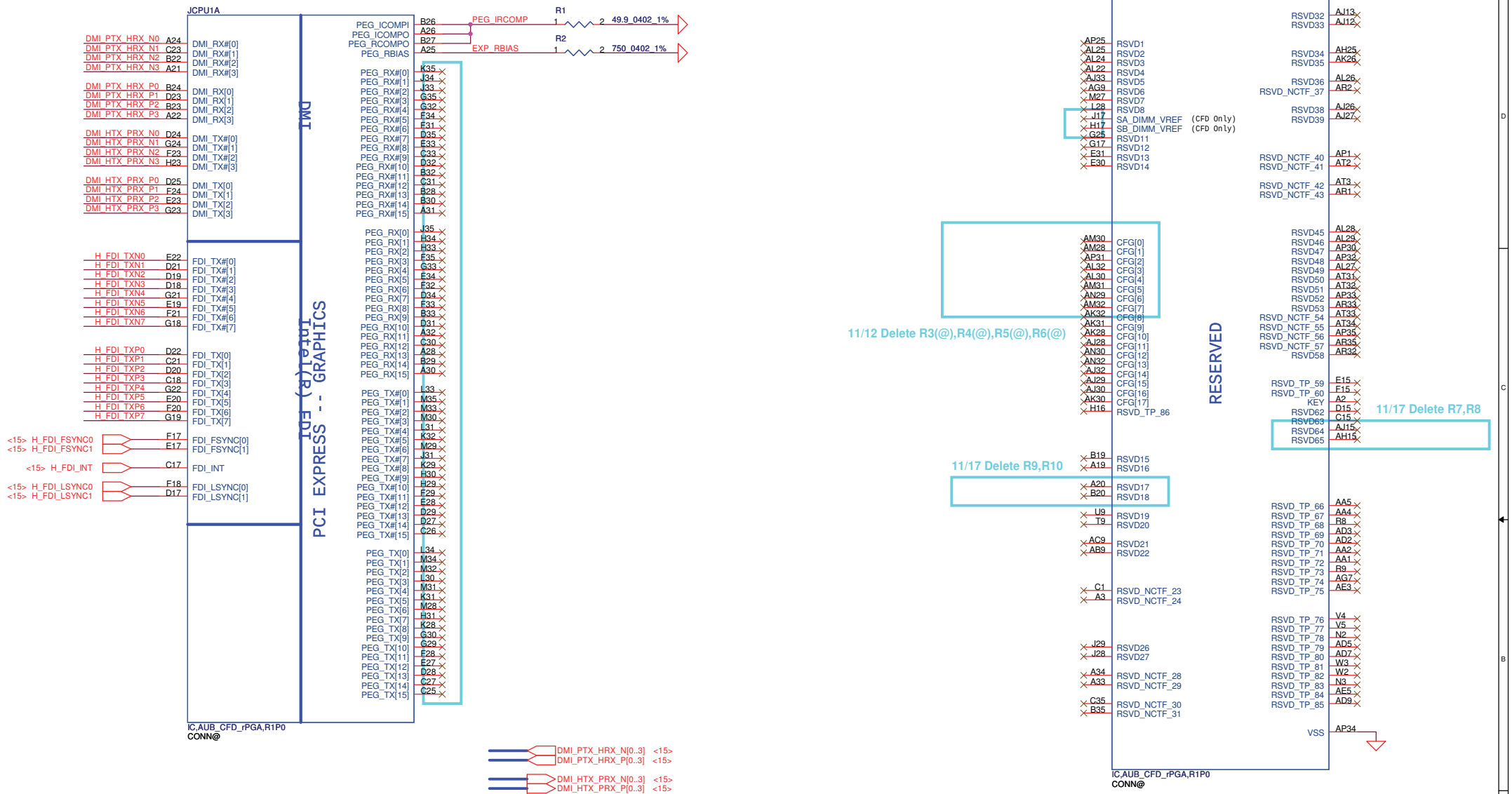

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

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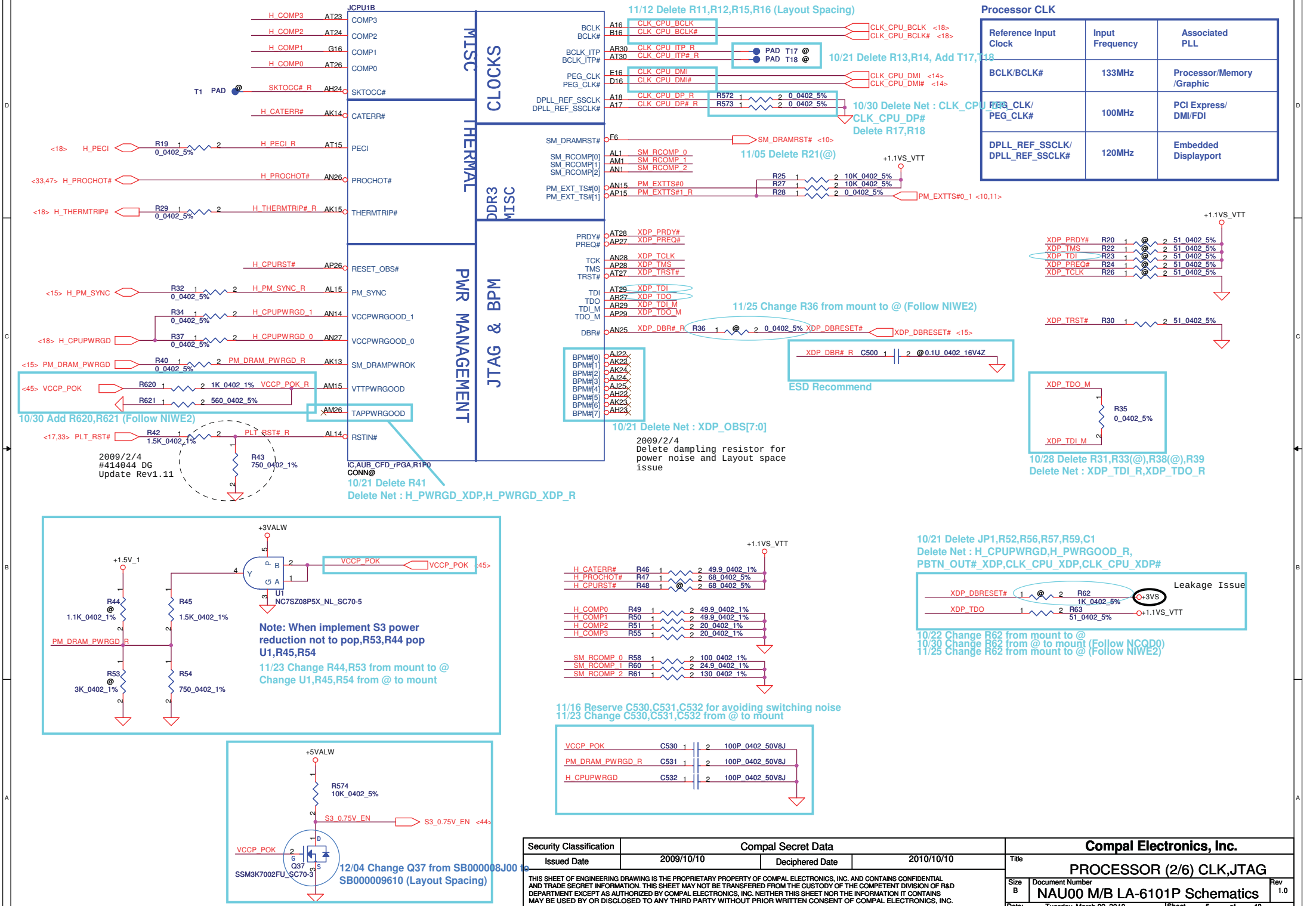

11/12 Delete R11,R12,R15,R16 (Layout Spacing)

10/21 Delete R13,R14, Add T17,T18

10/30 Delete Net : CLK_CPU_PEG_CLK/CLK_CPU_DP#
Delete R17,R18

11/05 Delete R21(@)

11/25 Change R36 from mount to @ (Follow NIWE2)

ESD Recommend

10/30 Add R620,R621 (Follow NIWE2)

2009/2/4
#414044 DG
Update Rev1.11

10/21 Delete R41
Delete Net : H_PWRGD_XDP,H_PWRGD_XDP_R

10/21 Delete Net : XDP_OBS[7:0]

2009/2/4
Delete dampling resistor for power noise and Layout space issue

10/28 Delete R31,R33(@),R38(@),R39
Delete Net : XDP_TDI_R,XDP_TDO_R

Note: When implement S3 power reduction not to pop,R53,R44 pop U1,R45,R54

11/23 Change R44,R53 from mount to @
Change U1,R45,R54 from @ to mount

10/21 Delete JP1,R52,R56,R57,R59,C1
Delete Net : H_CPUPWRGD,H_PWRGOOD_R,
PBTN_OUT#_XDP,CLK_CPU_XDP,CLK_CPU_XDP#

10/22 Change R62 from mount to @
10/30 Change R62 from @ to mount (Follow NCQD0)
11/25 Change R62 from mount to @ (Follow NIWE2)

11/16 Reserve C530,C531,C532 for avoiding switching noise
11/23 Change C530,C531,C532 from @ to mount

12/04 Change Q37 from SB000008J00 to SB000009610 (Layout Spacing)

Processor CLK

Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	133MHz	Processor/Memory /Graphic
PEG_CLK/ PEG_CLK#	100MHz	PCI Express/ DMI/FDI
DPLL_REF_SSCLK/ DPLL_REF_SSCLK#	120MHz	Embedded Displayport

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Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

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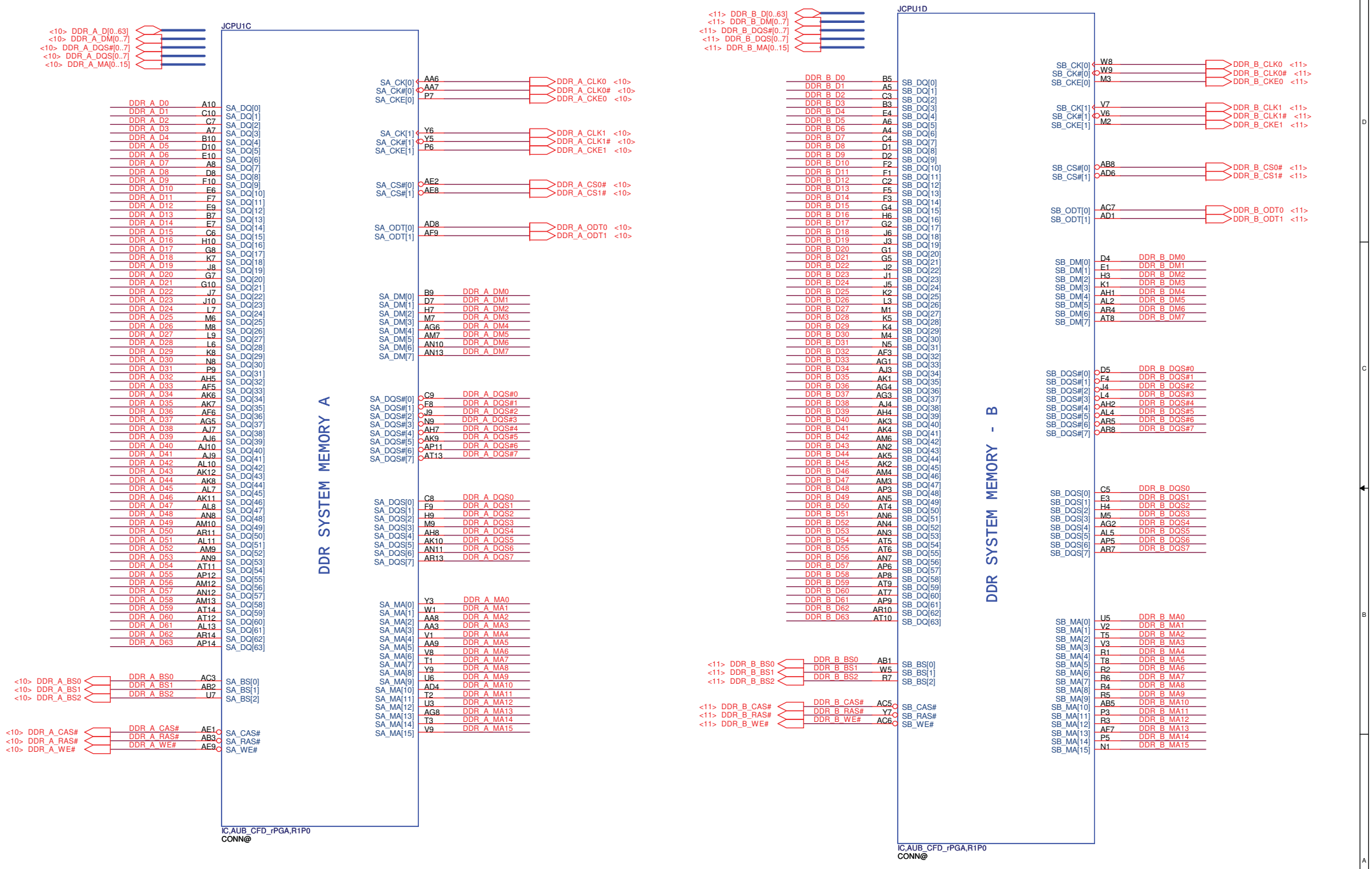

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Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

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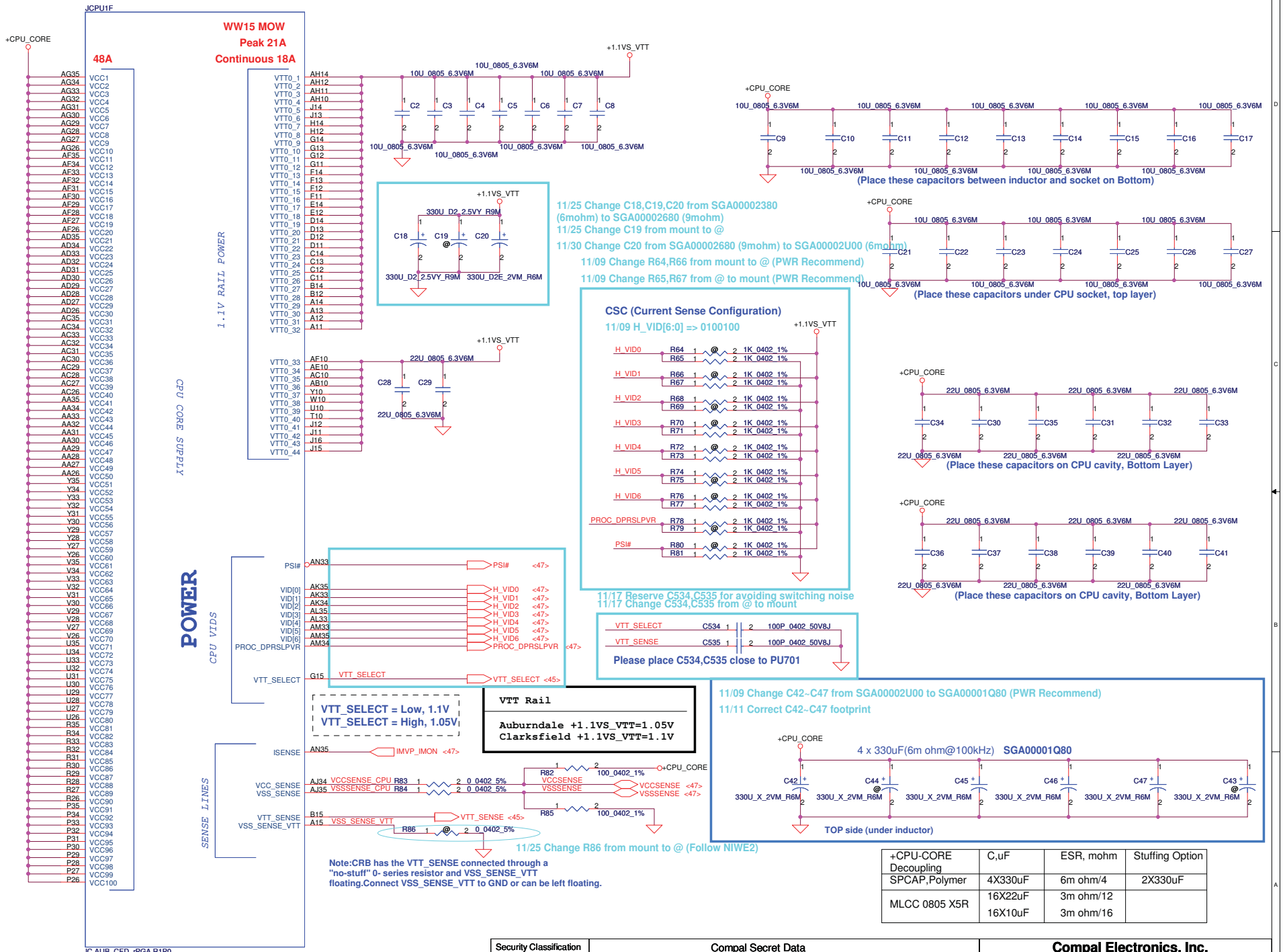

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	2X330uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Issued Date	2009/10/10	Deciphered Date	2010/10/10

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Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

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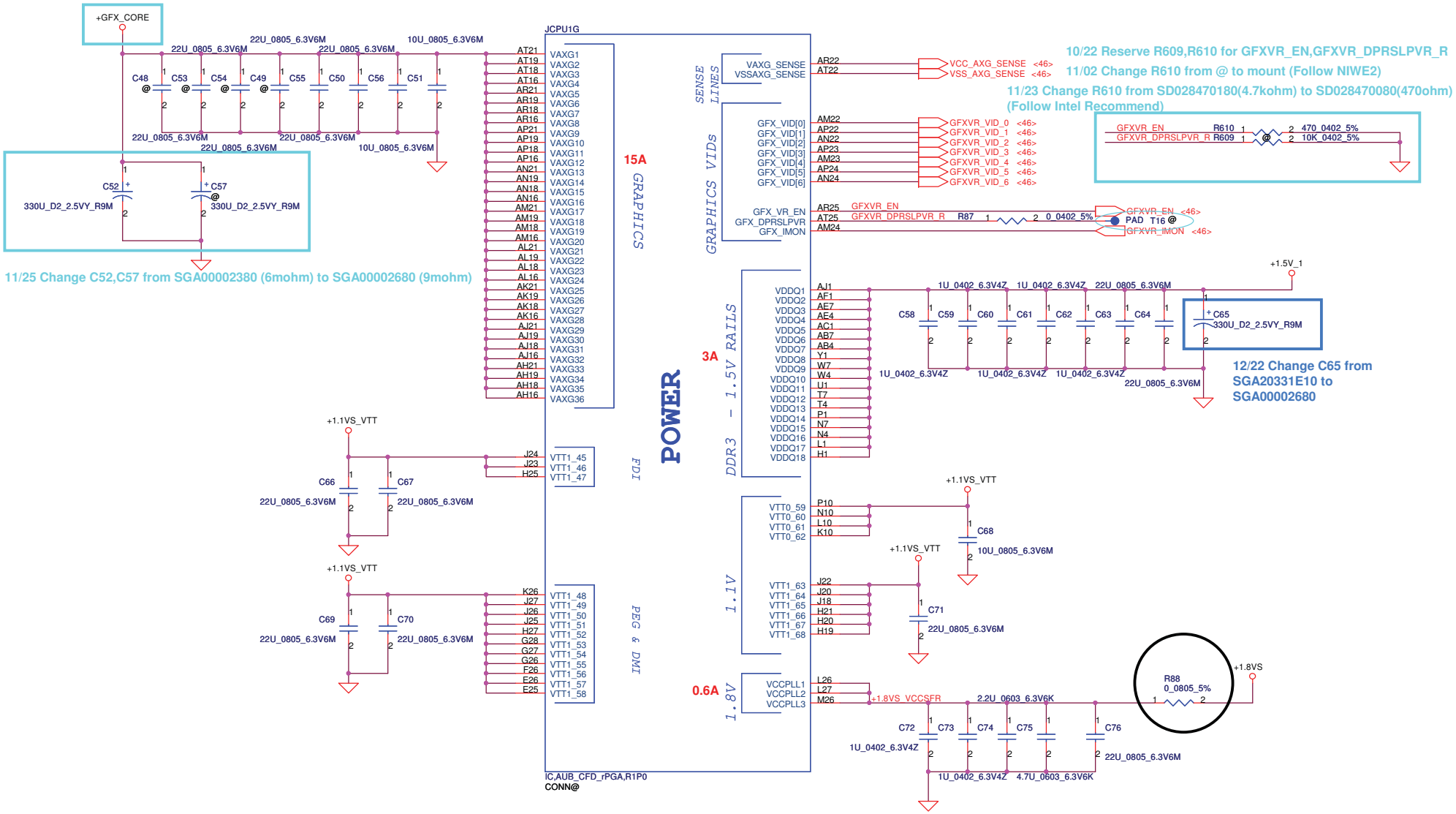

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Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

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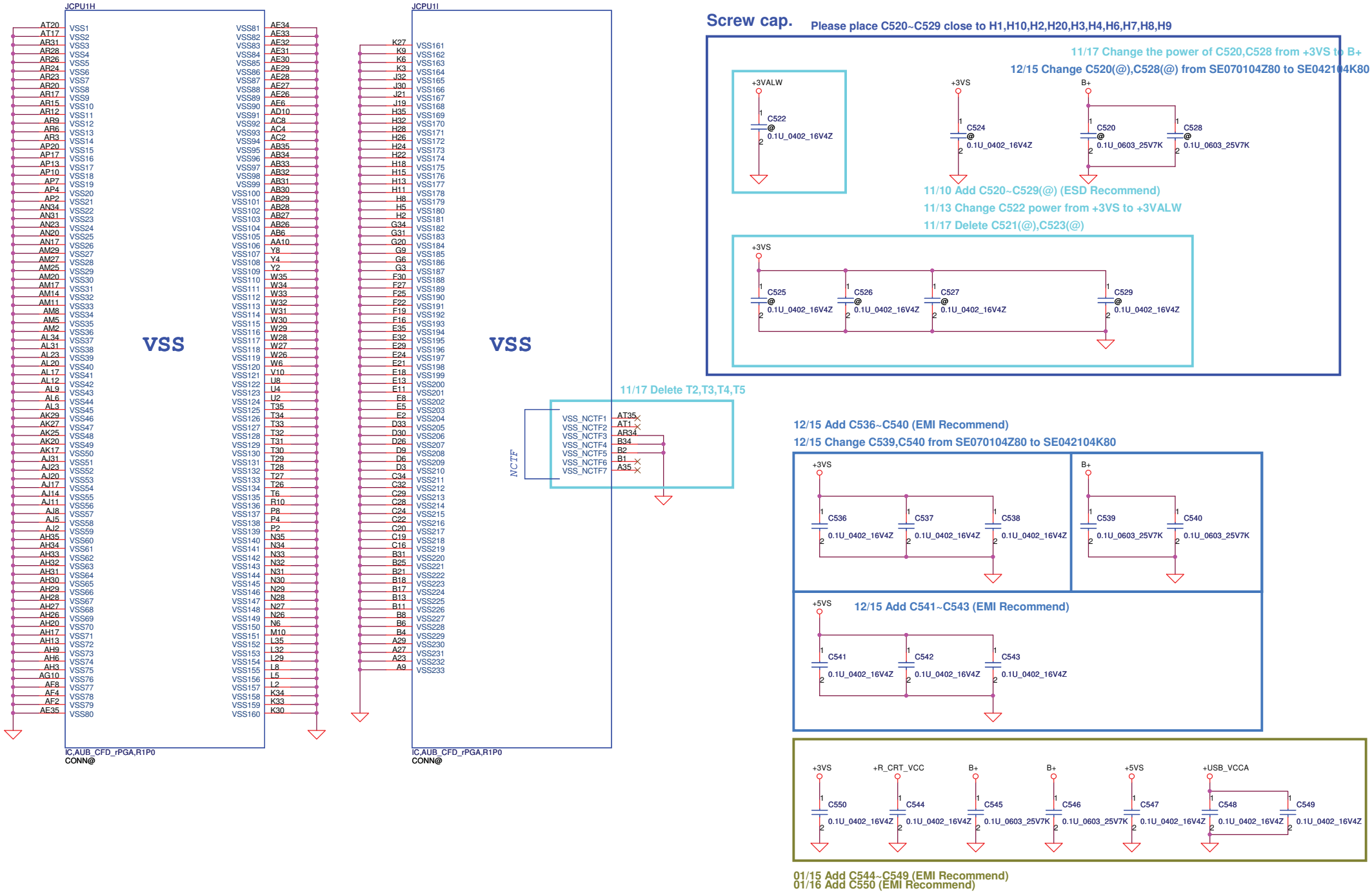

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Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

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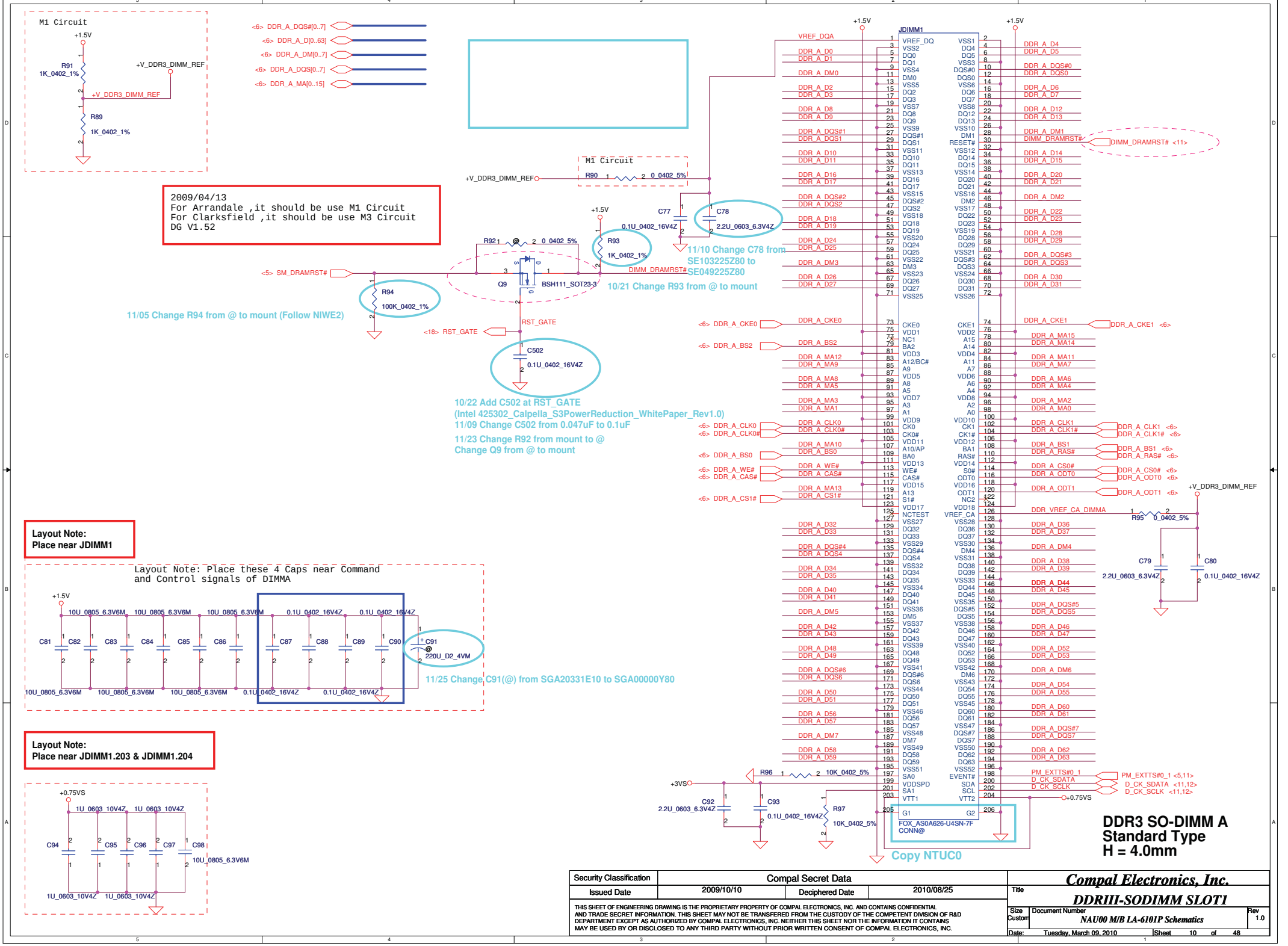
M1 Circuit
+1.5V
R91
1K_0402_1%
+V_DDR3_DIMM_REF
R89
1K_0402_1%
<6> DDR_A_DQS#[0..7]
<6> DDR_A_D[0..63]
<6> DDR_A_DM[0..7]
<6> DDR_A_DQS[0..7]
<6> DDR_A_MA[0..15]
2009/04/13
For Arrandale ,it should be use M1 Circuit
For Clarksfield ,it should be use M3 Circuit
DG V1.52
M1 Circuit
R90 0_0402_5%
C77 0.1U_0402_16V4Z
C78 2.2U_0603_6.3V4Z
11/10 Change C78 from SE103225Z80 to SE049225Z80
R92 @ 0_0402_5%
R93 1K_0402_1%
<5> SM_DRAMRST#
Q9 BSH111_SOT23-3
DIMM_DRAMRST#
10/21 Change R93 from @ to mount
R94 100K_0402_1%
11/05 Change R94 from @ to mount (Follow NIWE2)
RST_GATE
<18> RST_GATE
C502 0.1U_0402_16V4Z
10/22 Add C502 at RST_GATE
(Intel 425302_Calpella_S3PowerReduction_WhitePaper_Rev1.0)
11/09 Change C502 from 0.047uF to 0.1uF
11/23 Change R92 from mount to @
Change Q9 from @ to mount
JDIMM1
FOX_AS0A626-U4SN-7F
CONN@
Copy NTUC0
DDR3 SO-DIMM A
Standard Type
H = 4.0mm
Layout Note:
Place near JDIMM1
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA
C81 10U_0805_6.3V6M
C82 10U_0805_6.3V6M
C83 10U_0805_6.3V6M
C84 10U_0805_6.3V6M
C85 10U_0805_6.3V6M
C86 10U_0805_6.3V6M
C87 0.1U_0402_16V4Z
C88 0.1U_0402_16V4Z
C89 0.1U_0402_16V4Z
C90 0.1U_0402_16V4Z
C91 @ 220U_D2_4VM
11/25 Change C91(@) from SGA20331E10 to SGA00000Y80
Layout Note:
Place near JDIMM1.203 & JDIMM1.204
+0.75VS
C94 1U_0603_10V4Z
C95 1U_0603_10V4Z
C96 1U_0603_10V4Z
C97 1U_0603_10V4Z
C98 10U_0805_6.3V6M
R96 10K_0402_5%
+3VS
C92 2.2U_0603_6.3V4Z
C93 0.1U_0402_16V4Z
R97 10K_0402_5%
R95 0_0402_5%
C79 2.2U_0603_6.3V4Z
C80 0.1U_0402_16V4Z
DDR_A_CKE1 <6>
DDR_A_CLK1 <6>
DDR_A_CLK1# <6>
DDR_A_BS1 <6>
DDR_A_RAS# <6>
DDR_A_CS0# <6>
DDR_A_ODT0 <6>
DDR_A_ODT1 <6>
DIMM_DRAMRST# <11>
PM_EXTTS#0_1 <5,11>
D_CK_SDATA <11,12>
D_CK_SCLK <11,12>
Security Classification
Compal Secret Data
Issued Date
2009/10/10
Deciphered Date
2010/08/25
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Title
DDRIII-SODIMM SLOT1
Size Custom
Document Number
NAU00 M/B LA-6101P Schematics
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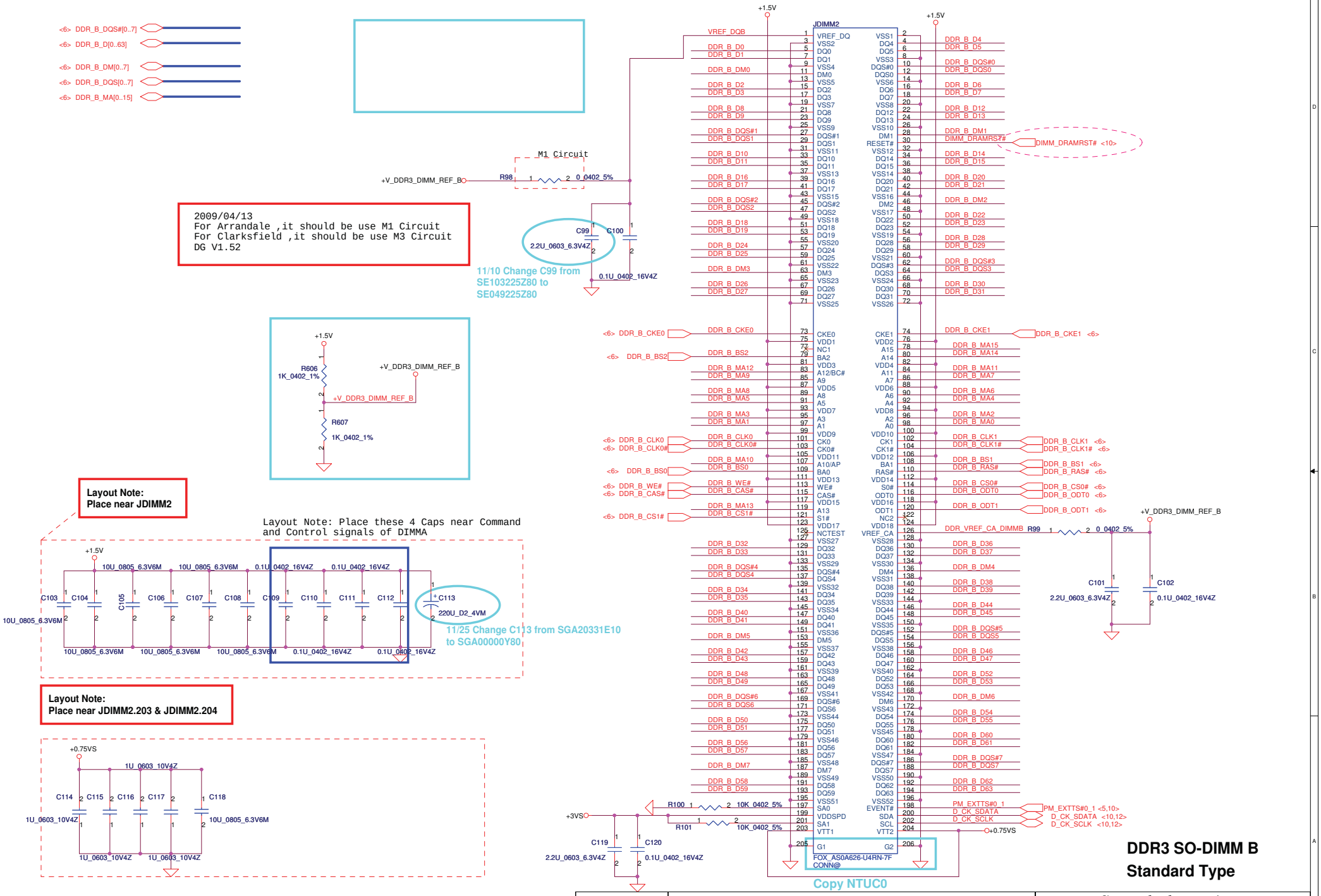

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

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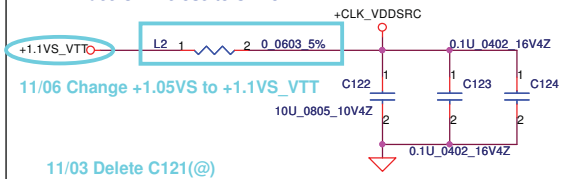
Layout note:
Place C122 close to L2
Place C123 close to U2.15
Place C124 close to U2.18

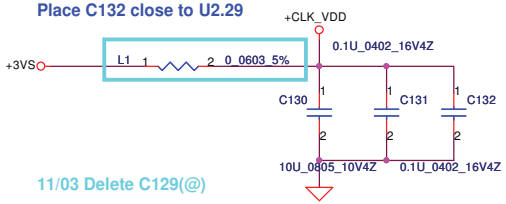


11/06 Change +1.05VS to +1.1VS_VTT

11/03 Delete C121(@)

11/03 Change L2 from SM01000AX00 to 0ohm (Follow NIWE2)

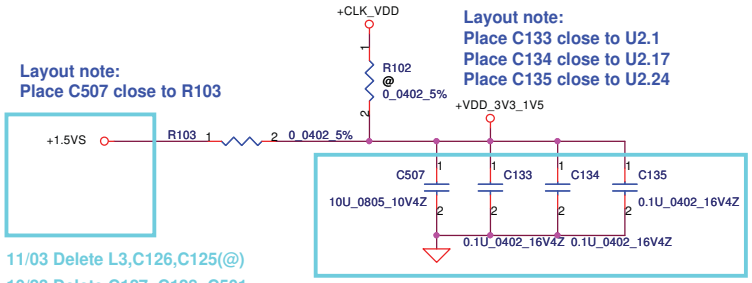
Layout note:
Place C130 close to L1
Place C131 close to U2.5
Place C132 close to U2.29



11/03 Delete C129(@)

11/03 Change L1 from SM01000AX00 to 0ohm (Follow NIWE2)

Layout note:
Place C507 close to R103



11/03 Delete L3,C126,C125(@)

10/23 Delete C127, C128, C501 on +CLK_1.5VDD

10/23 Add C1000 on +VDD_3V3_1V5
Change C133, C134, C135 from +CLK_VDD to +VDD_3V3_1V5
11/03 Change C507 from @ to mount

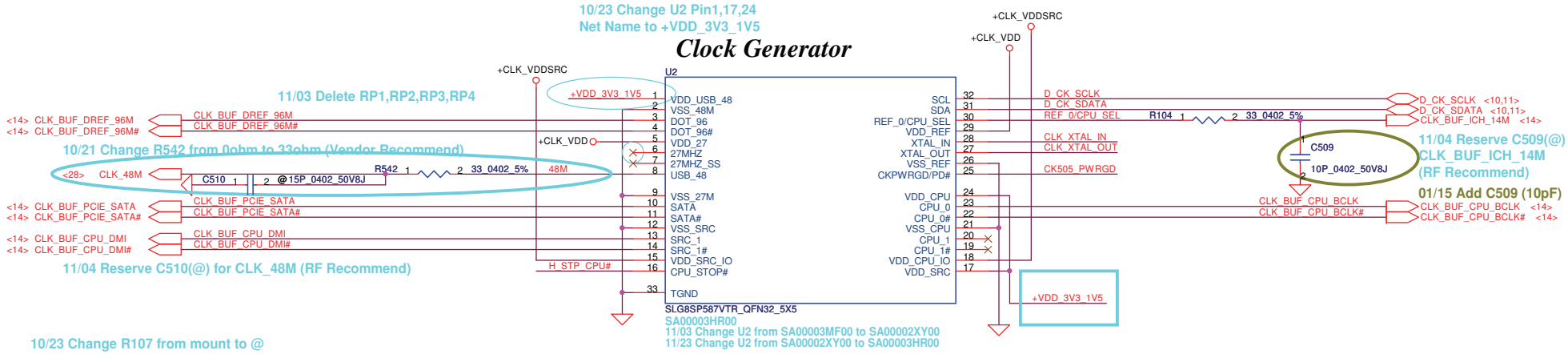
Type	R102	R103
Standard	Mount	@
Low Power	@	Mount

10/23 Change U2 Pin1,17,24
Net Name to +VDD_3V3_1V5

Clock Generator

11/03 Delete RP1,RP2,RP3,RP4

10/21 Change R542 from 0ohm to 33ohm (Vendor Recommend)



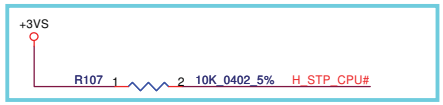
11/04 Reserve C509(@) for CLK_BUF_ICH_14M (RF Recommend)

01/15 Add C509 (10pF)

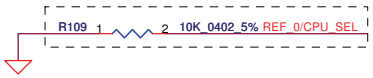
11/04 Reserve C510(@) for CLK_48M (RF Recommend)

SLG8SP587VTR_QFN32_5X5
SA00003HR00
11/03 Change U2 from SA00003MF00 to SA00002XY00
11/23 Change U2 from SA00002XY00 to SA00003HR00

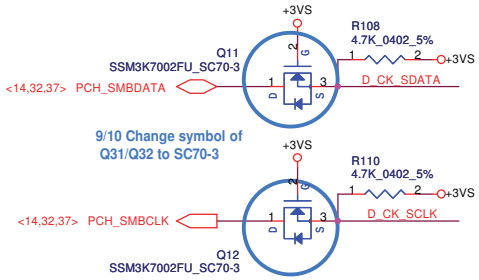
10/23 Change R107 from mount to @
11/03 Change R107 from @ to mount



IDT& Realtek Have Internal Pull-Down

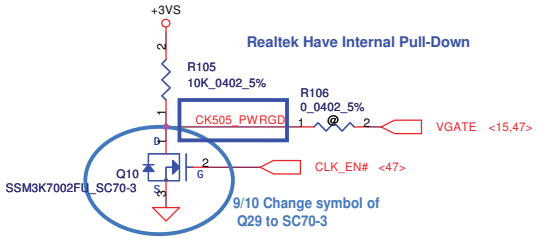


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

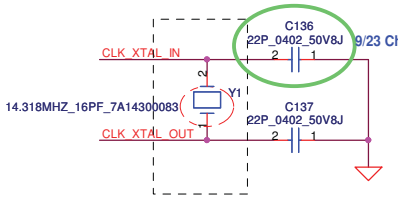


9/10 Change symbol of Q31/Q32 to SC70-3

Realtek Have Internal Pull-Down



9/10 Change symbol of Q29 to SC70-3



9/23 Change C495 to 22pF

update PCB footprint

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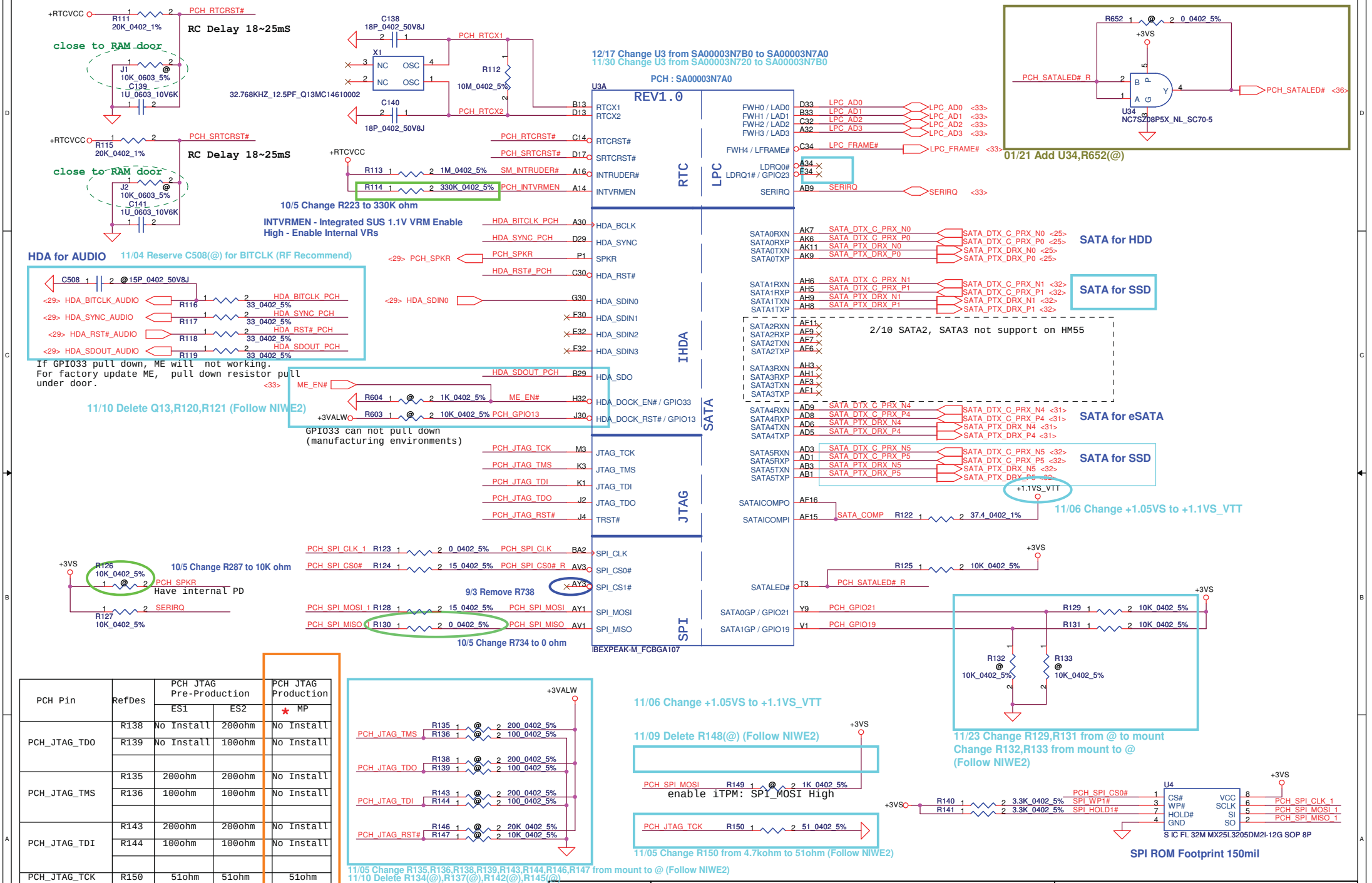
Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 12 of 48



PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R138	No Install	200ohm	No Install
	R139	No Install	100ohm	No Install
PCH_JTAG_TMS	R135	200ohm	200ohm	No Install
	R136	100ohm	100ohm	No Install
PCH_JTAG_TDI	R143	200ohm	200ohm	No Install
	R144	100ohm	100ohm	No Install
PCH_JTAG_TCK	R150	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R146	20Kohm	20Kohm	No Install
	R147	10Kohm	10Kohm	No Install

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Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

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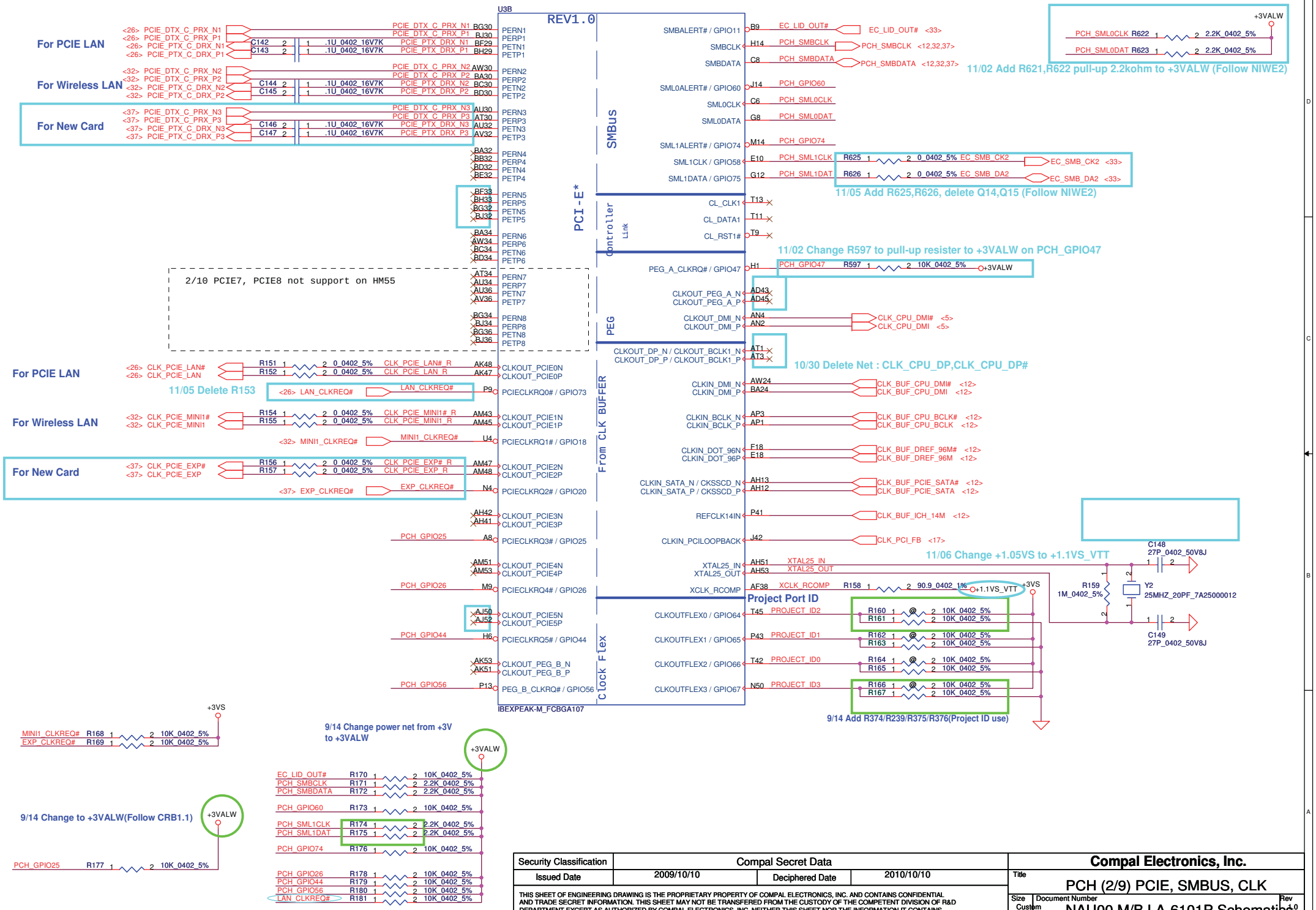
Date: Tuesday, March 09, 2010 | Sheet 13 of 48



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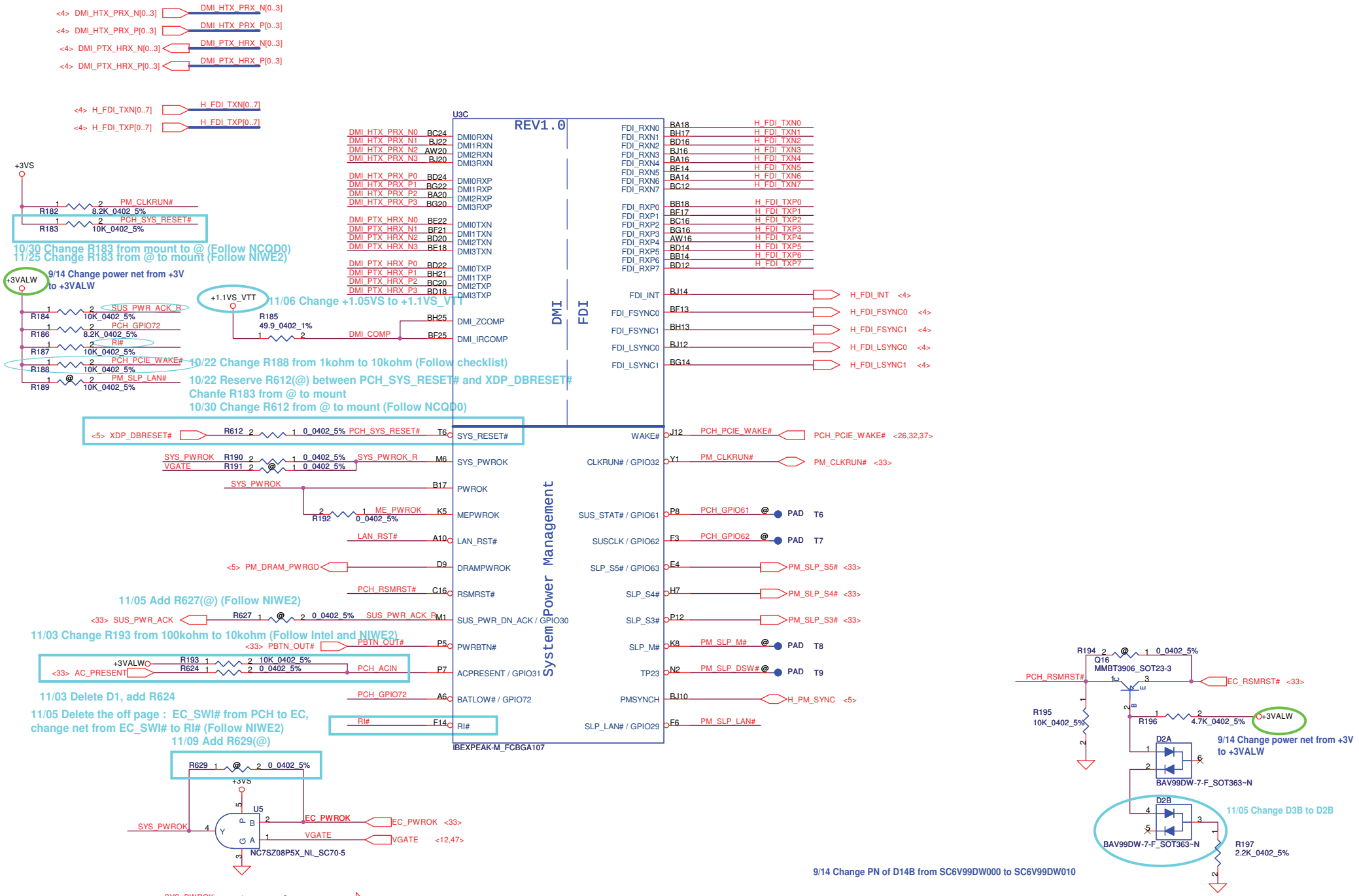
Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 14 of 48



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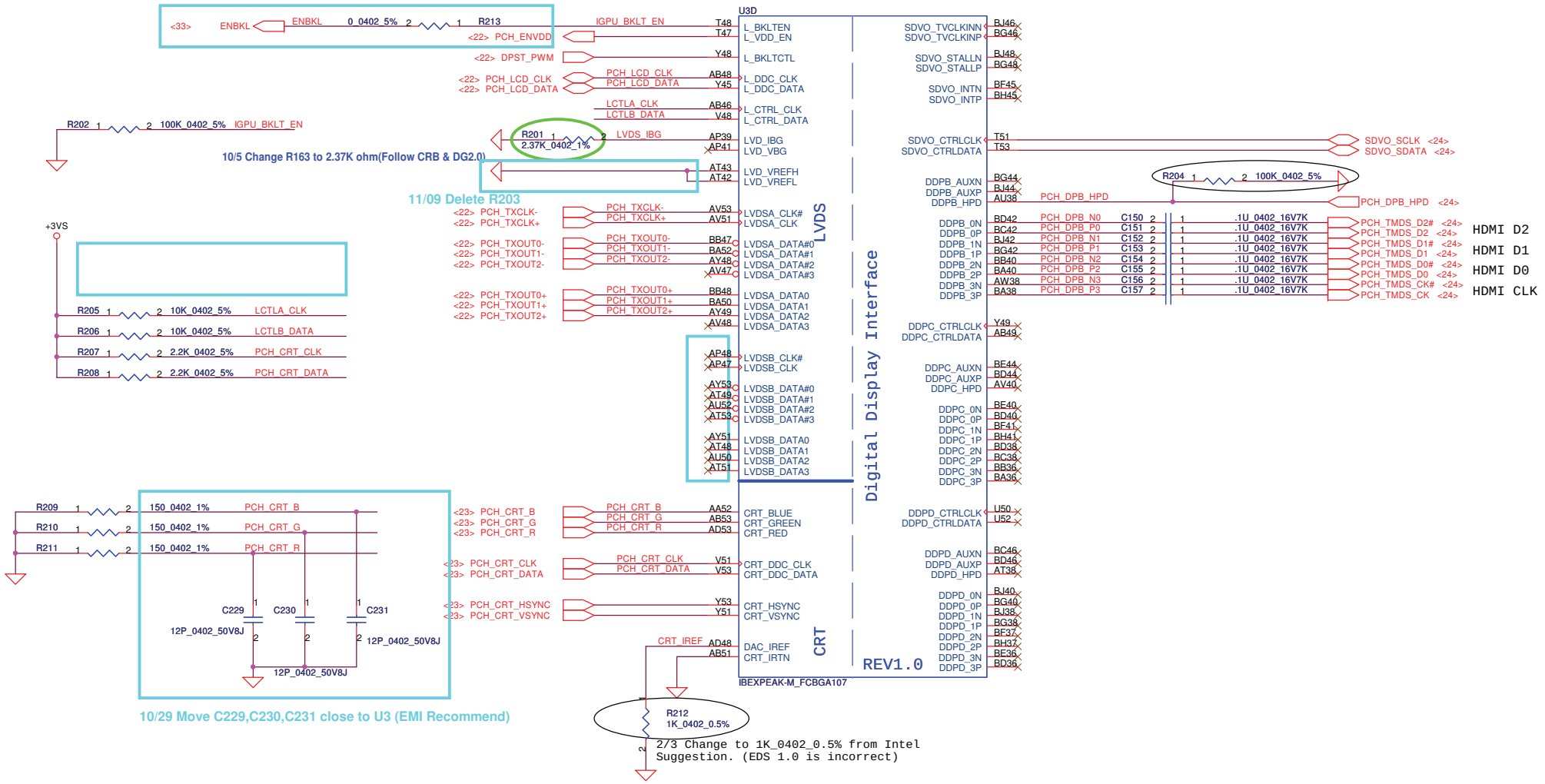
Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 15 of 48



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Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

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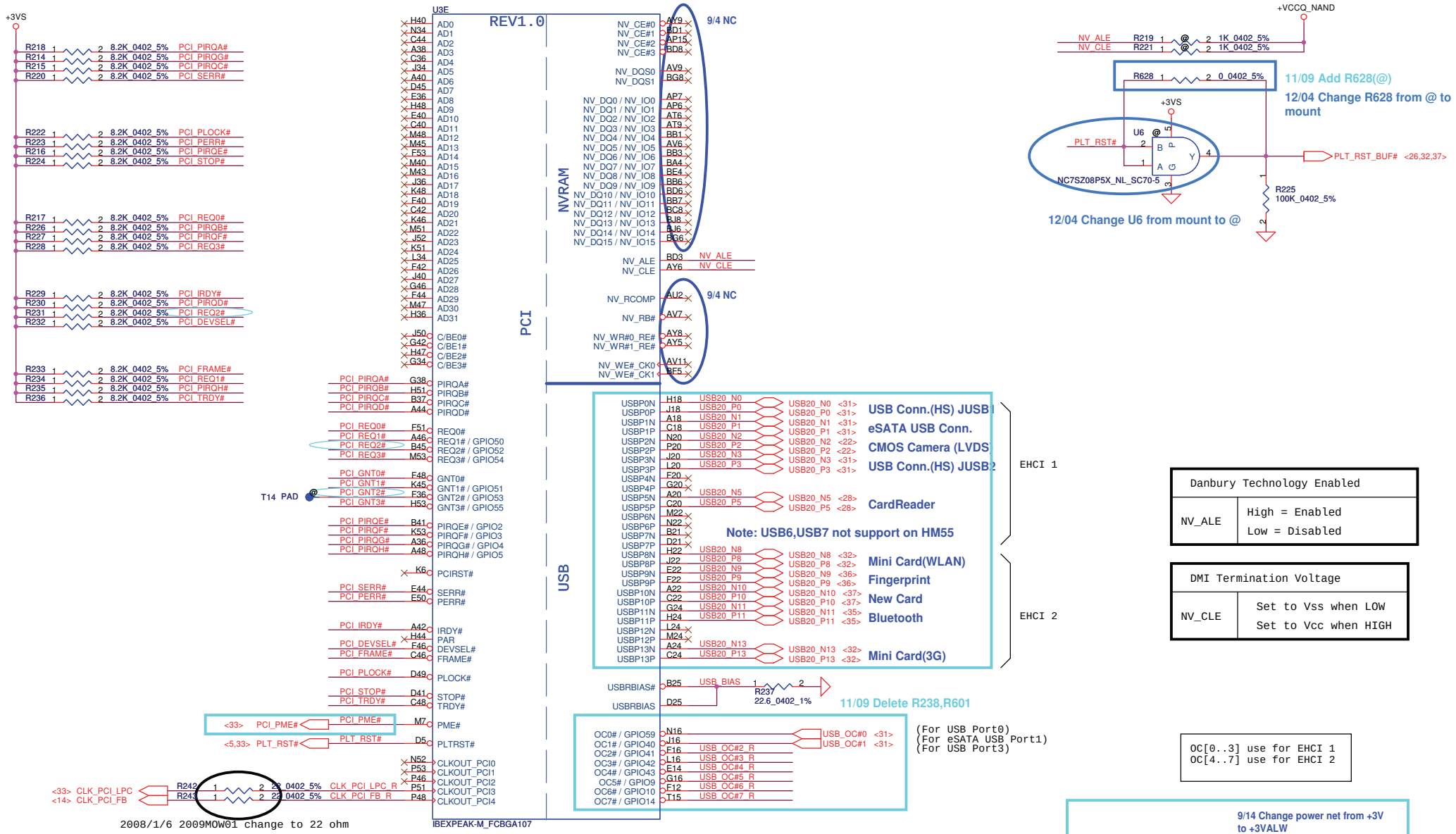
Date: Tuesday, March 09, 2010 | Sheet 16 of 48



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

*

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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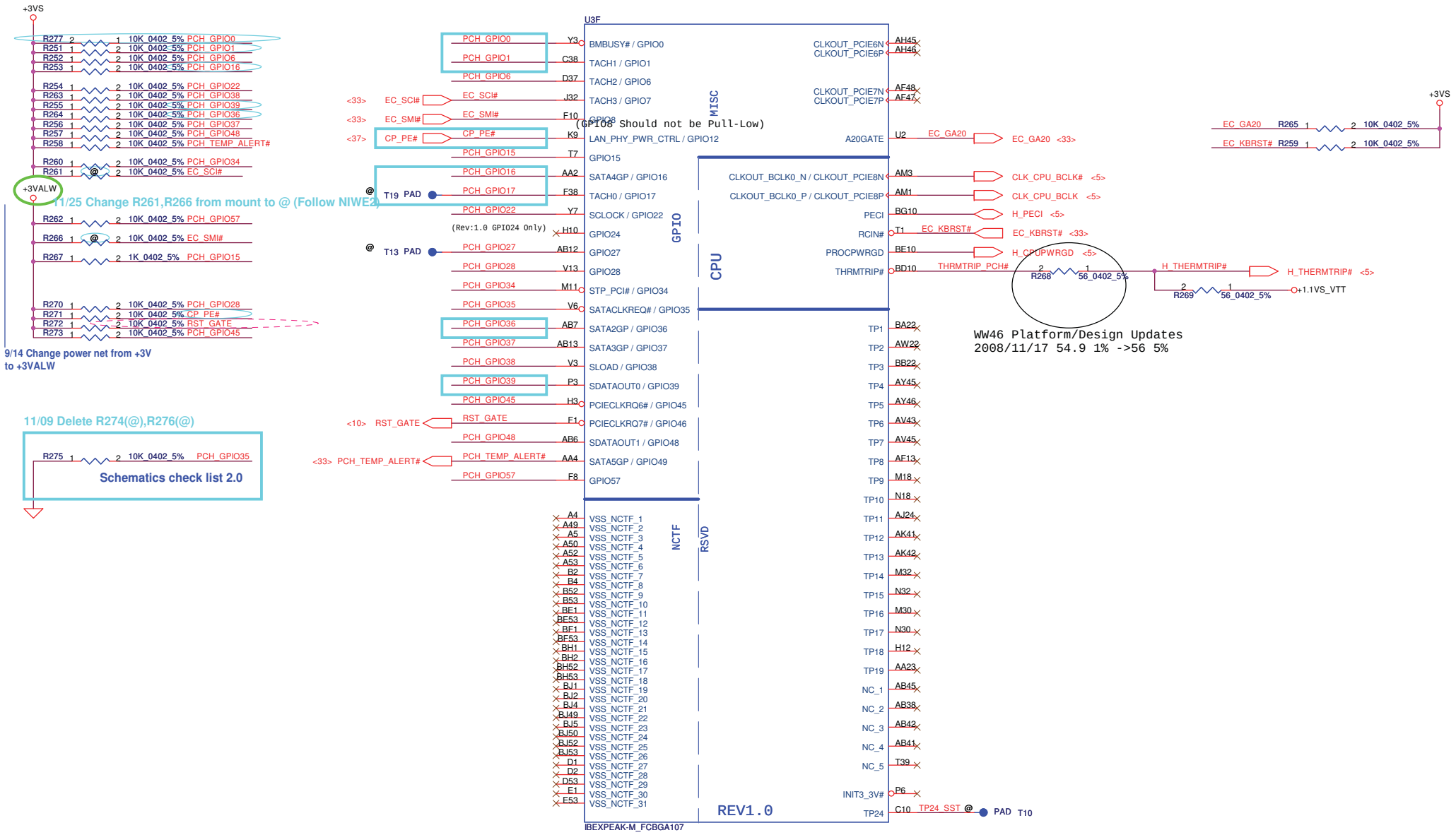
Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 17 of 48



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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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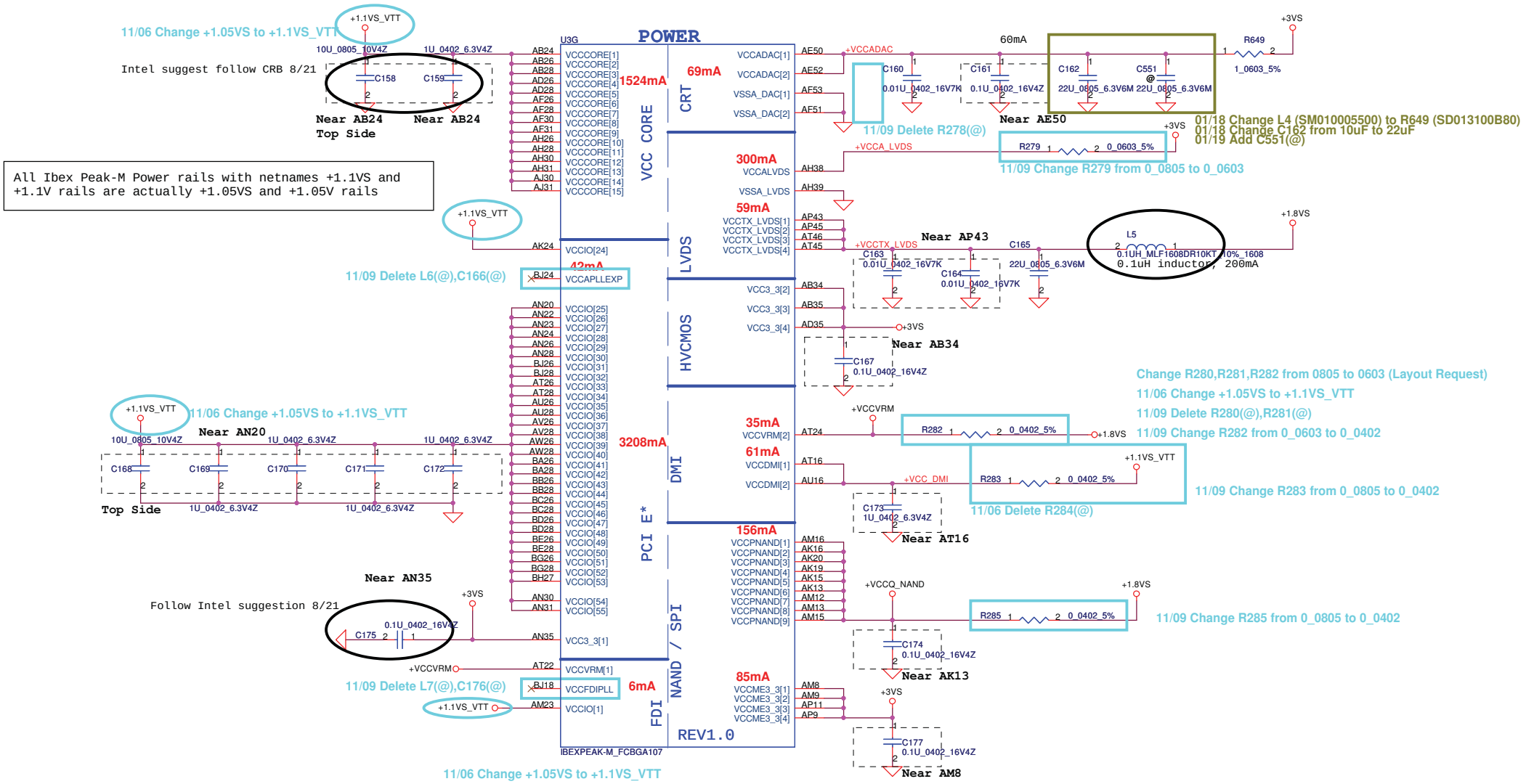
CRB 0.9 is 180 ohm @ 100MHz
DG0.8 is 600 ohm FB (Page 290)



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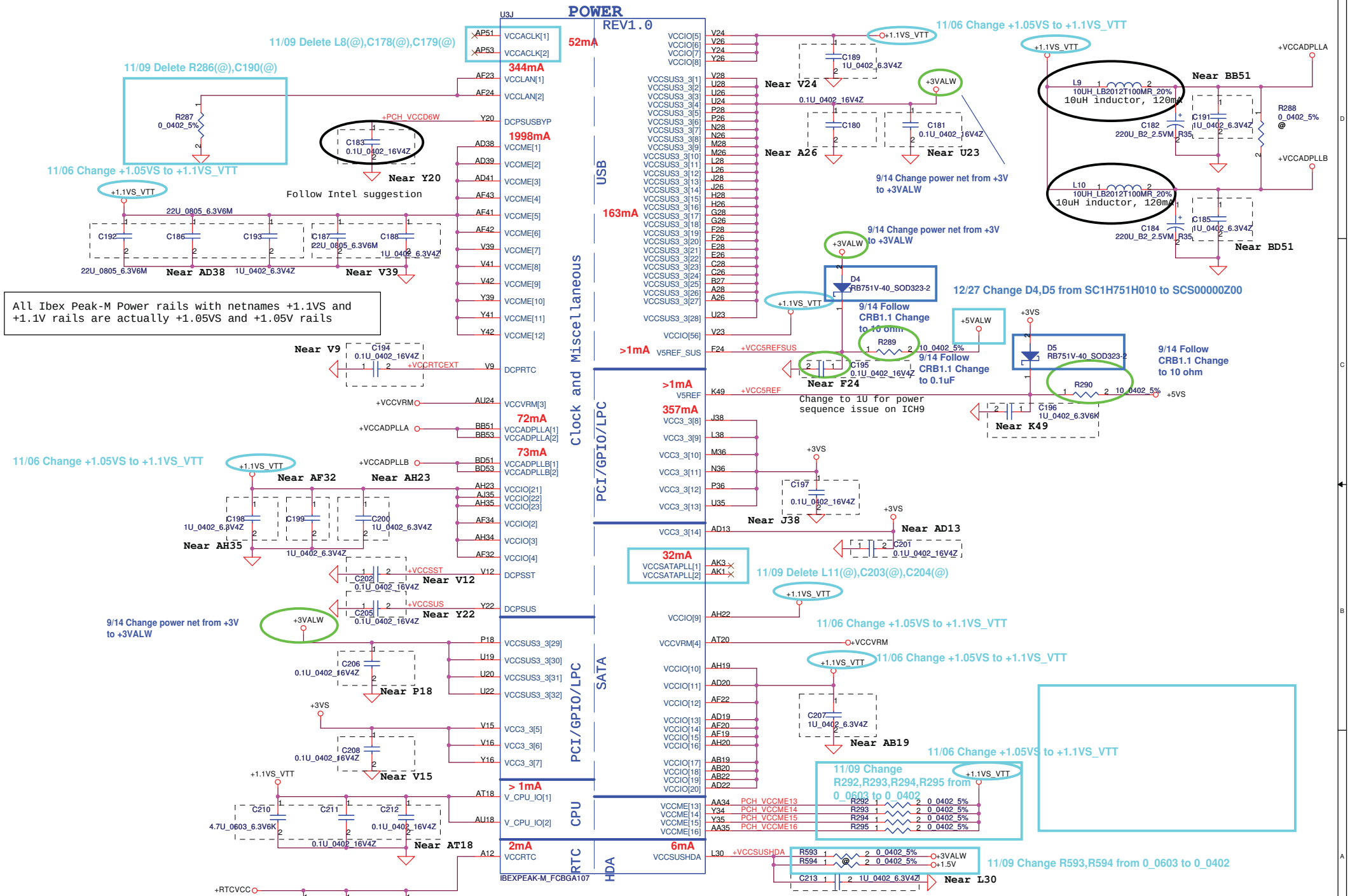
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Friday, February 26, 2010 | Sheet 19 of 48



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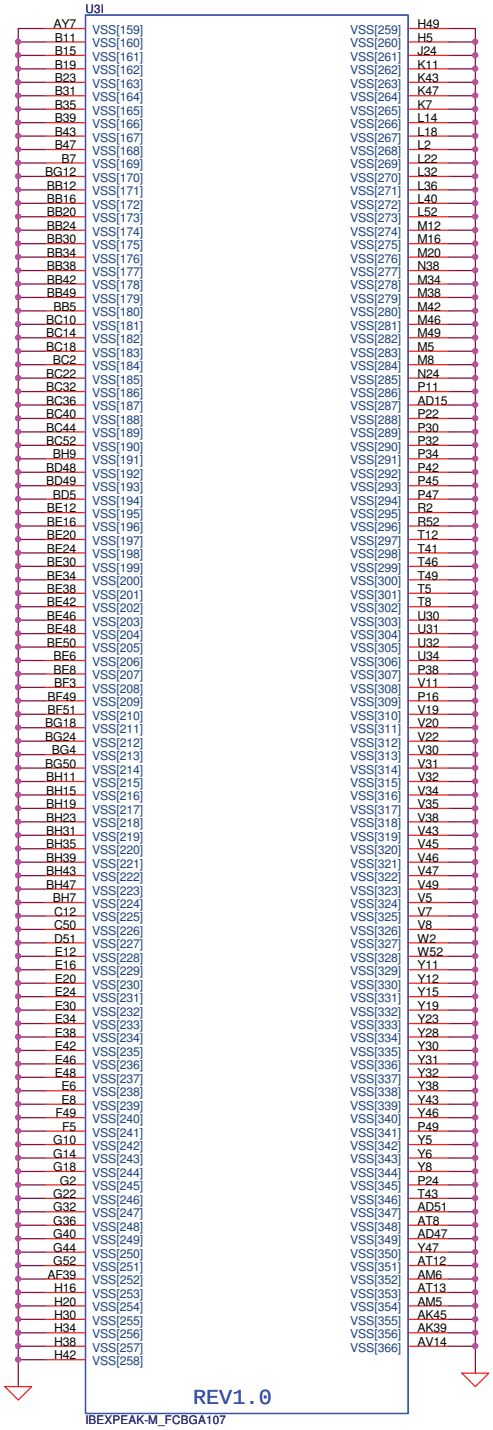
Compal Electronics, Inc.

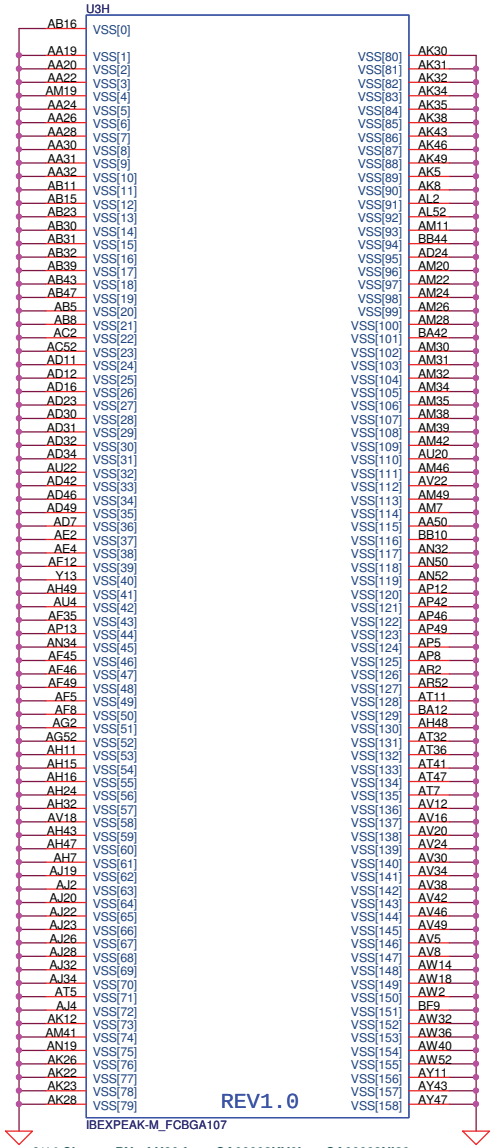
Title: PCH (8/9) PWR

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Friday, February 26, 2010 | Sheet 20 of 48



9/14 Change PN of U60 from SA00002KV0L to SA00003NI20



9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

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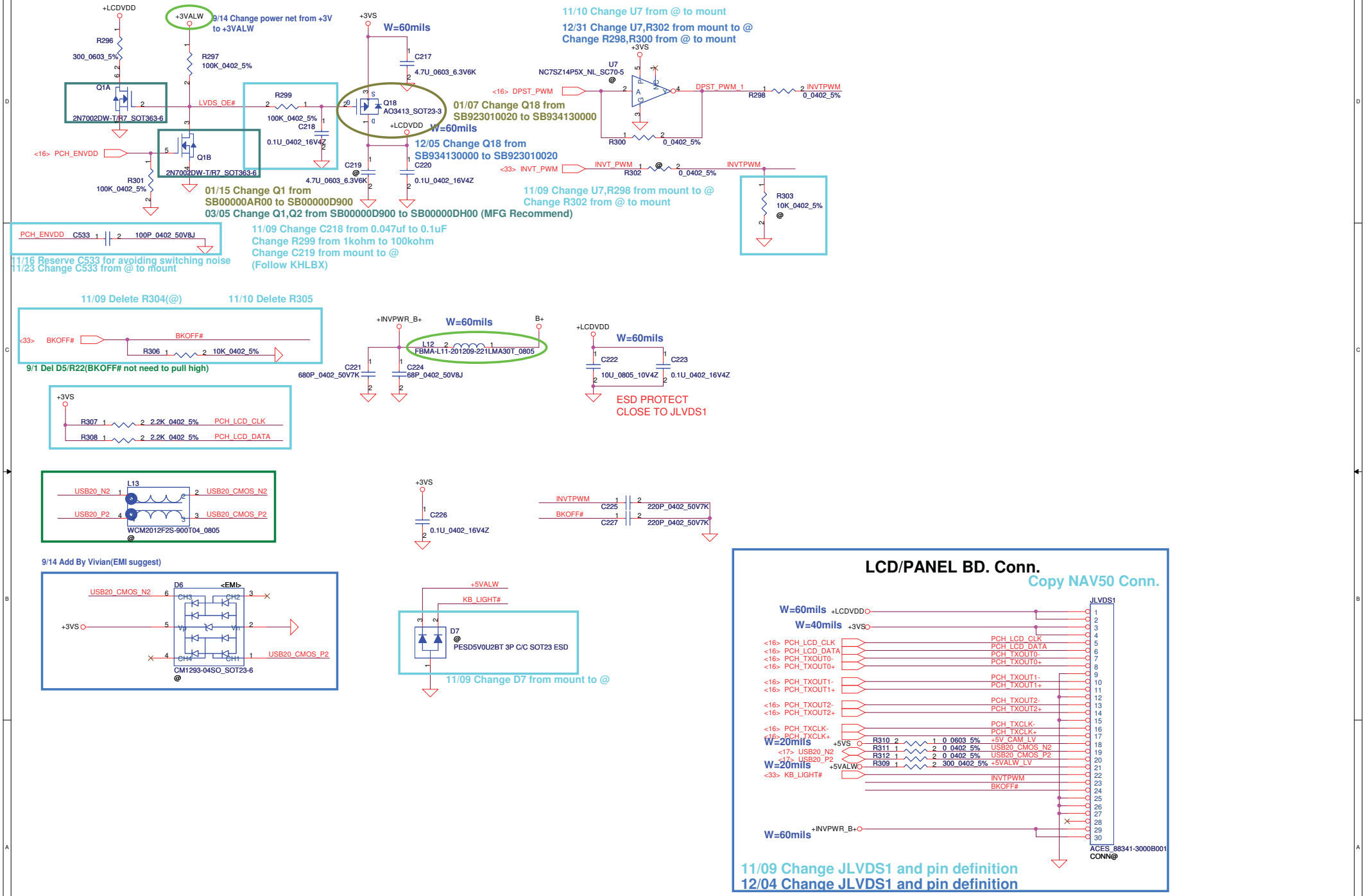
Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Friday, February 26, 2010 | Sheet 21 of 48

LCD POWER CIRCUIT



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Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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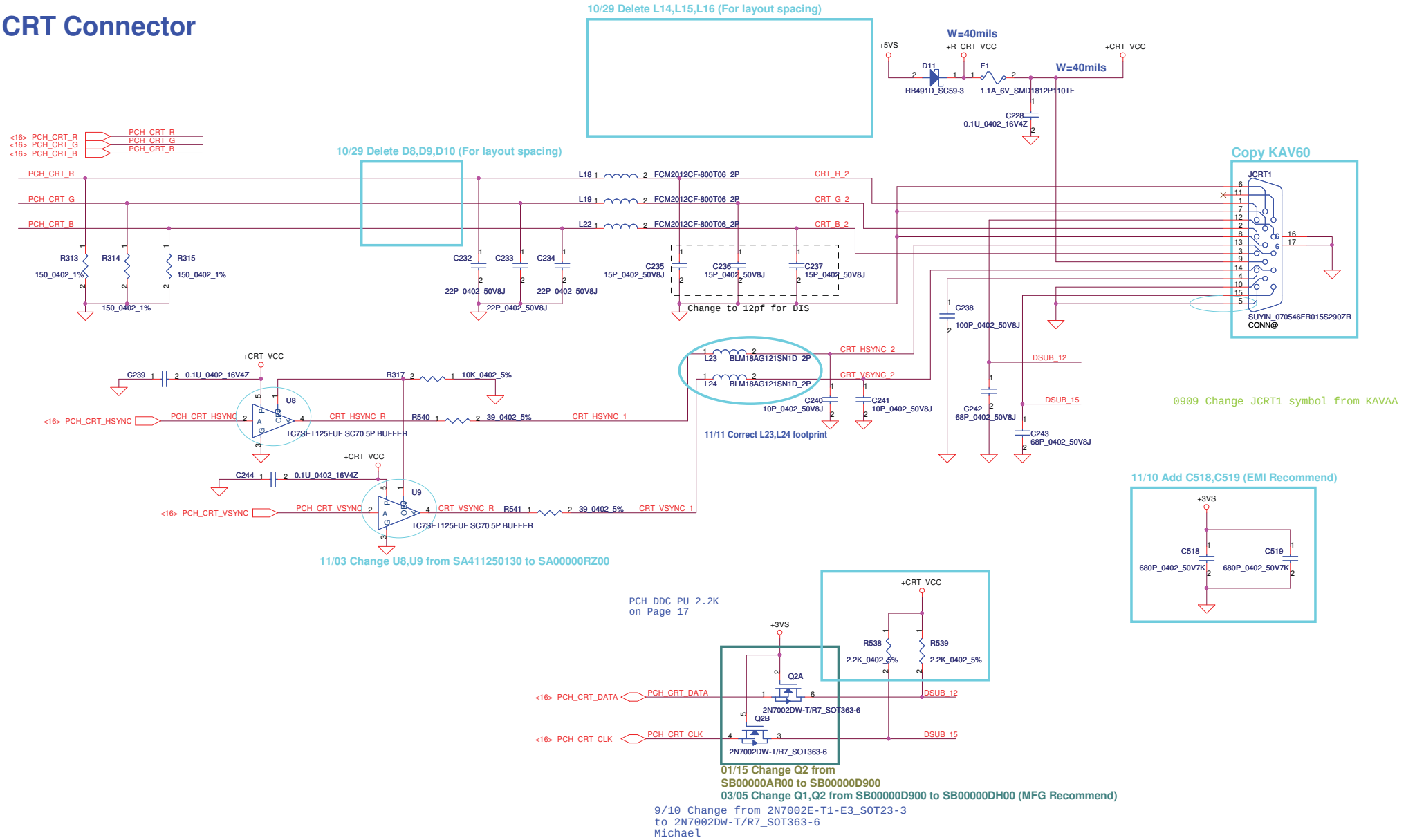
CRT Connector



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Issued Date	2009/10/10	Deciphered Date	2010/10/10

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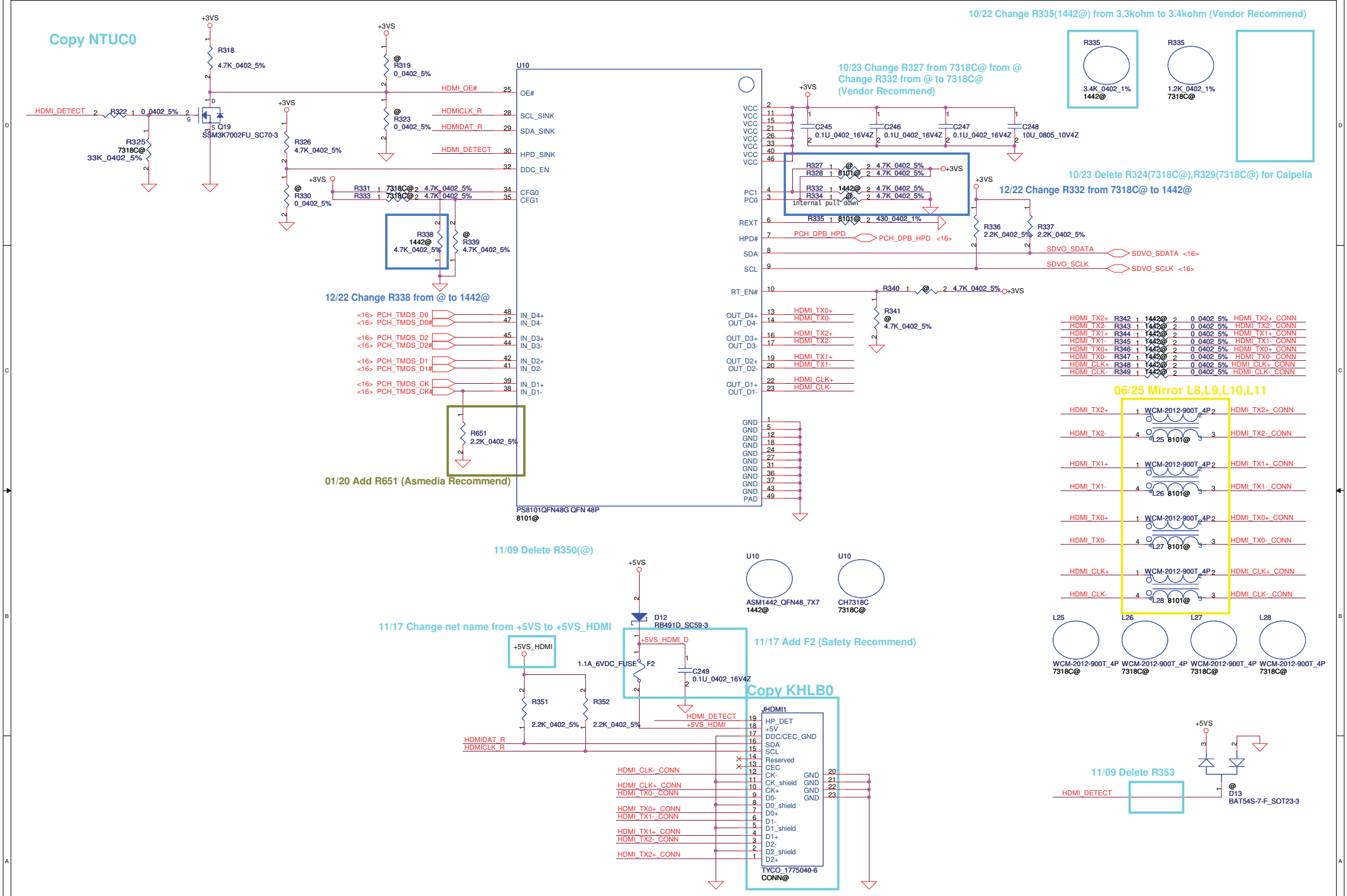
Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 23 of 48



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Compal Electronics, Inc.

Title: **HDMI Level Shifter & Conn.**

Size: Custom | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

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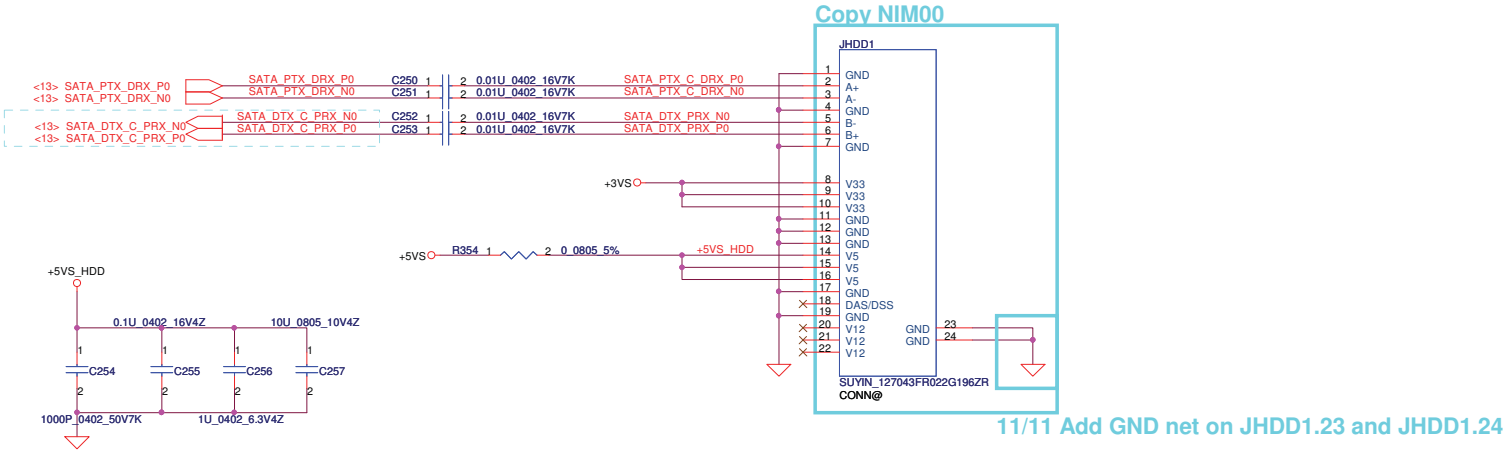
HDD

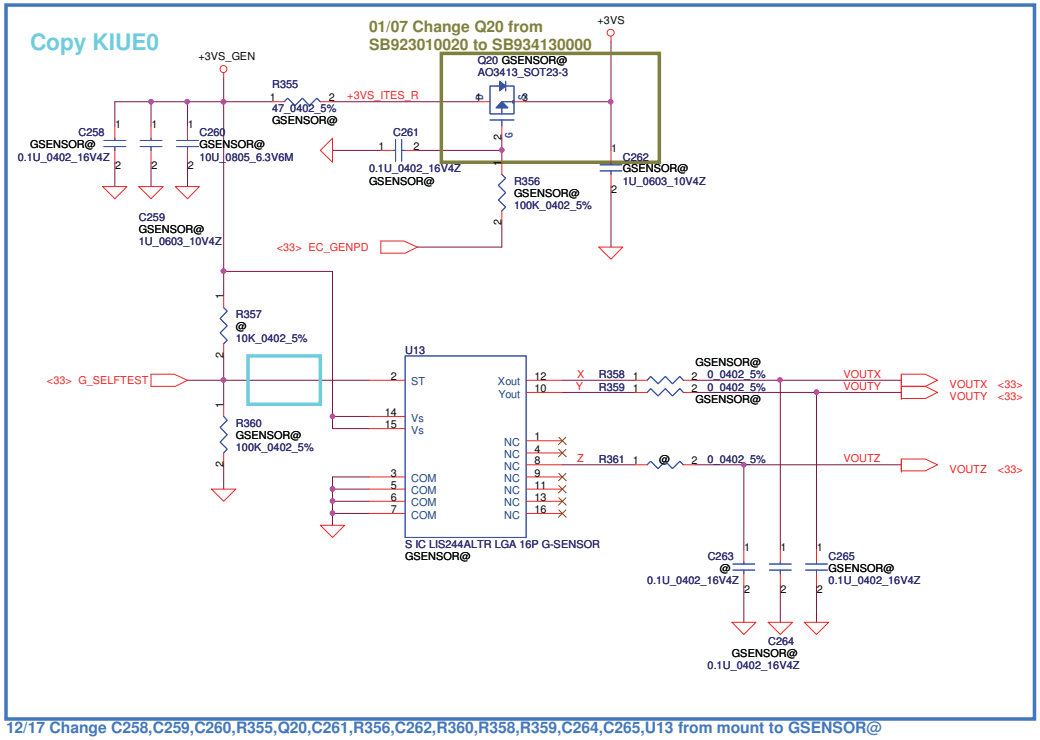
SATA HDD Conn.



11/11 Add GND net on JHDD1.23 and JHDD1.24

G-Sensor

11/11 Correct Q20 footprint



12/17 Change C258,C259,C260,R355,Q20,C261,R356,C262,R360,R358,R359,C264,C265,U13 from mount to GSENSOR@

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Compal Electronics, Inc.

Title: **HDD Conn/G-Sensor**

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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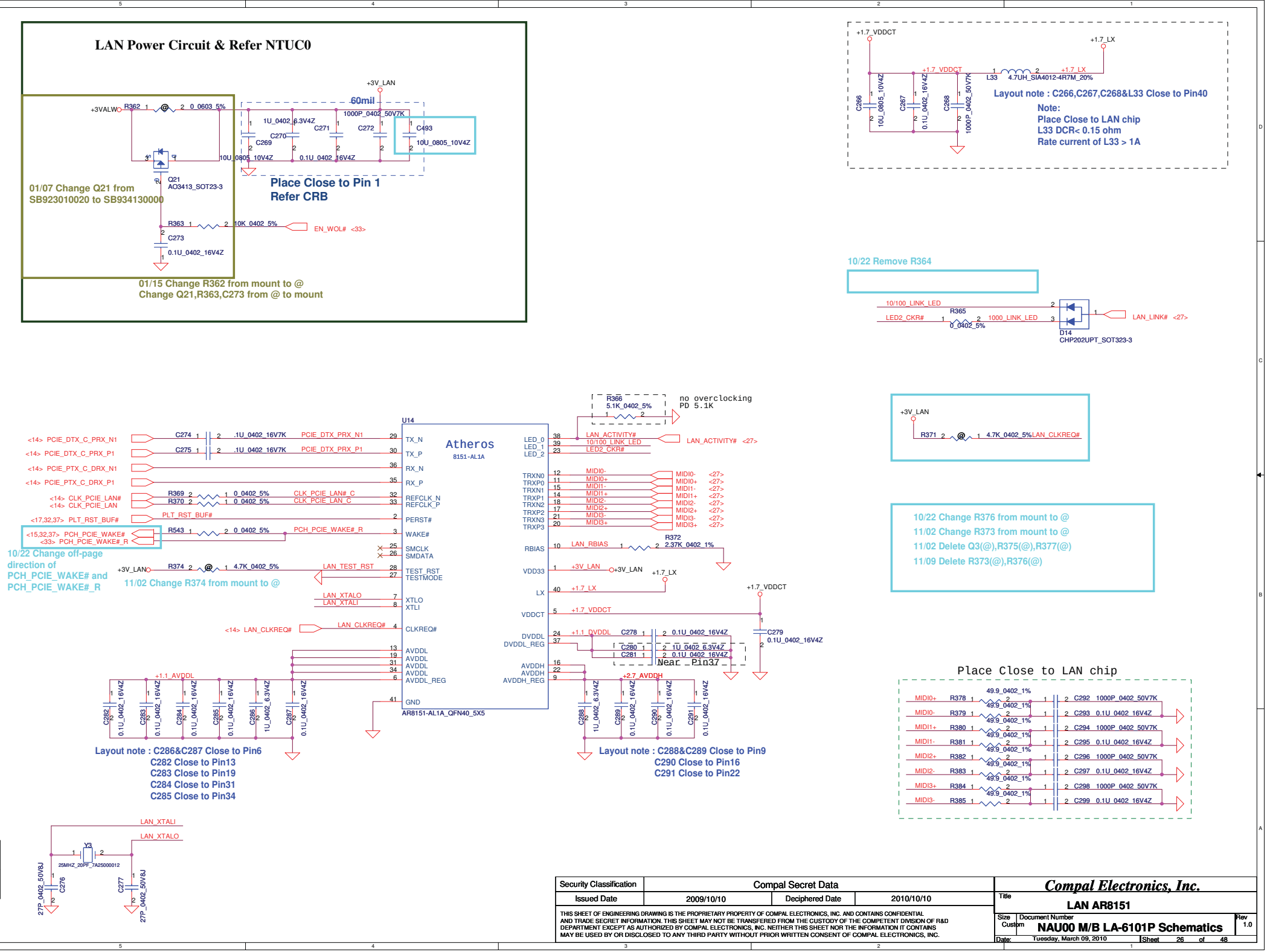
LAN Power Circuit & Refer NTUC0
+3V_LAN
60mil
+3VALW
R362 1 @ 2 0_0603_5%
1U_0402_6.3V4Z
C270
C271
C272
1000P_0402_50V7K
C493
10U_0805_10V4Z
C269
10U_0805_10V4Z
0.1U_0402_16V4Z
Q21
AO3413_SOT23-3
01/07 Change Q21 from
SB923010020 to SB934130000
Place Close to Pin 1
Refer CRB
R363 1 2 10K_0402_5%
EN_WOL# <33>
C273
0.1U_0402_16V4Z
01/15 Change R362 from mount to @
Change Q21,R363,C273 from @ to mount
+1.7_VDDCT
+1.7_LX
L33 4.7UH_SIA4012-4R7M_20%
C266
10U_0805_10V4Z
C267
0.1U_0402_16V4Z
C268
1000P_0402_50V7K
Layout note : C266,C267,C268&L33 Close to Pin40
Note:
Place Close to LAN chip
L33 DCR< 0.15 ohm
Rate current of L33 > 1A
10/22 Remove R364
10/100_LINK_LED
LED2_CKR#
R365
0_0402_5%
1000_LINK_LED
D14
CHP202UPT_SOT323-3
LAN_LINK# <27>
U14
Atheros
8151-AL1A
AR8151-AL1A_QFN40_5X5
<14> PCIE_DTX_C_PRX_N1
<14> PCIE_DTX_C_PRX_P1
<14> PCIE_PTX_C_DRX_N1
<14> PCIE_PTX_C_DRX_P1
C274 .1U_0402_16V7K PCIE_DTX_PRX_N1
C275 .1U_0402_16V7K PCIE_DTX_PRX_P1
<14> CLK_PCIE_LAN#
<14> CLK_PCIE_LAN
R369 0_0402_5% CLK_PCIE_LAN#_C
R370 0_0402_5% CLK_PCIE_LAN_C
<17,32,37> PLT_RST_BUF#
PLT_RST_BUF#
<15,32,37> PCH_PCIE_WAKE#
<33> PCH_PCIE_WAKE#_R
R543 0_0402_5% PCH_PCIE_WAKE#_R
10/22 Change off-page
direction of
PCH_PCIE_WAKE# and
PCH_PCIE_WAKE#_R
+3V_LAN
R374 4.7K_0402_5%
LAN_TEST_RST
11/02 Change R374 from mount to @
LAN_XTALO
LAN_XTALI
<14> LAN_CLKREQ#
LAN_CLKREQ#
TX_N
TX_P
RX_N
RX_P
REFCLK_N
REFCLK_P
PERST#
WAKE#
SMCLK
SMDATA
TEST_RST
TESTMODE
XTLO
XTLI
CLKREQ#
AVDDL
AVDDL
AVDDL
AVDDL
AVDDL_REG
GND
LED_0
LED_1
LED_2
TRXN0
TRXP0
TRXN1
TRXP1
TRXN2
TRXP2
TRXN3
TRXP3
RBIAS
VDD33
LX
VDDCT
DVDDL
DVDDL_REG
AVDDH
AVDDH
AVDDH_REG
R366 5.1K_0402_5%
no overclocking
PD 5.1K
LAN_ACTIVITY#
10/100_LINK_LED
LED2_CKR#
LAN_ACTIVITY# <27>
MIDI0- <27>
MIDI0+ <27>
MIDI1- <27>
MIDI1+ <27>
MIDI2- <27>
MIDI2+ <27>
MIDI3- <27>
MIDI3+ <27>
LAN_RBIAS
R372 2.37K_0402_1%
+3V_LAN
+1.7_LX
+1.7_VDDCT
+1.1_DVDDL
C278 0.1U_0402_16V4Z
C280 1U_0402_6.3V4Z
C281 0.1U_0402_16V4Z
Near Pin37
C279 0.1U_0402_16V4Z
+1.1_AVDDL
+2.7_AVDDH
Layout note : C286&C287 Close to Pin6
C282 Close to Pin13
C283 Close to Pin19
C284 Close to Pin31
C285 Close to Pin34
Layout note : C288&C289 Close to Pin9
C290 Close to Pin16
C291 Close to Pin22
R371 4.7K_0402_5% LAN_CLKREQ#
10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)
Place Close to LAN chip
MIDI0+ R378 49.9_0402_1% C292 1000P_0402_50V7K
MIDI0- R379 49.9_0402_1% C293 0.1U_0402_16V4Z
MIDI1+ R380 49.9_0402_1% C294 1000P_0402_50V7K
MIDI1- R381 49.9_0402_1% C295 0.1U_0402_16V4Z
MIDI2+ R382 49.9_0402_1% C296 1000P_0402_50V7K
MIDI2- R383 49.9_0402_1% C297 0.1U_0402_16V4Z
MIDI3+ R384 49.9_0402_1% C298 1000P_0402_50V7K
MIDI3- R385 49.9_0402_1% C299 0.1U_0402_16V4Z
LAN_XTALI
LAN_XTALO
Y3
25MHZ_20PF_7A25000012
C276 27P_0402_50V8J
C277 27P_0402_50V8J
Security Classification
Compal Secret Data
Issued Date
2009/10/10
Deciphered Date
2010/10/10
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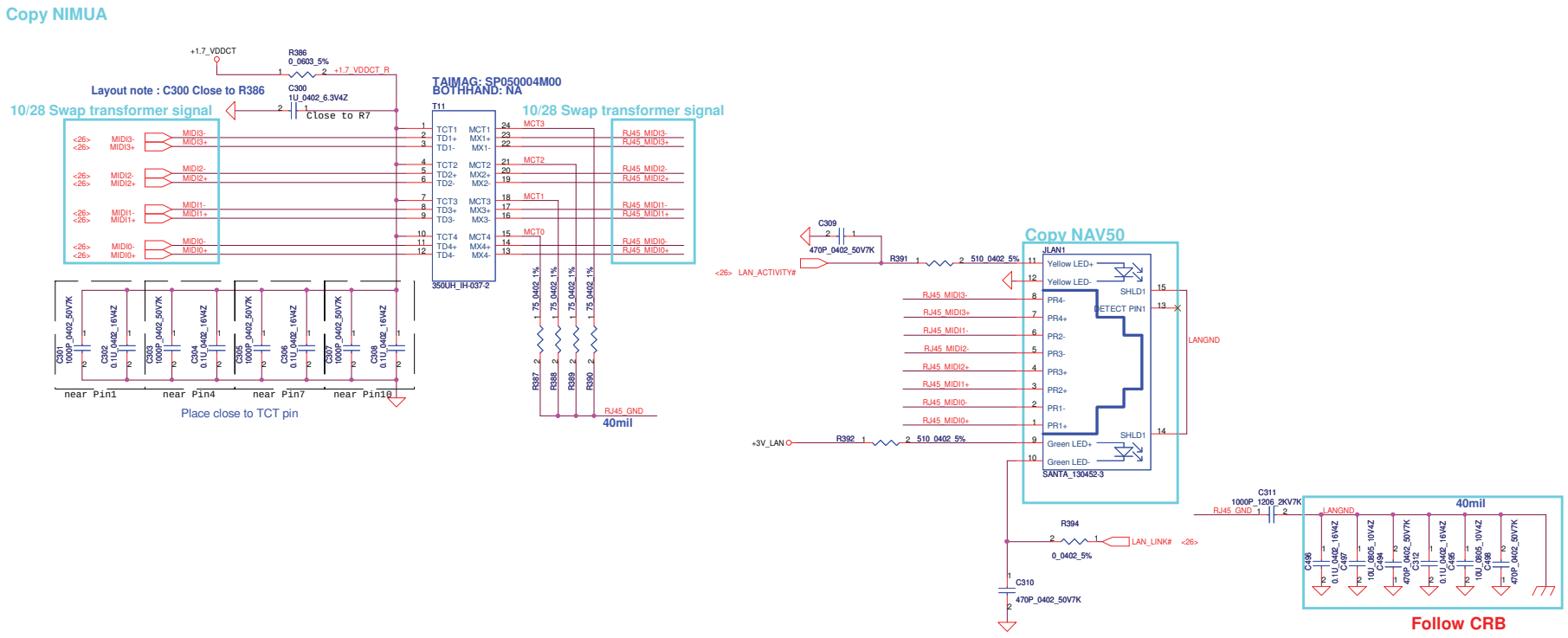
Compal Electronics, Inc.
Title
LAN AR8151
Size Custom
Document Number
NAU00 M/B LA-6101P Schematics
Rev 1.0
Date: Tuesday, March 09, 2010
Sheet 26 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

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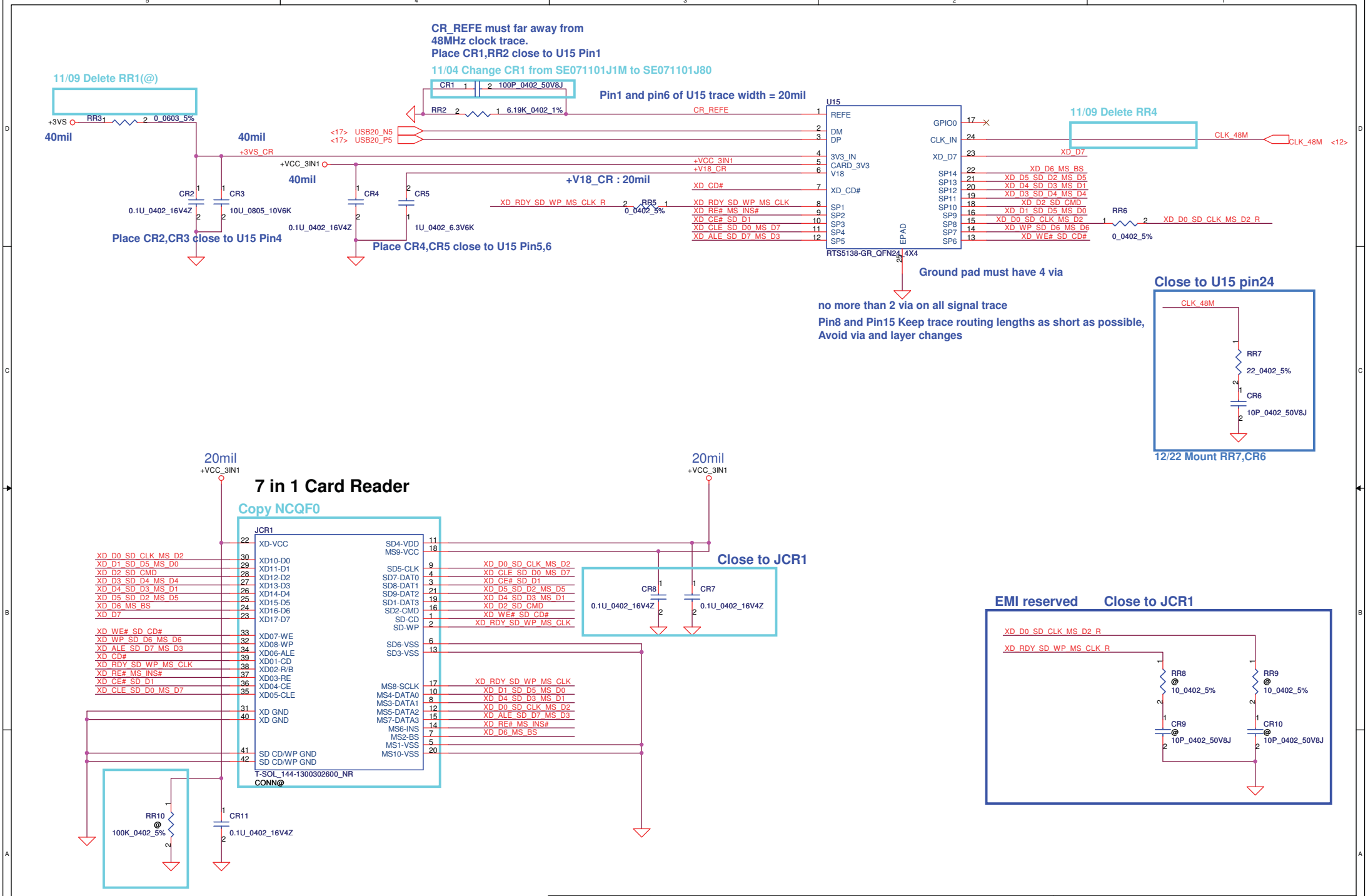
Compal Electronics, Inc.

Title: **LAN Magnetic & RJ45**

Size | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 27 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

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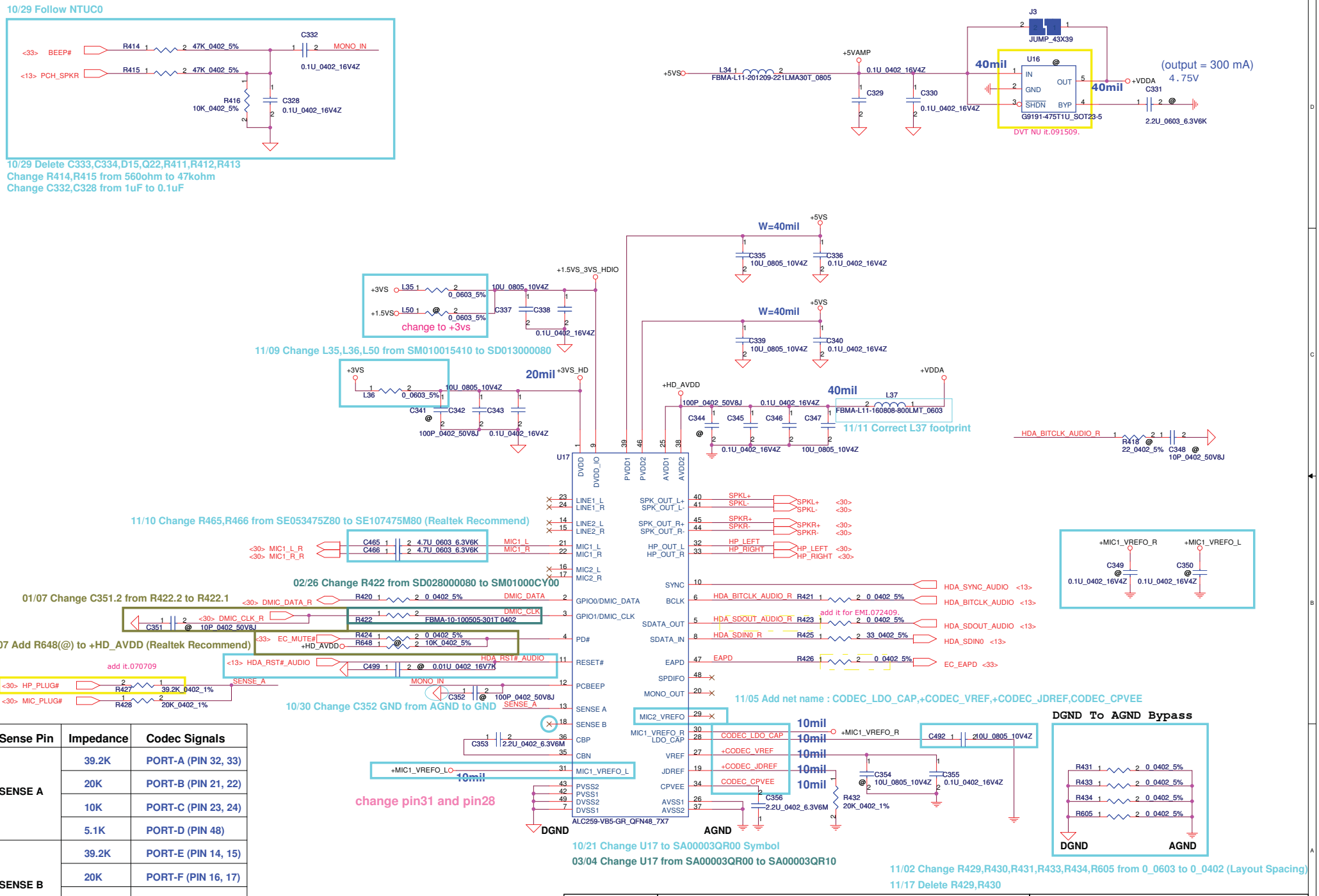
Compal Electronics, Inc.

Title: **Card Reader/7-IN-1 Socket**

Size: Custom | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 28 of 48



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

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Compal Electronics, Inc.

Title: HDA Codec ALC259Q-GR

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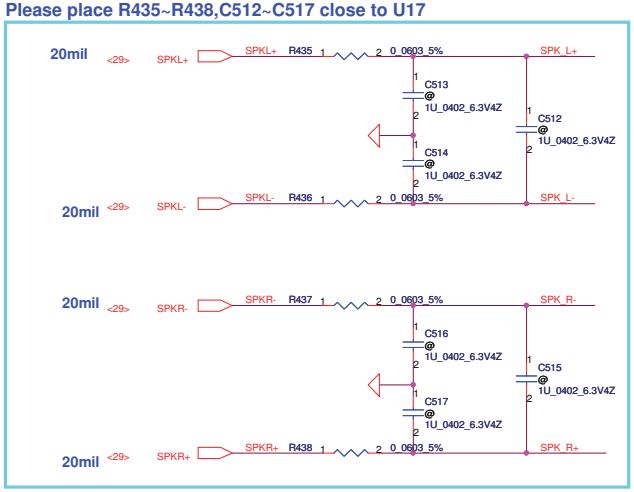
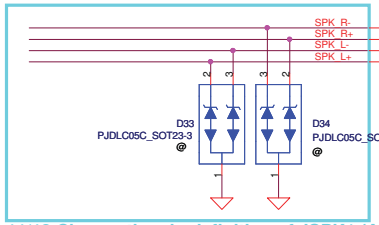
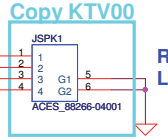
11/11 Change R435~R438 from SM010012010 to SD013000080
11/10 Add C512~C517(@) for EMI (Follow Realtek CRB)
Please place R435~R438,C512~C517 close to U17



Int. Speaker Conn.



Copy KTV00

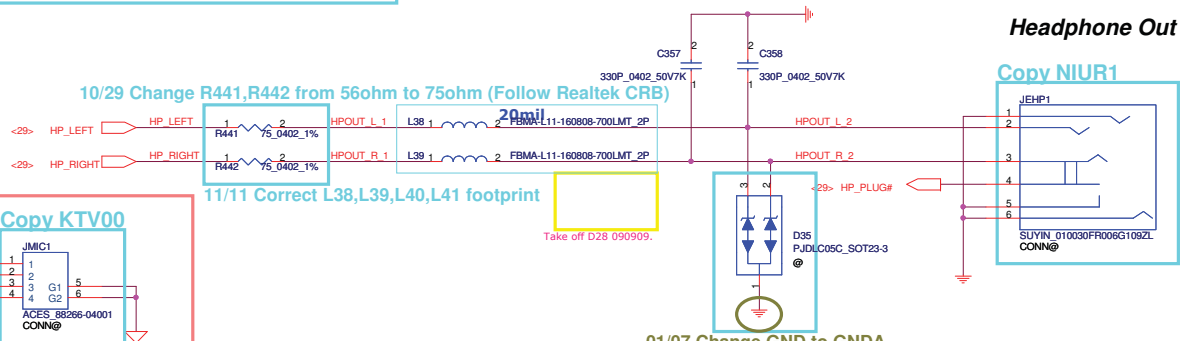


Right
Left

11/18 Change the pin definition of JSPK1 (Audio Recommend)
11/18 Swap D33

Headphone Out

10/29 Change R441,R442 from 56ohm to 75ohm (Follow Realtek CRB)



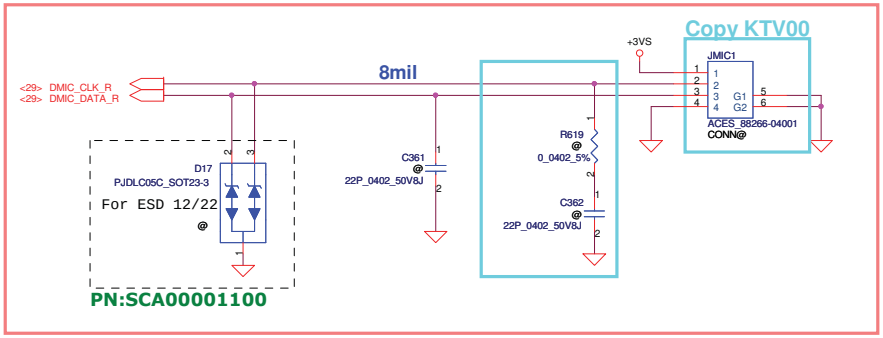
Copy NIUR1

11/11 Correct L38,L39,L40,L41 footprint

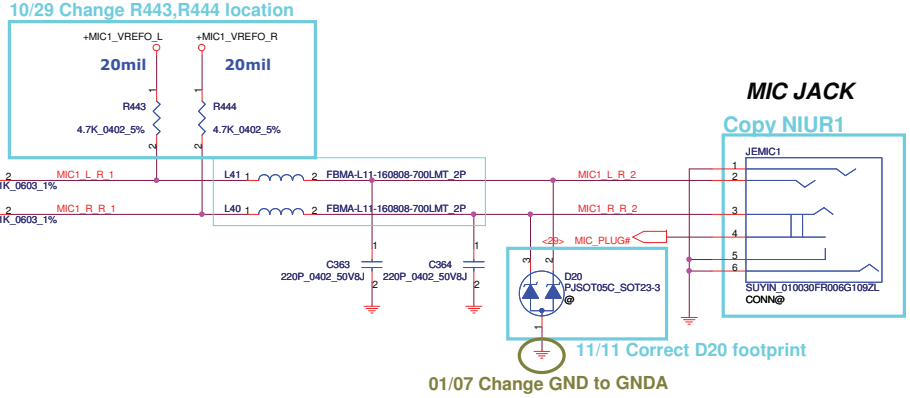
Take off D28 090909.

01/07 Change GND to GNDA

Copy KTV00



10/29 Short D18,D19 (Follow Realtek CRB)
10/29 Change R443,R444 location



MIC JACK

Copy NIUR1

11/11 Correct D20 footprint

01/07 Change GND to GNDA

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Compal Electronics, Inc.

Title: Audio Jack/MIC Conn/SPK Conn

Size: Custom | Document Number: NXXXX M/B LA-6101P Schematics | Rev: 1.0

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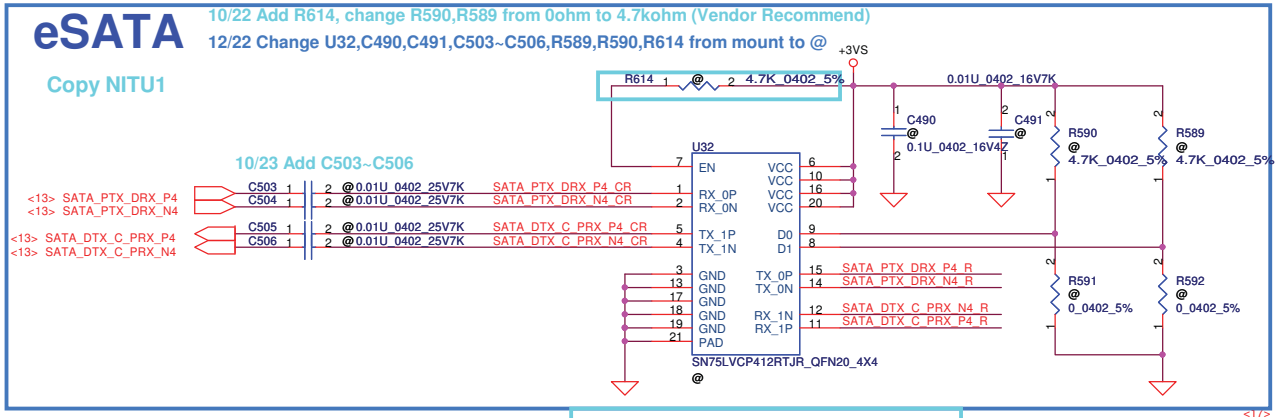
eSATA

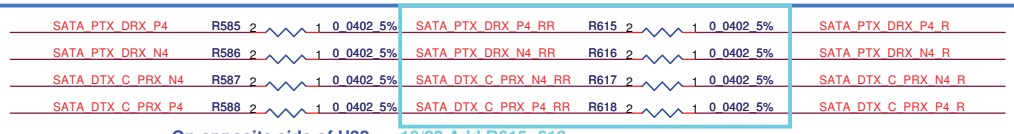
10/22 Add R614, change R590,R589 from 0ohm to 4.7kohm (Vendor Recommend)

12/22 Change U32,C490,C491,C503~C506,R589,R590,R614 from mount to @

Copy NITU1

10/23 Add C503~C506



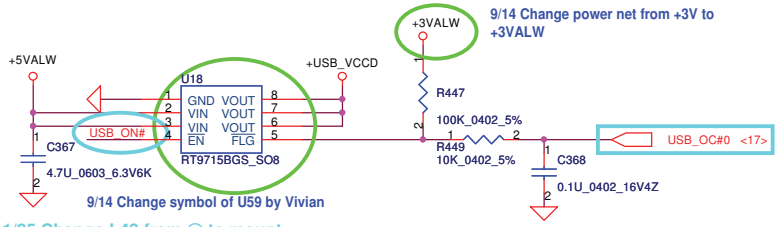


On opposite side of U32

10/23 Add R615~618

12/22 Change R585~R588,R615~R618 from @ to mount

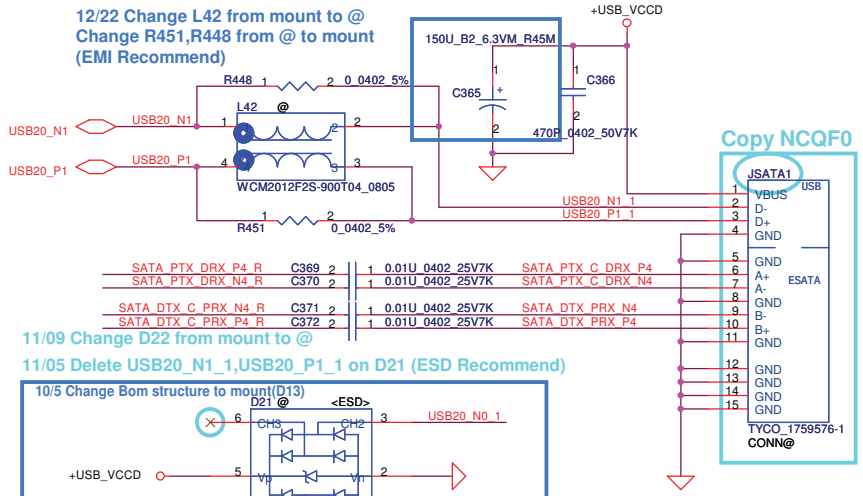
TI:D0 D1					SN75LVCP412		
EN	BA	BB			CHANNEL 0	CHANNEL 1	
0	X	X			Low-power	Low-power	
1	0	0			0dB	0dB	(Default)
1	1	0			2.5dB pre-emphasis	0dB	
1	0	1			0dB	2.5dB pre-emphasis	
1	1	1			2.5dB pre-emphasis	2.5dB pre-emphasis	



11/25 Change L42 from @ to mount
Change R451,R448 from mount to @
(EMI Recommend)

12/22 Change L42 from mount to @
Change R451,R448 from @ to mount
(EMI Recommend)

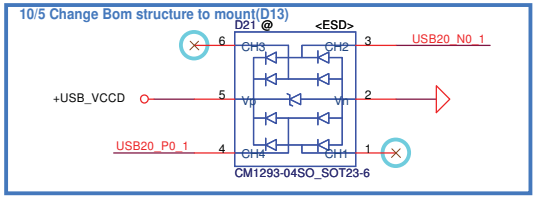
12/27 Change C365 from SGA00002N80 to SGA00001E00



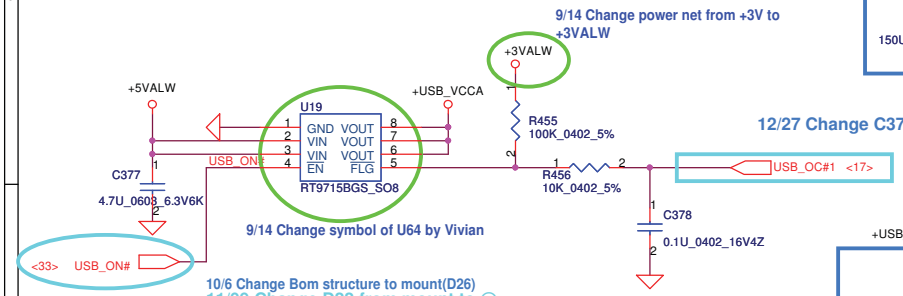
11/09 Change D22 from mount to @

11/05 Delete USB20_N1_1,USB20_P1_1 on D21 (ESD Recommend)

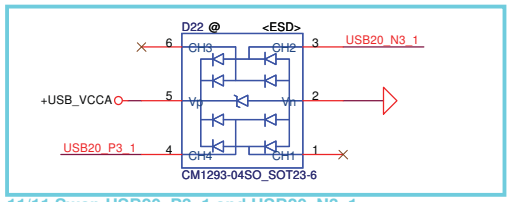
10/5 Change Bom structure to mount(D13)



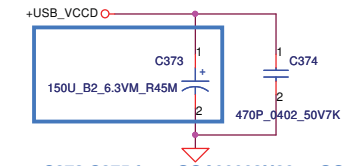
USB Port



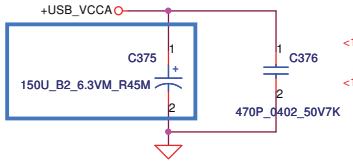
10/6 Change Bom structure to mount(D26)
11/09 Change D22 from mount to @

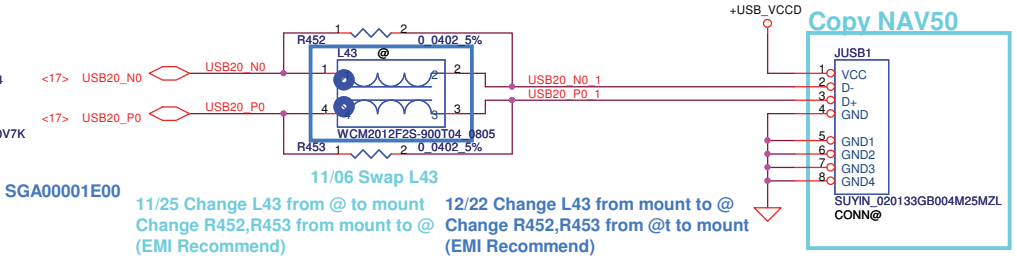


11/11 Swap USB20_P3_1 and USB20_N3_1



12/27 Change C373,C375 from SGA00002N80 to SGA00001E00

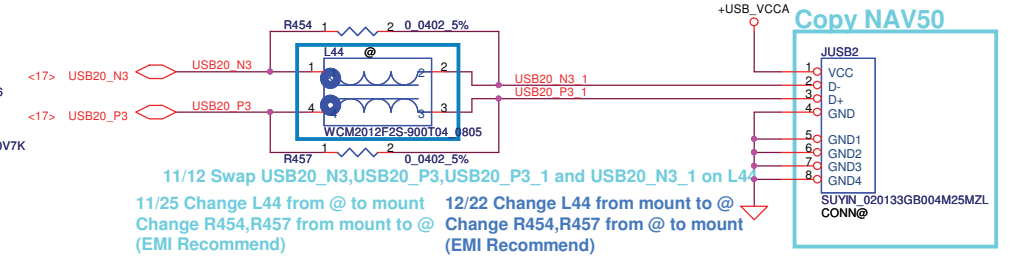




11/06 Swap L43

11/25 Change L43 from @ to mount
Change R452,R453 from mount to @
(EMI Recommend)

12/22 Change L43 from mount to @
Change R452,R453 from @t to mount
(EMI Recommend)



11/12 Swap USB20_N3,USB20_P3,USB20_P3_1 and USB20_N3_1 on L44

11/25 Change L44 from @ to mount
Change R454,R457 from mount to @
(EMI Recommend)

12/22 Change L44 from mount to @
Change R454,R457 from @ to mount
(EMI Recommend)

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Compal Electronics, Inc.

Title: USB / BT / eSATA

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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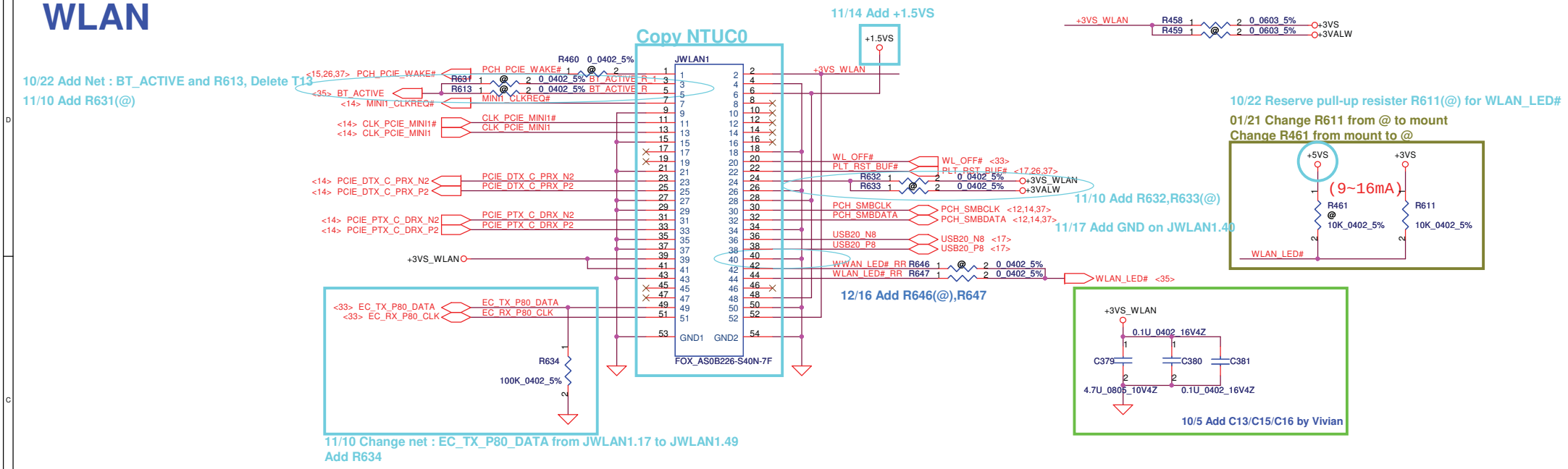
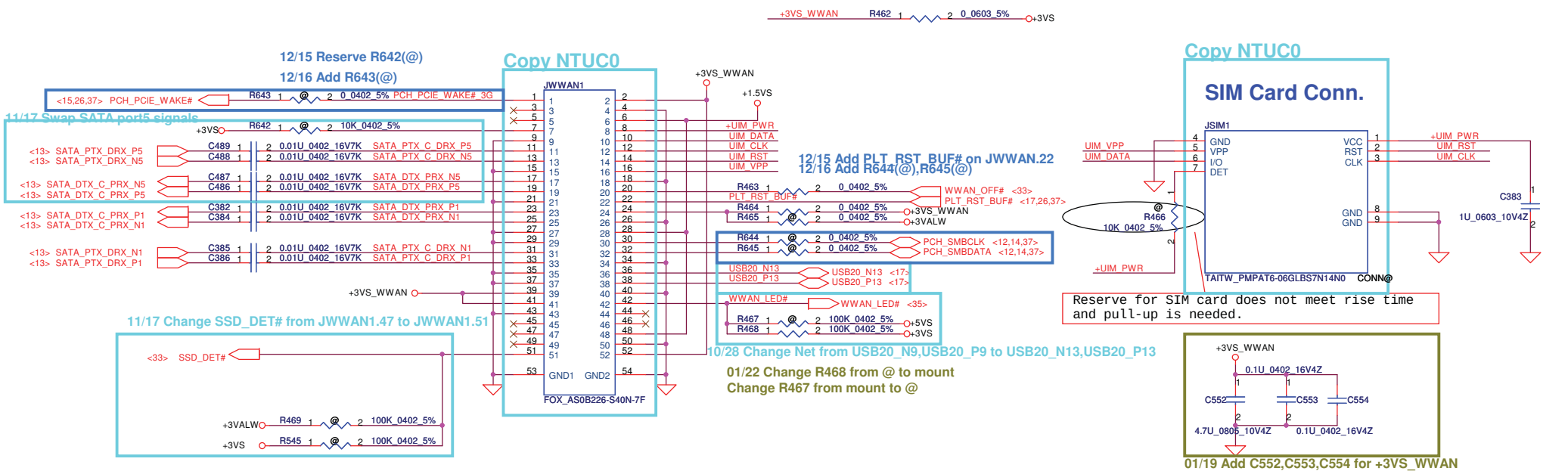
WLAN



WWAN



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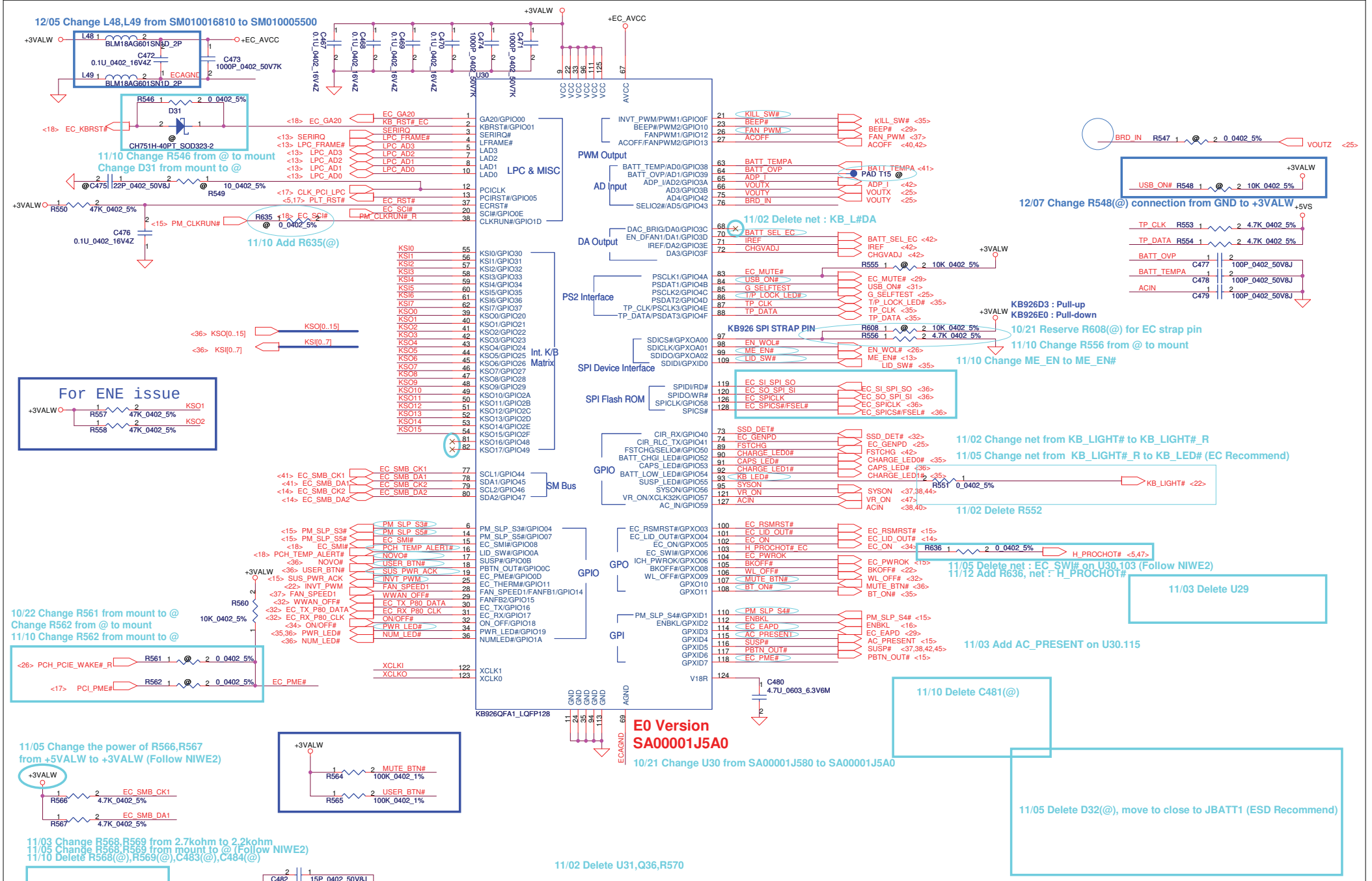
Compal Electronics, Inc.

Title: **WLAN/WWAN**

Size: Custom | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 32 of 48



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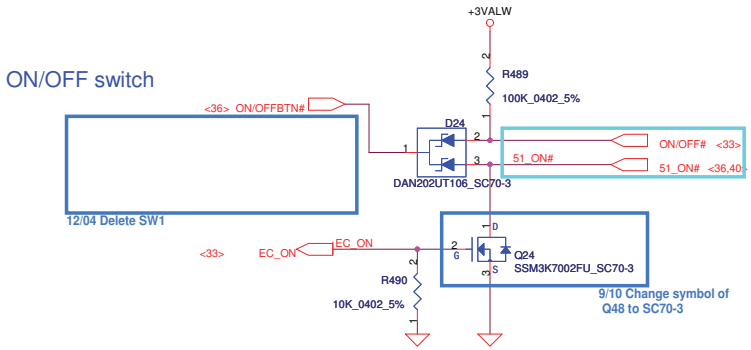
Compal Electronics, Inc.

Title: **EC ENE-KB926**

Size: Custom | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 33 of 48

Power Button



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

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Compal Electronics, Inc.

Title: Power OK/PBN/TP Lock/LED

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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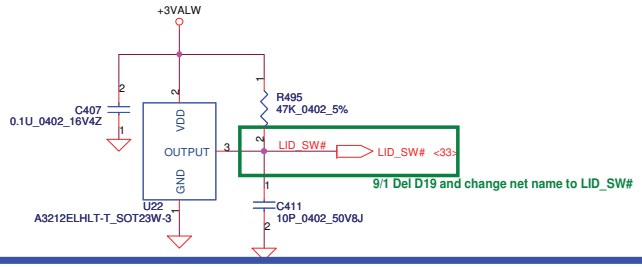
Lid Switch

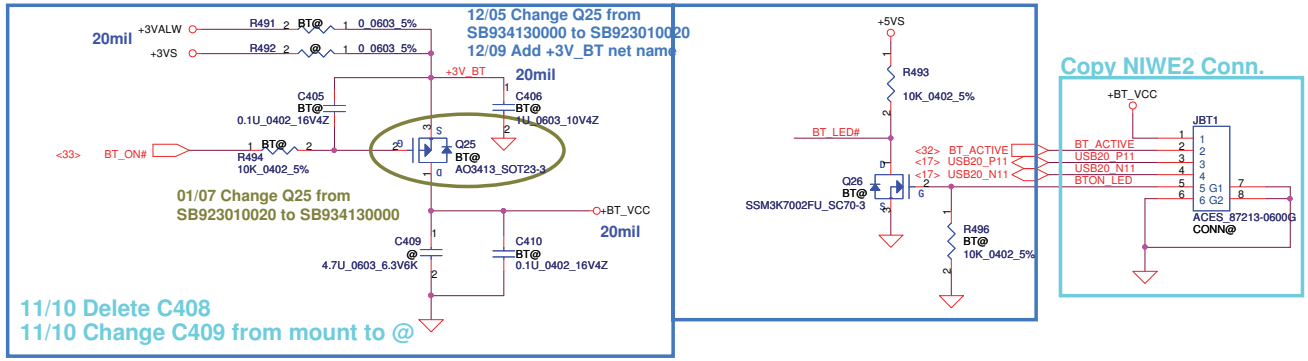
(Hall Effect Switch)



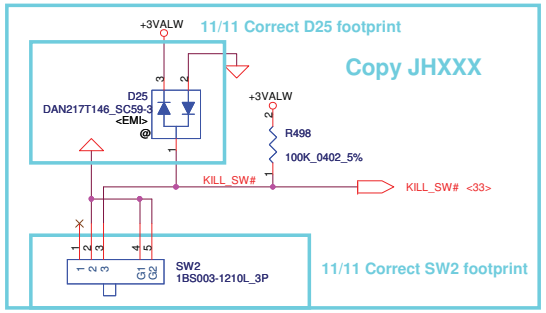
9/1 Del D19 and change net name to LID_SW#

BT

12/17 Change R491,C405,R494,C406,Q25,C410,Q26,R496 from mount to BT@

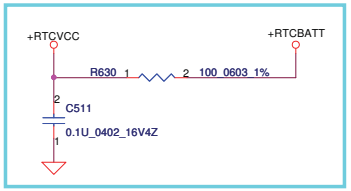


KILL Switch



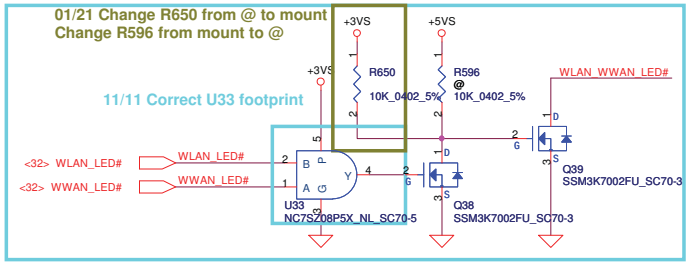
RTC

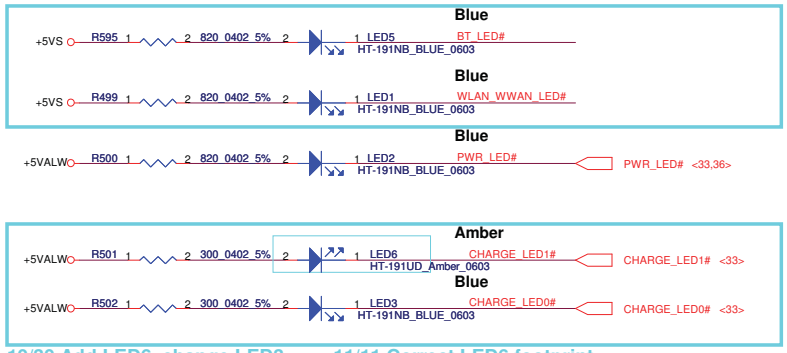
11/10 Delete D26,C412,R497, Add R630,C511 (Follow NIWE2)



LED

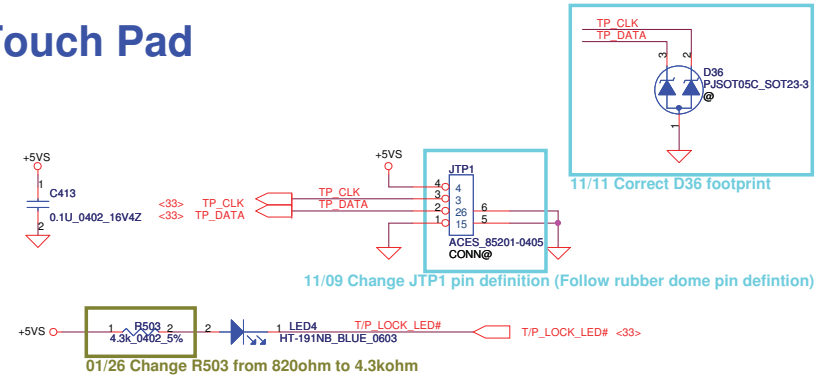
01/20 Add R650(@)





10/30 Add LED6, change LED3 11/11 Correct LED6 footprint

Touch Pad



01/26 Change R503 from 820ohm to 4.3kohm

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Compal Electronics, Inc.

Title: LID/RTC/BT/TP/KILL SW/LED

Size | Document Number: NAU00 M/B LA-6101P Schematics | Rev 1.0

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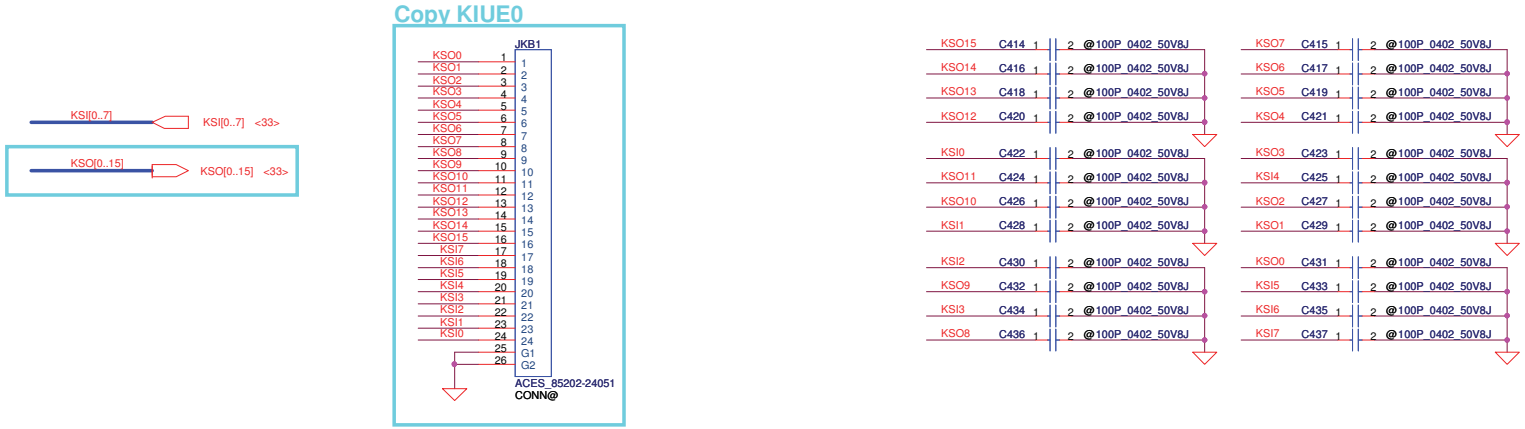
INT_KBD Conn.



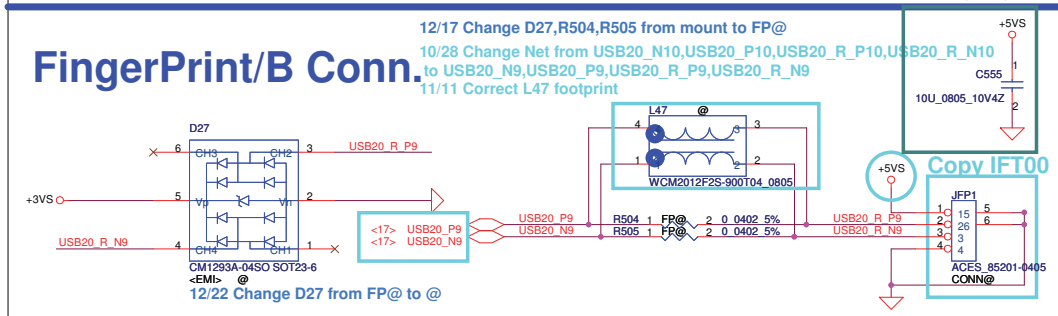
03/02 Add C555 (10uF) for FP power

FingerPrint/B Conn.

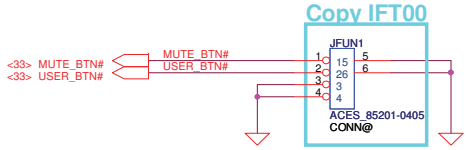
12/17 Change D27,R504,R505 from mount to FP@

10/28 Change Net from USB20_N10,USB20_P10,USB20_R_P10,USB20_R_N10 to USB20_N9,USB20_P9,USB20_R_P9,USB20_R_N9

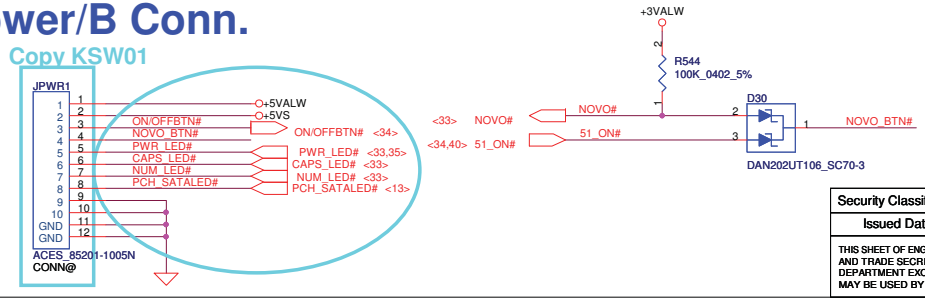
11/11 Correct L47 footprint



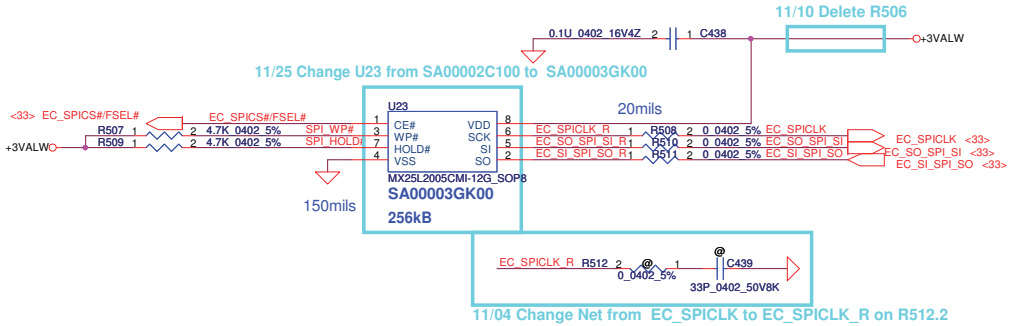
Function/B Conn.



Power/B Conn.



EC SPI ROM



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Title: BIOS/KBD/Fun_B/PWR_B/FP_B

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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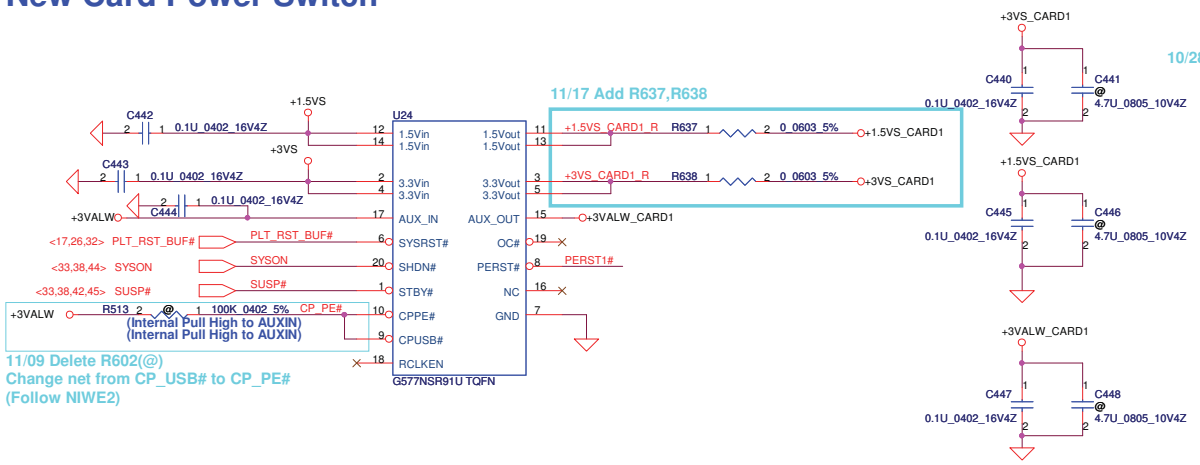
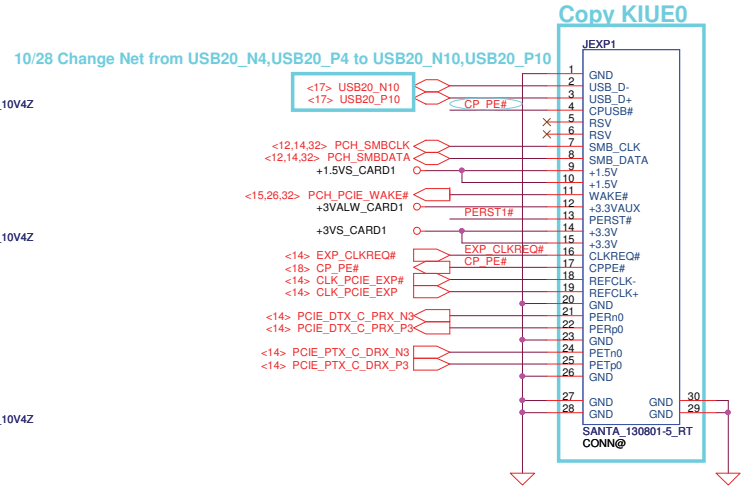
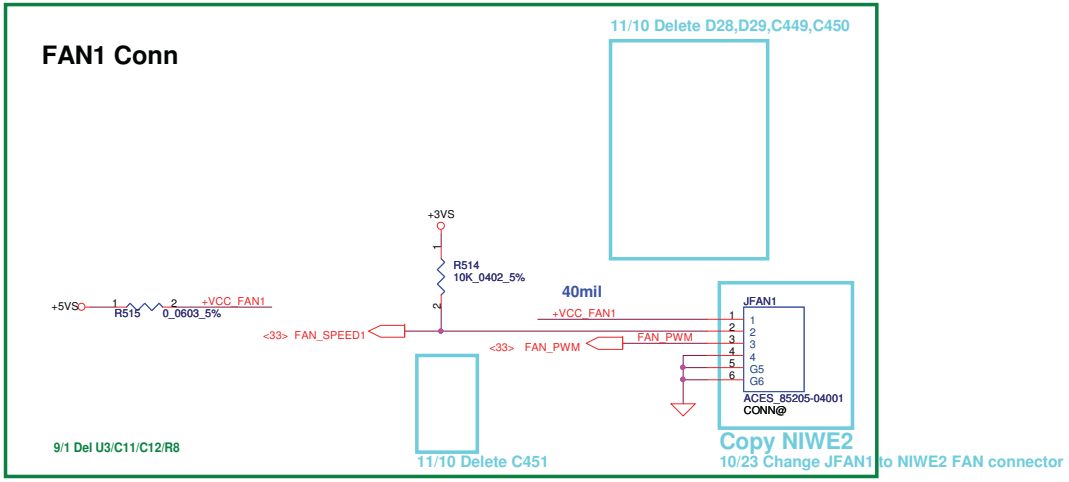
New Card Power Switch

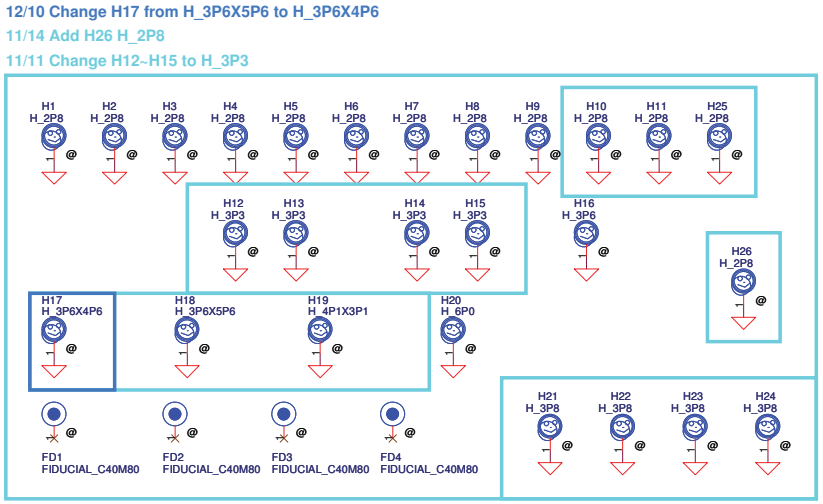


New Card Socket



FAN1 Conn





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Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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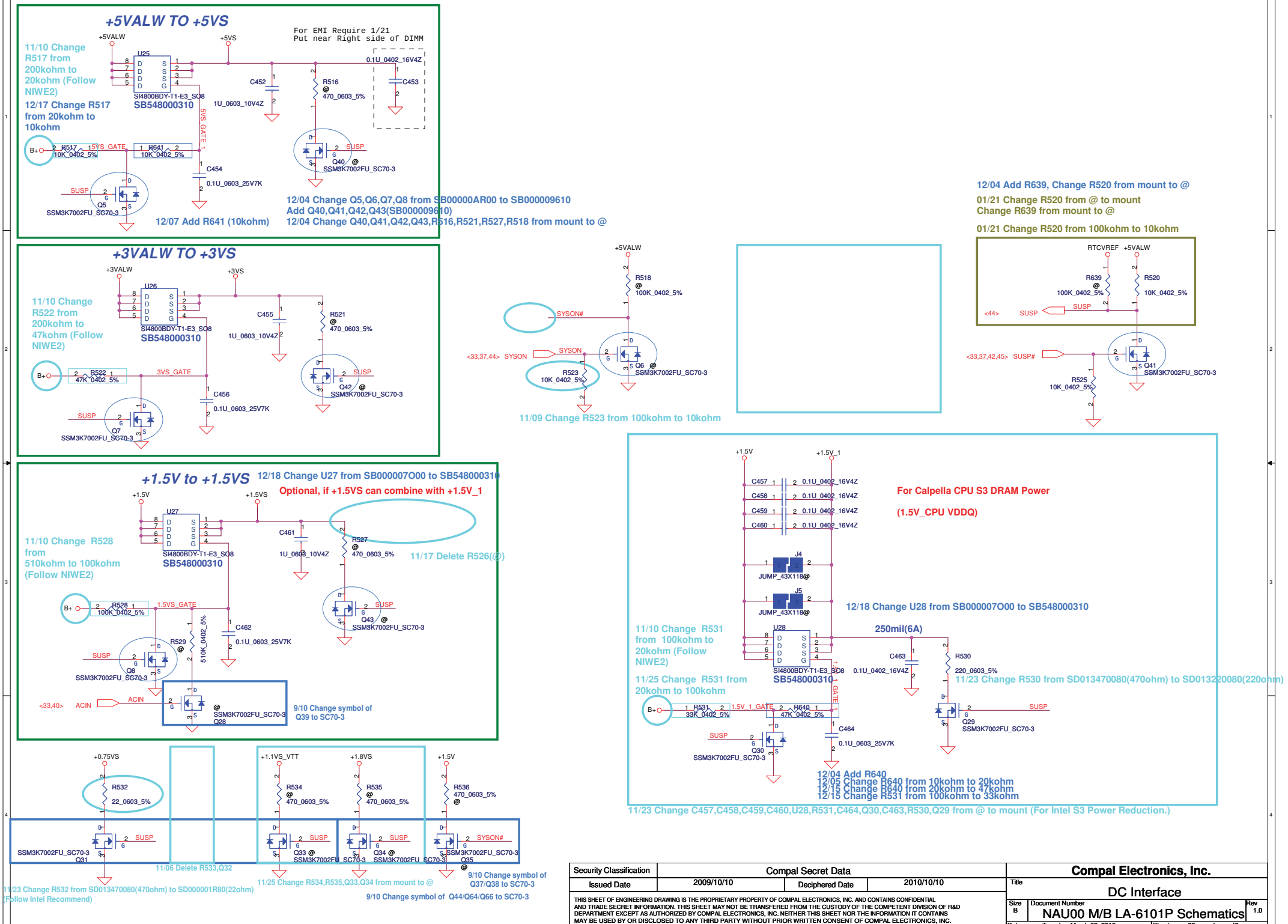
+5VALW TO +5VS
11/10 Change R517 from 200kohm to 20kohm (Follow NIWE2)
12/17 Change R517 from 20kohm to 10kohm
For EMI Require 1/21
Put near Right side of DIMM
U25
SI4800BDY-T1-E3_SO8
SB548000310
+5VALW
+5VS
C452
1U_0603_10V4Z
R516
@
470_0603_5%
0.1U_0402_16V4Z
C453
R517
10K_0402_5%
R641
10K_0402_5%
5VS_GATE
C454
0.1U_0603_25V7K
Q40
@
SSM3K7002FU_SC70-3
Q5
SSM3K7002FU_SC70-3
12/07 Add R641 (10kohm)
12/04 Change Q5,Q6,Q7,Q8 from SB00000AR00 to SB000009610
Add Q40,Q41,Q42,Q43(SB000009610)
12/04 Change Q40,Q41,Q42,Q43,R516,R521,R527,R518 from mount to @
+3VALW TO +3VS
11/10 Change R522 from 200kohm to 47kohm (Follow NIWE2)
U26
SI4800BDY-T1-E3_SO8
SB548000310
+3VALW
+3VS
C455
1U_0603_10V4Z
R521
@
470_0603_5%
R522
47K_0402_5%
3VS_GATE
C456
0.1U_0603_25V7K
Q42
@
SSM3K7002FU_SC70-3
Q7
SSM3K7002FU_SC70-3
+5VALW
R518
@
100K_0402_5%
SYSON#
<33,37,44> SYSON
R523
10K_0402_5%
Q6
@
SSM3K7002FU_SC70-3
11/09 Change R523 from 100kohm to 10kohm
12/04 Add R639, Change R520 from mount to @
01/21 Change R520 from @ to mount
Change R639 from mount to @
01/21 Change R520 from 100kohm to 10kohm
RTCVREF
+5VALW
R639
@
100K_0402_5%
R520
10K_0402_5%
<44> SUSP
<33,37,42,45> SUSP#
Q41
SSM3K7002FU_SC70-3
R525
10K_0402_5%
+1.5V to +1.5VS
12/18 Change U27 from SB000007O00 to SB548000310
Optional, if +1.5VS can combine with +1.5V_1
11/10 Change R528 from 510kohm to 100kohm (Follow NIWE2)
U27
SI4800BDY-T1-E3_SO8
SB548000310
+1.5V
+1.5VS
C461
1U_0603_10V4Z
R527
@
470_0603_5%
11/17 Delete R526(@)
R528
100K_0402_5%
1.5VS_GATE
C462
0.1U_0603_25V7K
R529
@
510K_0402_5%
Q43
@
SSM3K7002FU_SC70-3
Q8
SSM3K7002FU_SC70-3
<33,40> ACIN
@
SSM3K7002FU_SC70-3
Q28
9/10 Change symbol of Q39 to SC70-3
+1.5V
+1.5V_1
C457 0.1U_0402_16V4Z
C458 0.1U_0402_16V4Z
C459 0.1U_0402_16V4Z
C460 0.1U_0402_16V4Z
For Calpella CPU S3 DRAM Power
(1.5V_CPU VDDQ)
J4
JUMP_43X118@
J5
JUMP_43X118@
12/18 Change U28 from SB000007O00 to SB548000310
250mil(6A)
11/10 Change R531 from 100kohm to 20kohm (Follow NIWE2)
11/25 Change R531 from 20kohm to 100kohm
U28
SI4800BDY-T1-E3_SO8
SB548000310
C463
0.1U_0402_16V4Z
R530
220_0603_5%
11/23 Change R530 from SD013470080(470ohm) to SD013220080(220ohm)
R531
33K_0402_5%
1.5V_1_GATE
R640
47K_0402_5%
C464
0.1U_0603_25V7K
Q29
SSM3K7002FU_SC70-3
Q30
SSM3K7002FU_SC70-3
12/04 Add R640
12/05 Change R640 from 10kohm to 20kohm
12/15 Change R640 from 20kohm to 47kohm
12/15 Change R531 from 100kohm to 33kohm
11/23 Change C457,C458,C459,C460,U28,R531,C464,Q30,C463,R530,Q29 from @ to mount (For Intel S3 Power Reduction.)
+0.75VS
R532
22_0603_5%
Q31
11/06 Delete R533,Q32
11/23 Change R532 from SD013470080(470ohm) to SD000001R80(22ohm)
(Follow Intel Recommend)
+1.1VS_VTT
+1.8VS
+1.5V
R534
@
470_0603_5%
R535
@
470_0603_5%
R536
470_0603_5%
@
Q33
@
SSM3K7002FU_SC70-3
Q34
@
SSM3K7002FU_SC70-3
Q35
@
SSM3K7002FU_SC70-3
11/25 Change R534,R535,Q33,Q34 from mount to @
9/10 Change symbol of Q37/Q38 to SC70-3
9/10 Change symbol of Q44/Q64/Q66 to SC70-3
SUSP
SYSON#
Security Classification
Compal Secret Data
Issued Date
2009/10/10
Deciphered Date
2010/10/10
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Title
DC Interface
Size
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Document Number
NAU00 M/B LA-6101P Schematics
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1.0
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Tuesday, March 09, 2010
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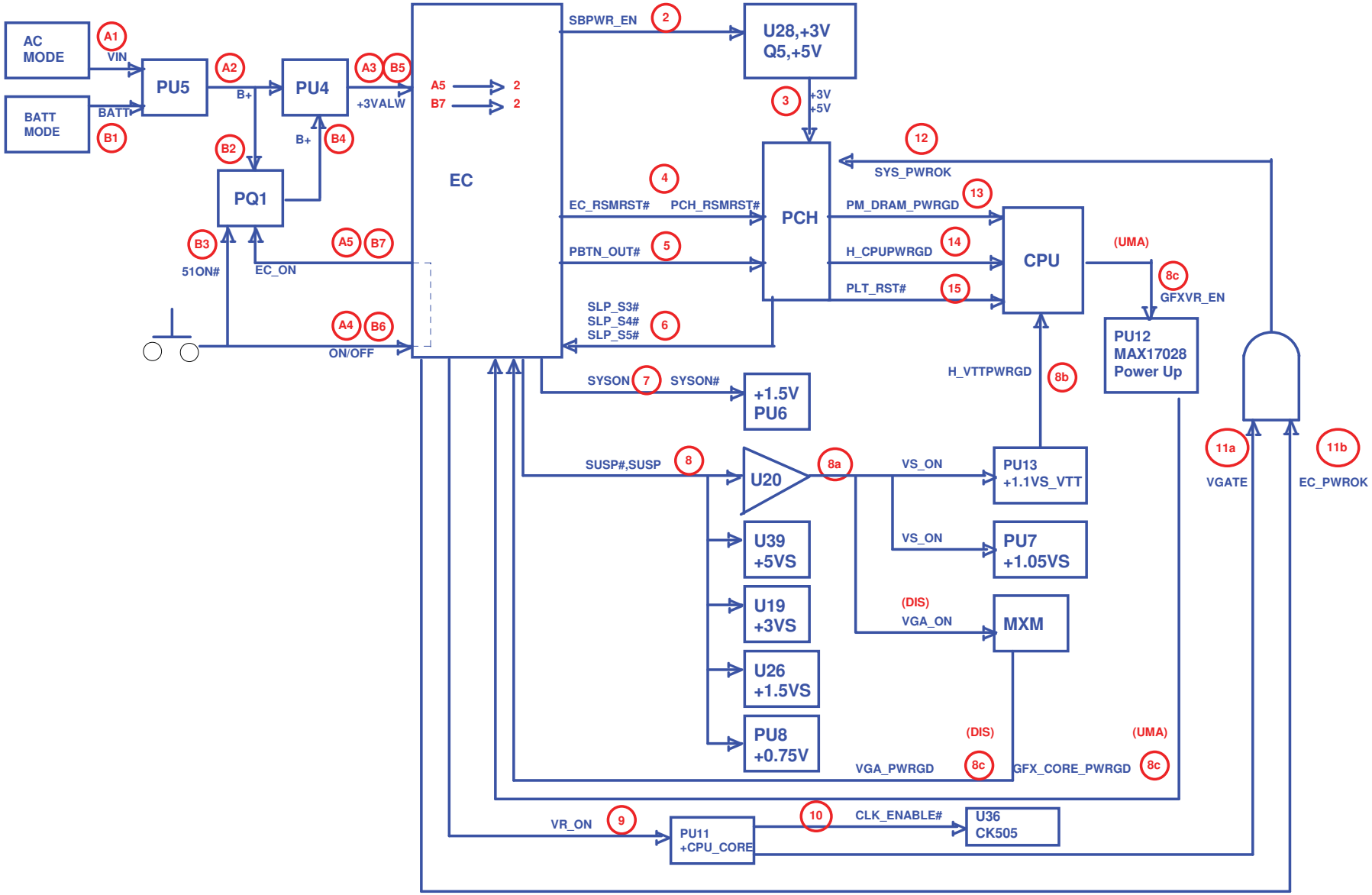
COMPAL CONFIDENTIAL

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



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Title: Power Sequence Block Diagram

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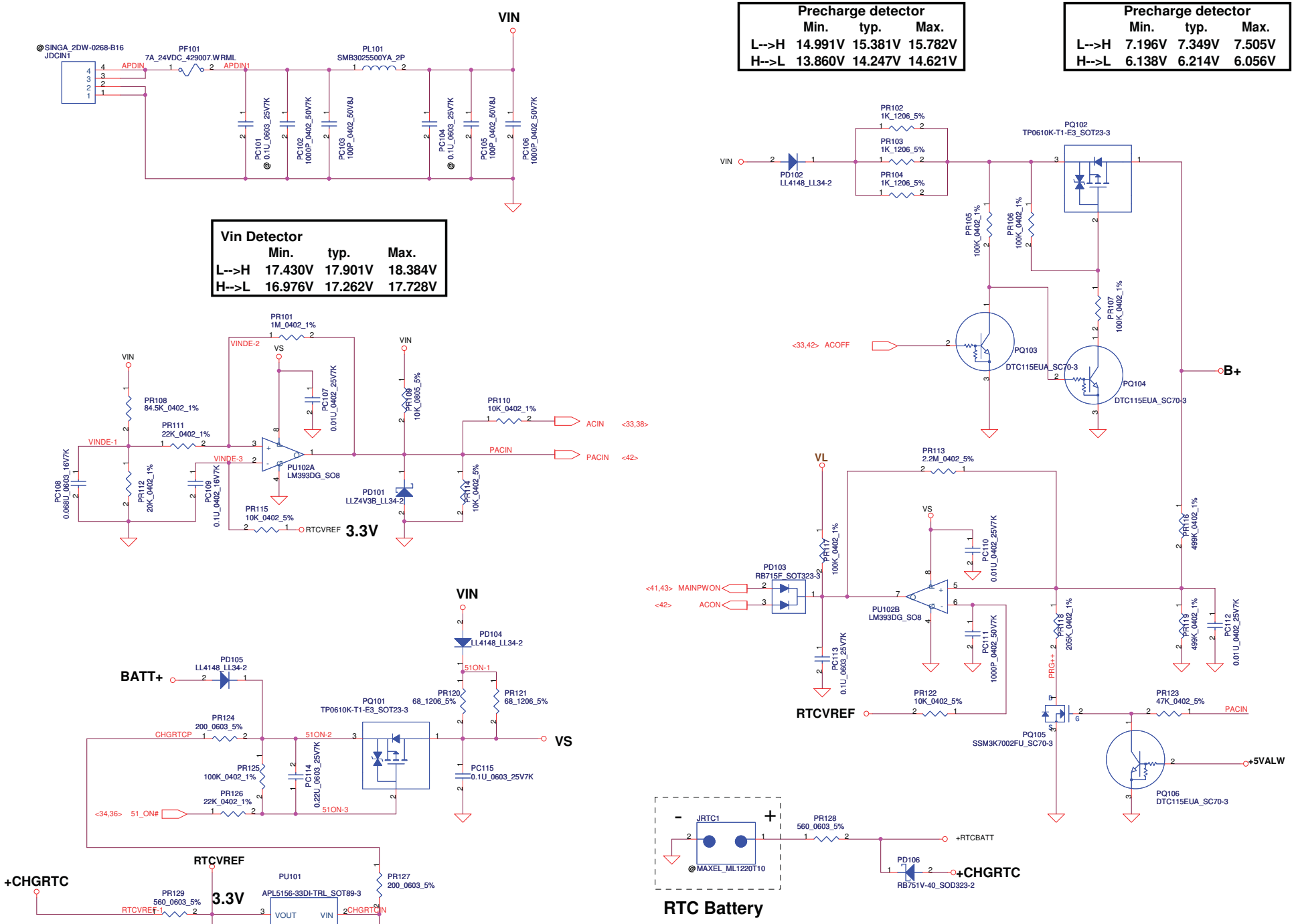

ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

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Title: DCIN & DETECTOR

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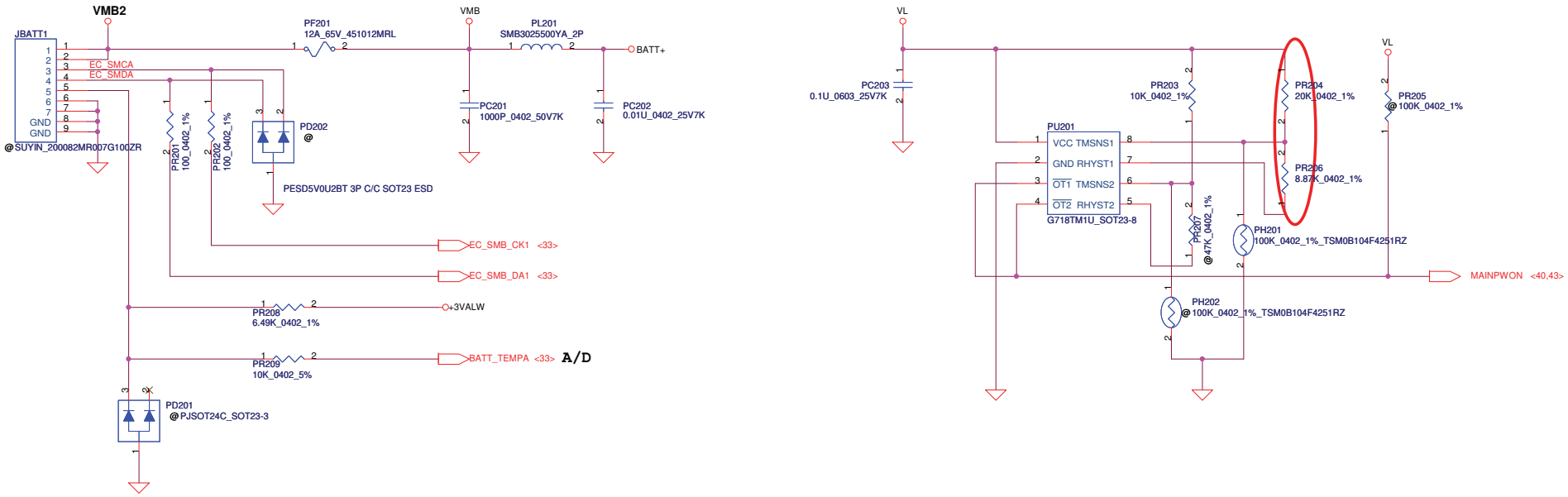
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



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Title: BATTERY CONN / OTP

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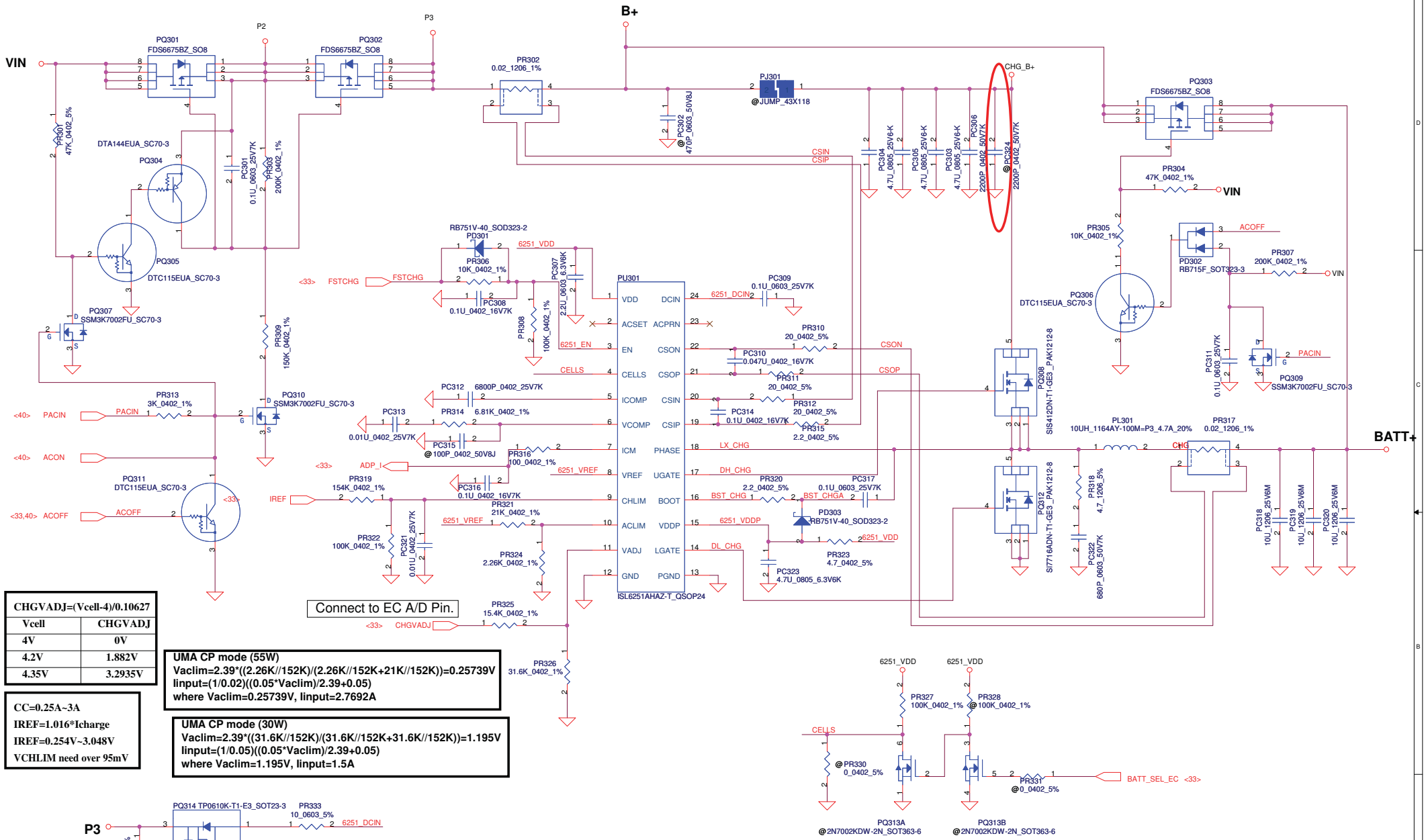

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

UMA CP mode (55W)
Vaclim=2.39*((2.26K//152K)/(2.26K//152K+21K//152K))=0.25739V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.25739V, Iinput=2.7692A

UMA CP mode (30W)
Vaclim=2.39*((31.6K//152K)/(31.6K//152K+31.6K//152K))=1.195V
Iinput=(1/0.05)((0.05*Vaclim)/2.39+0.05)
where Vaclim=1.195V, Iinput=1.5A

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Title: **CHARGER**

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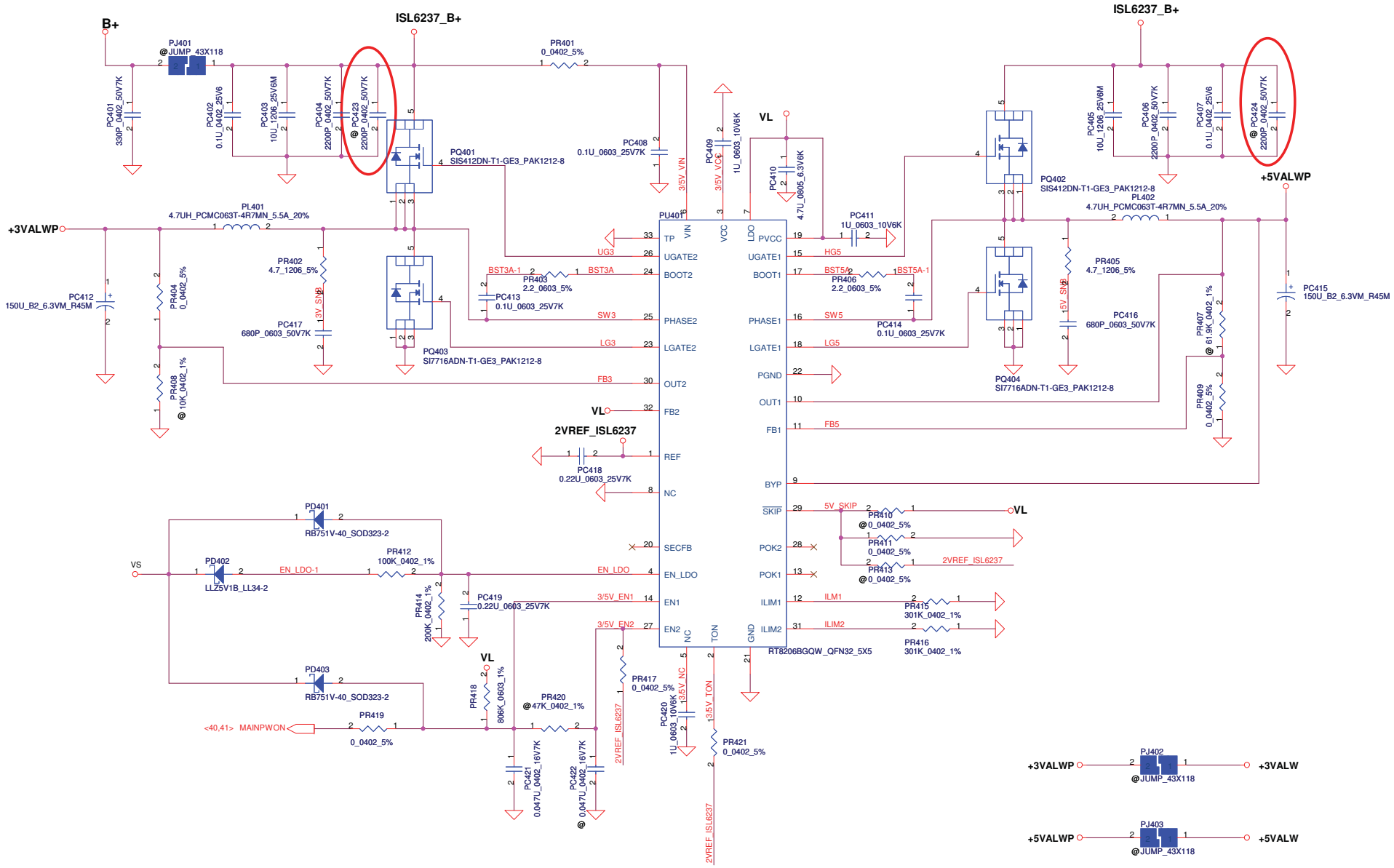

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Issued Date	2009/10/10	Deciphered Date	2010/01/06

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Title: 3VALW/5VALW

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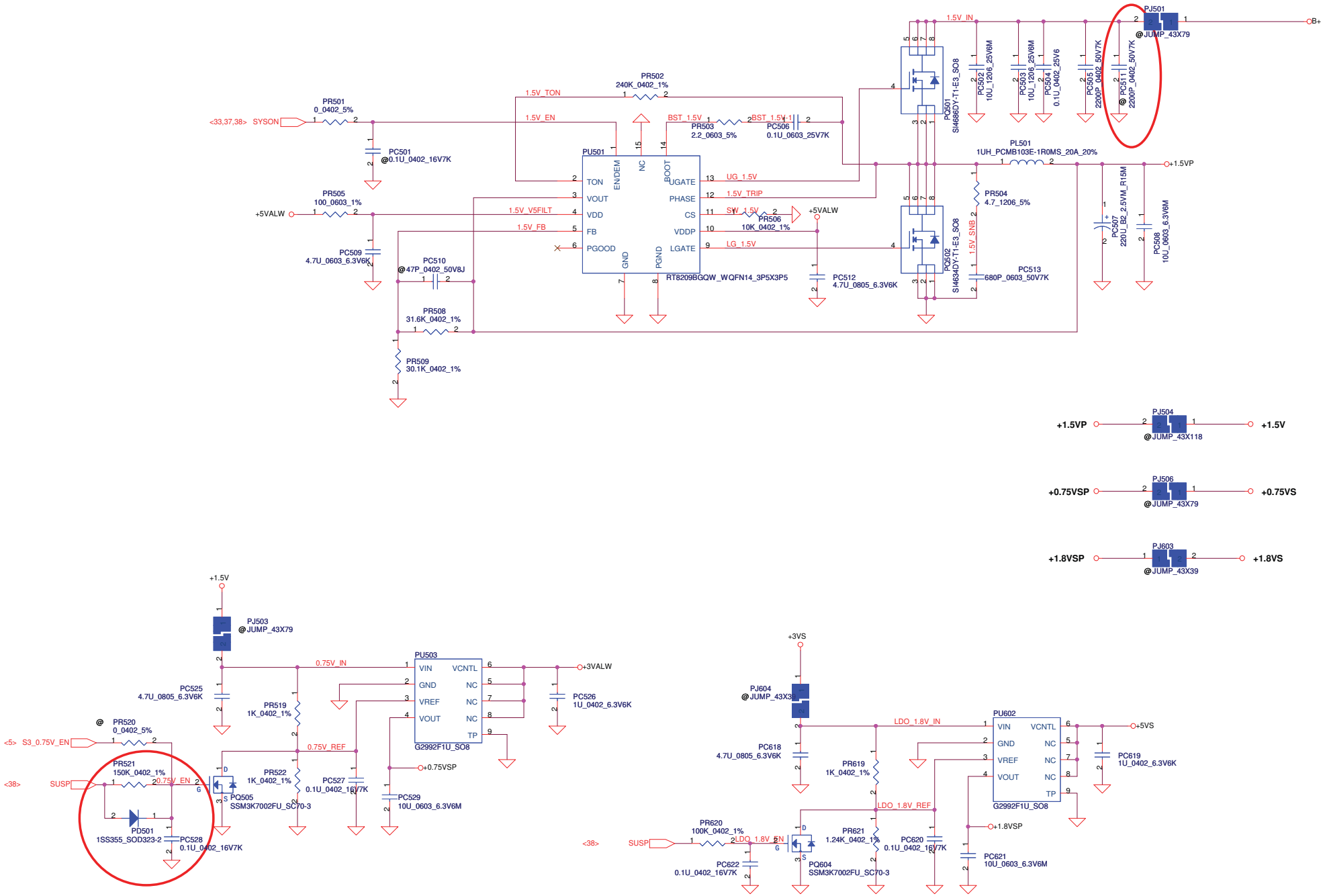

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/10/10	Deciphered Date	2010/01/06	Title: 1.5V/0.75V/1.8V
				Size: Document Number: Rev 0.1
				Date: Tuesday, March 09, 2010 Sheet 44 of 48

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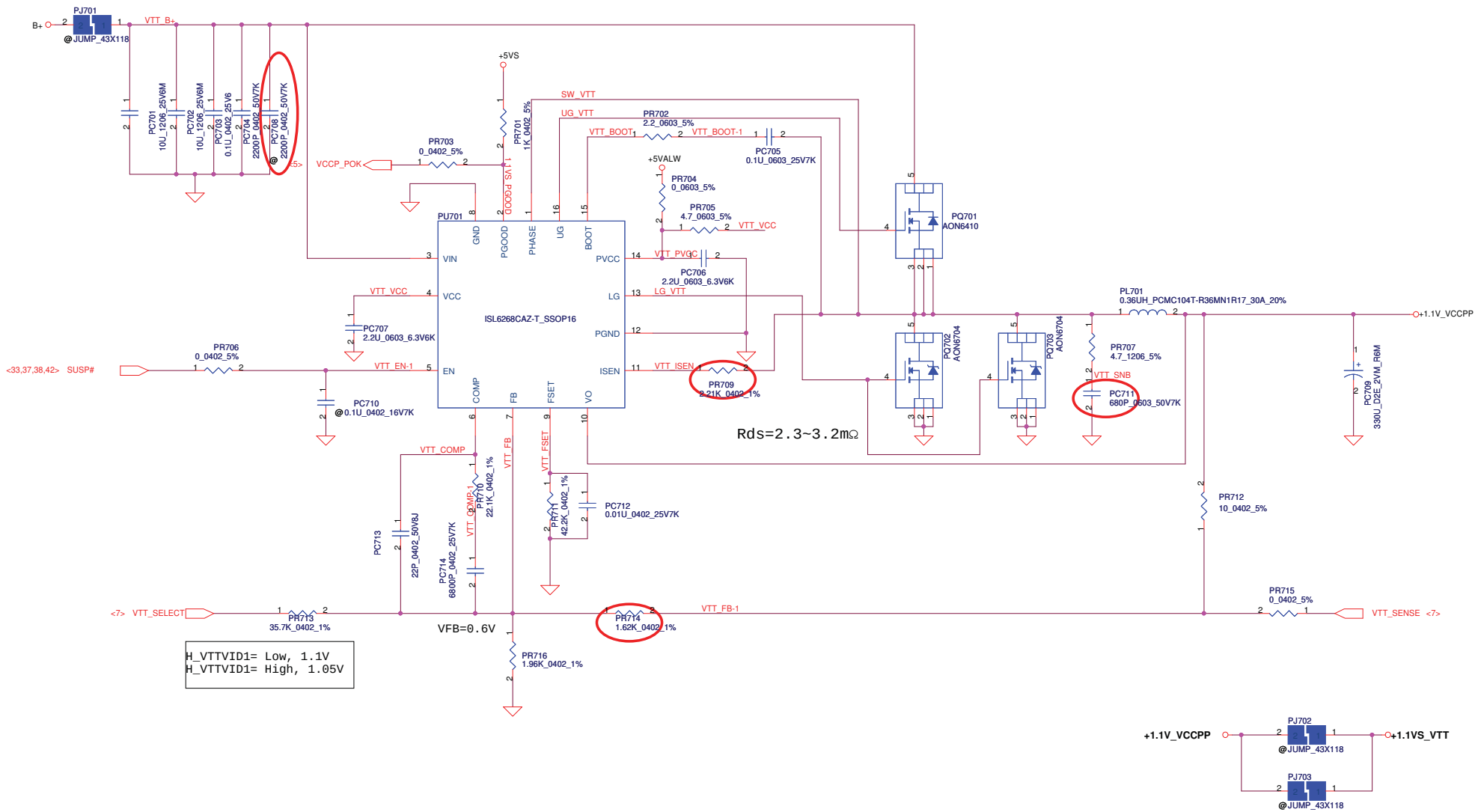

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Compal Electronics, Inc.

Title: +1.1VS_VTT

Size: Custom | Document Number | Rev: 0.1

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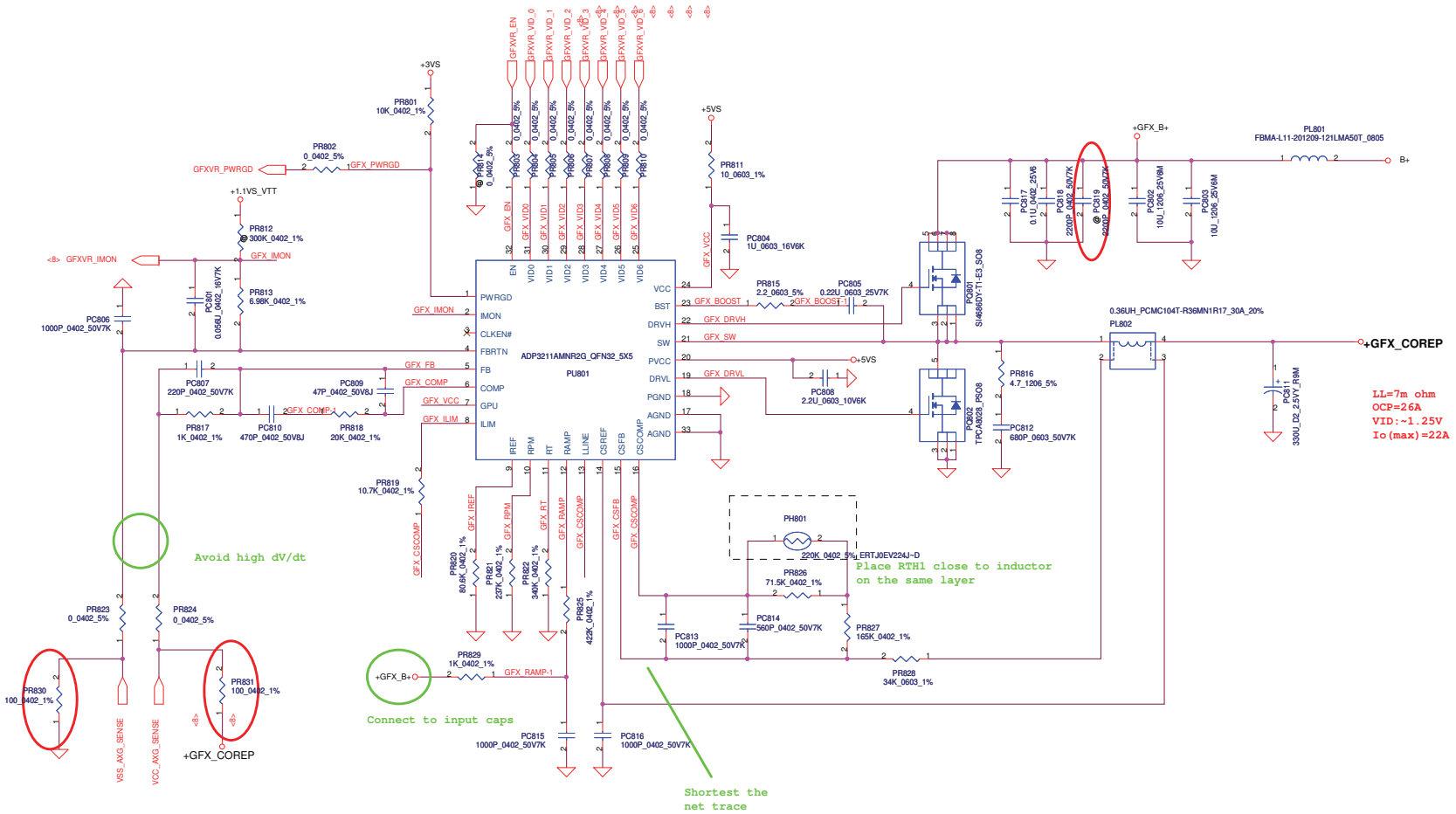
change name



(15A,600mils ,Via NO.= 30)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: GFX_CORE

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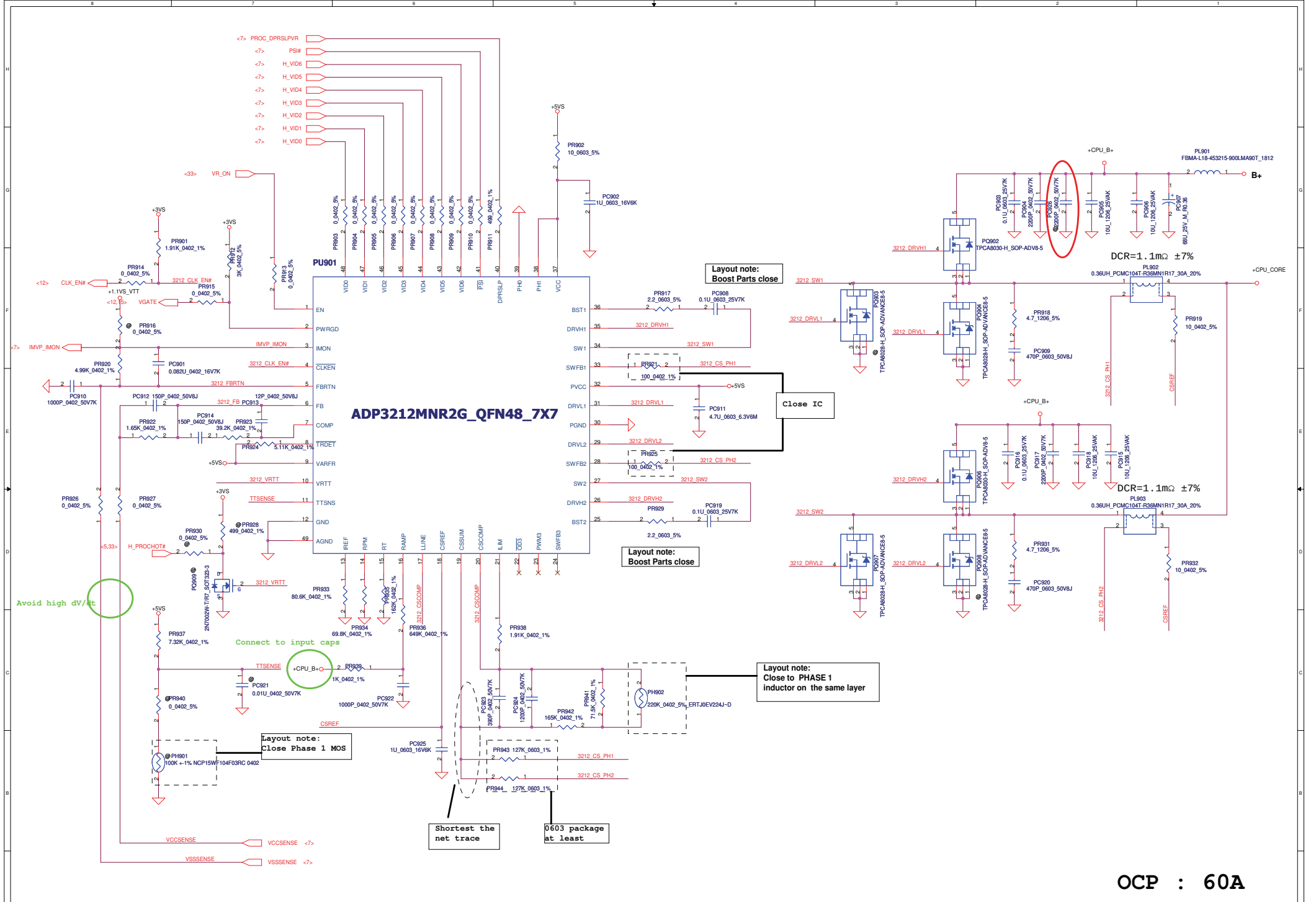

OCP : 60A

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Compal Electronics, Inc.

Title: CPU_CORE

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For ESD	P41	Add PD202	2009.11.5	EVT
2	For HW request remove +1.05V's JUMP	P41	Remove +1.05V's JUMP	2009.11.6	EVT
3	Because limited high is not enough.	P47	Change PC907 from 220uF to 68uF	2009.11.6	EVT
4	Add PR830,PR831 for GFX_CORE sence.	P46	Add PR830,PR831 for GFX_CORE sence.	2009.11.17	EVT
5	Change Battery connent footprint.	P41	Change Battery connent footprint.	2009.11.17	EVT
6	Change PR521 from 0ohm to 150Kohm. Add PC528 on BOM.	P44	HW request	2009.11.25	EVT
7	Add PD501.	P44	HW request	2009.12.16	DVT
8	Reserve Cap. on B+ for RF.		RF request	2010.1.15	PVT
9	Change PR204 from 21.5Kohm to 20Kohm. Change PR206 from 9.76Kohm to 8.87Kohm.	P41	Thermal team request to change OTP temp. change from 92 degree to 95 degree.	2010.1.22	PVT
10					
11					
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17				20081022	

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Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2009/01/06

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 0.1

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