

LCFC Confidential

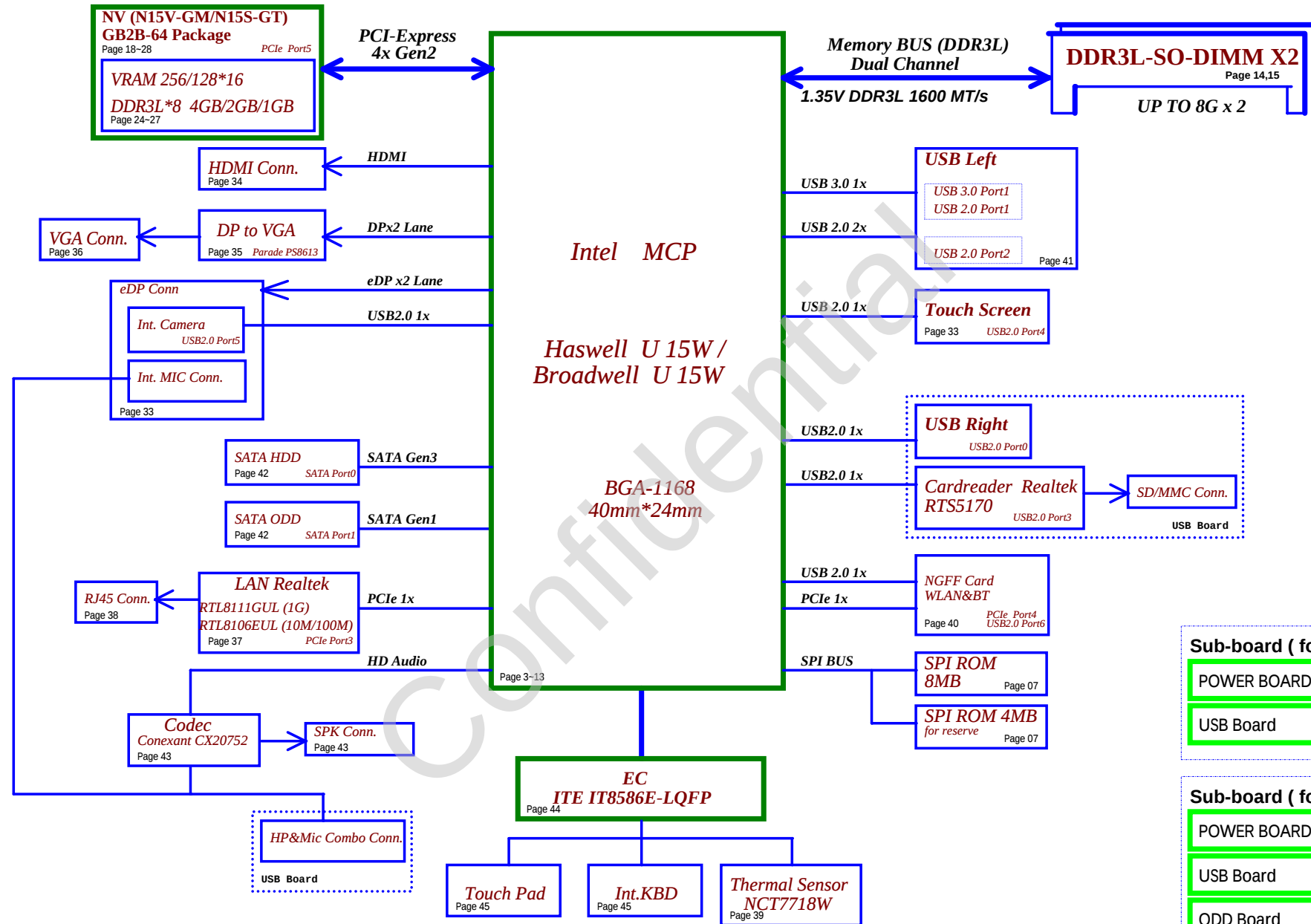
ACLUA M/B Schematics Document

Intel Haswell/Broadwell U-Processor with DDRIII L + NV (N15V-GM/N15S-GT) GPU

2013-12-26

REV: 0.3

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page	
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Title			
Block Diagram			
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Voltage Rails (O --> Means ON , X --> Means OFF)

<i>Power Plane</i>	<i>B+</i>	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
<i>State</i>					
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VAL#	+V	+VS	CLOCK
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

[illegible]

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

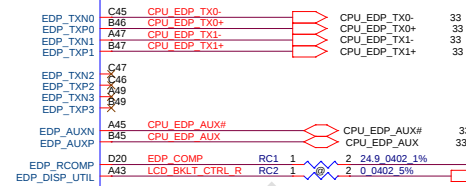
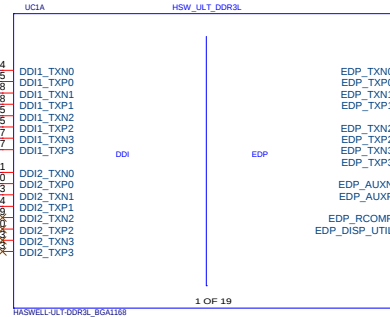
EC SM Bus1 address		EC SM Bus2 address	
Device		Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb
Charger	0001 0010 b	VGA	0x41(default)
		PCH	need to update

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

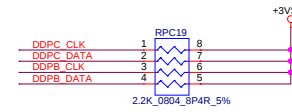
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Notes List			
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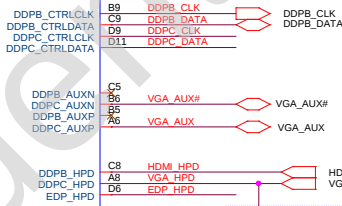
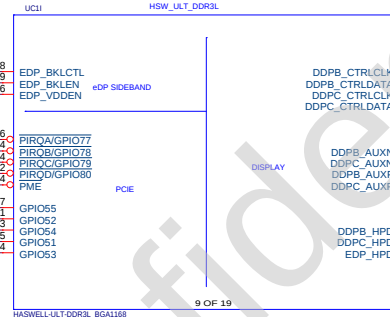
HDMI D2
HDMI D1
HDMI D0
HDMI CLK
DP TO VGA Converter



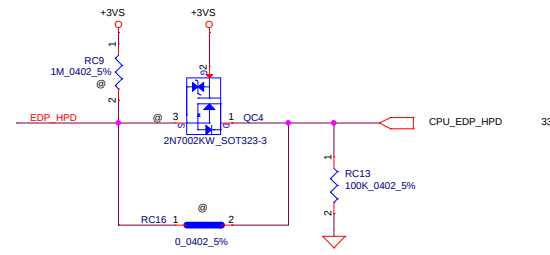
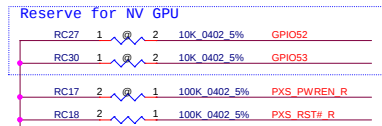
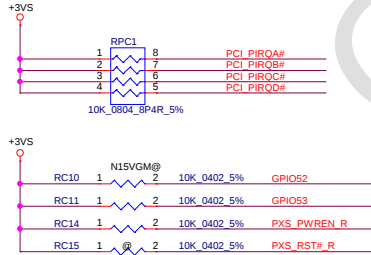
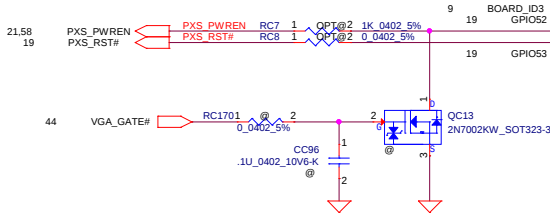
+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil



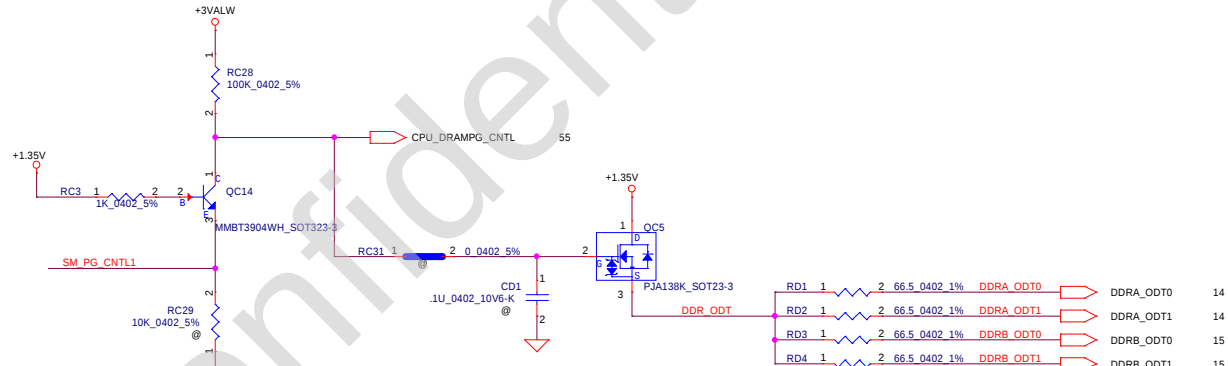
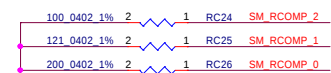
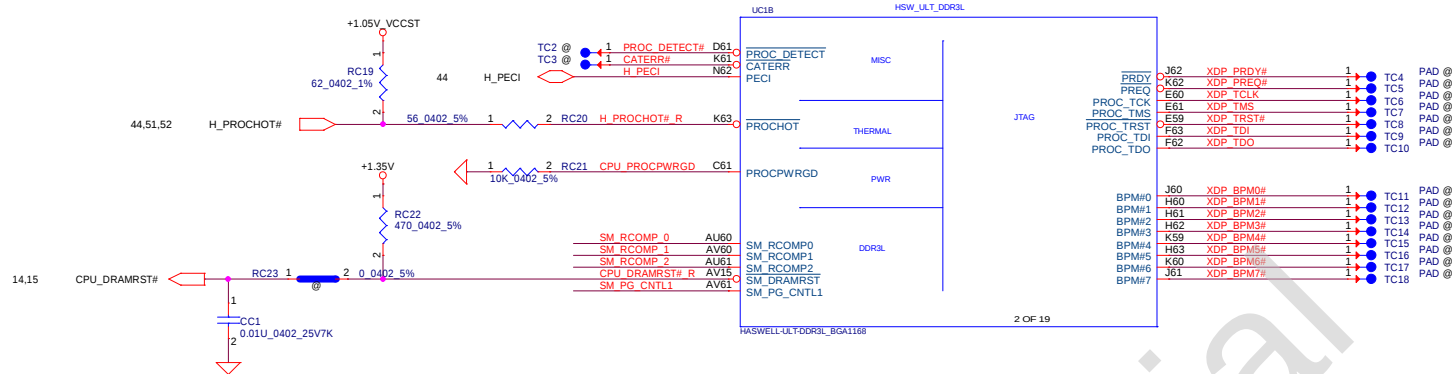
DDPx_CTRLDATA
The signal has a weak internal pull-down.
H Port is detected.
L Port is not detected.



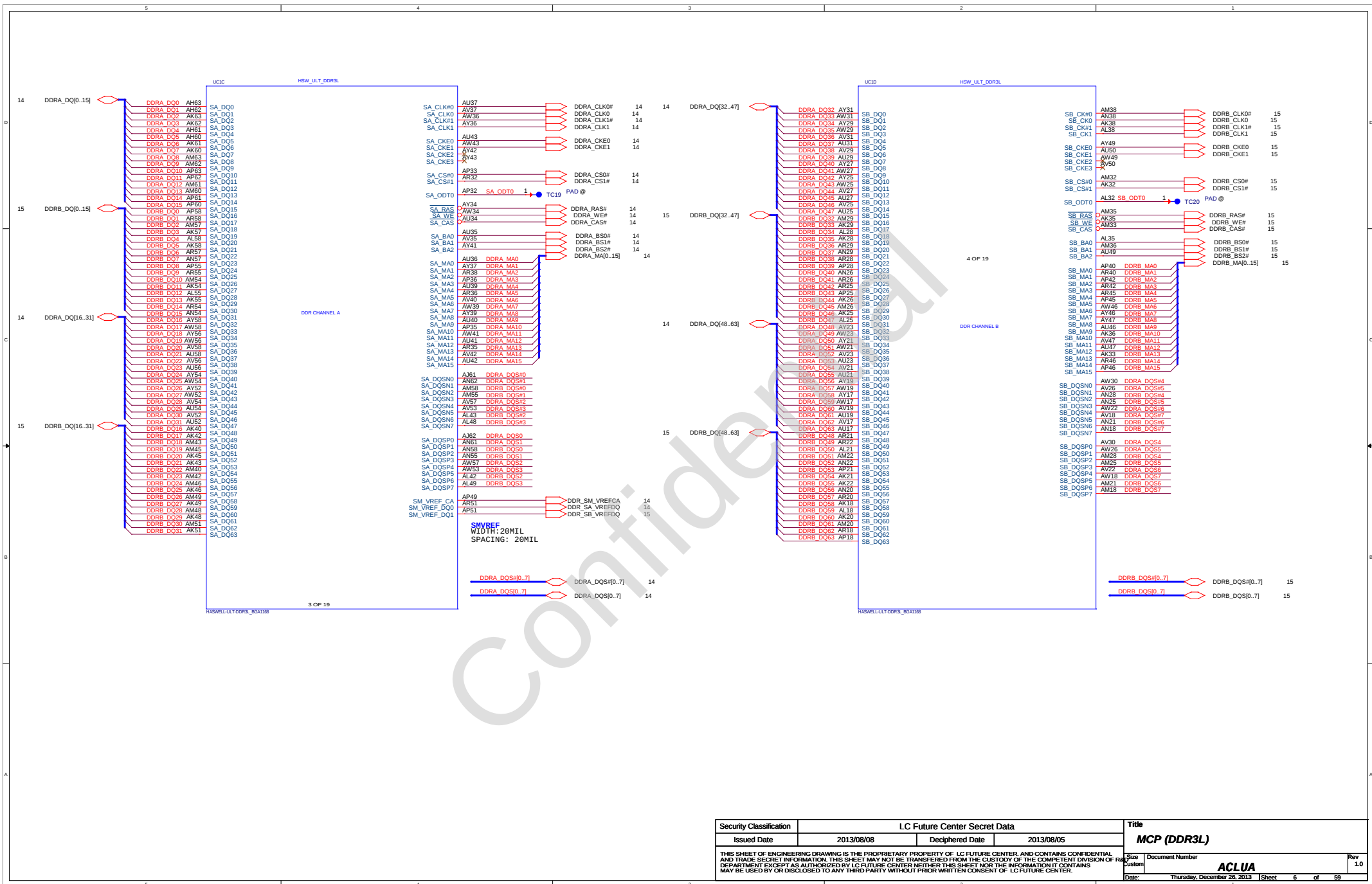
After confirm with vendor, HPD has internal pull-down ~100K at PS8613, just reserve in case. RC37 can be removed next phase if no issue.

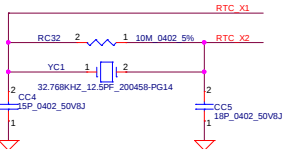


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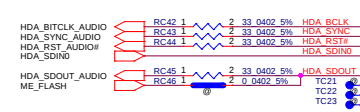
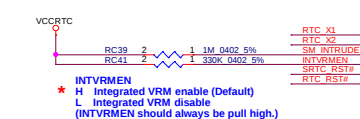
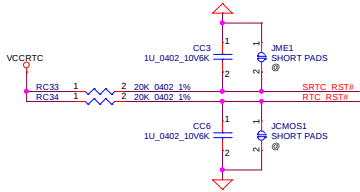


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				Rev	1.0

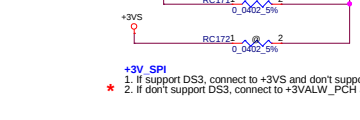
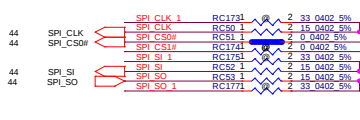
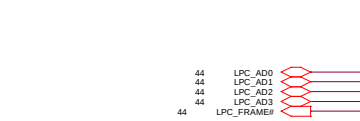




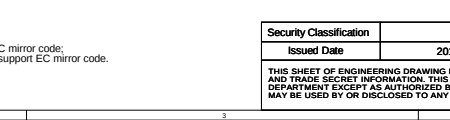
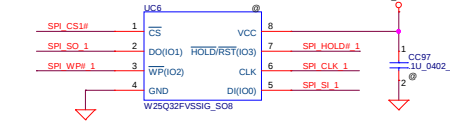
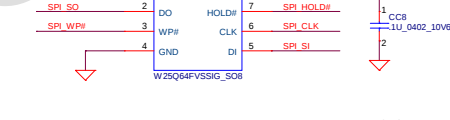
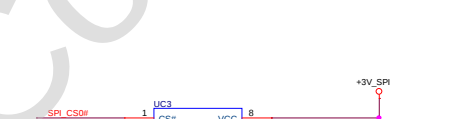
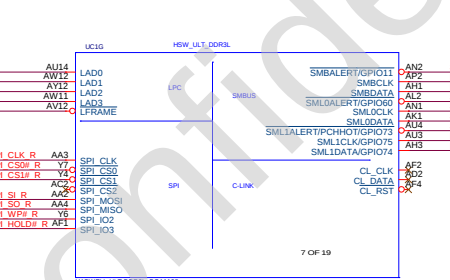
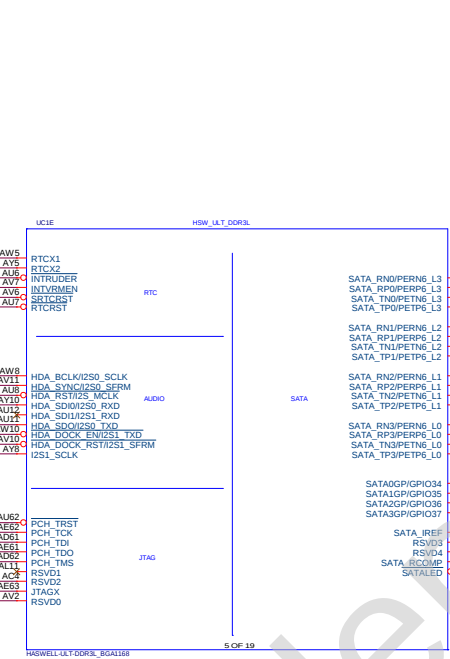
CRYSTAL
1. Space 15MIL
2. No trace under crystal
3. Place on opposite side of MCP for temp influence



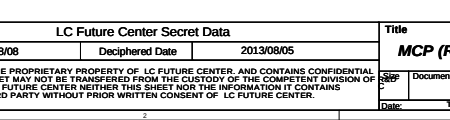
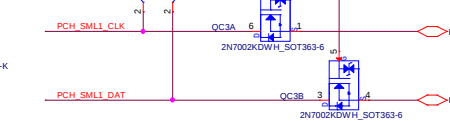
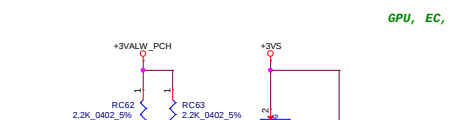
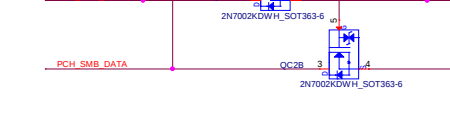
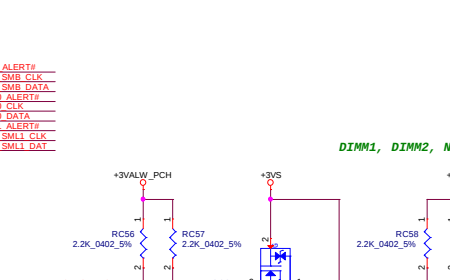
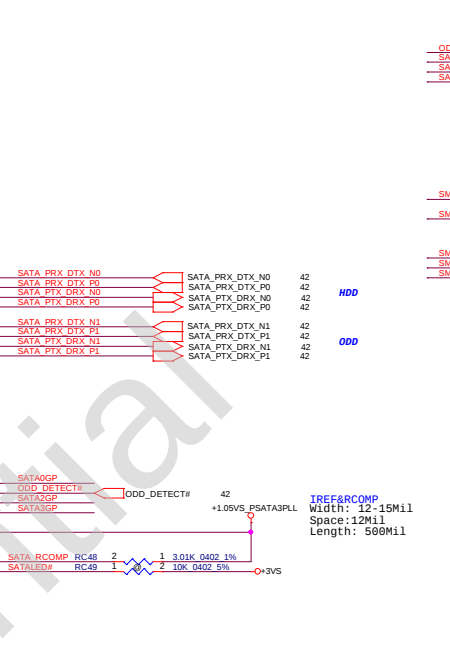
H Integrated VRM enable (Default)
L Integrated VRM disable
(INTVRMEN should always be pull high.)



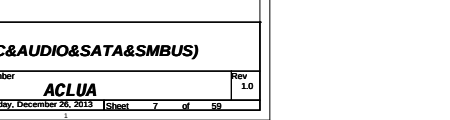
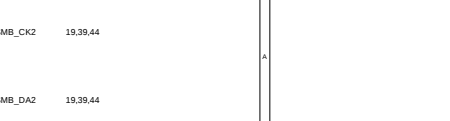
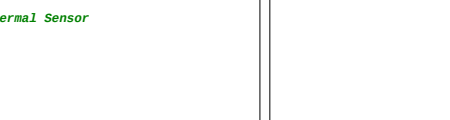
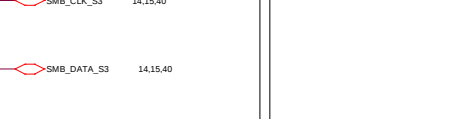
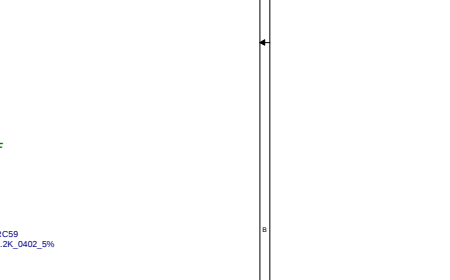
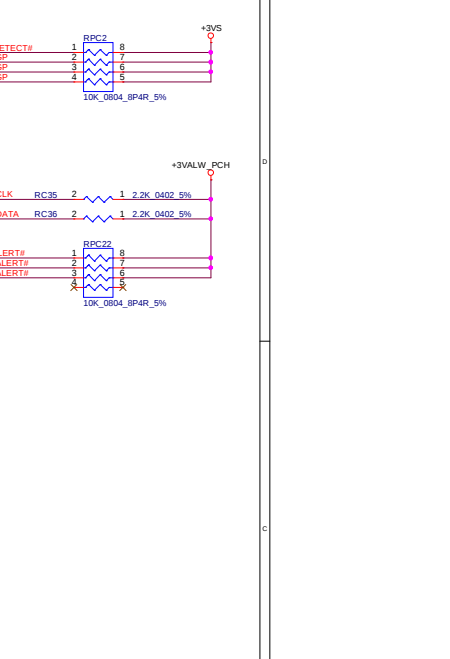
+3V SPI
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.



+3V SPI
1. If support DS3, connect to +3VS and don't support EC mirror code;
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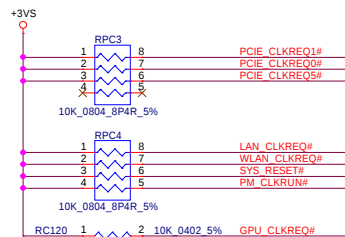


+3V SPI
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

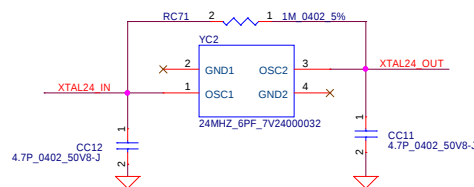
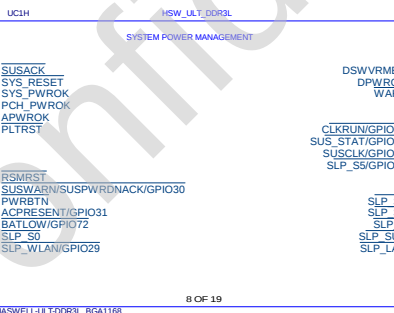
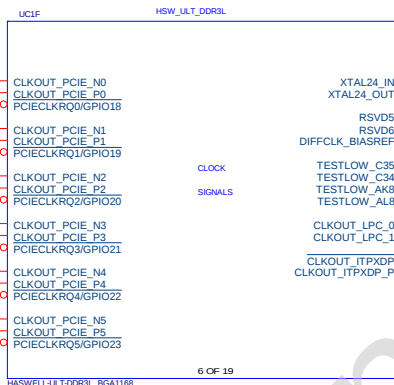
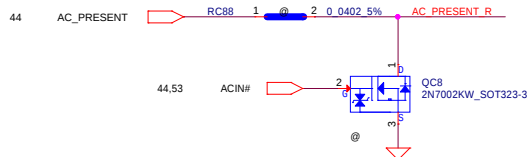
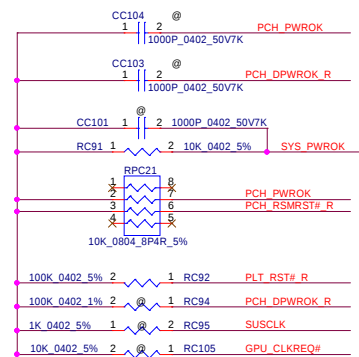
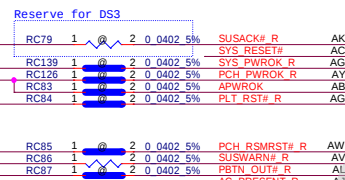
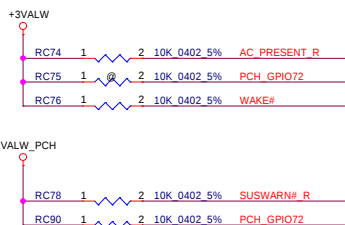


+3V SPI
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

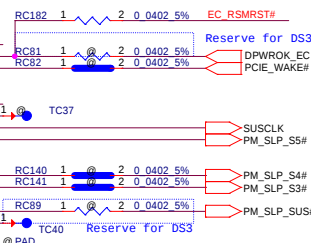
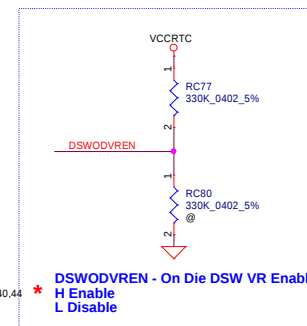
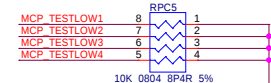
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PCIE CLK2 LAN
PCIE CLK3 WLAN
PCIE CLK4 GPU



DIFFCLK_BIASREF
 Width: 12-15mil
 Space: 12mil
 Length: 500mil

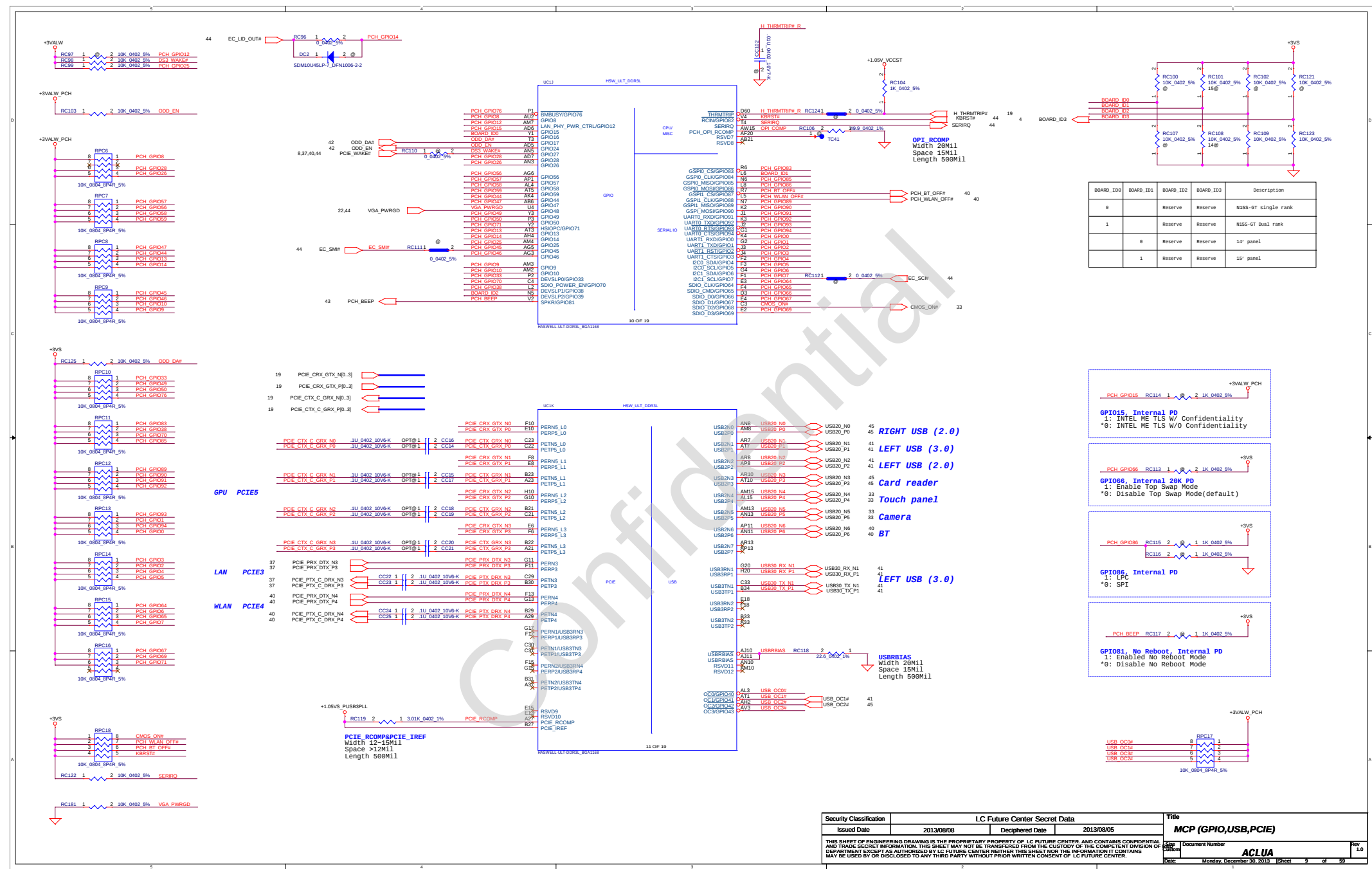


Reserve for DS3

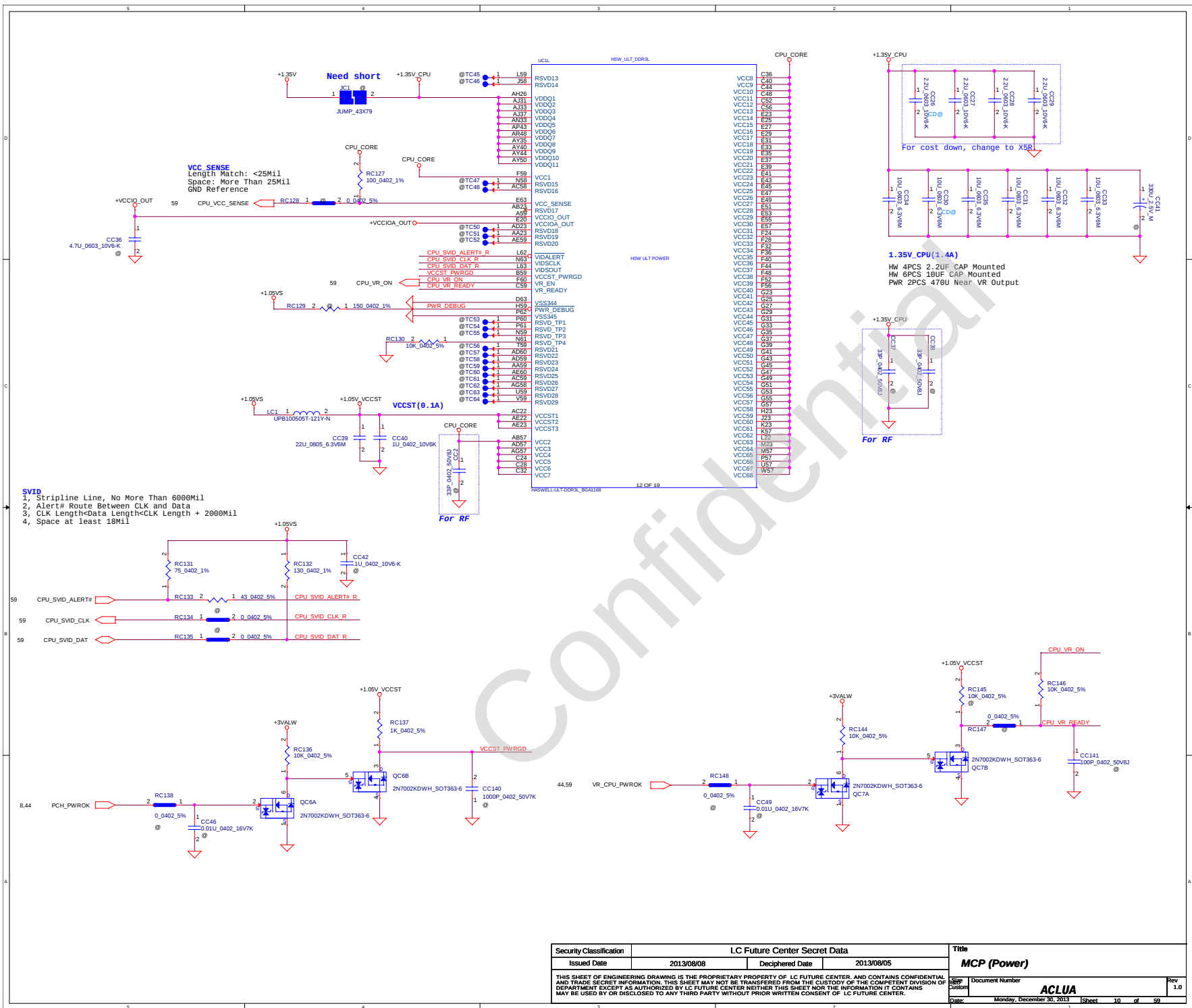
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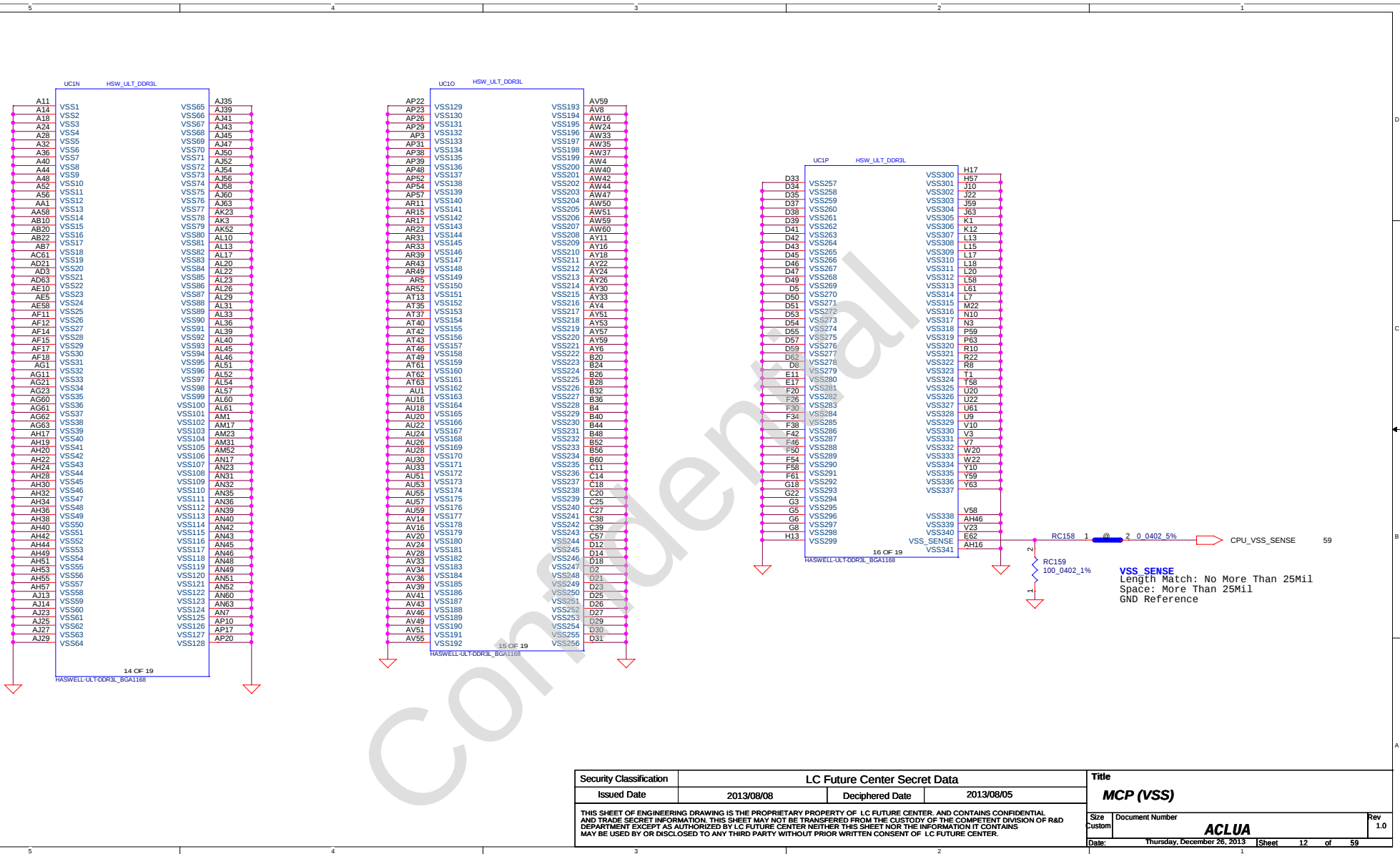
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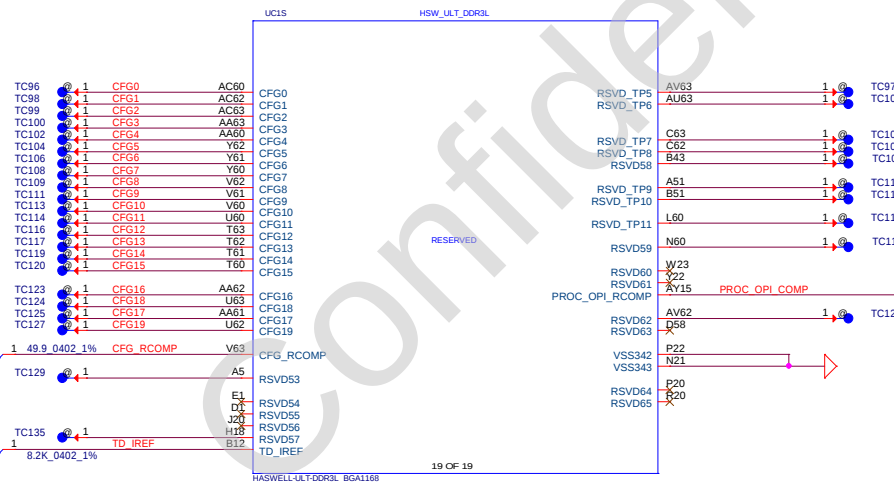
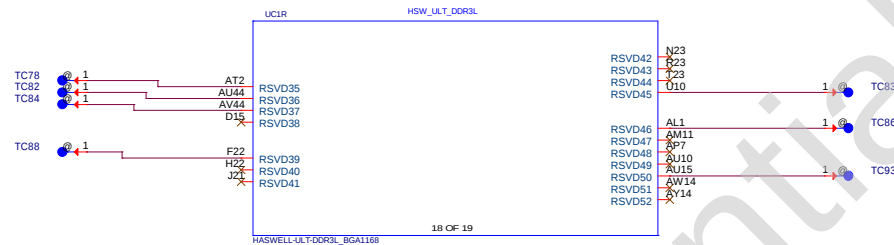
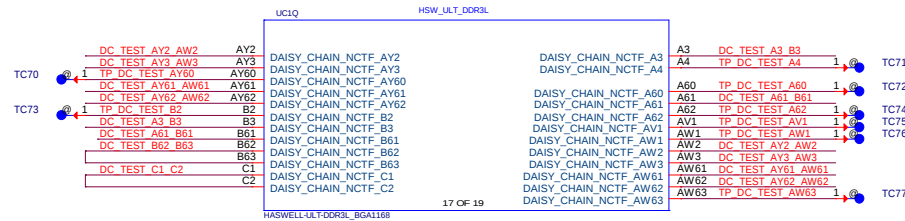
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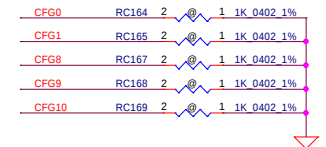




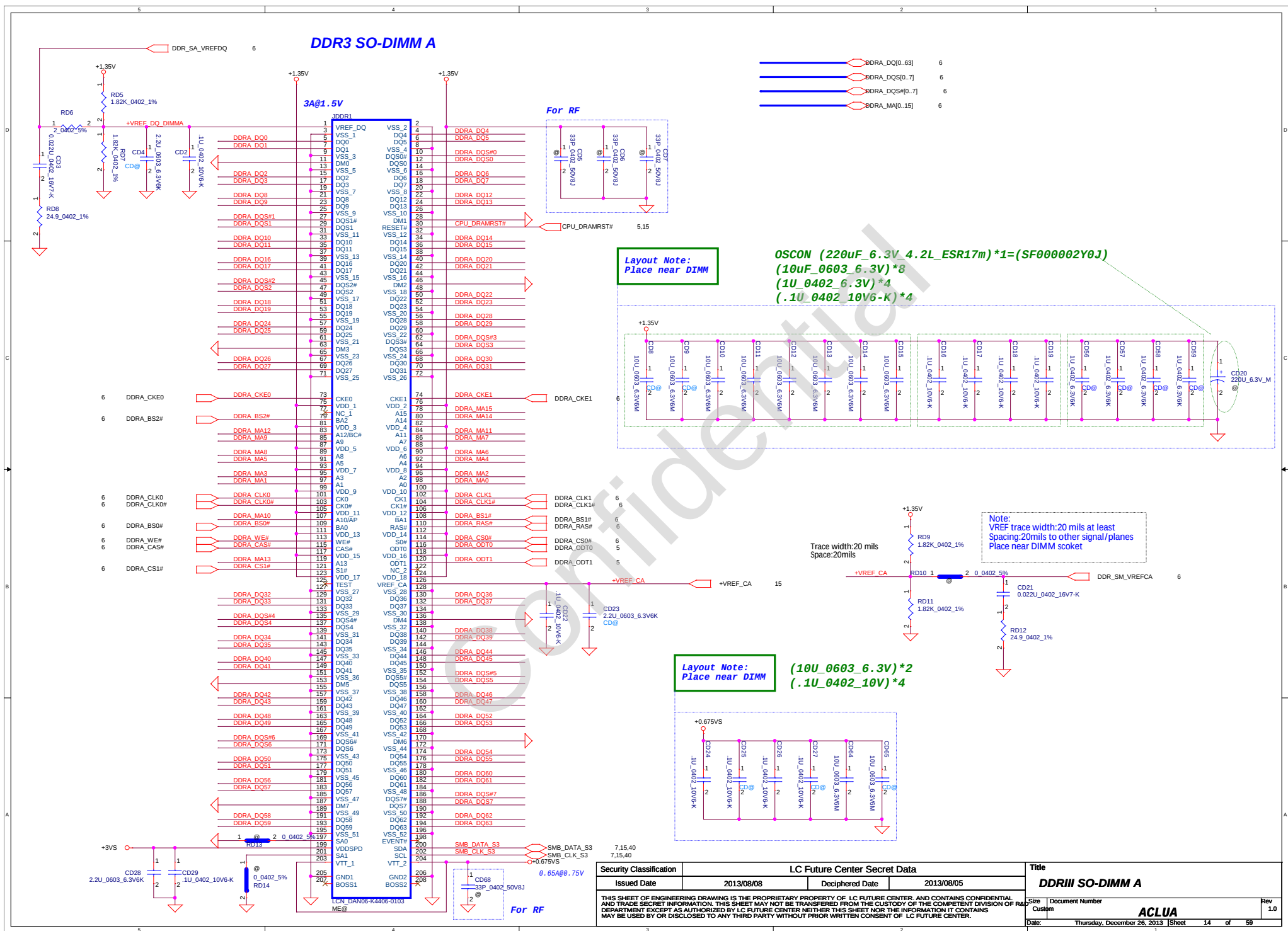
CFG_RCOMP&TD_IREF
Width 20Mil
Space 15Mil
Length 500Mil

CFG3
0: Disable
1: Enable, Set DFX Enabled BIT
In Debug Interface MSR

CFG4
*L: eDP enable
H: eDP disable



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DDR3 SO-DIMM B

3A@1.5V

For RF

Layout Note:
Place near DIMM

(10uF 0603 6.3V)*8
(1U 0402 6.3V)*8
(.1U 0402 10V6-K)*4

Layout Note:
Place near DIMM

(10U 0603 6.3V)*2
(.1U 0402 10V)*4

Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR_B_DQ17
7	DQ1	DDR_B_DQ23
15	DQ2	DDR_B_DQ18
17	DQ3	DDR_B_DQ21
4	DQ4	DDR_B_DQ16
6	DQ5	DDR_B_DQ22
16	DQ6	DDR_B_DQ19
18	DQ7	DDR_B_DQ20
10	DQS#0	DDR_B_DQS#2
12	DQ8	DDR_B_DQS2
21	DQ8	DDR_B_DQ3
23	DQ9	DDR_B_DQ5
33	DQ10	DDR_B_DQ6
35	DQ11	DDR_B_DQ1
22	DQ12	DDR_B_DQ2
24	DQ13	DDR_B_DQ4
36	DQ14	DDR_B_DQ9
27	DQS#1	DDR_B_DQS#0
29	DQS1	DDR_B_DQS0
39	DQ16	DDR_B_DQ8
41	DDR_B_DQ10	
51	DDR_B_DQ18	
53	DQ19	DDR_B_DQ15
40	DQ20	DDR_B_DQ13
42	DQ21	DDR_B_DQ12
50	DQ22	DDR_B_DQ9
52	DQ23	DDR_B_DQ11
45	DQS#2	DDR_B_DQS#1
47	DQS2	DDR_B_DQS1
57	DQ24	DDR_B_DQ27
59	DQ25	DDR_B_DQ26
67	DQ26	DDR_B_DQ28
69	DQ27	DDR_B_DQ24
68	DQ28	DDR_B_DQ31
58	DQ29	DDR_B_DQ30
70	DQ30	DDR_B_DQ29
62	DQ31	DDR_B_DQ25
64	DQS#3	DDR_B_DQS#3
129	DQ32	DDR_B_DQ33
131	DQ33	DDR_B_DQ36
141	DQ34	DDR_B_DQ39
143	DQ35	DDR_B_DQ38
130	DQ36	DDR_B_DQ37
132	DQ37	DDR_B_DQ32
140	DQ38	DDR_B_DQ35
142	DQ39	DDR_B_DQ34
135	DQS#4	DDR_B_DQS#4
137	DQS4	DDR_B_DQS4
147	DQ40	DDR_B_DQ40
149	DQ41	DDR_B_DQ43
157	DQ42	DDR_B_DQ42
159	DQ43	DDR_B_DQ44
146	DQ44	DDR_B_DQ45
148	DQ45	DDR_B_DQ41
158	DQ46	DDR_B_DQ46
160	DQ47	DDR_B_DQ47
152	DQS#5	DDR_B_DQS#5
154	DQS5	DDR_B_DQS5
163	DQ48	DDR_B_DQ52
165	DQ49	DDR_B_DQ51
175	DQ50	DDR_B_DQ50
177	DQ51	DDR_B_DQ48
164	DQ52	DDR_B_DQ49
166	DQ53	DDR_B_DQ53
174	DQ54	DDR_B_DQ54
176	DQ55	DDR_B_DQ55
169	DQS#6	DDR_B_DQS#6
171	DQS6	DDR_B_DQS6
181	DQ56	DDR_B_DQ62
183	DQ57	DDR_B_DQ57
191	DQ58	DDR_B_DQ59
193	DQ59	DDR_B_DQ63
180	DQ60	DDR_B_DQ56
182	DQ61	DDR_B_DQ61
192	DQ62	DDR_B_DQ58
194	DQ63	DDR_B_DQ60
186	DQS#7	DDR_B_DQS#7
188	DQS7	DDR_B_DQS7

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4

3

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A

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2013/08/05

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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1.5) (W)	NVCLK /MCLK (MHz)	NVVDD (V) (A) (W)			FBVDD (1.35V) (A) (W)		FBVDDQ (GPU+Mem) (1.35V) (A) (W)		PCI Express (1.05V) (6) (mA) (W)		I/O and PLLVDD (1.05V) (mA) (W)		Other (3.3V) (mA) (W)	
N14X 120bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

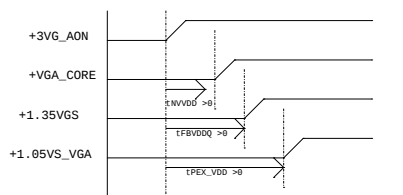
N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

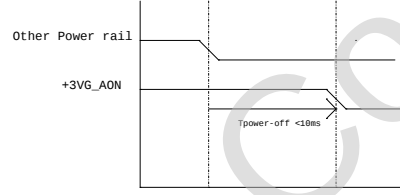
SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence

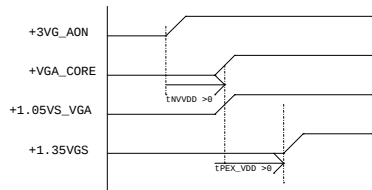


1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence

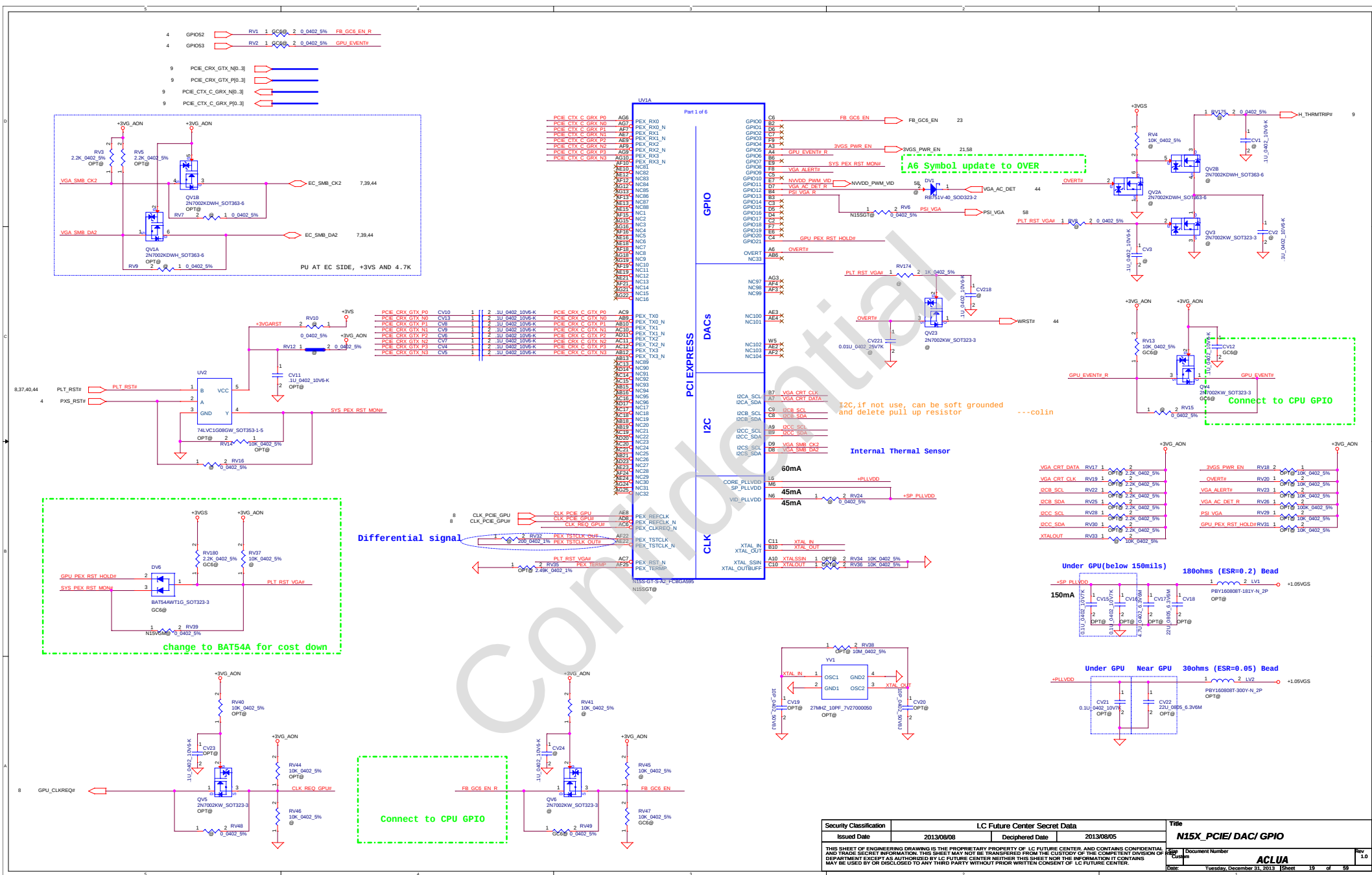


1. all power rail ramp up time should be larger than 40us

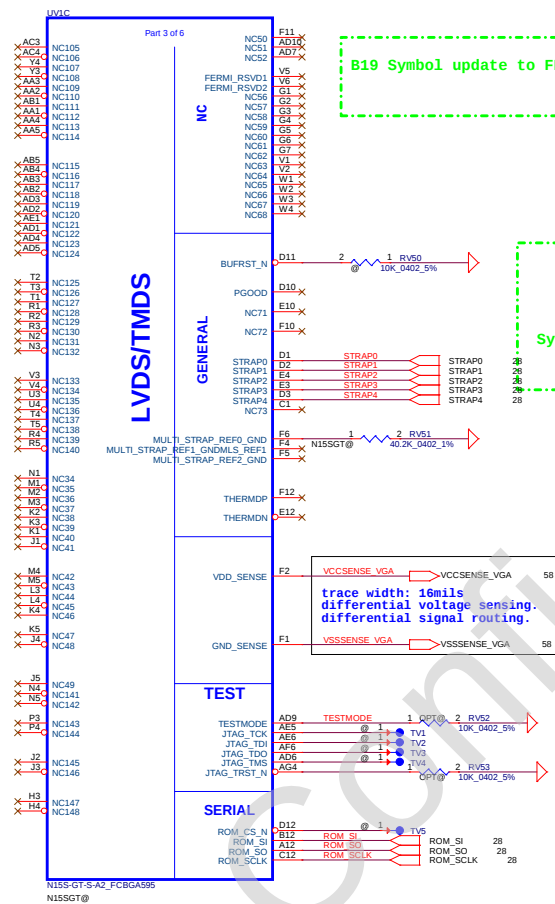
N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

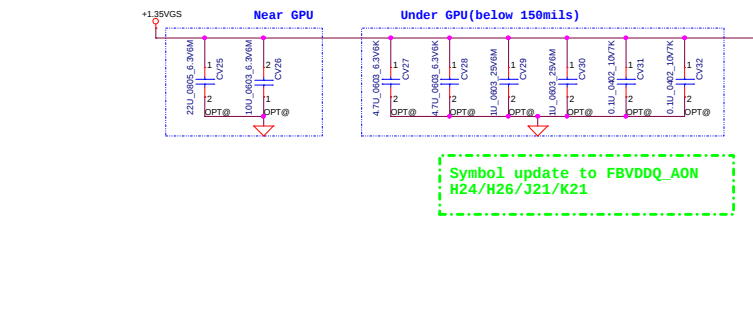
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	VGA Notes List
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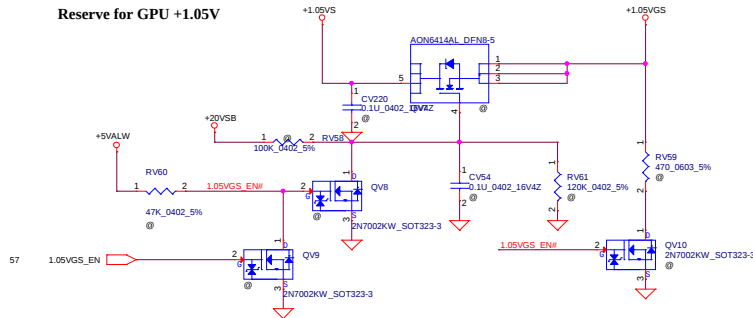
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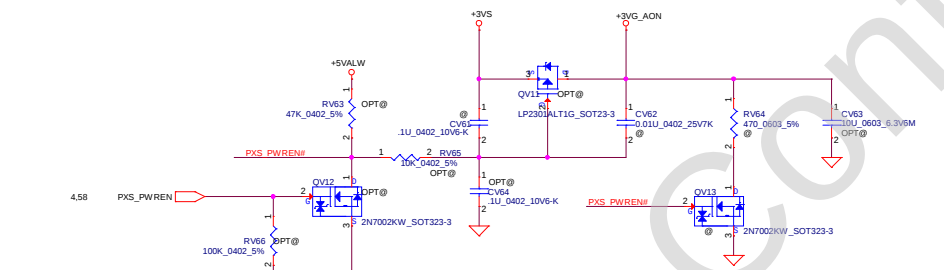
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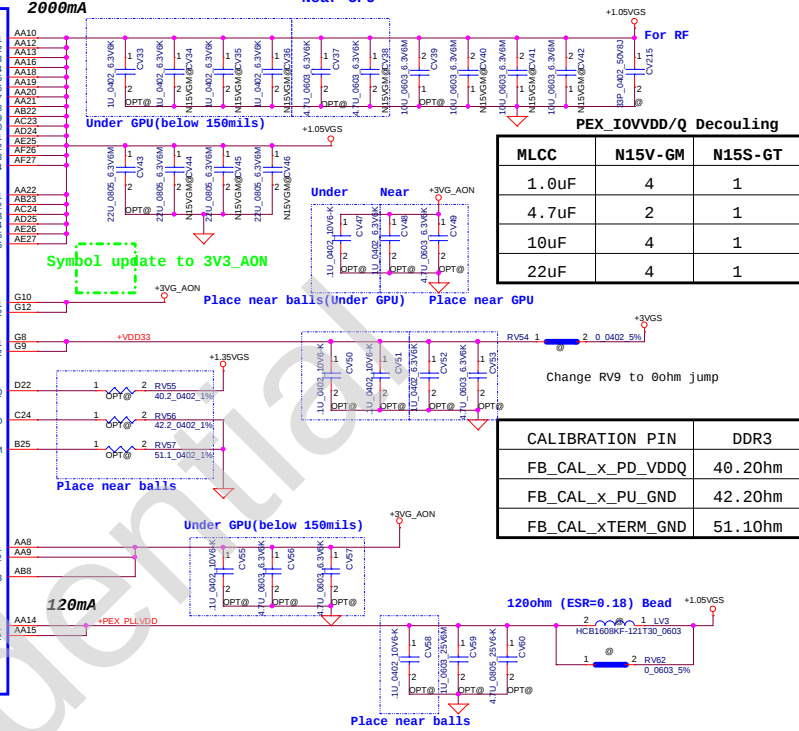
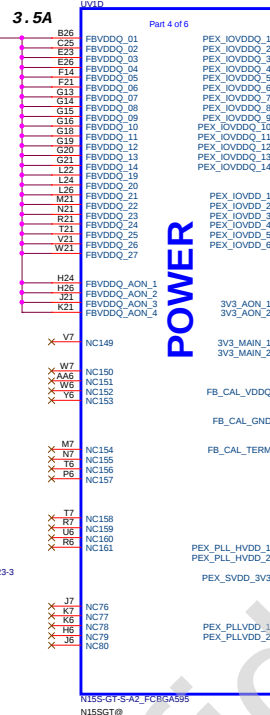
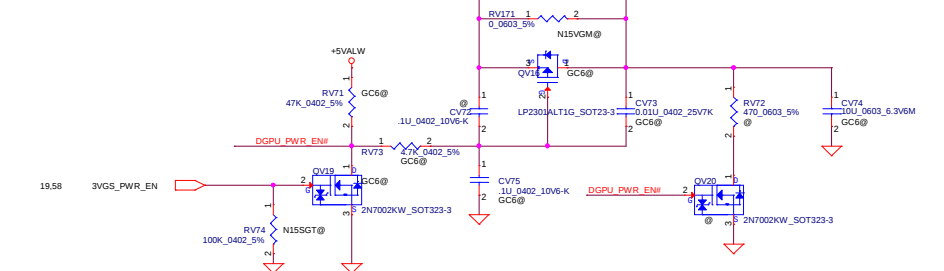
Reserve for GPU +1.05V



+3.3VS TO +3VG_AON



+3.3VS TO +3VGS

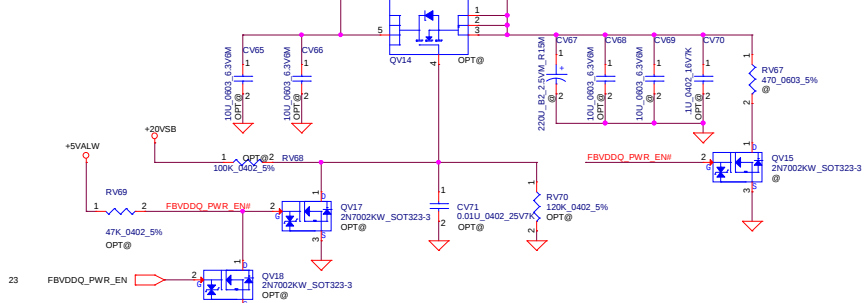


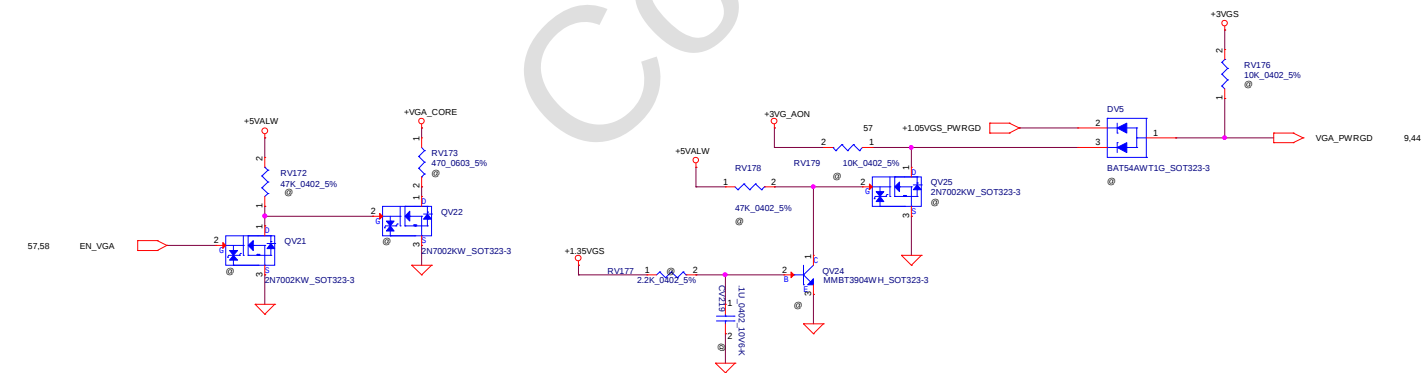
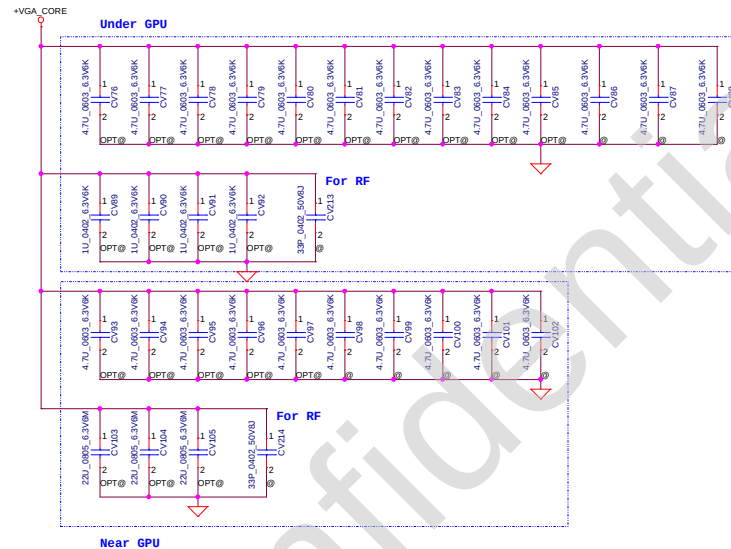
PEX_IOVDD/Q Decoupling

MLCC	N15V-GM	N15S-GT
1.0uF	4	1
4.7uF	2	1
10uF	4	1
22uF	4	1

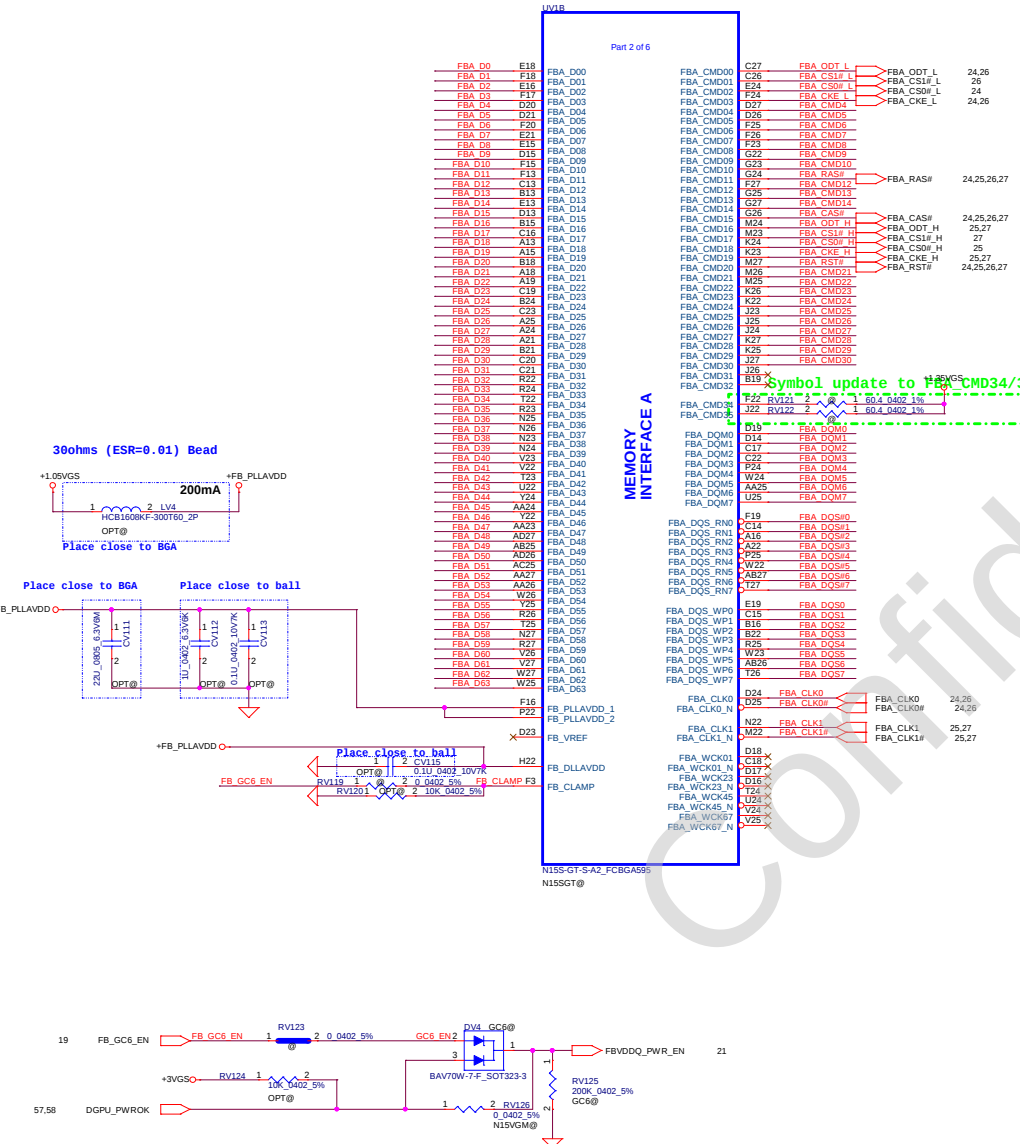
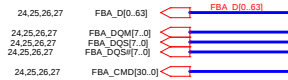
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	42.20hm
FB_CAL_xTERM_GND	51.10hm

+1.35V TO +1.35VGS





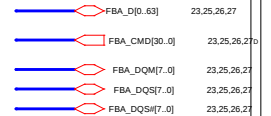
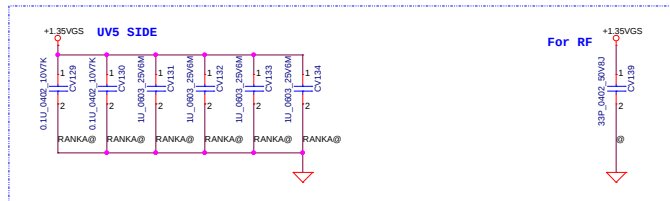
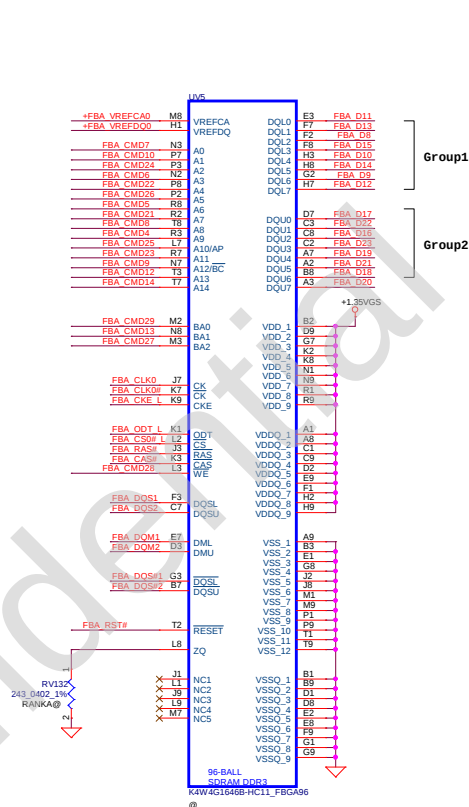
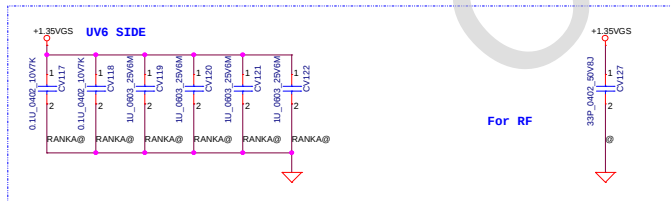
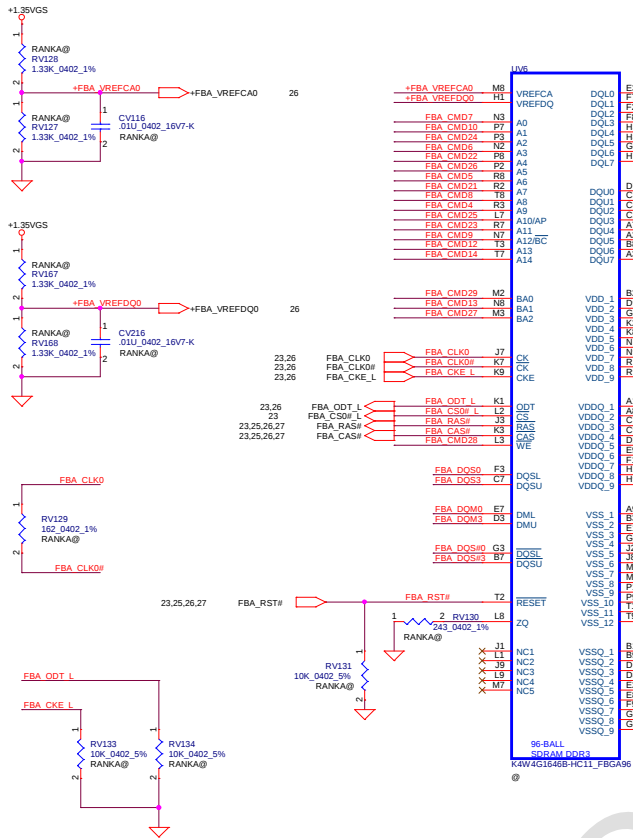
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CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FbX_CMD0	ODT_L		ODT_L	
FbX_CMD1			CS1#_L	
FbX_CMD2	CS0#_L			
FbX_CMD3	CKE_L		CKE_L	
FbX_CMD4	A9	A9	A11	A11
FbX_CMD5	A6	A6	A7	A7
FbX_CMD6	A3	A3	BA1	BA1
FbX_CMD7	A0	A0	A12	A12
FbX_CMD8	A8	A8	A8	A8
FbX_CMD9	A12	A12	A0	A0
FbX_CMD10	A1	A1	A2	A2
FbX_CMD11	RAS#	RAS#	RAS#	RAS#
FbX_CMD12	A13	A13	A14	A14
FbX_CMD13	BA1	BA1	A3	A3
FbX_CMD14	A14	A14	A13	A13
FbX_CMD15	CAS#	CAS#	CAS#	CAS#
FbX_CMD16		ODT_H		ODT_H
FbX_CMD17				CS1#_H
FbX_CMD18				
FbX_CMD19		CKE_H		CKE_H
FbX_CMD20	RST	RST	RST	RST
FbX_CMD21	A7	A7	A6	A6
FbX_CMD22	A4	A4	A5	A5
FbX_CMD23	A11	A11	A9	A9
FbX_CMD24	A2	A2	A1	A1
FbX_CMD25	A10	A10	WE#	WE#
FbX_CMD26	A5	A5	A4	A4
FbX_CMD27	BA2	BA2		
FbX_CMD28	WE#	WE#	A10	A10
FbX_CMD29	BA0	BA0	BA0	BA0
FbX_CMD30			BA2	BA2

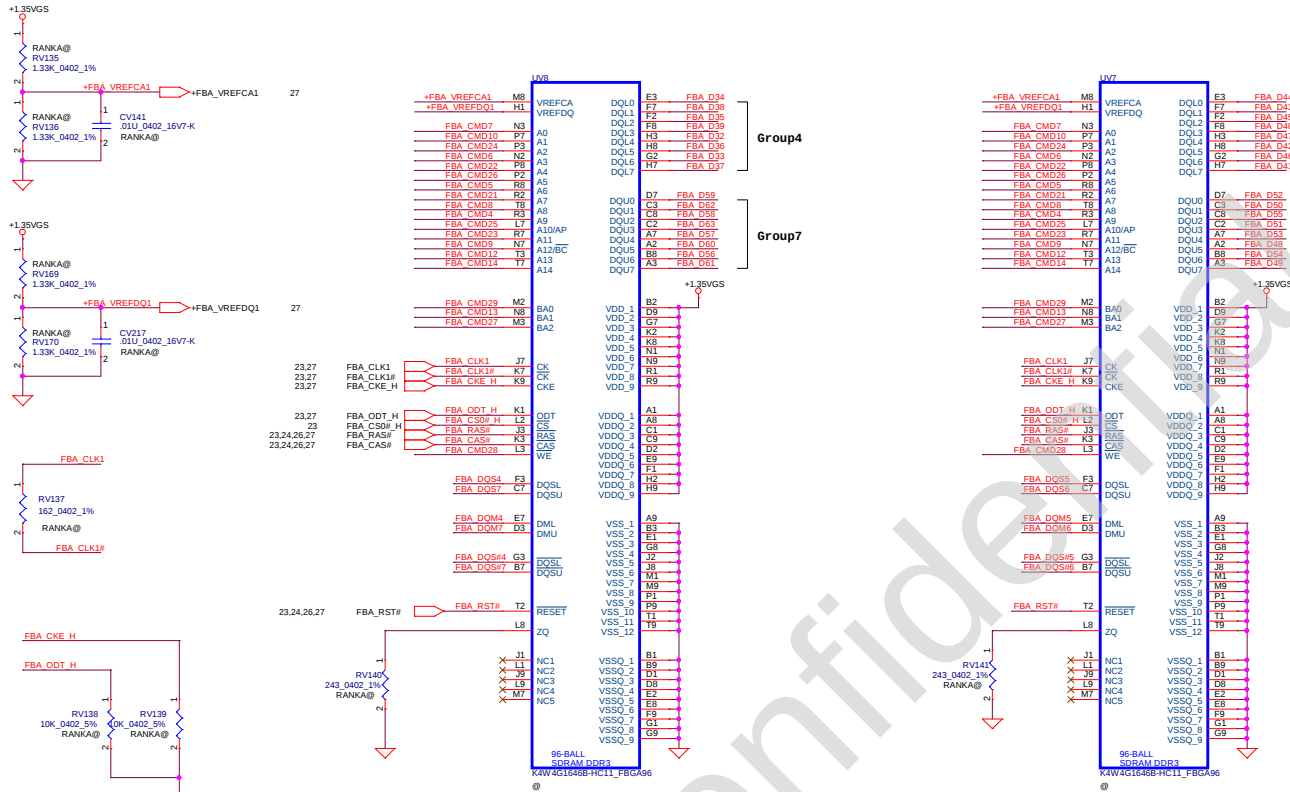
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode E

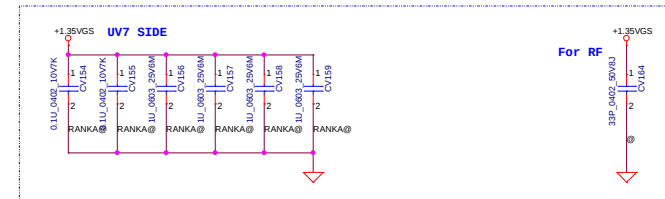
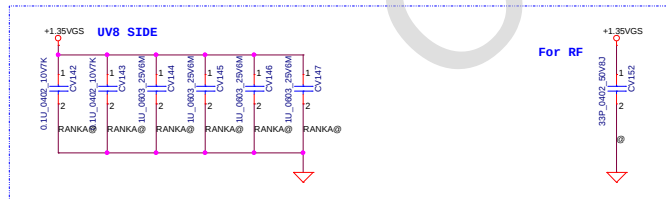
Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBX_CMD0	ODT_L		ODT_L	
FBX_CMD1			CS1#_L	
FBX_CMD2	CS0#_L			
FBX_CMD3	CKE_L		CKE_L	
FBX_CMD4	A9	A9	A11	A11
FBX_CMD5	A6	A6	A7	A7
FBX_CMD6	A3	A3	BA1	BA1
FBX_CMD7	A0	A0	A12	A12
FBX_CMD8	A8	A8	A8	A8
FBX_CMD9	A12	A12	A0	A0
FBX_CMD10	A1	A1	A2	A2
FBX_CMD11	RAS#	RAS#	RAS#	RAS#
FBX_CMD12	A13	A13	A14	A14
FBX_CMD13	BA1	BA1	A3	A3
FBX_CMD14	A14	A14	A13	A13
FBX_CMD15	CAS#	CAS#	CAS#	CAS#
FBX_CMD16		ODT_H		ODT_H
FBX_CMD17			CS1#_H	
FBX_CMD18		CS0#_H		
FBX_CMD19		CKE_H		CKE_H
FBX_CMD20	RST	RST	RST	RST
FBX_CMD21	A7	A7	A6	A6
FBX_CMD22	A4	A4	A5	A5
FBX_CMD23	A11	A11	A9	A9
FBX_CMD24	A2	A2	A1	A1
FBX_CMD25	A10	A10	WE#	WE#
FBX_CMD26	A5	A5	A4	A4
FBX_CMD27	BA2	BA2		
FBX_CMD28	WE#	WE#	A10	A10
FBX_CMD29	BA0	BA0	BA0	BA0
FBX_CMD30			BA2	BA2

at least 16 mils width(optimal)
20 mils spacing to other signals/planes

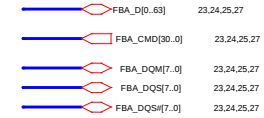
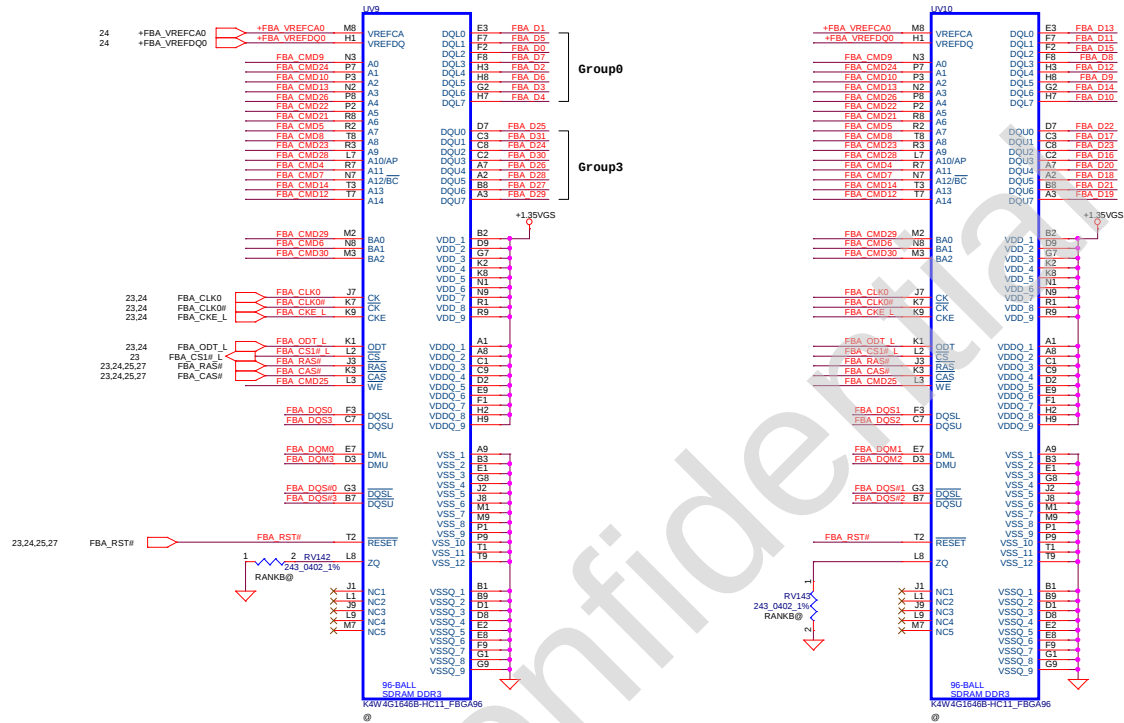


CMD mapping mod Mode E

Address	Rank0	Rank1
FbX_CMD0	0..31	0..31
FbX_CMD1	32..63	0..31
FbX_CMD2	ODT_L	ODT_L
FbX_CMD3	CS0#_L	CS1#_L
FbX_CMD4	CKE_L	CKE_L
FbX_CMD5	A9	A11
FbX_CMD6	A6	A7
FbX_CMD7	A3	BA1
FbX_CMD8	A0	A12
FbX_CMD9	A8	A8
FbX_CMD10	A12	A0
FbX_CMD11	A1	A2
FbX_CMD12	RAS#	RAS#
FbX_CMD13	A13	A14
FbX_CMD14	BA1	A3
FbX_CMD15	A14	A13
FbX_CMD16	CAS#	CAS#
FbX_CMD17	ODT_H	ODT_H
FbX_CMD18	CS0#_H	CS1#_H
FbX_CMD19	CKE_H	CKE_H
FbX_CMD20	RST	RST
FbX_CMD21	A7	A6
FbX_CMD22	A4	A5
FbX_CMD23	A11	A9
FbX_CMD24	A2	A1
FbX_CMD25	A10	WE#
FbX_CMD26	A5	A4
FbX_CMD27	BA2	BA2
FbX_CMD28	WE#	A10
FbX_CMD29	BA0	BA0
FbX_CMD30		BA2



at least 16 mils width(optimal)
20 mils spacing to other signals /planes

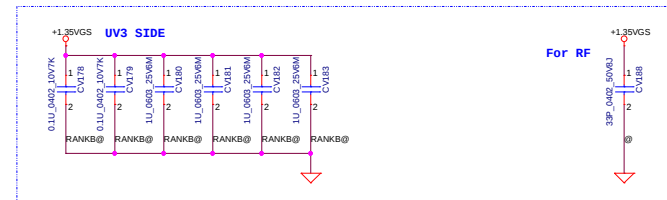
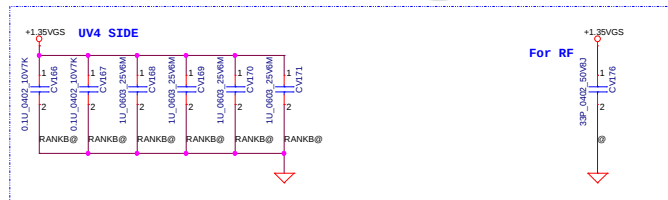


Group1

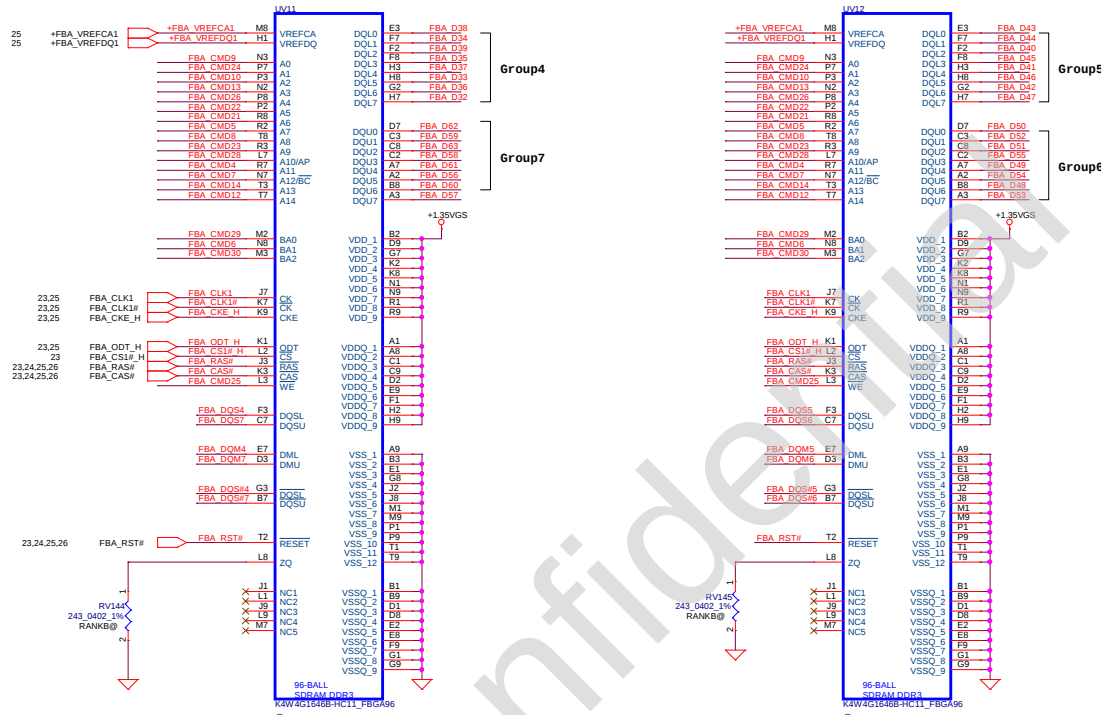
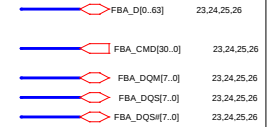
Group2

CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBX_CMD0	ODT_L		ODT_L	
FBX_CMD1			CS1#_L	
FBX_CMD2	CS0#_L			
FBX_CMD3	CKE_L		CKE_L	
FBX_CMD4	A9	A9	A11	A11
FBX_CMD5	A6	A6	A7	A7
FBX_CMD6	A3	A3	BA1	BA1
FBX_CMD7	A0	A0	A12	A12
FBX_CMD8	A8	A8	A8	A8
FBX_CMD9	A12	A12	A0	A0
FBX_CMD10	A1	A1	A2	A2
FBX_CMD11	RAS#	RAS#	RAS#	RAS#
FBX_CMD12	A13	A13	A14	A14
FBX_CMD13	BA1	BA1	A3	A3
FBX_CMD14	A14	A14	A13	A13
FBX_CMD15	CAS#	CAS#	CAS#	CAS#
FBX_CMD16		ODT_H		ODT_H
FBX_CMD17			CS1#_H	
FBX_CMD18		CS0#_H		
FBX_CMD19		CKE_H		CKE_H
FBX_CMD20	RST	RST	RST	RST
FBX_CMD21	A7	A7	A6	A6
FBX_CMD22	A4	A4	A5	A5
FBX_CMD23	A11	A11	A9	A9
FBX_CMD24	A2	A2	A1	A1
FBX_CMD25	A10	A10	WE#	WE#
FBX_CMD26	A5	A5	A4	A4
FBX_CMD27	BA2	BA2		
FBX_CMD28	WE#	WE#	A10	A10
FBX_CMD29	BA0	BA0	BA0	BA0
FBX_CMD30			BA2	BA2

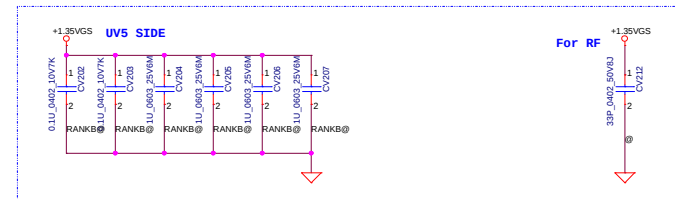
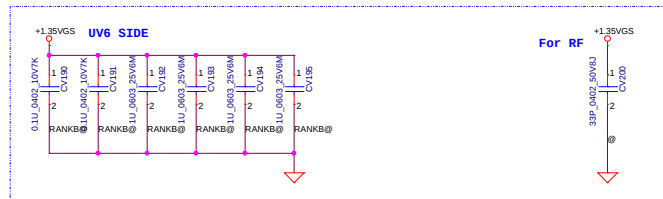


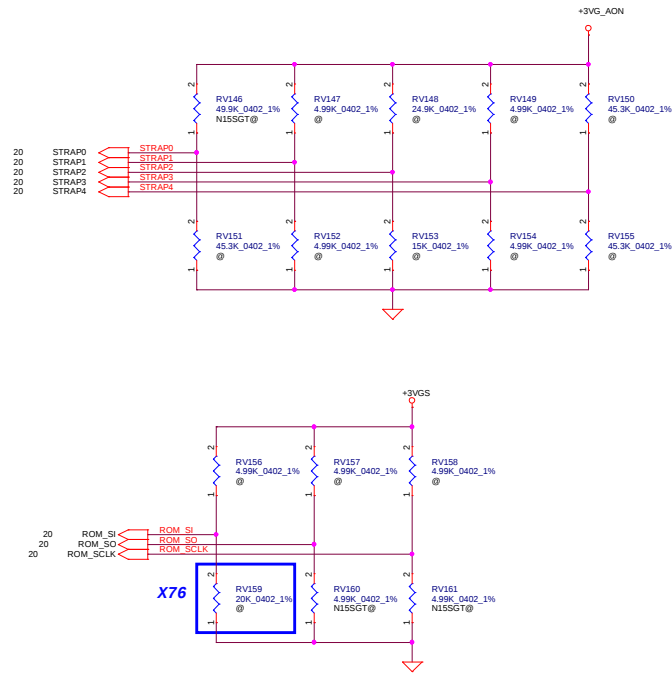
at least 16 mils width(optimal)
20 mils spacing to other signals/planes



CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3			CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16	ODT_H		ODT_H	
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	S0R3_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-CPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4663AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 20K							
	Micron 900MHz	MT41J256M16HA-0936:E	0x4							
		256M x 16	PD 24.9K							
	Samsung 900MHz	K4W4G1646D-BC1A	0x5							
		256M x 16	PD 30.1K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (16 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		

GPU	FB Memory (DDR3)		STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	H5TC4663AFR-11C		PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	256M x 16	0x4								
	MT41J256M16HA-0936:E		PU 10K	PU 10K	PD 10K	PU 10K				
	256M x 16	0xD								

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C									
B									
A									
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LCD POWER CIRCUIT

CMOS Camera

Touch Screen

Security Classification

LC Future Center Secret Data

Title

Issued Date

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2013/08/08

2013/08/05

edPI CMOS/Touch screen

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LCD POWER CIRCUIT

CMOS Camera

Touch Screen

Security Classification

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Title

Issued Date

Deciphered Date

2013/08/08

2013/08/05

edPI CMOS/Touch screen

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LCD POWER CIRCUIT

CMOS Camera

Touch Screen

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LCD POWER CIRCUIT

CMOS Camera

Touch Screen

Security Classification

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Title

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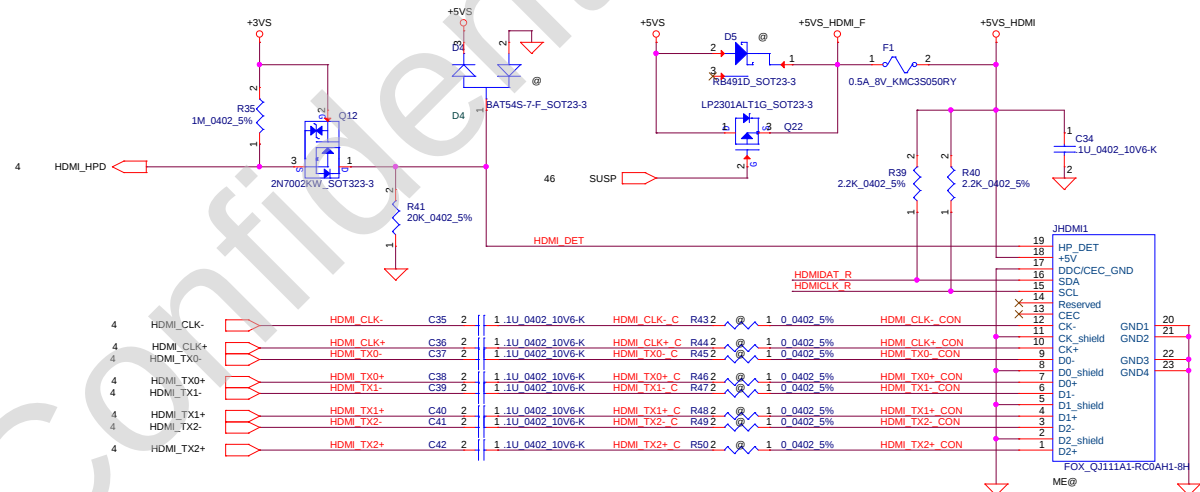
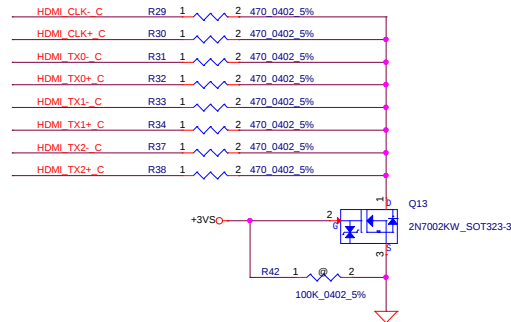
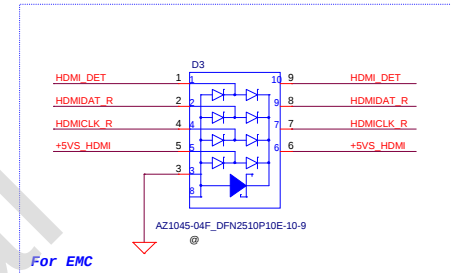
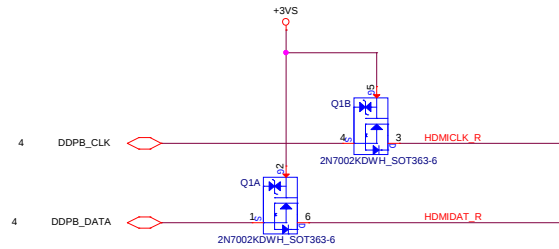
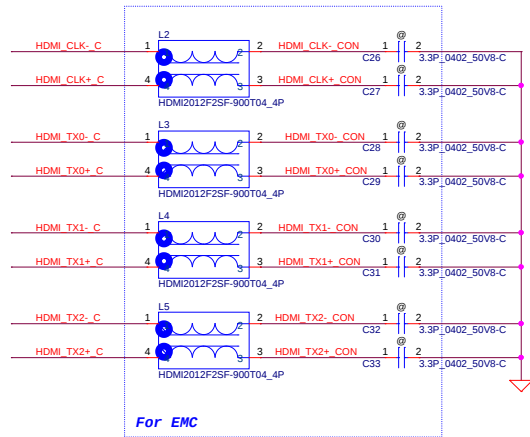
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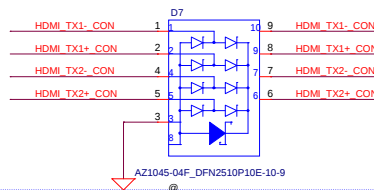
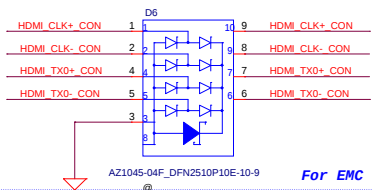
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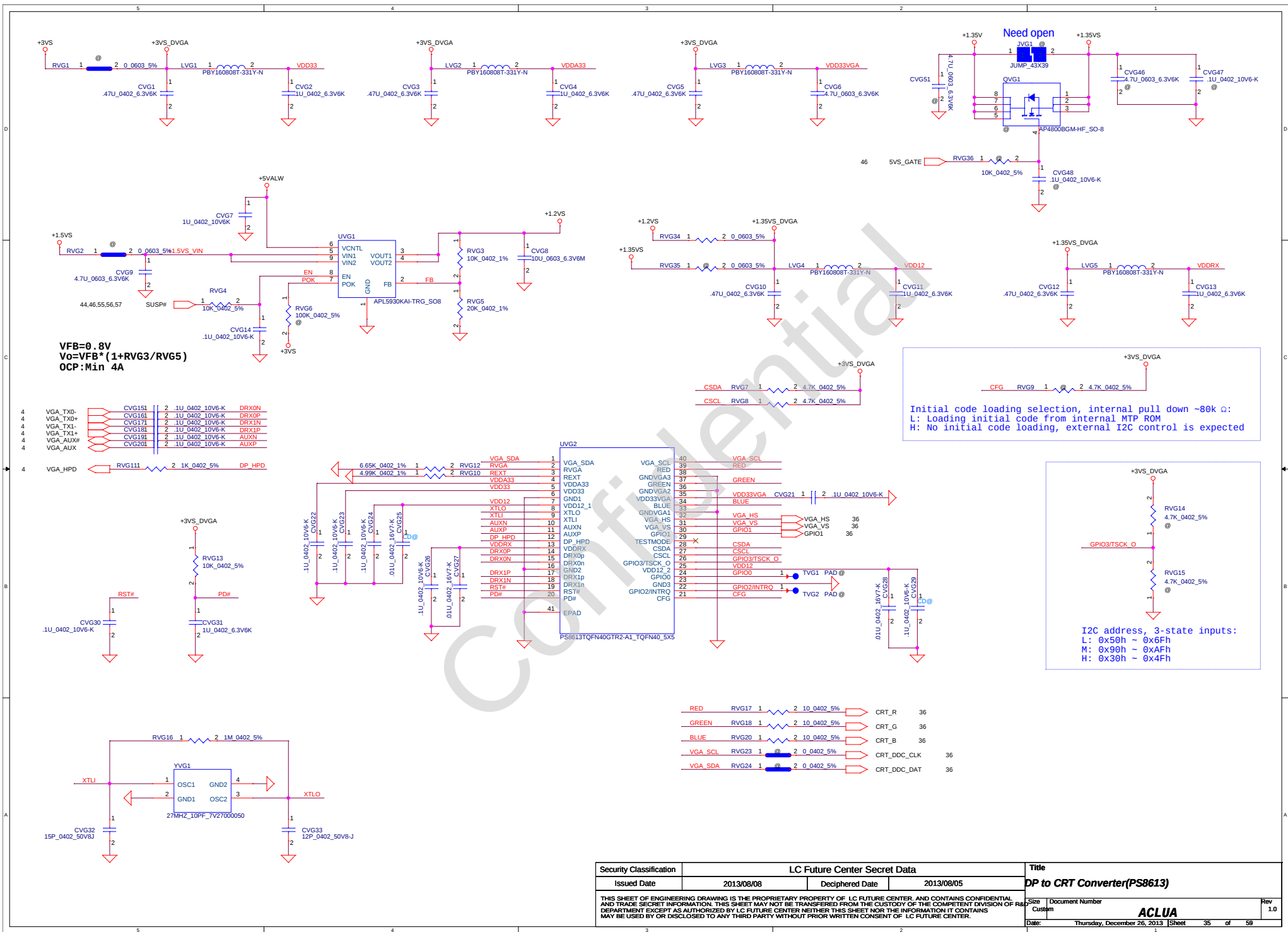
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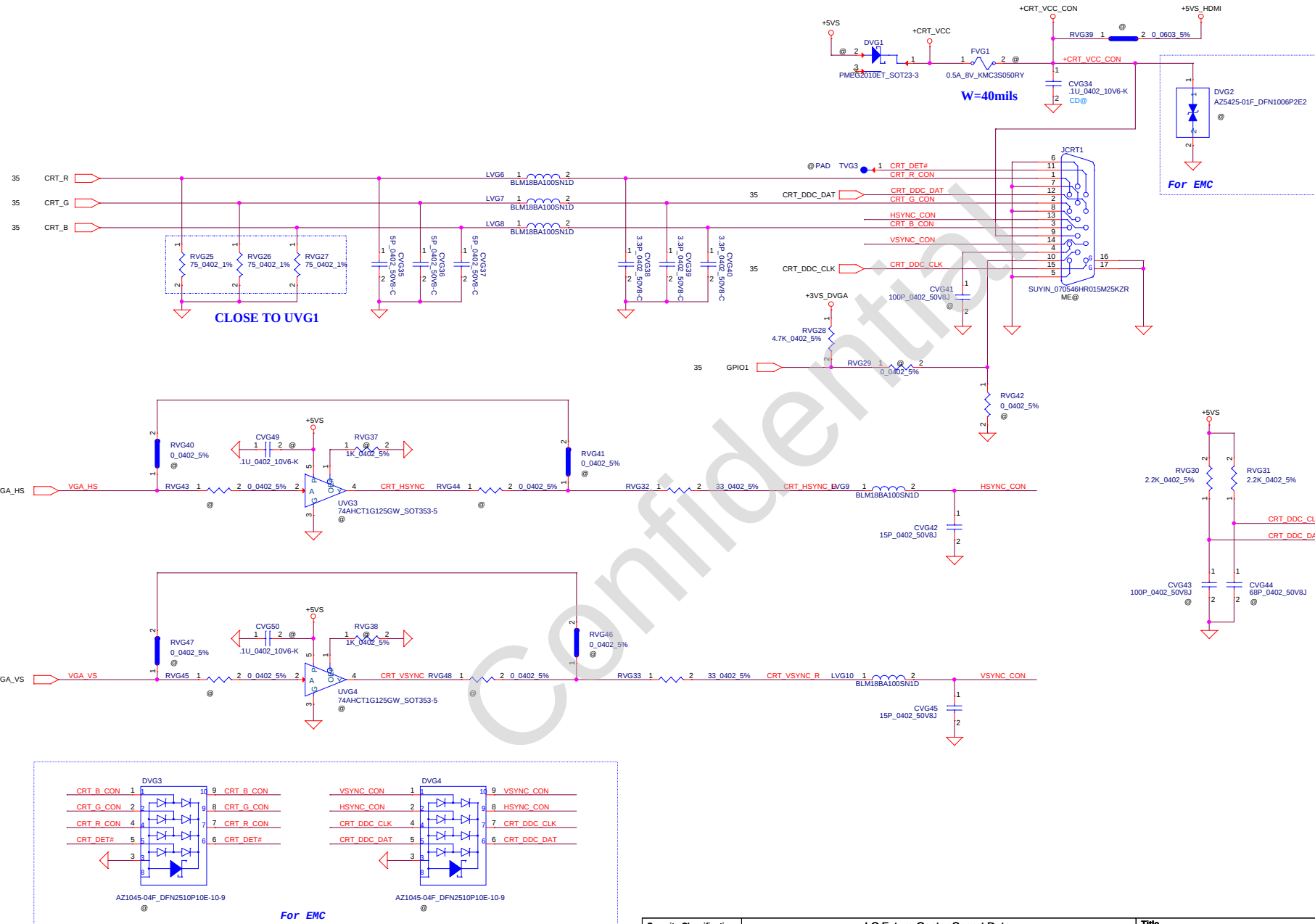
Close to JHDMI1



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CRT Connector



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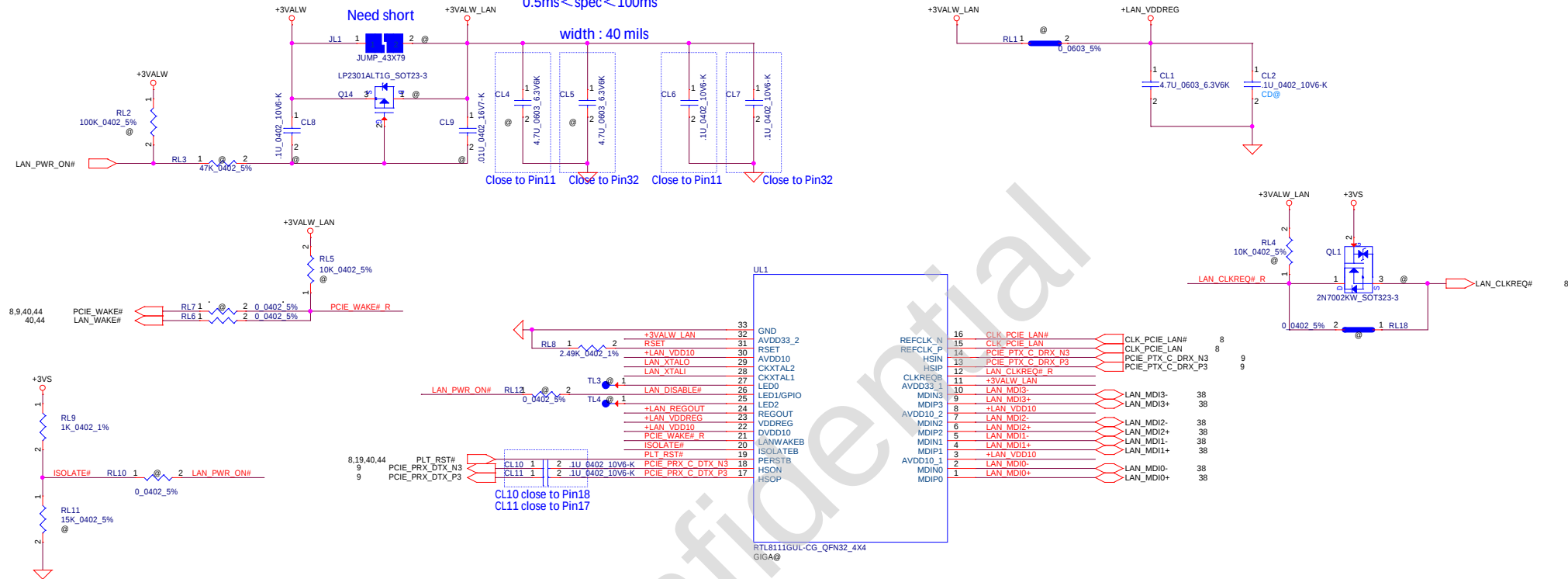
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100ms

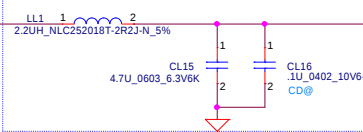
Need short

width : 40 mils

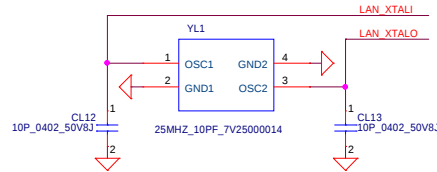
Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32



For RTL8111GUL/ RTL8106EUL (SWR mode)

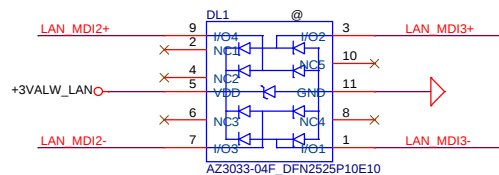


Layout Note: LL1 must be within 200mil to Pin36,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

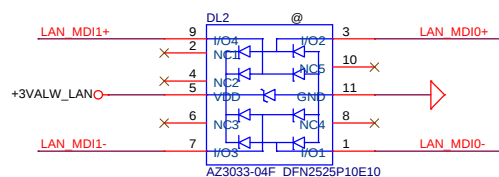


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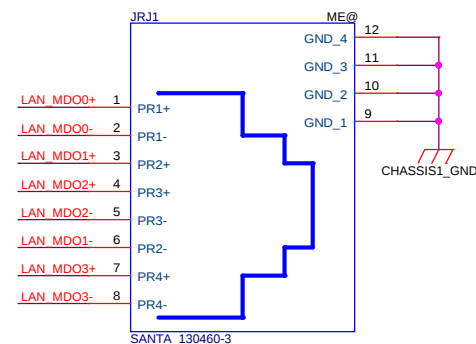
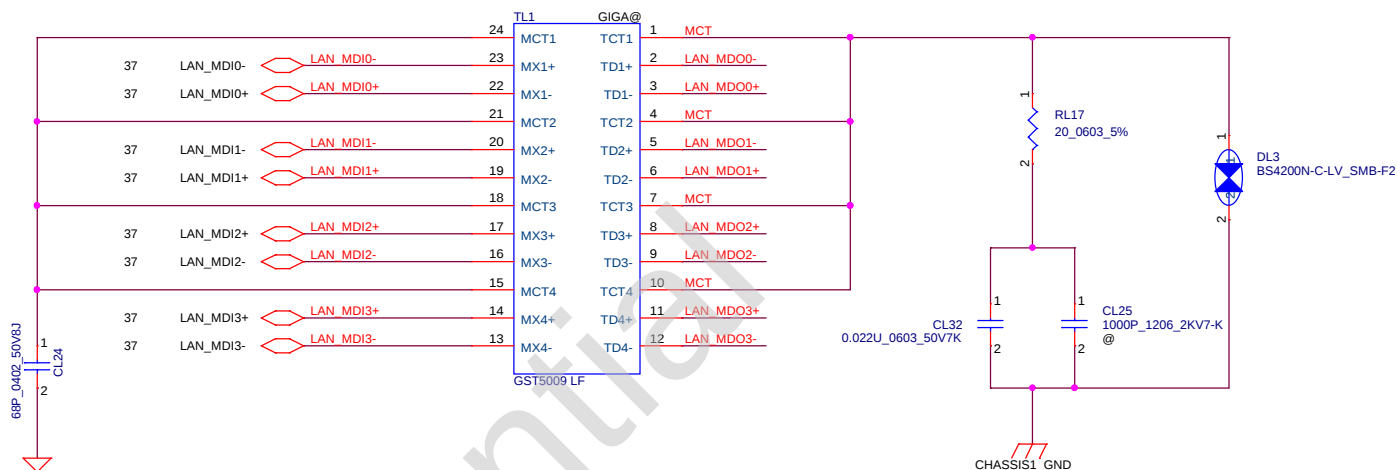
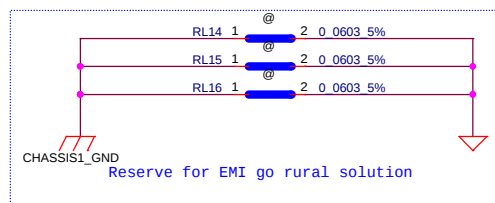
DL1/DL2
1'S PN:SC300003M00



Place Close to TL1

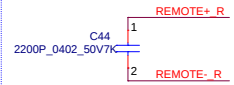


Place Close to TL2

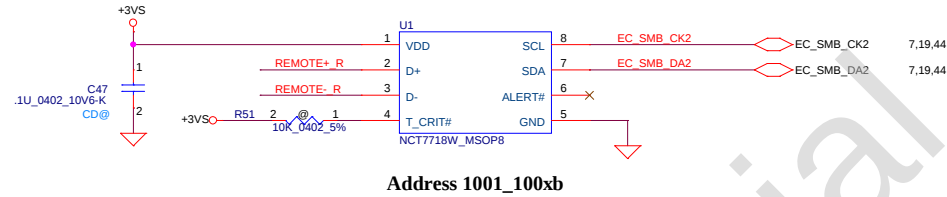


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Close to U1

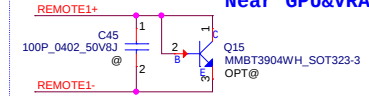


SMSC thermal sensor placed near DIMM

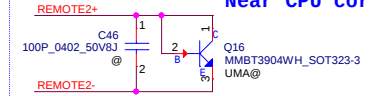


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

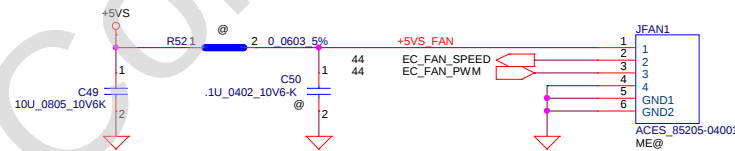
Near GPU&VRAM



Near CPU core

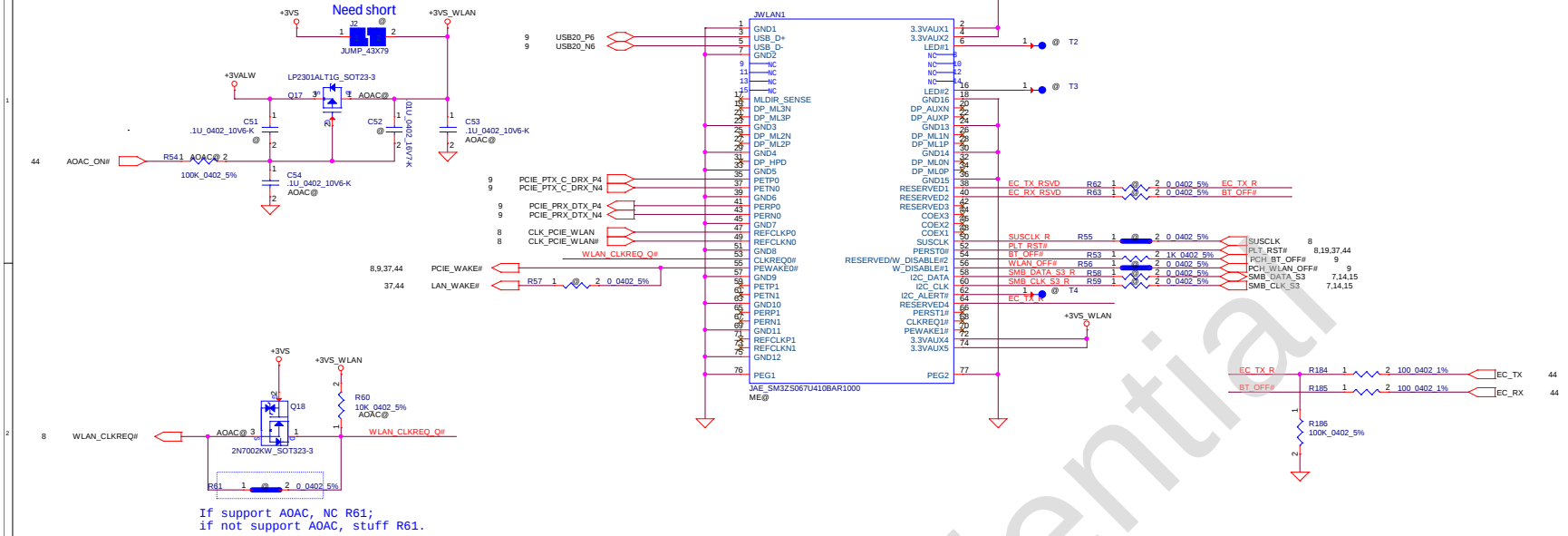


FAN Conn



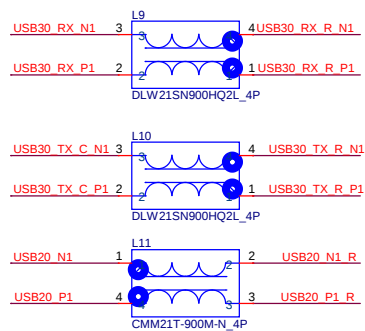
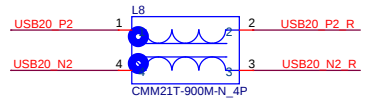
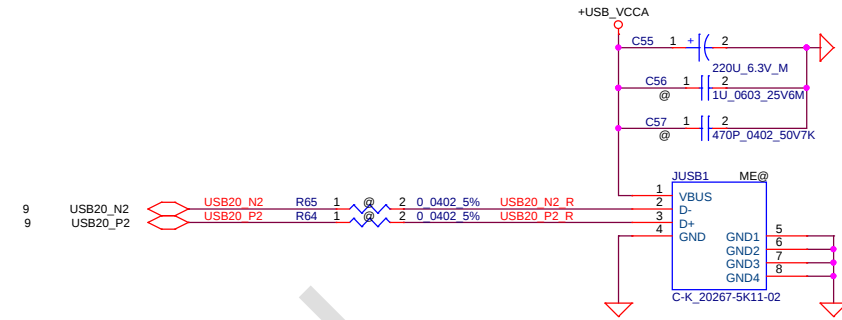
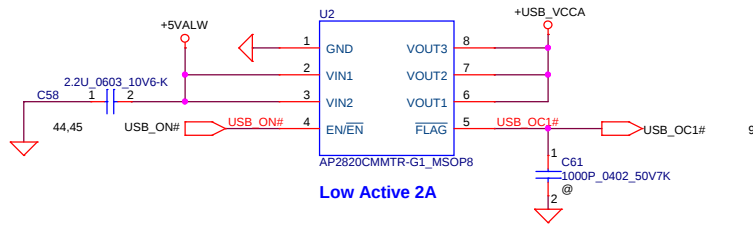
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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				Date: Thursday, December 26, 2013	Rev 1.0
				Sheet 39	of 59

Mini-Express Card(WLAN/WiMAX)

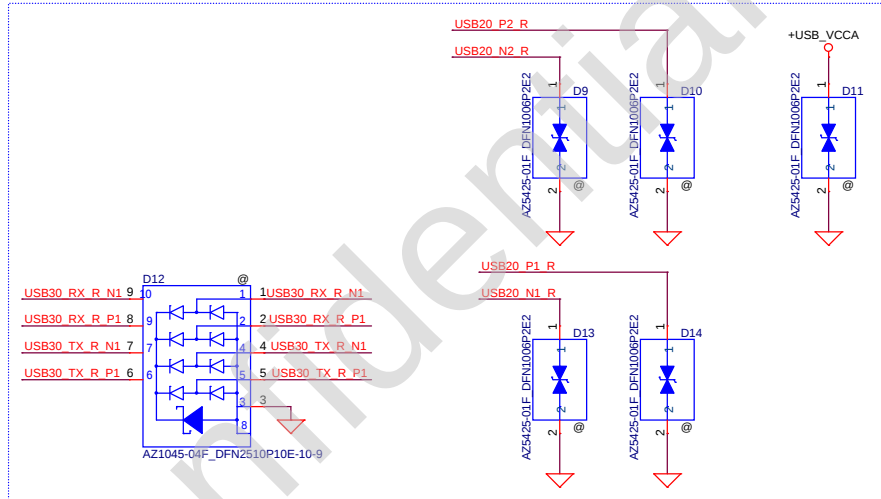


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	NGFF WLAN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Sign Custodian	Rev 1.0
				ACLU	
				Date: Thursday, December 26, 2013	Sheet 40 of 59

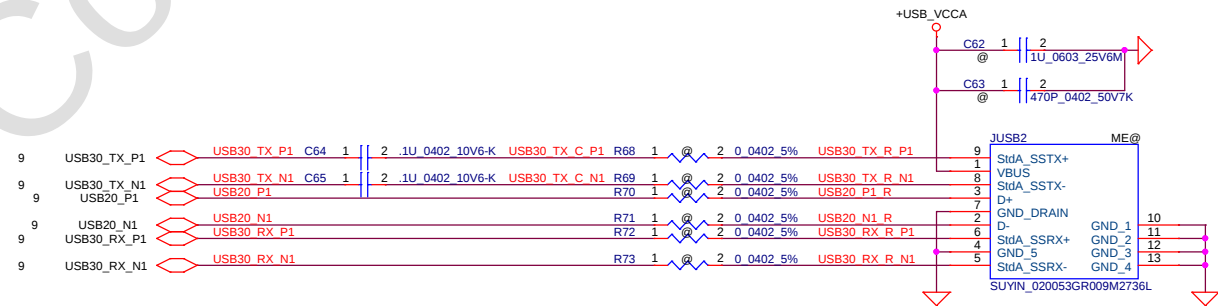
LEFT SIDE USB3.0 PORT X2



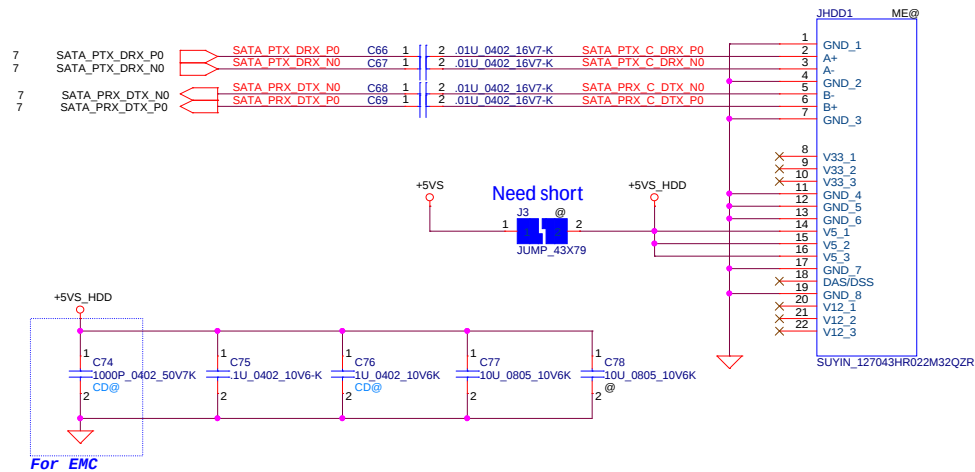
For EMC



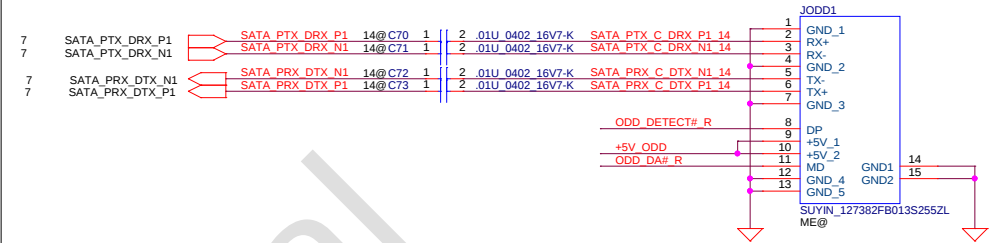
For EMC



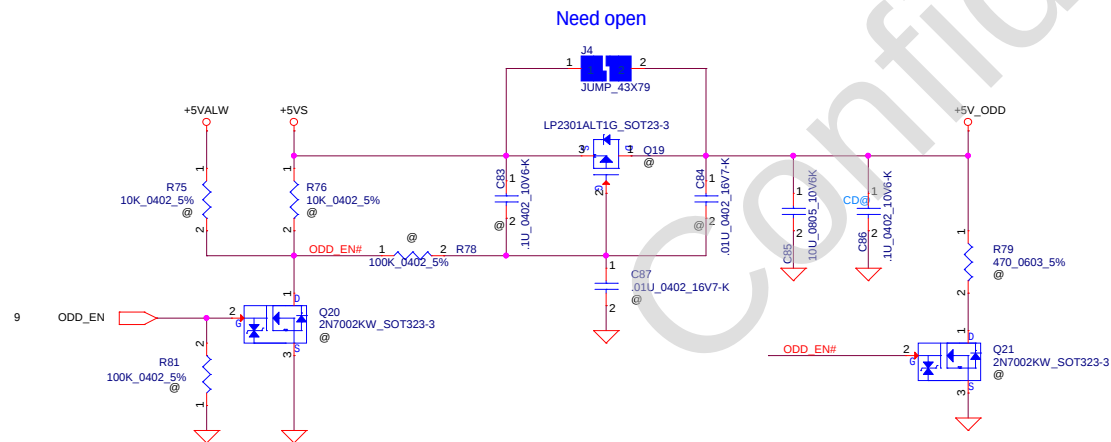
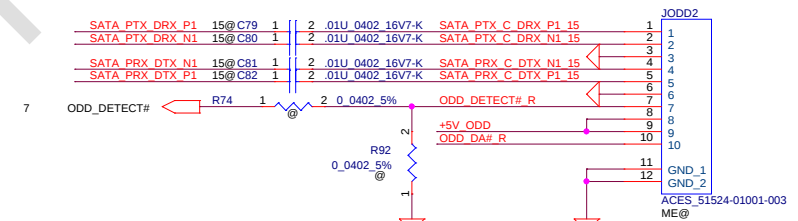
Security Classification				Title			
LC Future Center Secret Data				USB2.0/USB3.0 PORT (LEFT)			
Issued Date	2013/08/08	Deciphered Date	2013/08/05				
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				Custom	ACLUA	1.0	
				Date:	Thursday, December 26, 2013	Sheet	41 of 59

SATA HDD Conn.

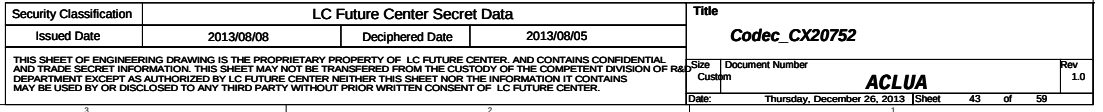
FOR 14"
SATA ODD Conn.

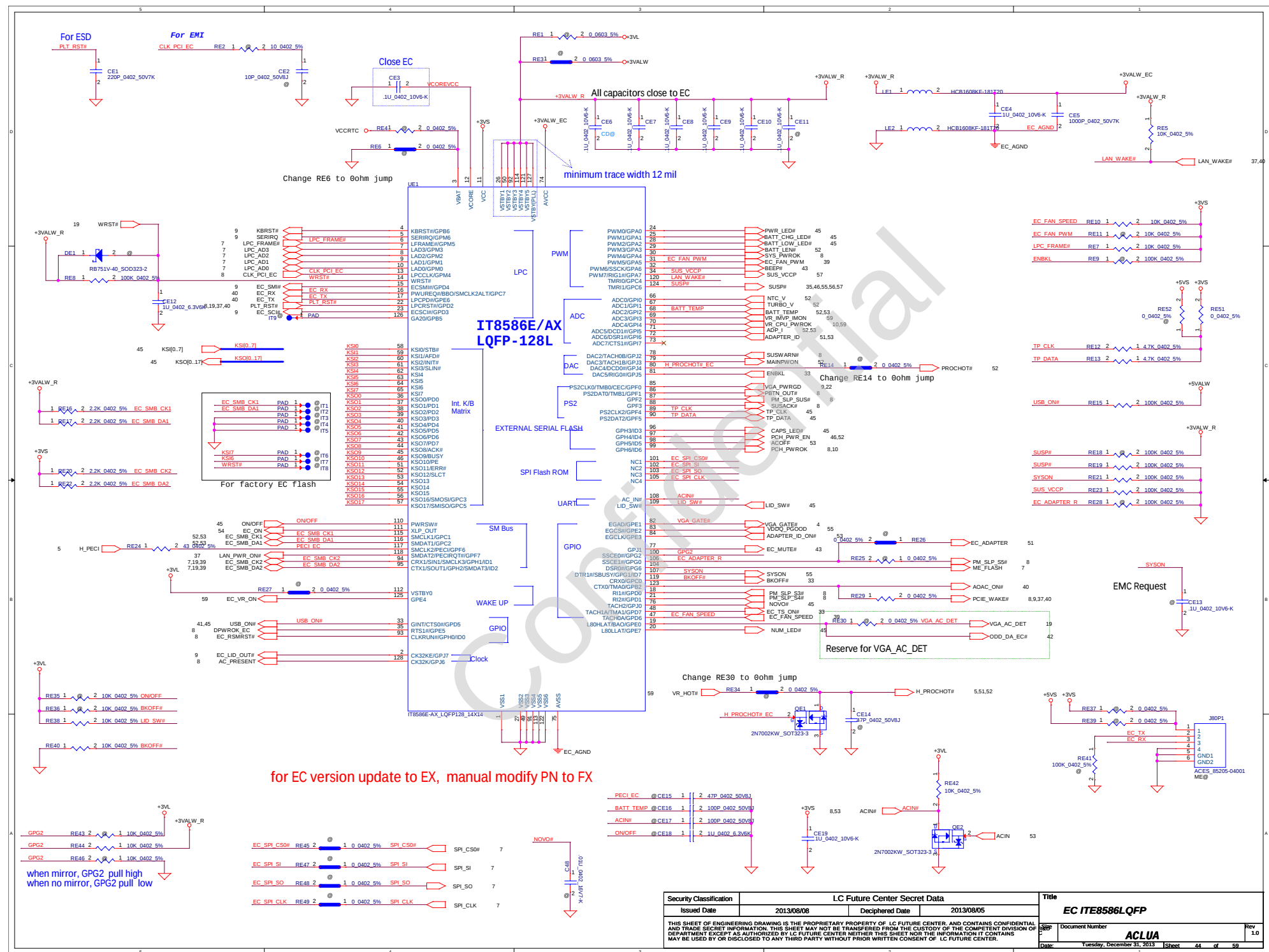


FOR 15"
SATA ODD FFC Conn



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	HDD/ODD CONN	
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				Custom	1.0
Date:				Thursday, December 26, 2013	Sheet 42 of 59





TP/B Connector

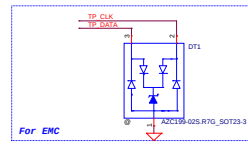
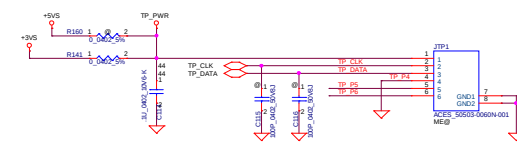
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44 CAPS_LED0 CAPS_LED0 30

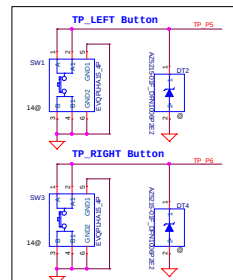
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NS209	21

Pin	Function
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34	PWR_CAPS_LED
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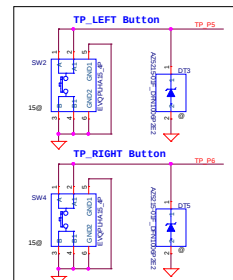
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RB.2	K517.14	K512.15
RB.3	K516.14	K513.15
RB.4	K509.14	K506.15
RB.5	K514.14	K501.15
RB.6	K515.14	K518.15
RB.7	K508.14	K502.15
RB.8	K513.14	K504.15
RB.9	K513.14	K507.15
RB.10	K516.14	K503.15
RB.11	K501.14	K508.15
RB.12	K510.14	K503.15
RB.13	K502.14	K5012.15
RB.14	K504.14	K5013.15
RB.15	K507.14	K5014.15
RB.16	K508.14	K5011.14
RB.17	K506.14	K5010.15
RB.18	K503.14	K5015.15
RB.19	K5012.14	K5016.15
RB.20	K5013.14	K5017.15
RB.21	K5014.14	RB_LED_PWR_15
RB.22	K5011.14	CAPS_LED_PWR_15
RB.23	K5015.14	VID_15
RB.24	K5015.14	NUR_LED_15



For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R



For 14"



For 15"

[illegible]

Right Side USB2.0 Port X 1 (USB/B)

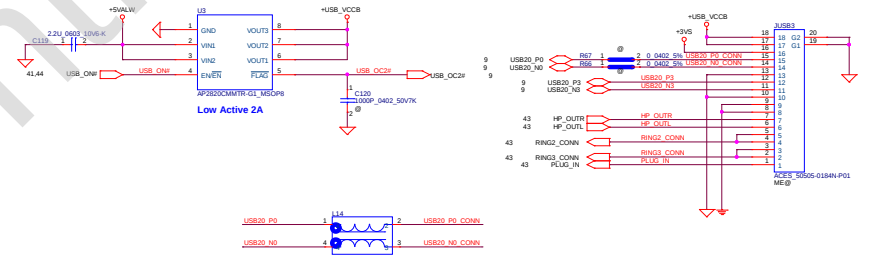
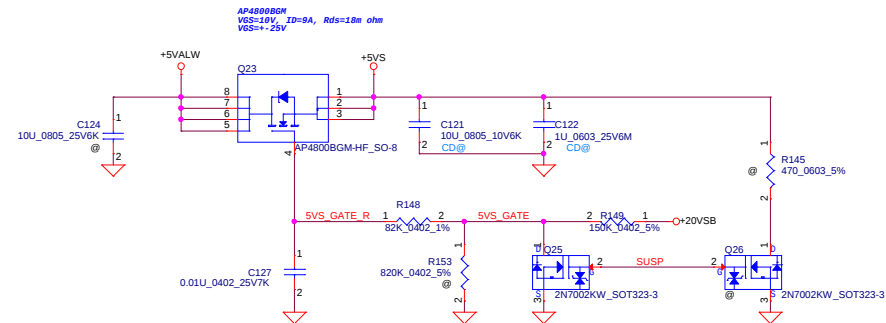


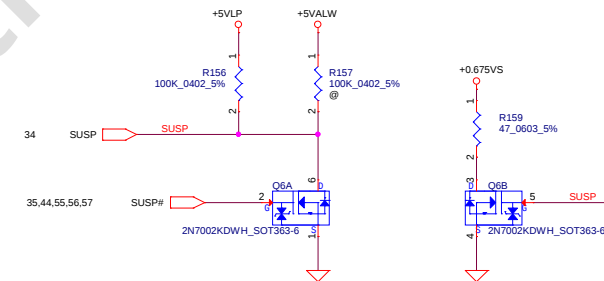
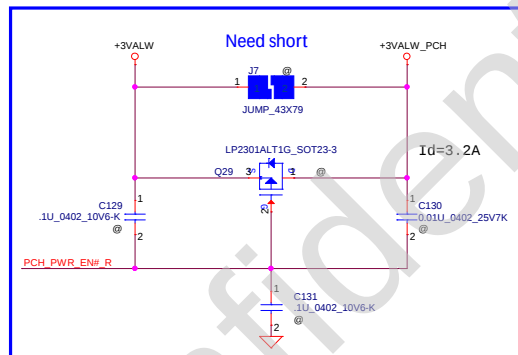
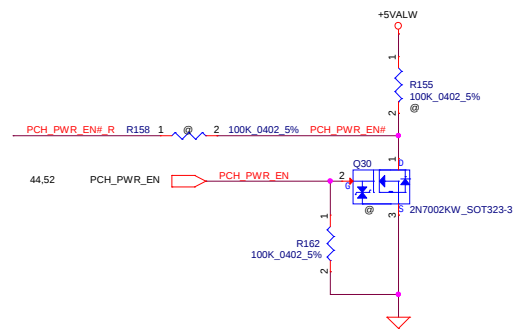
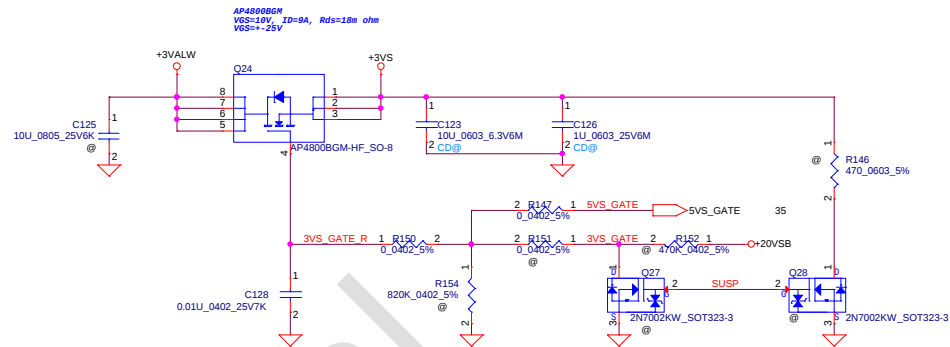
Figure 10 is a schematic diagram of the LED driver circuit. It shows three identical LED driver stages. Each stage consists of a MOSFET (D13), a diode (D14), and a current source (D15). The MOSFETs are driven by a common gate signal (G13). The current sources are connected to a common source (S13). The LED strings are connected to the drains of the MOSFETs. The first stage drives PWR_LED1 through PWR_LED4. The second stage drives BATT_LOW_LED1 through BATT_LOW_LED4. The third stage drives BATT_CHG_LED1 through BATT_CHG_LED4. The LED strings are connected to a common anode (A13).

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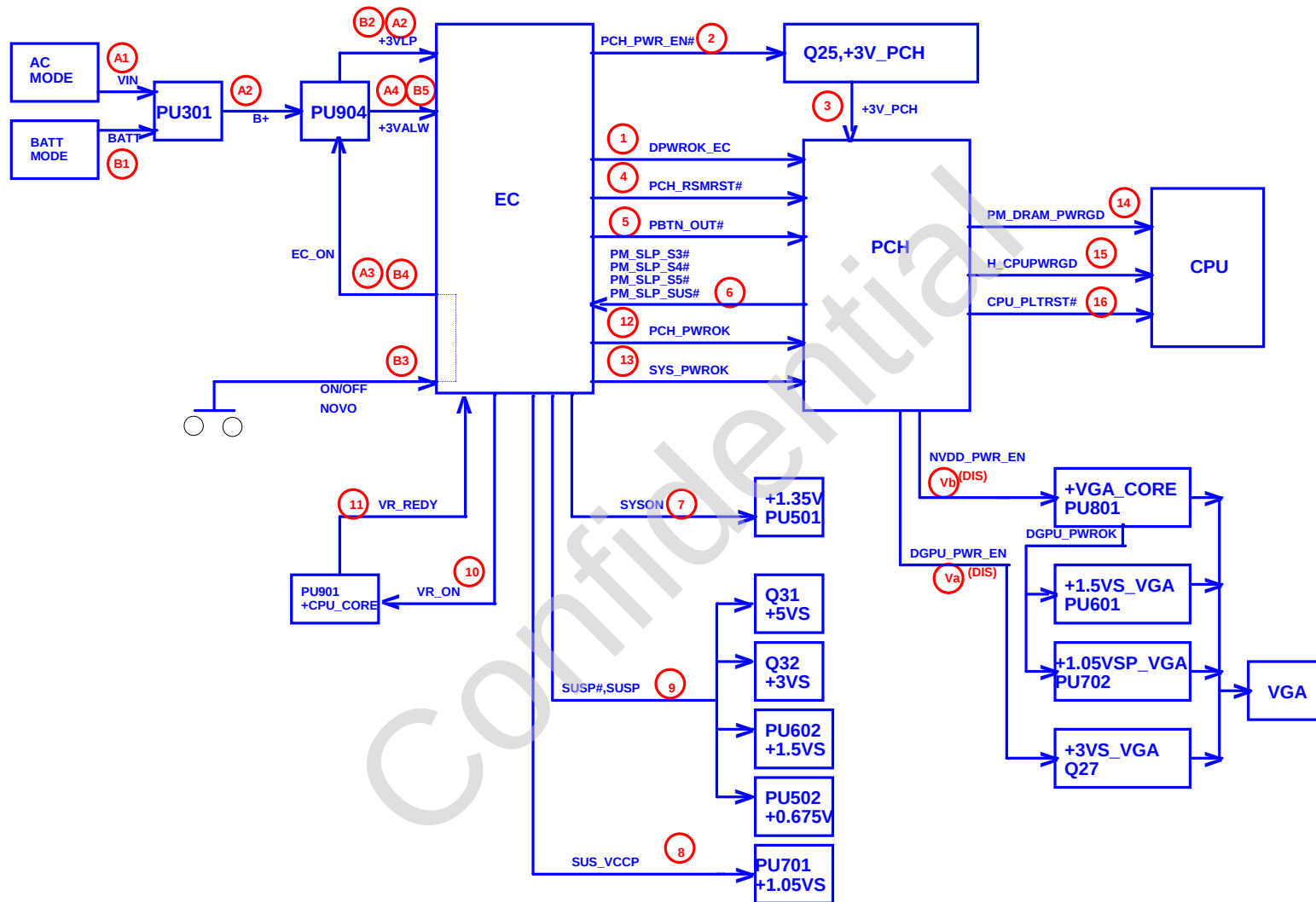
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+3VALW to +3VS



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LAN chip



Transformer

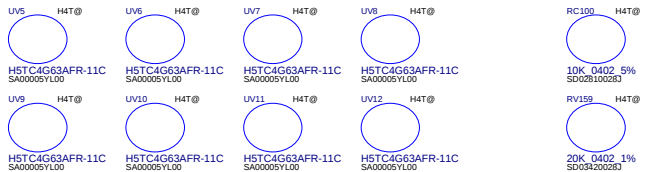


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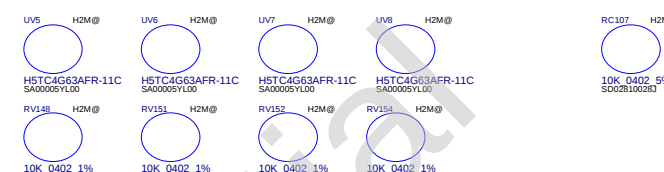


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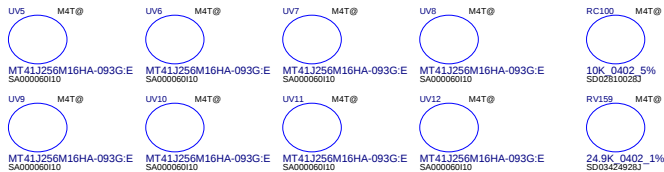
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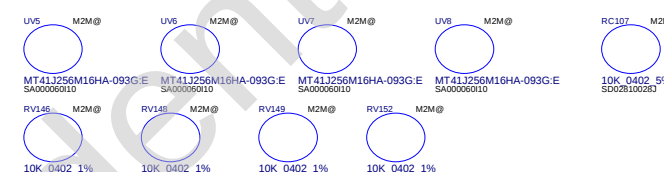
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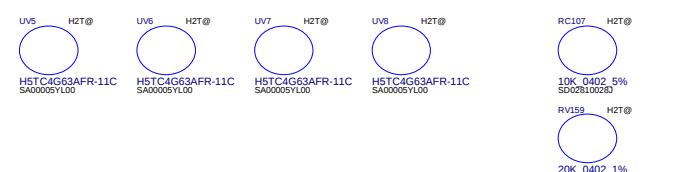
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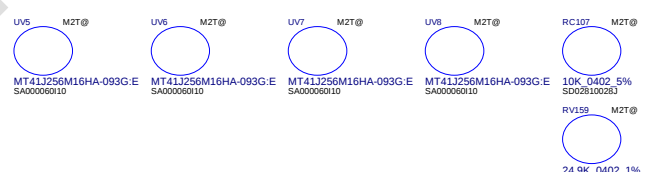
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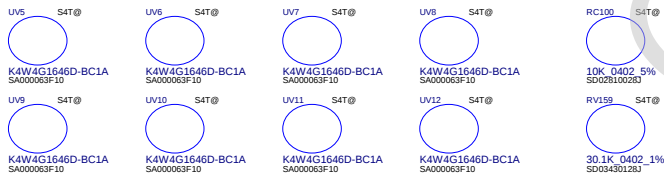
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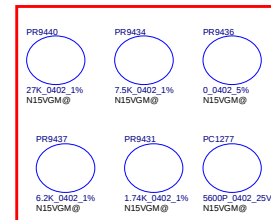
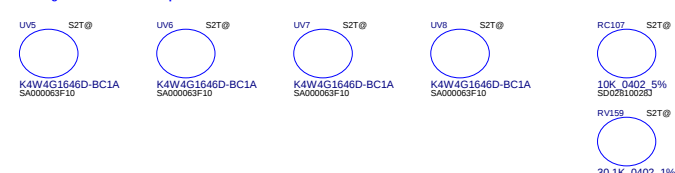
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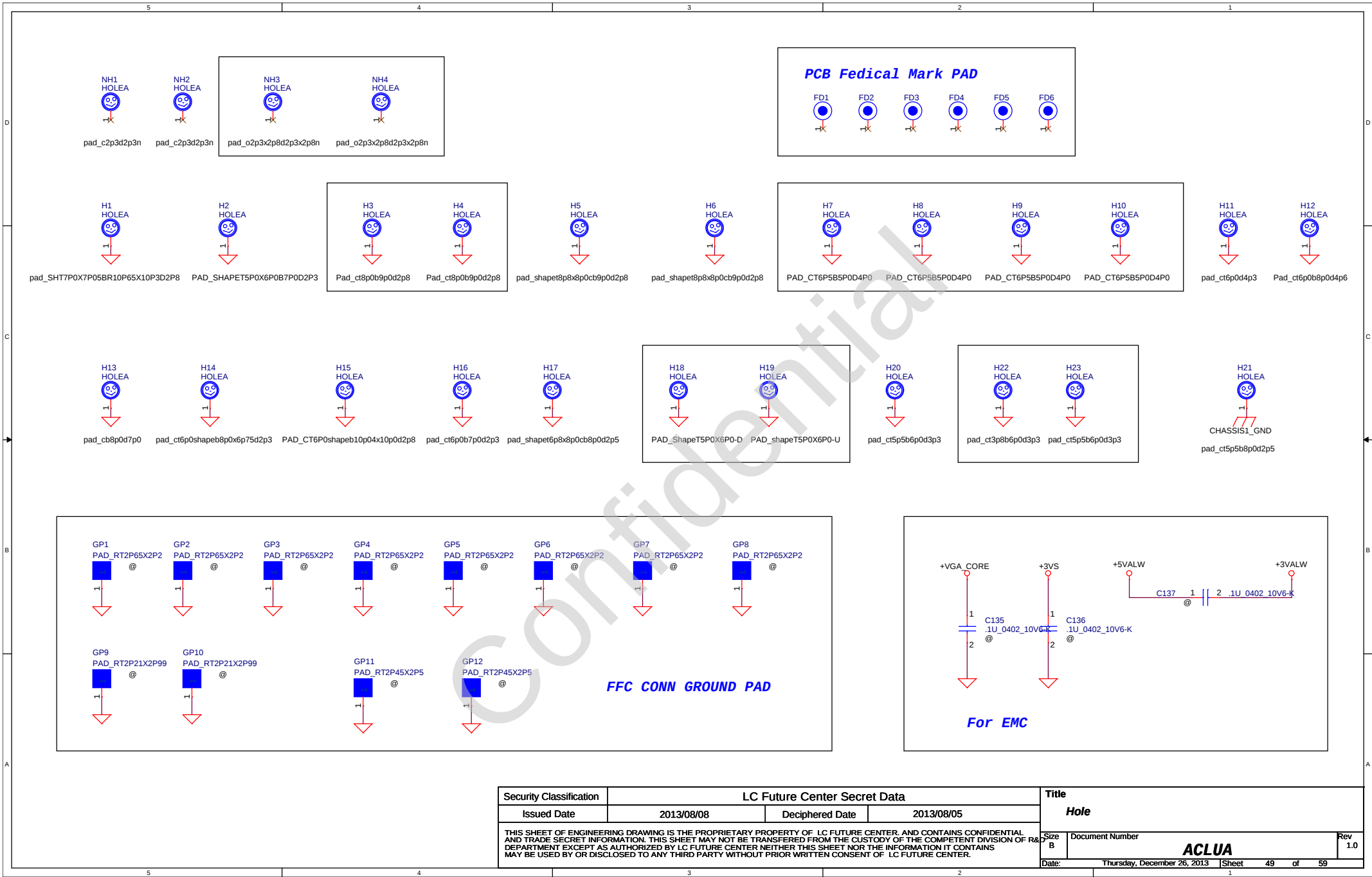
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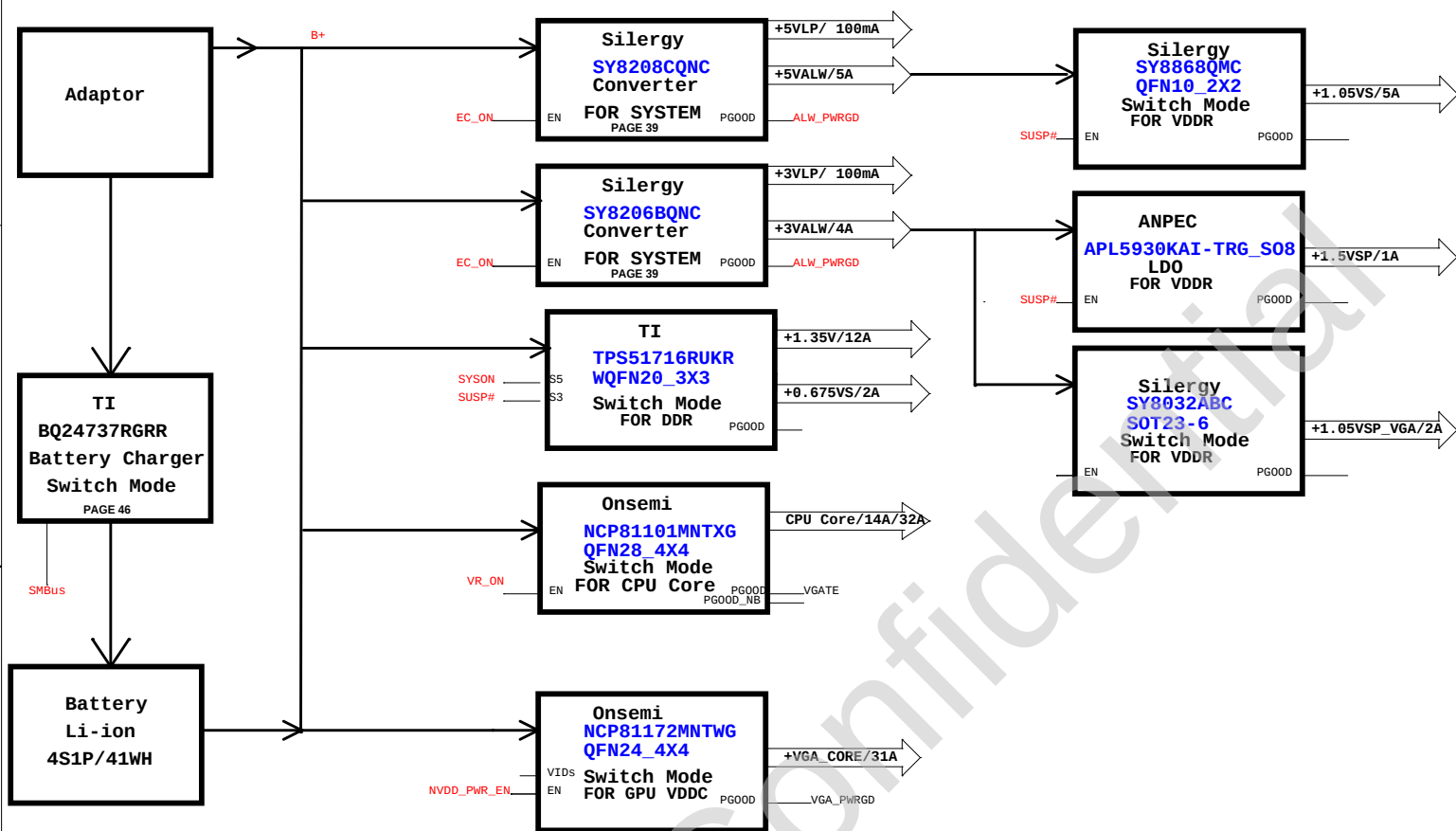
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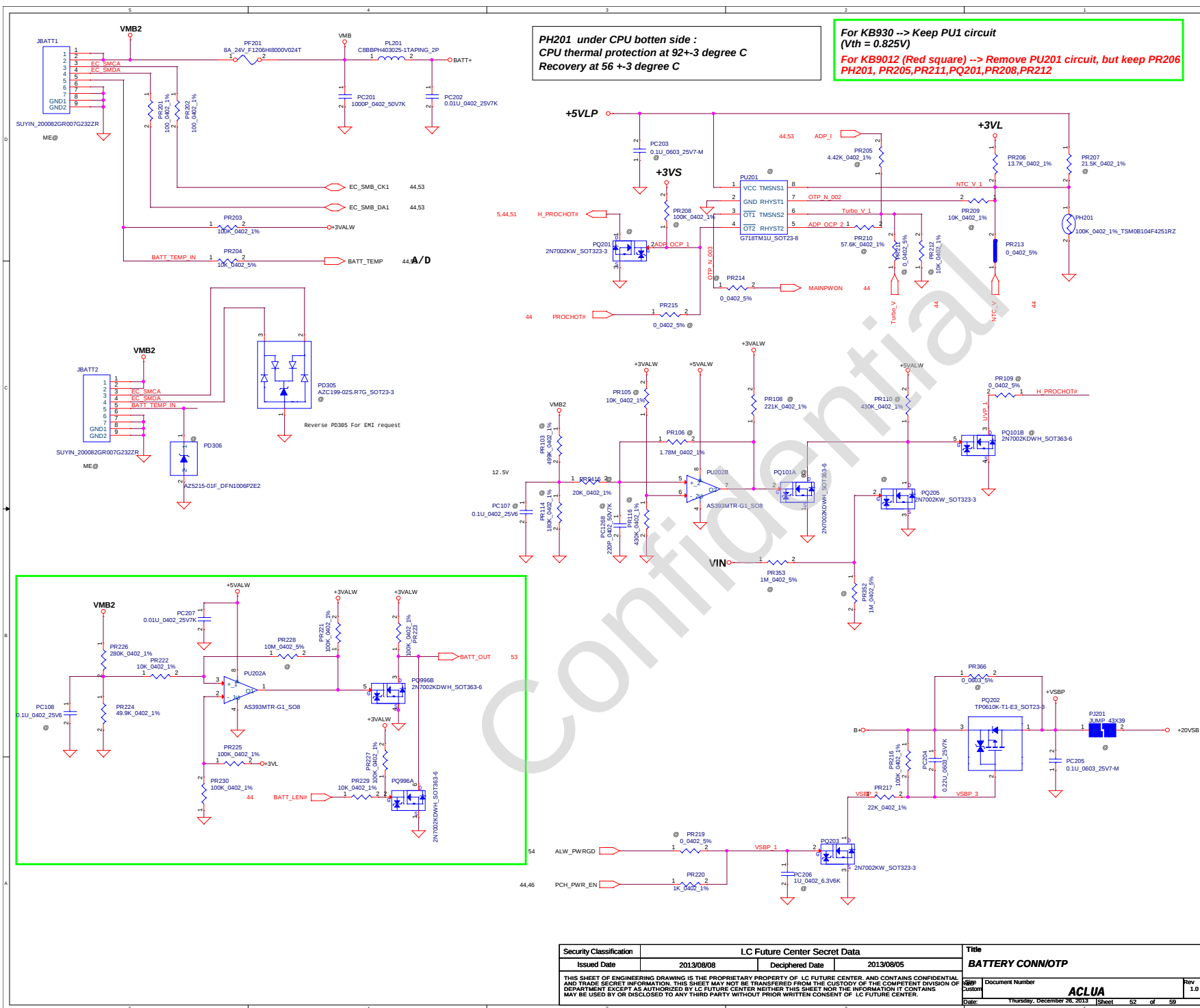
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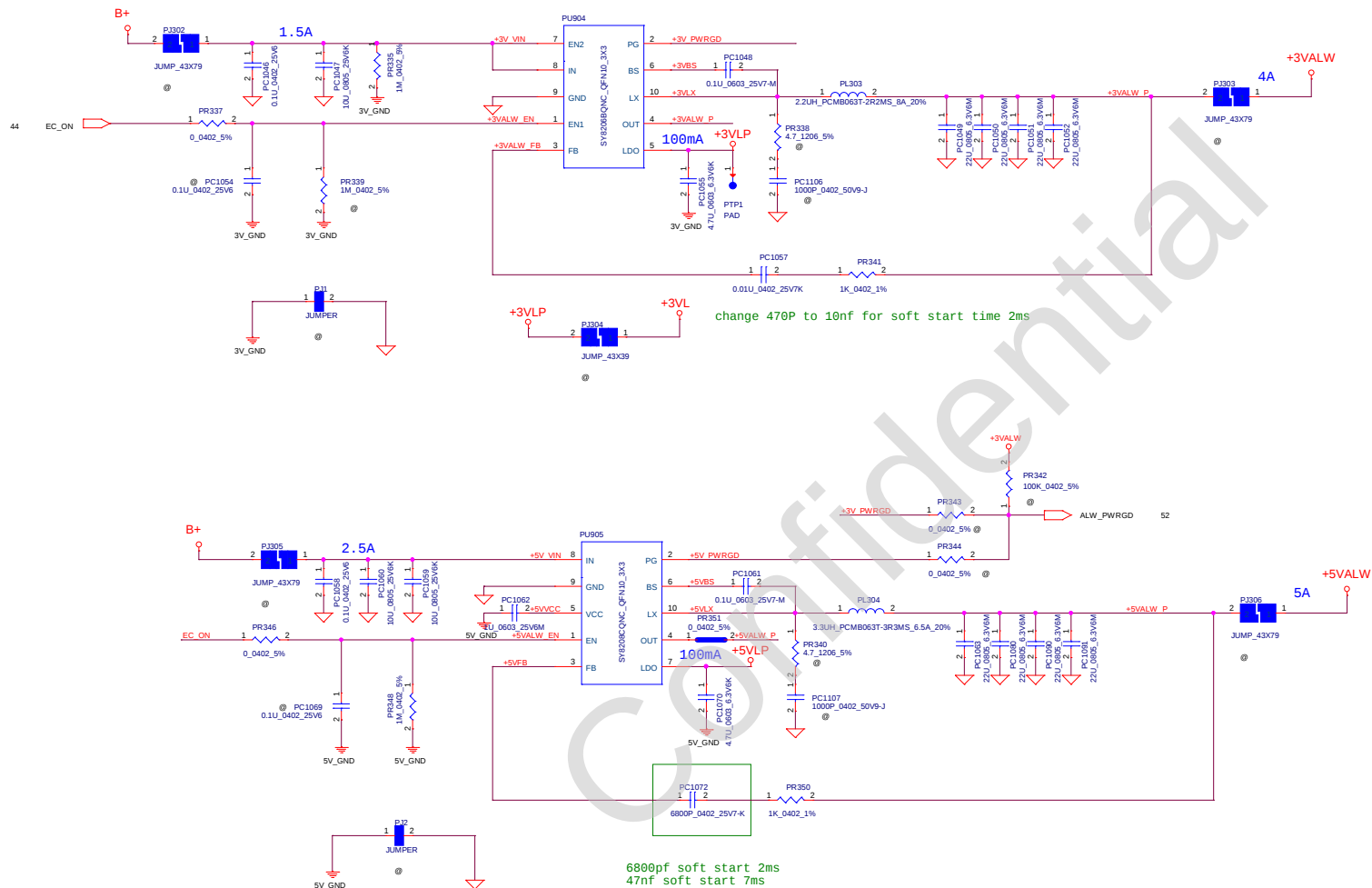
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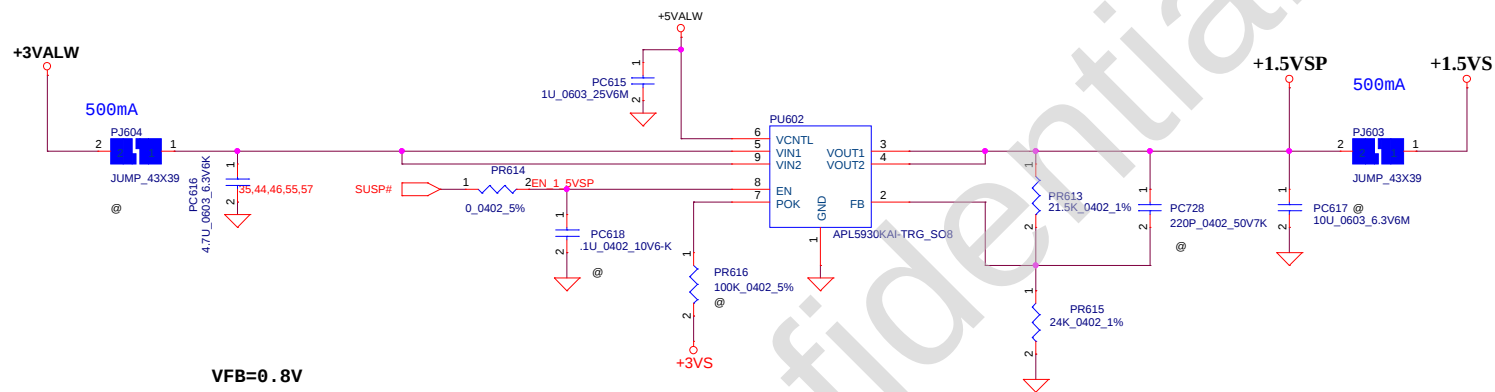
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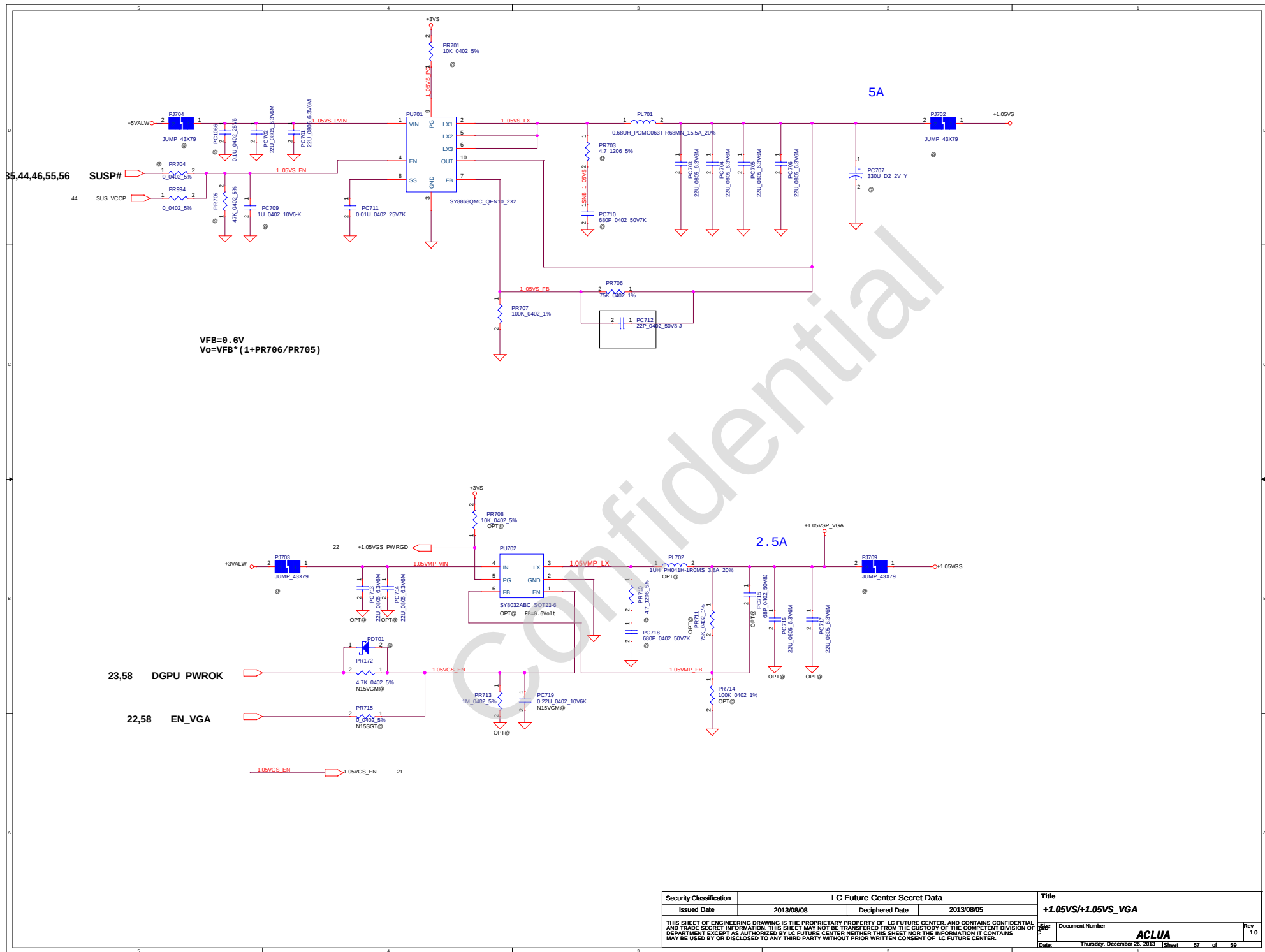
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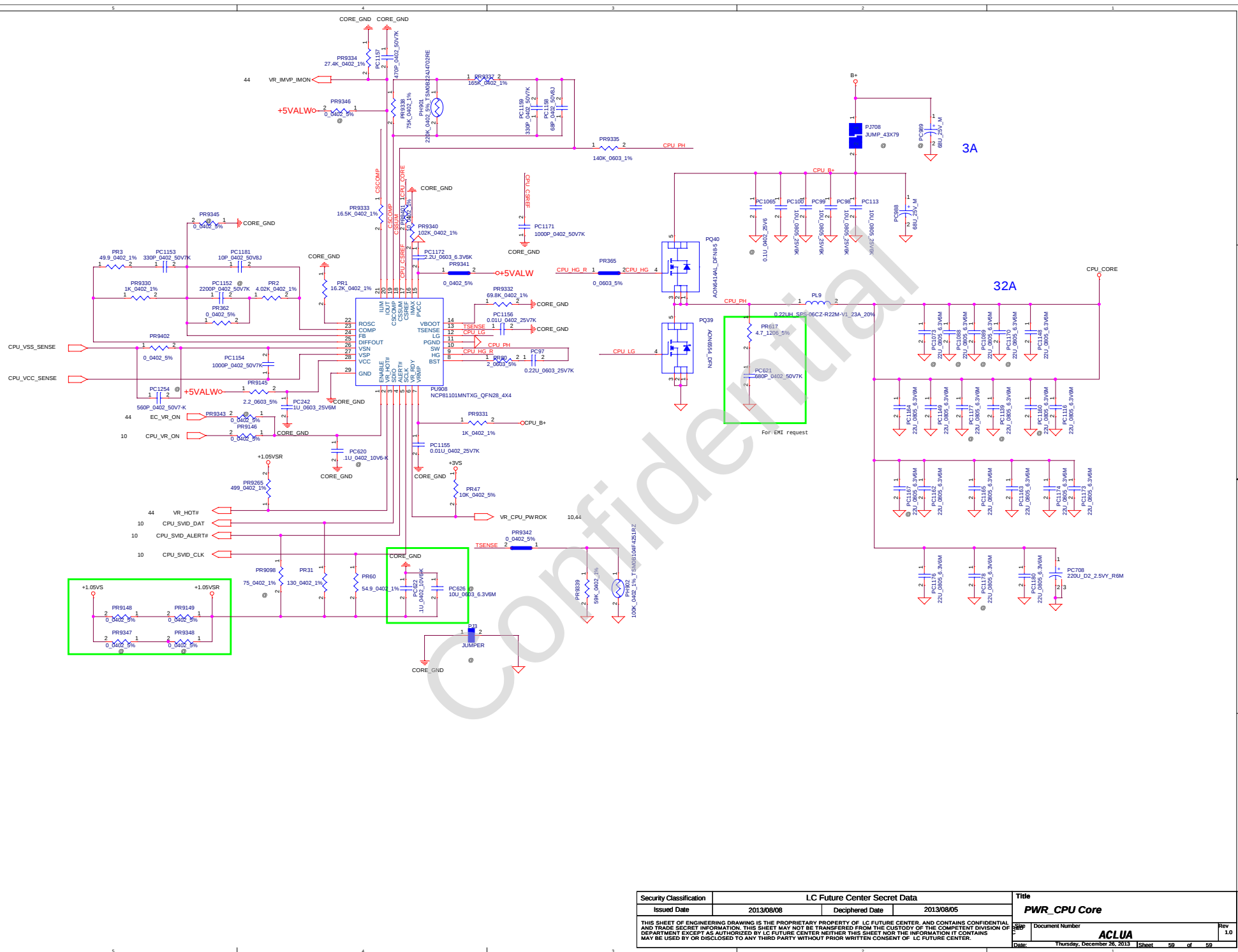
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