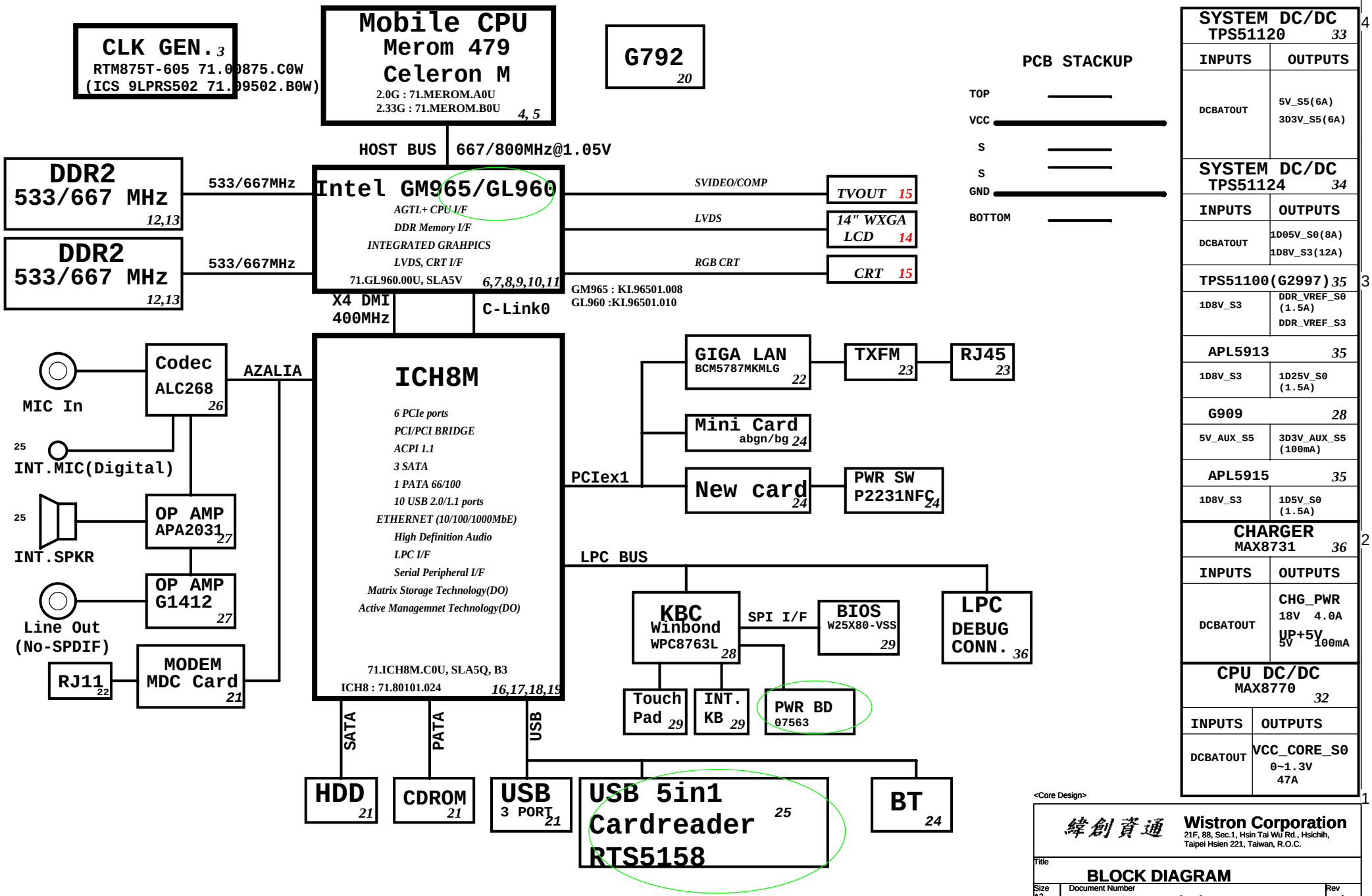
Calado Block Diagram

Project code: 91.4X401.001
PCB P/N : 07227
REVISION : -1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 33

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 34

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(8A) 1D8V_S3(12A)

TPS51100(G2997) 35

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5913 35

1D8V_S3	1D25V_S0 (1.5A)

G909 28

5V_AUX_S5	3D3V_AUX_S5 (100mA)

APL5915 35

1D8V_S3	1D5V_S0 (1.5A)

CHARGER MAX8731 36

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 32

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: Calado | Rev: -1

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ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	BT
6	Cardreader
7	MINICARD
8	CCD
9	NEW1

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Title: Reference

Size: A3 | Document Number: Volvi2 | Rev: -1

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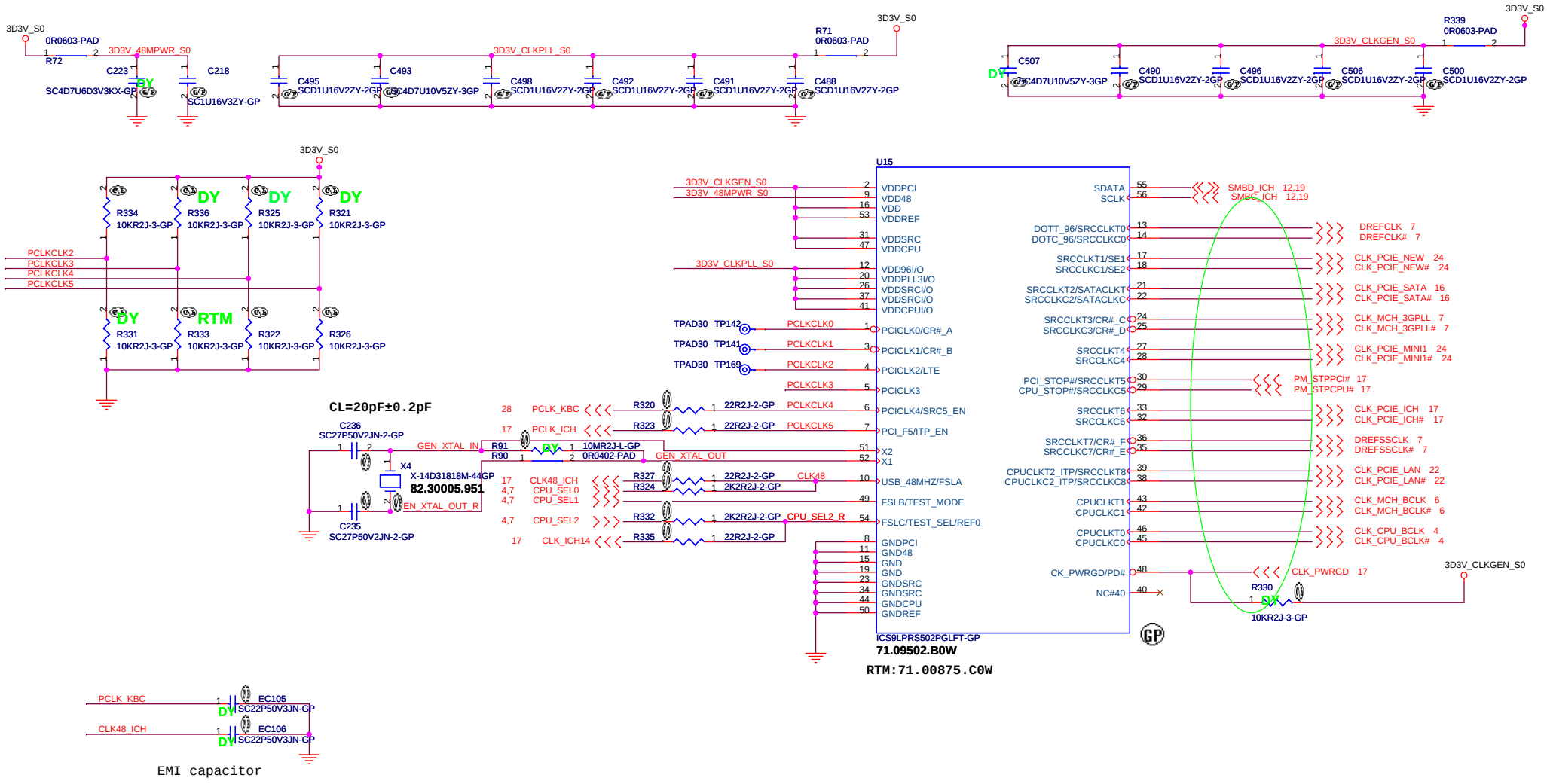

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

<Core Design>

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Title: Clock Generator

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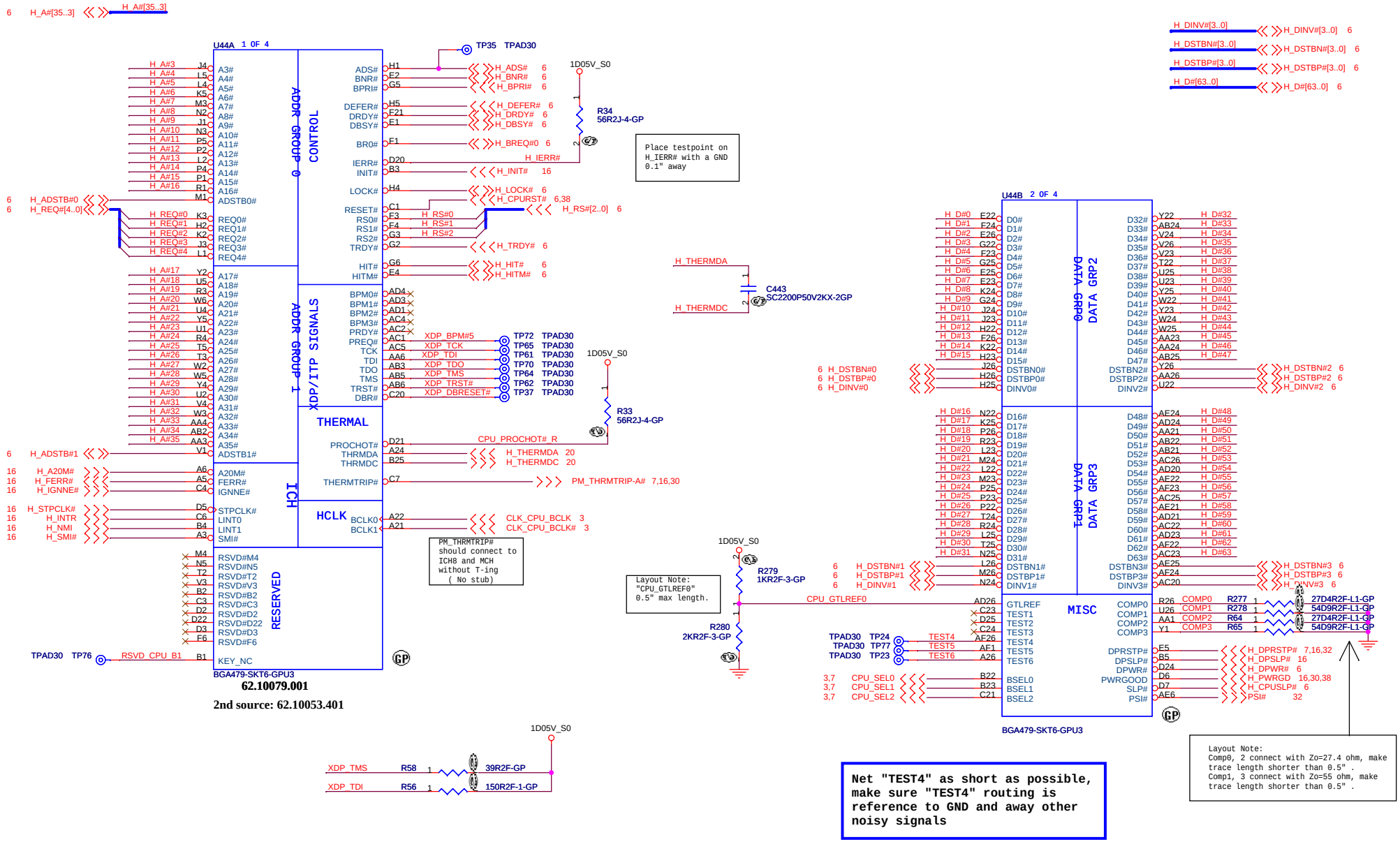

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Title: CPU (1 of 2)

Size | Document Number: Calado | Rev: -1

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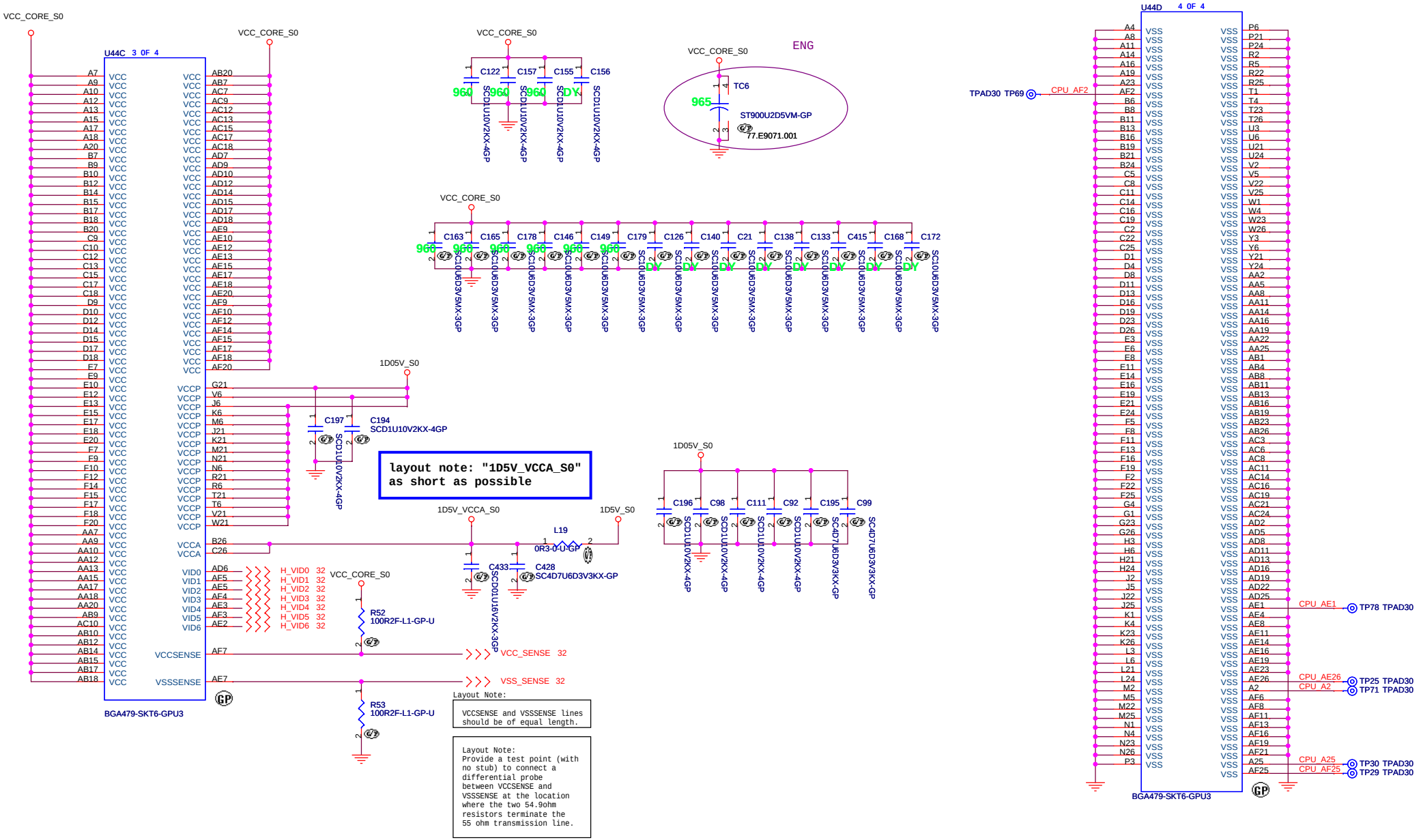

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Title	**CPU (2 of 2)**
Size	Document Number: **Calado**
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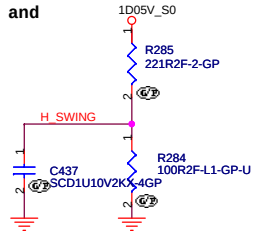
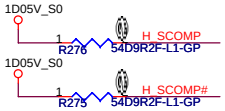
H_SWING routing Trace width and Spacing use 10 / 20 mil

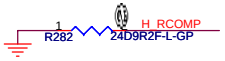
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

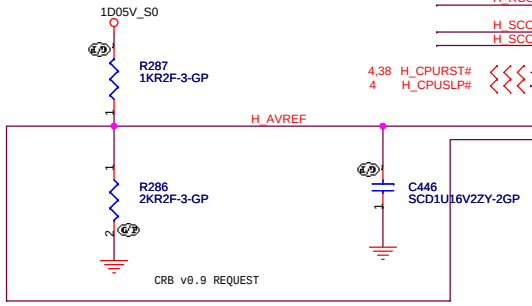


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil



<Core Design>

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Title	**GMCH (1 of 6)**
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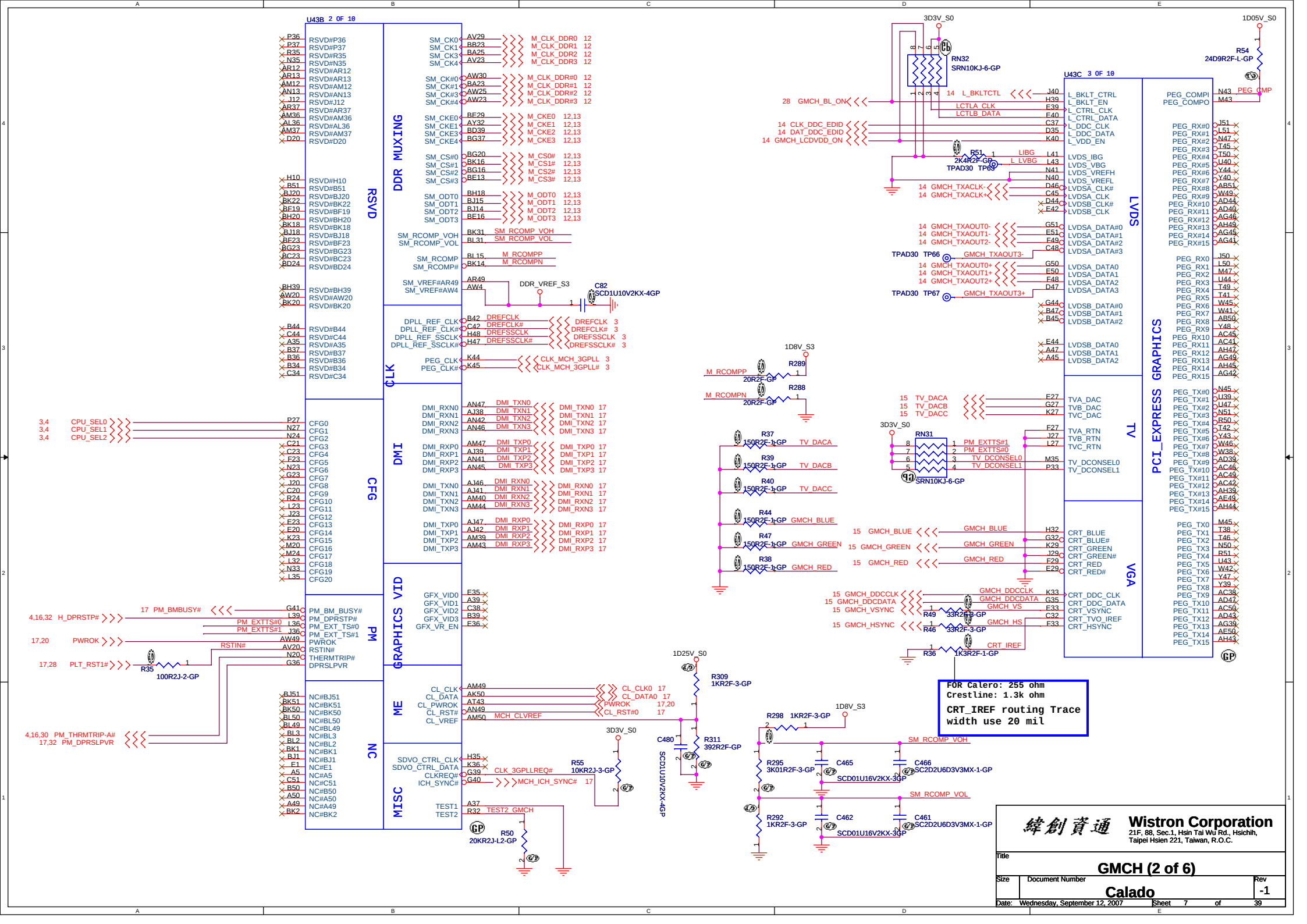
U43B 2 OF 10
RSVD
DDR MUXING
CLK
CFG
DMI
GRAPHICS VID
PM
ME
NC
MISC
U43C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
RN32 SRN10KJ-6-GP
RN31 SRN10KJ-6-GP
R54 24D9R2F-L-GP
R51 2K4R2F-GP
R37 150R2F-1-GP TV_DACA
R39 150R2F-1-GP TV_DACB
R40 150R2F-1-GP TV_DACC
R44 150R2F-1-GP GMCH_BLUE
R47 150R2F-1-GP GMCH_GREEN
R38 150R2F-1-GP GMCH_RED
R289 20R2F-GP M_RCOMPP
R288 20R2F-GP M_RCOMPN
R309 1KR2F-3-GP
R311 392R2F-GP
R298 1KR2F-3-GP
R295 3K01R2F-3-GP
R292 1KR2F-3-GP
R55 10KR2J-3-GP
R50 20KR2J-L2-GP
R35 100R2J-2-GP
R49 33R2F-3-GP
R46 33R2F-3-GP
R36 1K3R2F-1-GP
C82 SCD1U10V2KX-4GP
C480 SCD1U10V2KX-4GP
C465 SCD01U16V2KX-3GP
C466 SC2D2U6D3V3MX-1-GP
C462 SCD01U16V2KX-3GP
C461 SC2D2U6D3V3MX-1-GP
3D3V_S0
1D8V_S3
1D25V_S0
1D05V_S0
DDR_VREF_S3
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
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Title
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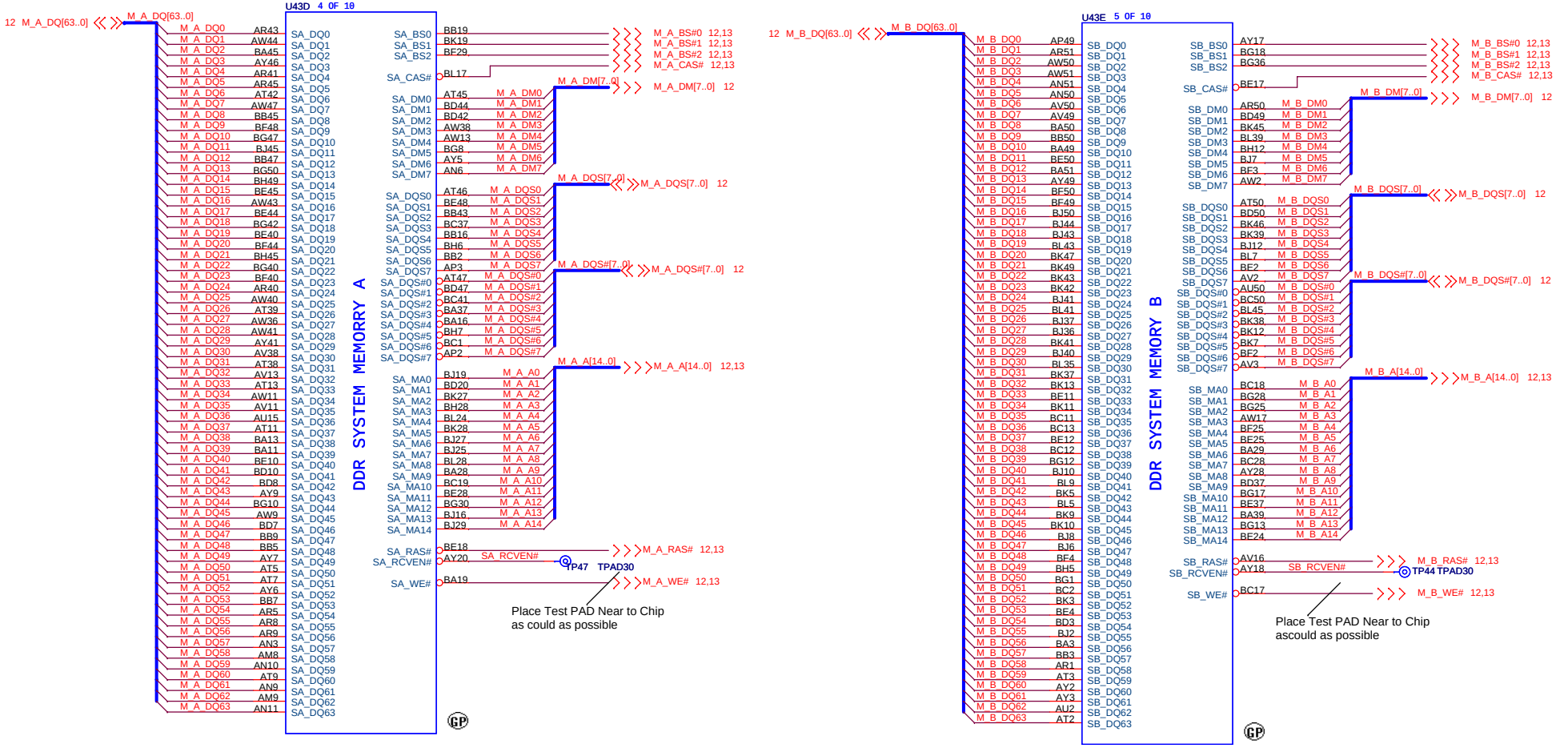

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Title: **GMCH (3 of 6)**

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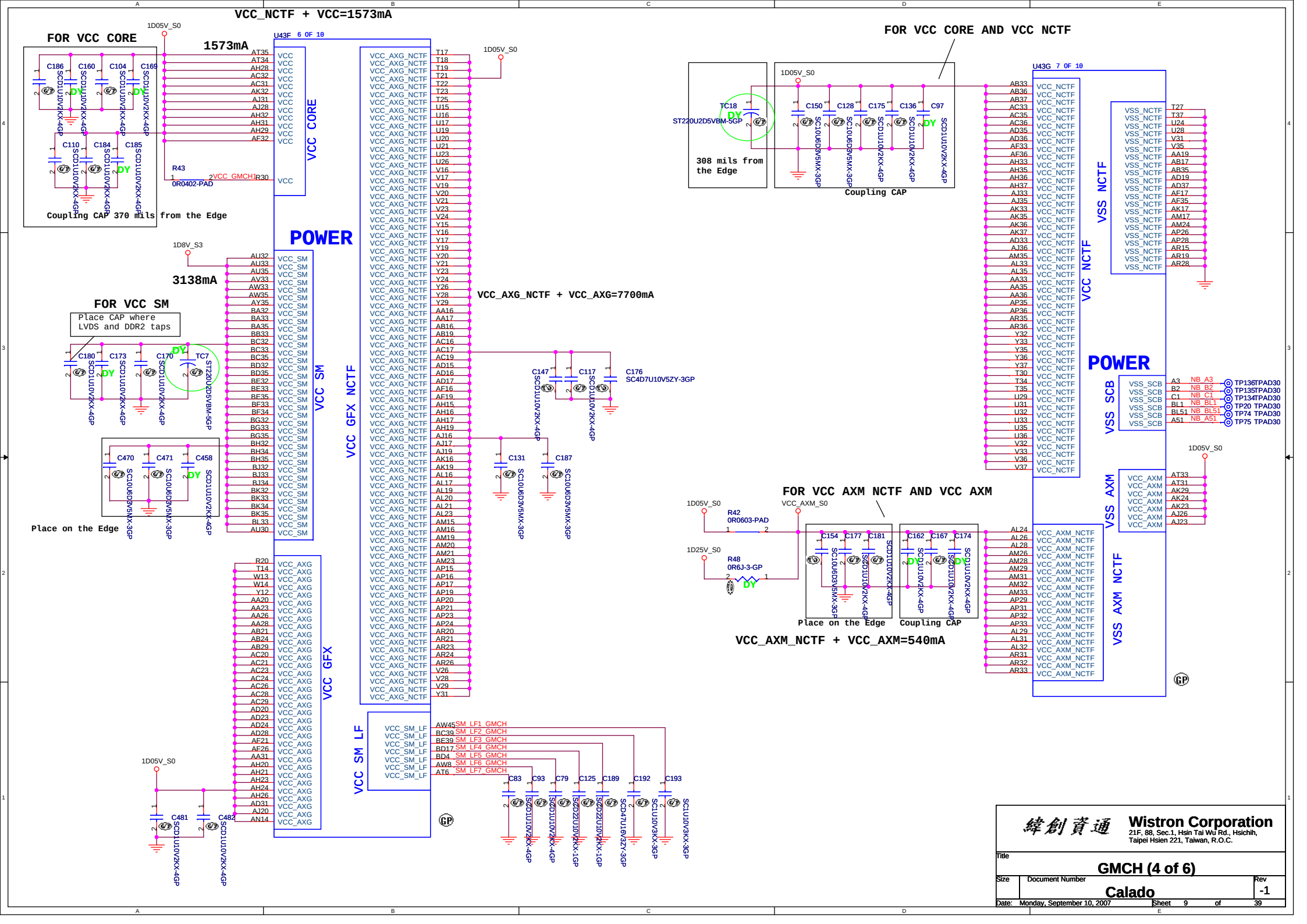
VCC_NCTF + VCC=1573mA
FOR VCC CORE
1573mA
1D05V_S0
U43F 6 OF 10
VCC CORE
Coupling CAP 370 mils from the Edge
R43
0R0402-PAD
VCC_GMCH
POWER
1D8V_S3
3138mA
FOR VCC SM
Place CAP where
LVDS and DDR2 taps
VCC SM
VCC GFX NCTF
VCC_AXG_NCTF + VCC_AXG=7700mA
Place on the Edge
VCC GFX
VCC SM LF
FOR VCC CORE AND VCC NCTF
308 mils from
the Edge
Coupling CAP
U43G 7 OF 10
VCC NCTF
VSS NCTF
POWER
VSS SCB
VSS AXM
VSS AXM NCTF
FOR VCC AXM NCTF AND VCC AXM
VCC_AXM_S0
Place on the Edge
Coupling CAP
VCC_AXM_NCTF + VCC_AXM=540mA
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Title
GMCH (4 of 6)
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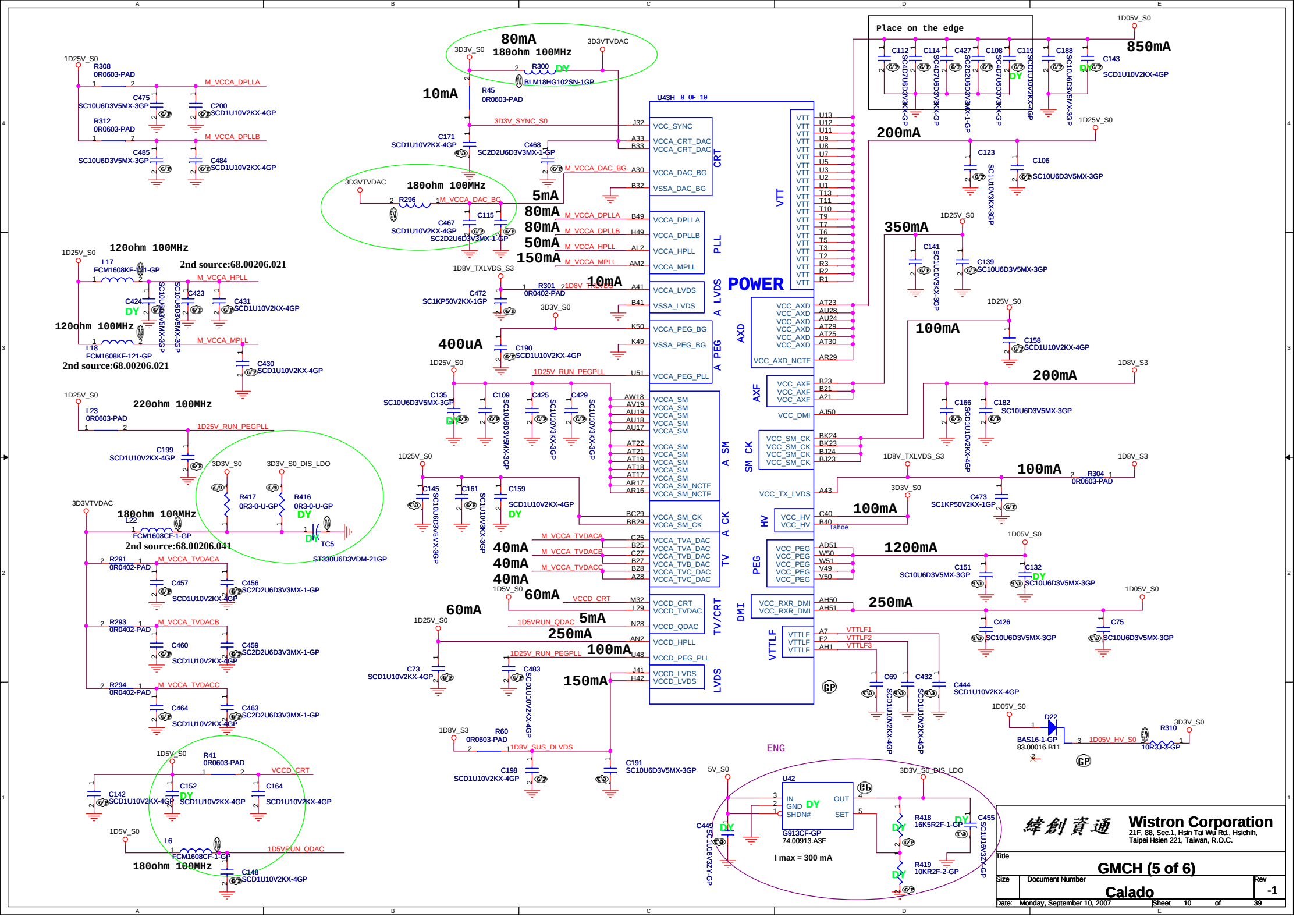
POWER
Place on the edge
80mA
180ohm 100MHz
10mA
5mA
400uA
60mA
250mA
100mA
150mA
200mA
350mA
1200mA
850mA
40mA
120ohm 100MHz
220ohm 100MHz
2nd source:68.00206.021
2nd source:68.00206.041
I max = 300 mA
ENG
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GMCH (5 of 6)
Calado
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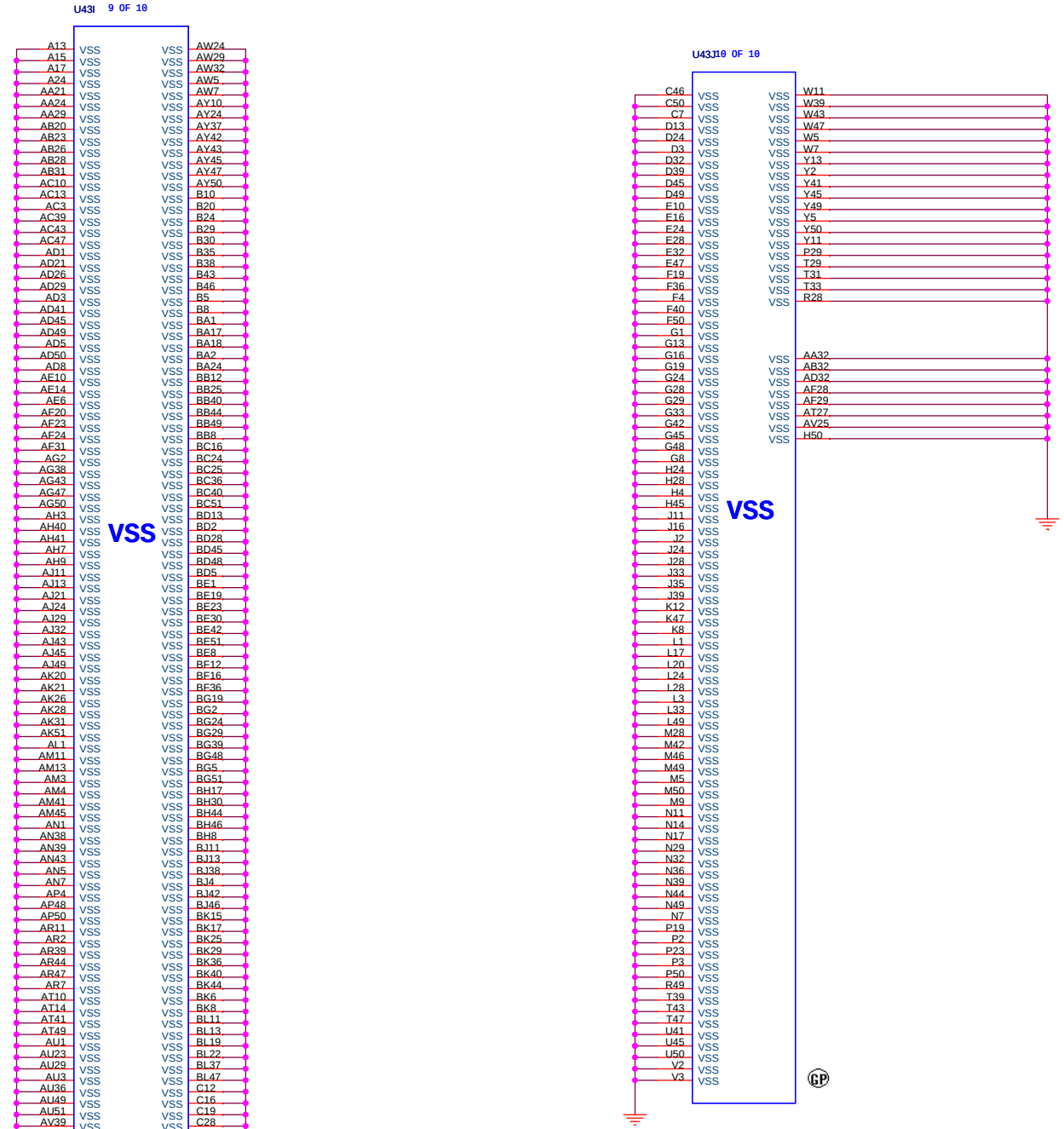

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Title: **GMCH (6 of 6)**

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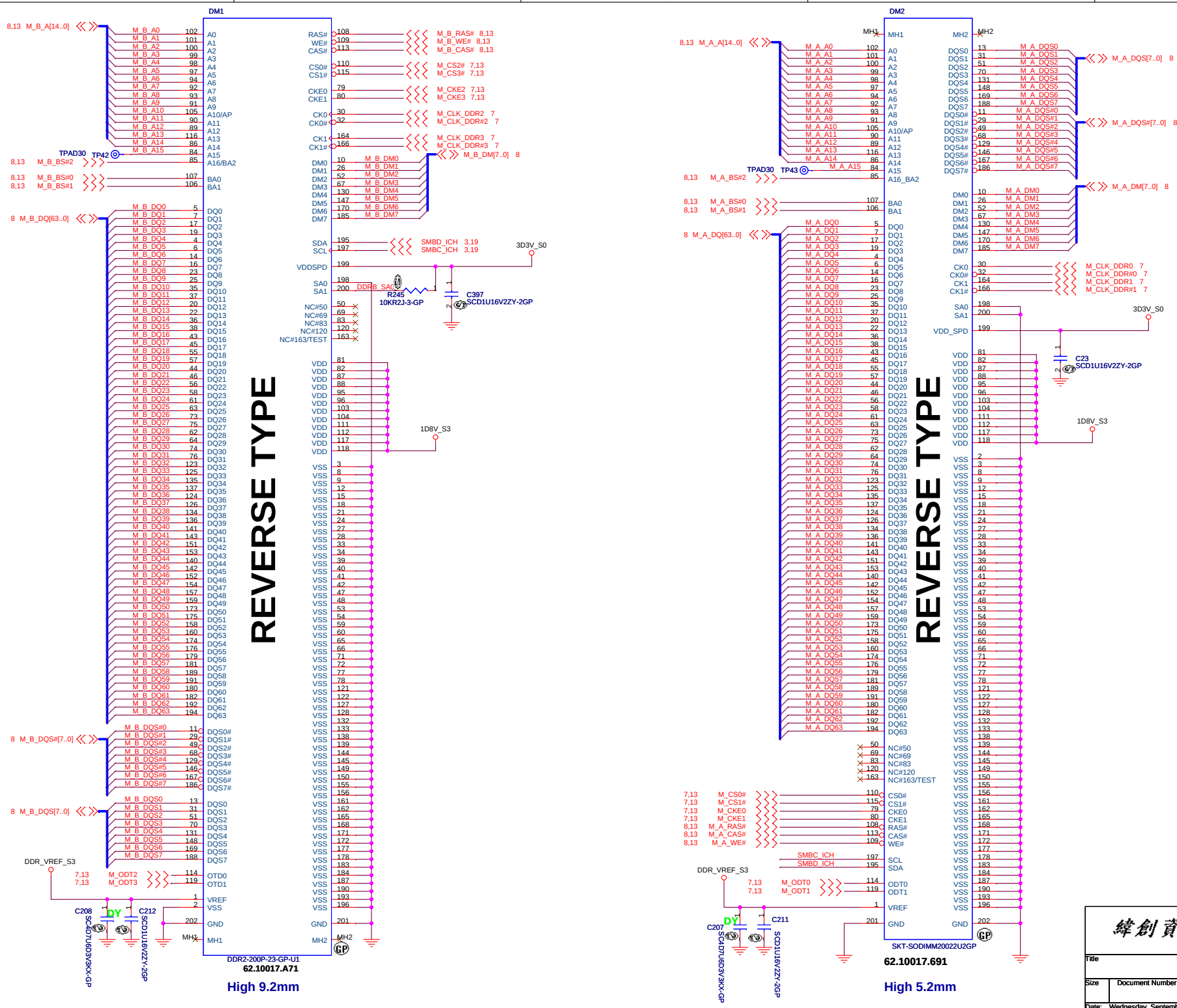

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Title: **DDR2 Socket**

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PARALLEL TERMINATION

DDR_VREF_S0

Put decap near power(0.9V) and pull-up resistor

RN14 SRN56J-5-GP
- M_CKE0 7,12
- M_CKE1 7,12
- M_A_BS#2 8,12
- M_A_A12

RN11 SRN56J-5-GP
- M_B_A9
- M_B_A5
- M_B_A8

RN15 SRN56J-5-GP
- M_CKE2 7,12
- M_CKE3 7,12
- M_B_BS#2 8,12
- M_B_A12

RN7 SRN56J-5-GP
- M_B_A3
- M_B_A1
- M_B_A10
- M_B_WE# 8,12

RN3 SRN56J-5-GP
- M_B_A13
- M_ODT2 7,12
- M_ODT3 7,12
- M_B_RAS# 8,12

RN8 SRN56J-5-GP
- M_B_BS#1 8,12
- M_B_A2
- M_B_A0
- M_B_A4

RN12 SRN56J-5-GP
- M_B_A14
- M_B_A6
- M_B_A7
- M_B_A11

RN2 SRN56J-5-GP
- M_B_BS#0 8,12
- M_B_CAS# 8,12
- M_CS3# 7,12
- M_CS2# 7,12

RN4 SRN56J-5-GP
- M_A_A13
- M_ODT0 7,12
- M_CS0# 7,12
- M_A_RAS# 8,12

RN9 SRN56J-5-GP
- M_A_BS#1 8,12
- M_A_A2
- M_A_A0
- M_A_A4

RN5 SRN56J-5-GP
- M_A_CAS# 8,12
- M_CS1# 7,12
- M_ODT1 7,12

RN10 SRN56J-5-GP
- M_A_A9
- M_A_A8
- M_A_A5
- M_A_A3

RN13 SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11
- M_A_A14

RN6 SRN56J-5-GP
- M_A_A1
- M_A_A10
- M_A_BS#0 8,12
- M_A_WE# 8,12

M_A_A[14..0] — M_A_A[14..0] 8,12

M_B_A[14..0] — M_B_A[14..0] 8,12

Decoupling Capacitor

DDR_VREF_S0

Put decap near power(0.9V) and pull-up resistor

C71 C86 C85 C103 C88 C78 C101 C121 C70 C100 C120 — SCD1U16V2ZY-2GP

C127 C89 C105 C144 C129 C153 C96 C116 C134 C74 C130 — SCD1U16V2ZY-2GP

Place these Caps near DM1

1D8V_S3

C84 C124 C102 C95 C107 — SC2D2U6D3V3MX-1-GP

C77 C113 C118 C94 — SCD1U16V2ZY-2GS

Place these Caps near DM2

1D8V_S3

C445 C454 C72 C450 C137 — SC2D2U6D3V3MX-1-GP

C452 C80 C442 C447 — SCD1U16V2ZY-2GP

緯創資通 **Wistron Corporation**
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Title: **DDR2 Termination Resistor**

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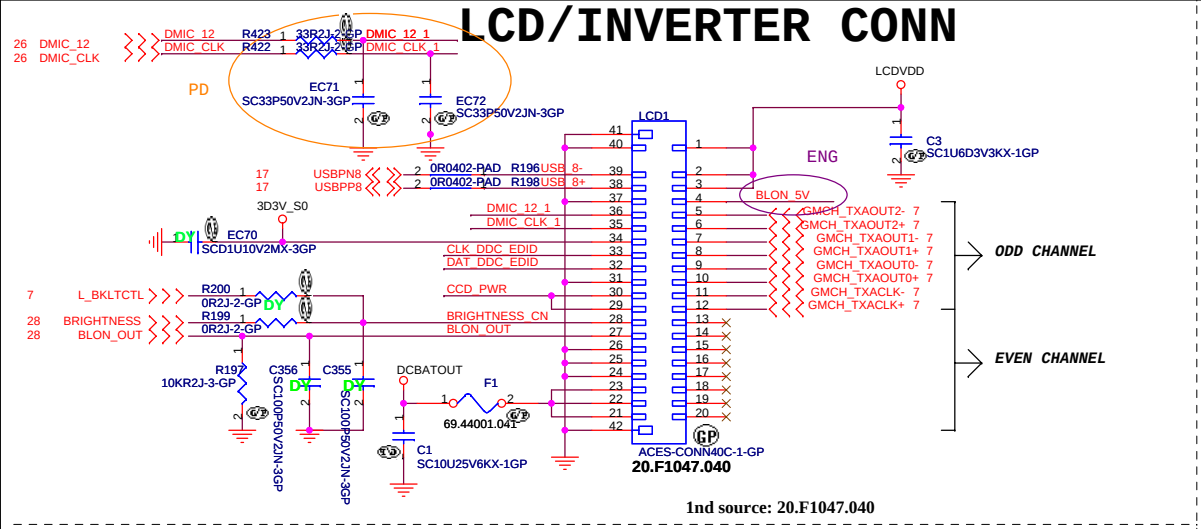
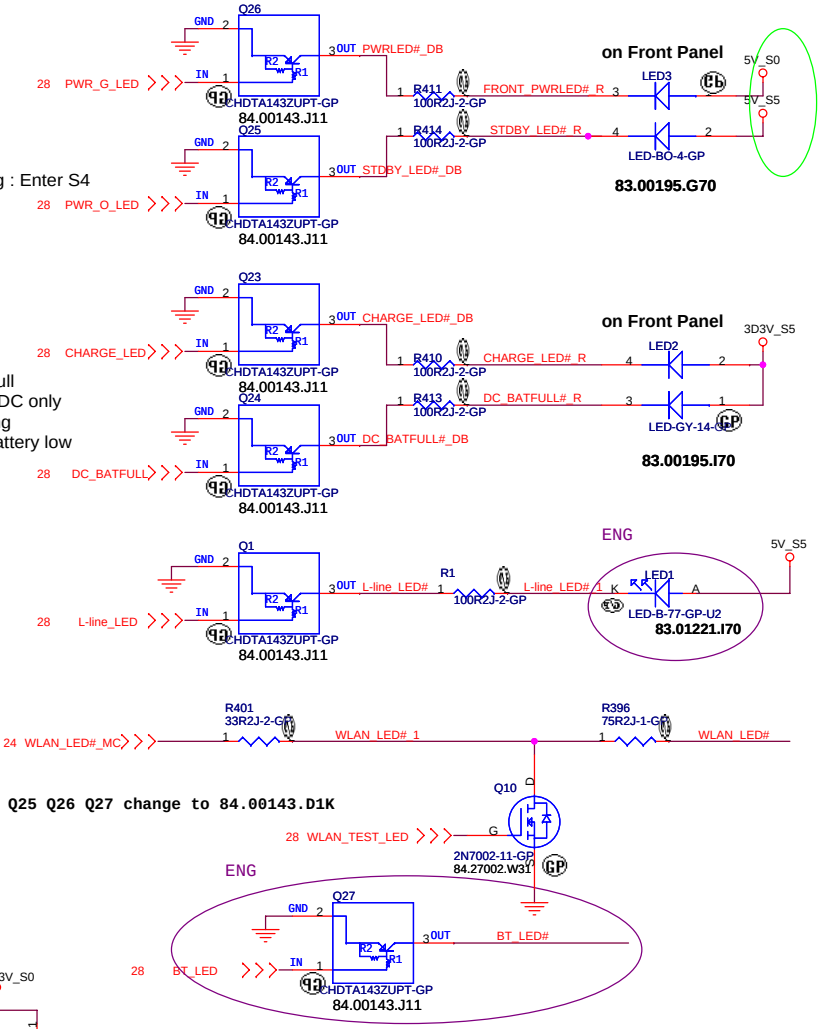
LCD/INVERTER CONN

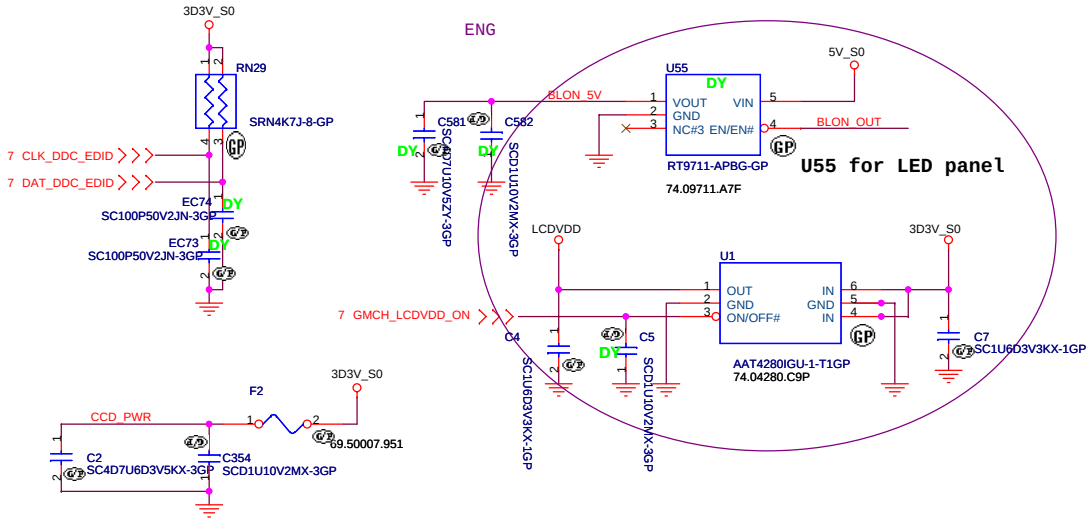


LED

Power:
BLUE : S0
Orange : S3
Orange Blinking : Enter S4

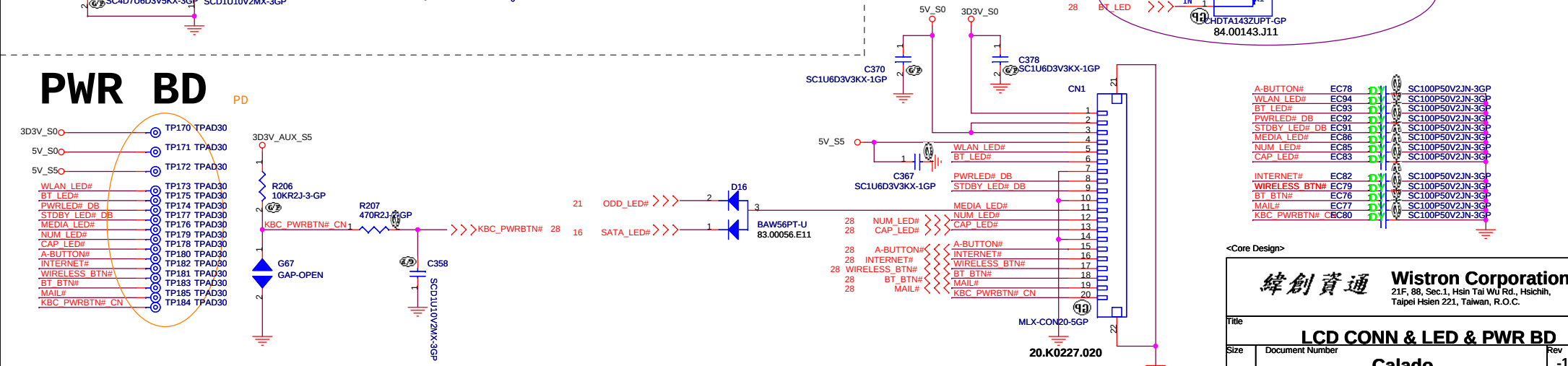
Charger:
Green: Battary Full
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low





Q1 Q23 Q24 Q25 Q26 Q27 change to 84.00143.D1K

PWR BD



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED & PWR BD

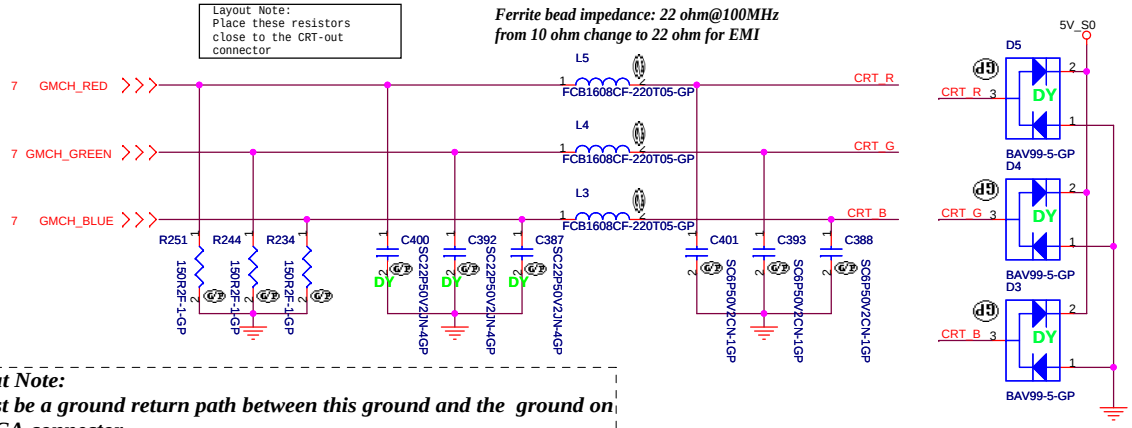
Size | Document Number: Calado | Rev: -1

Date: Wednesday, September 12, 2007 | Sheet 14 of 39

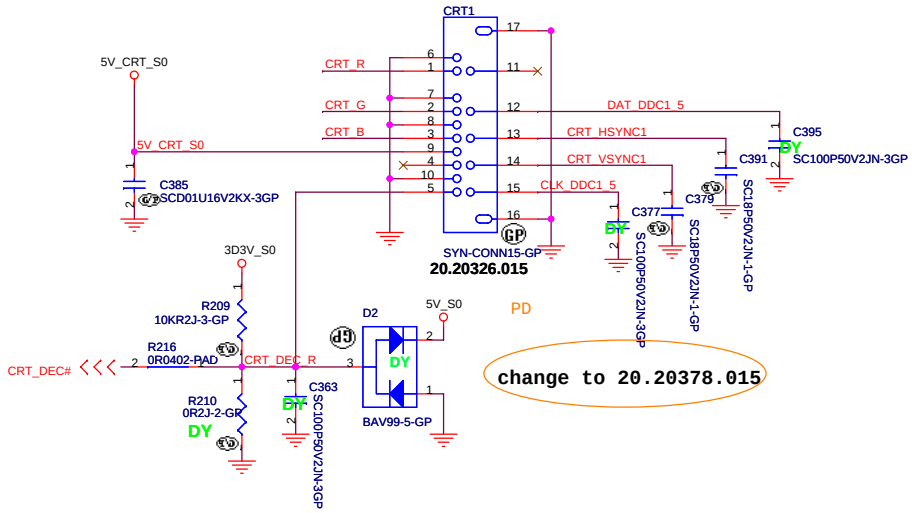
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

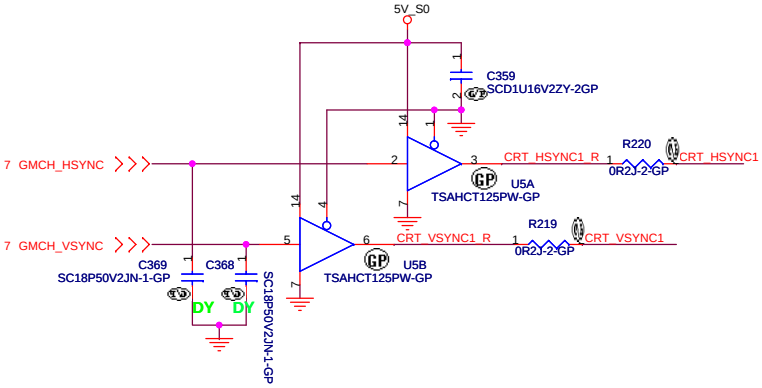
Ferrite bead impedance: 22 ohm@100MHz from 10 ohm change to 22 ohm for EMI

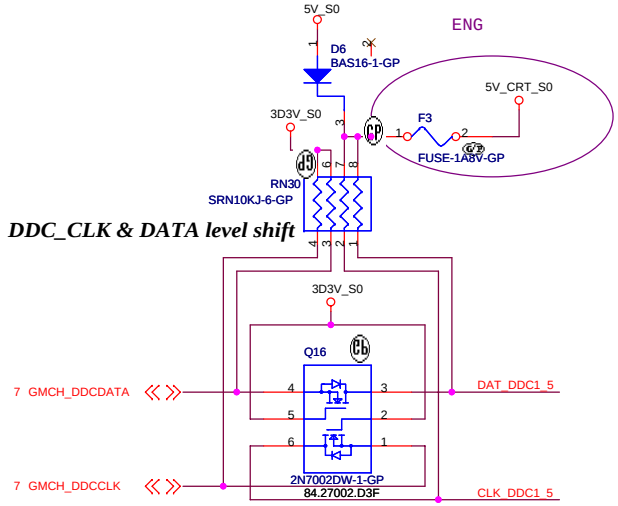


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

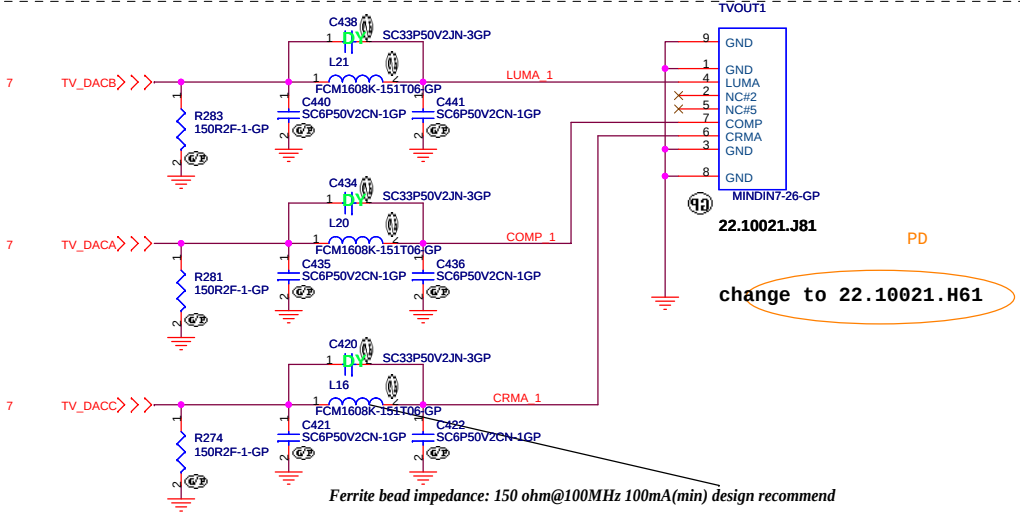


Hsync & Vsync level shift



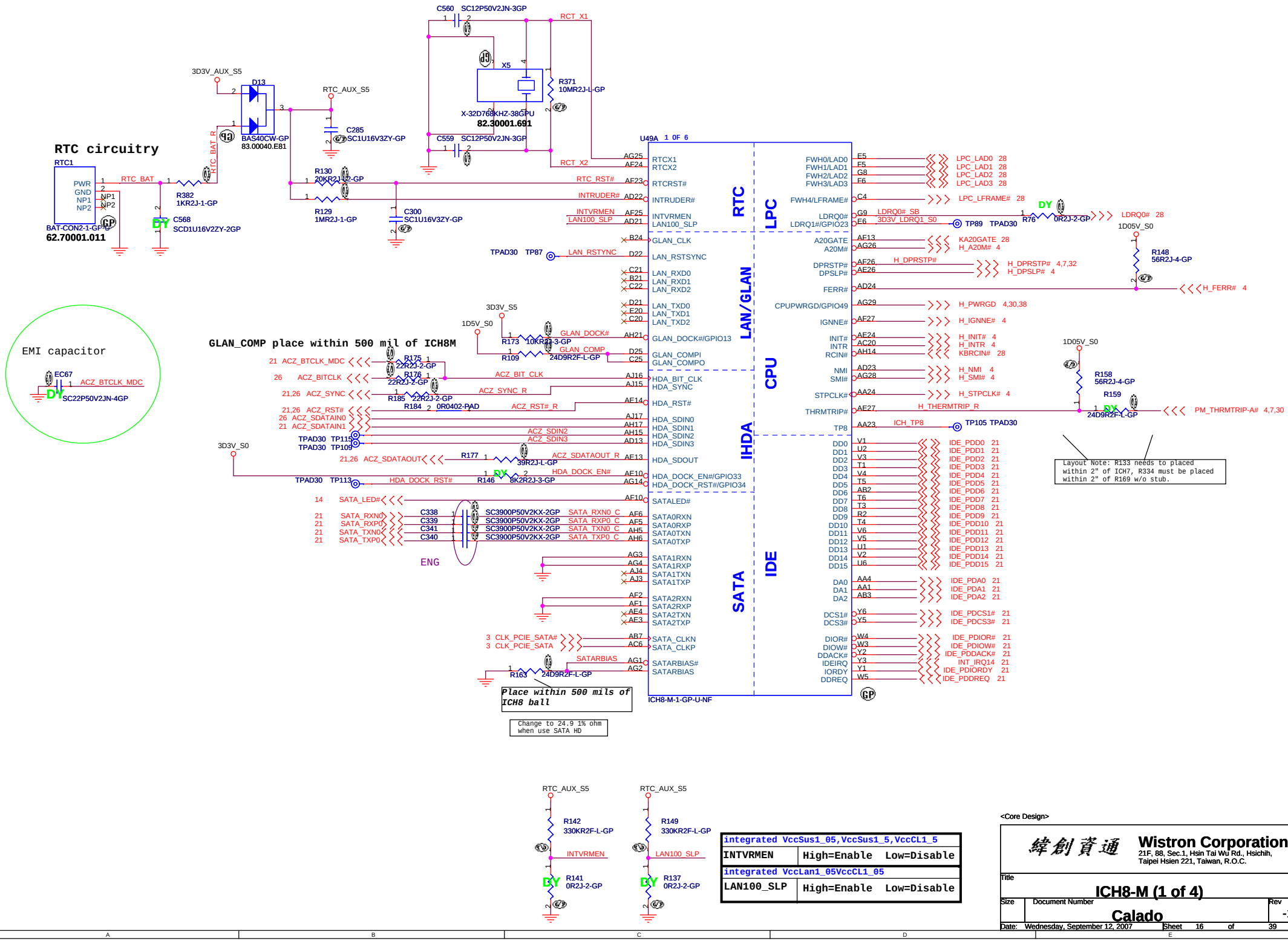


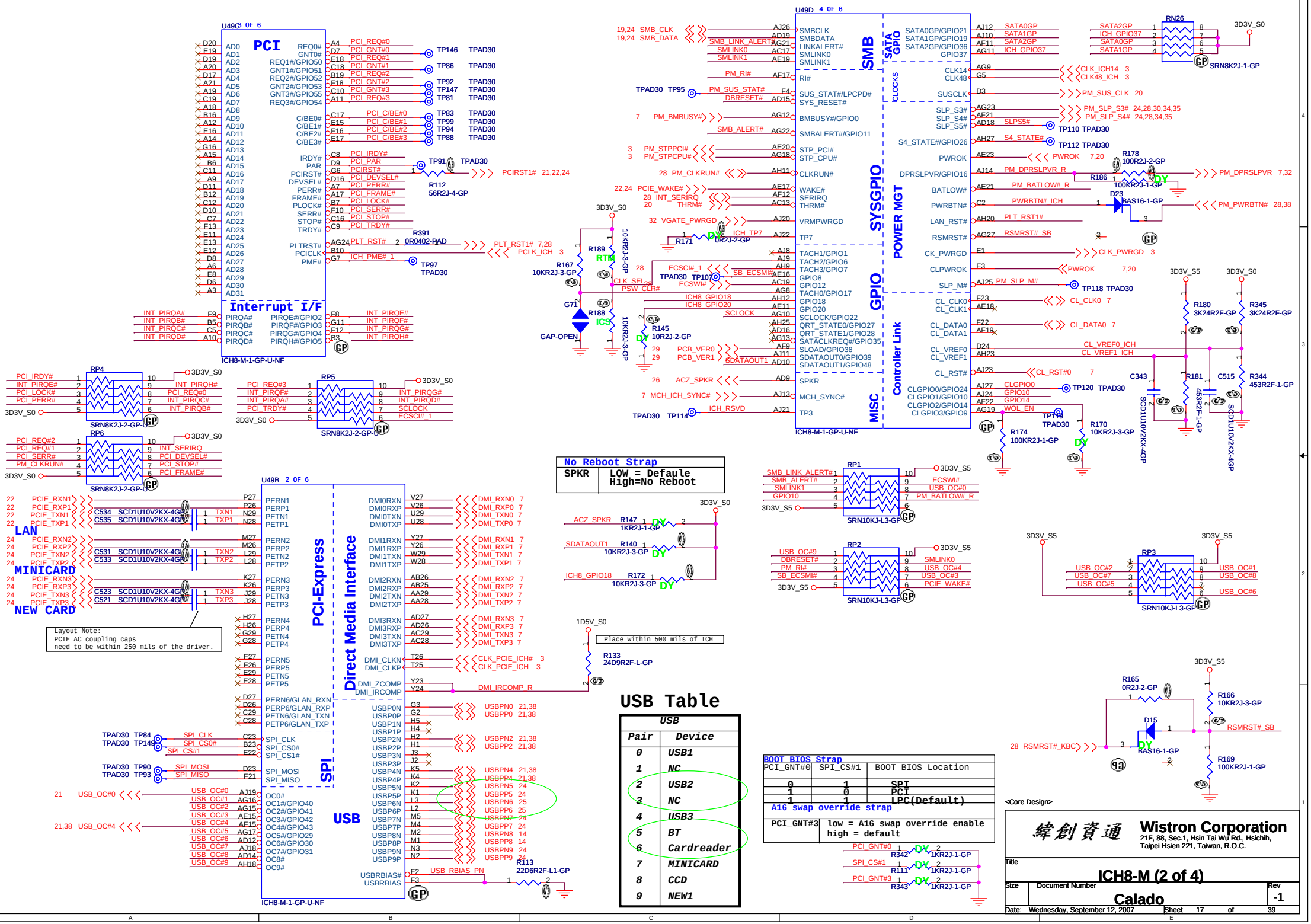
TV CONN

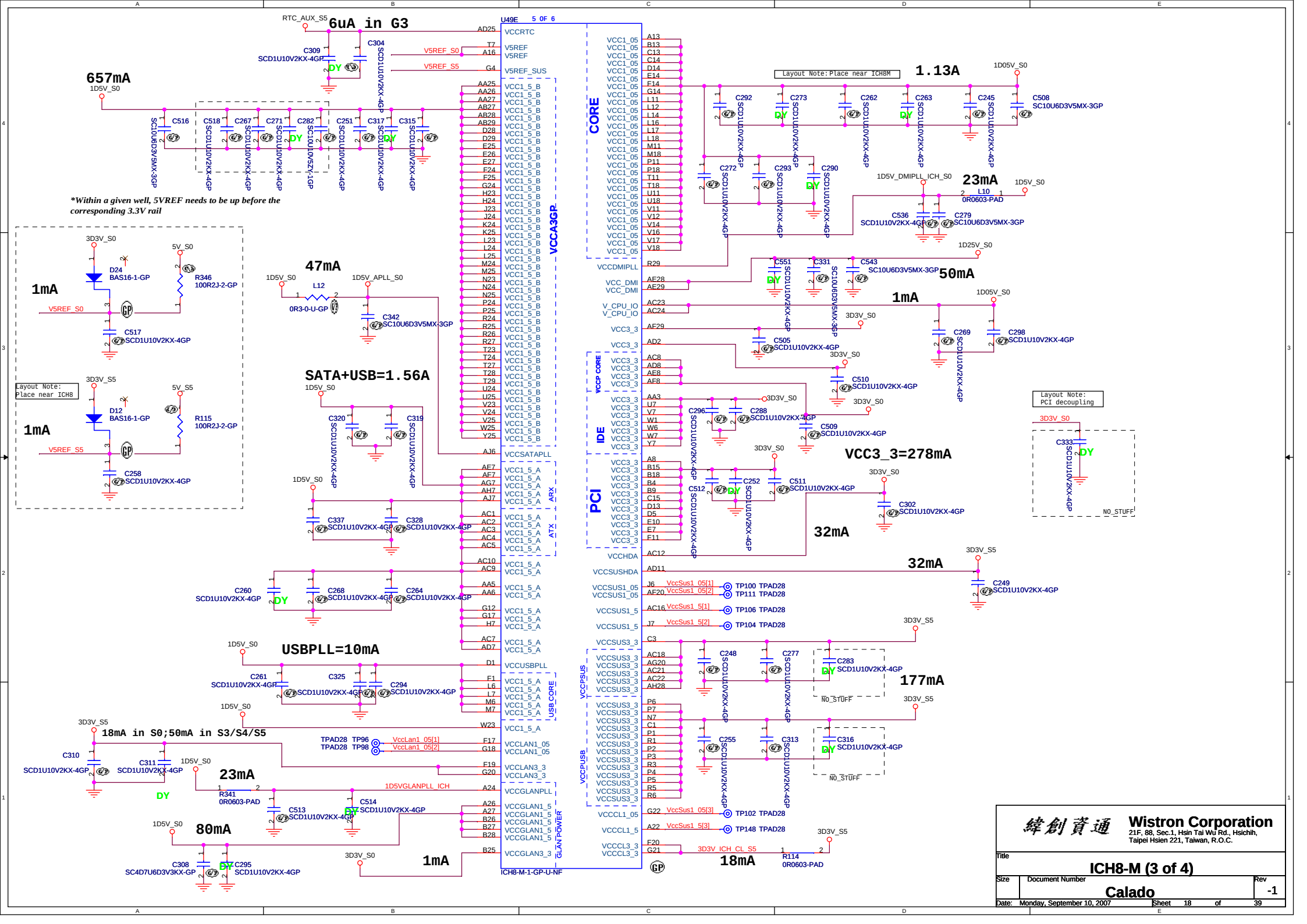


Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend

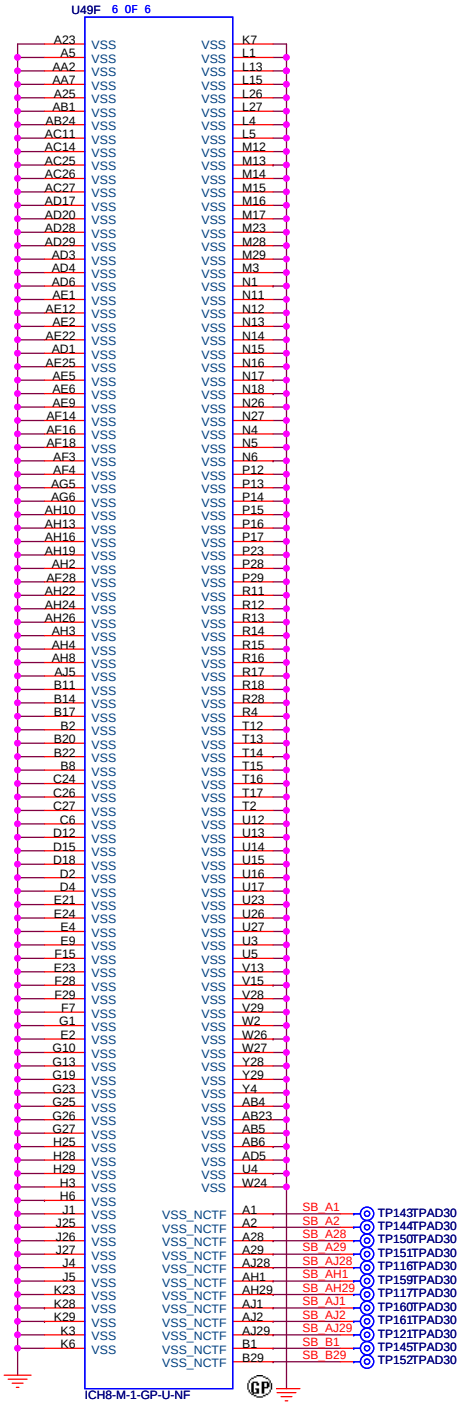
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT/TV Connector**	
Size	Document Number **Calado**	Rev -1
Date: Thursday, September 13, 2007	Sheet 15 of 39	

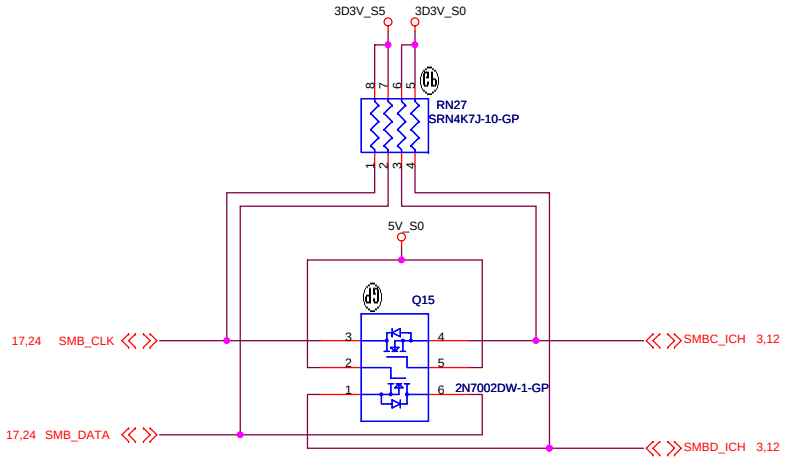

RTC circuitry
RTC1
BAT-CON2-1-GP
62.70001.011
R382 1KR2J-1-GP
C568 SCD1U16V2ZY-2GP
D13
BAS40CW-GP
83.00040.E81
C285 SC1U16V3ZY-GP
R130 20KR2J-2-GP
R129 1MR2J-1-GP
C300 SC1U16V3ZY-GP
C560 SC12P50V2JN-3GP
C559 SC12P50V2JN-3GP
X5
X-32D768KHZ-38CPU
82.30001.691
R371 10MR2J-L-GP
EMI capacitor
EC67
SC22P50V2JN-4GP
GLAN_COMP place within 500 mil of ICH8M
R175 22R2J-2-GP
R176 22R2J-2-GP
R185 22R2J-2-GP
R184 0R0402-PAD
R173 10KR2J-3-GP
R109 24D9R2F-L-GP
R177 39R2J-L-GP
R146 8K2R2J-3-GP
SC3900P50V2KX-2GP
ENG
R142 330KR2F-L-GP
R141 0R2J-2-GP
R149 330KR2F-L-GP
R137 0R2J-2-GP
R163 24D9R2F-L-GP
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
U49A 1 OF 6
RTC
LAN/GLAN
CPU
IHDA
SATA
LPC
IDE
ICH8-M-1-GP-U-NF
R76 0R2J-2-GP
TP89 TPAD30
R148 56R2J-4-GP
R158 56R2J-4-GP
R159 24D9R2F-L-GP
TP105 TPAD30
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Calado
Rev
-1
Date: Wednesday, September 12, 2007
Sheet 16 of 39


U49C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U-NF
U49D 4 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U-NF
U49B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U-NF
LAN
MINICARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
Place within 500 mils of ICH
USB Table
USB
Pair Device
0 USB1
1 NC
2 USB2
3 NC
4 USB3
5 BT
6 Cardreader
7 MINICARD
8 CCD
9 NEW1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size Document Number Rev
Calado -1
Date: Wednesday, September 12, 2007 Sheet 17 of 39



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ICH8-M (3 of 4)
Size	Document Number: Calado — Rev: -1
Date: Monday, September 10, 2007	Sheet 18 of 39





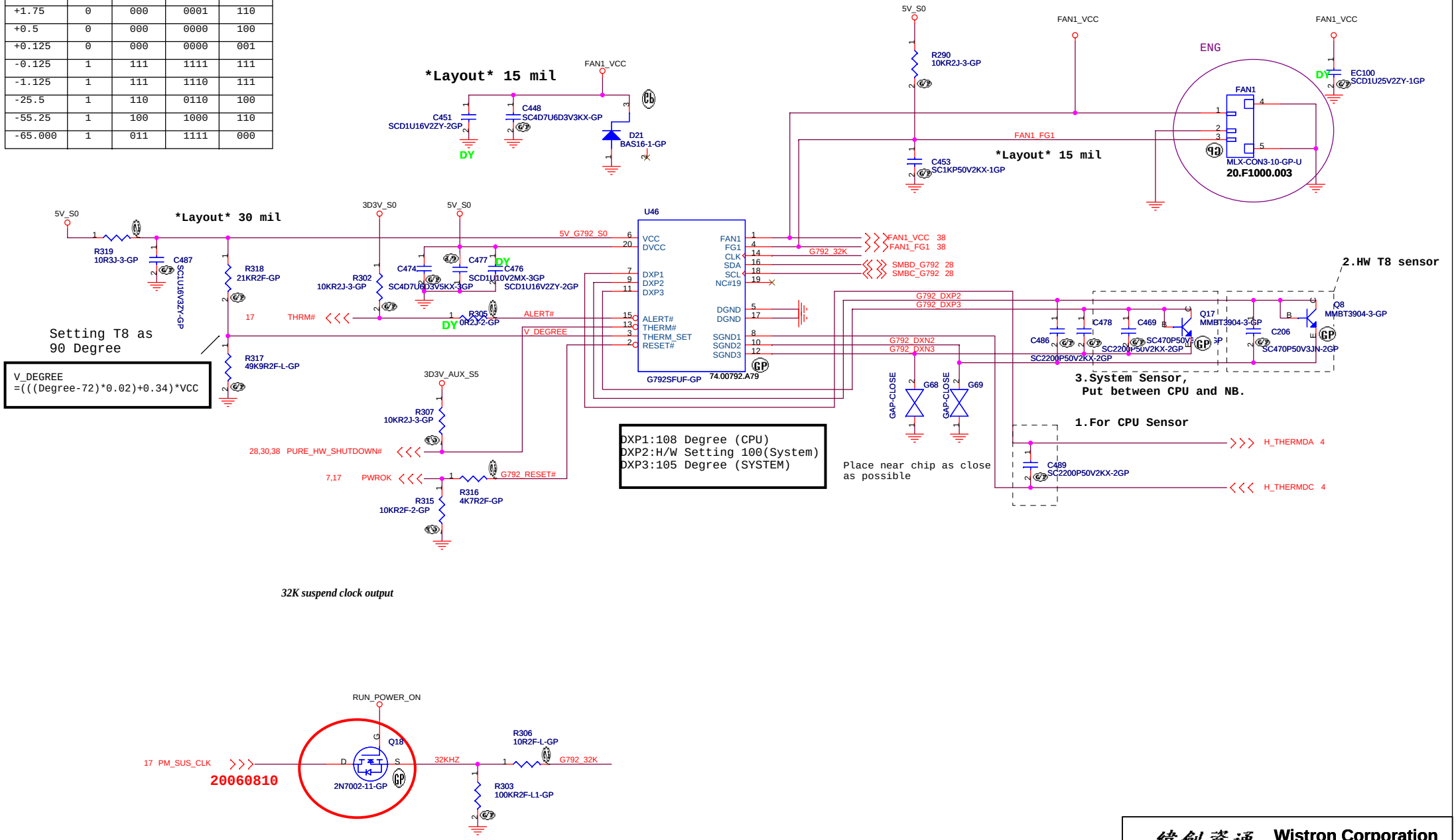
Q12 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH8-M (4 of 4)	
Size	Document Number: Calado	Rev: -1
Date: Wednesday, September 12, 2007	Sheet 19 of 39	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



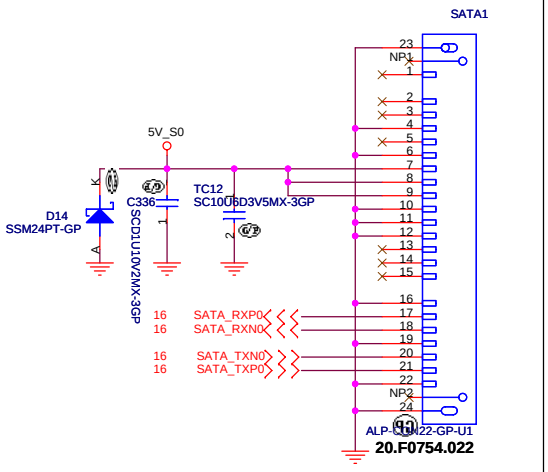
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

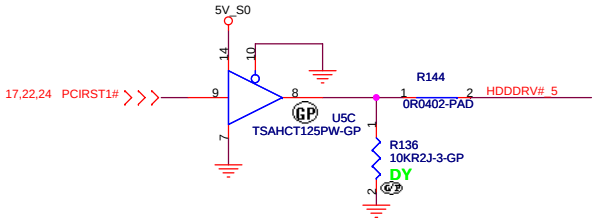
Size	Document Number	Rev
	Calado	-1

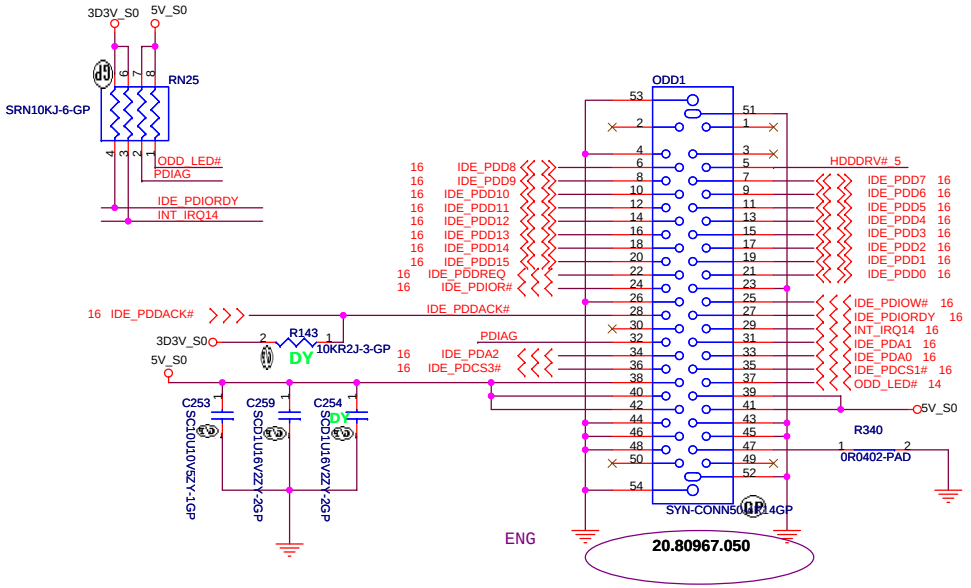
Date: Thursday, September 13, 2007 Sheet 20 of 39

SATA HD Connector

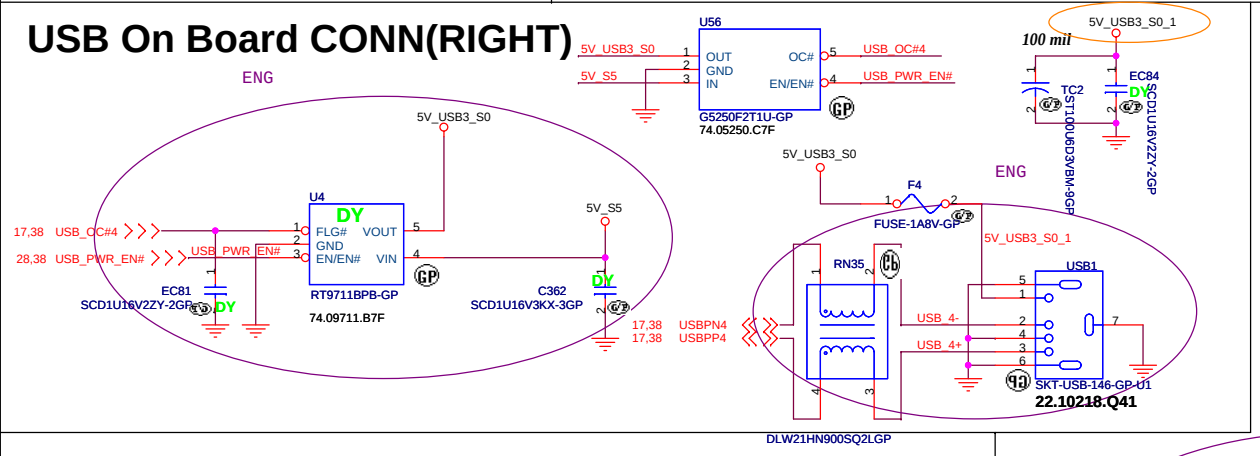


ODD Connector

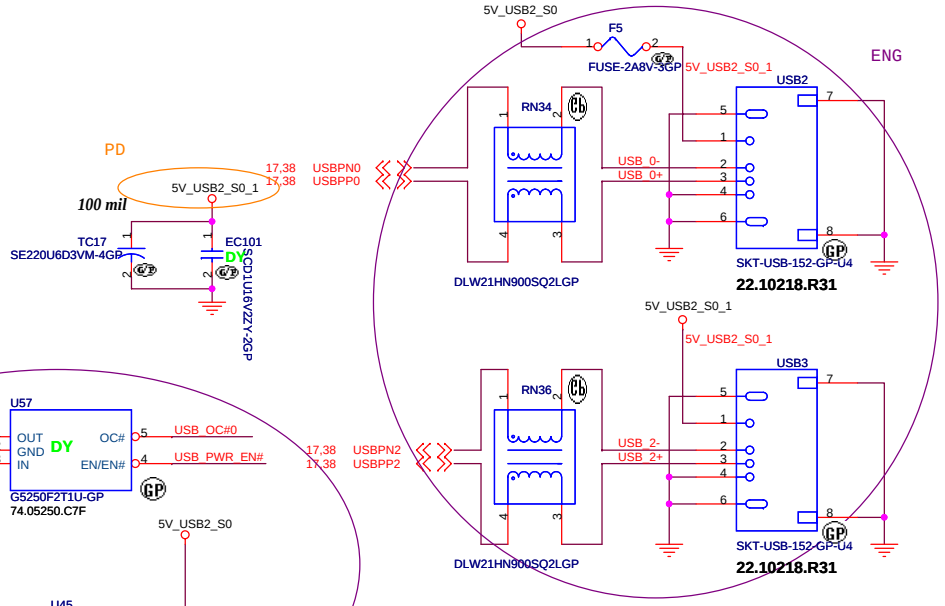




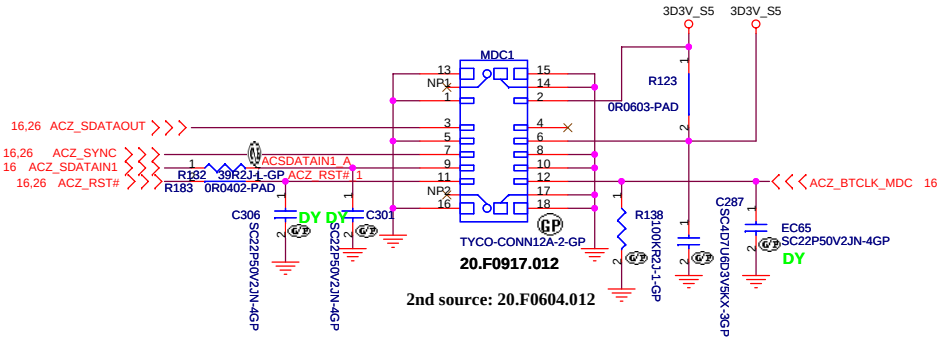
USB On Board CONN(RIGHT)

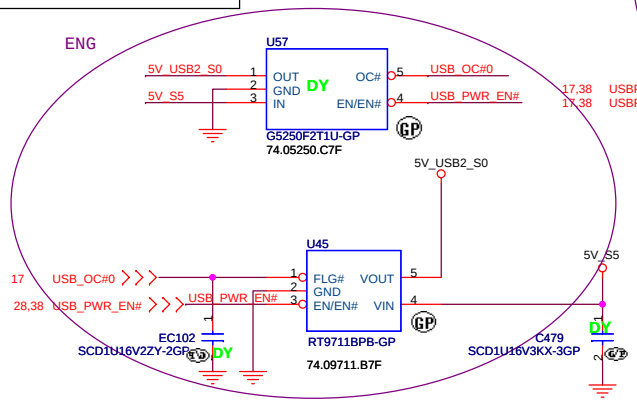


USB On Board CONN(LEFT)



MDC 1.5 CONN





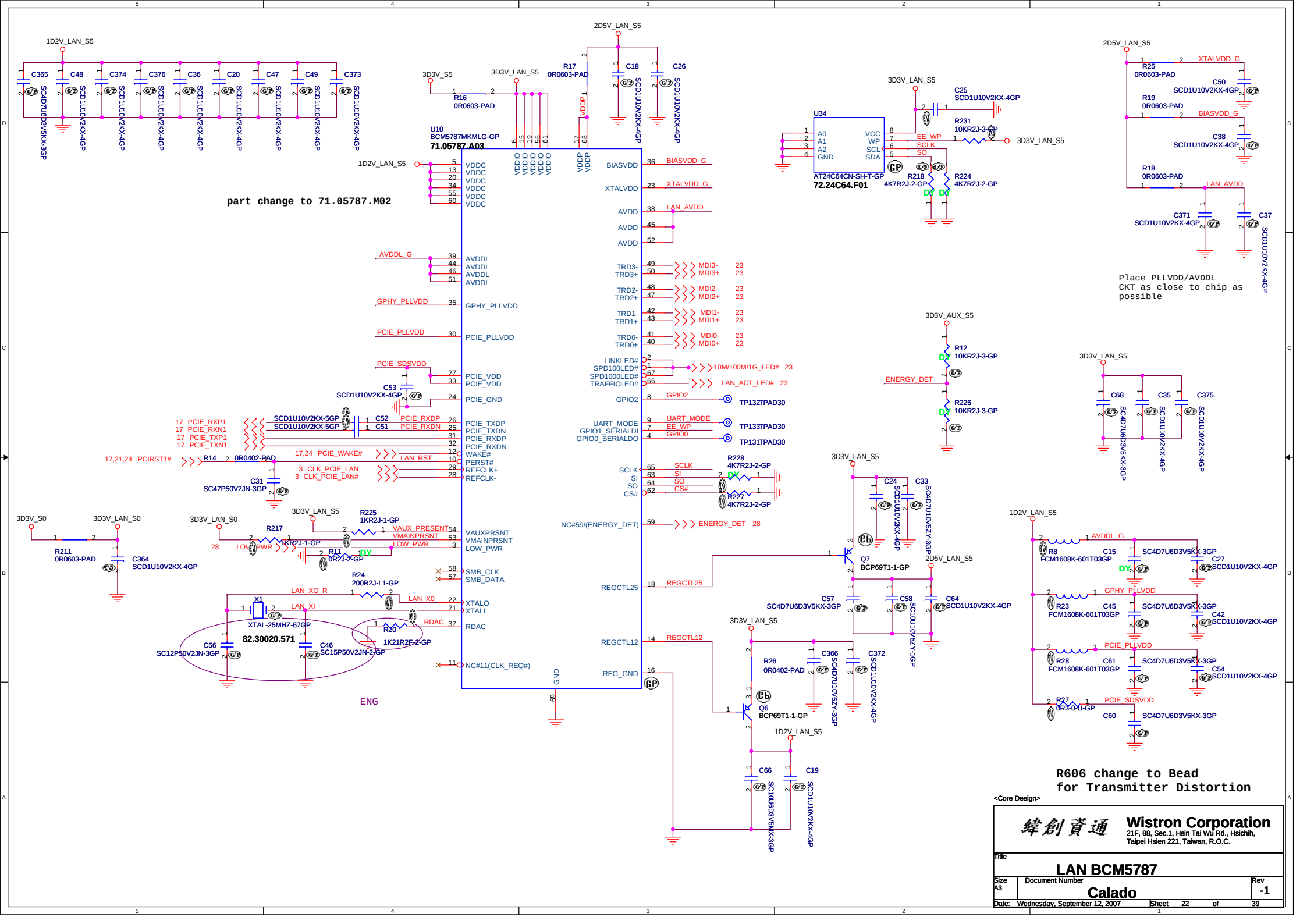
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM / USB / MDC**

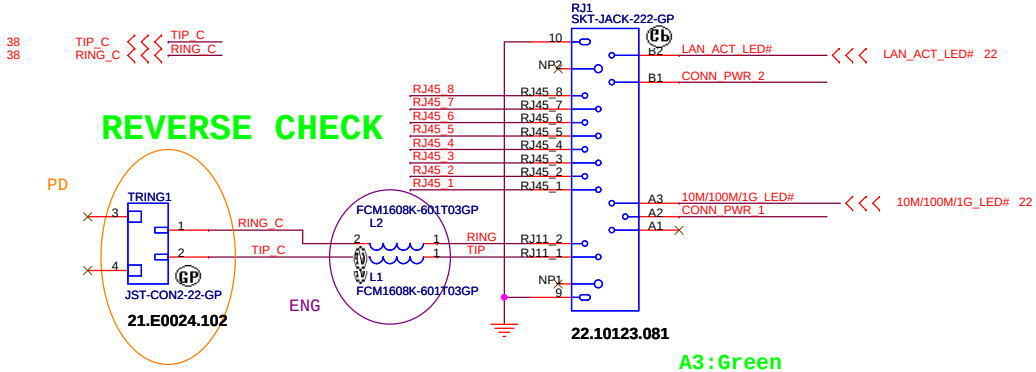
Size	Document Number	Rev
	Calado	-1

Date: Wednesday, September 12, 2007 Sheet 21 of 39


1D2V_LAN_S5
C365 SC4D7U6D3V5KX-3GP
C48 SCD1U10V2KX-4GP
C374 SCD1U10V2KX-4GP
C376 SCD1U10V2KX-4GP
C36 SCD1U10V2KX-4GP
C20 SCD1U10V2KX-4GP
C47 SCD1U10V2KX-4GP
C49 SCD1U10V2KX-4GP
C373 SCD1U10V2KX-4GP
2D5V_LAN_S5
3D3V_S5
3D3V_LAN_S5
R16 0R0603-PAD
R17 0R0603-PAD
C18 SCD1U10V2KX-4GP
C26 SCD1U10V2KX-4GP
U10
BCM5787MKMLG-GP
71.05787.A03
part change to 71.05787.M02
VDDIO
VDDP
VDDP1
BIASVDD
XTALVDD
AVDD
AVDDL
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_VDD
PCIE_GND
PCIE_TXDP
PCIE_TXDN
PCIE_RXDP
PCIE_RXDN
WAKE#
PERST#
REFCLK+
REFCLK-
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
10M/100M/1G_LED#
LAN_ACT_LED#
GPIO2
UART_MODE
GPIO1_SERIALDI
GPIO0_SERIALDO
SCLK
SI
SO
CS#
NC#59/(ENERGY_DET)
ENERGY_DET
REGCTL25
REGCTL12
REG_GND
VAUXPRSNT
VMAINPRSNT
LOW_PWR
SMB_CLK
SMB_DATA
XTALO
XTALI
RDAC
NC#11(CLK_REQ#)
GND
17 PCIE_RXP1
17 PCIE_RXN1
17 PCIE_TXP1
17 PCIE_TXN1
17,21,24 PCIRST1#
17,24 PCIE_WAKE#
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
LAN_RST
SCD1U10V2KX-5GP
C52 PCIE_RXDP
C51 PCIE_RXDN
R14 0R0402-PAD
C31 SC47P50V2JN-3GP
C53 SCD1U10V2KX-4GP
R211 0R0603-PAD
C364 SCD1U10V2KX-4GP
R217 1KR2J-1-GP
R225 1KR2J-1-GP
R11 0R2J-2-GP
R24 200R2J-L1-GP
X1
XTAL-25MHZ-67GP
82.30020.571
C56 SC12P50V2JN-3GP
C46 SC15P50V2JN-2GP
R20 1K21R2F-2-GP
LAN_XO_R
LAN_XI
LAN_X0
ENG
U34
AT24C64CN-SH-T-GP
72.24C64.F01
A0
A1
A2
GND
VCC
WP
SCL
SDA
C25 SCD1U10V2KX-4GP
R231 10KR2J-3-GP
EE_WP
SCLK
SO
R218 4K7R2J-2-GP
R224 4K7R2J-2-GP
R25 0R0603-PAD
C50 SCD1U10V2KX-4GP
R19 0R0603-PAD
C38 SCD1U10V2KX-4GP
R18 0R0603-PAD
C371 SCD1U10V2KX-4GP
C37 SCD1U10V2KX-4GP
XTALVDD_G
BIASVDD_G
LAN_AVDD
AVDDL_G
Place PLLVDD/AVDDL
CKT as close to chip as
possible
3D3V_AUX_S5
R12 10KR2J-3-GP
R226 10KR2J-3-GP
R228 4K7R2J-2-GP
R227 4K7R2J-2-GP
C68 SC4D7U6D3V5KX-3GP
C35 SCD1U10V2KX-4GP
C375 SCD1U10V2KX-4GP
C24 SCD1U10V2KX-4GP
C33 SC4D7U10V5ZY-3GP
Q7
BCP69T1-1-GP
C57 SC4D7U6D3V5KX-3GP
C58 SC10U10V5ZY-1GP
C64 SCD1U10V2KX-4GP
R26 0R0402-PAD
C366 SC4D7U10V5ZY-3GP
C372 SCD1U10V2KX-4GP
Q6
BCP69T1-1-GP
C66 SC10U6D3V5MX-3GP
C19 SCD1U10V2KX-4GP
R8 FCM1608K-601T03GP
C15 SC4D7U6D3V5KX-3GP
C27 SCD1U10V2KX-4GP
R23 FCM1608K-601T03GP
C45 SC4D7U6D3V5KX-3GP
C42 SCD1U10V2KX-4GP
R28 FCM1608K-601T03GP
C61 SC4D7U6D3V5KX-3GP
C54 SCD1U10V2KX-4GP
R27 0R3-0-U-GP
C60 SC4D7U6D3V5KX-3GP
R606 change to Bead
for Transmitter Distortion
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN BCM5787
Size A3
Document Number
Calado
Rev -1
Date: Wednesday, September 12, 2007
Sheet 22 of 39

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

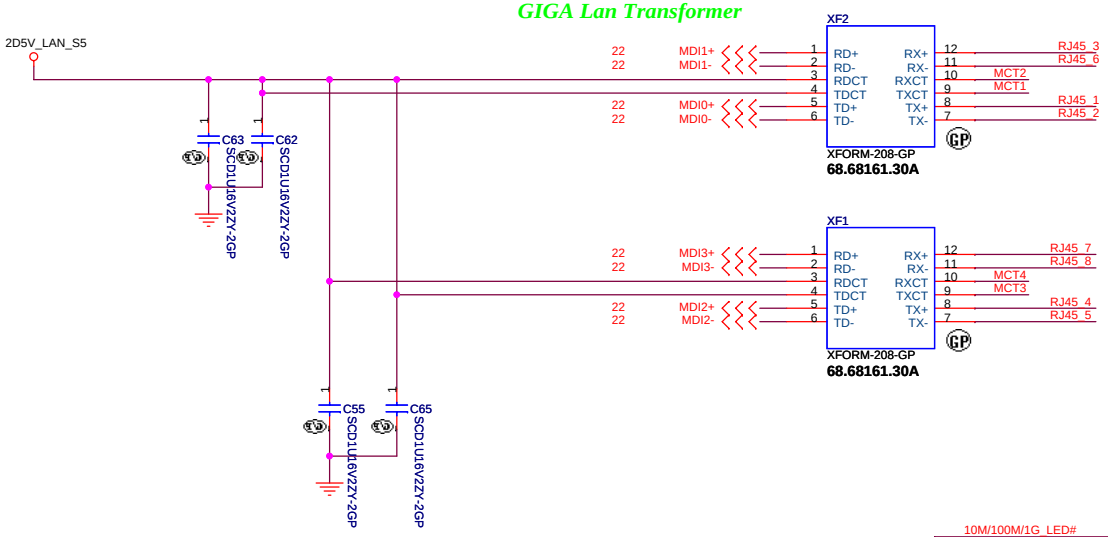


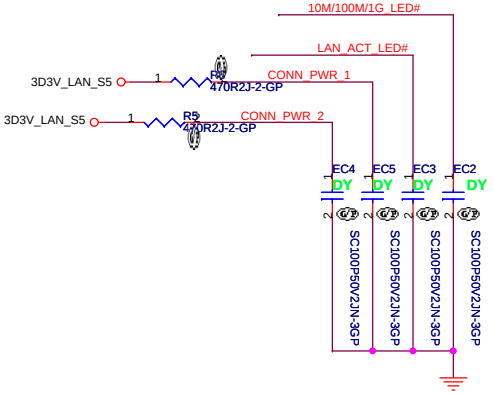
A3:Green
B2:YELLOW

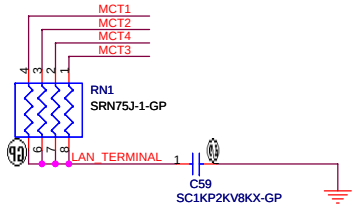
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

GIGA Lan Transformer







1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

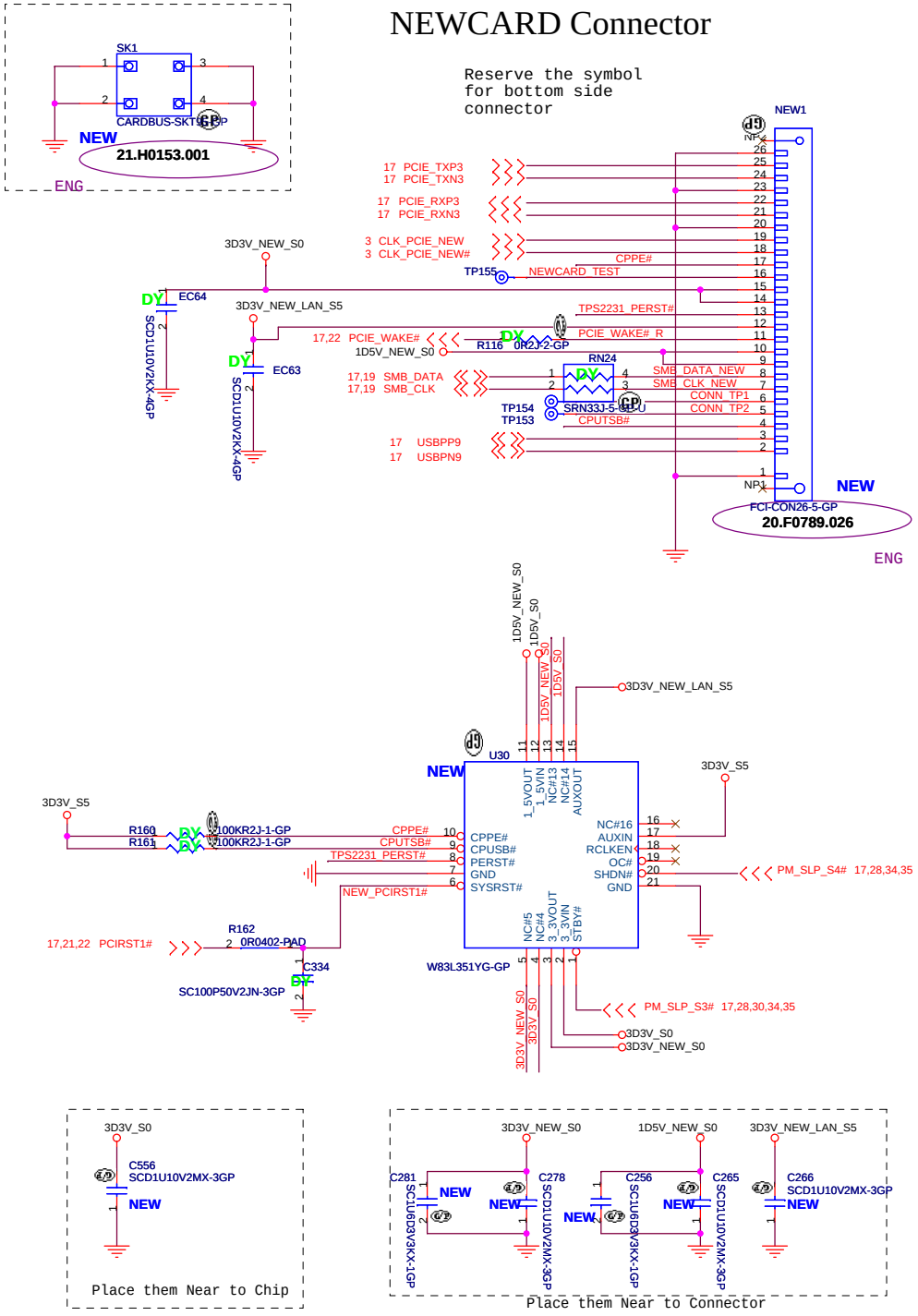
<Core Design>

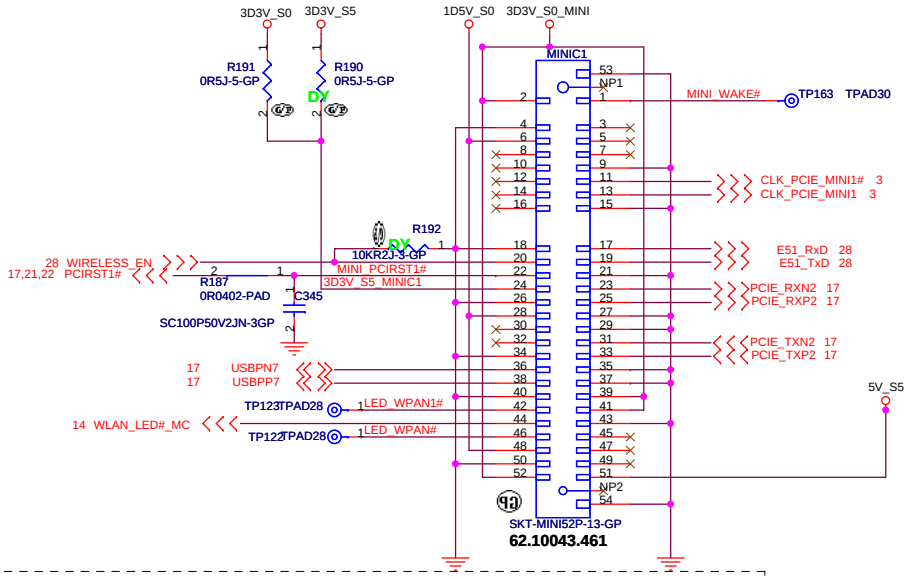
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

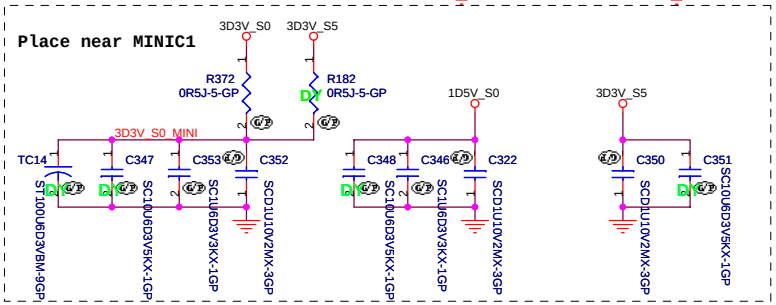
Title: LAN Connector
Size: A3
Document Number: Calado
Rev: -1
Date: Wednesday, September 12, 2007
Sheet 23 of 39

Mini Card Connector

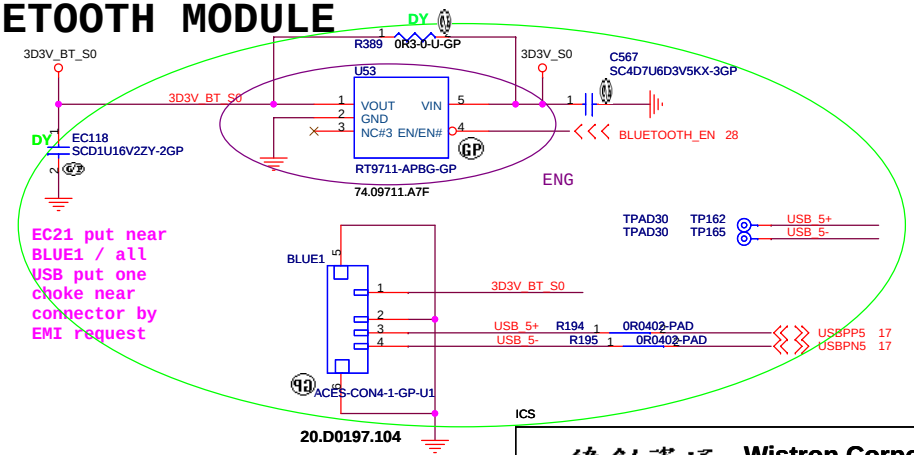
NEWCARD Connector





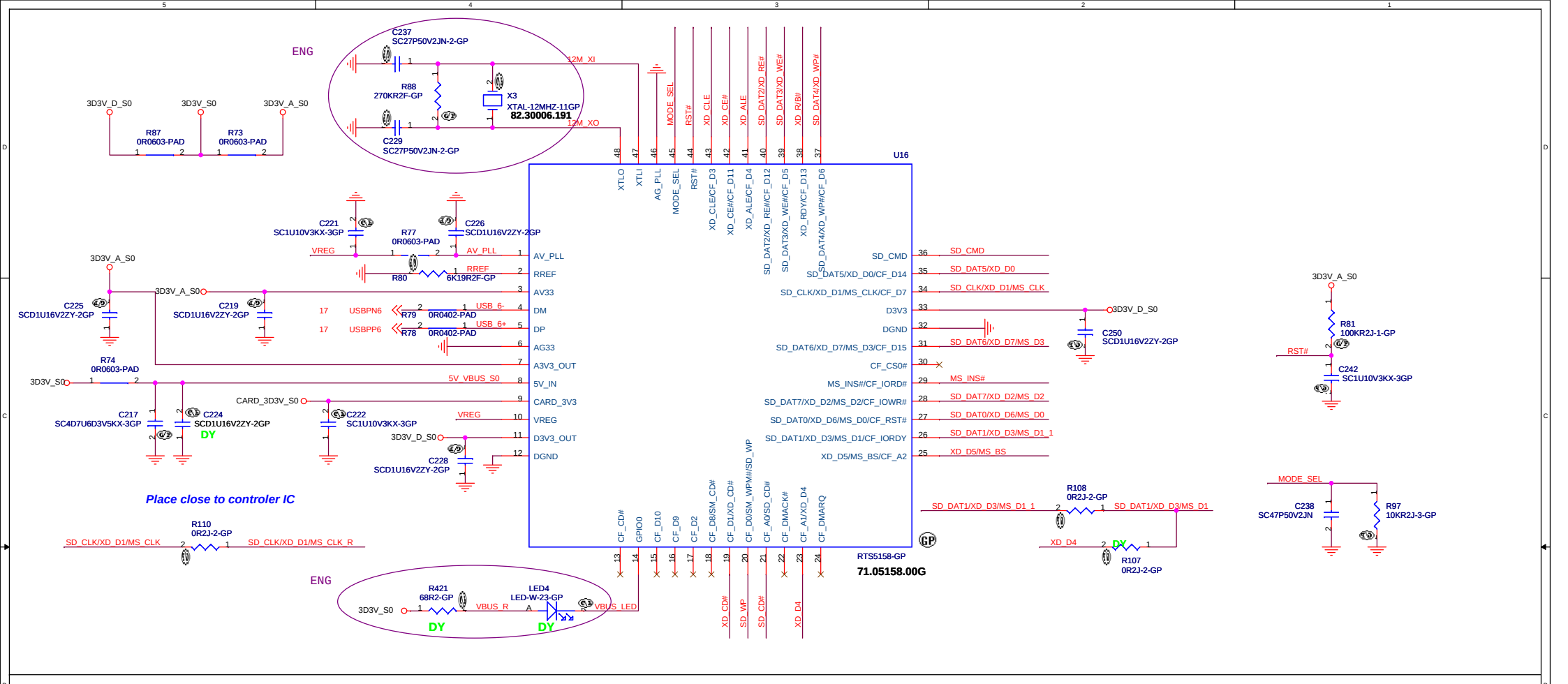


BLUETOOTH MODULE

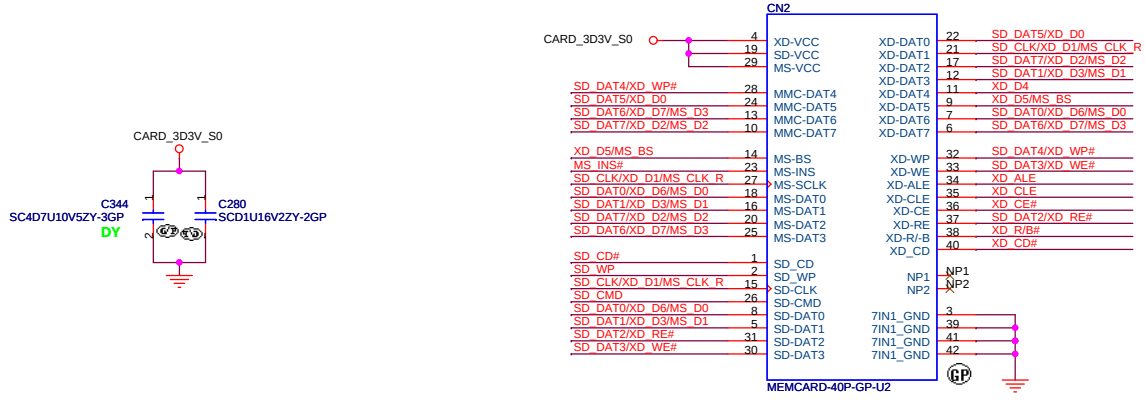


1st source:20.D0197.104
2nd source:20.F0984.004

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD / NEW CARD/BT	
Size	Document Number: Calado	Rev: -1
Date: Wednesday, September 12, 2007	Sheet 24 of 39	



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

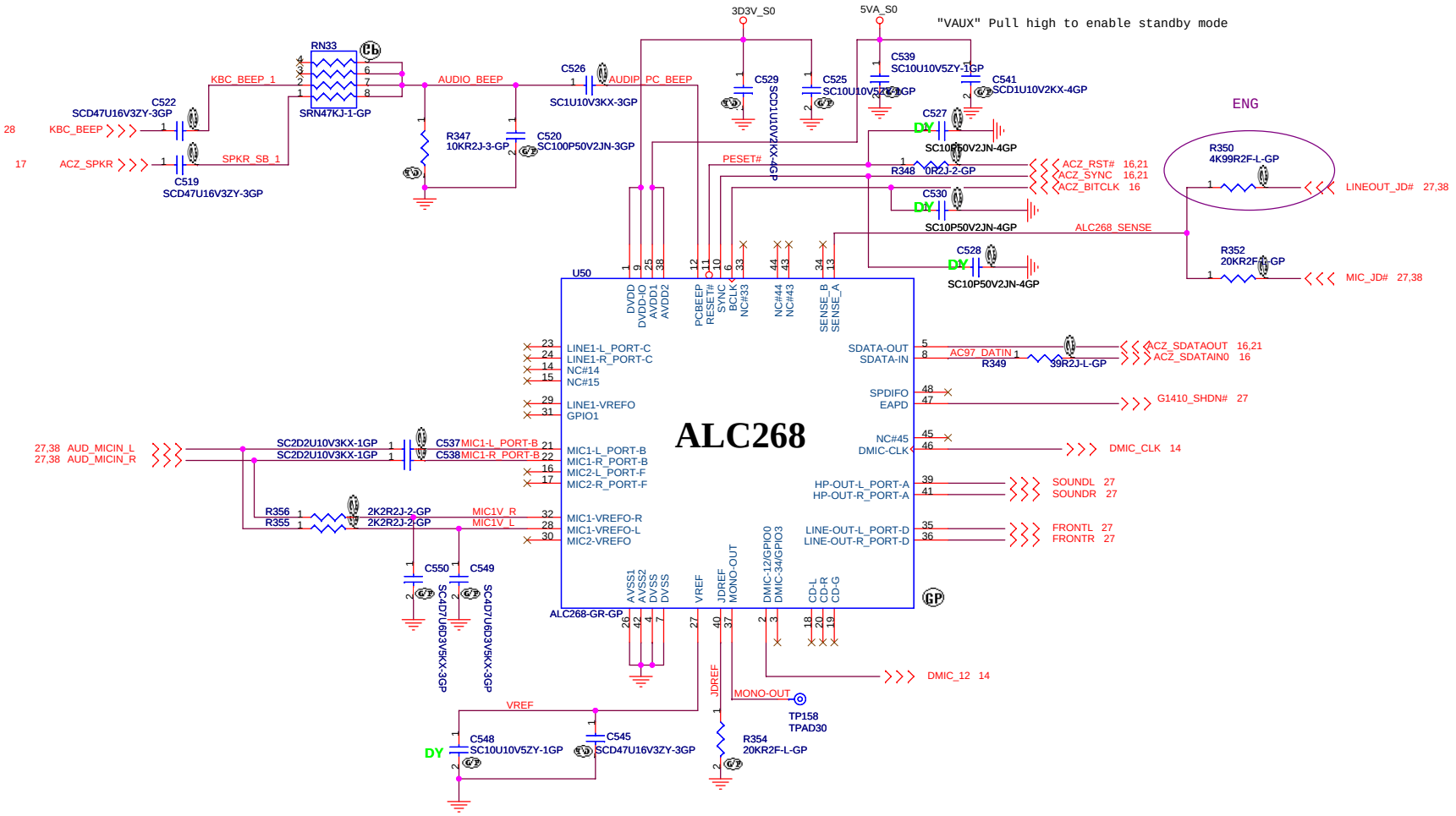


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Card Reader Controller - RTS5158

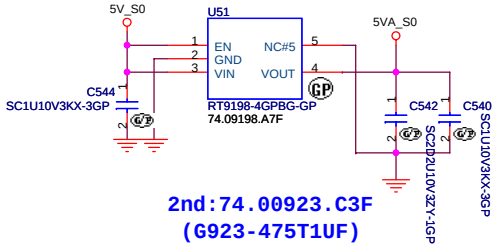
Size	Document Number	Rev
	Calado	-1

Date: Wednesday, September 12, 2007 Sheet 25 of 39



POWER GENERATE

Layout
20 mil



ICS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AZALIA CODEC - ALC268**

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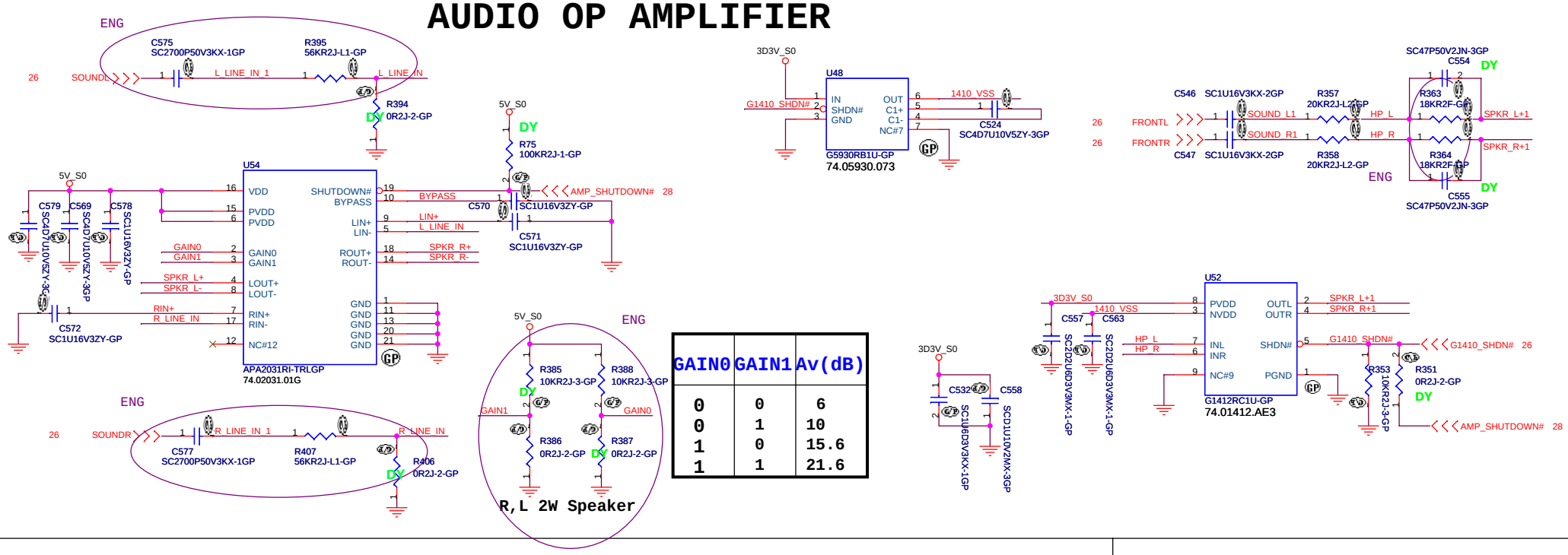
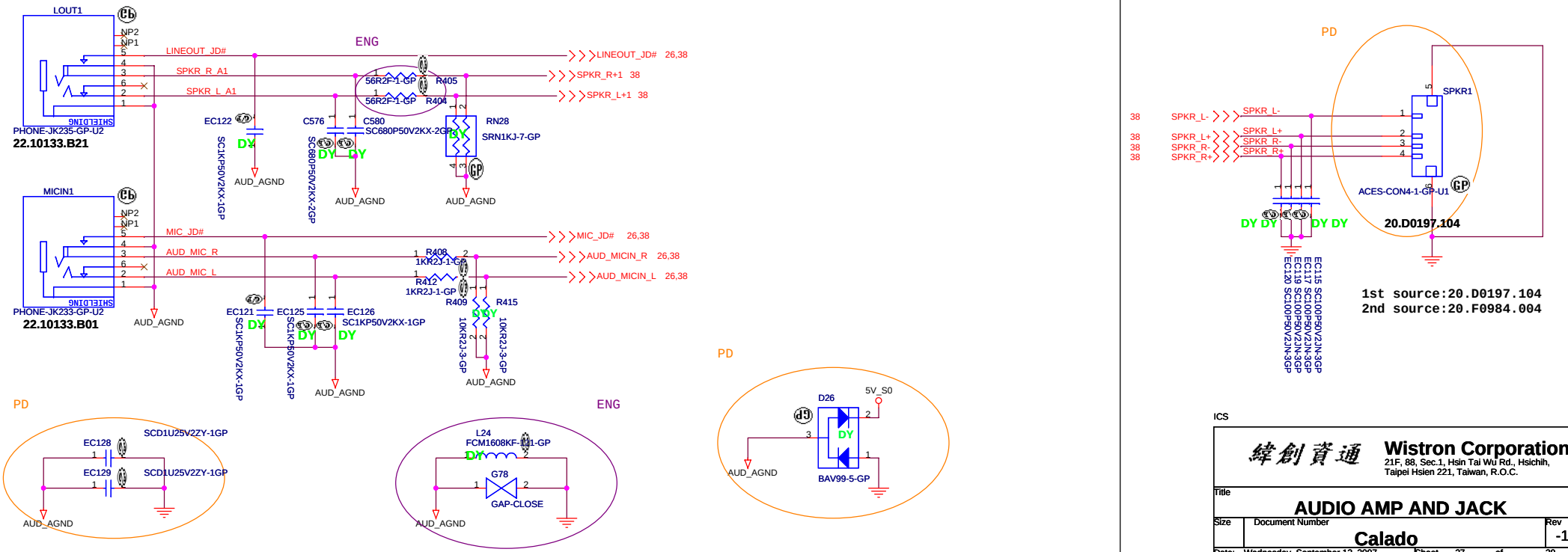
AUDIO OP AMPLIFIER



GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



Internal Speaker

1st source:20.D0197.104
2nd source:20.F0984.004

ICS

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Title: **AUDIO AMP AND JACK**

Size	Document Number	Rev
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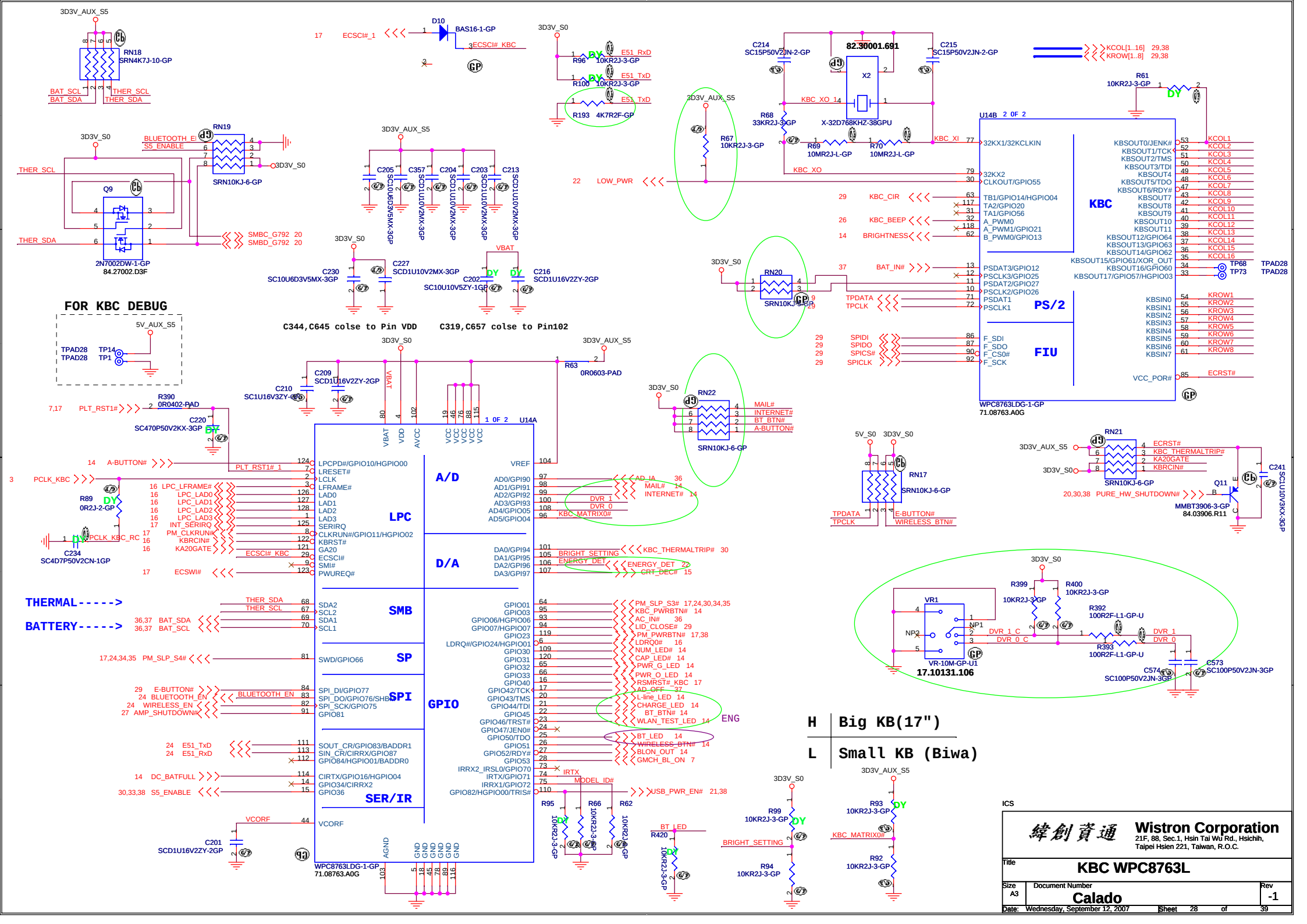
FOR KBC DEBUG
C344,C645 colse to Pin VDD
C319,C657 colse to Pin102
THERMAL----->
BATTERY----->
H | Big KB(17")
L | Small KB (Biwa)
KBC
PS/2
FIU
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
ENG
WPC8763LDG-1-GP
71.08763.A0G
82.30001.691
17.10131.106
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8763L
Calado
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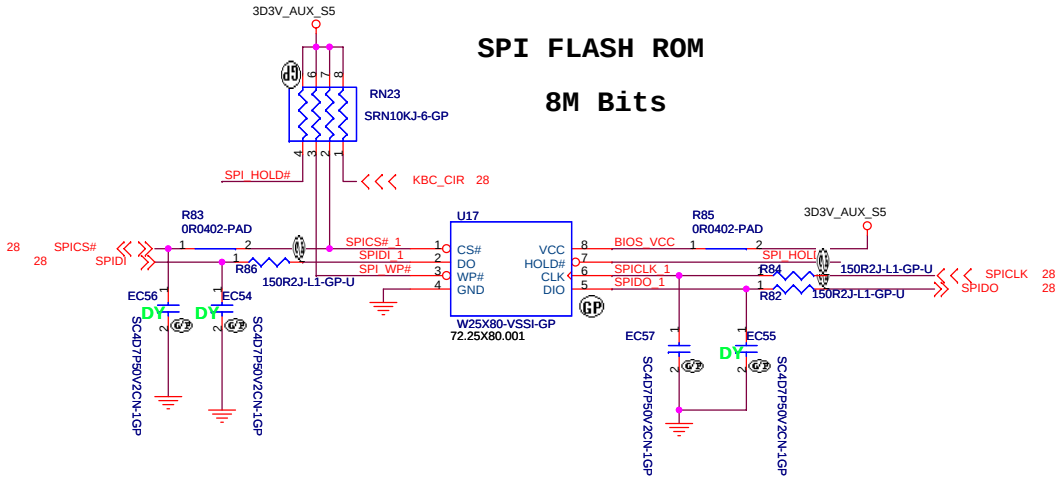

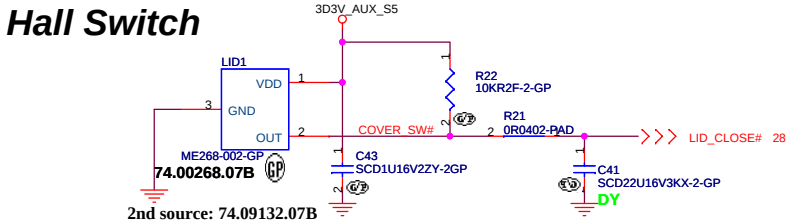

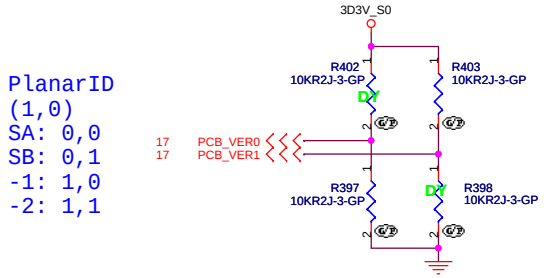

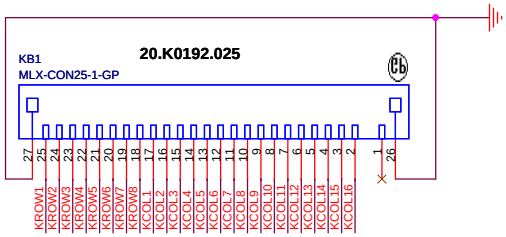

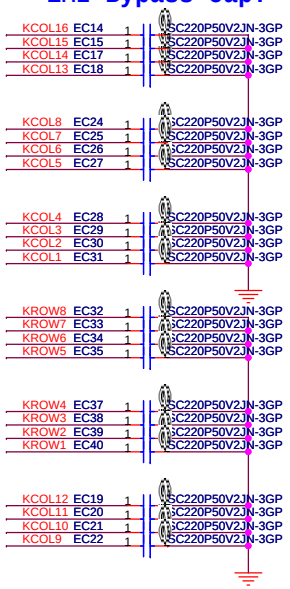

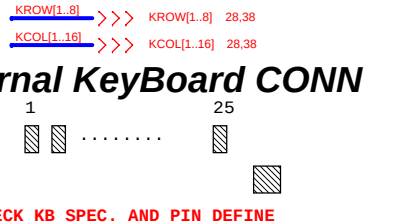

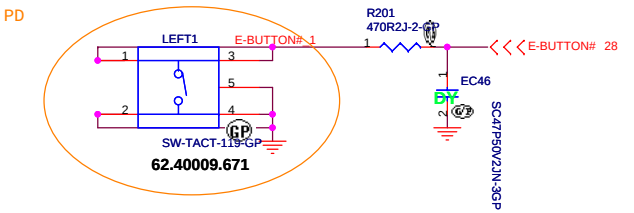

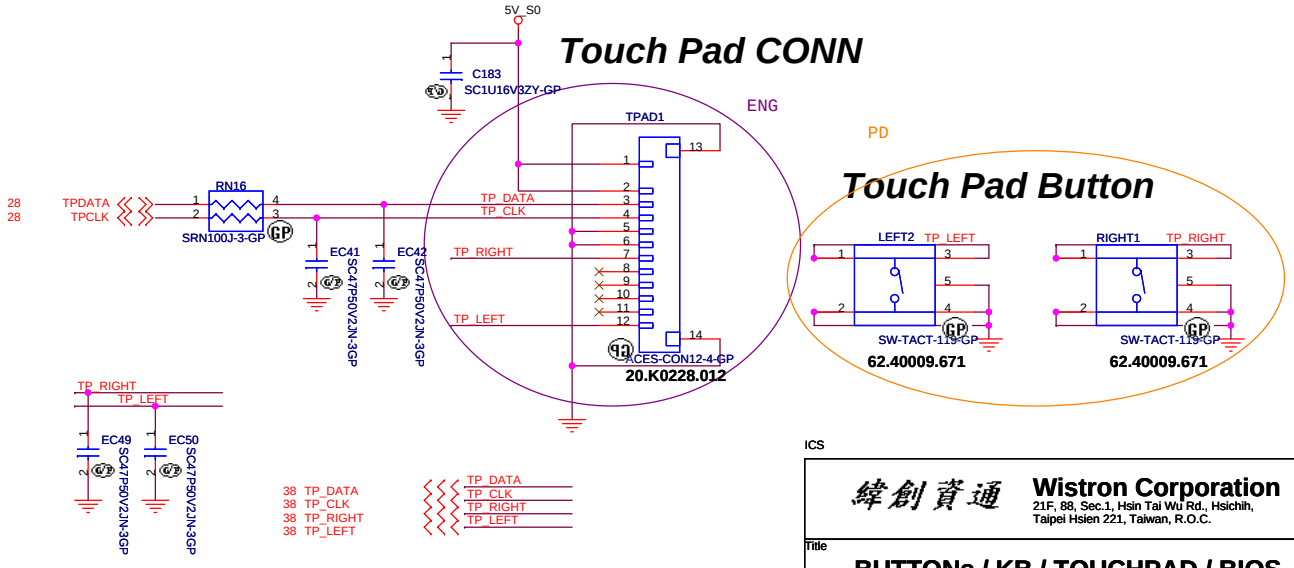

ICS

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Title: **BUTTONs / KB / TOUCHPAD / BIOS**

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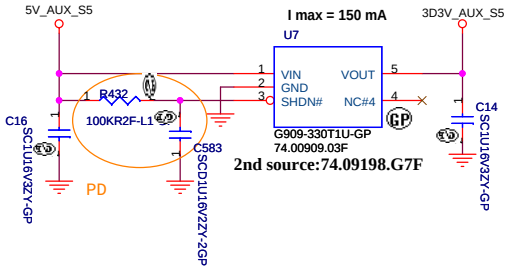
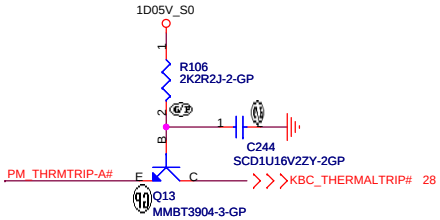
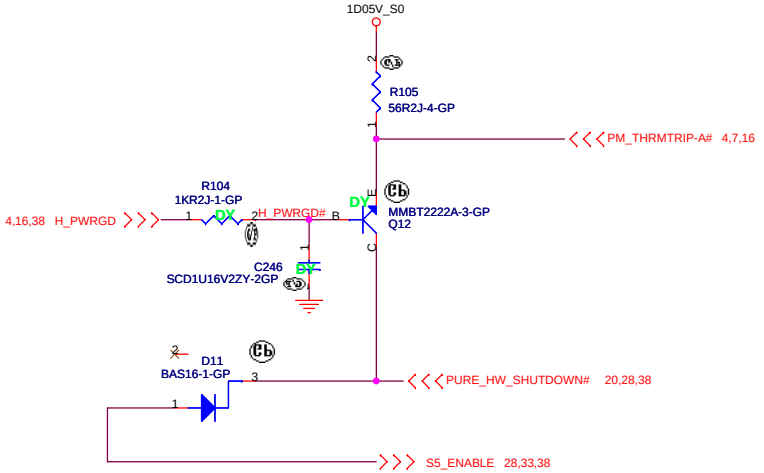
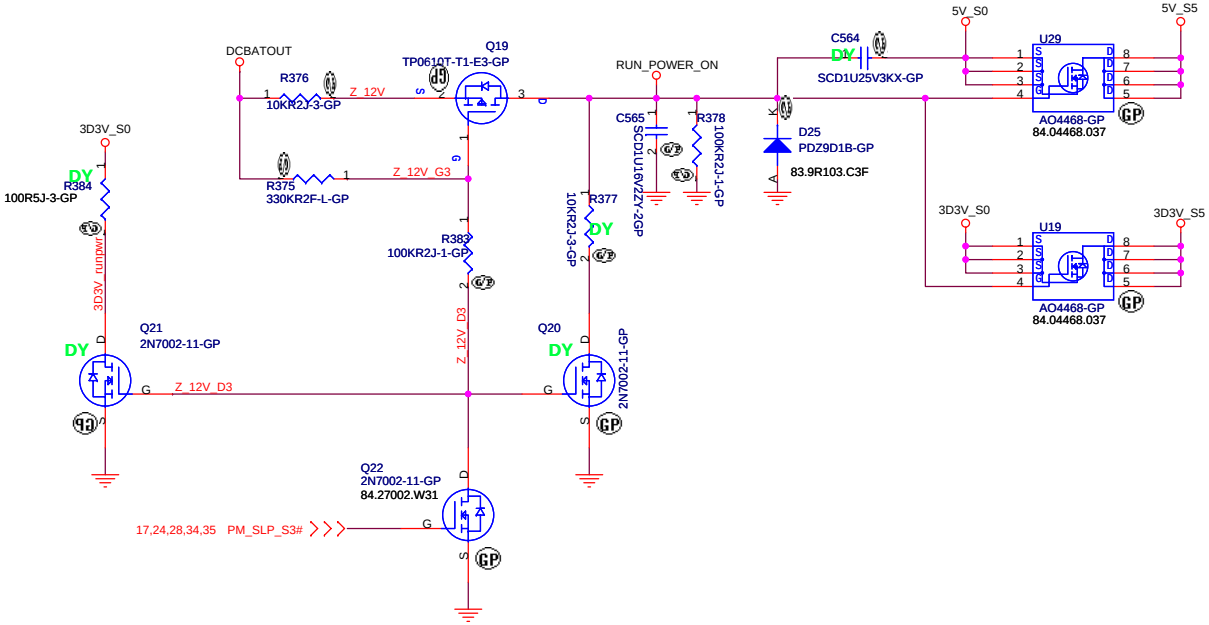
Aux Power 3D3V_AUX_S5







Run Power



ICS

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Title: **RUN POWER and 3D3V_AUX_S5**

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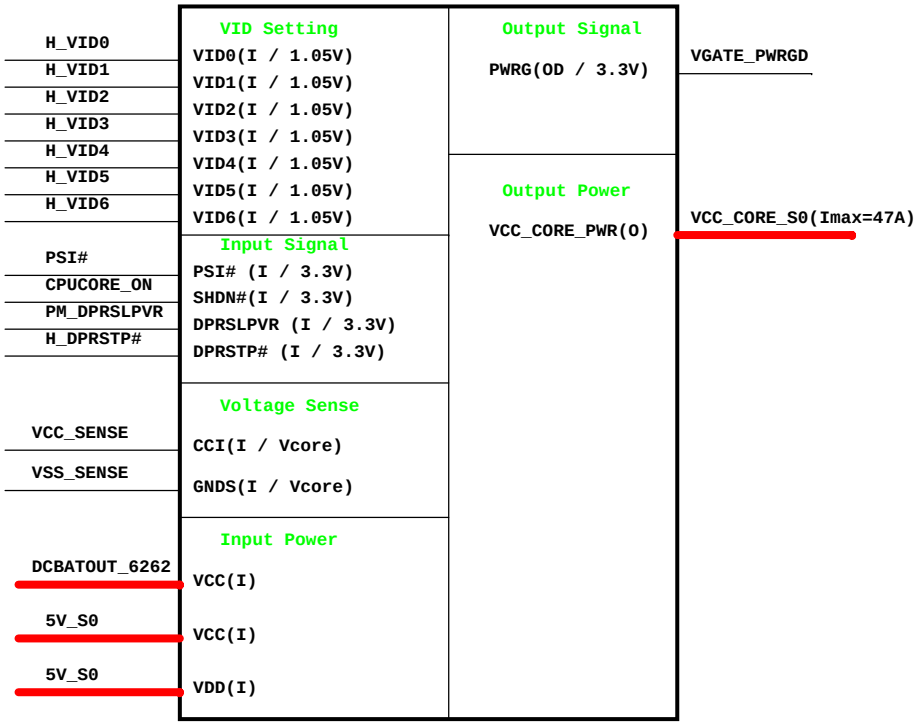
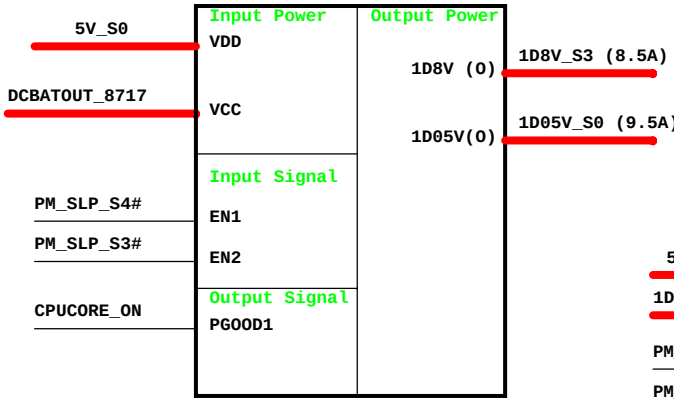
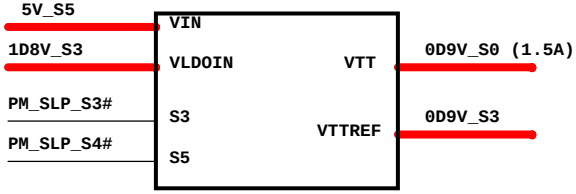
CPU_CORE
MAX8770



TPS51124
1D8V/1D05V

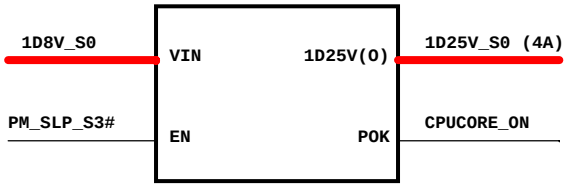


0D9V_S0



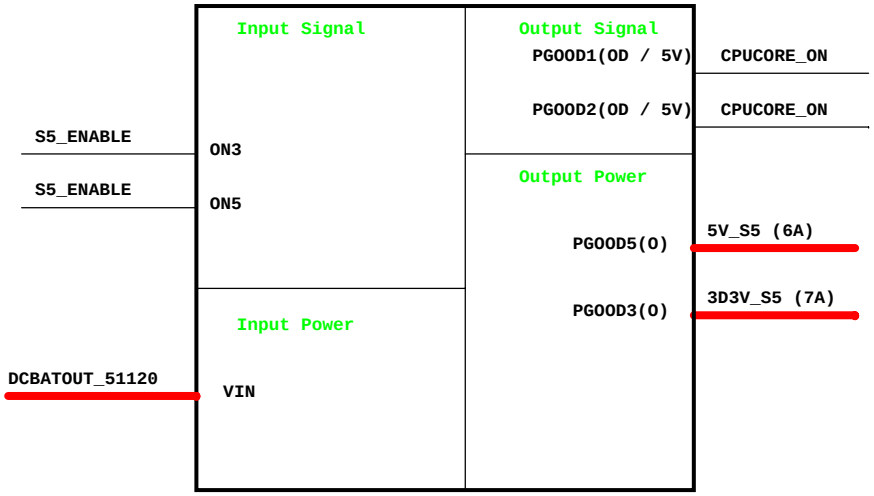
TPS51100

1D25V_S0

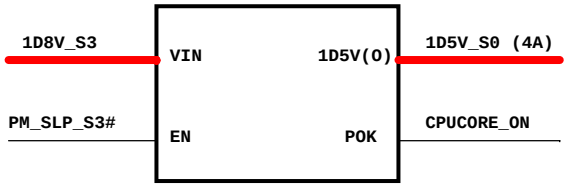


APL5913

TPS51120
5V/3D3V

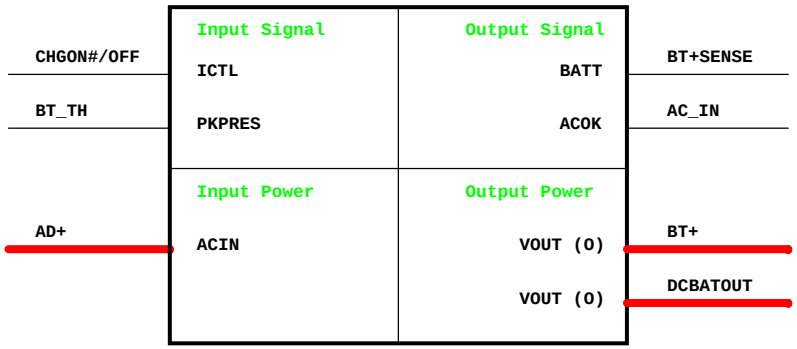


1D5V_S0



APL5915

Charger MAX8731



ICS

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
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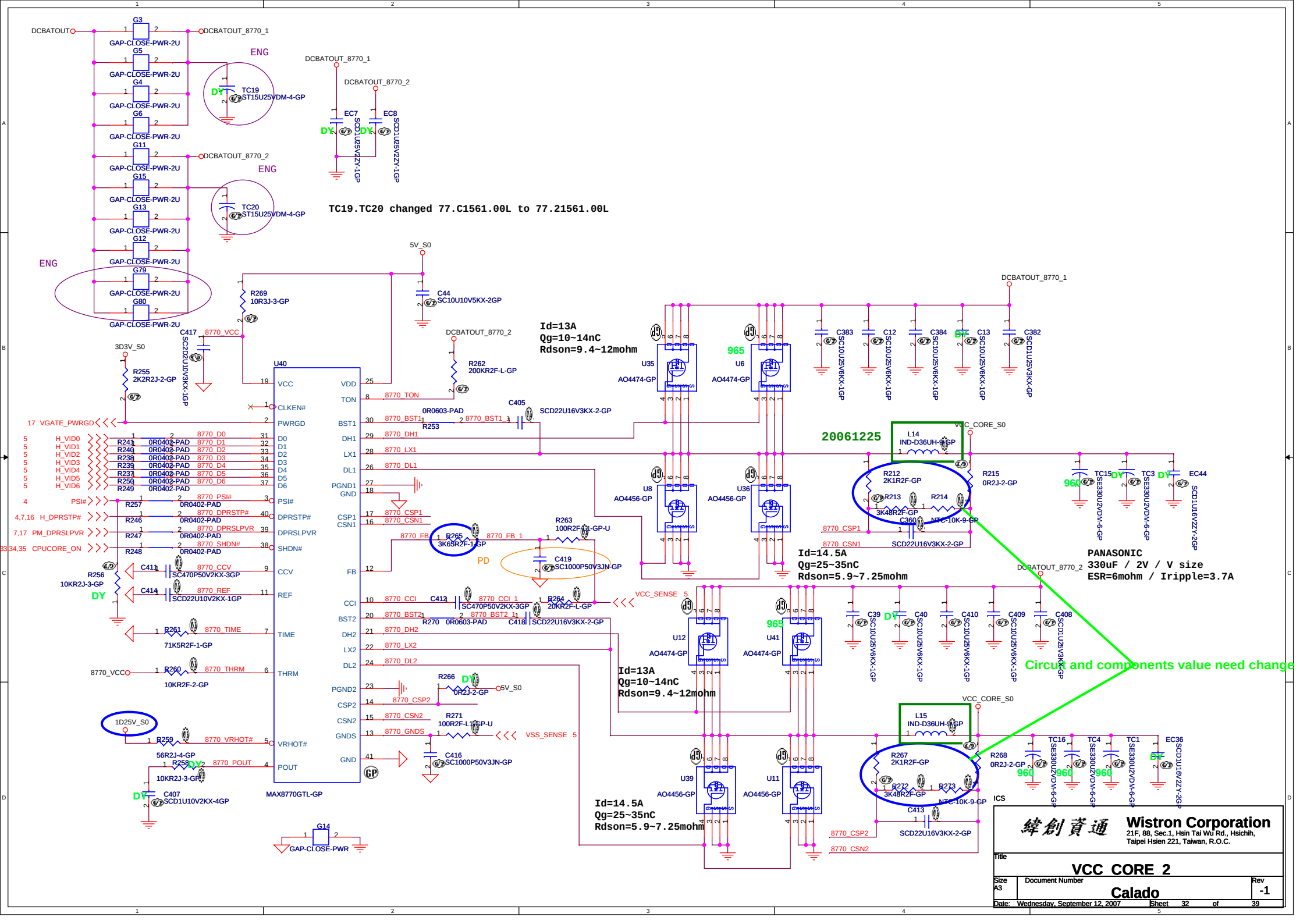
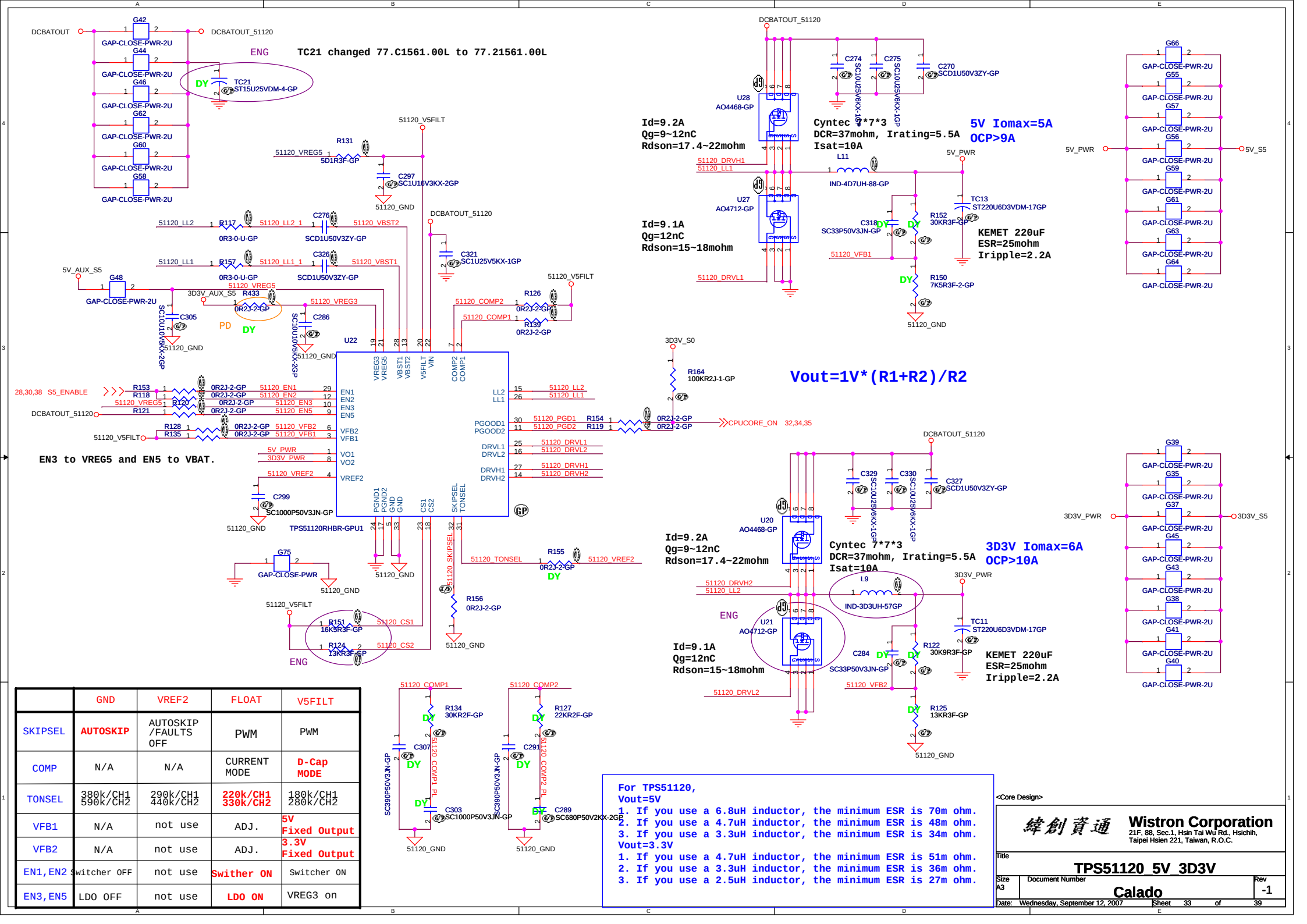

DCBATOUT
DCBATOUT_8770_1
DCBATOUT_8770_2
ENG
DY
TC19.TC20 changed 77.C1561.00L to 77.21561.00L
5V_S0
3D3V_S0
1D25V_S0
8770_VCC
MAX8770GTL-GP
U40
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
20061225
VCC_CORE_S0
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
VCC_SENSE
VSS_SENSE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Calado
Wednesday, September 12, 2007



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swither ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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Title: TPS51120_5V_3D3V
Size: A3 | Document Number: Calado | Rev: -1
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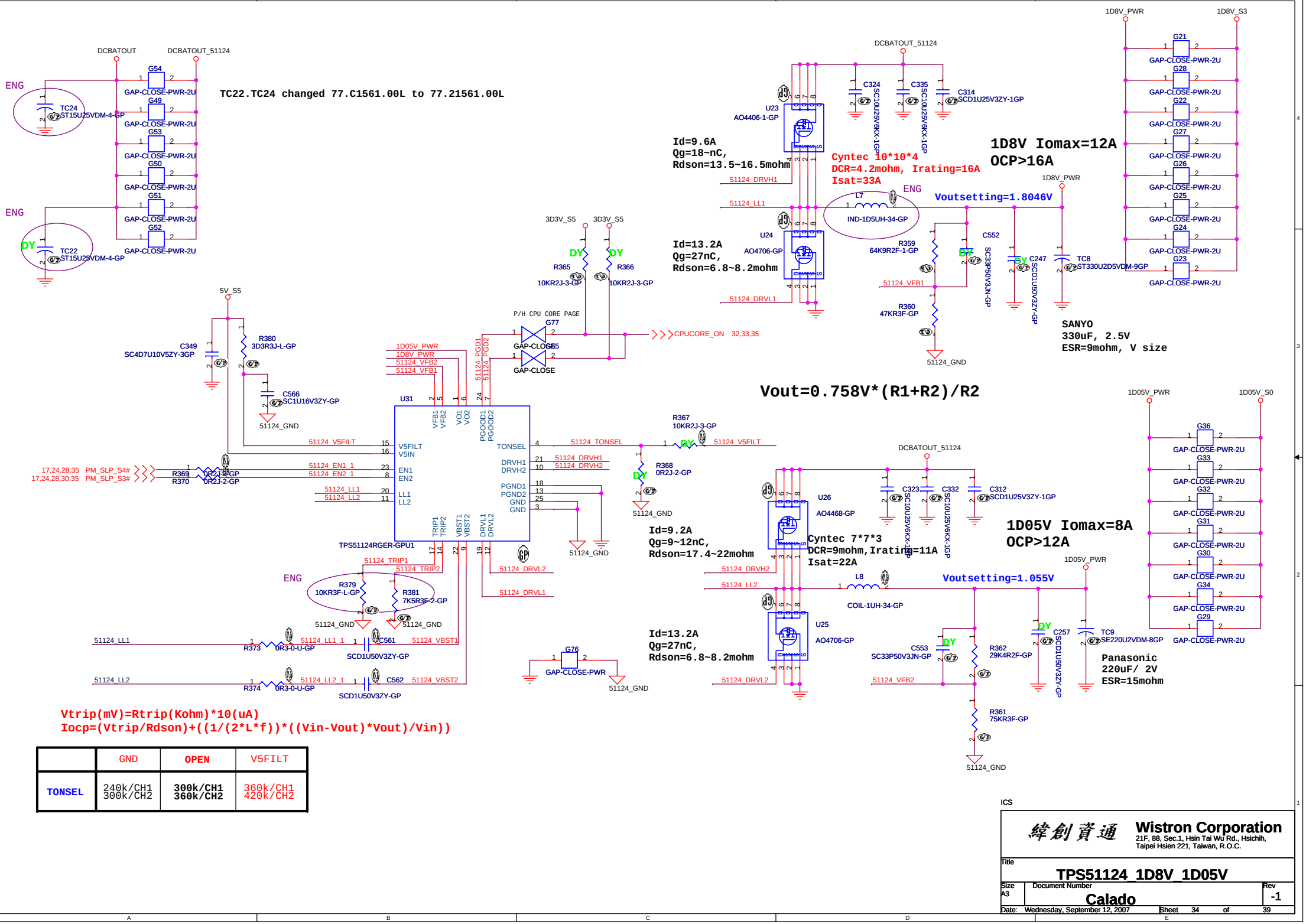
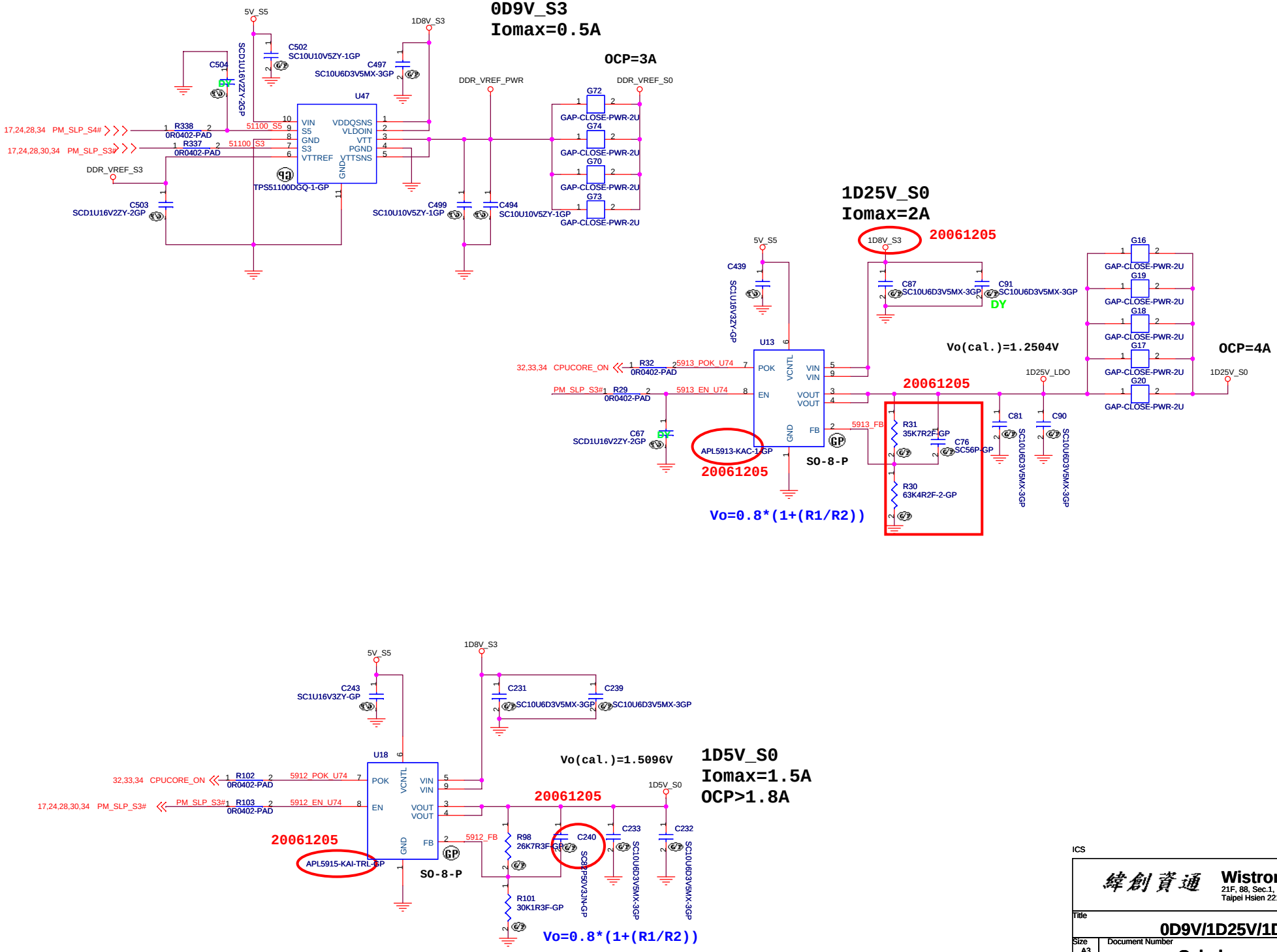


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2


0D9V_S3
Iomax=0.5A
OCP=3A
5V_S5
1D8V_S3
C502
SC10U10V5ZY-1GP
C504
SCD1U16V2ZY-2GP
C497
SC10U6D3V5MX-3GP
U47
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
TPS51100DGQ-1-GP
DDR_VREF_PWR
DDR_VREF_S0
G72
G74
G70
G73
GAP-CLOSE-PWR-2U
17,24,28,34 PM_SLP_S4#
17,24,28,30,34 PM_SLP_S3#
R338
R337
0R0402-PAD
51100_S5
51100_S3
DDR_VREF_S3
C503
SCD1U16V2ZY-2GP
C499
SC10U10V5ZY-1GP
C494
SC10U10V5ZY-1GP
1D25V_S0
Iomax=2A
20061205
1D8V_S3
5V_S5
C439
SC1U16V3ZY-GP
C87
SC10U6D3V5MX-3GP
C91
SC10U6D3V5MX-3GP
DY
U13
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5913-KAC-1-GP
SO-8-P
32,33,34 CPUCORE_ON
PM_SLP_S3#
R32
R29
5913_POK_U74
5913_EN_U74
5913_FB
C67
SCD1U16V2ZY-2GP
Vo(cal.)=1.2504V
OCP=4A
1D25V_LDO
1D25V_S0
R31
35K7R2F-GP
C76
SC56P-GP
R30
63K4R2F-2-GP
C81
C90
SC10U6D3V5MX-3GP
Vo=0.8*(1+(R1/R2))
G16
G19
G18
G17
G20
1D5V_S0
Iomax=1.5A
OCP>1.8A
1D8V_S3
5V_S5
C243
SC1U16V3ZY-GP
C231
C239
SC10U6D3V5MX-3GP
U18
APL5915-KAI-TRL-GP
Vo(cal.)=1.5096V
32,33,34 CPUCORE_ON
17,24,28,30,34 PM_SLP_S3#
R102
R103
5912_POK_U74
5912_EN_U74
5912_FB
R98
26K7R3F-GP
C240
SC82P50V3JN-GP
C233
C232
R101
30K1R3F-GP
Vo=0.8*(1+(R1/R2))
ICS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
0D9V/1D25V/1D5V
Size
A3
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Calado
Rev
-1
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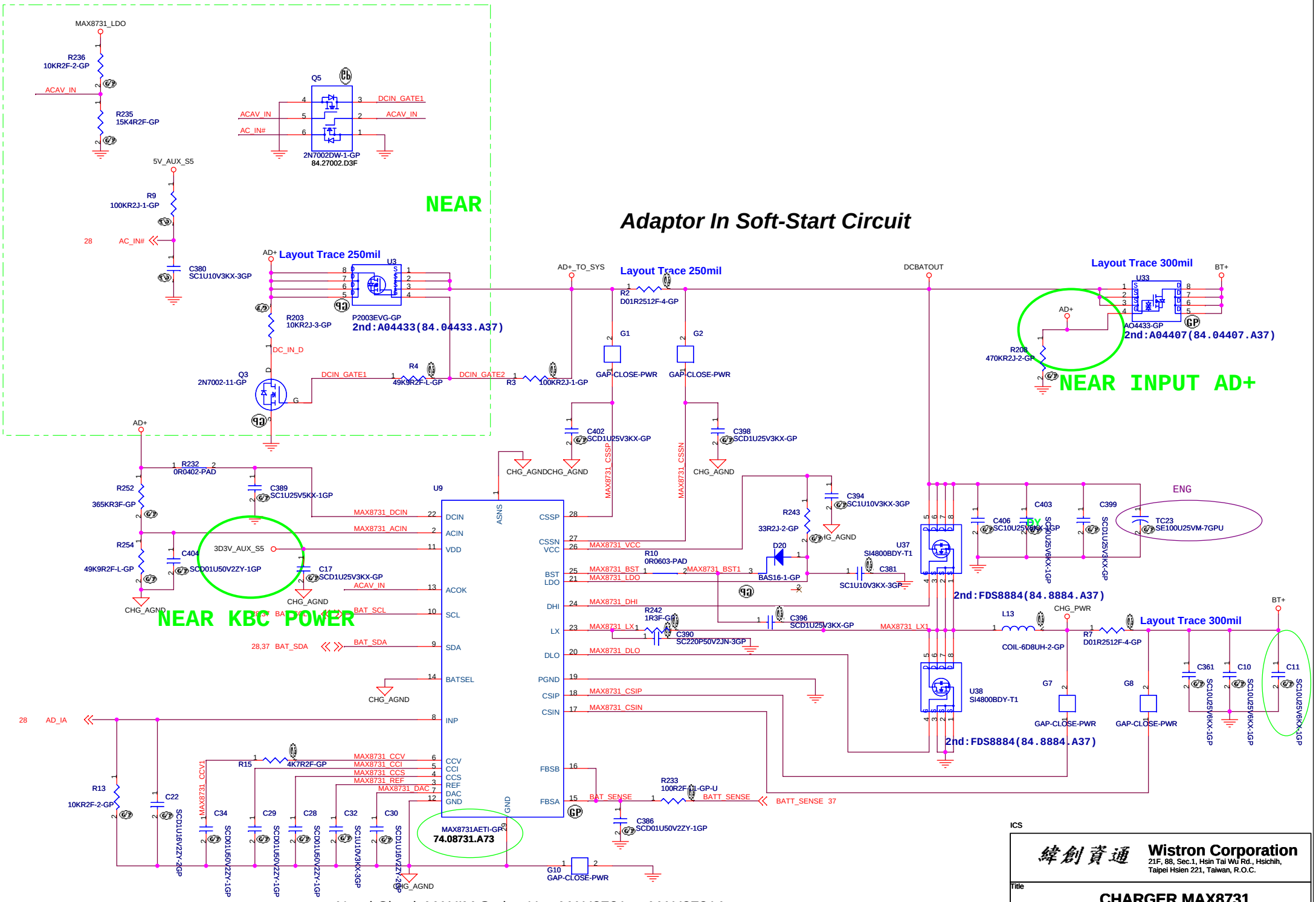
Adaptor In Soft-Start Circuit
NEAR
NEAR INPUT AD+
NEAR KBC POWER
Layout Trace 250mil
Layout Trace 300mil
2nd:A04433(84.04433.A37)
2nd:A04407(84.04407.A37)
2nd:FDS8884(84.8884.A37)
MAX8731_LDO
ACAV_IN
AC_IN#
5V_AUX_S5
AD+
AD+_TO_SYS
DCBATOUT
BT+
DCIN_GATE1
DCIN_GATE2
DC_IN_D
3D3V_AUX_S5
CHG_AGND
CHG_PWR
BAT_SCL
BAT_SDA
BATT_SENSE
AD_IA
MAX8731_DCIN
MAX8731_ACIN
MAX8731_VCC
MAX8731_BST
MAX8731_LDO
MAX8731_DHI
MAX8731_LX
MAX8731_DLO
MAX8731_CSIP
MAX8731_CSIN
MAX8731_CCV
MAX8731_CCI
MAX8731_CCS
MAX8731_REF
MAX8731_DAC
MAX8731_CSSP
MAX8731_CSSN
MAX8731_BST1
MAX8731_LX1
ENG
MAX8731AETI-GP
74.08731.A73
Need Check MAXIM Sming Use MAX8731 or MAX8731A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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CHARGER MAX8731
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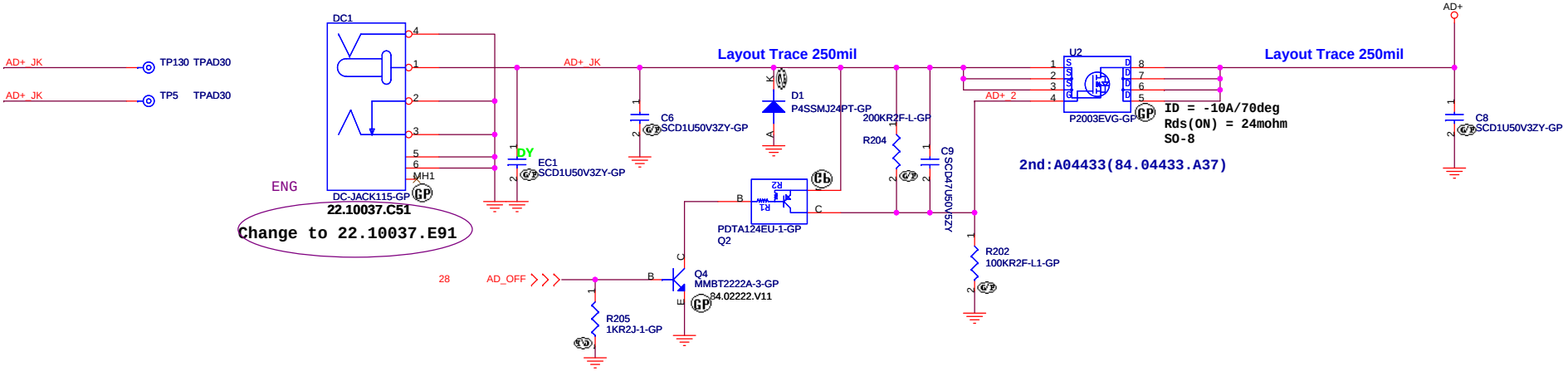
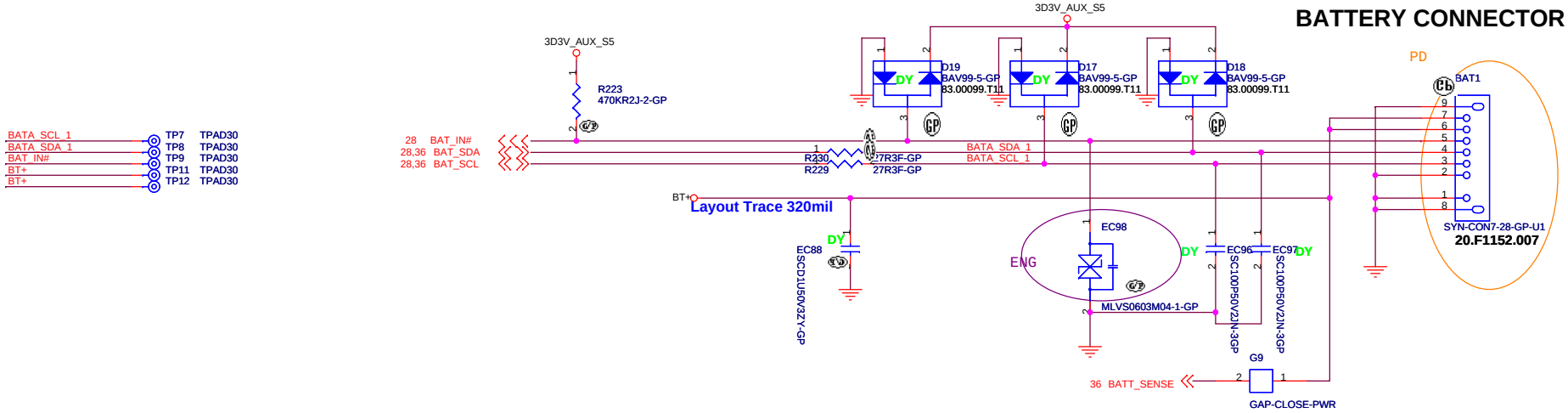
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title: **AD/BATT CONN**

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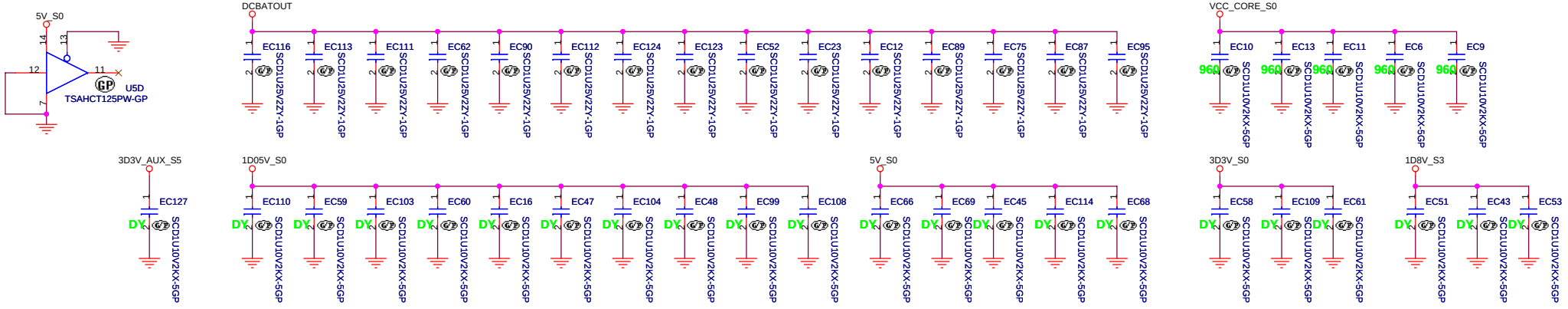

ENG

PD

FAN CONN

20	FAN1_VCC	FAN1_VCC	TP33	TPAD30
20	FAN1_FG1	FAN1_FG1	TP39	TPAD30
20,28,30	PURE_HW_SHUTDOWN#	PURE_HW_SHUTDOWN#	TP82	TPAD30

Audio Connector

26,27	LINEOUT_JD#	LINEOUT_JD#	TP156	TPAD30
27	SPKR_R+1	SPKR_R+1	TP166	TPAD30
27	SPKR_L+1	SPKR_L+1	TP164	TPAD30
26,27	MIC_JD#	MIC_JD#	TP157	TPAD30
26,27	AUD_MICIN_R	AUD_MICIN_R	TP167	TPAD30
26,27	AUD_MICIN_L	AUD_MICIN_L	TP168	TPAD30

Internal Speaker

27	SPKR_L-	SPKR_L-	TP124	TPAD30
27	SPKR_L+	SPKR_L+	TP126	TPAD30
27	SPKR_R-	SPKR_R-	TP127	TPAD30
27	SPKR_R+	SPKR_R+	TP128	TPAD30

USB ZIF CONN

Test Point

	5V_S5	TP79	TPAD30	
	5V_S5	TP6	TPAD30	
17,21	USBPN0	USBPN0	TP59	TPAD30
17,21	USBPP0	USBPP0	TP60	TPAD30
17,21	USBPN2	USBPN2	TP138	TPAD30
17,21	USBPP2	USBPP2	TP137	TPAD30
17,21	USBPN4	USBPN4	TP101	TPAD30
17,21	USBPP4	USBPP4	TP103	TPAD30
17,21	USB_OC#4	USB_OC#4	TP108	TPAD30
21,28	USB_PWR_EN#	USB_PWR_EN#	TP80	TPAD30

Internal KeyBoard CONN

Test Point

28,29	KROW[1..8]	KROW[1..8]		
28,29	KCOL[1..16]	KCOL[1..16]		
	KCOL1	TP45	TPAD30	
	KCOL2	TP41	TPAD30	
	KCOL3	TP40	TPAD30	
	KCOL4	TP38	TPAD30	
	KCOL5	TP36	TPAD30	
	KCOL6	TP34	TPAD30	
	KCOL7	TP32	TPAD30	
	KCOL8	TP31	TPAD30	
	KCOL9	TP28	TPAD30	
	KCOL10	TP26	TPAD30	
	KCOL11	TP22	TPAD30	
	KCOL12	TP21	TPAD30	
	KCOL13	TP19	TPAD30	
	KCOL14	TP18	TPAD30	
	KCOL15	TP16	TPAD30	
	KCOL16	TP17	TPAD30	
	KROW1	TP56	TPAD30	
	KROW2	TP55	TPAD30	
	KROW3	TP52	TPAD30	
	KROW4	TP51	TPAD30	
	KROW5	TP50	TPAD30	
	KROW6	TP49	TPAD30	
	KROW7	TP48	TPAD30	
	KROW8	TP46	TPAD30	

TRING CONN

Test Point

23	TIP_C	TIP_C	TP2	TPAD30
23	RING_C	RING_C	TP3	TPAD30

Touch Pad CONN

Test Point near TPAD1

	5V_S0	TP10	TPAD30	
29	TP_DATA	TP_DATA	TP54	TPAD30
29	TP_CLK	TP_CLK	TP53	TPAD30
29	TP_RIGHT	TP_RIGHT	TP57	TPAD30
29	TP_LEFT	TP_LEFT	TP58	TPAD30

Check test point

	3D3V_S0	TP4	TPAD30	
	3D3V_AUX_S5	TP13	TPAD30	
	3D3V_S5	TP15	TPAD30	
	5V_S5	TP125	TPAD30	
17,28	PM_PWRBTN#	TP140	TPAD30	
4,16,30	H_PWRGD	TP85	TPAD30	
28,30,33	S5_ENABLE	TP139	TPAD30	
4,6	H_CPURST#	TP27	TPAD30	

CPU **NB** **MDC** **MINI CARD**

H5 HOLE, H6 HOLE, H8 HOLE

H7 HOLE, H9 HOLE

H10 HOLE, H11 HOLE

H1 HOLE, H2 HOLE

34.42Y01.011 34.42Y01.011 34.42Y01.011 34.4G502.001

H3 HOLE, H4 HOLE, H12 HOLE, H13 HOLE, H14 HOLE, H15 HOLE, H16 HOLE, H17 HOLE, H18 HOLE, H19 HOLE, H20 HOLE, H21 HOLE, H22 HOLE, H23 HOLE

GND3 SPRING-23-GP DY

GND6 SPRING-6

GND7 SPRING-6

GND4 SPRING-16

GND5 SPRING-16

34.13B01.001 34.43E28.001

GND8 SPRING-9-GP

GND9 SPRING-9-GP

GND10 SPRING-9-GP

GND11 SPRING-9-GP

GND12 SPRING-9-GP

GND13 SPRING-9-GP

34.49U23.001

Test Point放在Dimm Door打開可量測處

ICS

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Title: EMI/Spring/Boss

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SA to SB
1.TC6 change to 900U
2.modify U42(change to G913 300mA) add R417 for TV CRT ripple.
3.add Q27 for BT LED signal
4.change LED1 to 83.01221.I70(right angle)
5.add U55 BLON_5V for LED panel
6.change U1 to 74.04280.C9P for source request
7.add polyswitch F3 for safety.
8.C338 C339 C341 C340 change to 0402 size for SATA signal.
9.FAN1 change to 20.F1000.003 for ME.
10.USB1 swap pin3 pin4 signal.
11.USB2 USB3 change to 22.10218.R31 for ME.
12.add polyswitch F4 F5 for safety.
13.change U4 U45 to 74.09711.B7F ,U56 U57 74.05250.C7F for source request.
14.R20 change to 1.21K for IEEE.
15.C56 change to 12P for Oscillation report.
16.U53 change to 74.09711.A7F for source request.
17.NEW1 change to 20.F07890.026.SK1 change to 21.H0153.001 for ME
18.add R421 LED4 for CardReader test.
19.C237 C229 change to 27P for Oscillation report.
20.R350 change to 4.99K for jack detection.
21.R363 R364 change to 18K.R404 R405 change to 56 ohm for audio report.
22.add AUD_AGND.L24 for audio niose.
23.C575 C577 change to 2700p Cut frequency at 500HZ
24.add BT_LED to KBC GPIO50.
25.add TC19 TC20 TC21 TC22 TC23 TC24 for acoustic noise.
26.C419 change to 1000p for power team.
27.U21 change to 84.04712.037.L9 change to 68.3R310.20A for power team.
28.R151 change to 16.5K.R124 change to 13K for OCP.
29.L7 change to 68.1R510.10J for power team.
30.R379 change to 10K.R381 change to 7.5K for OCP.
31,BAT1 change to 20.80977.007 for ME.
32.EC98 add 69.80007.031 for EC damaged.
33.R402 change to 10K.R397 DY for planar ID.
34.ODD1 change to 20.80967.050 for ME.
35.add G79.G80 for power.
36.R385.R386.R388.R387 change for Gain.R395.R407 change to 56K.
37.add EC6.EC9.EC10.EC11.EC13 to 960 for EMI.
38.add EC41.EC42.EC49.EC50.EC127 for EMI.
39.add R423.R422 for EMI.
40.add RN34.RN35.RN36 for EMI.
41.remove Golden finger
42.swap Touchpad pin define.
43.change L1 L2 to 68.00084.371.
44.change DC1 to 22.10037.E91 for ME.
45.change TVOUT1 to 22.10021.F41 for ME.
SB to -1
1.add AFTE test point for power board Conn.
2.add R432.C583 change G47 to R433 for 3D3V_AUX_S5 power option
3.change to 0 ohm pad for R45.R41.R216.R391.R183.R184.R14.R162.
R78.R79.R74.R87.R73.R77.R390.R21.R194.R187
4.change SPKR1 to 20.D0197.104 for ME.
5.change TRING1 to 21.E0024.102 for ME.
6.remove D7.D8.D9 for EMI.
7.add EC116.EC113.EC111.EC62.EC90.EC112.EC124.EC123.EC52.EC23.EC12.EC89.EC75.EC87.EC95.
8.change R422.R423 to 33 ohm.add EC71.EC72 to 33P for EMI.
9.add EC128.EC129 for EMI.
10.change c419 to 78.10234.1BL for source OBSOLETED.
11.change LEFT1.LEFT2.RIGHT1 to 62.40009.671 for ME.
12.change TVOUT1 to 22.10021.H61 for ME.
13.change BAT1 to 20.F1152.007 for ME.
14.add D26 for EMI.
15.change TC17 to 79.22710.3AL for USB droop test fial.
16.change TC2.EC84 to 5V_USB3_S0_1,change TC17.EC101 to5V_USB2_S0_1 for UPT2 fail.
17.add GND6.GND7.GND8.GND9.GND10.GND11.GND12.GND13 fot EMI.
18.change CRT1 to 20.20378.015 for ME.
19.del GND1.GND2.

ICS

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Title: Change List

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