Compal Confidential

JALA0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

(With Ati & nVidia MXM/B)

2008-04-18

REV:1.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2007/09/20	Deciphered Date 2008/09/20	Title: SCHEMATIC MB A4221

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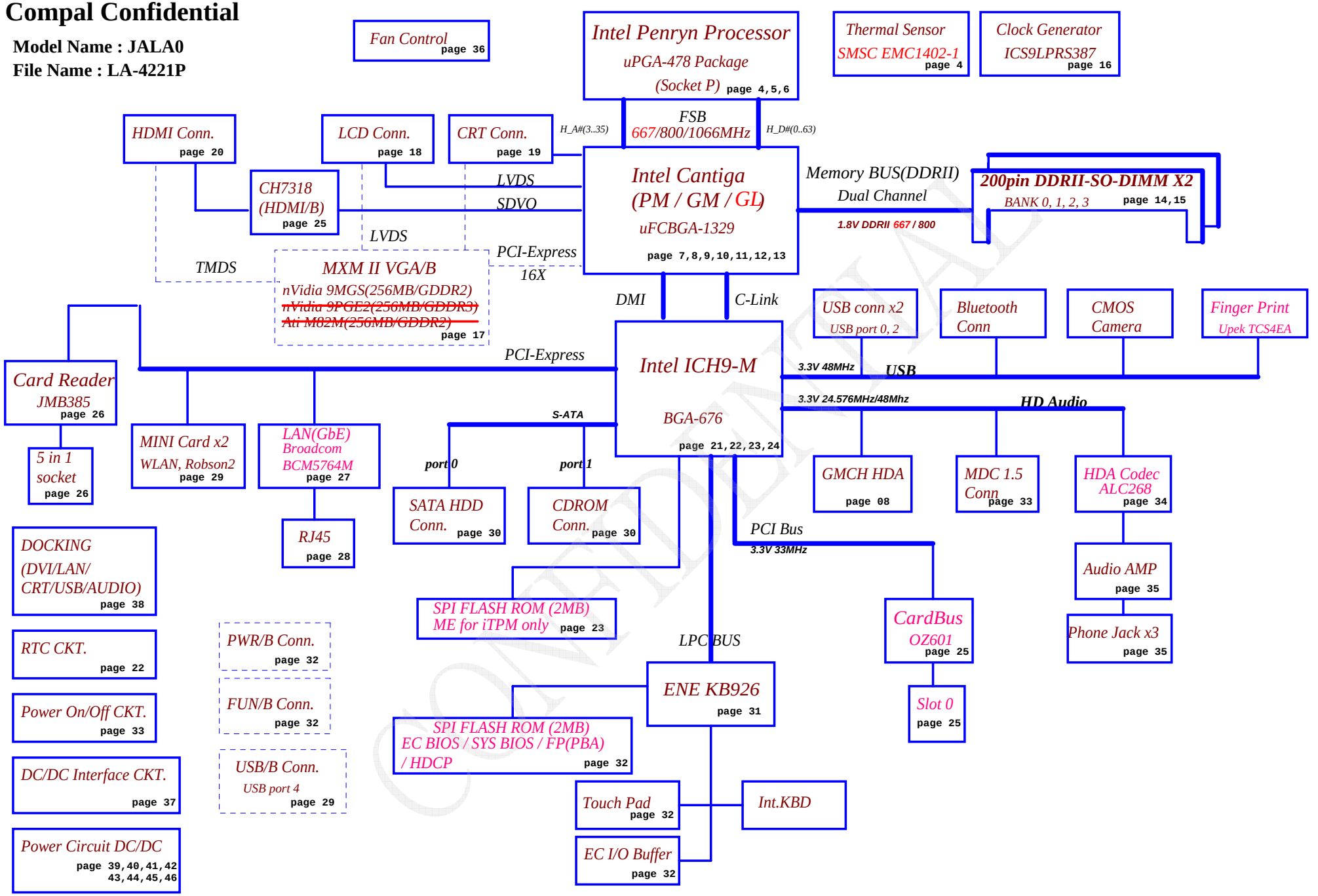
Compal Confidential

Model Name : JALA0
File Name : LA-4221P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Cardbus OZ601	AD16	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GPU(MXM/B)	1001 111X b

EC SM Bus2 address

Device	Address
ADT7421	1001 100X b
(LAN BCM5764M)	Reserved

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 010Xb
LAN BCM5764M	Reserved
(MINI CARD_WL_Robson)	Reserved

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete_H	PM@
UMA	GM@
UMA_H	UMAGM@
UMA_L	UMAGL@
Kinabalu_H	MAIN@
Kinabalu_L	VALUE@
RTC Batt	45@
ICH9M BASE	ICH9MB@
ICH9M ENHANCE	ICH9ME@
SB ROM(2MB)	SPI2MB@
SB ROM(4MB)	SPI4MB@
iTPM enable	WITHITPM@
iTPM disable	WOITPM@
HDMI enable	HDMI@
HDMI GM DET	HDMIGM@
HDMI GL/PM DET	HDMILPM@

Kinabalu_L : UMA(GL) & w/o Dock & w/o Mini card 2 & w/o iTPM

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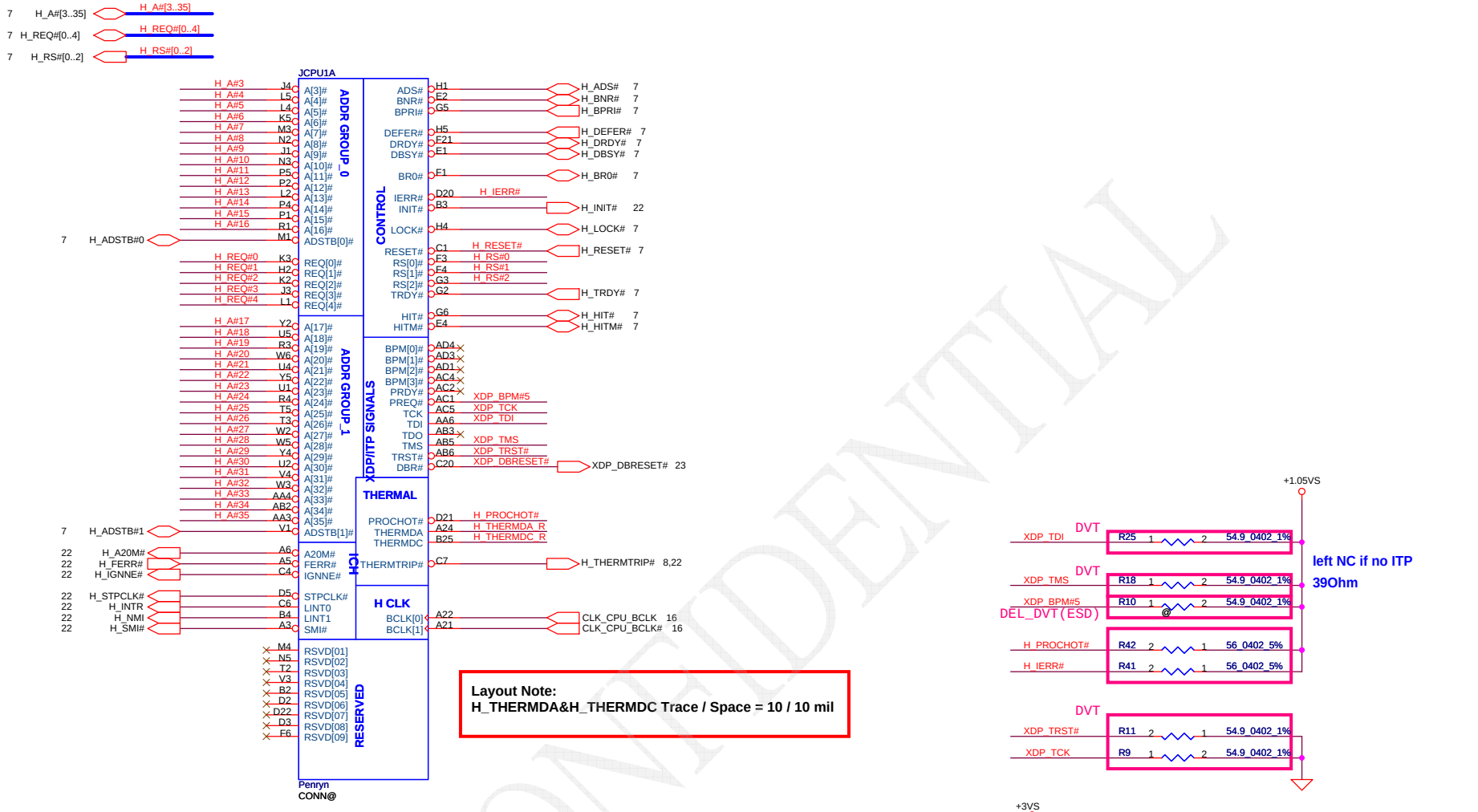
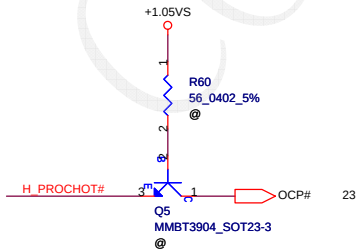
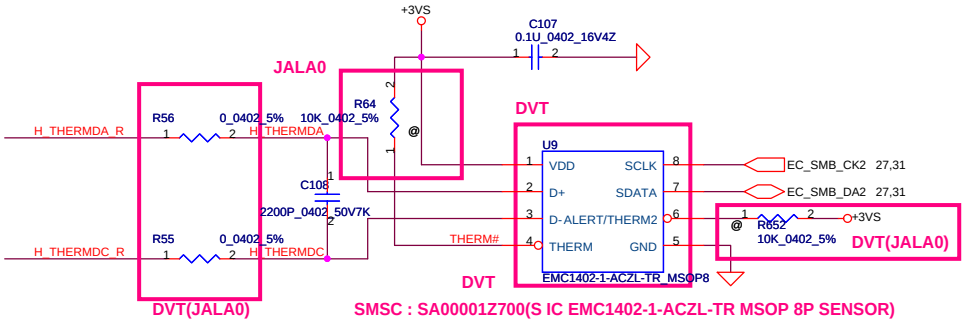


BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166





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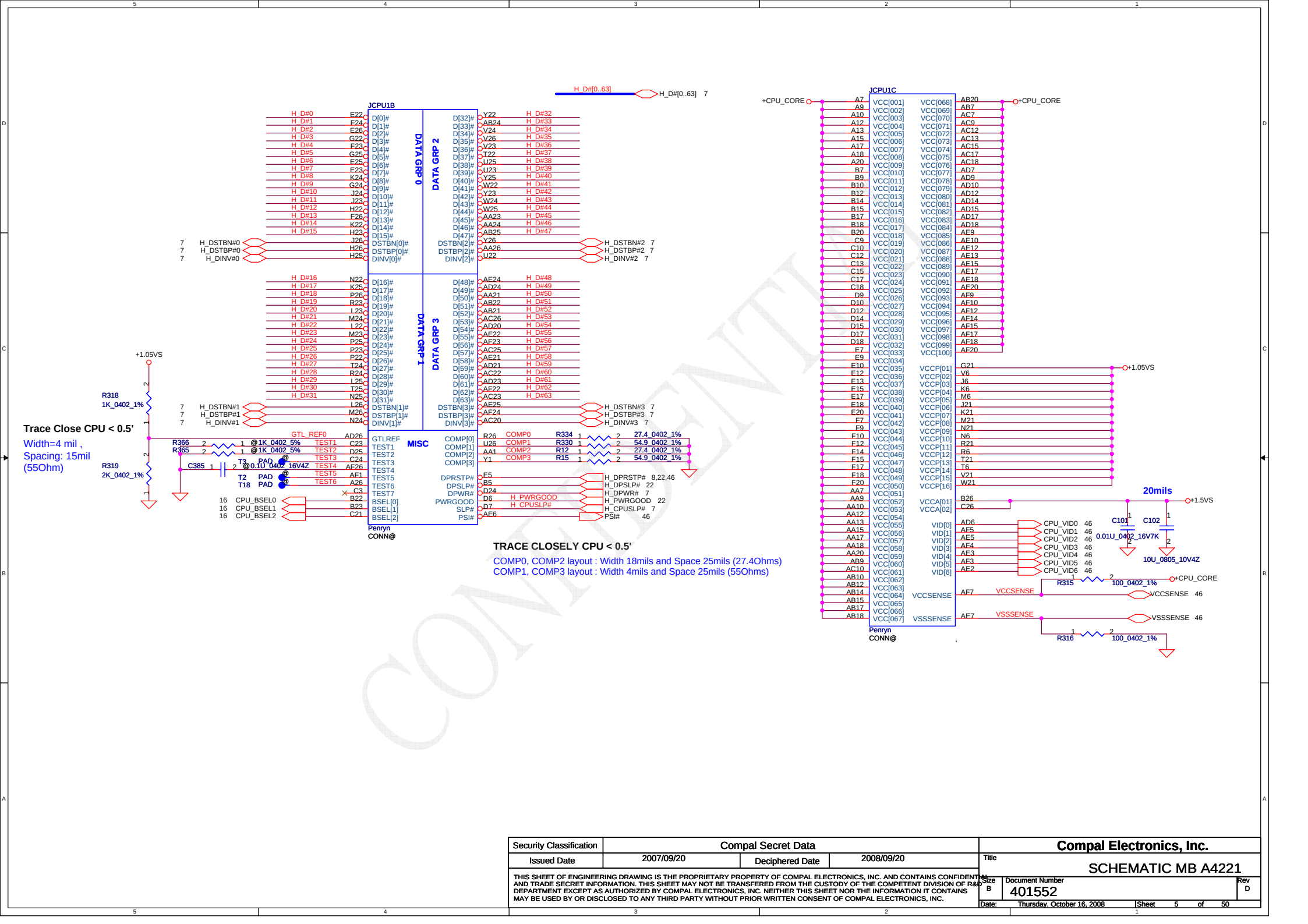

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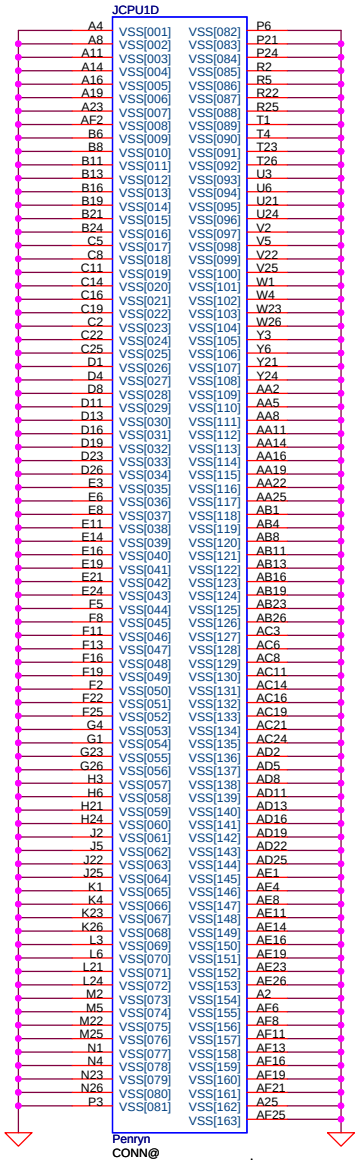
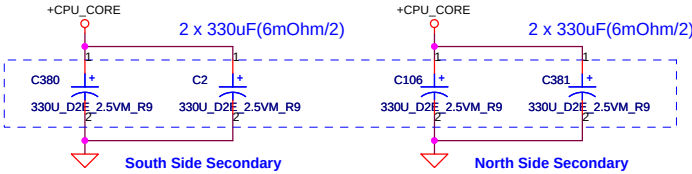
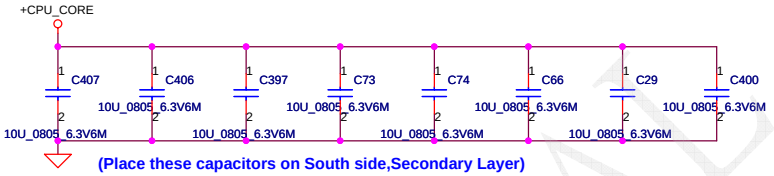
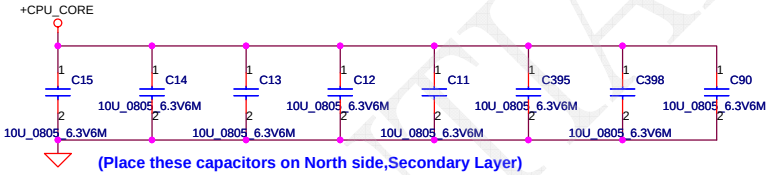
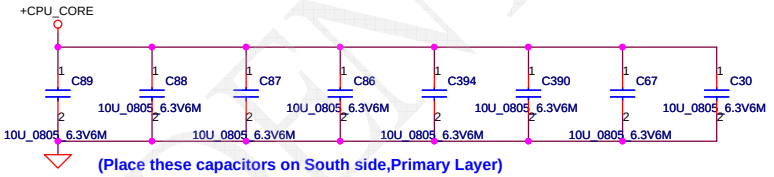
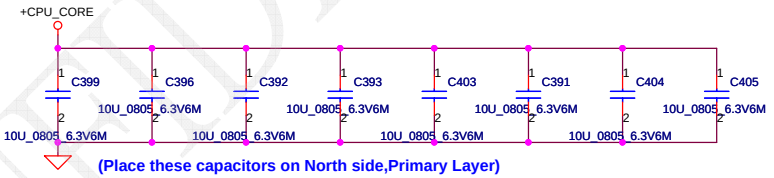




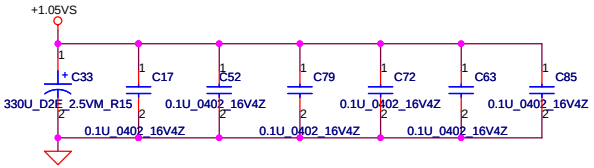








+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF 32X10uF	3m ohm/32 3m ohm/32	0.6nH/32 0.6nH/32



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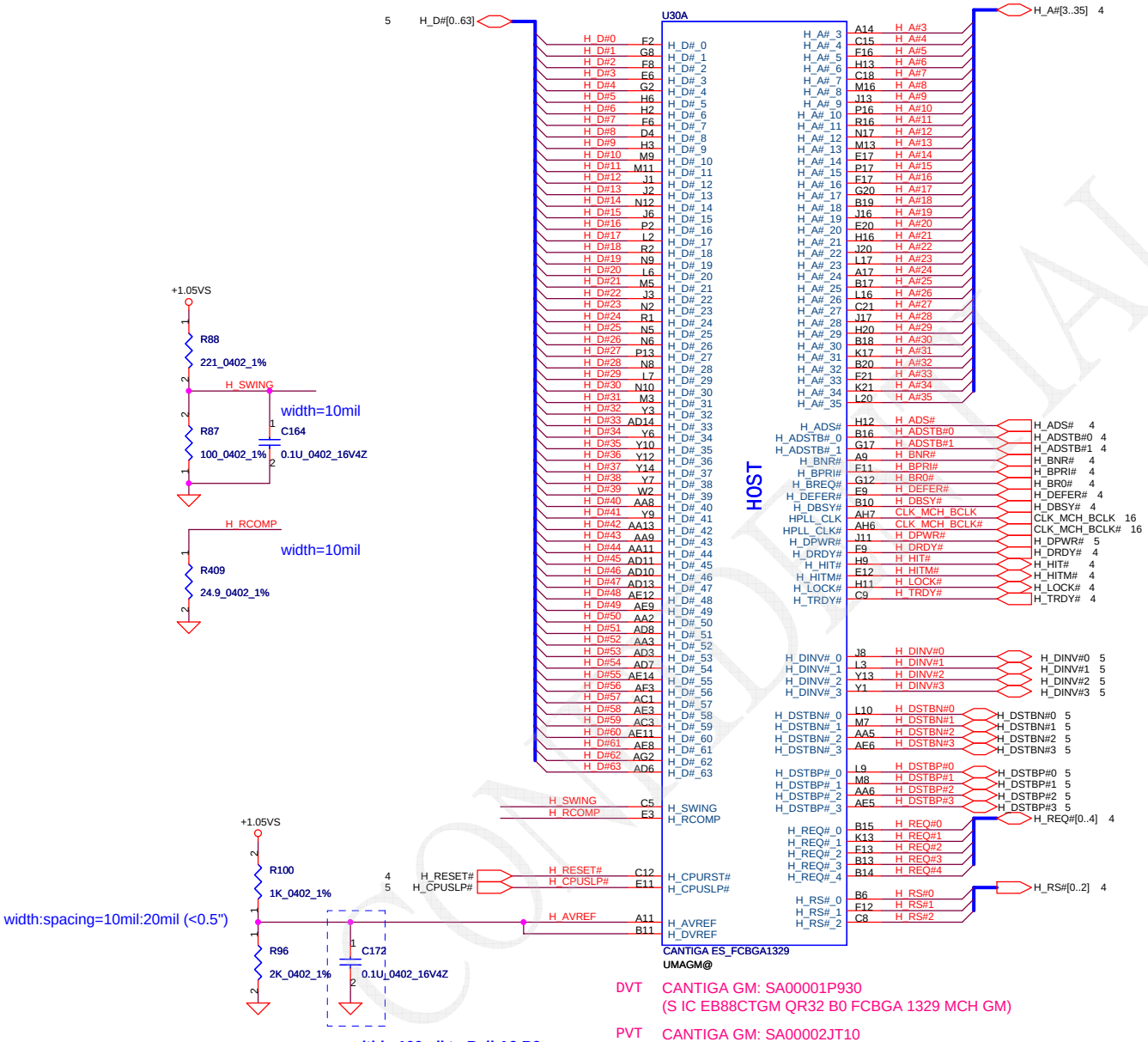

DVT CANTIGA GM: SA00001P930
(S IC EB88CTGM QR32 B0 FCBGA 1329 MCH GM)

PVT CANTIGA GM: SA00002JT10
(S IC AC88CTGM QT62 B2 FCBGA 1329 GMCH GM)

PVT2 CANTIGA GM: SA00002JT50
(S IC AC88CTGM QU36 B3 FCBGA 1329 GMCH GM)

Pre-MP CANTIGA GM: SA00002JTB0
(S IC AC82GM45 SLB94 B3 FCBGA1329 GM ABO!)

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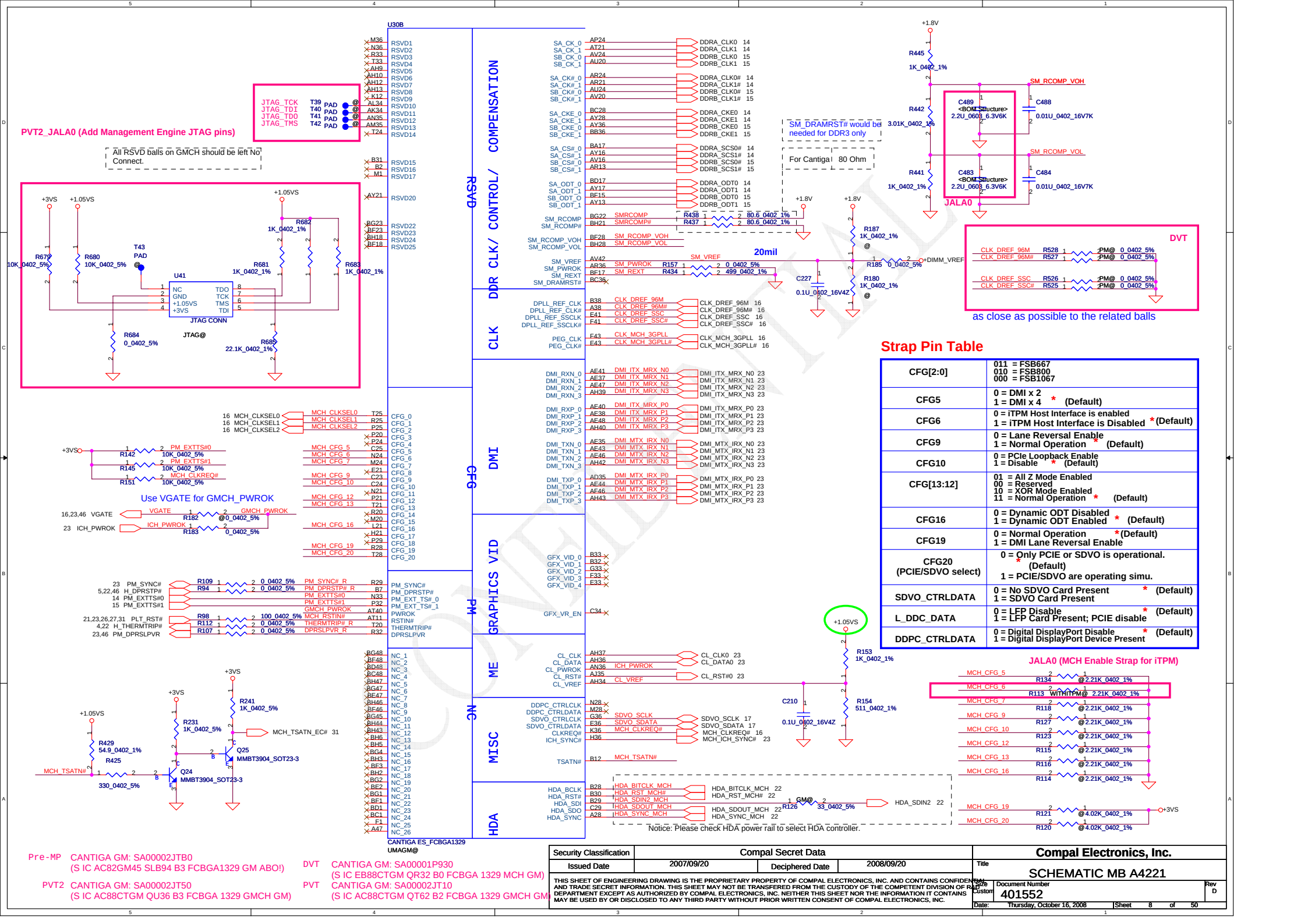

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

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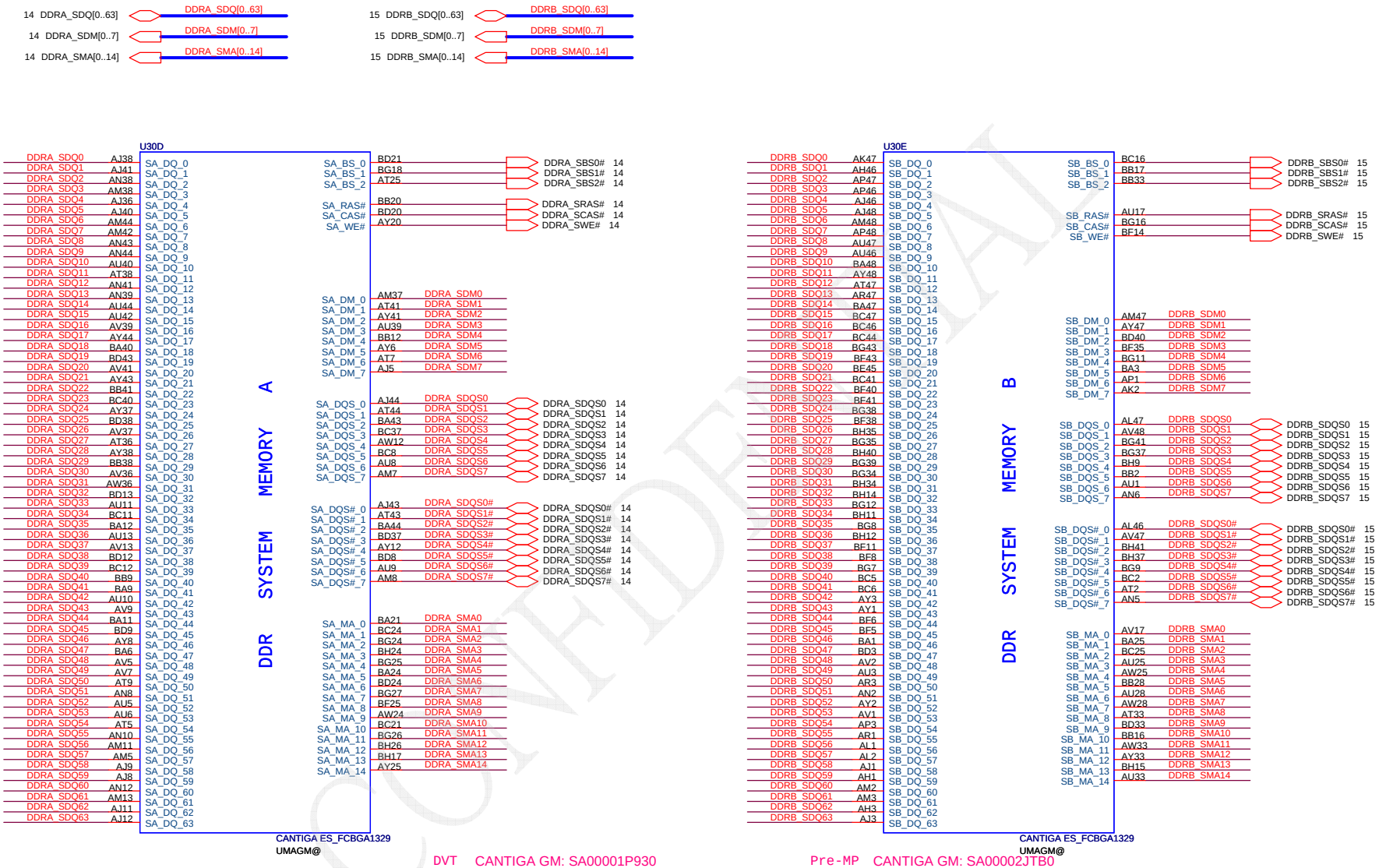

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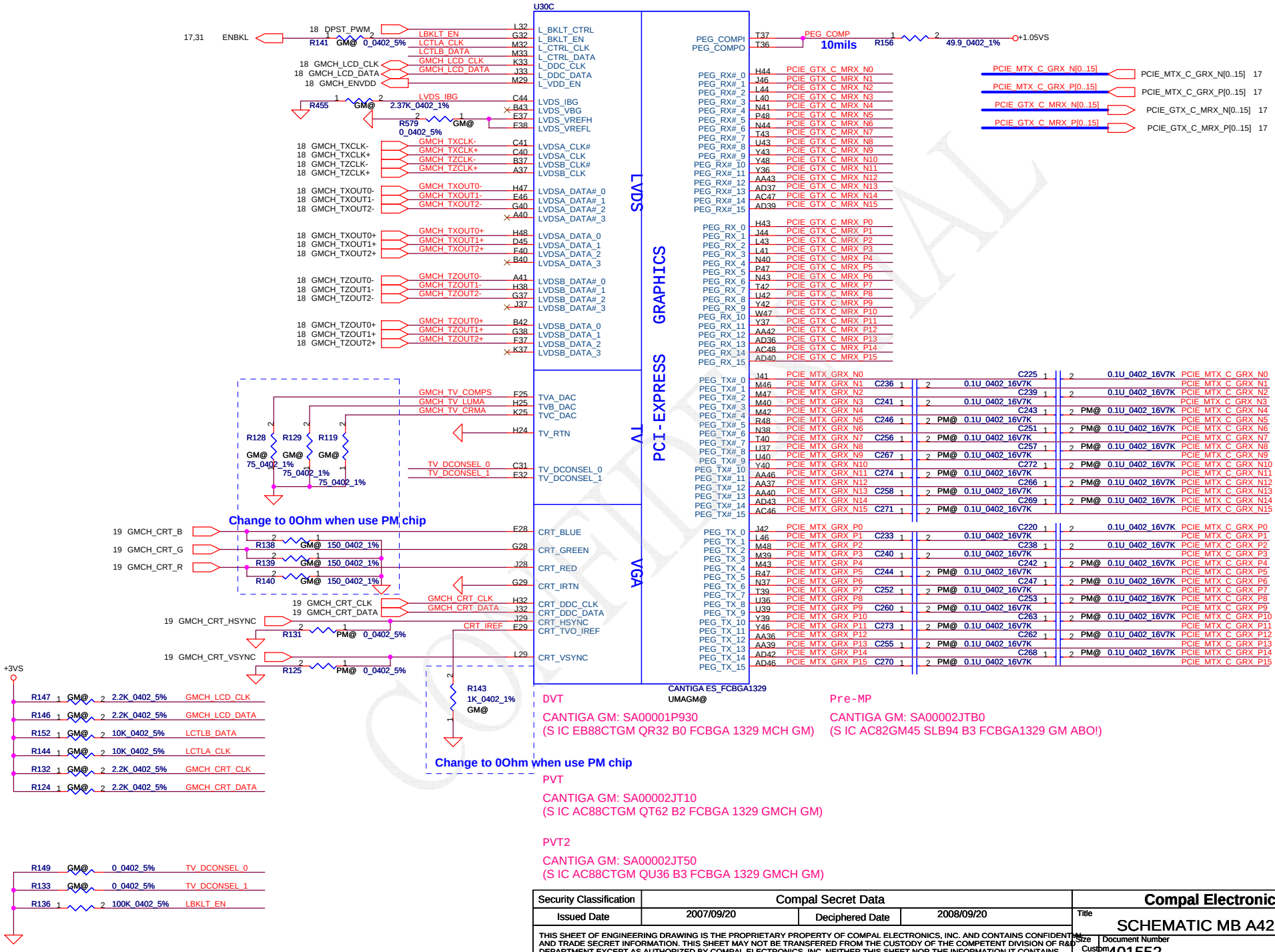

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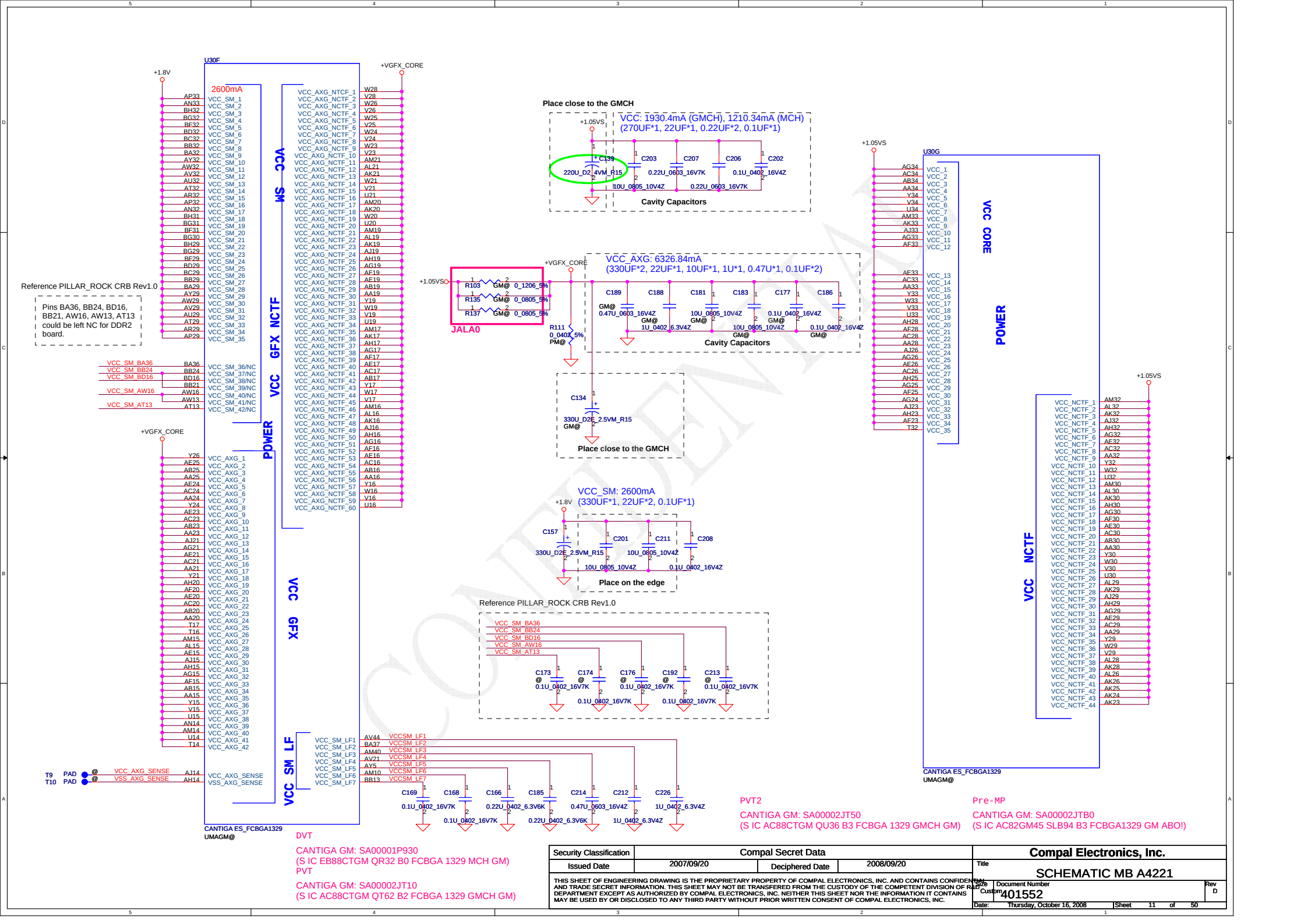

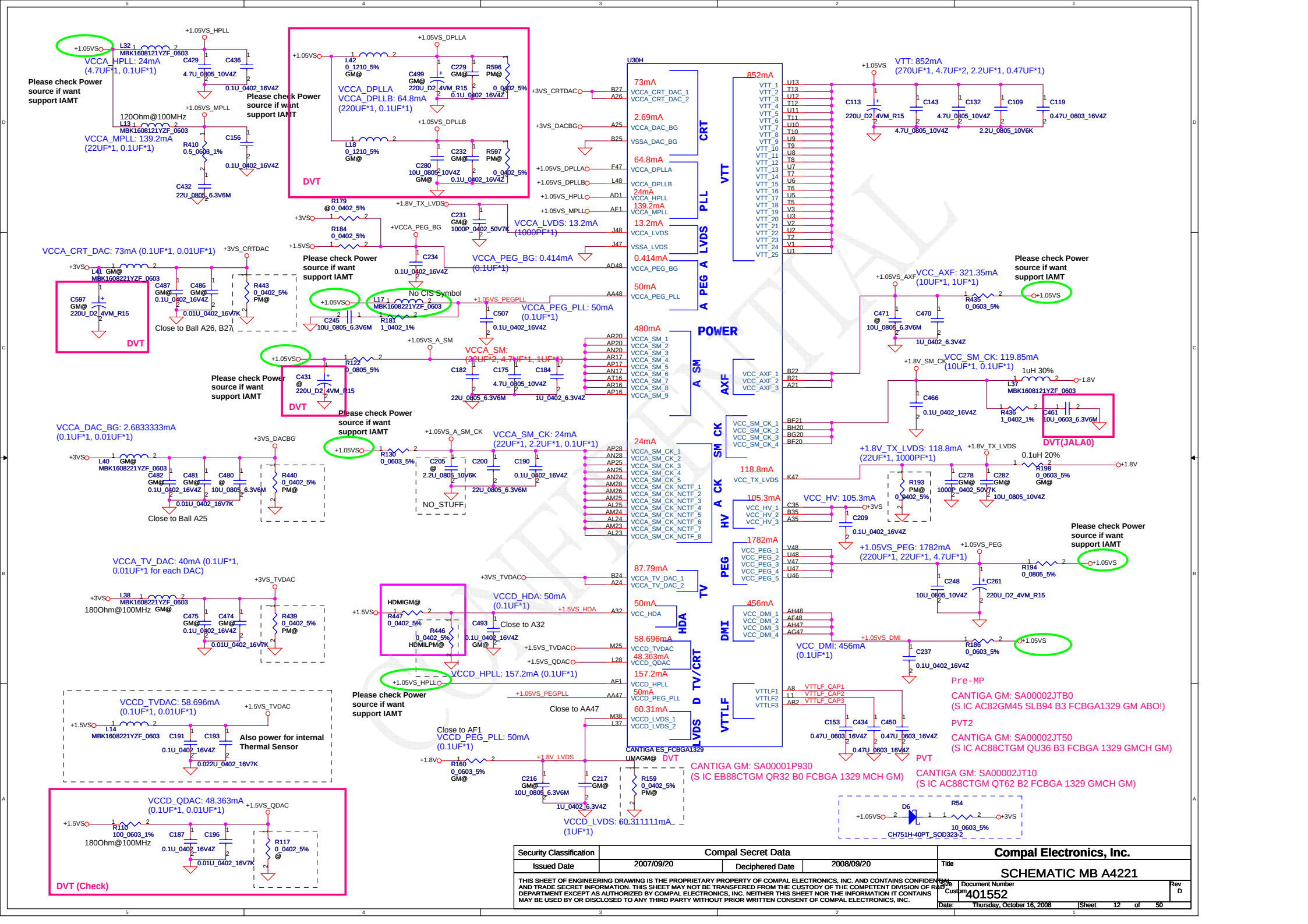

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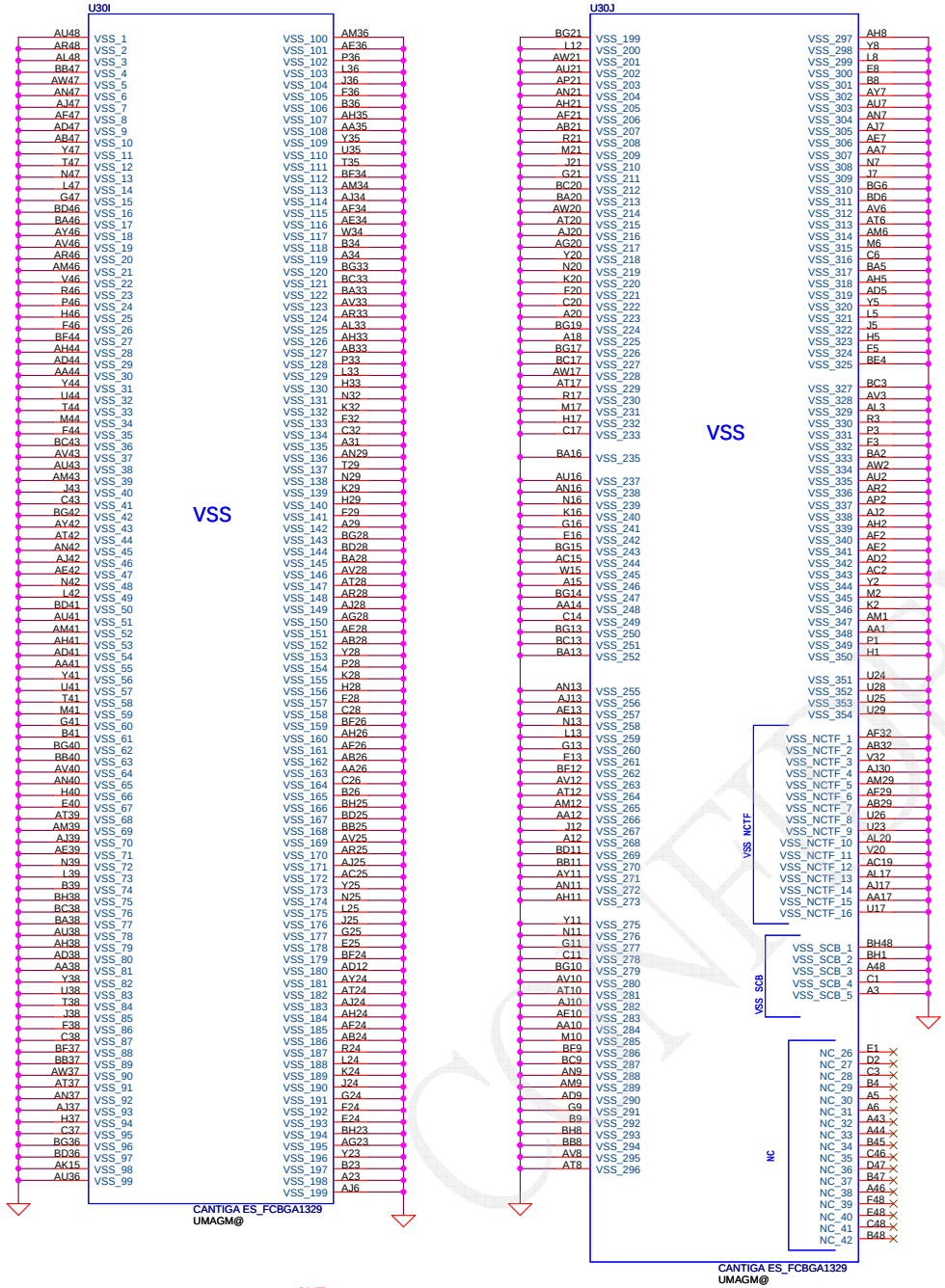

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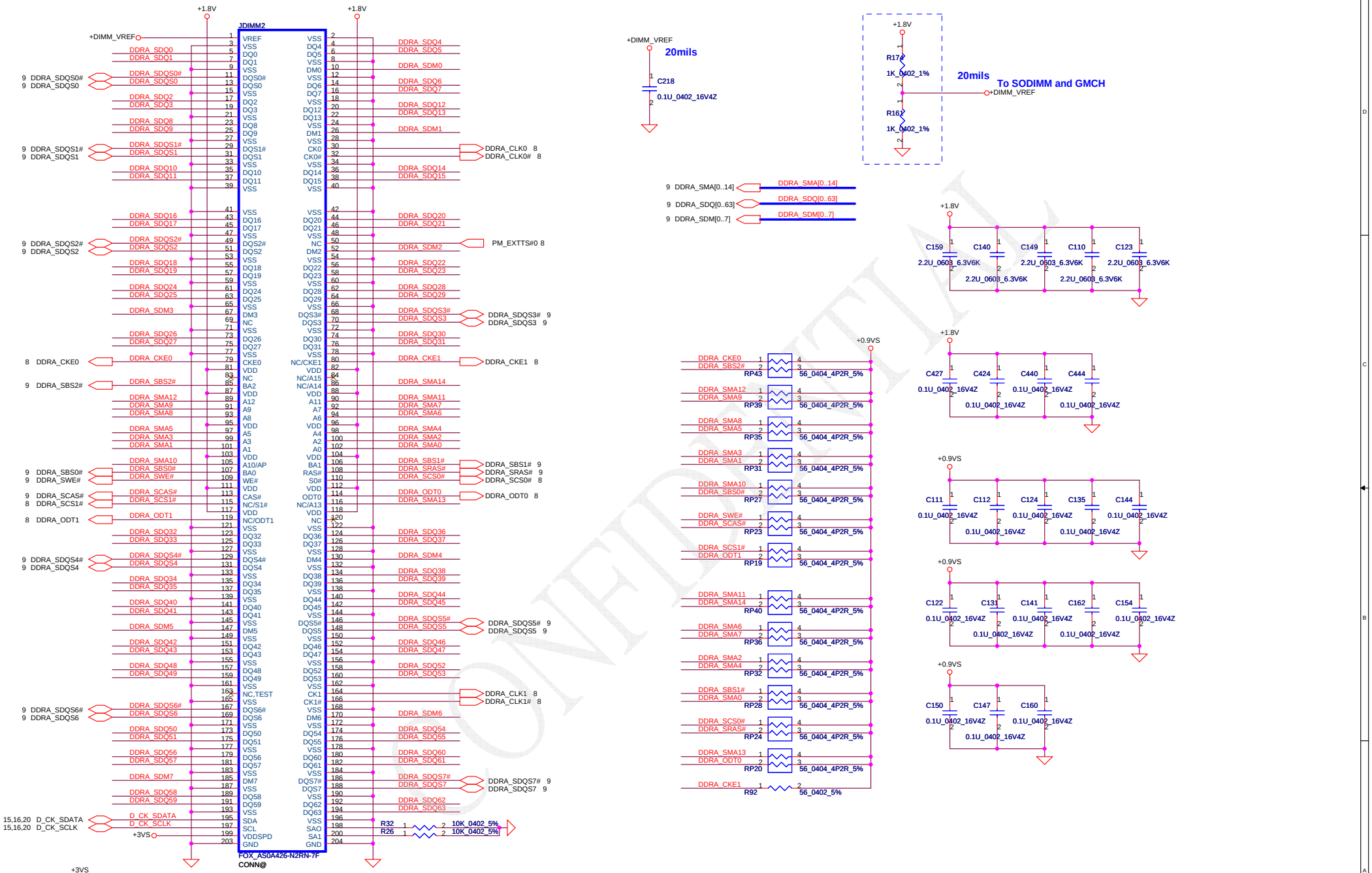

DIMM0 REV H:5.2mm (BOT)

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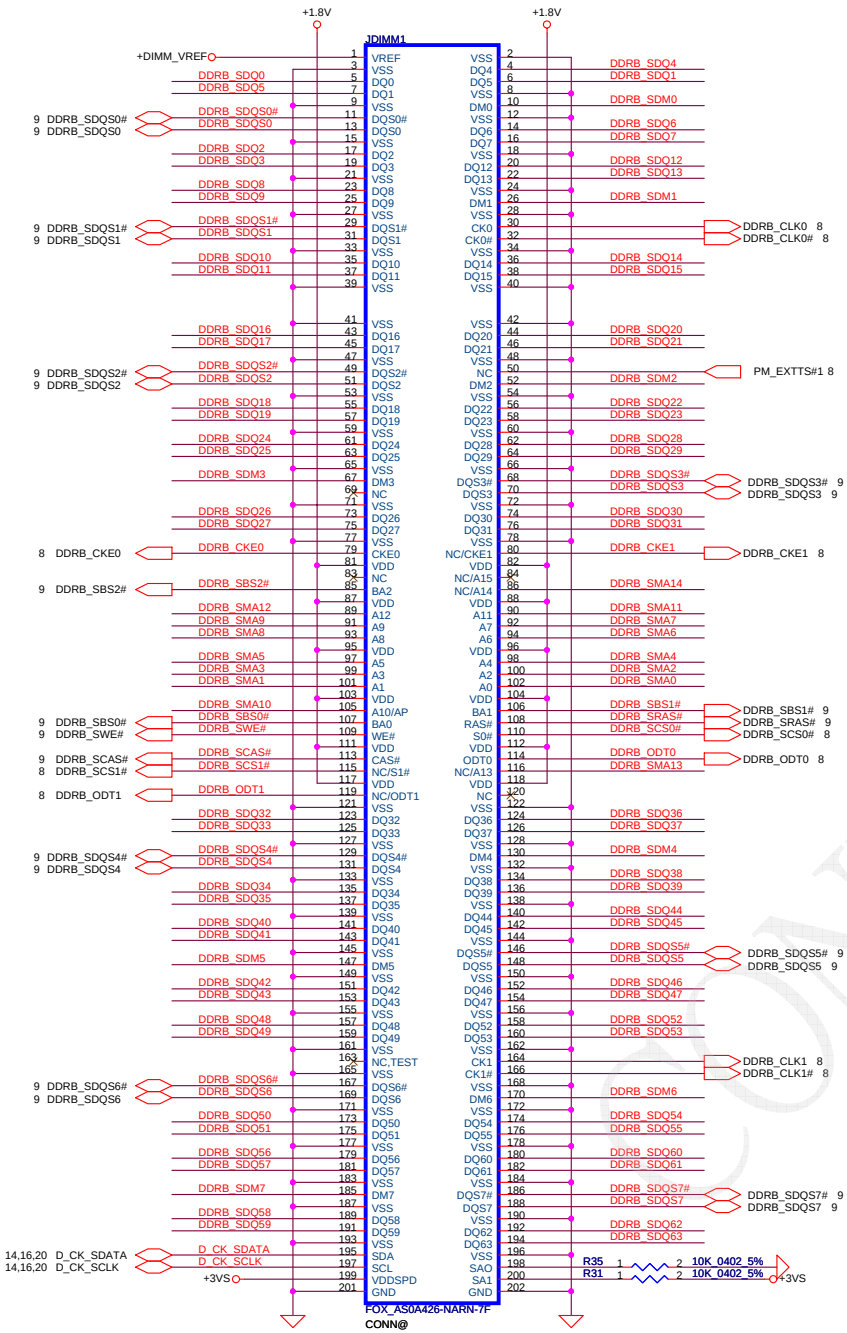
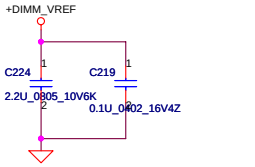
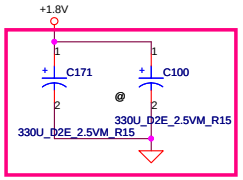
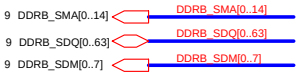
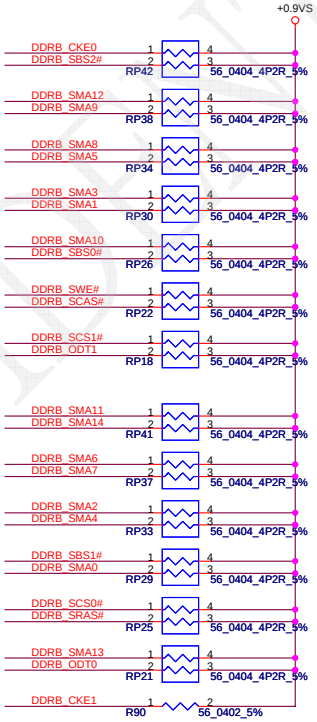


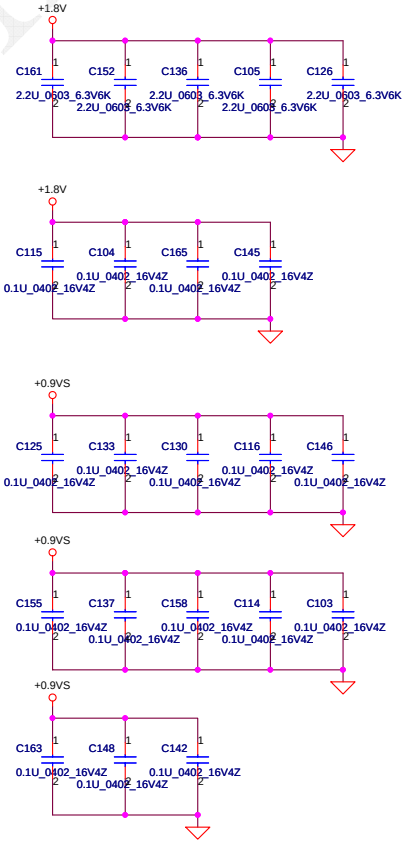
DIMM1 REV H:9.2mm (BOT)











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Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)

mount to Enable ITP_CLK

CLK_PCI5=0, Pin63,64 is SRC_CLK
CLK_PCI5=1, Pin63,64 is ITP_CLK

CLK_PCI4=0, Pin28, 29 is SRC_CLK
Pin24, 25 is DOT96_CLK

For EMI Requrie 10/9

Cardbus usage for JALA0

VGA: disable this pair by BIOS

VGA: disable this pair by BIOS

UMA: disable this pair by BIOS

New Card usage for JAL90

New Card usage for JAL90

PVT

DVT

DVT
SA000020H10
(S IC ICS9LPRS387BKLFT MLF 72P CLK GEN)

PVT2(JALA0)
MP(JALA0)_add part

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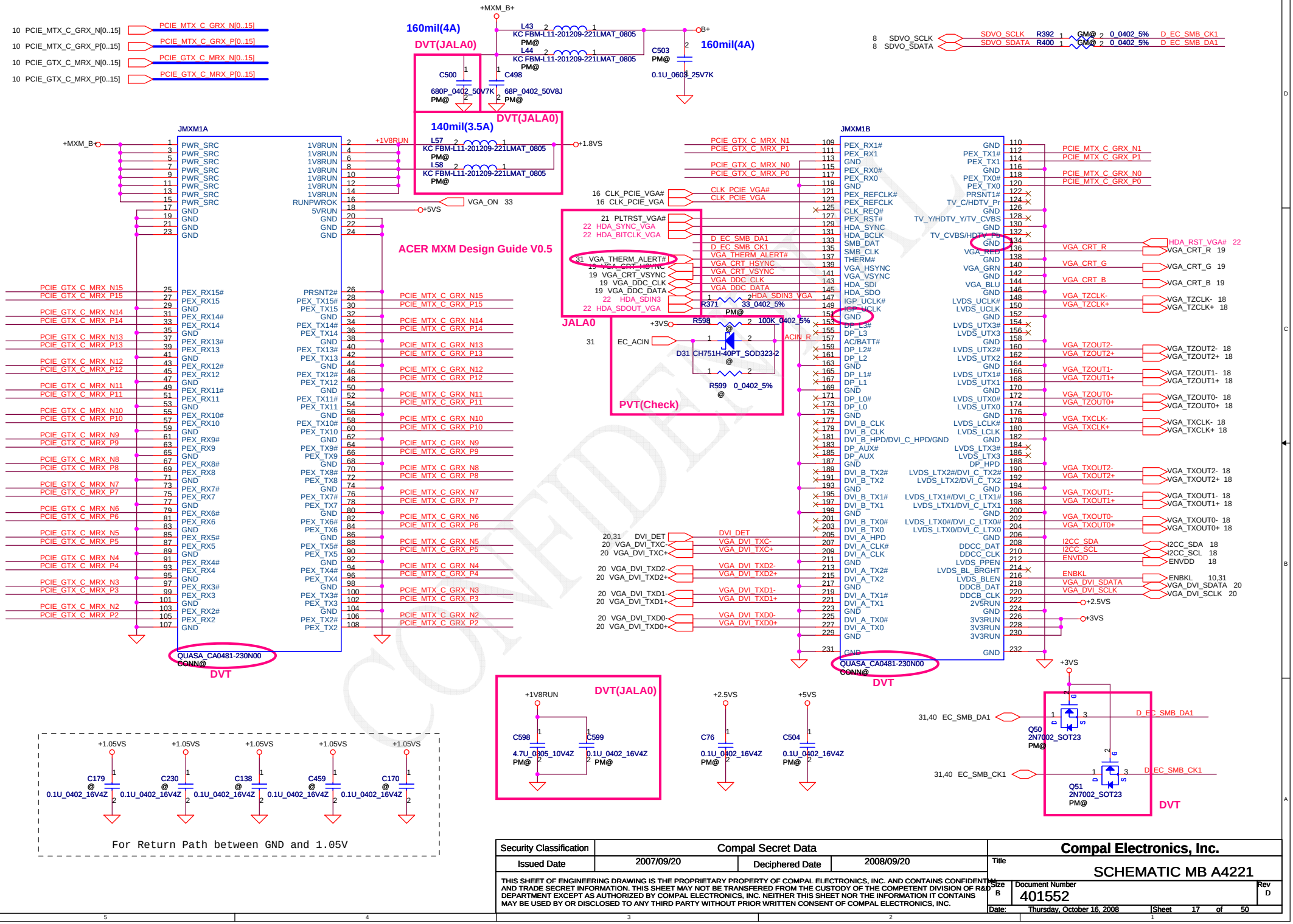

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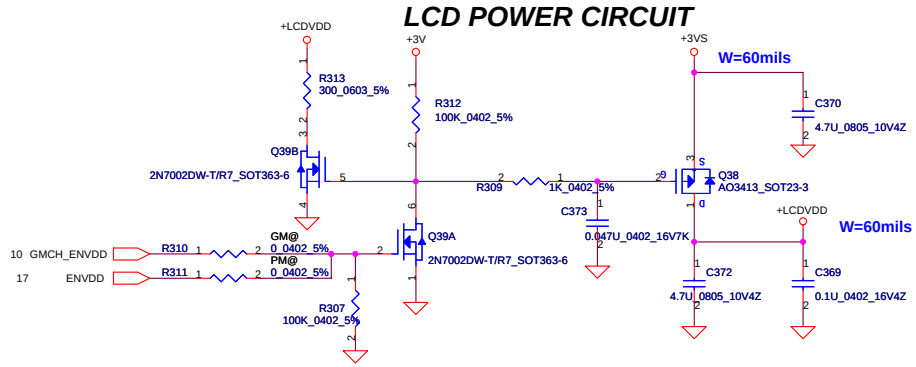
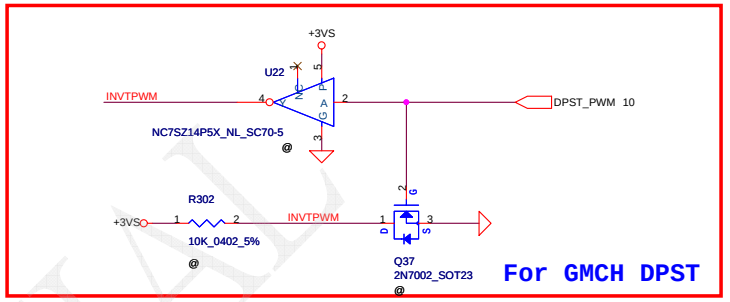
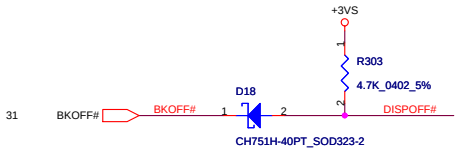
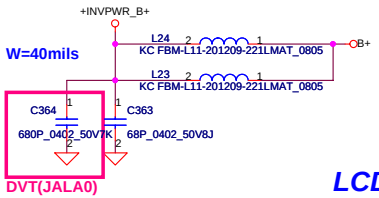
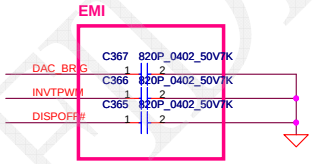
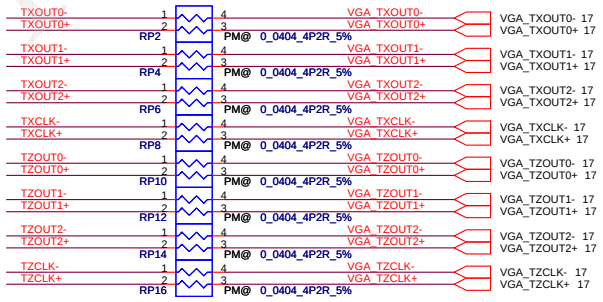


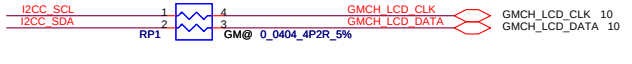


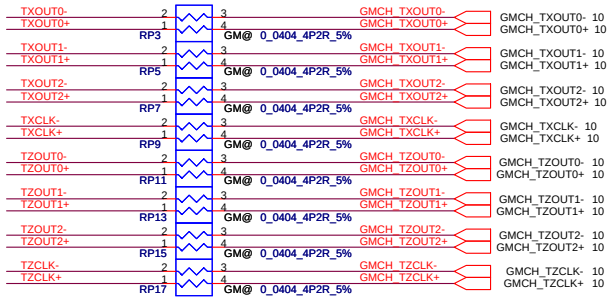




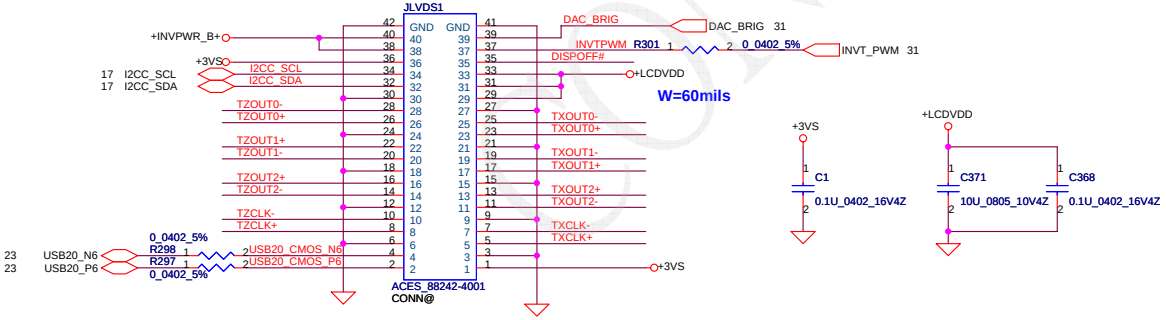








LCD/PANEL BD. Conn.



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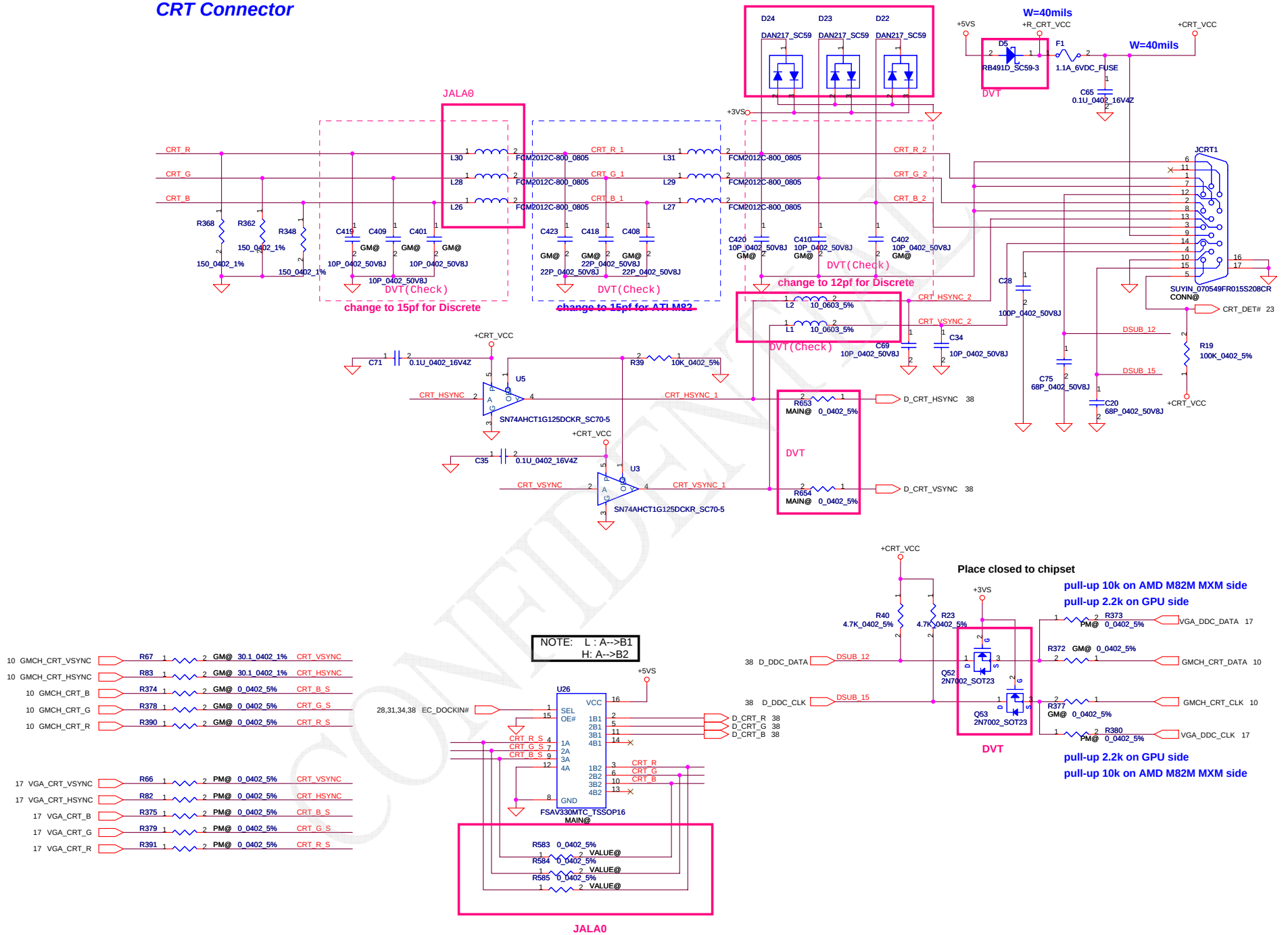
CRT Connector



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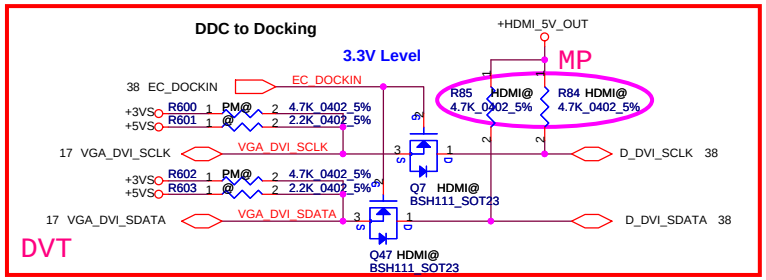

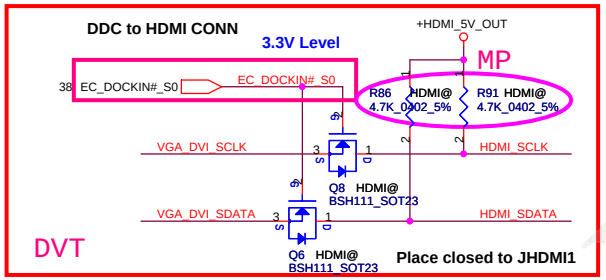

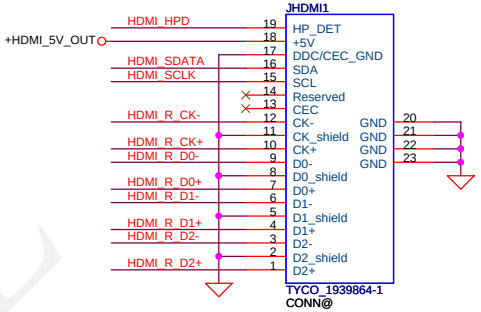

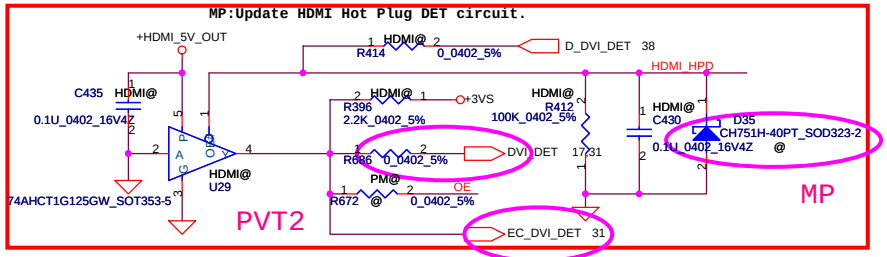

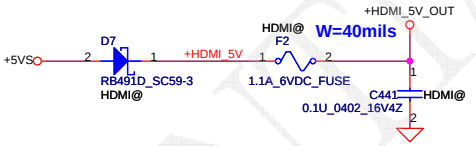

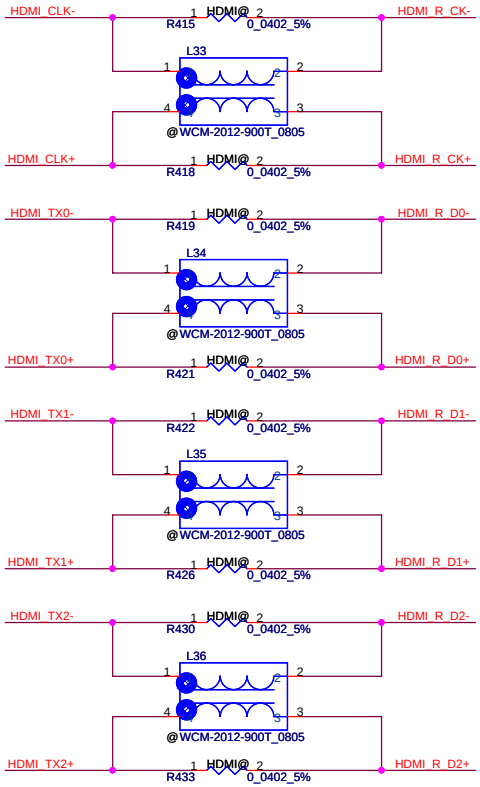

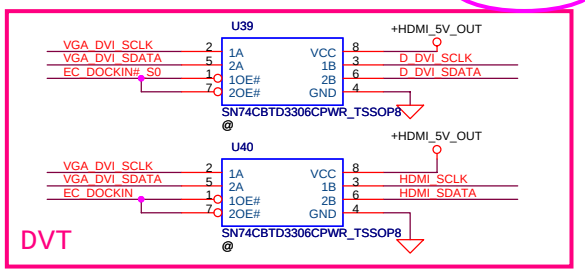

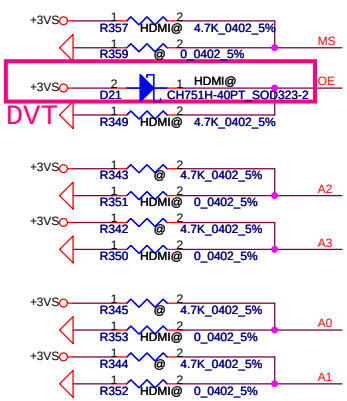

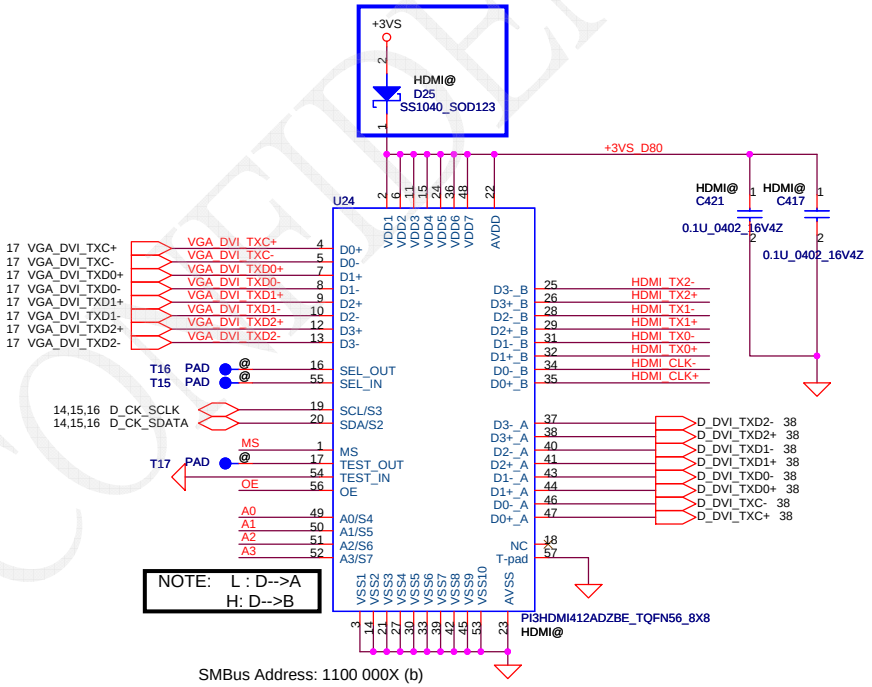

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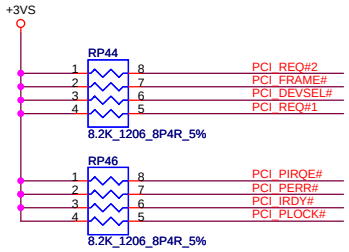
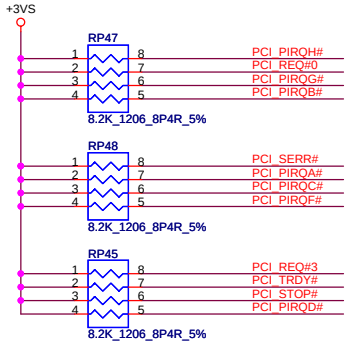
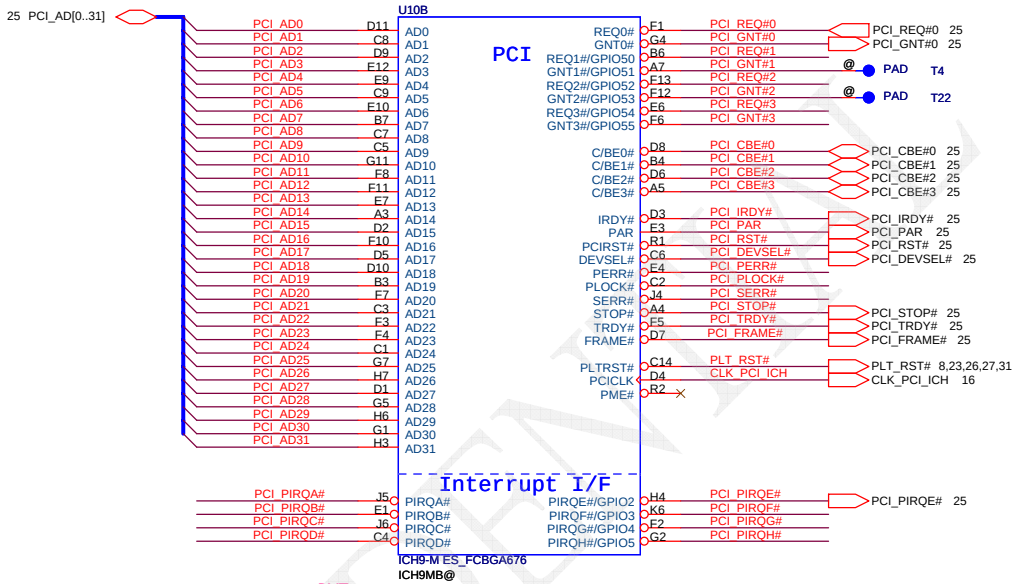
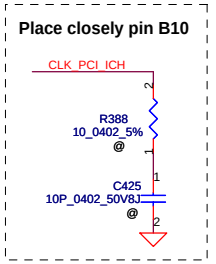




DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



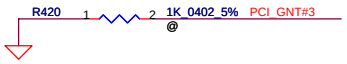


DVT ICH9-M: SA00002AN10
(S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)

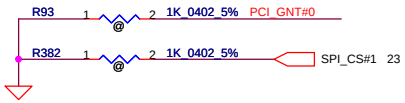
PVT ICH9-M: SA00002JH00
(S IC AF82801IBM QT09 A3 PBG 676P ICH9M)

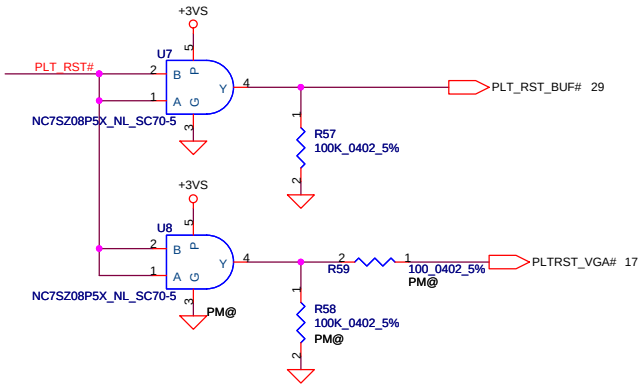
Pre-MP ICH9-M: SA00002JH70
(S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*





For VGA/B

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CMOS Settings	R376
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R381
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN

+RTCVCC
R411 1M_0402_5%
SM_INTRUDER#

+RTCVCC
R408 332K_0402_1%
ICH_INTVRMEN
High = Internal VR Enable

C117 18P_0402_50V8J
C118 18P_0402_50V8J
X1 32.768KHZ_12.5P_MC-306
ICH_RTCX1
ICH_RTCX2
R78 10M_0402_5%

+RTCVCC
R394 20K_0402_5%
close to RAM_door
R376 @ 10K_0603_5%
C426 1U_0603_10V6K

+RTCVCC
R395 20K_0402_5%
close to RAM_door
R381 @ 10K_0603_5%
C453 1U_0603_10V6K

ICH_RTCRST#
ICH_SRTCRST#
SM_INTRUDER#
ICH_INTVRMEN

+3VS
R163 10K_0402_5%
SATA_LED#

+3V
R77 10K_0402_5%
ICH_GPIO56

Need check
+1.5VS_PCIE_ICH
R397 24.9_0402_1%
GLAN_COMP

33 HDA_BITCLK_MDC R467 33_0402_5% HDA_BITCLK_ICH
33 HDA_SYNC_MDC R469 33_0402_5% HDA_SYNC_ICH
33 HDA_RST_MDC# R470 33_0402_5% HDA_RST_ICH#
34 HDA_SDIN0
33 HDA_SDIN1
8 HDA_SDIN2
17 HDA_SDIN3
33 HDA_SDOUT_MDC R468 33_0402_5% HDA_SDOUT_ICH

32 SATA_LED#

SATA for HDD
30 SATA_DTX_C_IRX_N0
30 SATA_DTX_C_IRX_P0
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_ITX_DRX_N0
SATA_ITX_DRX_P0

SATA for ODD
30 SATA_DTX_C_IRX_N1
30 SATA_DTX_C_IRX_P1
SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_ITX_DRX_N1
SATA_ITX_DRX_P1

U10A
ICH9-M ES_FCBGA676
ICH9MB@

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN, LAN100_SLP
LAN / GLAN: GLAN_CLK, LAN_RSTSYNC, LAN_RXD0, LAN_RXD1, LAN_RXD2, LAN_TXD_0, LAN_TXD_1, LAN_TXD_2, GPIO56, GLAN_COMPI, GLAN_COMPO
CPU: HDA_BIT_CLK, HDA_SYNC, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDOUT, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO34, SATALED#
IHDA: SATA0RXN, SATA0RXP, SATA0TXN, SATA0TXP, SATA1RXN, SATA1RXP, SATA1TXN, SATA1TXP
SATA: SATA4RXN, SATA4RXP, SATA4TXN, SATA4TXP, SATA5RXN, SATA5RXP, SATA5TXN, SATA5TXP, SATA_CLKN, SATA_CLKP, SATARBIAS#, SATARBIAS
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23

LPC_AD0 31
LPC_AD1 31
LPC_AD2 31
LPC_AD3 31
LPC_FRAME# 31
R423 10K_0402_5% +3VS
EC_GA20 31
H_A20M# 4
R462 0_0402_5% H_DPRSTP#
R463 0_0402_5% H_DPSLP#
H_DPRSTP# 5,8,46
H_DPSLP# 5
H_FERR# 4
R461 56_0402_5%
H_PWRGOOD 5
H_IGNNE# 4
H_INIT# 4
H_INTR 4
EC_KBRST# 31
H_NMI 4
H_SMI# 4
H_STPCLK# 4
R460 54.9_0402_1% H_THERMTRIP#
H_THERMTRIP# 4,8
TP12

R258 need to place within 2" of ICH9M
R257 must be place within 2" of R258 w/o stub.

+1.05VS
H_DPRSTP# R476 @ 56_0402_5%
H_DPSLP# R477 @ 56_0402_5%
R475 56_0402_5%
R428 10K_0402_5% +3VS

CLK_PCIE_SATA# 16
CLK_PCIE_SATA 16
SATARBIAS
R162 24.9_0402_1%
10mils width less than 500mils

DVT ICH9-M: SA00002AN10
(S IC NH82801IBM QP23 A2 FCBGA 676P ICH9M)
PVT ICH9-M: SA00002JH00
(S IC AF82801IBM QT09 A3 PBG 676P ICH9M)
Pre-MP ICH9-M: SA00002JH70
(S IC AF82801IBM SLB8Q A3 676P ICH9M ABO!)

close ICH9
C506 0.01U_0402_16V7K
C505 0.01U_0402_16V7K
C502 0.01U_0402_16V7K
C501 0.01U_0402_16V7K

HDA for AUDIO
34 HDA_BITCLK_AUDIO R471 33_0402_5% HDA_BITCLK_ICH
34 HDA_SYNC_AUDIO R473 33_0402_5% HDA_SYNC_ICH
34 HDA_RST_AUDIO# R456 33_0402_5% HDA_RST_ICH#
34 HDA_SDOUT_AUDIO R472 33_0402_5% HDA_SDOUT_ICH

HDA for GMCH
8 HDA_BITCLK_MCH GM@ R457 33_0402_5% HDA_BITCLK_ICH
8 HDA_SYNC_MCH GM@ R459 33_0402_5% HDA_SYNC_ICH
8 HDA_RST_MCH# GM@ R466 33_0402_5% HDA_RST_ICH#
8 HDA_SDOUT_MCH GM@ R458 33_0402_5% HDA_SDOUT_ICH

HDA for VGA
17 HDA_BITCLK_VGA PM@ R480 33_0402_5% HDA_BITCLK_ICH
17 HDA_SYNC_VGA PM@ R479 33_0402_5% HDA_SYNC_ICH
17 HDA_RST_VGA# PM@ R478 1K_0402_5% HDA_RST_ICH#
17 HDA_SDOUT_VGA PM@ R481 33_0402_5% HDA_SDOUT_ICH
DVT(Check)

+VCC_HDA_ICH
R454 1K_0402_5% @ HDA_SDOUT_ICH
ICH_TP3 23
R72 1K_0402_5% @

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap

GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

MAINPWON 40,41
R175 @ 330_0402_5%
+1.05VS
Q14 2SC2411K_SOT23 @
H_THERMTRIP#

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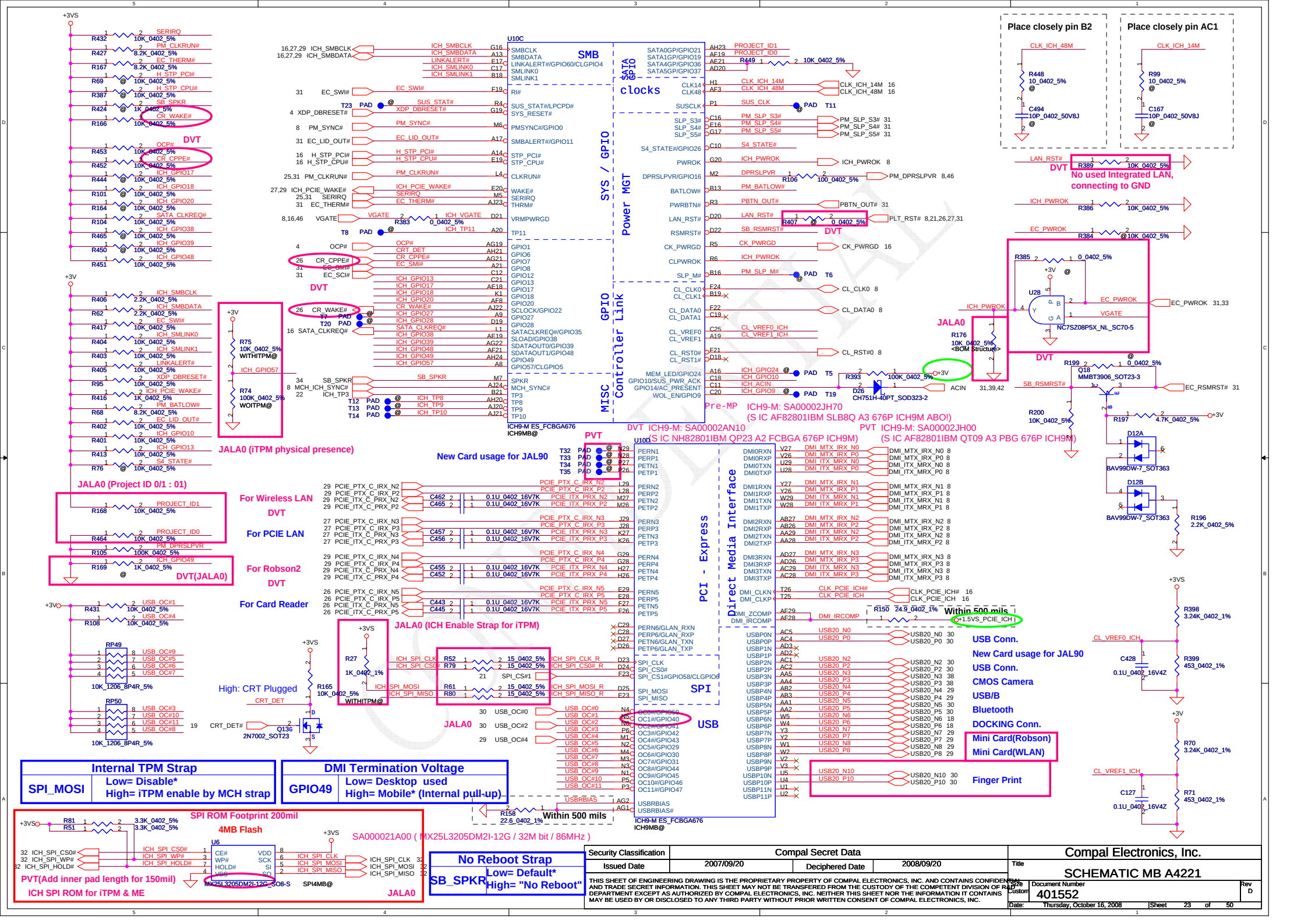

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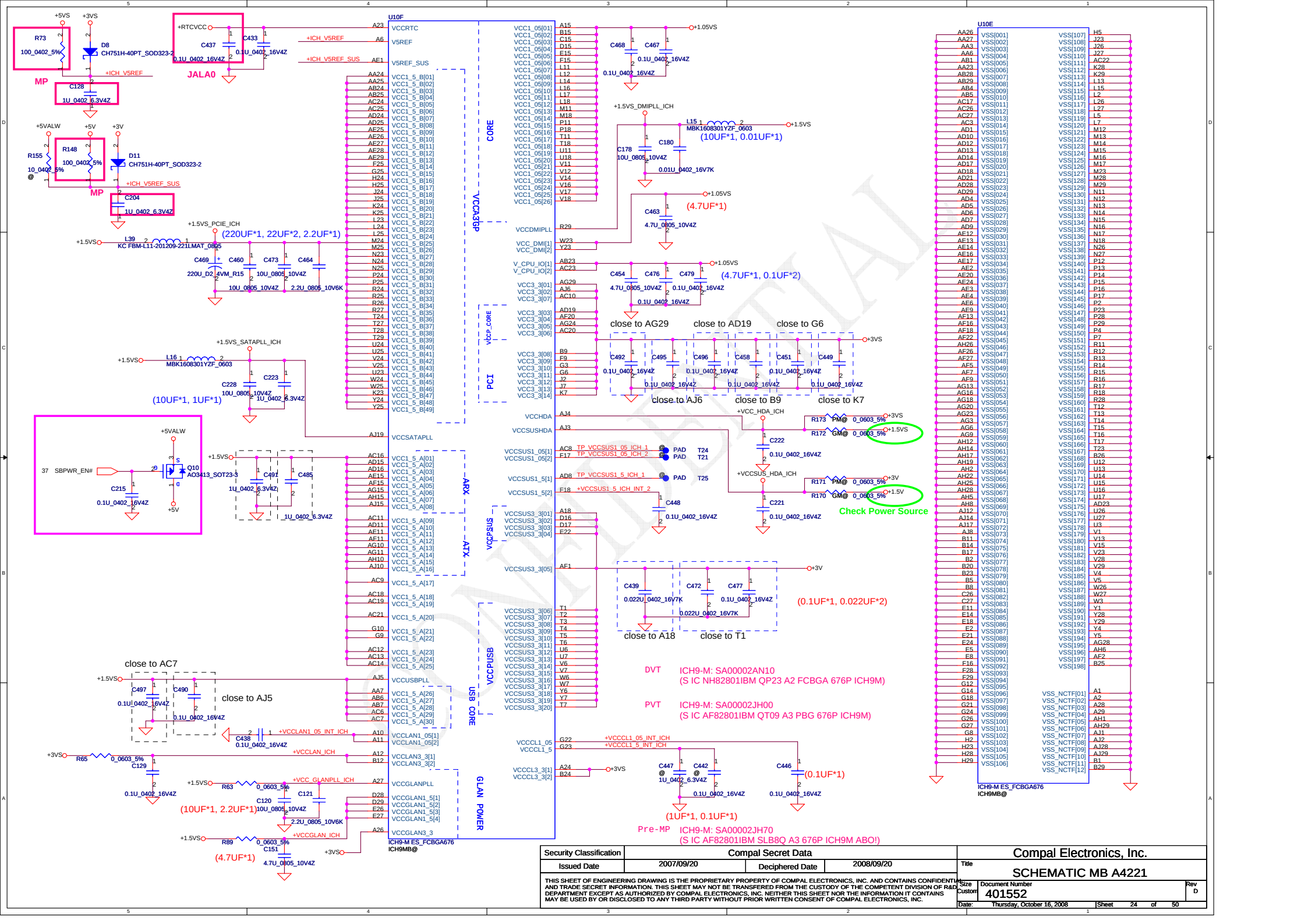

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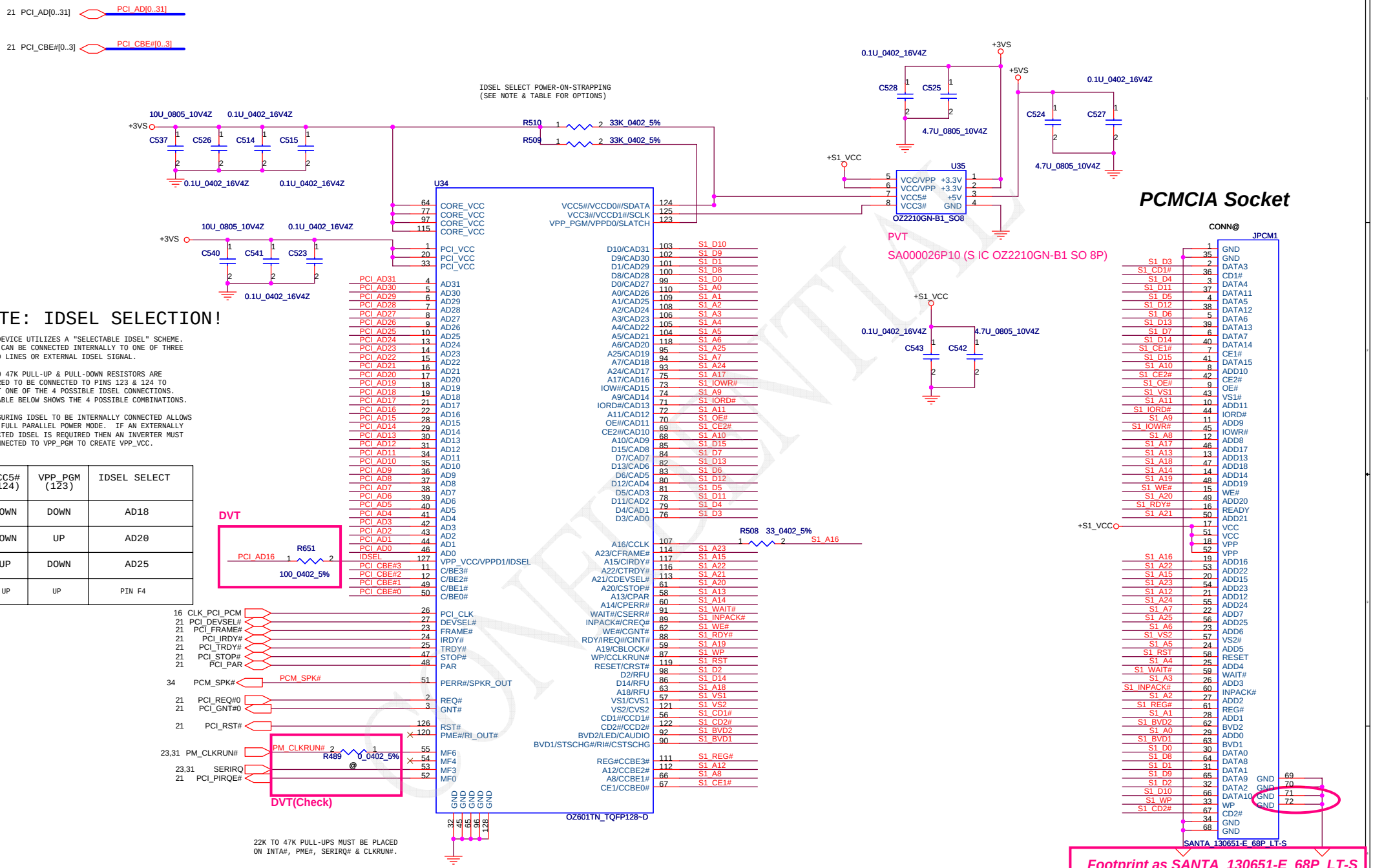

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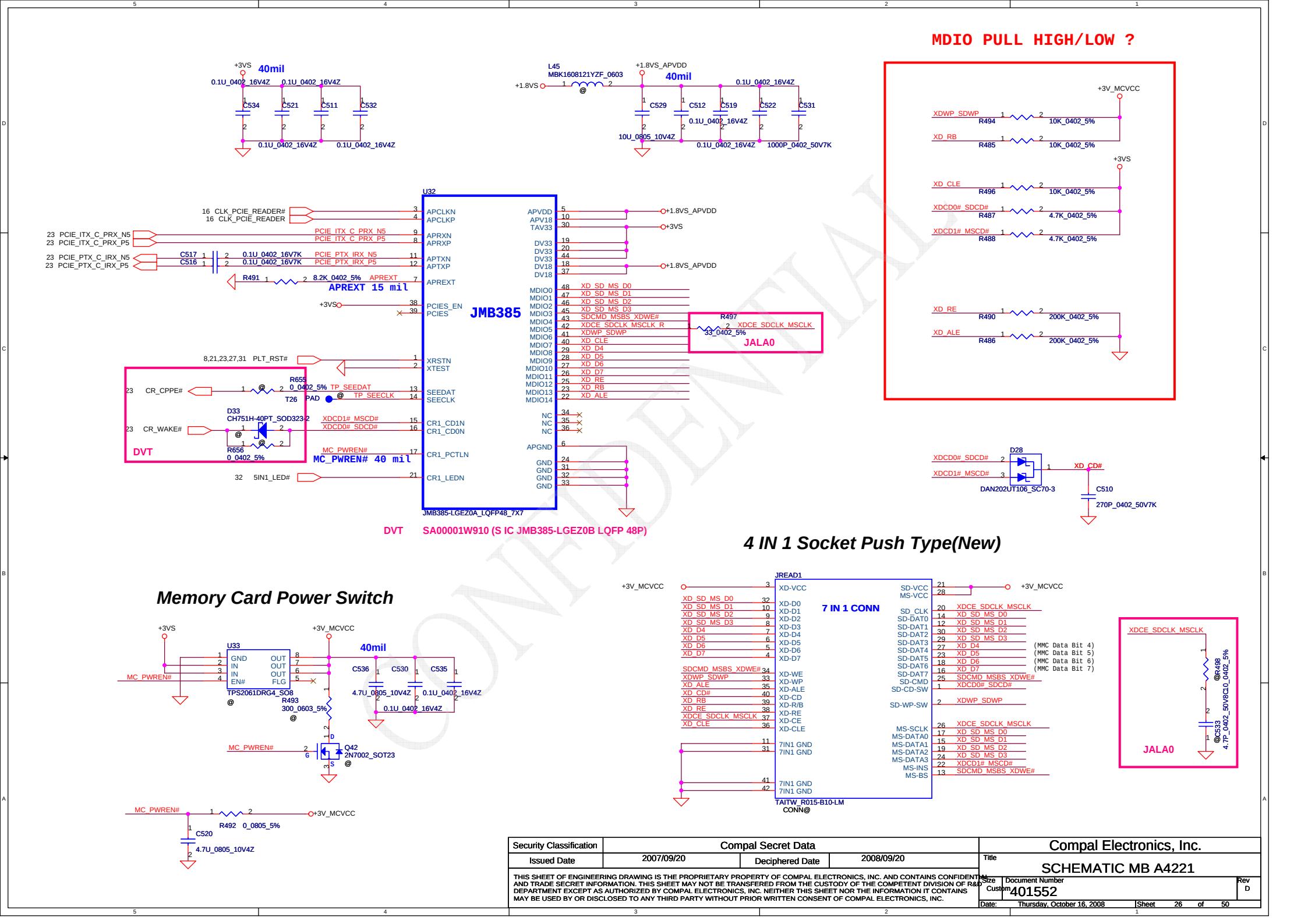

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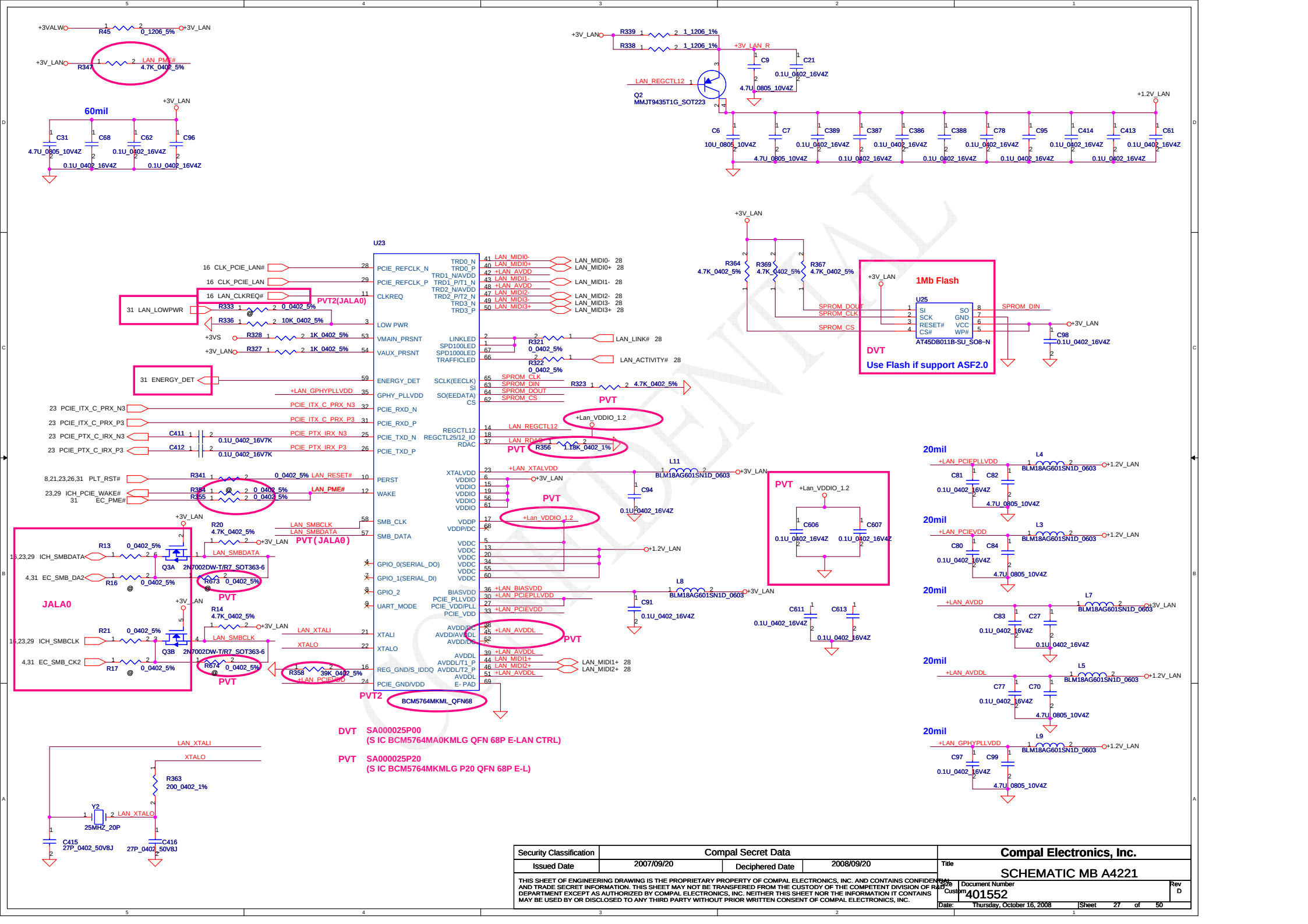

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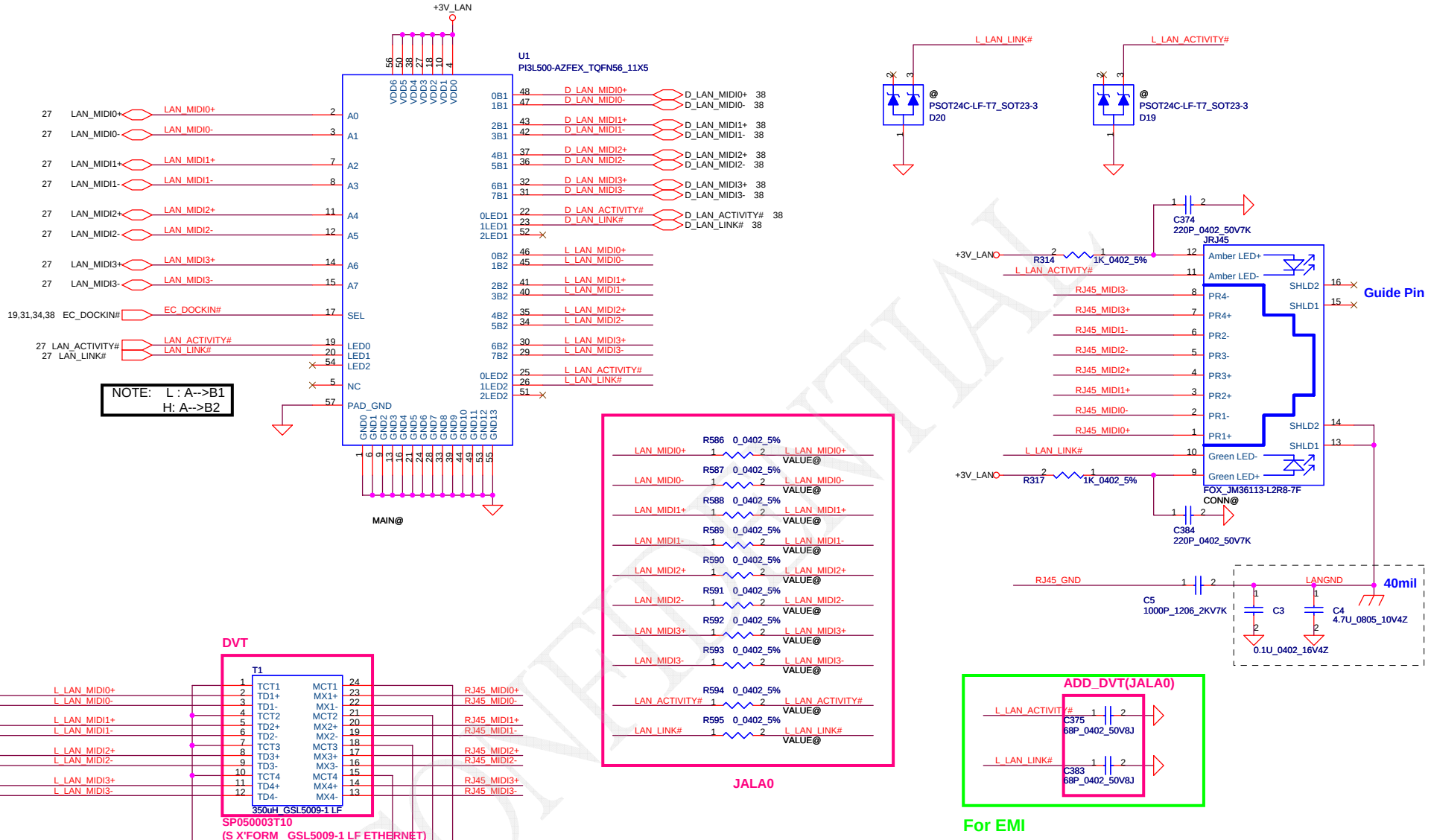

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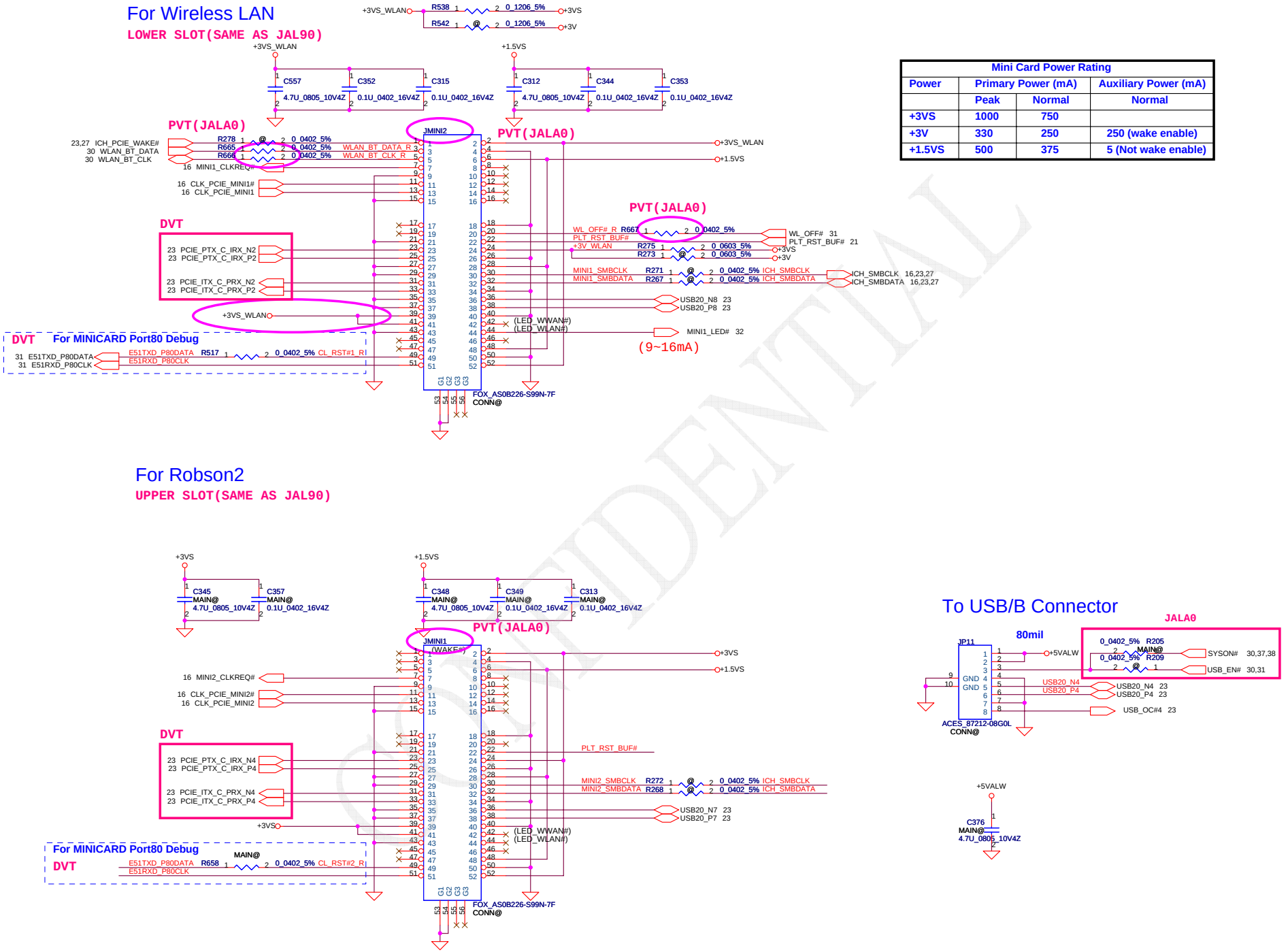

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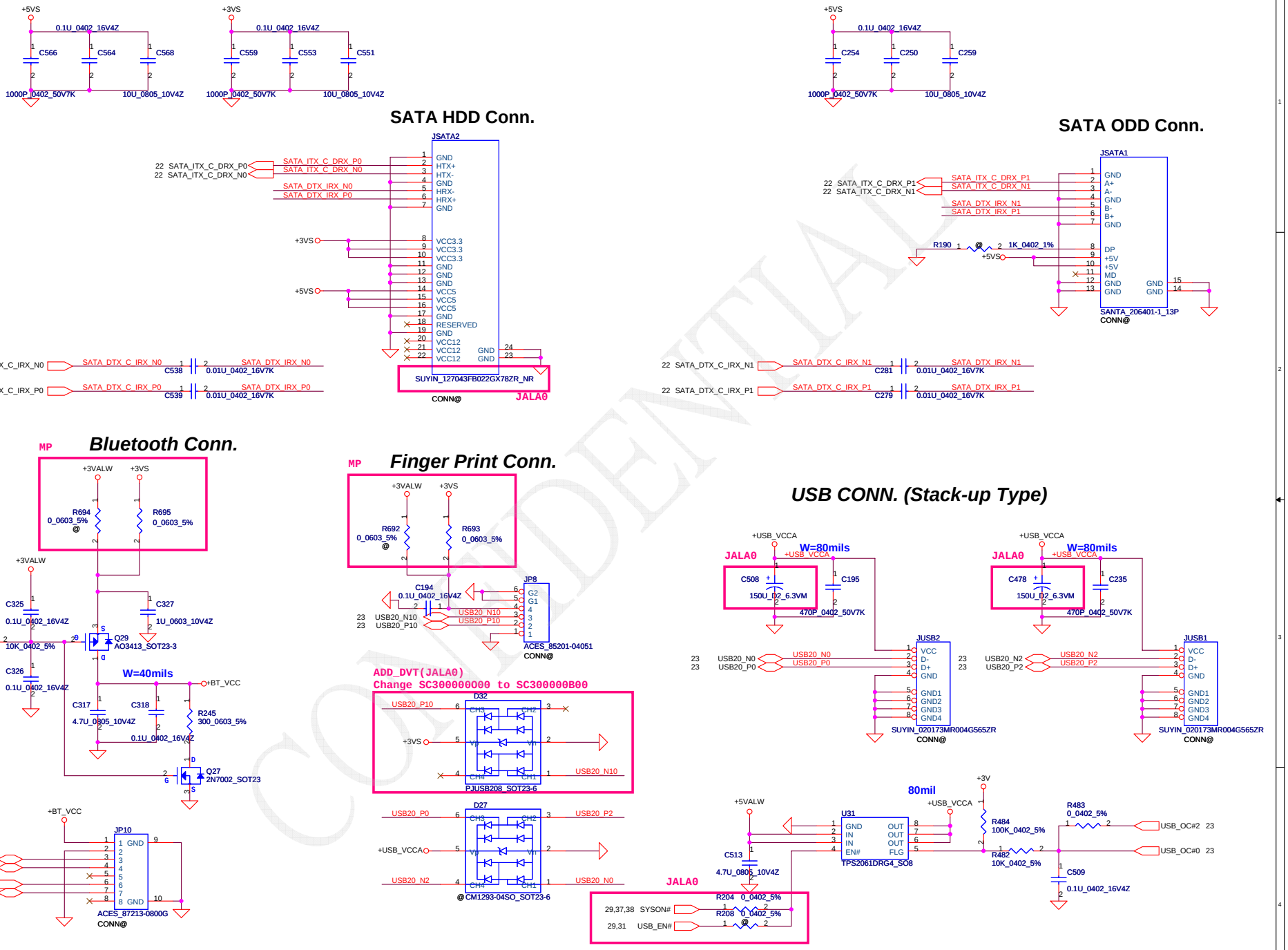

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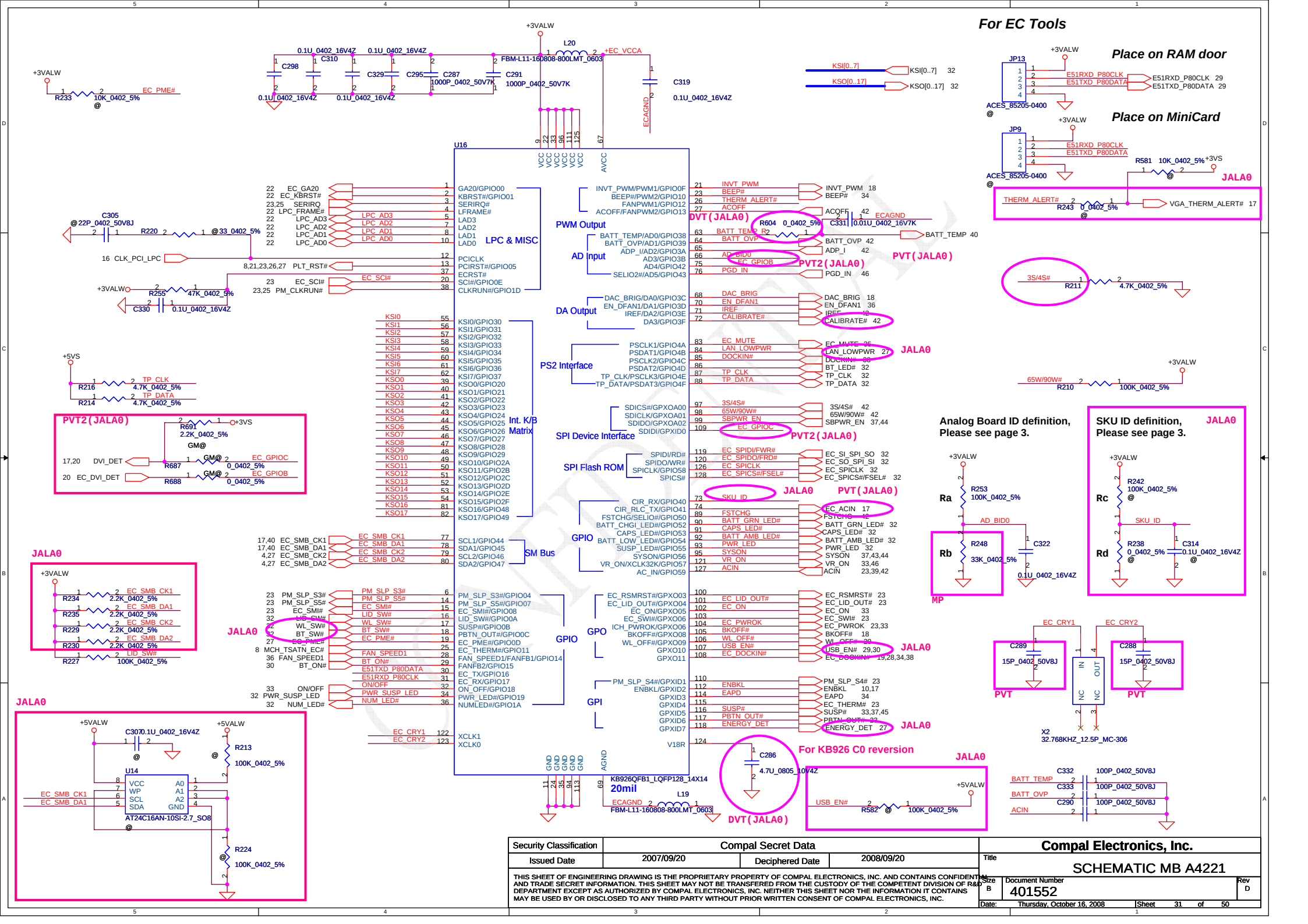
For EC Tools
Place on RAM door
Place on MiniCard
U16
KB926QFB1_LQFP128_14X14
20mil
AT24C16AN-10SI-2.7_SO8
U14
Analog Board ID definition, Please see page 3.
SKU ID definition, Please see page 3.
For KB926 C0 reversion
PVT2(JALA0)
DVT(JALA0)
PVT(JALA0)
JALA0
MP
PVT
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Security Classification
Compal Secret Data
Issued Date
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2MB : SA00001IT00 (MXIC , S IC FL 16MBIT MX25L1605AM2C-12G SO8 ROM , 85MHz)
2MB : SA00001OZ00 (WINBOND , S IC FL 32MBIT W25X32VSSIG SOIC 8P 3.3V , 75MHz)

DVT(JALA0) SYS & EC & FP(PBA) & HDCP

+3VALW R239 0_0603_5% C299 0.1U_0402_16V4Z +SPI_VCC

U15 MX25L1605AM2C-12G_SOP8

31 EC_SPICS#/FSEL# R225 4.7K_0402_5% SPI_WP# R219 4.7K_0402_5% SPI_HOLD# +3VALW

R226 R232 R218 0_0402_5% EC_SPICLK 31 EC_SO_SPI_SI 31 EC_SI_SPI_SO 31

2MB Flash
SPI ROM Footprint 200mil

U17 MX25L512AMC-12G_SO8 @
EC_SPICS#/FSEL# SPI_WP# SPI_HOLD# +SPI_VCC EC_SPICLK_R EC_SO_SPI_SI EC_SI_SPI_SO

Reserved for BIOS simulator.
Footprint SO8
SPI ROM Footprint 150mil

ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

INT_KBD Conn.

KSI[0..7] KSI[0..7] 31
KSO[0..17] KSO[0..17] 31

JP3 ACES_88747-2601 CONN@

(Left) KSO0–KSO17 KSI0–KSI7
(Right) KSO15–KSO0 KSI0–KSI7

KSO16 C58 KSO17 C59 KSI2 C64 KSO9 C45 KSI3 C53 KSO8 C44
KSO0 C36 KSI5 C55 KSI6 C50 KSI7 C51
KSO15 C57 KSO14 C56 KSO13 C49 KSO12 C48
KSI0 C60 KSO11 C47 KSO10 C46 KSI1 C32
KSO7 C43 KSO6 C42 KSO5 C41 KSO4 C40
KSO3 C39 KSI4 C54 KSO2 C38 KSO1 C37

@100P_0402_50V8J

To POWER/B(BTN/B)

DVT(JALA0)

JP6 ACES_85201-1205 CONN@

PWR_LED# PWR_SUSP_LED# KSI4 KSI3 KSI2 KSO0 KSI5 KSI6 KSI7
ON/OFFBTN# 33 LID_SW# 31
+3VALW +5VS +5VALW

To FUN/B(LED/B)

JP5 ACES_85201-10051 CONN@

+5VS KSO0 KSI1 KSI5 KSI6 KSI7 MEDIA_LED#
CAPS_LED# 31 NUM_LED# 31

	KSO0
KSI1	PRESENTATION
KSI2	Program_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#
KSI6	SYNC
KSI7	LOCK

To TP/B Conn.

JP7 ACES_85201-0605 CONN@

31 TP_CLK 31 TP_DATA +5VS TP_CLK TP_DATA LEFT_BTN# RIGHT_BTN#
C199 100P_0402_50V8J C198 100P_0402_50V8J
C197 0.1U_0402_16V4Z
D10 @ PSOT24C_SOT23
SW1 SMT1-05-A_4P <BOM Structure> LEFT_BTN#
SW2 SMT1-05-A_4P RIGHT_BTN#

PWR_LED# PWR_SUSP_LED#
31 PWR_LED R262 10K_0402_5% Q31A 2N7002DW-T/R7_SOT363-6
31 PWR_SUSP_LED R258 10K_0402_5% Q31B 2N7002DW-T/R7_SOT363-6

Compal Footprint

4 2
3 1

PVT(JALA0)_Check

(AMB/GREEN) HT-297DQ-GQ_AMB-YG LED1
+5VALW R290 453_0402_1% PWR_SUSP_LED#
+5VS R291 240_0402_5% PWR_LED#
MP(JALA0)

(AMB/GREEN) HT-297DQ-GQ_AMB-YG LED2
+5VALW R293 453_0402_1% BATT_AMB_LED# BATT_AMB_LED# 31
+5VALW R294 240_0402_5% BATT_GRN_LED# BATT_GRN_LED# 31
MP(JALA0)

R296 LED4 (AMB) +3VS 300_0402_5% HT-191UD_Amber_0603 MINI1_LED# MINI1_LED# 29

R292 LED3 (BLUE) +5VS 300_0402_5% HT-191NBQA_BLUE_0603 BT_LED# BT_LED# 31

DVT(JALA0)

+3VALW D17 DAN217_SC59 @ R288 100K_0402_5% WL_SW# 31
SW3 SSS-12R-V-T/R_4P
Wireless SWITCH

SN200001B00 (DIPTRONICS , S DIP SW SSS-12R-V-T/R 1P2T DIPTRO H2 4P)
SN200001G00 (MISAKI , S DIP SW NSS607-212N-EEEG1T 1P2T MISAKI H2 4P)

+3VALW D16 DAN217_SC59 @ R287 100K_0402_5% BT_SW# 31
SW4 SSS-12R-V-T/R_4P
BT SWITCH

JALA0

PVT(JALA0) @ U4 MX25L512AMC-12G_SO8
23 ICH_SPI_CS0# ICH_SPI_WP# ICH_SPI_HOLD# +3VS ICH_SPI_CLK ICH_SPI_MOSI ICH_SPI_MISO 23

Reserved for BIOS simulator.
Footprint SO8
SPI ROM Footprint 150mil

+3VS Q11A 2N7002DW-T/R7_SOT363-6
26 5IN1_LED# 22 SATA_LED# SATA_LED# MEDIA_LED#
Q11B 2N7002DW-T/R7_SOT363-6

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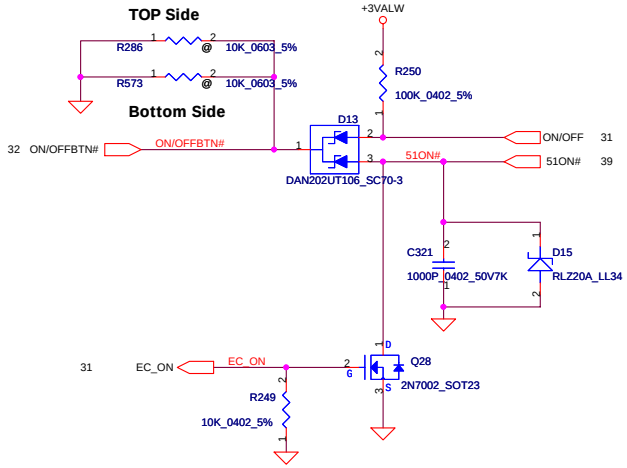
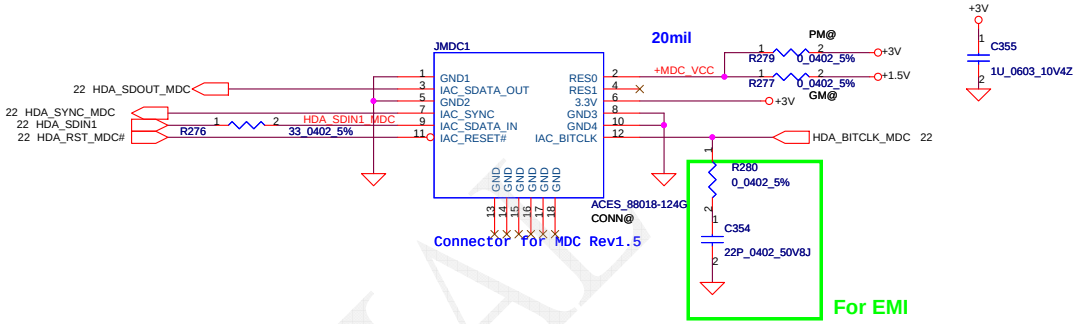
Power Button

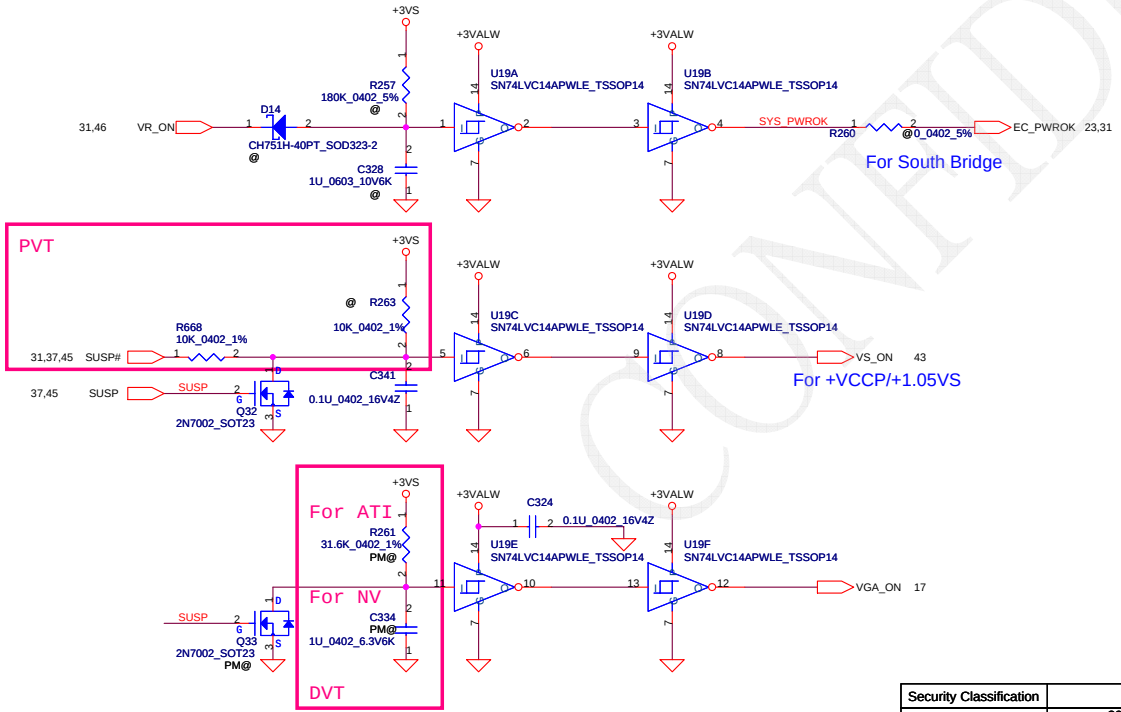
ON/OFF switch

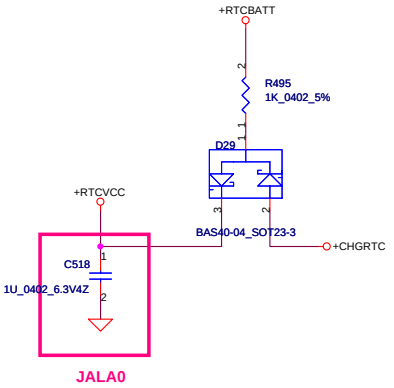


HDA MDC Conn.



Power ON Circuit





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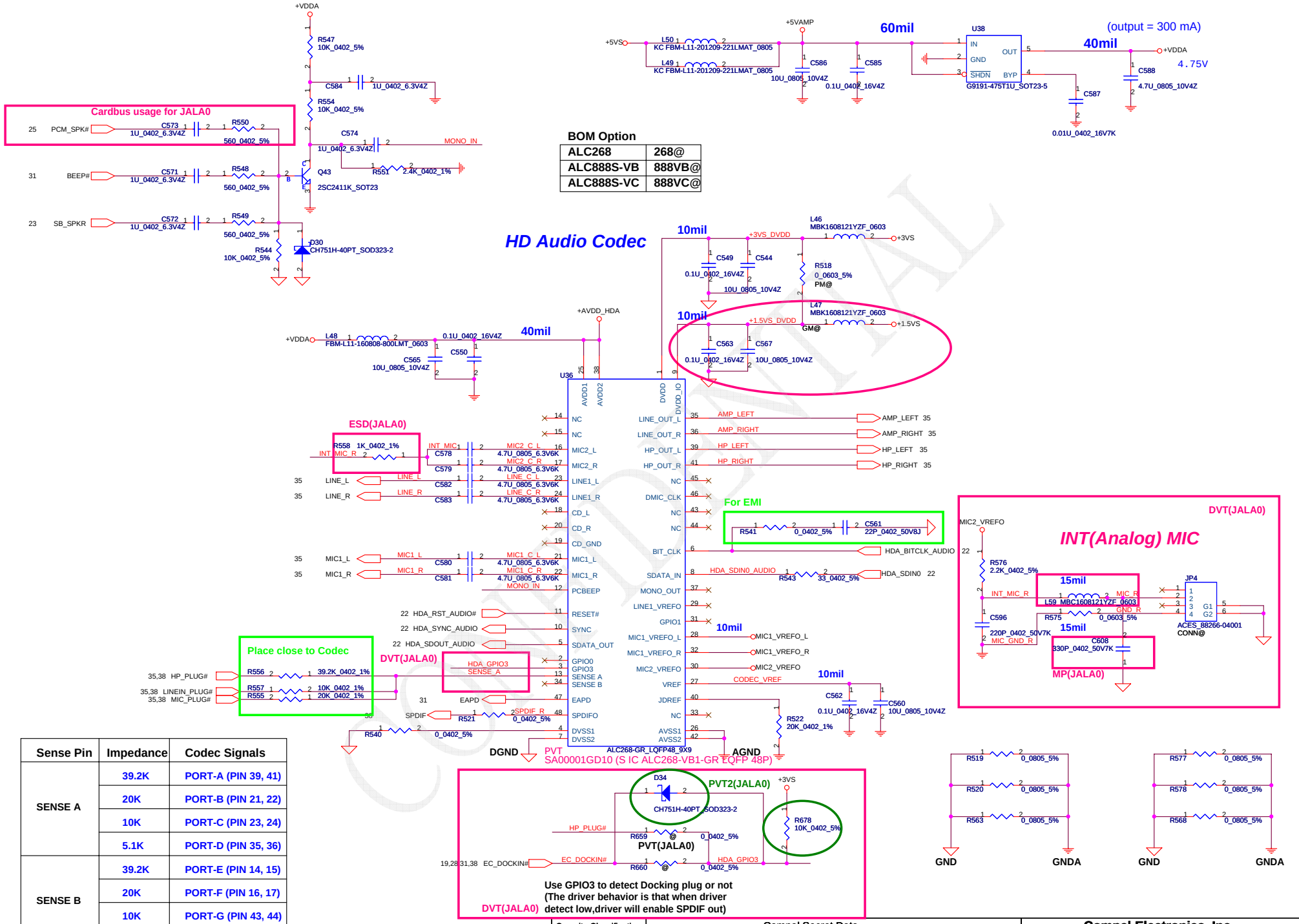

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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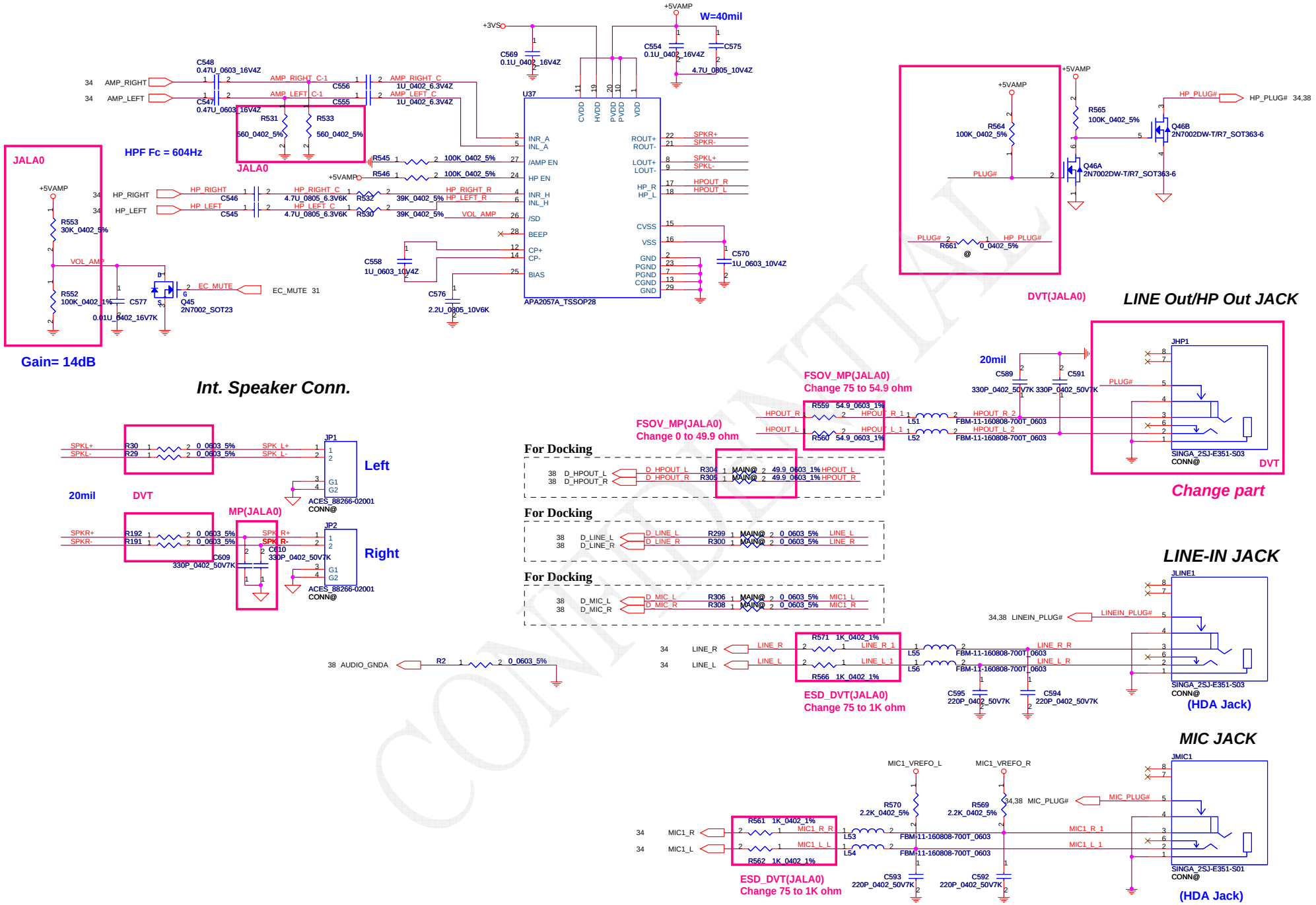

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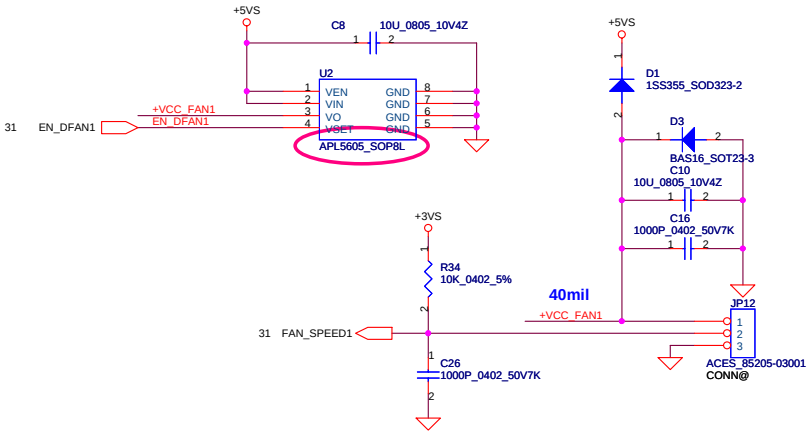
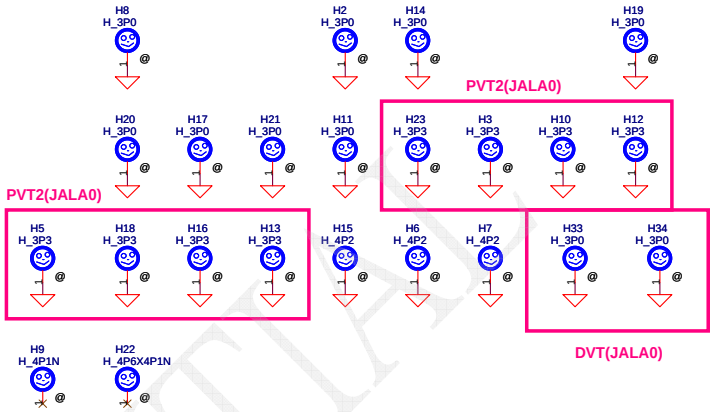
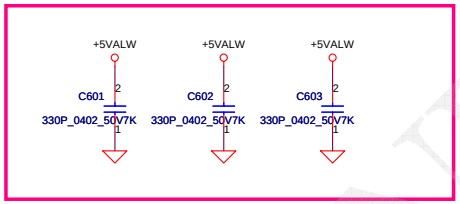
FAN1 Conn



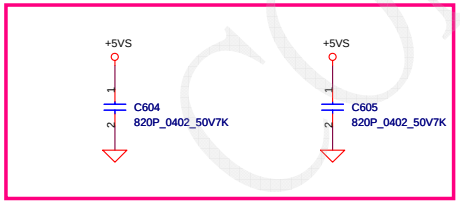


EMI



ADD_DVT(JALA0)

EMI



ADD_PVT(JALA0)

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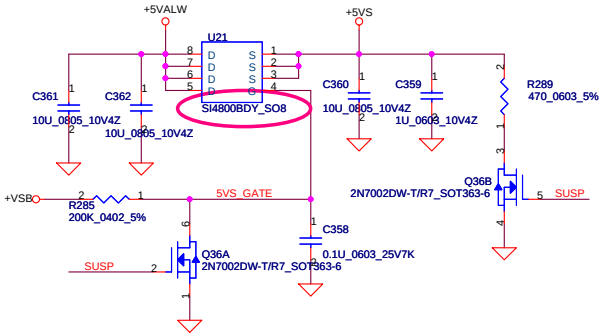
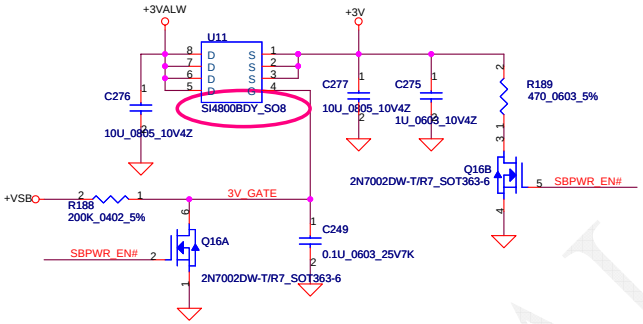
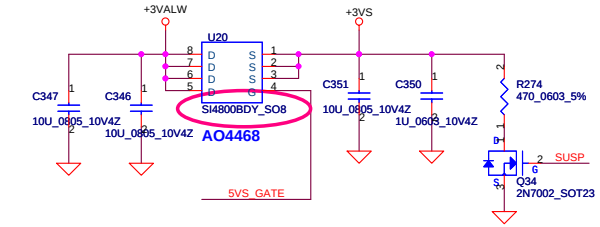
+5VALW TO +5VS



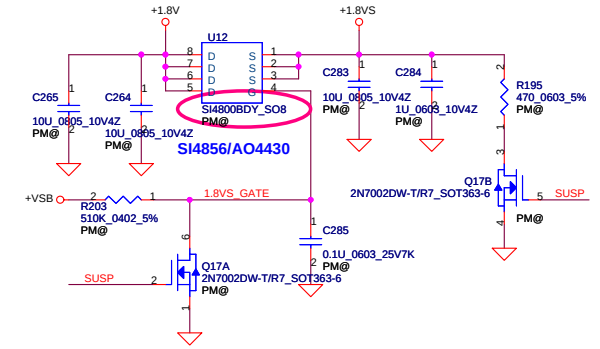
+3VALW TO +3V(ICH9M AUX Power)



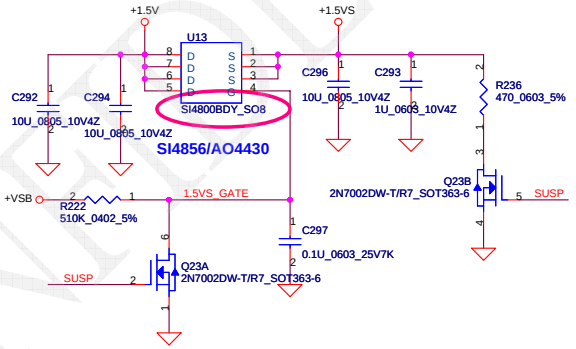
+3VALW TO +3VS

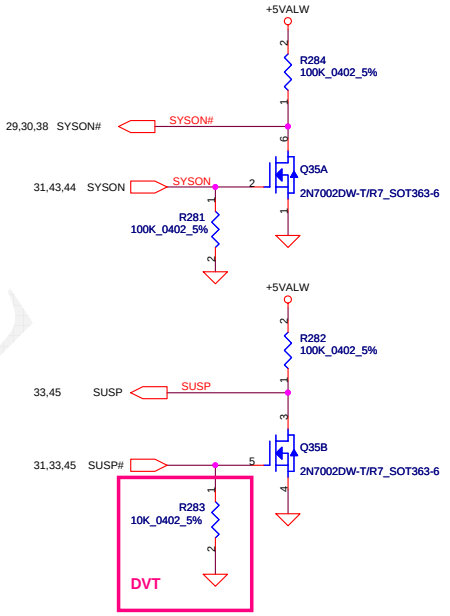


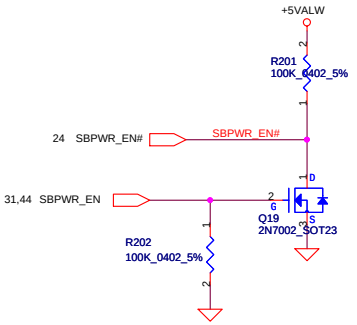
+1.8V to +1.8VS

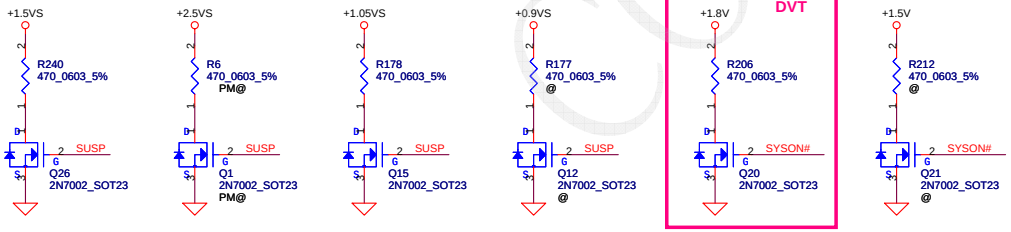


+1.5V to +1.5VS









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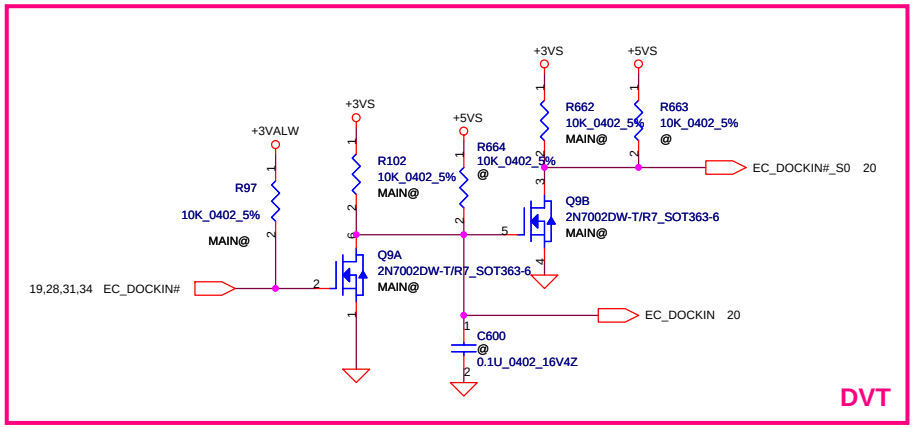
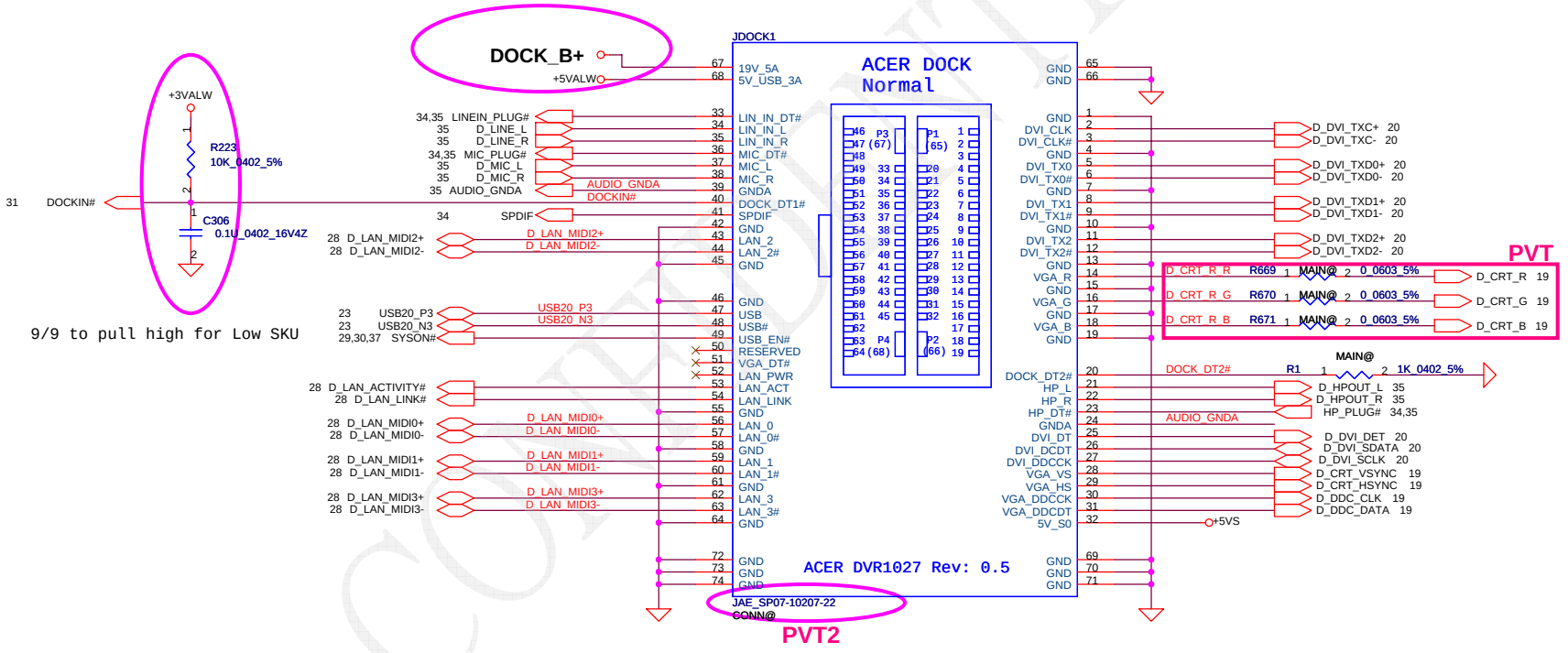


10/15 Acer DVR 1028 Rev0.3



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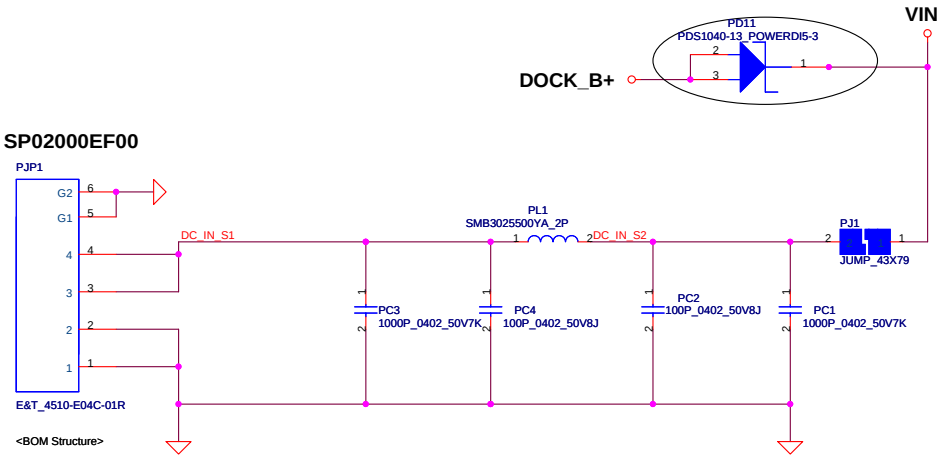
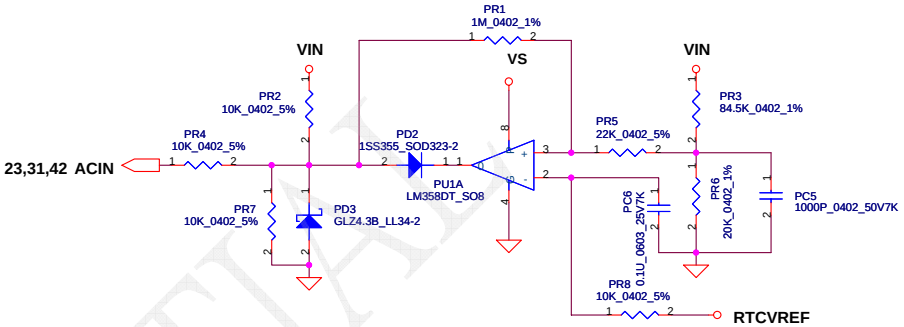
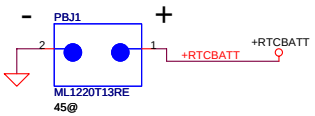
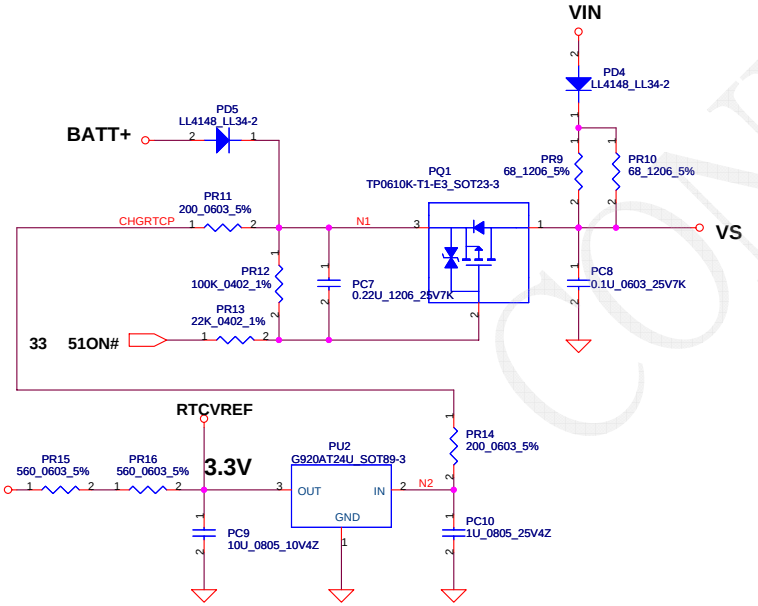
Place at HW side

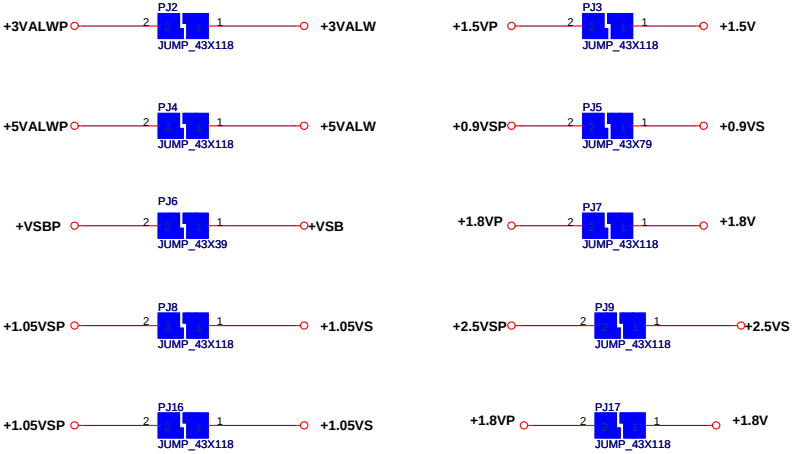




Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V







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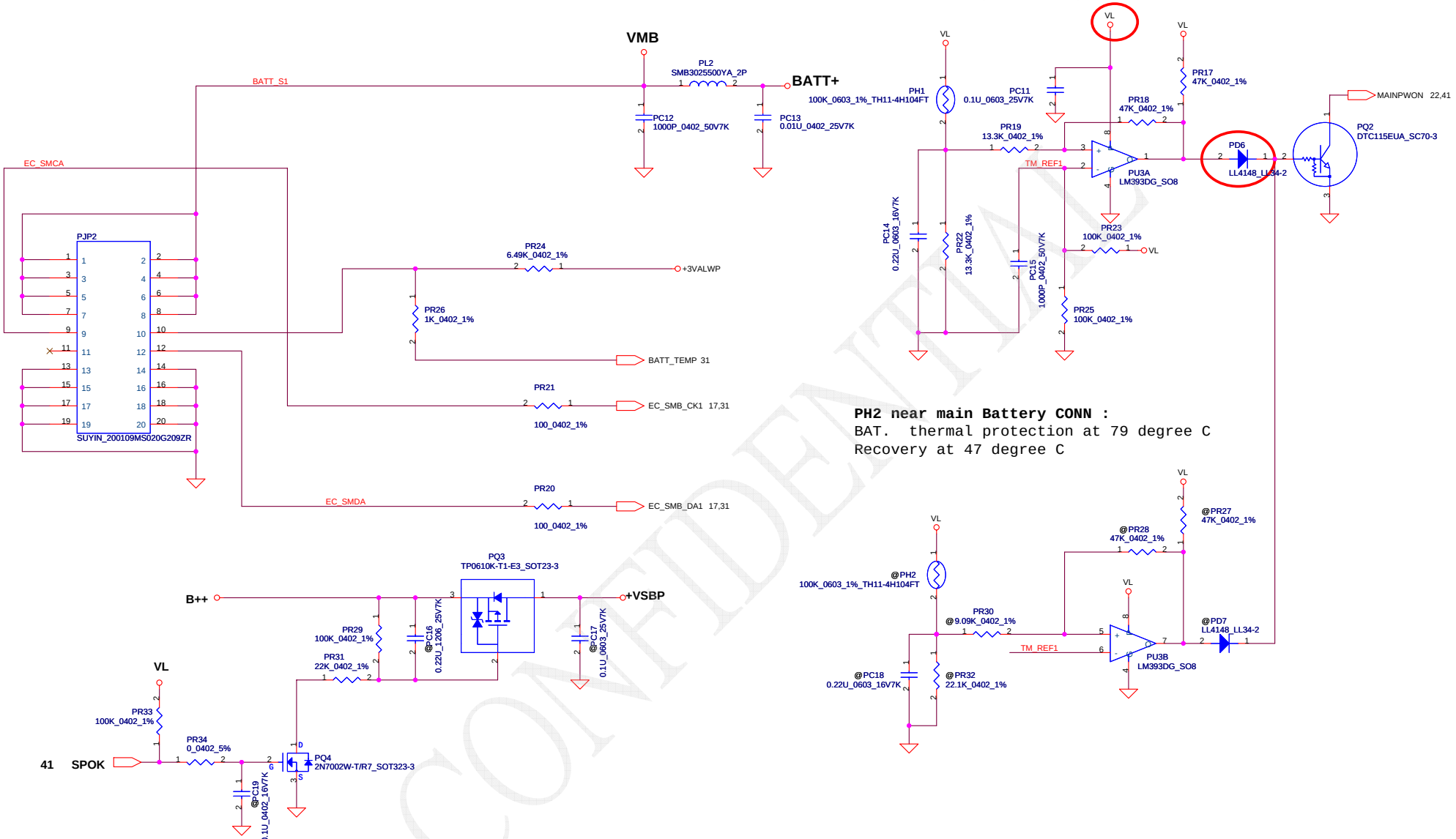
PH1 under CPU botten side :
CPU thermal protection at 96 degree C
Recovery at 60 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C

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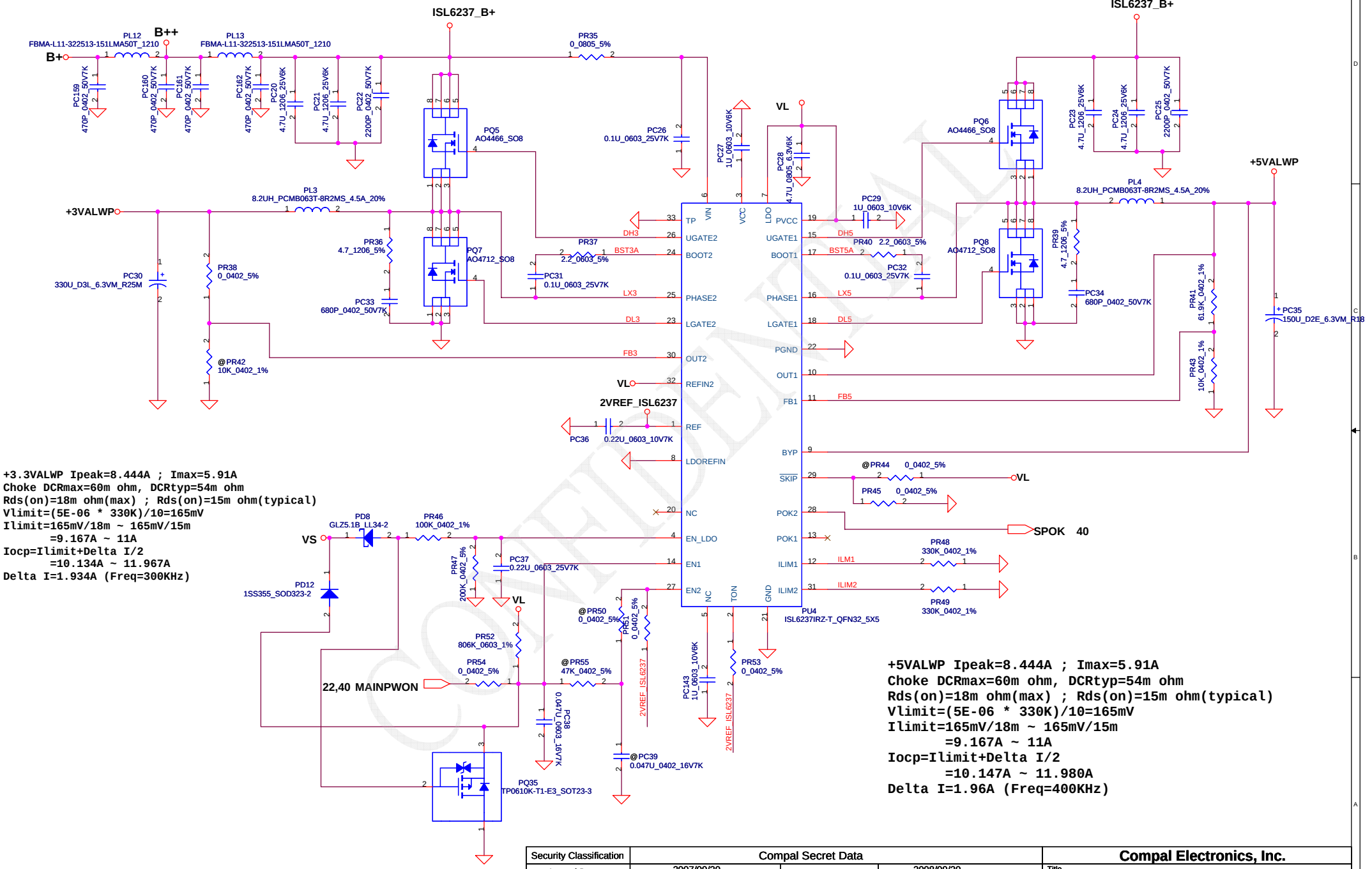

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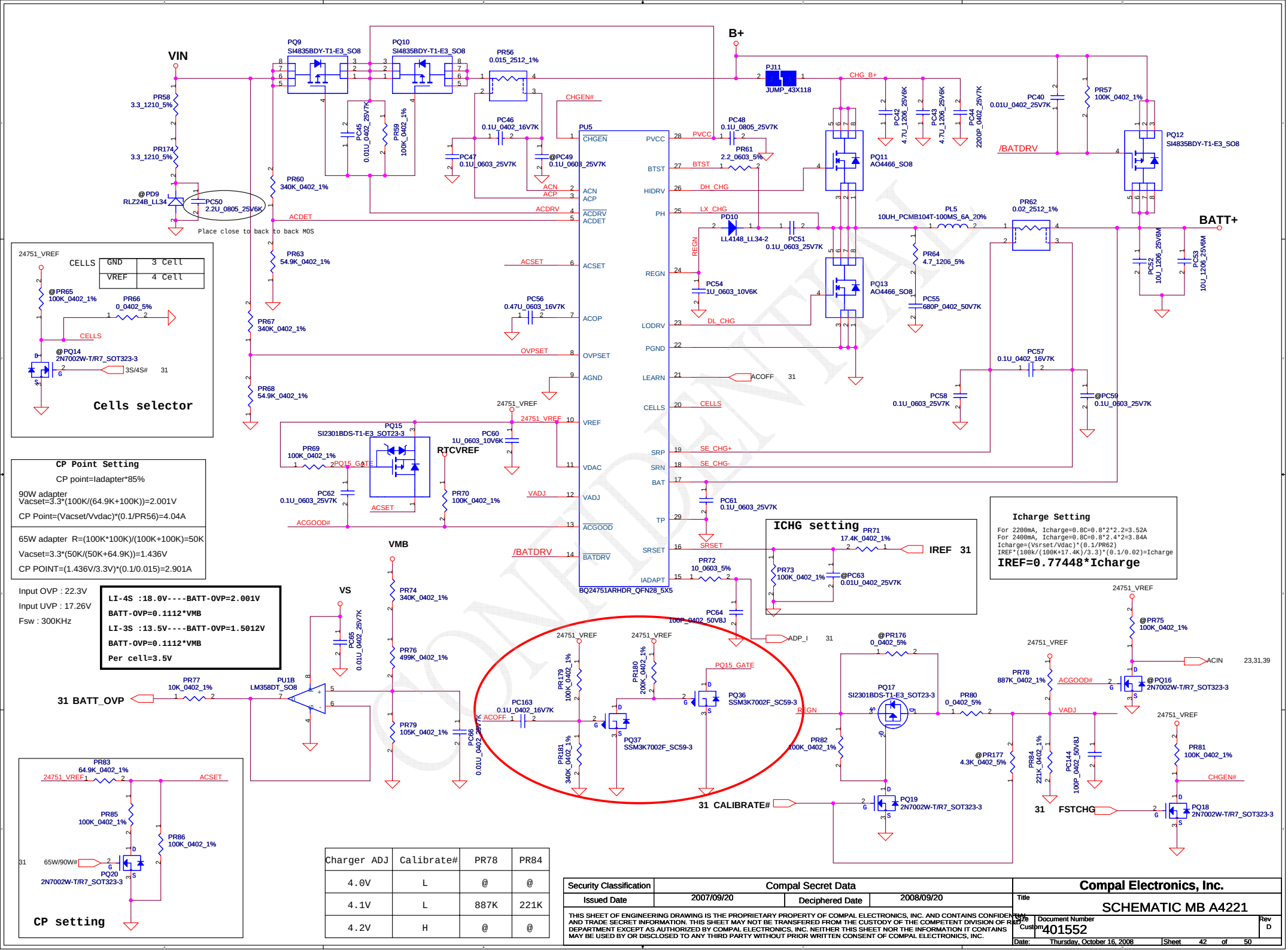

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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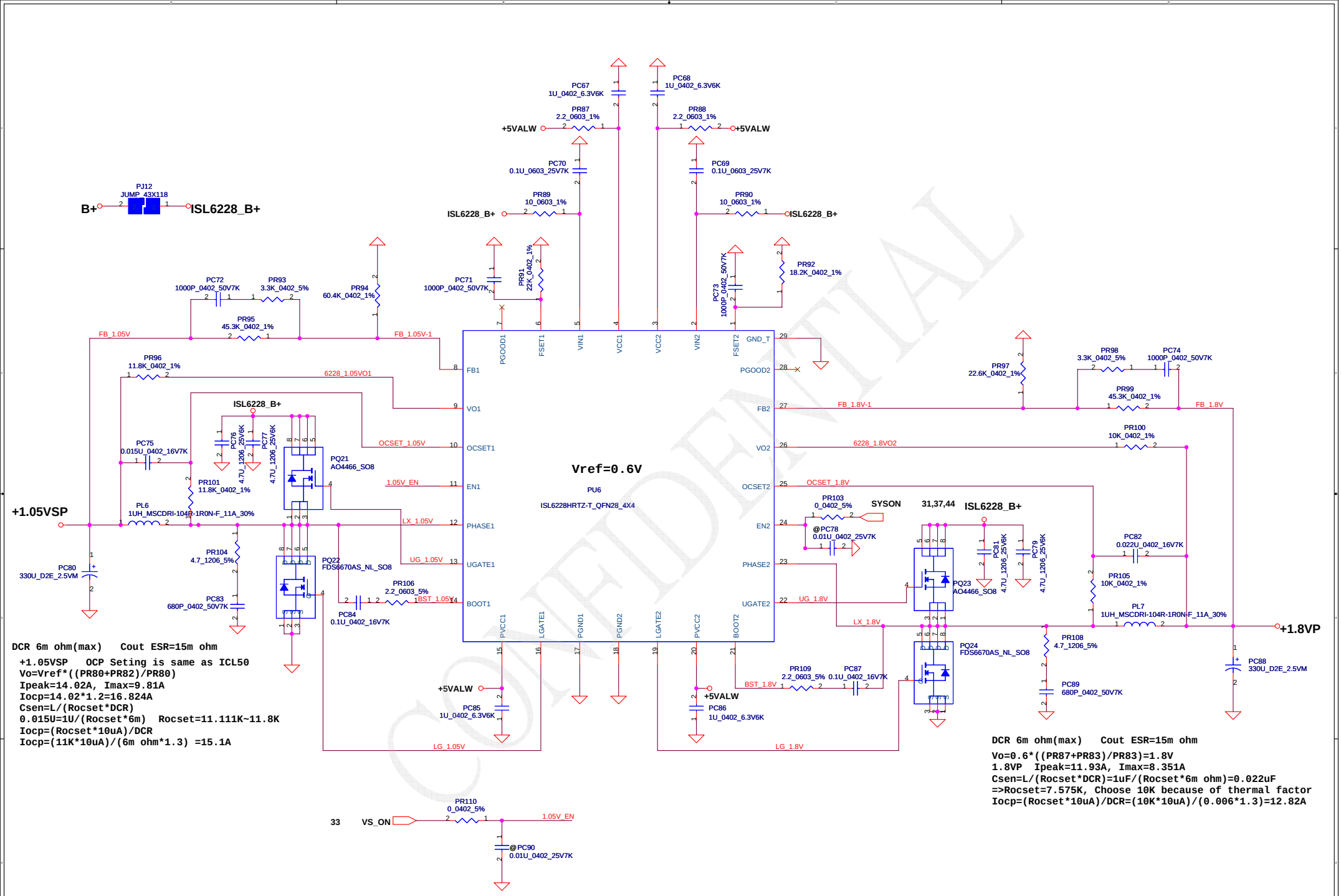

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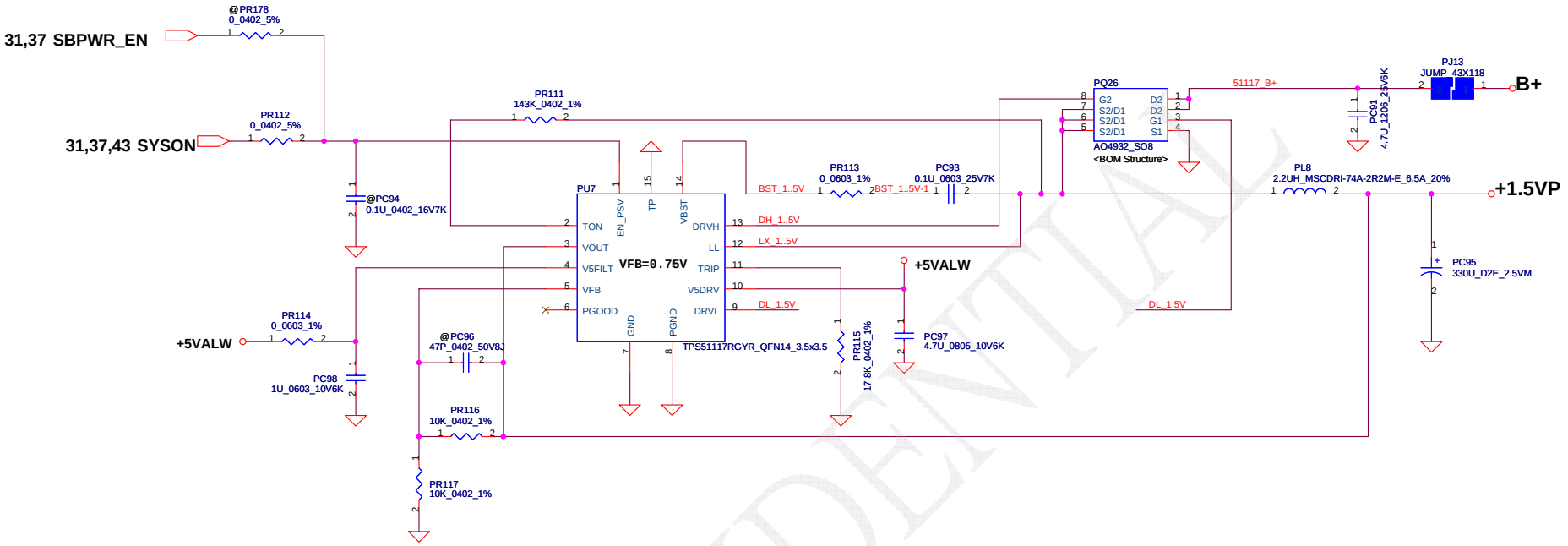

VFB=0.75V
Vo=VFB*(1+PR87/PR88)=0.75*(1+10K/10K)=1.5V
Ton=19*e-12*143000(((2/3)*Vo+100mV)/19)+50ns
=2.645e-7 us
=>Vo/Vin=D=Ton/Ts =>Ts=3.35us
Fsw=298KHz

Cout ESR=15m ohm
Ipeak=4.71A, Imax=3.297A, Iocp=5.652A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.107A
=>1/2DeltaI=1.053A
Vtrip=Rtrip*10uA=17.8K*10uA=0.178V
Iocpmin=Vtrip/Rdsonmax*1.2+1.053A
=0.178/(0.027*1.2)+1.053=5.493A+1.053A=6.546A
Iocpmax=(0.178/(0.021*1.1))+1.053A=7.705A+1.053A
=8.758A
Iocp=6.546A~8.758A

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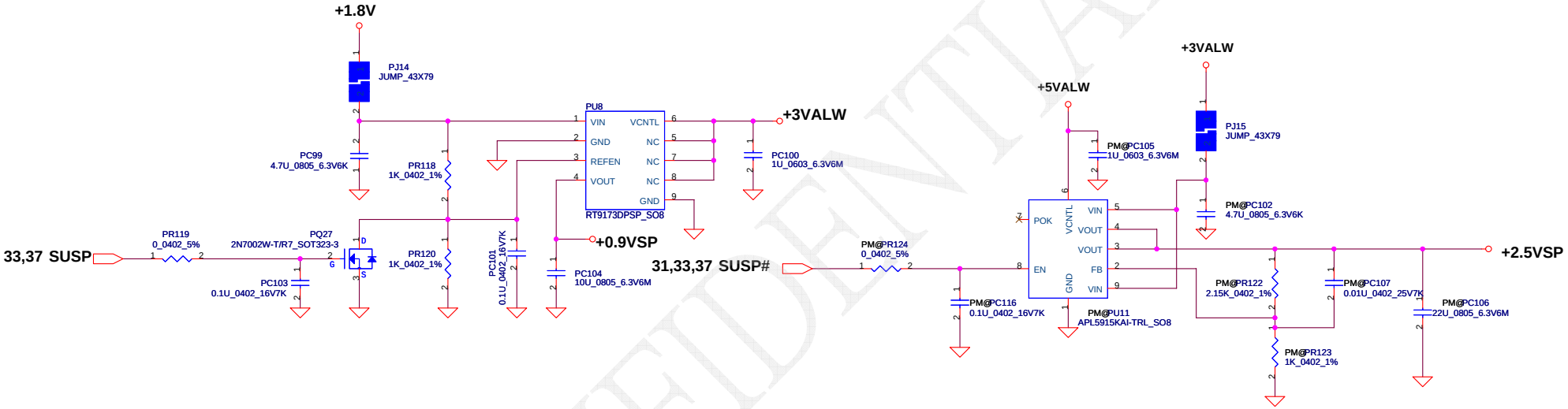

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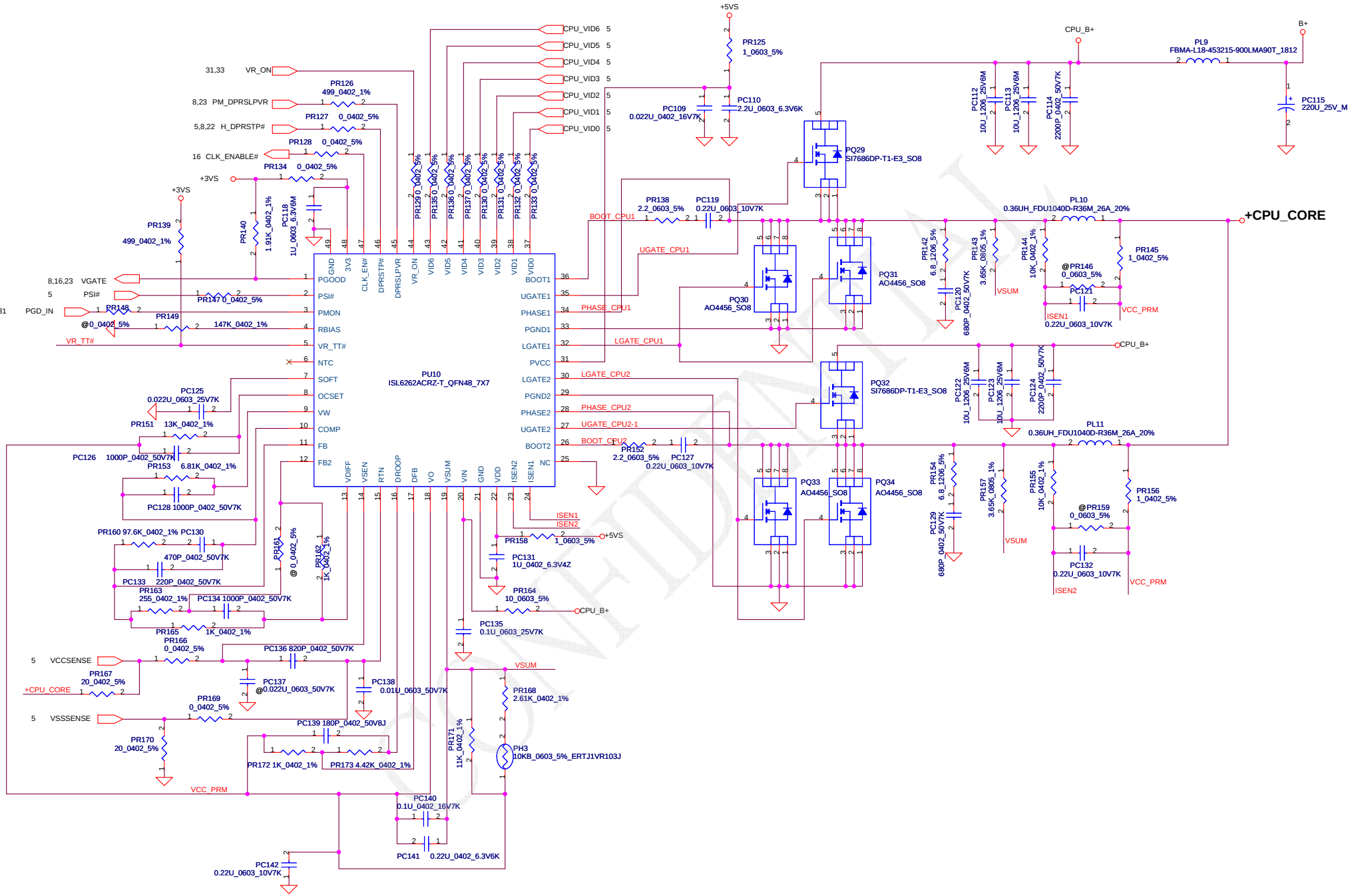

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Delete PD1.	Because we can cost down and DOCK_B+ has another one.	0.1	39	1 Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071108	EVT
2	3/5V exit on battery mode shutdown.	To prevent 3/5V exit on battery mode shutdown.	0.2	41	Add SC100001K00 (S DIO 1SS355 SOD323 T/R-5K	20071221	DVT
3	PD11 has over temp. issue.	Because PD11 has over temperature issue in JAQ60, we change it to a 10A diode.	0.2	39	Change PD11 from SCSB540C080 to SCS00002F00 .	20071221	DVT
4	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PR36 and PR39 to SD001470B80	20071221	DVT
5	Down size.	Down size. by sourcer request.	0.2	46	Change PC136 from SE025821K80 to SE000003W00	20071221	DVT
6	Down size.	Down size. by sourcer request.	0.2	46	Change PC120 and PC129 from SE024681J80 to SE074681K80	20071221	DVT
7	Down size.	Down size. by sourcer request.	0.2	43	Change PC72 and PC74 from SE068102J80 to SE074102K80	20071221	DVT
8	2nd source trial run TI controller.	2nd source trial run TI controller.	0.2	41	Add PC143 SE080105K80	20071221	DVT
9	Add snubber in 3/5V by EMI request.	Add snubber in 3/5V by EMI request.	0.2	41	Add PC33 and PC34 SE074681K80	20071221	DVT
10	To meet Jeta SPEC.	To meet Jeta SPEC.	0.2	42	Add PC144 SE074102K80	20071221	DVT
12	Add EMI solution.	Add 3/5V boost resistor.	0.3	41	Add PR37, PR40 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
13	Add EMI solution.	Add charger boost resistor.	0.3	42	Add PR61 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
14	Add EMI solution.	Add charger snubber.	0.3	42	Add PR64 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC55 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
15	Add EMI solution.	Add 1.05V/1.8V boost resistor.	0.3	43	Add PR106, PR109 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
16	Add EMI solution.	Add 1.05V snubber.	0.3	43	Add PR104 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC83 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
17	Add EMI solution.	Add 1.8V snubber.	0.3	43	Add PR108 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC89 SE074681K80(S CER CAP 680P 50V K X7R 0402)	20080102	DVT
18	Add EMI solution.	Add CPU boost resistor.	0.3	46	Add PR138, PR152 SD013220B80 (S RES 1/10W 2.2 +-5% 0603)	20080102	DVT
19	Add EMI solution.	Add 3/5V input capacitor filter..	0.3	41	Add PC159, PC160, PC161, PC162 SE074471K80(S CER CAP 470P 50V K X7R 0402)	20080102	DVT
20	Add EMI solution.	Add 3/5V input beat	0.3	41	Add PL12, PL13 SM010016410(S SUPPRE_ KC FBMA-L11-322513-151LMA50T)	20080102	DVT
21							
22							
23							

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NF?QC	N?EC	KMBGDGA?RGML JGQR	NSPNMQC
DVT	P.4	Change R25 , R18 , R11 , R19 from 56 to 54.9 ohm	Reference standard circuit
	P.4	Delete R10	Foe ESD
	P.4	Change CPU temp sensor U9 , R55 / R56 from 100 to0 ohm , delete R64 / R652	ADI had issue , for SMSC / Fintek temp sensor , no used for OD output
	P.8	Change R525 , R527 connected from +1.05Vs to GND	Reference standard circuit
		Change Cantiga GM U30 as SA00001P930 (Ver:B0) Change Cantiga PM U30 as SA00001ZO30 (Ver:B0)	Revision upgrade
	P.12	Change L42 , L18 , C499 , C229 , C280 , C232 as GM@ Change R596 , R597 as PM@	Reference standard circuit For UMA CRT
	P.12	Add C597 (220U)	Reserved
	P.12	Add C597 (220U)	Reference standard circuit
	P.12	Change R110 , C187 , C196 as stuff , R117 un-stuff	DFX
	P.12	C461 down size as 10U_0603	NA
	P.16	Change Q30 (dual N-MOS) as Q48 , Q49 (2 single N-MOS)	NA
	P.17	C500 down size as 680P_0402	For BOM
	P.17	Add L57 , L58 , C598 , C599 for +1V8RUN	+1V8RUN ripple (+1V8RUN is for MXM +PEX1V2)
	P.17	Add R599 as 0ohm	Reserve R598 , D31
	P.17	Update JMXM1 footprint	NA
	P.17	Change Q41 (dual N-MOS) as Q50 , Q51 (2 single N-MOS)	NA
	P.18	C364 down size as 680P_0402	For BOM
	P.18	C365 , C366 , C367 change from 220P to 820P	For EMI
	P.19	D5 change as RB411DT146_SOT23-3	Common part
	P.19	Change Q40 (dual N-MOS) as Q52 , Q53 (2 single N-MOS)	NA
	P.19	Change C401 , C409 , C419 as 15P	For DISCRETE CRT
	P.19	Change C402 , C410 , C420 as 12P	For DISCRETE CRT
	P.19	C408 , C418 , C423 (22P) stuff for UMA only	For UMA CRT only
	P.19	Change L1 , L2 from FCM1608C-121T_0603 as 10ohm_0603	For CRT
	P.20	Change Q7 from 2N7002_SOT23(Dual N-MOS) as Q7 & Q47(Single BSH111 N-MOS)	For DVI SMBUS level shifter
	P.20	Add R600 & R602 (4.7K ohm) pull high +3Vs	For DVI SMBUS
	P.20	Reserve R601 & R603 (2.7K ohm) pull high +5Vs	For DVI SMBUS
	P.20	Reserve U39 & U40 (SN74CBTD3306CPWR_TSSOP8)	For DVI & HDMI SMBUS
	P.20	Change D21 from RB751V_SOD323 as CH751H-40PT_SOD323-2	NA
	P.22	Change R478 from 33 ohm as 1K ohm	Customer request
	P.22	LAN_RST# connect to GND	No used Integrated LAN
	P.22	R169 un-stuff	For mobile
	P.22	Add CR_CPPE#(GPIO7) & CR_WAKE#(GPIO22)	For JMB385 power management
	P.22	Swap PCIE(x1) port 2 & port 4	NA
	P.22	R385 un-stuff , U28 stuff	For sequence
	P.25	U34.127 is used as externel IDSEL	NA
	P.25	R489 un-stuff	For PCMCIA Lan card not support PM_CLKRUN# function
	P.25	Update JPCM1 footprint	For DFX
	P.26	Reserve R655 , R656 , D33 for CR_CPPE# & CR_WAKE#	For JMB385 power management
	P.26	Cantiga JMB385 U32 as SA00001W910 (Ver:B)	Revision upgrade
	P.27	Delete BCM5787M co-lay schematic	NA
	P.27	Update U25 footprint	For DFX
	P.28	Change T1 from GSL5009 as GSL5009-1(SP050003T10)	NA
	P.28	Add C375 , C383 (68P)	For EMI
	P.29	Add R658	Add 80 port function on JMINI2
	P.30	D32(SC300000B00) stuff	For ESD
	P.31	Add R604	NA
	P.31	R248 change from 0 ohm as 8.2K ohm	Foe Board ID as 1 define

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NF?QC	N?EC	KMBGDGA?RGML JGQR	NSPNMQC
DVT	P.31	C286 change from 3.3U as 4.7U	Stable KB926 internal +1.8V regulator , ENE suggestion value
	P.32	JP6 pin define reverse	NA
	P.32	Change SW3 & SW4 type	NA
	P.32	U15 change from 1MB as 2MB capacity SPI ROM	Add Finger print code
	P.33	R261 change from 10K as 31.6K	Fix ATI MXM sku can't power on for battery mode issue
	P.33	C334 change from 0.1U as 1U	Fix nVIDIA MXM sku power on issue
	P.34	Delete Internal(Digital) MIC reserved circuit	NA
	P.34	Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI
	P.34	Add R660 to connect HDA_GPIO3 with DOCKIN#	For docking spdif feature enable
	P.34	Change R574 (0 ohm) as L59 (MBC1608121YZF)	For EMI
	P.35	R559 / R560 change from 47 ohm as 75 ohm	For Audio precision FSOV
	P.35	R561 / R562 / R566 / R571 change from 75 ohm as 1K ohm	For ESD , Realtek suggestion value
	P.36	Add C601 , C602 , C603 (330P) on +5VALW	For EMI
	P.37	R283 change from 100K to 10K	NA
	P.37	R206 , Q20 stuff	For +1.8V discharge
	P.38	Add switch to enable/disable EC_DOCKIN#_S0 for HDMI SMBUS	NA
	P.38	Update JDOCK1 footprint	NA
PVT1			
	P.16	Change C308 / C311 (33P) as 27P	For RTC accuracy
	P.23	Use 4MB SPI ROM	For Kinabalu_High & Kinabalu_Low
	P.23	Add test point T32 / T33 / T34 / T35	Reserved for PCIE(X1) port 1
	P.25	Change U35 as SA000026P10(OZ2210GN-B1)	For B1 version
	P.27	Change U23 as SA000025P20(BCM5764MKMLG P20)	For B0 version
	P.27	Reserved R673 , R674 (0 ohm)	For Lan SMBUS
	P.27	Reserved Lan GPIO0(LAN_ALERT#) / LAN_ALERT#_EC / R675 , R676 , R677 to EC	For Lan ASF workaround
	P.27	U23 Pin17 / Pin5 / Pin55 connect to U23 Pin18 for power +Lan_VDDIO_1.2	U23 Pin18 is power source +Lan_VDDIO_1.2 for U23 Pin17 / Pin5 / Pin55
	P.27	U23 Pin38 / Pin52 NC	NA
	P.29	Change JMINI1 for Robson2 , chnage JMINI2 for Wireless	NA
	P.31	Add LAN_ALERT#_EC & EC_ACIN for EC	Reserved for ASF workrund & Nvidia MXM power saving
	P.33	Add R668(10K) & reserved R263(10K)	Fine tune +1.05VS timing for UMA boot display flash
	P.34	Change U36 as ALC268-VB1-GR(SA00001GD10)	Version upgrade
	P.34	Stuff R659 & un-stuff R660	For SPDIF feature on docking
	P.36	Add C604 , C605 (820P_0402)	For EMI
	P.50	Chipset change as GM(SA00002JT10) / PM(SA00002JJ00) /ICH9M(SA00002JH00)	Version upgrade
PVT2	P.27	Update U23 CIS symbol	U23 Pin38 , 52 can't be changed as NC
	P.34	Add D34 , R678	For ACER docking SPDIF feature (No SPDIF on board)
	P.38	Update JDOCK1 CIS symbol	Docking connector modify (add boss x 2) for DFX
	P.35	Delete D2 , D4 (Int SPK ESD diode)	NA
	P.34	Delete D9 (Int MIC ESD diode)	NA
	P.35	Add C609 , C610 (330P_0603) on Right SPK	For EMI
	P.34	Add C608 (330P_0603) on Int MIC	For EMI
	P.08	Add Test point (T39 , T40 , T41 , T42)	Add Management Engine JTAG pins
	P.27	Add C612 , C614 (0.1u_0402) for +LAN_AVDD	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV
	P.27	Add C615 , C616 , C617 (0.1u_0402) for +LAN_AVDDL	For lower 1000Base-T Comm-Mode O/P Voltage < 50mV
	P.08	Add U41, R679 , R680 , R681 , R682 , R683 , R684 , R685 , T43	Reserved for Management Engine JTAG debug
	P.07	Chipset change as GM(SA00002JT50) / PM(SA00002JJ50)	Version upgrade
	P.20 , P.31	Add EC_DVI_DET , EC_GPIOB , EC_GPIOC , R687 , R688 , R691	Reserved for DVI detect delay control (by EC)
MP	P.24	R73 , R148 change from 10_0402 to 100_0402 C128 , C204 change from 0.1U_0402 to 1U_0402	For USB issue on ICH9M A3 stepping
	P.34 , P.35	C608 , C609 , C610 change from 330P_0603 to 330P_0402	For 330P_0402 is standard part
	P.31	Change R248 as 33K	Board ID upgrade
	P.30	Add R692 / R693 (0_0603)	Reserved S3 power rail for check finger print sensor S3 resume too slow

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NF?QC	N?EC	KMBGDGA?RGML JGQR	NSPNMQC
P.20		Add D35	Reserved for HDMI_HPD
P.30		Add R694 / R695 (0_0603)	Reserved for check
P.27		Delete C612 , C614 , C615 , C616 , C617 (0.1u_0402)	No need
P.16		Stuff R689 / R690	Reserved for LAN power saving
P.35		R559 , R560 change from 75 to 54.9 ohm	For FSOV between 420mv~480mv
		Chipset change as GM(SA00002JTB0) / PM(SA00002JJA0) /ICH9M(SA00002JH70)	Version upgrade
P.32		R291 , R294 change from 300_0402_5% to 240_0402_5%	For ACER Hank's request to fine tune brighter
P.20		R84 , R85 , R86 , R91 change from 2K_0402_5% to 4.7K_0402_5%	For UMA DVI/HDMI monitor P193WA (x) detect issue (On JAL90)
P.35		R304 , R305 change from 0 to 49.9 ohm	For FSOV between 420mv~480mv with docking
P.03	Date:06042008	Add BOM Structure : WITHITPM@ , WOITPM@	Update BOM as WOITPM(iTPM disable)
P.50		Chipset change as GL40(SA00002Q830)	NA
P.20		Add BOM Structure : HDMI@	NA
P.38		Add R223 & C306 for LOW sku (Remove BOM Structure : Main@)	Prevent DOCKIN# as floating & make wrong behavior
P.37		Change U11 , U12 , U13 , U20 , U21 as SI4800 (SB548000310)	Prevent MOSFET burn out issue
P.36		Change U2 as APL5605(SA00001Z900)	Due to original G993(SA009930010) is EOL

PCB

ZZZ

PCB 047 LA-4221P REV1 M/B

LA4221MB Rev0: DA600007R00
LA4221MB Rev1: DA600007R10
LA4221MB with Sub/B Rev1: DAZ04800100

IC

U30

PM@

CANTIGA ES_FCBGA1329

DVT CANTIGA PM: SA00001ZO30 (S IC EB88CTPM QR34 B0 FCBGA 1329 ES)
PVT CANTIGA PM: SA00002JJ00 (S IC AC88CTPM QT78 B2 FCBGA 1329 PM)
PVT2 CANTIGA PM: SA00002JJ50 (S IC AC88CTPM QU38 B3 FCBGA 1329 PM)
Pre-MP CANTIGA PM: SA00002JJA0 (S IC AC82PM45 SLB97 B3 FCBGA1329 PM ABO!)

U30

UMAGL@

CANTIGA ES_FCBGA1329

DVT(Check_TBD) CANTIGA GL: SA000023Z00 (S IC CANTIGA ES FCBGA 1329 MCH GL)
PVT CANTIGA GL: SA00002Q830 (S IC AC88CTGL QU37 B3 FCBGA 1329 GMCH GL)
MP CANTIGA GL: SA00002Q810 (S IC AC82GL40 SLB95 B3 GL CANTIGA ABO!)

For Discrete

CRT

C419 C409 C401

PM@ 1 2 15P_0402_50V8J

C420 C410 C402

PM@ 1 2 12P_0402_50V8J

15P_0402_50V8J: SE071150J80
12P_0402_50V8J: SE071120J80

DVT(Check)

MCH

R128 R129 R119 R138 R139 R140 R143

PM@ 2 1 0_0402_5%

0_0402_5%: SD028000080

DC Cable

ZZZ

DC Cable (65W)

@ PVT(54 Rank)

DC301003R00(CONN SET 048 DCJACK-MB 2DW-G756-I50 65W)

ZZZ

DC Cable (90W)

@ PVT(54 Rank)

DC301003S00(CONN SET 048 DCJACK-MB 2DW-G756-I49 90W)

U10

ICH9ME@

ICH9-M ES_FCBGA676

ICH9-M: SA00002G120
(S IC AF82801IEM QT10 A3 PBGA 676P ICH9M)

U6

WITHITPM@

W25X16-VSSIG_SO8

2MB Flash

MP Winbond: SA00001KN00
(S IC FL 16MBIT W25X16-VSSIG SOIC 8P)

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