

Compal Confidential

HCW50 Schematics Document

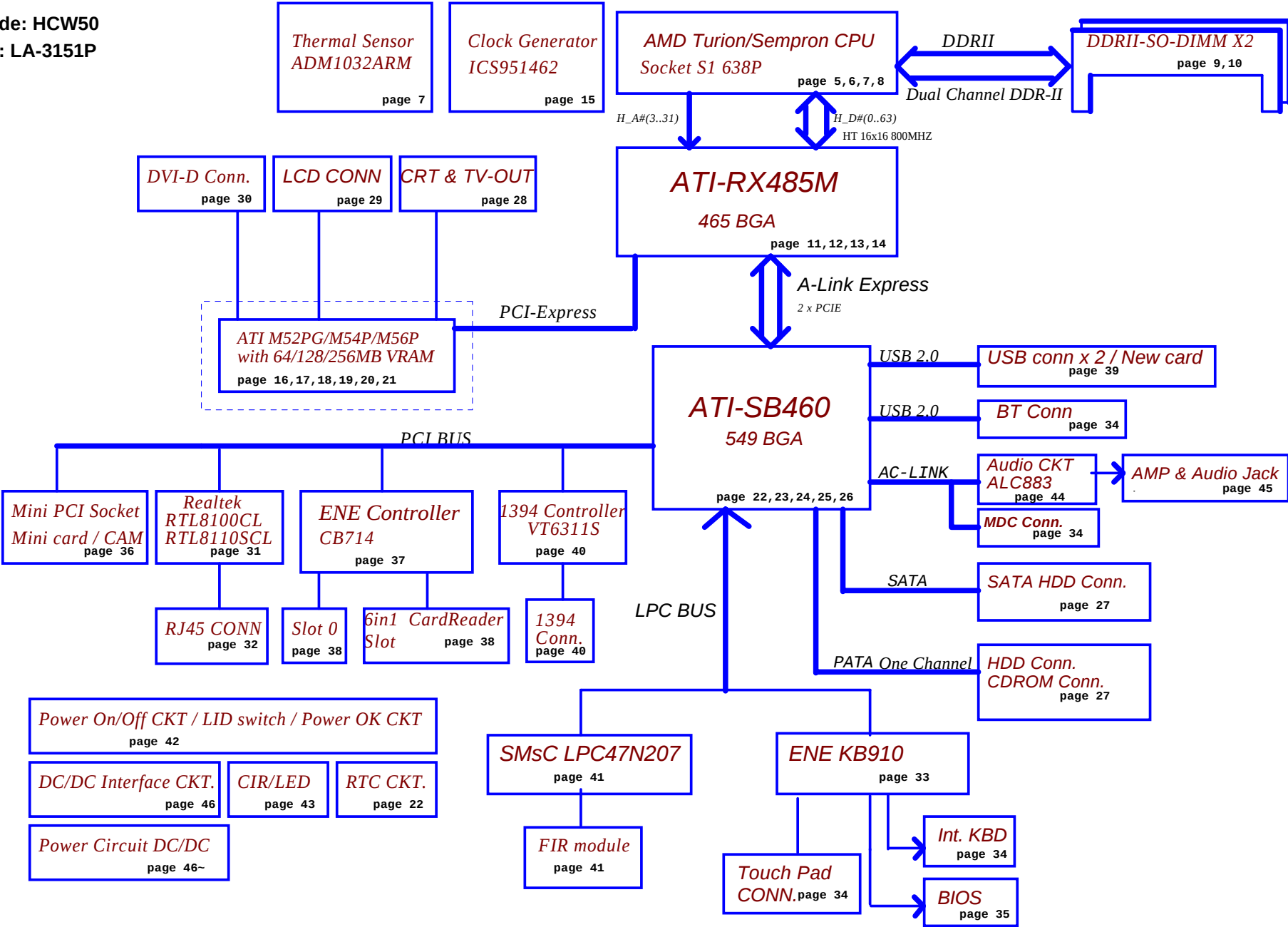
AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

2006 / 02 / 28 Rev:0.3 (For PVT)

Security Classification		Compal Secret Data		Compal Electronics, inc.		
Issued Date	2005/05/09	Deciphered Date	2006/03/08	Title SCHEMATIC, M/B LA-3151P		
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Project Code: HCW50
File Name : LA-3151P



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0~1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PC(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

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Date:

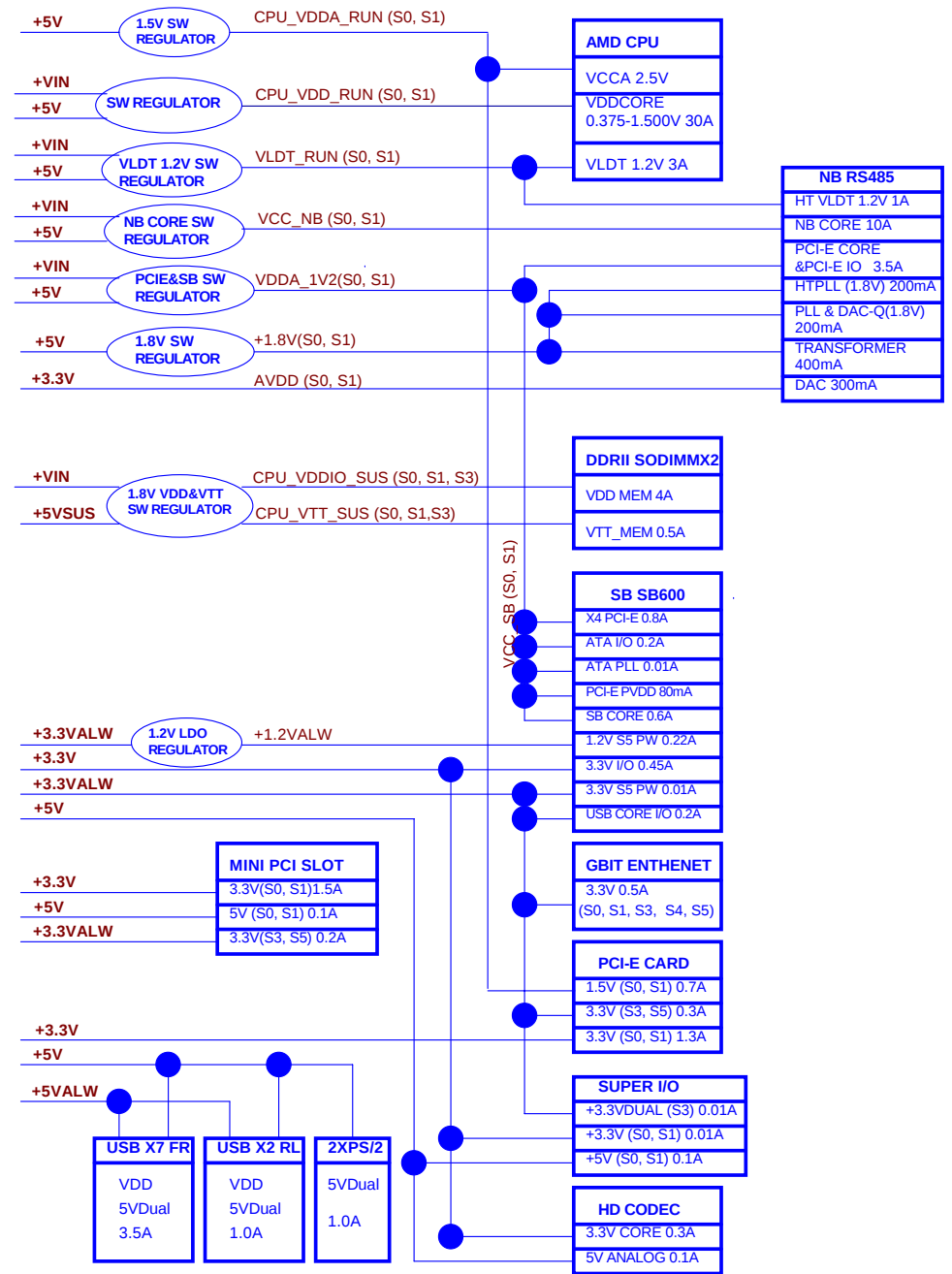
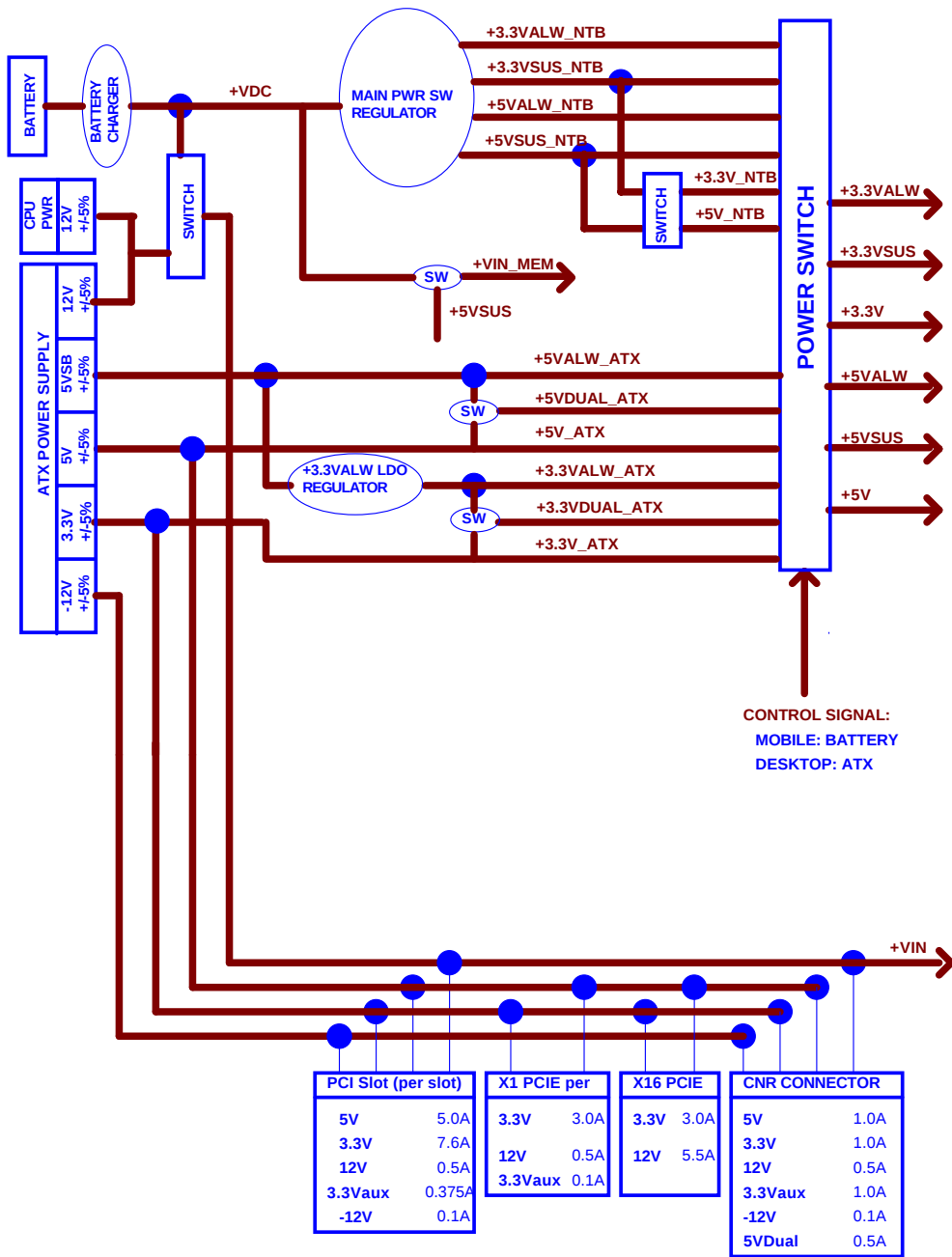
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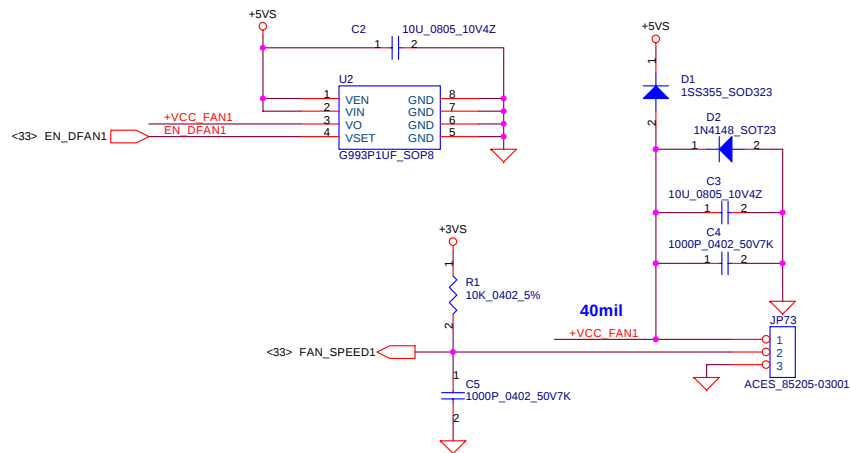
<11> H_CADIP[0..15] H_CADIN[0..15] H_CADOP[0..15] H_CADON[0..15] <11>

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



FAN1 Conn

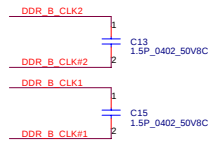
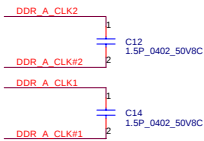
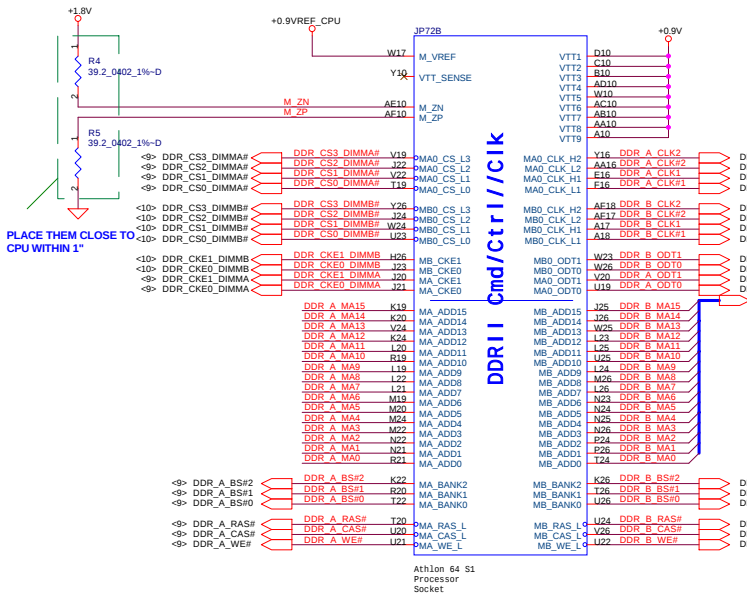


LAYOUT: Place bypass cap on topside of board

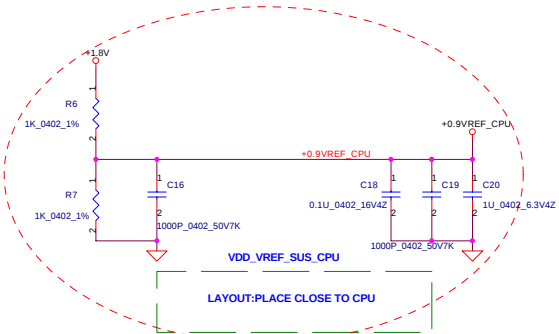
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

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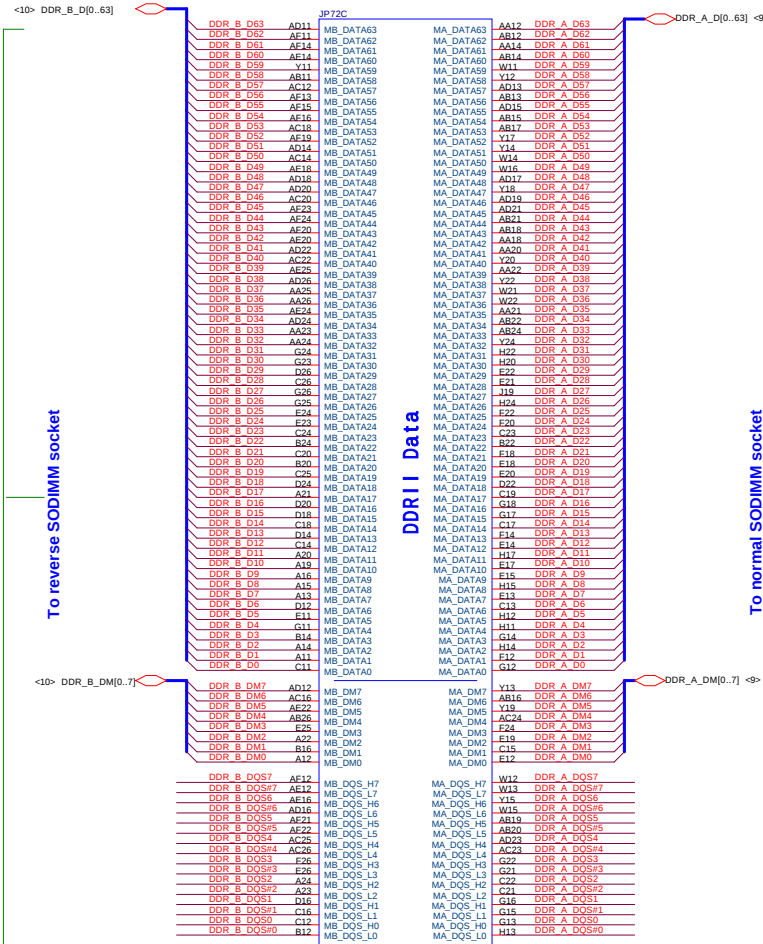
VDD, VTT, SUS, CPU IS CONNECTED TO THE VDD, VTT, SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



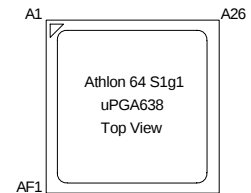
ATI check , Use +0.9V PWR , can delete or not



Processor DDR2 Memory Interface



<9> DDR_A_DQS[0..7] <9> DDR_A_DQS[0..7]
<9> DDR_A_DQS[0..7] <9> DDR_A_DQS[0..7]



ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

SB460 ONLY

place them to CPU within 1"

MISC

Modify 11/22

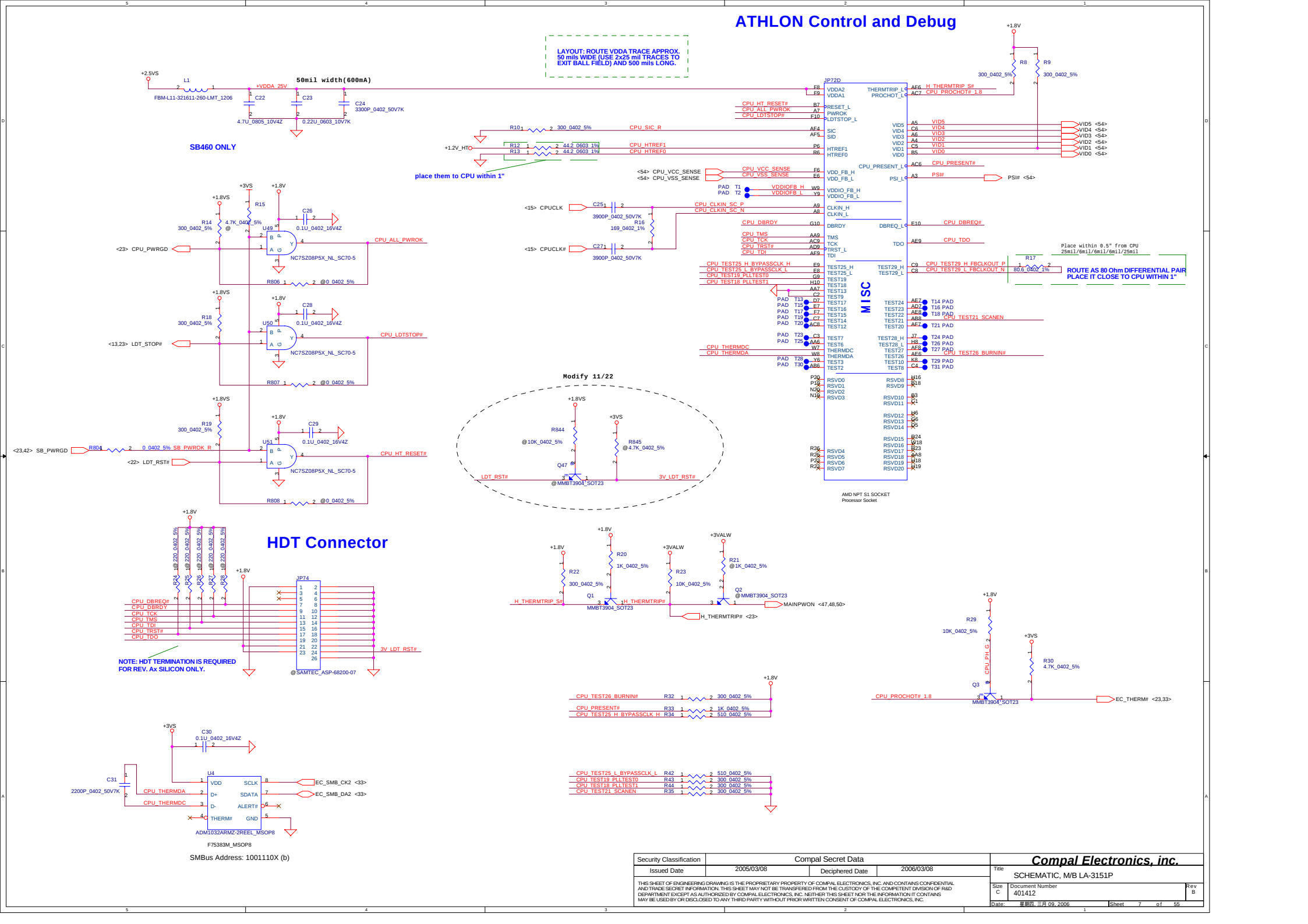
AMD NPT S1 SOCKET
Processor Socket

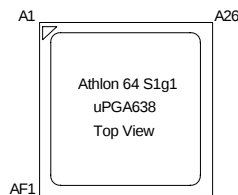
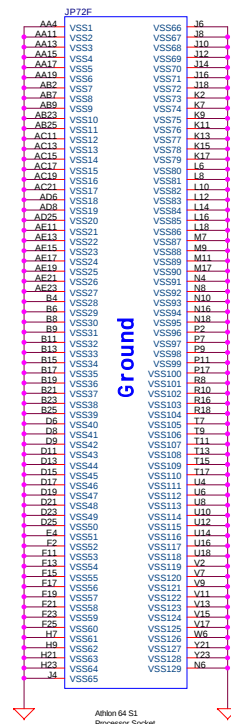
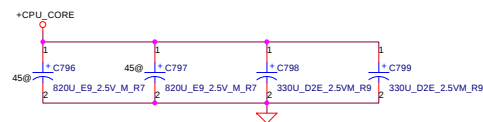
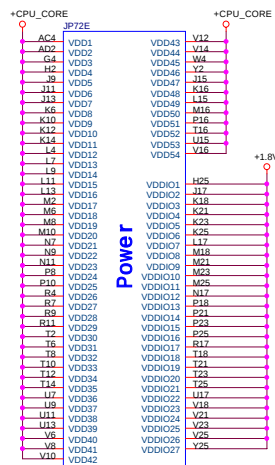
HDT Connector

NOTE: HDT TERMINATION IS REQUIRED
FOR REV. Ax SILICON ONLY.

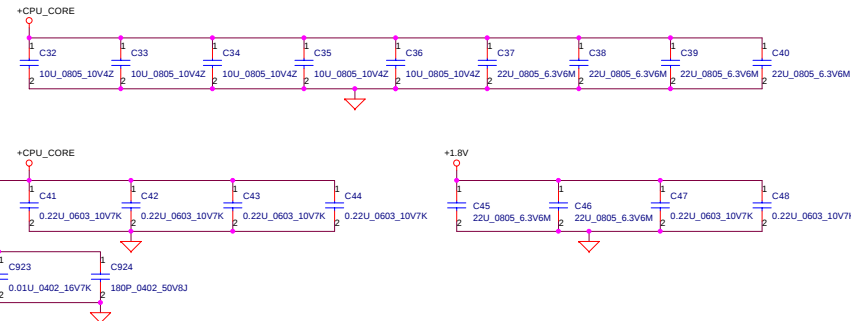
SMBus Address: 1001110X (b)

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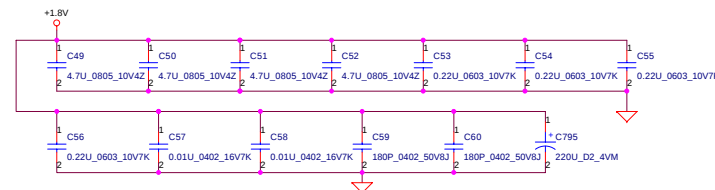




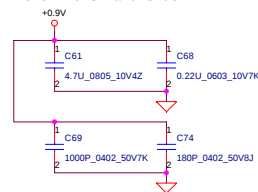
BOTTOMSIDE DECOUPLING



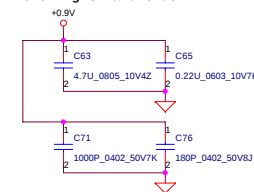
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



CPU left-hand side

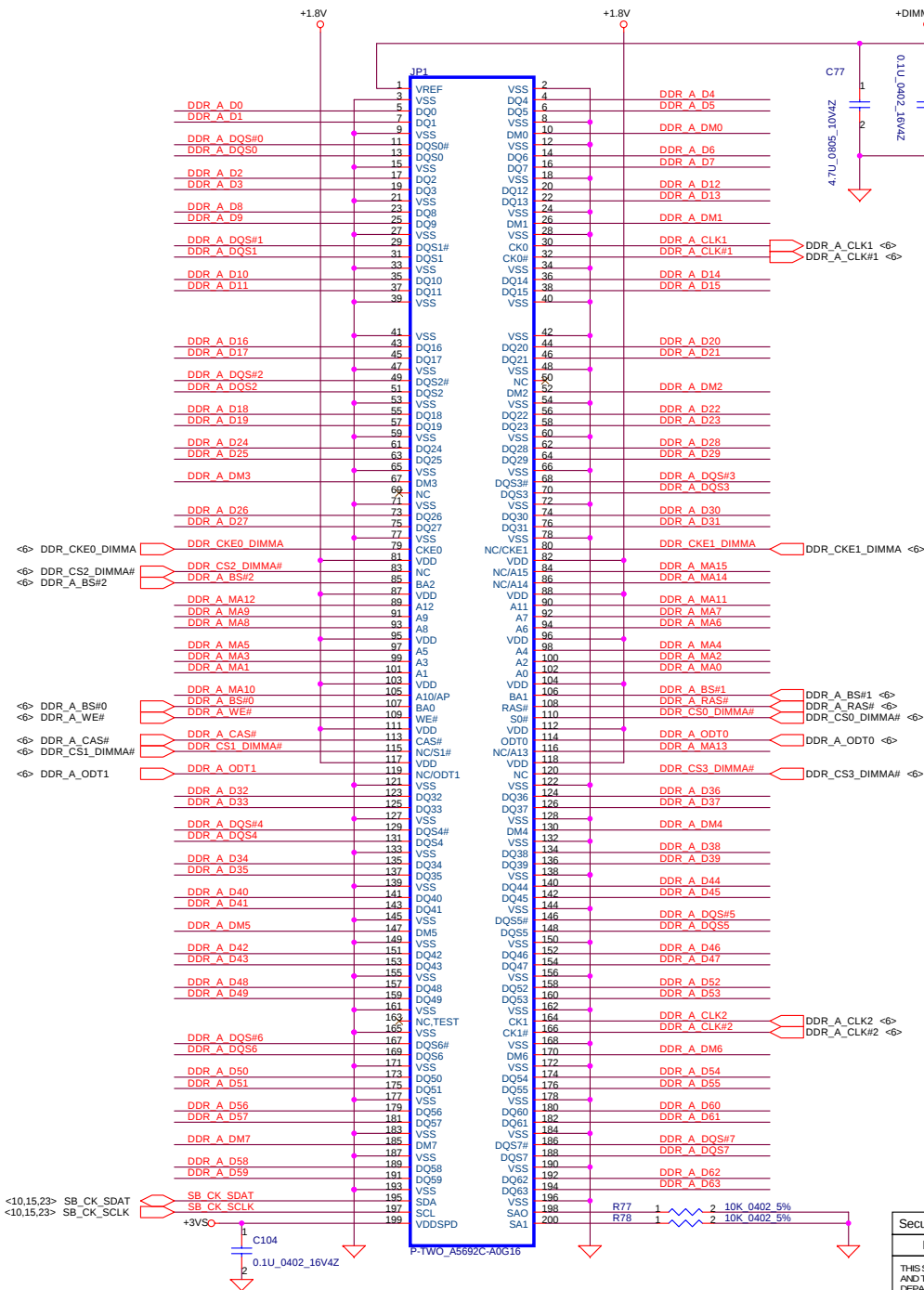


CPU right-hand side

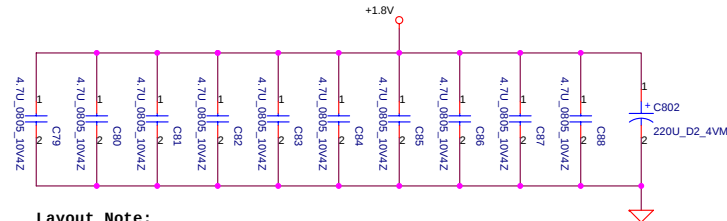


PROCESSOR POWER AND GROUND

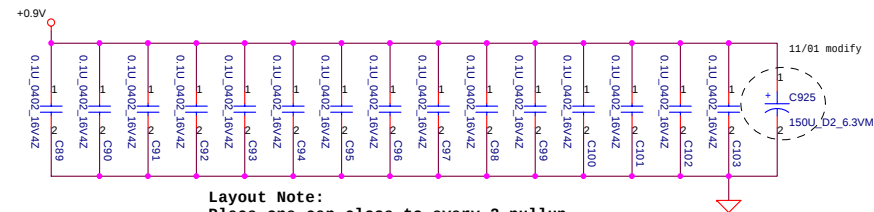
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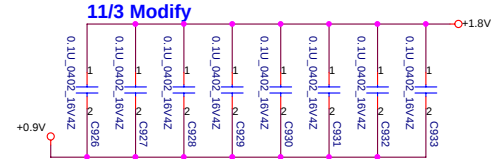
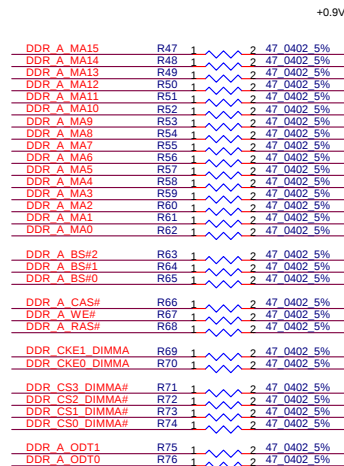
<6> DDR_A_D[0..63] DDR A D[0..63]
<6> DDR_A_DM[0..7] DDR A DM[0..7]
<6> DDR_A_DQS[0..7] DDR A DQS[0..7]
<6> DDR_A_MA[0..15] DDR A MA[0..15]
<6> DDR_A_DQS#[0..7] DDR A DQS#[0..7]



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

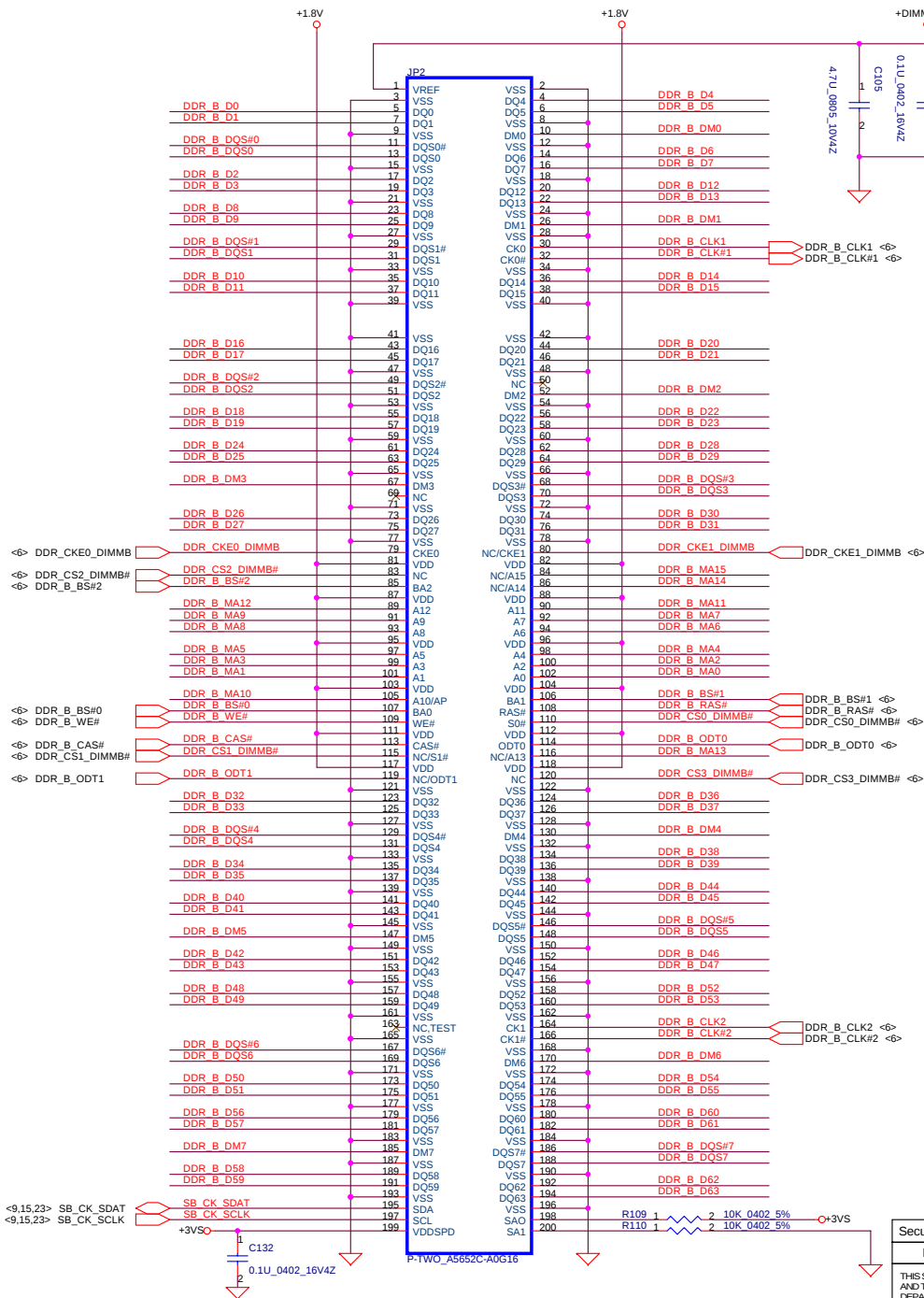


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

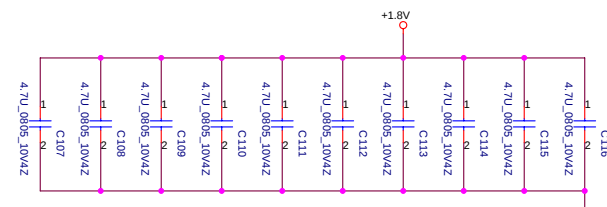


Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

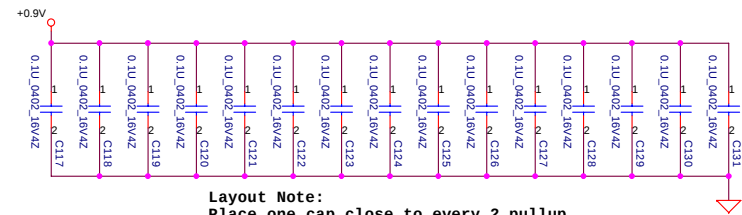
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- <6> DDR_B_D[0..63] DDR_B_D[0..63]
- <6> DDR_B_DM[0..7] DDR_B_DM[0..7]
- <6> DDR_B_DQS[0..7] DDR_B_DQS[0..7]
- <6> DDR_B_MA[0..15] DDR_B_MA[0..15]
- <6> DDR_B_DQS#[0..7] DDR_B_DQS#[0..7]

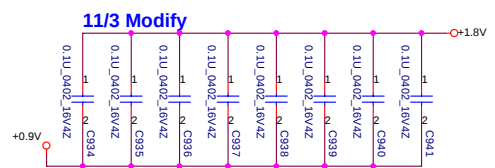


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

DDR_B_MA15	R79	1	2	47	0402	5%
DDR_B_MA14	R80	1	2	47	0402	5%
DDR_B_MA13	R81	1	2	47	0402	5%
DDR_B_MA12	R82	1	2	47	0402	5%
DDR_B_MA11	R83	1	2	47	0402	5%
DDR_B_MA10	R84	1	2	47	0402	5%
DDR_B_MA9	R85	1	2	47	0402	5%
DDR_B_MA8	R86	1	2	47	0402	5%
DDR_B_MA7	R87	1	2	47	0402	5%
DDR_B_MA6	R88	1	2	47	0402	5%
DDR_B_MA5	R89	1	2	47	0402	5%
DDR_B_MA4	R90	1	2	47	0402	5%
DDR_B_MA3	R91	1	2	47	0402	5%
DDR_B_MA2	R92	1	2	47	0402	5%
DDR_B_MA1	R93	1	2	47	0402	5%
DDR_B_MA0	R94	1	2	47	0402	5%
DDR_B_BS#2	R95	1	2	47	0402	5%
DDR_B_BS#1	R96	1	2	47	0402	5%
DDR_B_BS#0	R97	1	2	47	0402	5%
DDR_B_CAS#	R98	1	2	47	0402	5%
DDR_B_WE#	R99	1	2	47	0402	5%
DDR_B_RAS#	R100	1	2	47	0402	5%
DDR_CKE1_DIMMB	R101	1	2	47	0402	5%
DDR_CKE0_DIMMB	R102	1	2	47	0402	5%
DDR_CS3_DIMMB#	R103	1	2	47	0402	5%
DDR_CS2_DIMMB#	R104	1	2	47	0402	5%
DDR_CS1_DIMMB#	R105	1	2	47	0402	5%
DDR_CS0_DIMMB#	R106	1	2	47	0402	5%
DDR_B_ODT1	R107	1	2	47	0402	5%
DDR_B_ODT0	R108	1	2	47	0402	5%



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Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

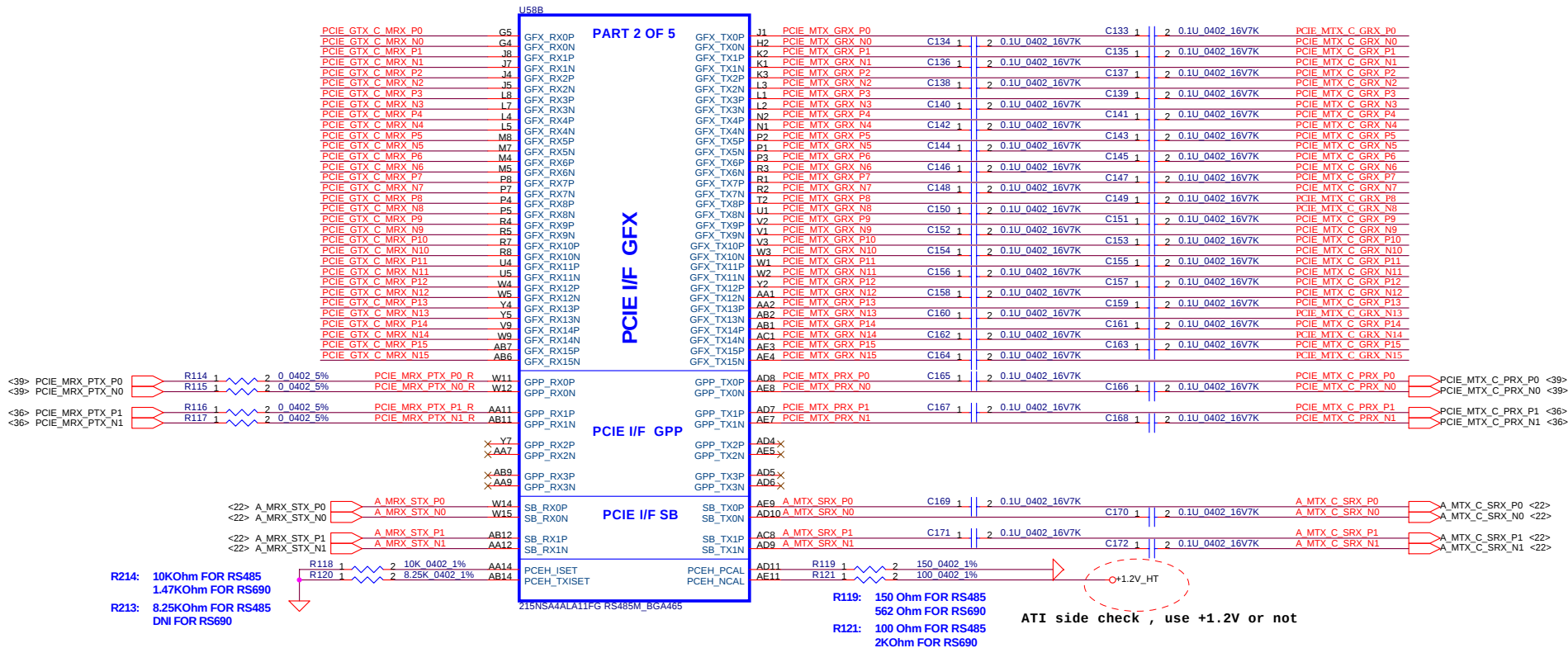
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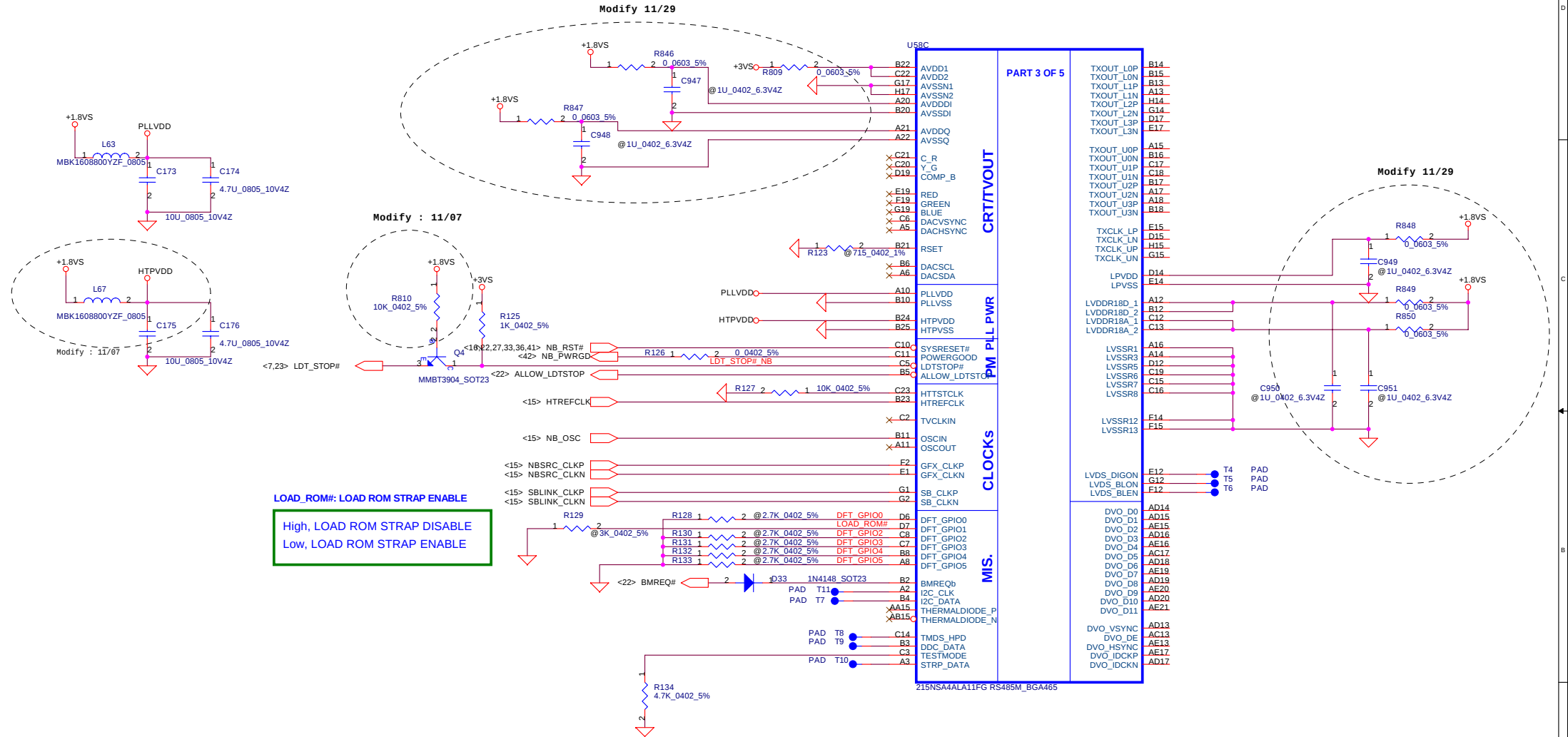
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<16> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
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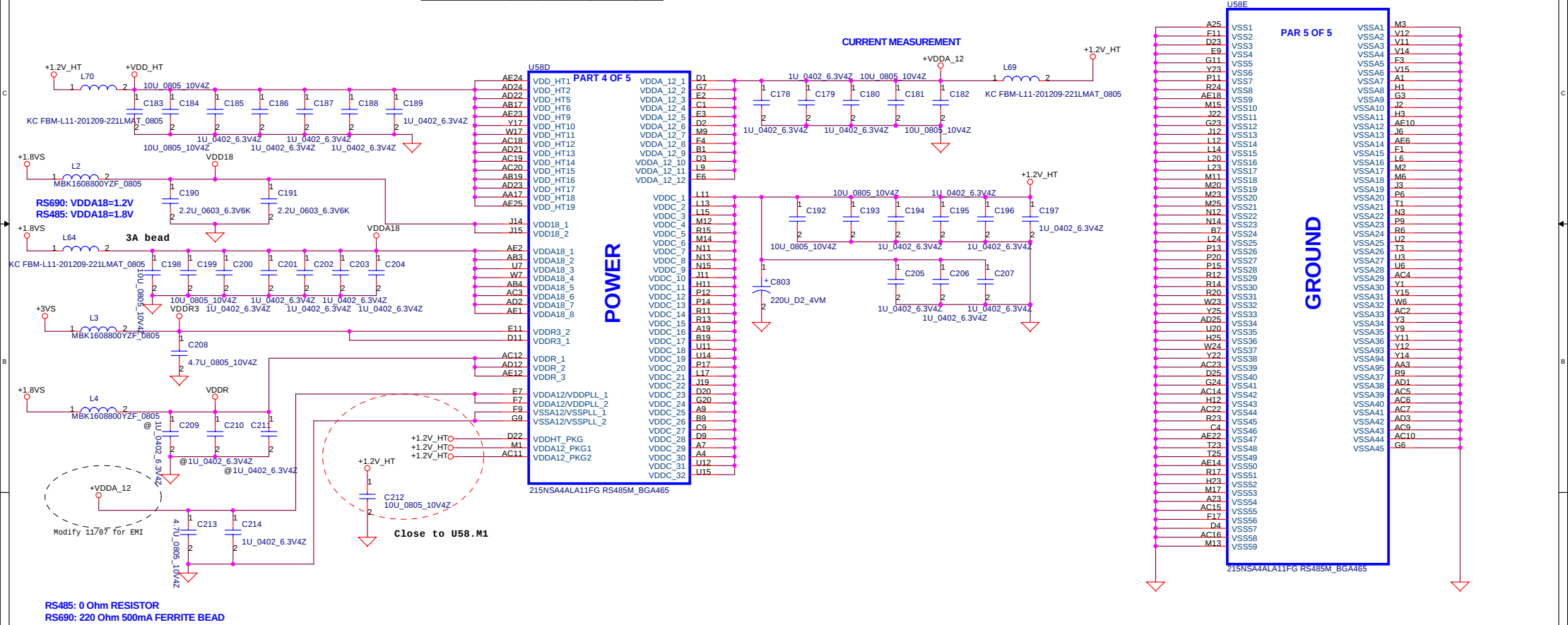
ATI check , CRT / TV/ LVDS can delete or not when I use RX485



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NB RS485 POWER STATES

Power	Signal	S0	S1	S3	S4/S5	G3
VDDHT		ON	ON	OFF	OFF	OFF
VDDR		ON	ON	OFF	OFF	OFF
VDD18		ON	ON	OFF	OFF	OFF
VDDC		ON	ON	OFF	OFF	OFF
VDDA18		ON	ON	OFF	OFF	OFF
VDDA12		ON	ON	OFF	OFF	OFF
AVDD		ON	ON	OFF	OFF	OFF
AVDDDI		ON	ON	OFF	OFF	OFF
PLLVD		ON	ON	OFF	OFF	OFF
HTPVDD		ON	ON	OFF	OFF	OFF
VDDR3		ON	ON	OFF	OFF	OFF
LPVDD		ON	ON	OFF	OFF	OFF
LVDDR18D		ON	ON	OFF	OFF	OFF
LVDDR18A		ON	ON	OFF	OFF	OFF





- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Parallel Resonance Crystal

$I_{oh} = 5 \cdot I_{ref}$
(2.32mA)
 $V_{oh} = 0.71V @ 60 ohm$

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HIT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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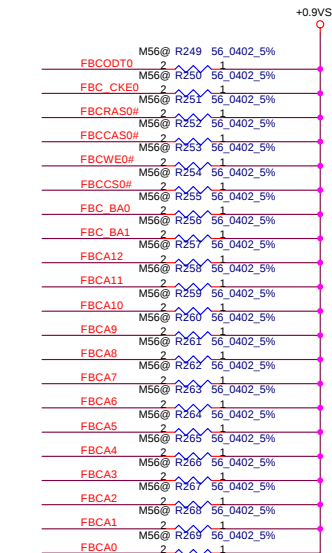


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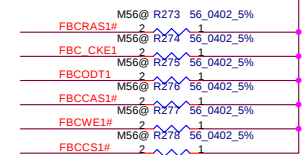
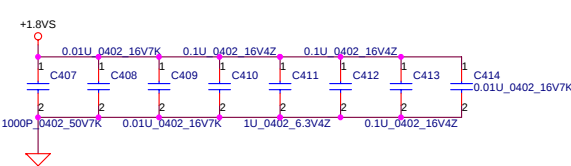
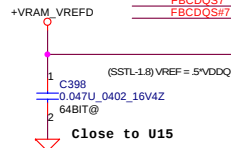
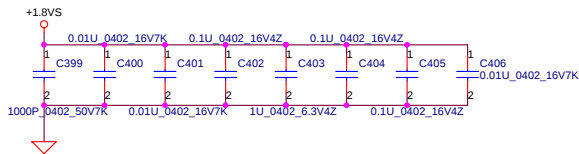
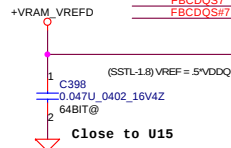
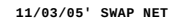
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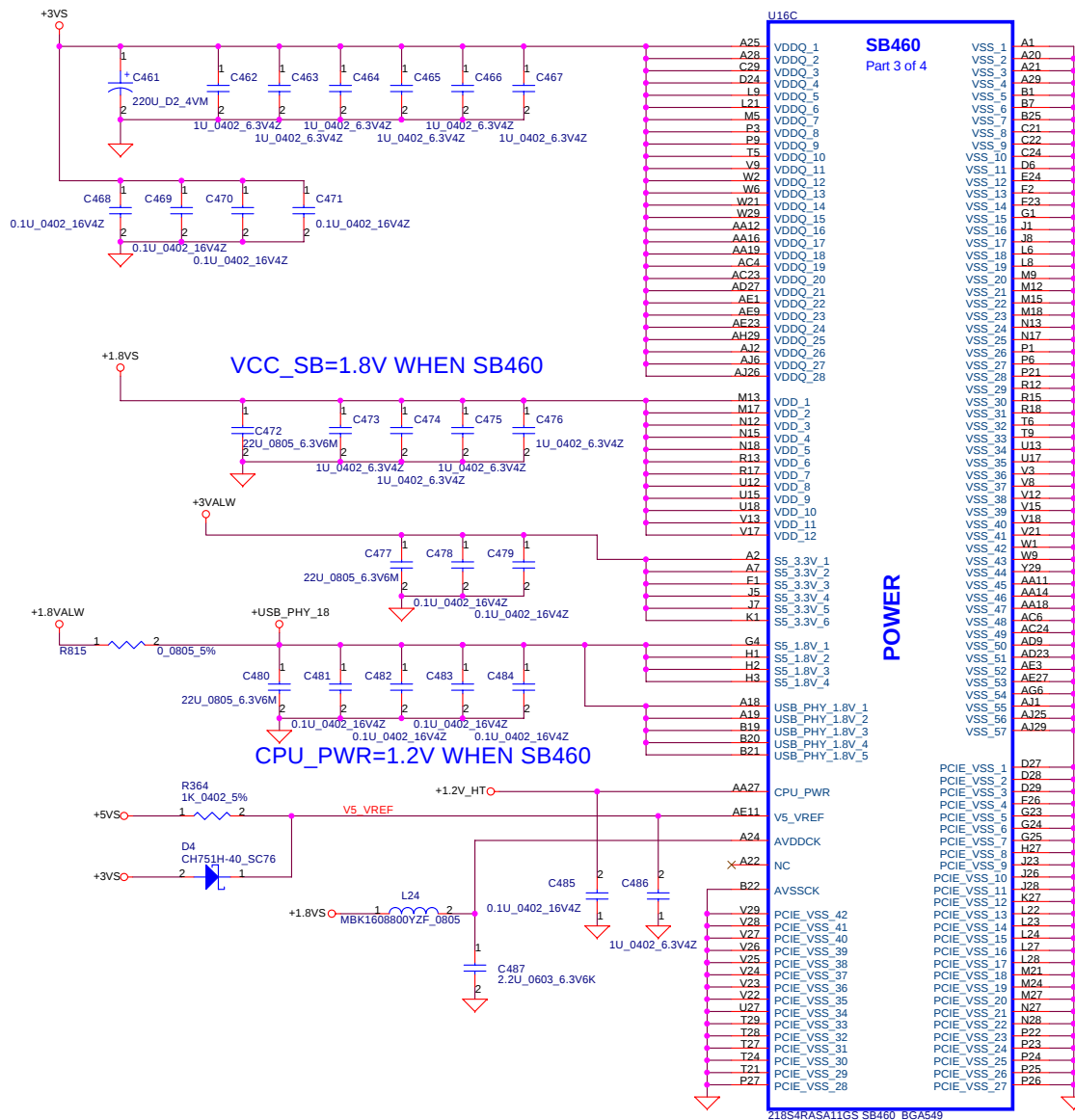
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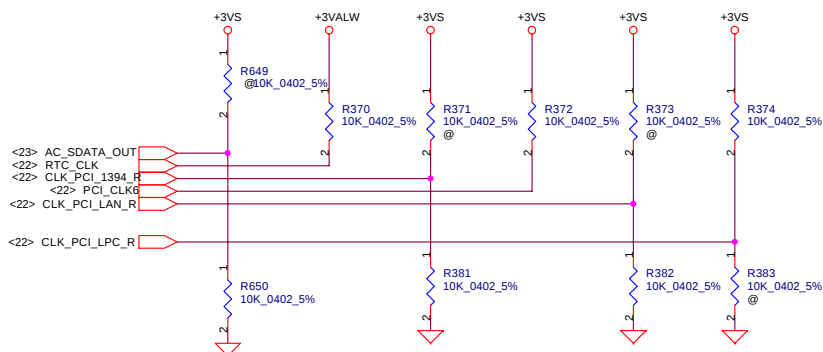
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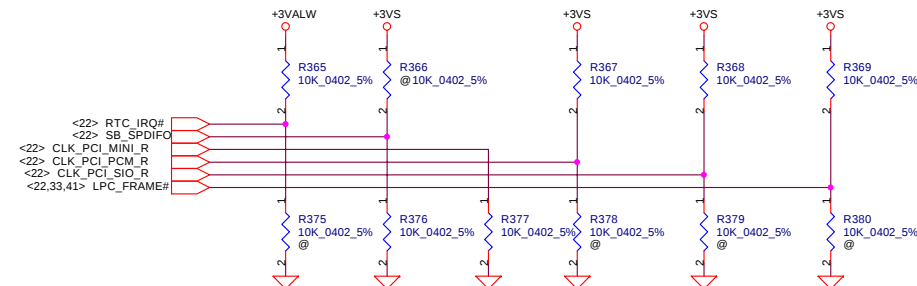
REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



NOTE: R365 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB460
TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY



	SB600				SB460			
	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCI_CLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]			

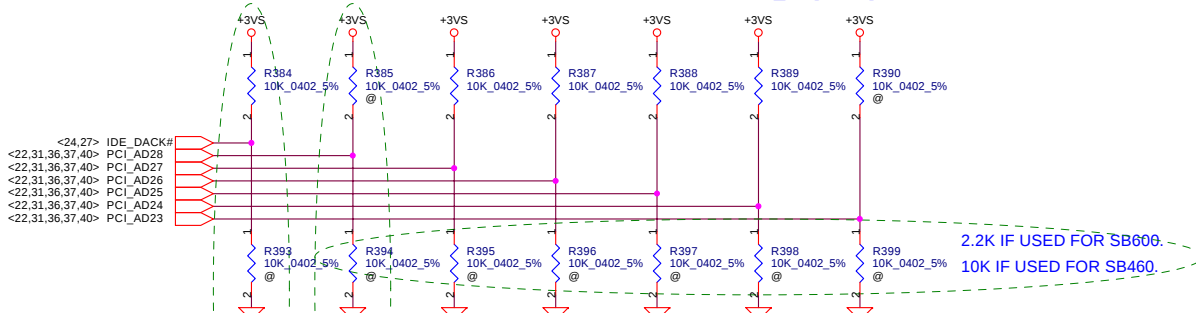
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
	RTC_IRQ#	SB_SPDIFO	CLK_PCI_MINI	CLK_PCI_PCM	CLK_PCI_SIO	LPC_FRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHZ	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHZ DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

NOTE: FOR
SB460,
PCI_AD23 IS
RESERVED

SB460 ONLY

SB600 ONLY

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<24> IDE_D[0..15] IDE_D[0..15]
<24> IDE_A[0..2] IDE_A[0..2]

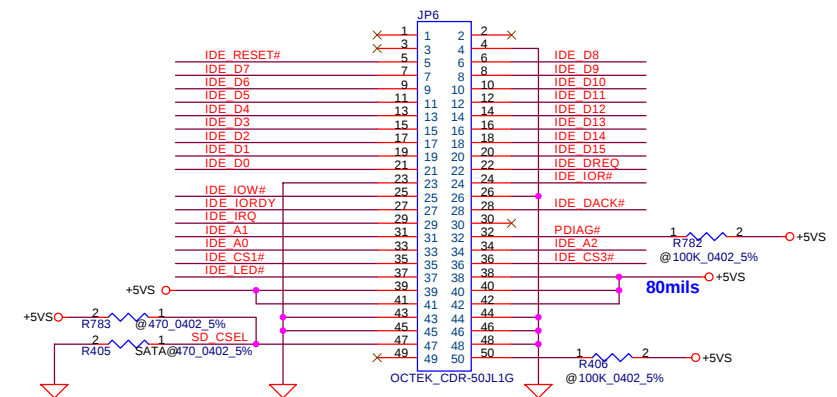
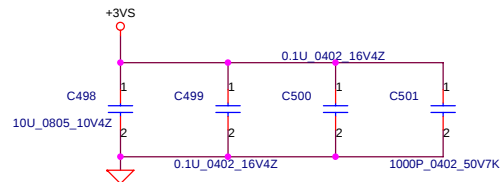
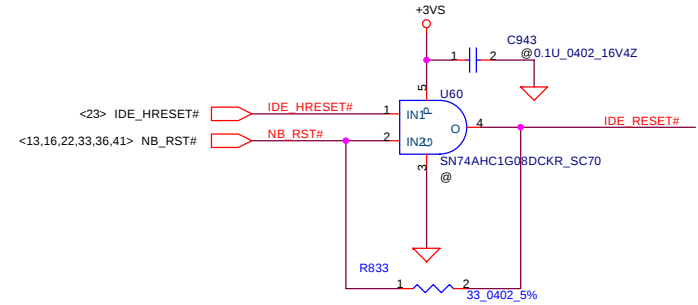


Diagram illustrating the SATA signal connections for the OCEK SAT-22S61G-1R board, showing the connection of SATA STX_C and SATA DTX_C controllers to the SATA STX_C and SATA DTX_C headers.

The diagram shows two SATA controllers, SATA STX_C and SATA DTX_C, each with four signal lines (P0, N0, SRX_N0, SRX_P0). These are connected to a 3V3 and 5V5 power plane. A dashed oval encloses the power plane and the SATA controllers, with a note "Modify 11/07 for EMI".

The power plane is connected to the board's power pins (J7) and the SATA controllers. The SATA controllers are connected to the SATA STX_C and SATA DTX_C headers.

Legend for J7 pins:

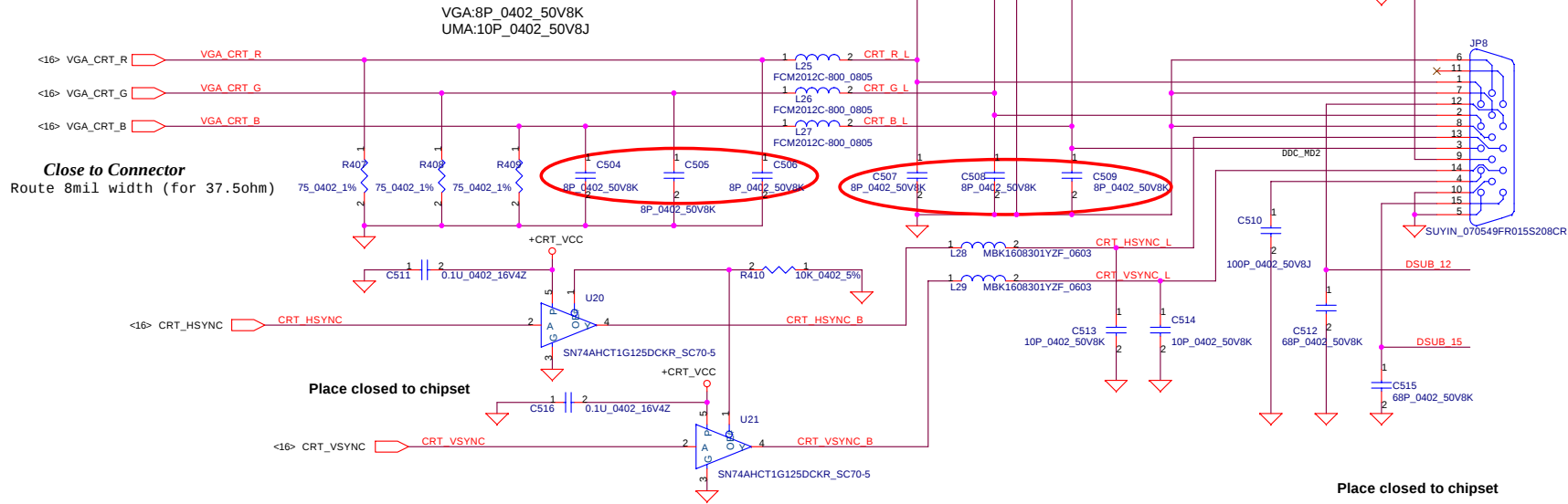
- 1: GND
- 2: HTX+
- 3: HTX-
- 4: GND
- 5: HRX-
- 6: HRX+
- 7: GND
- 8: VCC3.3
- 9: VCC3.3
- 10: VCC3.3
- 11: GND
- 12: GND
- 13: GND
- 14: VCC5
- 15: VCC5
- 16: VCC5
- 17: GND
- 18: RESERVED
- 19: GND
- 20: GND
- 21: VCC12
- 22: VCC12

SATA@ OCEK SAT-22S61G-1R (NEW)

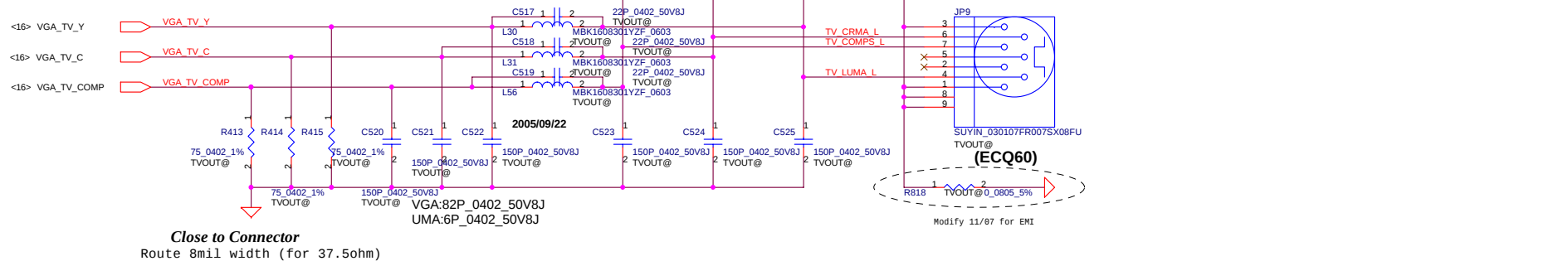
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CRT Connector

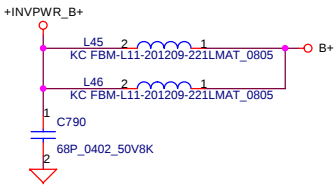
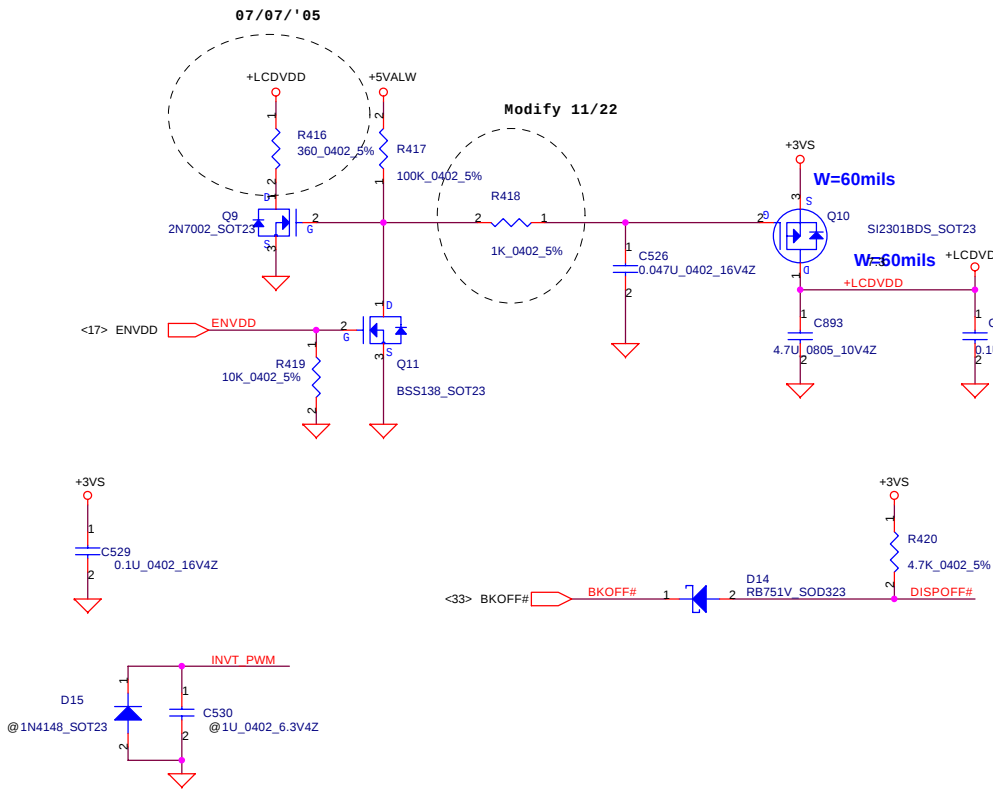


TV-OUT Conn.

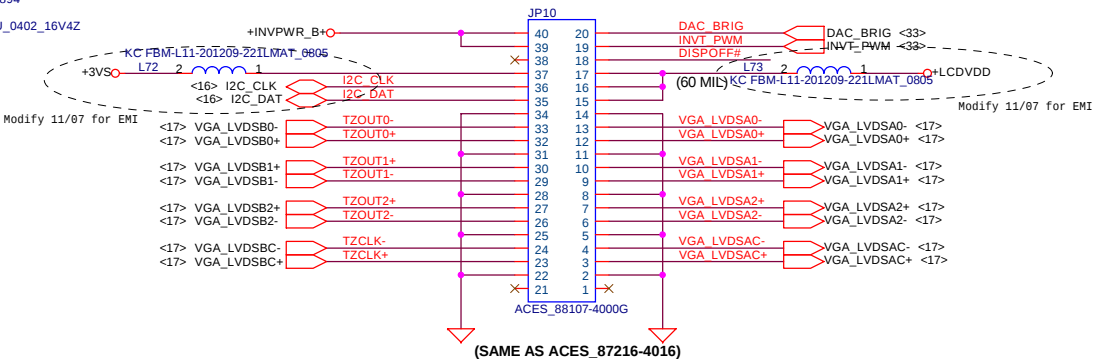


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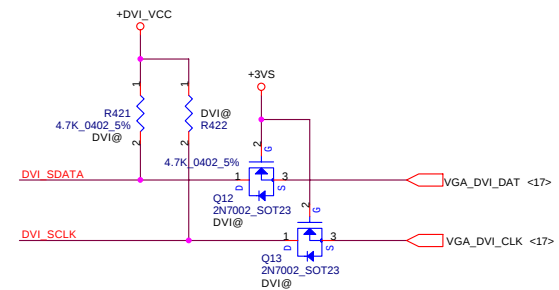
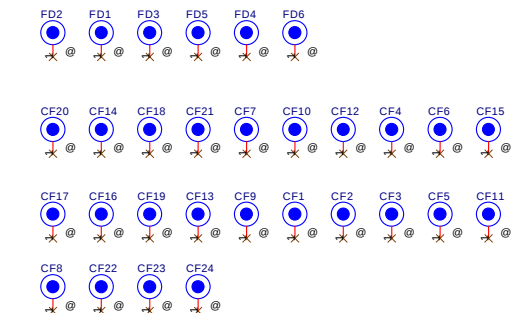
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

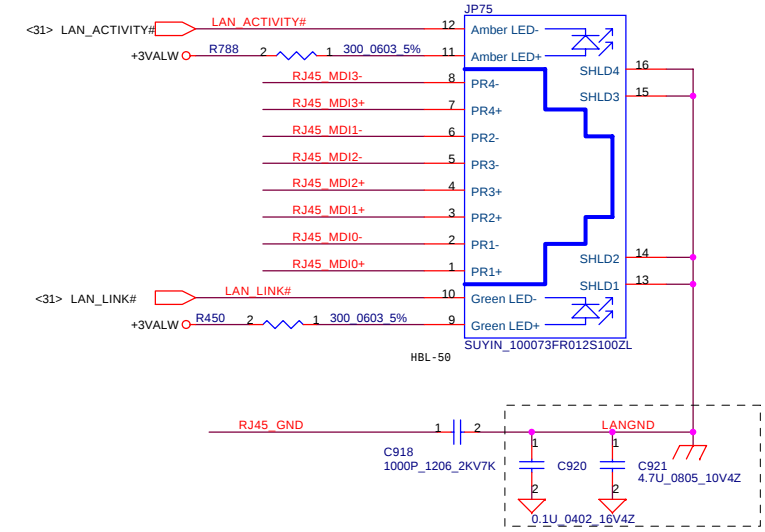
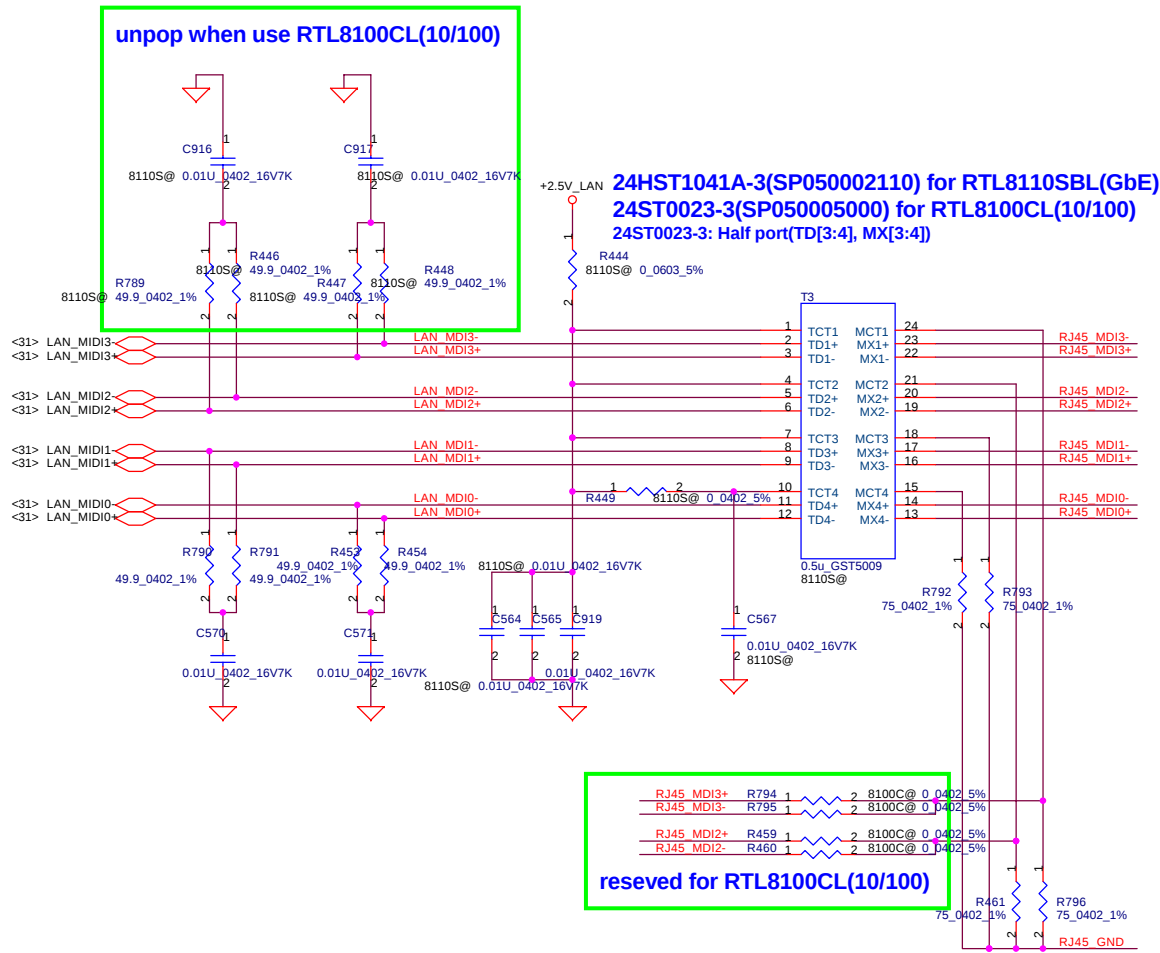


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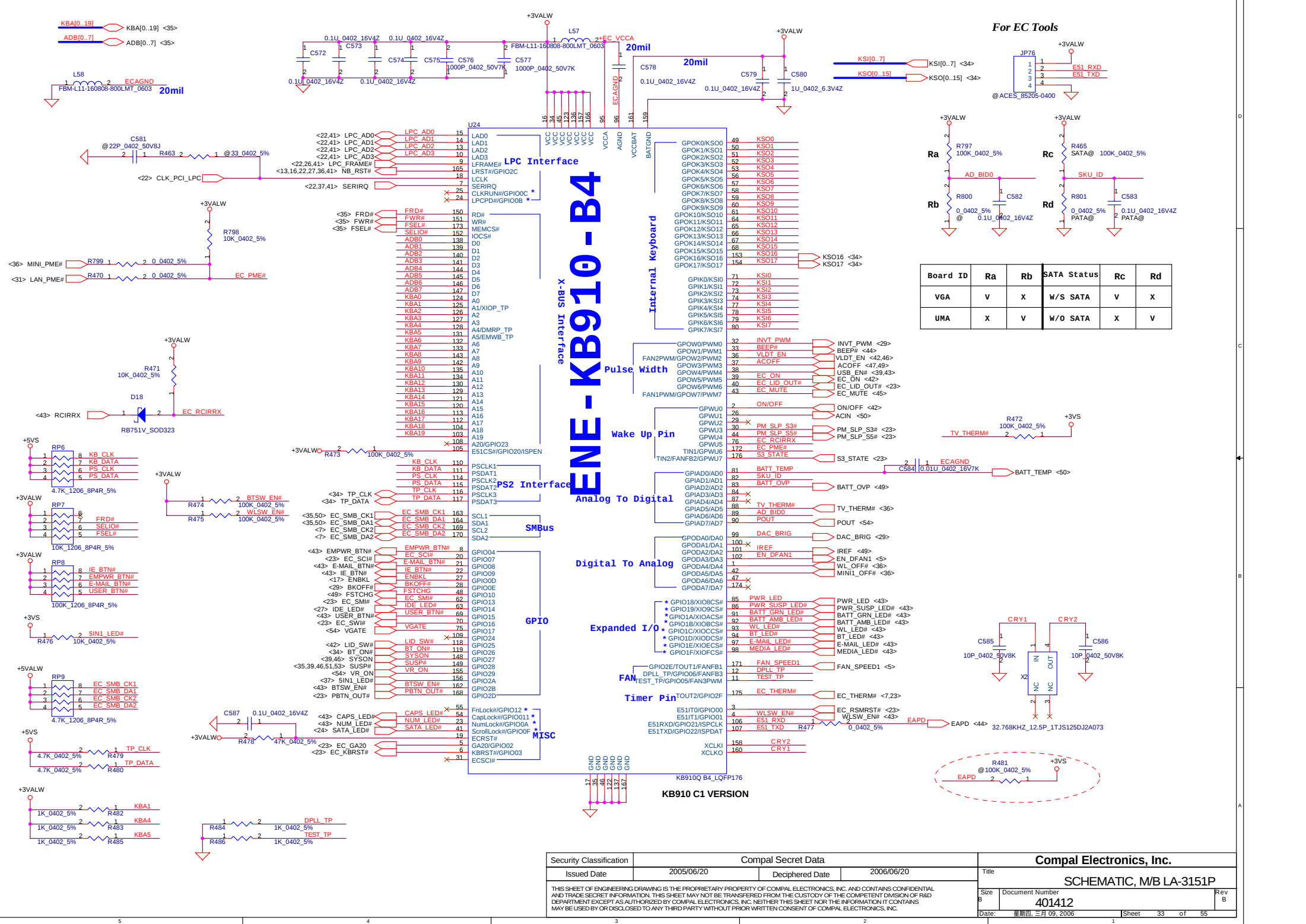


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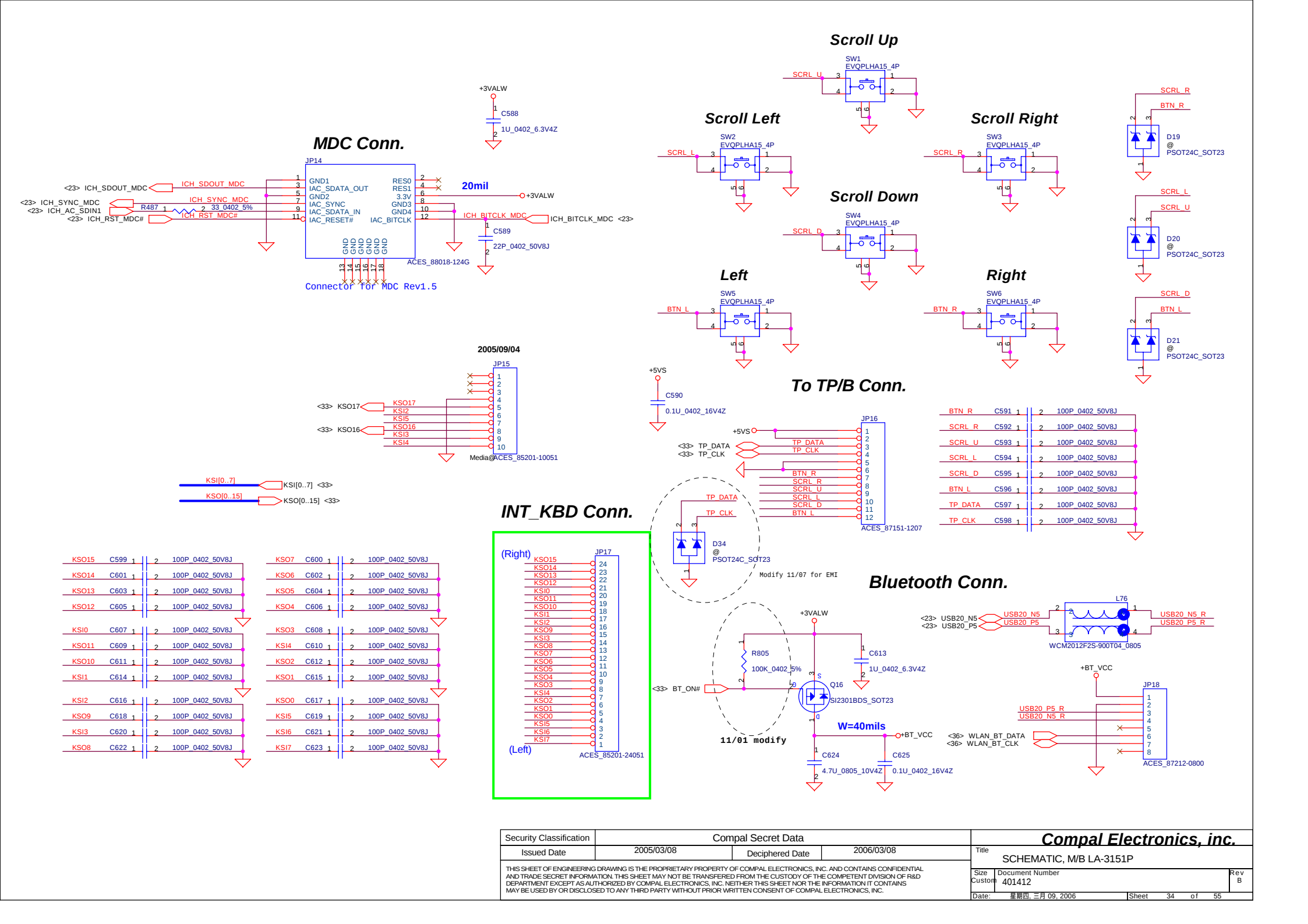
LAN RTL8110SBL/RTL8100CL



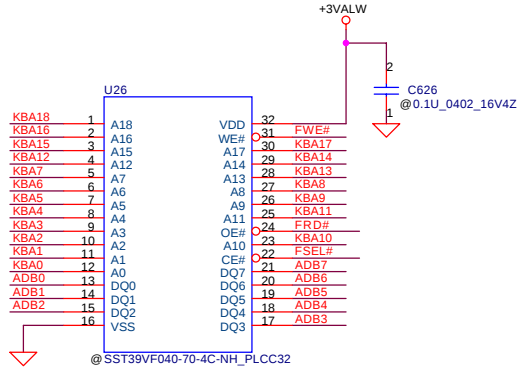
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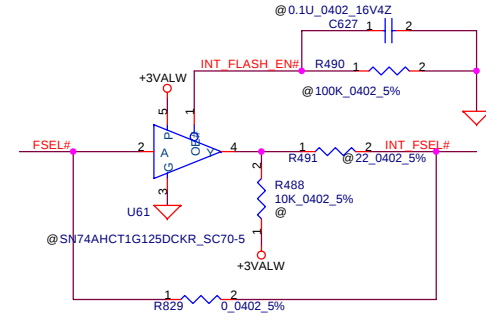
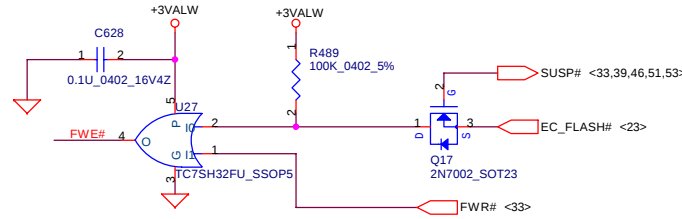
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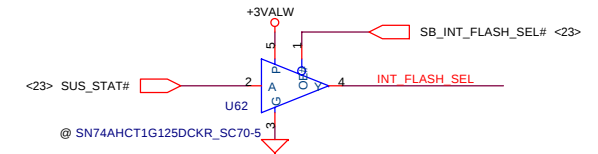
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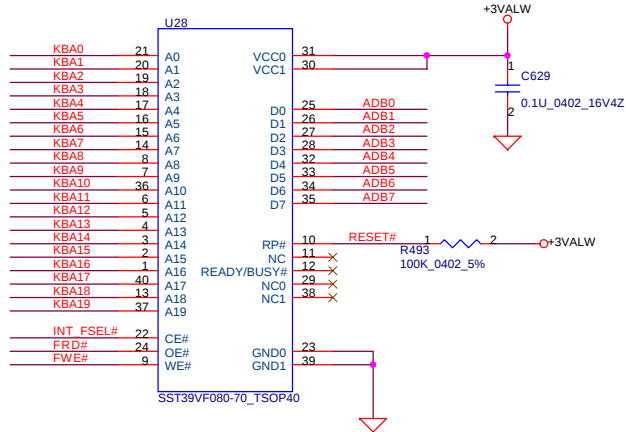
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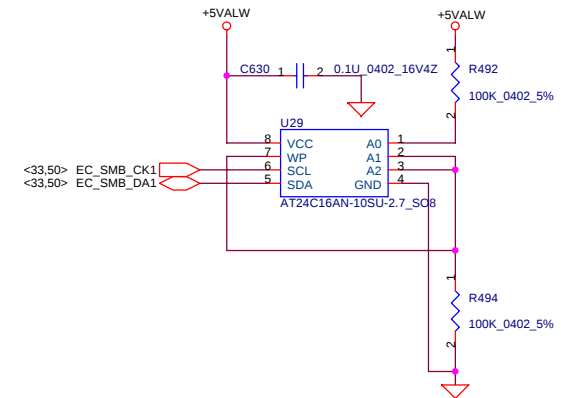
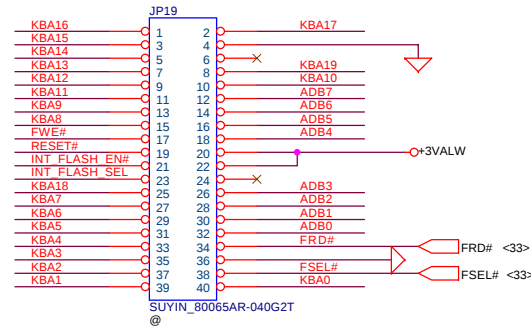
FOR DEBUG ONLY



1MB Flash ROM



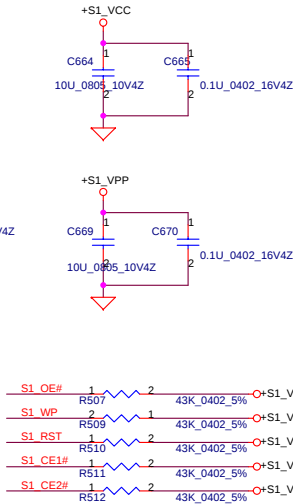
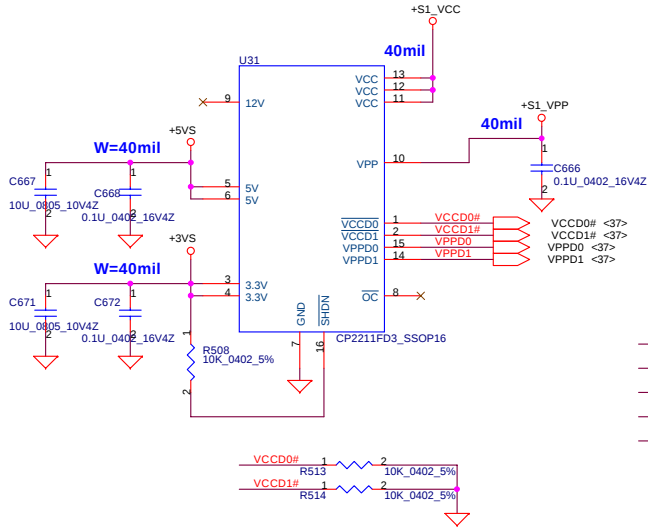
1MB Flash ROM



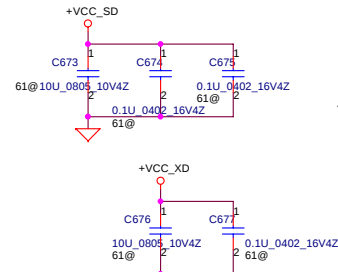
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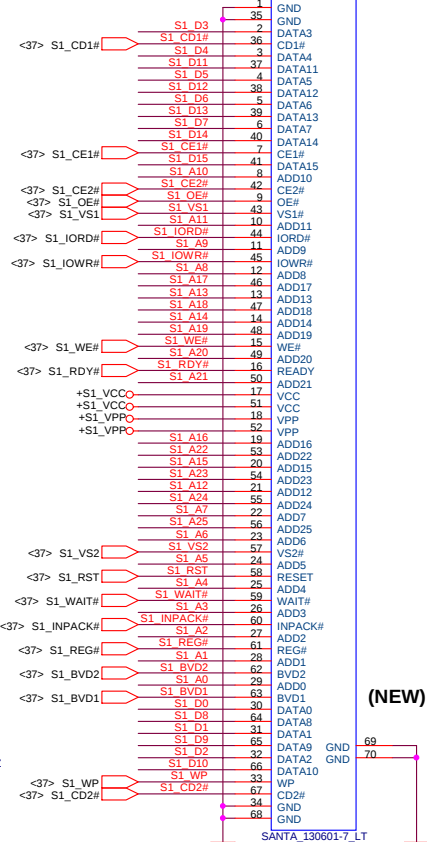
PCMCIA Power Control



<37> S1_A[0..25] S1_A[0..25]
<37> S1_D[0..15] S1_D[0..15]

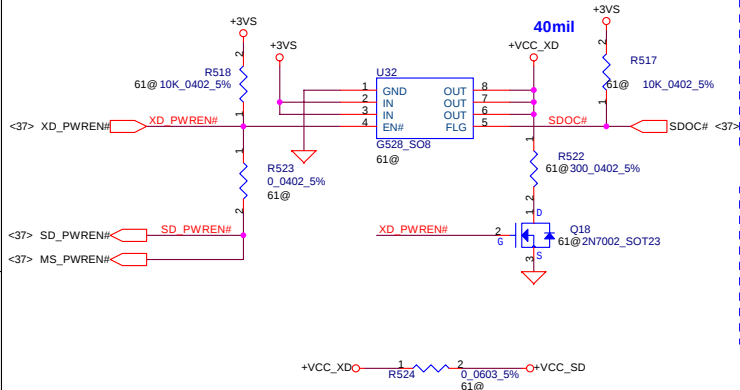


PCMCIA Socket

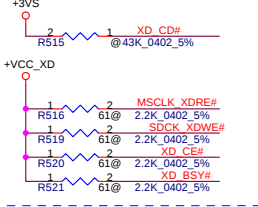


SD/MS Power Control

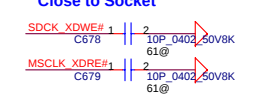
XD Power Control



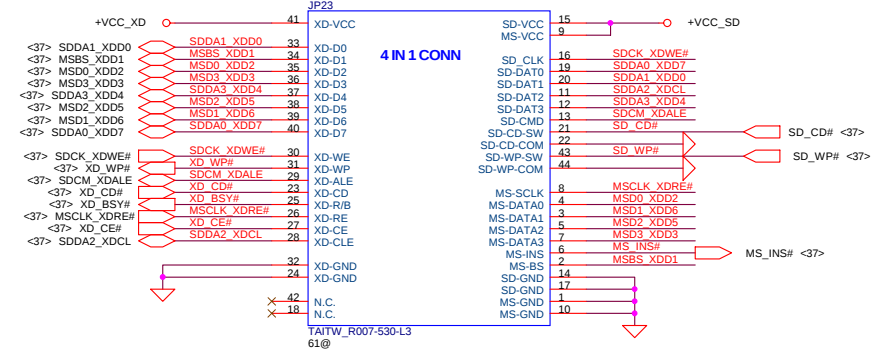
xD PU and PD. Close to Socket



Reserve for SD,MS CLK. Close to Socket



4 IN 1 Socket (HDQ70)



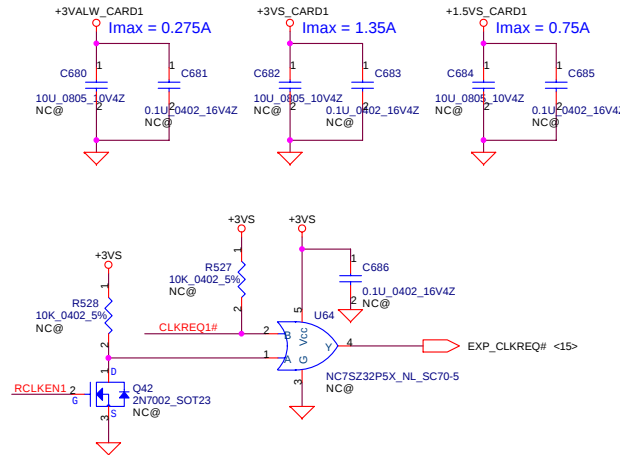
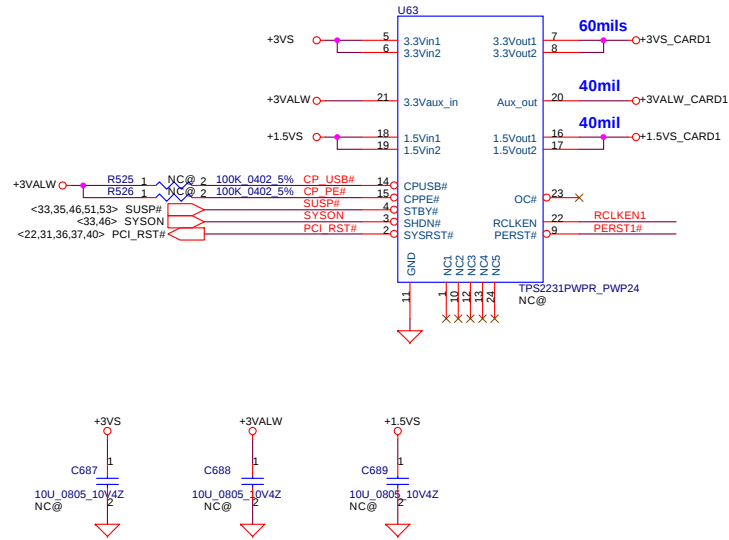
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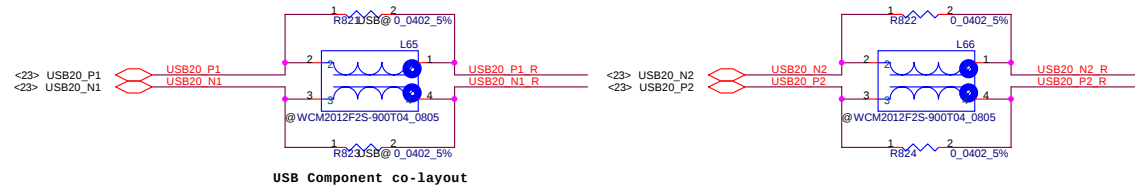
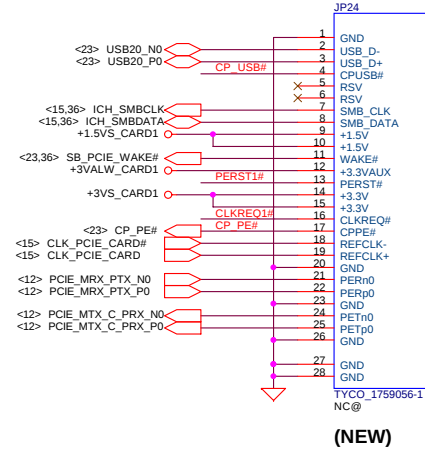
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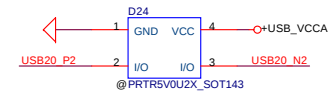
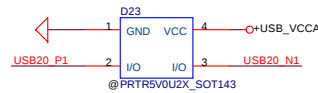
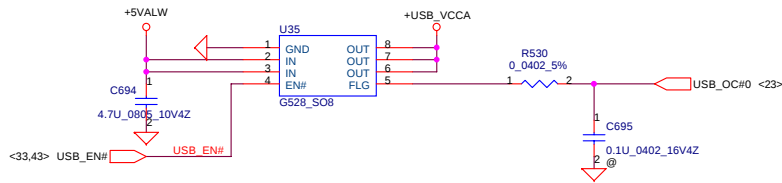
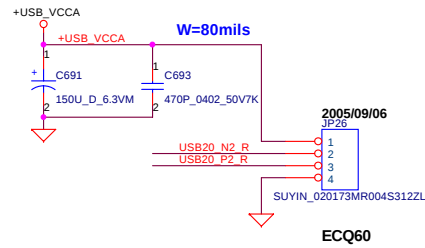
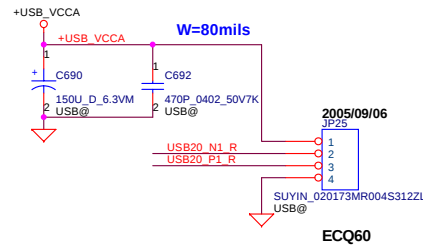
New Card Power Switch



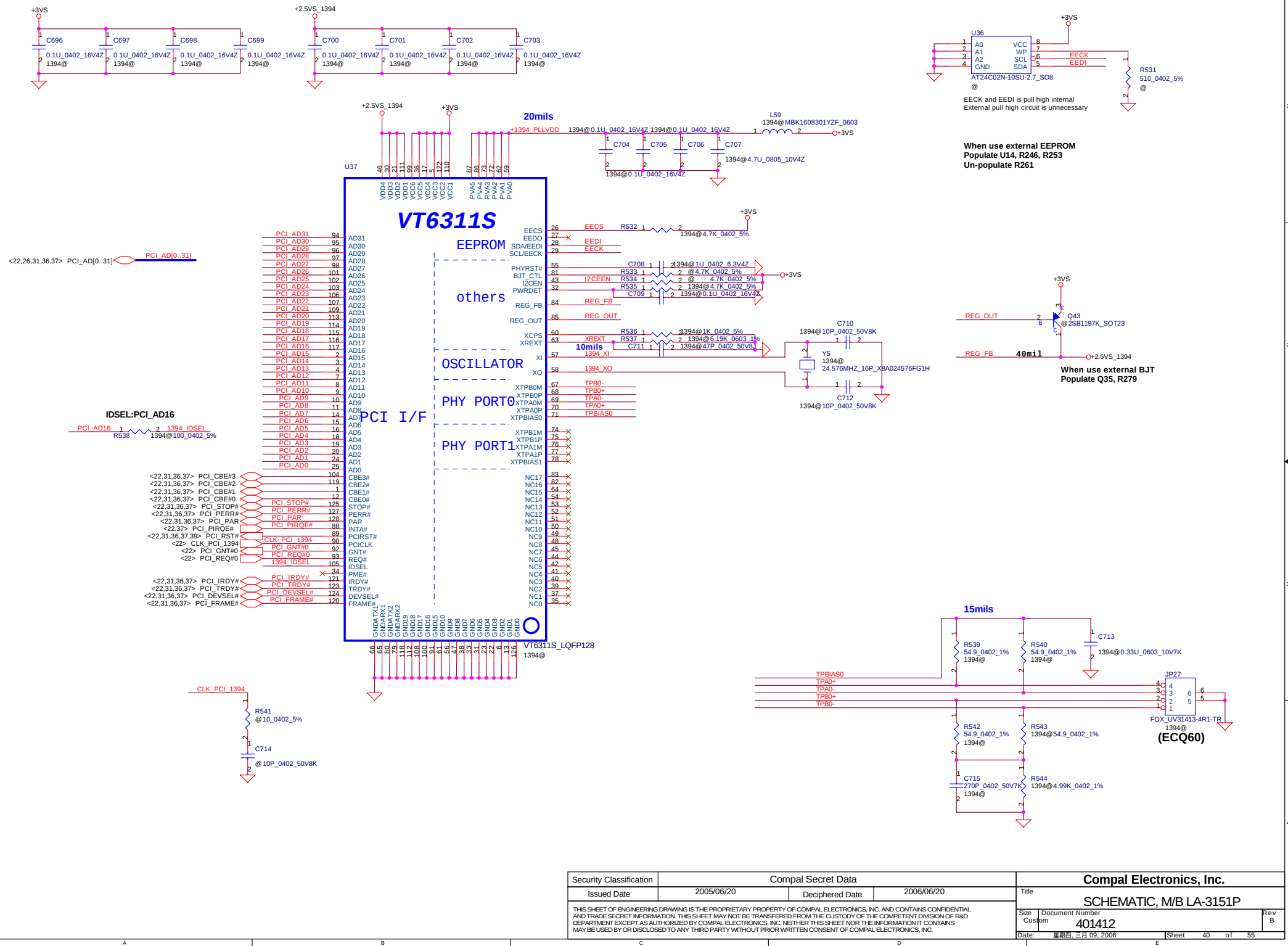
New Card Socket (Left)



USB CONN. 1 & 2

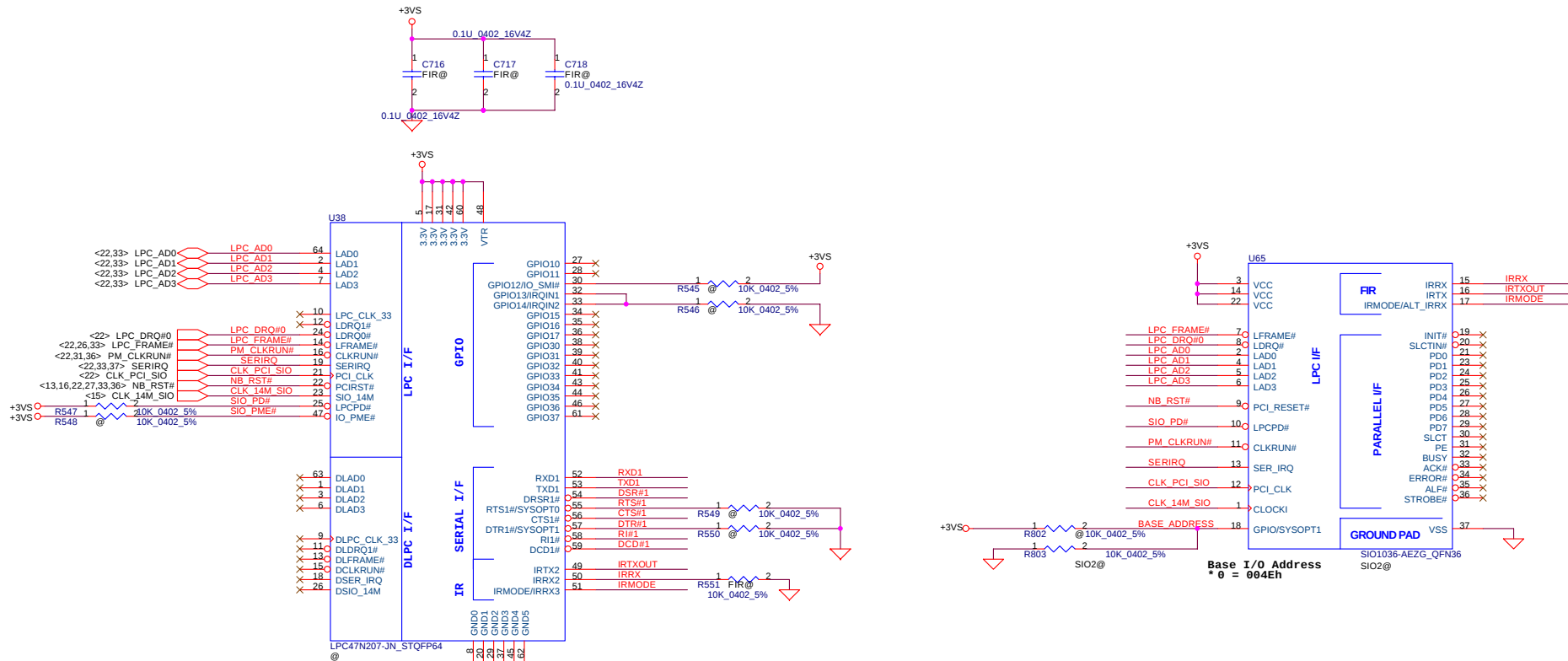


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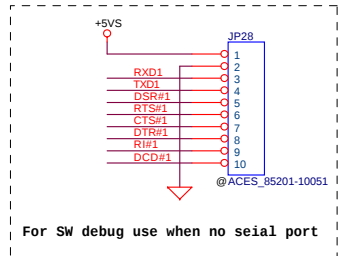
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SUPER I/O SMSc LPC47N207

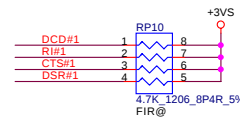


RTS#1
Base I/O Address
* 0 = 02Eh
1 = 04Eh

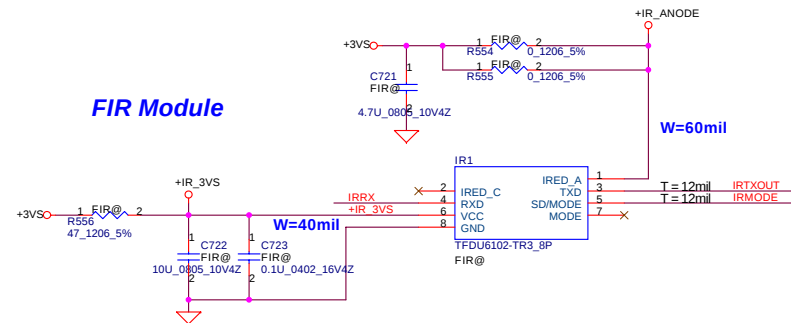
Place on the BOT side(near MINIPCI conn.)



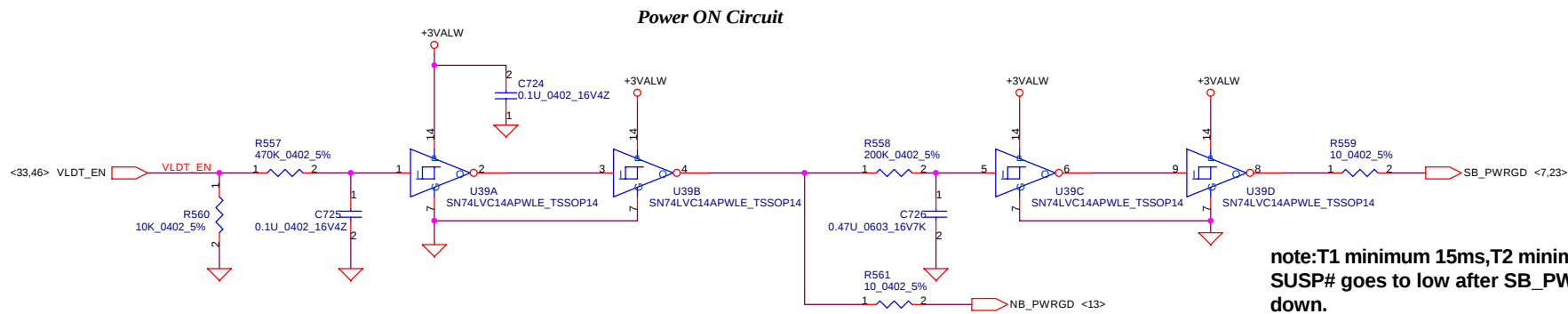
For SW debug use when no seial port



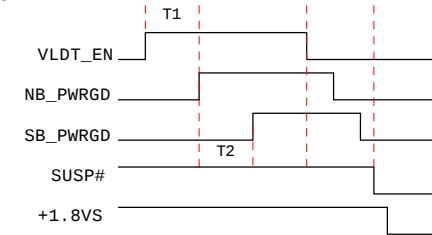
FIR Module



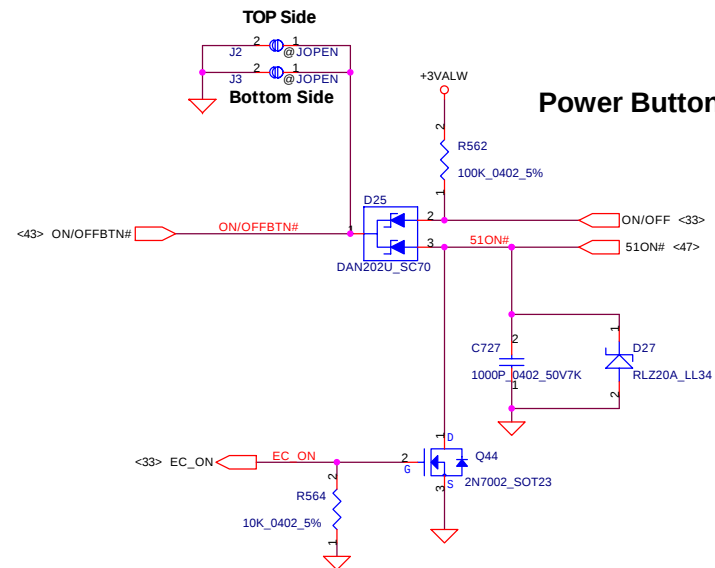
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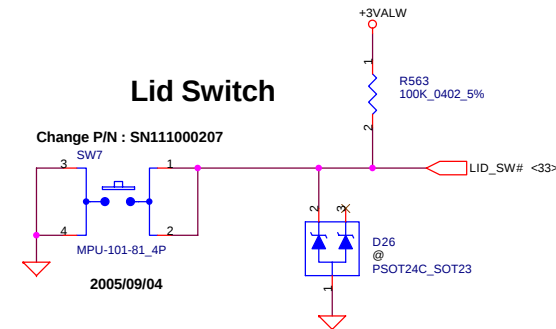
note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



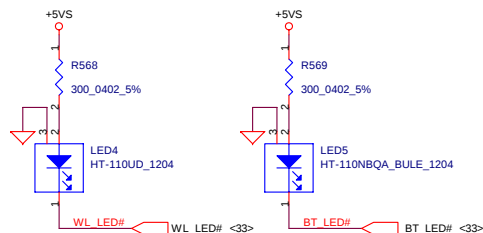
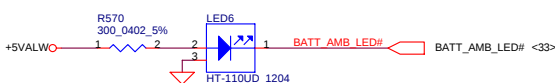
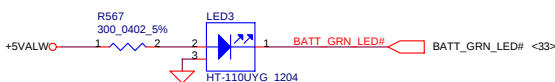
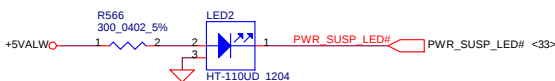
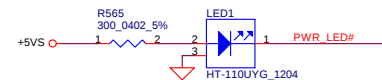
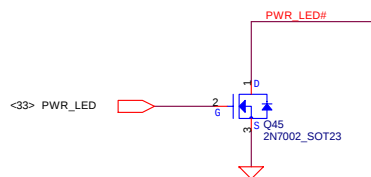
ON/OFF switch



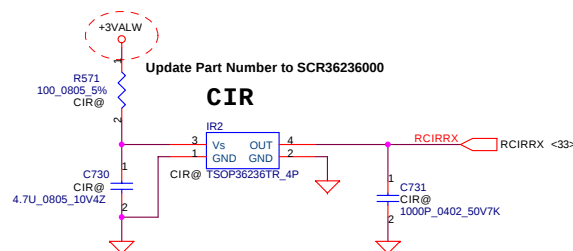
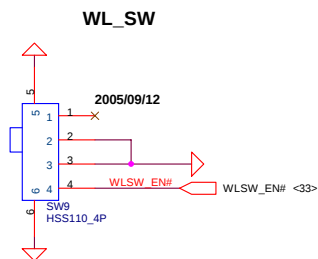
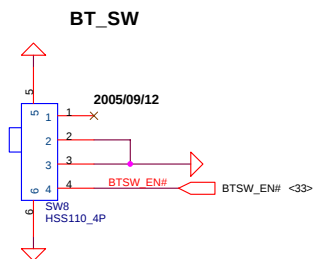
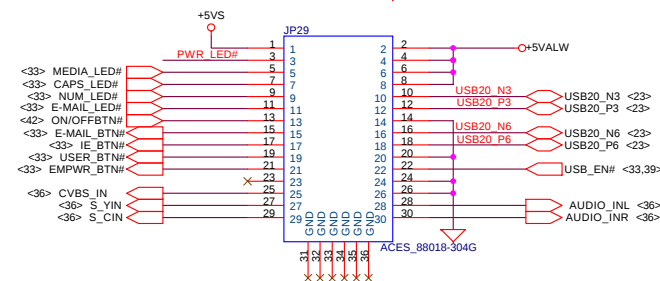
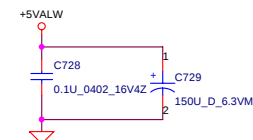
Lid Switch



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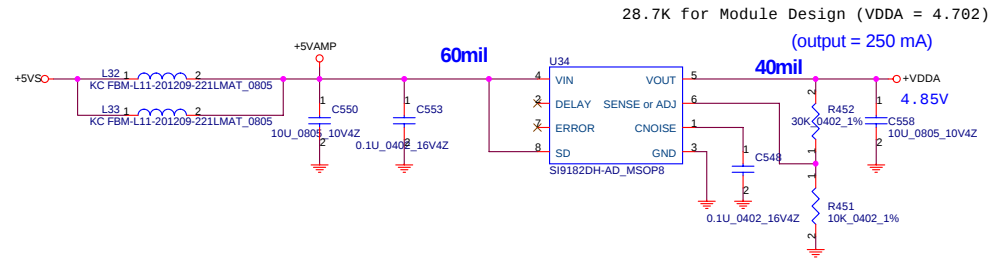
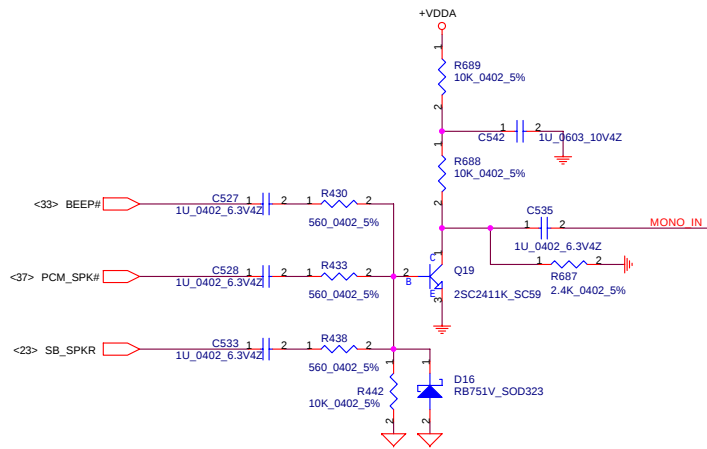


To LED/B Conn.

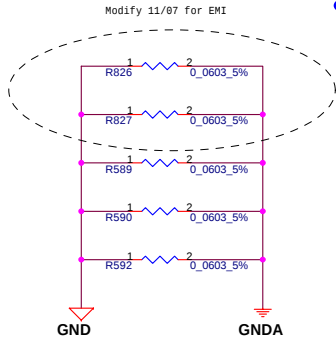
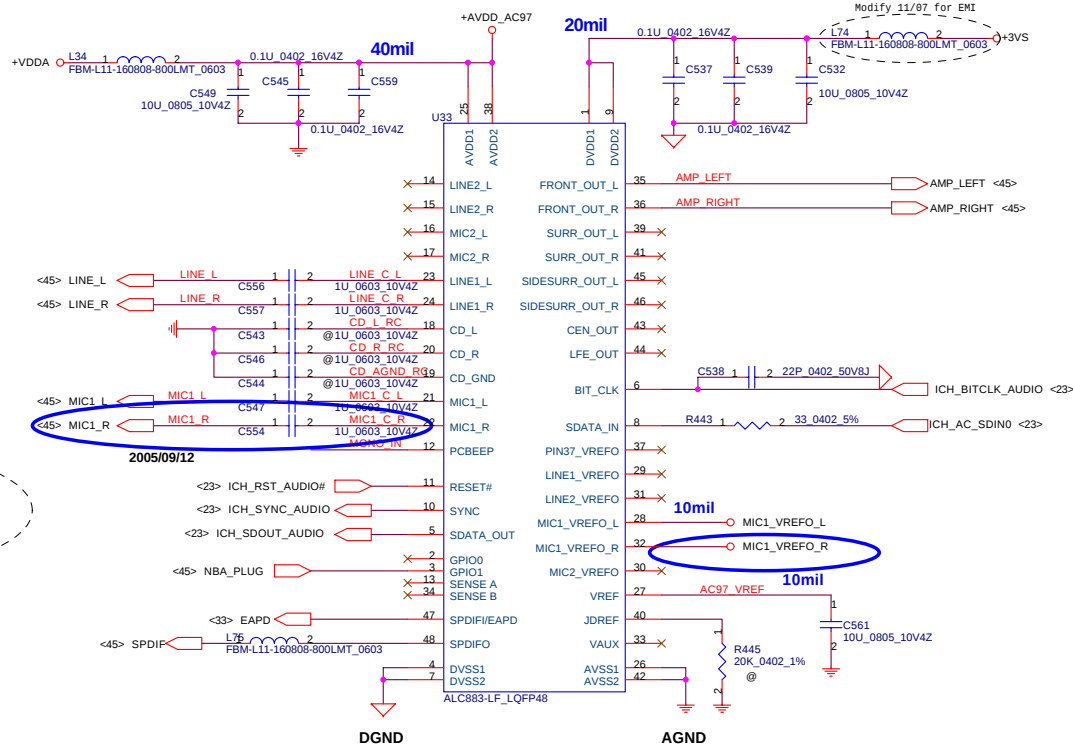


Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER	KSI2	PLAY	
KSI3	STOP		KSI3	STOP	VOL_UP
KSI4	NEXT		KSI4	NEXT	VOL_DOWN
KSI5	REV		KSI5	REV	ARCADE_TV
KSI6		RECORD			

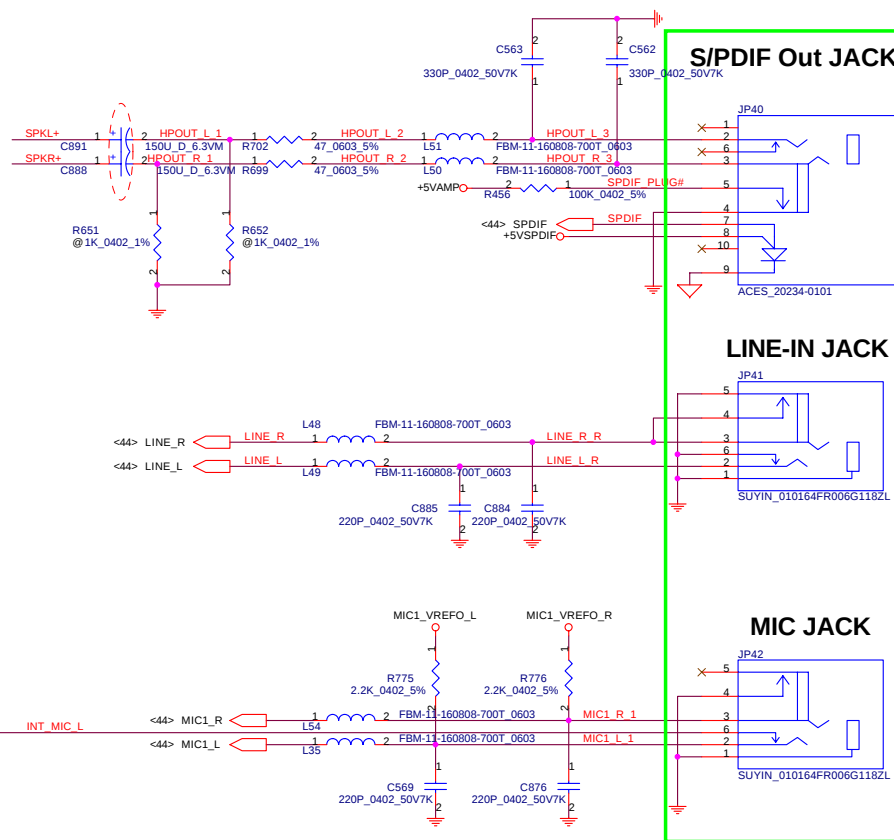
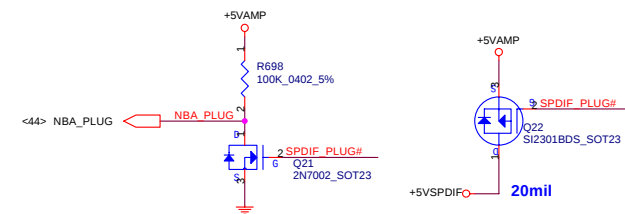
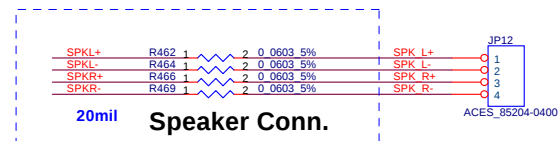
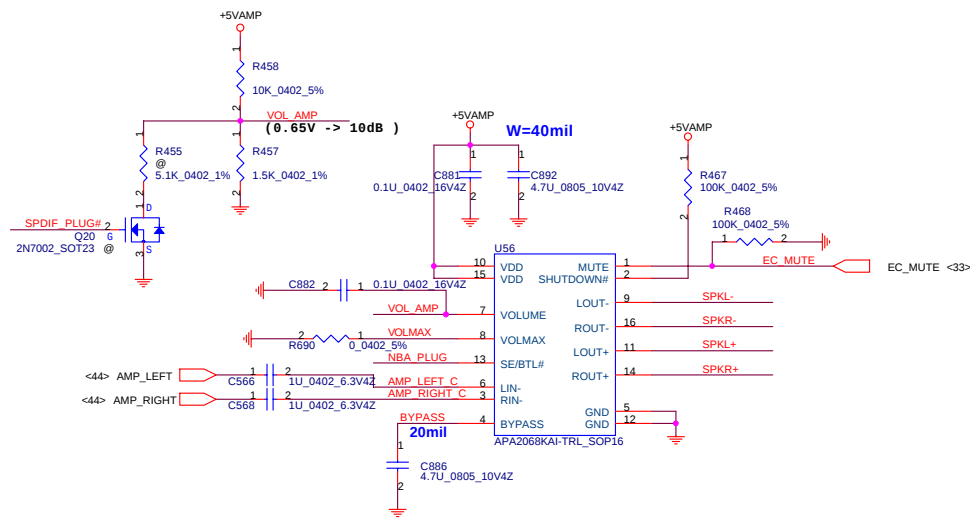
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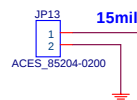
HD Audio Codec



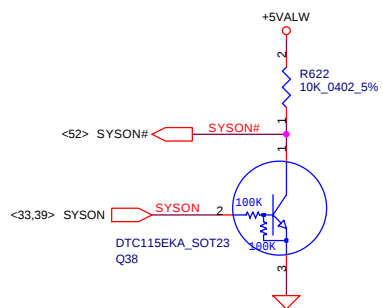
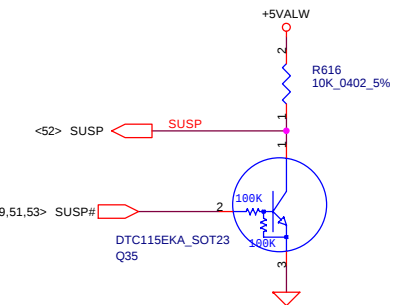
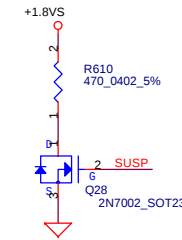
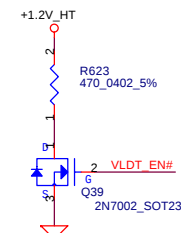
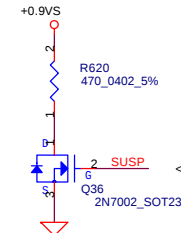
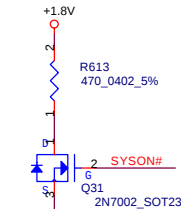
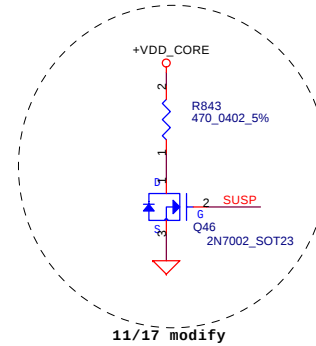
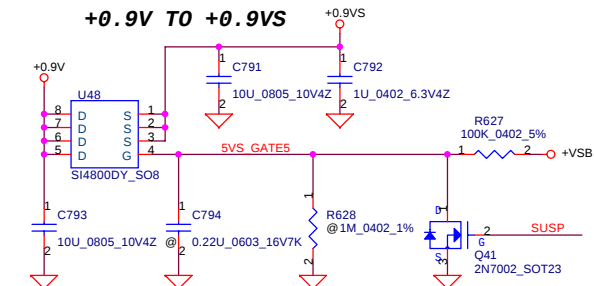
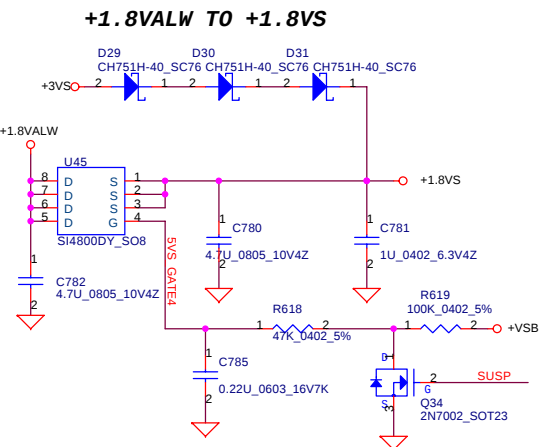
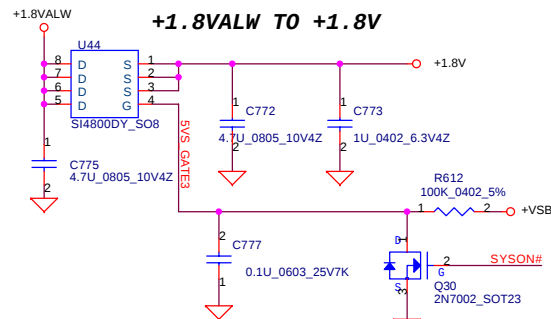
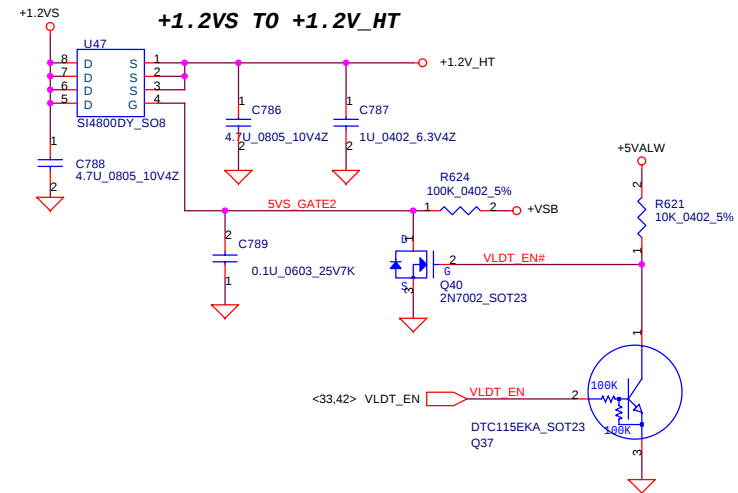
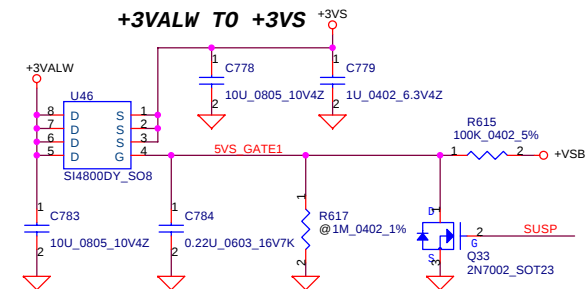
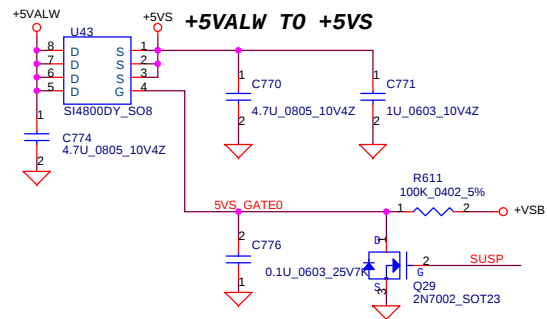
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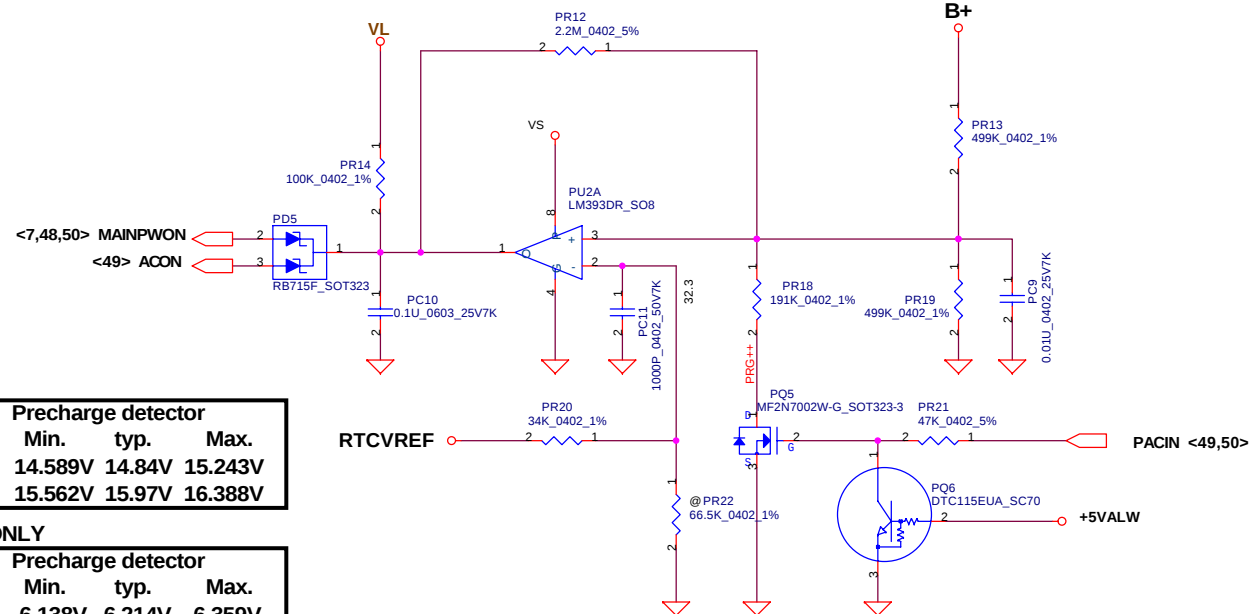
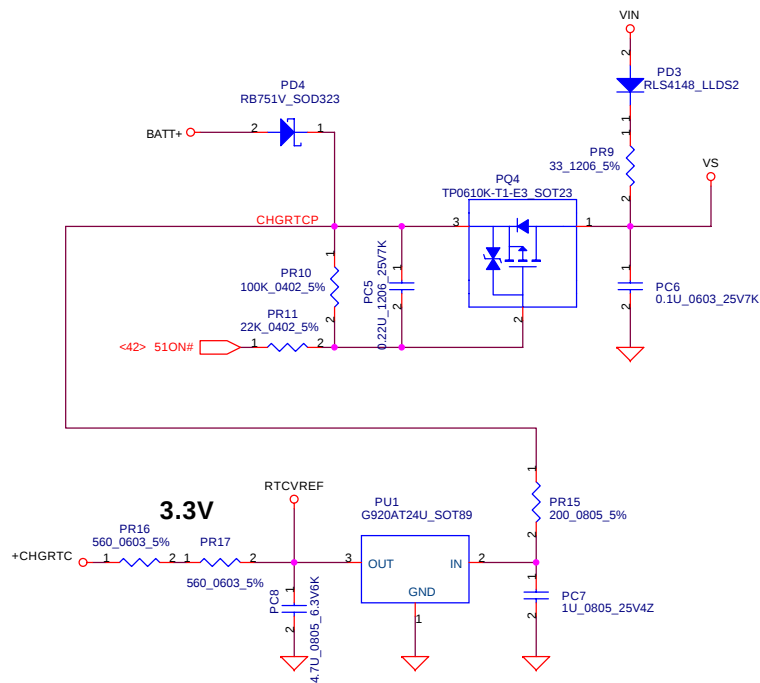
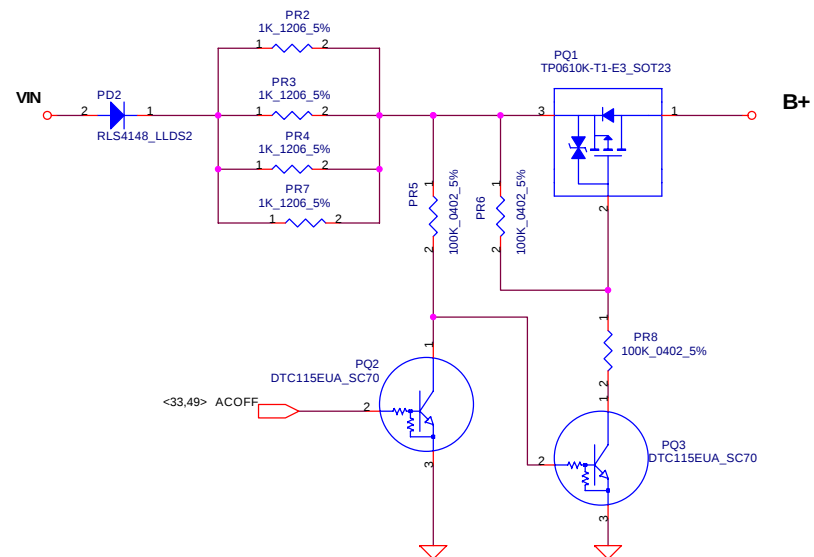
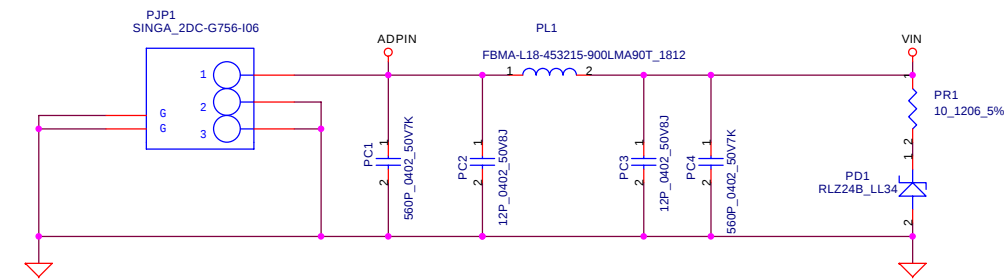
Int MIC Conn.



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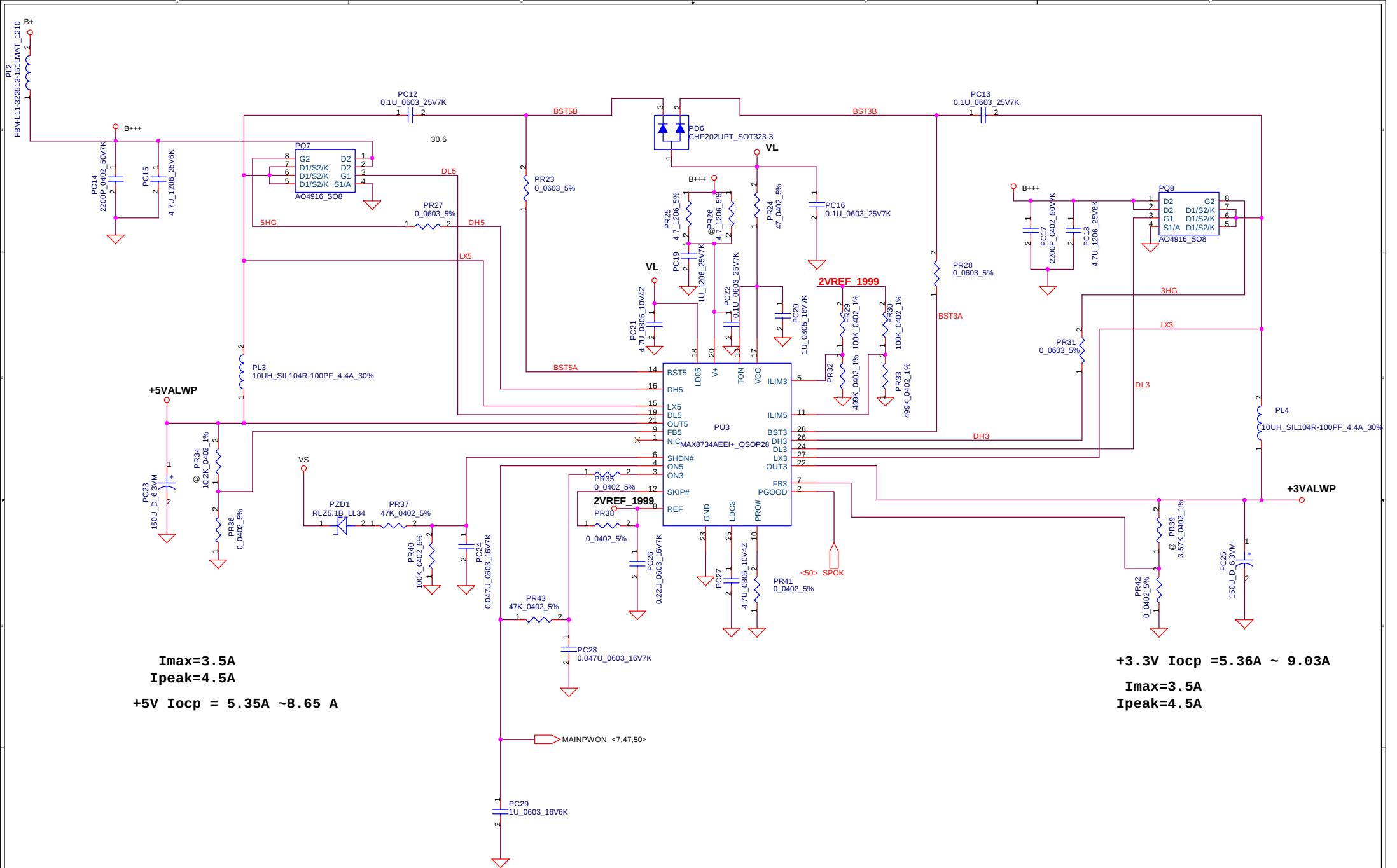
ACIN

	Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V	
L-->H	15.562V	15.97V	16.388V	

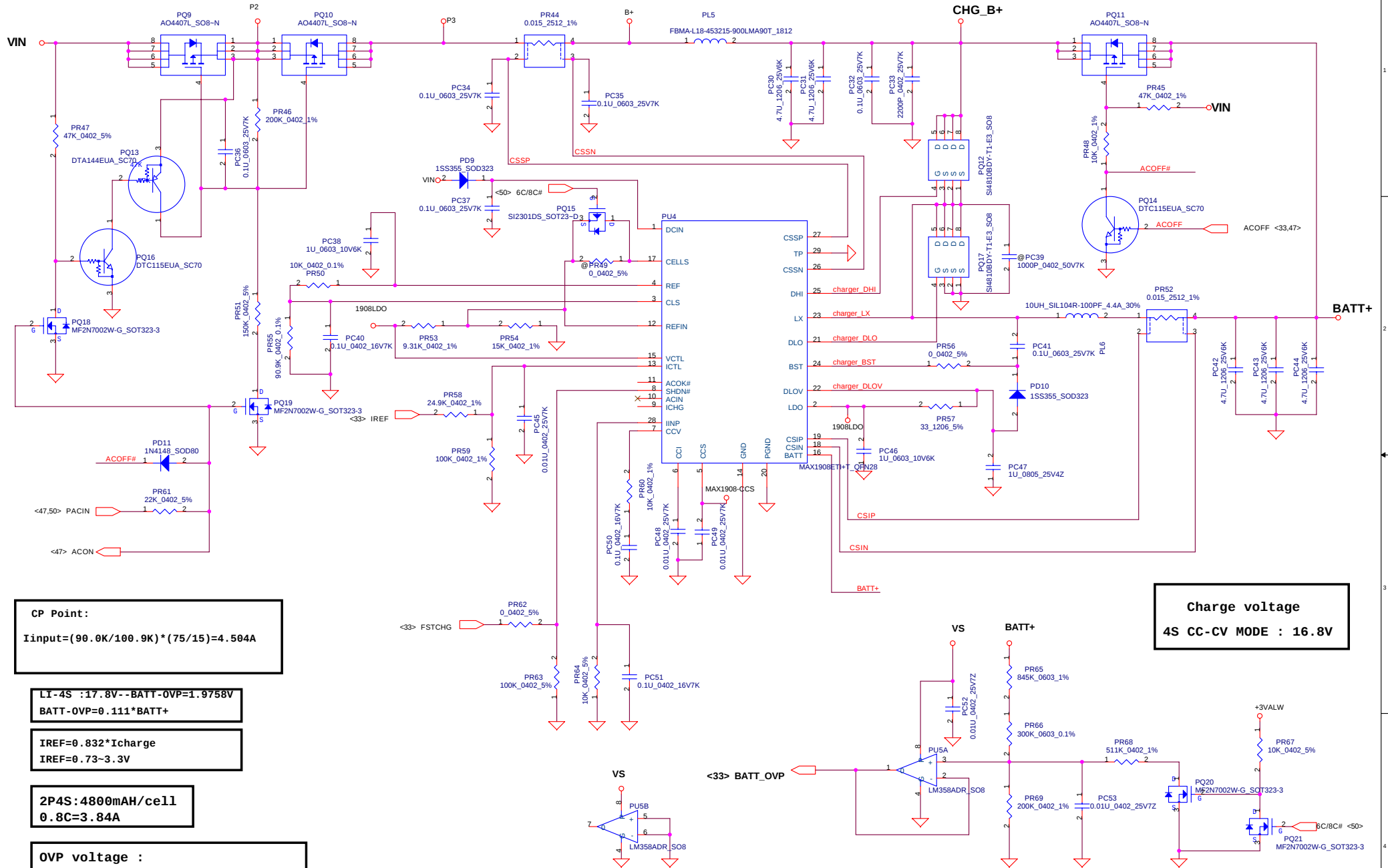
BATT ONLY

	Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V	
L-->H	7.196V	7.349V	7.505V	

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I_{adp}=0~4.5A (90W)

CP Point:

$$I_{\text{input}} = (90.0\text{K} / 100.9\text{K}) * (75/15) = 4.504\text{A}$$

LI-4S : 17.8V -- BATT-OVP = 1.9758V

BATT-OVP = 0.111 * BATT+

IREF = 0.832 * I_{charge}

IREF = 0.73 ~ 3.3V

2P4S : 4800mAh/cell

0.8C = 3.84A

OVP voltage :

LI-3S : 17.8V --- BATT-OVP = 1.9758V

BATT-OVP = 0.111 * BATT+

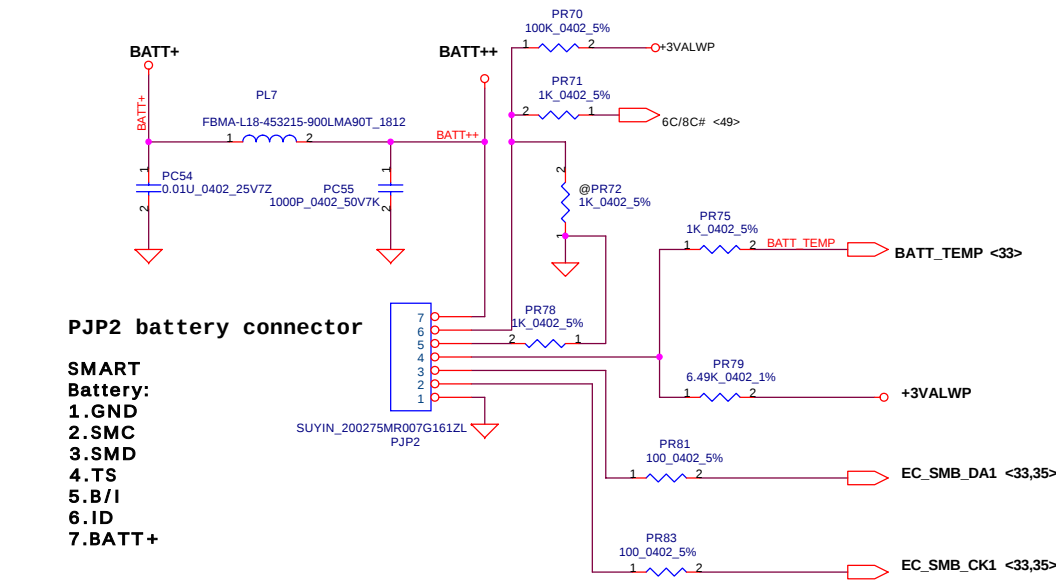
Charge voltage

4S CC-CV MODE : 16.8V

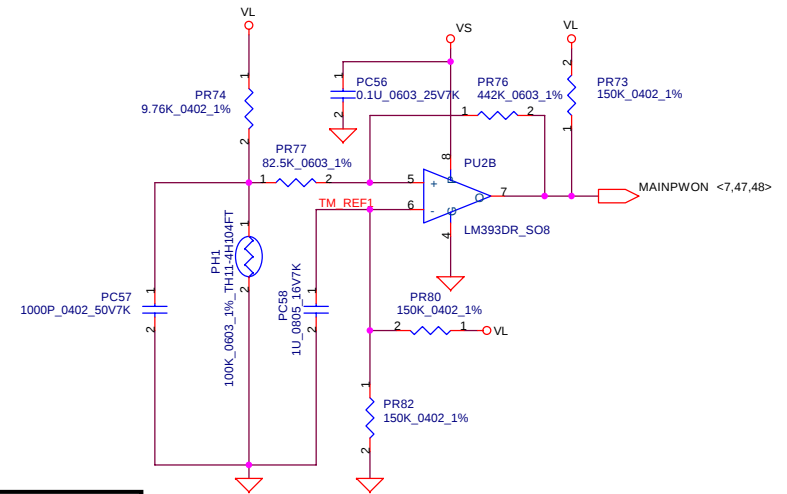
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PJP2 battery connector

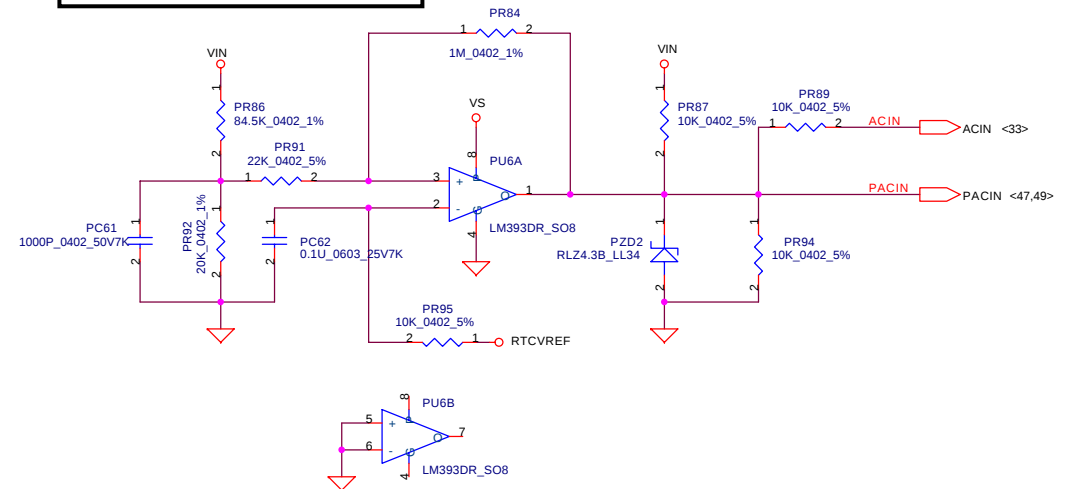
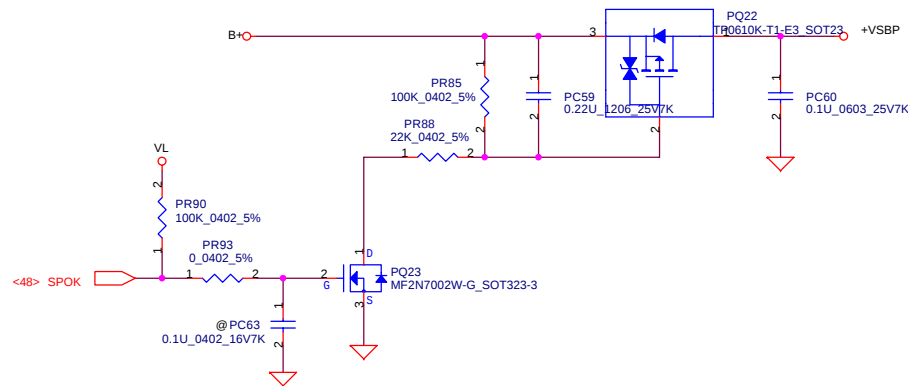
SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



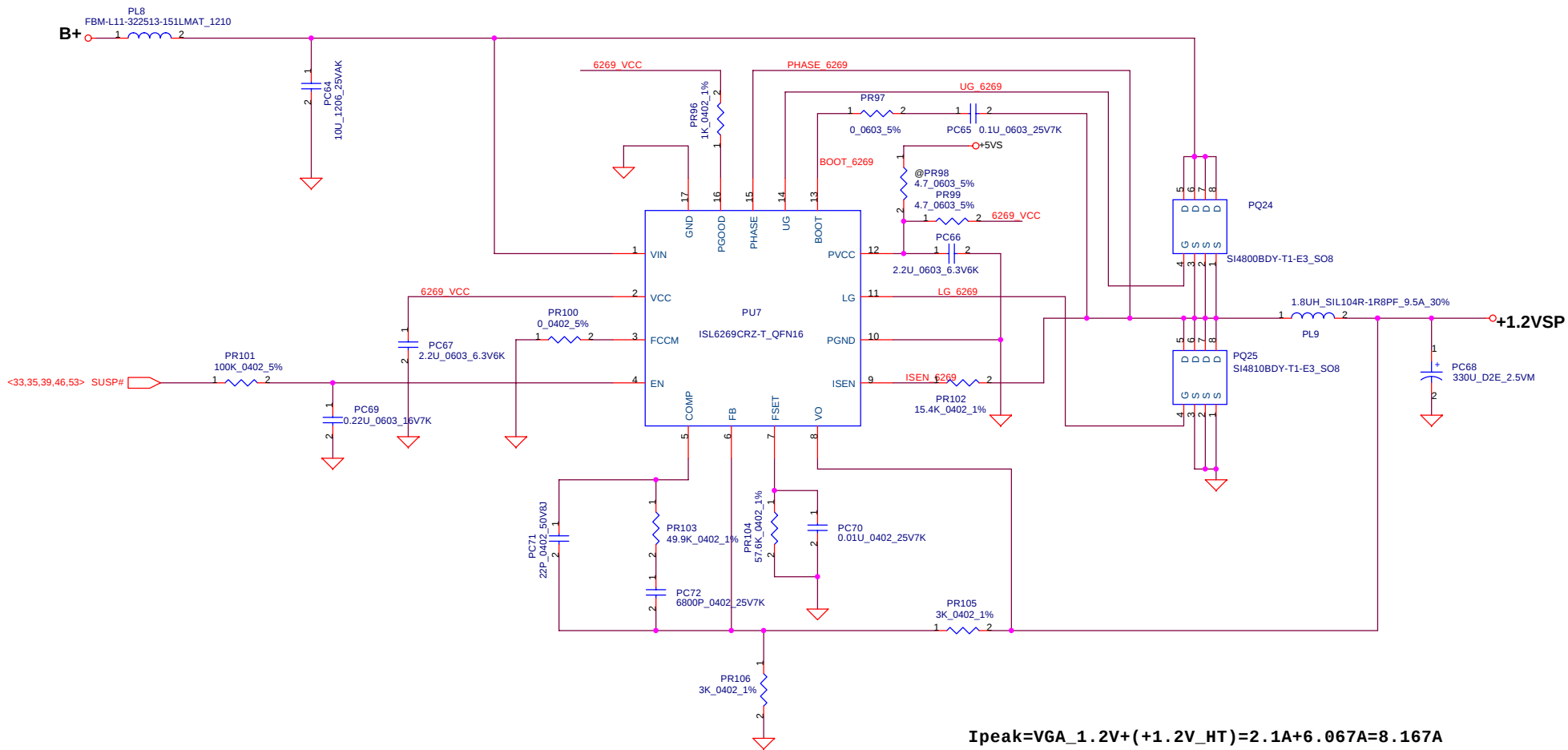
PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C



Vin Detector
 Min. typ. Max.
 H-->L 16.976V 17.257V 17.728V
 L-->H 17.430V 17.901V 18.384V

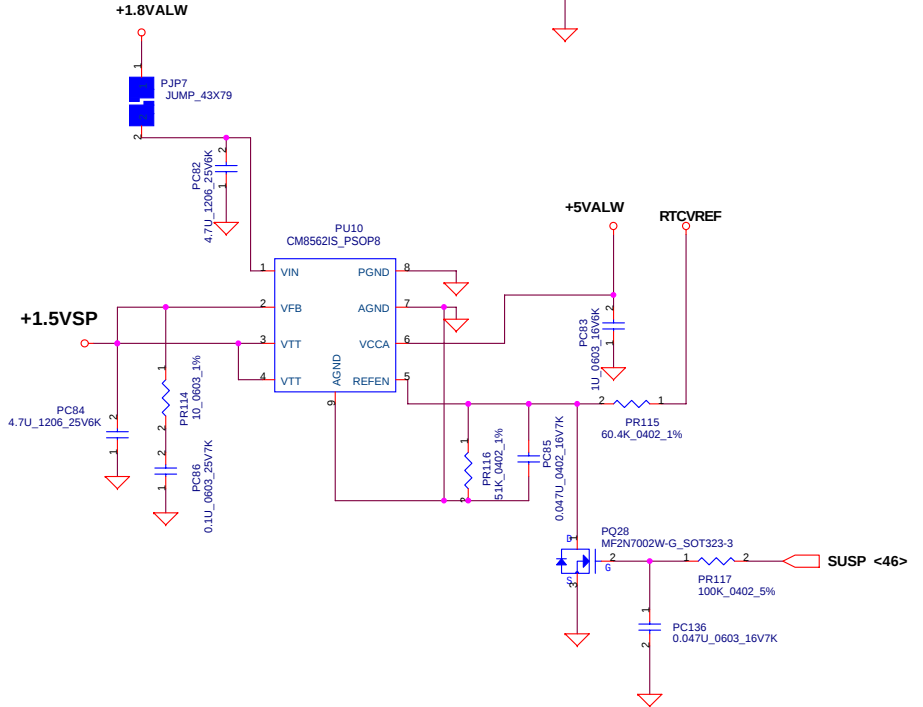
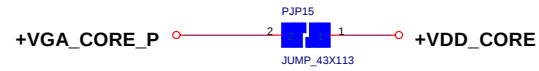
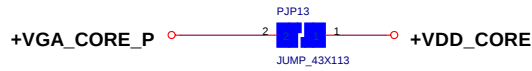
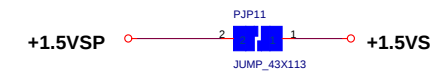
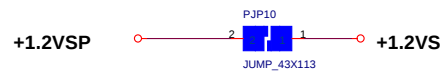
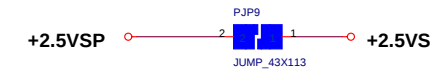
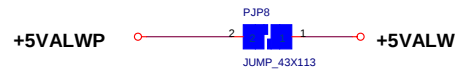
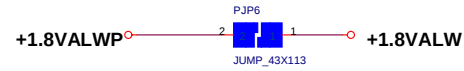
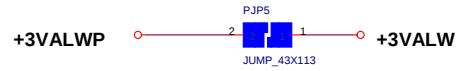
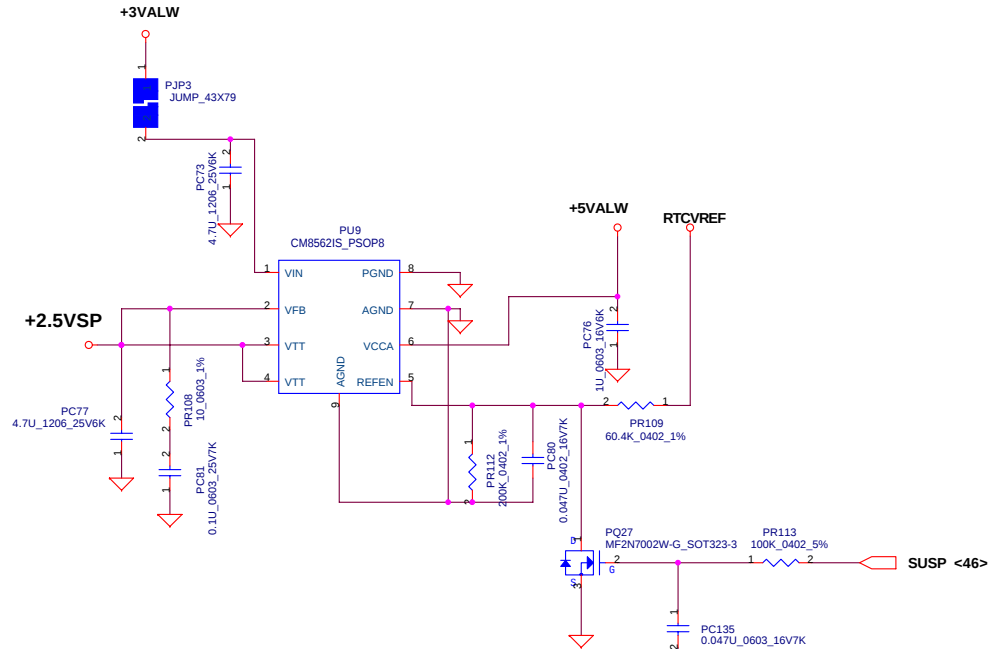
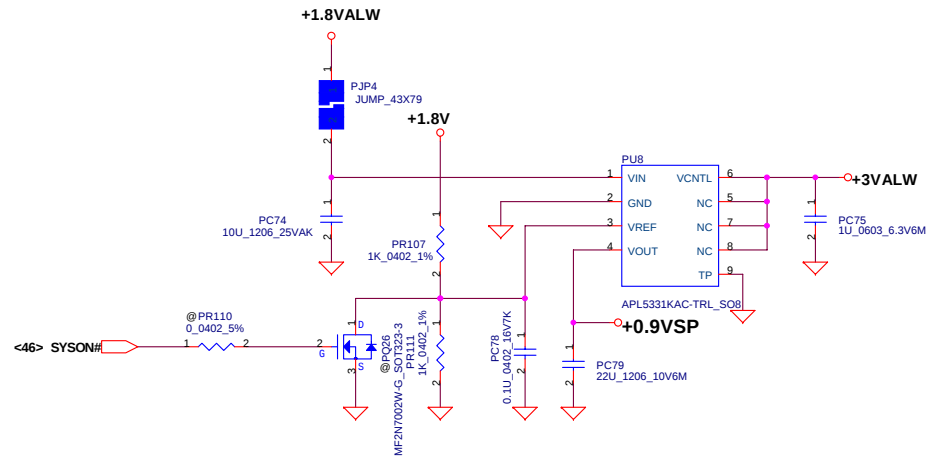


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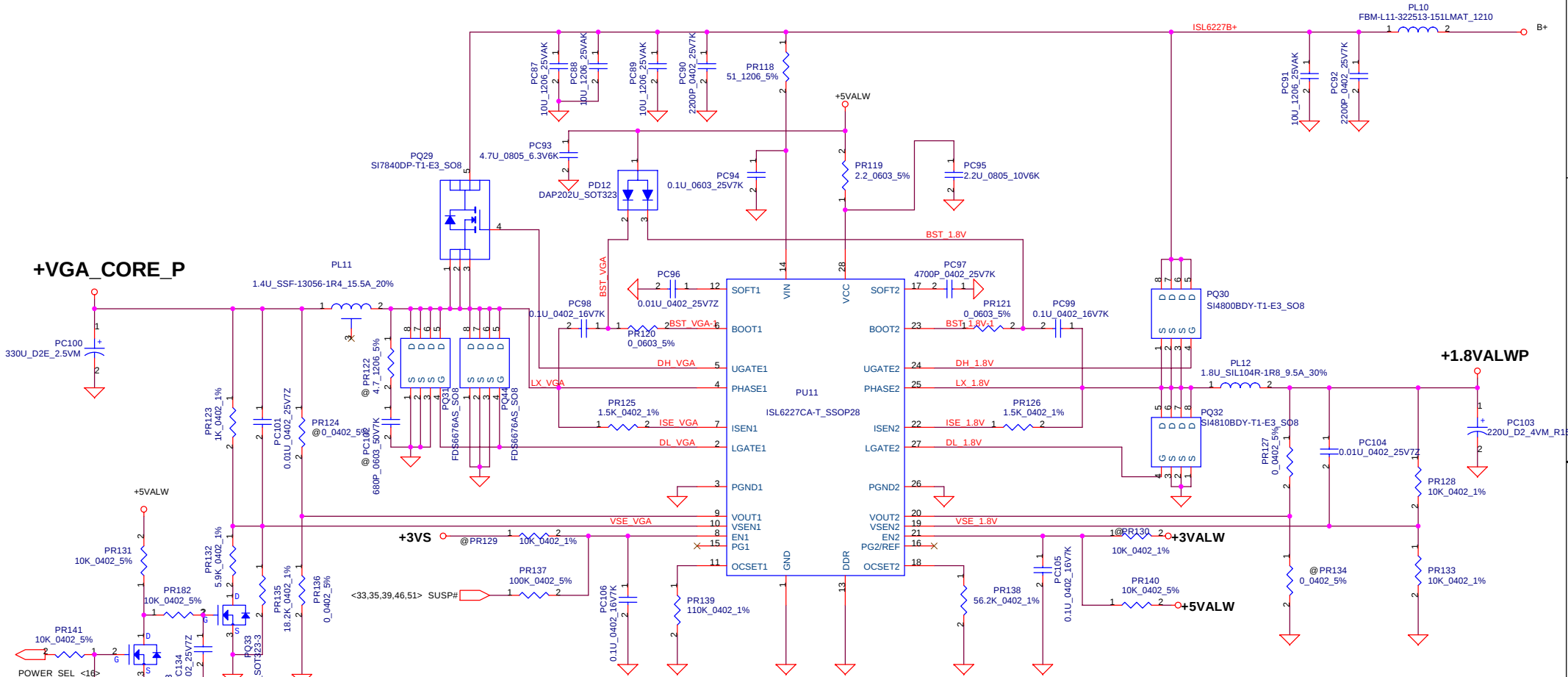


Ipeak=VGA_1.2V+(+1.2V_HT)=2.1A+6.067A=8.167A
Imax=5.7A
Iocmin=9.23A
Iocmax=19.23A

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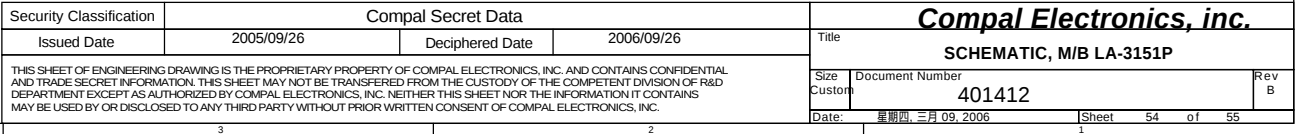


For VGA chipset type, that should be dynamic change by everytime load BOM.

Ipeak=16.40A
Imax=12.25A
Iocpmin=22.07A
Iocpmax=38.67A

Ipeak=8.5A
Imax=6A
Iocpmin=8.76A
Iocpmax=13.46A

M52P6	M54P	M56P
PR123=1K	PR123=1K	PR123=1K
PR135=18.2K	PR135=8.87K	PR135=18.2K
PR132=17.8K	PR132=8.87K	PR132=5.9K
L=1.000V	L=1.102V	L=1.102V
H=0.949V	H=1.001V	H=0.949V



Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
8							
9							