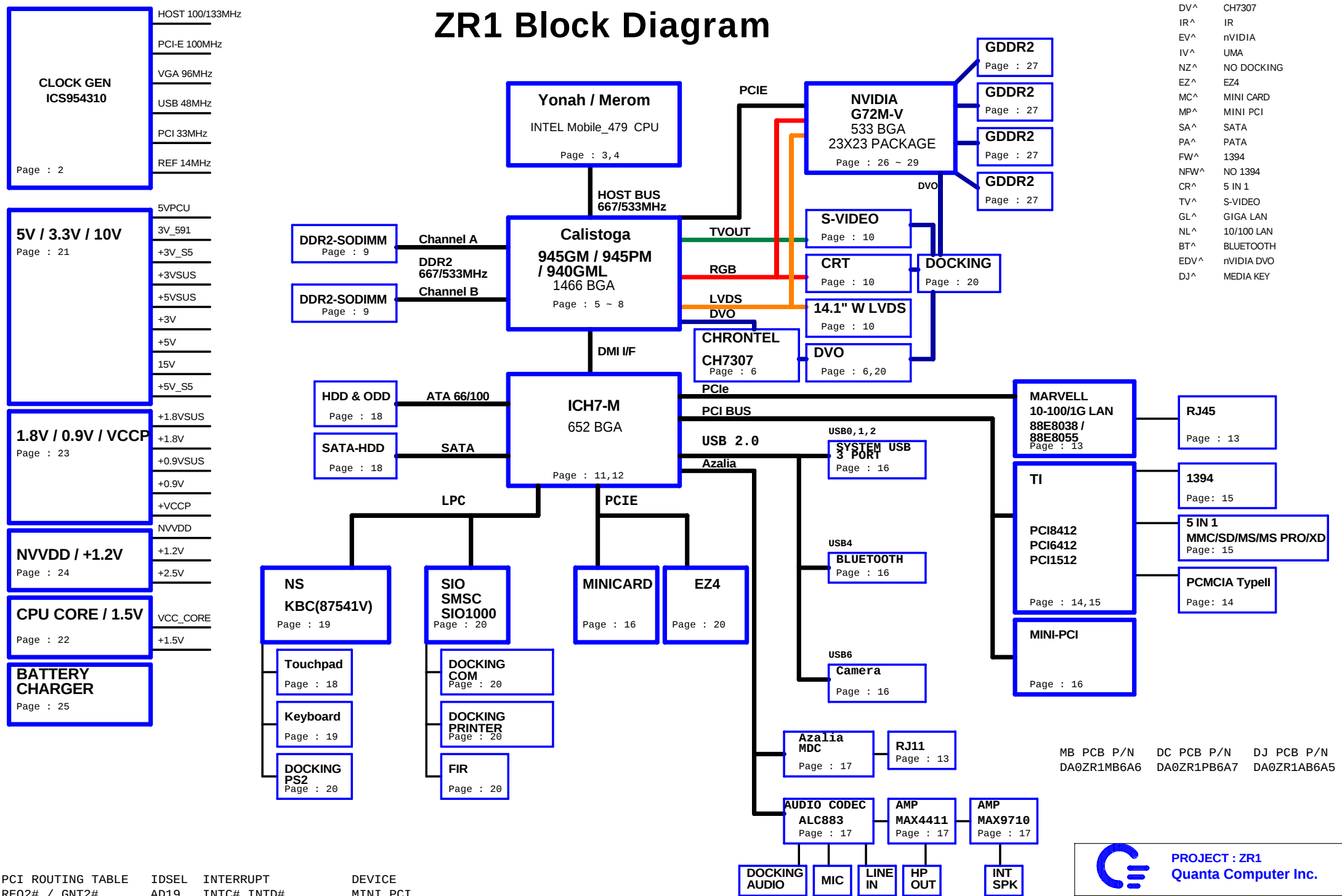


ZR1 Block Diagram



- DV^ CH7307
- IR^ IR
- EV^ nVIDIA
- IV^ UMA
- NZ^ NO DOCKING
- EZ^ EZ4
- MC^ MINI CARD
- MP^ MINI PCI
- SA^ SATA
- PA^ PATA
- FW^ 1394
- NFW^ NO 1394
- CR^ 5 IN 1
- TV^ S-VIDEO
- GL^ GIGA LAN
- NL^ 10/100 LAN
- BT^ BLUETOOTH
- EDV^ nVIDIA DVO
- DJ^ MEDIA KEY

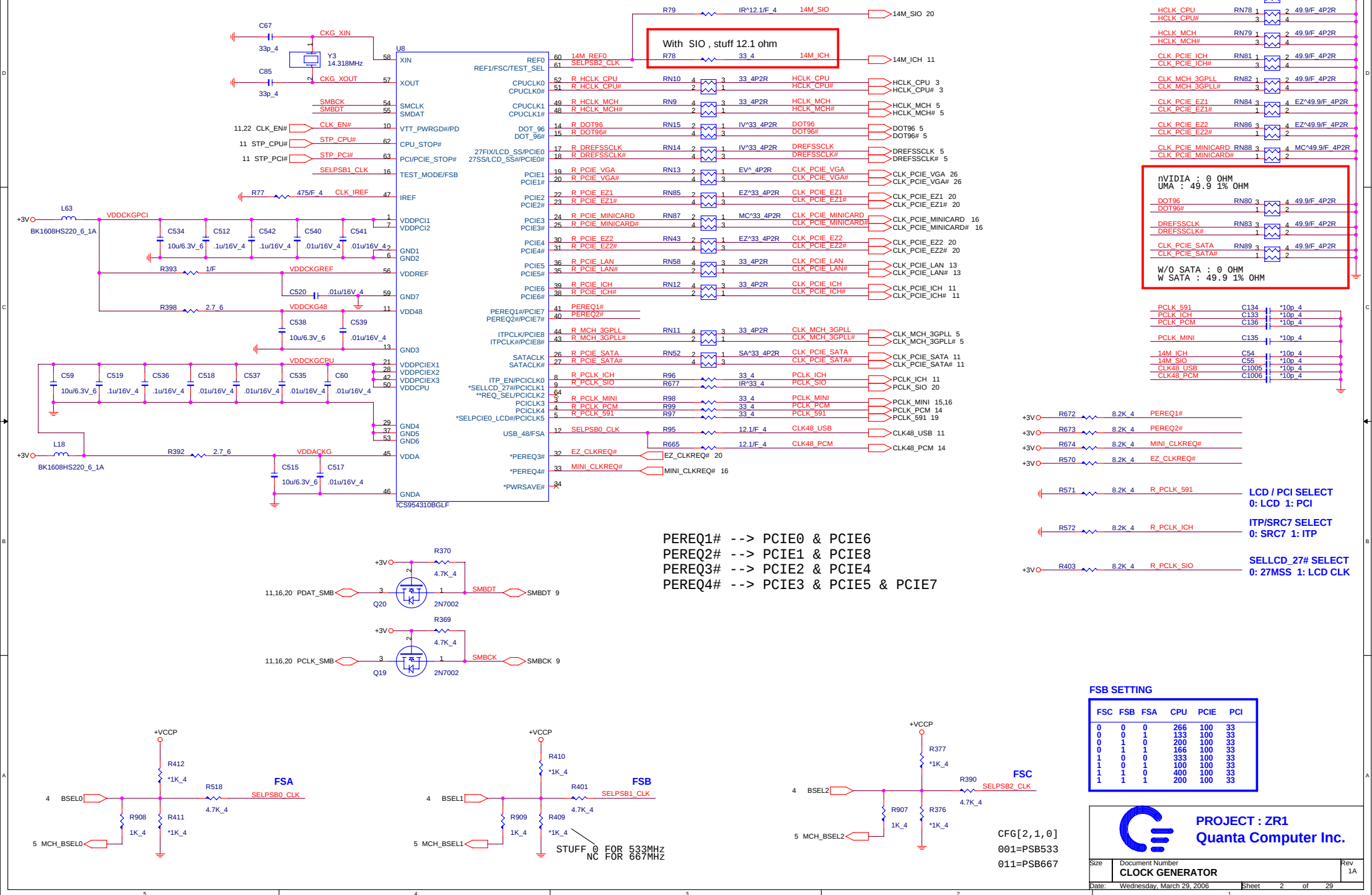
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ2# / GNT2#	AD19	INTC#, INTD#	MINI PCI
REQ0# / GNT0#	AD25	INTE#, INTF#, INTG#	TI XX12

MB PCB P/N DA0ZR1MB6A6 DC PCB P/N DA0ZR1PB6A7 DJ PCB P/N DA0ZR1AB6A5

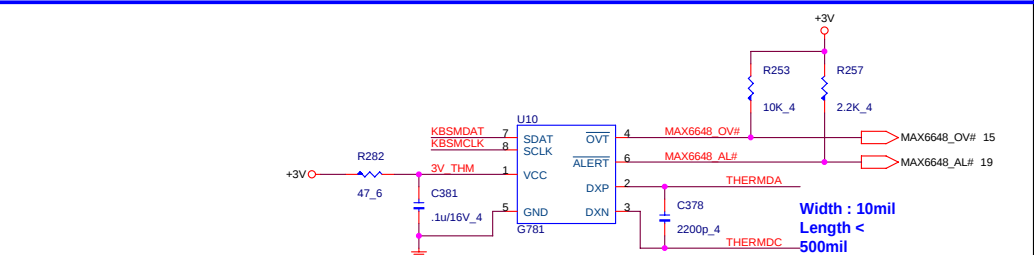
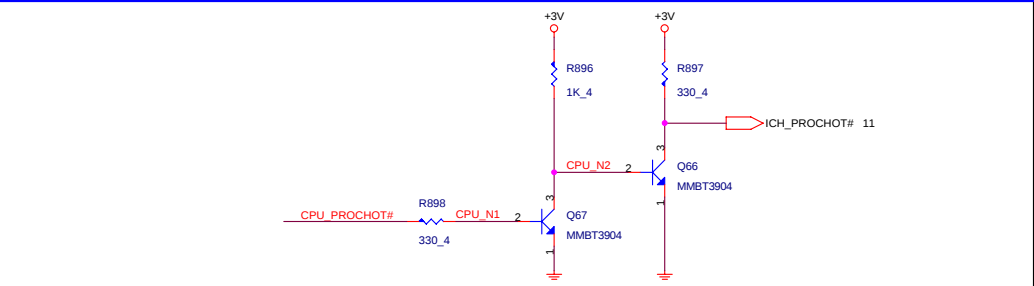
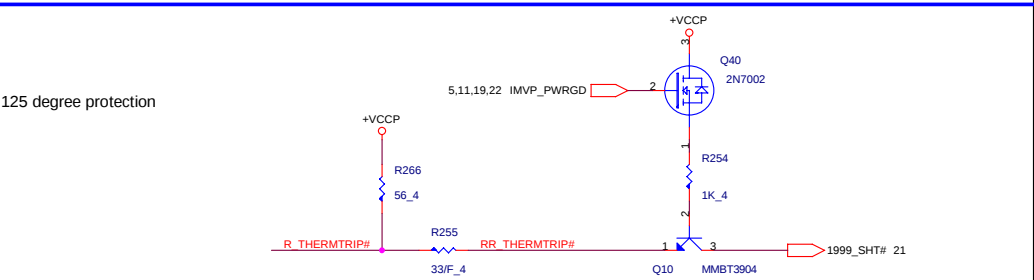
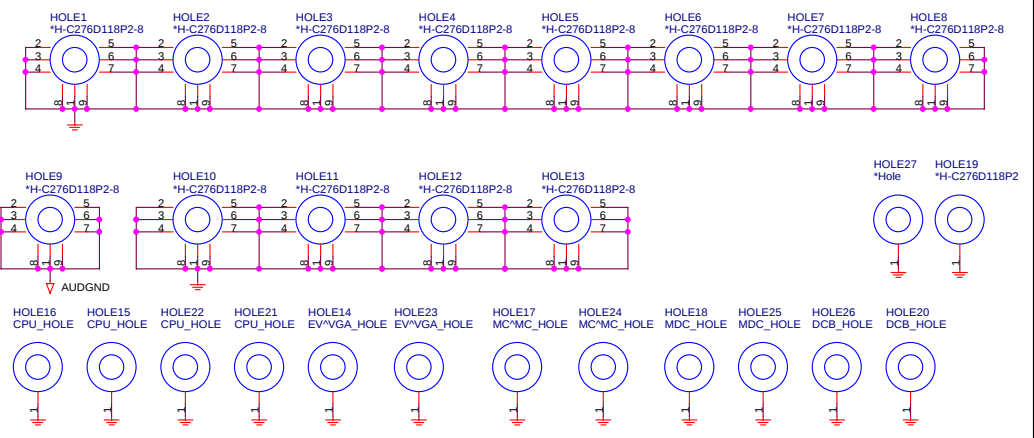
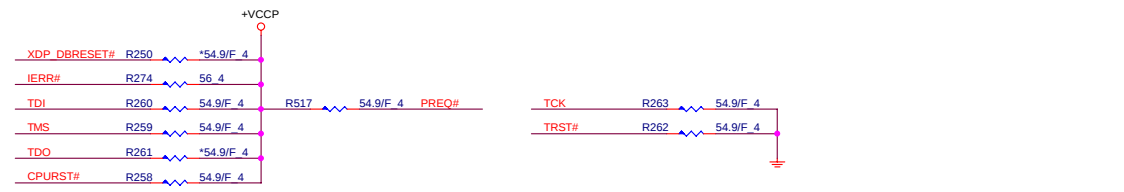
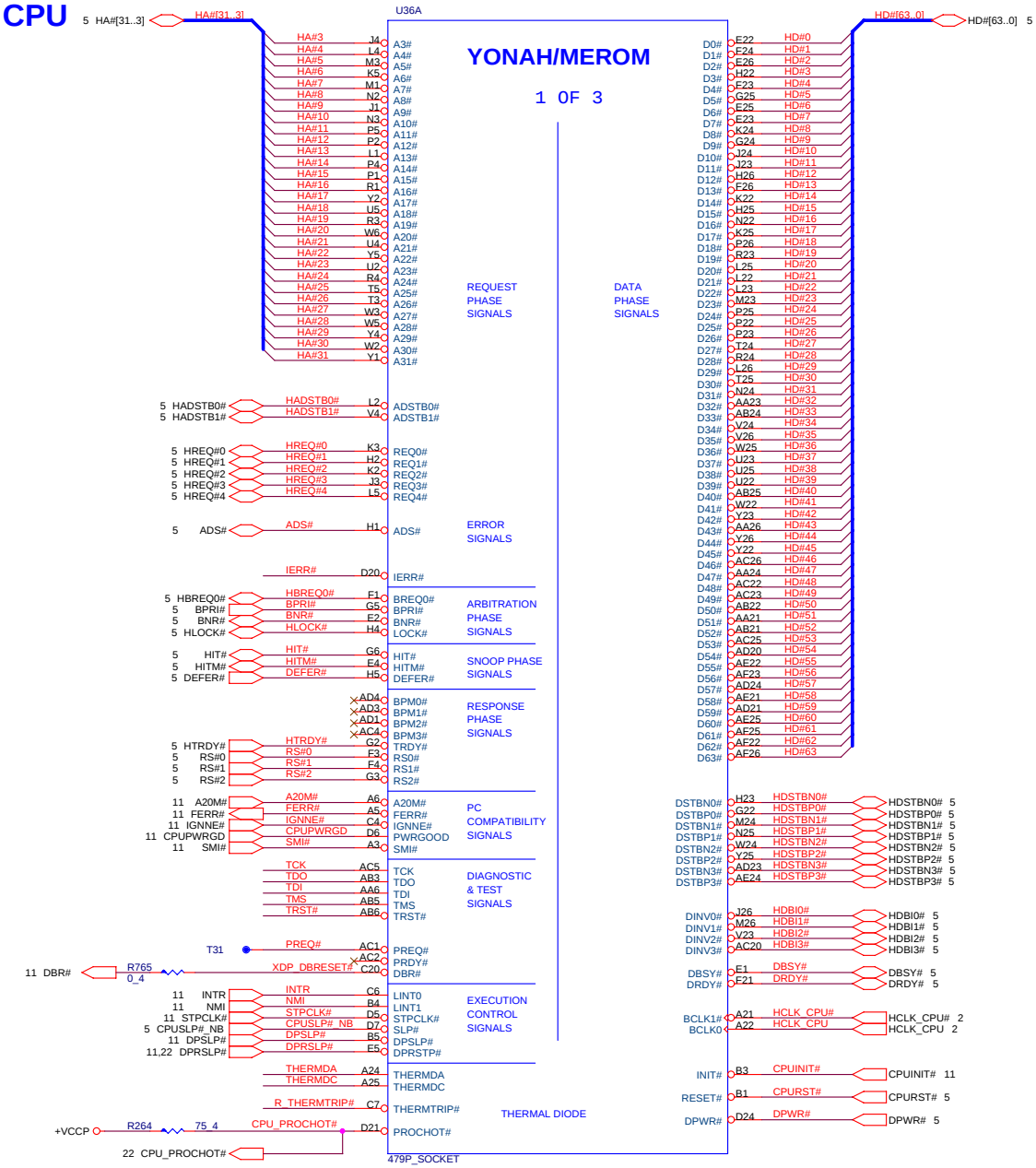

PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Wednesday, March 29, 2006	Sheet	1 of 29

CLOCK GENERATOR



CPU



MAXIM 6657 : AL006657020
GMT G781 : AL000781101



PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number CPU (HOST)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 3 of 29

CPU

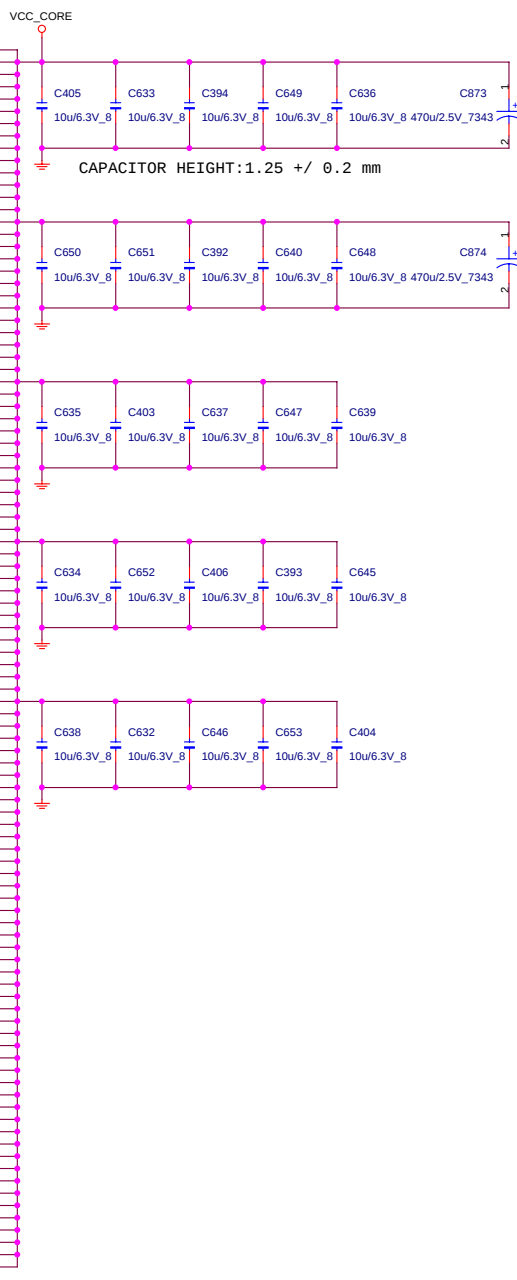
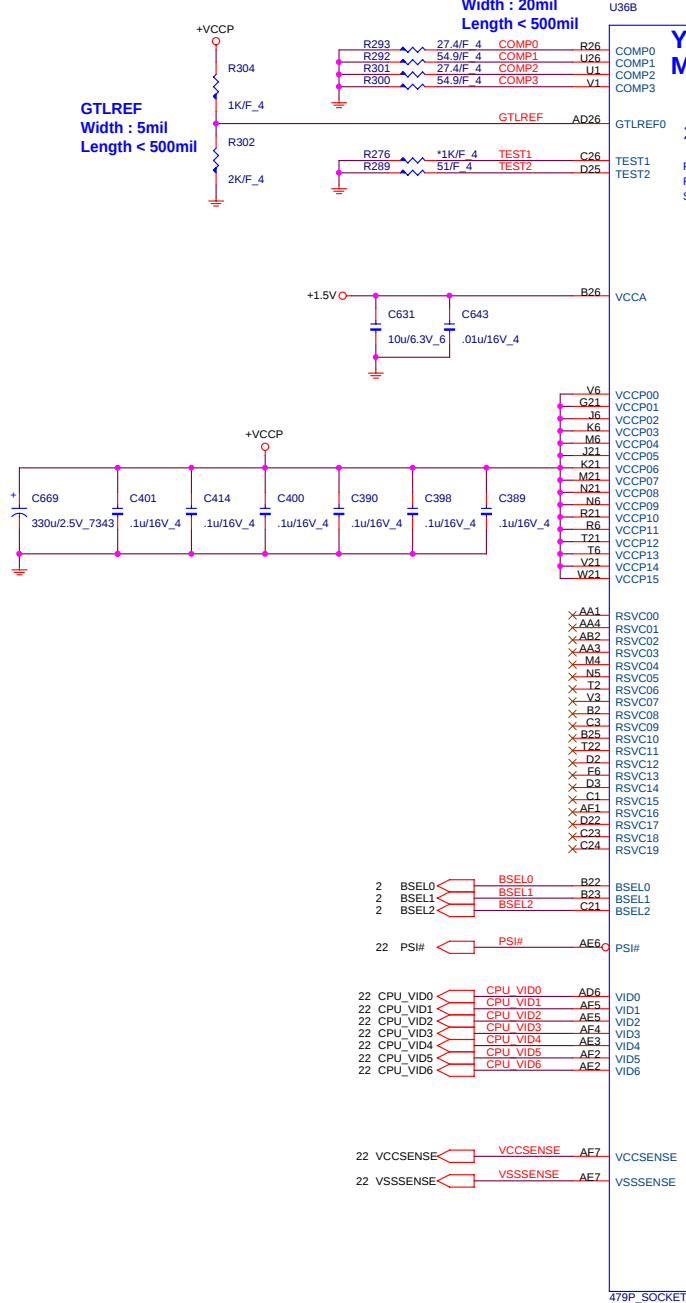
COMP0 - COMP3
Width : 20mil
Length < 500mil

YONAH /
MEROM

2 OF 3

POWER,
RESERVED
SIGNALS

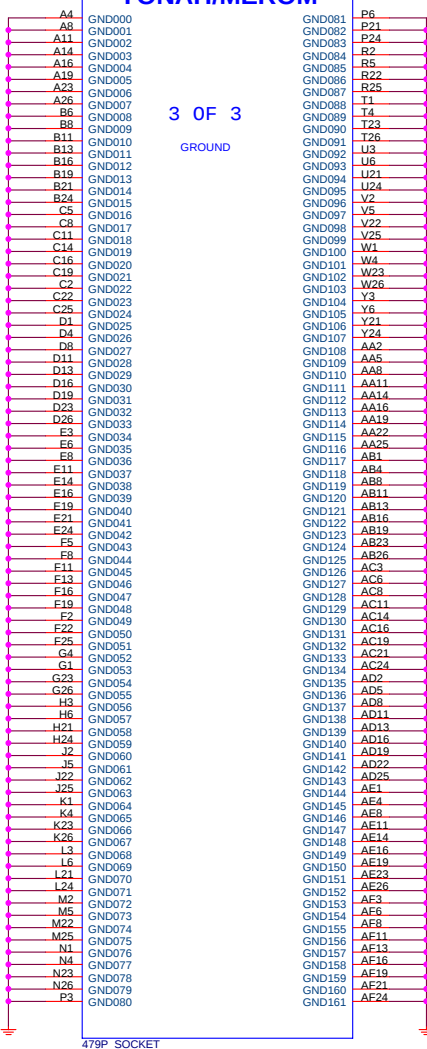
GTLREF
Width : 5mil
Length < 500mil



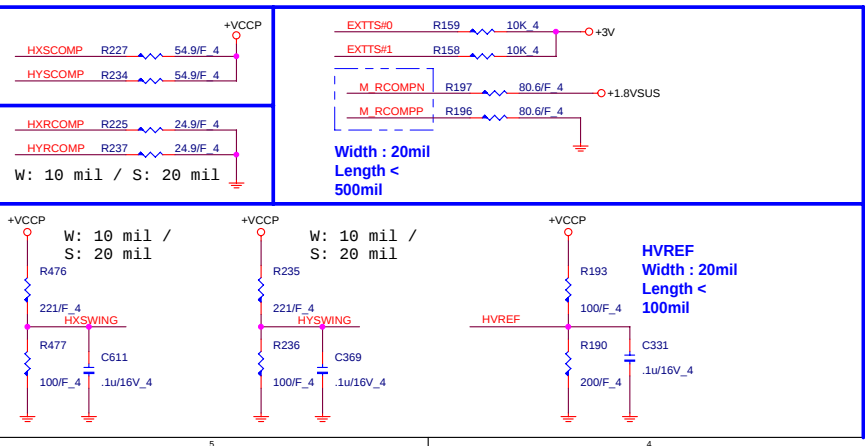
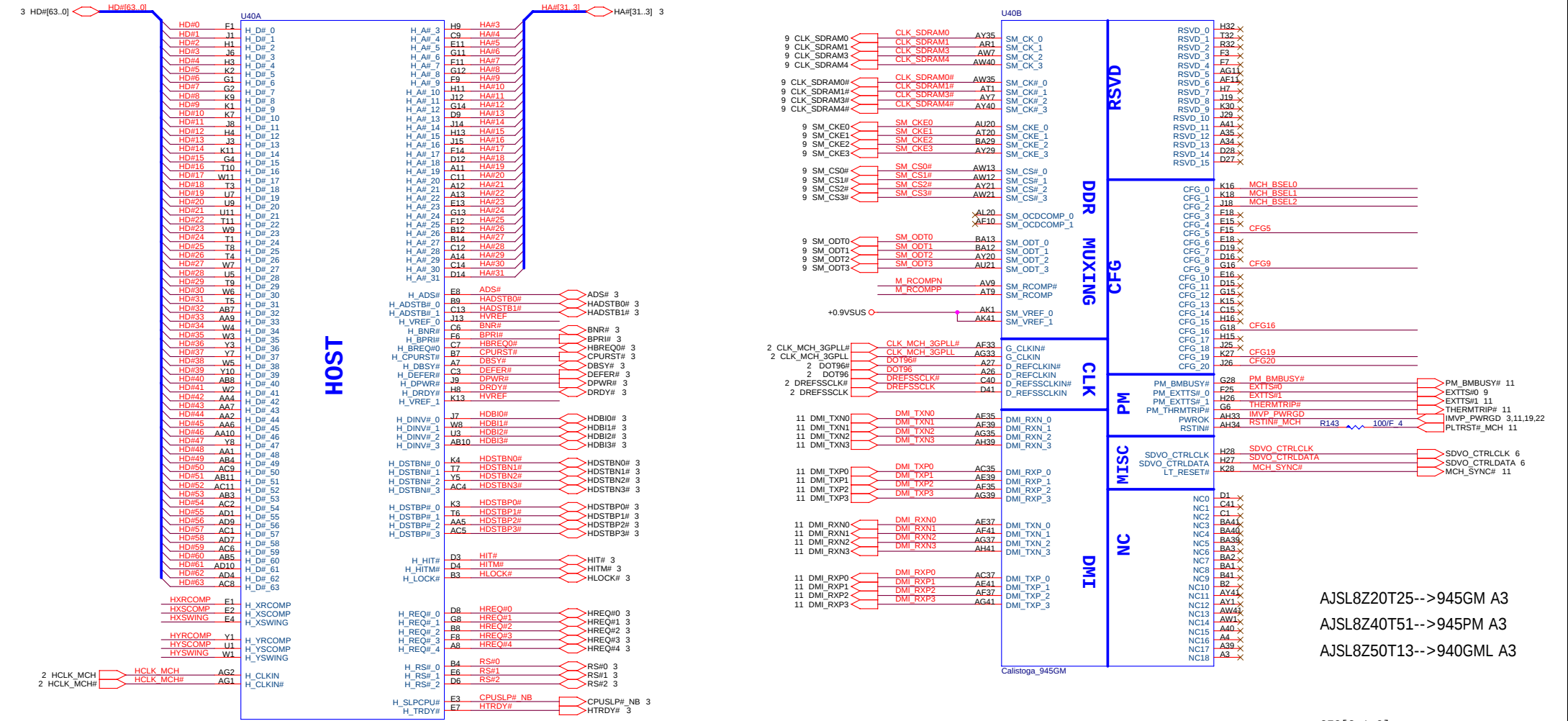
YONAH/MEROM

3 OF 3

GROUND

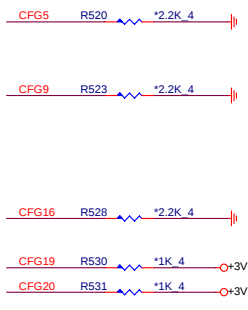


NB_945GM/PM/940GML



- 1.MCH_CFG_5 : Low = DMI X2, High=DMIX4
- 2.MCH_CFG_6 : Low = Moby Dick, High = Calistoga (Default)
- 3.MCH_CFG_7 : Low = RSVD, High = Mobile CPU
- 4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reverse lane ,High=Normal
- 5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- 6.MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- 7.MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled, High= Dynamic ODT Enabled.
- 8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- 9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- 10.MCH_CFG_20 PCIe Backward interoperability mode: Low= only SDVO or PCIe x1 is operational (defaults) , High=SDVO and PCIe x1 are operation simultaneously via the PEG port.

GMCH Strap pin

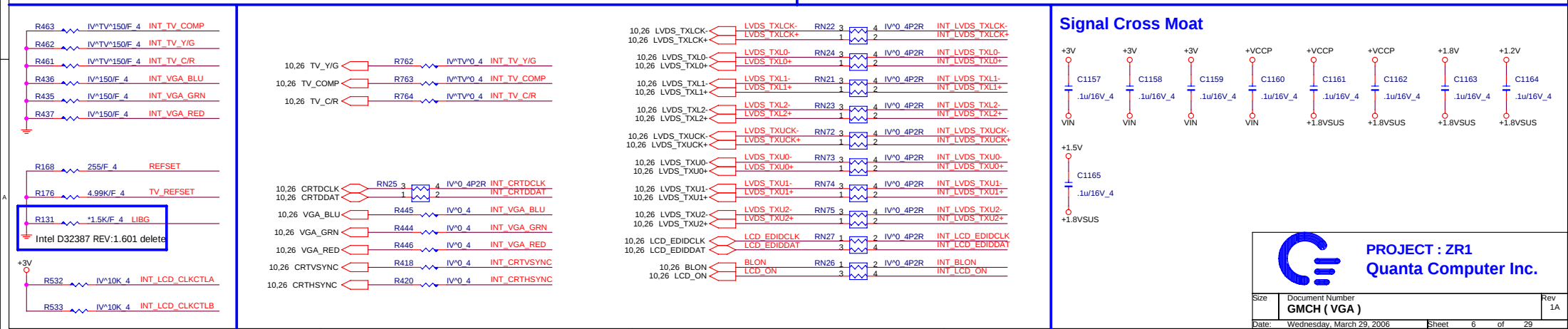
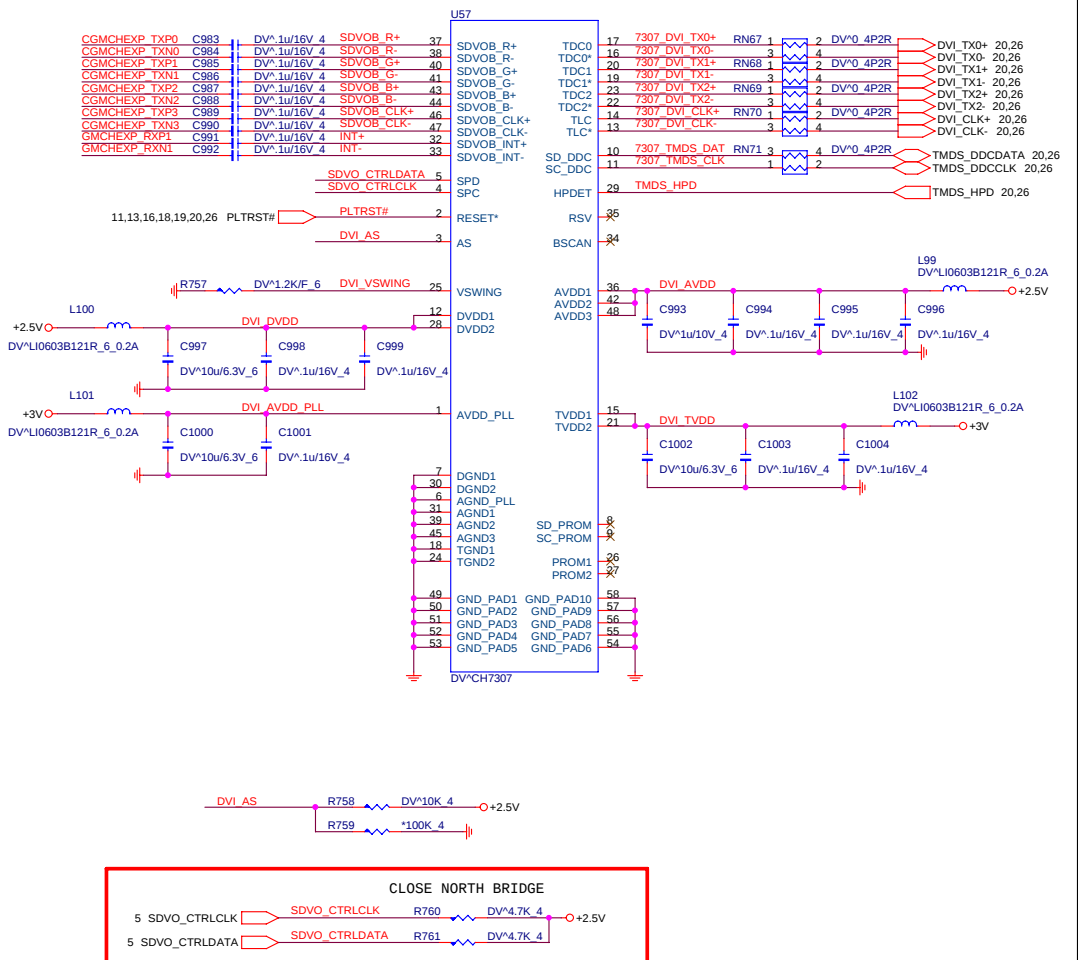
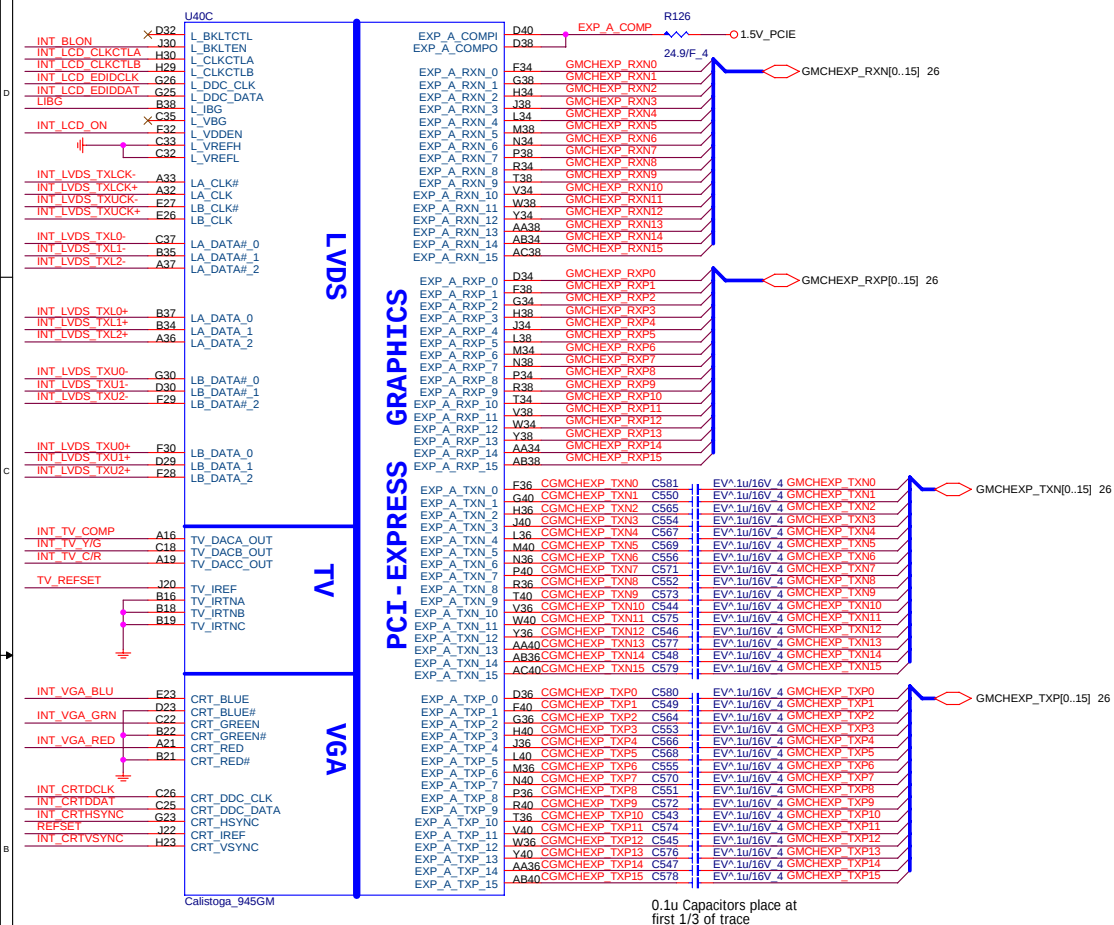


AJSL8Z20T25-->945GM A3
AJSL8Z40T51-->945PM A3
AJSL8Z50T13-->940GML A3

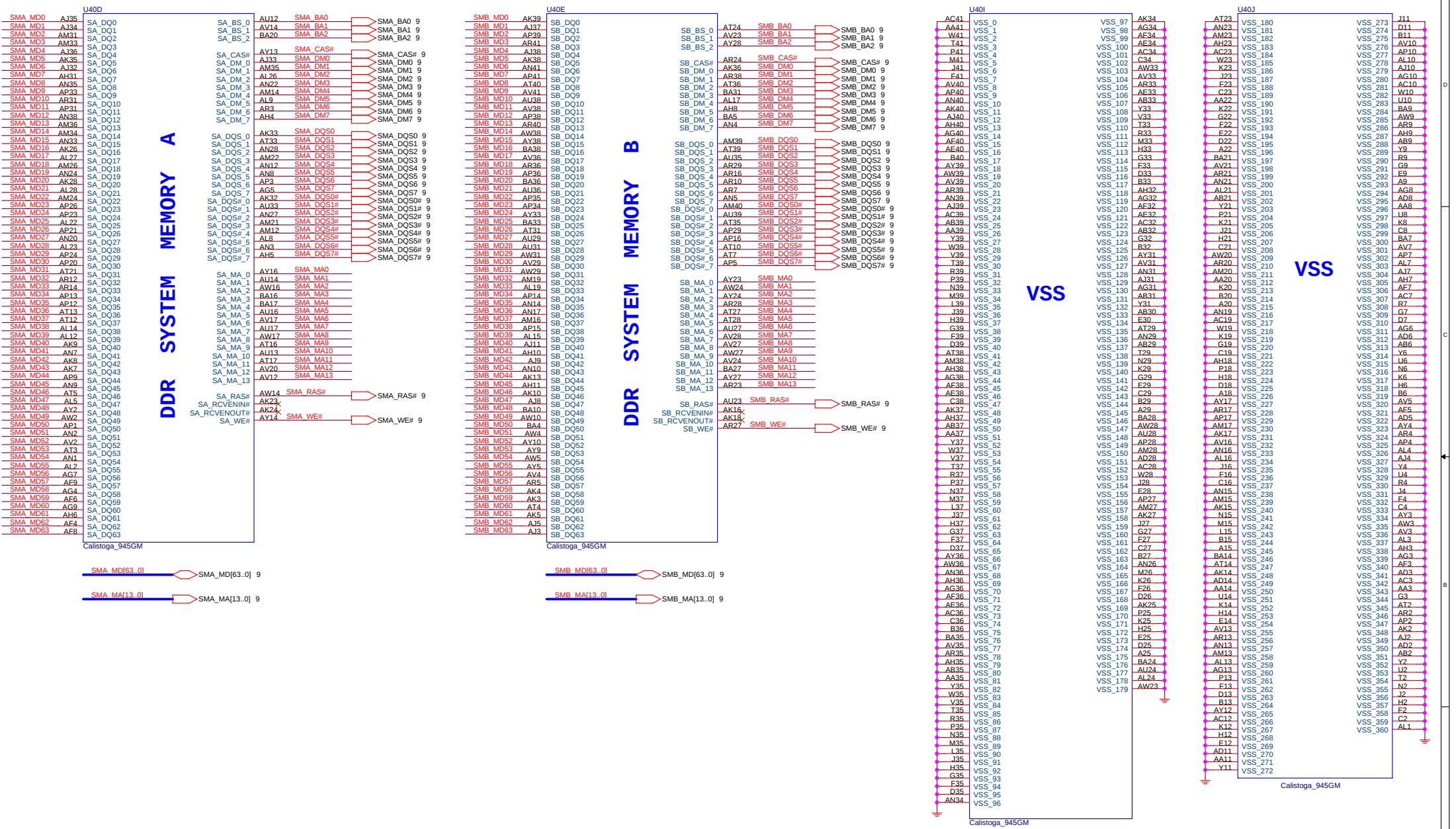
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (HOST / DMI)	1A
Date:	Wednesday, March 29, 2006	Sheet 5 of 29

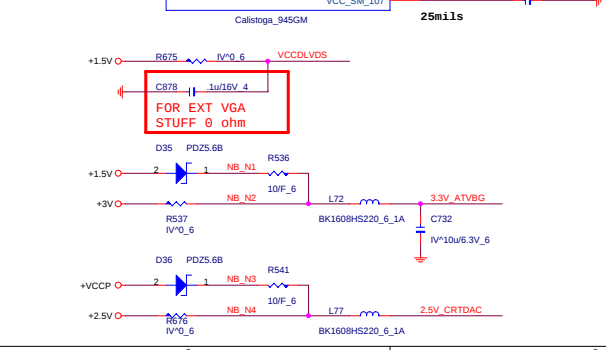
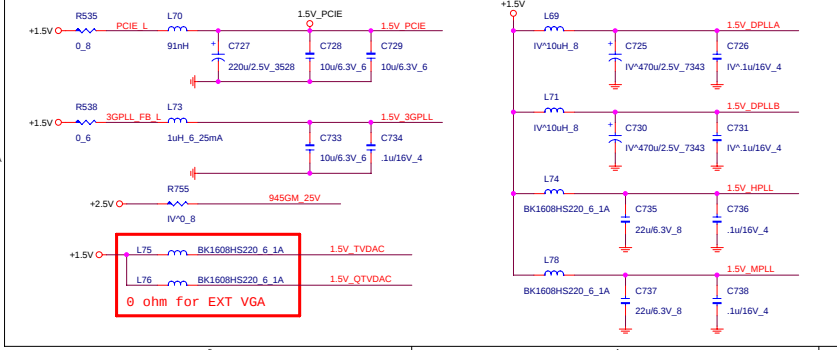
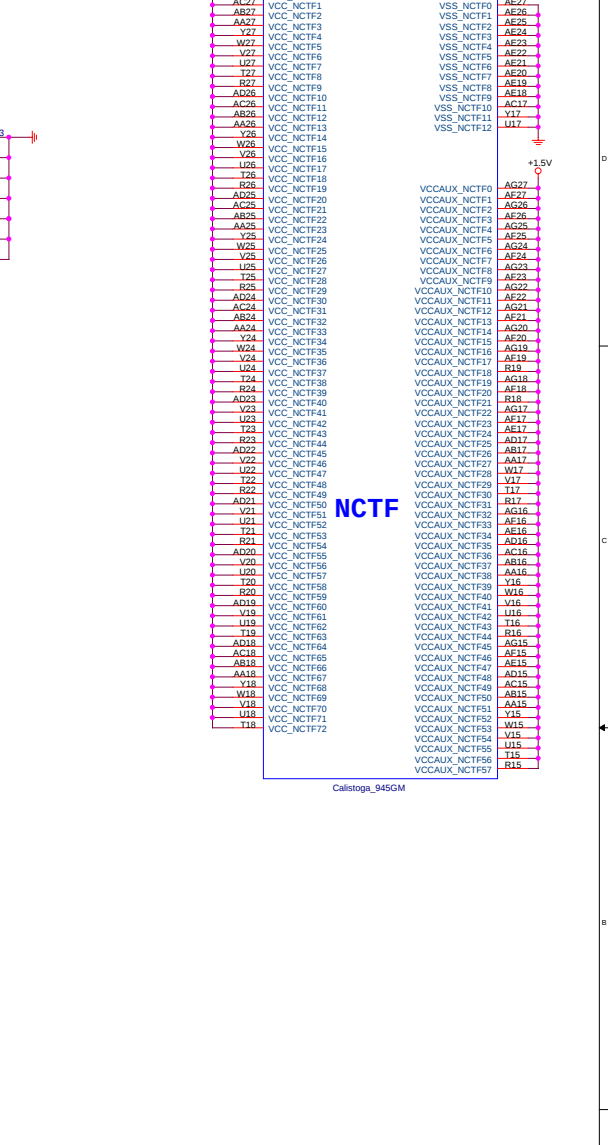
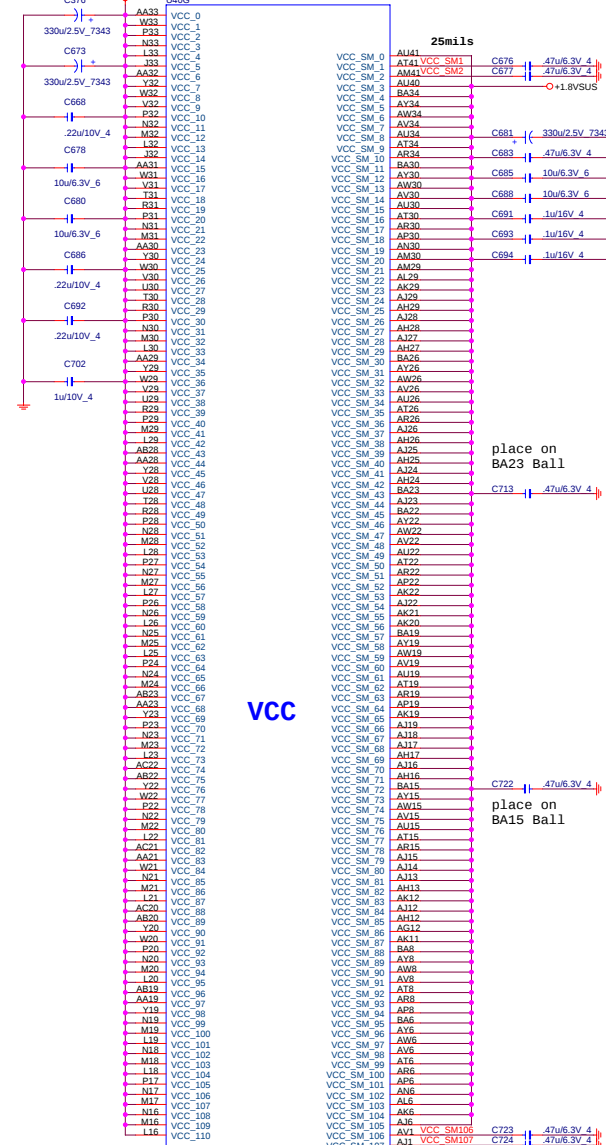
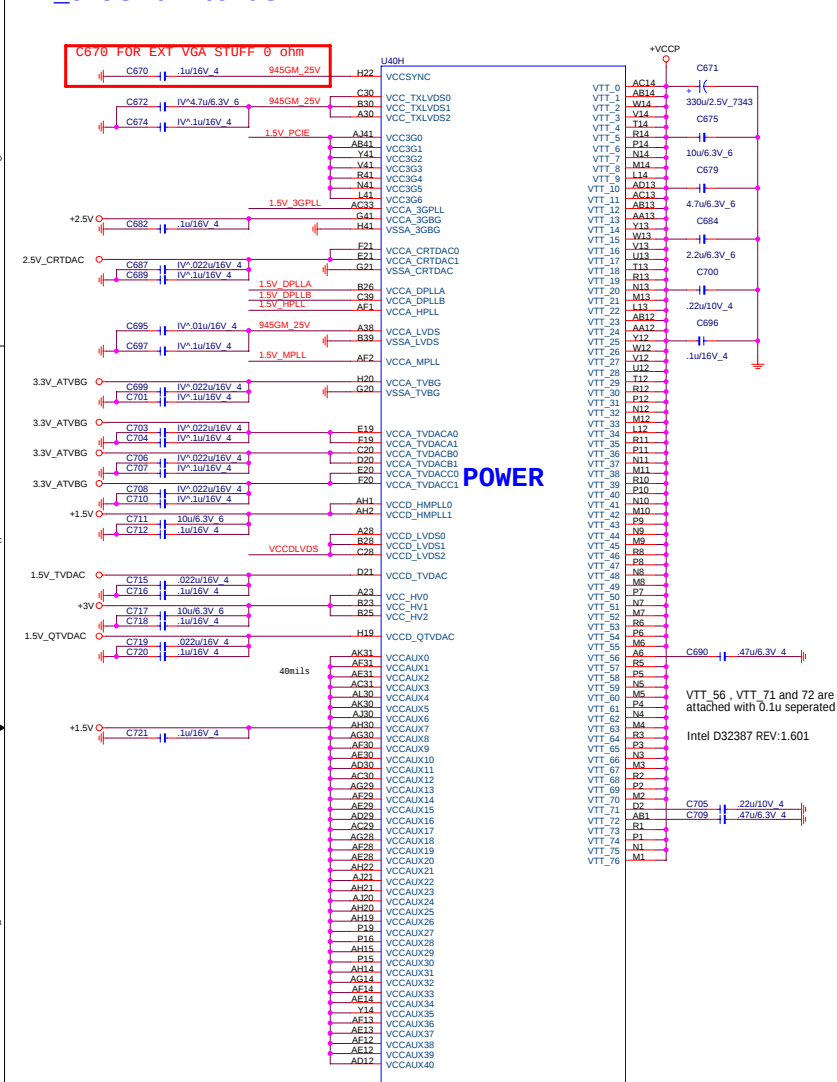
NB_945GM/PM/940GML



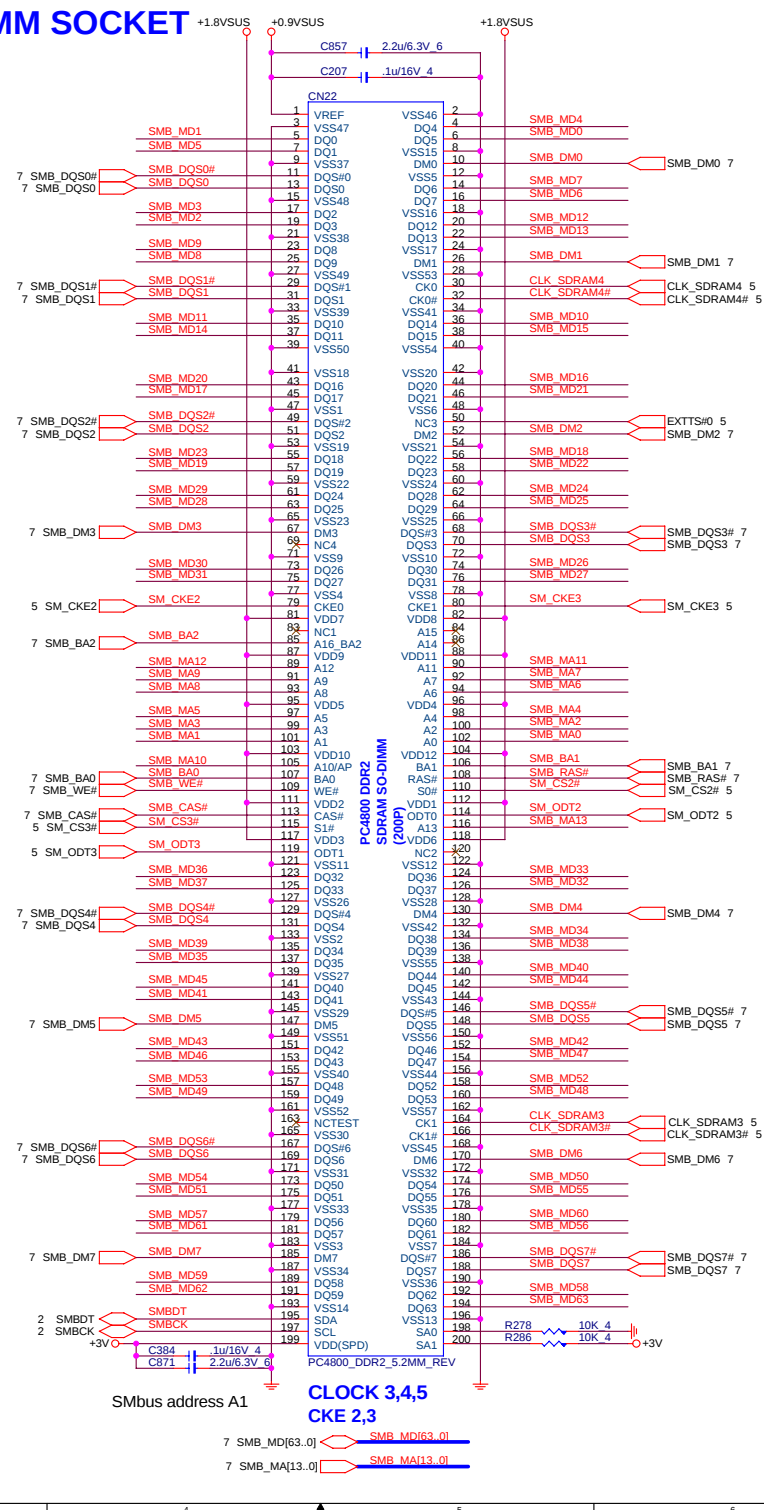
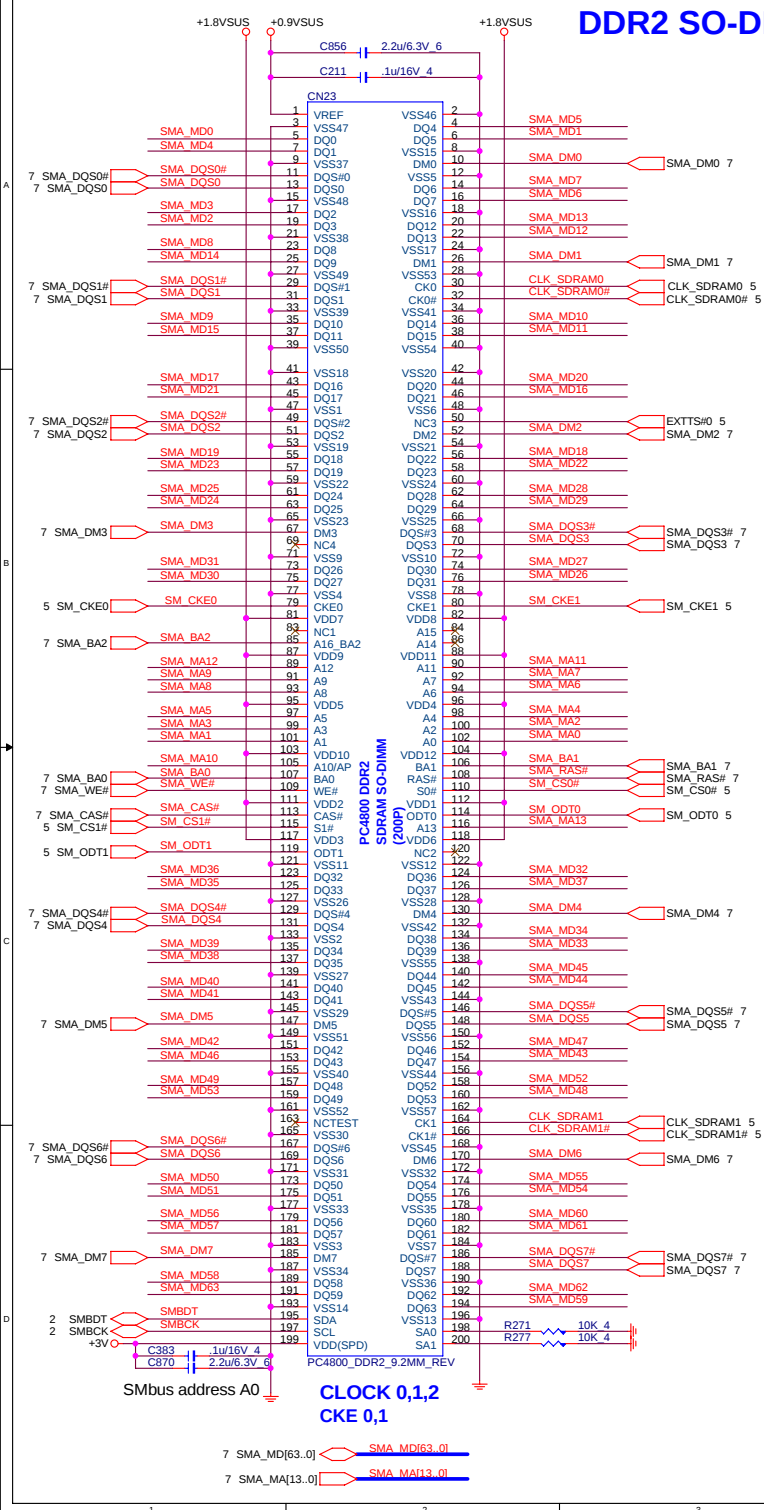
NB_945GM/PM/940GML



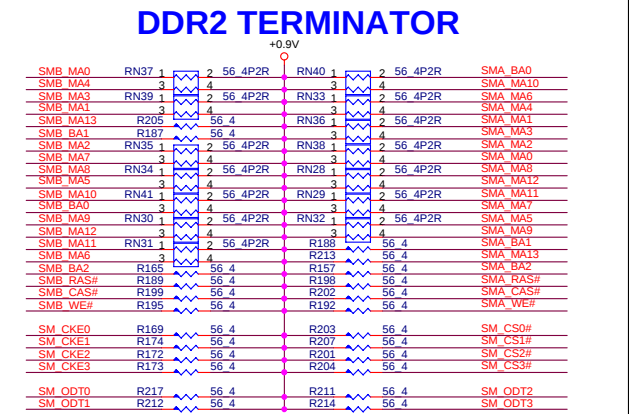
NB 945GM/PM/940GML



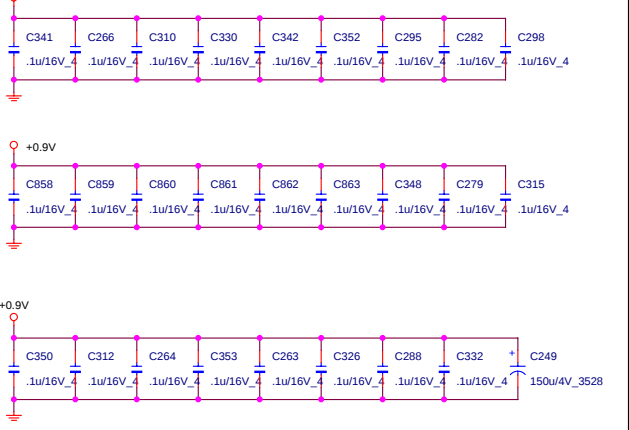
DDR2 SO-DIMM SOCKET



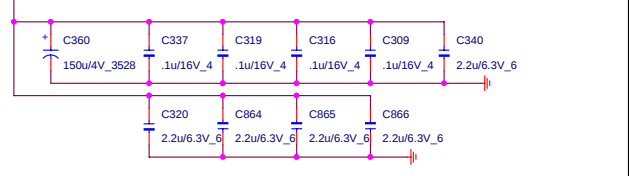
DDR2 TERMINATOR



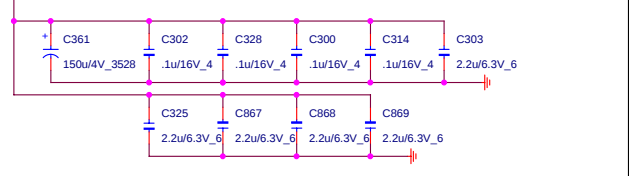
TERMINATOR DECOUPLING CAPACITOR



CLOSE SO-DIMM SOCKET CAPACITORS



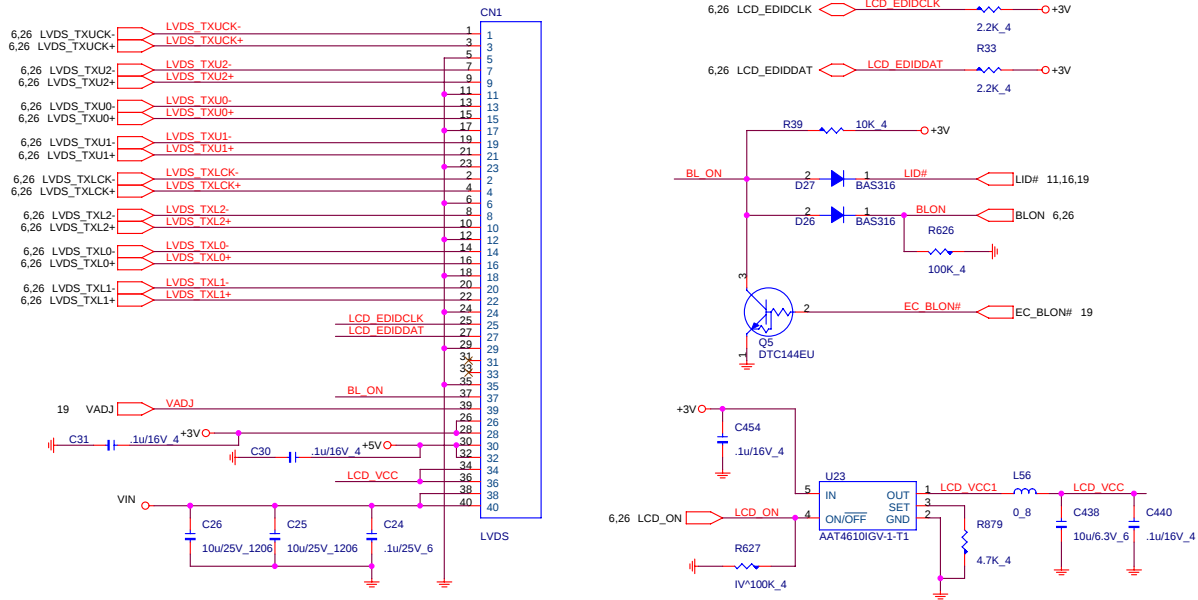
CLOSE SO-DIMM SOCKET CAPACITORS



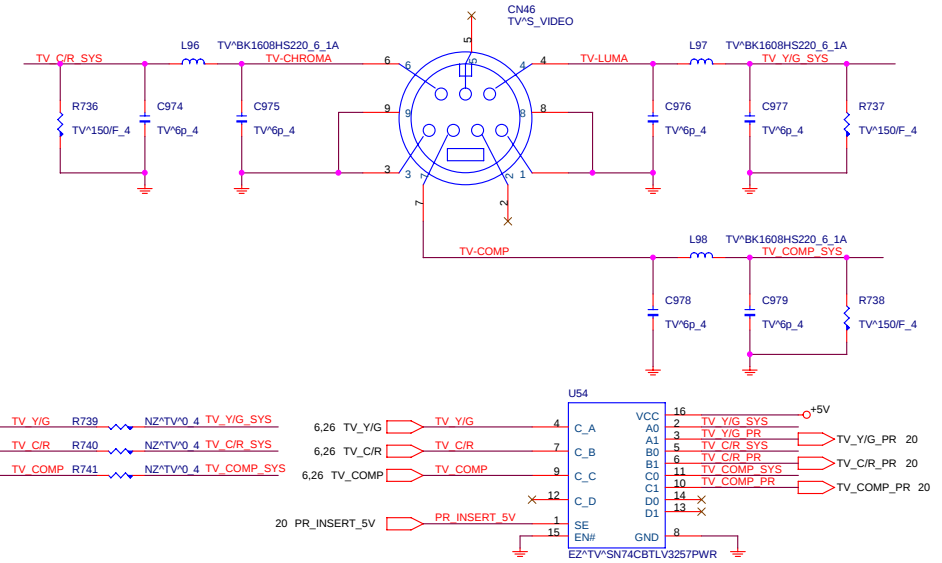
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	DDR SO-DIMM(200P)	1A
Date:	Wednesday, March 29, 2006	Sheet 9 of 29

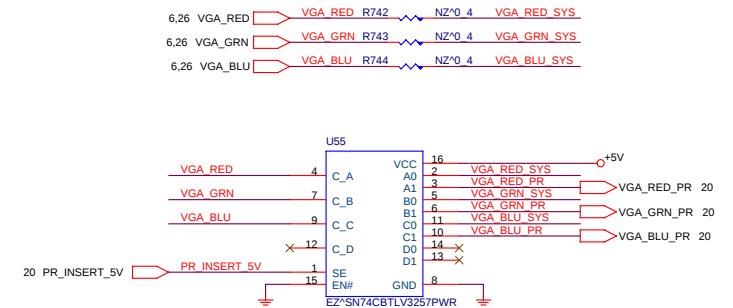
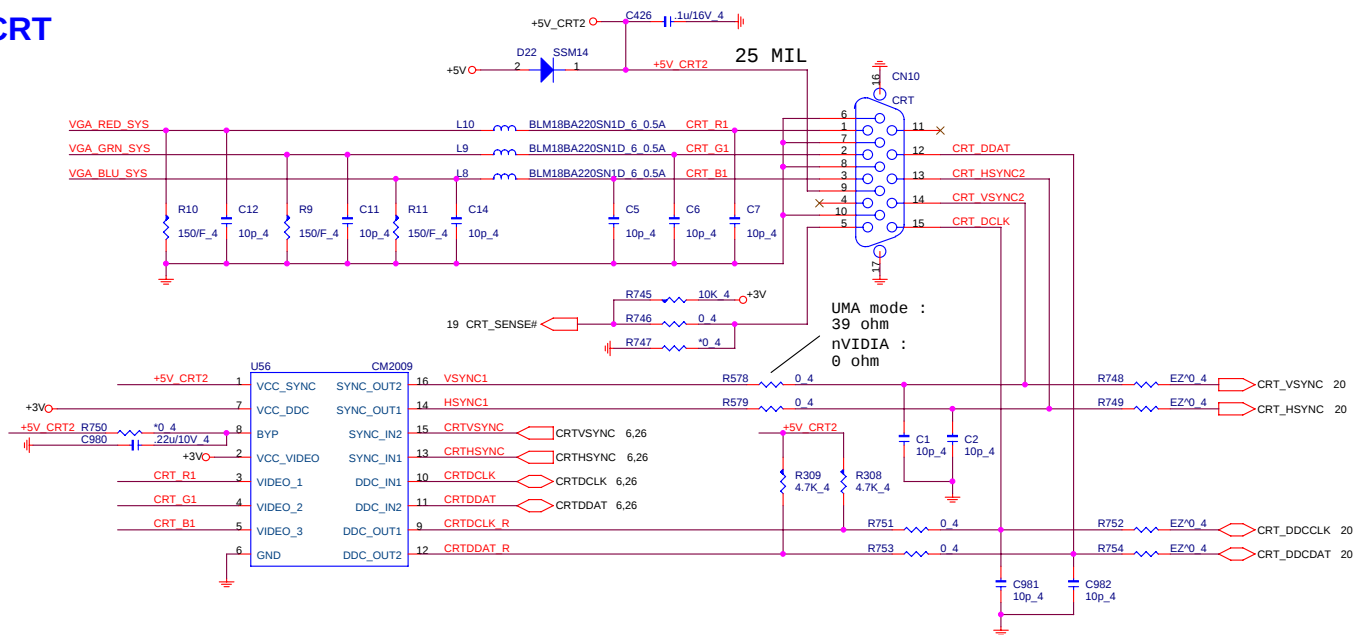
LVDS



S-VIDEO

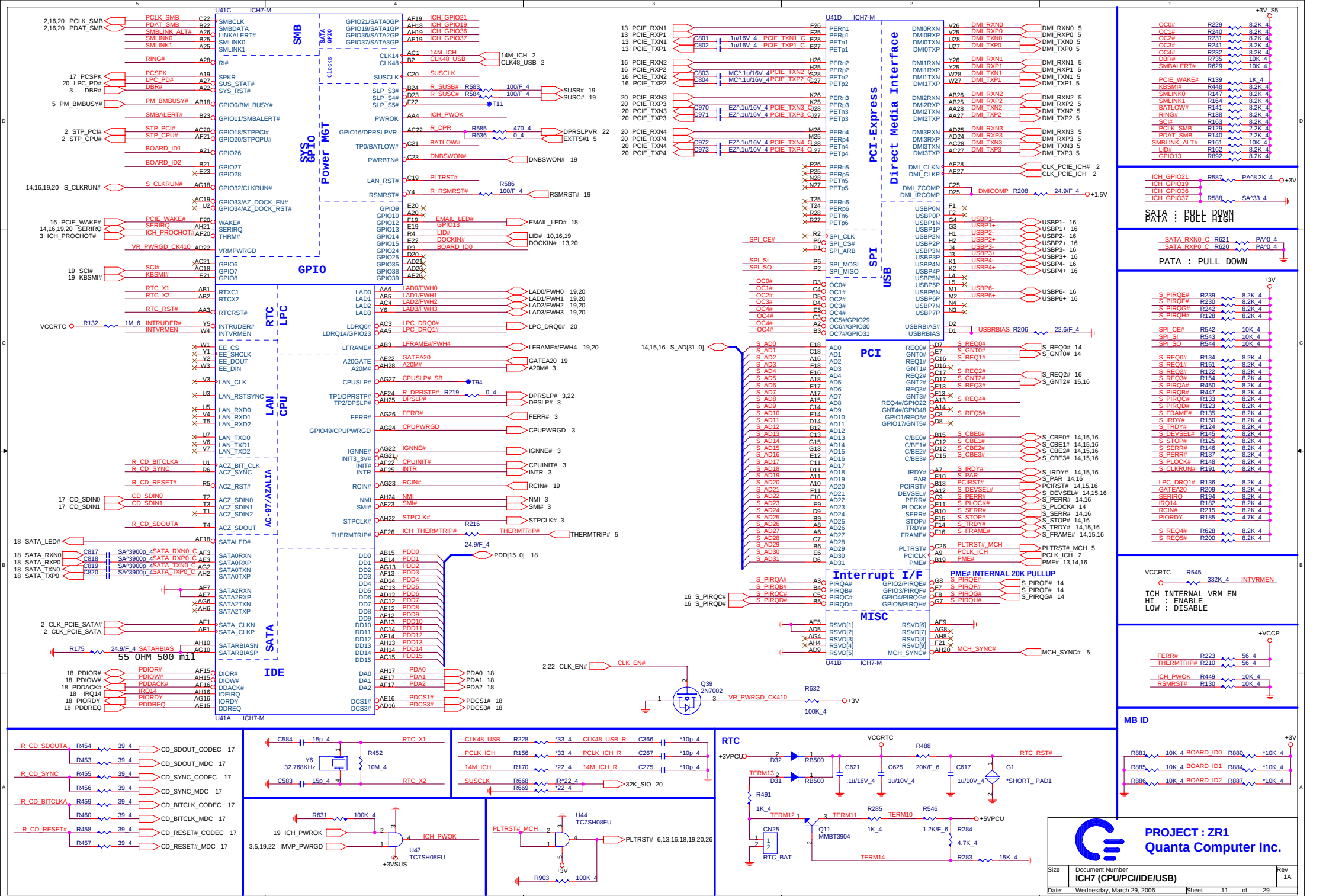


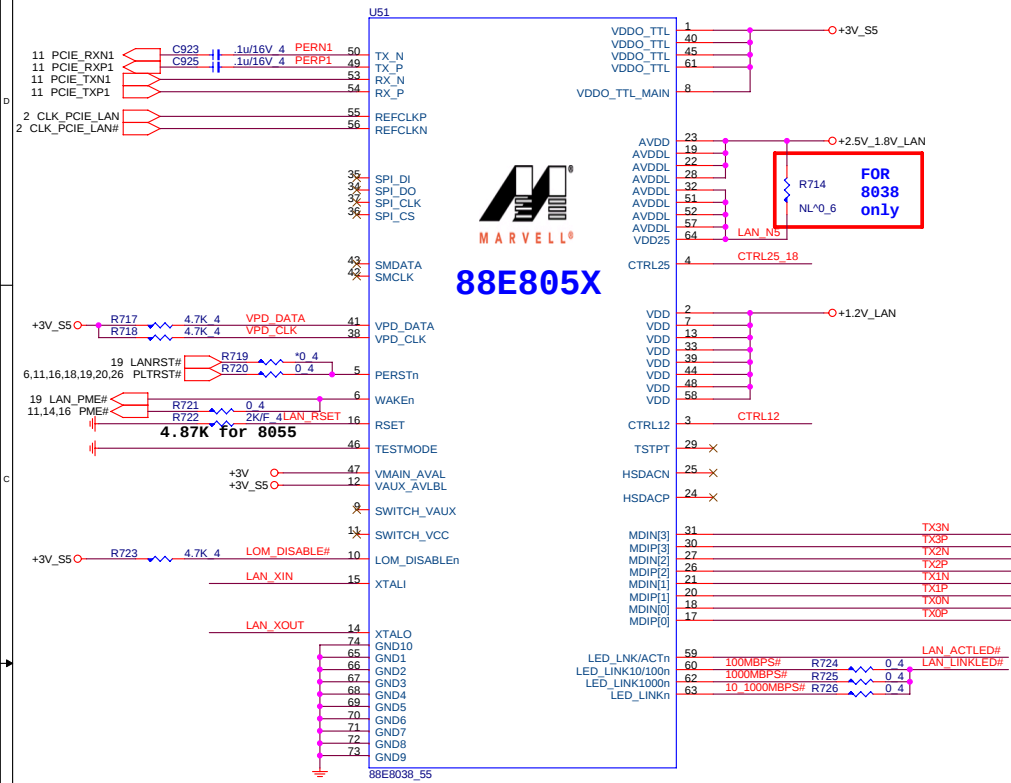
CRT



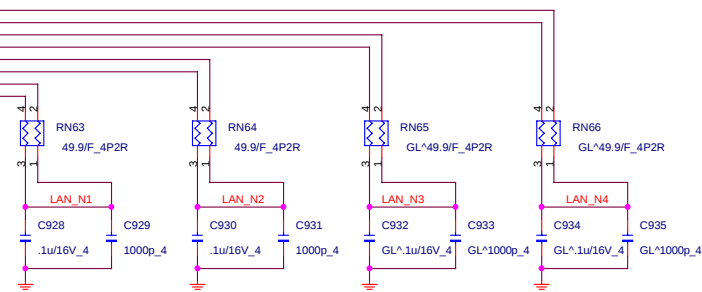
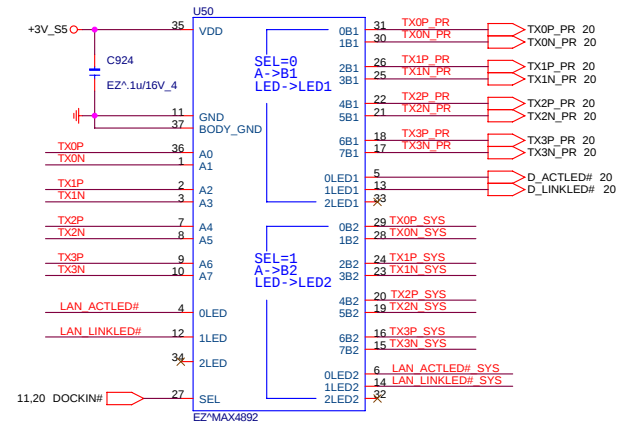
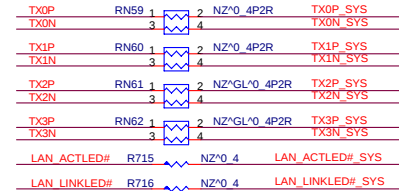
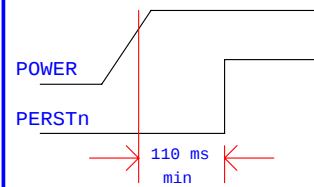
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number LCD / CRT / TV	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 10 of 29

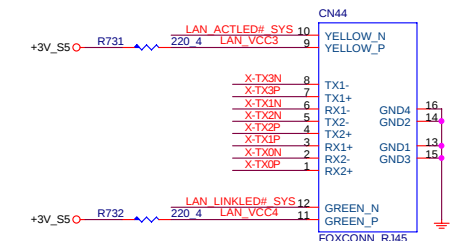
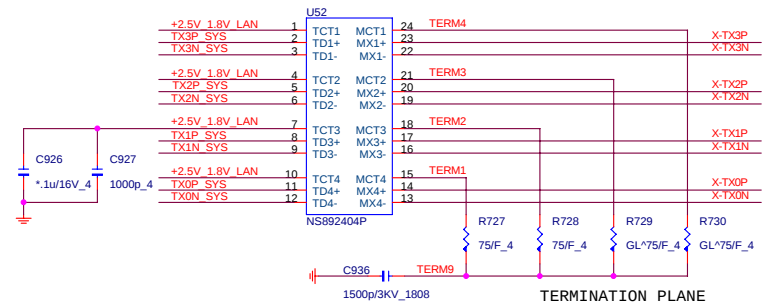
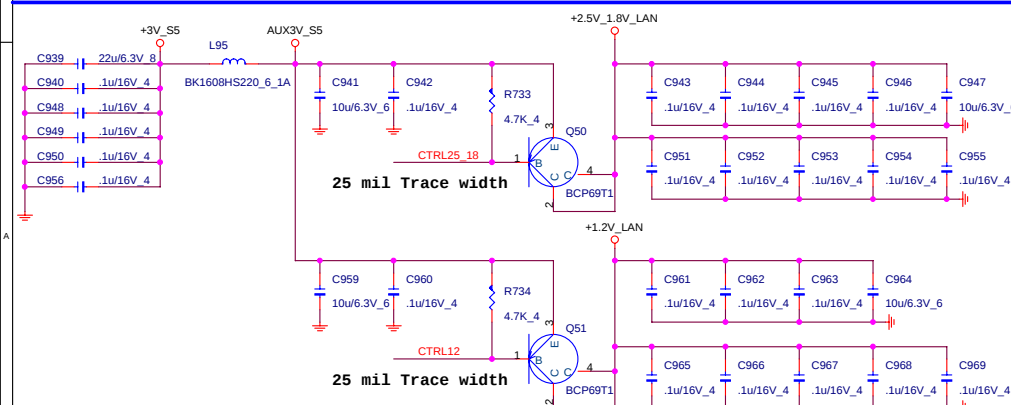
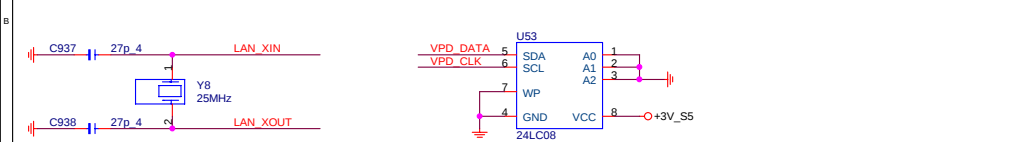




RESET TIMING



	BOTHHAND	FCE
10/100	DB0KN7LAN24	DBED2LLAN05
GiGa	DBKN1NLAN03	DB0ZH1LAN06



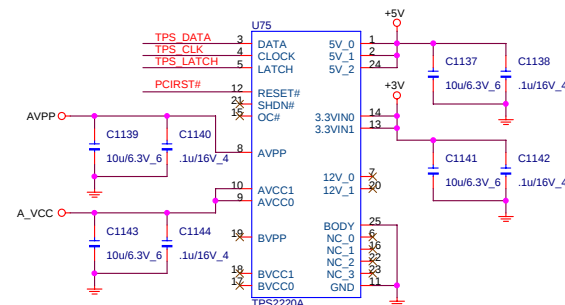
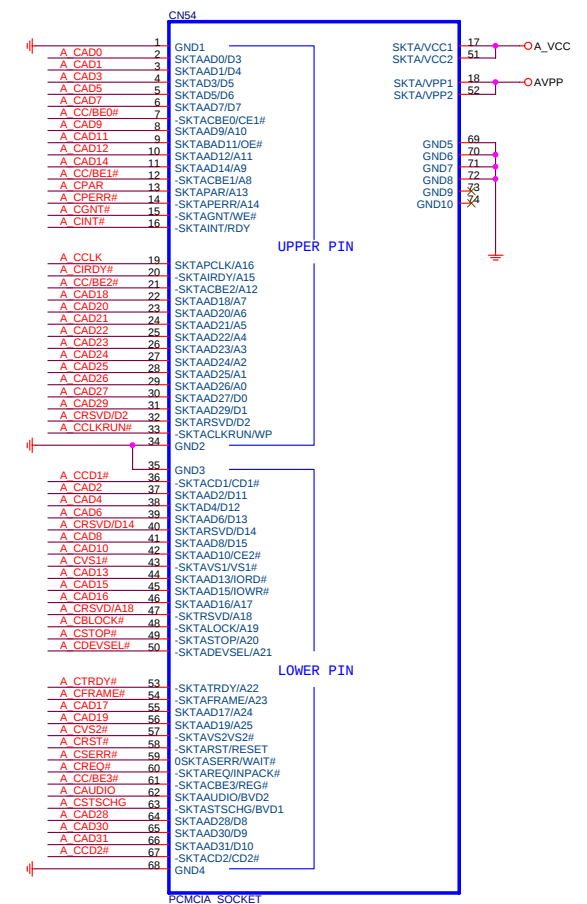
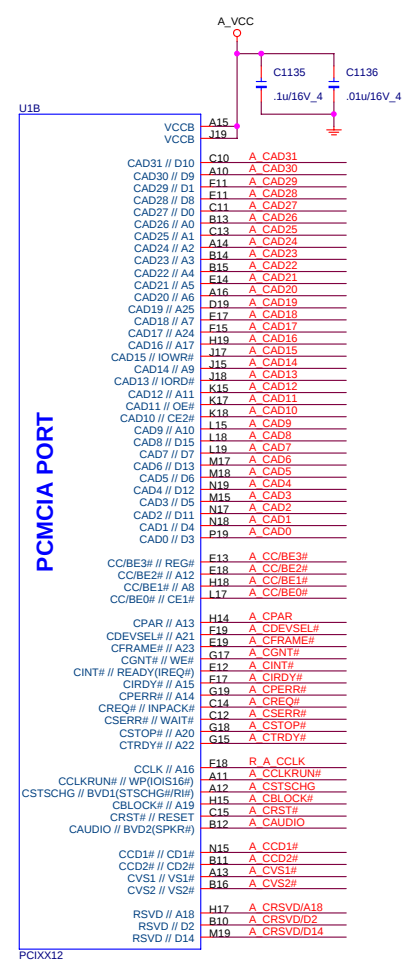
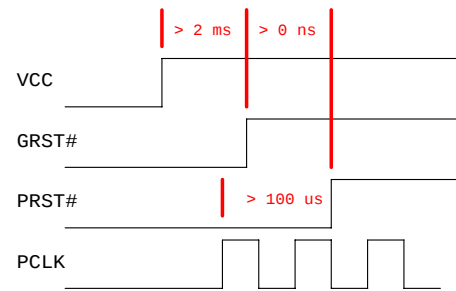
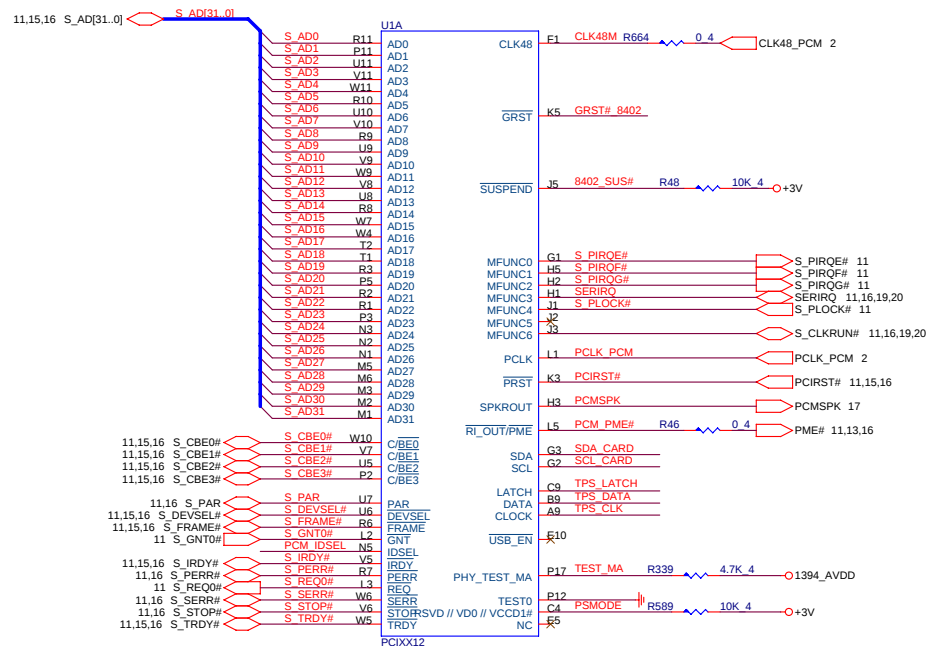
PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number LAN (MARVELL 8038/8055)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 13 of 29

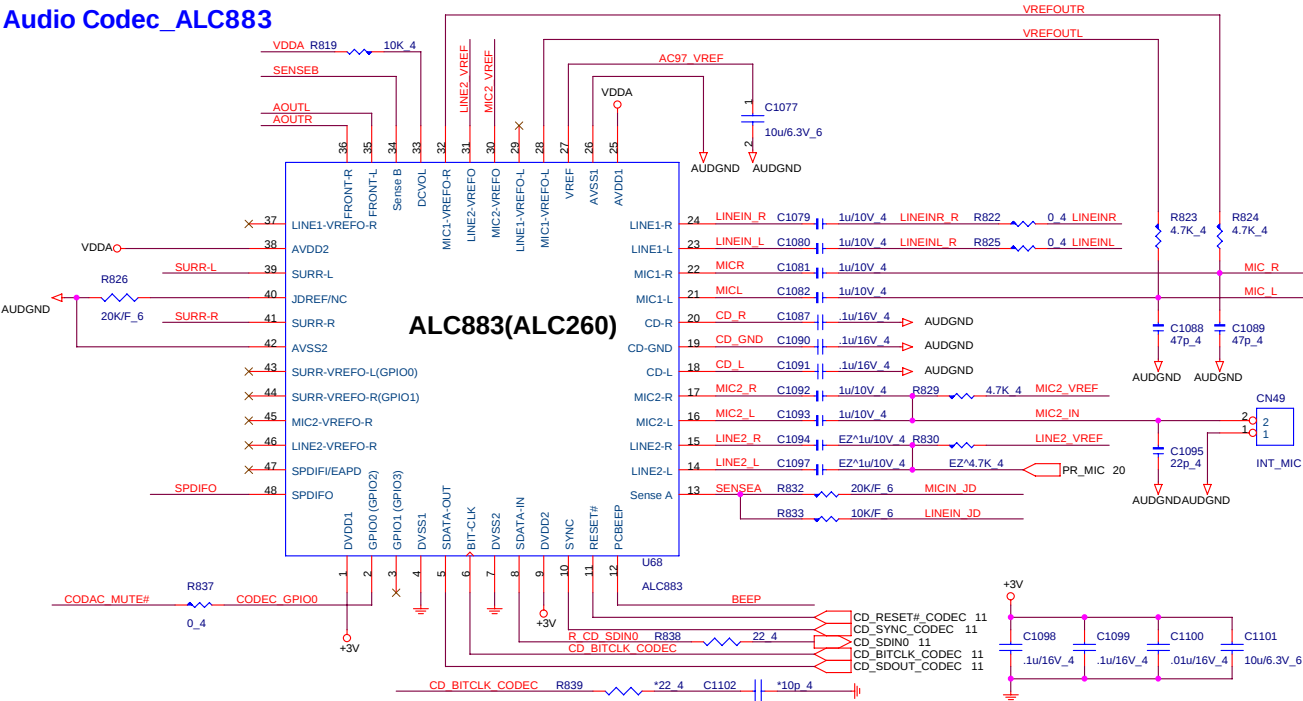
REQ0# AD25
GNT0# PIRQ(E,F,G)#

S_AD25 R346 150/F 4 PCM_IDSEL

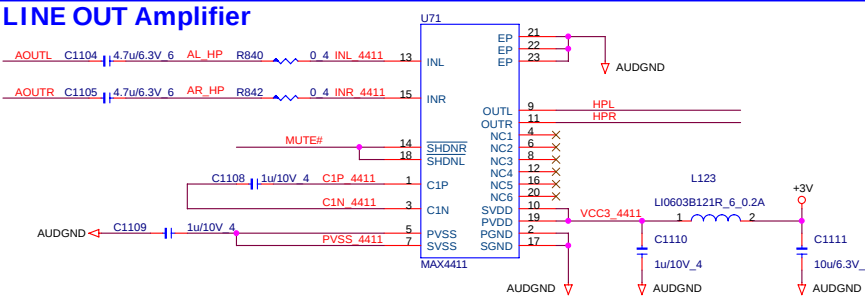
PCI1512 : AJ015120T02 PCMCIA



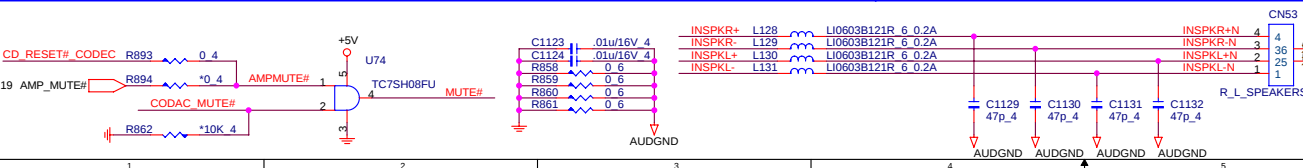
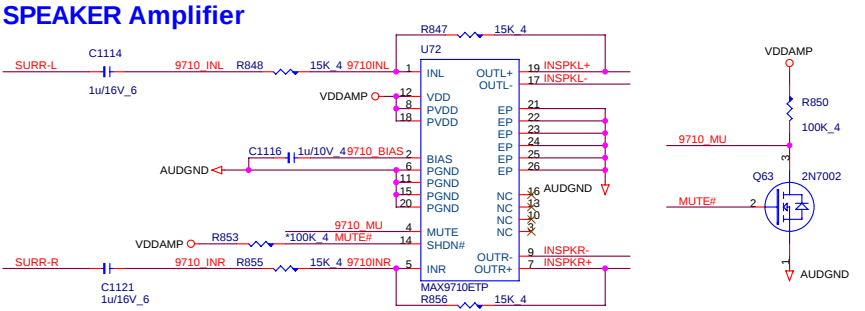
Audio Codec_ALC883



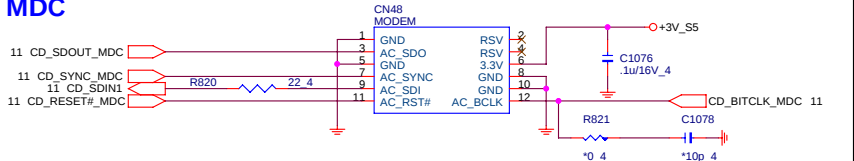
LINE OUT Amplifier



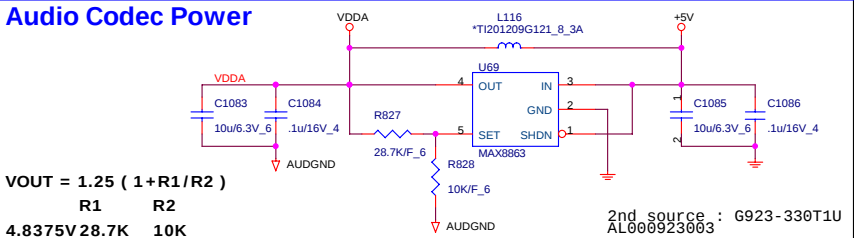
SPEAKER Amplifier



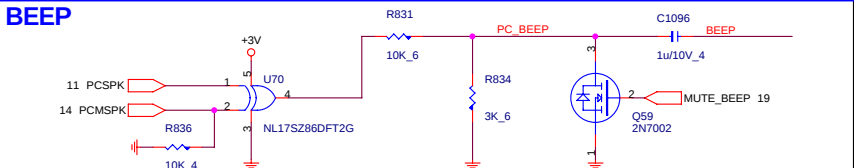
MDC



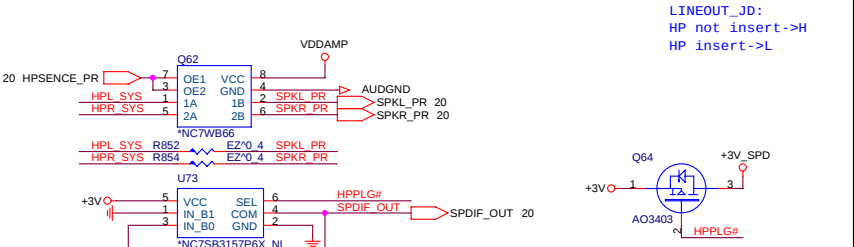
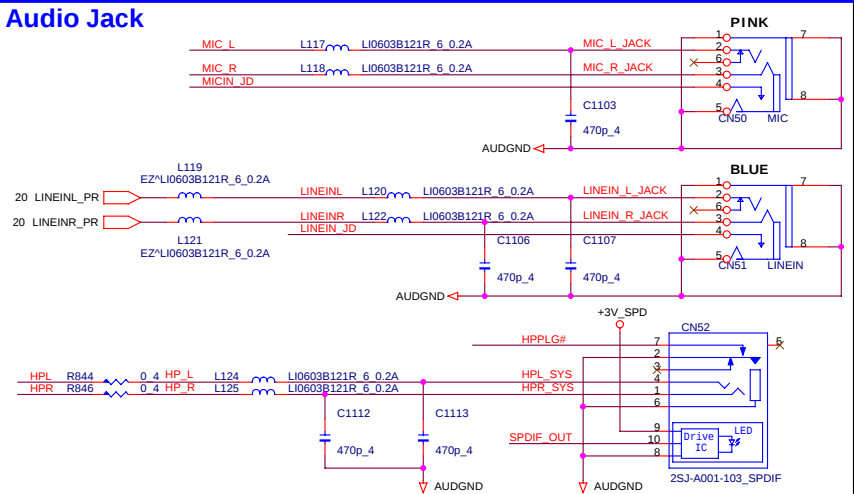
Audio Codec Power



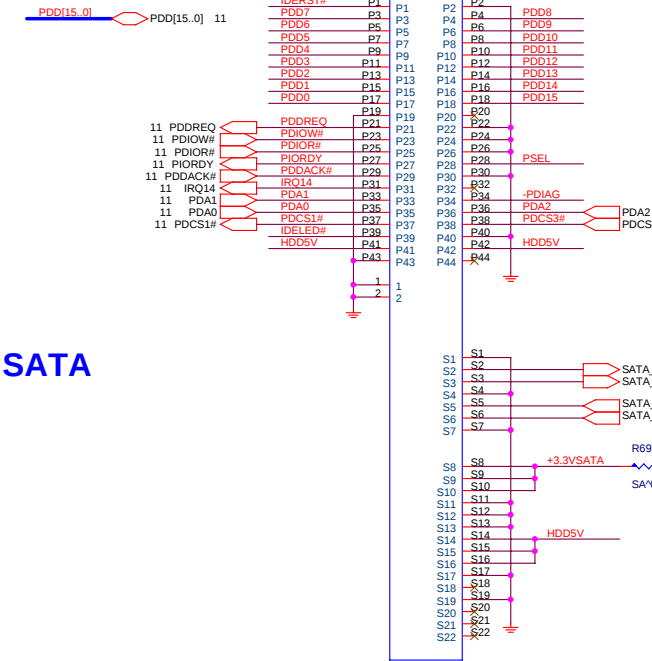
BEEP



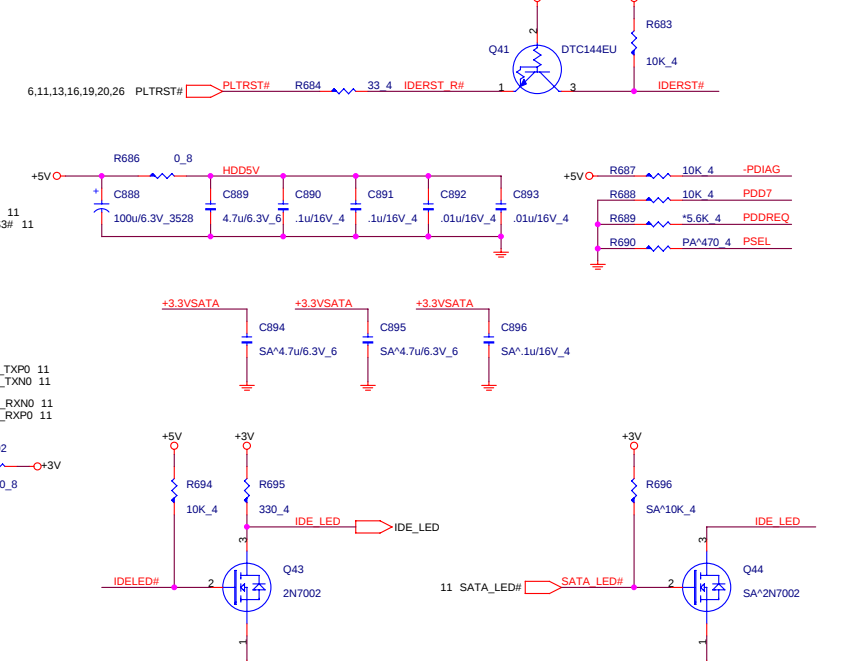
Audio Jack



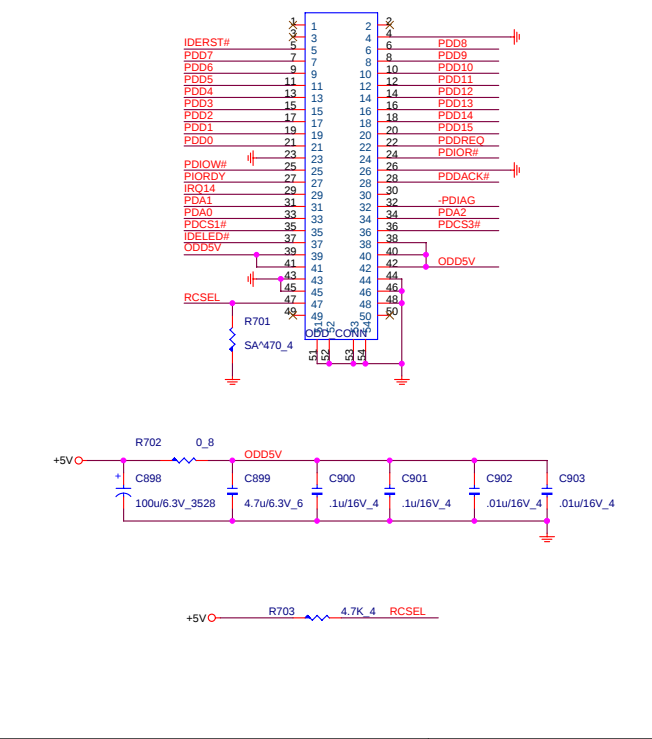
HDD



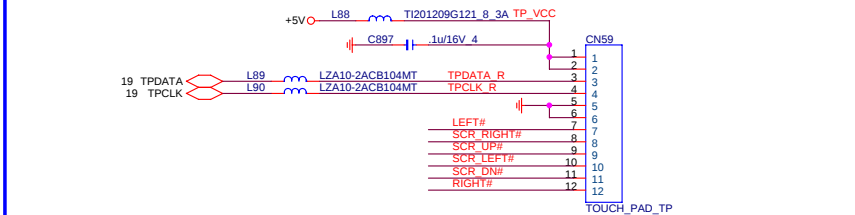
SATA



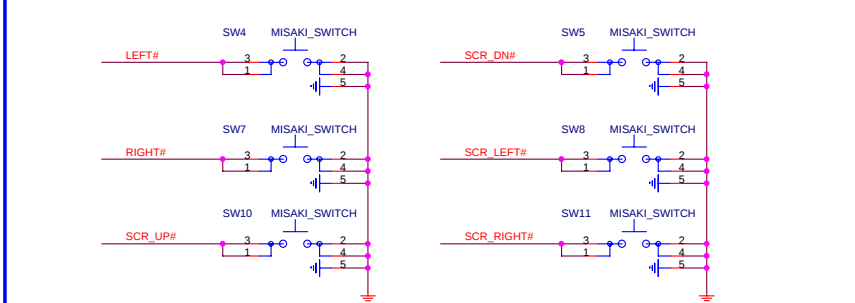
ODD



TP CONN



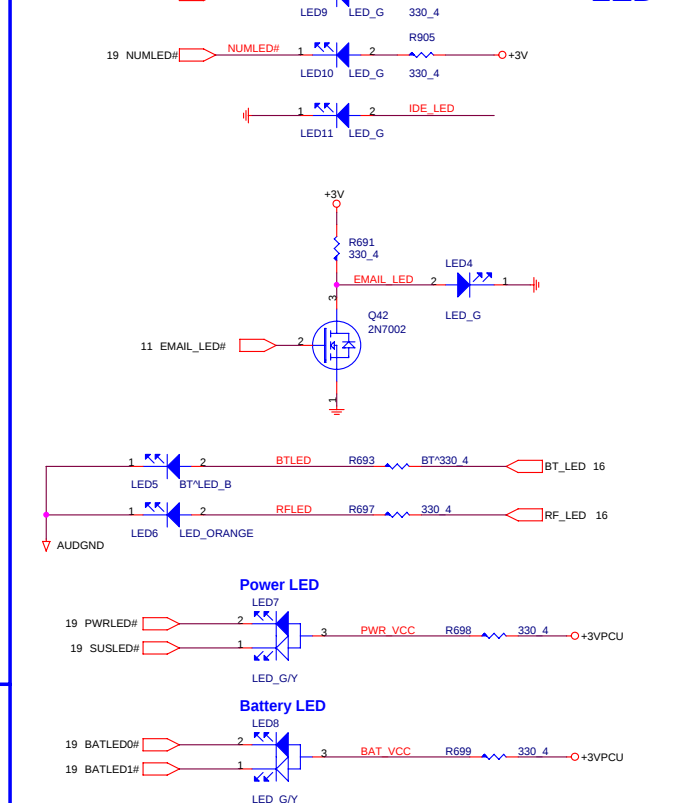
TP SWITCH



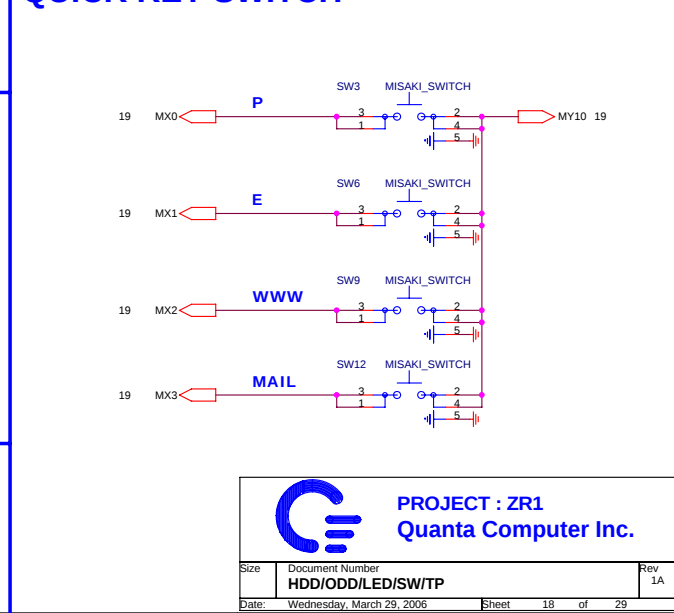
WL & BT SWITCH



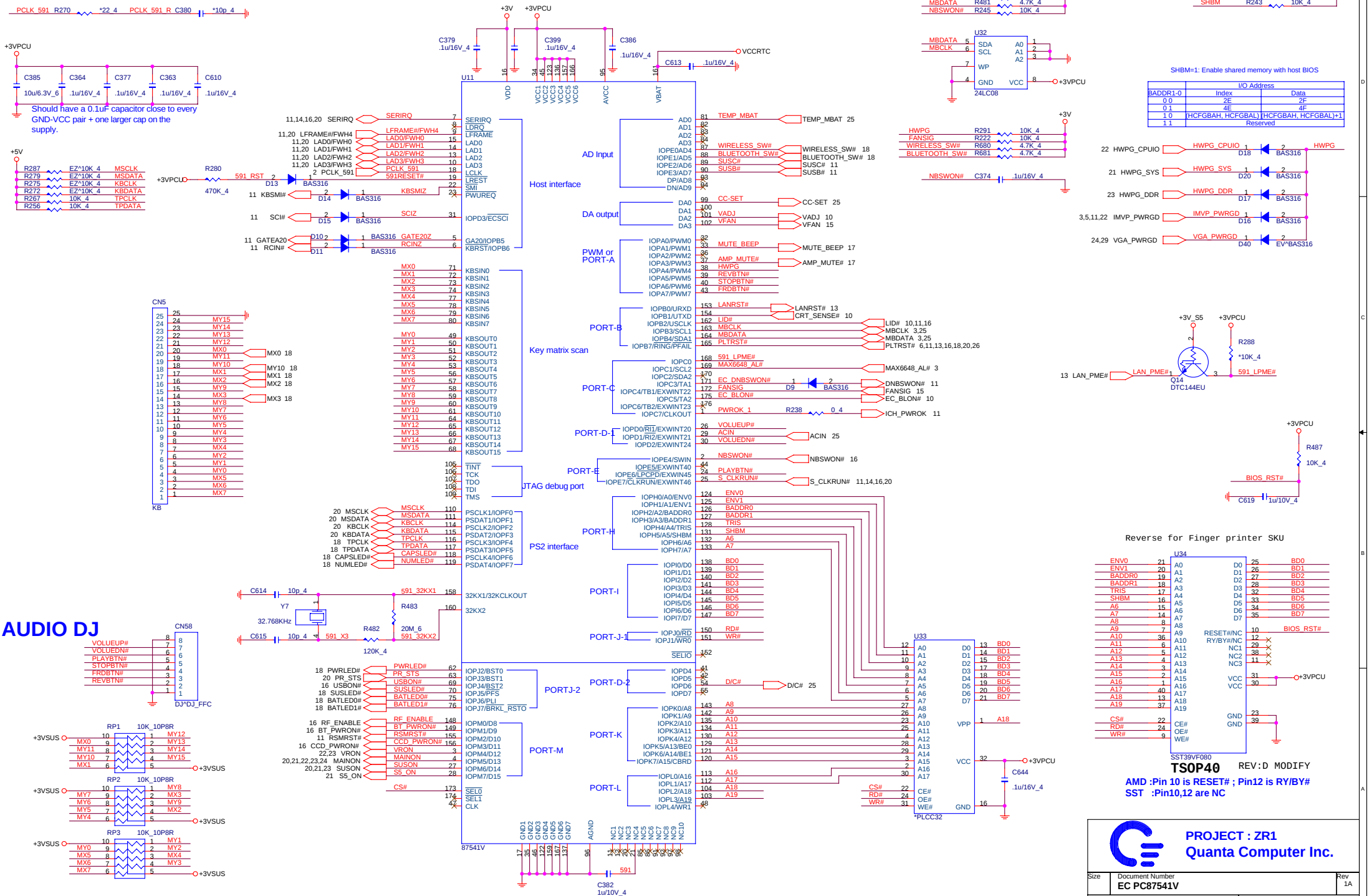
LED



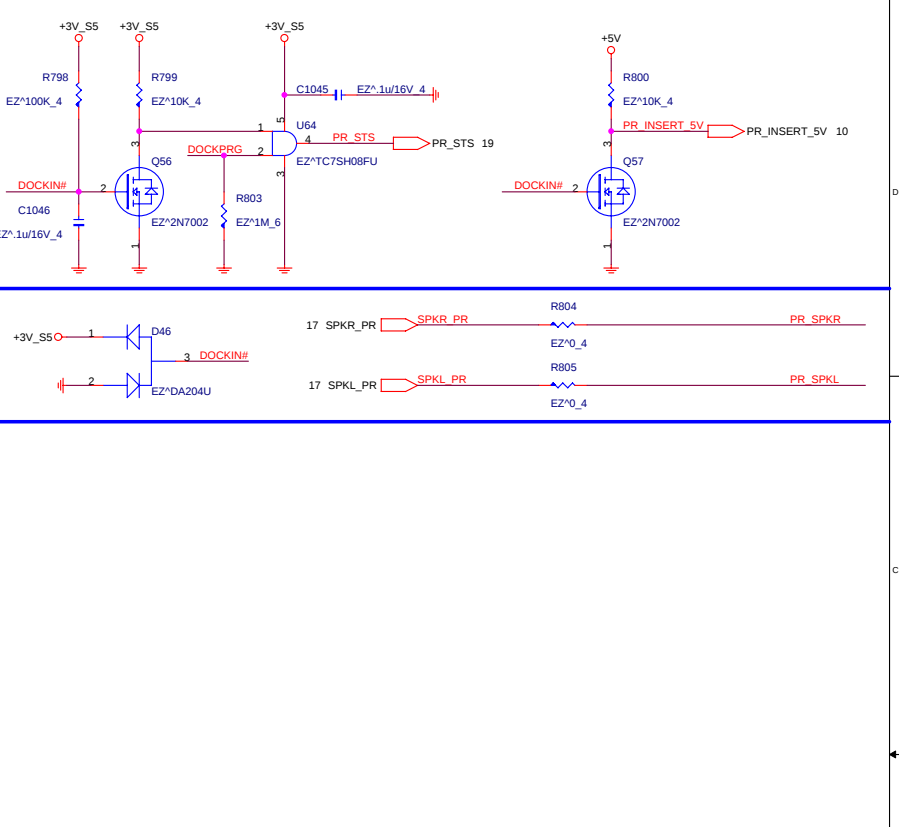
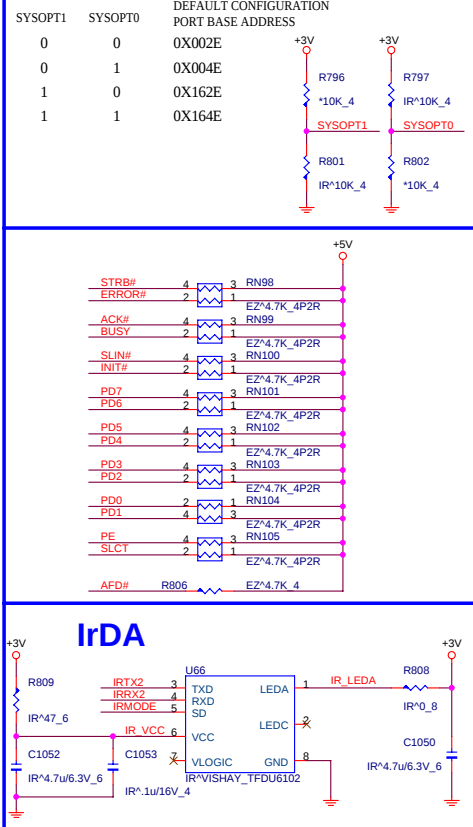
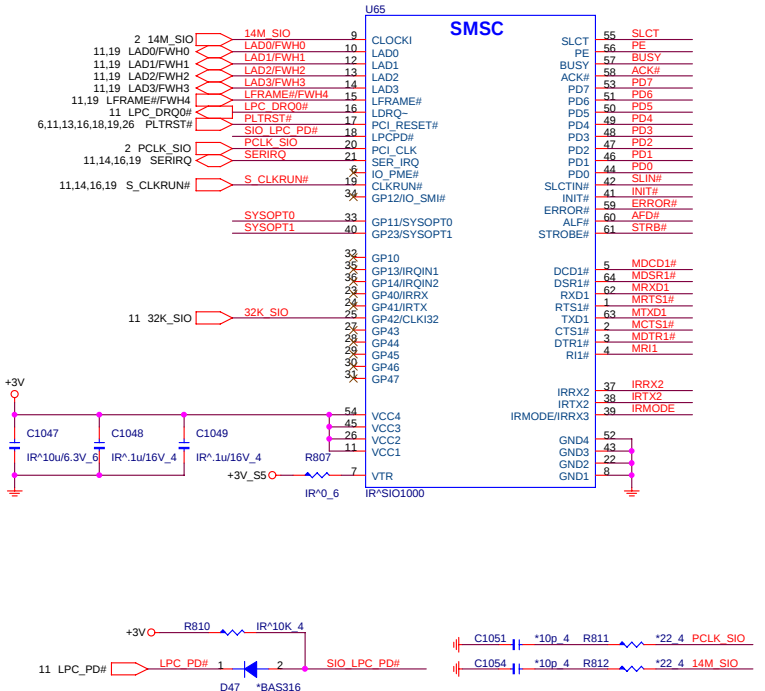
QUICK KEY SWITCH



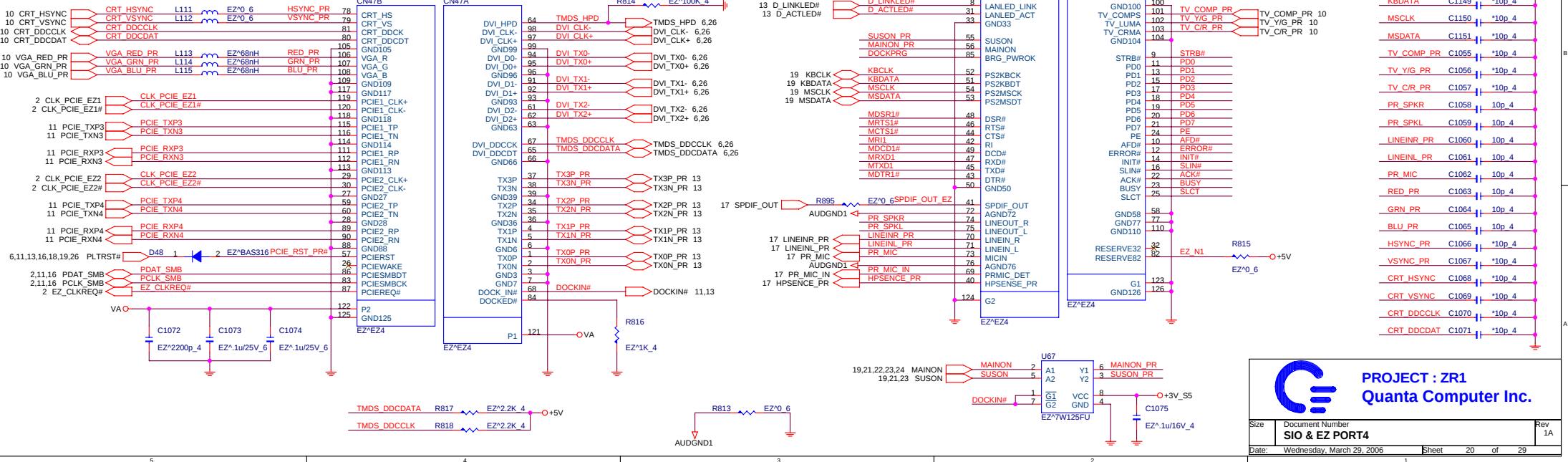
K/B CONTROLLER

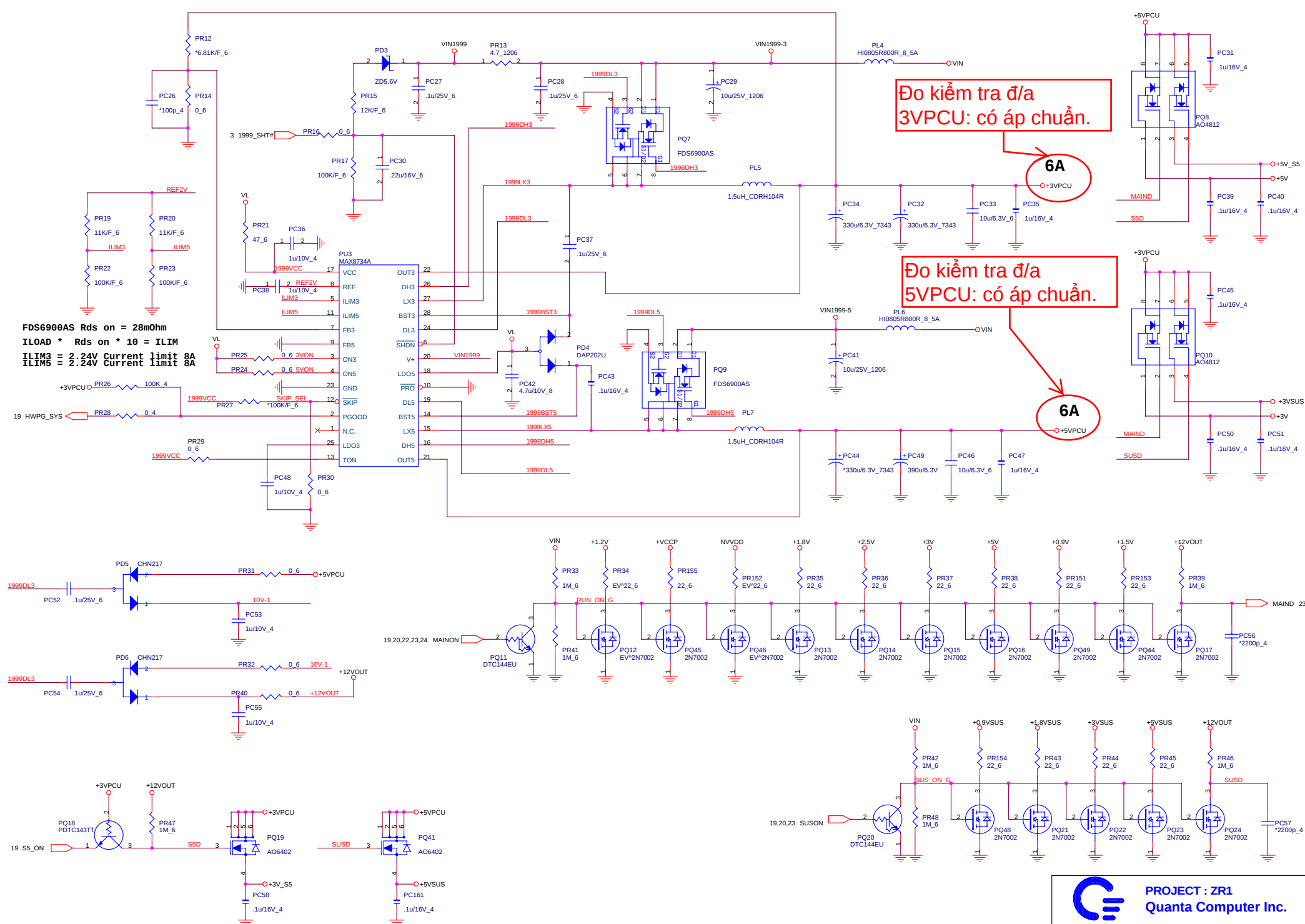


SMSC SIO1000



EZ4





Đo kiểm tra đ/a
3VPCU: có áp chuẩn.

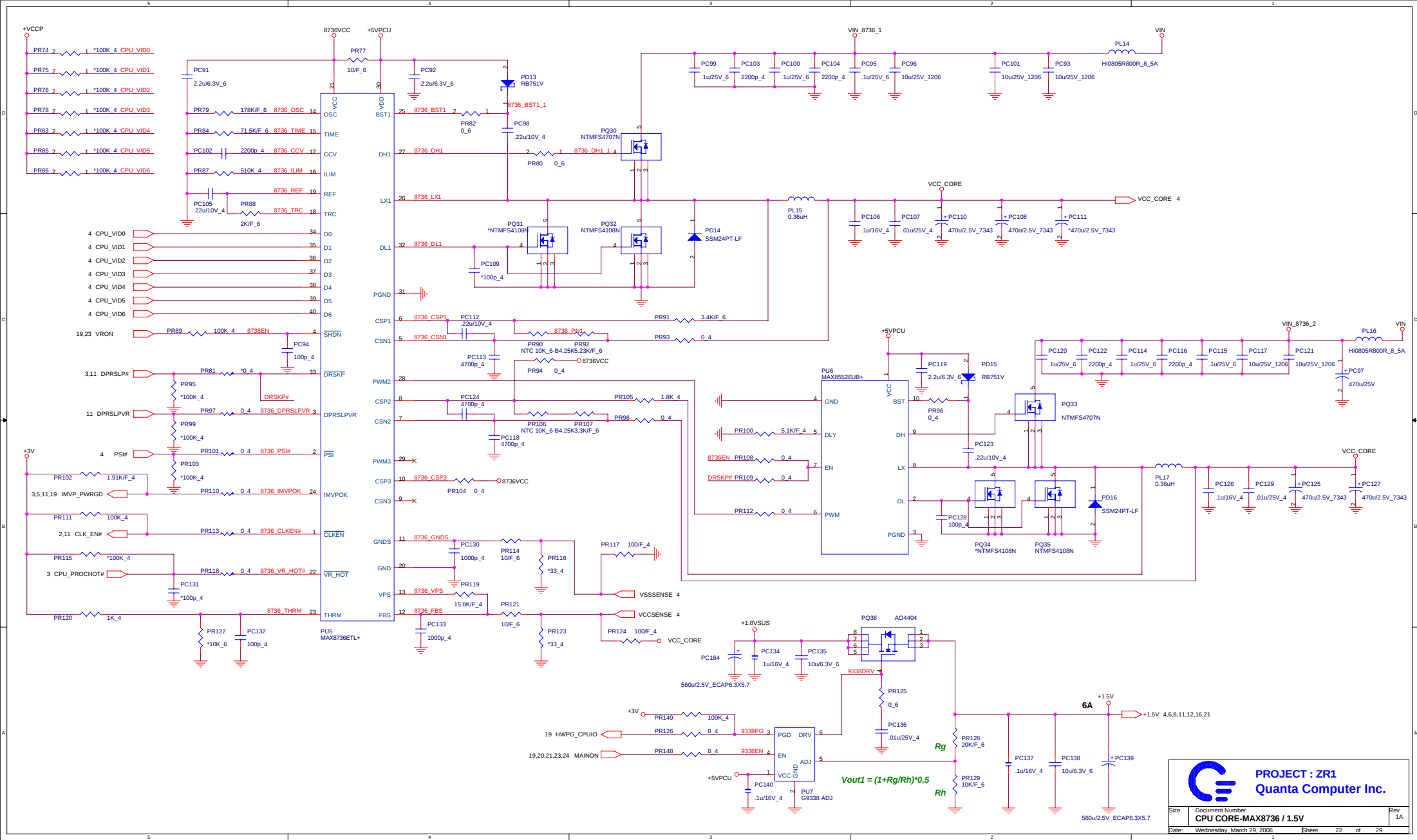
6A

Đo kiểm tra đ/a
5VPCU: có áp chuẩn.

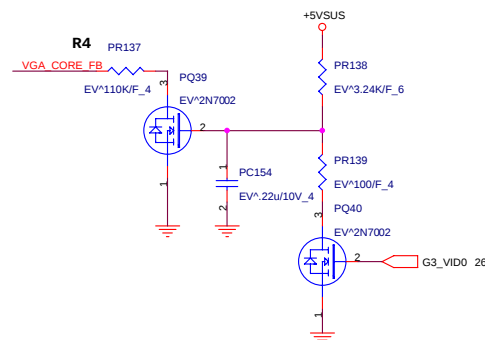
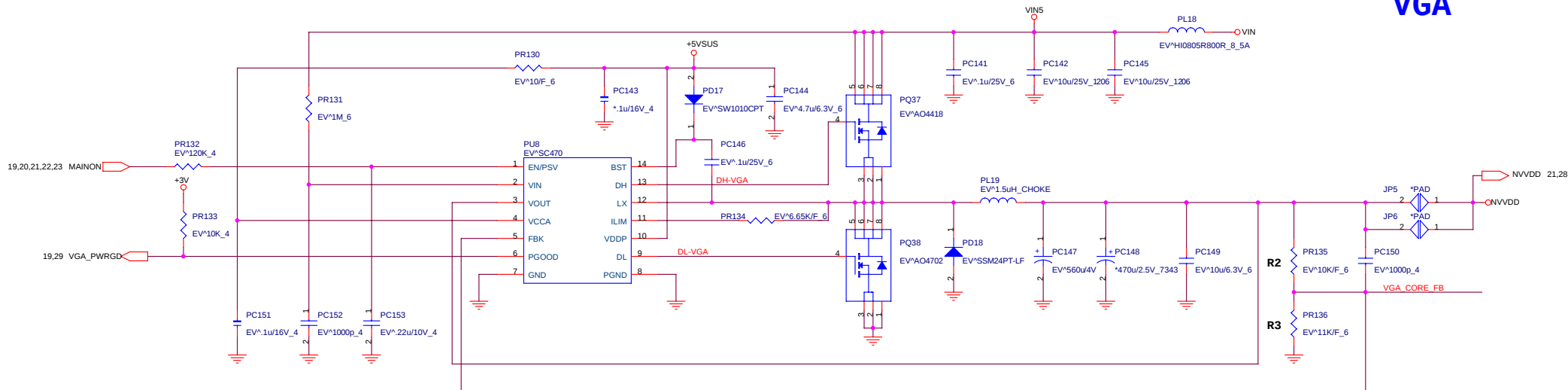
6A



PROJECT : ZR1
Quanta Computer Inc.



VGA



$$HI \rightarrow VOUT = (1 + R2/R3) * 0.5$$

$$LO \rightarrow VOUT = (1 + R2/(R3//R4)) * 0.5$$

M52P (G)

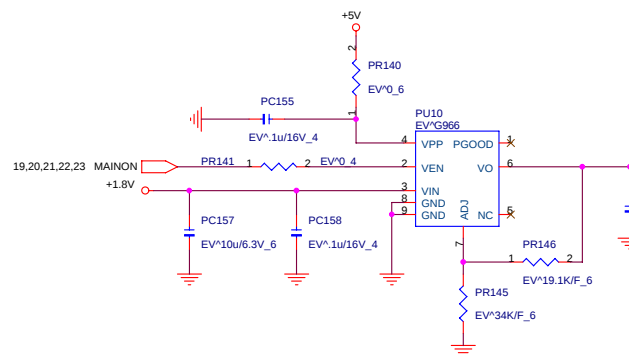
PR1 : 10K
PR4 : 11K
PR2 : 110K

M54P

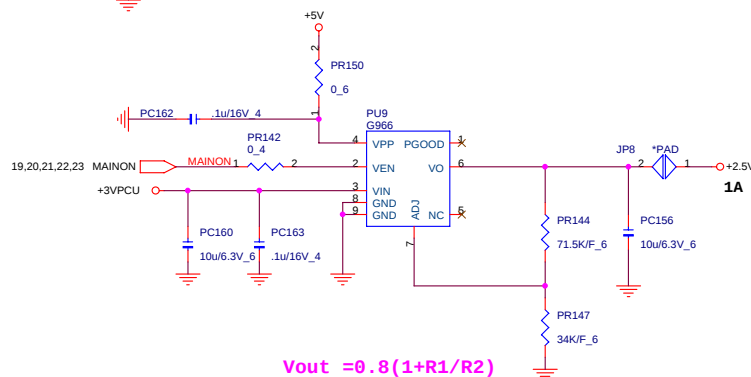
PR1 : 12K
PR4 : 12K
PR2 : 60.4K

Power Play Mode

VGA_PWR_SW	VGA_CORE
HI	0.95V -- M52P (G) 1.0V -- M54P
Default LO	1.0V -- M52P (G) 1.1V -- M54P



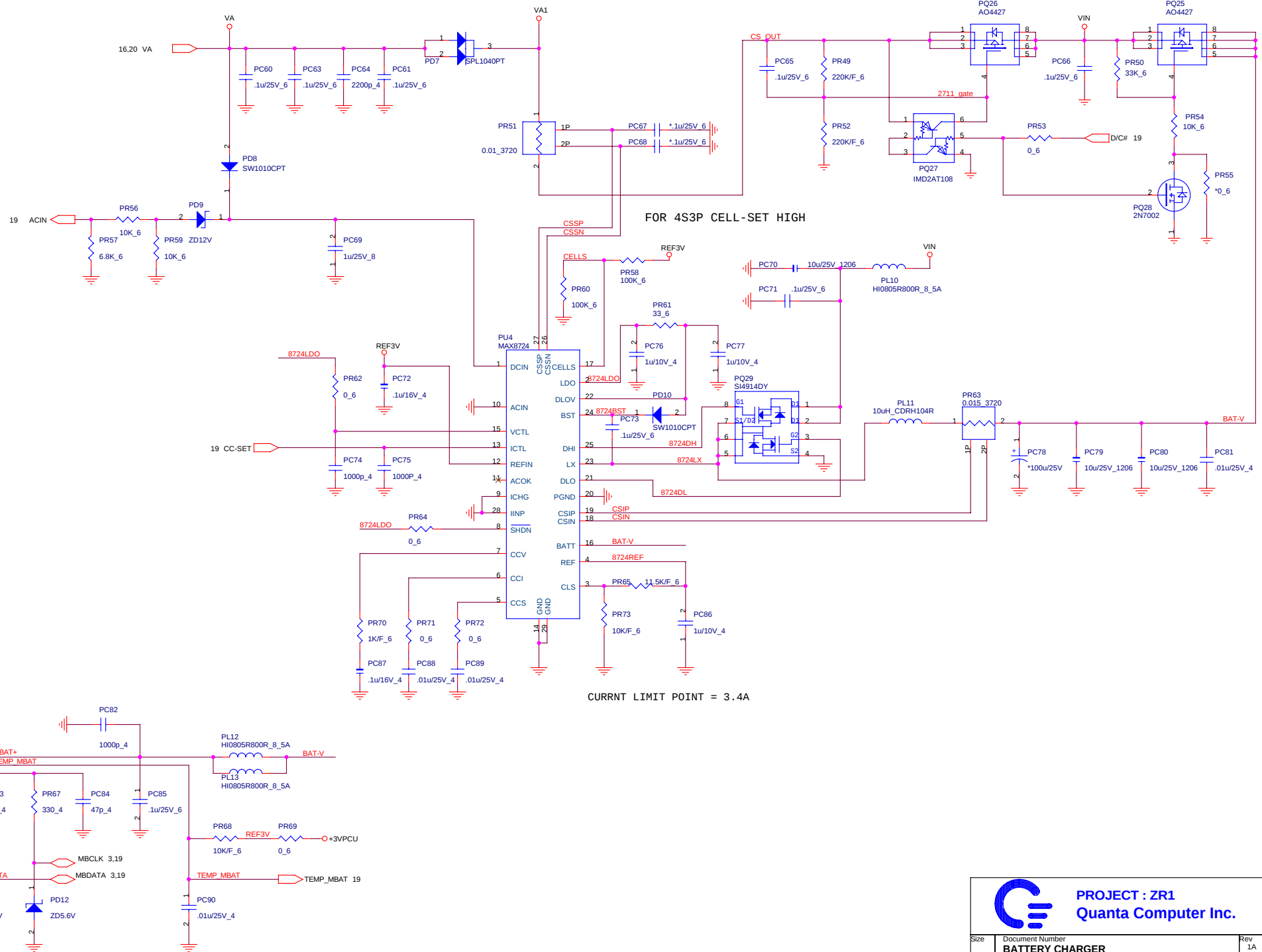
$$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 1.2V$$



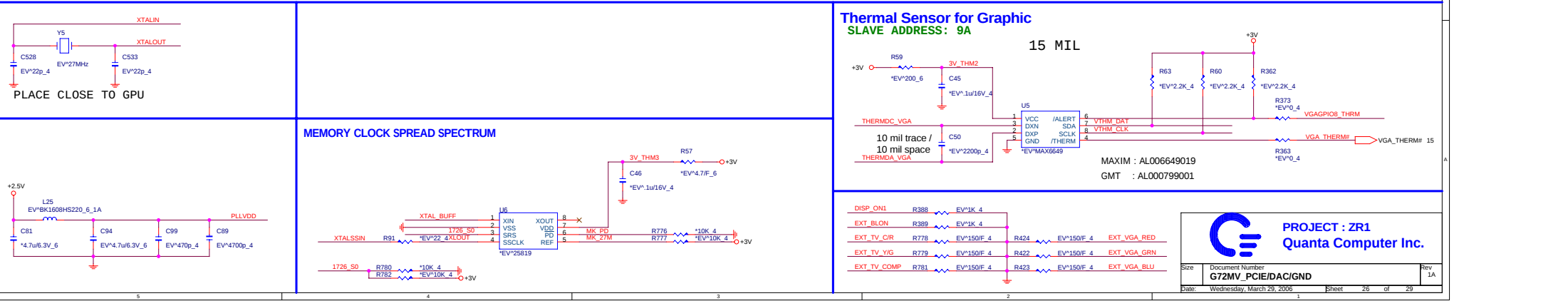
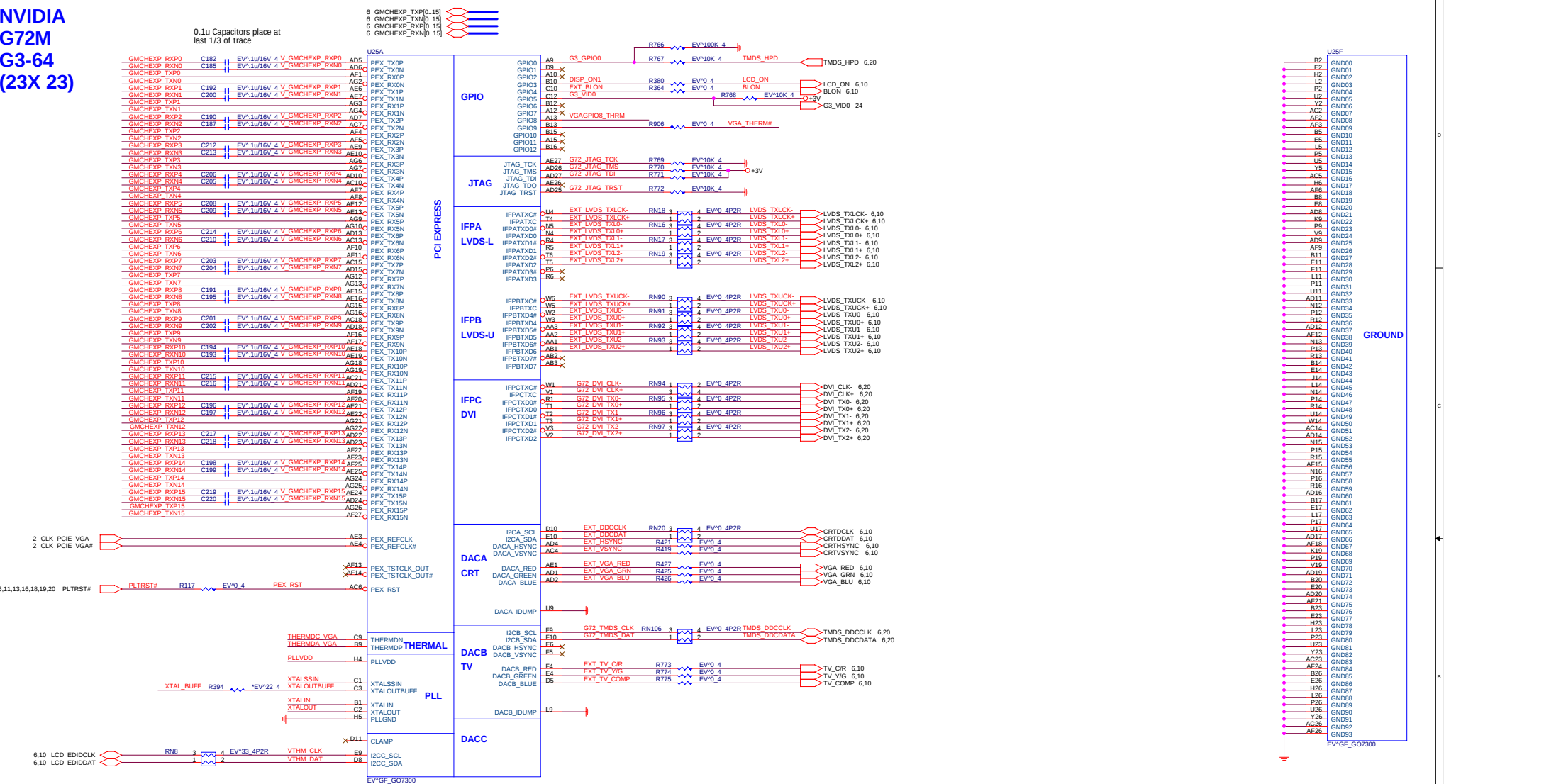
$$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 2.5V$$

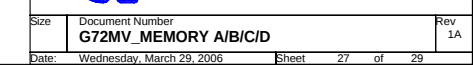


PROJECT : ZR1
Quanta Computer Inc.



NVIDIA
G72M
G3-64
(23X 23)





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