

ZZZ8
DAZ@
PCB
DAZ04300100

ZZZ1
DA2@
PCB
MAIN BOARD
DA600007E10

ZZZ2
DA2@
PCB
E board
DA40000A910

ZZZ3
DA2@
PCB
FP board
DA600007D10

ZZZ4
DA2@
PCB
Function board
DA40000AA10

ZZZ5
DA2@
PCB
USB board
DA40000AB10

ZZZ6
DA2@
PCB
IO board
DA40000AC10

ZZZ7
DA2@
PCB
Power board
DA40000AD10

Compal Confidential

JAT10 M/B Schematics Document

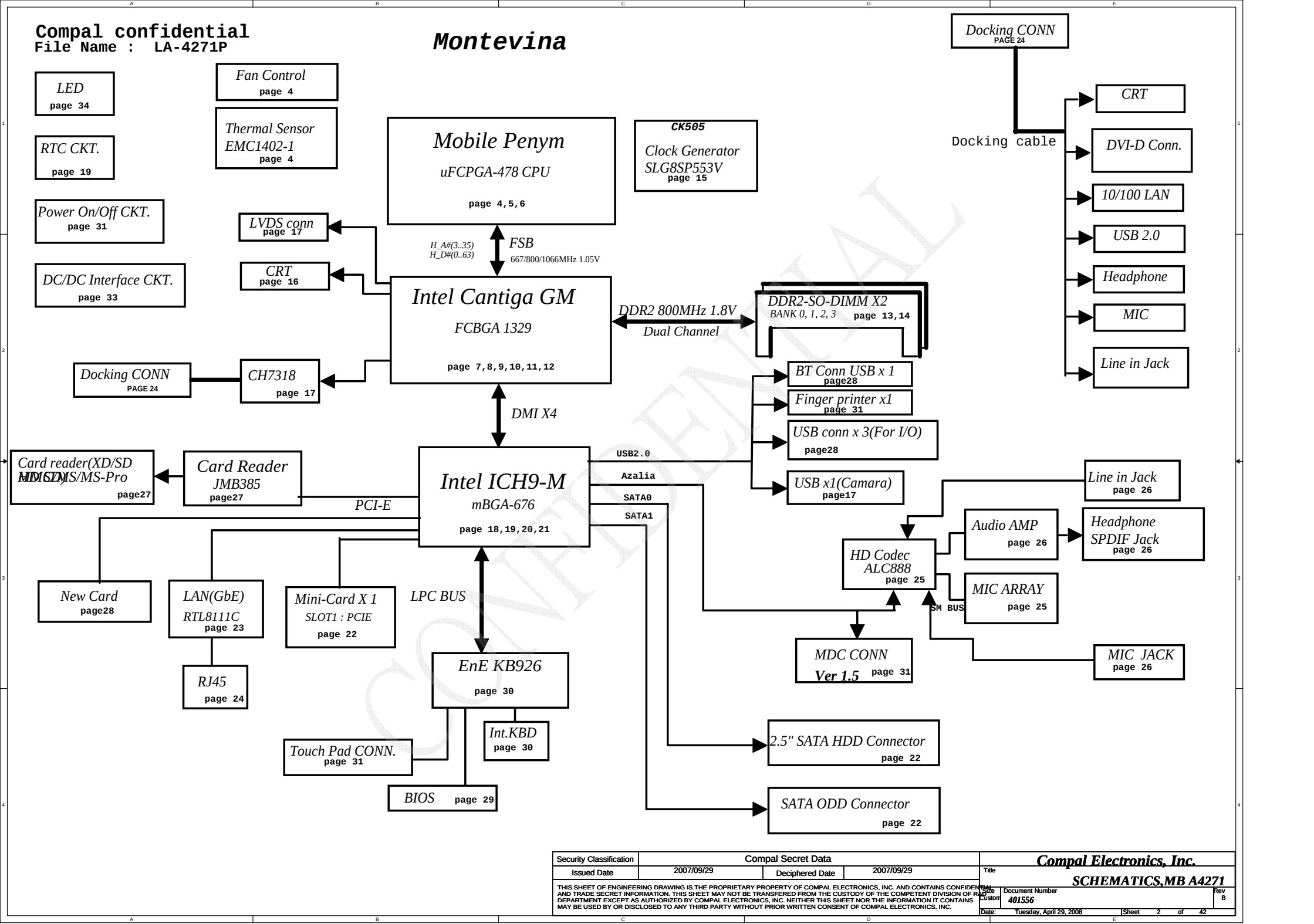
Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-04-07

REV:1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	SCHEMATICS,MB A4271
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Date: Tuesday, April 29, 2008				Rev	B
Sheet 1 of 42					

Montevina



power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

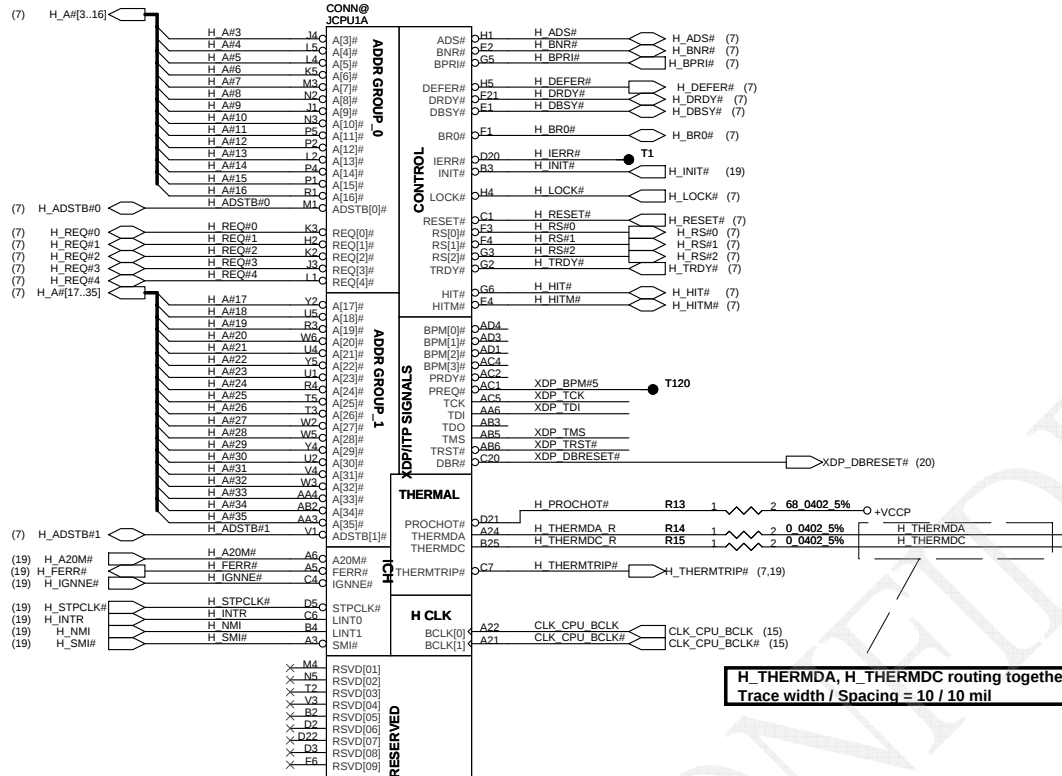
@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

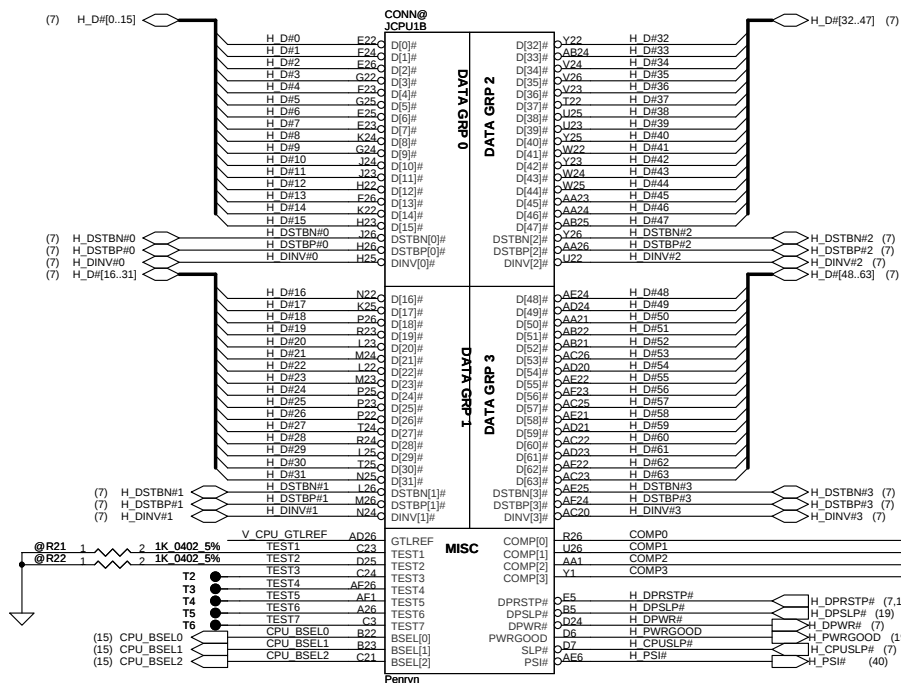
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

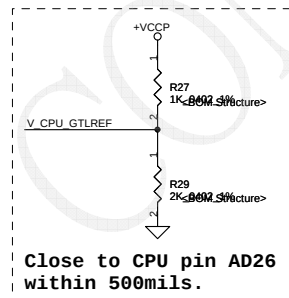
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010



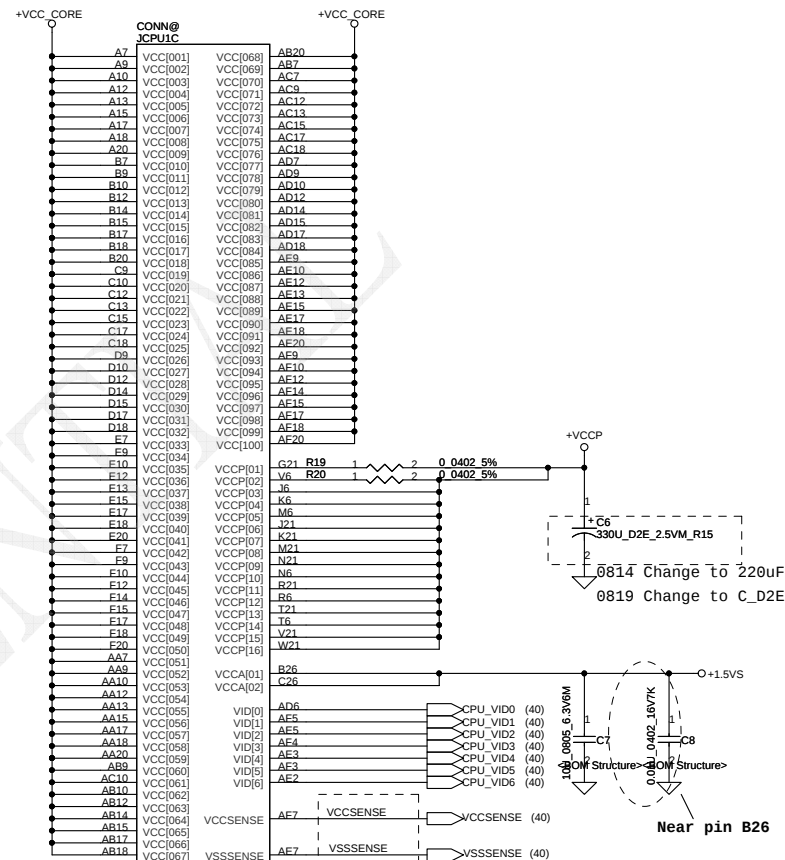


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

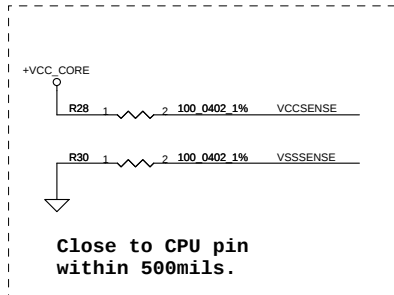
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

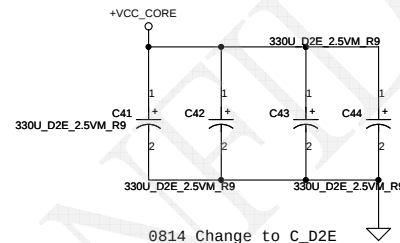
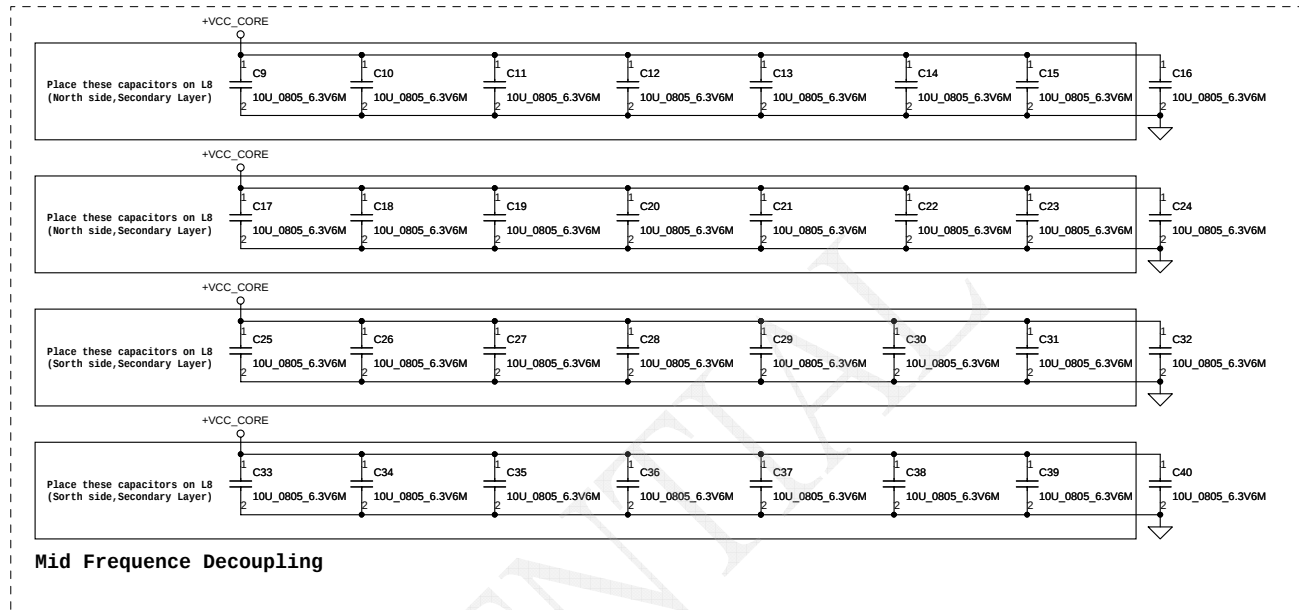
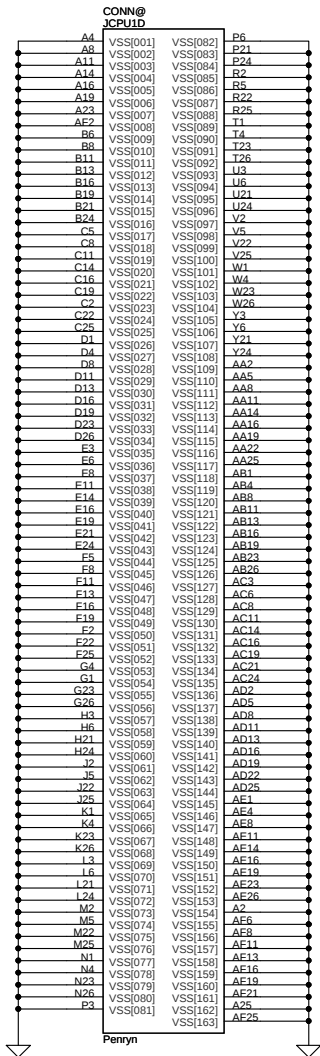


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

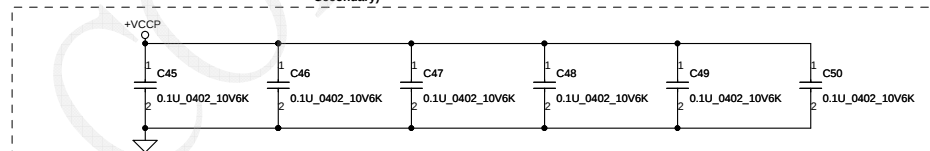


Length match within 25 mils. The trace width/space/other is 20/7/25.

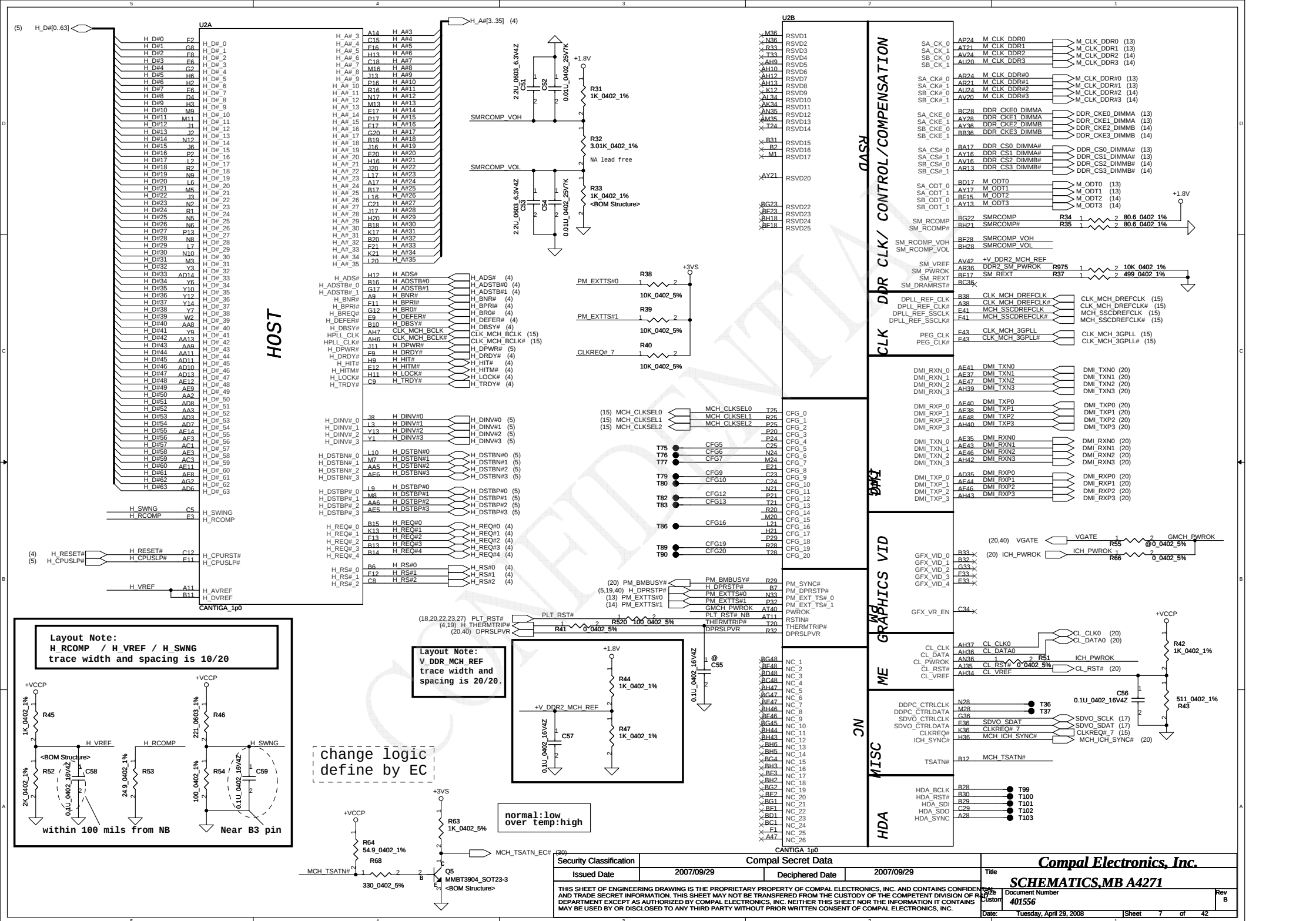




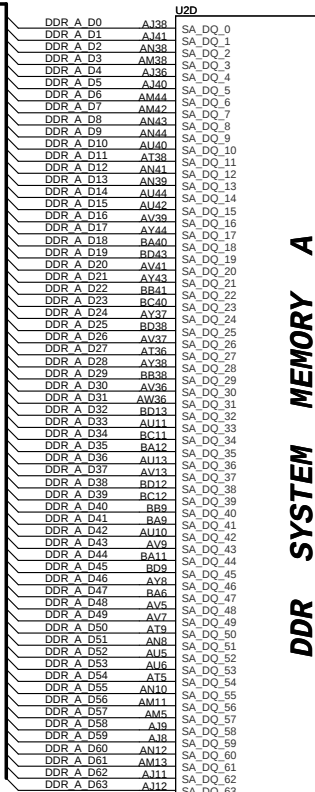
Place these inside socket cavity on L8 (North side Secondary)



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Date: Tuesday, April 29, 2008				Sheet	6 of 42

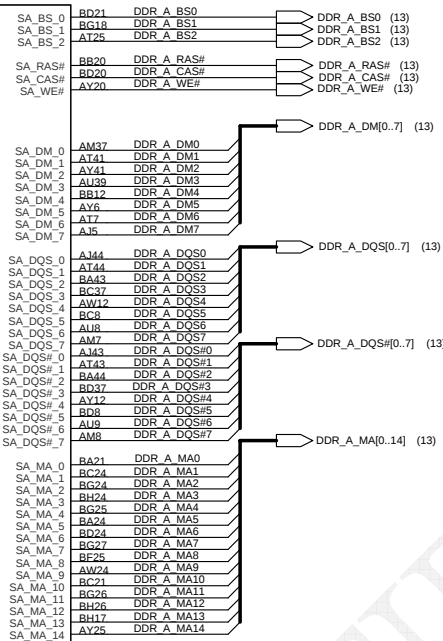


(13) DDR_A_D[0..63]

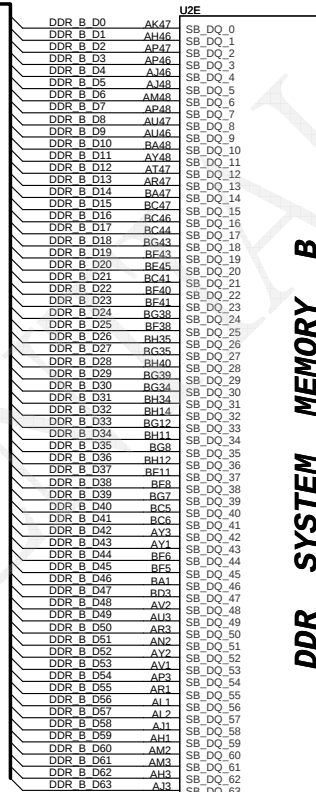


DDR SYSTEM MEMORY A

CANTIGA_1p0

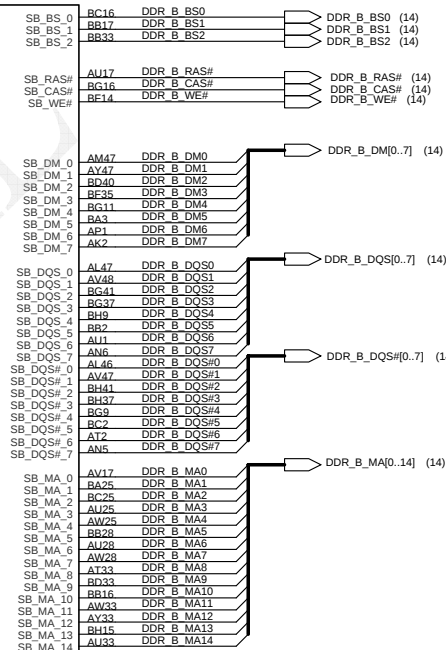


(14) DDR_B_D[0..63]

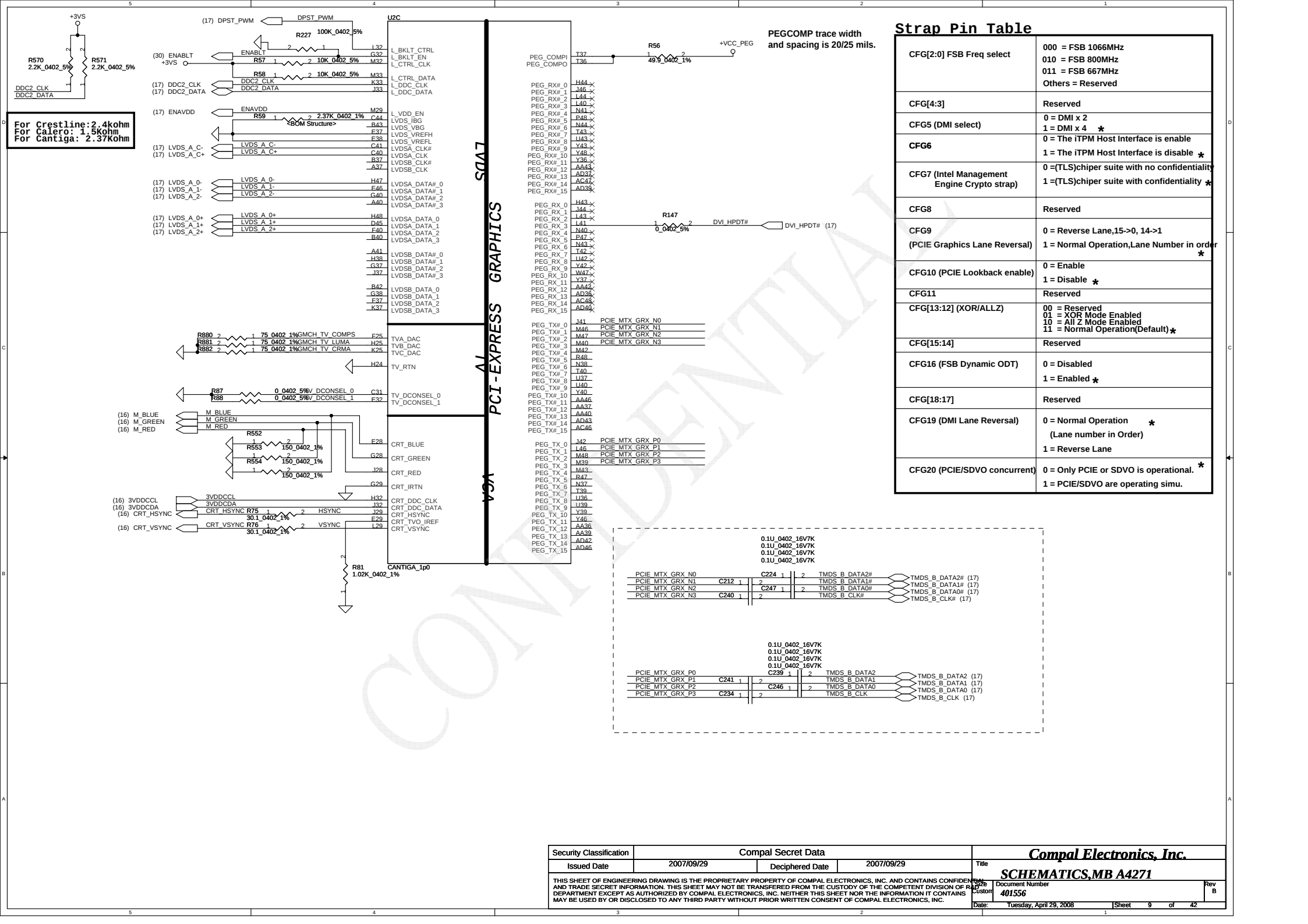


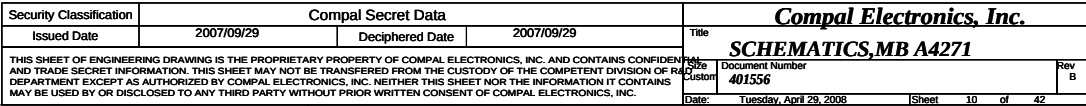
DDR SYSTEM MEMORY B

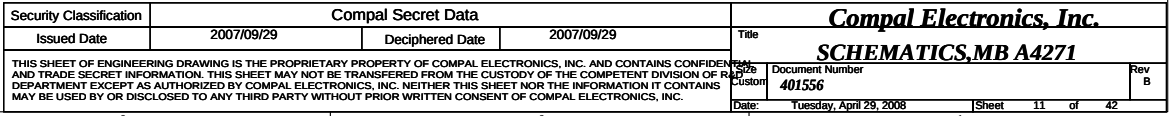
CANTIGA_1p0

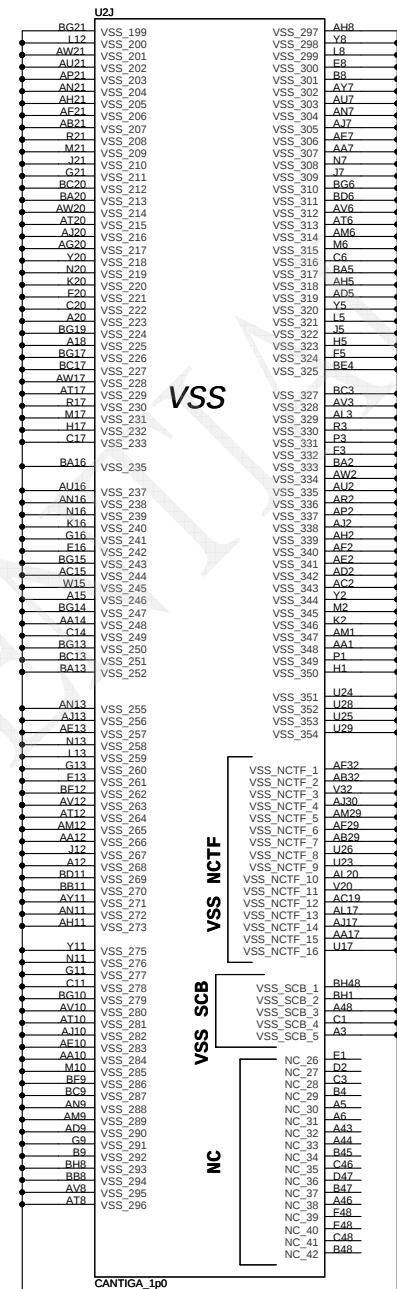
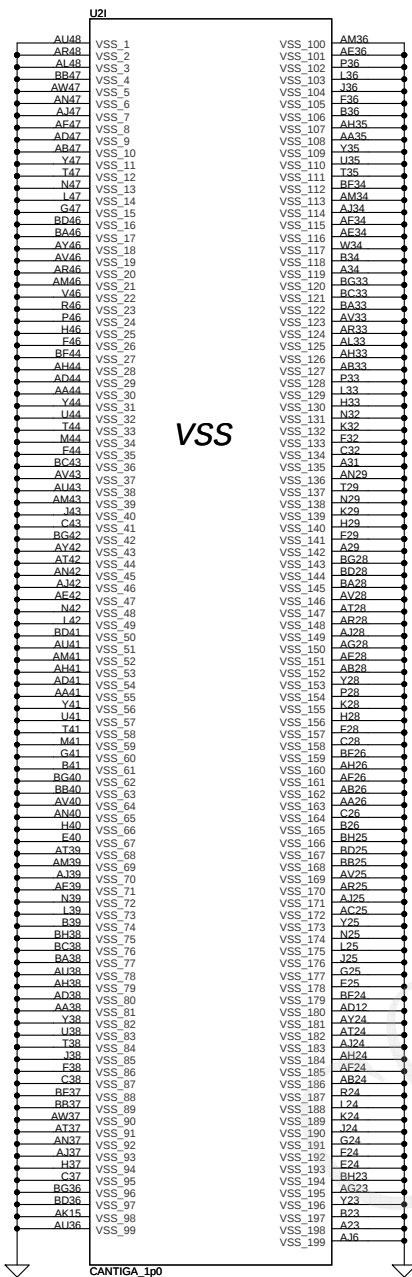


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Date:	Tuesday, April 29, 2008	Sheet	8	of 42

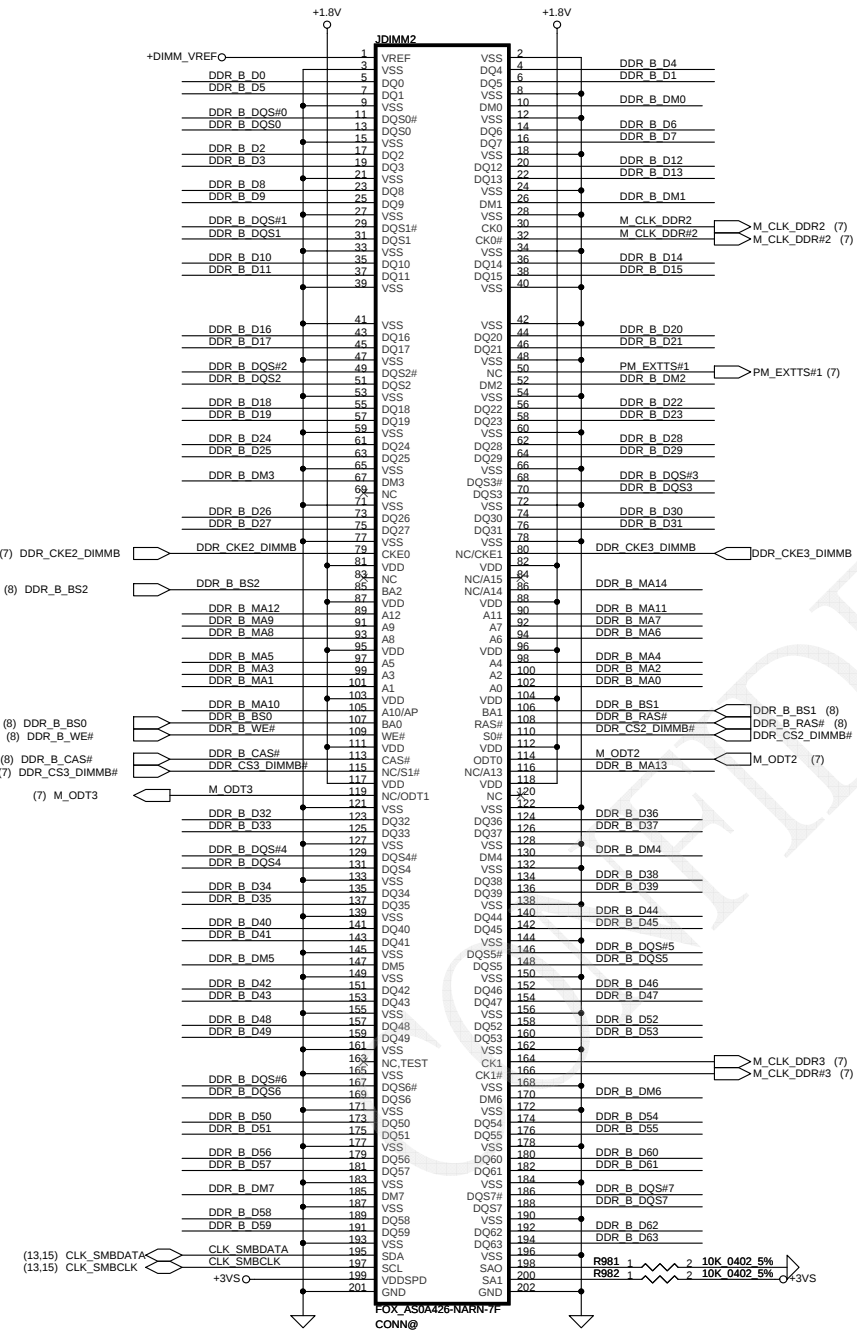


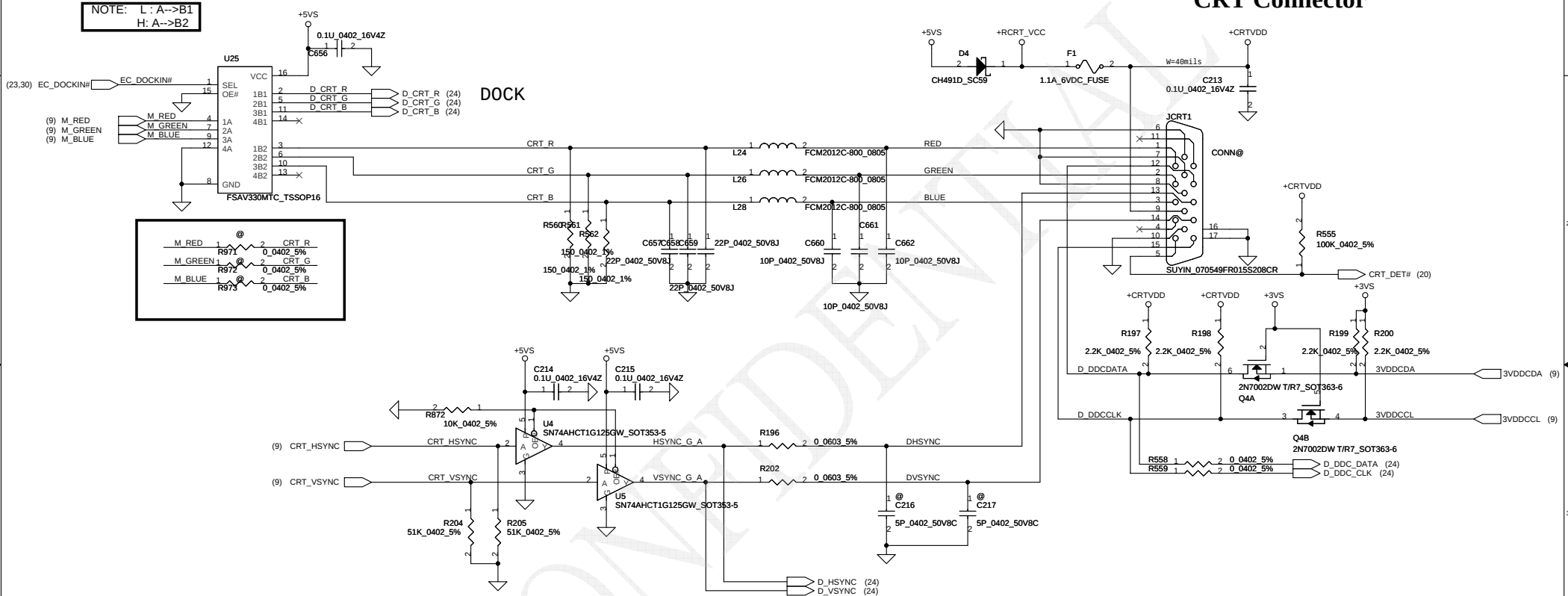






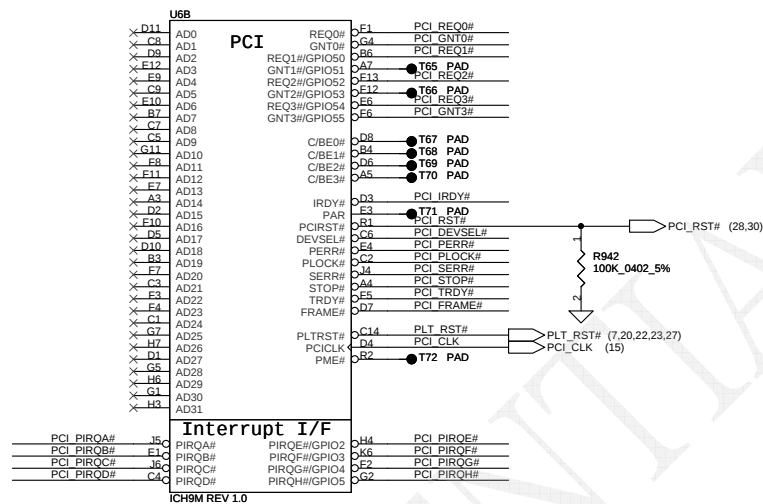
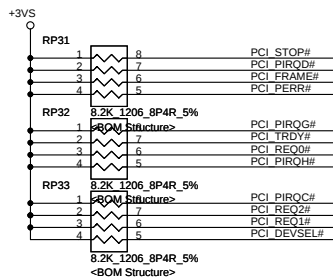
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				401556	401556
				Date: Tuesday, April 29, 2008	Sheet 12 of 42



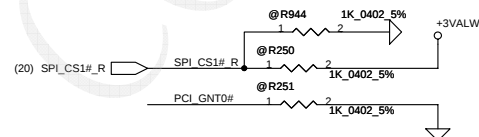
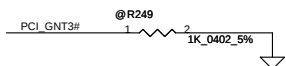


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Date: Tuesday, April 29, 2008				Sheet 16	of 42

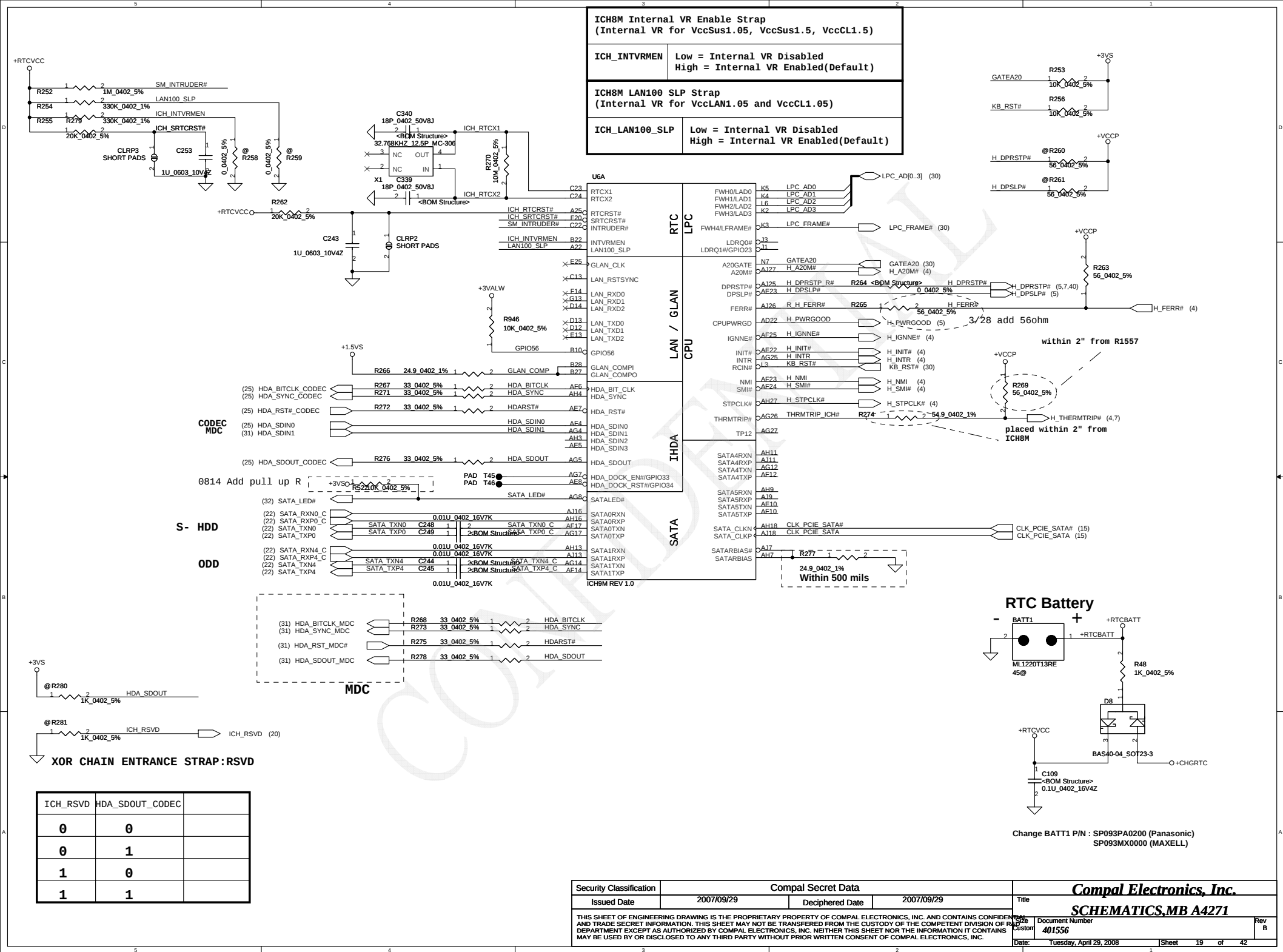
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SCHEMATICS, MB A4271



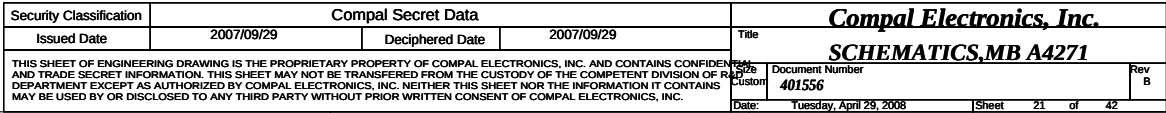
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

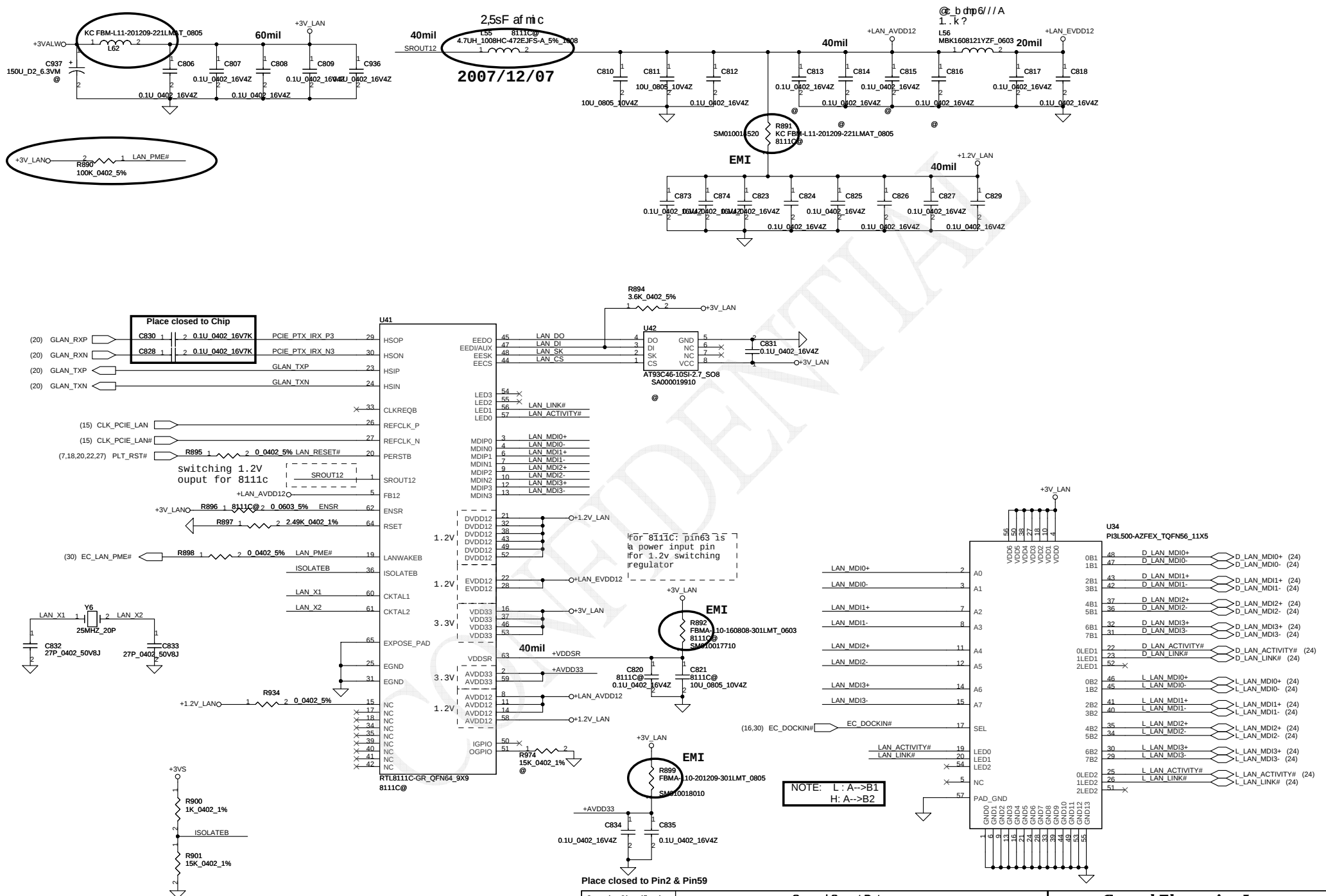


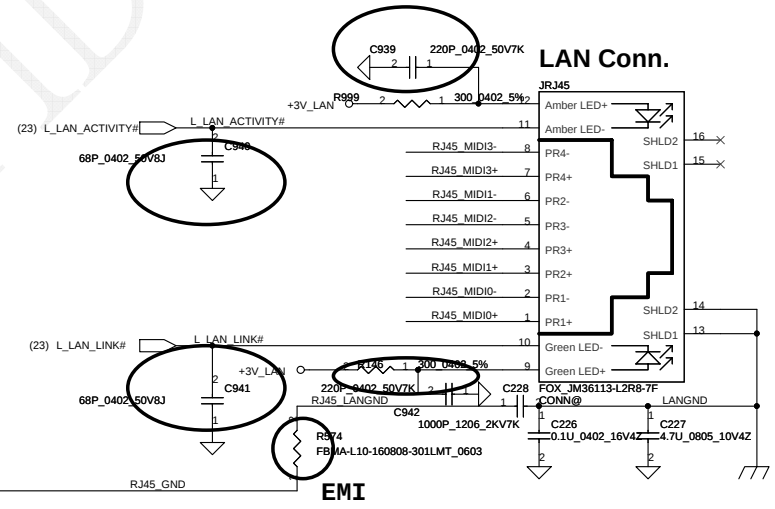
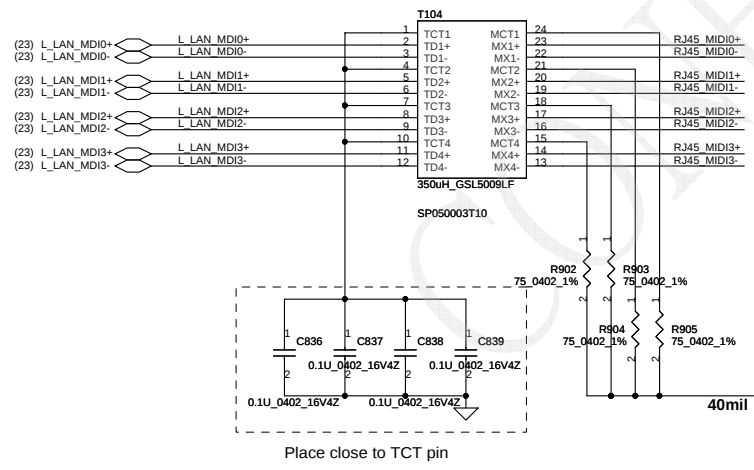
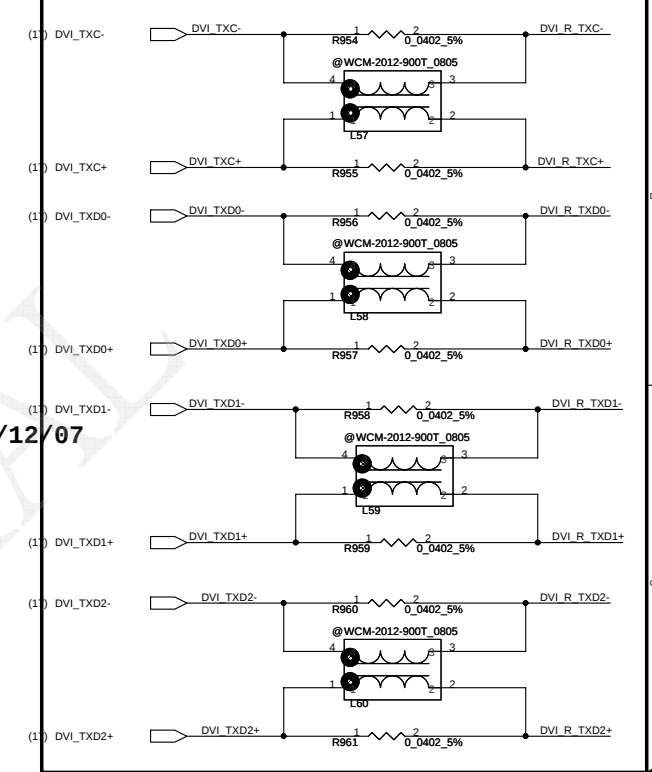
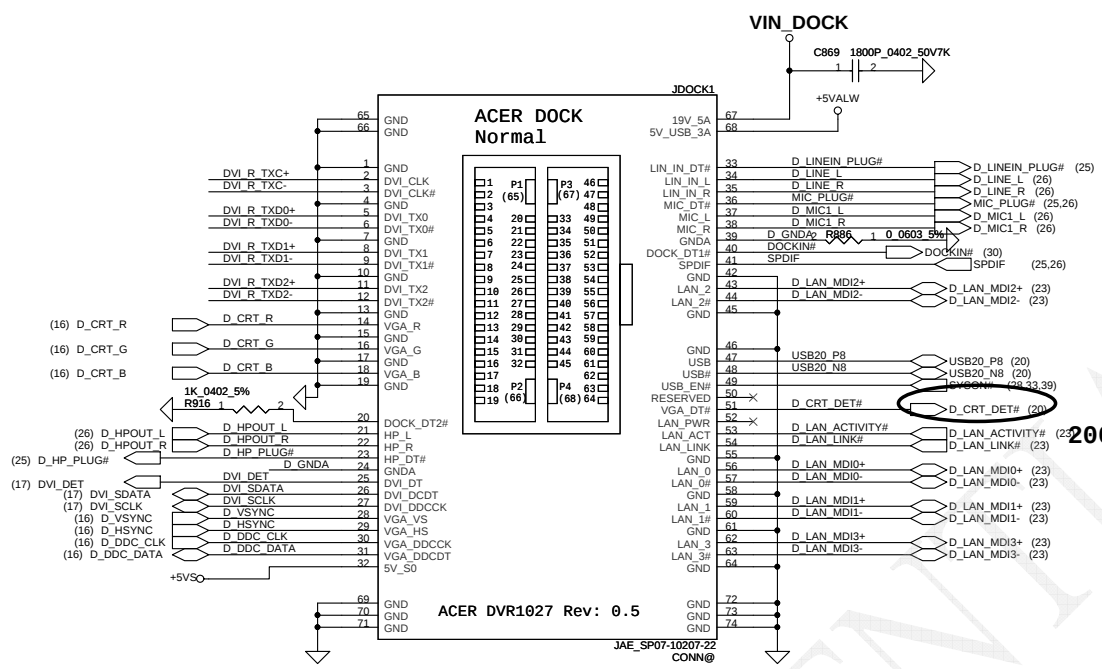
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					401556	B
				Date:	Tuesday, April 29, 2008	Sheet 18 of 42



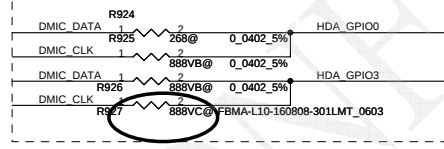
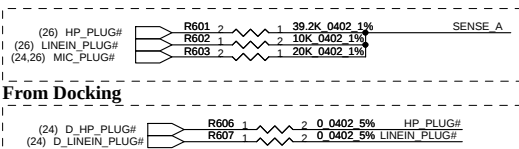
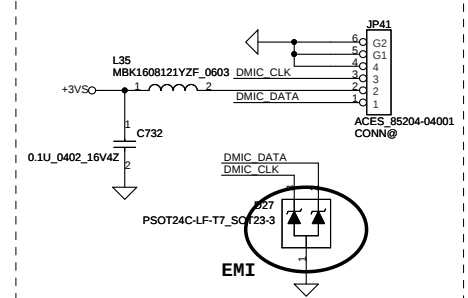
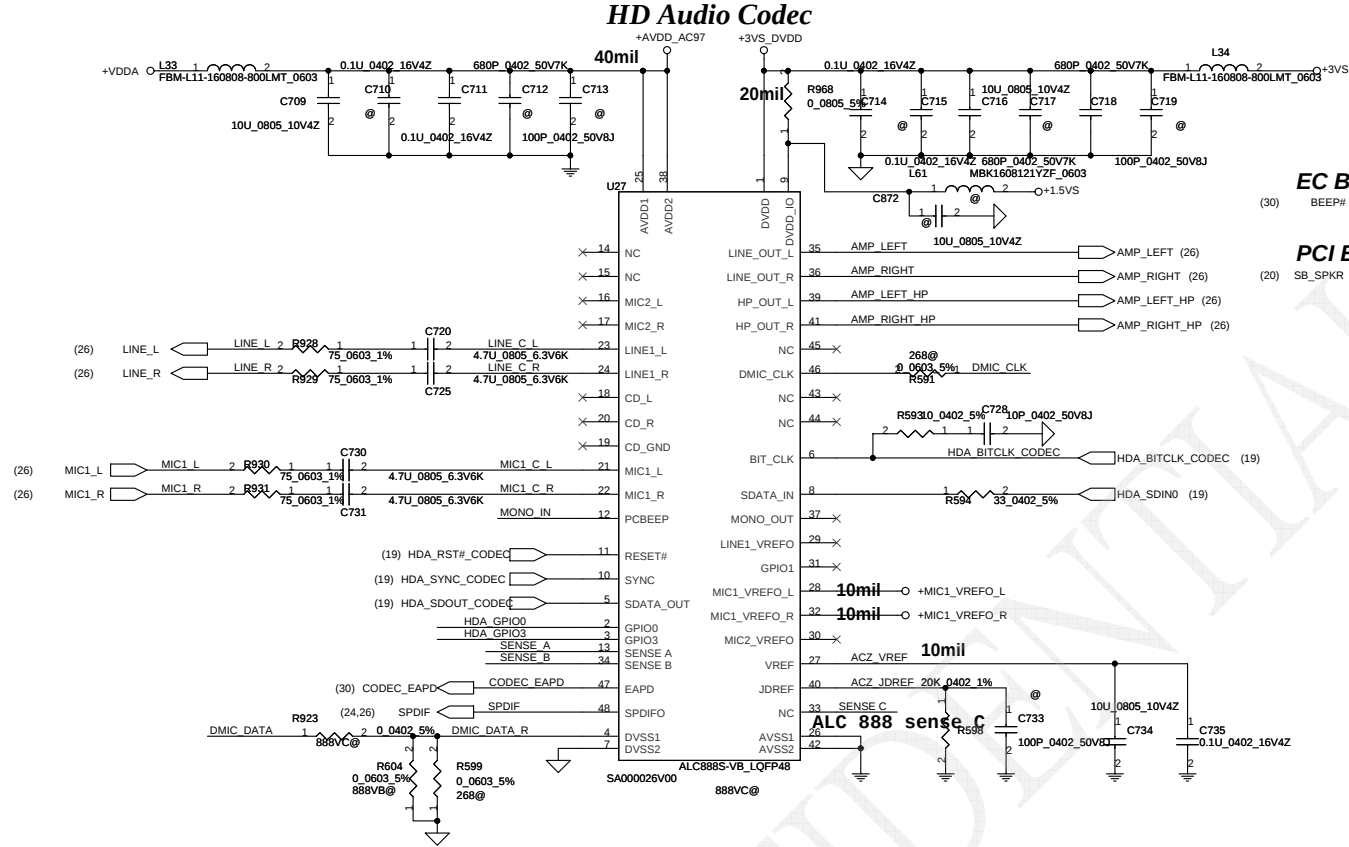
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								401556							
								Date:		Tuesday, April 29, 2008				Sheet 20 of 42	



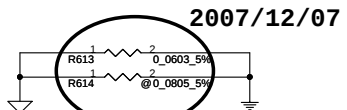
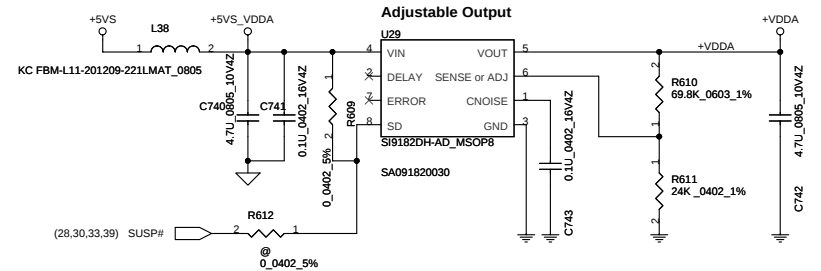




HD Audio Codec

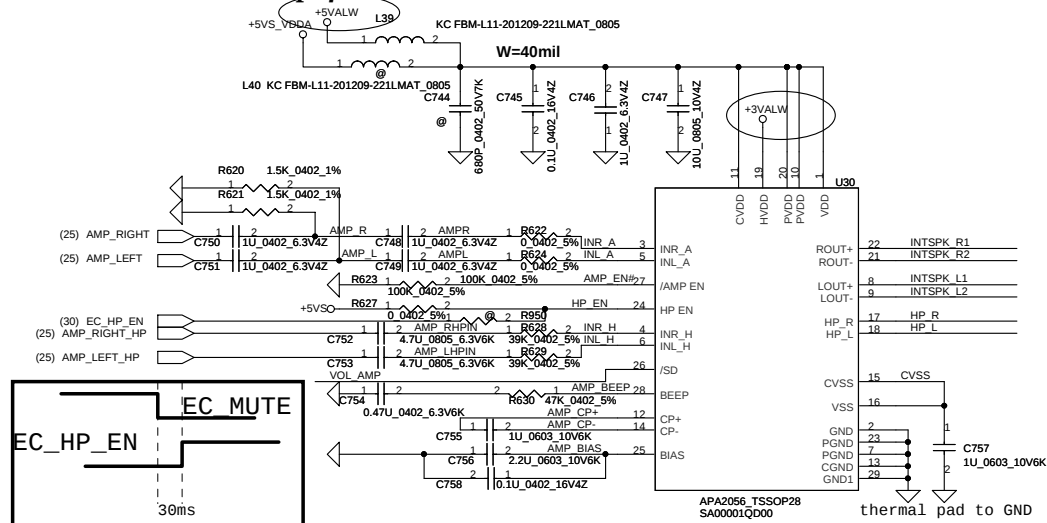


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)
SENSE C	39.2K	CD
	20K	1st S/PDIF Out
	10K	2nd S/PDIF Out
	5.1K	S/PDIF-IN

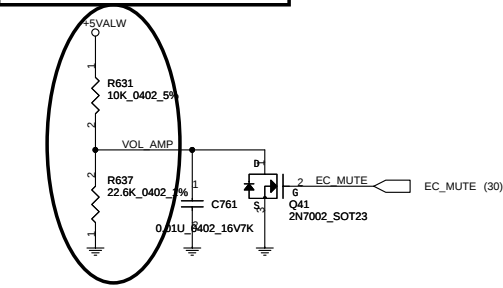


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				Date:	Tuesday, April 29, 2008	Sheet 25 of 42

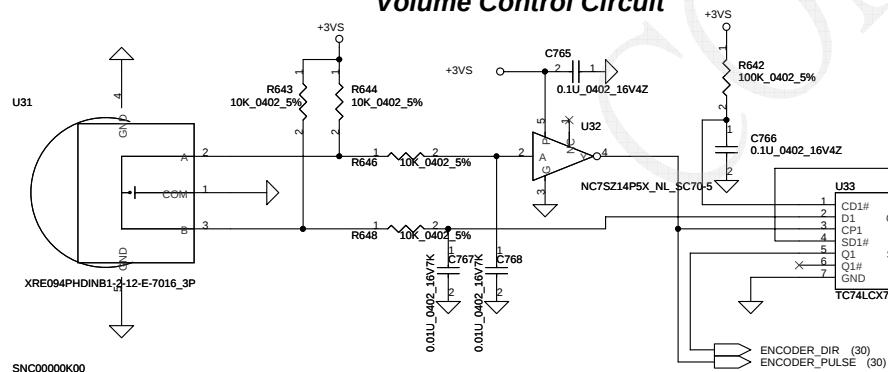
APA2057 SPK/HP Amplifier



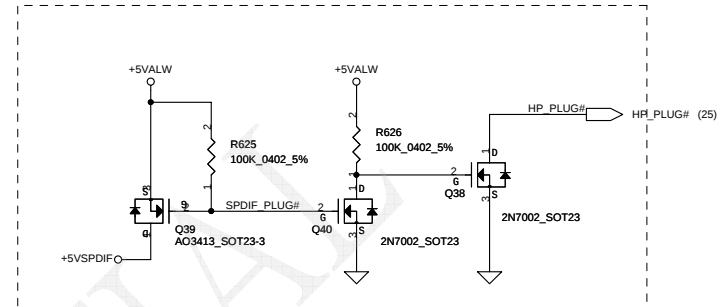
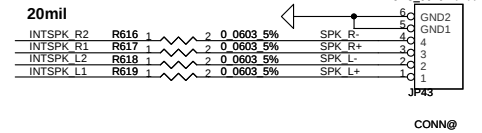
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



Volume Control Circuit

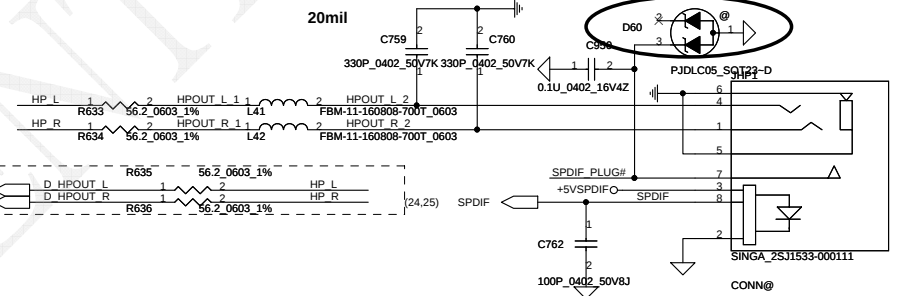


Int. Speaker Conn.

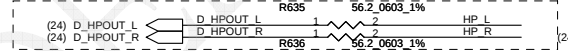


LINE Out/Headphone Out

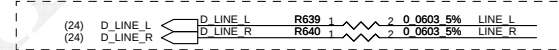
2007/12/07 SPDIF Out JACK



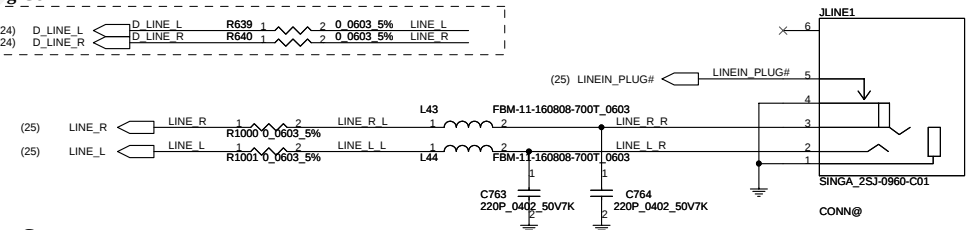
Docking Conn



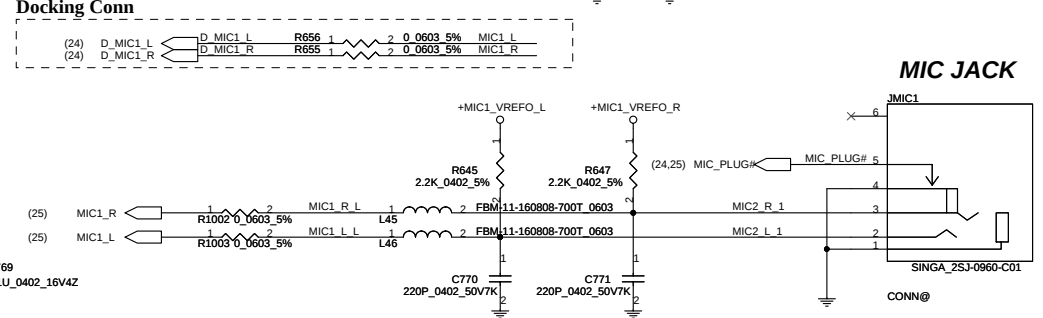
Docking Conn



LINE-IN JACK

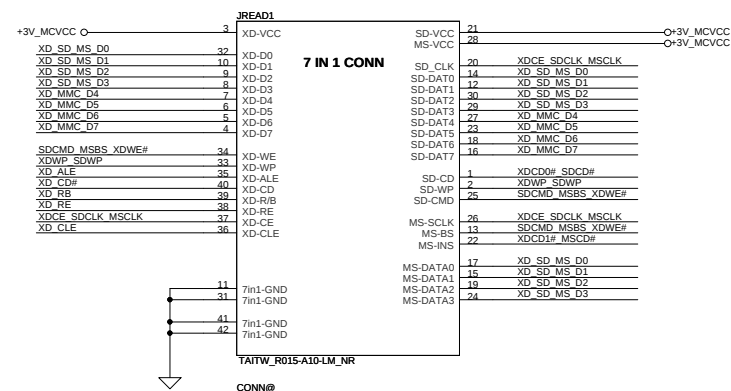
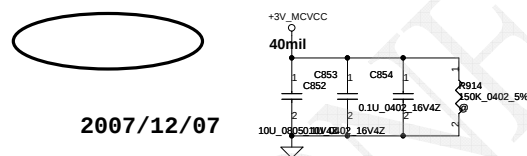
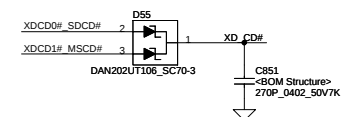
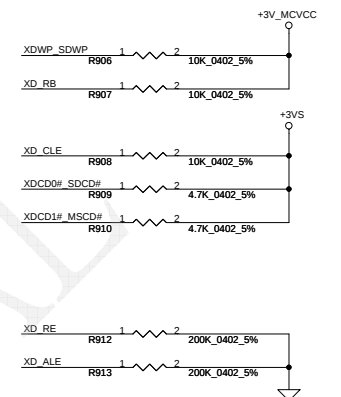
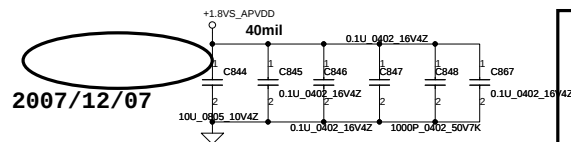


MIC JACK



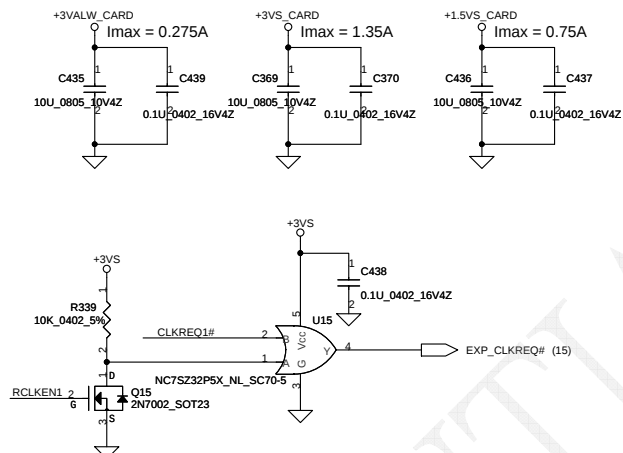
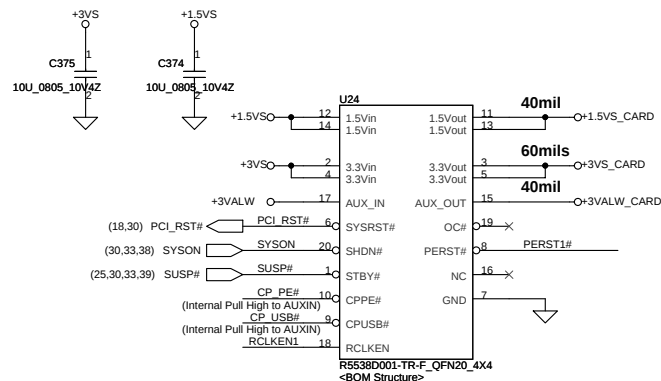
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				401556	
				Date: Tuesday, April 29, 2008	Sheet 26 of 42

SCHEMATICS, MB A4271

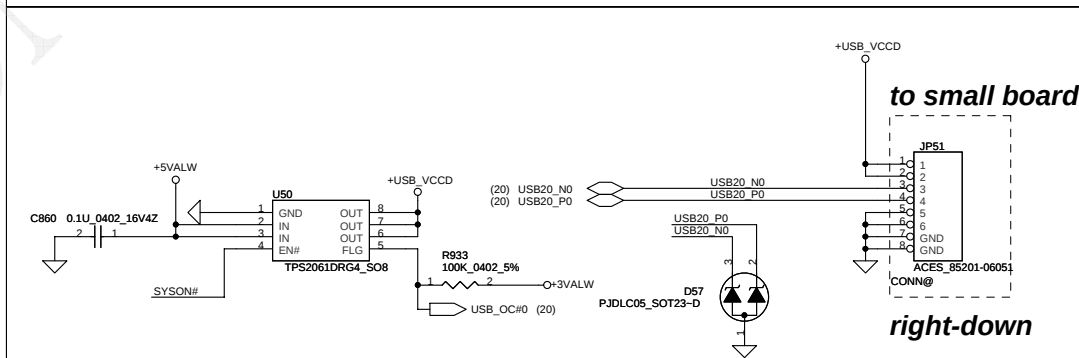
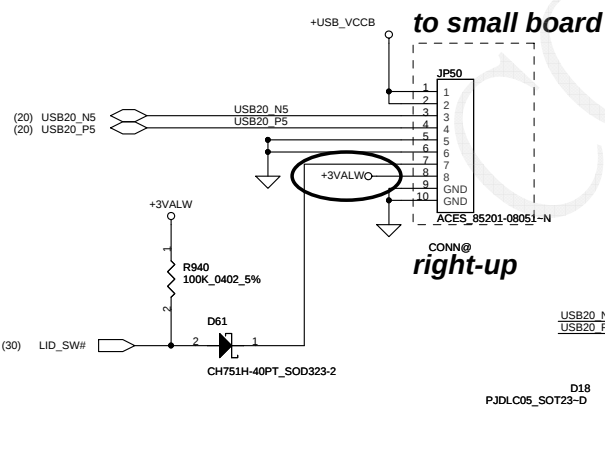
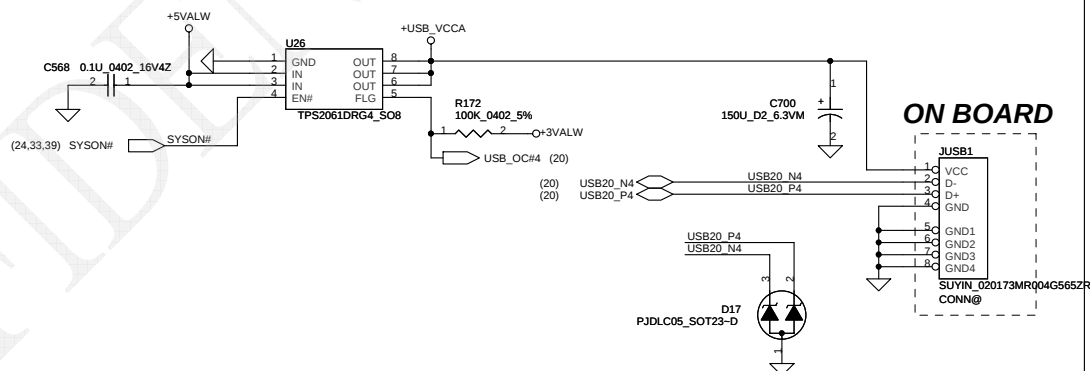
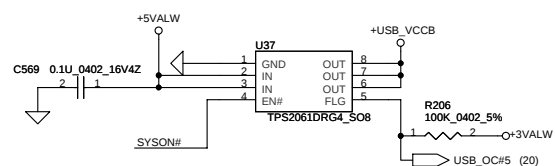
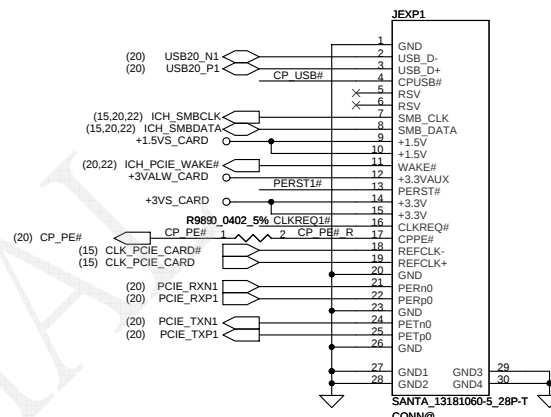


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				Custom	401556	
				Date:	Tuesday, April 29, 2008	Sheet 27 of 42

New Card Power Switch

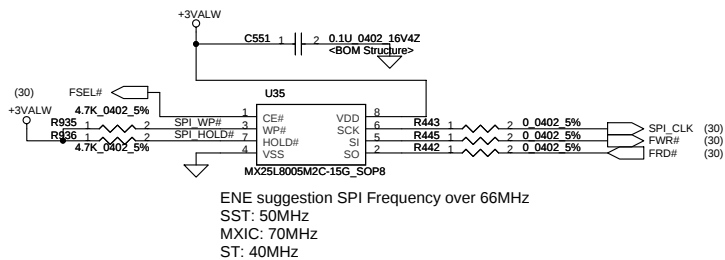


New Card Socket (Left/TOP)



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				401556	
Date: Tuesday, April 29, 2008				Sheet 28	of 42

BIOS

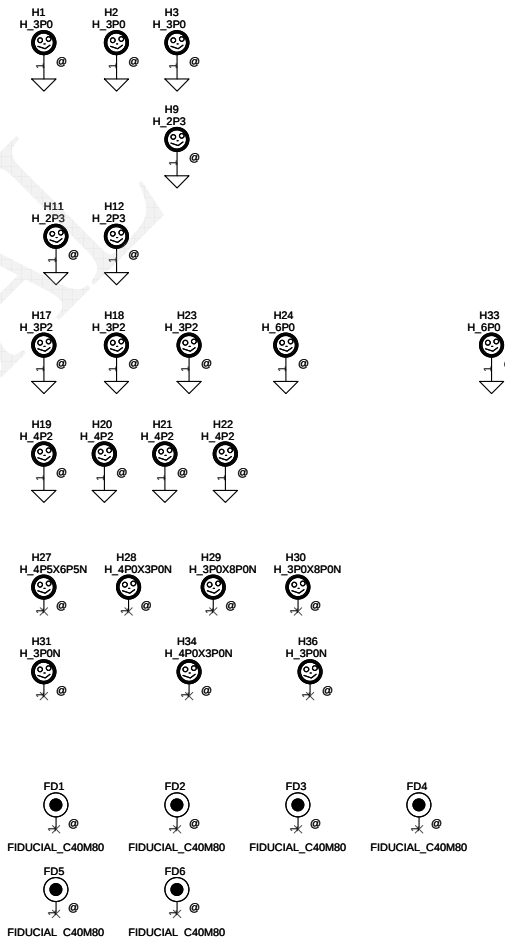
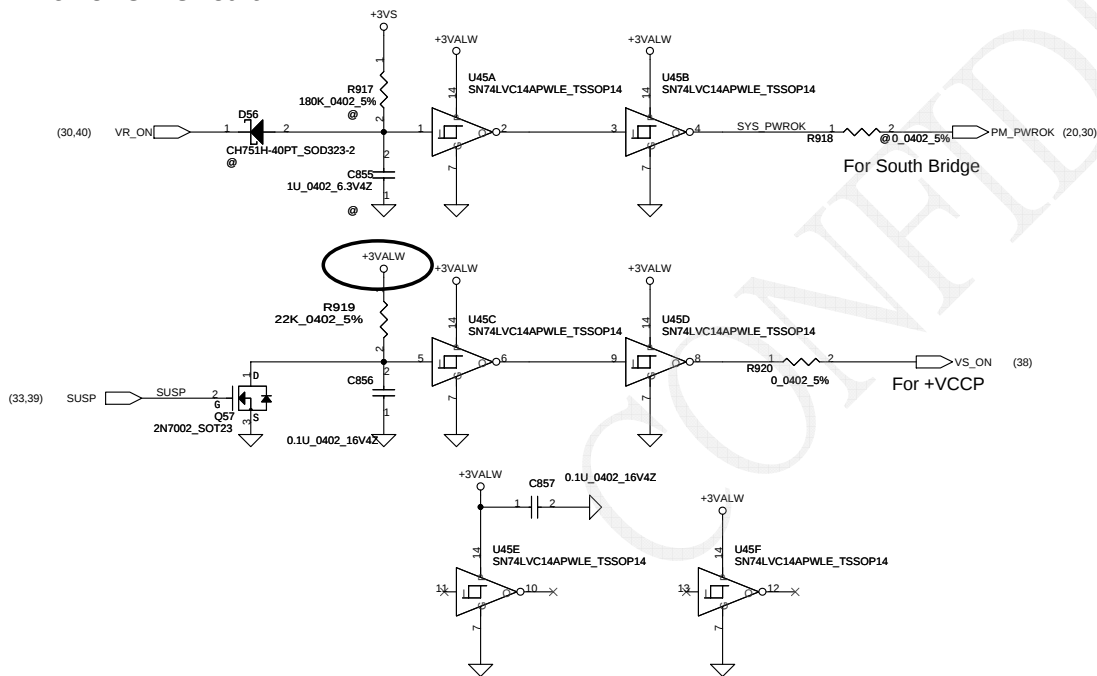


2007/12/07

reserve

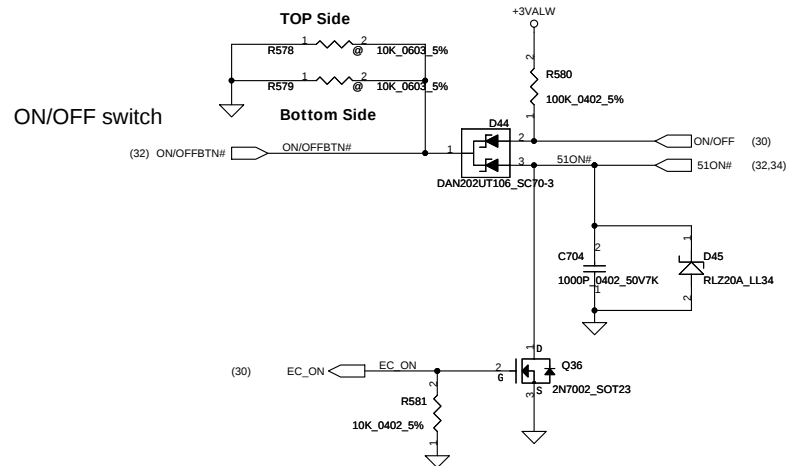
VS_ON will be driven by EC

Power ON Circuit

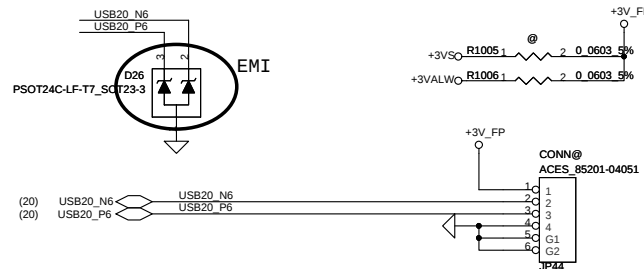


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				Date	Tuesday, April 29, 2008
				Sheet	29 of 42

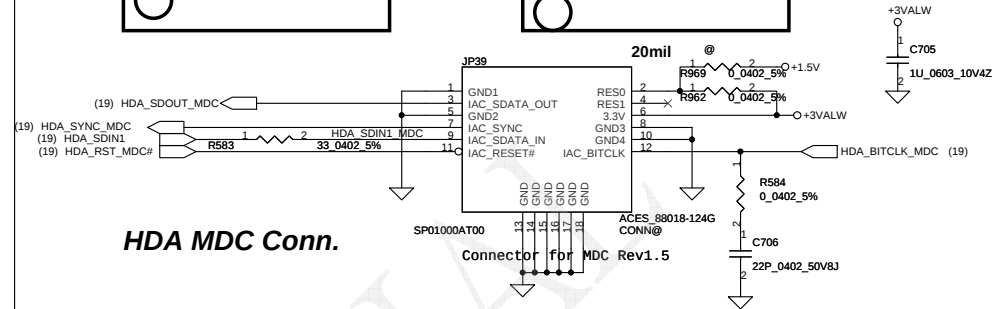
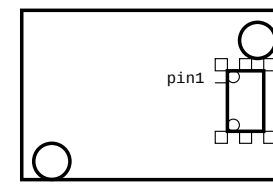
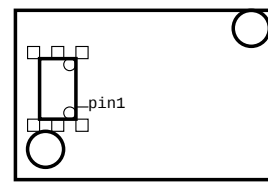
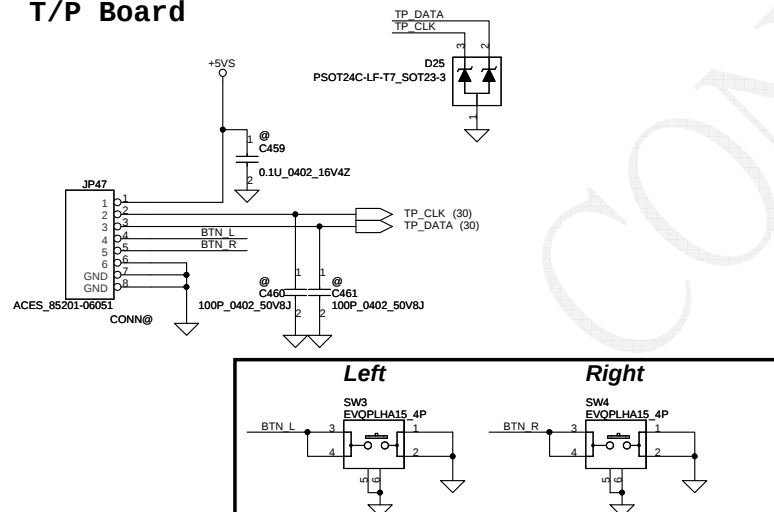
Power Button



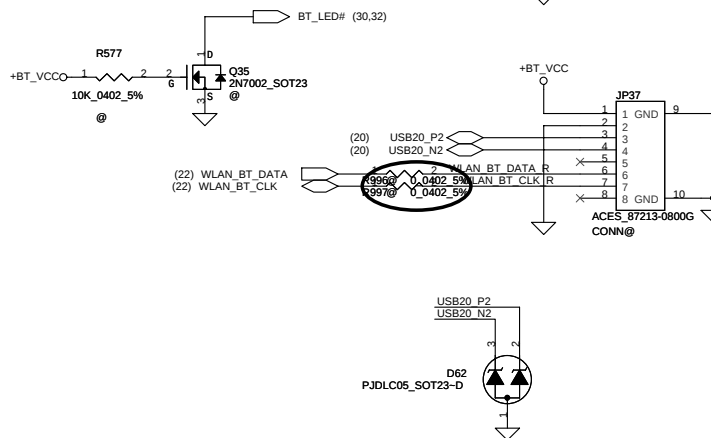
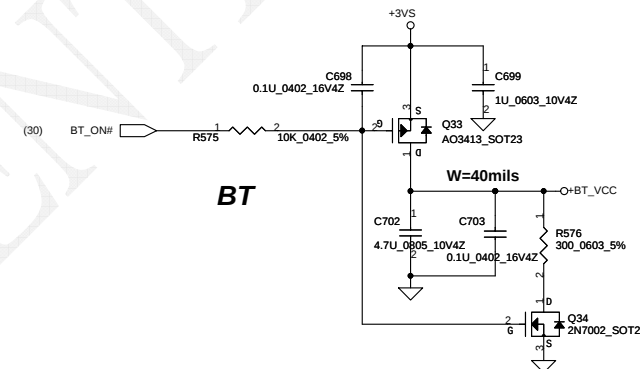
Finger Print Conn



T/P Board

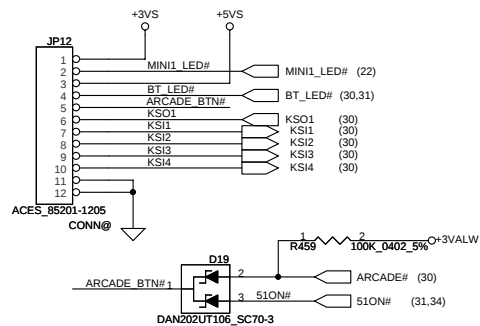


HDA MDC Conn.



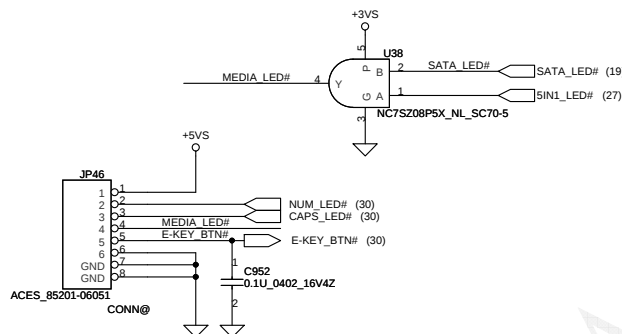
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					401556	B
				Date:	Tuesday, April 29, 2008	Sheet 31 of 42

TO S/W B

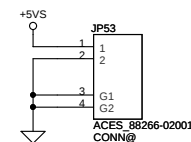
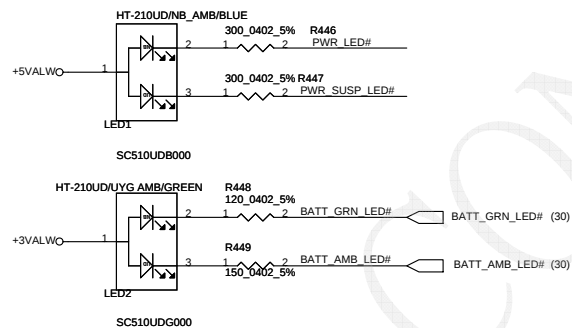
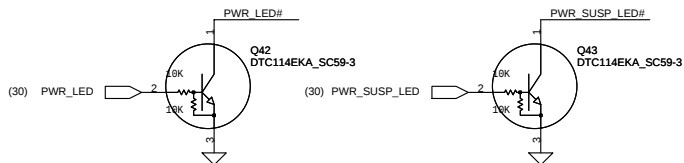
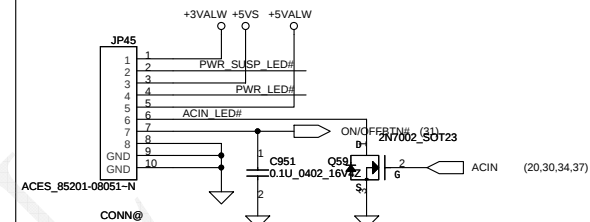


	KSO1
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#

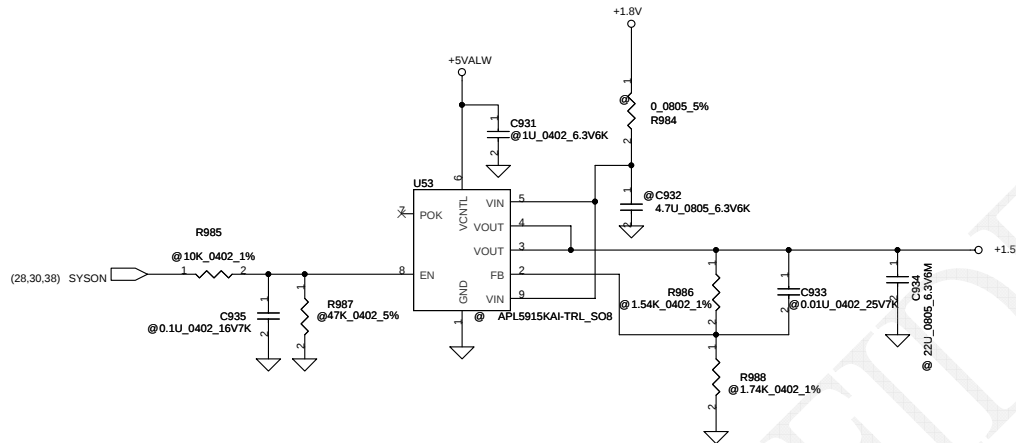
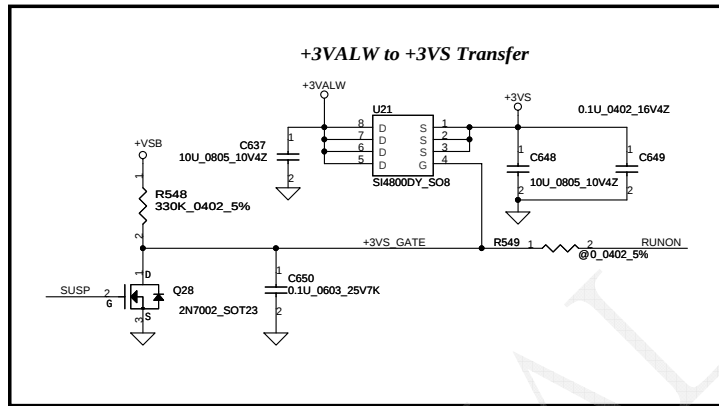
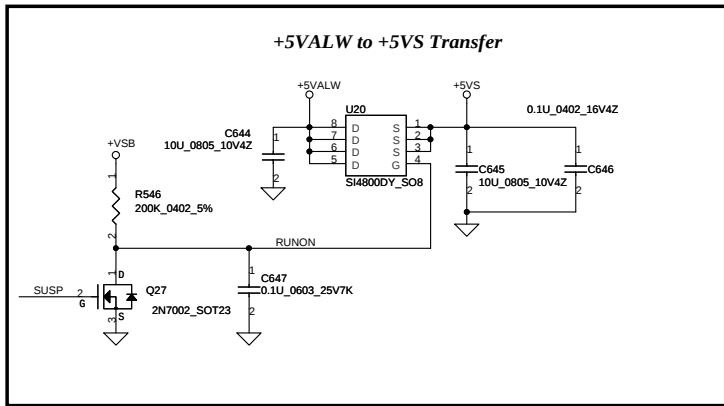
LED & E-BTN/B



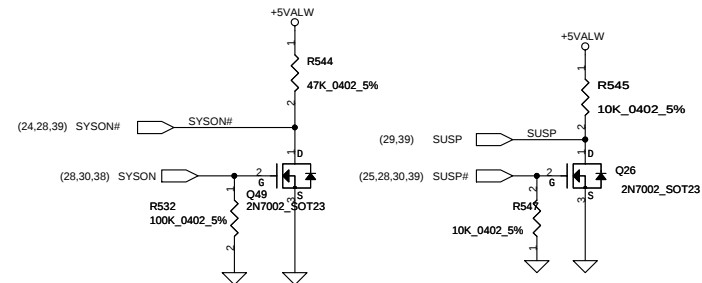
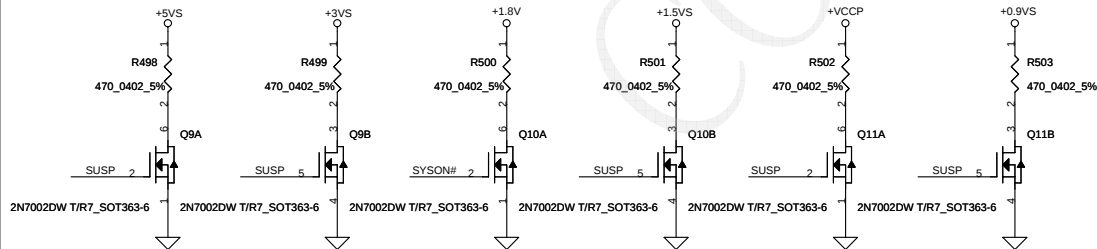
TO POWER BTN/B



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				401556
				Rev B
				Date: Tuesday, April 29, 2008
				Sheet 32 of 42



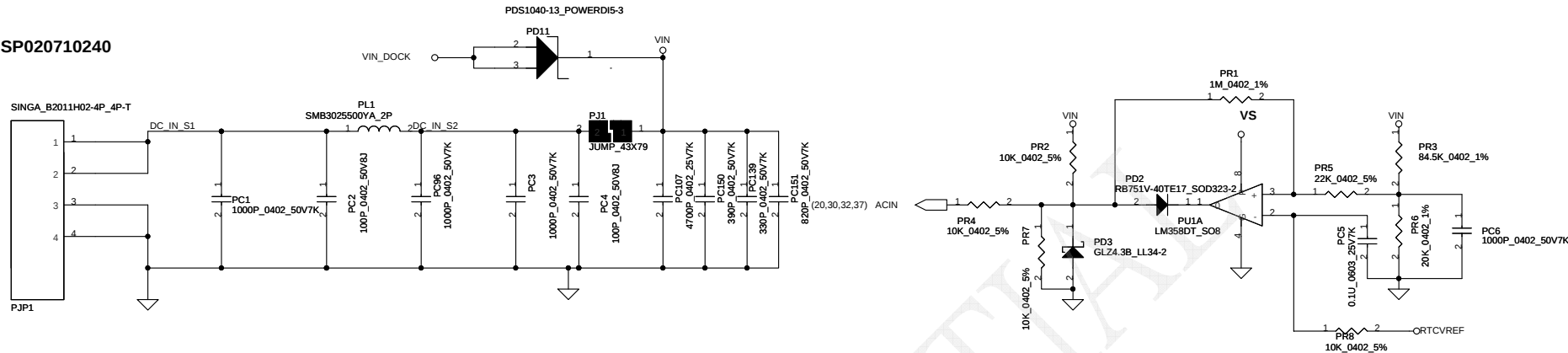
Discharge circuit



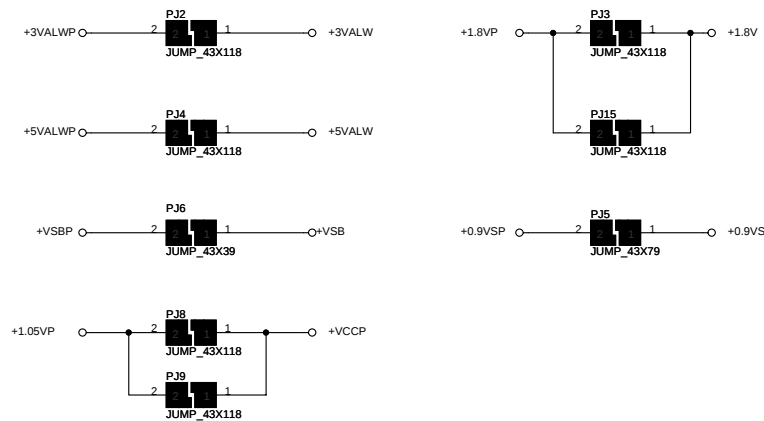
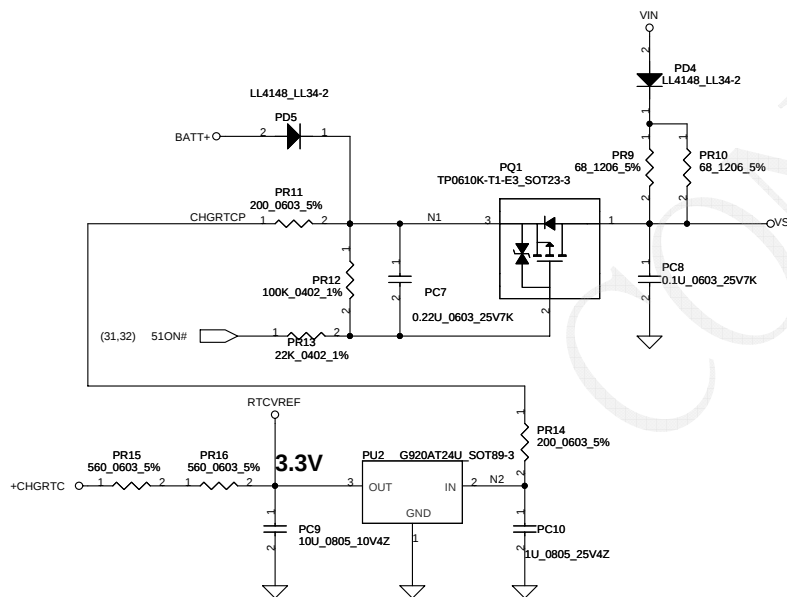
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Date: Tuesday, April 29, 2008				Sheet	33 of 42

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SCHEMATICS, MB A4271

SP020710240

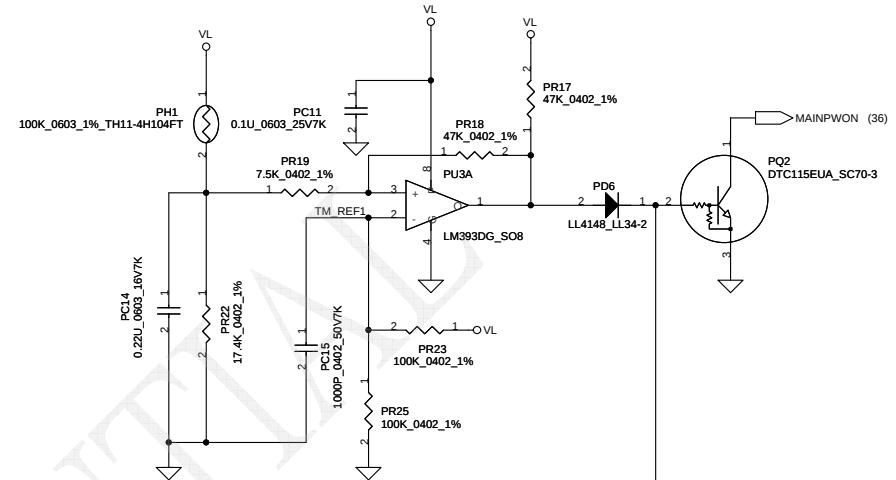
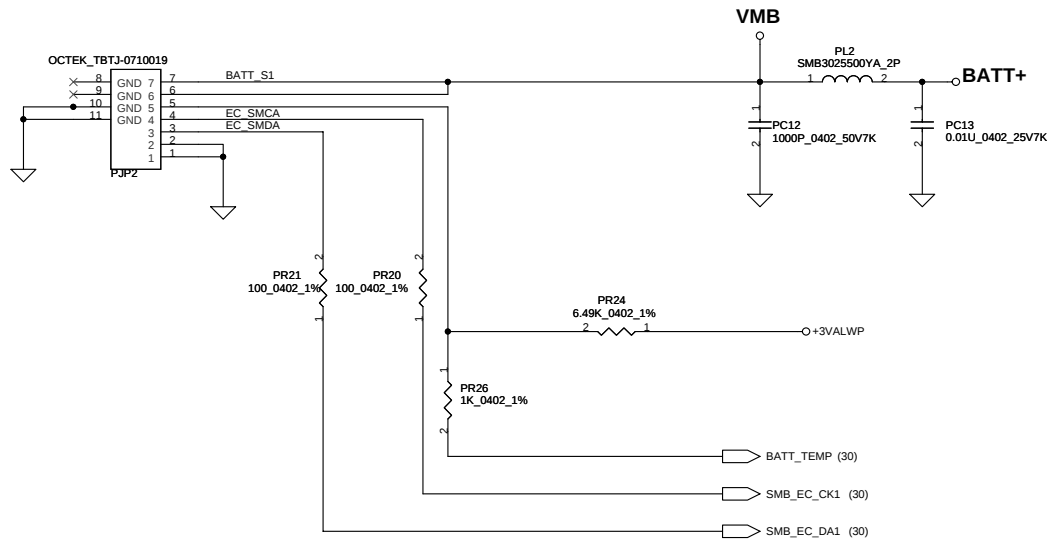


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

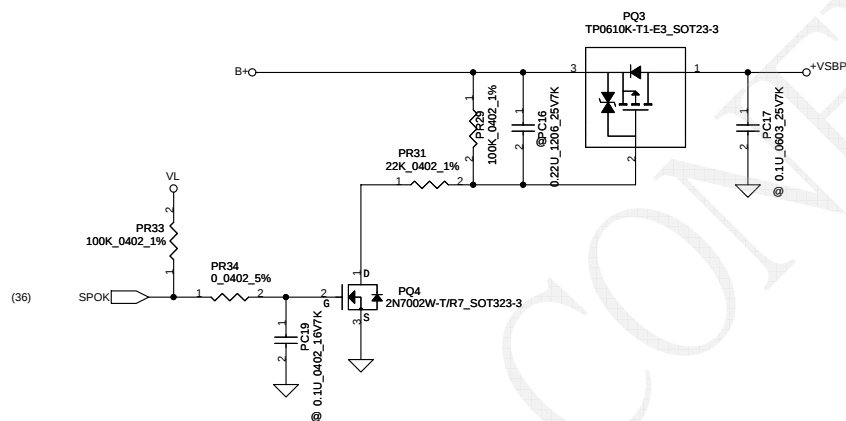
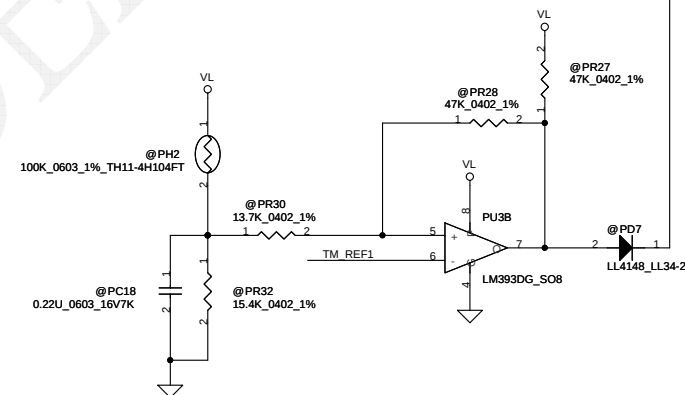


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				Date:	Tuesday, April 29, 2008
				Sheet	34 of 42
				Rev	8

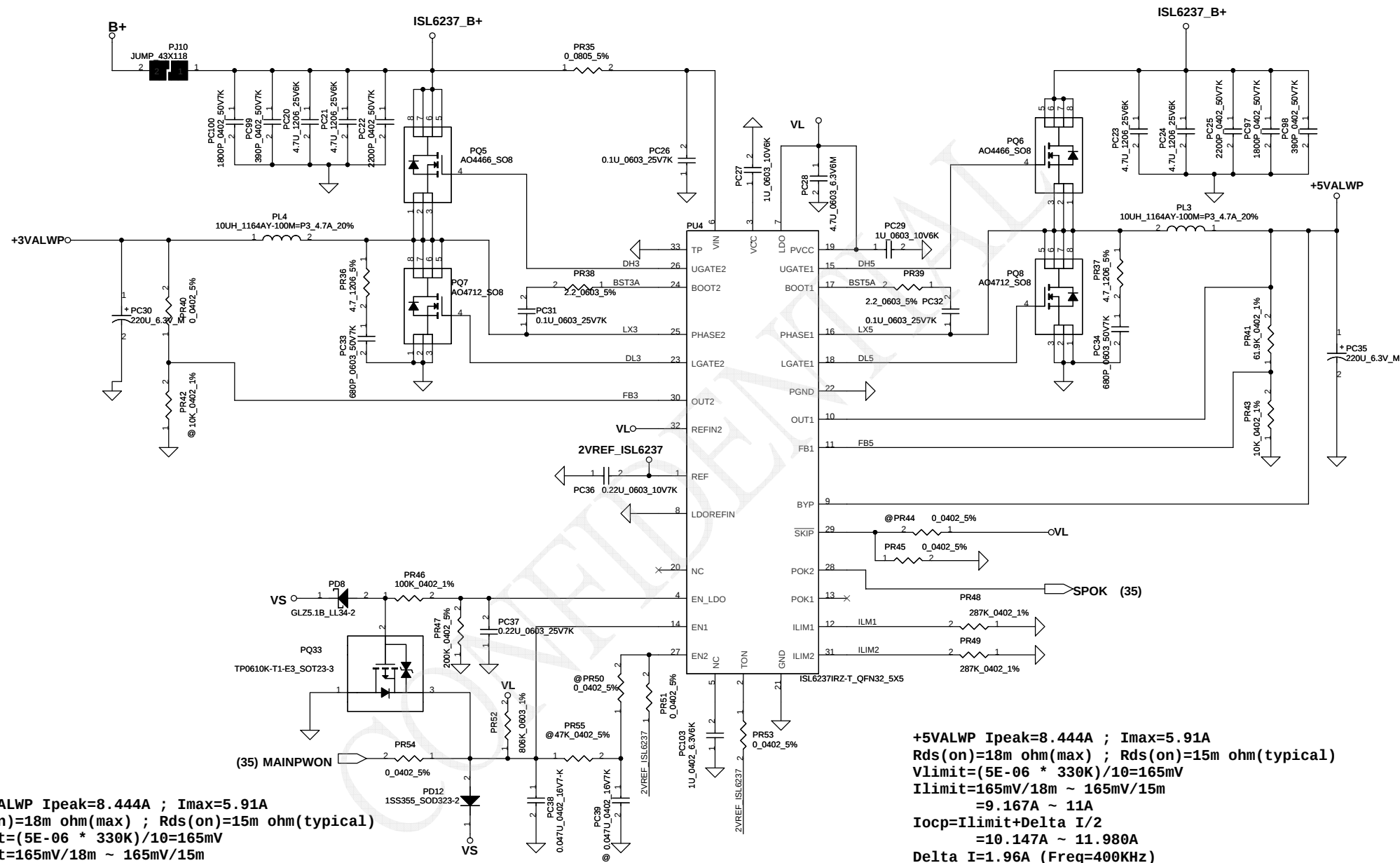
PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 56 degree C



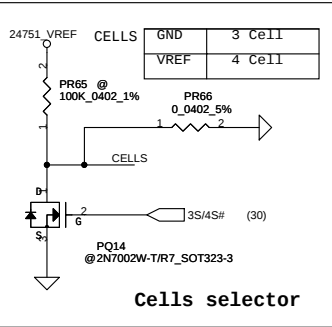
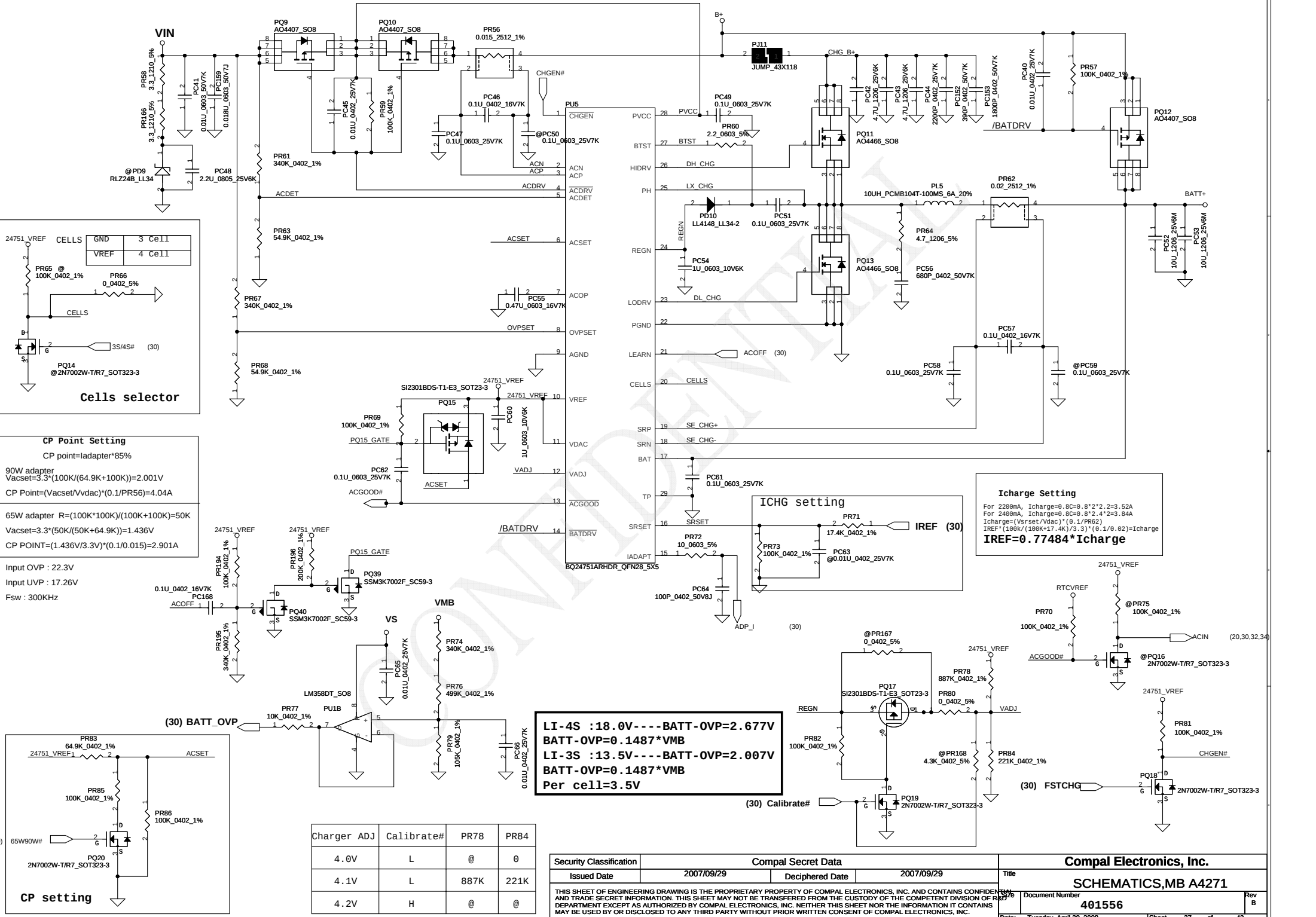
PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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				Date	Tuesday, April 29, 2008
				Sheet	35 of 42



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				Document Number	401556
				Date	Wednesday, April 30, 2008
				Sheet	36 of 42
				Rev	B



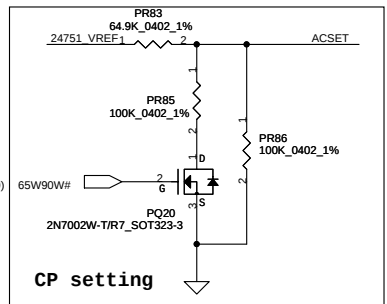
CP Point Setting

CP point=lapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
 $CP\ Point=(V_{acset}/V_{dca}) \cdot (0.1/PR56)=4.04A$

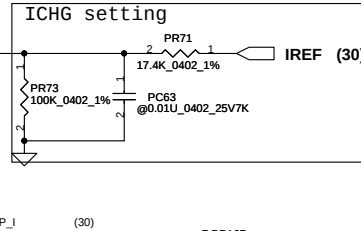
65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
 $CP\ POINT=(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	0
4.1V	L	887K	221K
4.2V	H	@	@

LI-4S : 18.0V --- BATT-OVP=2.677V
BATT-OVP=0.1487*VMB
LI-3S : 13.5V --- BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V

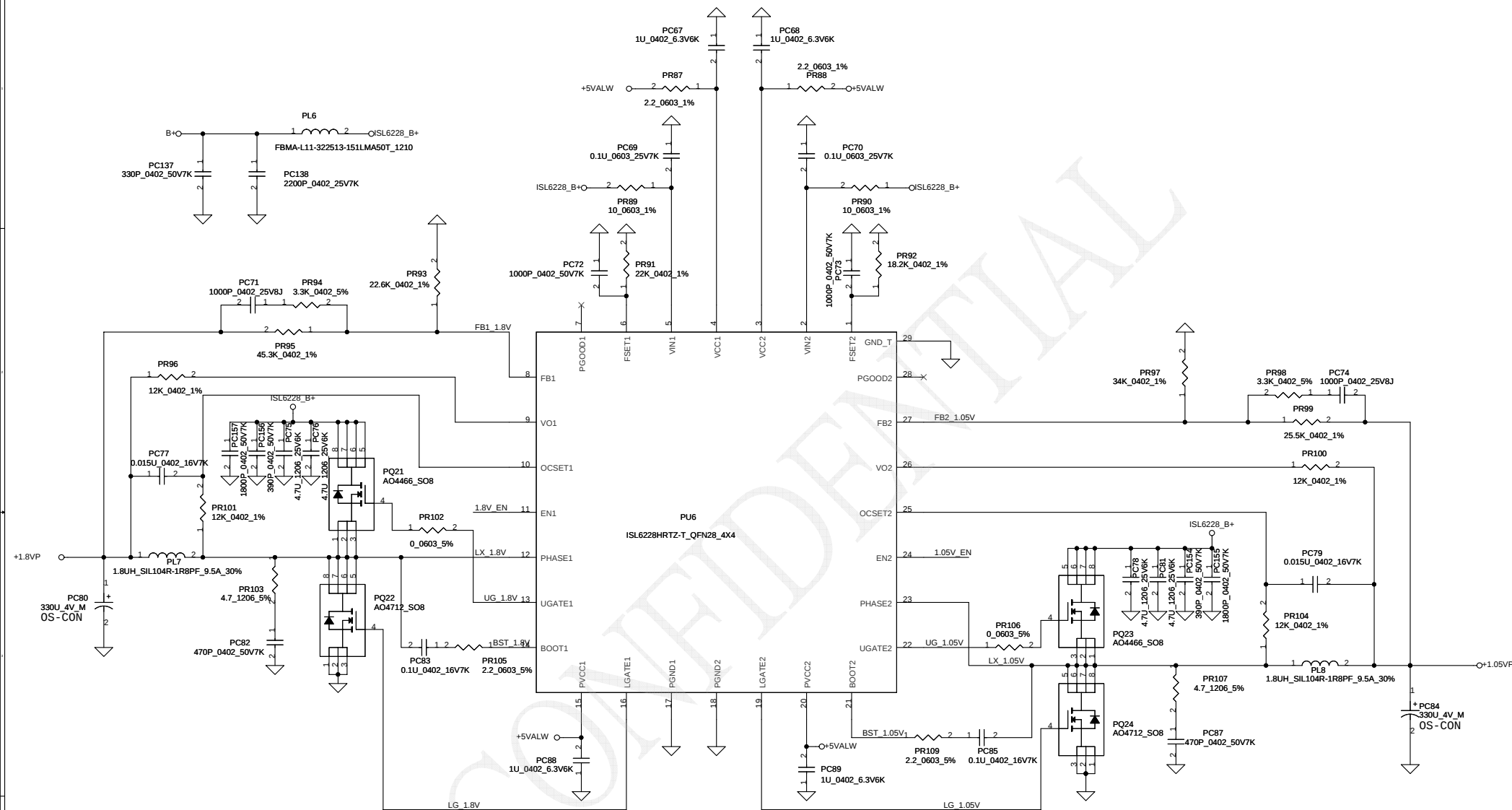


Icharge Setting

For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
For 2400mA, Icharge=0.8C=0.8*2.4*2=3.84A
 $I_{charge}=(V_{srset}/V_{dca}) \cdot (0.1/PR62)$
 $IREF=(180K/(180K+17.4K)/3.3) \cdot (0.1/0.02)=I_{charge}$
IREF=0.77484*Icharge

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SCHEMATICS, MB A4271			
Document Number	401556	Rev	B
Date:	Tuesday, April 29, 2008	Sheet	37 of 42



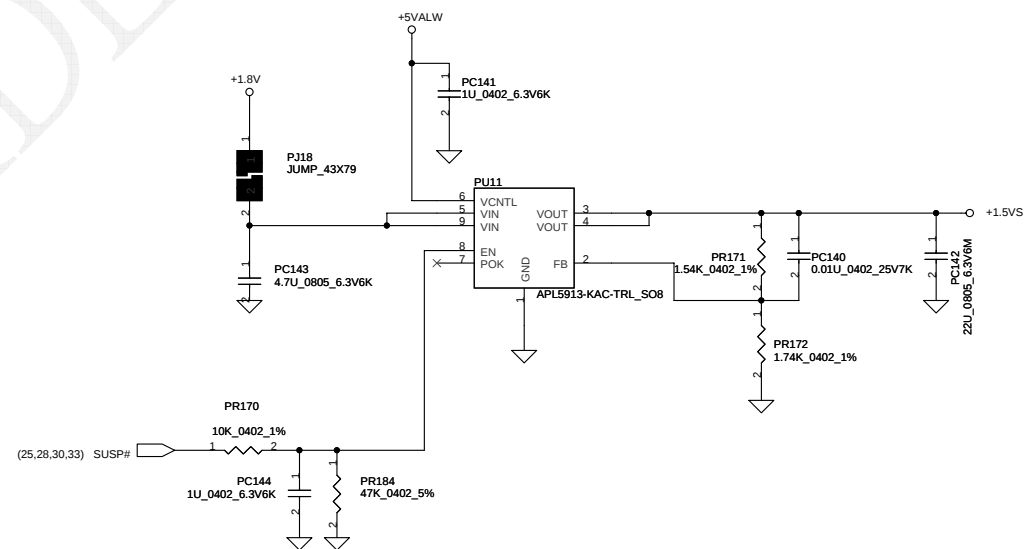
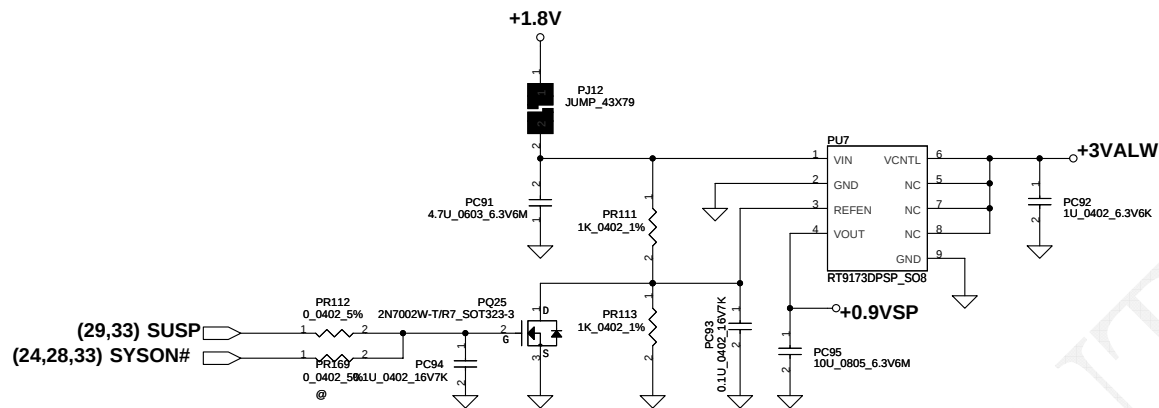
1.8VP Ipeak=9.45A ; Imax=6.615A
 DCR=10m ohm (max)
 $R_{ocset} = (I_{ocp} \cdot DCR) / (10E-06) = 12K \text{ ohm}$
 $I_{ocp} = 12A$
 $C_{sen} = L / (R_{ocset} \cdot DCR) = 0.015uF$

Freq=303KHz
 $R_{fset} = 1 / (1.5E-10 \cdot Freq) = 22K$

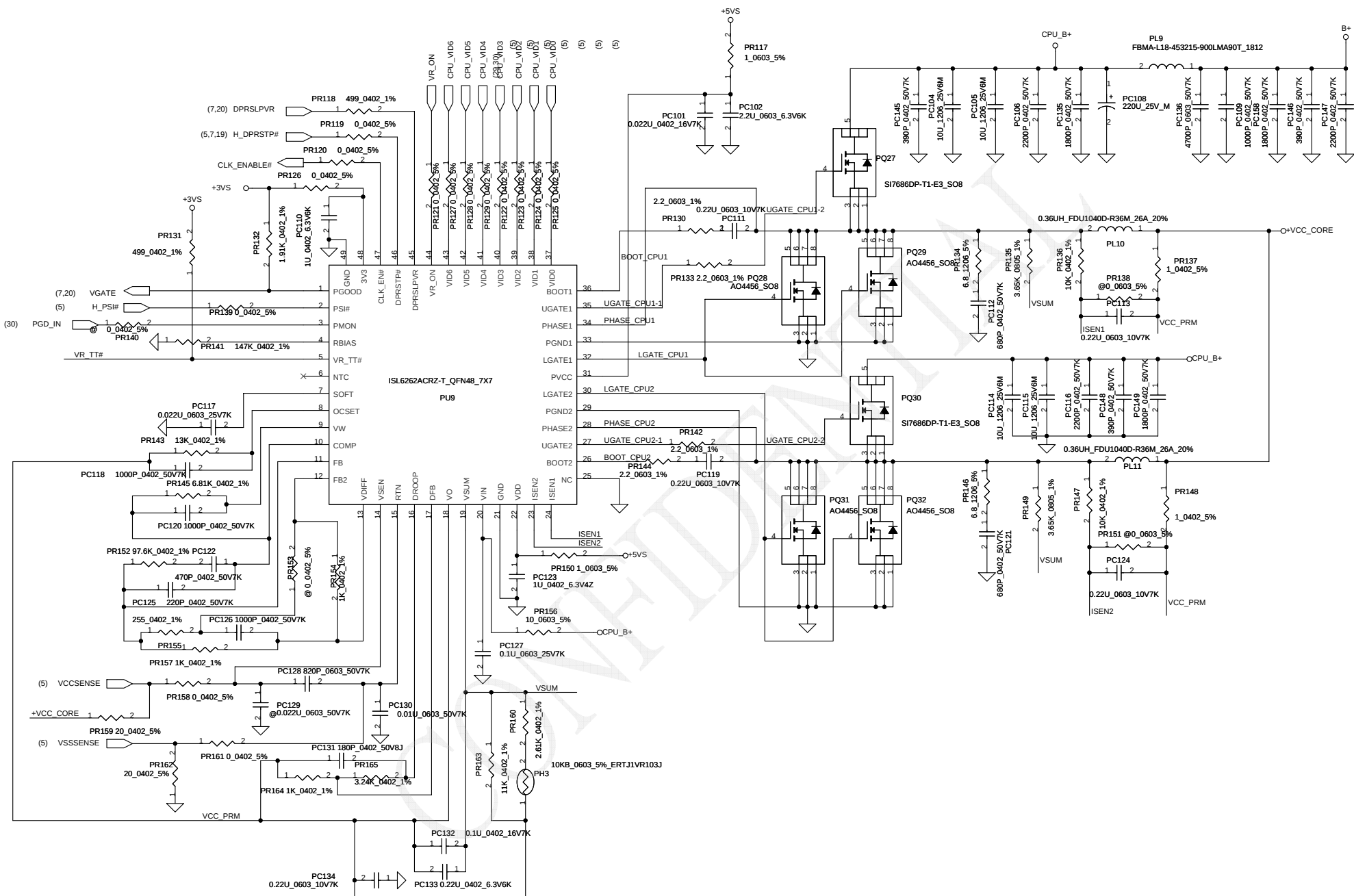
1.05VP Ipeak=8.8A ; Imax=6.16A
 DCR=10m ohm (max)
 $R_{ocset} = (I_{ocp} \cdot DCR) / (10E-06) = 12K \text{ ohm}$
 $I_{ocp} = 12A$
 $C_{sen} = L / (R_{ocset} \cdot DCR) = 0.015uF$

Freq=366KHz
 $R_{fset} = 1 / (1.5E-10 \cdot Freq) = 18.2K$

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				401556	B
Date: Wednesday, April 30, 2008				Sheet	42



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						Document Number		401556		Rev B	
						Date: Wednesday, April 30, 2008		Sheet 39 of 42			



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Date: Wednesday, April 30, 2008					Sheet 40 of 42

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Exchange battery connector pin	Use wrong model		35	Swap pin definition of PJP2	2007 12/12	EVT
2		For 2nd source of ISL6237		36	Add PC103 SE107105M80(S CER CAP 1U 6.3V M X5R 0603) on pin 5 of PU4	2007 12/12	EVT
3		Some risk in heavy load		37	Change PL5 to SH000005Z80(S COIL 10UH +-20% PCMB104T-100MS 6A)	2007 12/12	EVT
4		For EN function of PU4		36	Add PD12 SC100001K00(S DIO 1S355 SOD323 T/R-5K) on pin 3 of PQ33 to VS	2007 12/12	EVT
5		Down size		36	Change PC38 from 0603 to 0402(SE076473K80)	2007 12/12	EVT
6		Down size		34	Change PC7 from 1206 to 0603(SE000005Z80)	2007 12/12	EVT
7		Down size		37	Change PC49 from 0805 to 0603(SE042104K80)	2007 12/12	EVT
8		Down size		36	Change PC28 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
9		Down size		39	Change PC91 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
10		Down size		39	Change PC96 from 0805 to 0603(SE107475M80)	2007 12/12	EVT
11		Down size		39	Change PC92 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
12		Down size		39	Change PC97 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
13		Down size		40	Change PC110 from 0603 to 0402(SE000000K80)	2007 12/12	EVT
14		Down size		35	Change PC14 from 0805 to 0603(SE026224K80)	2007 12/12	EVT
15		Down size		35	Change PC18 from 0805 to 0603(SE026224K80)	2007 12/12	EVT
16		For EMI		34	Add PC107 SE075472K80(S CER CAP 4700P 25V K X7R 0402) from VIN to GND	2007 12/12	EVT
17		For EMI		34	Add PC139 SE074331K80(S CER CAP 330P 50V K X7R 0402) from VIN to GND	2007 12/12	EVT
18		For EMI		40	Add PC135 SE074182K80(S CER CAP 1800P 50V K X7R 0402) from CPU_B+ to GND	2007 12/12	EVT
19		For EMI		40	Add PC136 SE025472K80(S CER CAP 4700P 50V K X7R 0603) from B+ to GND	2007 12/12	EVT
20		For EMI		38	Add PR103 SD001470B80(S RES 1/4W 4.7 +-5% 1206) from pin 12 of PU6 to PC82	2007 12/12	EVT
21		For EMI		38	Add PC82 SE074471K80(S CER CAP 470P 50V K X7R 0402) from PR103 to GND	2007 12/12	EVT
22		For EMI		38	Add PR107 SD001470B80(S RES 1/4W 4.7 +-5% 1206) from pin 23 of PU6 to PC82	2007 12/12	EVT
23		For EMI		38	Add PC87 SE074471K80(S CER CAP 470P 50V K X7R 0402) from PR107 to GND	2007 12/12	EVT

Compal Electronics, Inc.

Title			SCHEMATICS,MB A4271		
Size	Document Number				Rev
	401556				B
Date:	Tuesday, April 29, 2008		Sheet	41	of 42

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
24		For more current		34	Change PD11 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/12	EVT
25		Space is not enough		34	Delete PD1	2007 12/18	EVT
26				37	Change PR70 Pin 1 to RTCVREF	2007 12/18	EVT
27		Down size		37	Change PC56 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
28		Down size		40	Change PC112 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
29		Down size		40	Change PC121 from 0603 to 0402(SE074681K80)	2007 12/18	EVT
30		Down size		36	Change PC103 from 0603 to 0402(SE000000K80)	2007 12/18	EVT
31		Down size		40	Change PC128 from 0603 to 0402(SE000003W00)	2007 12/20	EVT
32	API5913 EN pin impedance must keep under 20K	For API5913 EN risk		39	Change PR184 from 47K to 20K(SD028200280)	2007 12/31	EVT
33		Improve 3V/5V OCP		36	Change PR48 □ PR49 from 330K to 287K(SD000005D80) Change PL3 □ PL4 from 4.7uH to 10uH(SH000008R80)	2008 02/25	DVT
34		Improve Load line		40	Change PR165 from 4.42K to 3.24K(SD034324180)	2008 02/25	DVT
35		For EMI		34	Add PC96 1000pF(SE074102K80)	2008 02/25	DVT
36		For EMI			Add PC97 □ PC98 □ PC99 □ PC100 □ PC145 □ PC146 □ PC147 □ PC148 □ PC149 □ PC150 □ PC151 □ PC152 □ PC153 □ PC154 □ PC155 □ PC156 □ PC157 Delete PR64 □ PC56 "@"-mark Change PR38 □ PR39 □ PR60 □ PR105 □ PR109 □ PR130 □ PR144 from 0 to 2.2	2008 02/27	DVT
37							
38		Prevent ACOP issue		37	Add PC168 □ PQ39 □ PQ40 □ PR194 □ PR195 □ PR196	2008 02/27	DVT
39		HW request		39	Change PC144 to 1uF , delete PR184 "@" mark	2008 02/27	DVT
40		For EMI			Add PC158 □ PC159	2008 03/03	DVT
41		Thermal request		35	Change PR19 from 13.7K to 7.5K (SD034750180) Change PR22 from 15.4K to 17.4K (SD034174280)	2008 03/14	PVT1
42							
43							
44							
45							
46							

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Title			SCHEMATICS,MB A4271
Size	Document Number	401556	
Date:		Tuesday, April 29, 2008	Sheet 42 of 42
			Rev B