

ZZZ8
DAZ@
DAZ04300100
PCB

ZZZ1
DA2@
MAIN BOARD
DA600007E10
PCB

ZZZ2
DA2@
E board
DA40000A910
PCB

ZZZ3
DA2@
FP board
DA600007D10
PCB

ZZZ4
DA2@
Function board
DA40000AA10
PCB

ZZZ5
DA2@
USB board
DA40000AB10
PCB

ZZZ6
DA2@
IO board
DA40000AC10
PCB

ZZZ7
DA2@
Power board
DA40000AD10
PCB

Compal Confidential

KAQB0 M/B Schematics Document

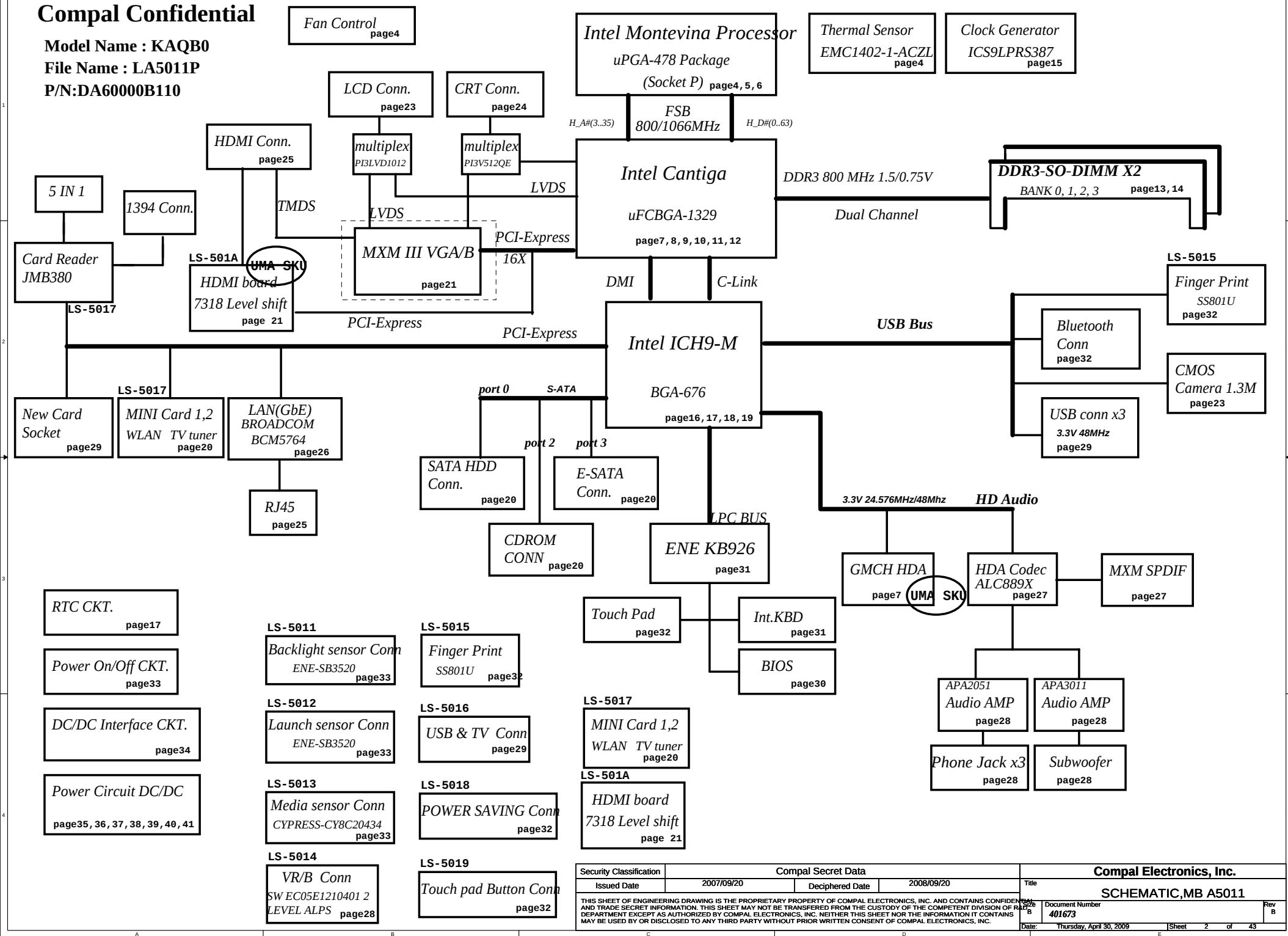
Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-27

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	SCHEMATIC,MB A5011
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Model Name : KAQB0
File Name : LA5011P
P/N:DA60000B110



power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

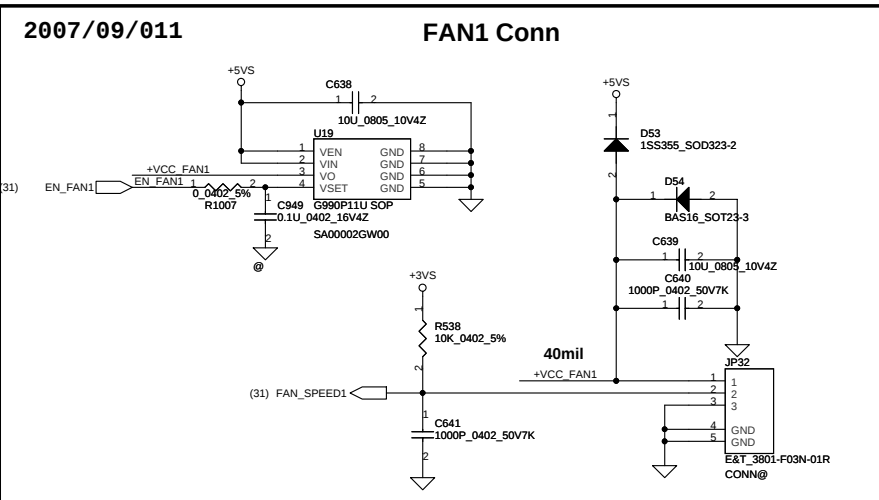
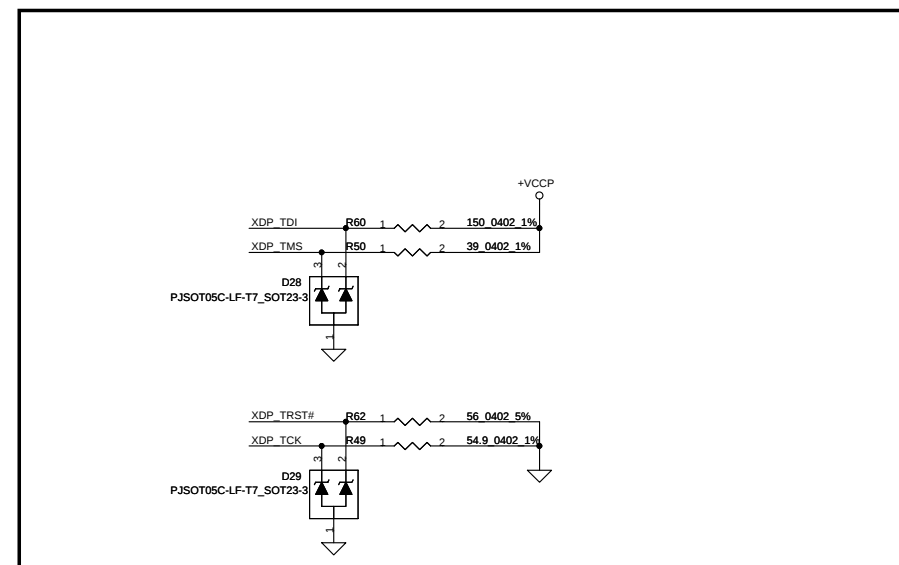
@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

SMBUS Control Table

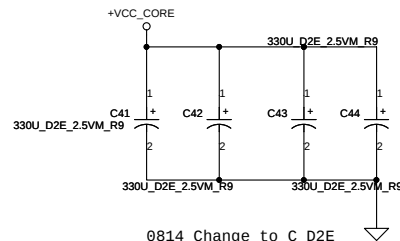
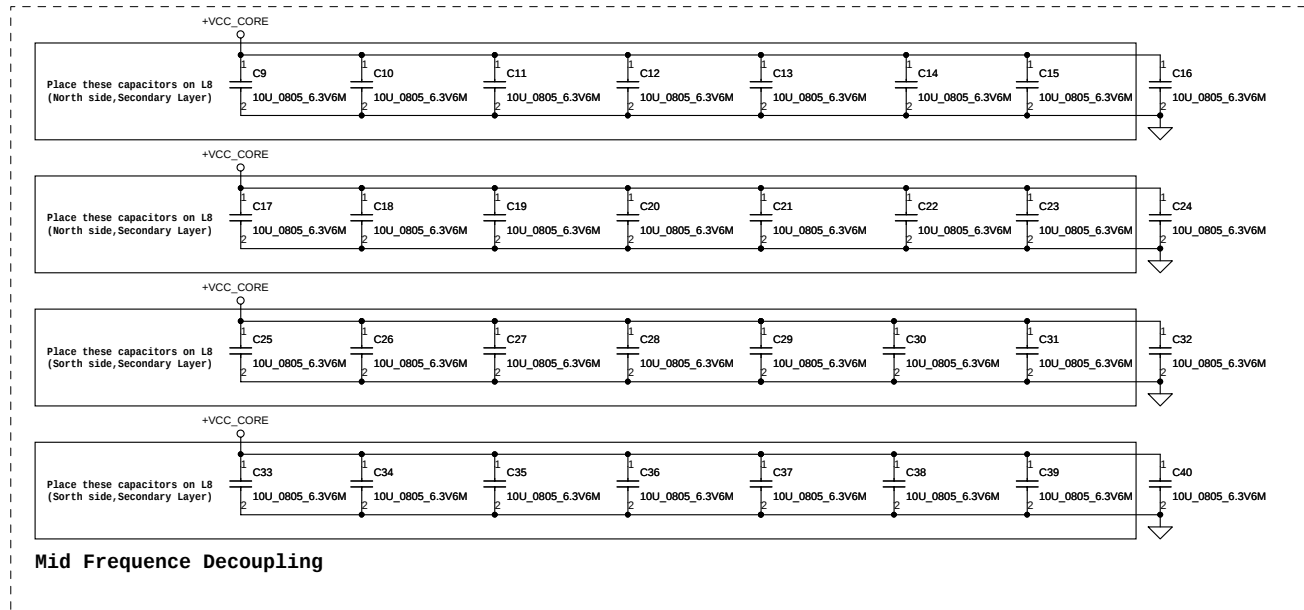
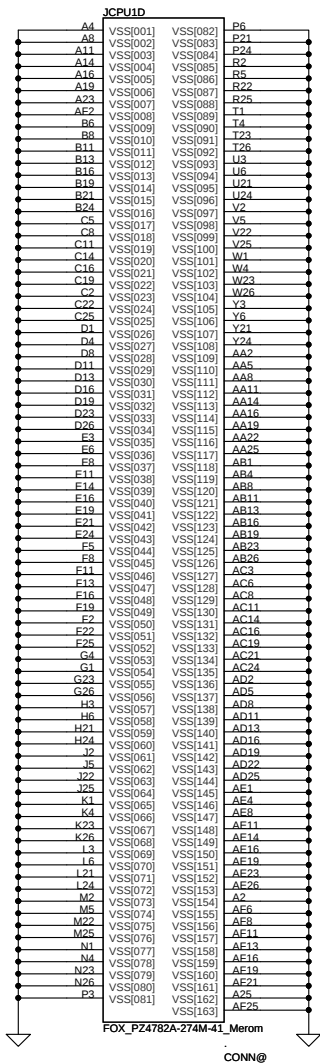
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

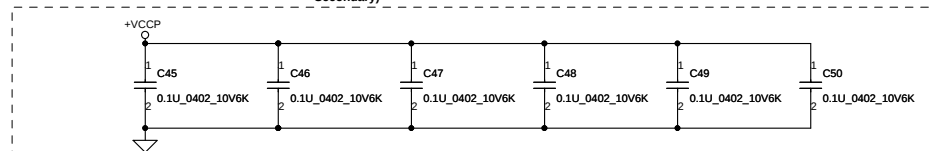
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0



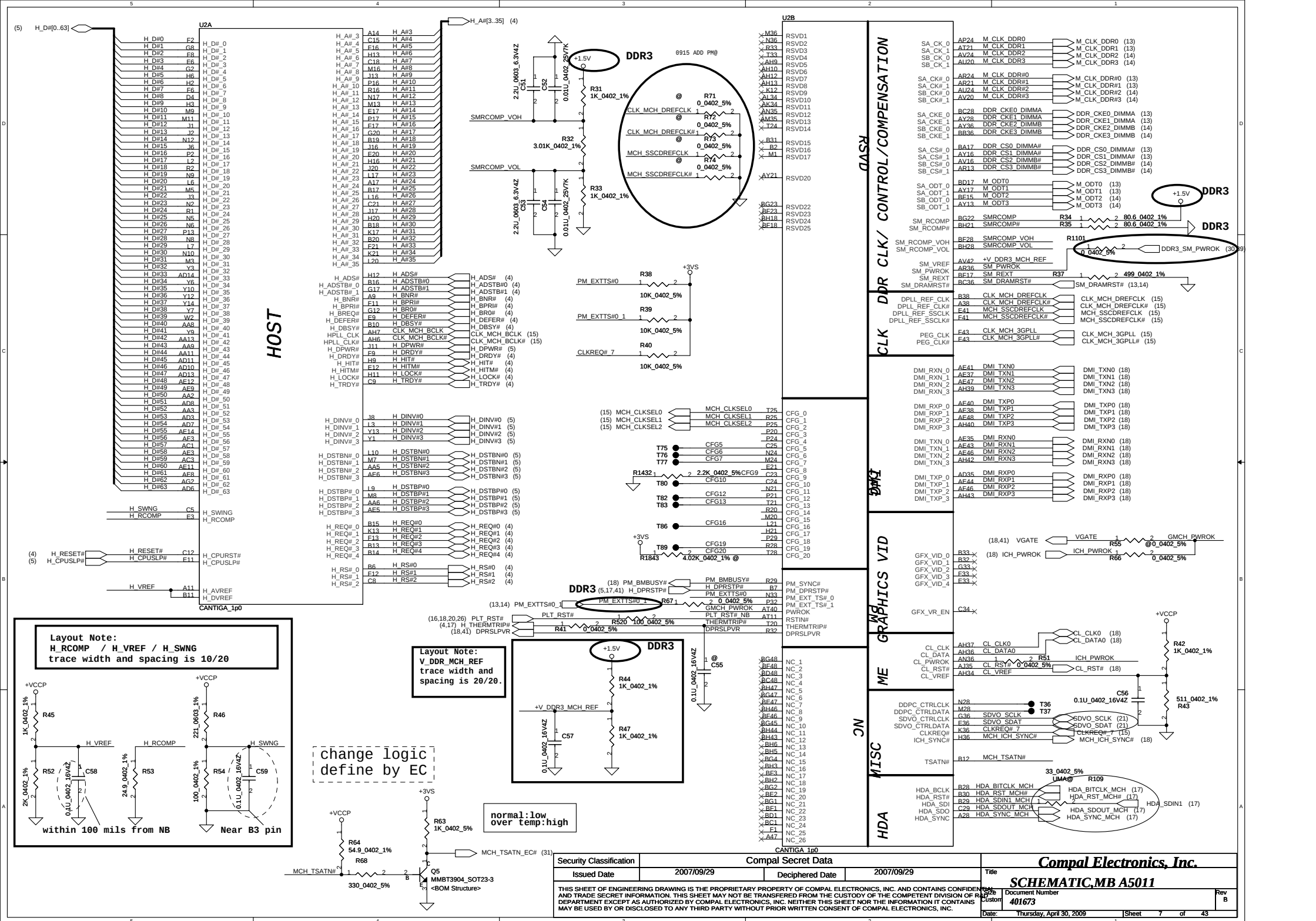
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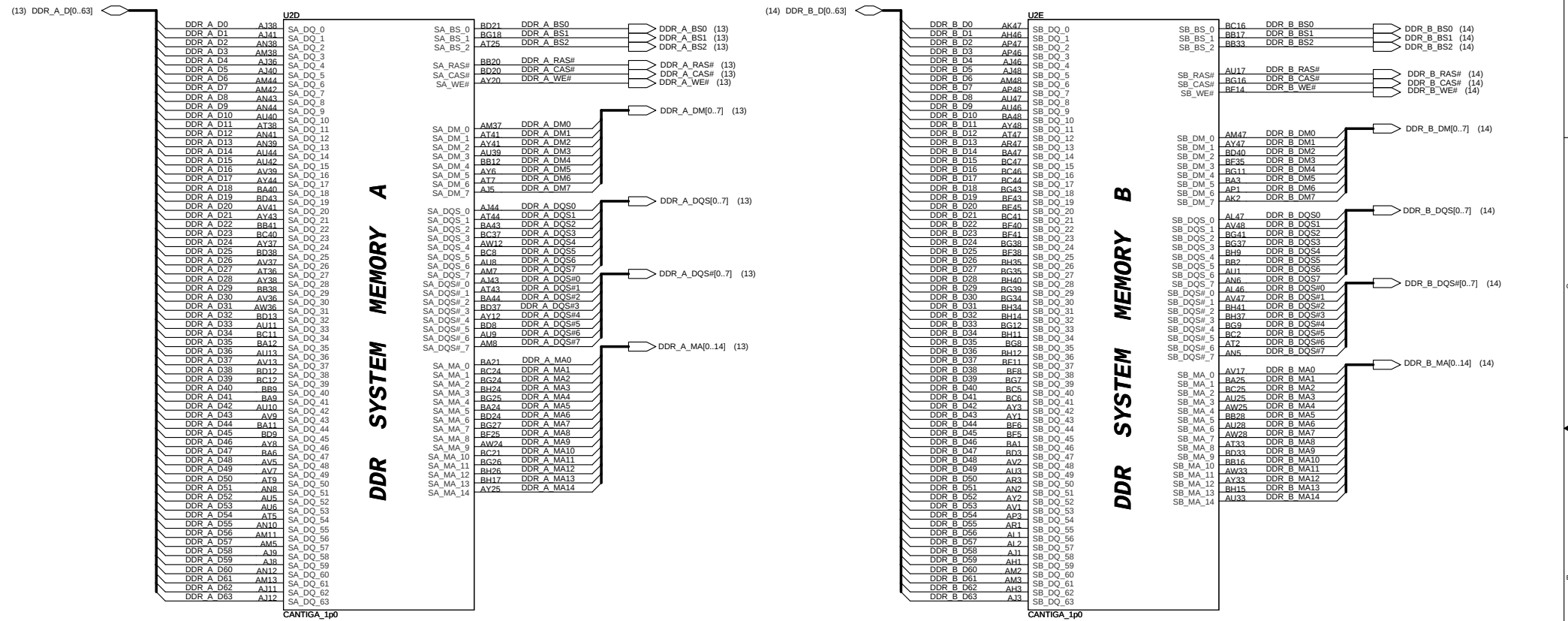


Place these inside
socket cavity on L8
(North side
Secondary)

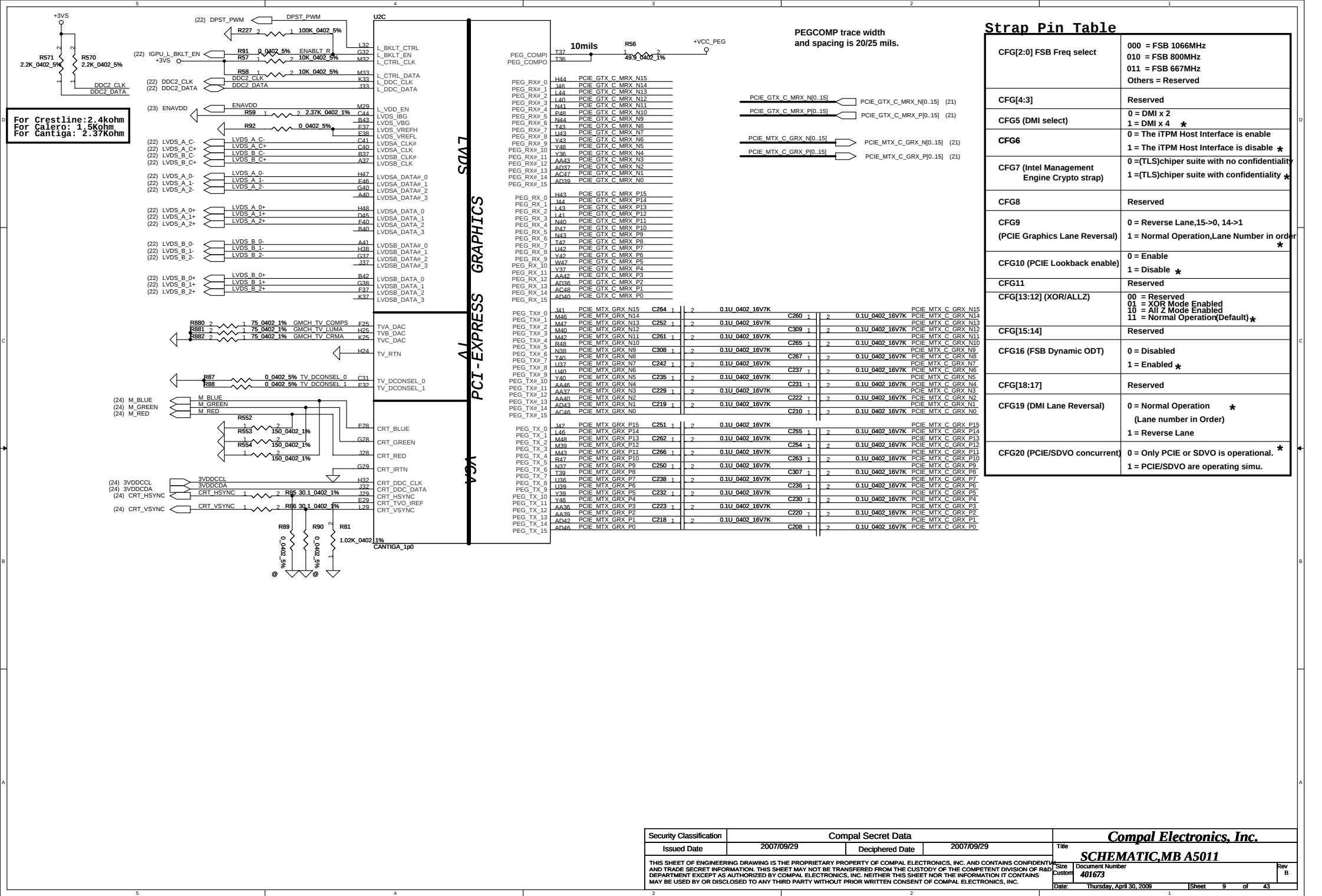


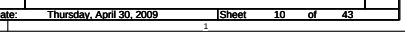
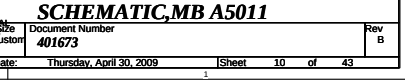
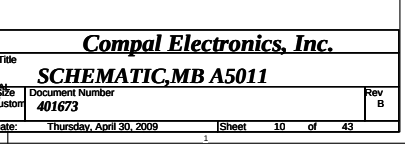
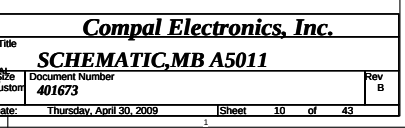
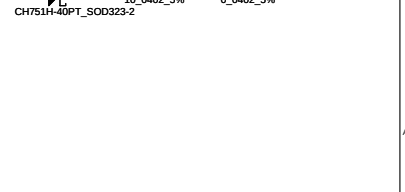
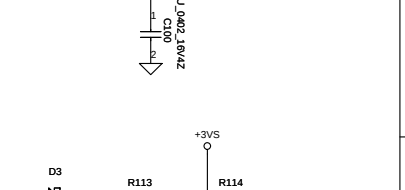
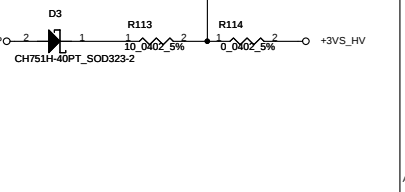
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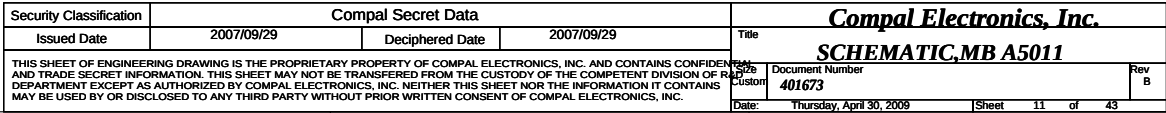


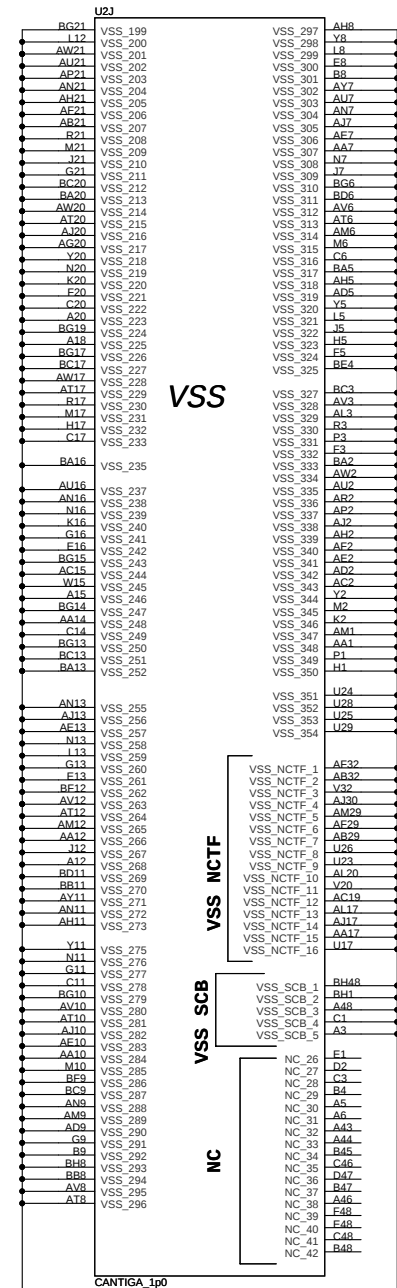
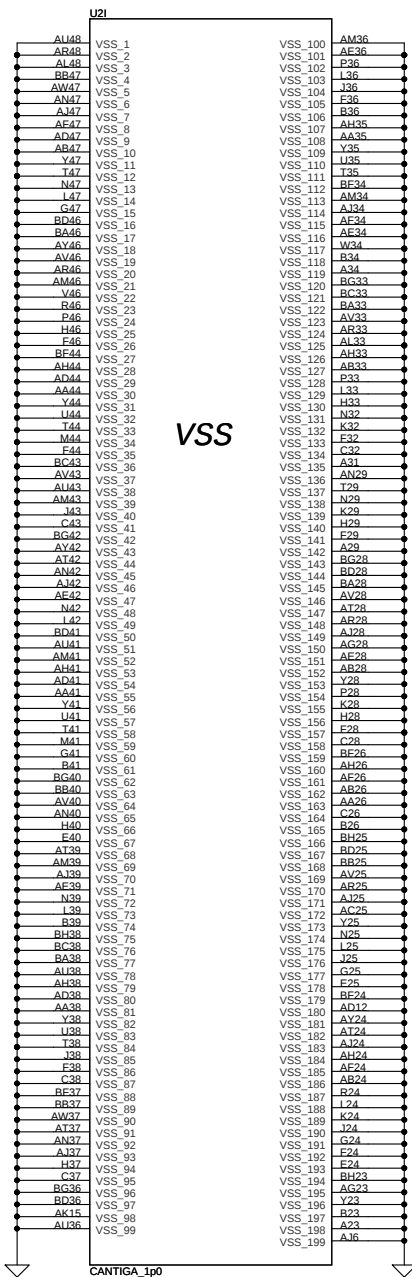
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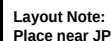
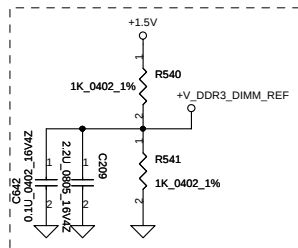


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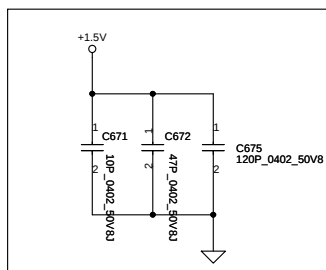
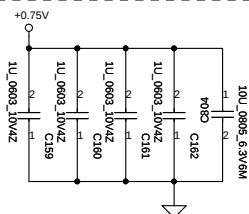




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[illegible]

Layout Note:
Place near JP4.203 & JP4.204

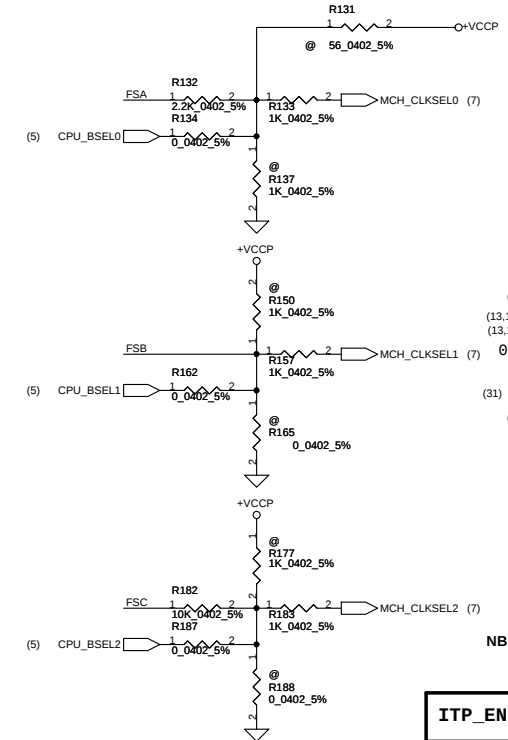
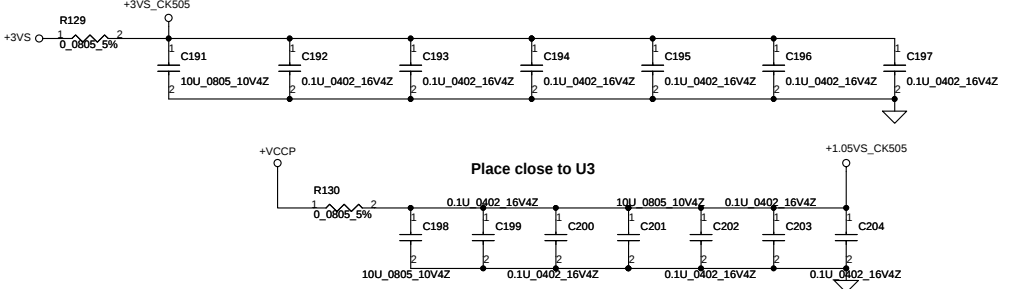
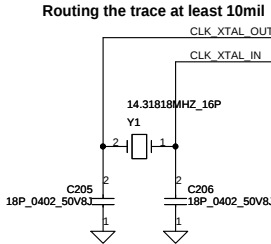


DDR3 SO-DIMM A REVERSE

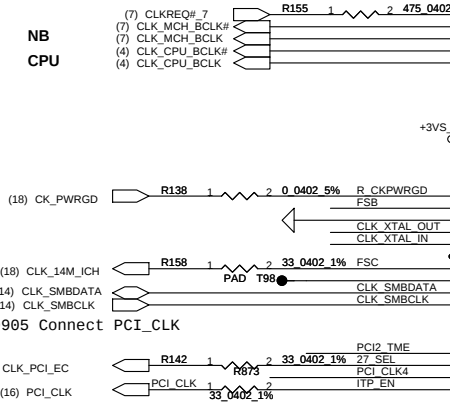
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

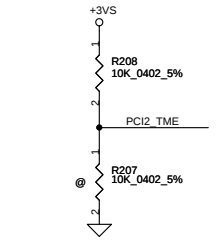
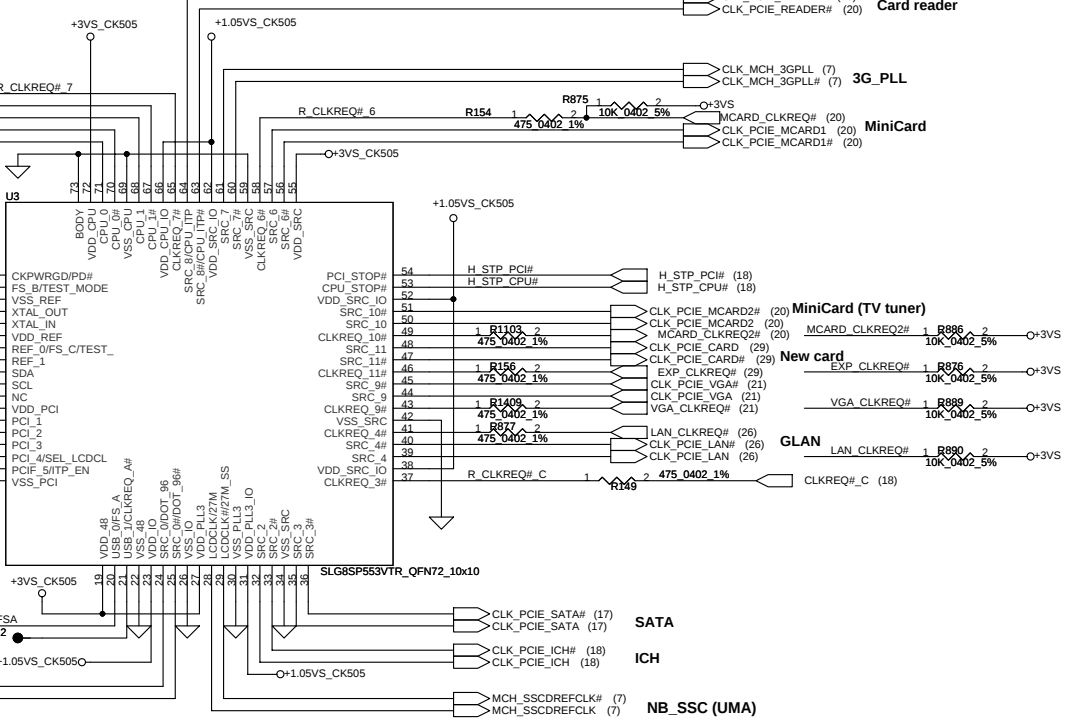


NB
CPU



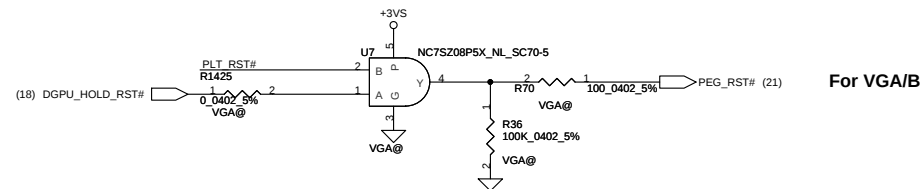
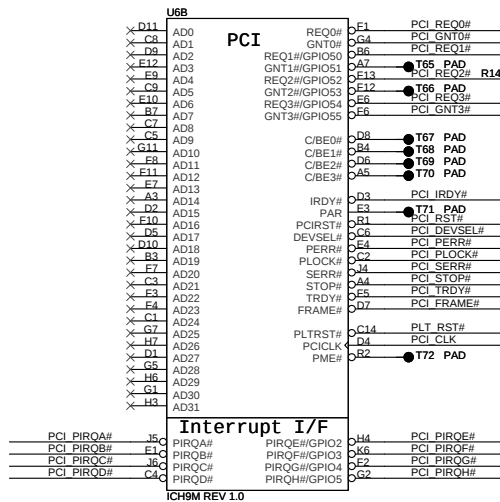
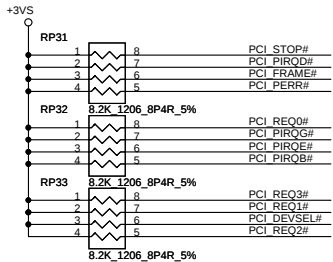
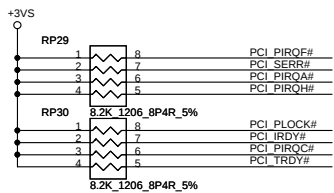
NB (UMA)

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

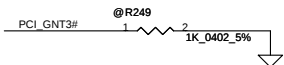


for ICS Overclocking setting
0=Overclocking of CPU and SRC allowed
1=Overclocking of CPU and SRC NOT allowed

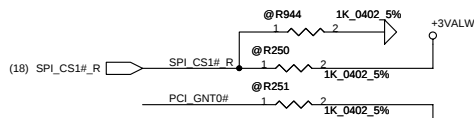
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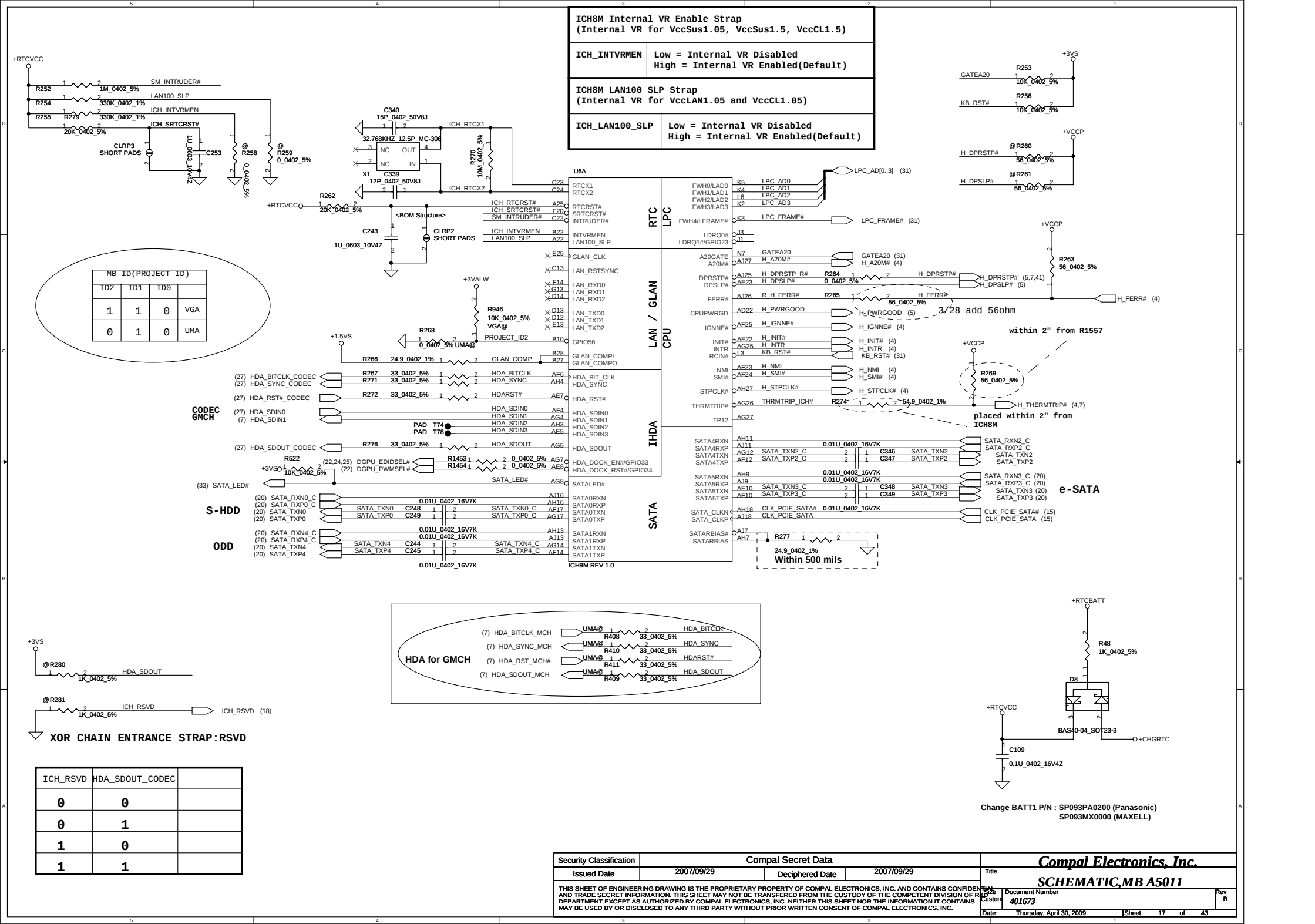


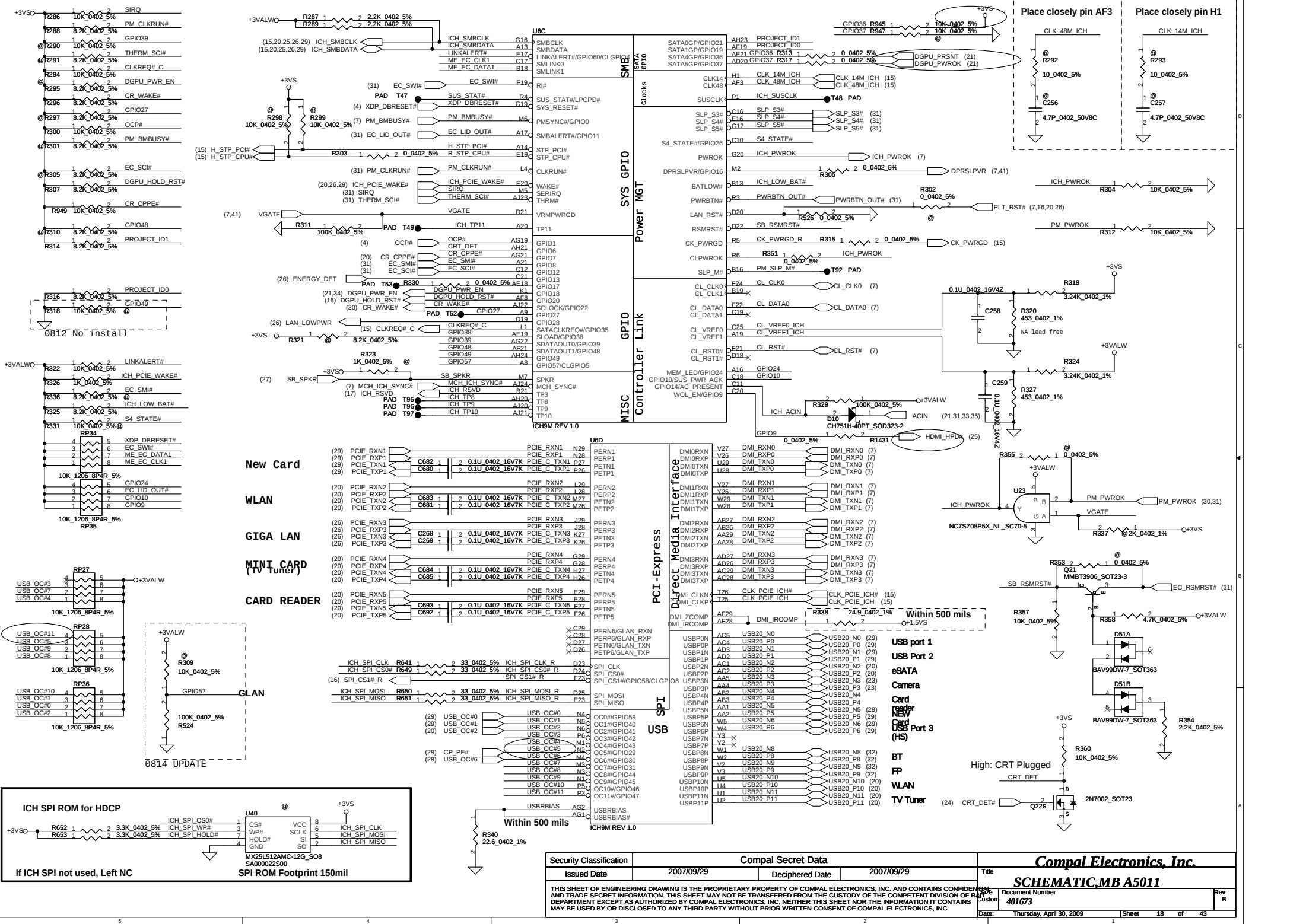
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



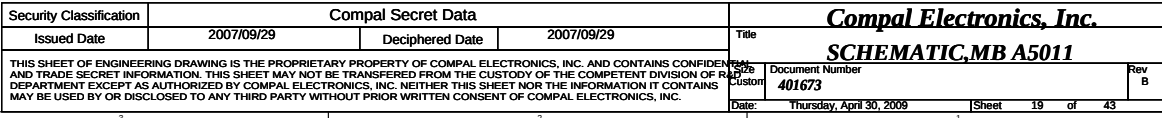
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

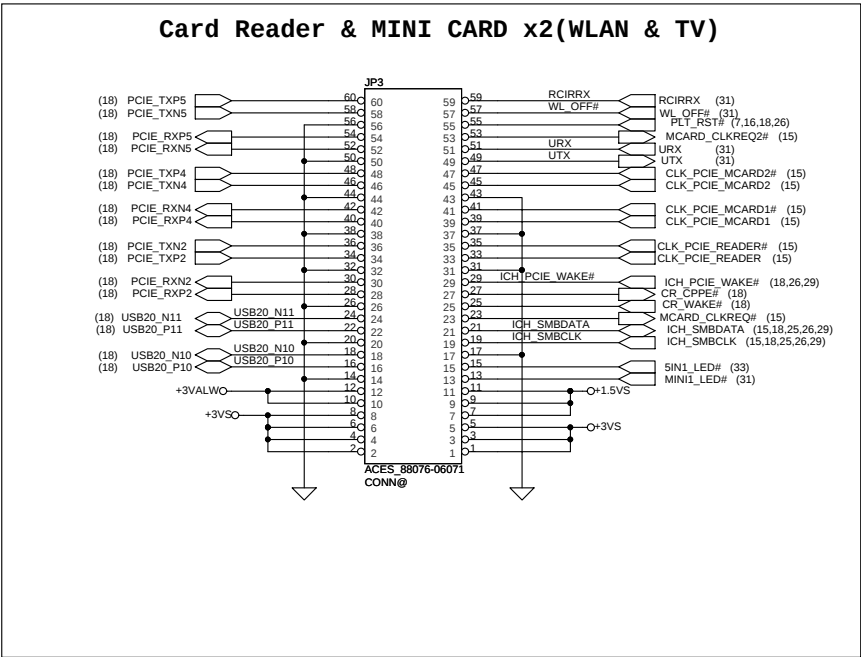
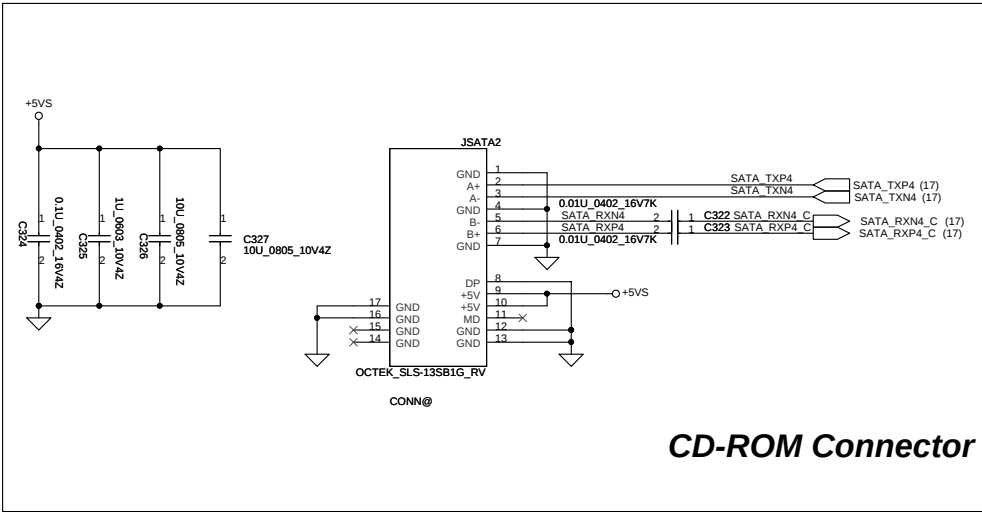
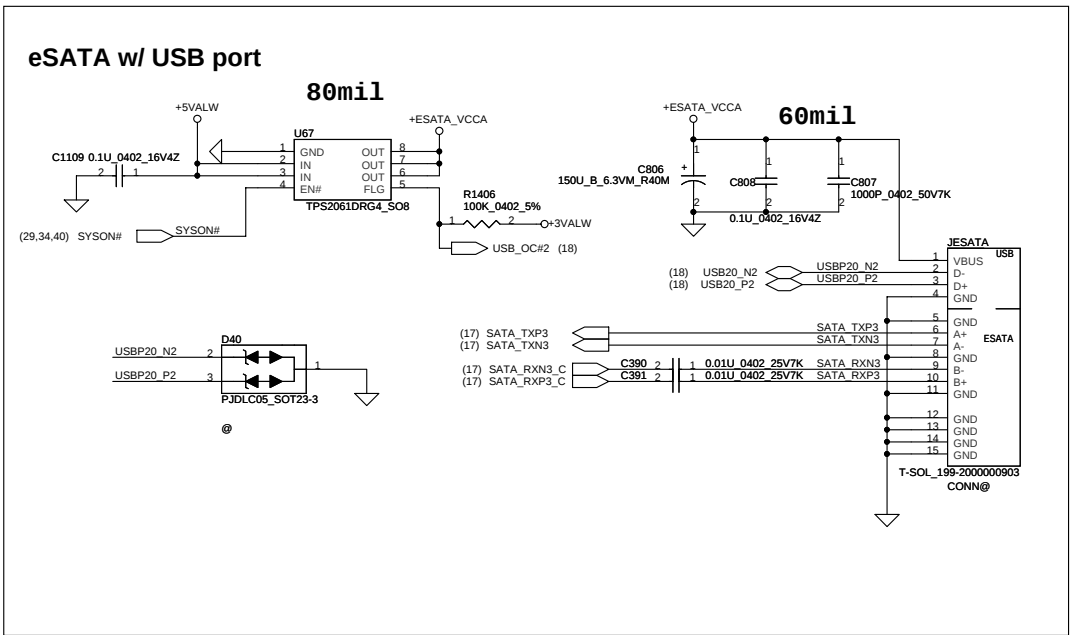
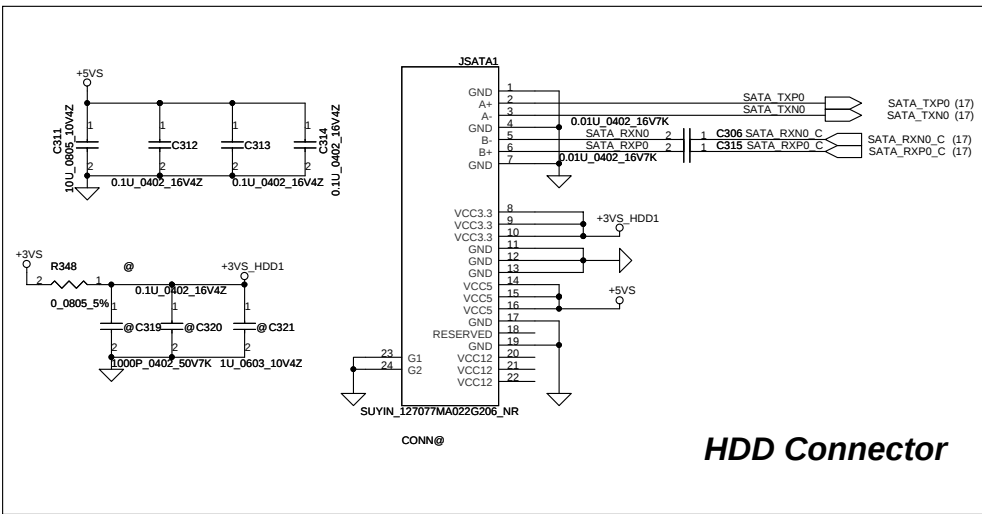




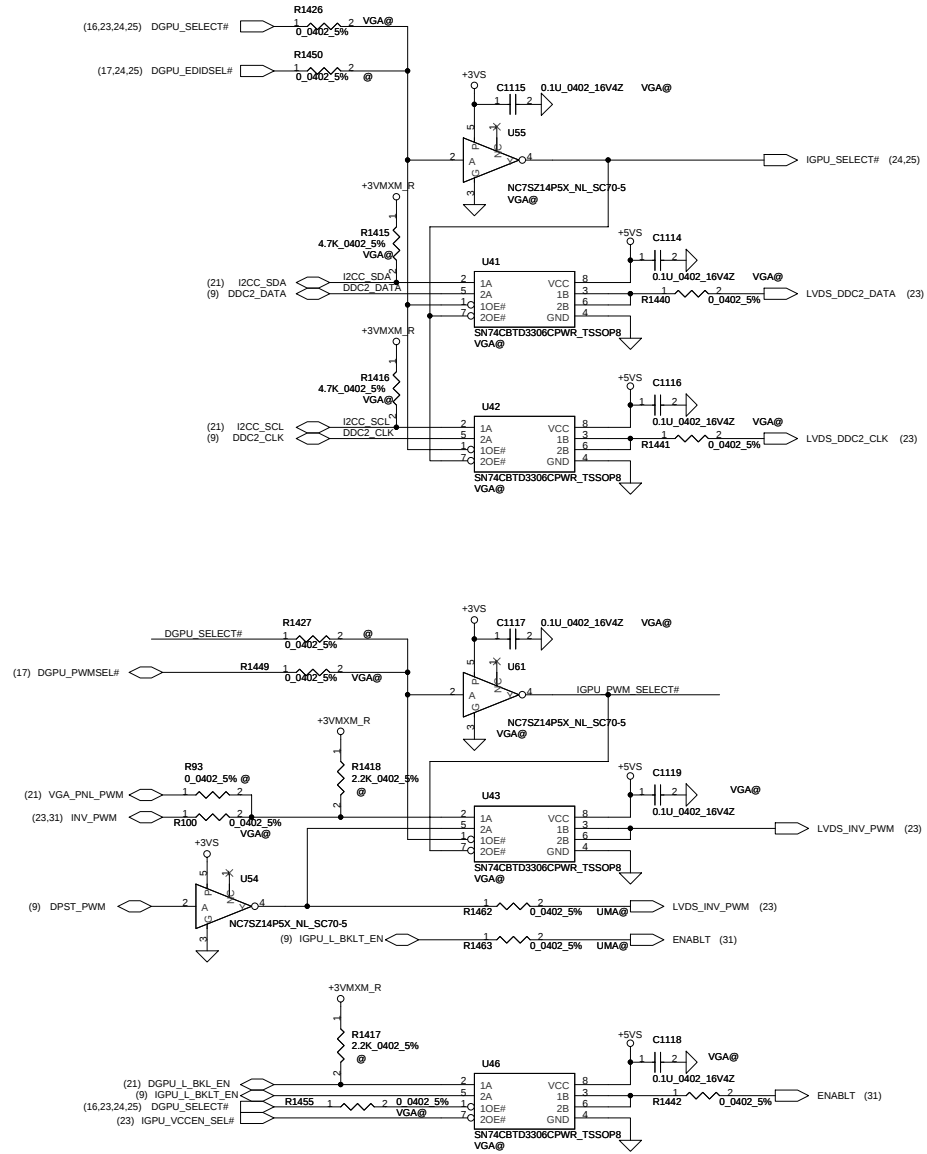
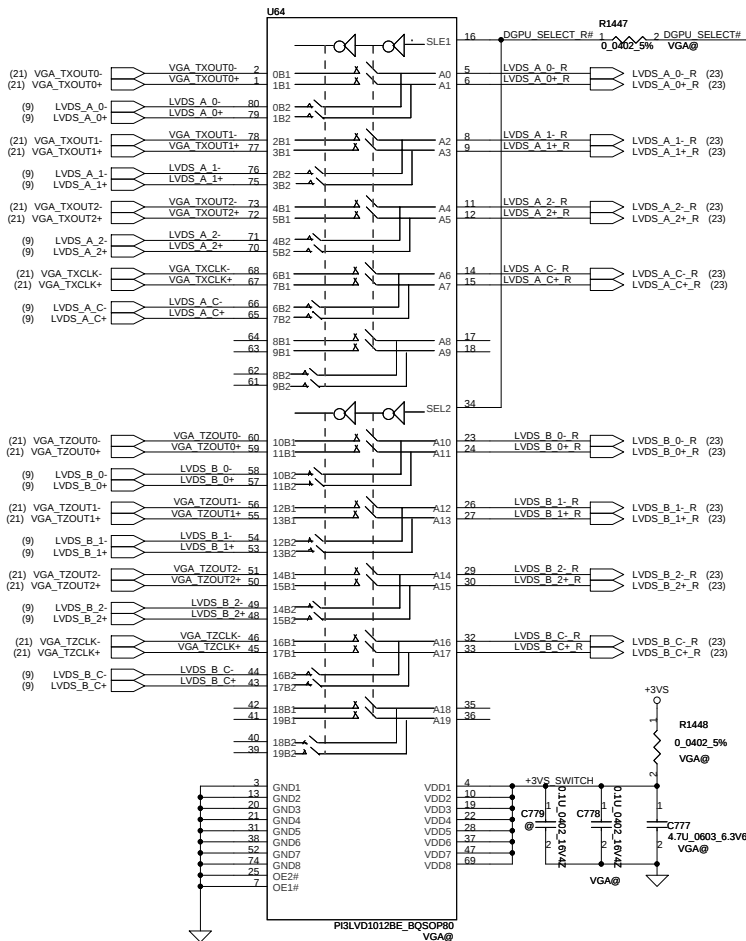


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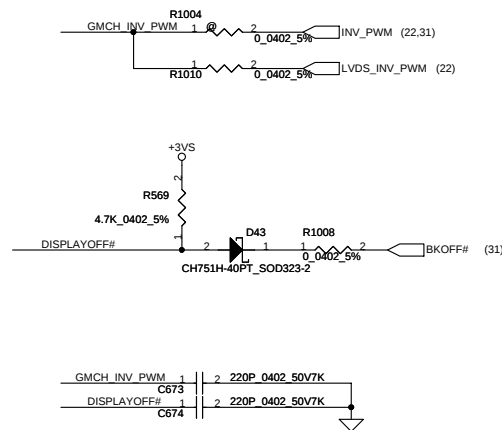
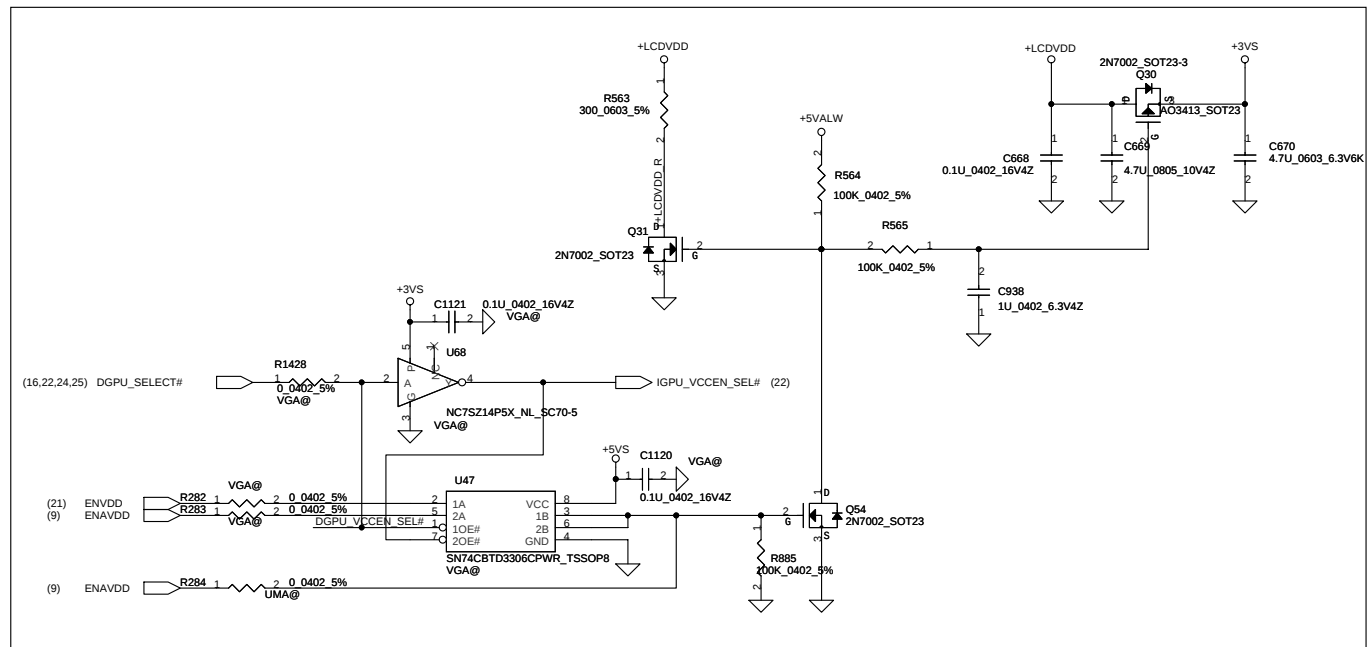
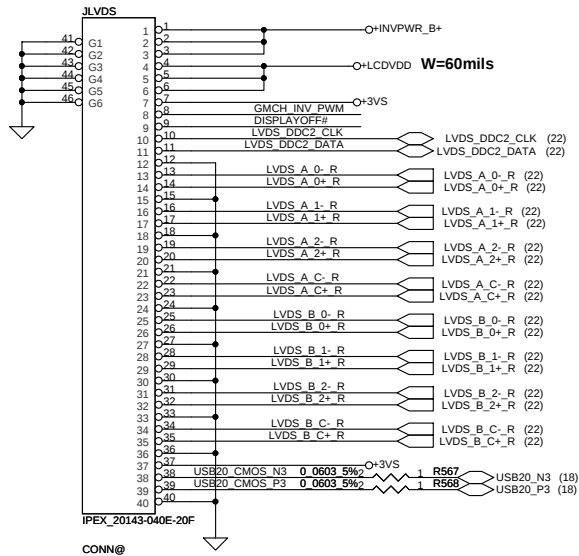
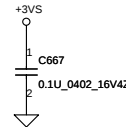
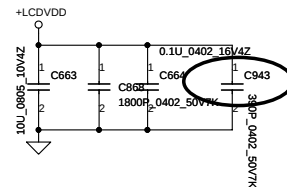
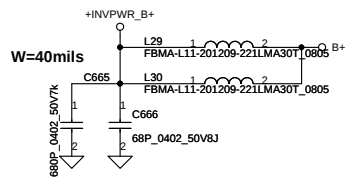


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								Date:		Thursday, April 30, 2009	



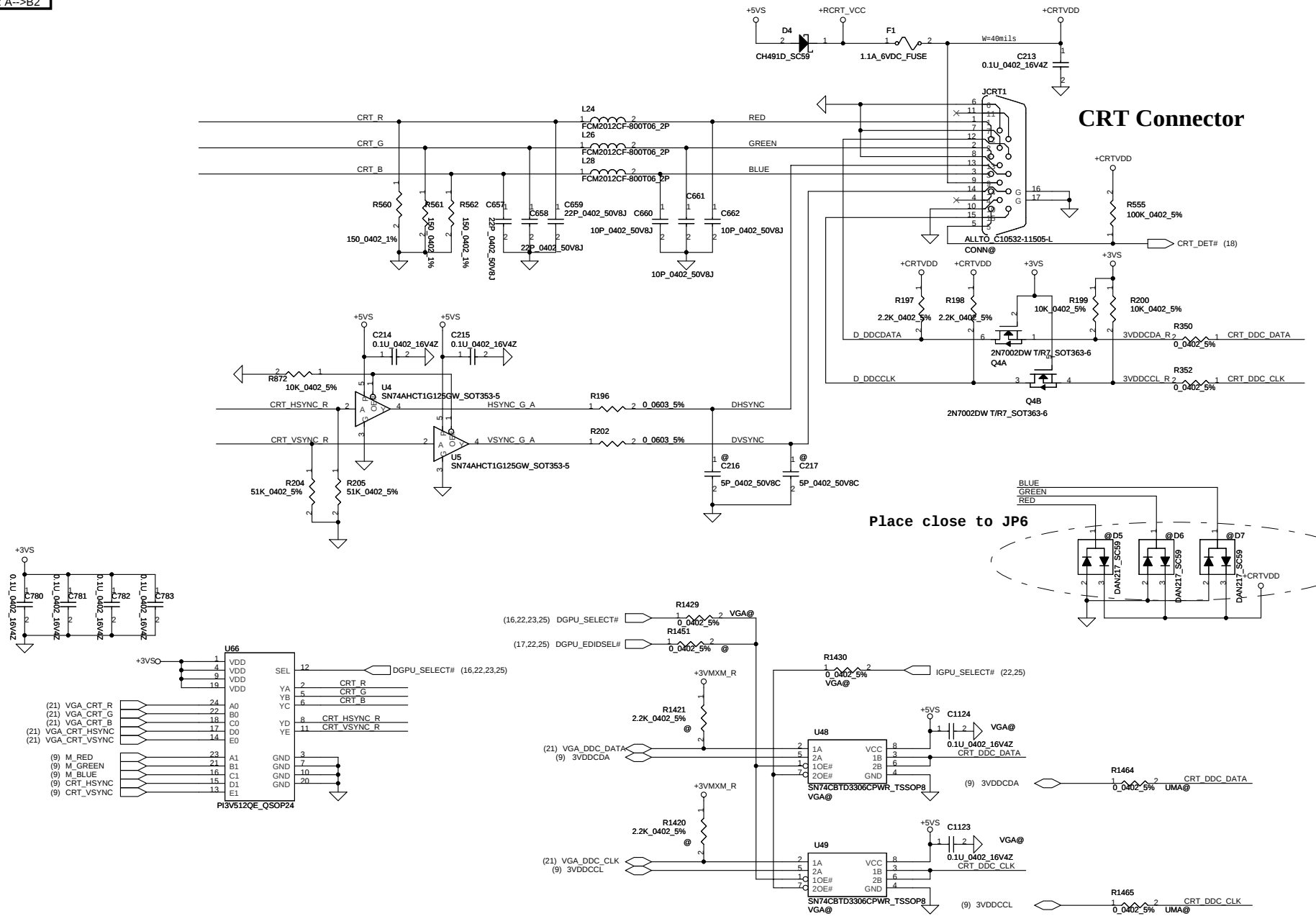
Security Classification		Compal Secret Data		Title	
Issued Date	2007/09/29	Deciphered Date	2007/09/29	Compal Electronics, Inc.	
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LVDS and USB CAM connector

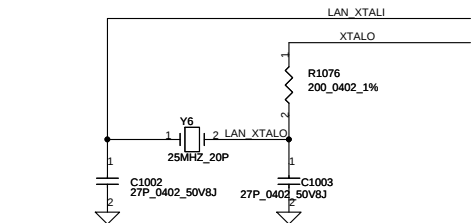
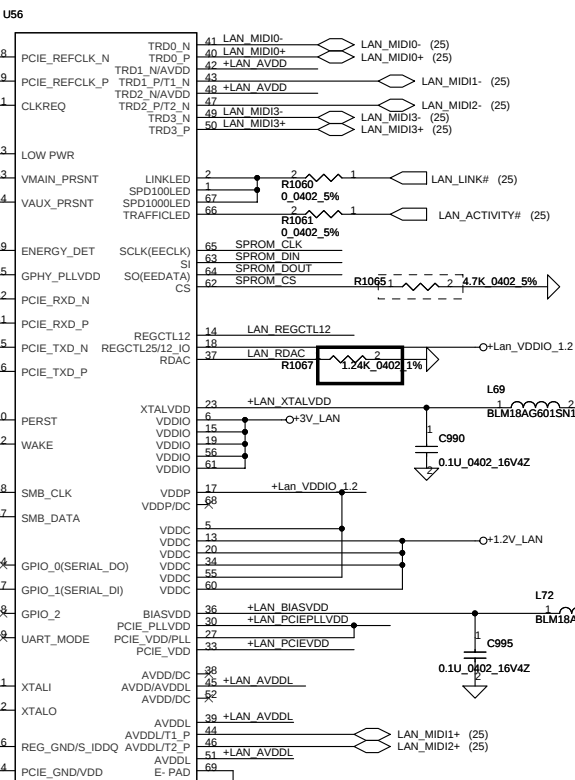
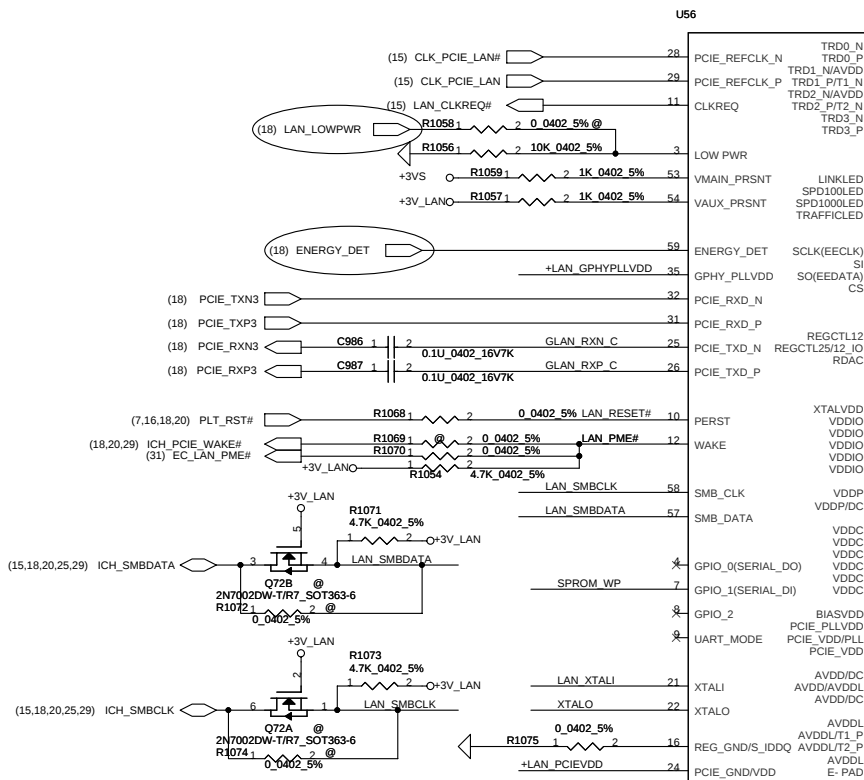
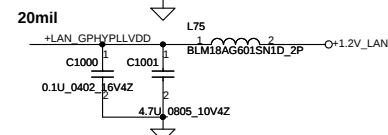
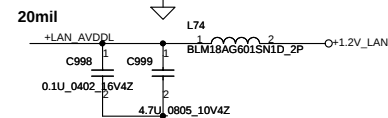
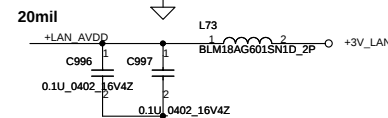
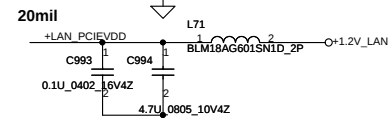
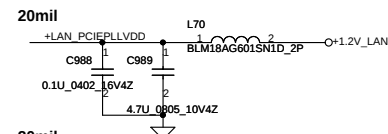
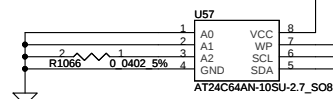
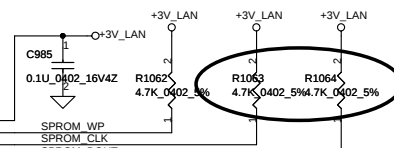
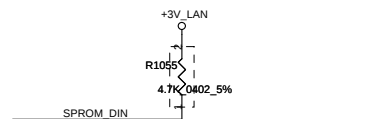
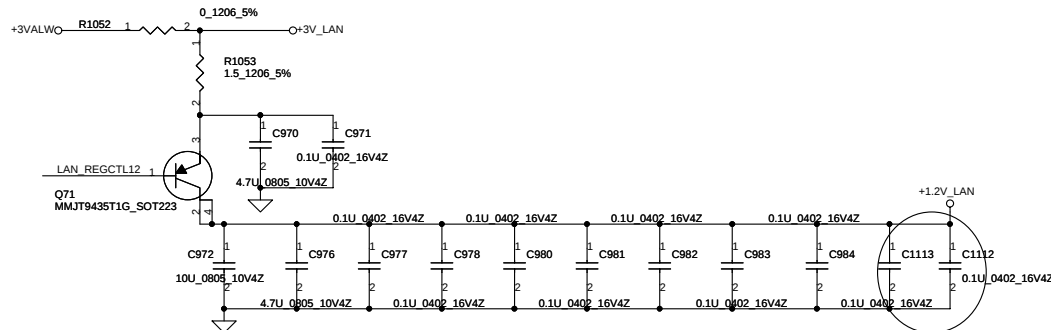
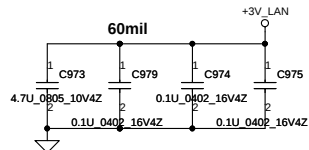


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NOTE: L: A-->B1
H: A-->B2

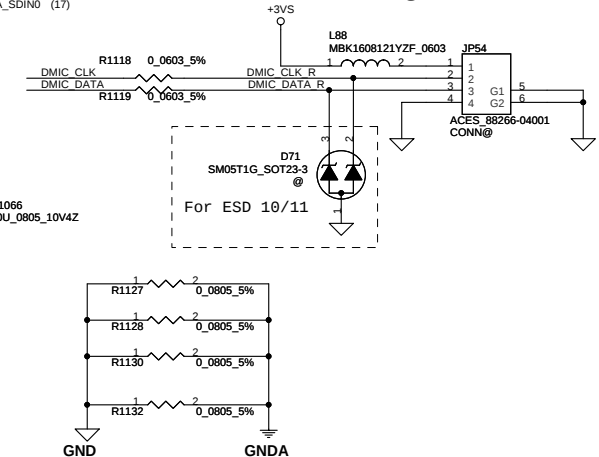
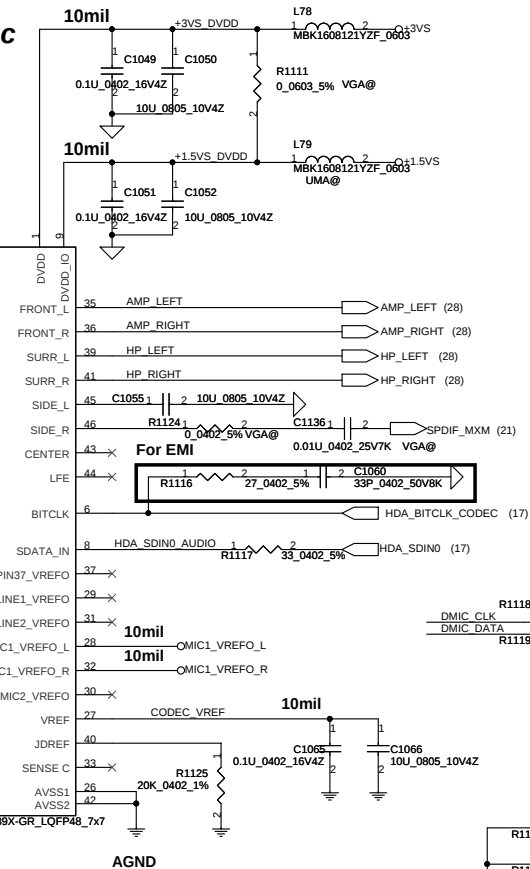


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Place closed to Pin2 & Pin59

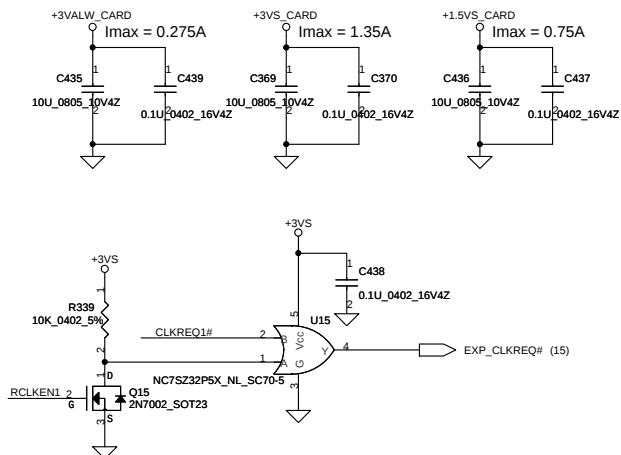
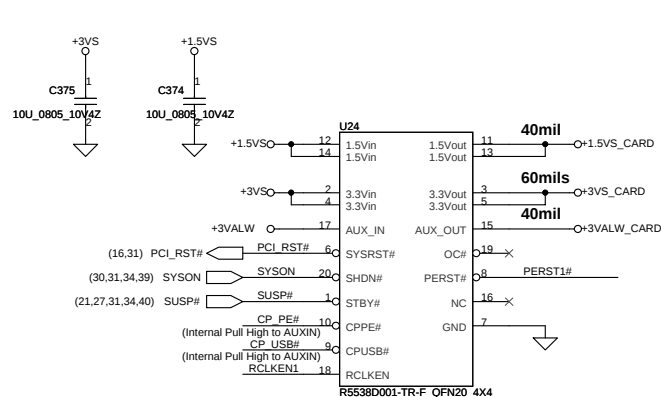
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Issued Date	2007/09/29	Deciphered Date	2007/09/29	SCHEMATIC,MB A5011	
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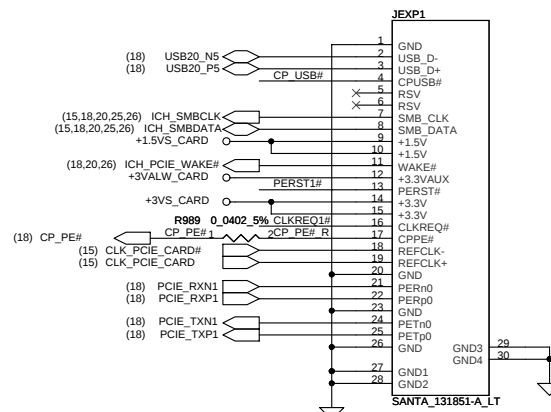
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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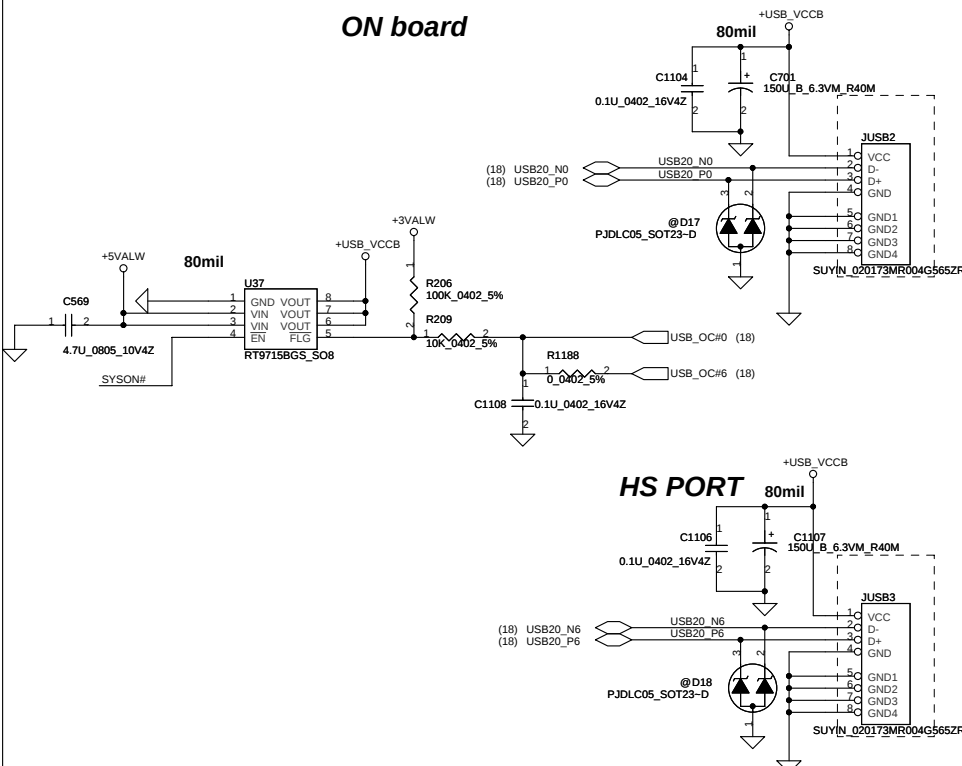
New Card Power Switch



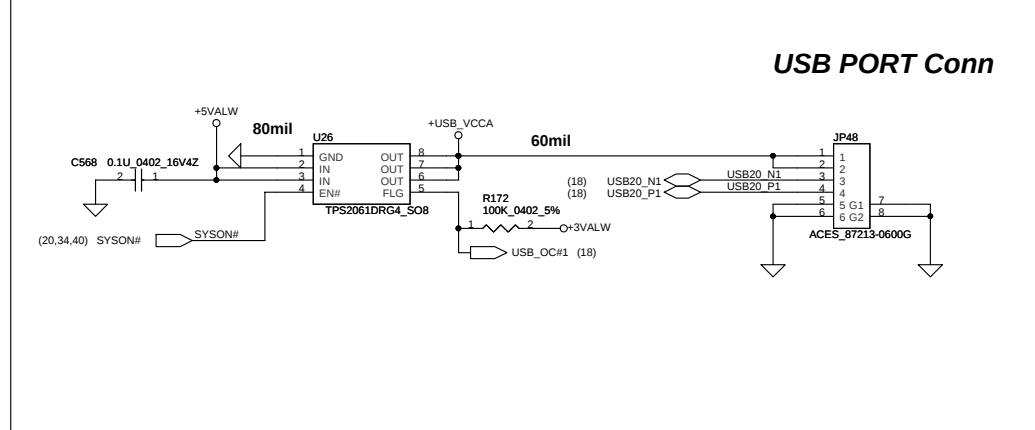
New Card Socket (Left/TOP)



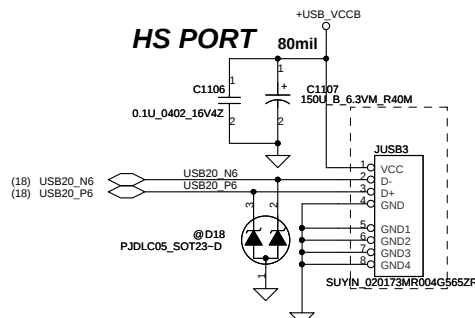
ON board



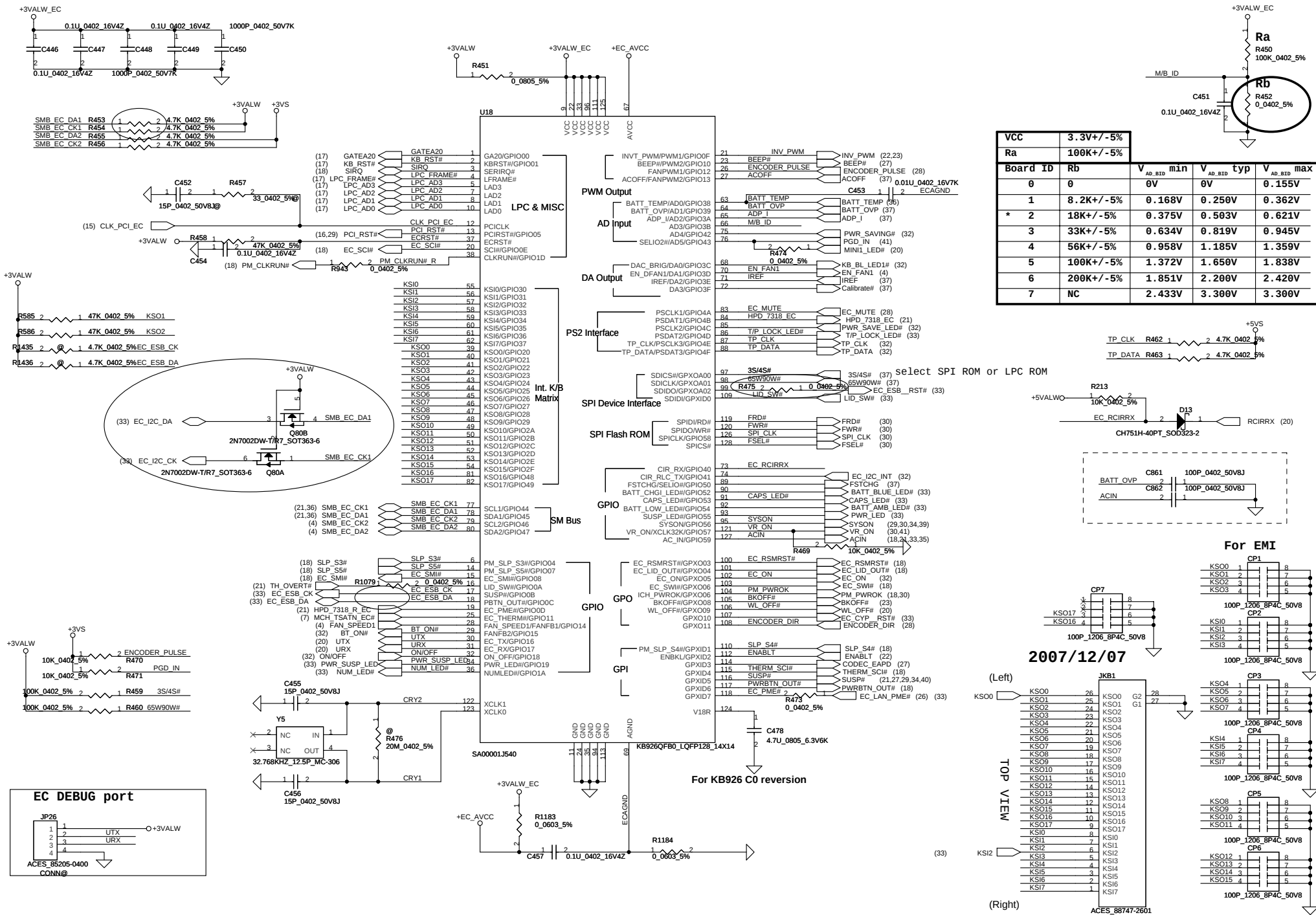
USB PORT Conn



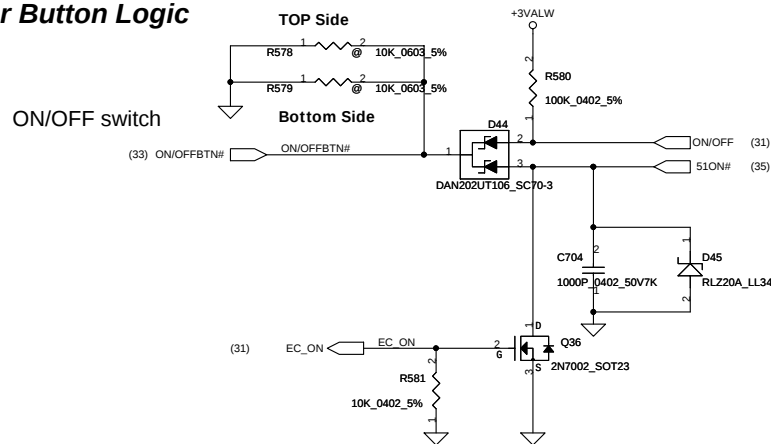
HS PORT



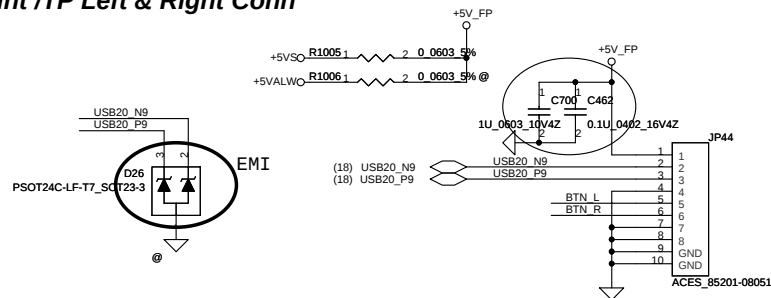
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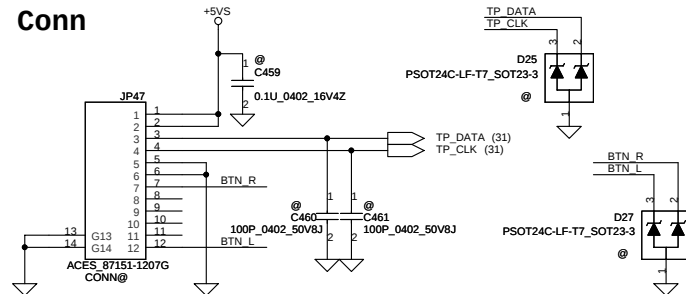
Power Button Logic



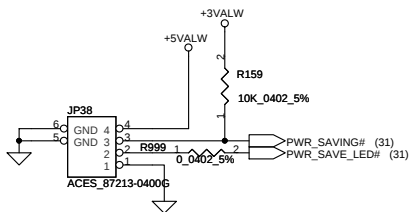
Finger Print /TP Left & Right Conn



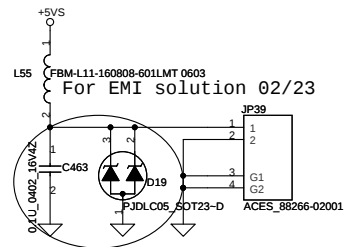
T/P Board Conn



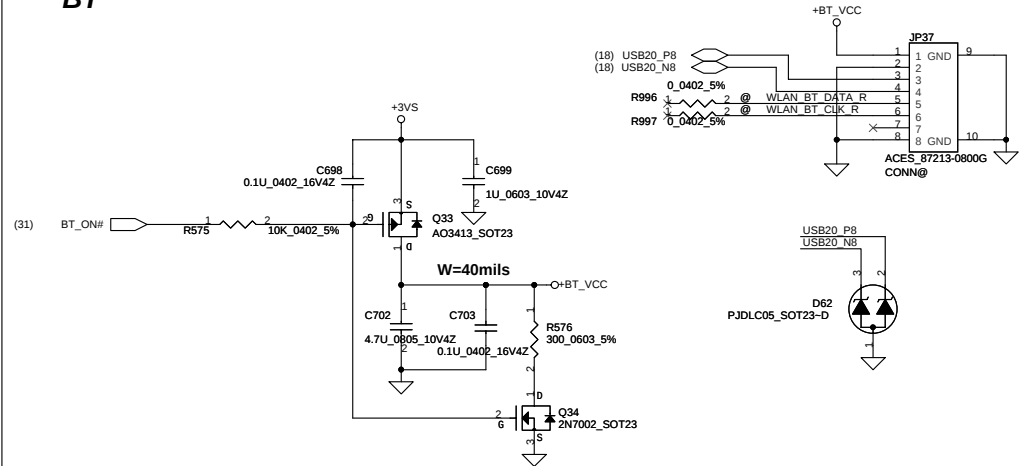
POWER SAVING Conn



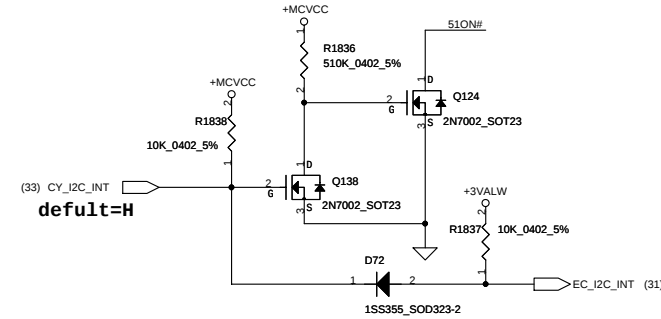
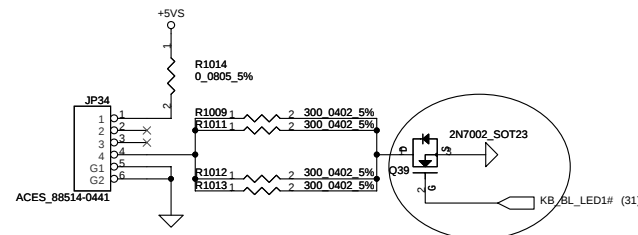
ACER LOGO BackLight Conn



BT



KB back light Conn

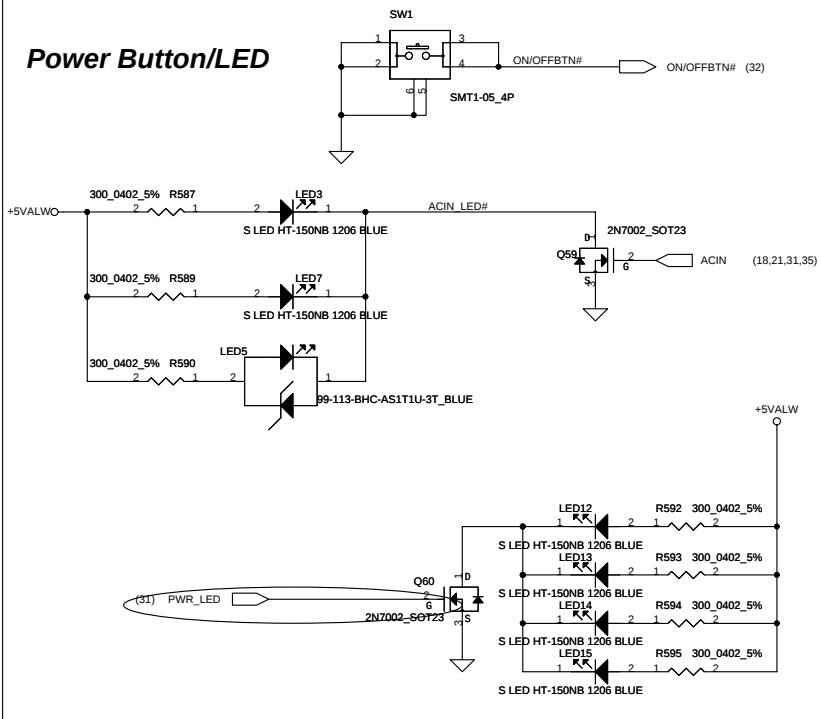


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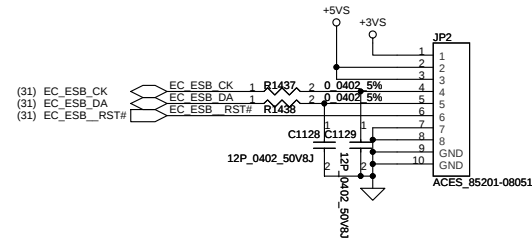
Compal Electronics, Inc.

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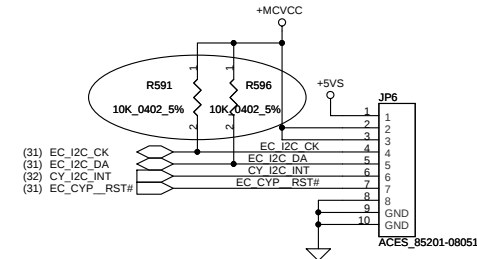
Power Button/LED



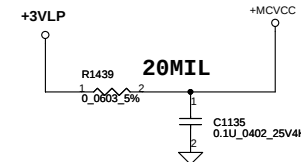
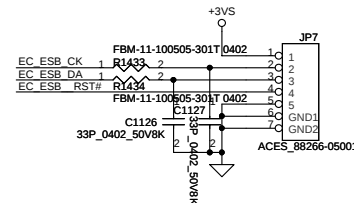
CAP Sensor left(ENE)



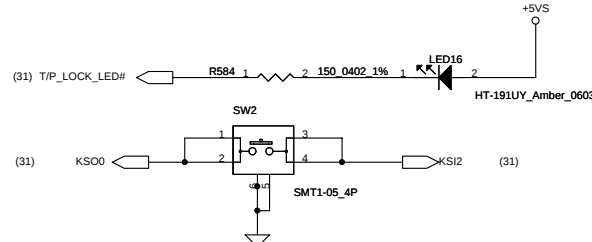
CAP Sensor right(Cypress)



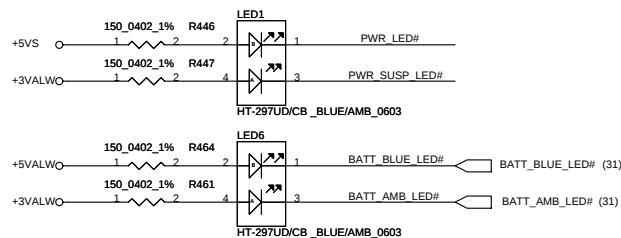
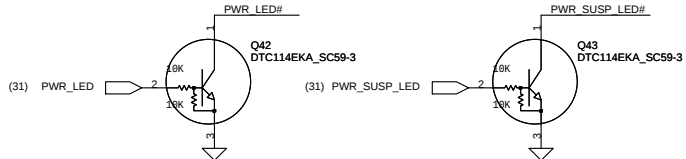
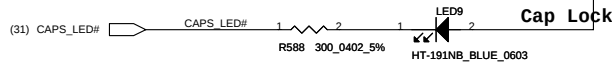
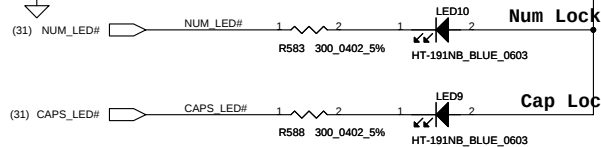
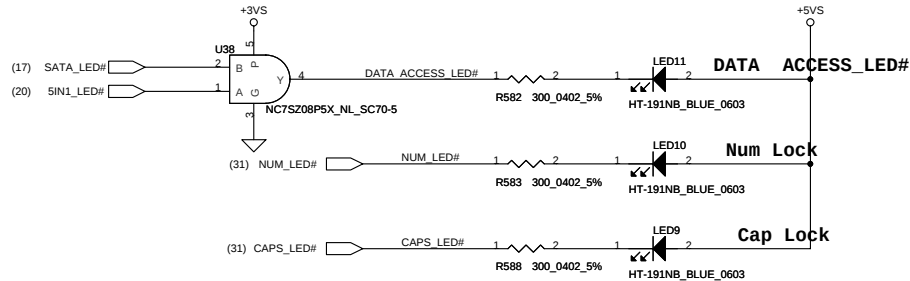
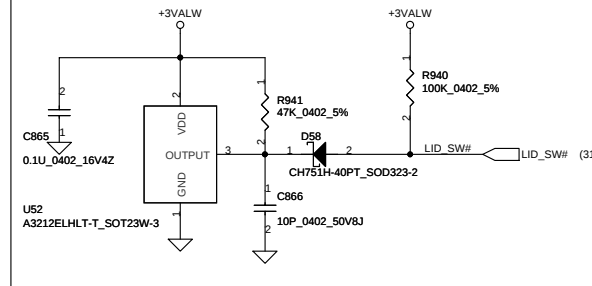
CAP Sensor B COVER(ENE)



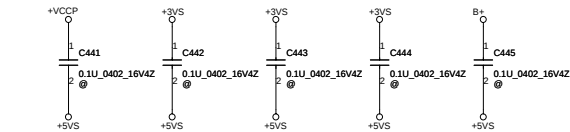
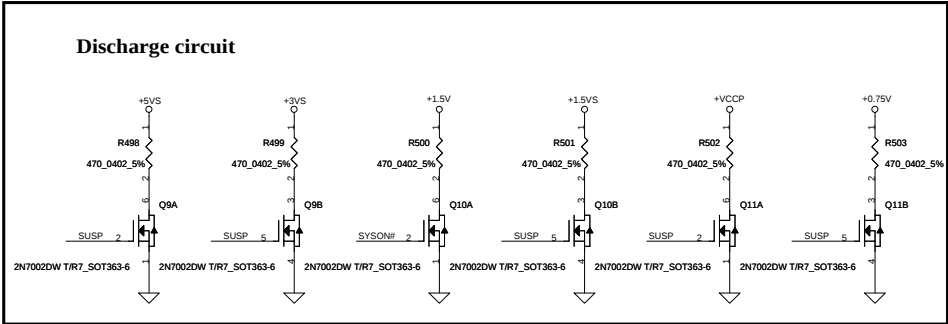
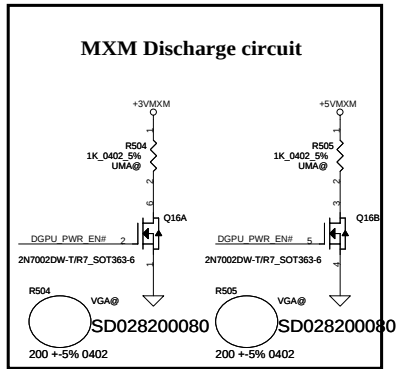
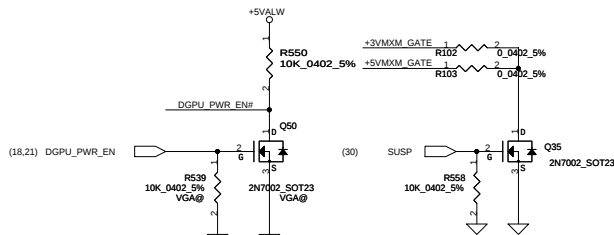
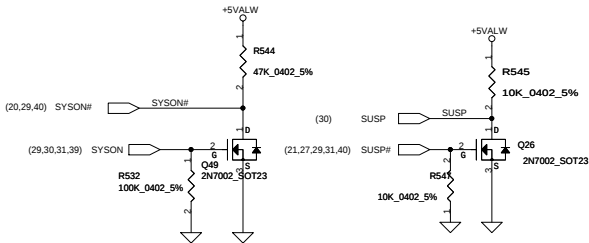
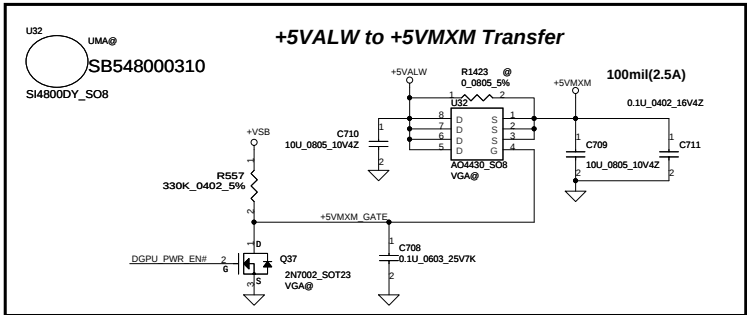
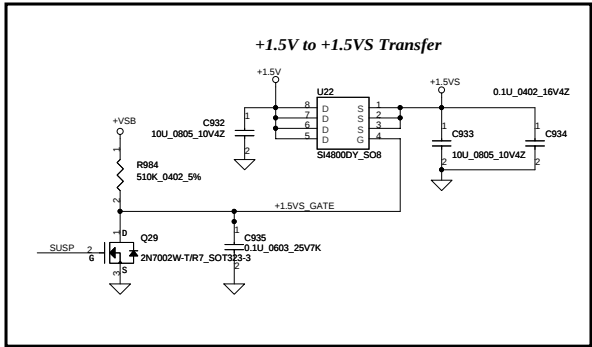
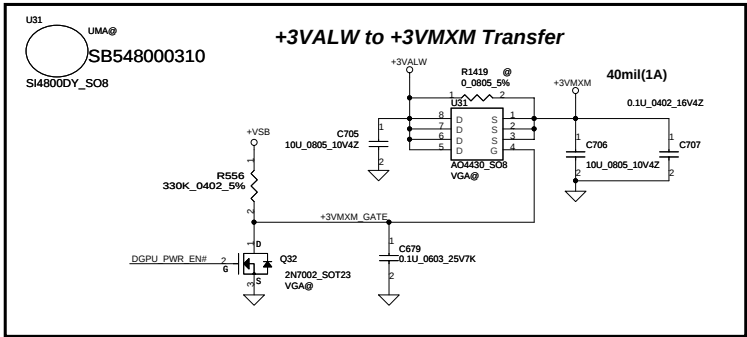
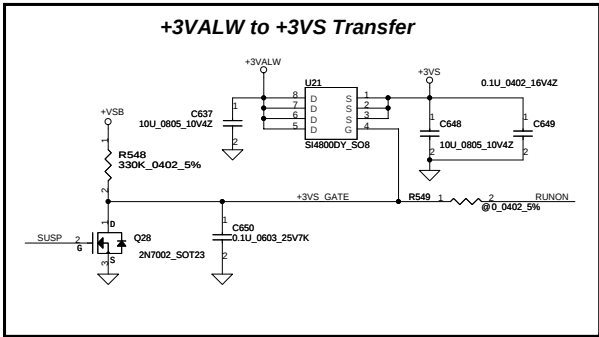
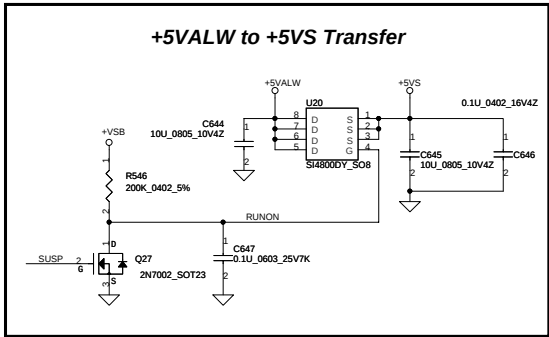
T/IP Lock Button/LED



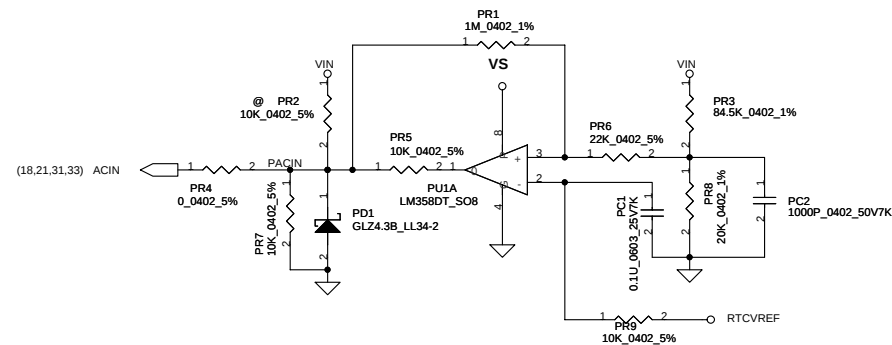
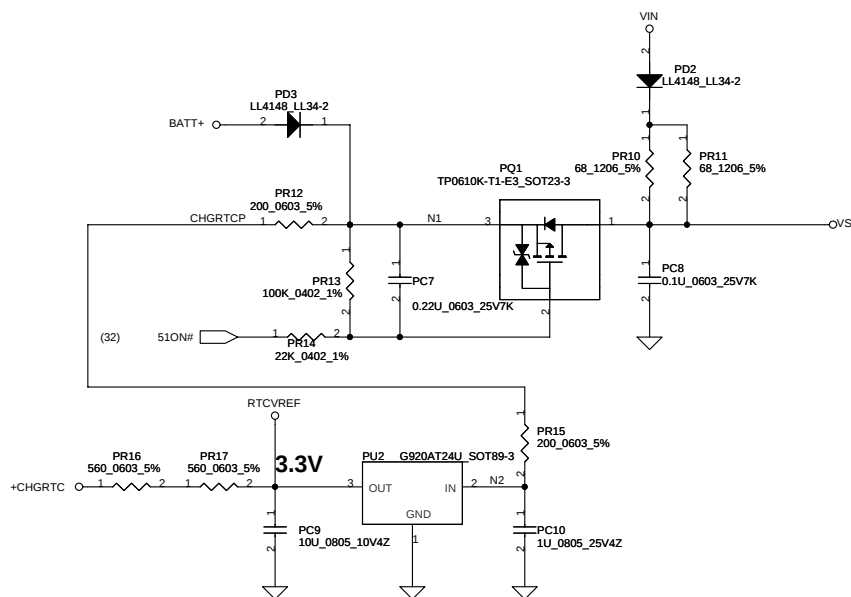
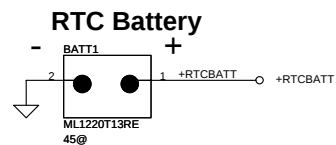
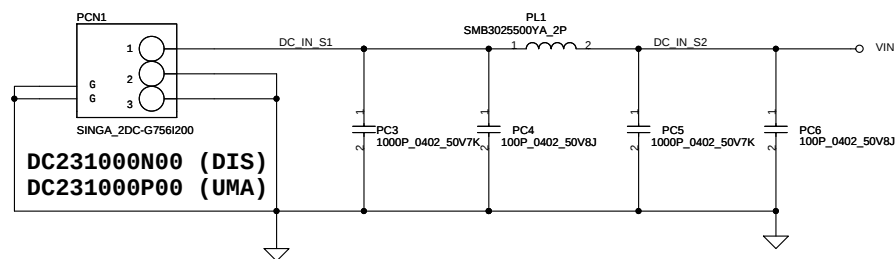
(Hall Effect Switch)



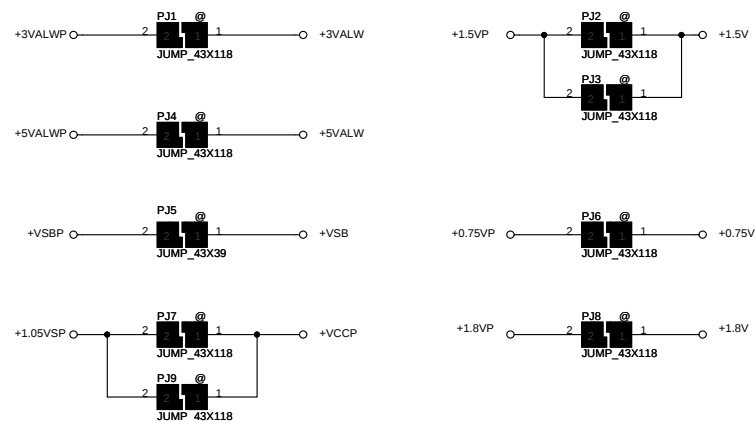
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Vin Detector			
	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V



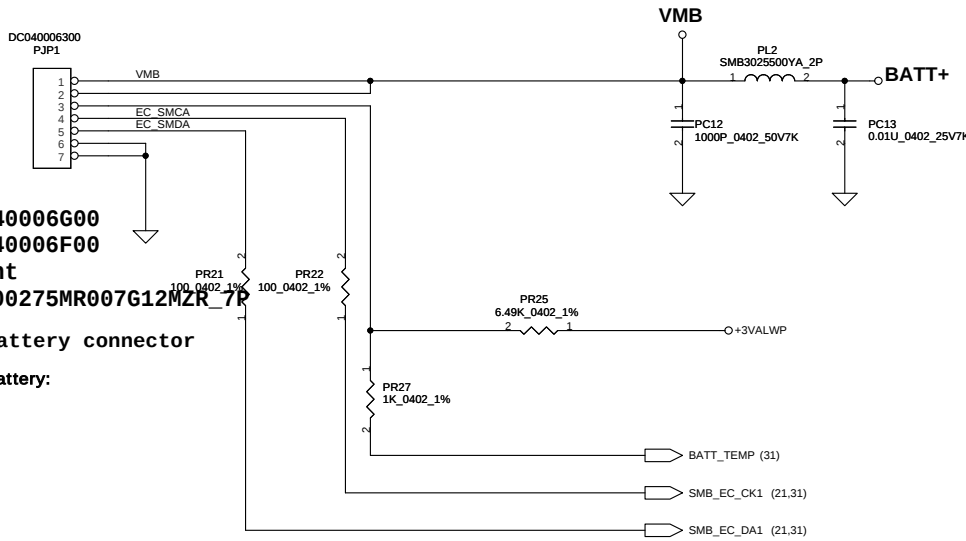
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改 DC040006G00
2nd DC040006F00
Footprint
SUYIN_200275MR007G12MZR_7P

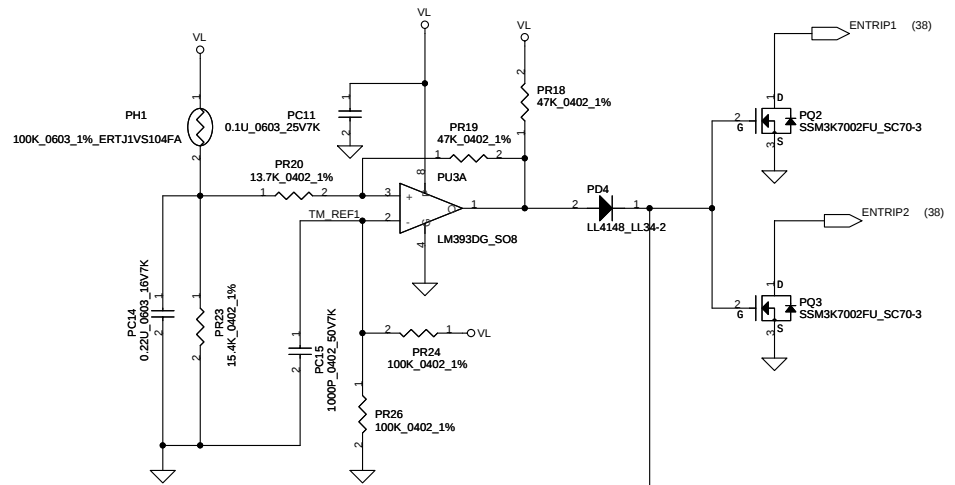
PJP1 battery connector

SMART Battery:

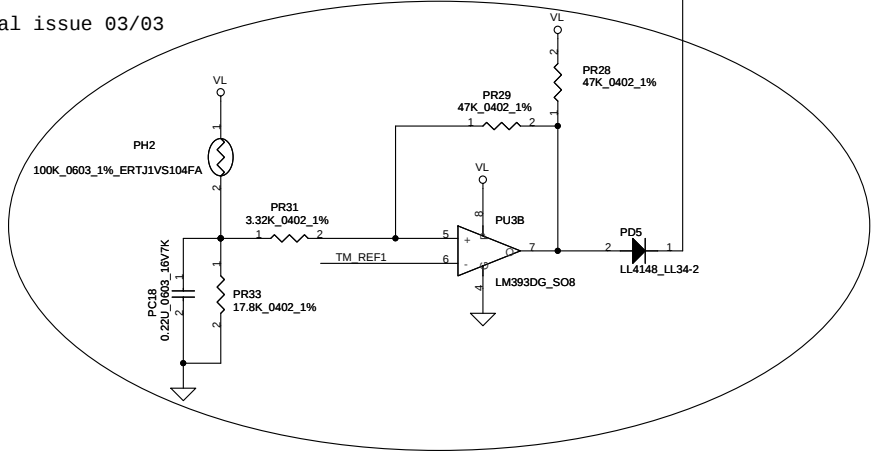
- 1.VMB
- 2.VMB
- 3.TSA
- 4.SMC
- 5.SMD
- 6.GND
- 7.GND



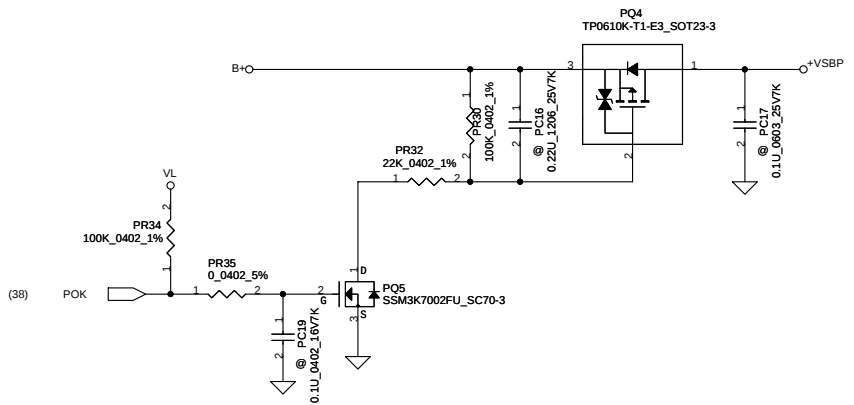
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

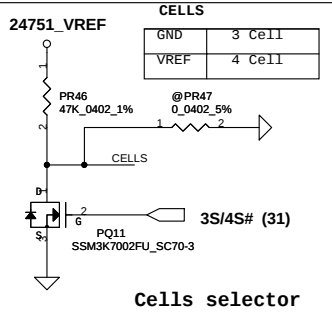
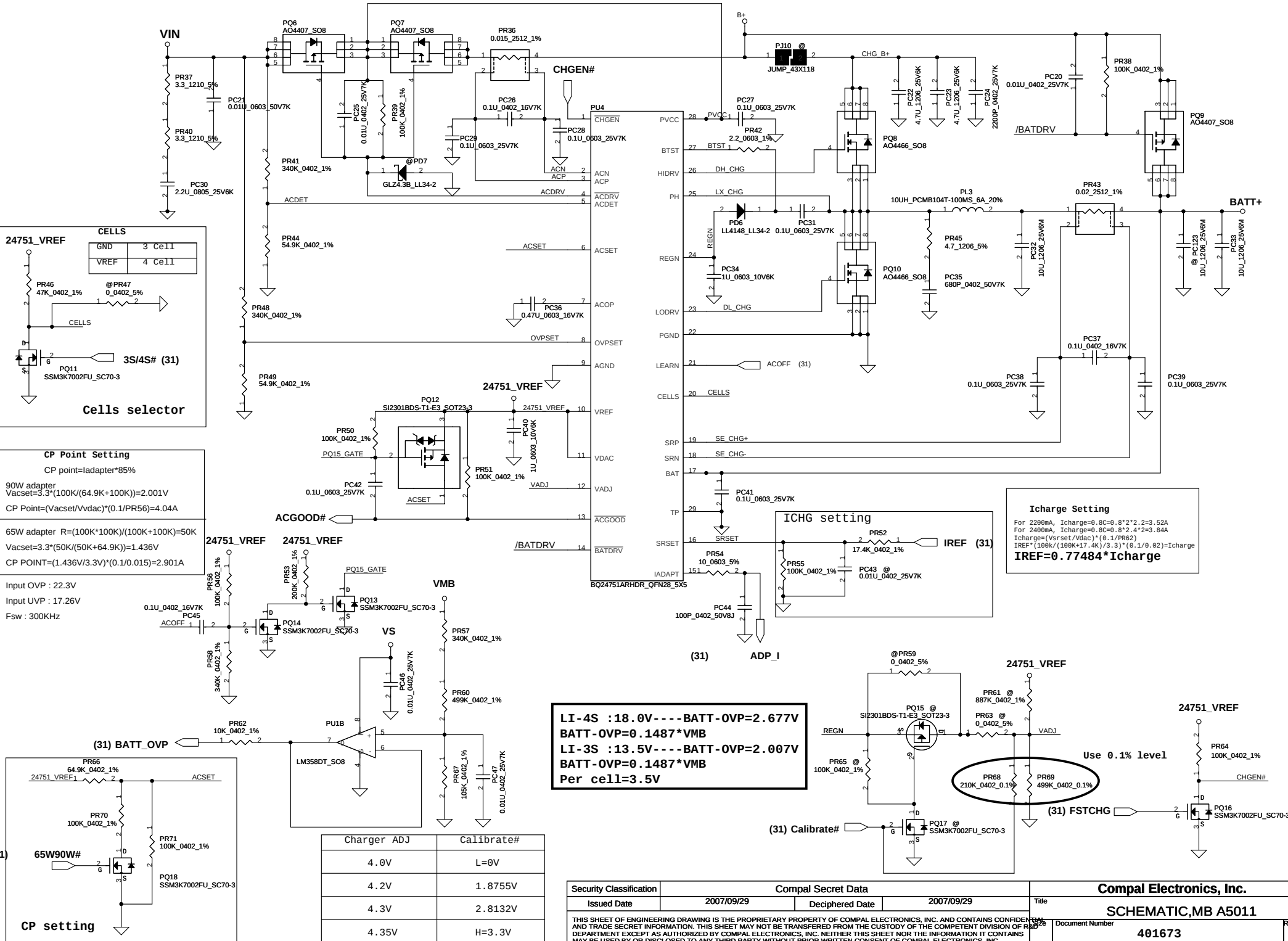


PH2 near main Battery CONN :
BAT. thermal protection at 76 degree C
Recovery at 72 degree C



solve battery thermal issue 03/03



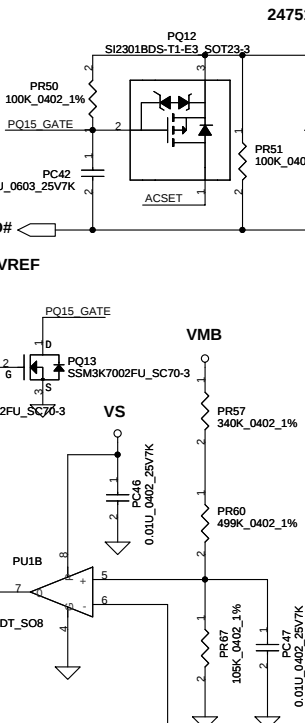
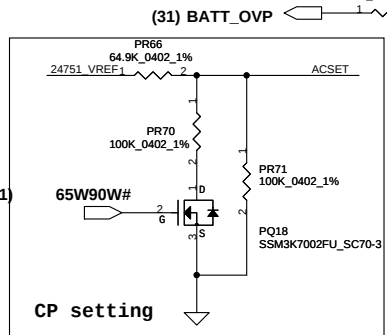


CP Point Setting
CP point=ladapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$
CP Point=(V_{acset} / V_{vdac}) * (0.1 / PR56) = 4.04A

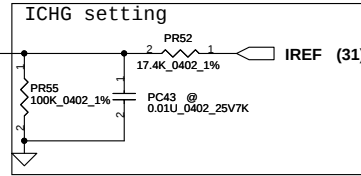
65W adapter $R = (100K \cdot 100K) / (100K + 100K) = 50K$
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$
CP POINT=($1.436V / 3.3V$) * (0.1 / 0.015) = 2.901A

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

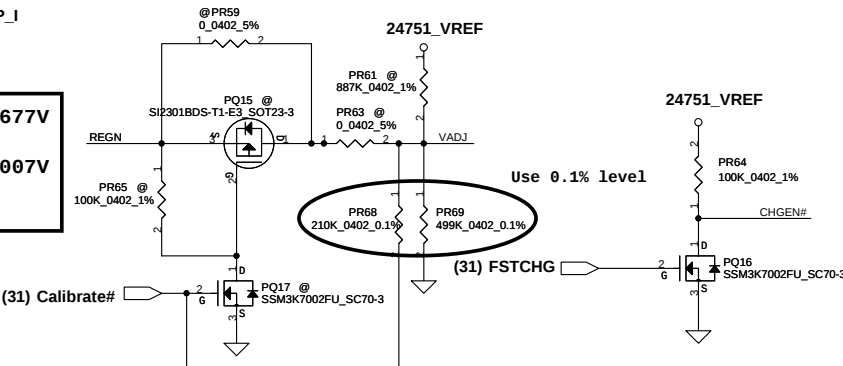


Charger ADJ	Calibrate#
4.0V	L=0V
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

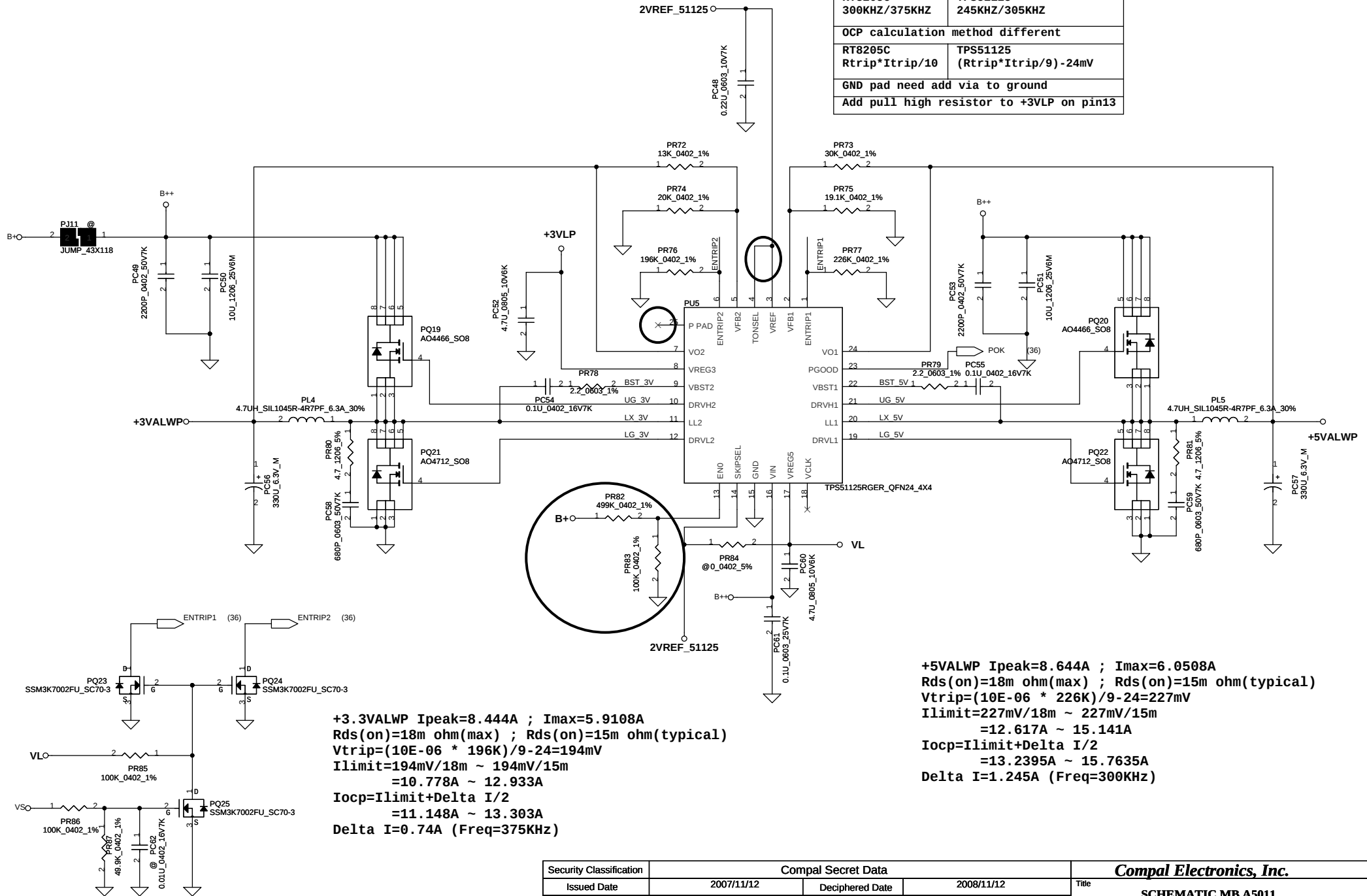
LI-4S : 18.0V --- BATT-OVP=2.677V
BATT-OVP=0.1487*VMB
LI-3S : 13.5V --- BATT-OVP=2.007V
BATT-OVP=0.1487*VMB
Per cell=3.5V



Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
For 2400mA, Icharge=0.8C=0.8*2.4*2=3.84A
Icharge=(Vsrset/Vdac) * (0.1 / PR62)
IREF=(180K / (180K + 17.4K) / 3.3) * (0.1 / 0.02) = Icharge
IREF=0.77484*Icharge



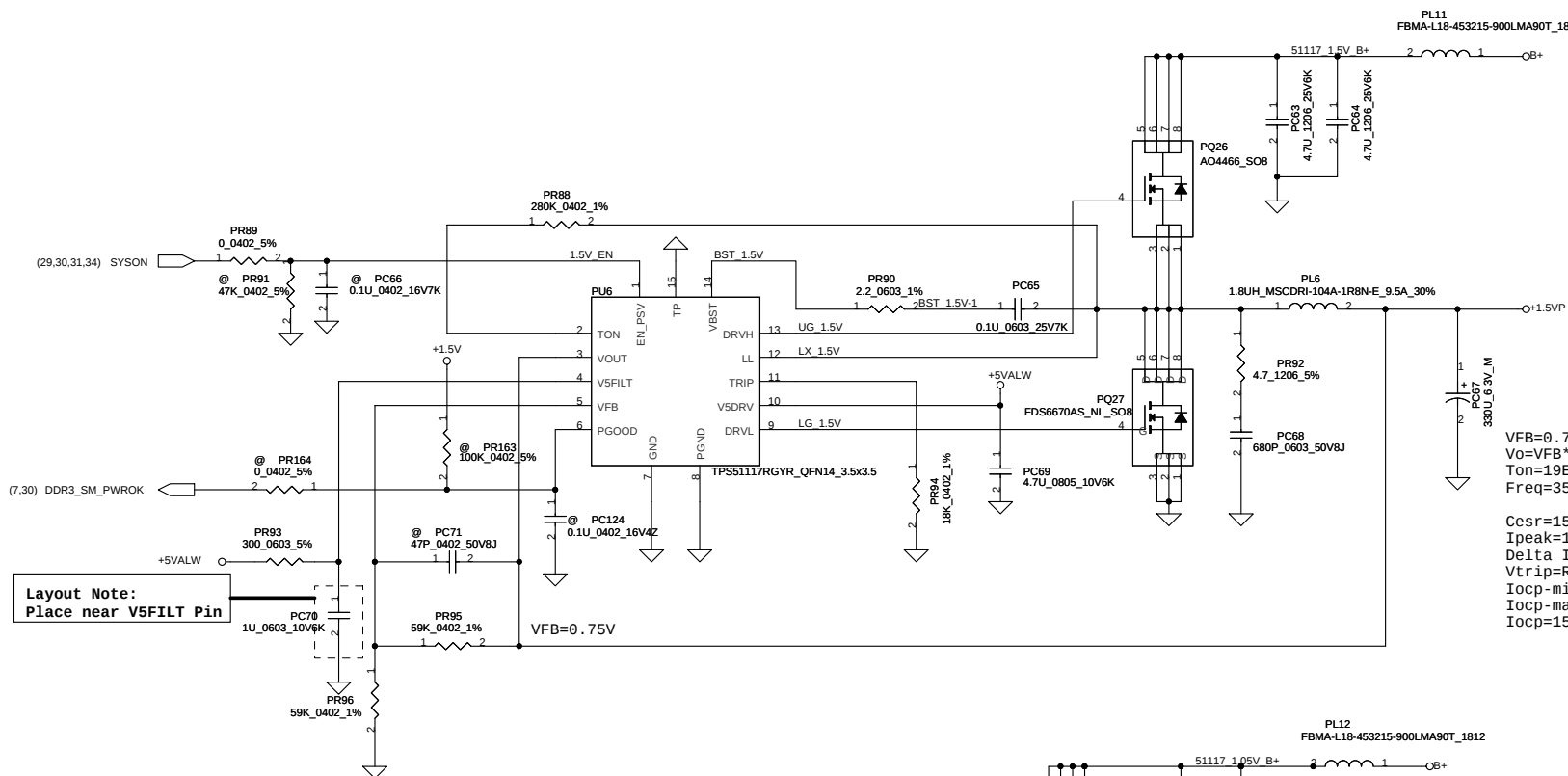
Frequency different	
RT8205C 300KHZ/375KHZ	TPS51125 245KHZ/305KHZ
OCP calculation method different	
RT8205C Rtrip*Itrip/10	TPS51125 (Rtrip*Itrip/9)-24mV
GND pad need add via to ground	
Add pull high resistor to +3VLP on pin13	



+3.3VALWP Ipeak=8.444A ; Imax=5.9108A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vtrip=(10E-06 * 196K)/9-24=194mV
Ilimit=194mV/18m ~ 194mV/15m
=10.778A ~ 12.933A
Iocp=Ilimit+Delta I/2
=11.148A ~ 13.303A
Delta I=0.74A (Freq=375KHz)

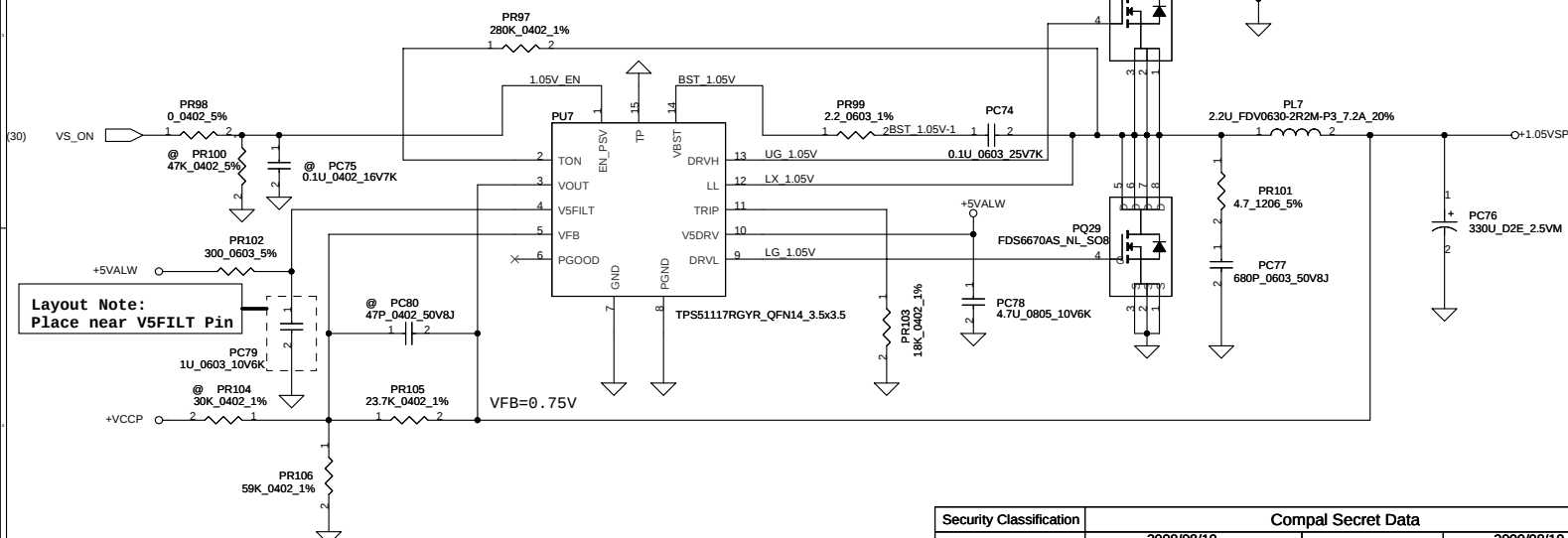
+5VALWP Ipeak=8.644A ; Imax=6.0508A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vtrip=(10E-06 * 226K)/9-24=227mV
Ilimit=227mV/18m ~ 227mV/15m
=12.617A ~ 15.141A
Iocp=Ilimit+Delta I/2
=13.2395A ~ 15.7635A
Delta I=1.245A (Freq=300KHz)

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Layout Note:
Place near V5FILT Pin

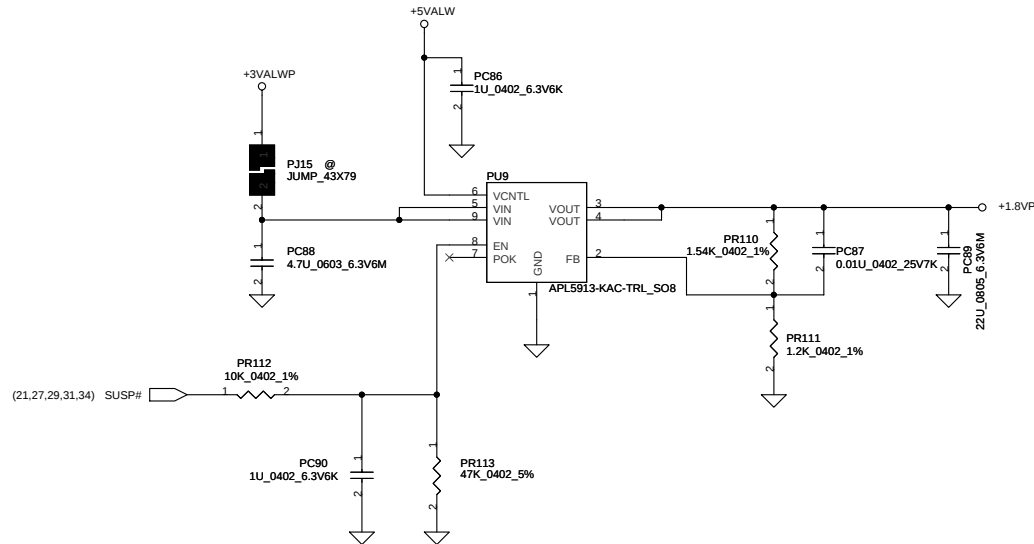
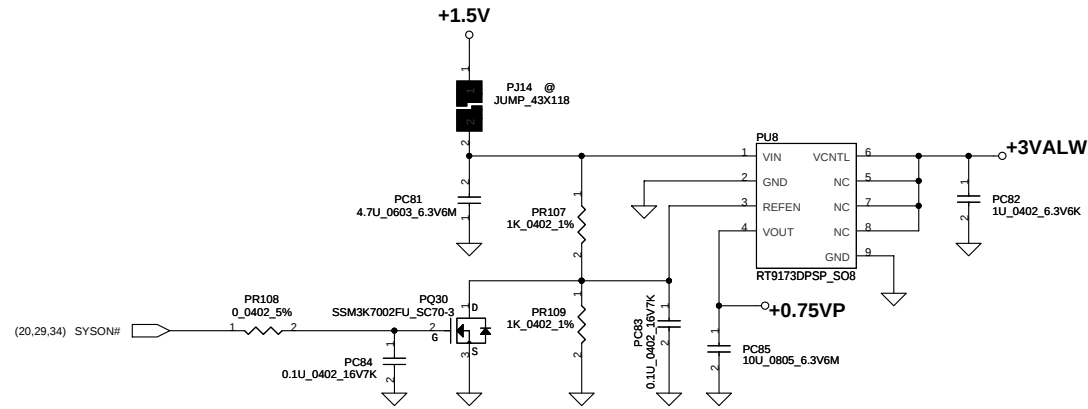
VFB=0.75V
 $V_o = VFB * (1 + PR95/PR96) = 1.5V$
 $Ton = 19E-12 * Ron * (((2/3) * V_o + 150mV) / Vin) + 50ns = 4.68E-7$
 Freq=356KHz
 Ccsr=15m ohm
 Ipeak=13.67A Imax=9.569A
 $\Delta I = ((19.5 - 1.5) * (1.5/19.5)) / (L * Freq) = 2.429A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.180V$
 $I_{ocp-min} = V_{trip} / R_{dsonmax} * 1.1 + 2.429 = 15.161A$
 $I_{ocp-max} = V_{trip} / R_{dsonmax} * 1.1 + 2.429 = 23.436A$
 $I_{ocp} = 15.161 - 23.436A$



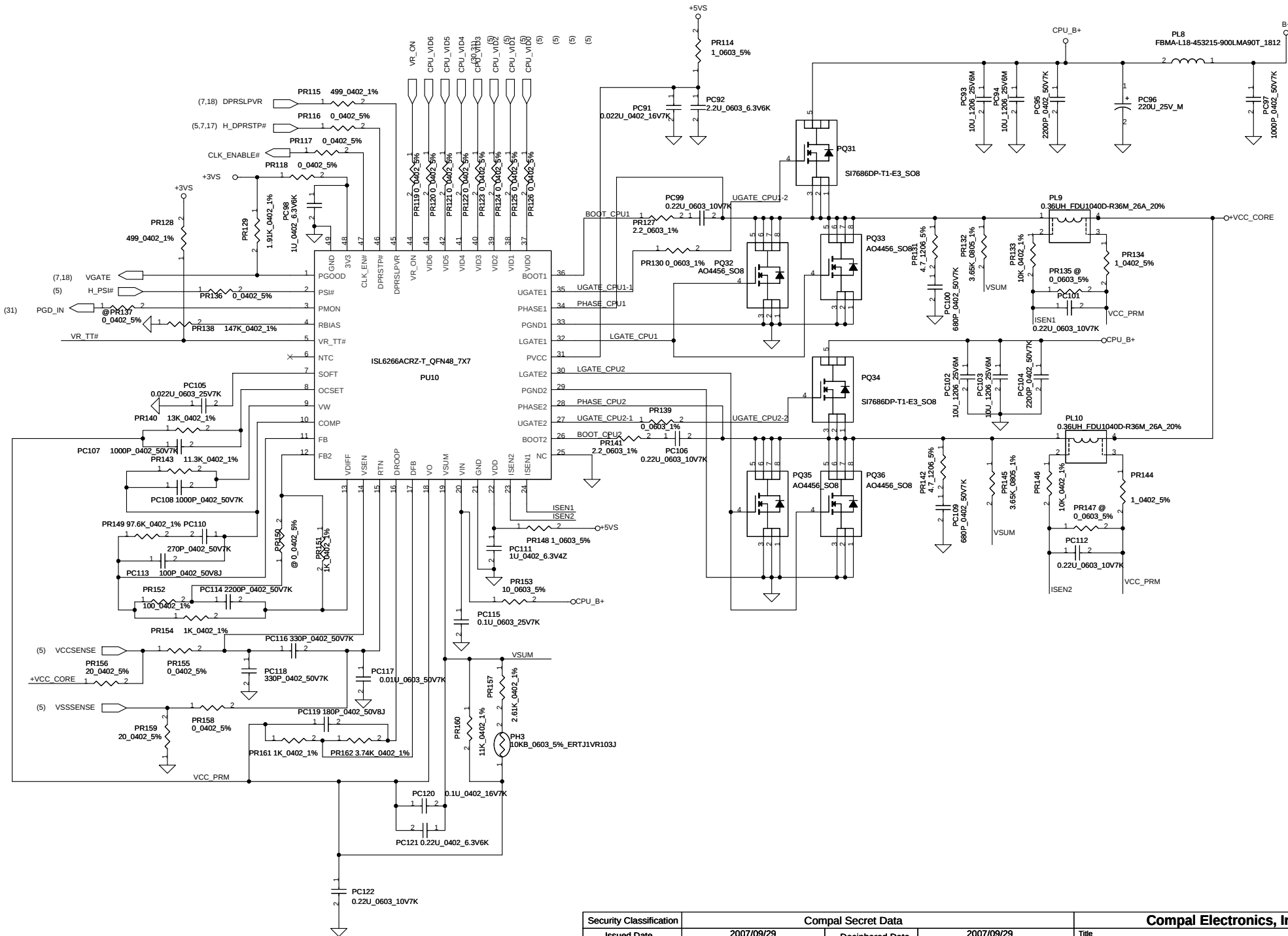
Layout Note:
Place near V5FILT Pin

VFB=0.75V
 $V_o = VFB * (1 + PR105/PR106) = 1.05V$
 $Ton = 19E-12 * Ron * (((2/3) * V_o + 150mV) / Vin) + 50ns = 3.54E-07$
 Freq=330KHz
 Ccsr=15m ohm
 Ipeak=17.47A Imax=12.229A
 $\Delta I = ((19.5 - 1.05) * (1.05/19.5)) / (L * Freq) = 1.597A$
 $V_{trip} = R_{trip} * I_{0uA} = 0.180V$
 $I_{ocp-min} = V_{trip} / R_{dsonmax} * 1.1 + 1.597 = 14.745A$
 $I_{ocp-max} = V_{trip} / R_{dsonmax} * 1.1 + 1.597 = 23.019A$
 $I_{ocp} = 14.745 - 23.019A$

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1		Unite parts			PQ5,PQ11,PQ13,PQ14,PQ16,PQ17,PQ18,PQ30 Change from SB000006800、SB000009080 to SB000009610	2008 12/19	EVT
2		EMI request			Add PR80,PR81,PR131,PR142 SD001470B80 (S RES 1/4W 4.7 +-5% 1206)	2008 12/19	EVT
3		EMI request			Change PR78,PR79,PR127,PR141 from 0 to 2.2 (SD014220B80)	2008 12/19	EVT
4		Reduse 1.5V, 1.05V frequency to about 300KHz			Change PR88,PR97 from 180K to 280K(SD034280380)	2008 12/19	EVT
5	Output voltage error	Set 1.8V voltage			Change PR111 from 1.71K to 1.2K(SD034120180)	2008 12/19	EVT
6		Down size			Change PC88 from 0805 to 0603(SE093475K80)	2008 12/19	EVT
7	Heavy load efficiency fail	Raise heavy load efficiency		38	Change PL4,PL5 from 10uF to 4.7uF(SH000006J80)	2008 12/19	EVT
8		EMI request			Add PC58,PC59 S CER CAP 680P 50V K X7R 0603 (SE025681K80)	2008 12/19	EVT
9		EMI request			Add PC100,PC109 S CER CAP 680P 50V K X7R 0402 (SE074681K80)	2008 12/19	EVT
10				41	Change PR143 from 8.25K to 11.3K(SD034113280)	2008 12/19	EVT
11		Improve load line		41	Change PR162 from 4.42K to 3.74K(SD034374180)	2008 12/22	EVT
12		New charge voltage setting		37	Delete PQ15,PQ17,PR61,PR63,PR65	2008 12/23	EVT
13		New charge voltage setting		37	Add PR68 210K_0402_1%(SD034210380)	2008 12/23	EVT
14		New charge voltage setting		37	Change PR69 from 221K to 49.9K(SD034499280)	2008 12/23	EVT
15	Battery can't charge to 100%			37	Change PR69 from 49.9K to 499K(SD034499380)	2009 01/12	DVT
16	HDMI 5V voltage test fail(should 4.8~5.3V)	Raise 5V voltage		38	Change PR75 from 20K to 19.1K(SD034191280)	2009 01/17	DVT
17		Prevent spike		37	Add PD7	2009 01/21	DVT
18		Improve charge voltage		37	Change PR68, PR69 from 1% to 0.1%	2009 01/22	DVT
19		EMI request		39	Change PR90, PR99 from 0 to 2.2(SD014220B80) Enable PR92, PR101, PC68, PC77	2009 02/04	DVT
20		EMI request		39	Change PJ12 to PL11(SM010020720) Change PJ13 to PL12(SM010020720)	2009 02/04	DVT
21		EMI request		37	Change PR42 from 0 to 2.2(SD014220B80) Enable PR45, PC35	2009 02/04	DVT
22	Protect logic low	Set trigger point at 76		36	Enable PD5, PH2, PR28, PR29, PR31, PR33, PC18	2009 02/25	PVT
23							

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
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