

Compal Confidential

KALG1- M/B Schematics Document

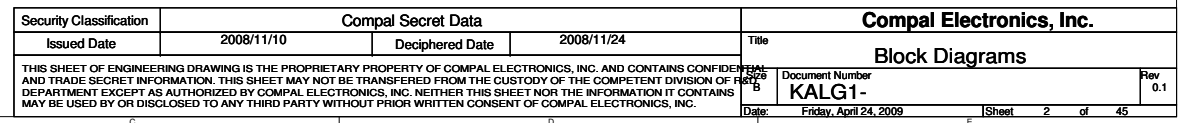
Intel Penryn Processor with Cantiga + DDRII + ICH9M

2009-04-17

REV 01

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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	Cover Page
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File Name : LA-XXXXP



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR2 DIMMA	1001 000Xb
DDR2 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	PCB 08Y LA-5271P REV1 M/B
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

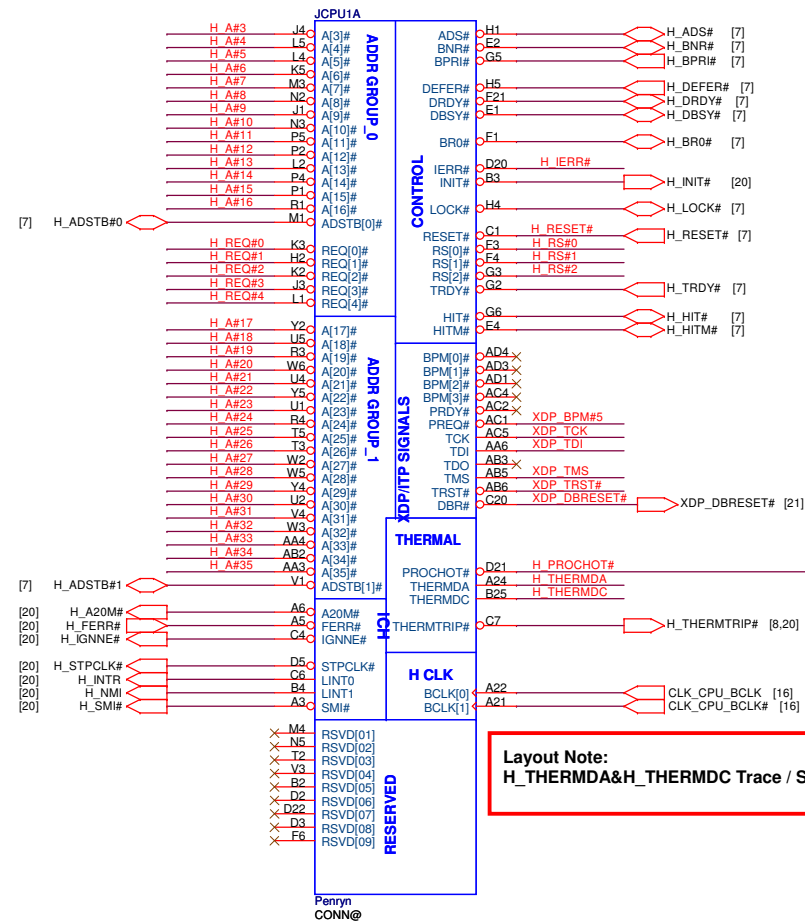
BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

BOM Configuration Table

Project	BOM Configuration
KALG1_GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1_GL40	GL40@/KALG1@/KAL90_G0_90+@
KAL90+_GL40	GL40@/KAL90_H0_90+@/KAL90_90+@/KAL90_G0_90+@
KAL90+_GM45	GM45@/KAL90_H0_90+@/KAL90_90+@/KAL90_G0_90+@
KALH0+_GL40	GL40@/KAL90_H0_90+@/KALH0@
KALH0+_GM45	GM45@/KAL90_H0_90+@/KALH0@

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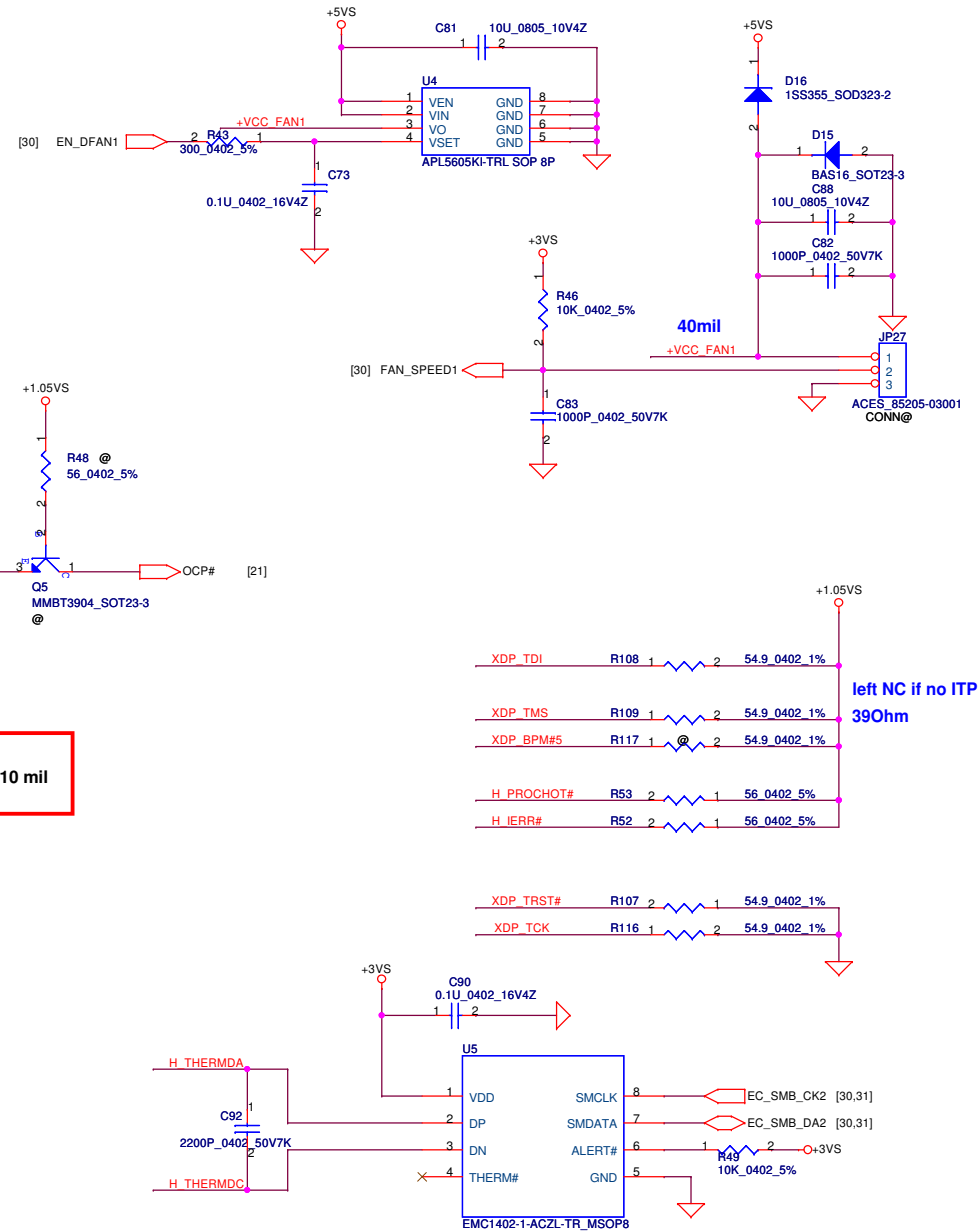
[7] H_A# [3..35]  H_A# [3..35]
 [7] H_REQ# [0..4]  H_REQ# [0..4]
 [7] H_RS# [0..2]  H_RS# [0..2]



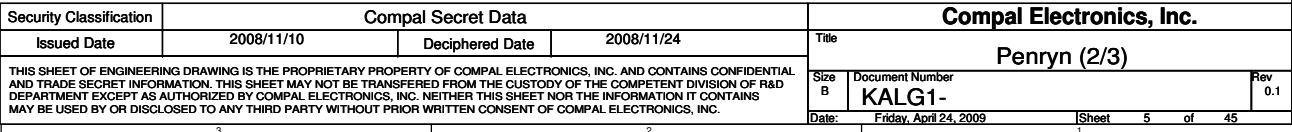
Layout Note:
 H_THERMDA & H_THERMDC Trace / Space = 10 / 10 mil

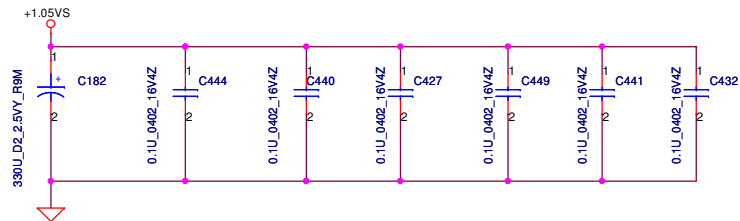
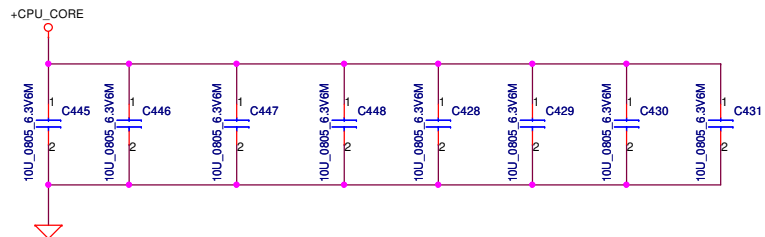
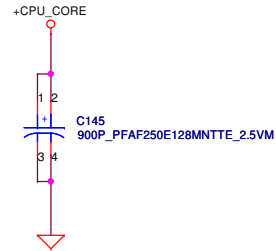
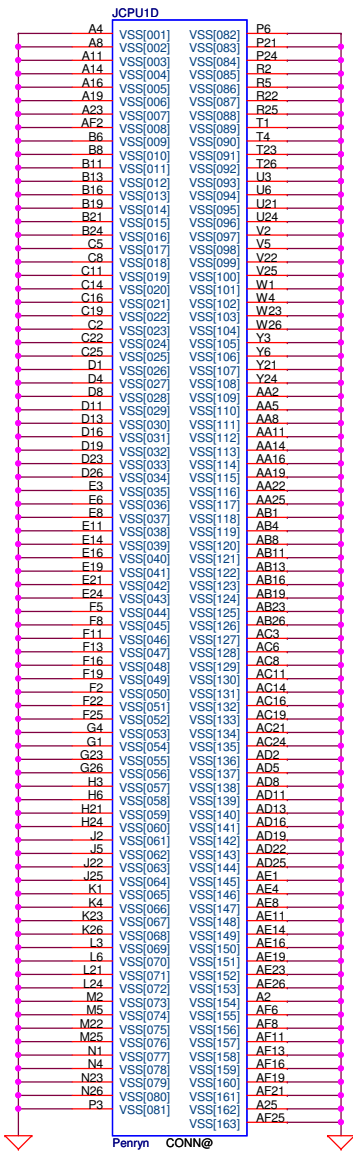
BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

FAN1 Conn

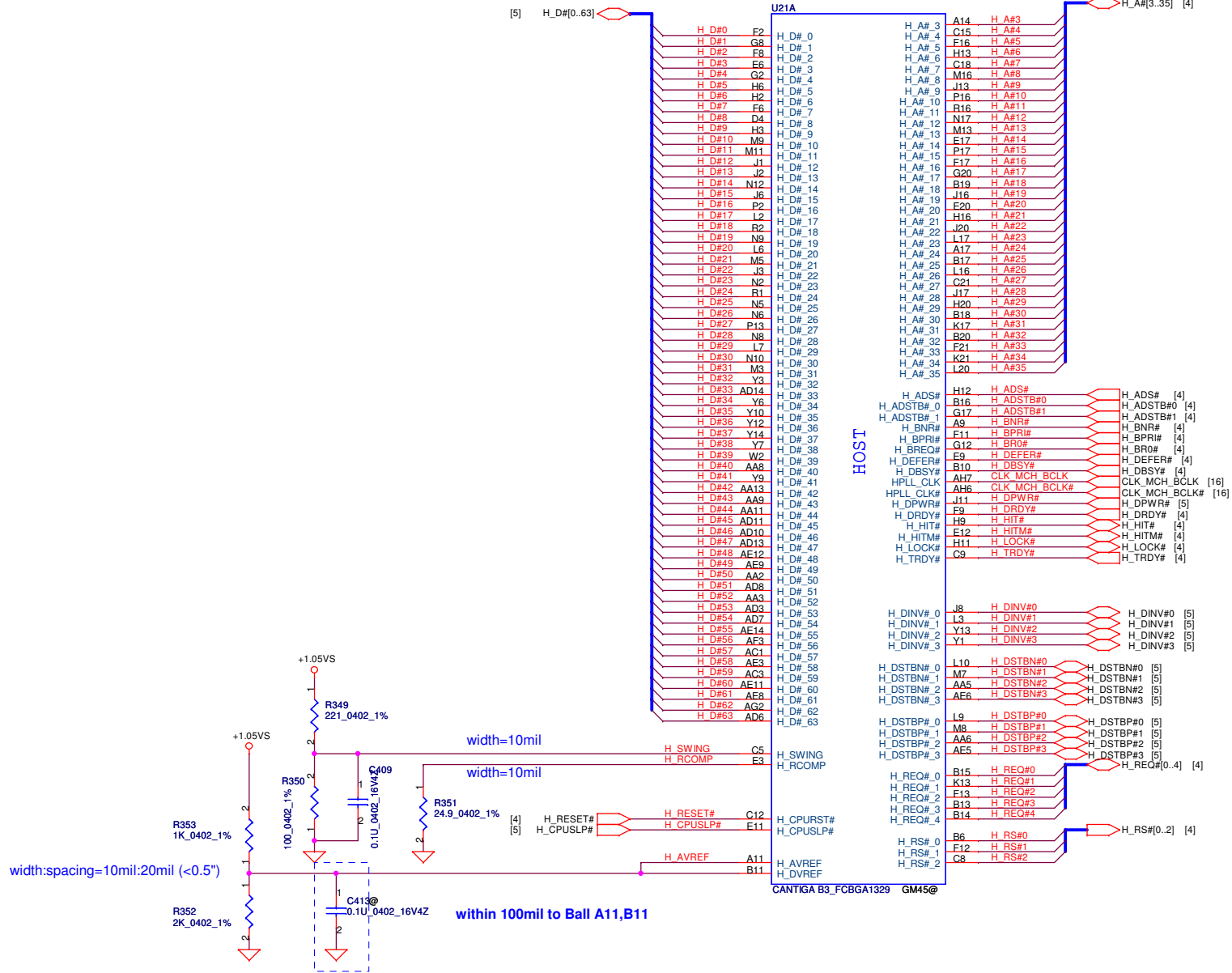


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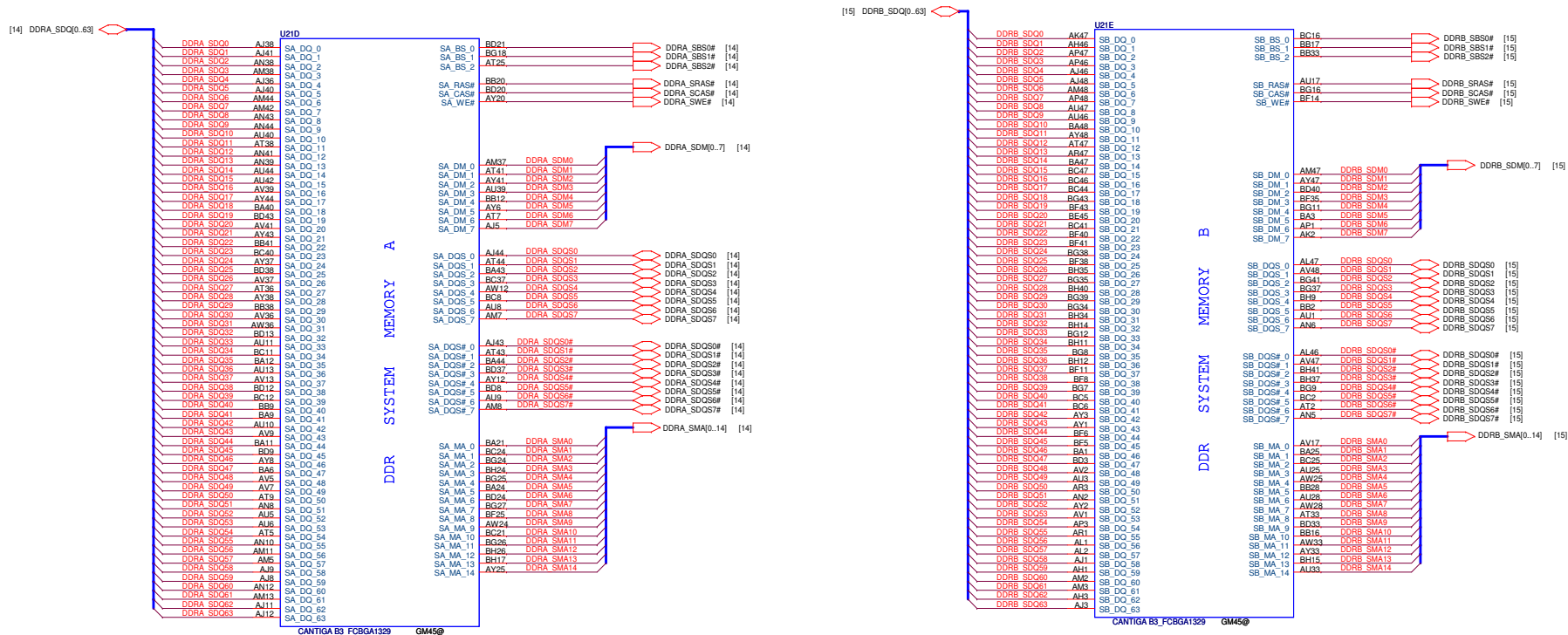


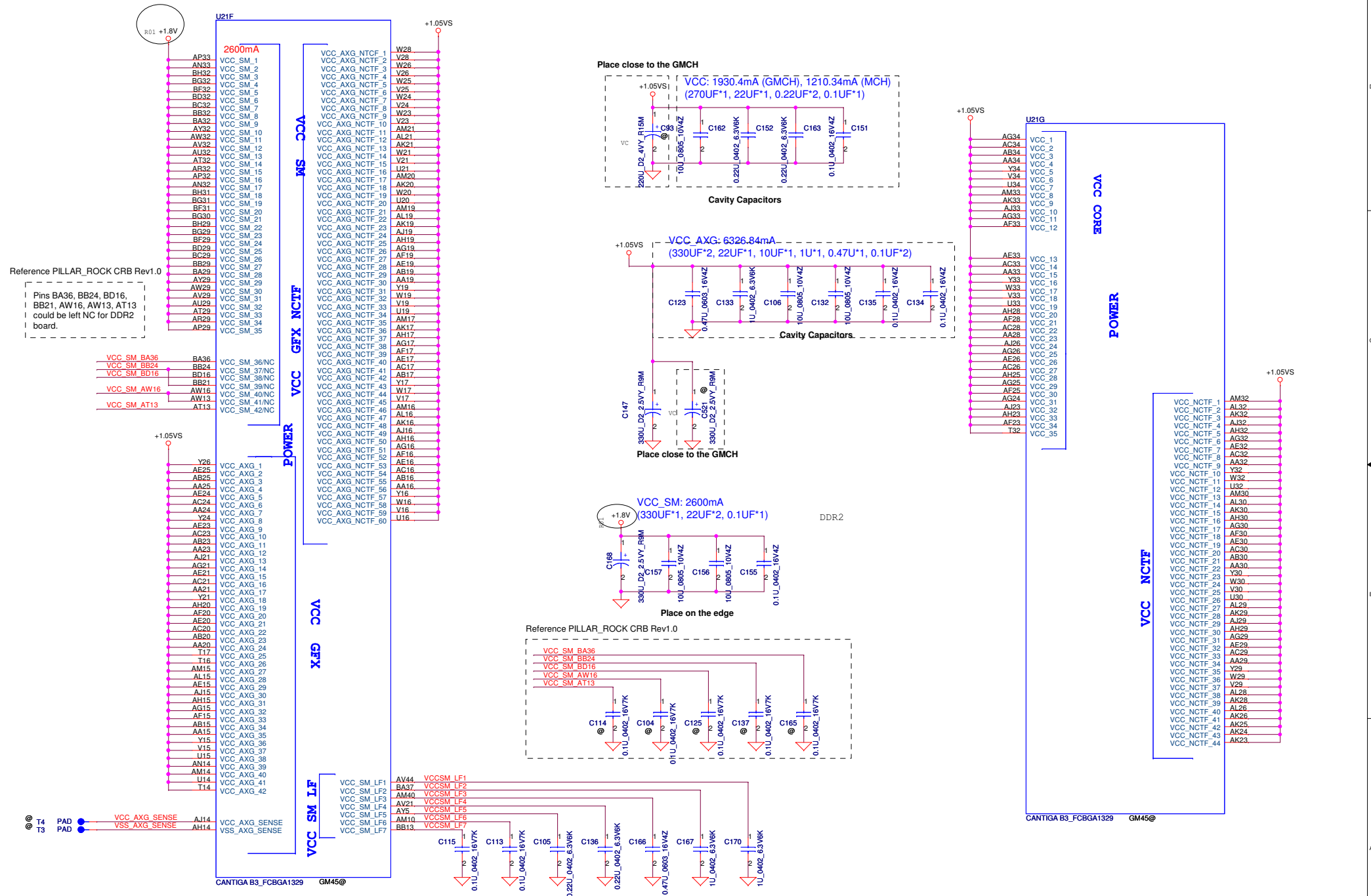


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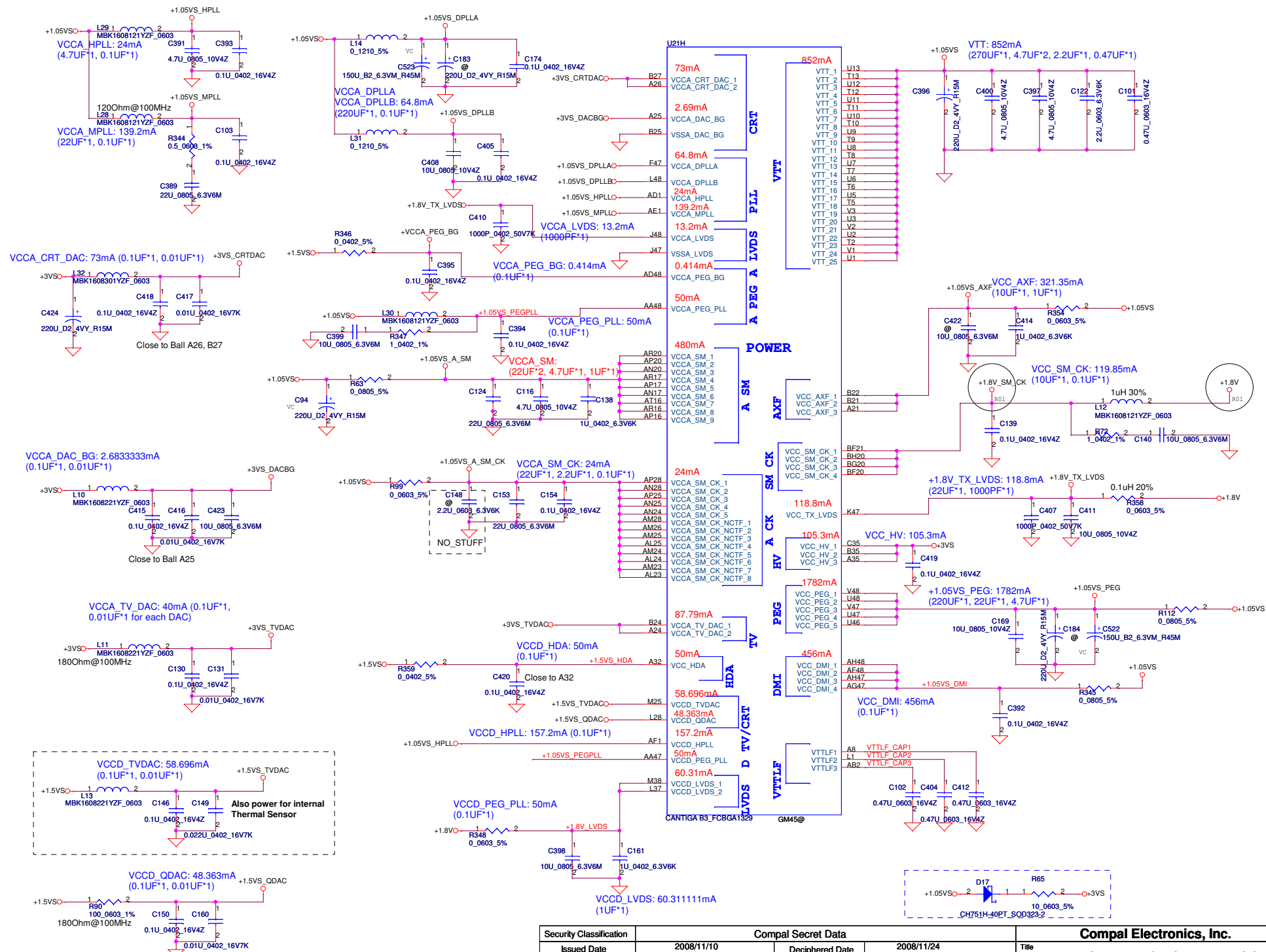


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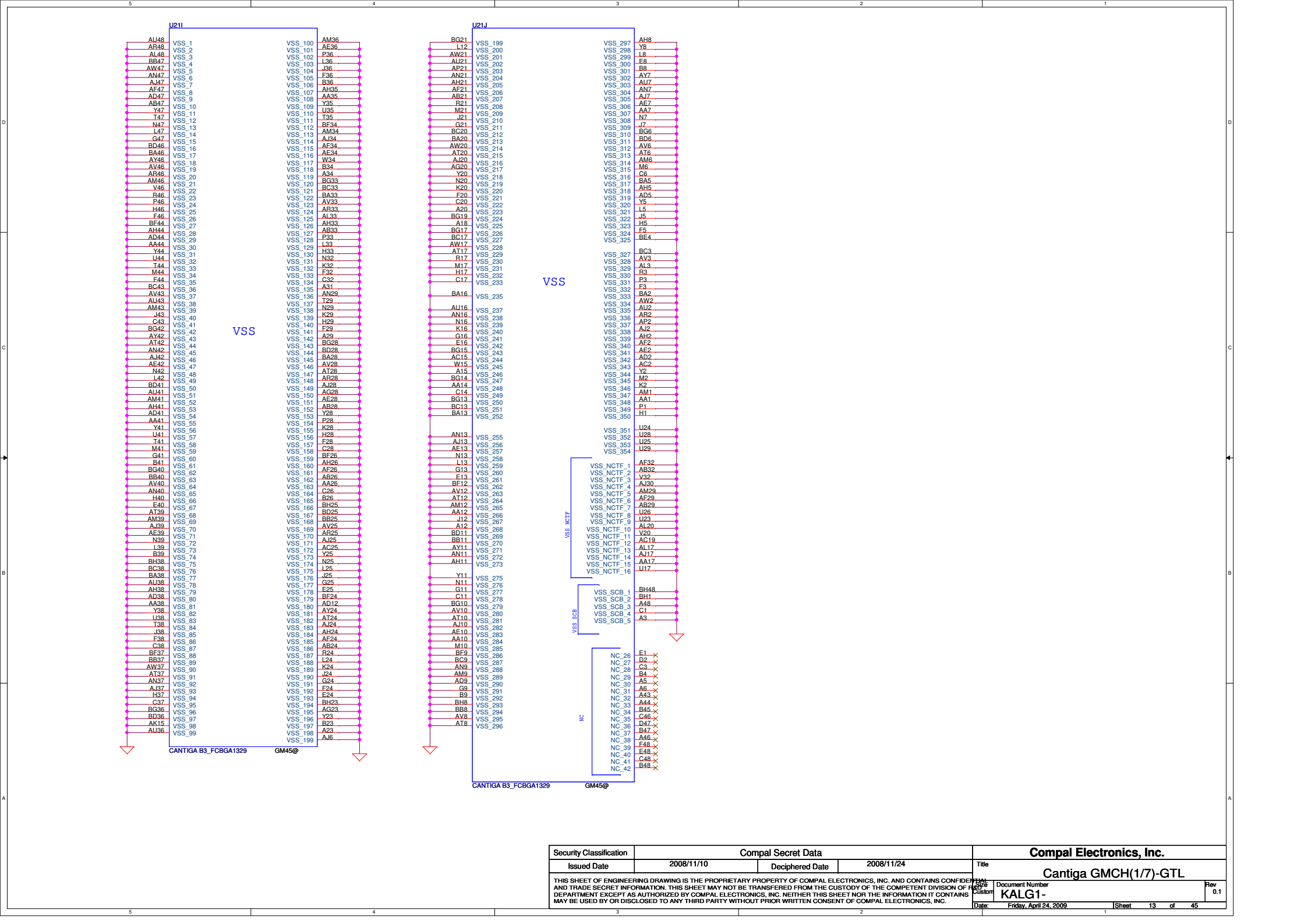


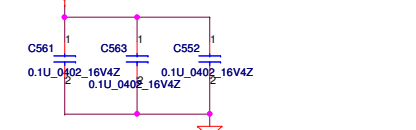
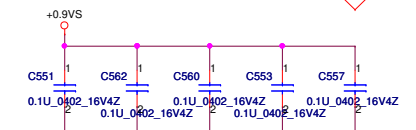
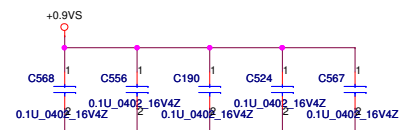
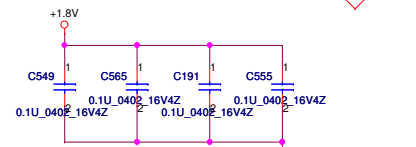
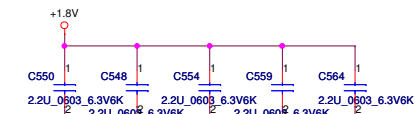
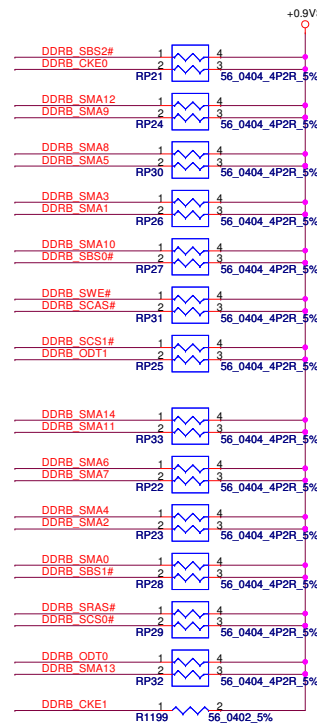
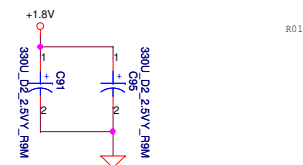
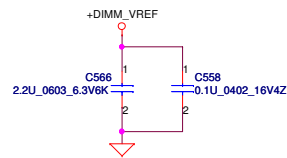
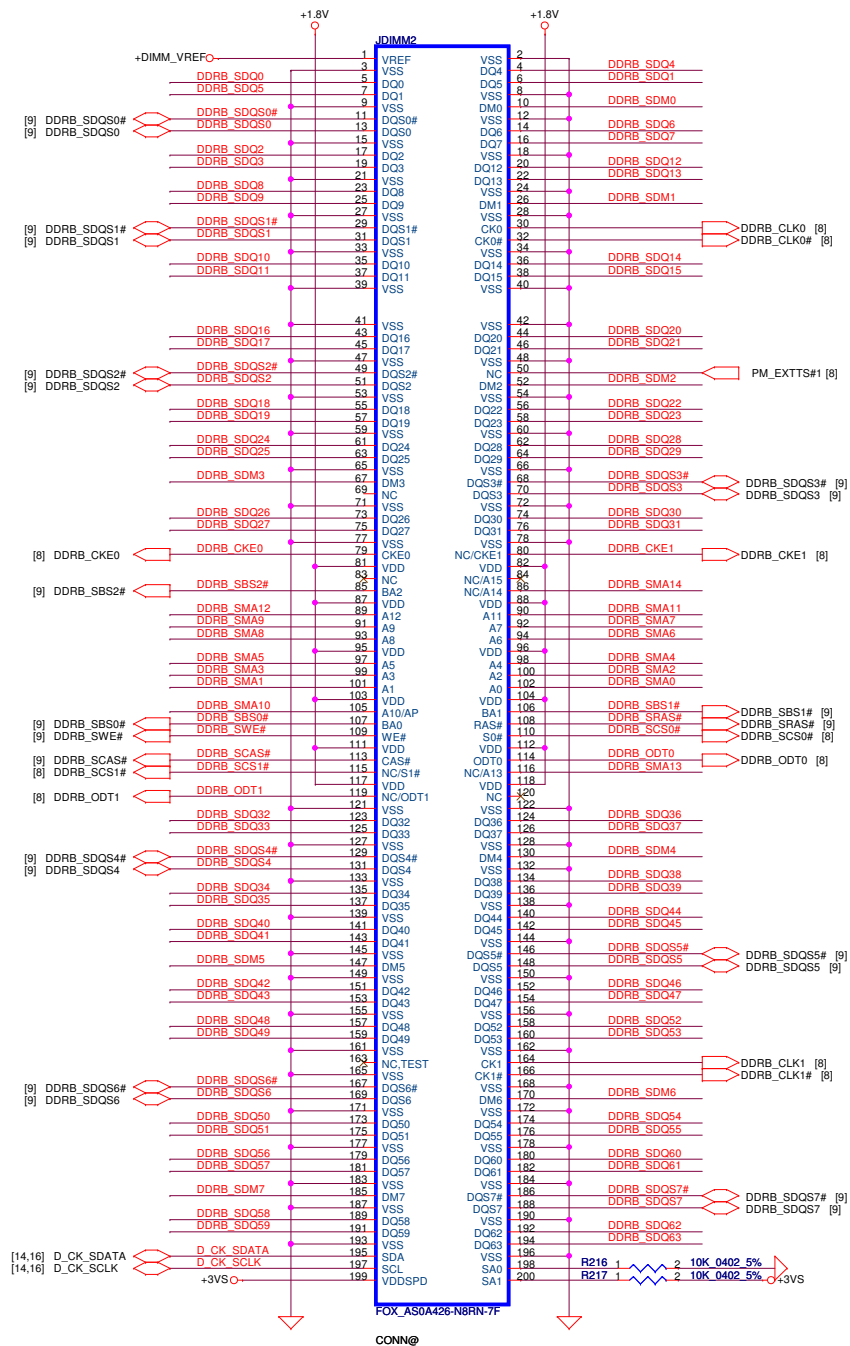


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Compal Electronics, Inc.
DDRII-SODIMM SLOT2

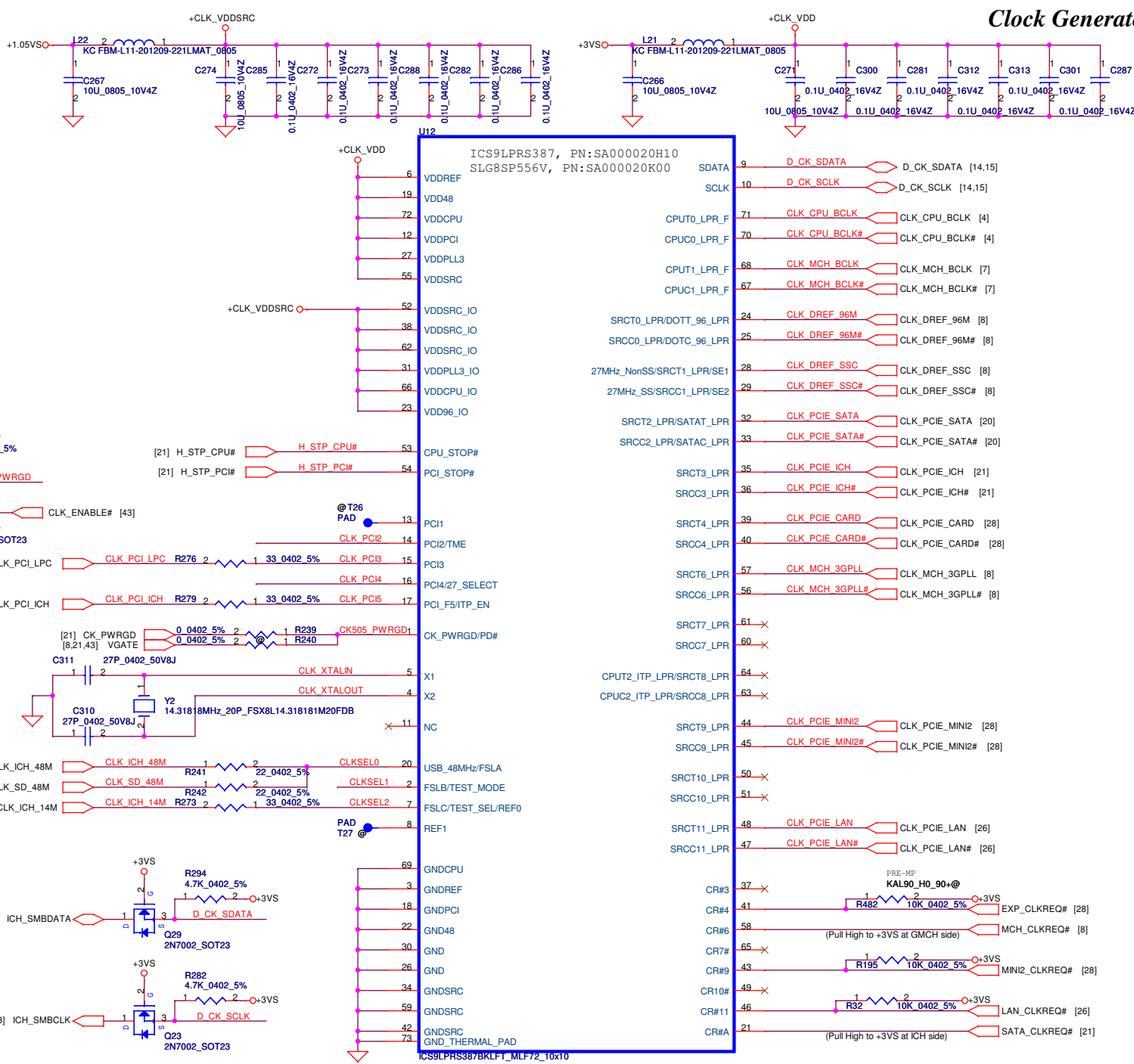
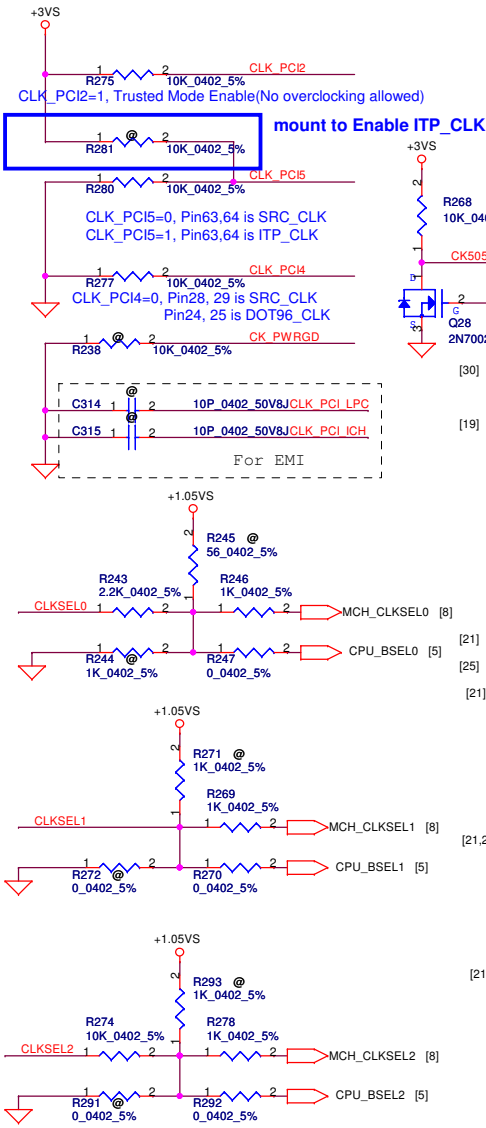
KALGI-

FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
CLKSEL2	CLKSEL1	CLKSEL0			
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

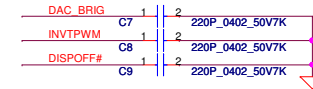
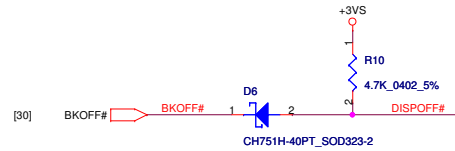
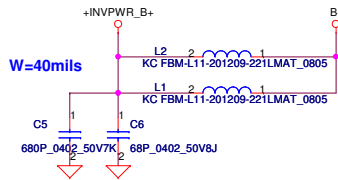
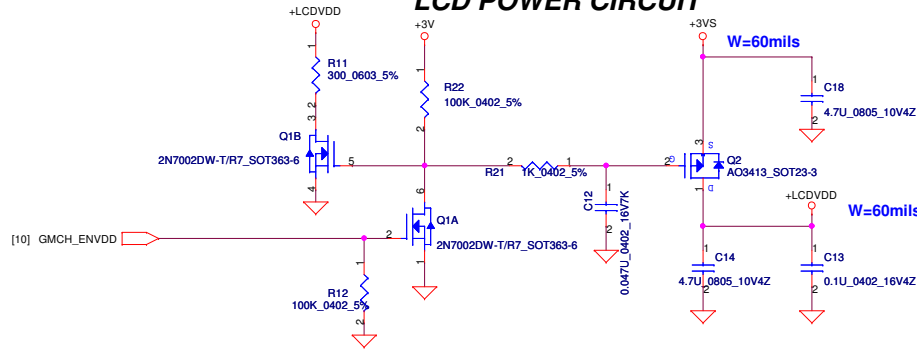
CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

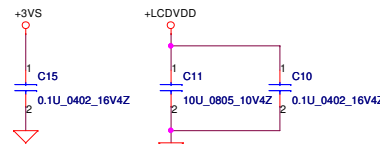
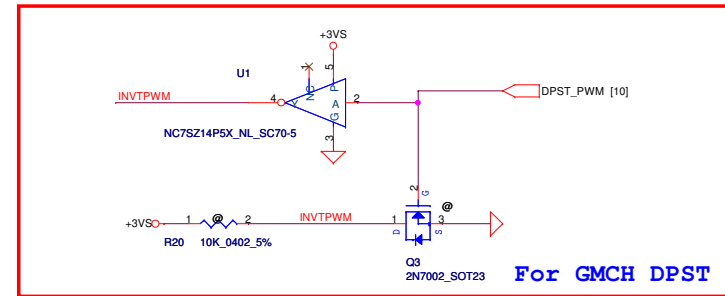
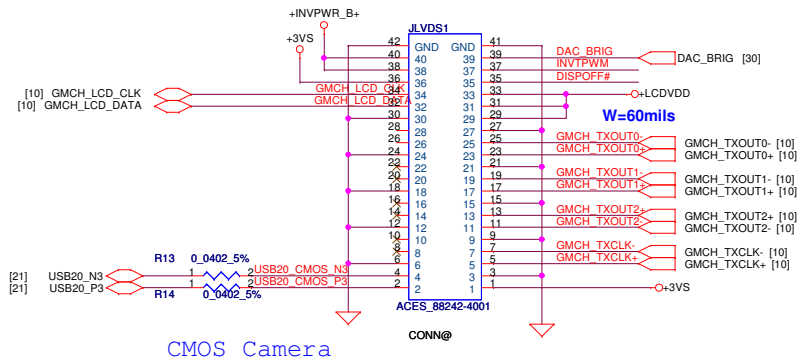


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LCD POWER CIRCUIT

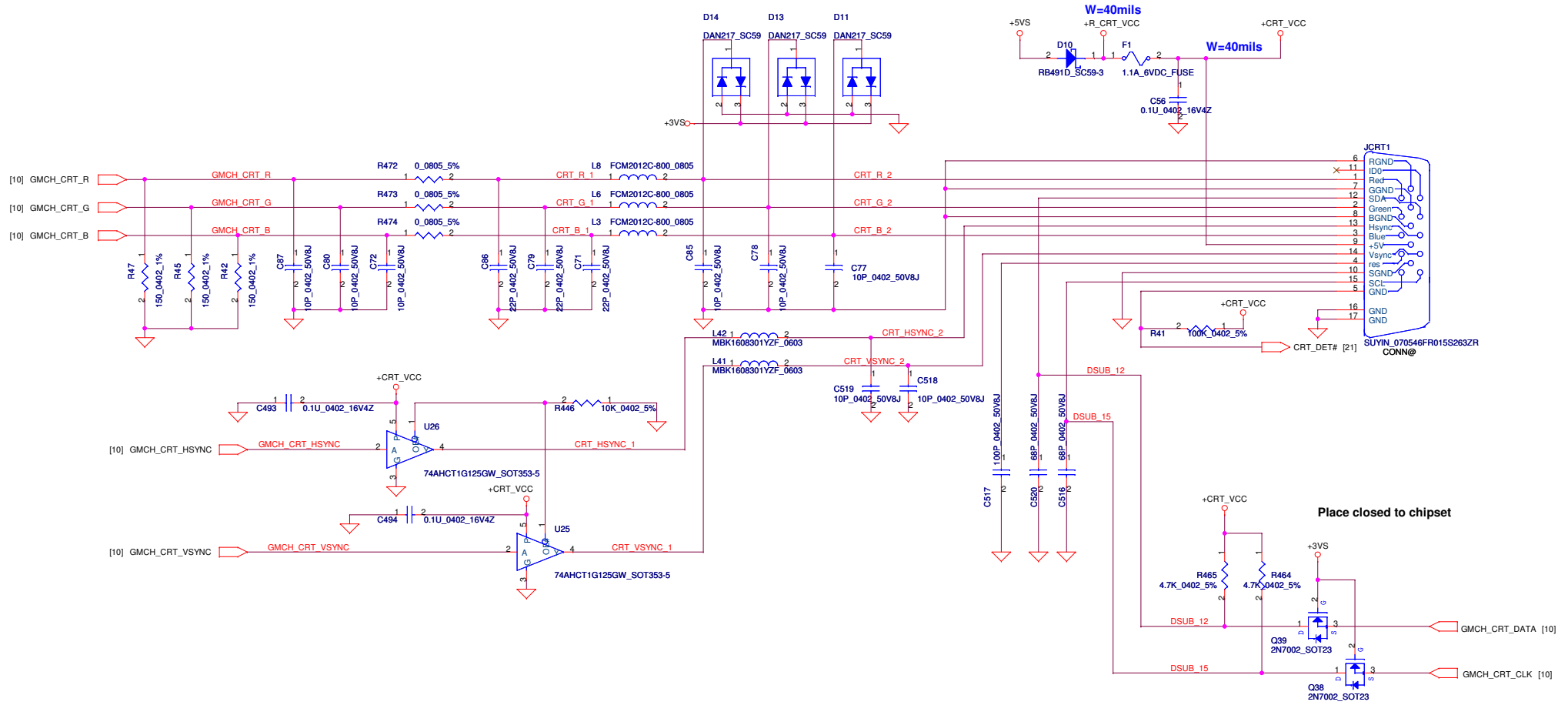


LCD/PANEL BD. Conn.

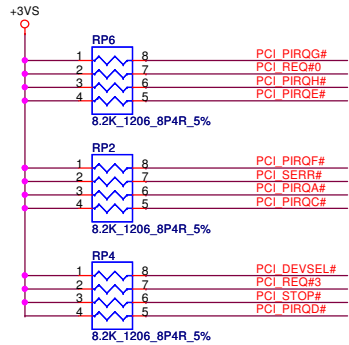
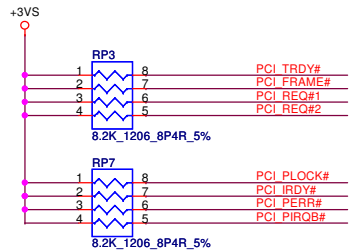


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CRT Connector

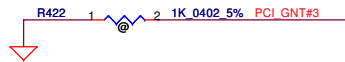


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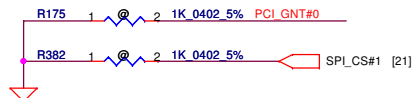


A16 Swap Override Strap

PCI_GNT#3 Low= A16 swap override Enable
High= Default*

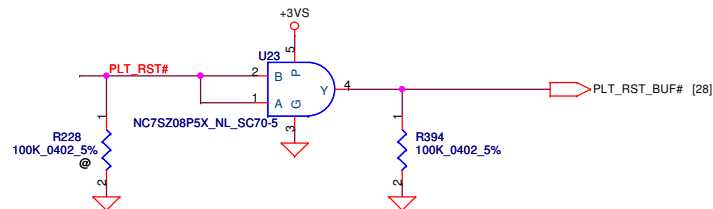
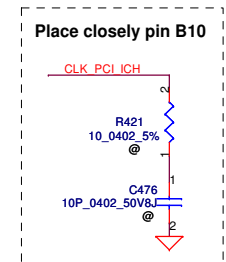
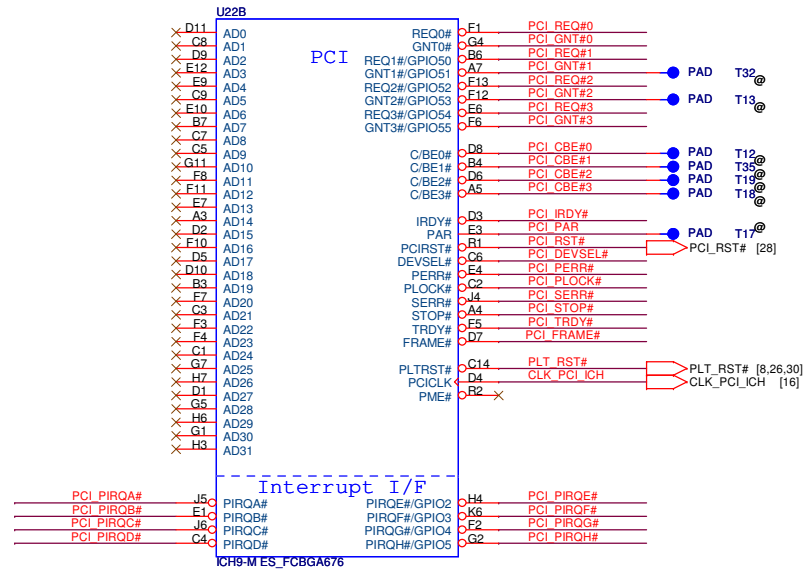


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



DMI for ESI-compatible operation

PCI_GNT#1 Low= DMI for ESI-compatible operation
High= Default* (Internal pull-up)

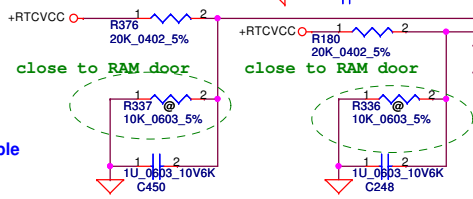
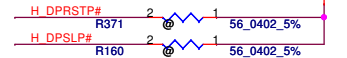


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CMOS Settings	R337
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R336
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN

Reset r1290 for power on then shut down issue



SATA for HDD

SATA for ODD

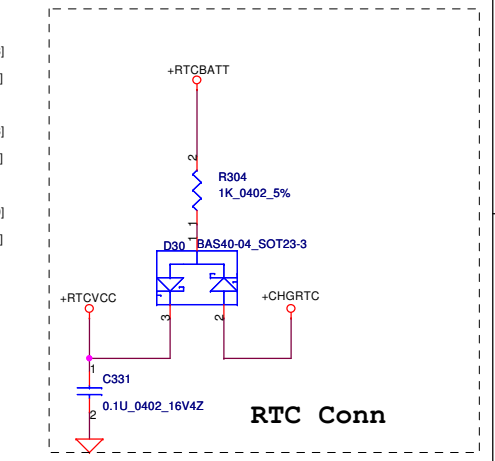
HDA for AUDIO

HDA for GMCH

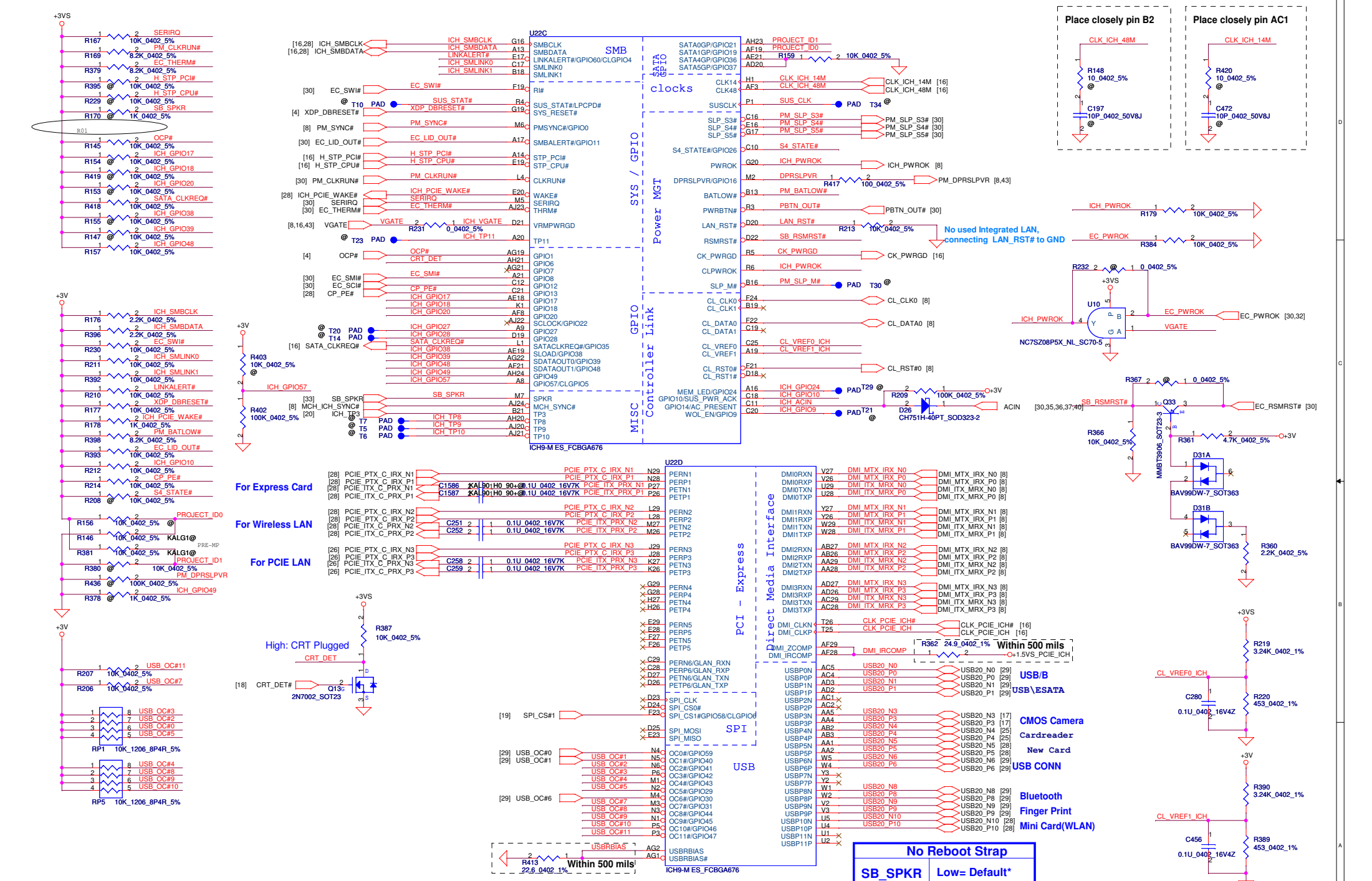
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

Security Classification		Compal Secret Data	
Issued Date	2008/11/10	Deciphered Date	2008/11/24
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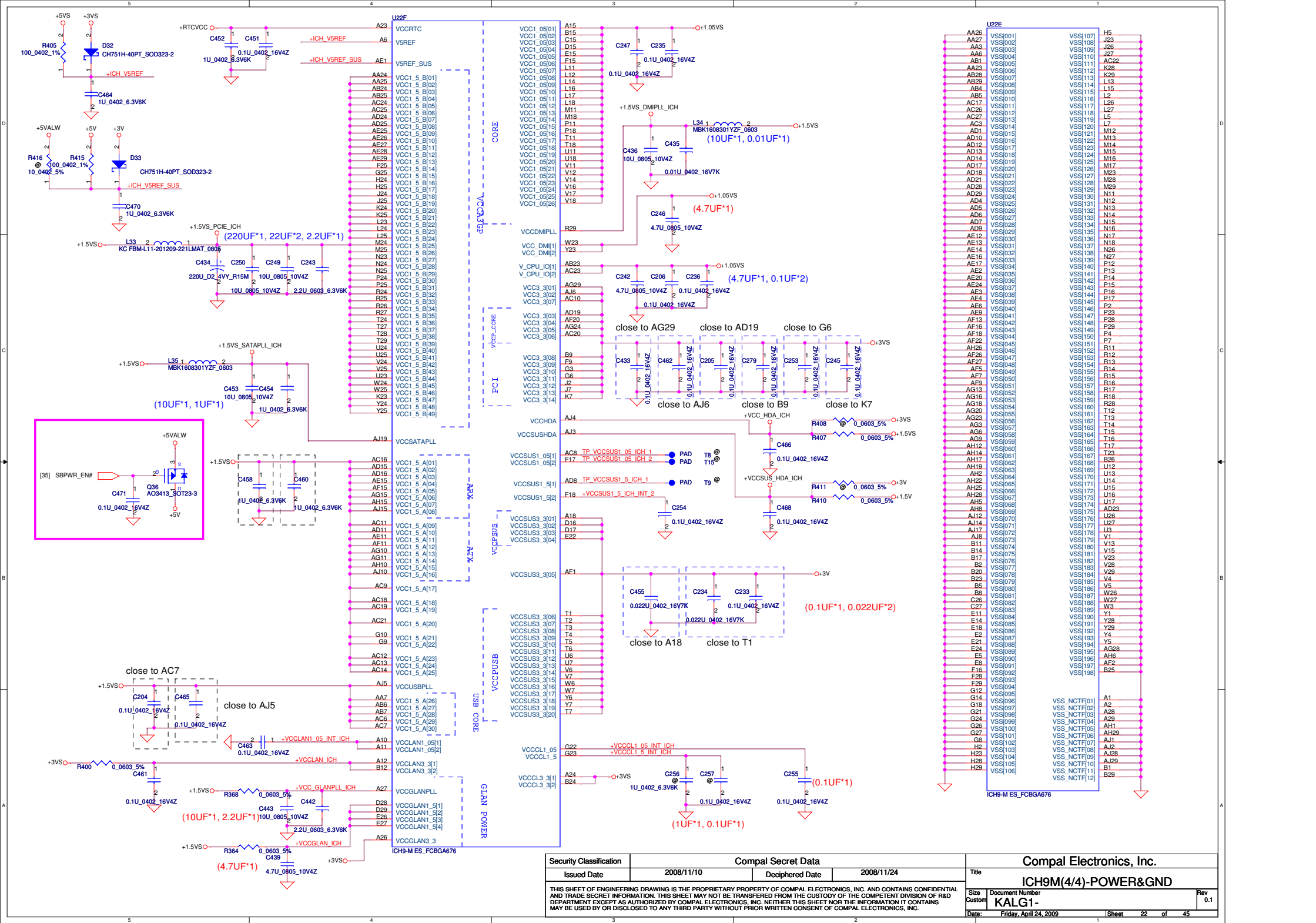
Compal Electronics, Inc.			
Title			
ICH9M(2/4)-LAN, IDELPC, RTC			
Size	Document Number	Rev	
Custom	KALG1-	0.1	
Date:	Friday, April 24, 2009	Sheet	20 of 45



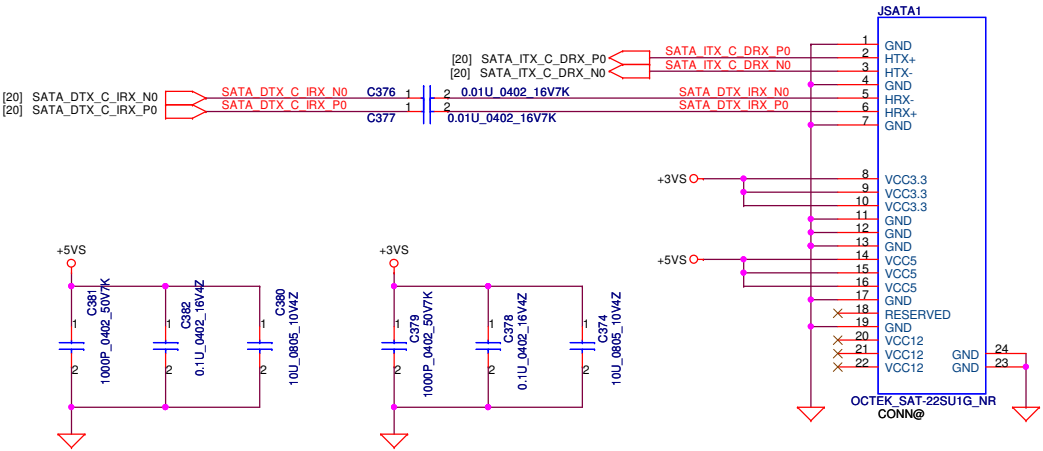
Internal TPM Strap		DMI Termination Voltage	
SPI_MOSI	Low= Disable* High= ITPM enable by MCH strap	GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

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Issued Date	2008/11/10	Deciphered Date	2008/11/24
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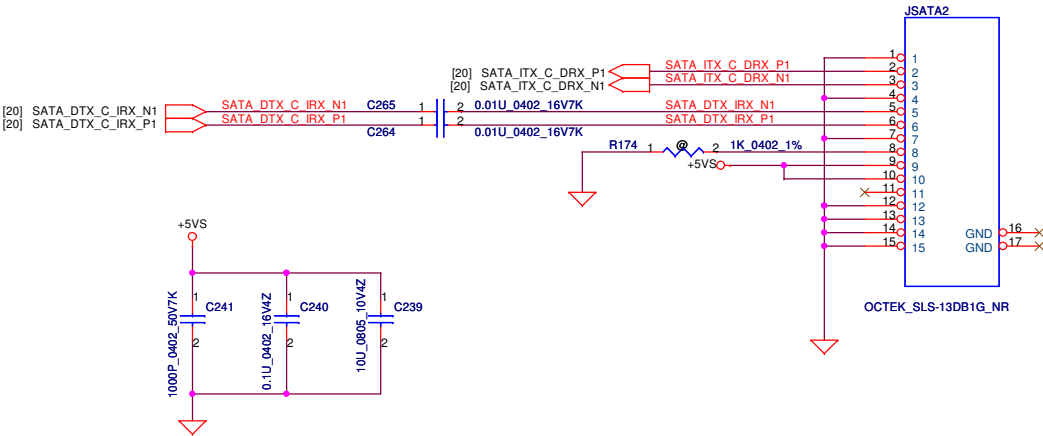
Title		Compal Electronics, Inc.	
ICH9M(3/4)-USB,GPIO,PCIE		Customer	
KALG1-		Rev 0.1	
Date: Friday, April 24, 2009		Sheet 21 of 45	



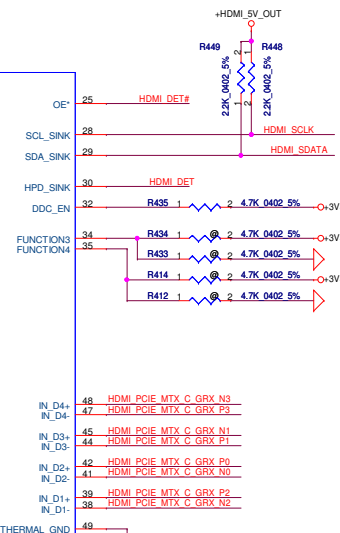
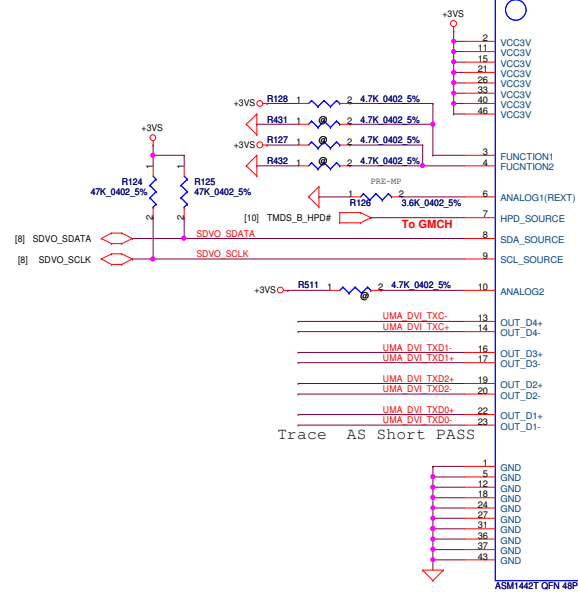
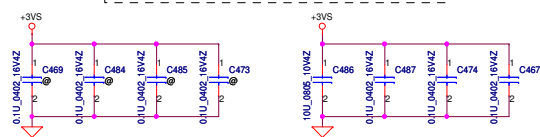
SATA HDD Conn.



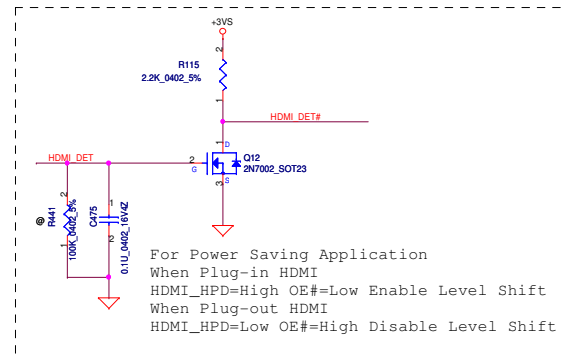
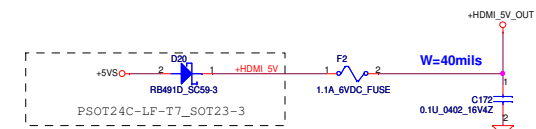
SATA ODD Conn.



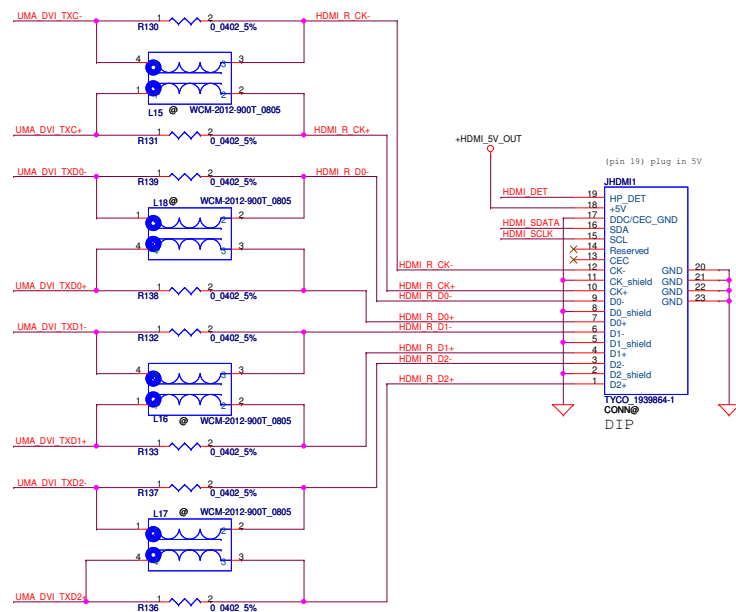
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2008/11/10		Deciphered Date		2008/11/24		Title			
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						Size	Document Number			Rev	
						Custom	KALG1-			0.1	
						Date:	Friday, April 24, 2009		Sheet 23 of 45		



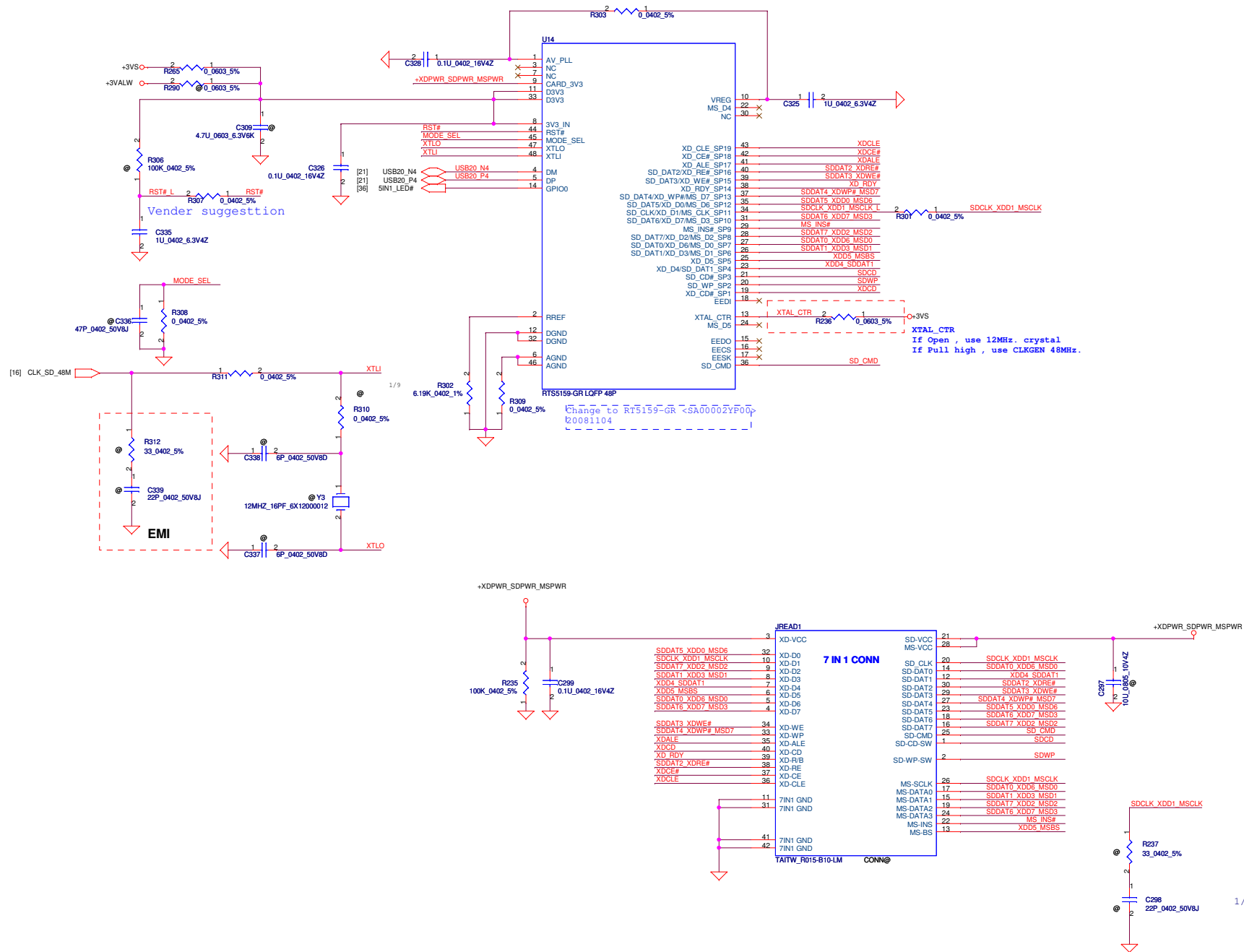
20071031:
Add U1. 49 (THERMAL_GND) to GND Plane

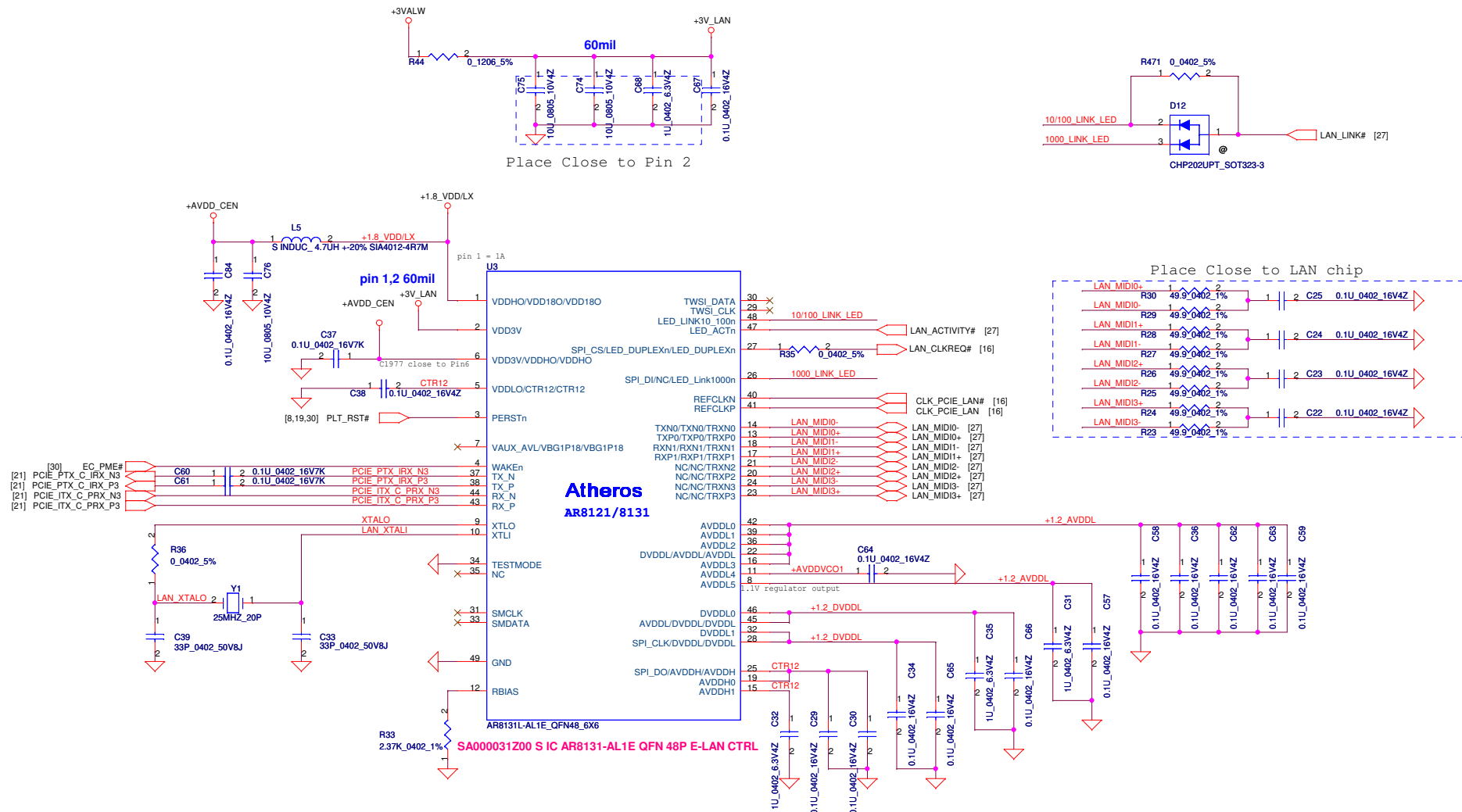


<u>HDMI_PCIE_MTX_C_GRX_N[0..3]</u>		HDMI_PCIE_MTX_C_GRX_N[0..3]	[10]
<u>HDMI_PCIE_MTX_C_GRX_P[0..3]</u>		HDMI_PCIE_MTX_C_GRX_P[0..3]	[10]



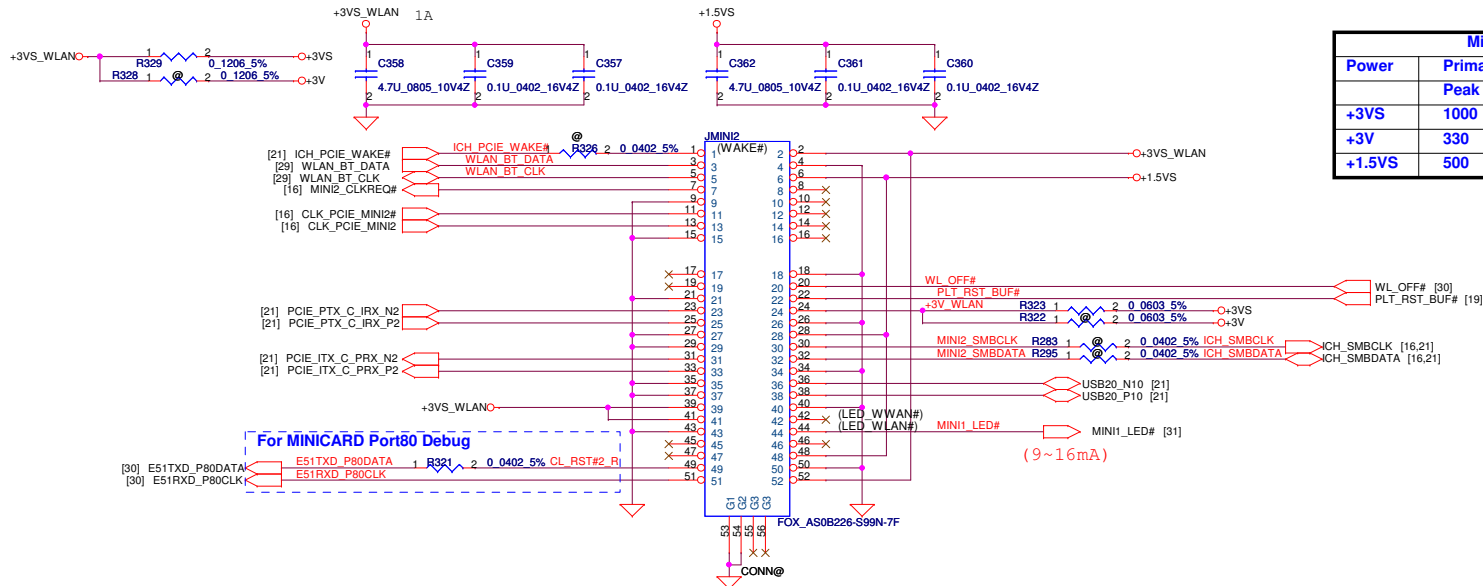
Intel Cantiga TMDs Pin Definition	
TMDs_B_CLK	PEG_TXP_3
TMDs_B_CLK#	PEG_TXN_3
TMDs_B_DATA0	PEG_TXP_2
TMDs_B_DATA0#	PEG_TXN_2
TMDs_B_DATA1	PEG_TXP_1
TMDs_B_DATA1#	PEG_TXN_1
TMDs_B_DATA2	PEG_TXP_0
TMDs_B_DATA2#	PEG_TXN_0
TMDs_B_HPD#	PEG_RXP_3





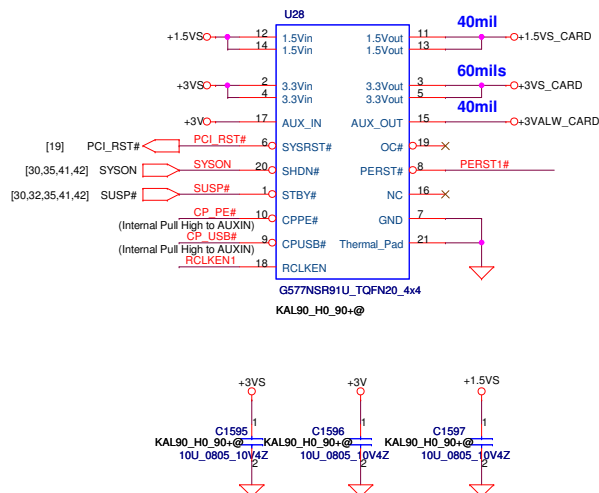
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Issued Date				2008/04/16				Deciphered Date			
								2008/11/24			
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								Atheros AR8131			
								Size			
								Document Number			
								KALG1-			
								Rev			
								0.1			
								Date:			
								Friday, April 24, 2009			
								Sheet			
								26			
								of			
								45			

For Wireless LAN

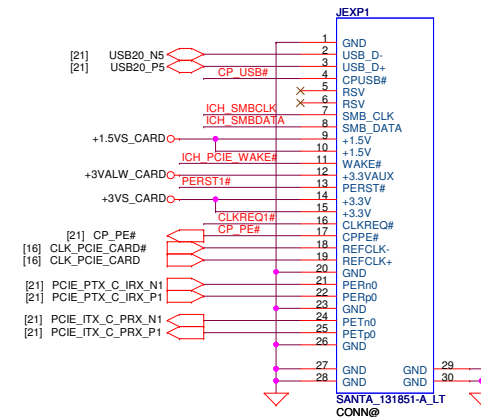
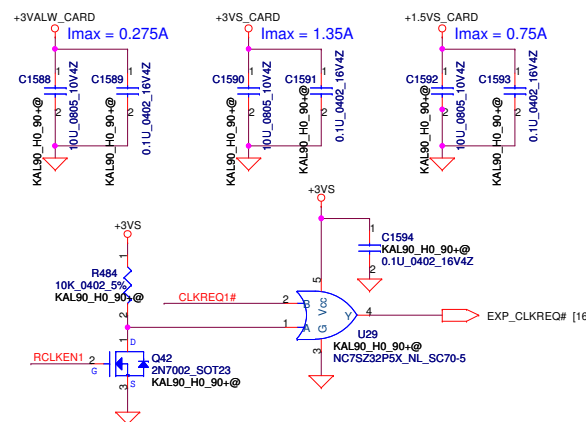


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

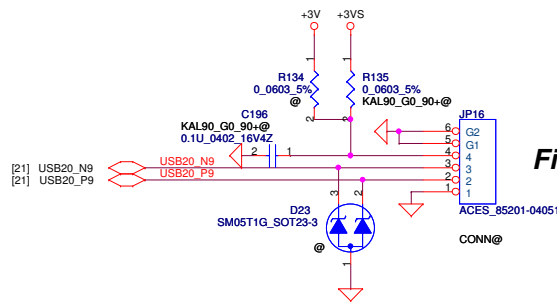
New Card Power Switch



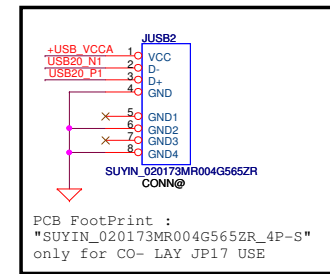
New Card Socket (Left/TOP)



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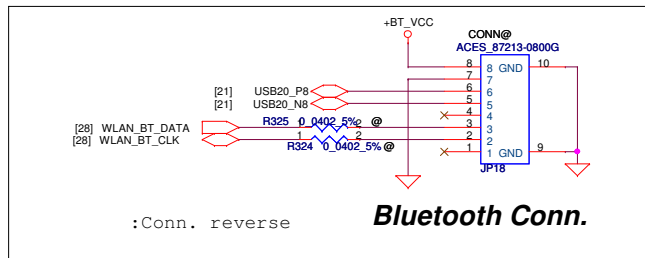
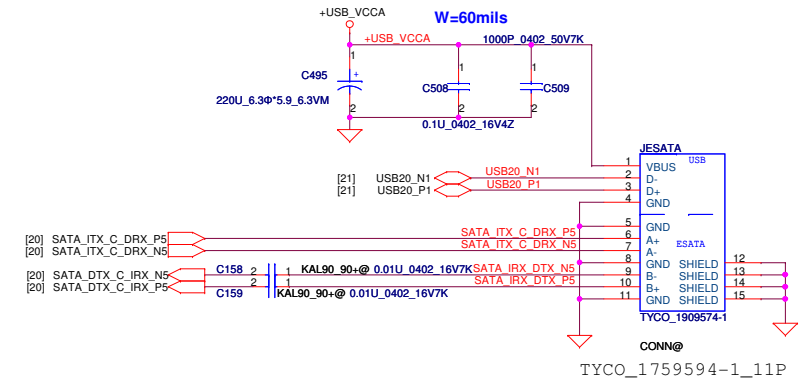
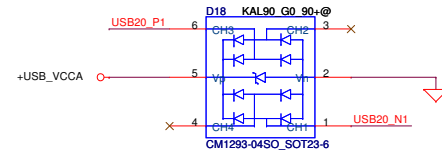
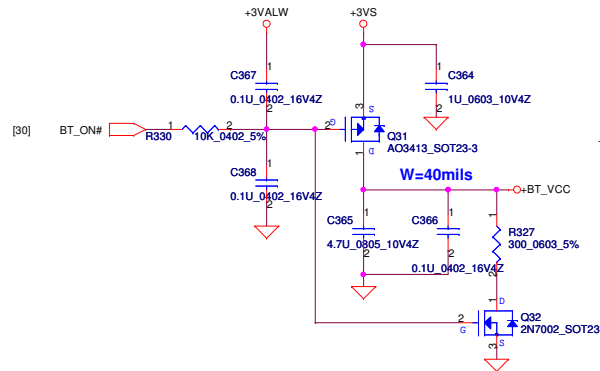


Finger Print Conn.



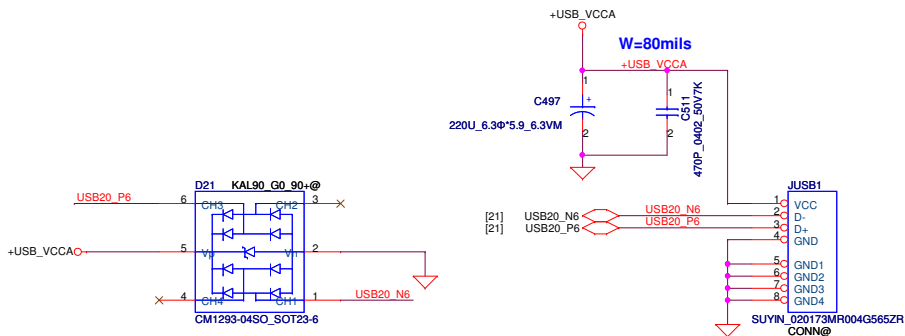
PCB FootPrint :
"SUYIN_020173MR004G5652R_4P-S"
only for CO- LAY JP17 USE

ESATA CONN

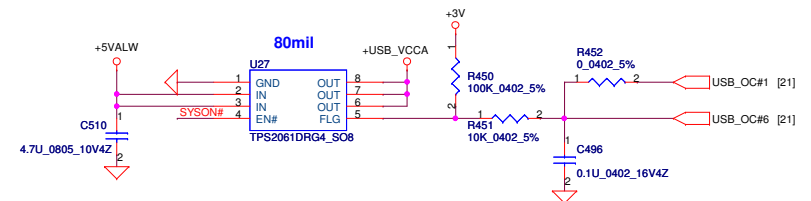


Bluetooth Conn.

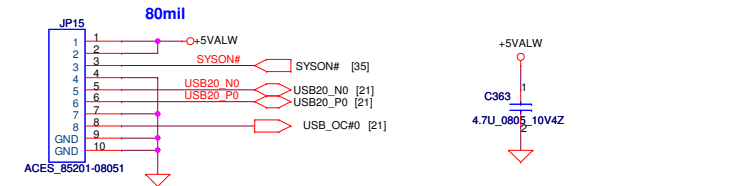
:Conn. reverse



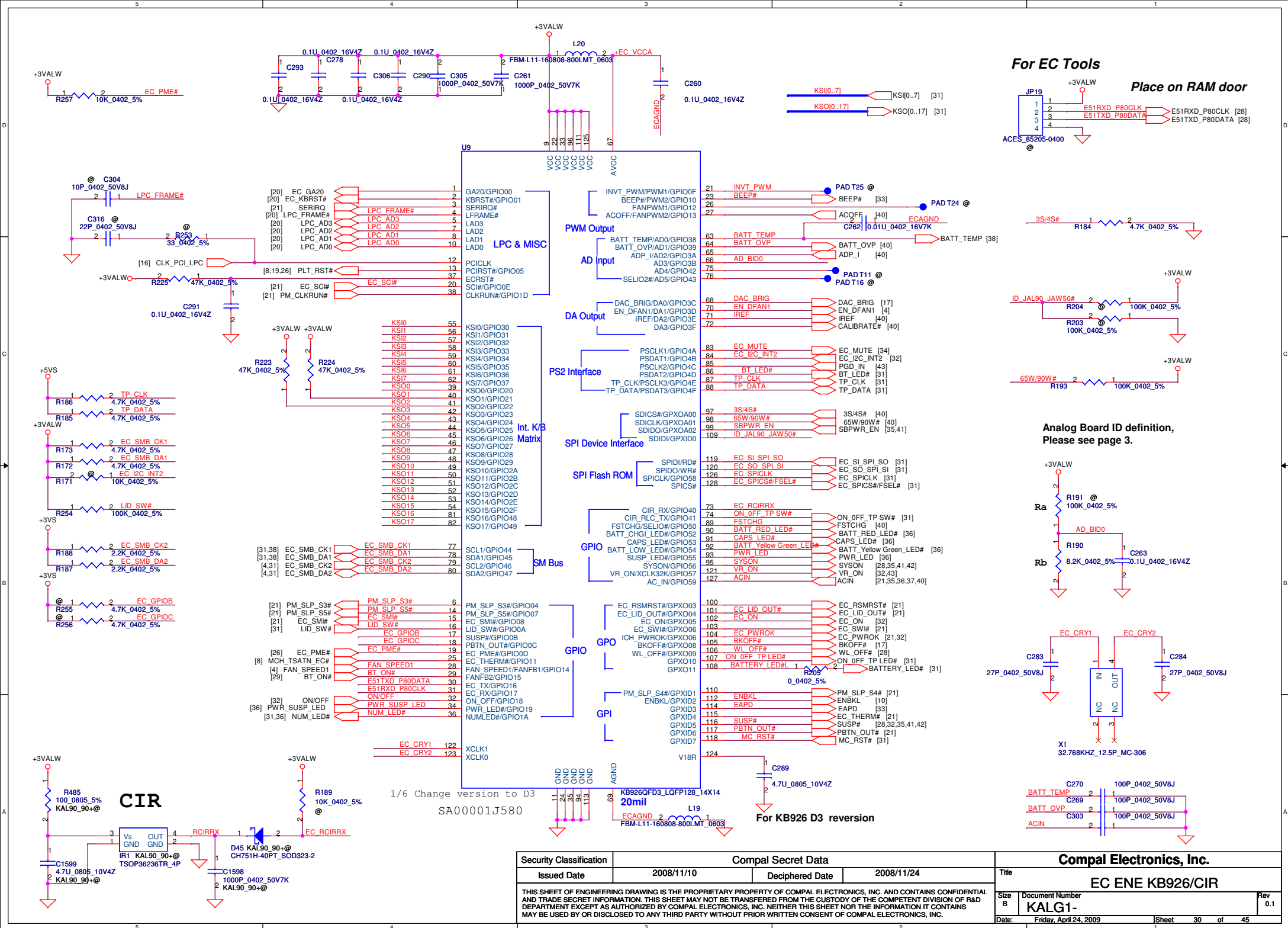
USB CONN.

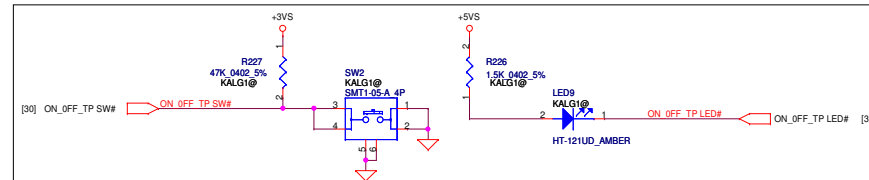
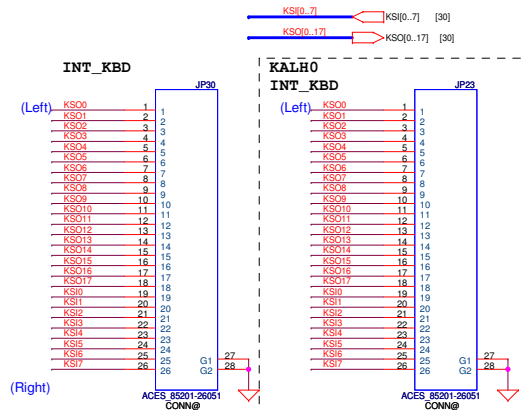
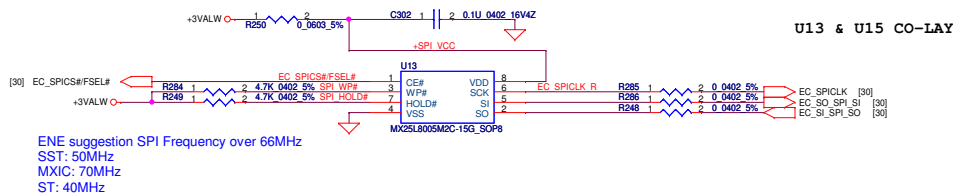


To USB/B Connector

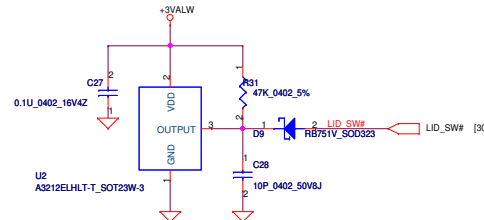


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								Document Number		KALG1-		Rev	
								Date		Friday, April 24, 2009		Sheet 29 of 45	





Lid Switch (Hall Effect Switch)

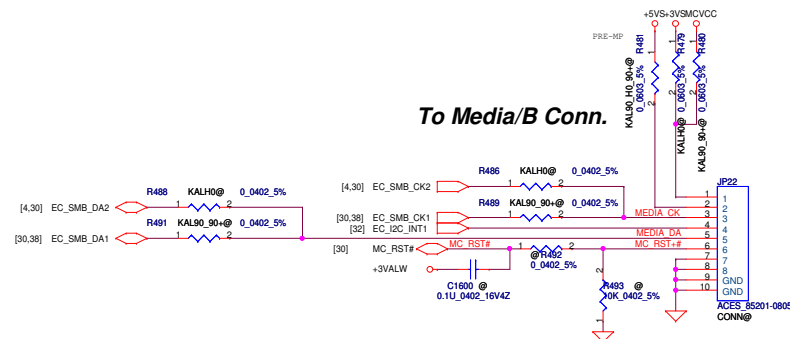


To BTN/B Conn.

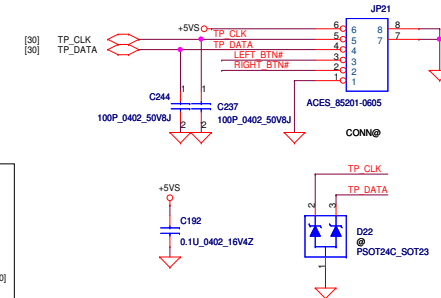
	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)

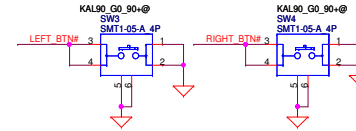
To Media/B Conn.



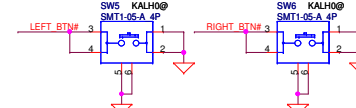
To TP/B Conn.



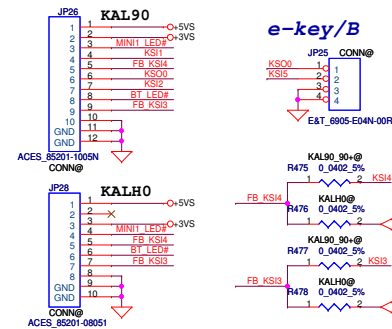
M/B TP SW



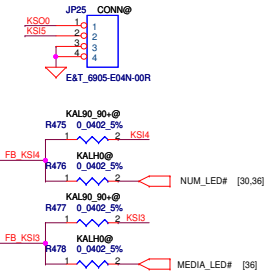
KALHO TP SW



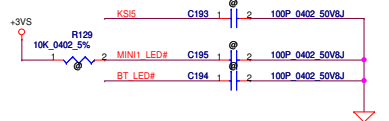
FN/B

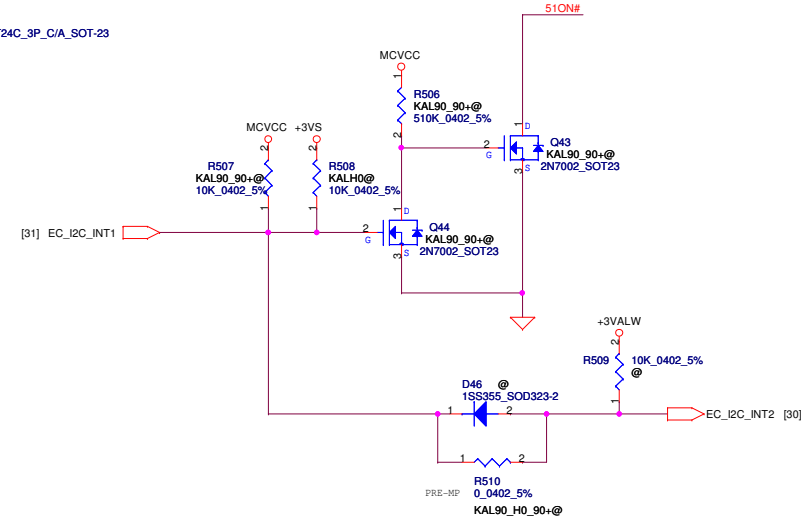
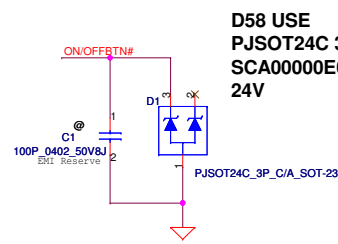
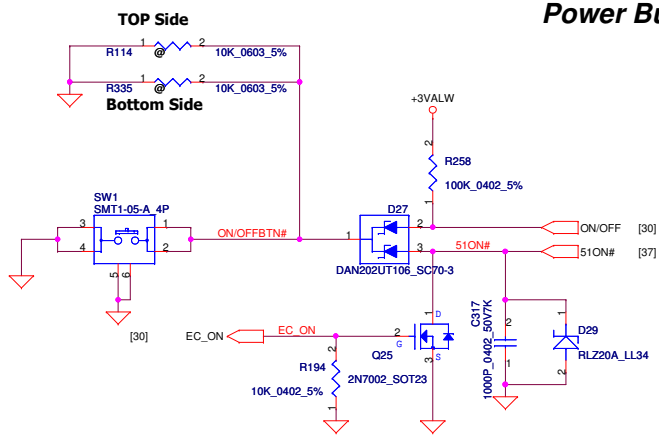


e-key/B



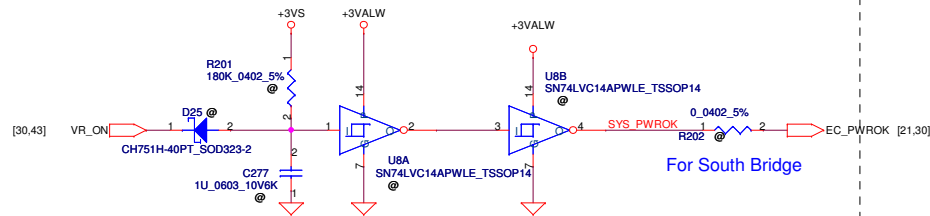
FOR EMI





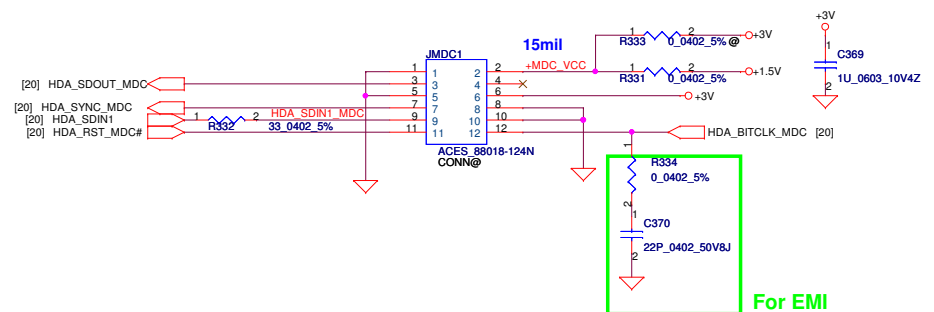
Power ON Circuit

RESERVE R01



For South Bridge

HDA MDC Conn.



For EMI

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Deciphered Date				2008/11/24				Power OK, Reset, MDC			
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Gain= 10dB

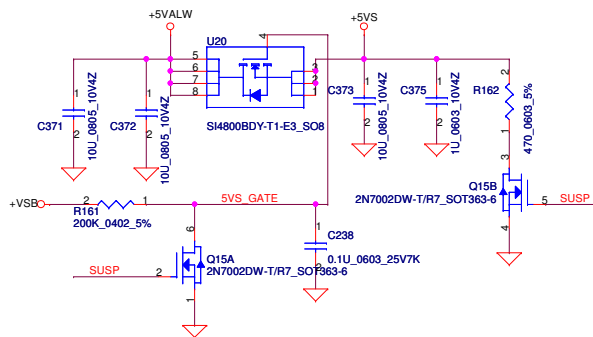
Int. Speaker Conn.

(HDA Jack)
MIC JACK

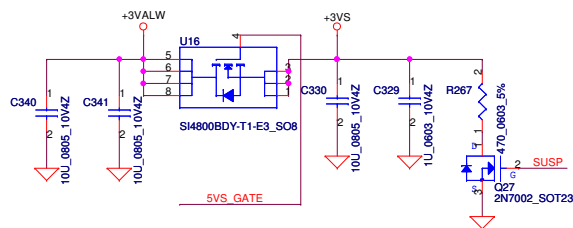
(HDA Jack)
LINE-IN JACK

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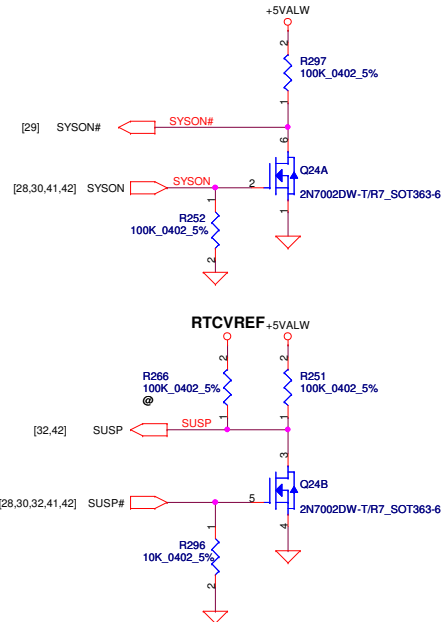
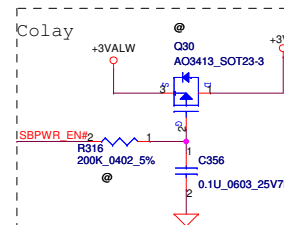
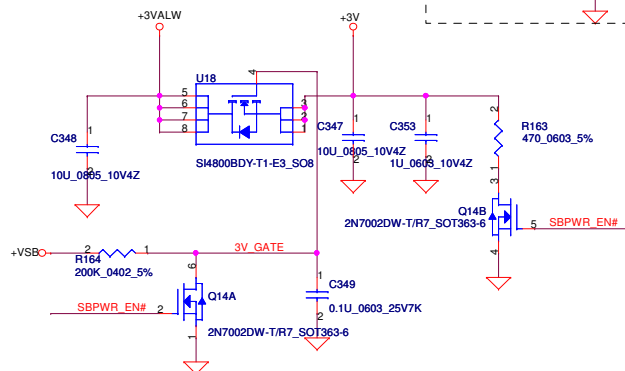
+5VALW TO +5VS



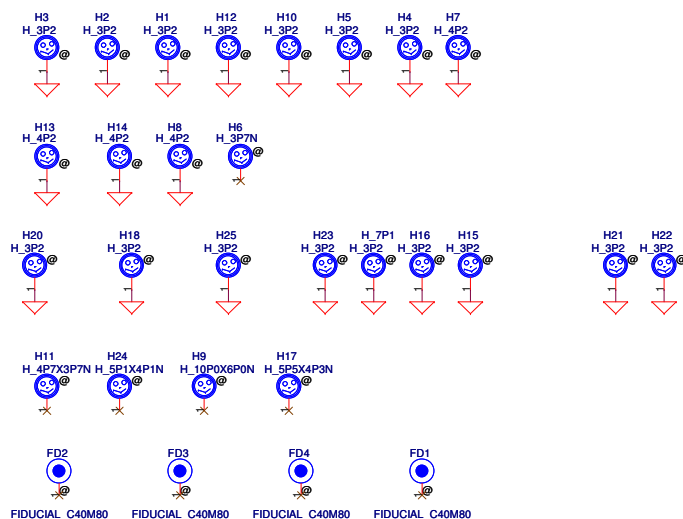
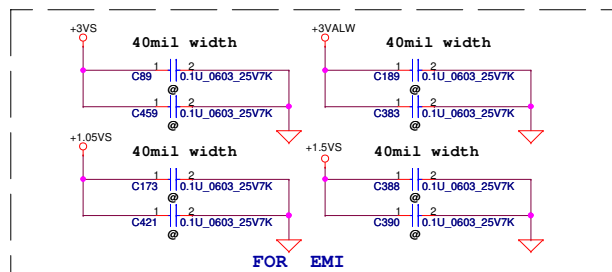
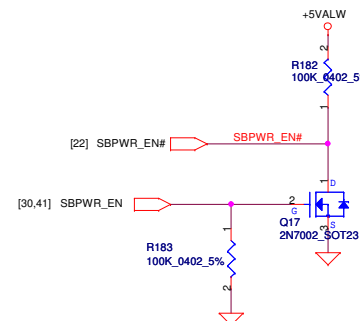
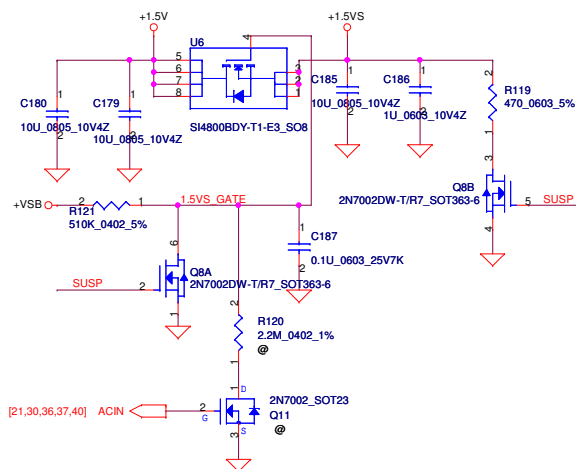
+3VALW TO +3VS



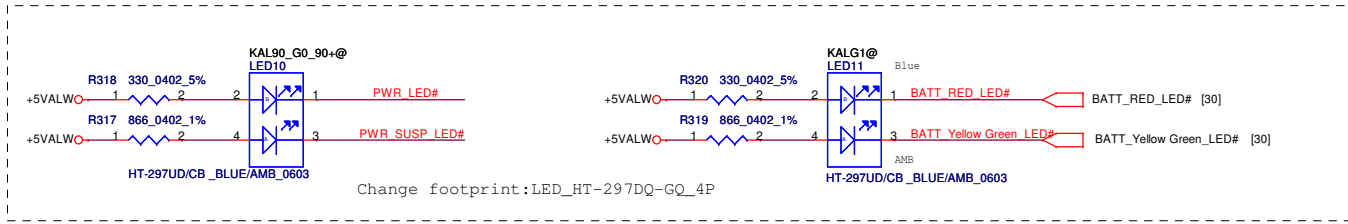
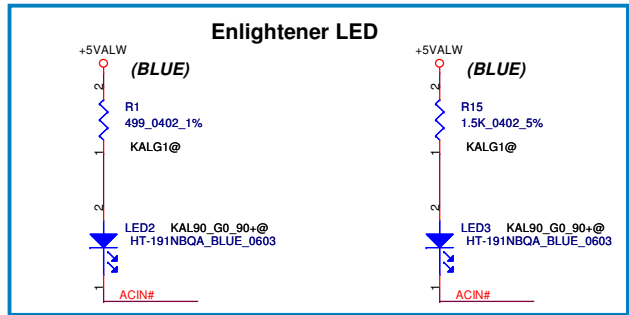
+3VALW TO +3V_SB(ICH8M AUX Power)



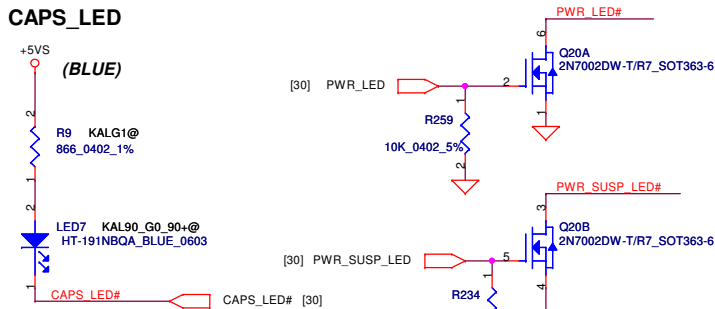
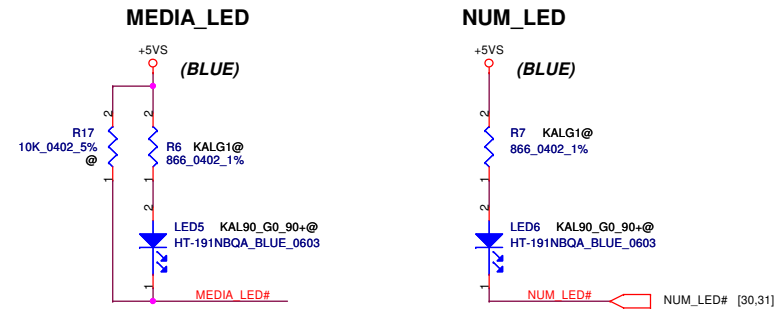
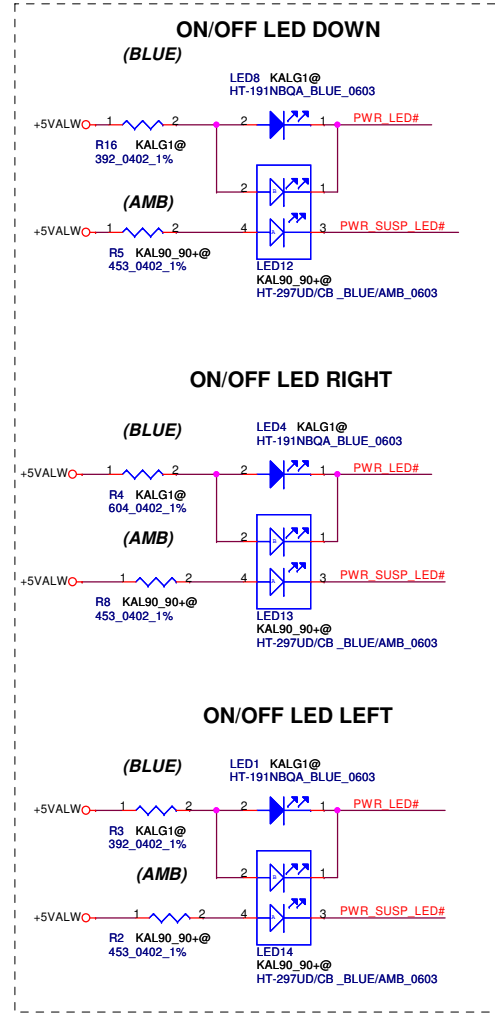
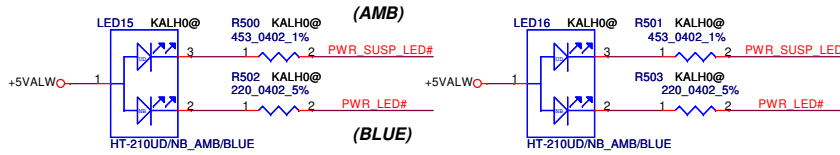
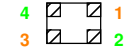
+1.5V to +1.5VS



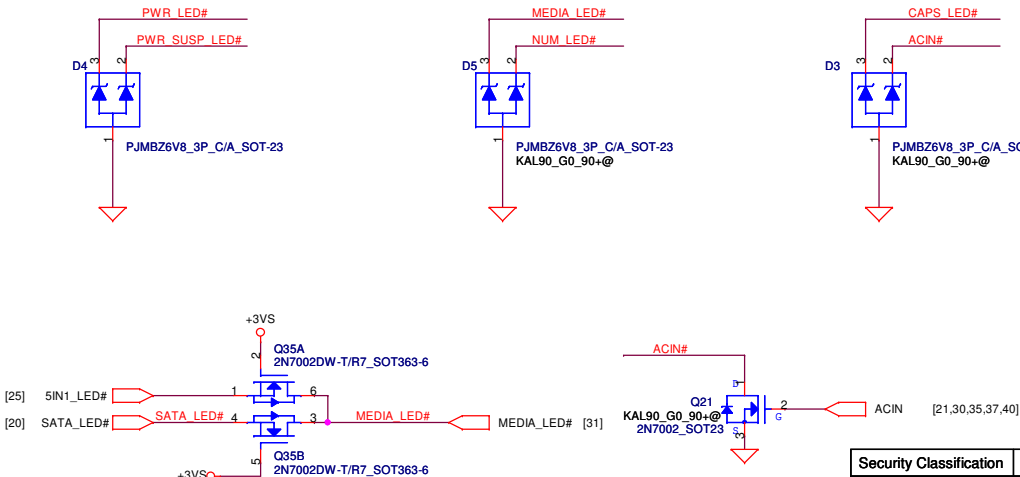
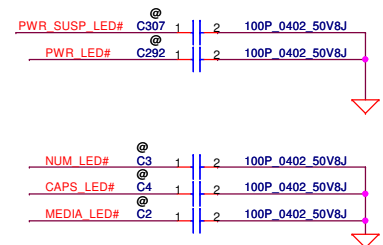
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Compal Footprint

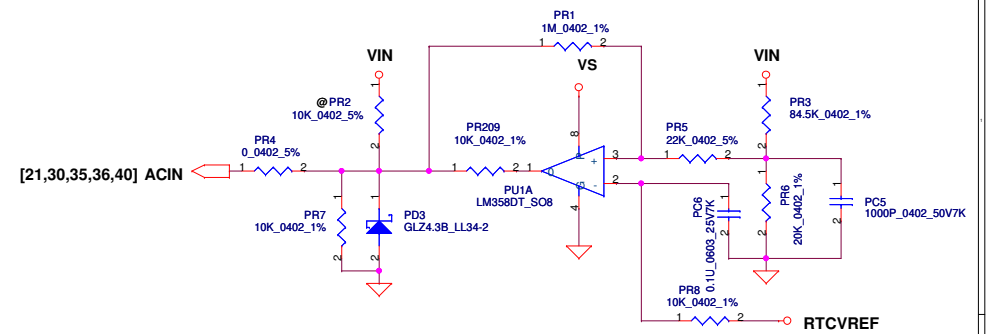
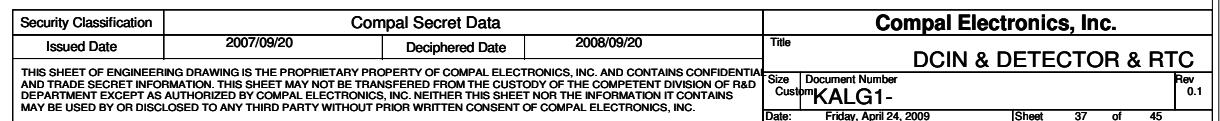
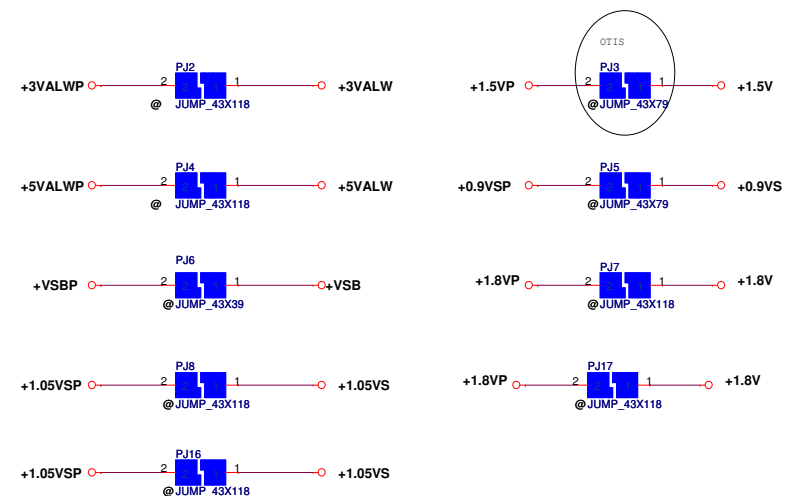


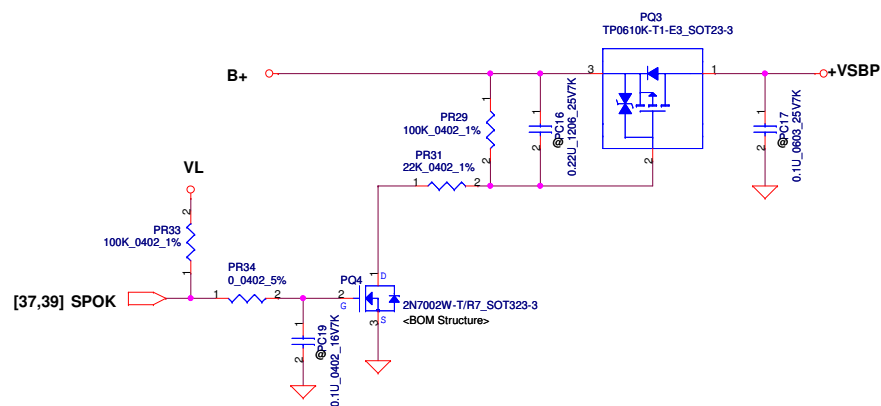
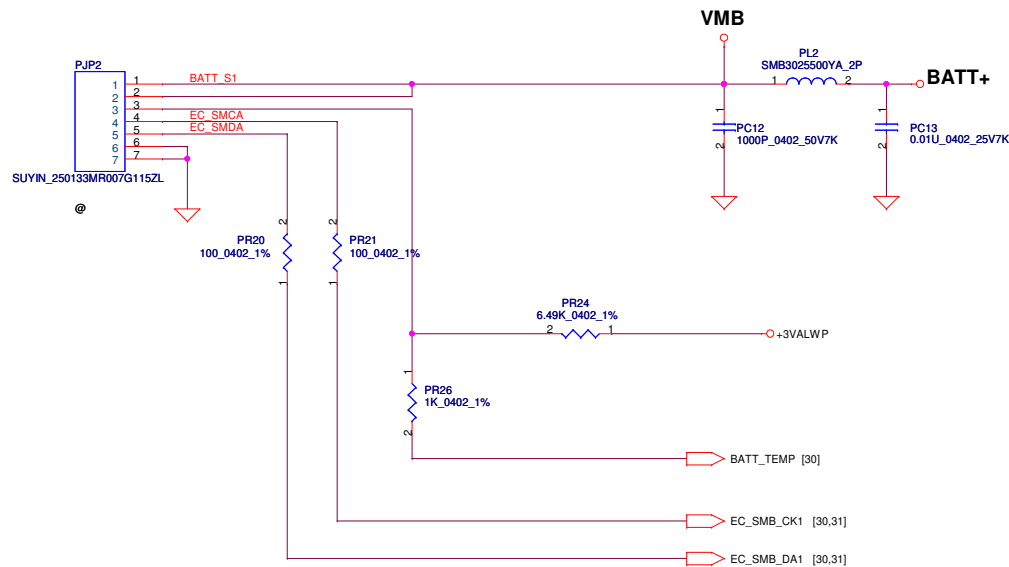
FOR EMI



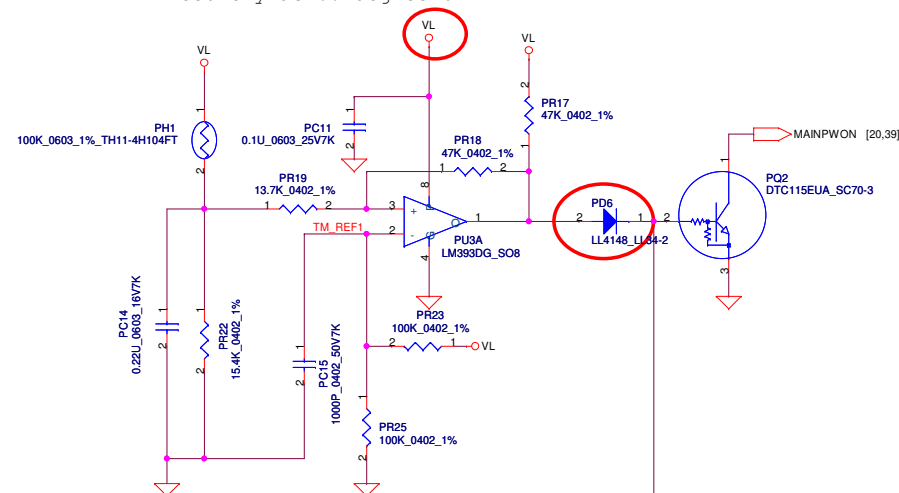
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	
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SINGA 3DC-G756I300

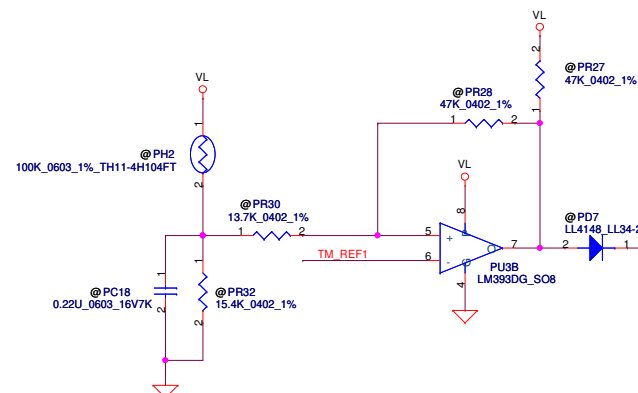
RTC Conn



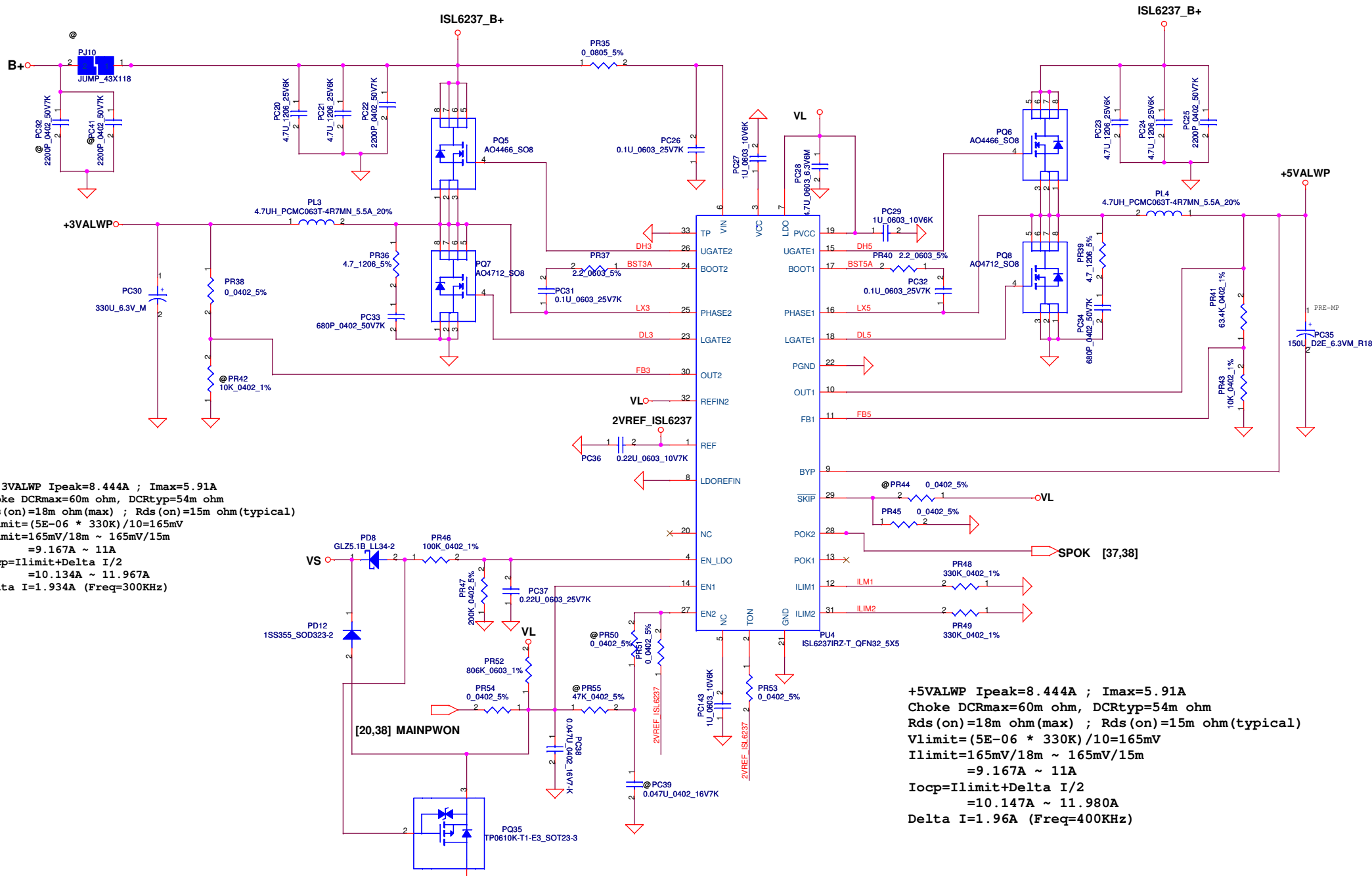
PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



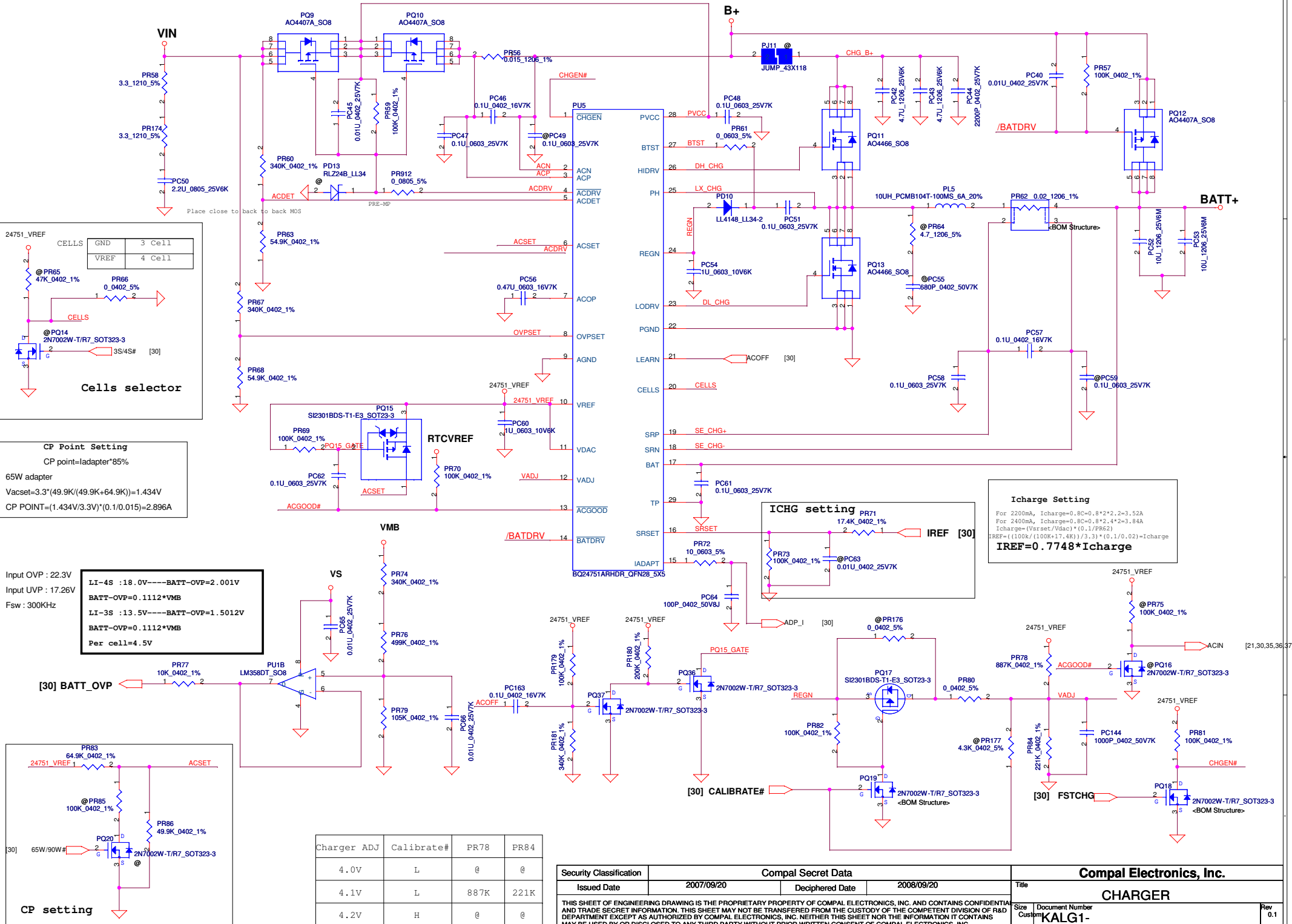
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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title	
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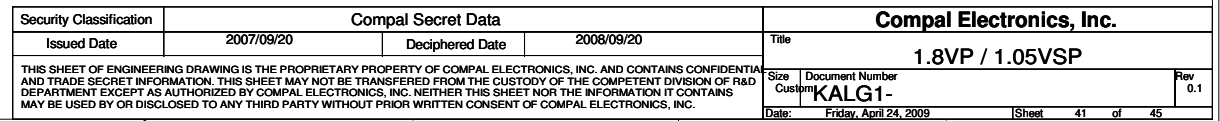


+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
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PCB

ZZZ



LA-5272P MB Rev0: DA60000DW00

PCB 08Y LA-5271P REV1 M/B

North Bridge

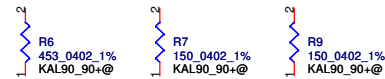
U21



GL40: SA00002Q8N0

S IC AC82GL40 SLGGM A1 FCBGA1329 GL ABO
GL40@

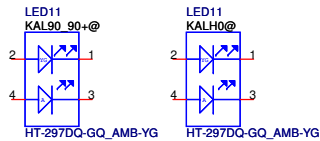
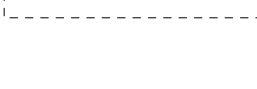
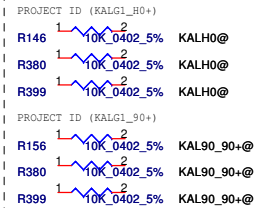
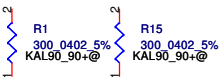
MEDIA_LED NUM_LED CAPS_LED



ON/OFF LED Risiter



Enlightener LED



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